COMPAL CONFIDENTIAL

INTEL SKYLAKE-H PROCESSOR WITH SPT-H_PCH
GPU N16P-Q1-A2

APW5U LA-C401P

2015-11-19 REV 1.0

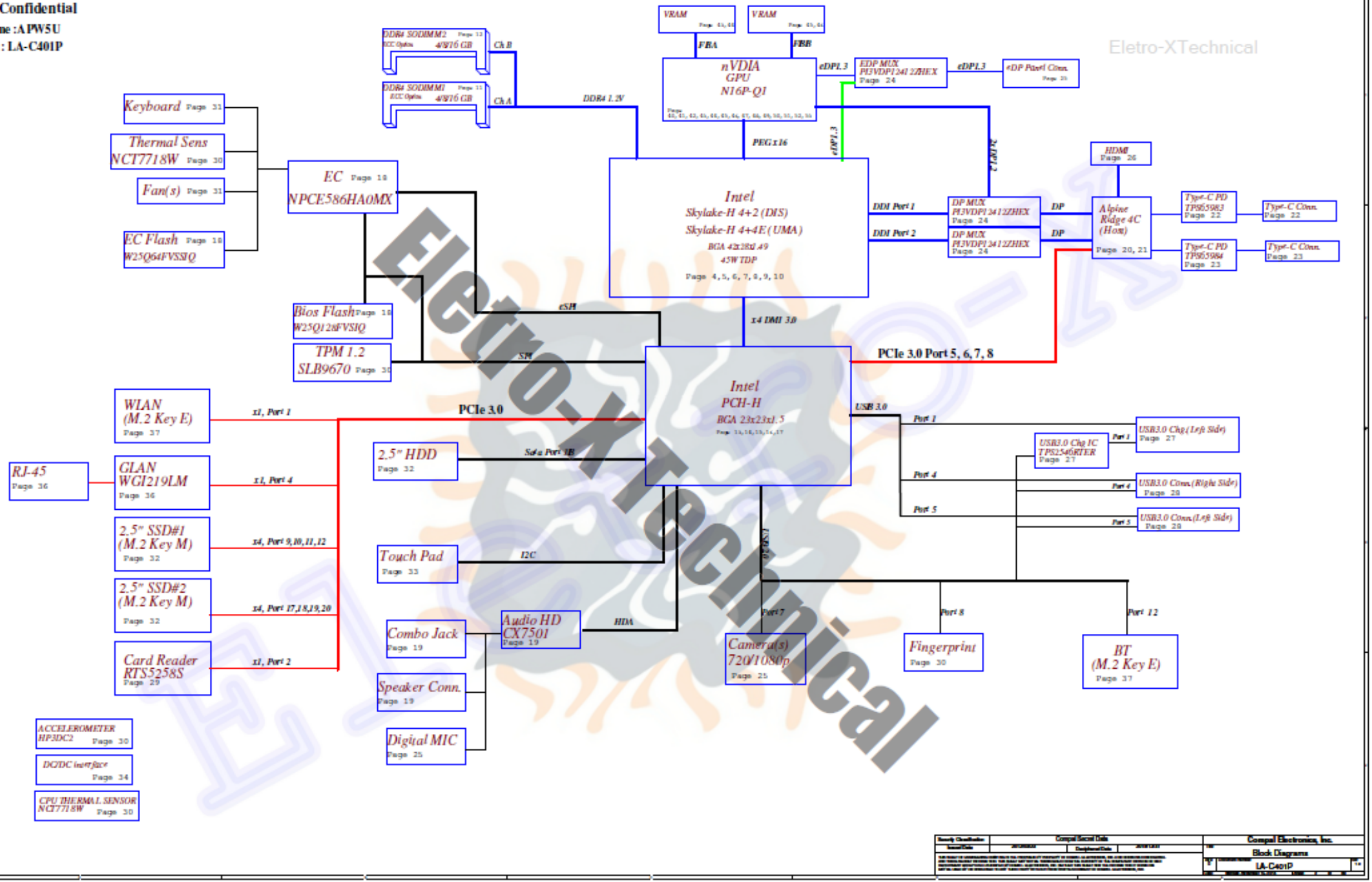
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2015/12/31

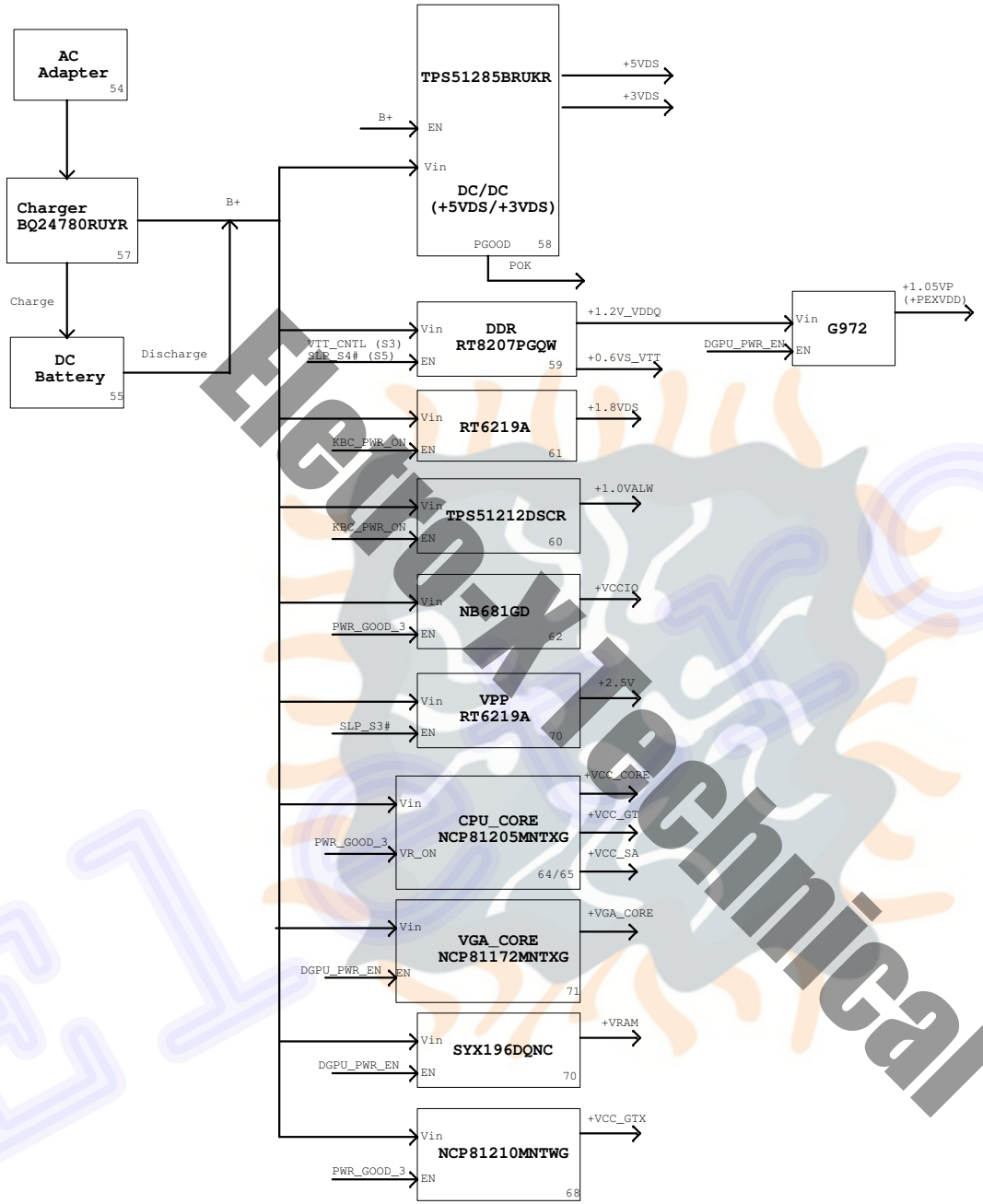
Compal Electronics, Inc.			
Title	Cover Page		
Size: Custom	Document Number: LA-C401P		Rev: 1.0
Date: Thursday, November 19, 2015	Sheet 1 of 58		

Compal Confidential

Model Name :APW5U

File Name : LA-C401P





CPU DC/DC NCP81205MNTXG	
INPUTS	OUTPUTS
B+	+VCC_VORE +VCC_GT +VCC_SA

CPU DC/DC NCP81210MNTWG	
INPUTS	OUTPUTS
B+	+VCC_GTX

VGA DC/DC NCP81172MNTXG	
INPUTS	OUTPUTS
B+	+VGA_CORE

VRAM DC/DC SYX196DQNC	
INPUTS	OUTPUTS
B+	+VRAM

SYSTEM DC/DC TPS51285BRUKR	
INPUTS	OUTPUTS
B+	+3VDS/5VDS

SYSTEM DC/DC RT8207PGQW	
INPUTS	OUTPUTS
B+	+1.2V_VDDQ +0.6VS_VTT

SYSTEM DC/DC RT6219A	
INPUTS	OUTPUTS
B+	+1.8VDS

SYSTEM DC/DC TPS51212DSCR	
INPUTS	OUTPUTS
B+	+1.0VALW

SYSTEM DC/DC NB681GD	
INPUTS	OUTPUTS
B+	+VCCIO

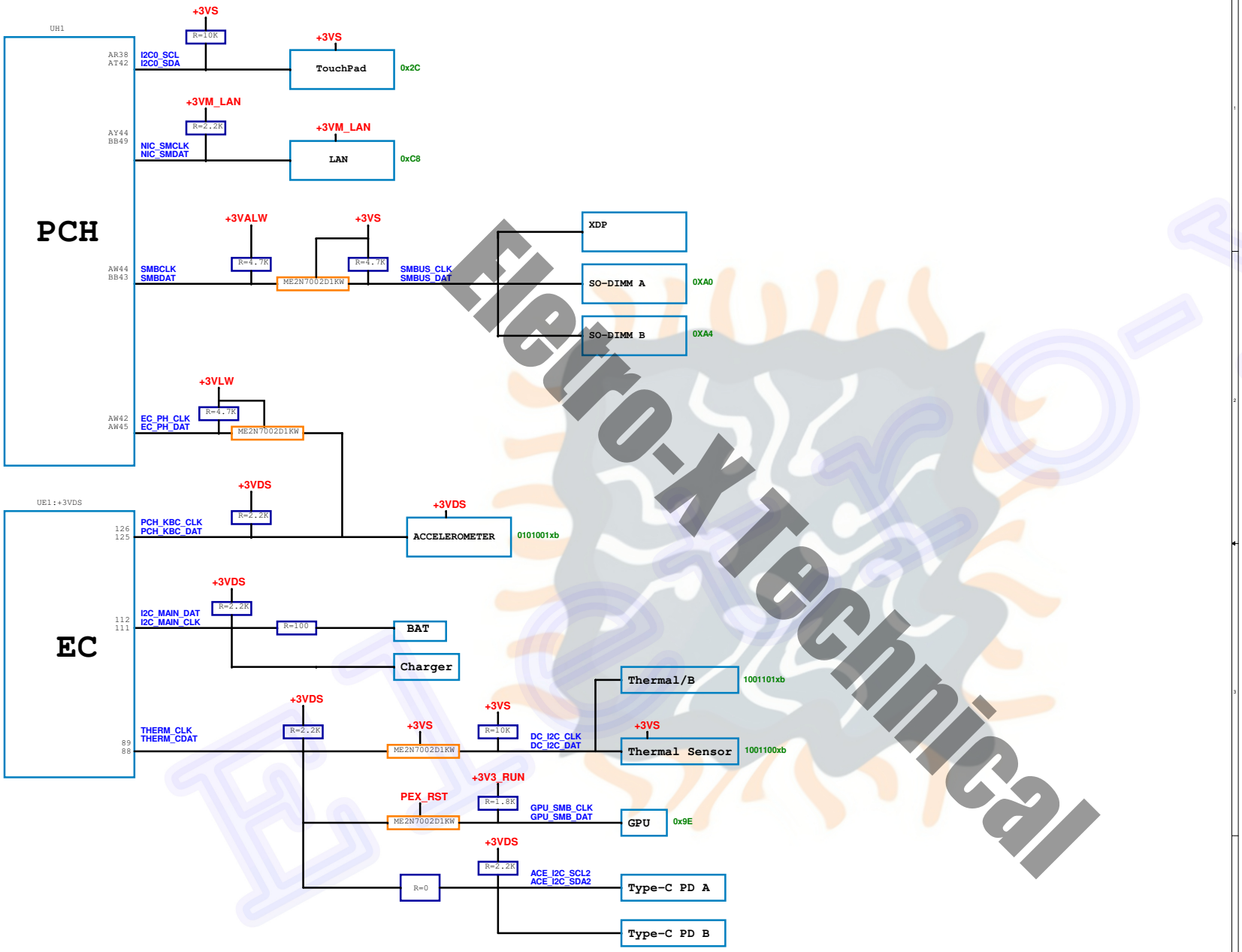
SYSTEM DC/DC RT6219A	
INPUTS	OUTPUTS
B+	+2.5V

CHARGER BQ24780RUYR	
INPUTS	OUTPUTS
VIN BATT	B+

SYSTEM LDO G972	
INPUTS	OUTPUTS
+1.2V_VDDQ	+1.05VP (+PEXVDD)

Switches	
INPUTS	OUTPUTS

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/03	Deciphered Date 2014/12/31	Title: Power Block Diagram
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number LA-8171P Rev 1.0
			Date: Monday, November 16, 2015 Sheet 76 of 89



Security Classification	Compal Secret Data		
Issued Date	2014/02/18	Deciphered Date	2015/02/20

Compal Electronics, Inc.	
Title	SMBus Block Diagram
Size: Custom	Document Number: LA-C401P
Rev	1.0
Date: Monday, November 16, 2015	Sheet 78 of 80

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VDS +3VDS +1.8VALW +1VALW	+1.2V_VDDQ +1.0V_VCCST +2.5V	+5VS +3VS +0.6VS_VTT +VCC_IO +VCC_GTX +VCC_CORE +VCC_GT +VCC_SA	
S0	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC	O	O	O	X	X	
S5 S4/ Battery only	O	O	X	X	X	
S5 S4/AC & Battery don't exist	O	X	X	X	X	

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

CONN@ : means ME part.

Layout Notes

07/24 update

: Question Area Mark.(Wait check)

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

ROYALTY@ : HDMI LOGO means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

EMI@ : means just build for EMI's part

ESD@ : means just build for ESD's part

RF@ : means just build for RF's part

LPC@ : means just build for LPC for EC

ESPI@ : means just build for eSPI for EC

HDD@ : means just build for HDD(option)

SSD@ : means just build for SSD (option)

H42@ : pop on CPU H42 sku only

H44e@ : pop on CPU H44e sku only

DIS@ : pop on DGPU sku only

UMA@ : pop on UMA sku only

DB@ : means just build for Debug port part Remove before MP

SMBUS Control Table

	SOURCE	BATT	Therm Sensor 1001100xb MB side	G-SENSOR 0101001xb	N16P 0x9E	NIC 0xC8	XDP	SODIMM 0XA0 0XA4	TP 0x2C	Therm Sensor 1001101xb DB side
I2C_MAIN_CLK I2C_MAIN_DAT	NPCE586	V	X	X	X	X	X	X	X	X
THERM_CLK THERM_DAT	NPCE586	X	V	X	V	X	X	X	X	V
PCH_KBC_CLK PCH_KBC_DATA	NPCE586	X	X	V	X	X	X	X	X	X
NIC_SMCLK NIC_SMDAT	Skylake	X	X	X	X	V	X	X	X	X
SMBUS_CLK SMBUS_DAT	Skylake	X	X	X	X	X	V	V	X	X
I2C0_SCL I2C0_SDA	Skylake	X	X	X	X	X	X	X	V	X

USB2.0 Port Table

USB2.0 Port	DESTINATION
1	USB2.0 (MB_Charge)
2	X
3	X
4	USB2.0 (MB_Left Side)
5	USB2.0 (MB_Right Side)
6	X
7	Camera
8	Finger printer
9	X
10	X
11	X
12	WLAN/BT
13	X
14	X

CLKOUT_PCIE Port Table

CLKOUT_PCIE	DESTINATION
0	SSD1
1	VGA
2	LAN
3	WLAN
4	Card Reader
5	Thunderbolt
6	SSD2
7	X
8	X
9	X
10	X
11	X
12	X
13	X
14	X
15	X

HSIO Port Table

Lane#	PCIE	SATA	USB3.0	DESTINATION
1			1	USB3.0(Charger)
2			2	X
3			3	X
4			4	USB3.0 (MB_Left Side)
5			5	USB3.0 (MB_Right Side)
6			6	X
7	1		7	WLAN
8	2		8	Card Reader(PCI-E)
9	3		9	X
10	4		10	LAN
11	5			Thunderbolt
12	6			
13	7			
14	8			
15	9	0A		SSD1 (SATA_SSD or PCIEx4 SSD)
16	10	~~1A~~		
17	11			
18	12			
19	13	0B		X
20	14	1B		HDD1
21	15	2		X
22	16	3		X
23	17	4		SSD2 (SATA_SSD or PCIEx4 SSD)
24	18	~~5~~		
25	19			
26	20			

Stapping Options Flash

GPIO 51 Bit 1	GPIO 19 Bit 0	Boot BIOS Destination
0	0	Reserved
0	1	RSVD
1	0	SPI
1	1	LPC

Stapping Options PLT_ID

PLT_ID0	PLT_ID1	PLT_ID2	SKU
0	0	0	
0	0	1	
0	1	0	
0	1	1	17W
1	0	0	
1	0	1	15W
1	1	0	
1	1	1	15U

CFG for AR HDMI SET

TBT_SRC_CFG1	HIGH	HDMI MODE

LPC/ESPI Options Resistor

RH198	RH292	RH263	RH282	RH36	RH275	RH117	RH243	RH165	RH168	LE1	LE2	RE85	RE90	RE113	RE110	RH109	RE112	RE39	RE115	RE114	RE89	MODE
V	X	V	V	V	V	V	V	V	X	V	X	V	V	V	V	X	X	X	X	X	X	LPC
X	V	X	X	X	X	X	X	X	V	X	V	X	X	X	X	V	V	V	V	V	V	ESPI

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date	2015/12/31
Title	Note List		
Size C	Document Number LA-C401P		Rev 1.0
Date: Monday, November 16, 2015	Sheet 3 of 80		

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date 2015/12/31	Title DDRIV

Size Custom	Document Number LA-C401P		Rev 1.0
Date: Monday, November 16, 2015	Sheet 4	of	

Layout Notes:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

PEG_CTX_GRX_P[0..15] → PEG_CTX_GRX_P[0..15] 40
PEG_CTX_GRX_N[0..15] → PEG_CTX_GRX_N[0..15] 40

PEG_CTX_GRX_C_P0	CC2	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_P0
PEG_CTX_GRX_C_N0	CC3	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_N0
PEG_CTX_GRX_C_P1	CC4	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_P1
PEG_CTX_GRX_C_N1	CC5	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_N1
PEG_CTX_GRX_C_P2	CC6	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_P2
PEG_CTX_GRX_C_N2	CC7	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_N2
PEG_CTX_GRX_C_P3	CC8	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_P3
PEG_CTX_GRX_C_N3	CC9	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_N3
PEG_CTX_GRX_C_P4	CC10	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_P4
PEG_CTX_GRX_C_N4	CC11	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_N4
PEG_CTX_GRX_C_P5	CC12	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_P5
PEG_CTX_GRX_C_N5	CC13	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_N5
PEG_CTX_GRX_C_P6	CC14	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_P6
PEG_CTX_GRX_C_N6	CC15	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_N6
PEG_CTX_GRX_C_P7	CC16	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_P7
PEG_CTX_GRX_C_N7	CC17	2	DIS@1	0.22U_0201_6.3V	PEG_CTX_GRX_N7
PEG_CTX_GRX_C_P8	CC18	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_P8
PEG_CTX_GRX_C_N8	CC19	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_N8
PEG_CTX_GRX_C_P9	CC20	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_P9
PEG_CTX_GRX_C_N9	CC21	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_N9
PEG_CTX_GRX_C_P10	CC22	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_P10
PEG_CTX_GRX_C_N10	CC23	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_N10
PEG_CTX_GRX_C_P11	CC24	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_P11
PEG_CTX_GRX_C_N11	CC25	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_N11
PEG_CTX_GRX_C_P12	CC26	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_P12
PEG_CTX_GRX_C_N12	CC27	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_N12
PEG_CTX_GRX_C_P13	CC28	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_P13
PEG_CTX_GRX_C_N13	CC29	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_N13
PEG_CTX_GRX_C_P14	CC30	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_P14
PEG_CTX_GRX_C_N14	CC31	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_N14
PEG_CTX_GRX_C_P15	CC32	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_P15
PEG_CTX_GRX_C_N15	CC33	1	DIS@2	0.22U_0201_6.3V	PEG_CTX_GRX_N15

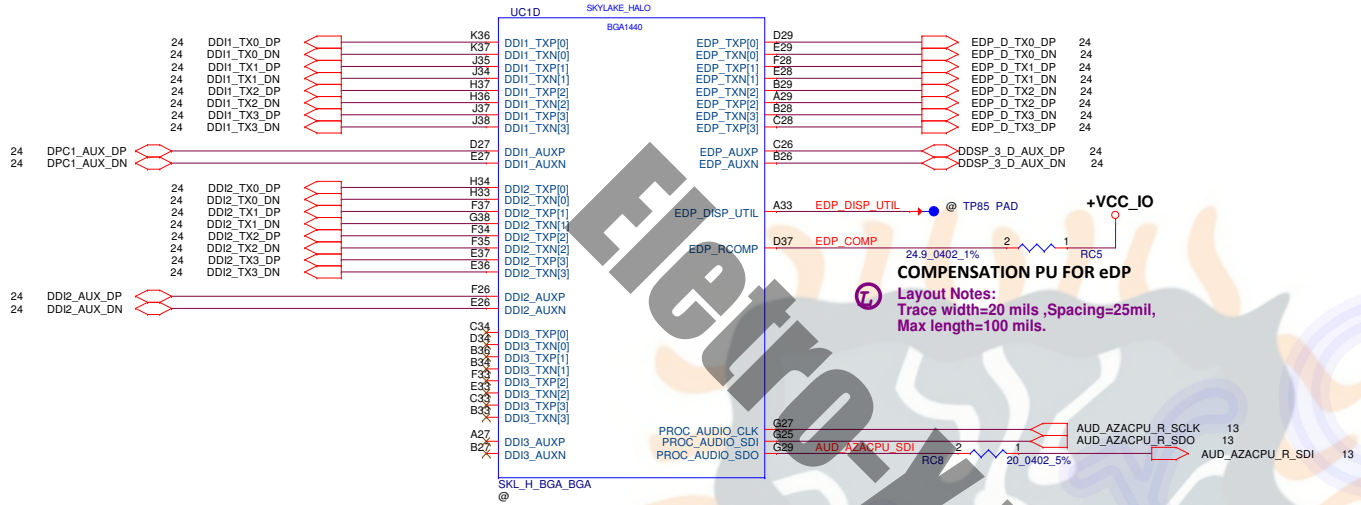
DMI_CTX_PRX_P0 14
DMI_CTX_PRX_N0 14
DMI_CTX_PRX_P1 14
DMI_CTX_PRX_N1 14
DMI_CTX_PRX_P2 14
DMI_CTX_PRX_N2 14
DMI_CTX_PRX_P3 14
DMI_CTX_PRX_N3 14

Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: DMI,PEG

Size: Custom	Document Number: LA-C401P	Rev: 1.0
Date: Monday, November 16, 2015	Sheet 5 of 80	



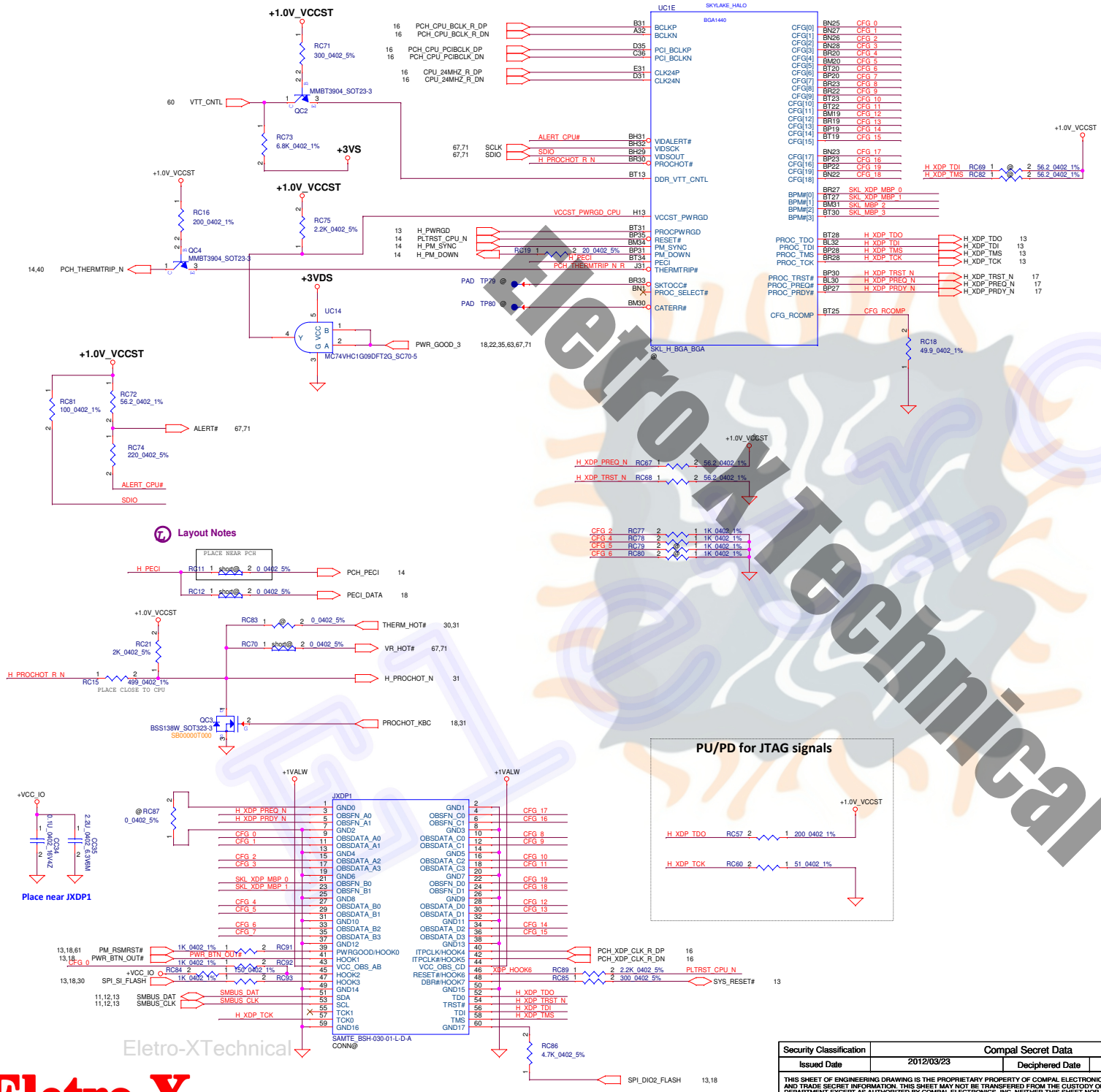
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: CPU-FDI,eDP,DDI

Size: Custom | Document Number: LA-C401P | Rev: 1.0

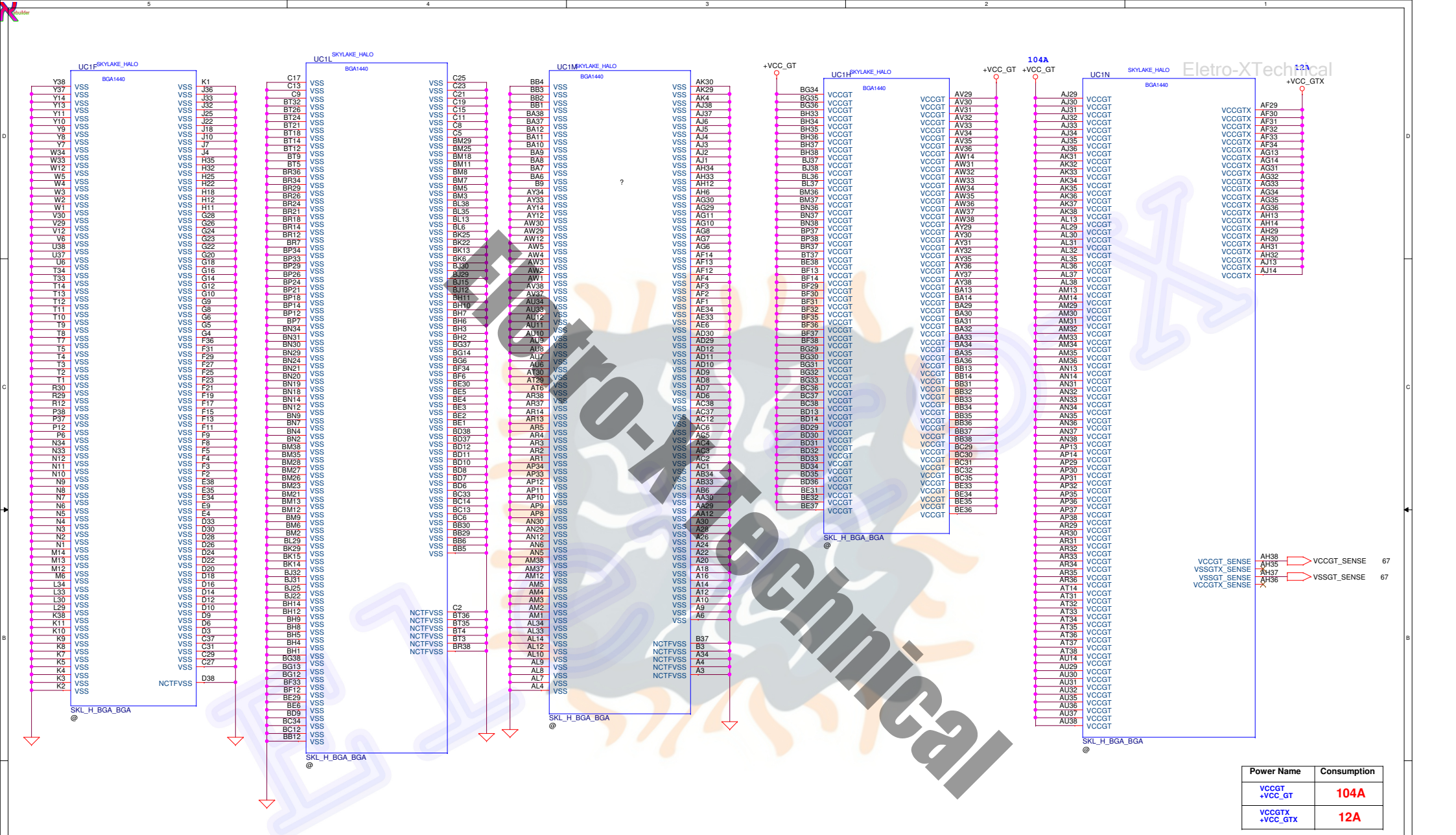
Date: Monday, November 16, 2015 | Sheet 6 of 8



Add 1k PD (open) resistor on the below CFG:
1).CFG[2]:Lanes numbe reversed.
2).CFG[4]:eDP enable.
3).CFG[5]: and [6]
4).CFG[7]

Contiguration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
Intel recommends placing test points on the board for CFG pins.
. CFG[0]:Stall reset sequence after PCU PLL lock until de-asserted:
-1=(Default) Normal Operation; No stall.
-0=Stall.
.CFG[1]:Reserved configuration lane.
.CFG[2]:PCI Express*Static x16 Lane Numbering Reversal.
-1=Normal operation
-0=Lane numbers reversed.
.CFG[3]:Reserved configuration lane.
.CFG[4]:eDP enable:
-1=Disabled.
-0=Enabled.
.CFG[6:5]:PCI Express* Bifurcation
-00=1x8,2x4 PCI Express*
-01=reserved
-10=2x8 PCI Express*
-11=1x16 PCI Express*
.CFG[7]:PEG Training:
-1=(default) PEG Train immediately following RESET# de assertion.
-0=PEG Wait for BIOS for assertion.
.CFG[19:8]:Reserved configuration lanes.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date	2015/12/31
Title	CPU-RSVD,CFG		
Size C	Document Number LA-C401P		Rev 1.0
Date: Monday, November 16, 2015	Sheet 7 of 80		



Power Name	Consumption
VCCGT +VCC_GT	104A
VCCGTX +VCC_GTX	12A

Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: CPU-VSS\VCCGT

Size: Custom | Document Number: LA-C401P

Date: Monday, November 16, 2015 | Sheet 8 of 8

4+2 CPU R1

UC1 SR2FQ@

CL8066202194635 SR2FQ R0 2.6G

SA000095Z30

UC1 SR2FU@

CL8066202194731 SR2FU R0 2.7G

SA000095X20

UC1 SR2FN@

CL8066202191415 SR2FN R0 2.8G

SA000095V20

4+4 CPU

UC1 QJR9@

JQ8066202598702 QJR9 M0 1.6G

SA000097C00

4+2 CPU R3

UC1 @

CL8066202194635 SR2FQ R0 2.6G A32!

SA000095Z40

UC1 @

CL8066202194731 SR2FU R0 2.7G A32!

SA000095X30

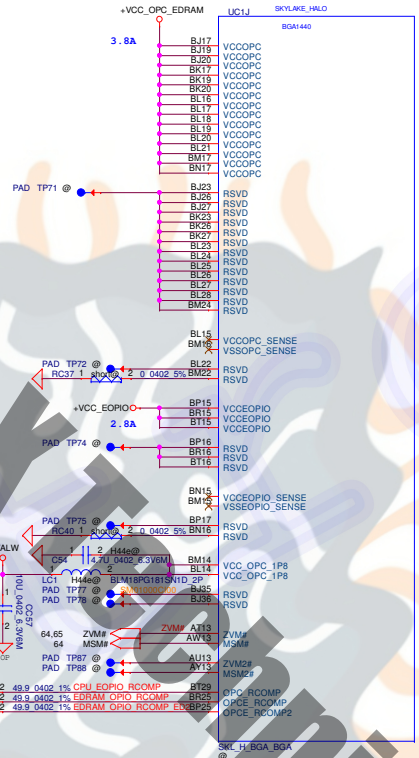
UC1 @

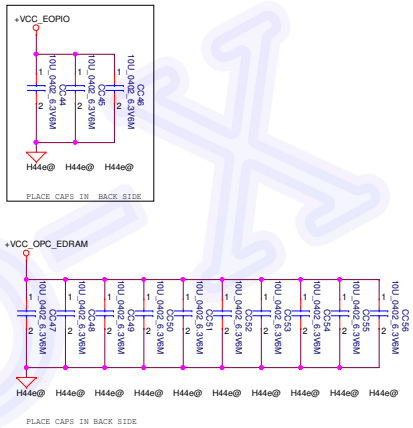
CL8066202191415 SR2FN R0 2.8G A32!

SA000095V10

4+4 CPU

Power Name	Consumption
VCCOPC +VCC_OPC_EDRAM	3.8A
VCCEOPIO +VCC_OPC_EDRAM	2.8A
VCC_OPC_1P8 +1.8VALW	50mA





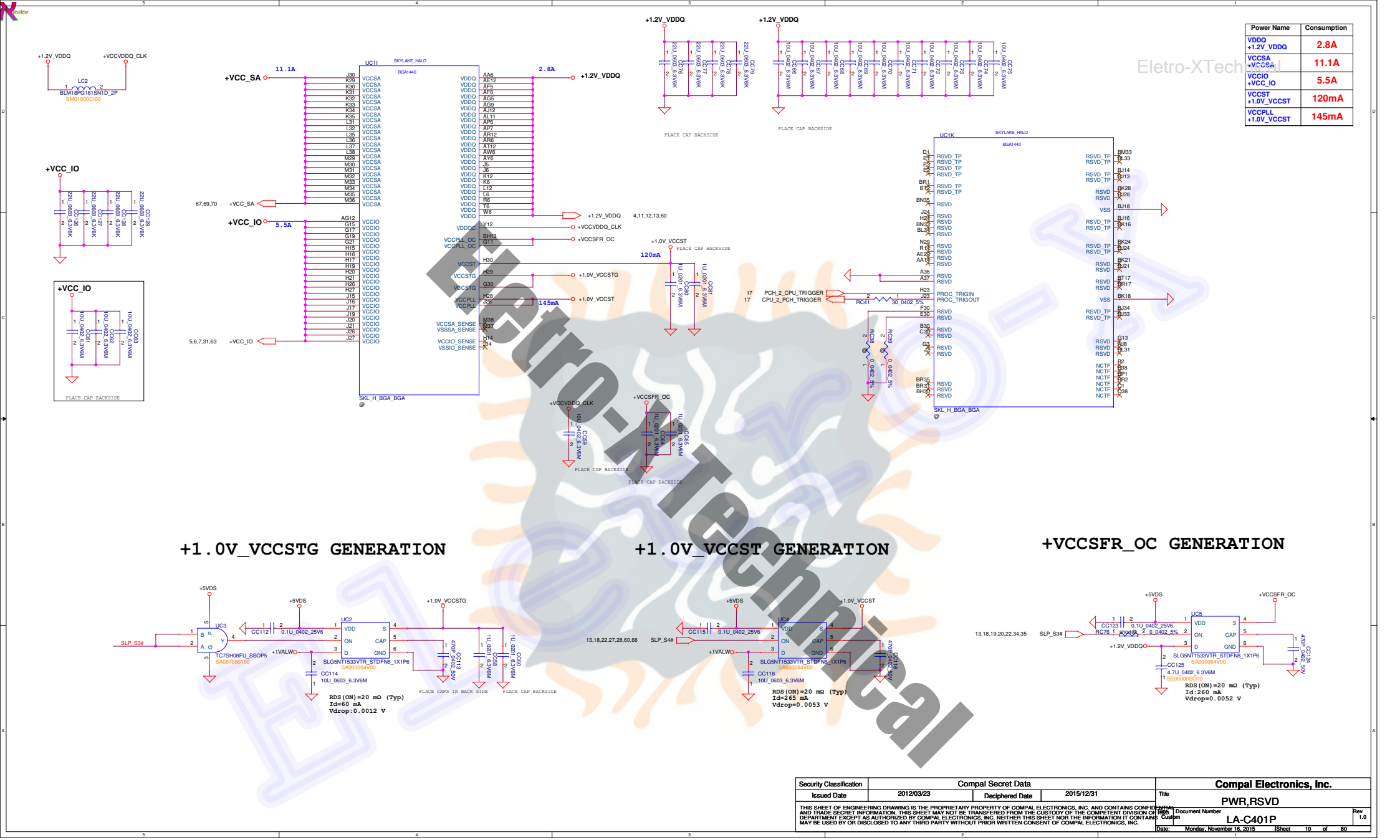
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: VCC,RSVD

Size: Custom | Document Number: LA-C401P | Rev: 1.0

Date: Monday, November 16, 2015 | Sheet 9 of 80



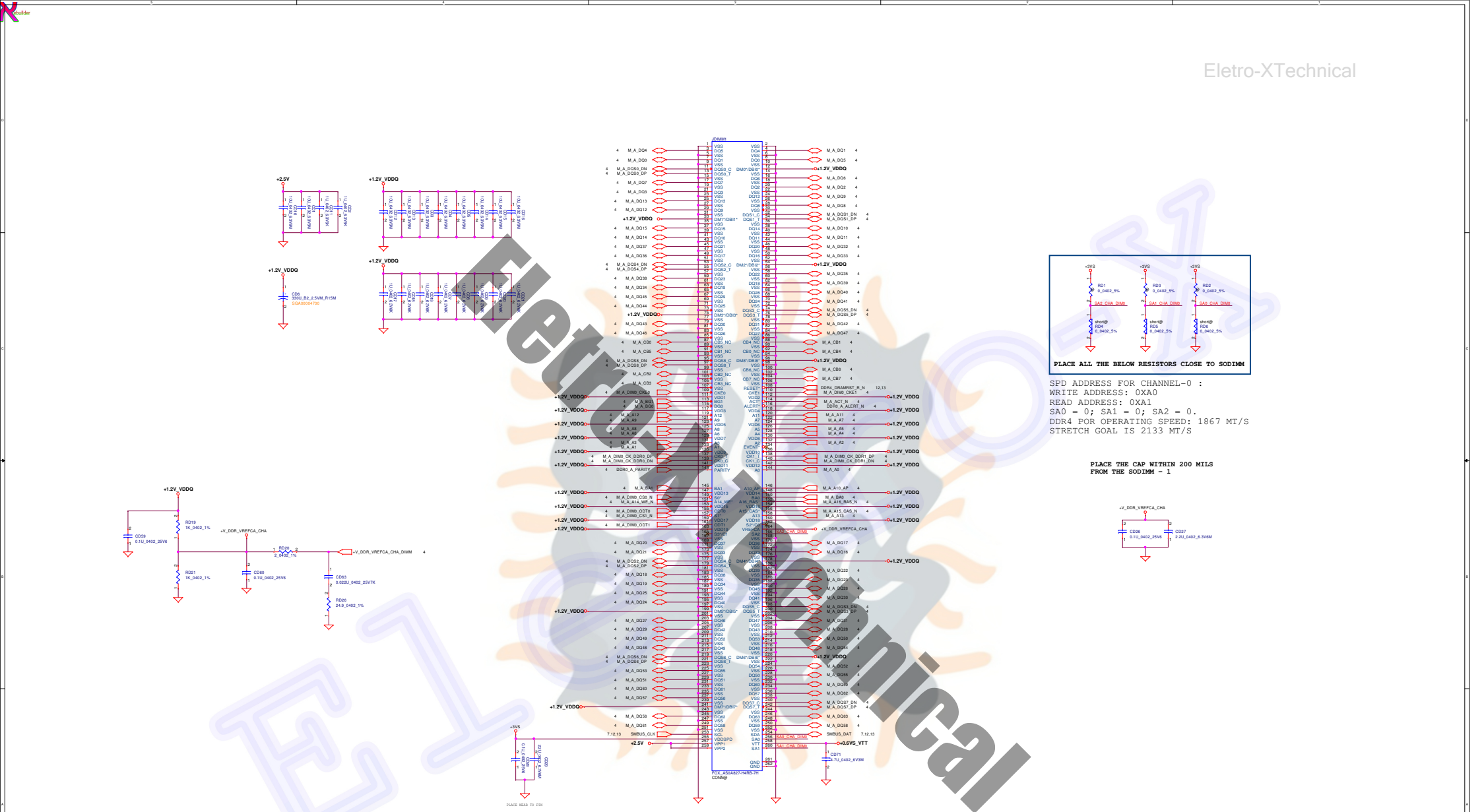
+1.0V_VCCSTG GENERATION

+1.0V_VCCST GENERATION

+VCCSFR_OC GENERATION

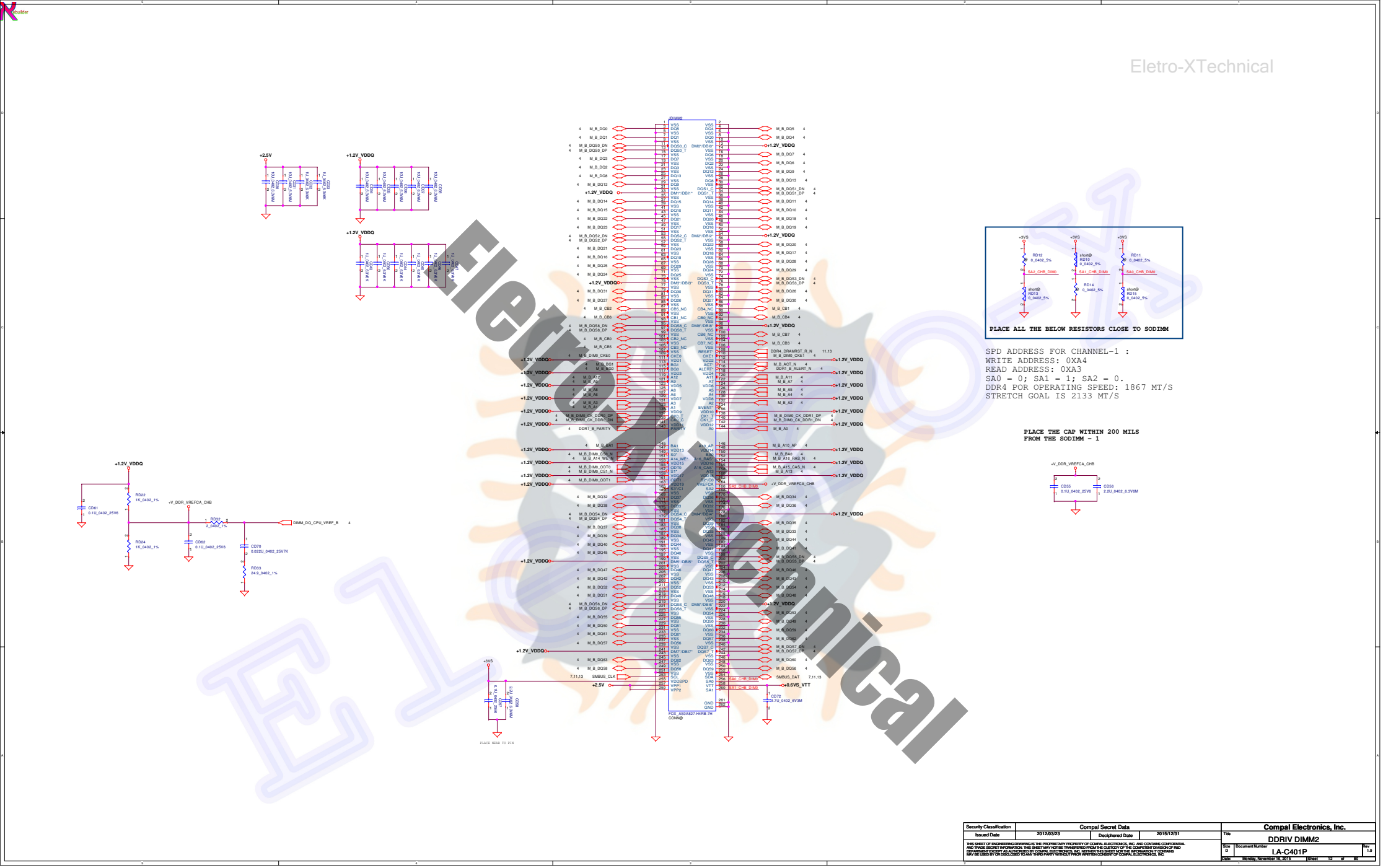
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2015/12/31

Compal Electronics, Inc.	
Title	PWR,RSVD
Size: B	Document Number: LA-C401P
Custom	Rev: 1.0
Date: Monday, November 16, 2015	Sheet 10 of 80



SPD ADDRESS FOR CHANNEL-0 :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date	2015/12/31
Title	DDRIV DIMM1		
Size D	Document Number LA-C401P		Rev 1.0
Date: Monday, November 16, 2015	Sheet 11 of 80		



PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL-1 :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

PLACE THE CAP WITHIN 200 MILS
FROM THE SODIMM - 1

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date	2015/12/31
Title	DDRIV DIMM2		
Size D	Document Number LA-C401P		Rev 1.0
Date: Monday, November 16, 2015	Sheet 12 of 60		

ME Debug Port

UH1 SR2CE@
GLCM236 SR2CE D1 FCBGA PCH-H
SA000096020
4+2 PCH R1

UH1 QJGE@
GLSSKU QJGE D1 FCBGA 837P PCH-H
SA00008RM50
4+4 PCH

UH1 @
GLCM236 SR2CE D1 FCBGA PCH-H A32!
SA000096010
4+2 PCH R3
4+4 PCH

Pinout on customer's board, as in the PDG, CDI #546884

Pin		Pin	
1	VccSus3_3	10	GND
2	SLP_S3#	11	PWRBTN#
3	VccDSW3_3	12	GND
4	SLP_S5#	13	SYS_RESET#
5	SLP_S4#	14	GND
6	SLP_A#	15	SLP_S0#
7	+3.3DS	16	NC
8	GND	17	NC
9	RTCRST#	14	NC

JME1
E-T_6718K-Y18N-21L
CONN@

Layout note:
RH336 close to UH1

GPP_B14	Func.
HIGH(1)	Enable "Top Swap"
LOW(0)	Disable "Top Swap"

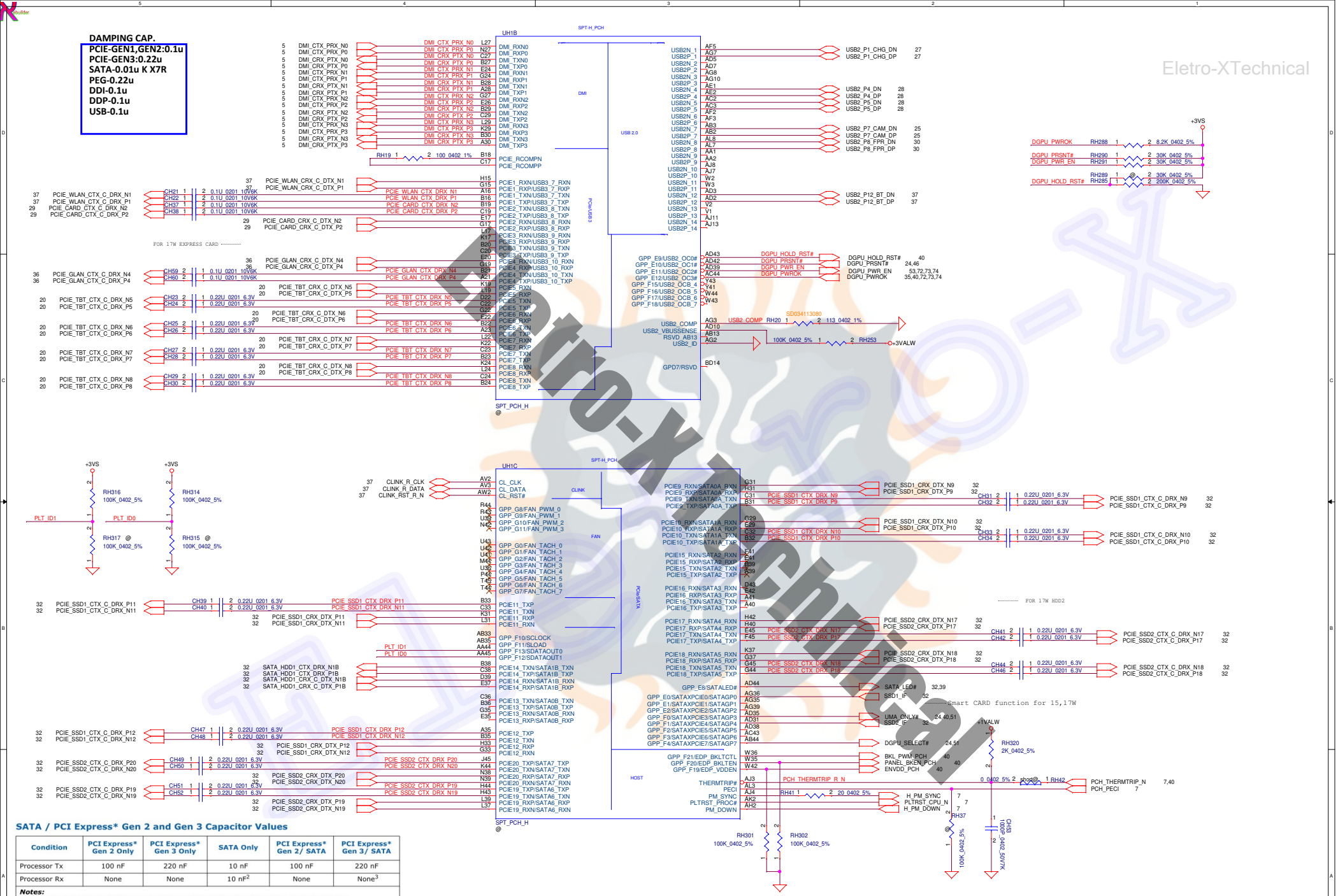
GPP_C2	Func.
HIGH	Enable Intel ME
LOW	Disable Intel ME

GPP_C5	Func.
HIGH	eSPI for EC
LOW	LPC for EC

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date	2015/12/31
Title	PCH-SPI		
Size C	Document Number LA-C401P		Rev 1.0
Date: Monday, November 16, 2015	Sheet 13 of 80		

DAMPING CAP.

PCIE-GEN1,GEN2:0.1u
PCIE-GEN3:0.22u
SATA-0.01u K X7R
PEG-0.22u
DDI-0.1u
DDP-0.1u
USB-0.1u



SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.

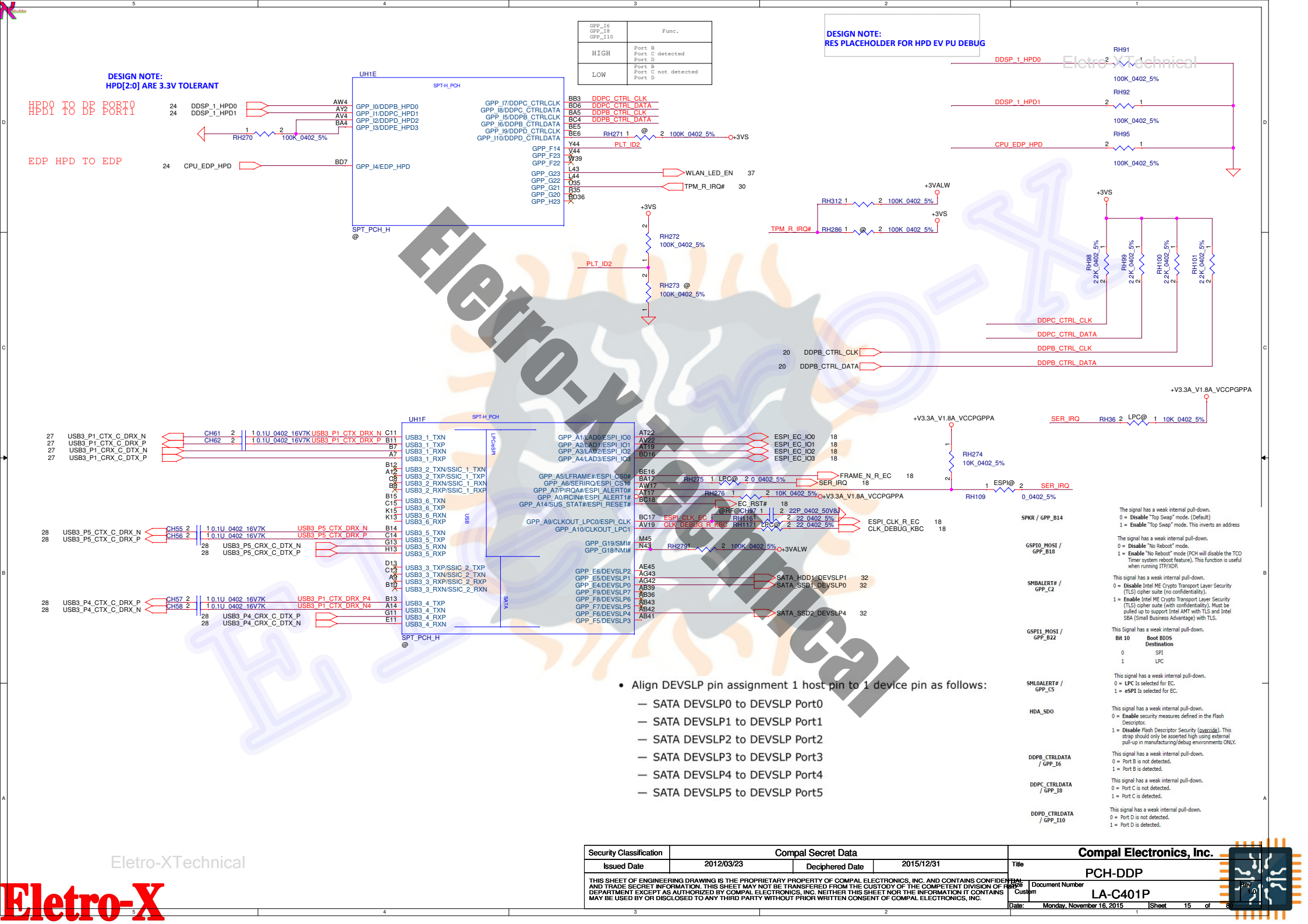
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: PCH-PCIE/DMI/USB

Size	Document Number	Rev
C	LA-C401P	1.0

Date: Monday, November 16, 2015 | Sheet 14 of 80



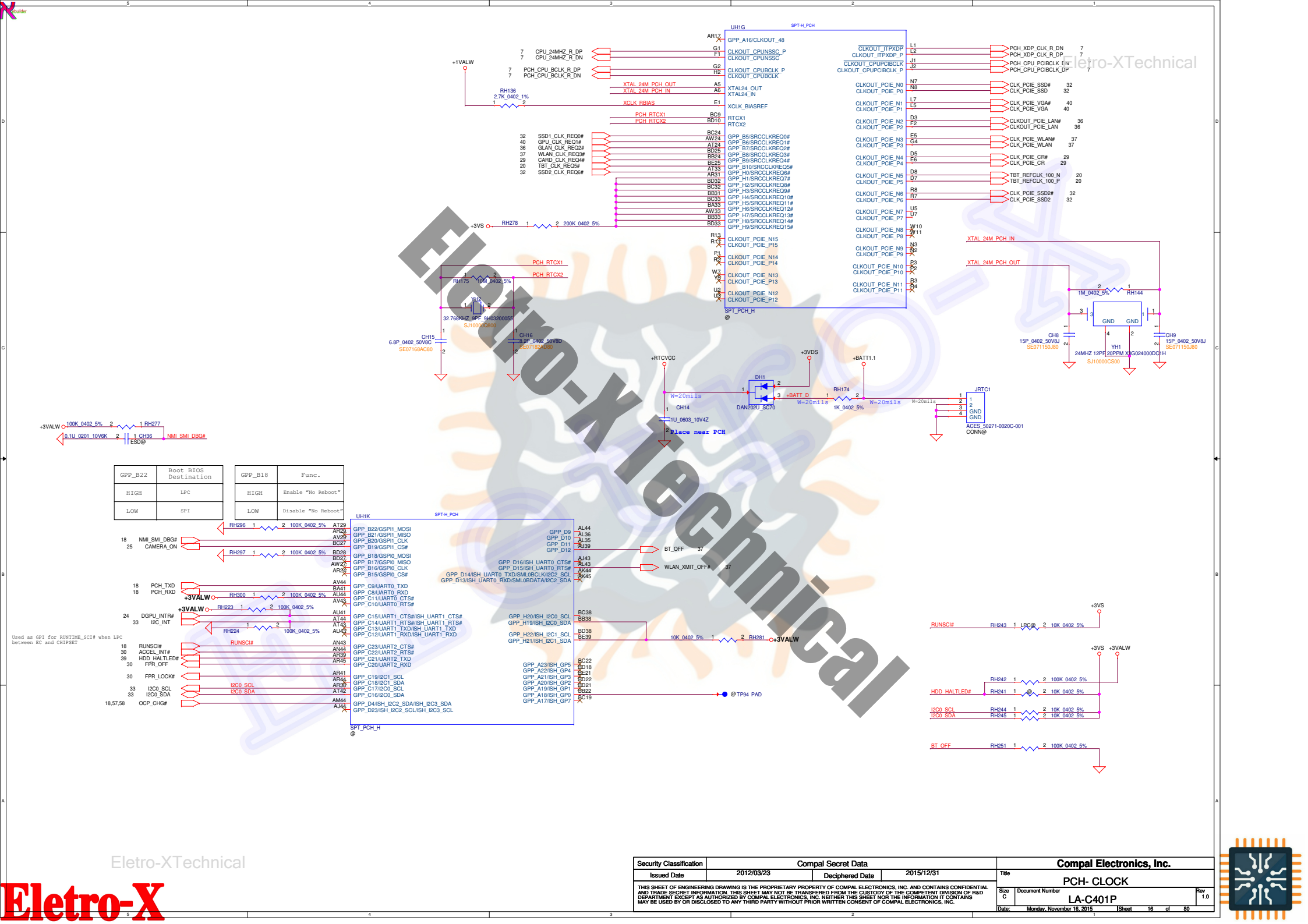
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: PCH-DDP

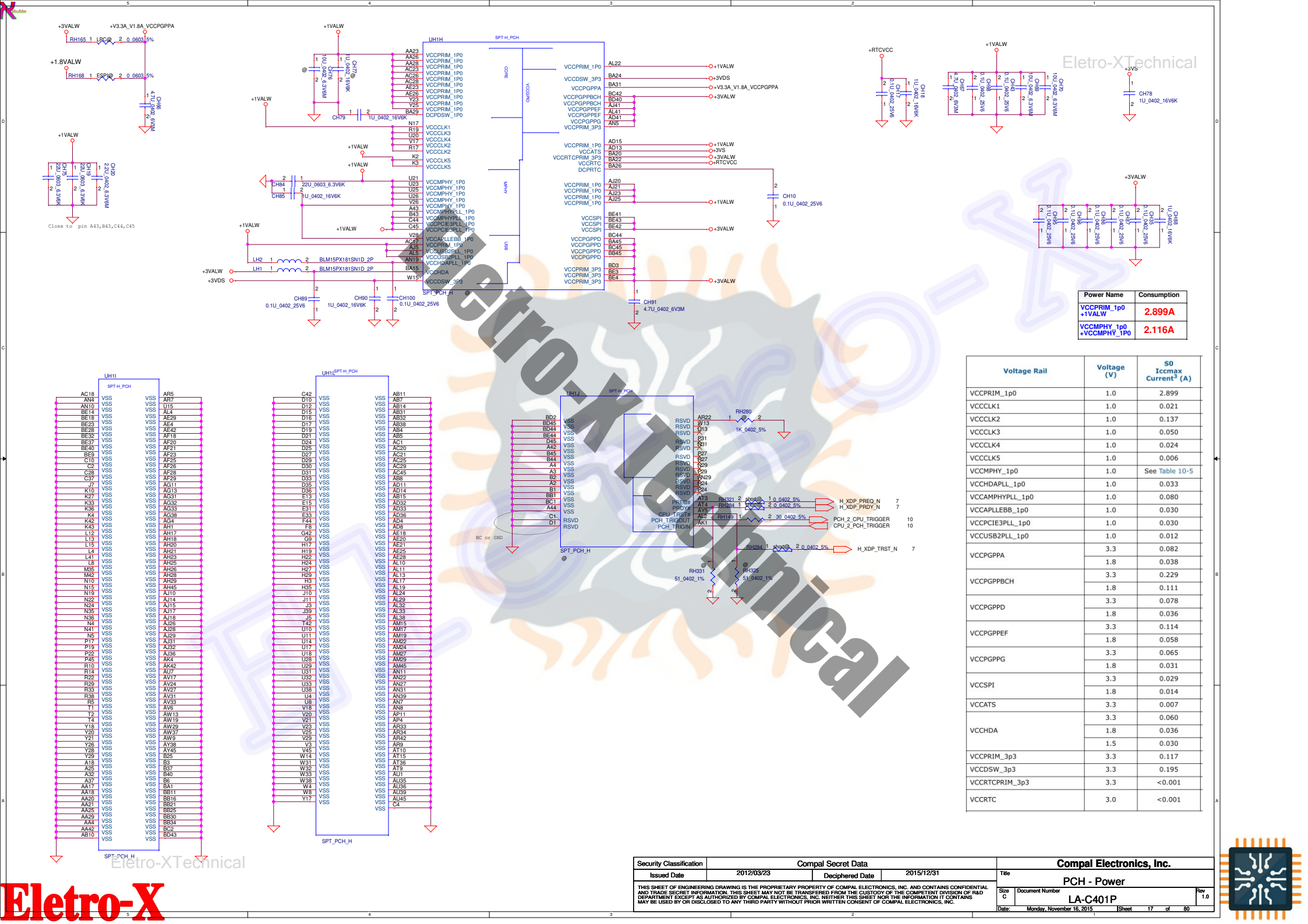
Size: Custom | Document Number: LA-C401P | Rev: 1.0

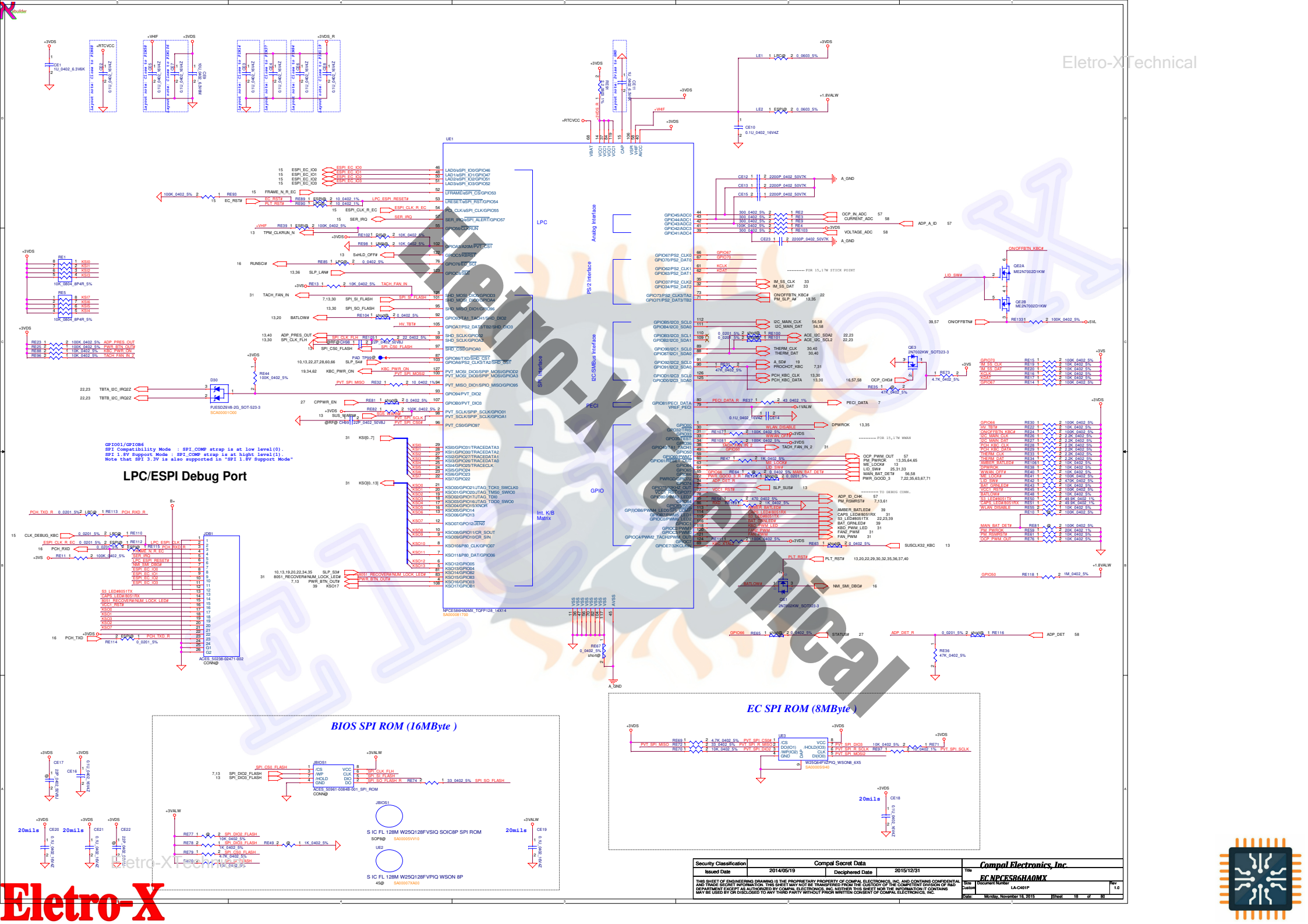
Date: Monday, November 16, 2015 | Sheet 15 of 80

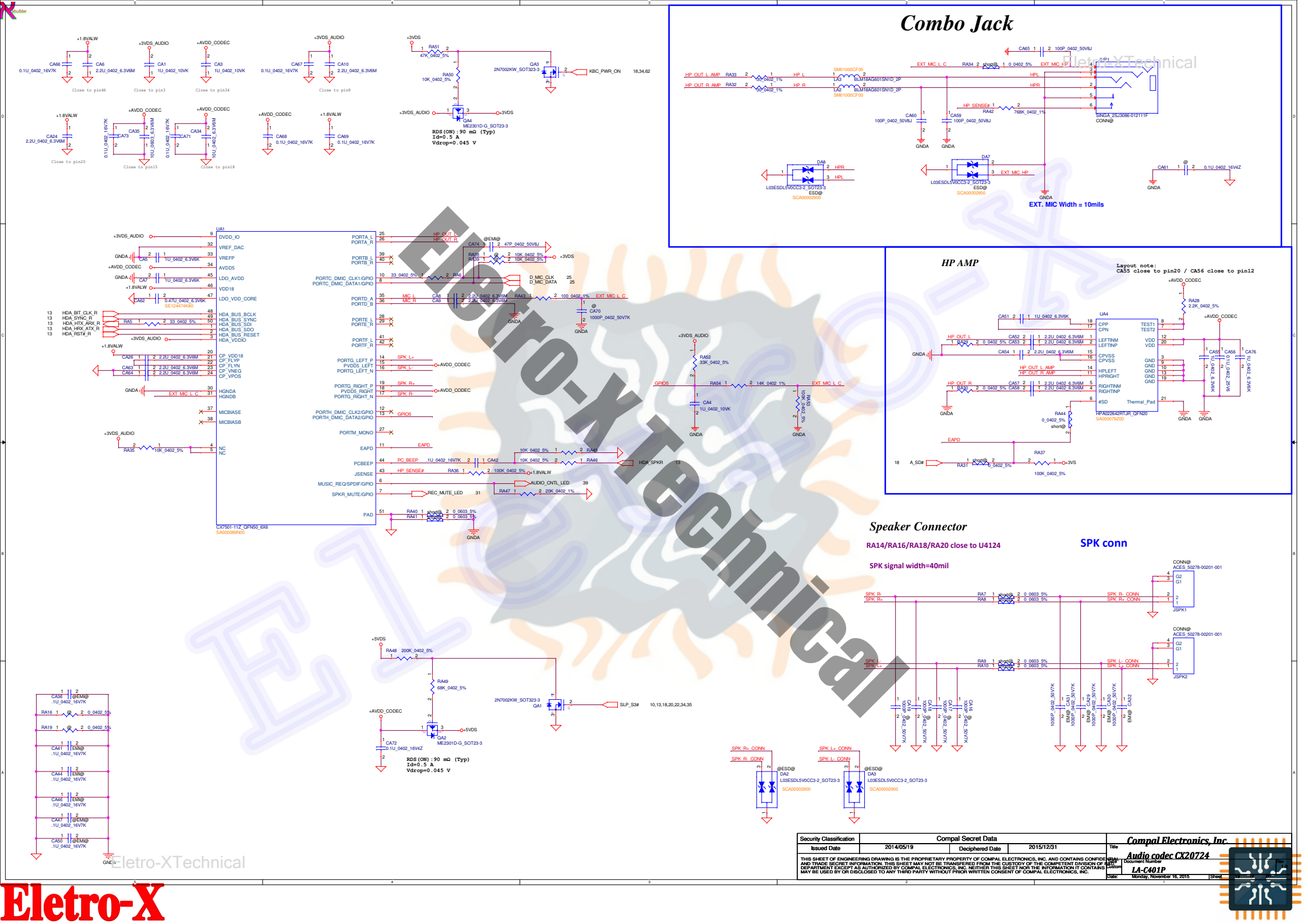


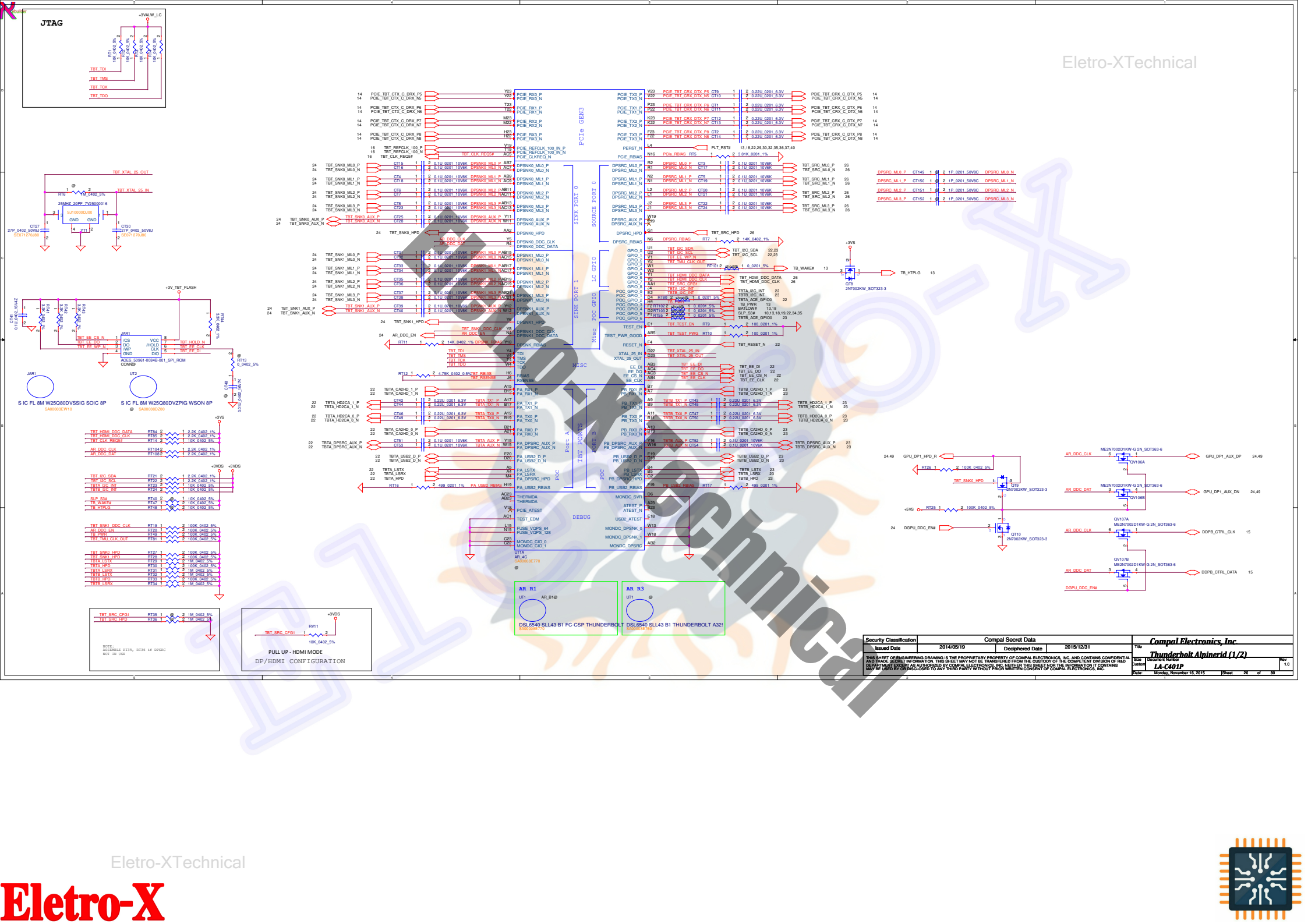
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date	2015/12/31

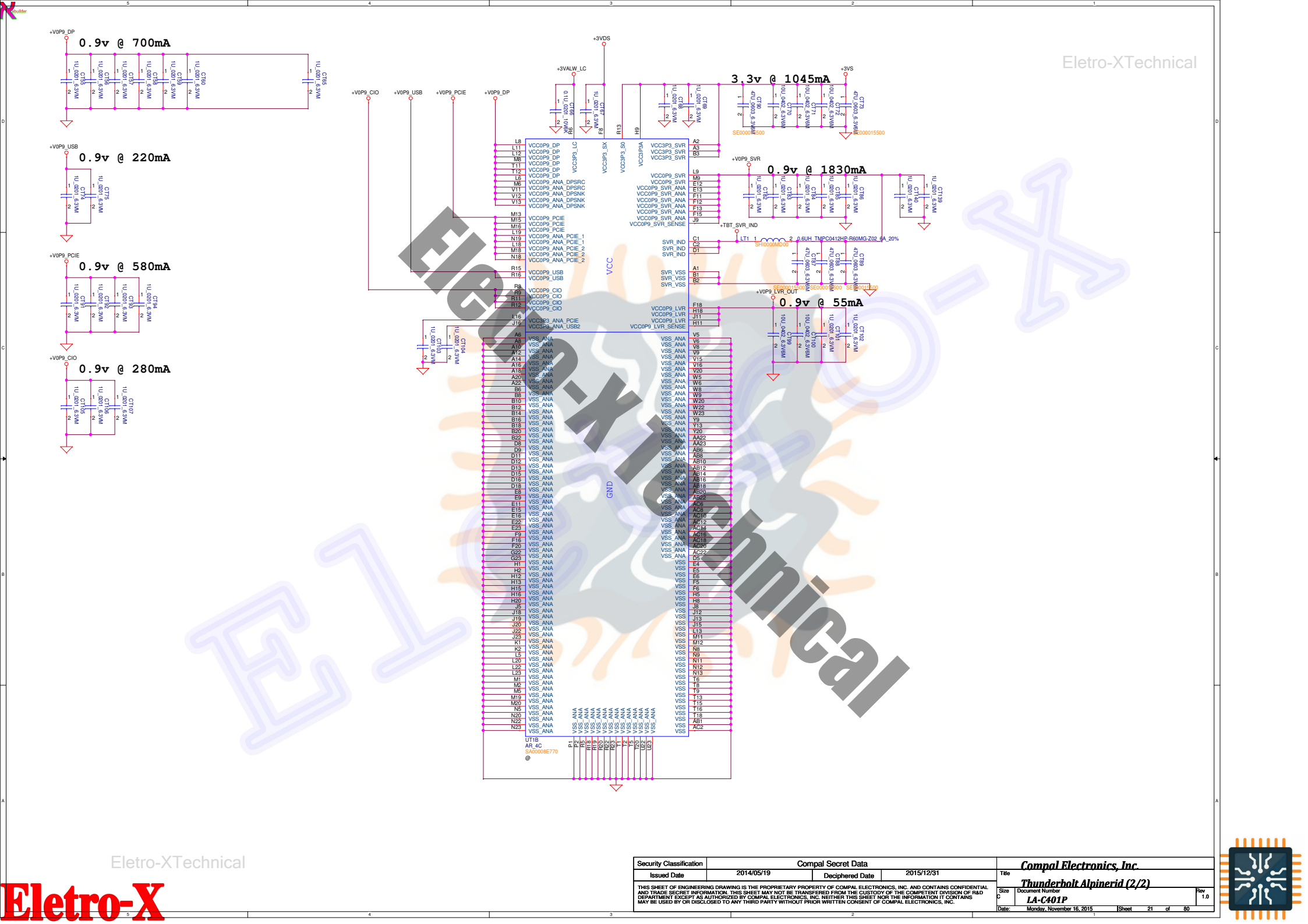
Title	PCH- CLOCK		
Size C	Document Number LA-C401P		Rev 1.0
Date: Monday, November 16, 2015	Sheet 16 of 80		


+3VALW
+V3.3A_V1.8A_VCCPGPPA
+1.8VALW
+1VALW
UH1H
SPT-H_PCH
VCCPRIM_1P0
VCCDSW_3P3
VCCPGPPA
VCCPGPPBCH
VCCPGPPBCH
VCCPGPPEF
VCCPGPPEF
VCCPGPPG
VCCPRIM_3P3
VCCCLK1
VCCCLK3
VCCCLK4
VCCCLK2
VCCCLK5
VCCCLK5
VCCMPHY_1P0
VCCMPHYPLL_1P0
VCCPCIE3PLL_1P0
VCCAPLLEBB_1P0
VCCUSB2PLL_1P0
VCCHDAPLL_1P0
VCCHDA
VCCDSW_3P3
VCCRTCPRIM_3P3
VCCRTC
DCPRTC
VCCSPI
VCCSPI
VCCSPI
VCCPGPPD
VCCPGPPD
VCCPGPPD
VCCPGPPD
VCCPRIM_3P3
VCCPRIM_3P3
VCCPRIM_3P3
+3VDS
+3VS
+RTCVCC
+3VALW
Close to pin A43,B43,C44,C45
Eletro-XTechnical
Power Name
Consumption
VCCPRIM_1p0 +1VALW
2.899A
VCCMPHY_1p0 +VCCMPHY_1P0
2.116A
Voltage Rail
Voltage (V)
S0 Iccmax Current[3] (A)
VCCPRIM_1p0
1.0
2.899
VCCCLK1
1.0
0.021
VCCCLK2
1.0
0.137
VCCCLK3
1.0
0.050
VCCCLK4
1.0
0.024
VCCCLK5
1.0
0.006
VCCMPHY_1p0
1.0
See Table 10-5
VCCHDAPLL_1p0
1.0
0.033
VCCAMPHYPLL_1p0
1.0
0.080
VCCAPLLEBB_1p0
1.0
0.030
VCCPCIE3PLL_1p0
1.0
0.030
VCCUSB2PLL_1p0
1.0
0.012
VCCPGPPA
3.3
0.082
1.8
0.038
VCCPGPPBCH
3.3
0.229
1.8
0.111
VCCPGPPD
3.3
0.078
1.8
0.036
VCCPGPPEF
3.3
0.114
1.8
0.058
VCCPGPPG
3.3
0.065
1.8
0.031
VCCSPI
3.3
0.029
1.8
0.014
VCCATS
3.3
0.007
VCCHDA
3.3
0.060
1.8
0.036
1.5
0.030
VCCPRIM_3p3
3.3
0.117
VCCDSW_3p3
3.3
0.195
VCCRTCPRIM_3p3
3.3
<0.001
VCCRTC
3.0
<0.001
UH1I
UH1L
UH1J
SPT_PCH_H
H_XDP_PREQ_N
H_XDP_PRDY_N
PCH_2_CPU_TRIGGER
CPU_2_PCH_TRIGGER
H_XDP_TRST_N
Security Classification
Compal Secret Data
Issued Date
2012/03/23
Deciphered Date
2015/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
PCH - Power
Size
C
Document Number
LA-C401P
Rev
1.0
Date:
Monday, November 16, 2015
Sheet
17
of
80




Combo Jack
HP AMP
Layout note:
CA55 close to pin20 / CA56 close to pin12
EXT. MIC Width = 10mils
Speaker Connector
RA14/RA16/RA18/RA20 close to U4124
SPK conn
SPK signal width=40mil
RDS(ON):90 mΩ (Typ)
Id=0.5 A
Vdrop=0.045 V
CX7501-11Z_QFN50_6X6
HPA00262421RJR_QFN20
Eletro-XTechnical
Eletro-X
Compal Secret Data
2014/05/19
2015/12/31
Compal Electronics, Inc.
Audio codec CX20724
LA-C401P
Monday, November 16, 2015



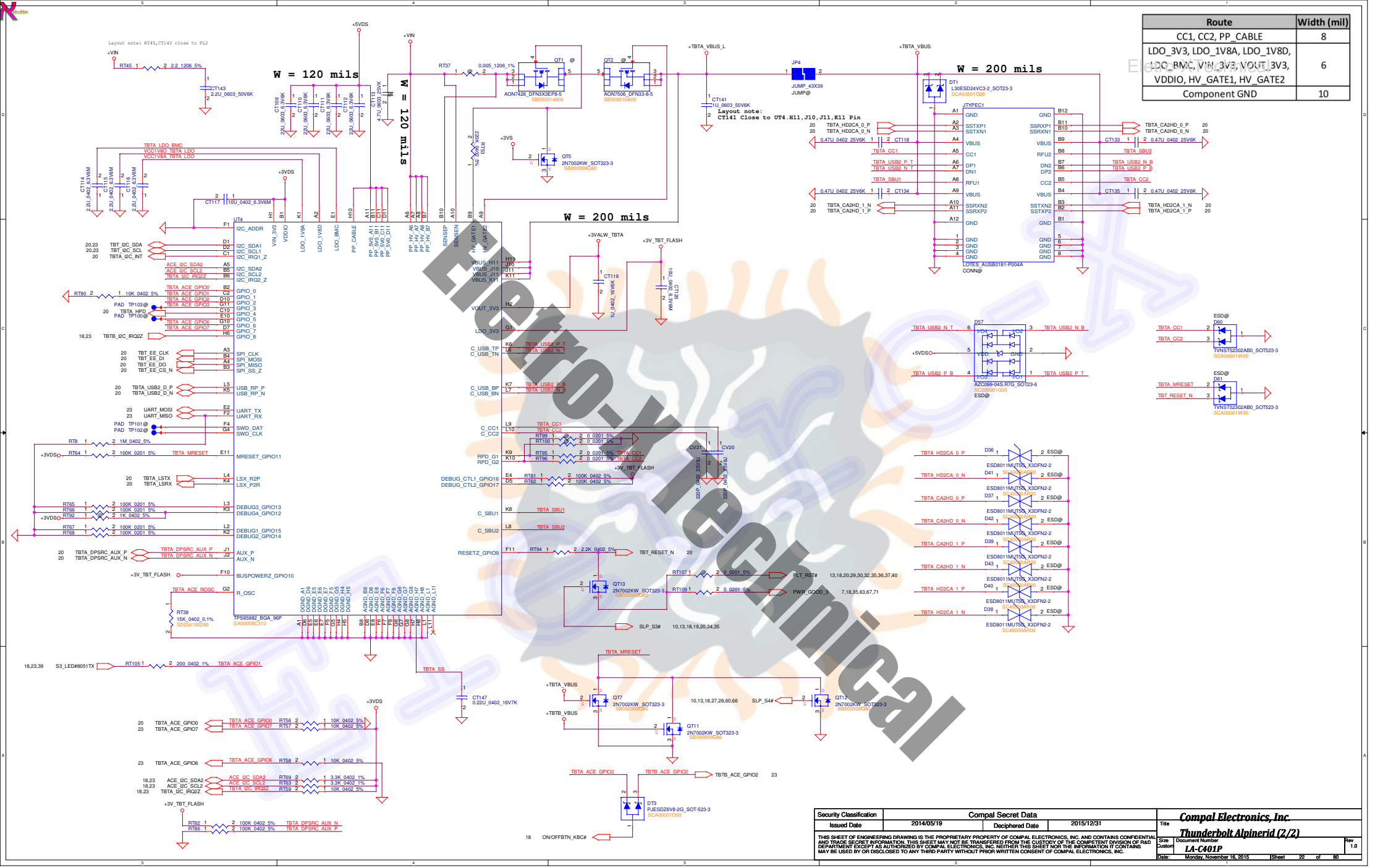


Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.			
Title: Thunderbolt Alpinerid (2/2)			
Size: C	Document Number: LA-C401P		Rev: 1.0
Date: Monday, November 16, 2015	Sheet 21 of 80		

Route	Width (mil)
CC1, CC2, PP_CABLE	8
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Component GND	10



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: Thunderbolt Alpinerid (2/2)

Size: Custom | Document Number: LA-C401P | Rev: 1.0

Date: Monday, November 16, 2015 | Sheet 22 of 80

Route	Width (mil)
CC1, CC2, PP_CABLE	8
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Component GND	10

W = 120 mils

W = 120 mils

W = 200 mils

W = 200 mils

CT142 1U_0603_50V6K
Layout note:
CT142 Close to UT6.H11,J10,J11,K11 Pin

Security Classification	Compal Secret Data
Issued Date	2014/05/19
Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: TBT PORTA

Size: Custom | Document Number: LA-C401P | Rev: 1.0

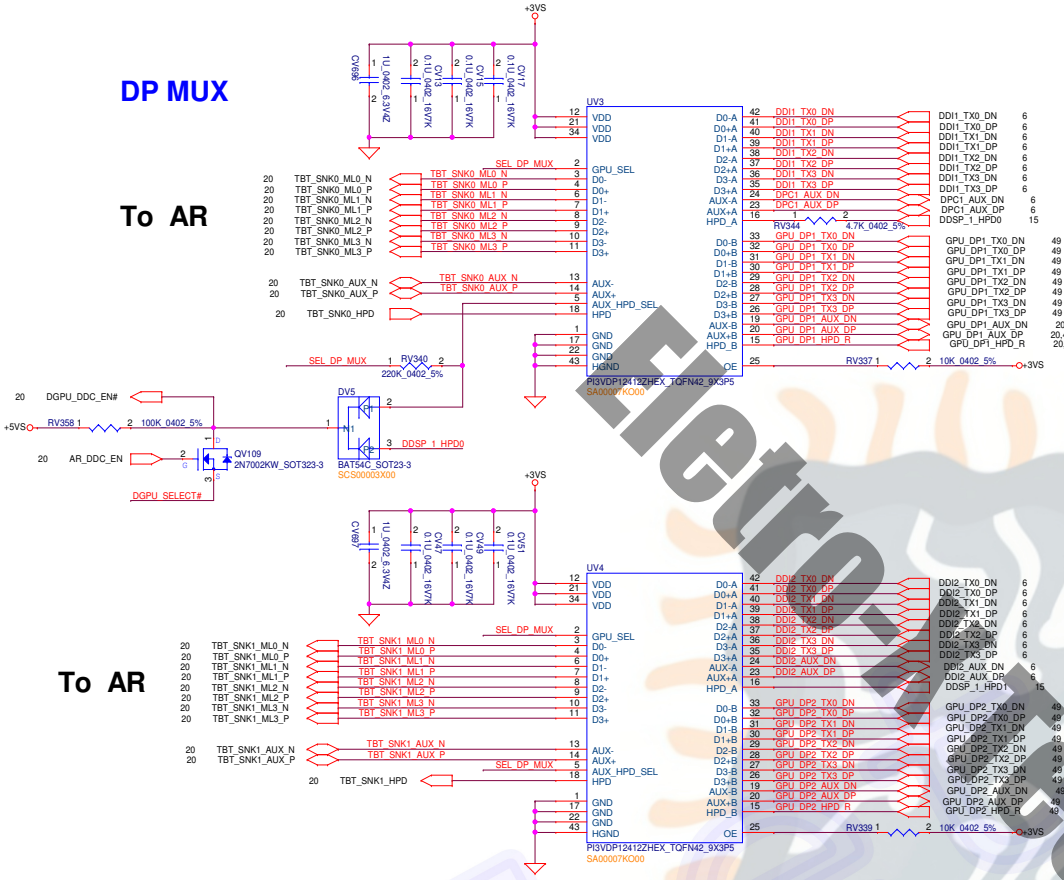
Date: Monday, November 16, 2015 | Sheet 23 of 80

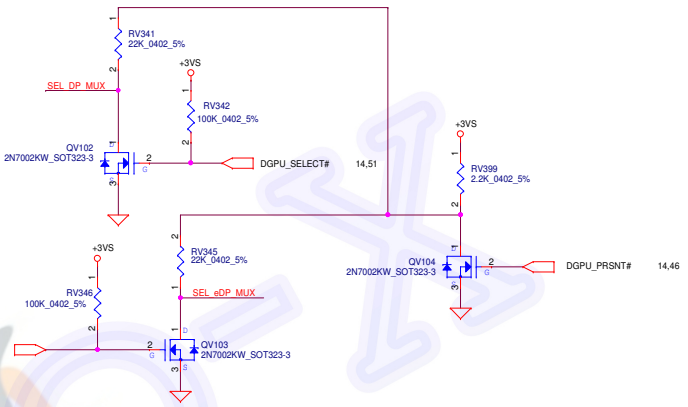
DP MUX

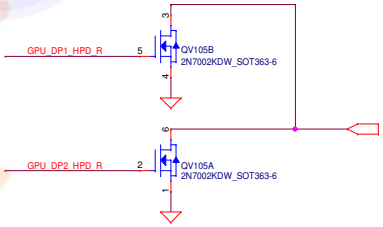
To AR

From CPU

From GPU







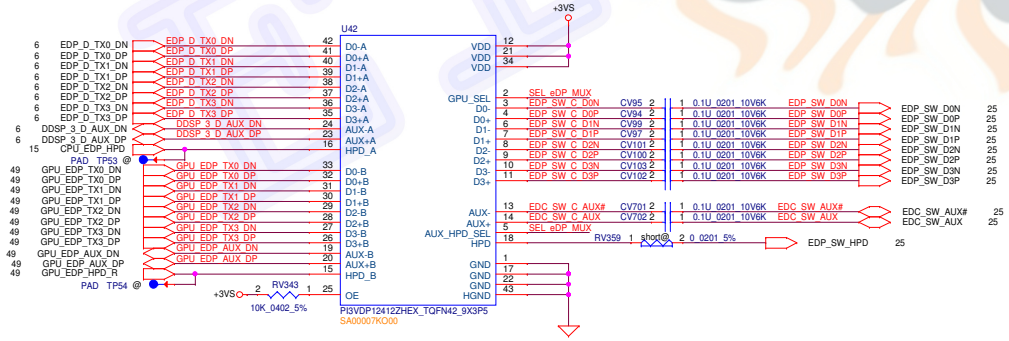
DGPU_SELECT#	UMA_ONLY#	Mode option
1	0	Invalid config
0	1	HP Hybrid SG
0	0	DGPU only
1	1	UMA/Headless SG

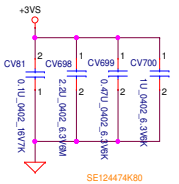
eDP MUX

From CPU

From GPU

To EDP Conn.

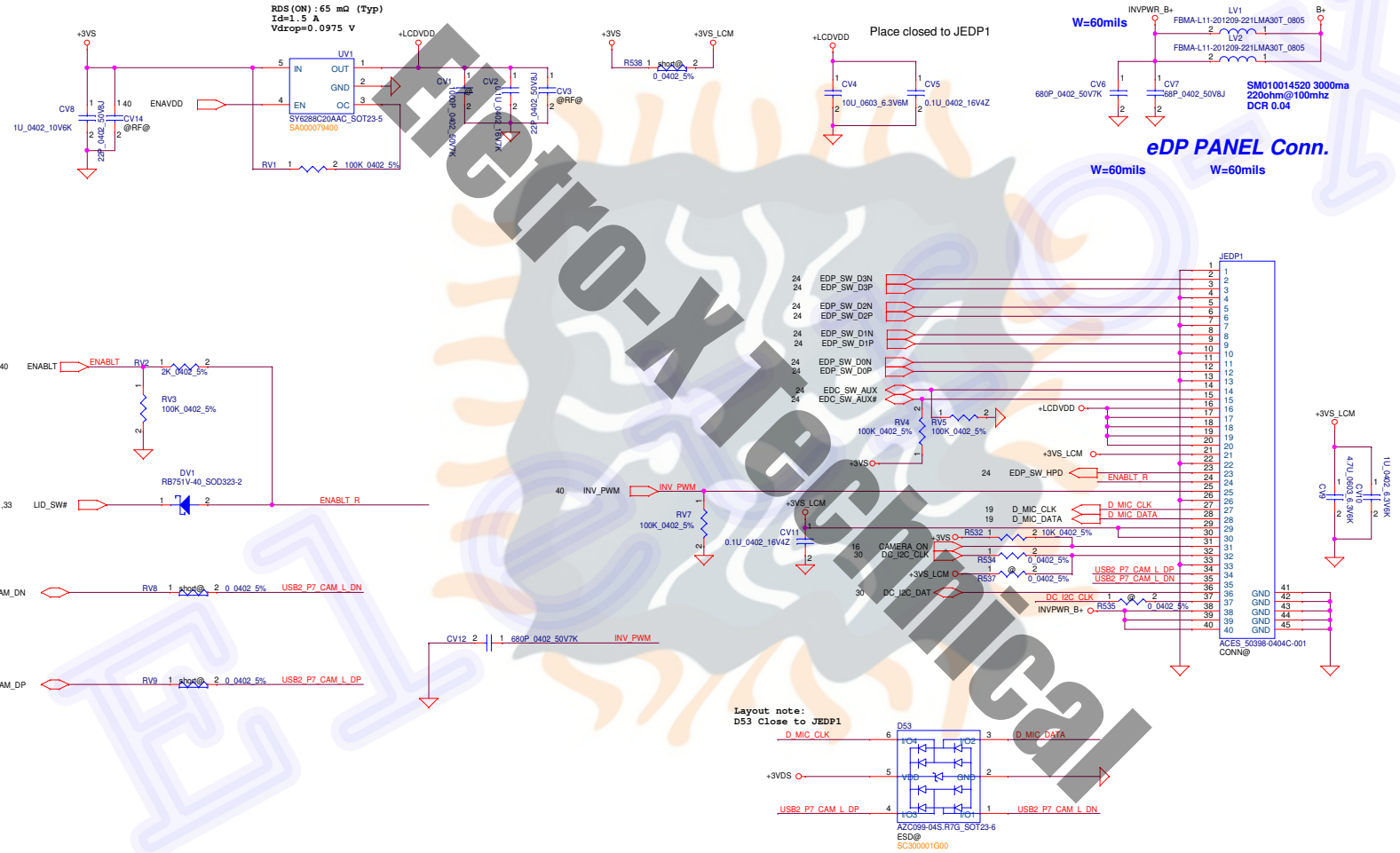




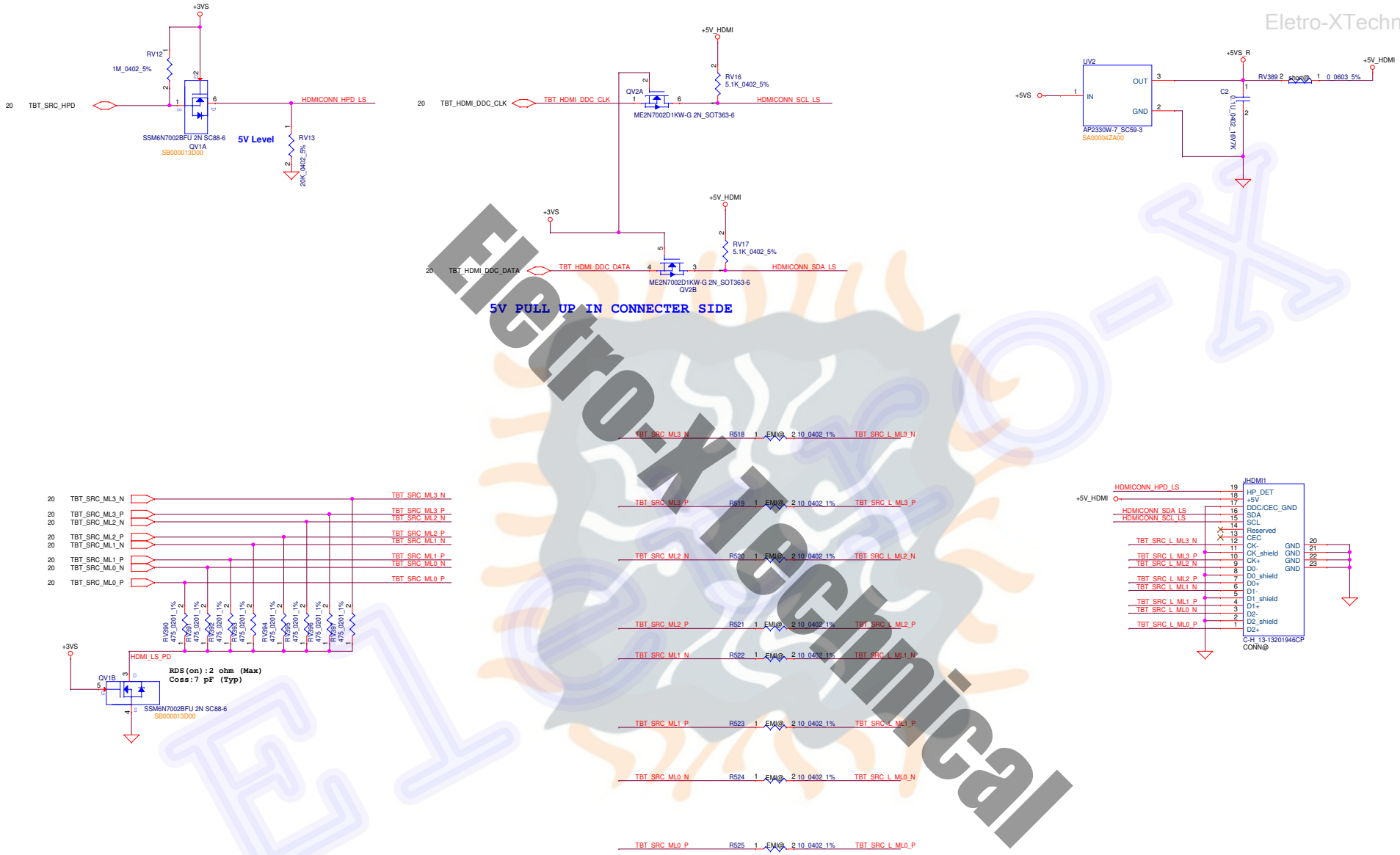
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	DP MUX to AP Ridge (1/2)		
Size	Document Number	Rev	
C	LA-C401P	1.0	
Date:	Monday, November 16, 2015	Sheet	24 of 80

LCD POWER CIRCUIT



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: eDP Panel
Size: C	Document Number: LA-C401P		Rev
Date: Monday, November 16, 2015	Sheet 25 of 80		

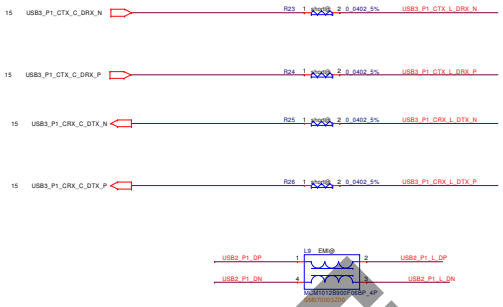


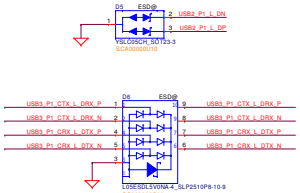
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: HDMI

Size	Document Number	Rev
C	LA-C401P	

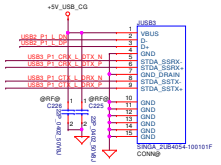
Date: Monday, November 16, 2015 Sheet 26 of 80

MB_USB 3.0 With charger function (Charging Port)

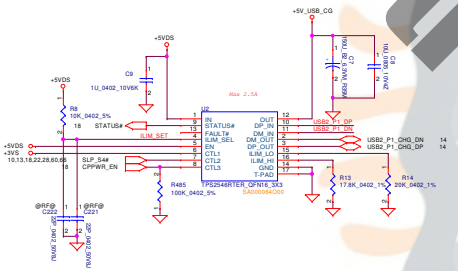




USB3.0 / USB2.0 Port1 (Left Side)



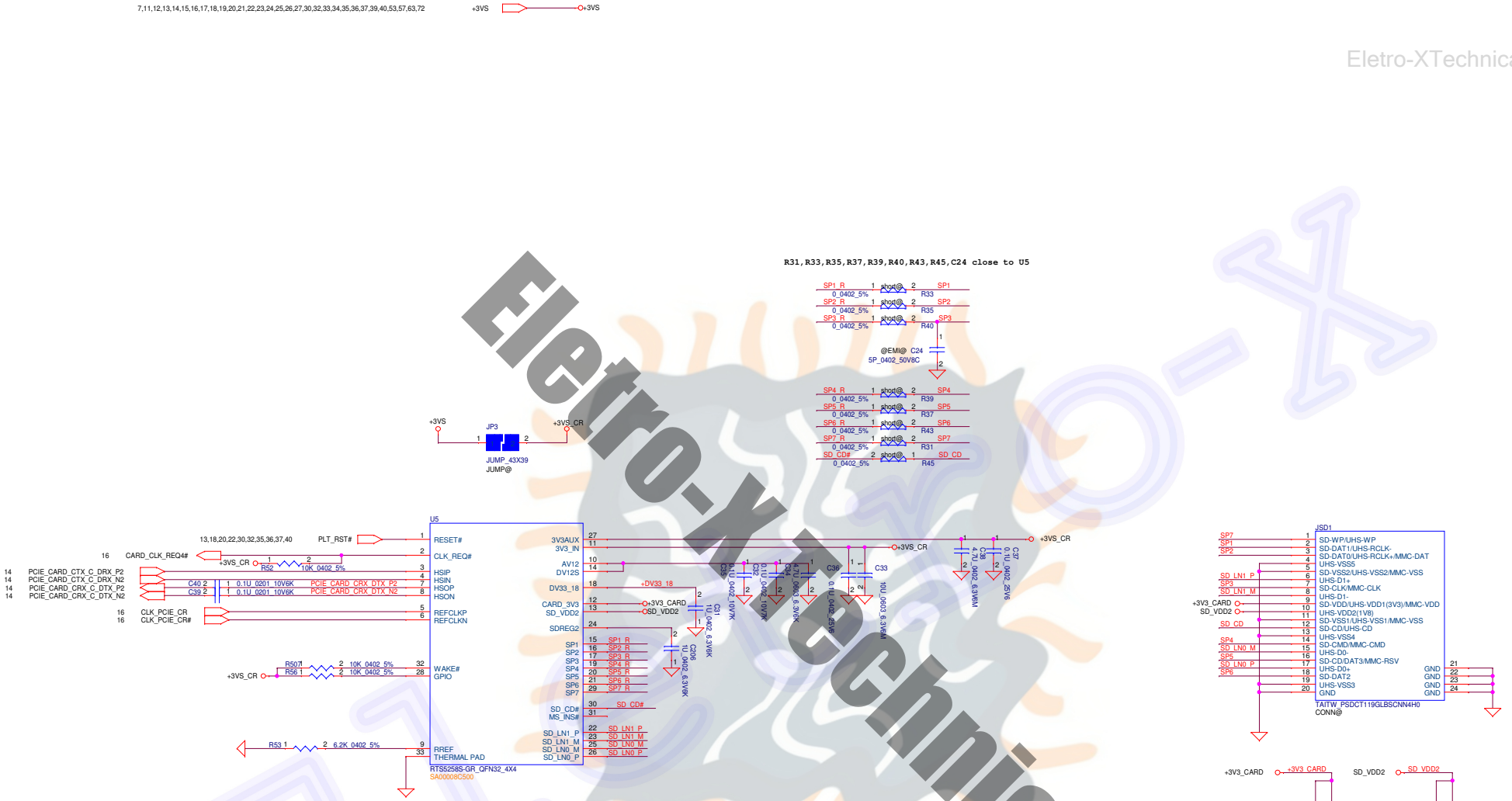
USB charger



State	S0				S3, S4, S5			
Mode	CDP				DCP			
Control pin	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL
	1	1	1	1	0	0	1	1

CDP:Charging Downstream Port
DCP:Dedicated Charging Port

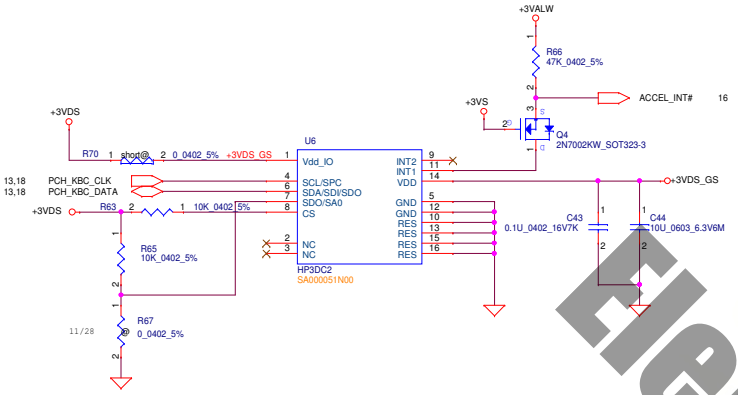
Security Classification	Compal Secret Data		Compal Electronics, Inc
Issued Date	2014/05/19	Deciphered Date 2015/12/31	Title: USB 3.0 MB port & charger
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: D; Document Number: LA-C401P; Rev: 1.0
			Date: Monday, November 16, 2015; Sheet 27 of 80



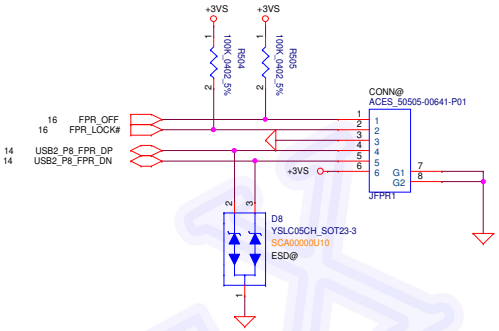
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: Card reader RTS5237-GR			
Size: C	Document Number: LA-C401P		Rev: 1.0
Date: Monday, November 16, 2015	Sheet 29 of 80		

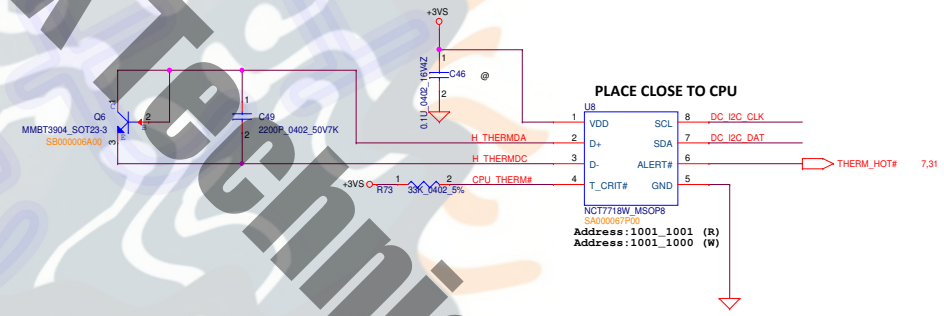
ACCELEROMETER



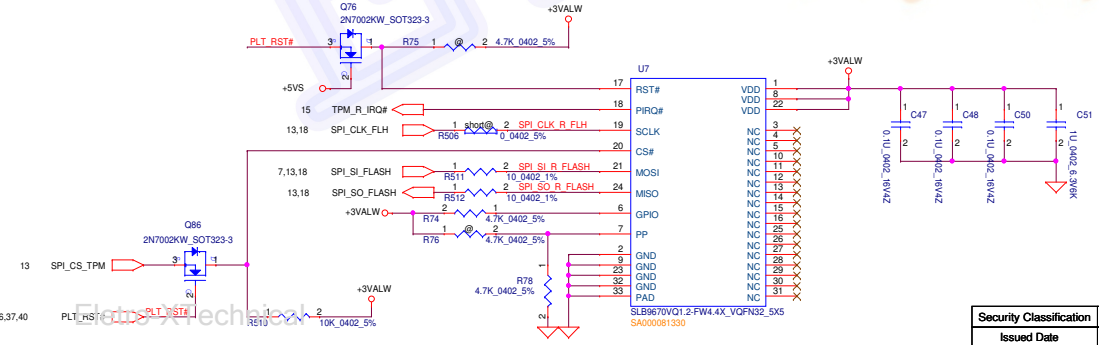
Finger printer

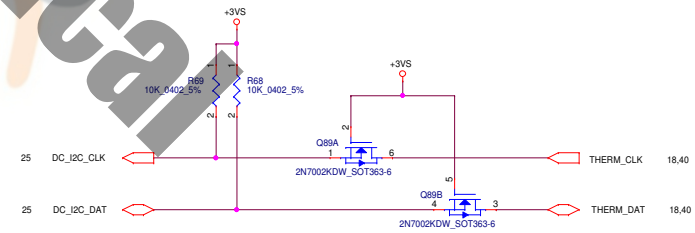


CPU THERMAL SENSOR



TPM





Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

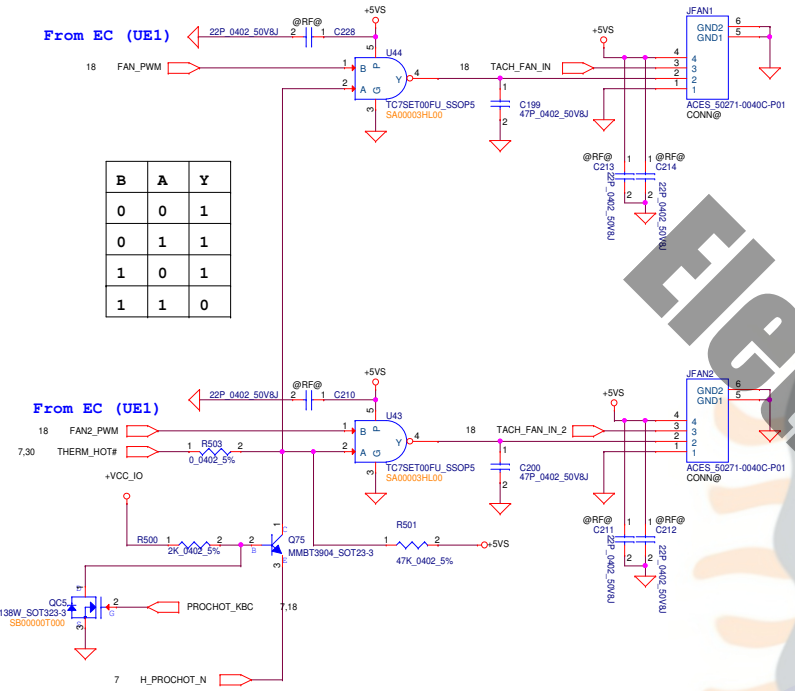
Compal Electronics, Inc.

Title: G-sensor & TPM&Thermal & FP

Size	Document Number	Rev
C	LA-C401P	1.0

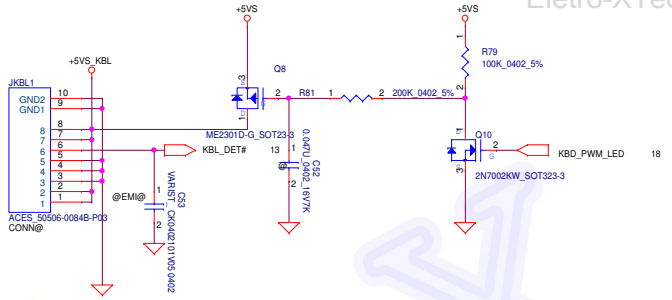
Date: Monday, November 16, 2015 Sheet 30 of 80

Fan Control Circuit

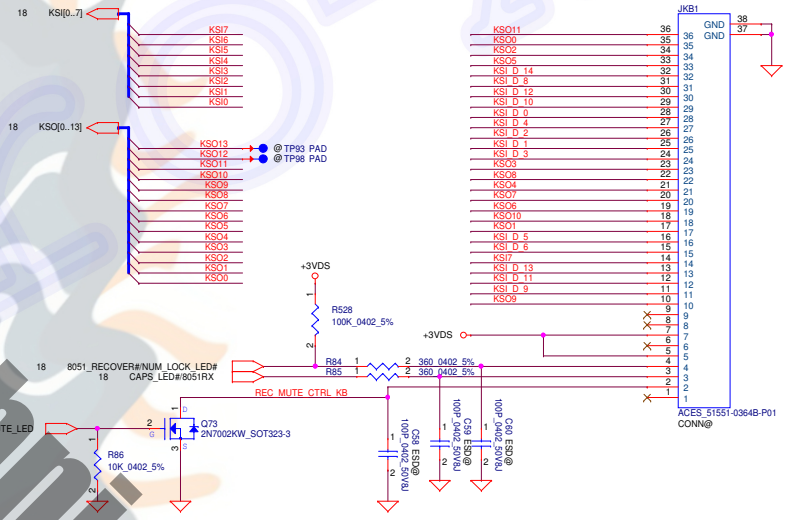


B	A	Y
0	0	1
0	1	1
1	0	1
1	1	0

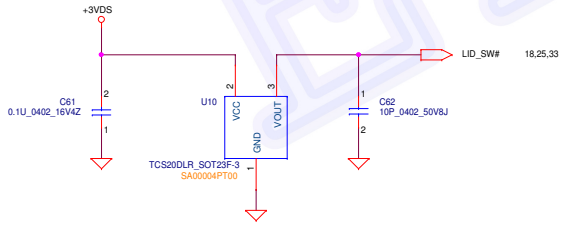
KB backlight Conn

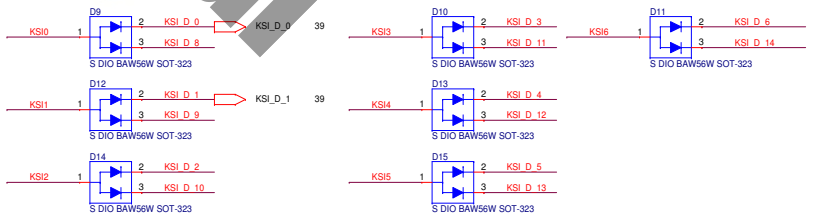


Keyboard conn



Lid Switch

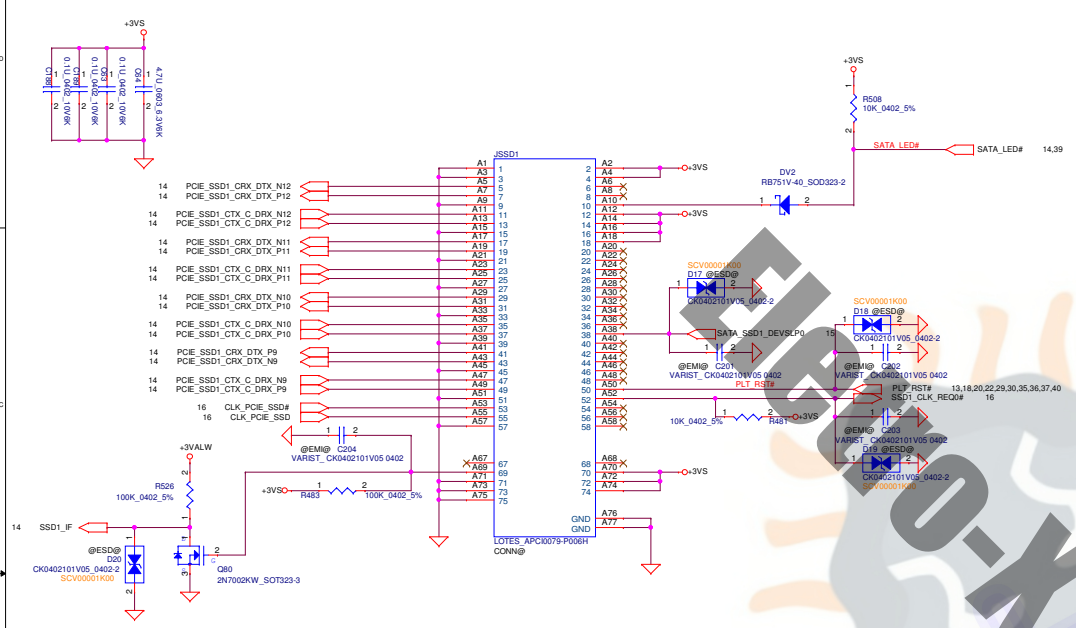


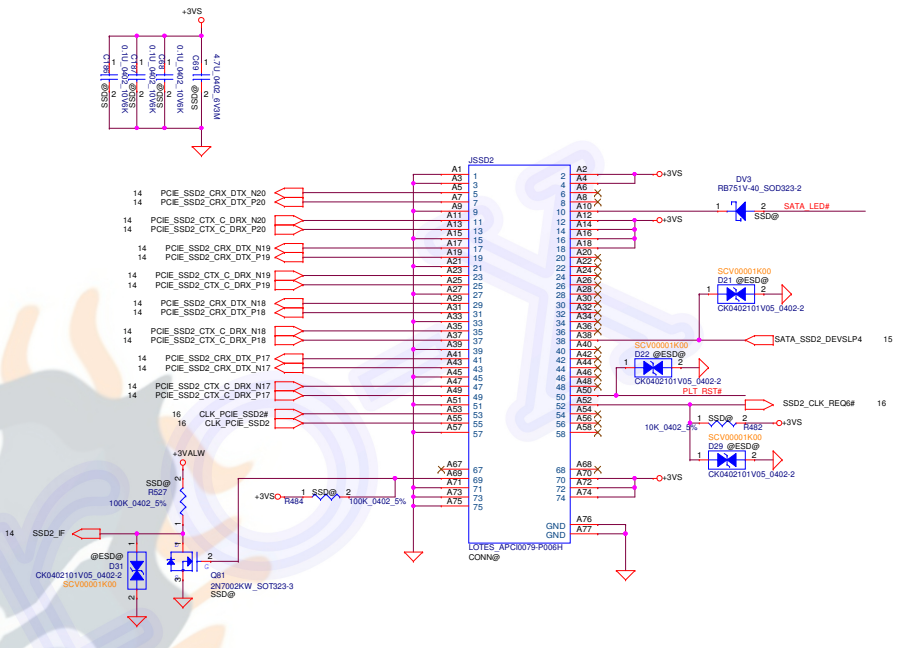


Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

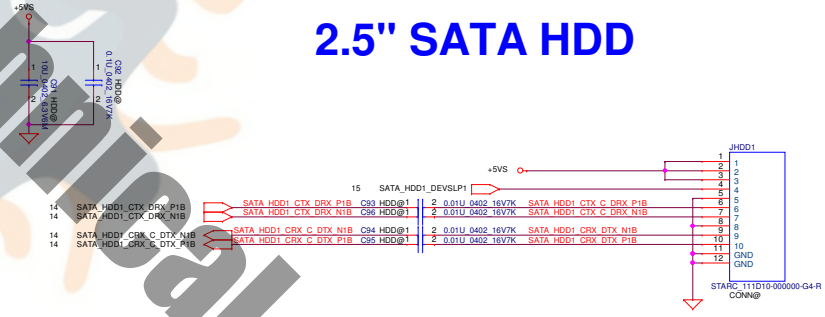
Compal Electronics, Inc.			
Title	KBL & FAN & LID		
Size C	Document Number LA-C401P		Rev 1.0
Date: Monday, November 16, 2015	Sheet 31 of 80		

M.2 SSD





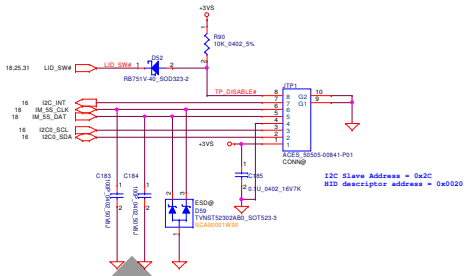
2.5" SATA HDD



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	M2 SSD & 2.5" HDD		
Size	Document Number		Rev
Custom	LA-C401P		1.0
Date:	Monday, November 16, 2015	Sheet	32 of 80

TP/B TO M/B

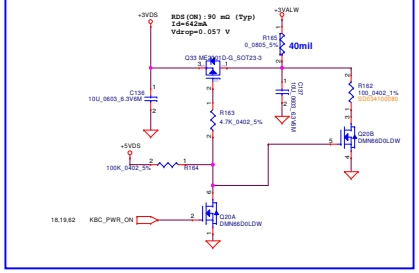


Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

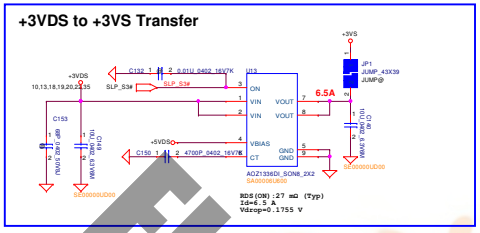
Compal Electronics, Inc.			
Title: IO Port			
Size: D	Document Number: LA-C401P		Rev: 1.0
Date: Monday, November 16, 2015	Sheet 33 of 80		

DC/DC

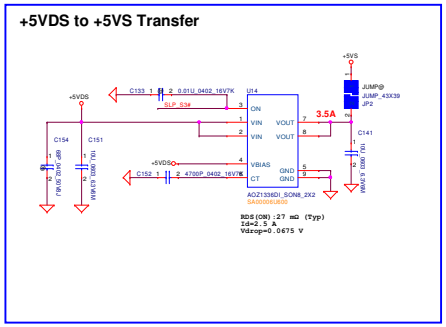
+3VDS TO +3VALW



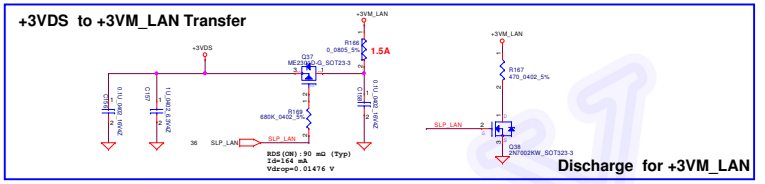
+3VDS to +3VS Transfer



+3VDS to +5VS Transfer

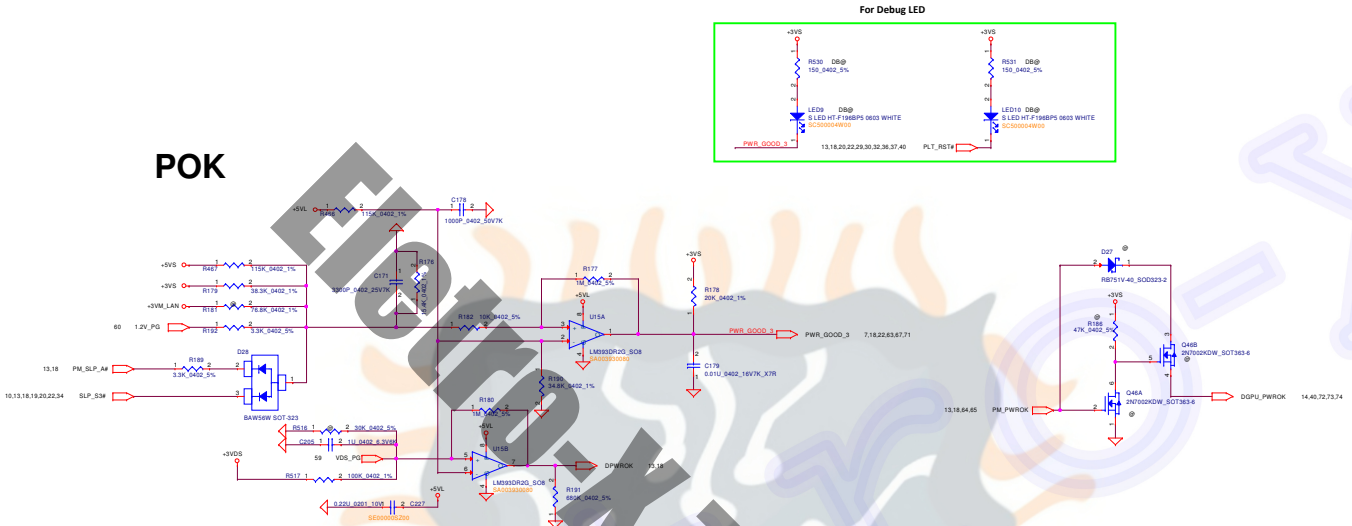


+3VDS to +3VM_LAN Transfer



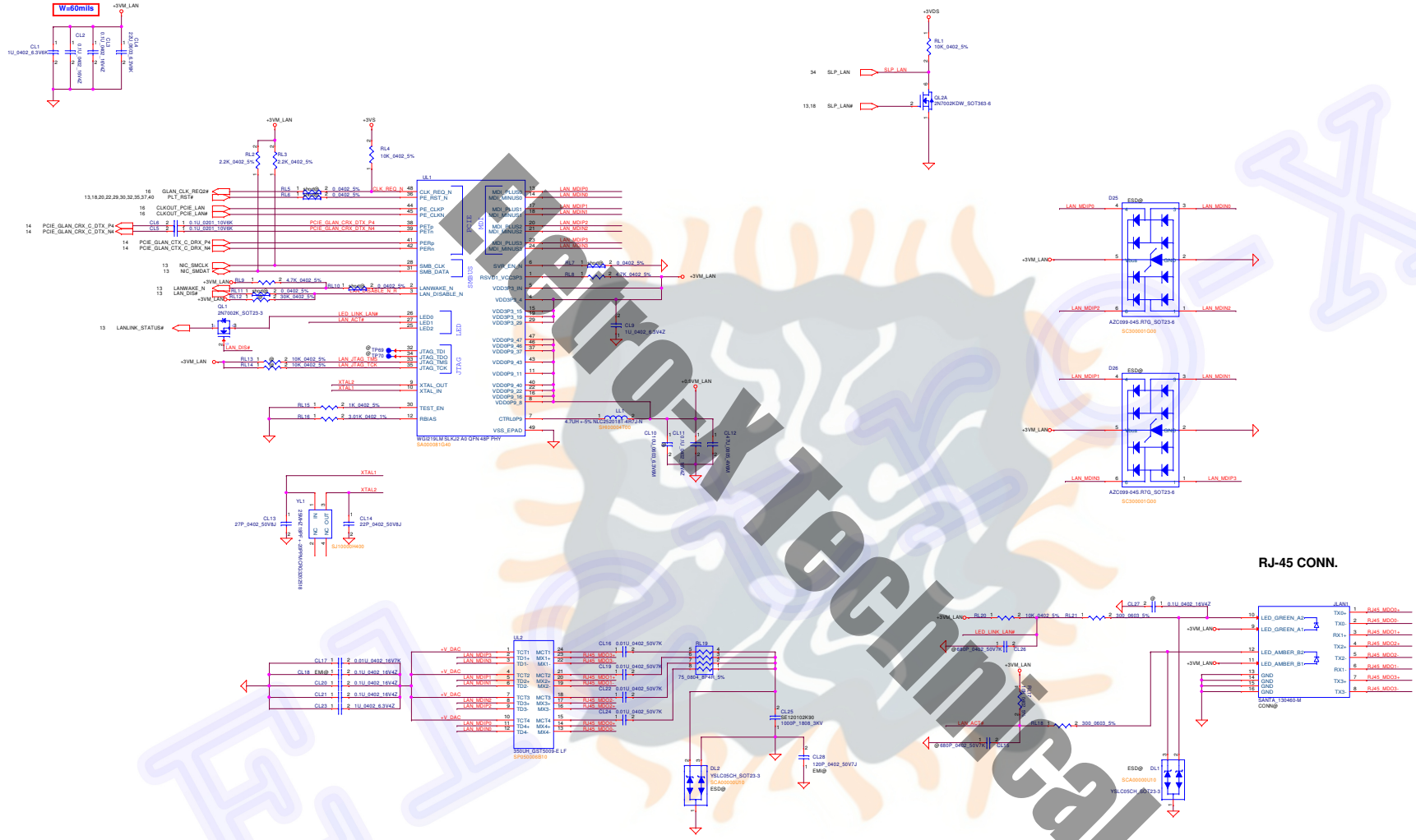
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/05/19	Deciphered Date	2015/12/31	Title: DC/DC
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: D	Document Number: LA-C401P	Rev: 1.0
			Date: Monday, November 16, 2015	Sheet 34 of 80

POK



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/05/19	Deciphered Date	2015/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Title: AUDIO JACK & HP AMP
			Size: D — Document Number: LA-C401P — Rev: 1.0
			Date: Monday, November 16, 2015 — Sheet 35 of 80

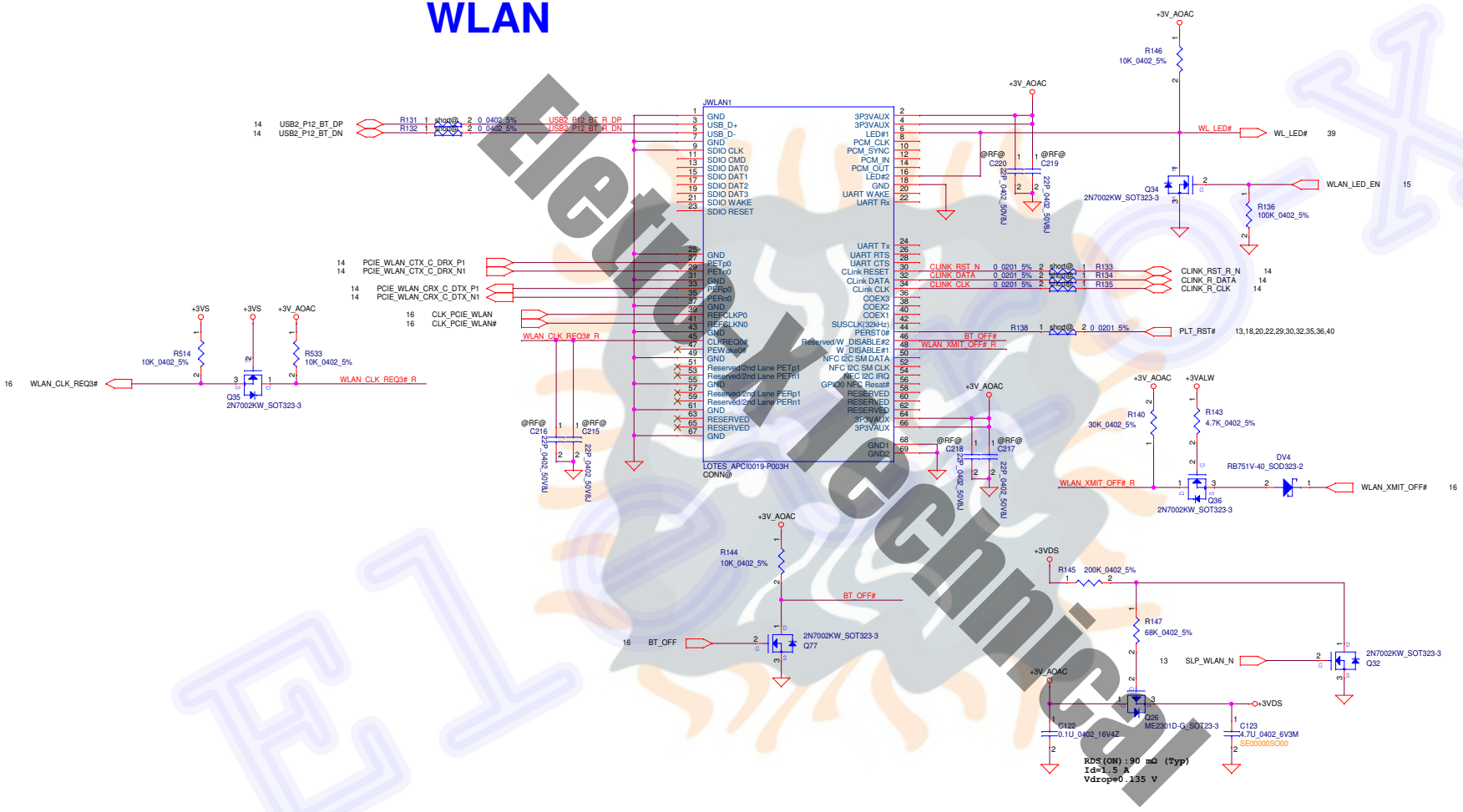
LAN



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.	
Title	Gigabit LAN CLARKVILLE
Size	Document Number: LA-C401P
Rev	1.0
Date: Monday, November 16, 2015	Sheet 36 of 80

WLAN



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: WLAN			
Size: C	Document Number: LA-C401P		Rev: 1.0
Date: Monday, November 16, 2015	Sheet 37 of 80		

Wifi & mute Button

POWER LED

POWER Button

MUTE

Wireless

WLAN LED

MUTE LED

DC-IN LED

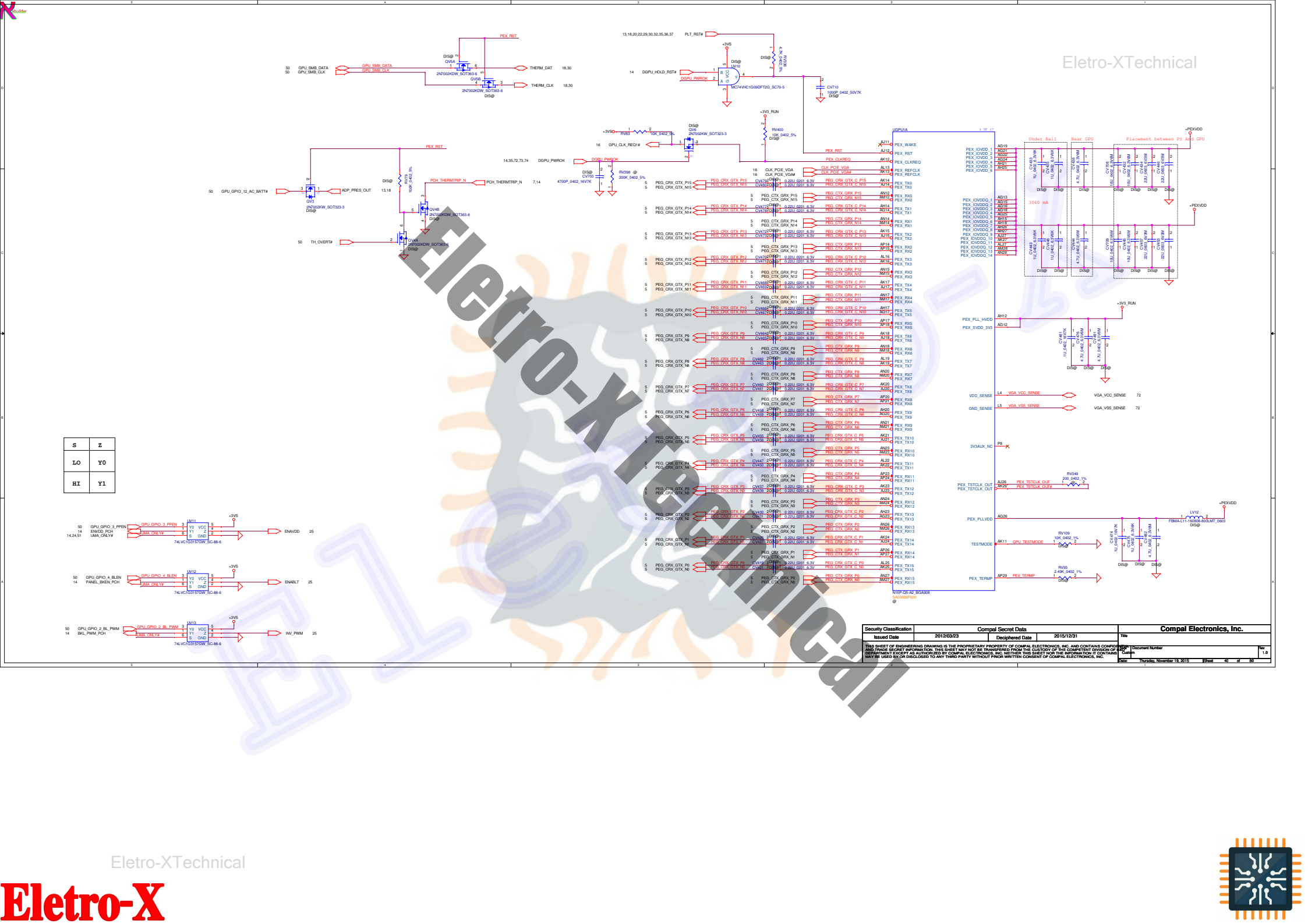
Connect to SB

HDD LED

Charger LED

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: Wifi & mute Button			
Size: C	Document Number: LA-C401P		Rev: 1.0
Date: Thursday, November 19, 2015	Sheet 39 of 80		



S	Z
LO	Y0
HI	Y1

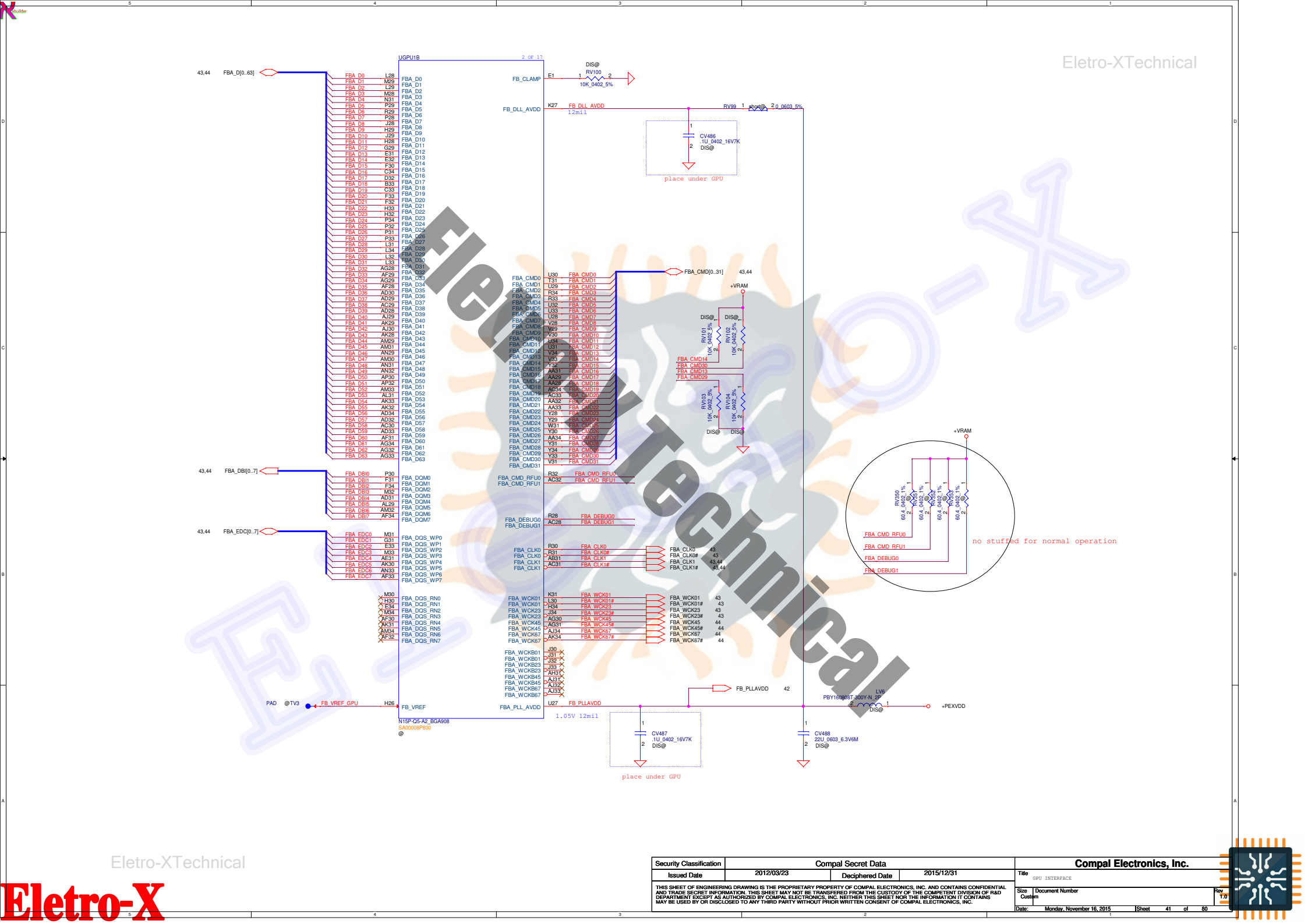
Security Classification	Compal Secret Data
Issued Date	2012/03/23
Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title

Size: Custom | Document Number | Rev 1.0

Date: Thursday, November 19, 2015 | Sheet 40 of 80



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date	2015/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title	GPU INTERFACE		
Size	Document Number		Rev
Custom			1.0
Date:	Monday, November 16, 2015	Sheet	41 of 80

N16P-Q1 VRAM STRAP

	X76@ Vendor	X76@ R_PD
	UV17,UV18,UV20,UV21, UV22,UV23,UV25,UV26	RV244
NS4G X7663732L11	Samsung SA000070800 128M32 K4G41325FC-HC03 FBGA 170P	20K SD034200280
NH4G X7663732L12	Hynix SA000085V00 128M32/2.5G H5GC4H24AJR-T2C FBGA	34.8K SD034348280

UGPU1 N16P@

N16P-Q1-A2 BGA 908P GPU

SA00008P800

UGPU1C 3 OF 17

45,46 FBB_D[0..63]

45,46 FBB_DBI[0..7]

45,46 FBB_EDC[0..7]

FBB_CMD[0..31] 45,46

+VRAM

DIS@ RV105 10K_0402_5% DIS@ RV106 10K_0402_5%

DIS@ RV107 10K_0402_5% DIS@ RV108 10K_0402_5%

FBB_CMD14 FBB_CMD30 FBB_CMD13 FBB_CMD29

RV354 60.4_0402_1% RV355 60.4_0402_1% RV356 60.4_0402_1% RV357 60.4_0402_1%

FBB_CMD_RFU0 FBB_CMD_RFU1 FBB_DEBUG0 FBB_DEBUG1

no stuffed for normal operation

FBB_DEBUG0 G14 FBB_DEBUG0 T1@ PAD

FBB_DEBUG1 G20 FBB_DEBUG1 T2@ PAD

FBB_CLK0 D12 FBB_CLK0 → FBB_CLK0 45

FBB_CLK0 E12 FBB_CLK0# → FBB_CLK0# 45

FBB_CLK1 E20 FBB_CLK1 → FBB_CLK1 45,46

FBB_CLK1 F20 FBB_CLK1# → FBB_CLK1# 45,45

FBB_WCK01 F8 FBB_WCK01 → FBB_WCK01 45

FBB_WCK01 E8 FBB_WCK01# → FBB_WCK01# 45

FBB_WCK23 A5 FBB_WCK23 → FBB_WCK23 45

FBB_WCK23 A6 FBB_WCK23# → FBB_WCK23# 45

FBB_WCK45 D24 FBB_WCK45 → FBB_WCK45 46

FBB_WCK45 D25 FBB_WCK45# → FBB_WCK45# 46

FBB_WCK67 B27 FBB_WCK67 → FBB_WCK67 46

FBB_WCK67 C27 FBB_WCK67# → FBB_WCK67# 46

FBB_PLL_AVDD H17 FB_PLLAVDD → FB_PLLAVDD 41

1.05V 12mil

CV489 .1U_0402_16V7K DIS@

place under GPU

N15P-Q5-A2_BGA908

SA00008P800

@

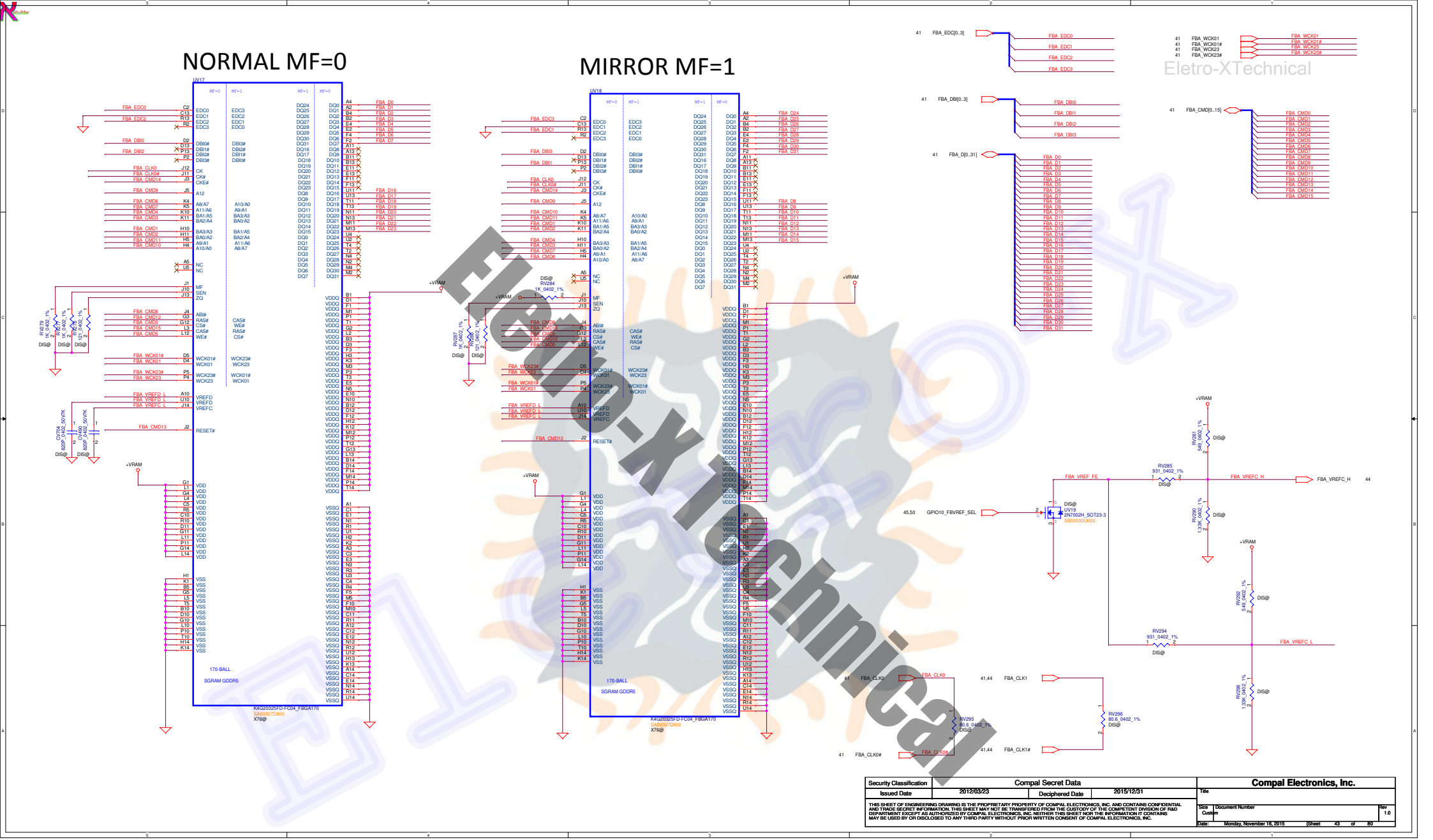
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2015/12/31

Compal Electronics, Inc.

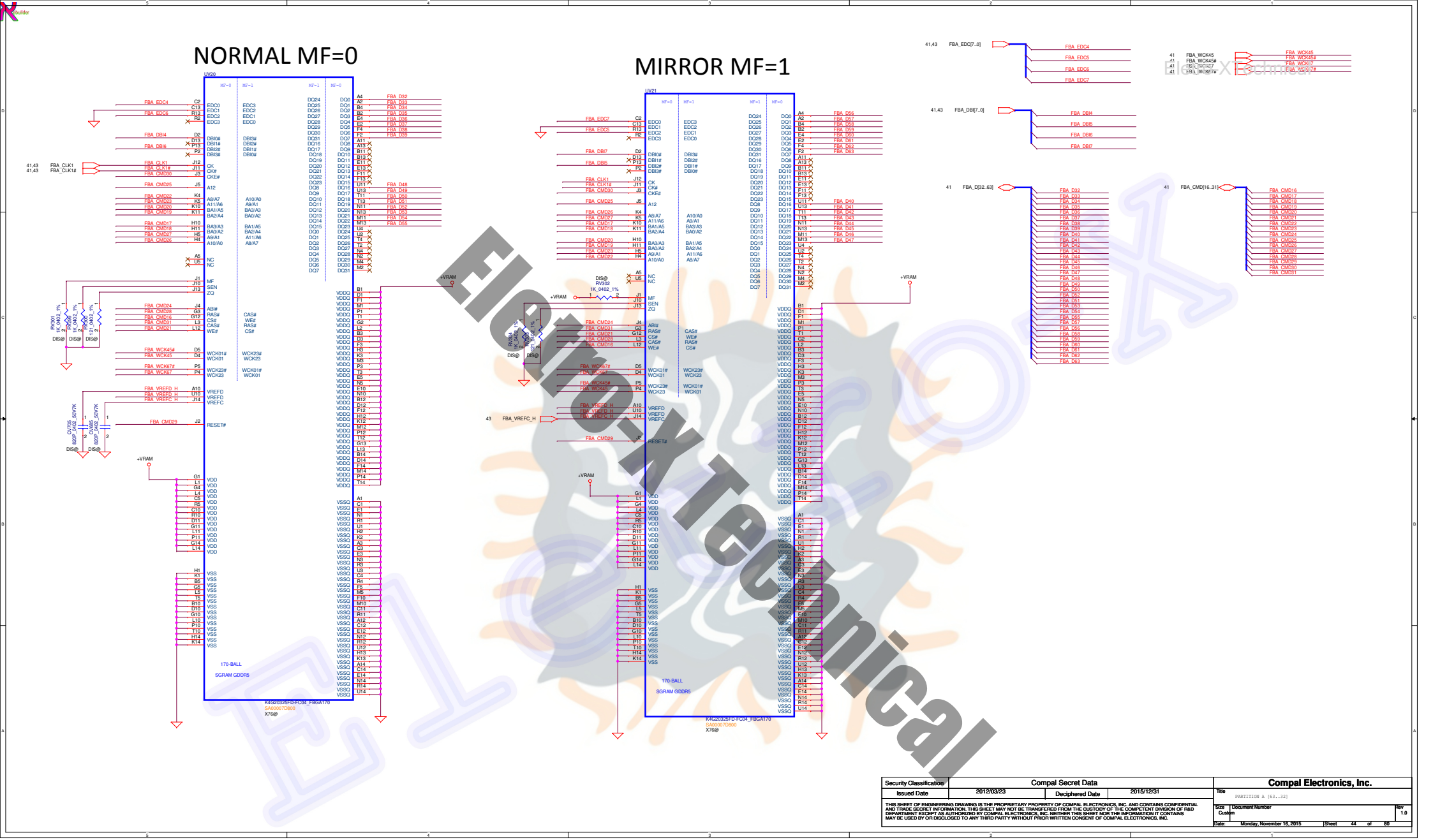
Title: GPU INTERFACE

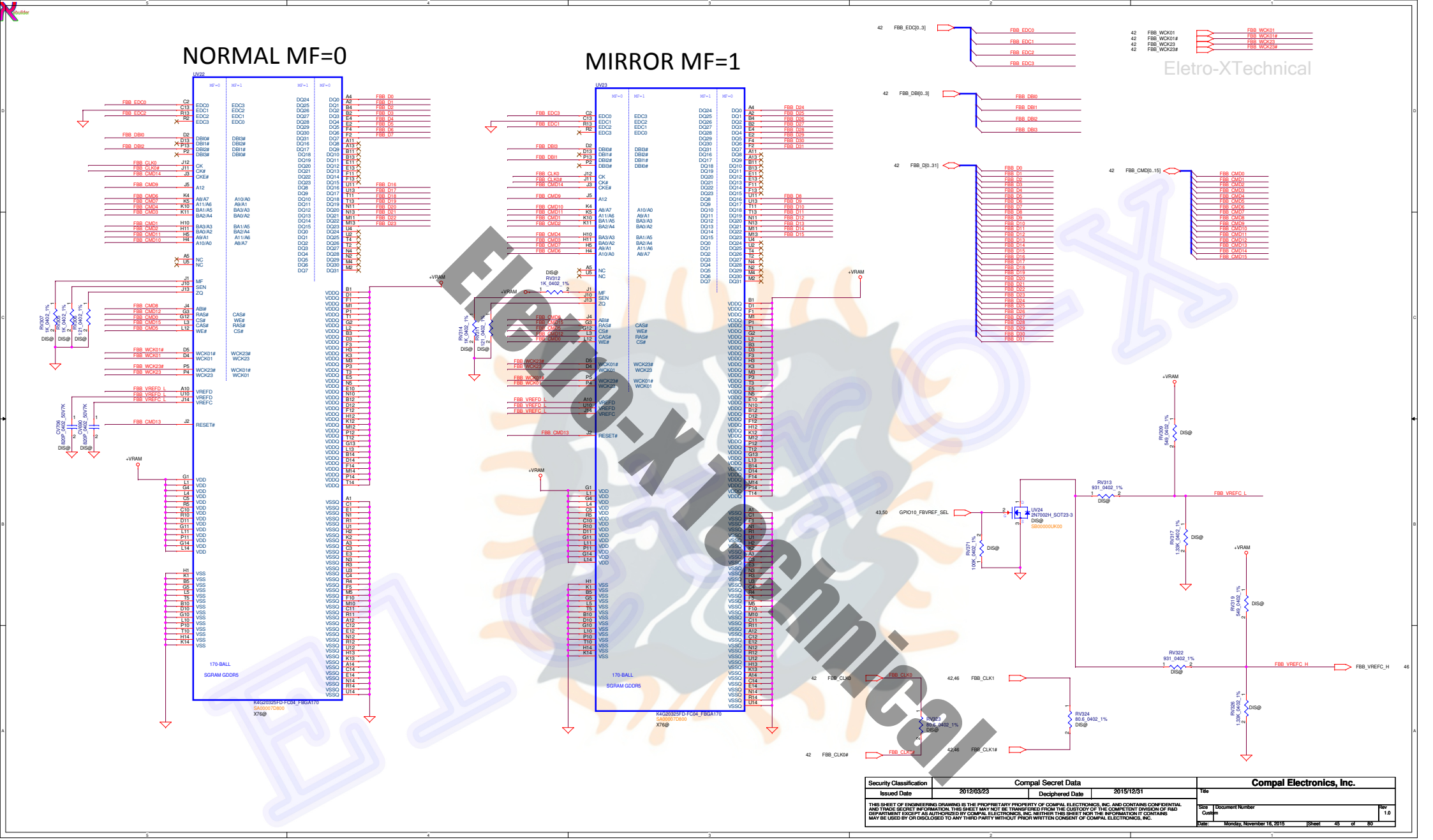
Size: Custom | Document Number | Rev: 1.0

Date: Monday, November 16, 2015 | Sheet 42 of 80



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date	2015/12/31
Title			
Size: Custom	Document Number		Rev: 1.0
Date: Monday, November 16, 2015	Sheet 43 of 80		



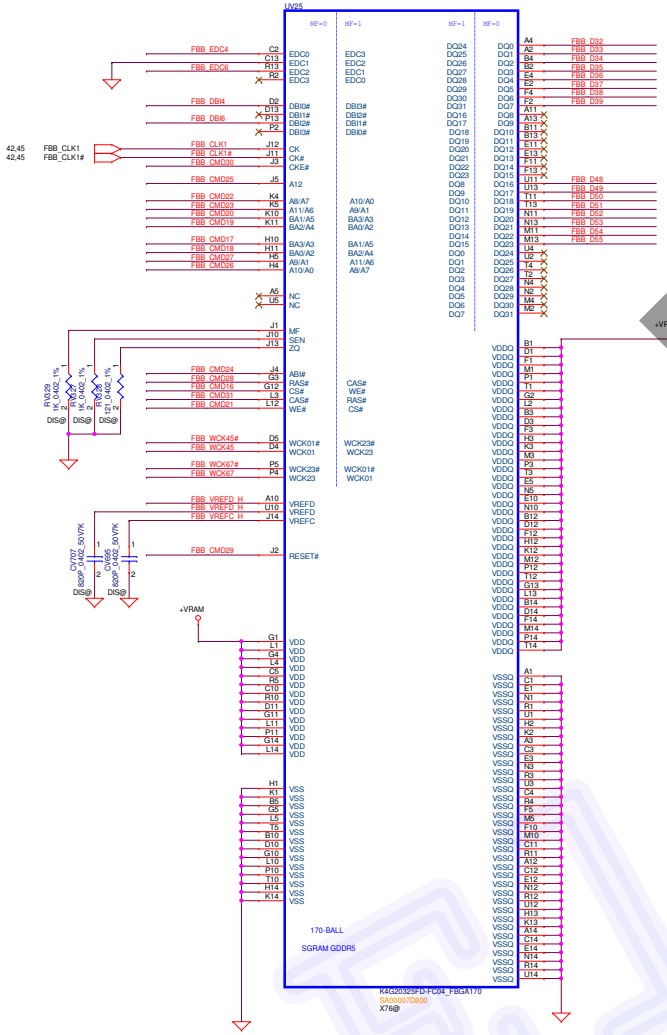


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date 2015/12/31	Title

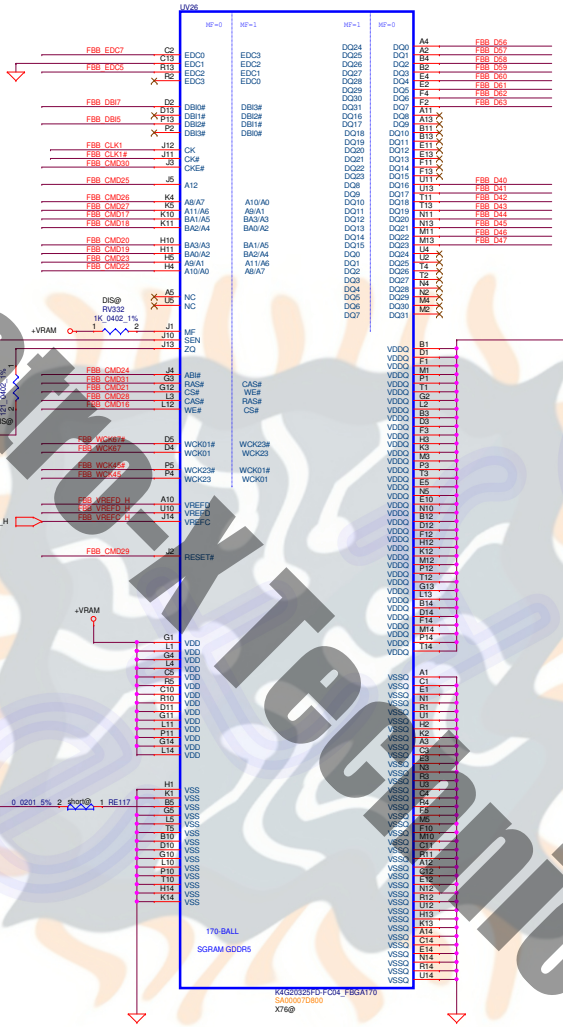
Size	Document Number	Rev
Custom		1.0

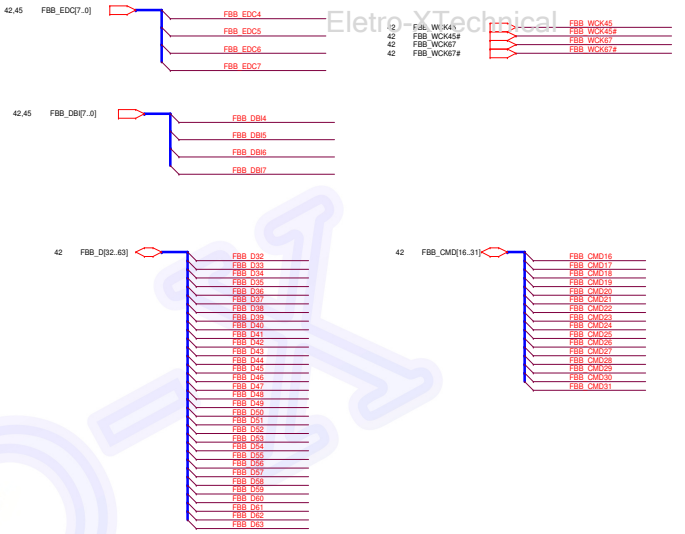
Date: Monday, November 16, 2015 Sheet 45 of 80

NORMAL MF=0



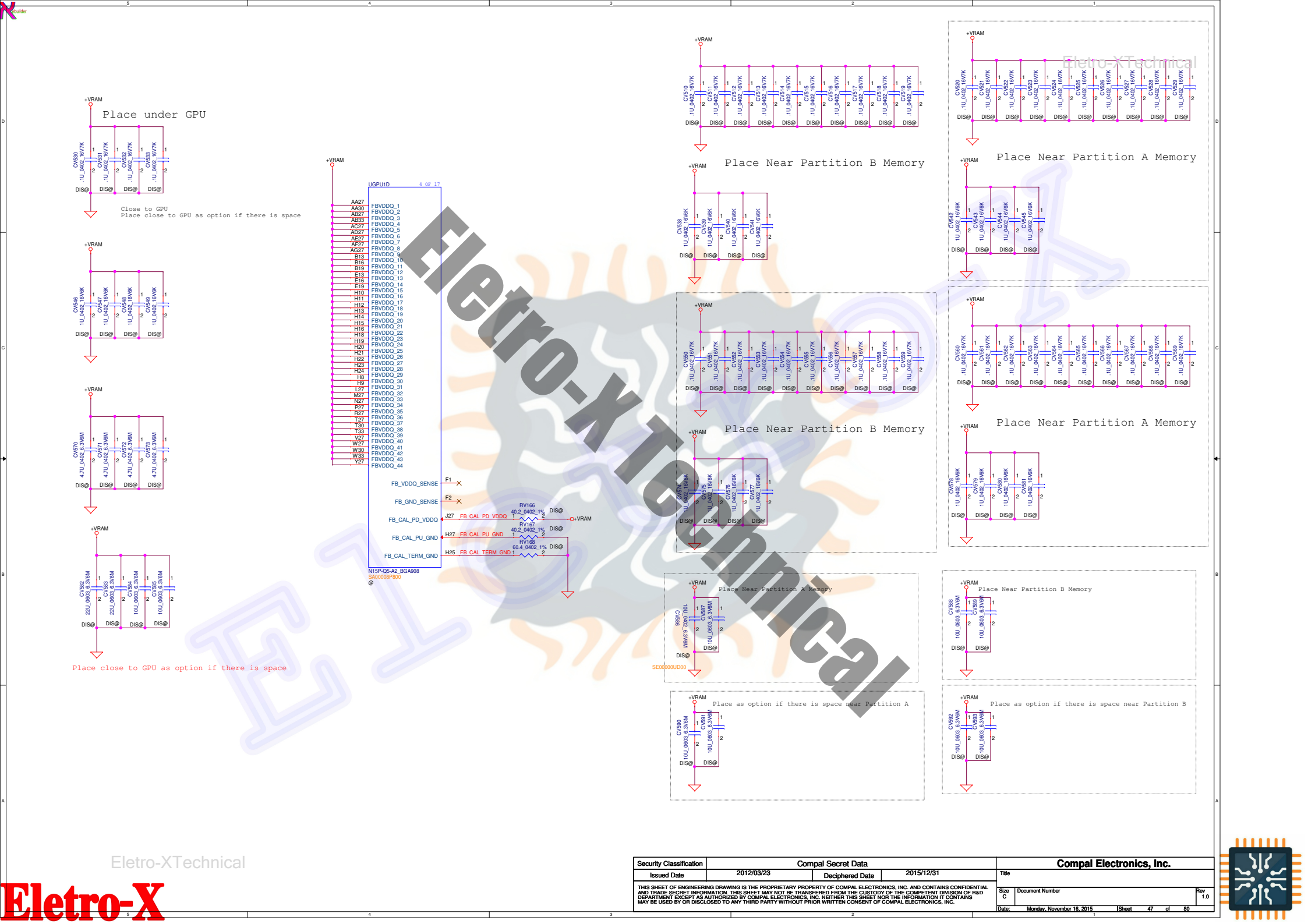
MIRROR MF=1





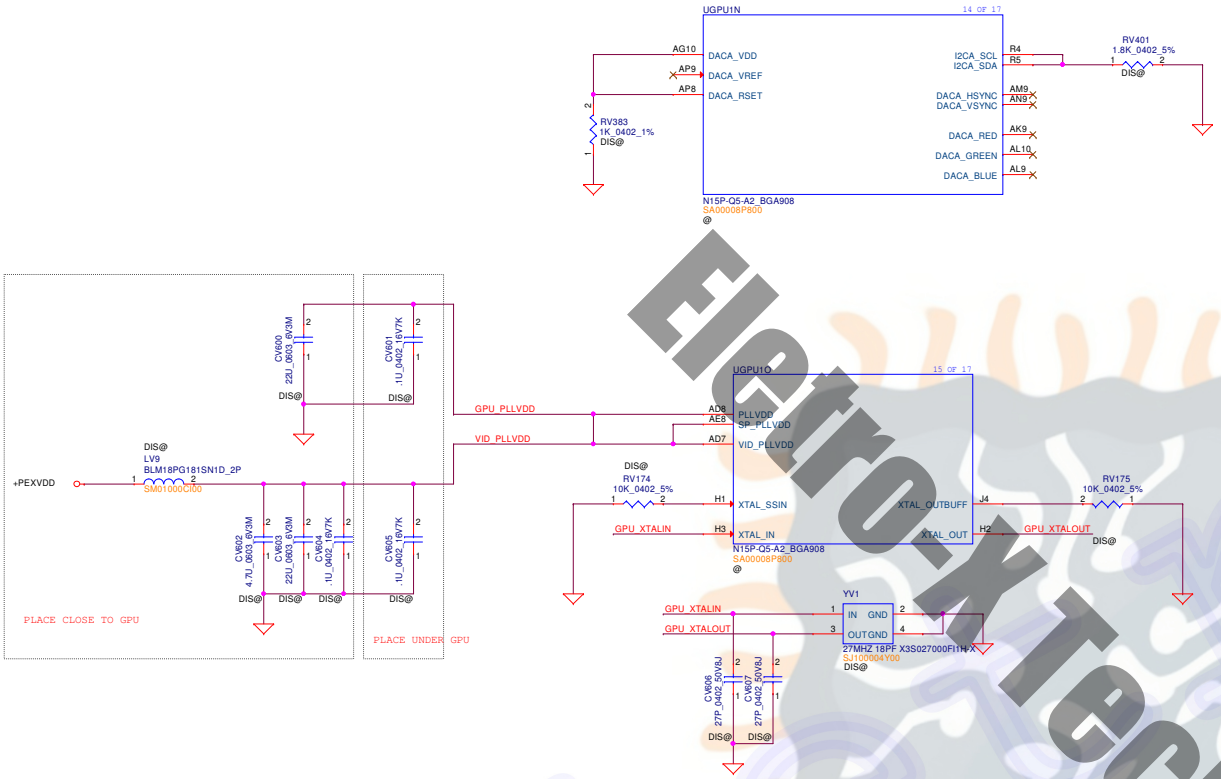
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date 2015/12/31	Title: PARTITION A [63..32]

Size: Custom	Document Number		Rev: 1.0
Date: Monday, November 16, 2015	Sheet 46 of 80		



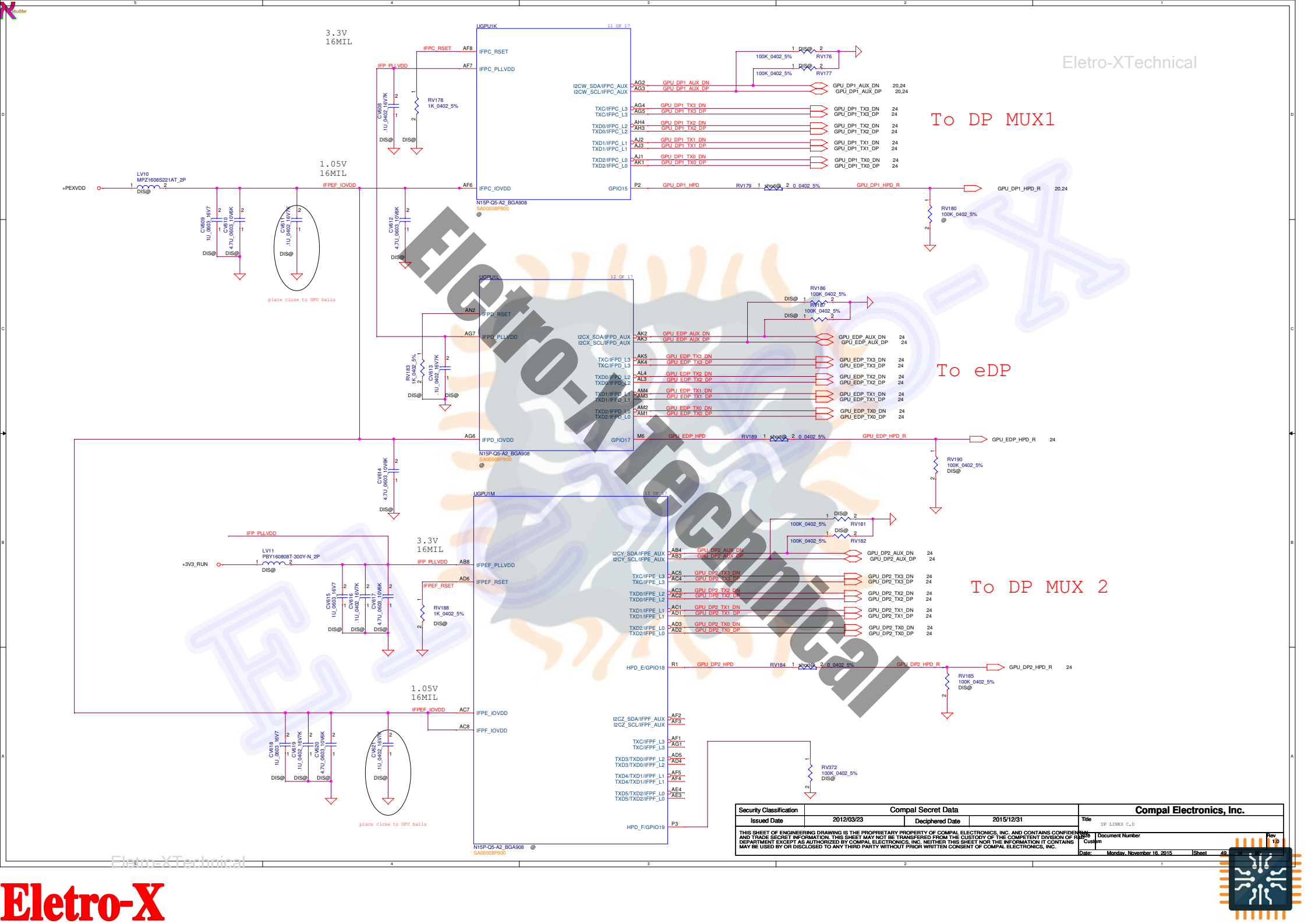
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date	2015/12/31

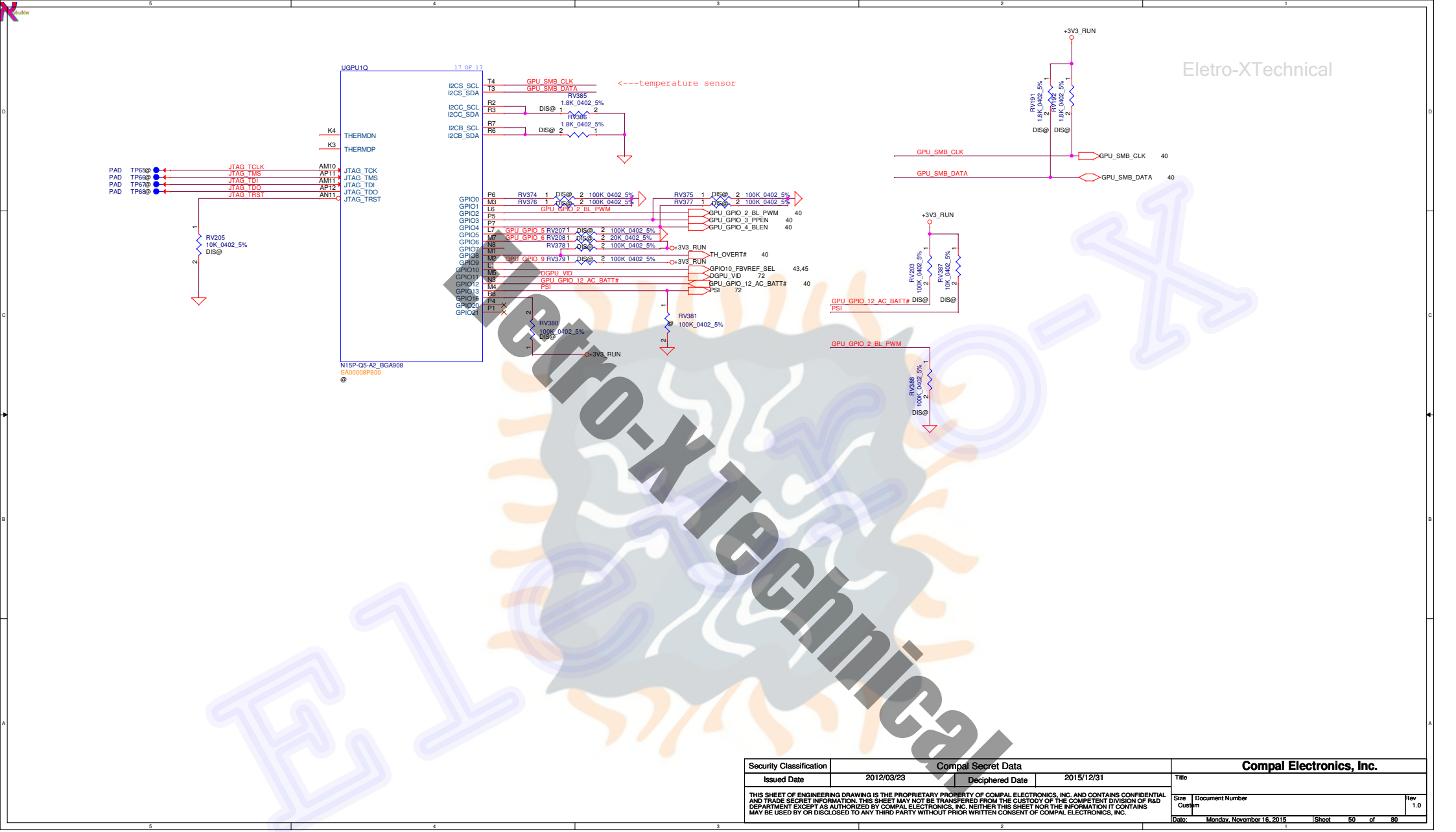
Title			
Size C	Document Number		Rev 1.0
Date: Monday, November 16, 2015	Sheet 47 of 80		



Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	DACA PLL, CRYSTAL		
Size	Document Number		Rev
Custom			1.0
Date:	Monday, November 16, 2015	Sheet	48 of 80


3.3V
16MIL
1.05V
16MIL
UGPU1K
11 OF 17
N15P-Q5-A2_BGA908
SA00008P800
UGPU1L
12 OF 17
UGPU1M
13 OF 17
To DP MUX1
To eDP
To DP MUX 2
place close to GPU balls
Eletro-XTechnical
Security Classification
Compal Secret Data
Issued Date
2012/03/23
Deciphered Date
2015/12/31
Compal Electronics, Inc.
Monday, November 16, 2015



Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title

Size	Document Number	Rev
Custom		1.0

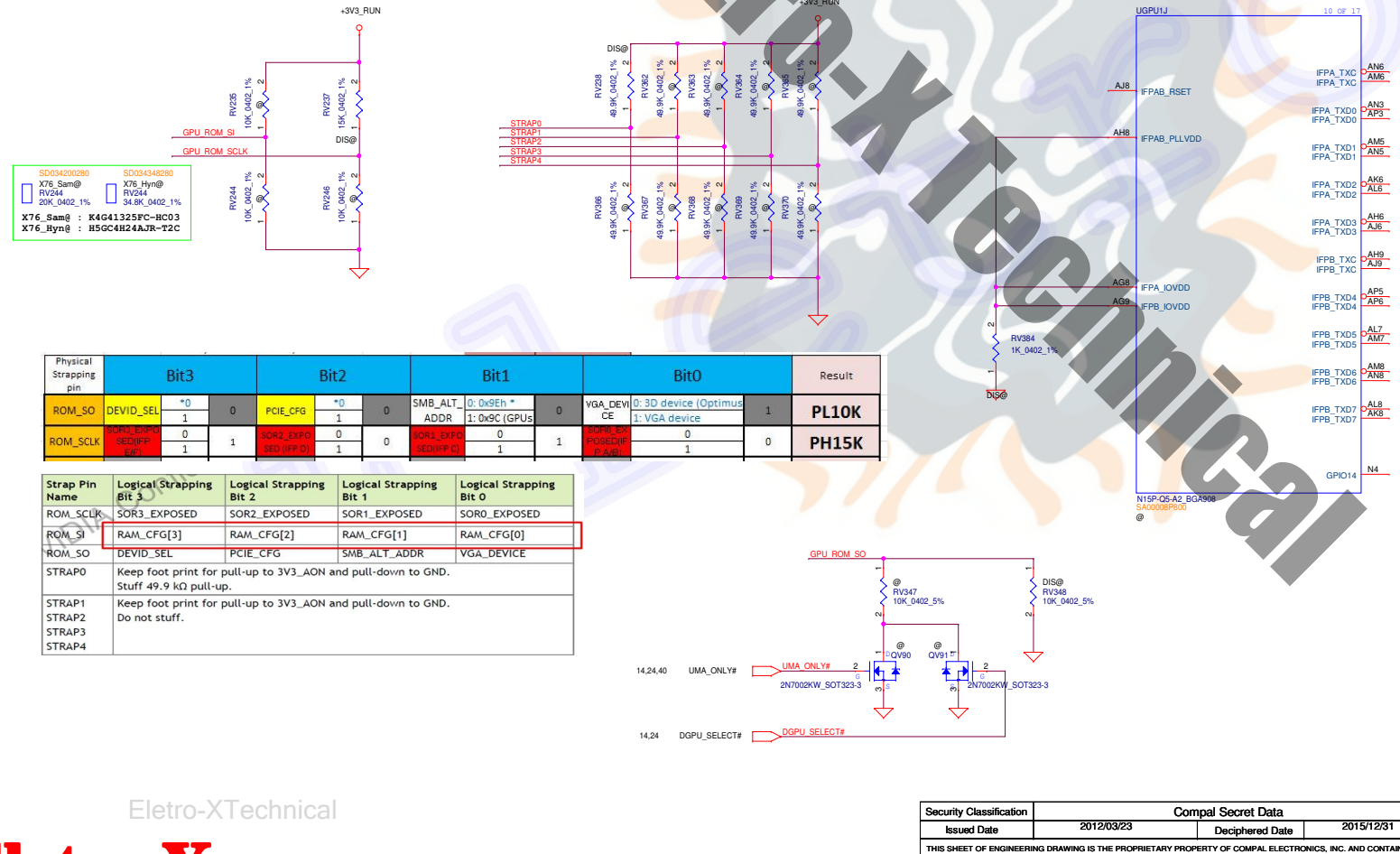
Date: Monday, November 16, 2015 Sheet 50 of 80

Multilevel Straps

0000 4.99K to GND	1000 4.99K to VCC
0001 10K to GND	1001 10K to VCC
0010 15K to GND	1010 15K to VCC
0011 20K to GND	1011 20K to VCC
0100 24.9K to GND	1100 24.9K to VCC
0101 30.1K to GND	1101 30.1K to VCC
0110 34.8K to GND	1110 34.8K to VCC
0111 45.3K to GND	1111 45.3K to VCC

GK107 Binary Straps

Function	Bringup Mode
RAMCFG[2]	ROM_SO
RAMCFG[1]	ROM_SI
RAMCFG[0]	STRAP3
3GIO_PADCFG_LUT_ADR[2]	STRAP2
3GIO_PADCFG_LUT_ADR[1]	STRAP1
3GIO_PADCFG_LUT_ADR[0]	STRAP0
SMB_ALT_ADDR	ROM_SCLK
PCIE_MAX_SPEED	STRAP4

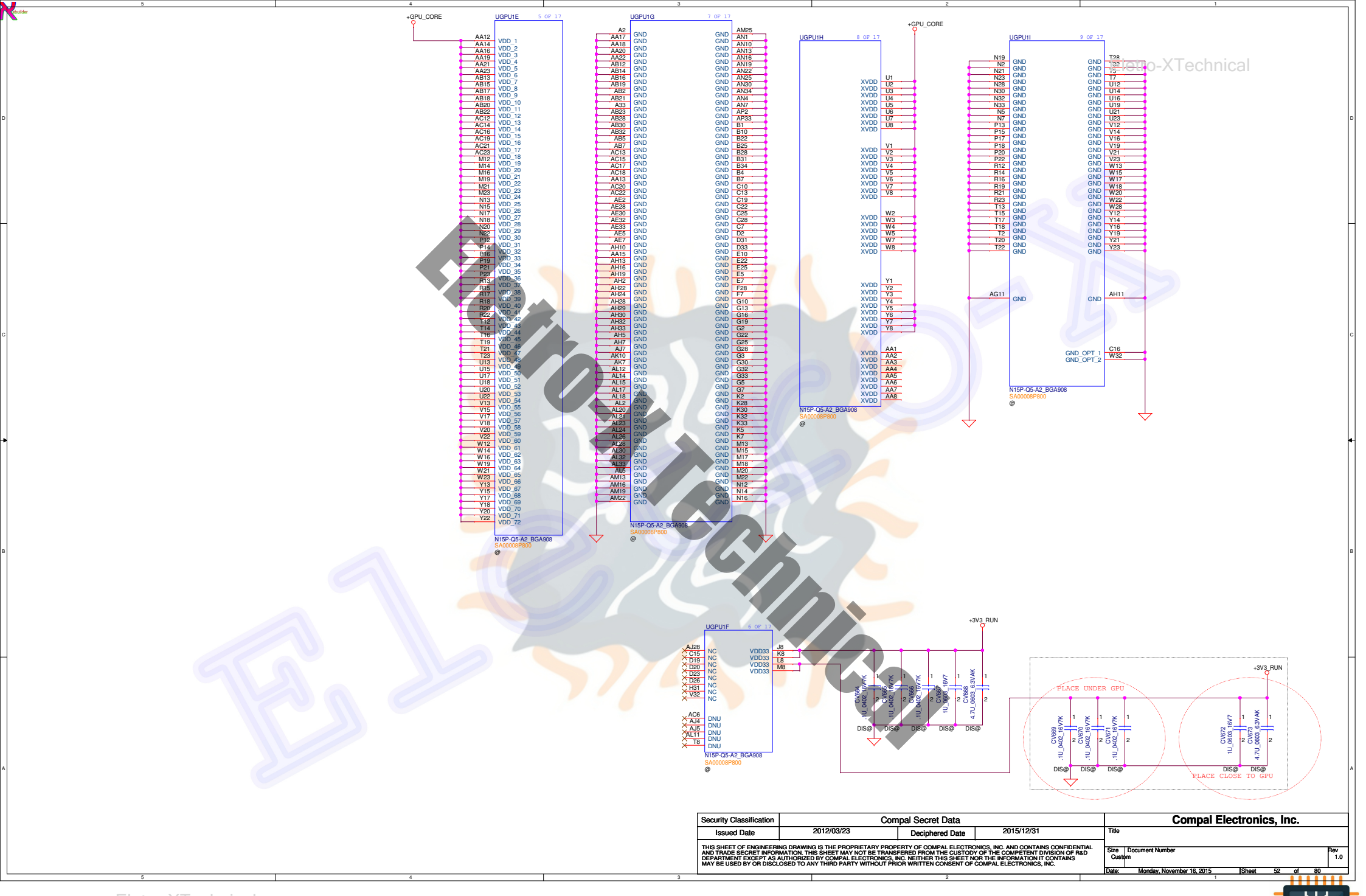


Physical Strapping pin	Bit3			Bit2			Bit1			Bit0			Result
ROM_SO	DEVID_SEL	*0	0	PCIE_CFG	*0	0	SMB_ALT_ADDR	0: 0x9Eh *	0	VGA_DEVICE	0: 3D device (Optimus	1	PL10K
		1			1			1: 0x9C (GPUs			1: VGA device		
ROM_SCLK	SOR3_EXPOSED(IFP E/F)	0	1	SOR2_EXPOSED (IFP D)	0	0	SOR1_EXPOSED(IFP C)	0	1	SOR0_EXPOSED(IFP A/B)	0	0	PH15K
		1			1			1			1		

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date 2015/12/31	Title

Size Custom	Document Number		Rev 1.0
Date: Monday, November 16, 2015	Sheet 51 of 80		



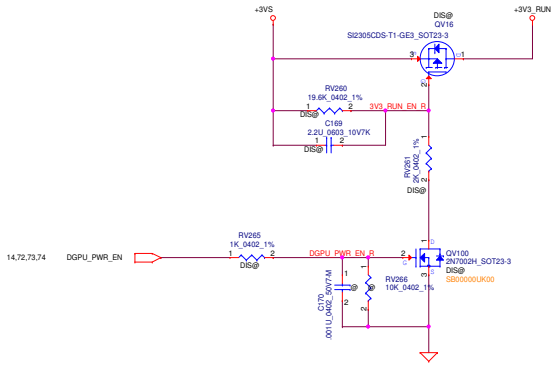
Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title

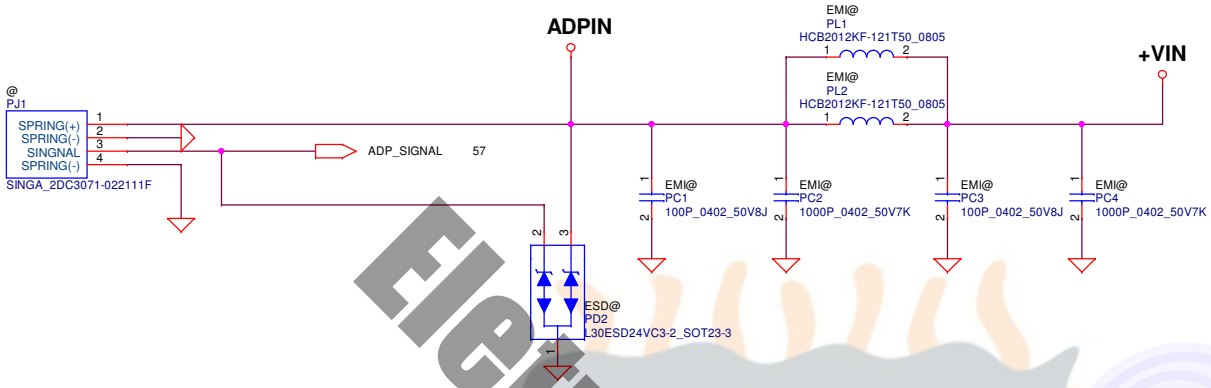
Size	Document Number	Rev
Custom		1.0

Date: Monday, November 16, 2015 Sheet 52 of 80



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/23	Deciphered Date 2015/12/31	Title

Size: Custom	Document Number		Rev: 1.0
Date: Monday, November 16, 2015	Sheet 53	of 80	



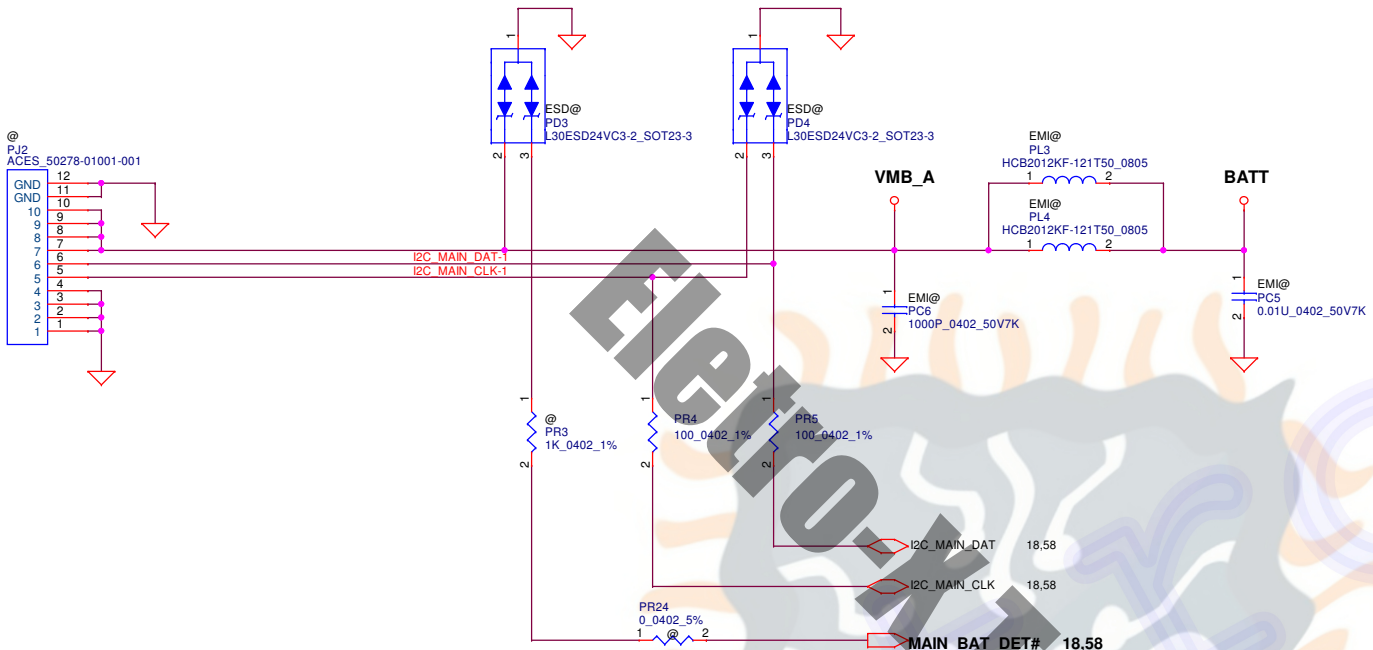
Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

Compal Electronics, Inc.

Title: PWR-DC CONN

Size: Custom | Document Number: LA-B191P | Rev: 1.0

Date: Monday, November 16, 2015 | Sheet 55 of 80



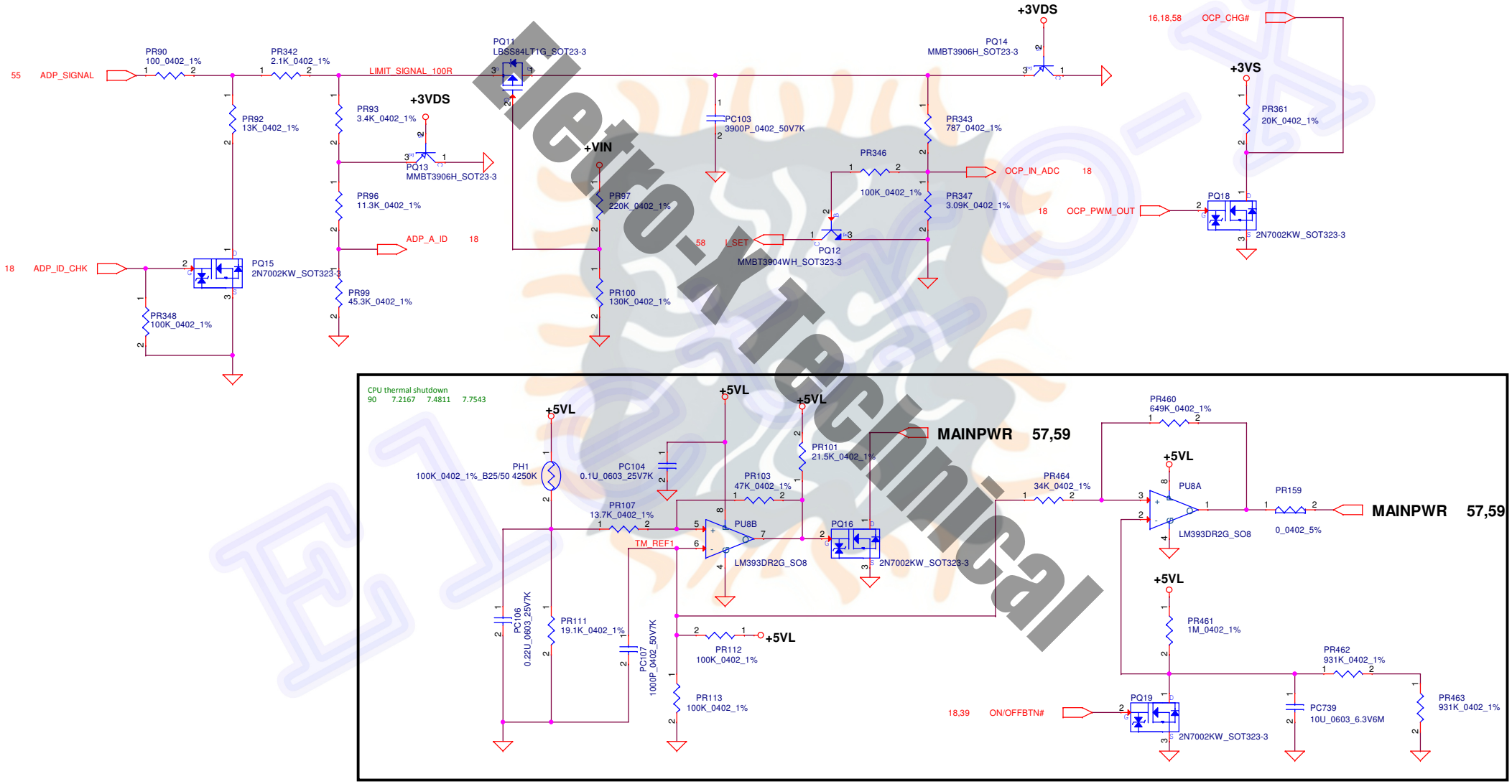
Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

Compal Electronics, Inc.

Title: **PWR-BATT CONN**

Size: Custom | Document Number: **LA-B191P** | Rev: 1.0

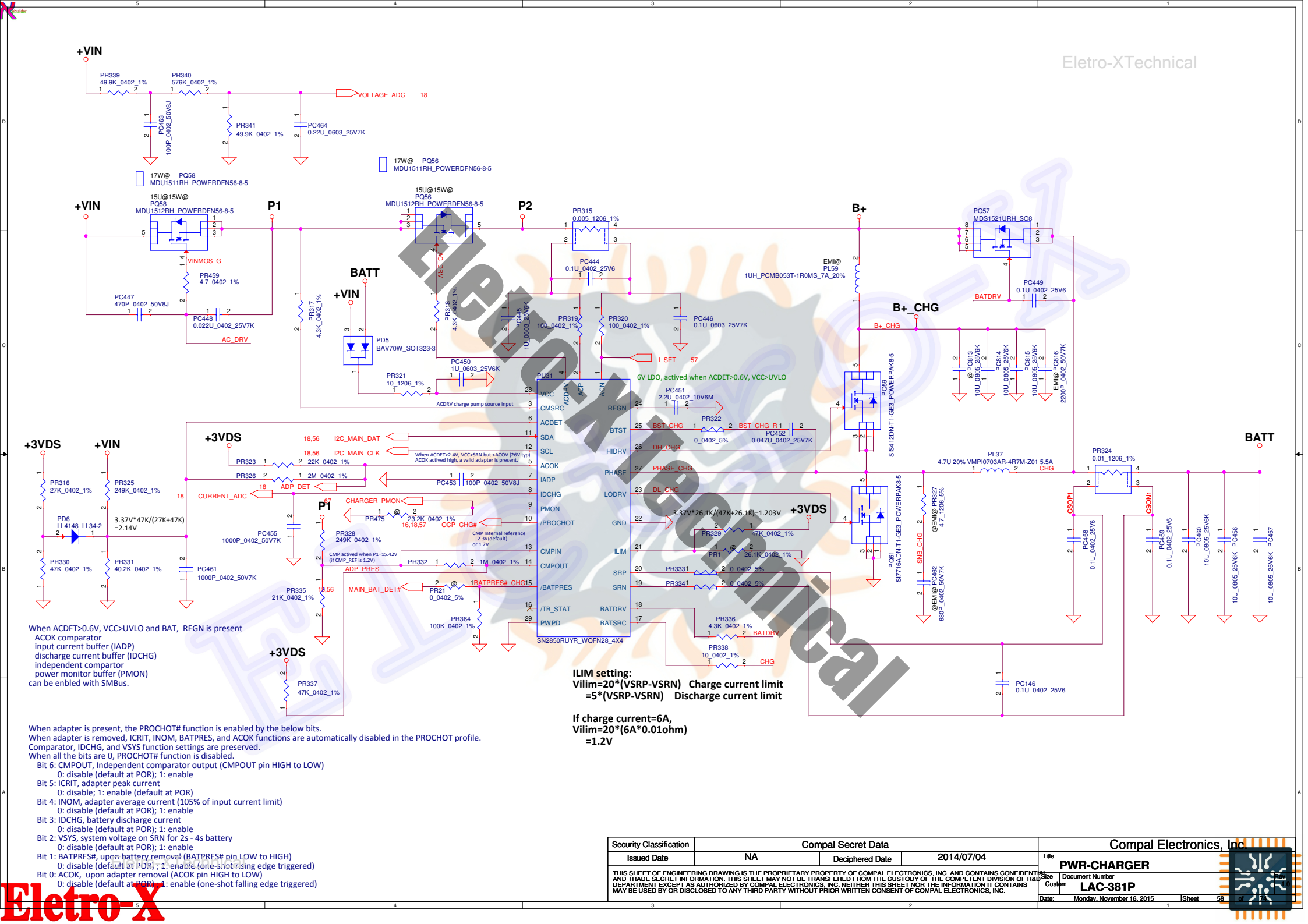
Date: Monday, November 16, 2015 | Sheet 56 of 80

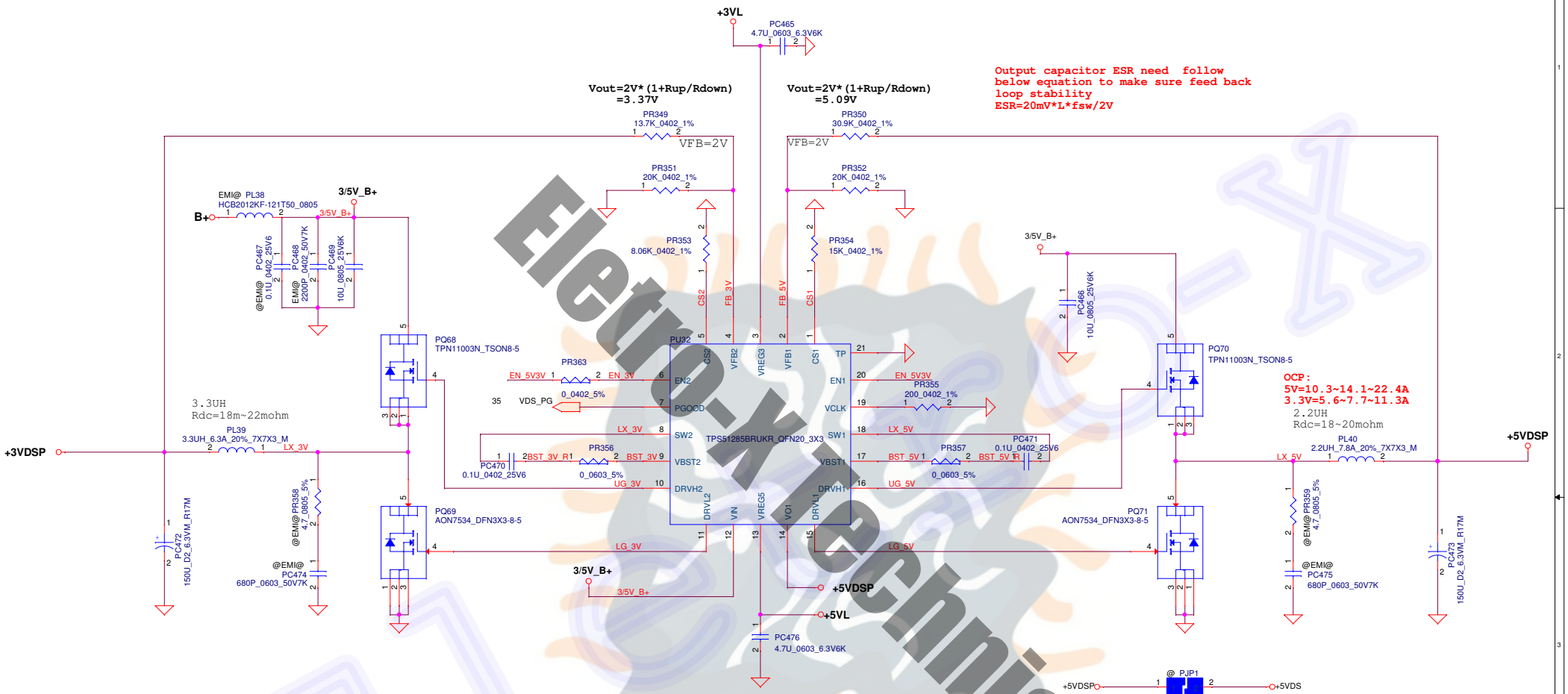


Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

Compal Electronics, Inc.

Title	PWR-ADP_OCP		
Size	Document Number		Rev
Custom	LA-B191P		1.0
Date:	Monday, November 16, 2015	Sheet	57 of 80





EN
Rising=1.6~0.3V

PR360 0_0402_5%

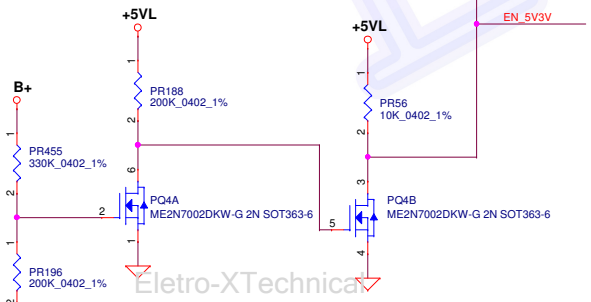
57 MAINPWR

OVP=Vout*(112.5%~117.5%)

OCP=Vtrip/Rdson+Iripple/2
Vtrip=Ics(min)*Rcs/8+1mV
Vcs=Ics*vcs should be in the range of 0.2~2V

Vout=VFB*(1+Rtop/Rbot)
VFB=2V

Vos=√SQU(Vomax)+L*SQU(I)/C)
CHOKE:4.7uH, DCR 35mOhm
Ploss=1.77W



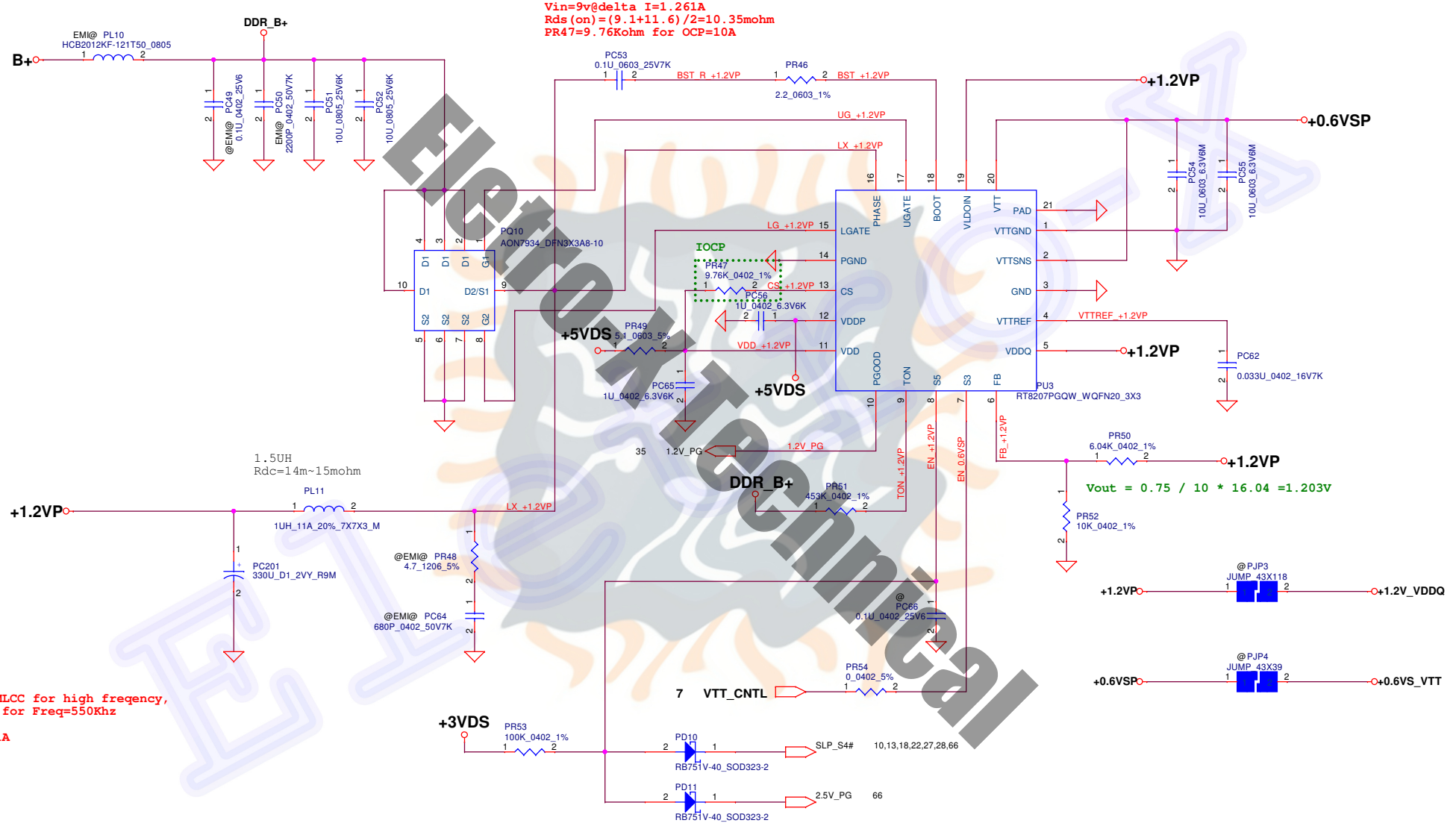
Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

Compal Electronics, Inc.

Title: PWR-3VDS/5VDS

Size: Custom | Document Number: LAC-381P | Rev: 1.0

Date: Monday, November 16, 2015 | Sheet 59 of 76



Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

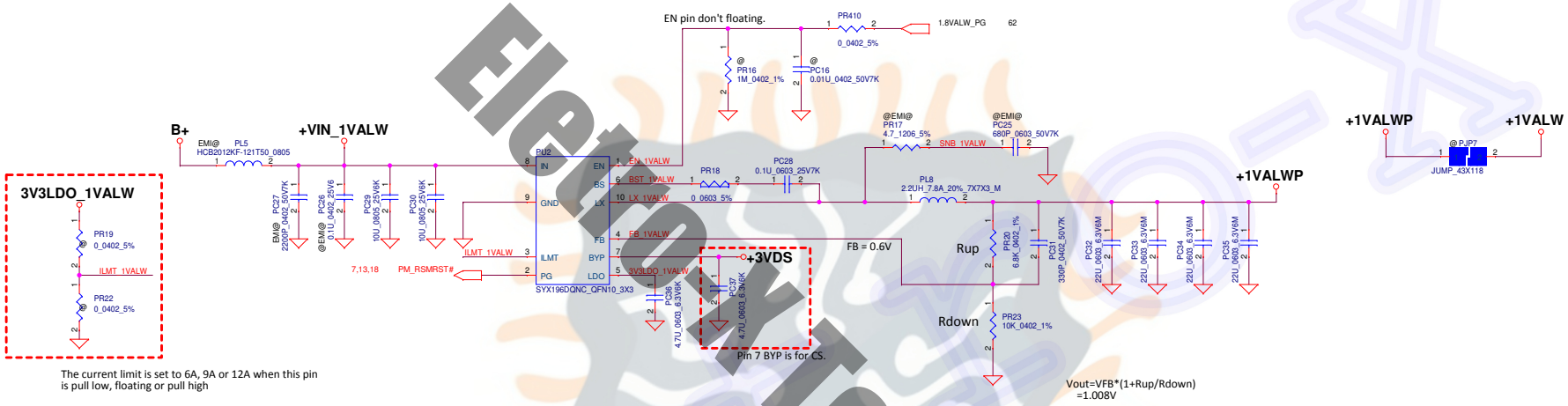
Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

Compal Electronics, Inc.

Title: PWR-1.0VALW

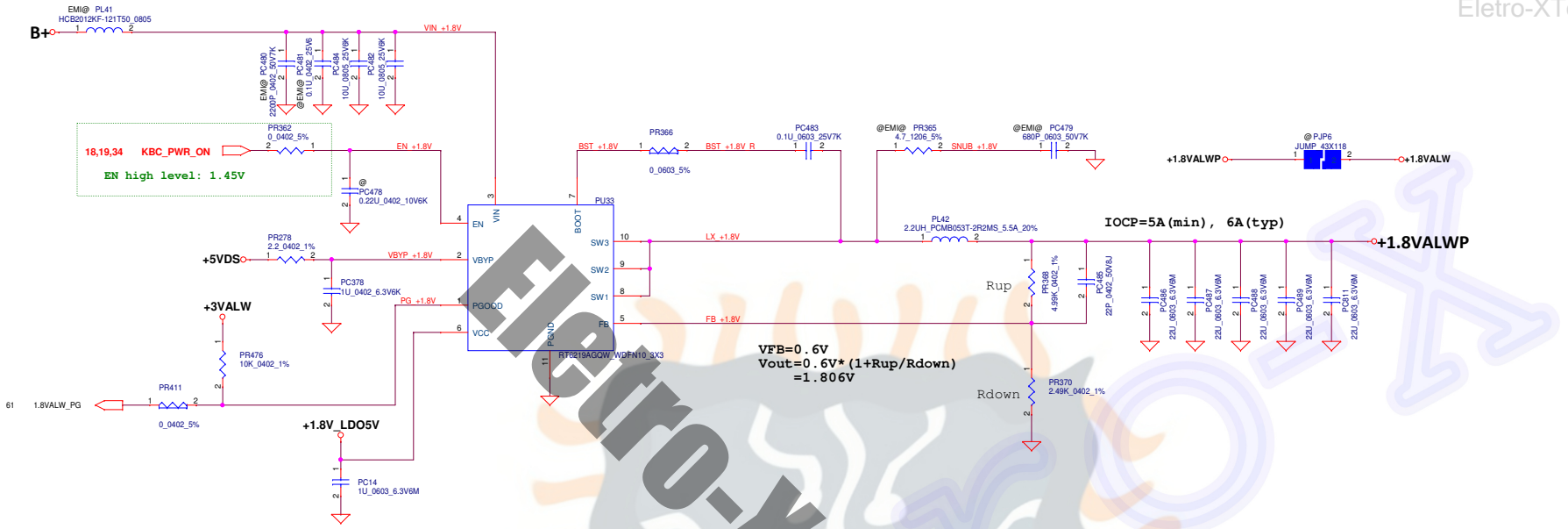
Size: Custom | Document Number: LAC-381P | Rev: 1.0

Date: Monday, November 16, 2015 | Sheet 60 of 80



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	NA	Deciphered Date 2014/07/04	Title PWR-1.0VALW
			Size C / Document Number LAC-381P / Rev 1.0
			Date: Monday, November 16, 2015 / Sheet 61 of 80



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	NA	Deciphered Date 2014/07/04	Title PWR-1.8VALW
			Size C / Document Number LAC-381P / Rev 1.0
			Date: Monday, November 16, 2015 / Sheet 62 of 80

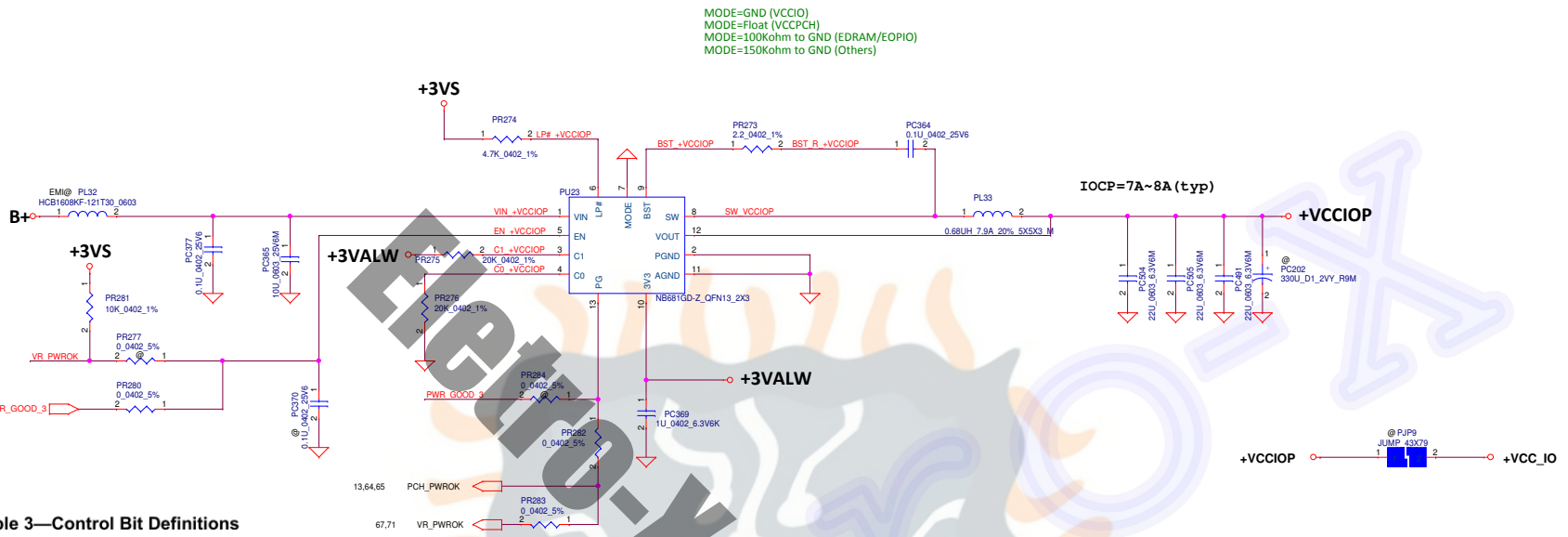


Table 3—Control Bit Definitions

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	NA	Deciphered Date 2014/07/04	Title PWR-VCCIO
			Size C / Document Number LAC-381P / Rev 1.0
			Date: Monday, November 16, 2015 / Sheet 63 of 80

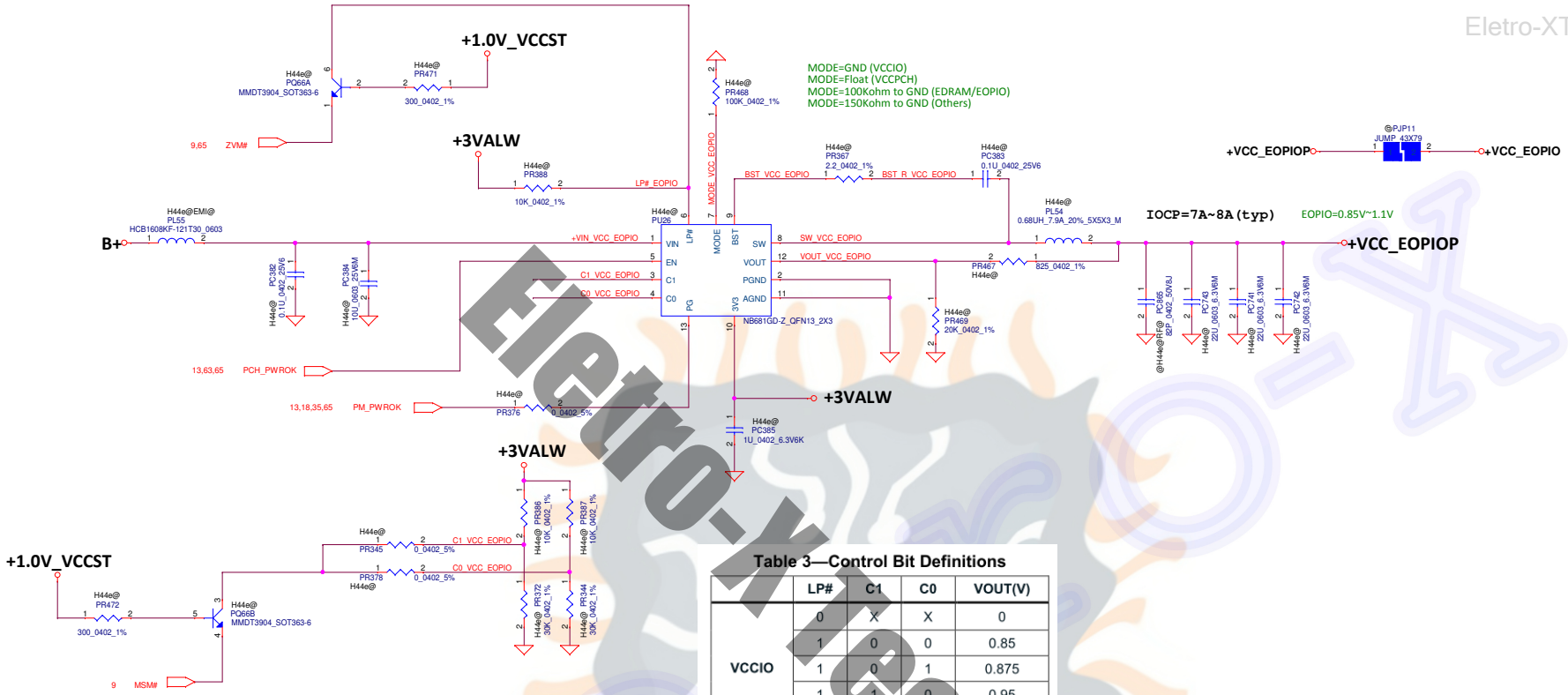


Table 3—Control Bit Definitions

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	NA	Deciphered Date 2014/07/04	Title PWR-VCC_EOPIO
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size C / Document Number LAC-381P / Rev 1.0
			Date: Monday, November 16, 2015 / Sheet 64 of 80

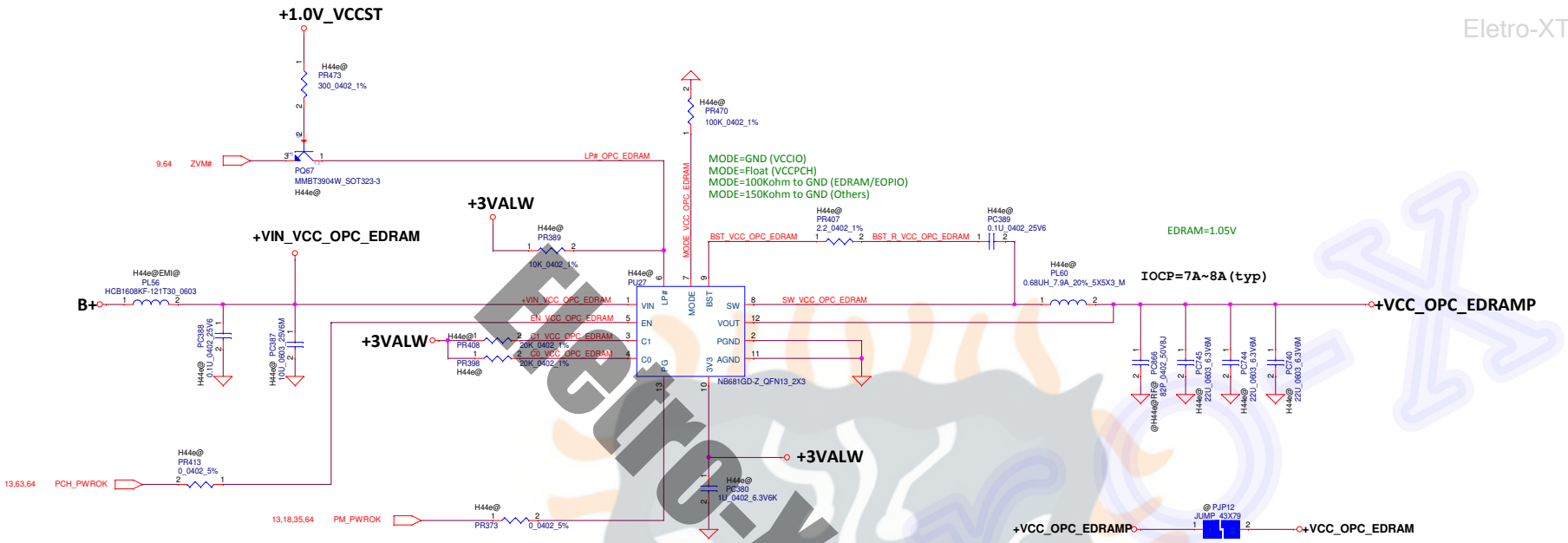
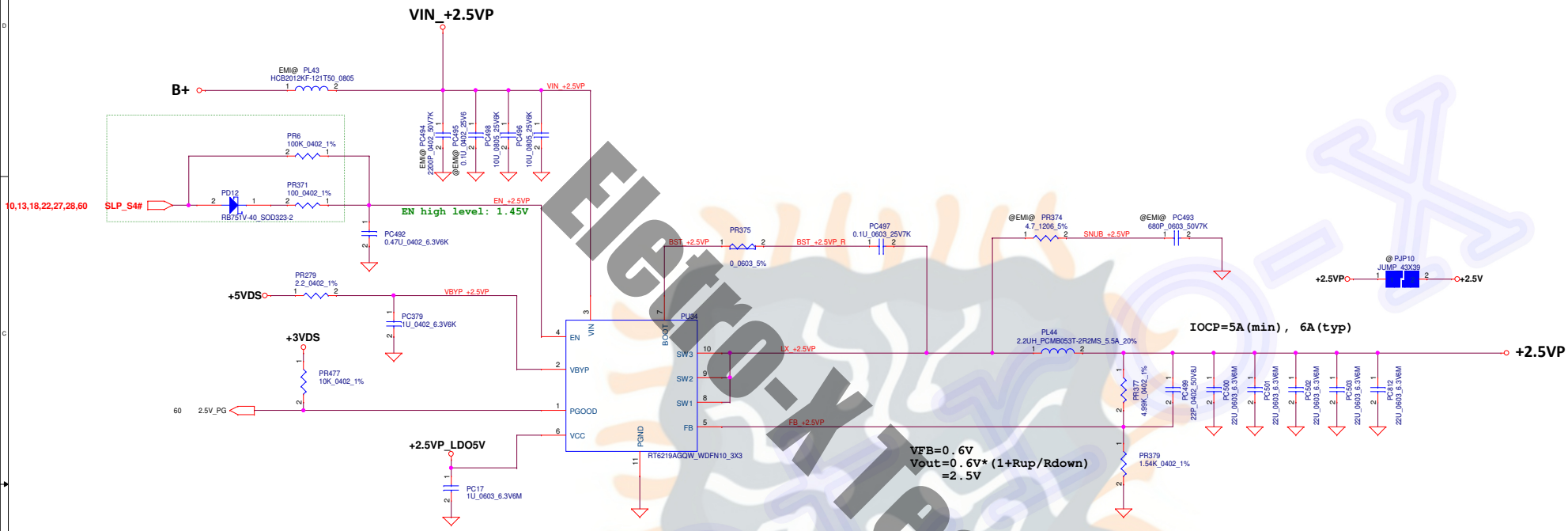


Table 3—Control Bit Definitions

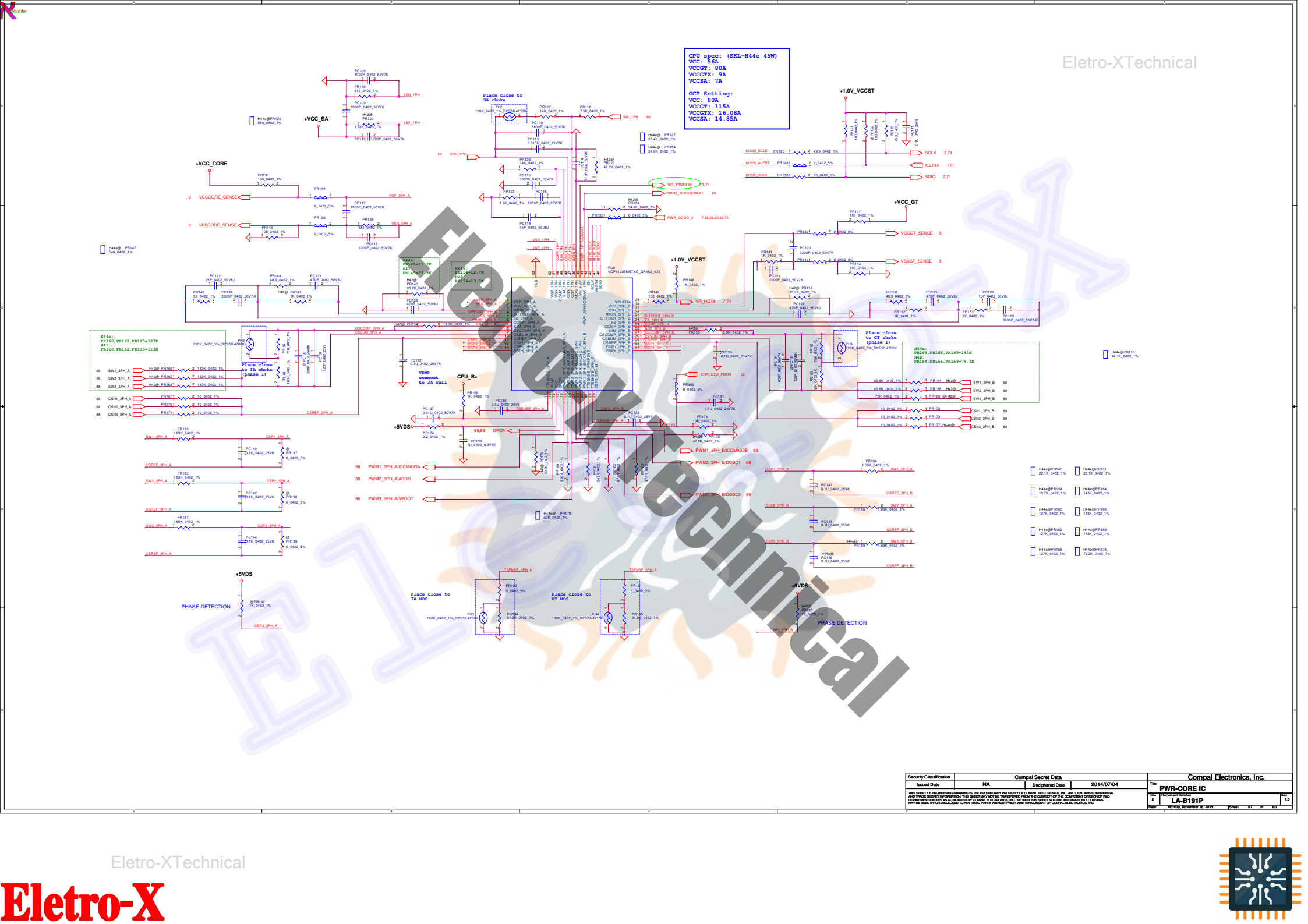
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	NA	Deciphered Date 2014/07/04	Title PWR-VCC_OPC_EDRAM
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size C / Document Number LAC-381P / Rev 1.0
			Date: Monday, November 16, 2015 / Sheet 65 of 80

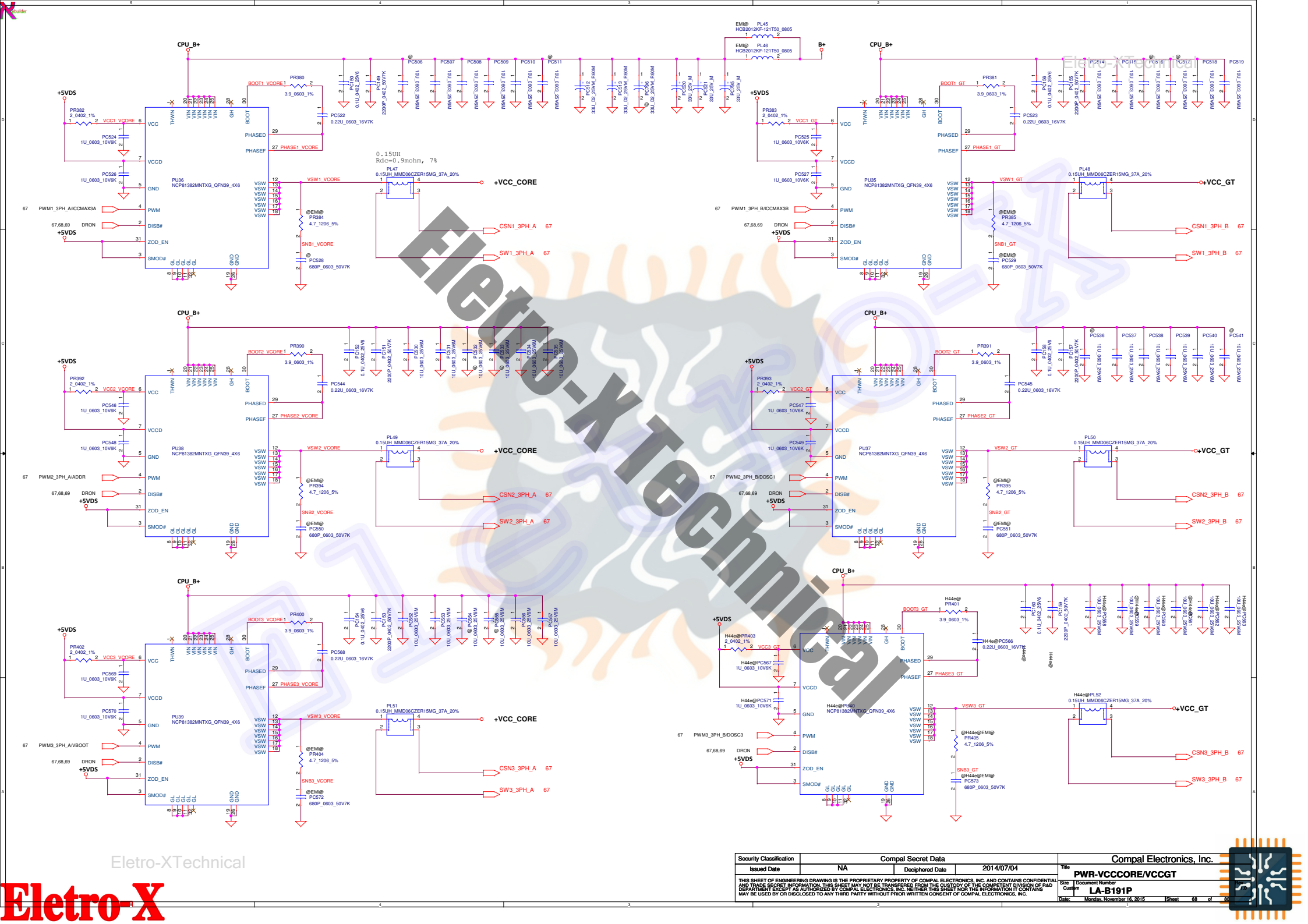


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	NA	Deciphered Date	2014/07/04

Title	PWR-VPP		
Size C	Document Number LAC-381P		Rev 1.0
Date: Monday, November 16, 2015	Sheet 66 of 80		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	NA	Deciphered Date	2014/07/04
Title: PWR-CORE IC			
Size: D	Document Number: LA-B191P		Rev: 1.0
Date: Monday, November 16, 2015	Sheet 67 of 80		



Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

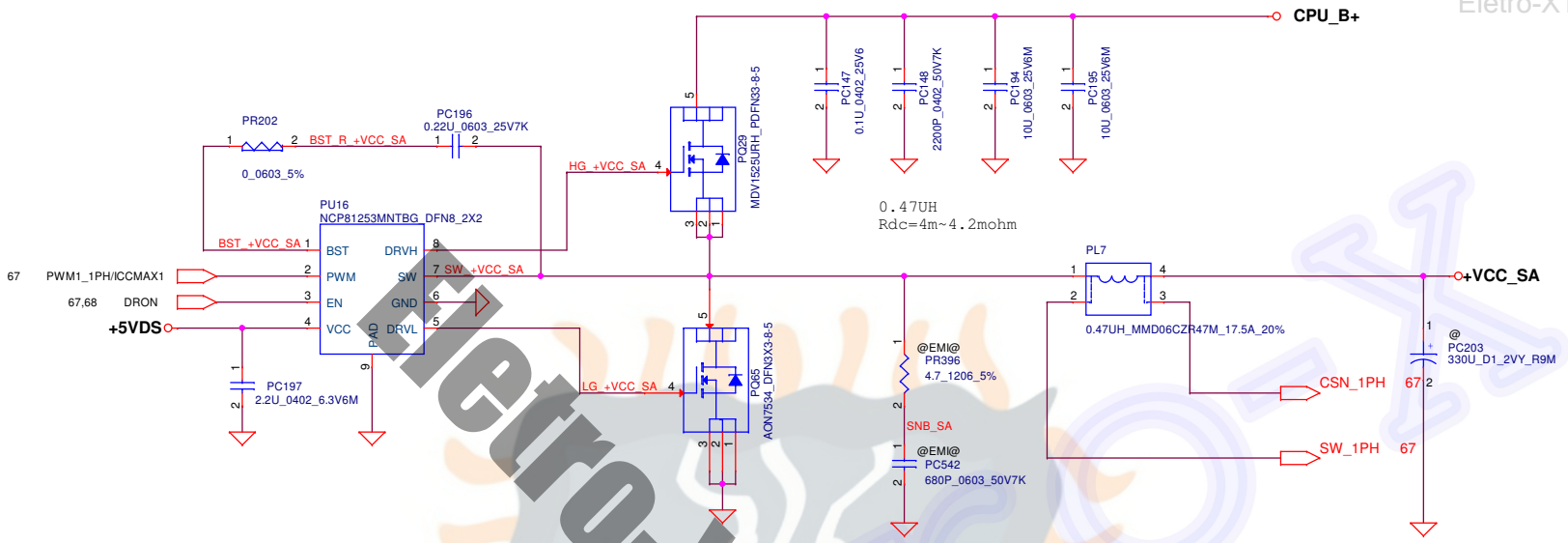
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: PWR-VCCCORE/VCCGT

Size: Custom | Document Number: LA-B191P | Rev: 1.0

Date: Monday, November 16, 2015 | Sheet 68 of 80



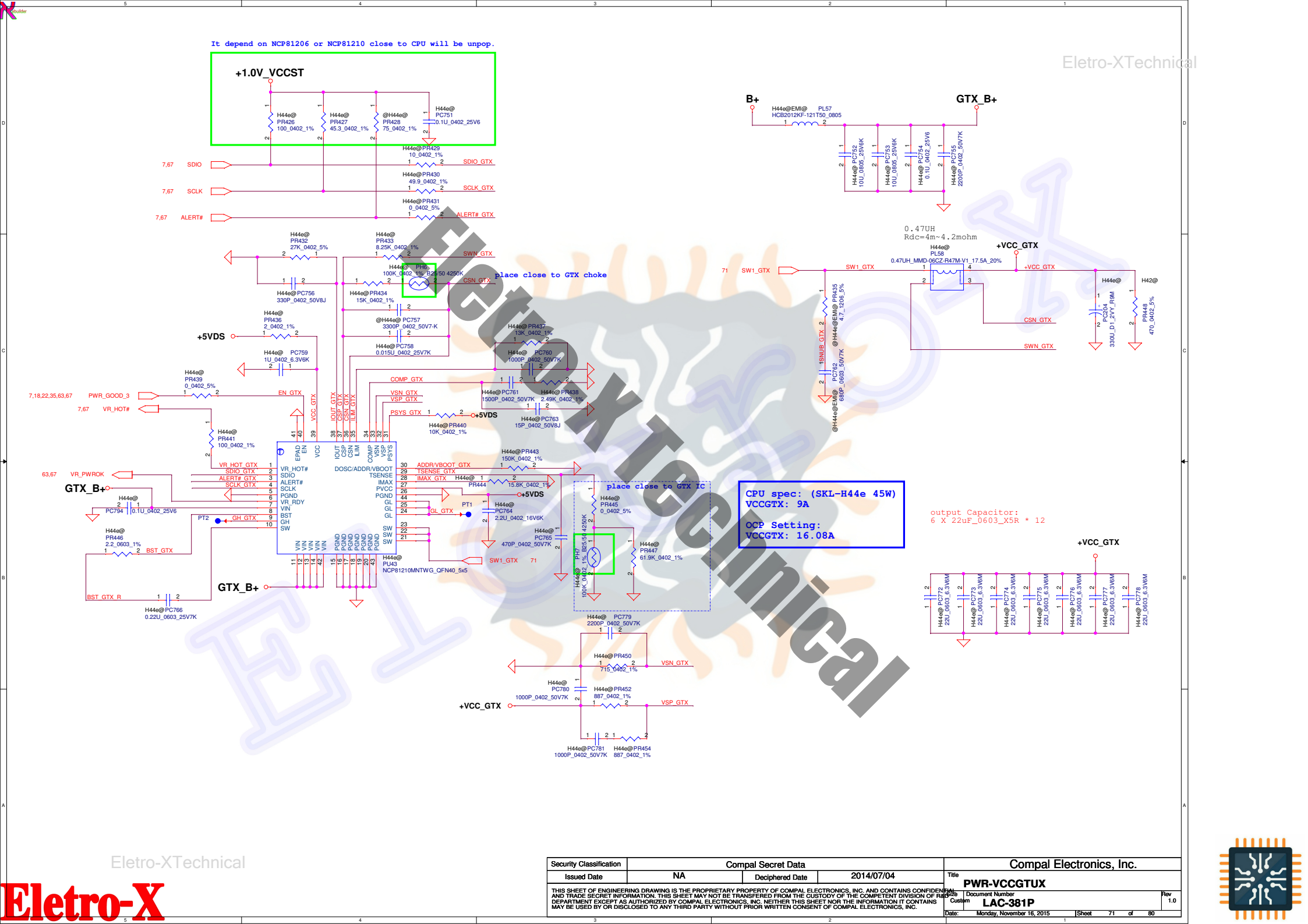
Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

Compal Electronics, Inc.

Title: PWR-VCCSA

Size: Custom | Document Number: LAC-381P | Rev: 1.0

Date: Monday, November 16, 2015 | Sheet 69 of 76



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	NA	Deciphered Date	2014/07/04
Title	PWR-VCCGTUX		
Size	Custom	Document Number	LAC-381P
Rev	1.0		
Date:	Monday, November 16, 2015	Sheet	71 of 80

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PWM-VID Spec and component Values

PWM-VID Spec	Config A	Config B	Config C
Vmin	0.6V	0.6V	0.65V
Vmax	1.2V	1.2V	1.15V
Vboot	0.875V	0.9V	0.9V
Voltage step	6.25mV	6.25mV	25mV
N of Voltage level	96	96	20
Rrefadj PR913	39K	20K	39K
Rref1 PR915	39K	20K	30K
Rboot PR930	1.5K	2K	3K
Rref2=PR914+PR904	30K	18K	24K
	1.5K	0	3K
Crefin PC940	1.5nf	2.7nf	1.8nf

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A
OCP Setting Current	42A	66A	54A	42A	42A	48A
Rocset （PR911）	6.98K	@	21K	6.98K	6.98K	6.98K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L
Polymer Cap 560U	4.5mohm	4.5mohm	4.5mohm	4.5mohm	4.5mohm	4.5mohm
Polymer Cap 330U	9mohm	9mohm	9mohm	9mohm	9mohm	9mohm
Or OSCON 560U	10mohm	10mohm	10mohm	10mohm	10mohm	10mohm
Or OSCON 390U	10mohm	10mohm	10mohm	10mohm	10mohm	10mohm

Module model information

NCP81172_V1A for IC portion
NCP81172_V1B for SW portion

Make sure PSI has been pulled high in HW circuit

PR931 = 40.2K ==>Fsw = 450KHz

Thermistor near MOSFET
trigger point 110 degree C.
To set a 100 degree C trigger
point please place PR926 5.68k.

To place PR933 PR934 close to GPU die sense pins

+GPU_CORE

VGA_B+

B+

+5VDS

+3VS

VGS=4.5V, ID=20A
Rds(on)=13.4 Max

VGS=4.5 V, ID=21A
Rds(on)=3.5 Max

7x7 DCR=0.98+/-5%
Heat Rating Current=28A
Saturation Current=28A

NCP81172MNTXG_QFN24_4X4

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

Compal Electronics, Inc.

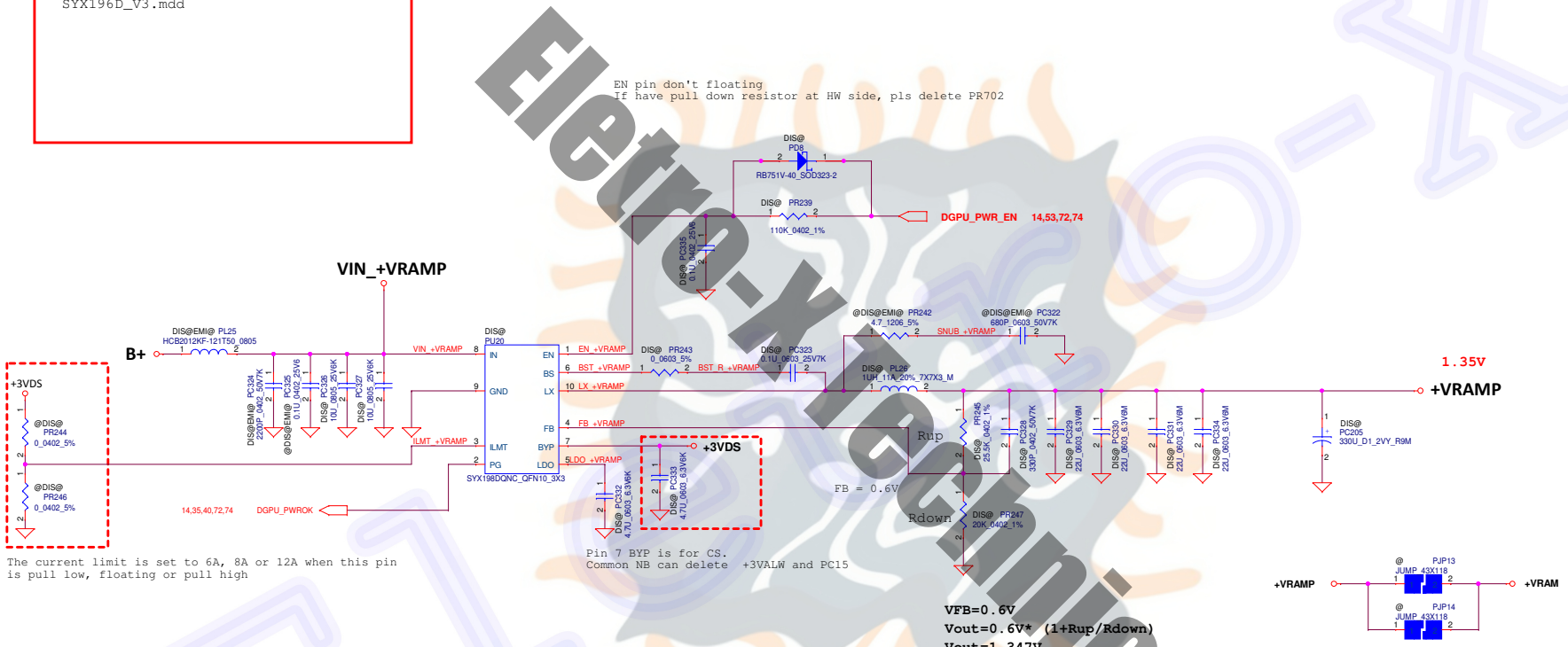
Title: +VGA_COREP

Size: Custom | Document Number: Common | Rev: 1.0

Date: | Sheet 72 of 80

Module model information

SYX196D_V3.mdd



Function Field :
+1VALW controller - 35.5
Rest of support elements - 35.6

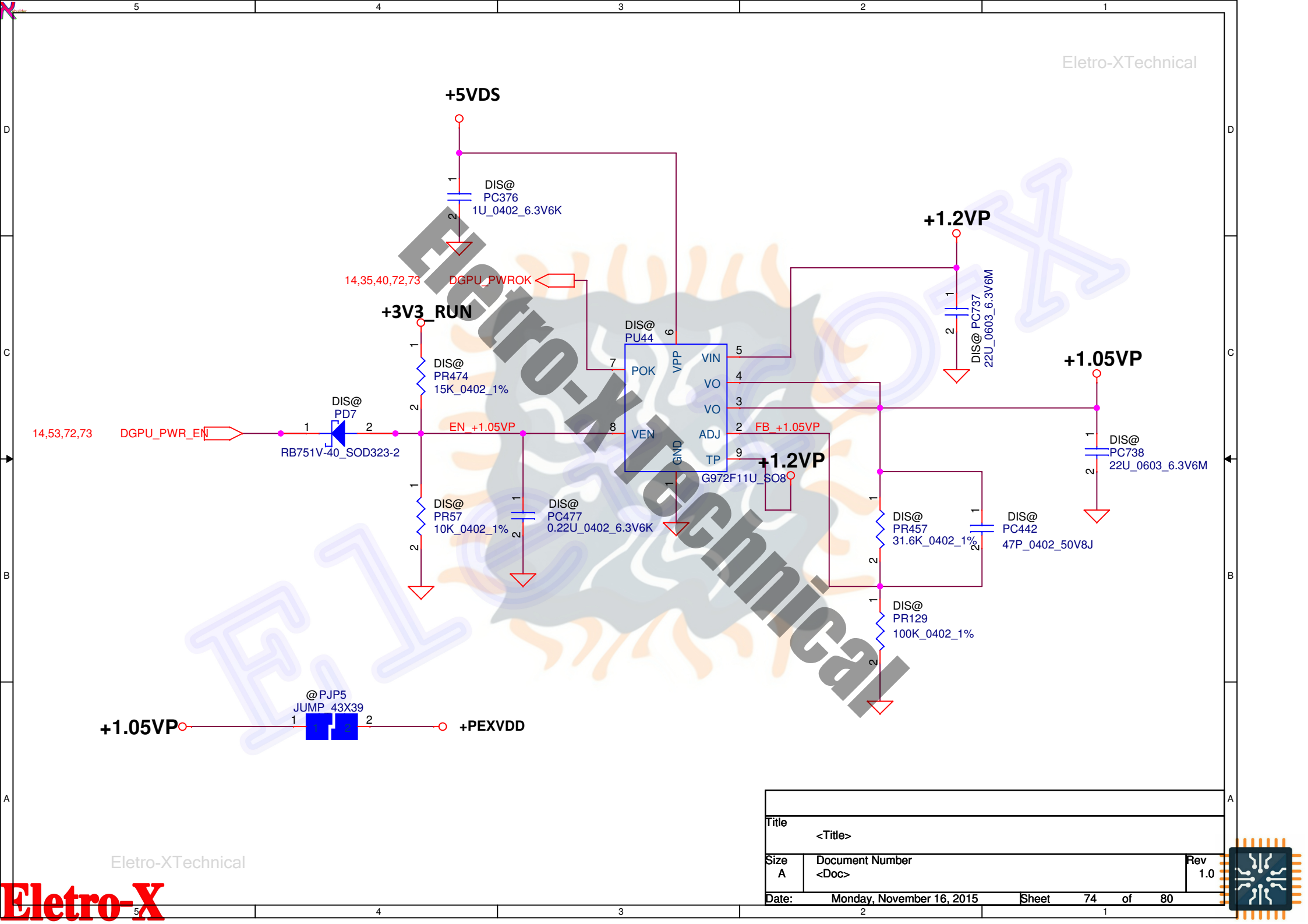
Security Classification	Compal Secret Data		
Issued Date	2014/07/31	Deciphered Date	2015/12/31

Compal Electronics, Inc.

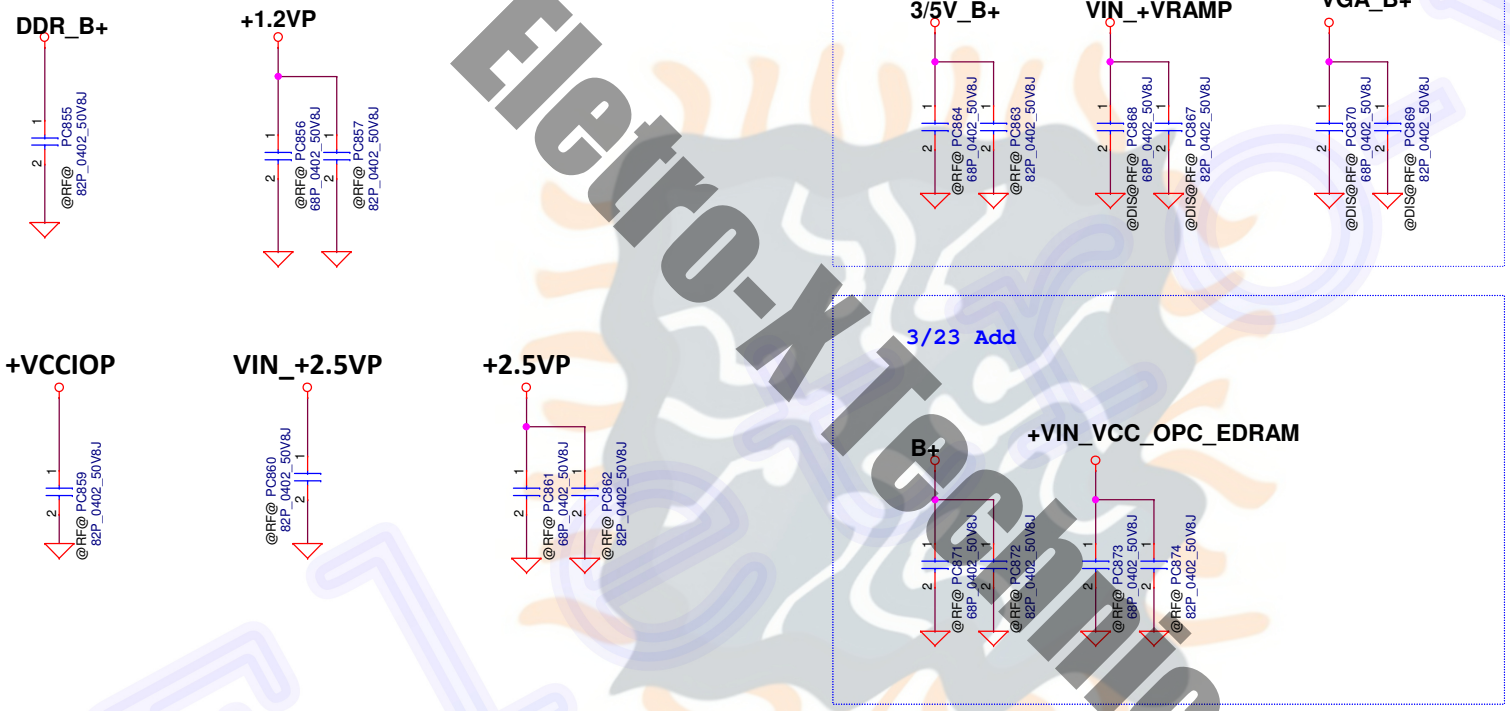
Title: +1VALWP

Size: C | Document Number: AAX05 | Rev: 1.0

Date: Monday, November 16, 2015 | Sheet 73 of 80



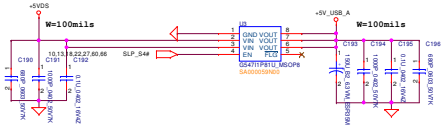
Title	<Title>	
Size A	Document Number <Doc>	Rev 1.0
Date: Monday, November 16, 2015	Sheet 74 of 80	

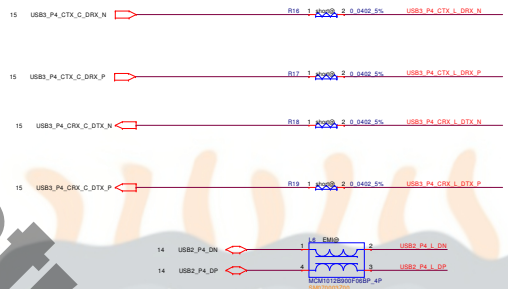


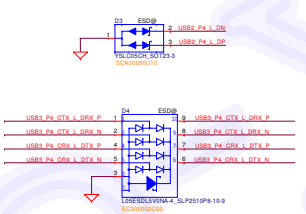
Security Classification	Compal Secret Data		
Issued Date	2014/07/31	Deciphered Date	2015/12/31

Title	RF caps		
Size B	Document Number AAX05		Rev 1.0
Date: Monday, November 16, 2015	Sheet 75 of 80		

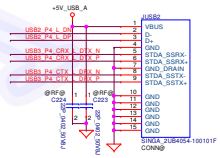
MB_USB 3.0 Without charger function

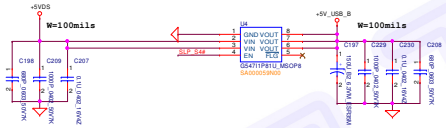


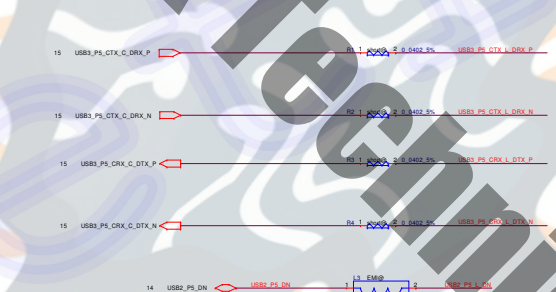


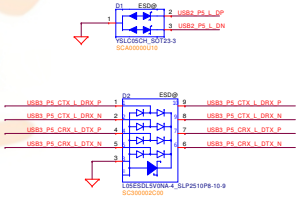


USB3.0 / USB2.0 Port4 (Left Side)

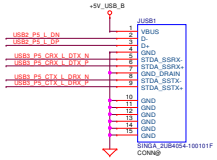




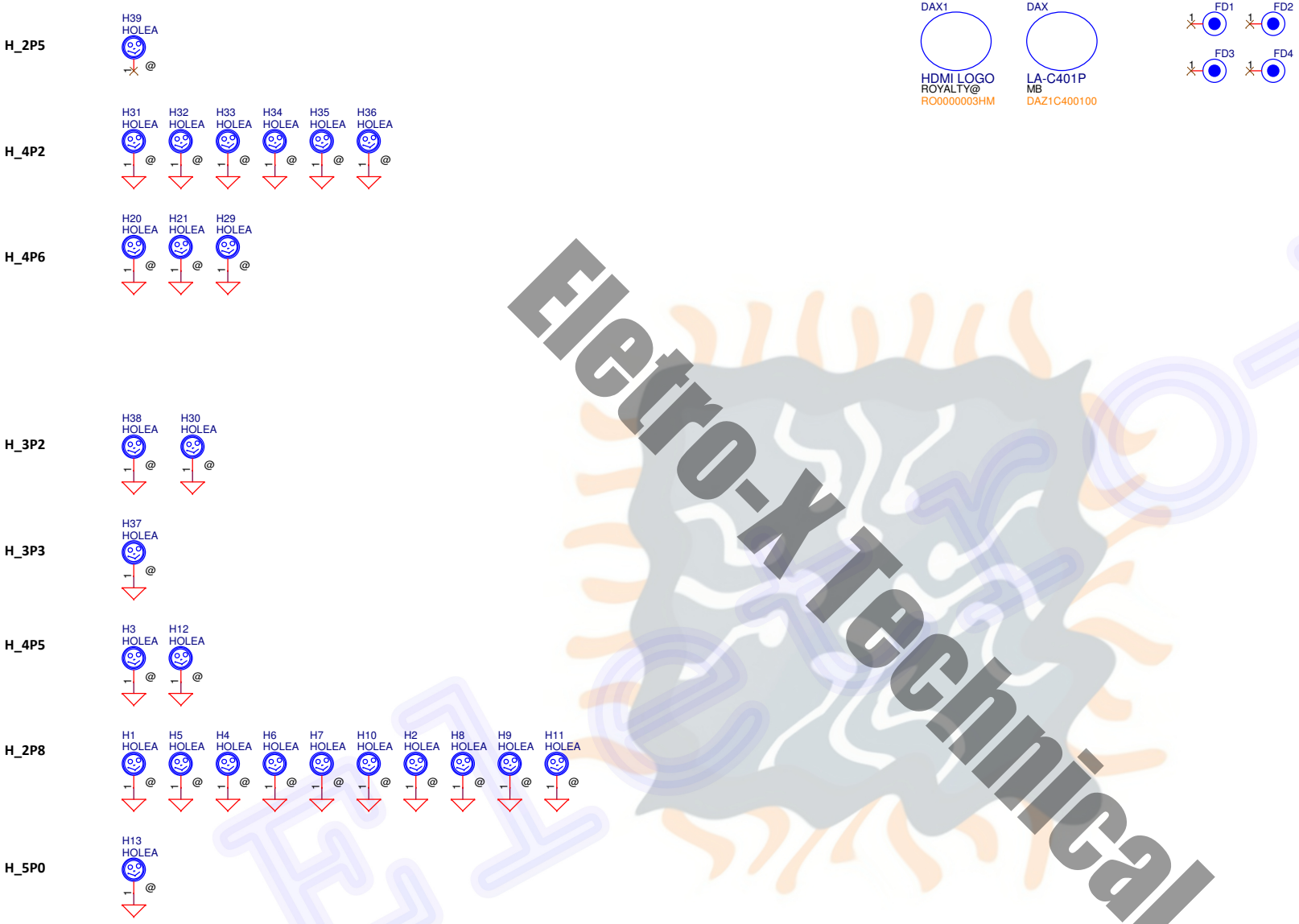




USB3.0 / USB2.0 Port5 (Right Side)

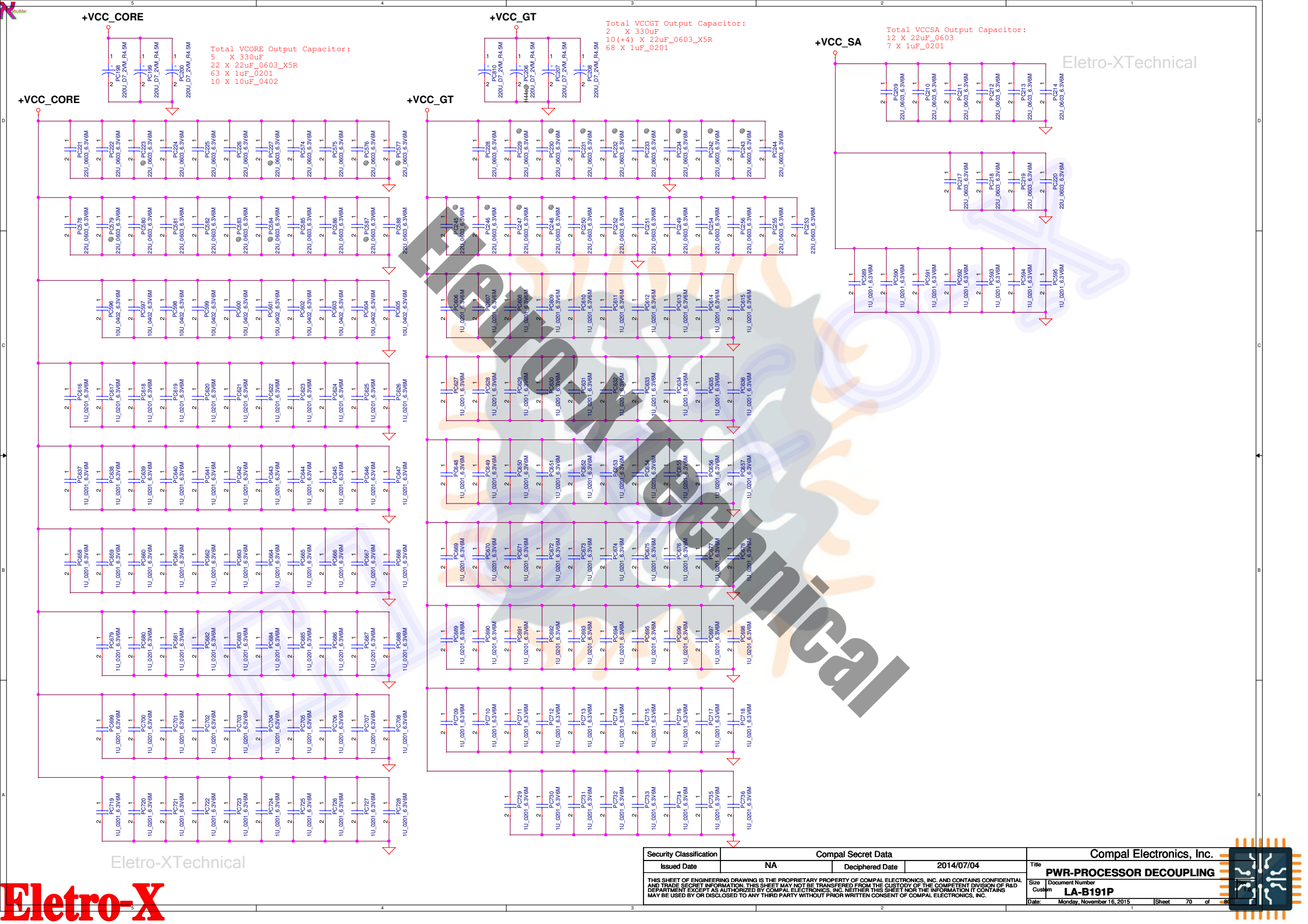


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/05/19	Deciphered Date 2015/12/31	Title: USB 3.0 IO port & repeater
			Size: D; Document Number: LA-C401P; Rev: 1.0
			Date: Monday, November 16, 2015; Sheet 28 of 60



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.		
Title: HOLE/PCB		
Size: B	Document Number: LA-C401P	Rev: 1.0
Date: Monday, November 16, 2015	Sheet 38 of 80	



Security Classification	Compal Secret Data		
Issued Date	NA	Deciphered Date	2014/07/04

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: PWR-PROCESSOR DECOUPLING

Size: Custom | Document Number: LA-B191P | Rev: 1.0

Date: Monday, November 16, 2015 | Sheet 70 of 90

Install below X63 level BOM structure for ver. 0.1

Un-pop parts BOM structure

@ : reserve, un-pop on all sku

@DIS@: Discrete sku parts, un-pop
@DIS@EMI@ : Discrete sku parts and belong to EMI parts, un-pop
@EMI@ : EMI parts, un-pop
@H44e@ : CPU H44e sku parts, un-pop
@H44e@EMI@ : CPU H44e sku parts and belong to EMI parts, un-pop

Pop parts BOM structure

DIS@: Discrete sku parts, pop
DIS@EMI@ : Discrete sku parts and belong to EMI parts, pop
EMI@ : EMI parts, pop
ESD@ : ESD parts, pop

H42@ : pop on CPU H42 sku only
H44e@ : pop on CPU H44e sku only
H44e@EMI@ : EMI parts, pop on CPU H44e sku only

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	NA	Deciphered Date 2014/07/04	Title: PWR-BOM STRUCTURE RULE
Size: B	Document Number: LA-B191P		Rev: 1.0
Date: Monday, November 16, 2015	Sheet 54 of 80		

Item	Reason for change	PG#	Modify List	Date	Phase
1	Modified schematic-15U_09-22C for 15W series.		1. Added charger discharge MOSFET PQ60. 2. Changed the EMI input cap of CPU core to SF000004M00. 3. Reserved DCIN MOSFET PQ102.	2014/09/23	DB0
2	Fine tune Vcore compensation	67	1. Change PR120 from 1.4k ohm to 1.69k ohm 2. Change PC110 from 1000pF to 3300pF 3. Change PC116 from 0.015uF to 8200pF 4. Change PR127 from 28.7k ohm to 48.7k ohm 5. Change PR145 from 22.6k ohm to 23.2k ohm 6. Change PC131 from 1000pF to 820pF 7. Change PR169 BOM Structure from H42@ to @H42@ 8. Change PR177 BOM Structure to @H42@ 9. Change PR164 from 75k ohm to 80.6k ohm 10. Change PR166 from 75k ohm to 80.6k ohm 11. Change PR189 BOM Structure to @H42@ 12. Change PC145 BOM Structure to @H42@ 13. Change PR193 BOM Structure from @ to H44e@	2015/01/05	DB1
3	Change Charger Pmon connection as HP request		1. Delete PC454 2. Reserve PR475, 23.2k ohm	2015/03/16	SI1
4	Fine tune Vcore compensation		1. Reserve PC161 & PR369 2. Un-pop PR122 3. Un-pop PR197, PR198, PR199	2015/03/16	SI1
5	HP request		1. On p60, change SLP_S4# to 2.5V_PG at PR53-1 and change PGGOD+1.2VP to 1.2V_PG at PU3-10, and remove PU4, PR91 and PR156. 2. On p61, change KBC_PWR_ON to 1.8VALW_PG at PR410-1, and change PR410 = 0 ohm and uninstall PC16. 3. On p62, Change PM_RSMRST# to 1.8VALW_PG, and add a 10k-R (pulled up to +3VALW) at PU33-1. 4. On p66, add a 10k-R (pulled up to +3VDS) at PU34-1 for 2.5V_PG.	2015/03/18	SI1
6	1.Change press button force shutdown circuit 2.Update battery detection connection		1.Change PR461 pin1 from +5VL to +5VDS 2.Delete PR364, Add PR24, PR21, PR364	2015/05/08	SI2
7	1. For Pmon setting 2. For thermal request 2. For +1.8V leakage issue		1.Change PR176 from 20k to 40.2k 2.Change PL35 & PL36 to Z=3mm 3.Change PR368 to 4.99k ohm and PR370 to 2.49k ohm	2015/06/03	SI2
8	1. Add GT phase3 compensation		1. Change PR189, PC145, PR177 to H44e@	2015/06/28	PV
9	1. Solve SN2850 Pmon accuracy issue		1. Change PR333, PR334 from 10 ohm to 0 ohm	2015/07/16	PV
10	1. For PU44 2nd source compatibility		1. Change PU44 TP pin from GND to VIN	2015/07/16	PV
11	1. Add Psys function		1. Install PC161 2. Change PR176 from 40.2k ohm to 13k ohm	2015/07/20	PV
12	Change OTP setting		1. Change PR111 from 14.3 kohm to 19.1kohm	2015/07/29	PV
13	Change VR H4+4e Ilim setting		1. Change PR155 from 16.9 kohm to 14.7kohm 2. Change PR151 from 21 kohm to 22.1kohm 3. Change PR175 from 84.5 kohm to 73.2kohm	2015/07/29	PV
14	1). During power up, delay +1.2V (VDDQ) powerup until +2.5V (VPP) is ready.	60	1. Change PR53 from 0 ohm to 100k ohm 2. Add PD10, PD11	2015/09/04	PVR
15	2). During power off, delay +2.5V (VPP) power off later than VDDQ via RC delay.	66	1. Change PR371 from 0 ohm to 100 ohm 2. Add PR6 100k ohm 3. Add PD12 4. Change PR472 from 0.22uF to 0.47uF and instal	2015/09/04	PVR
16	Fine tune power reset RC to meet 11~12 seconds	57	1. Change PR461 from 560k ohm to 1M ohm 2. Add PR462, PR463 931k ohm	2015/09/04	PVR
17	Change 0 ohm to short pad		PR18, PR128, PR132, PR135, PR136, PR139, PR142, PR369, PR159, PR202, PR322, PR333, PR334, PR356, PR357, PR360, PR363, PR411, PR366, PR375	2015/09/04	PVR
18	Fine tune power reset RC to meet 11~12 seconds	58	1. Change PR460 from 680k ohm to 649k ohm 2. Add PR464 34k_0402	2015/09/10	PVR
19	HP request	64	1. Change PR372, PR344 from 10k ohm to 30k ohm	2015/09/10	PVR
20	Fine tune CPU compensation for 4+4e	67	1. Change PR145 from 23.7k ohm to 22.1k ohm 2. Change PR154 from 12.7k ohm to 13.7k ohm 3. Change PR147 from 1k ohm to 549 ohm 4. Change PR179 from 52.3k ohm to 59k ohm	2015/09/14	PVR
21	Fine tune GTX compensation for 4+4e	71	1. Change PR432 from 43k ohm to 27k ohm 2. Change PR444 from 10k ohm to 15.8k ohm	2015/09/14	PVR
22	Fine tune CPU compensation for 4+4e	67	1. Change PR120 from 1.27k ohm to 866 ohm 2. Change PR127 from 48.7k ohm to 63.4k ohm 3. Change PR134 from 34.8k ohm to 24.9k ohm	2015/09/15	PVR
23	Change PQ19 pin2 net name		Change PQ19 pin2 net name from ON/OFFBTN_KBC# to ON/OFFBTN#		MV

Security Classification	Compal Secret Data		
Issued Date	2011/03/10	Deciphered Date	2009/06/22

Compal Electronics, Inc.		
Title: PWR-PIR		
Size:	Document Number:	Rev: 1.0
Date: Monday, November 16, 2015	Sheet 37 of 85	