B36H4-AD

Rev:1.1

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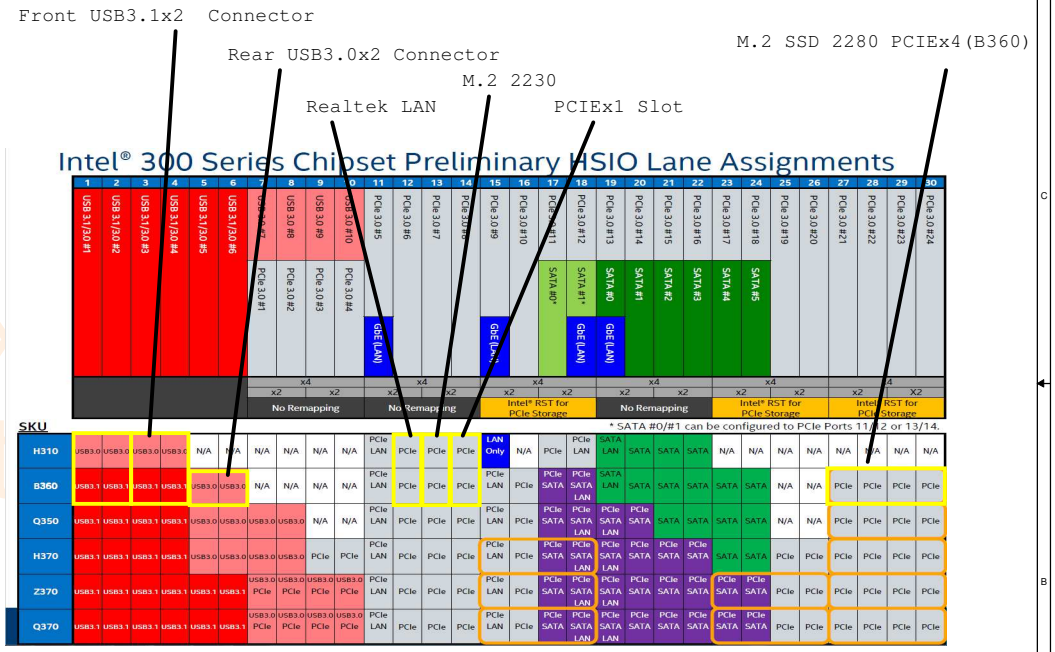

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Design Guide : 571264_CFL_S_PDG_Rev1p6
EDS PCH : 571182_CNL_PCH_H_EDS_Vol_1_Rev_1_1
EDS CPU : 570805_CFL_EDS_Vol1___Rev1.5

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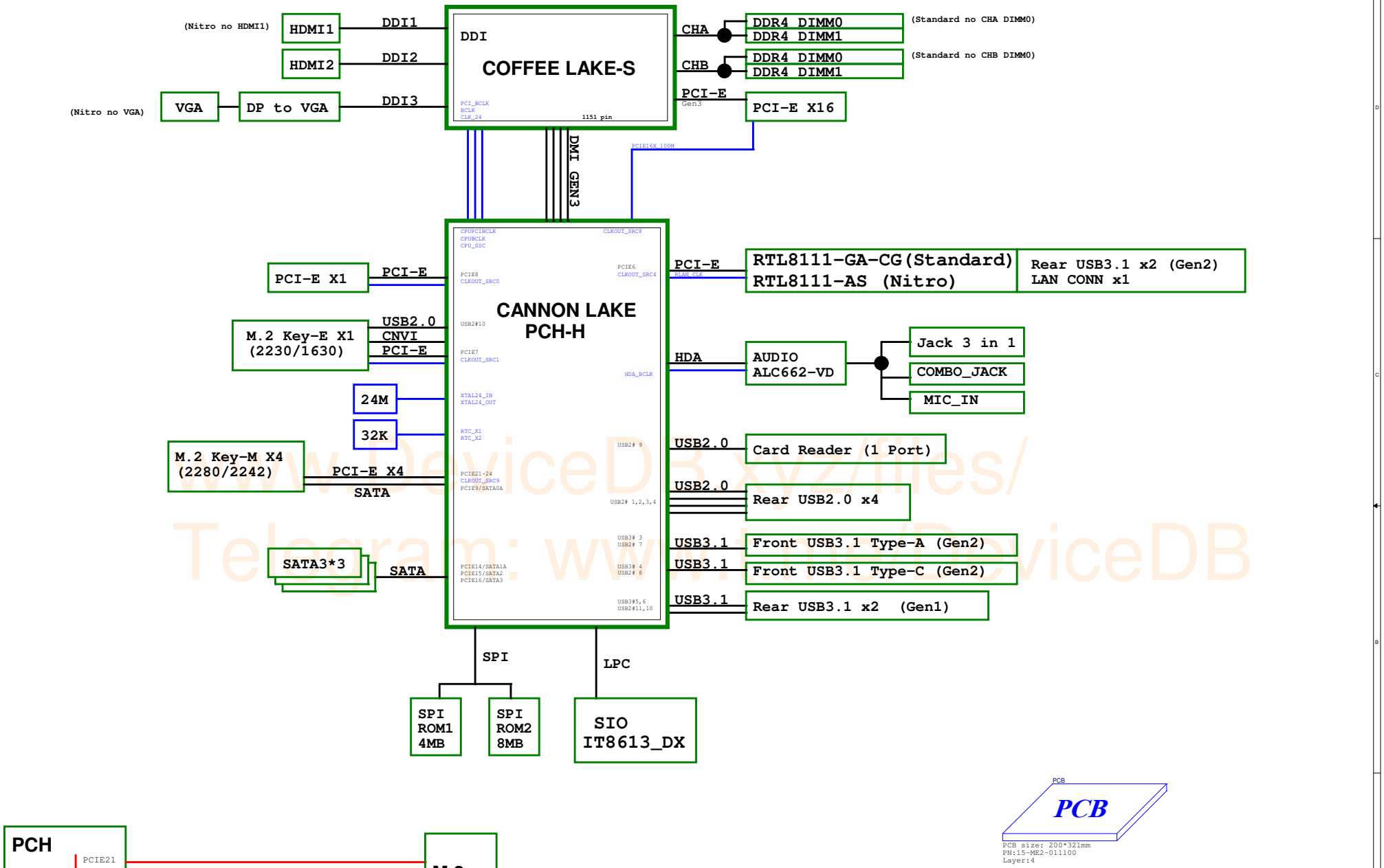

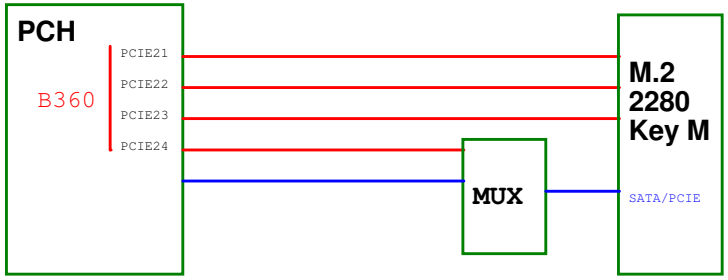

PCB size: 200*321mm
PN:15-ME2-011100
Layer:4

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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPP_F16	3VSB	GPP_F16 H: USB power enable	GPI
GPP_E8	VCC3	SATALED_L	SATA_LED#
GPP_A1	N/A	LPC_LAD0	LAD0
GPP_A2	N/A	LPC_LAD1	LAD1
GPP_A3	N/A	LPC_LAD2	LAD2
GPP_A4	N/A	LPC_LAD3	LAD3
GPP_G16	3VSB	LPC_PME_L	GPI
GPP_A0	VCC3	KBRST_L_RC	RCIN#
GPP_A6	VCC3	SERIRQ	SERIRQ
GPP_A7	3VSB	PIRQA_L	PIRQA_L
GPP_A9	N/A	PCH_SIO_24M	CLKOUT_LPC0
GPP_A10	N/A	SIO_LPC_24M_R	CLKOUT_LPC1
GPP_E4	VCC3	DEVSLP0	GPI
GPP_F5	3VSB	BOM option	GPI
GPP_D6	3VSB	MODEM_CLKREQ	MODEM_CLKREQ
GPP_D5	3VSB	CNV_RF_RESET	CNV_RF_RESET
GPD5	ATX_3VSB	SLP_S4_L	SLP_S4#
GPD10	ATX_3VSB	GPD10 (ME disabe by SW)	SLP_S5#
GPD0	ATX_3VSB	BATLOW_L	BATLOW#
GPD2	ATX_3VSB	LAN_WAKE	LAN_WAKE#
GPP_I11	3VSB	H_SKTOCC_L	GPI
GPP_I12	3VSB	WLAN_DISABLE_L	GPI
GPP_J0	V1P8A	CNV_PA_BLANKING	CNV_PA_BLA NKING
GPP_J4	V1P8A	CNV_BRI_DT	CNV_BRI_DT
GPP_J5	V1P8A	CNV_BRI_RSP	CNV_BRI_RSP
GPP_J6	V1P8A	CNV_RGI_DT	CNV_RGI_DT
GPP_J7	V1P8A	CNV_RGI_RSP	CNV_RGI_RSP
GPP_J8	V1P8A	GPP_J8_CNV_MFUART2_RX	CNV_MFUART2_RXD
GPP_J9	V1P8A	GPP_J8_CNV_MFUART2_RX	CNV_MFUART2_TXD
GPP_B5	VCC3	PCIE1X_CLKREQ_L_R	SRCCLKREQ0#
GPP_B6	VCC3	M2CLK_REQ1_L	SRCCLKREQ1#
GPP_B9	VCC3	RLAN_CLKREQ	SRCCLKREQ4#
GPP_H2	VCC3	PCIE16X_CLKREQ_L_R	SRCCLKREQ8#
GPP_H3	VCC3	M2_2280_CLKREQ9_L	SRCCLKREQ9#
GPP_I0	N/A	DDPB_HPD0	GPI
GPP_I1	N/A	DDPB_HPD1	GPI
GPP_I2	N/A	DDPB_HPD2	GPI
GPP_K16	VCC3	LPC_PME_L	GPI
GPP_E7	VCC3	GPP_E7_THERM	GPI
GPP_B3	3VSB	BT_DISABLE_L	GPI
GPP_H13	3VSB	GPP_H13 (ACER reserved GPIO)	GPI
GPP_H14	3VSB	GPP_H14 (ACER reserved GPIO)	GPI
GPP_H18	3VSB	BOM option	GPI

Interrupt mapping

Function	INT#port	PCIE*1 port	Device
SATA		NA	SATA3.0
RLAN		Port6	RTL8111GA
M.2 WLAN		Port7	WLAN Card
M.2 SSD		Port21/22/23/24	M.2 SSD Card
PCIEX1		Port8	PCIEx1 Slot

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP22	DIMM_5VDUAL	SIO_LED1	PCH_D0B
GP21	DIMM_5VDUAL	SIO_LED0	GP21
GP43	ATX_3VSB	LAN_PWR_CTRL	SST
GP31	3VS	GPP_E7_THERM	SST

SIO Strap

	Symbol	Value	Description
JP1 Pin-24	DSW_EUP_SEL	1	EUP
		0	DSW
JP2 Pin-56	WDT_EN	1	Disable WDT to reset PWROK
		0	Enable WDT to reset PWROK
JP3 Pin-58	FAN_CTL_SEL	1	EC Index 63h/73h/7B/A3 is 80h
		0	EC Index 63h/73h/7B/A3 is 00h
JP4 Pin-60	K8PWR_EN	1	Disable K8 Power Sequence
		0	Enable K8 Power Sequence

PCH_CPU-Strap

Pin Name	Usage	Default Status
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted	1 = (Default) Normal Operation
CFG1	CFG[1]: Reserved configuration lane	
CFG2:5:6	CFG[2]:1 = Normal operation CFG[6:5]:11 = 1 x16 PCI Express	Normal operation PCIE16X
CFG3	CFG[3]: Reserved configuration lane.	
CFG4	CFG[4]: eDP disable :	eDP Enable
CFG7	CFG[7]: PEG Training	1 = (default) PEG Train immediately following RESET# de assertion.
CFG19:8	CFG[19:8]:Reserved configuration lanes.	
SPKR/GPP_B14	Top Swap Override	0 =Disable "Top Swap" mode. (Default)
GSPI0_MOSI/GPP_B18	No Reboot	0 =Disable "No Reboot" mode
SMBALERT#/GPP_C2	TLS Confidentiality	1 =EnableIntel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS
GSPI1_MOSI/GPP_B22	Boot BIOS Strap Bit BBS	0=SPI
SML0ALERT#/GPP_C5	eSPI or LPC	0 =LPCIs selected for SIO.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 =Enable security measures defined in the Flash Descriptor.(default) 1 =Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
GPP_J4/CNV_BRI_DT/ UART0_RTS#	XTAL Frequency Select	0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected.
GPP_J6/CNV_RGI_DT/ UART0_TXD	M.2 CNV Mode Select	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail
GPD7	Reserved	0 = XTAL INPUT IS SINGLE-ENDEDDefault)
SPI0_MISO	Reserved	0 = JTAG ODT 1 = Normal (Default) V
GPP_B23/SML1ALERT#/ PCHHOT#	IntelR DCI-OOB	1 = Enable DCI. (CRB/Datasheet)
GPP_H12/SML2ALERT#	TBD	0 = Master Attached Flash Sharing (MAFS) enable (Default)
SPI0_MOSI	Reserved	0 = Boot Halt 1 = Normal (Default)
SPI0_IO2	Reserved	1 = Consent strap disable (Default)
SPI0_IO3	Reserved	1 = Personality strap disable (Default)
USB_OC3_L	TBD	DFX TEST MODE XTAL INPUT 0 = SINGLE ENDED 1 = DIFFERENTIAL

DDPB_CTRLDATA/GPP_I6	Display Port B Detected	1 = Port B is detected.
DDPC_CTRLDATA/GPP_I8	Display Port C Detected	1 = Port C is detected.
DDPB_CTRLDATA/GPP_I10	Display Port D Detected	1 = Port D is detected.

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Title: GPIO Function & INT# Mapping

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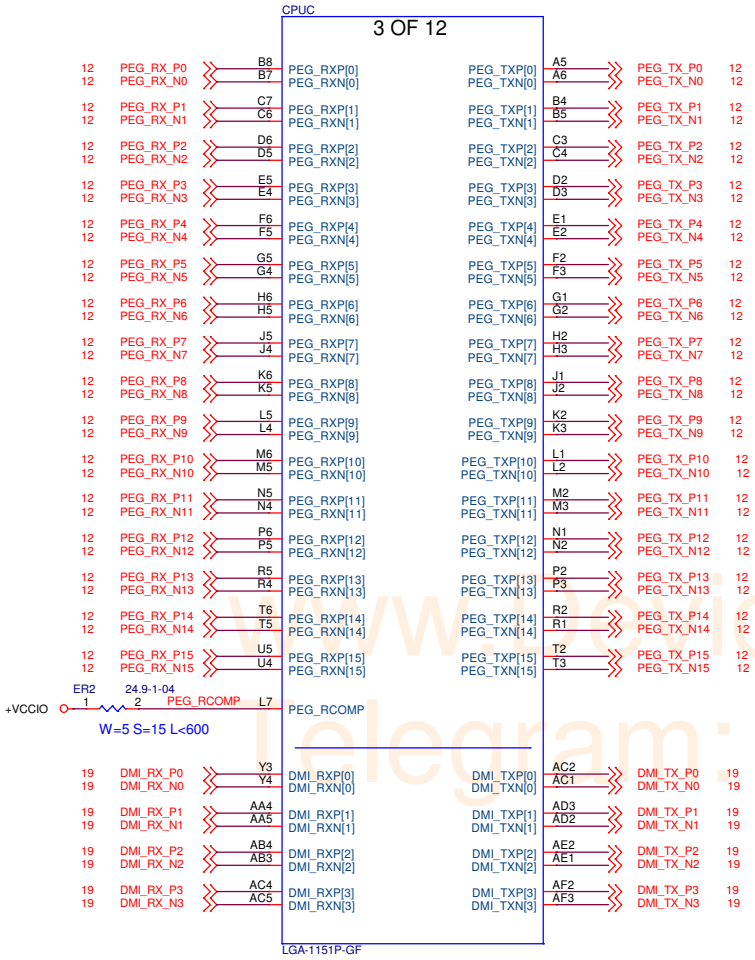

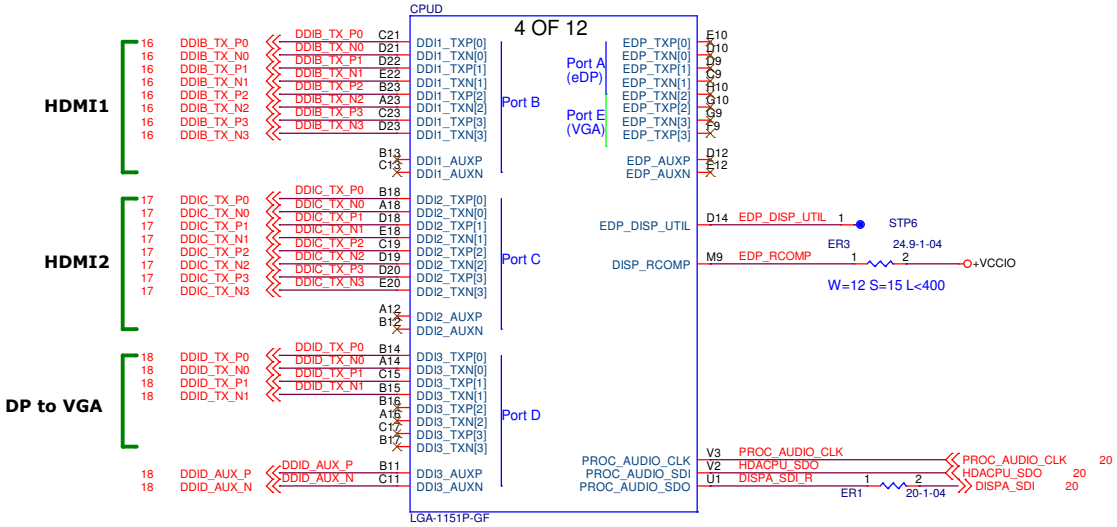

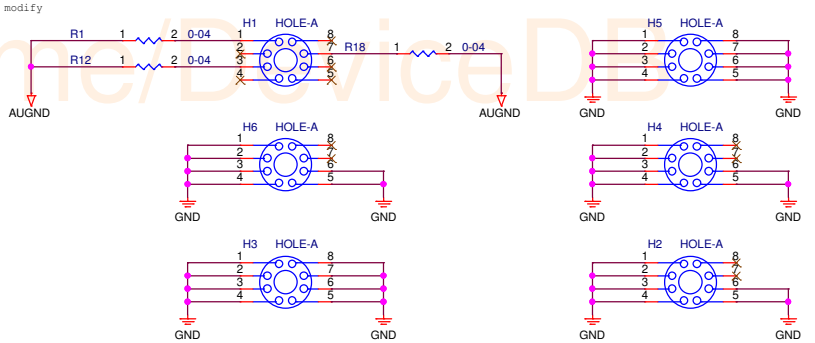

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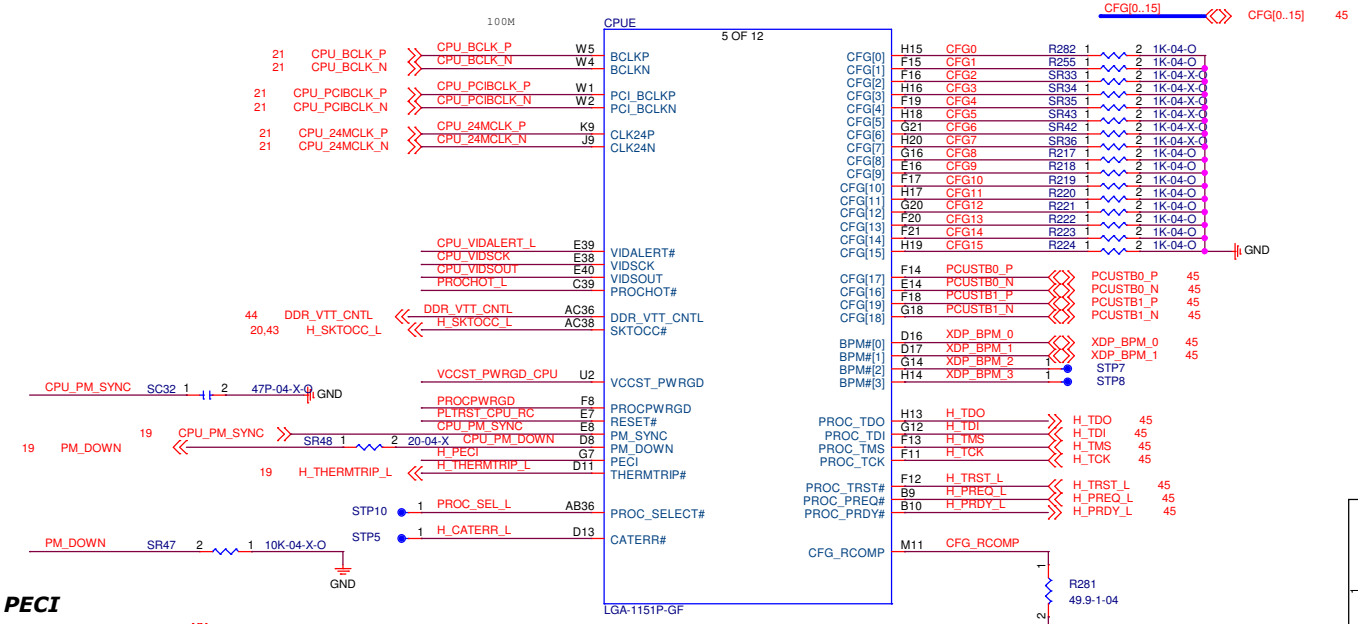
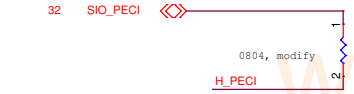
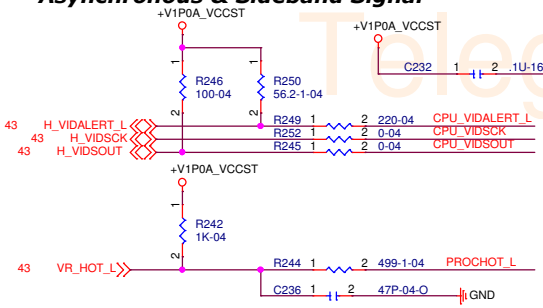


- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]:** PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.

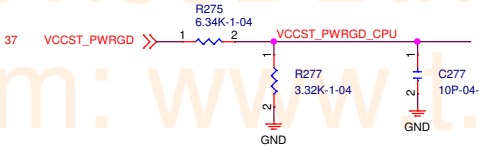
PECI

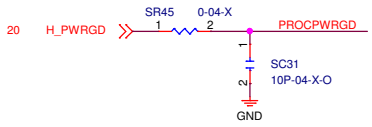


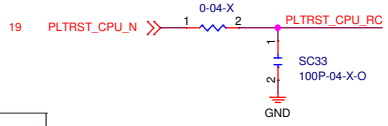
Asynchronous & Sideband Signal



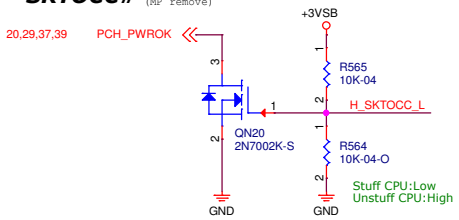
Processor Power Good

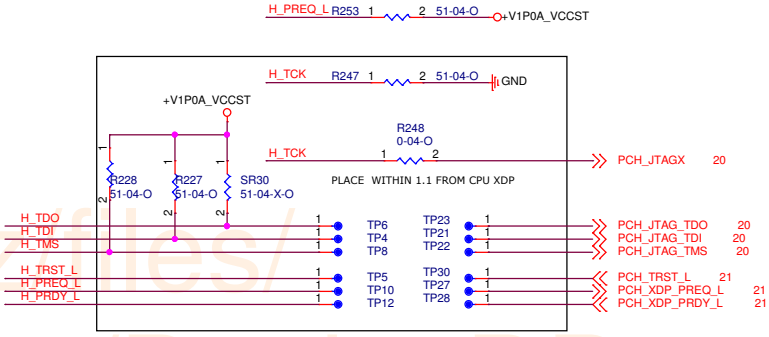


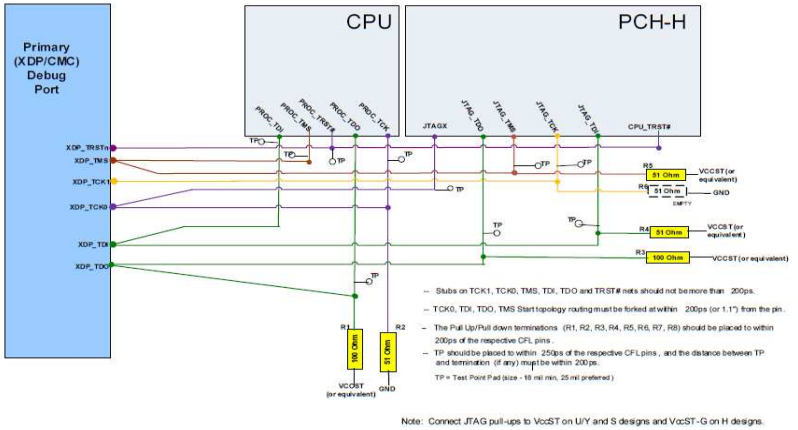




SKTOCC# (MP remove)







Note: Connect JTAG pull-ups to VccST on U/Y and S designs and VccST-G on H designs.

Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Pro-cessor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

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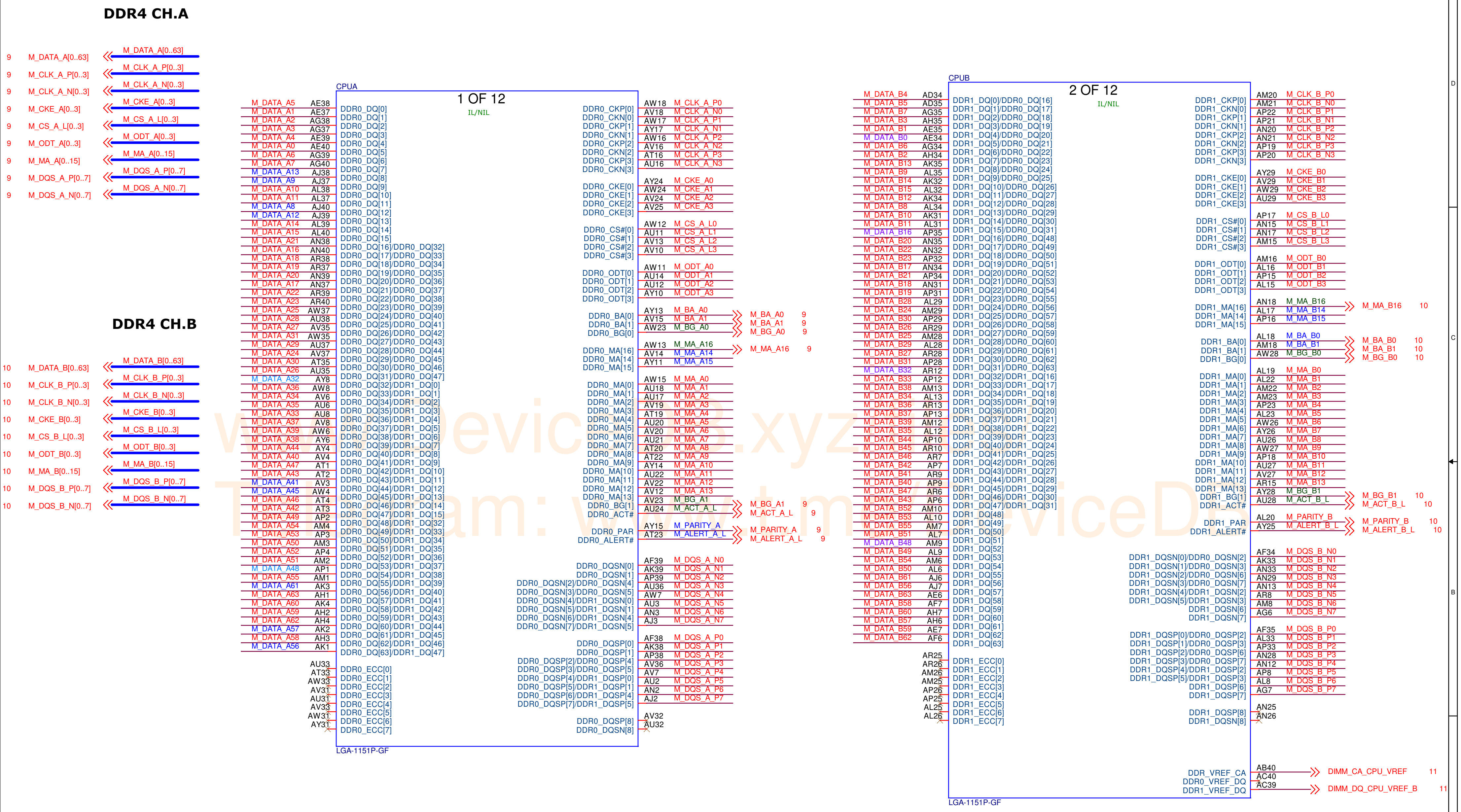

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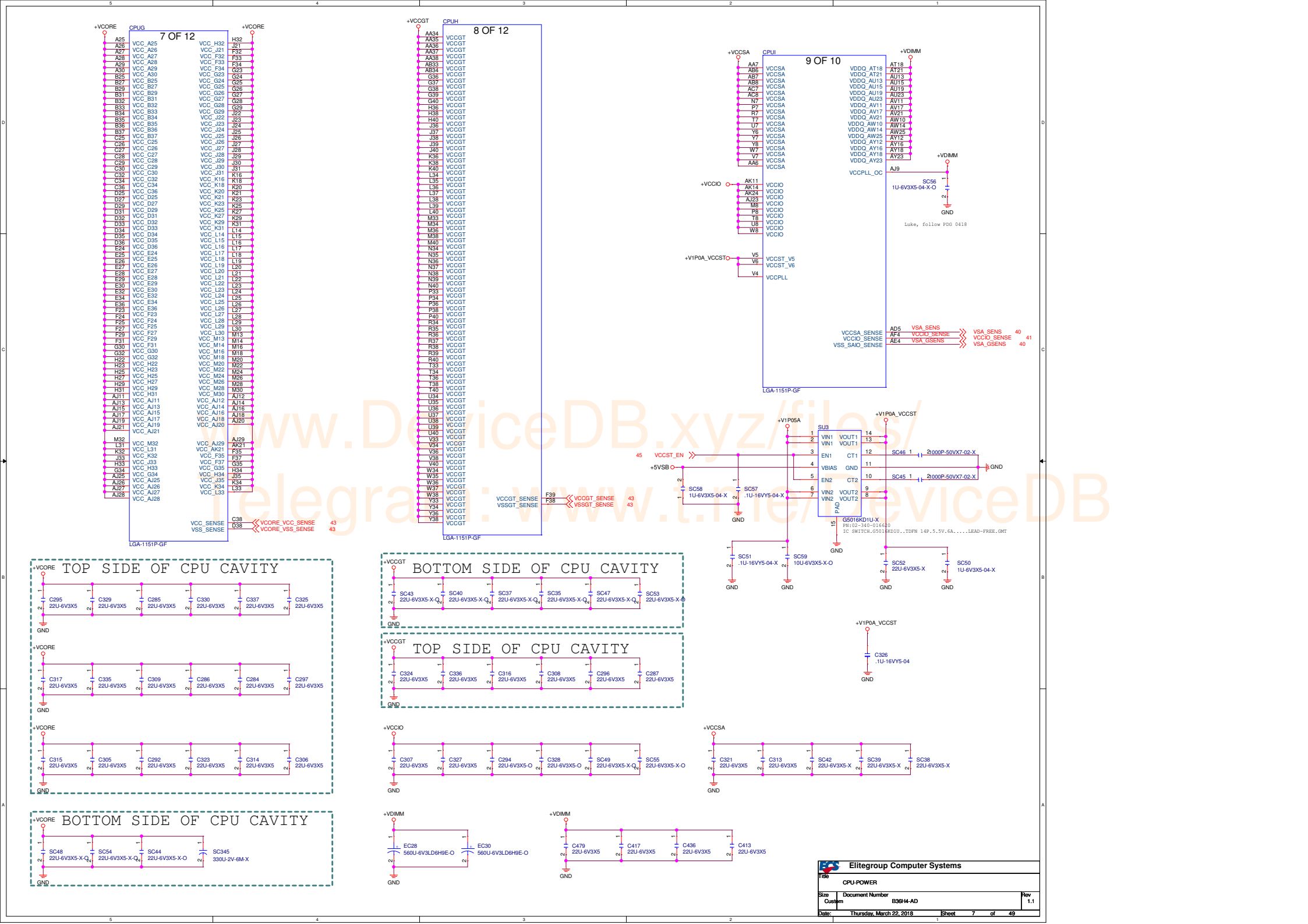

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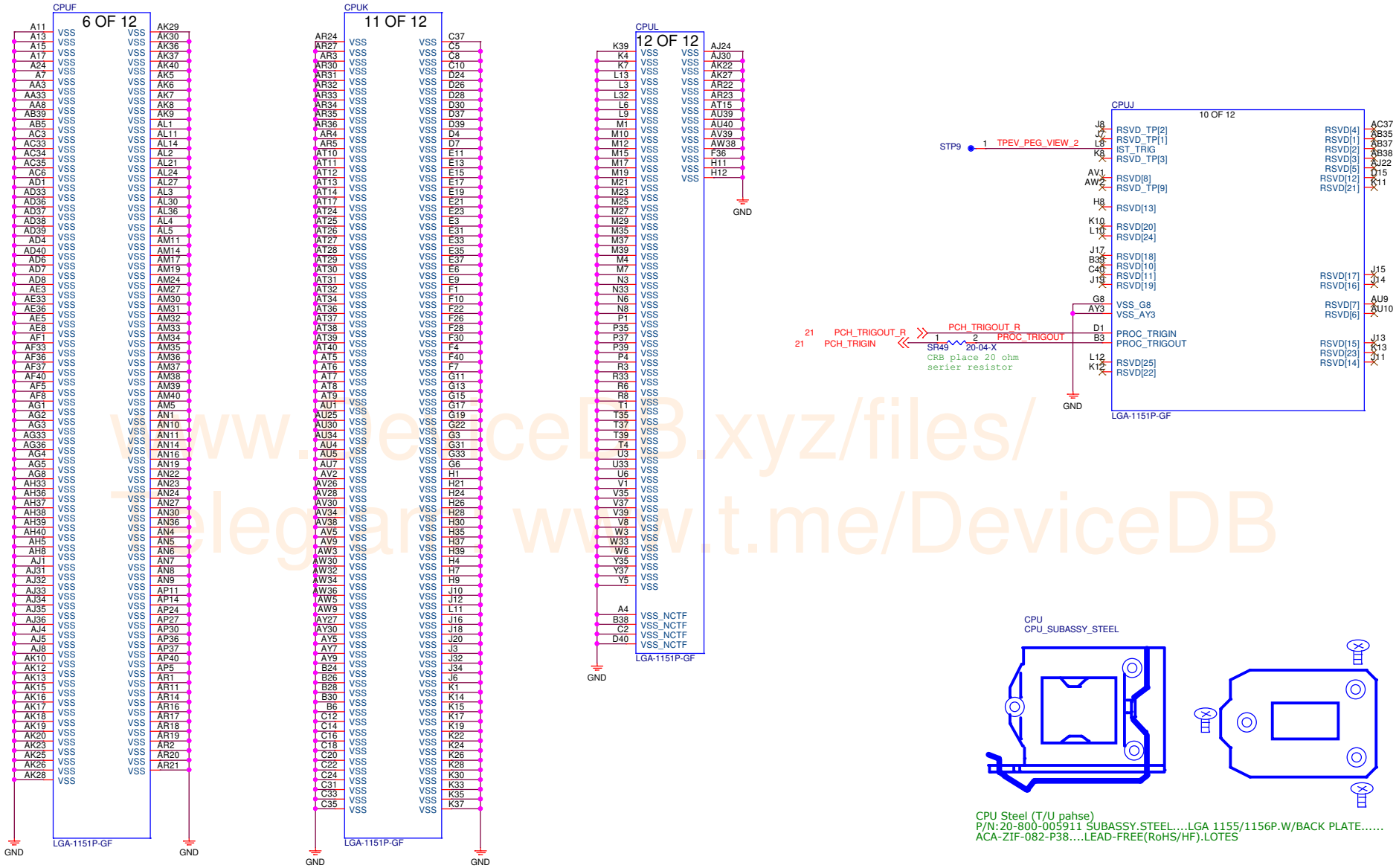

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P/N:20-800-005911 SUBASSY.STEEL....LGA 1155/1156P.W/BACK PLATE.....
ACA-ZIF-082-P38....LEAD-FREE(RoHS/HF).LOTES

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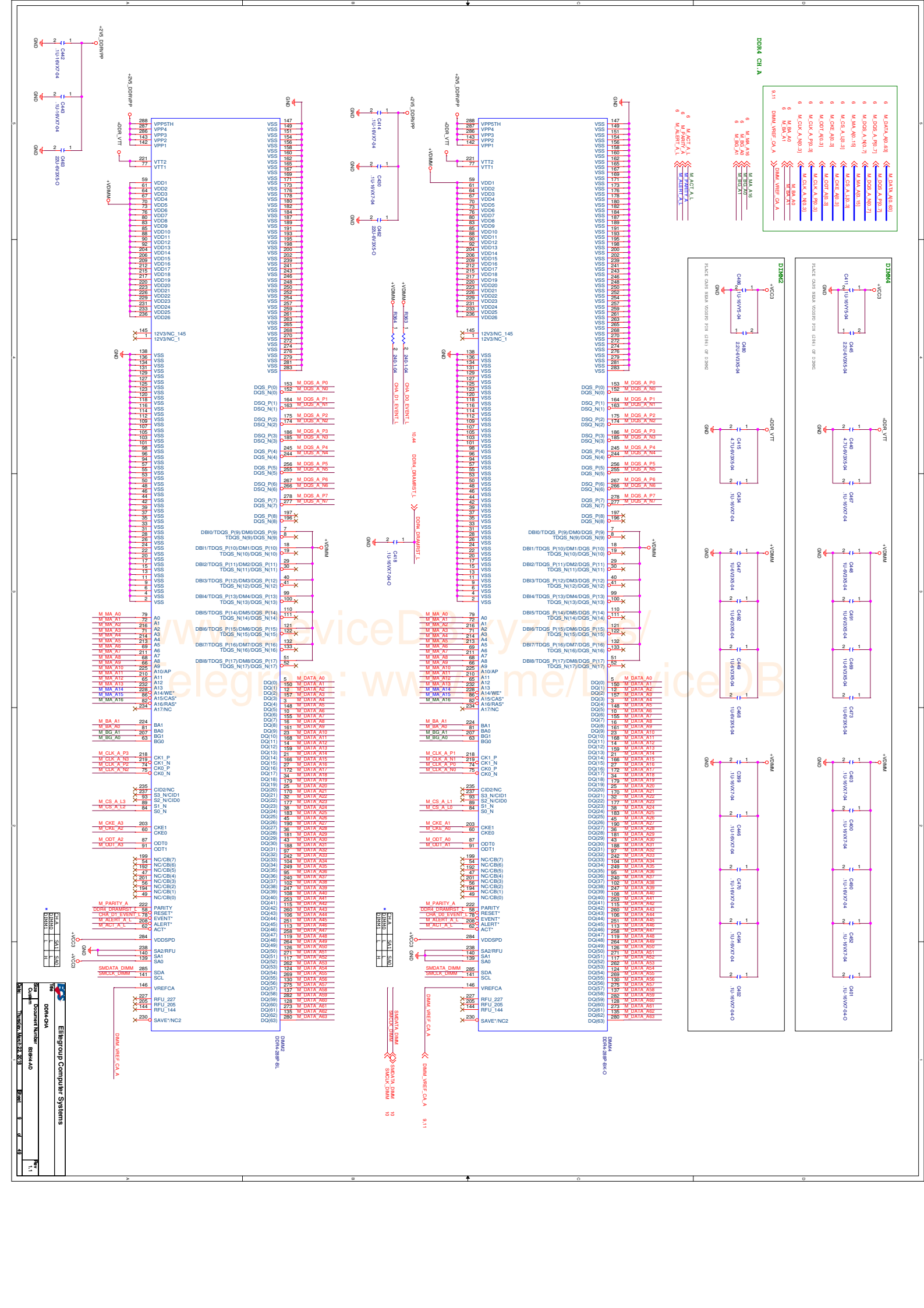

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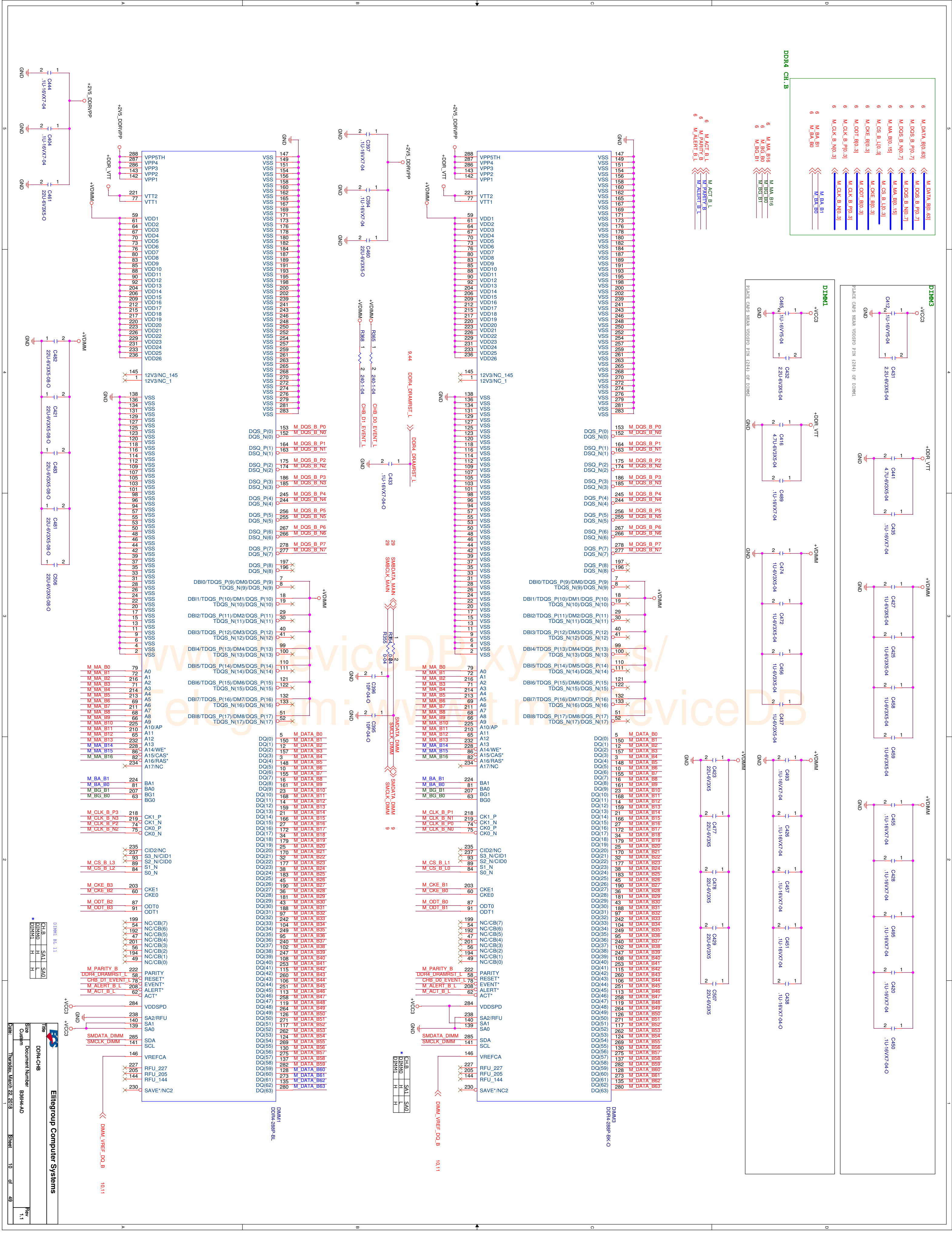
DDR4 CH.B
DIMM1
DDR4-288P-BL
DIMM3
DDR4-288P-BK-O
DIMM1
DIMM3
PLACE CAPS NEAR VDDSPD PIN (284) OF DIMM2
PLACE CAPS NEAR VDDSPD PIN (284) OF DIMM1
+2V5_DDRVPP
+DDR_VTT
+VDIMM
+VCC3
GND
VPP5TH
VTT2
VTT1
12V3/NC_145
12V3/NC_1
DDR4_DRAMRST_L
CHB_D0_EVENT_L
CHB_D1_EVENT_L
SMBDATA_MAIN
SMBCLK_MAIN
SMDATA_DIMM
SMCLK_DIMM
DIMM_VREF_DQ_B
M_DATA_B[0..63]
M_DQS_B_P[0..7]
M_DQS_B_N[0..7]
M_MA_B[0..15]
M_CS_B_L[0..3]
M_CKE_B[0..3]
M_ODT_B[0..3]
M_CLK_B_P[0..3]
M_CLK_B_N[0..3]
M_BA_B1
M_BA_B0
M_MA_B16
M_BG_B0
M_BG_B1
M_ACT_B_L
M_PARITY_B
M_ALERT_B_L
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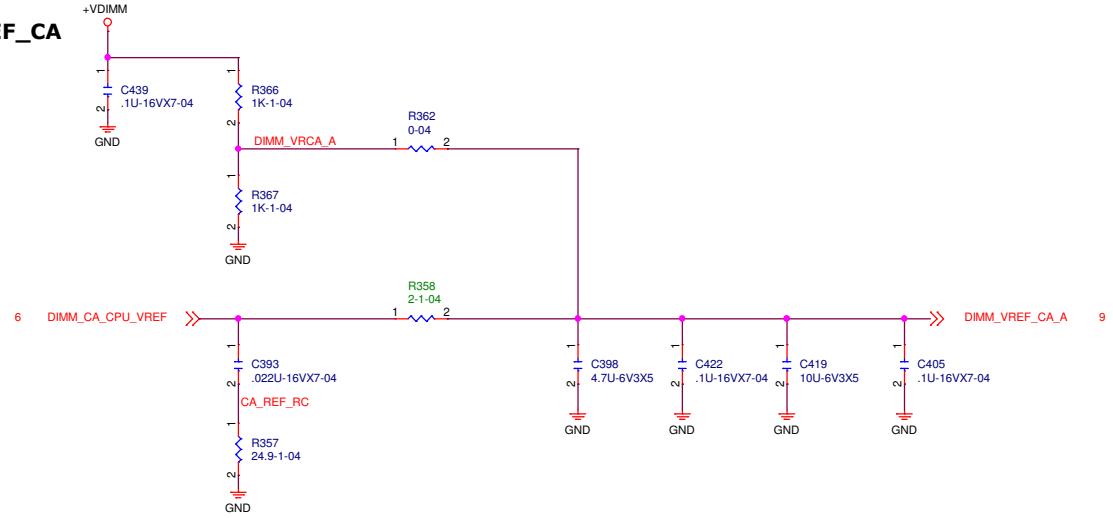
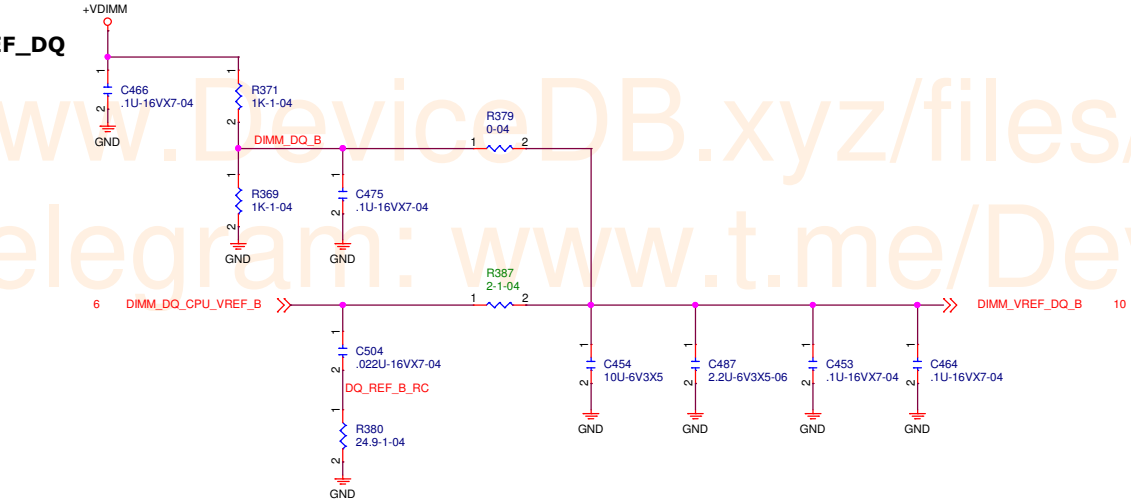
DIMM_VREF_CA



DIMM_VREF_DQ



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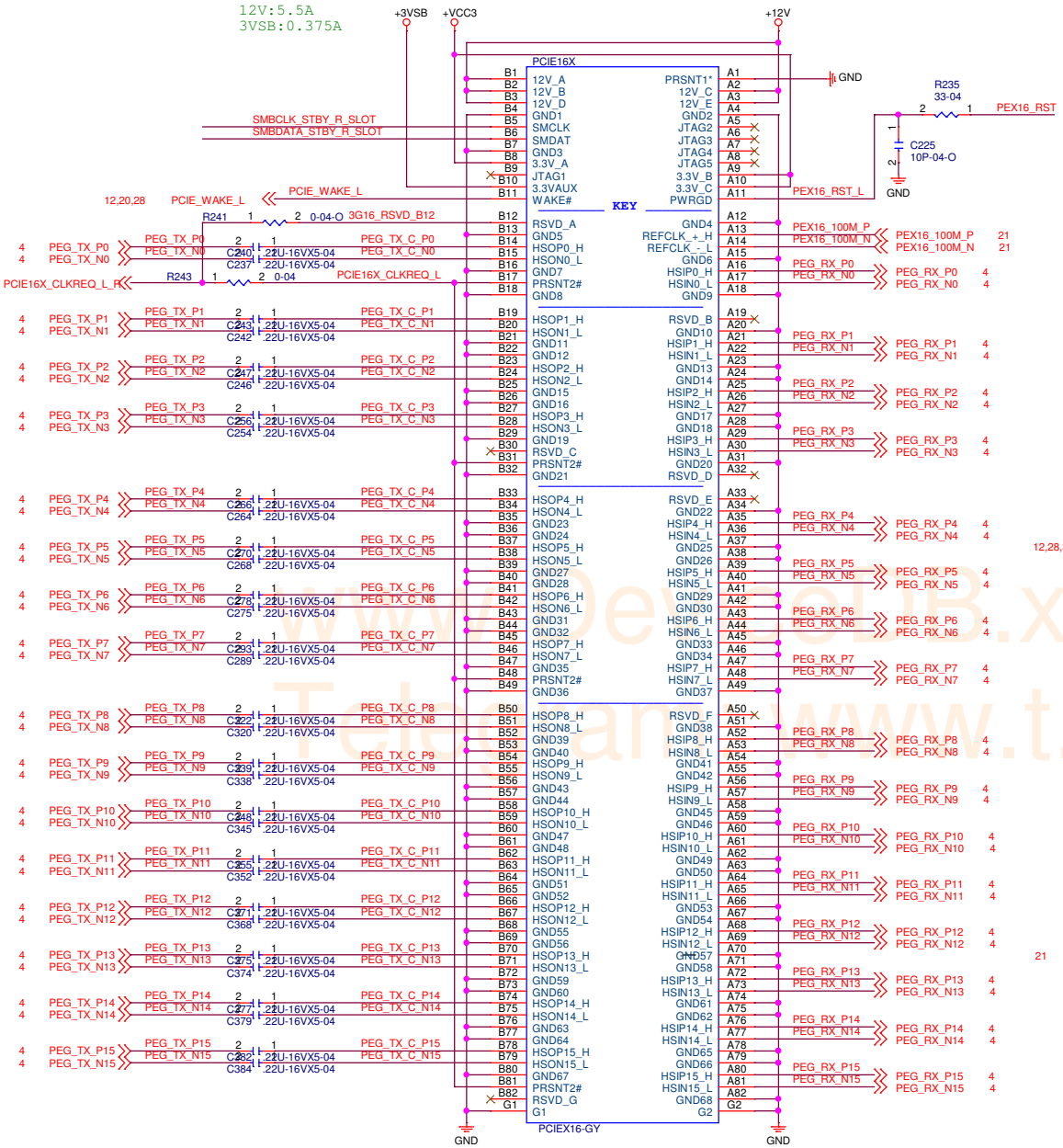
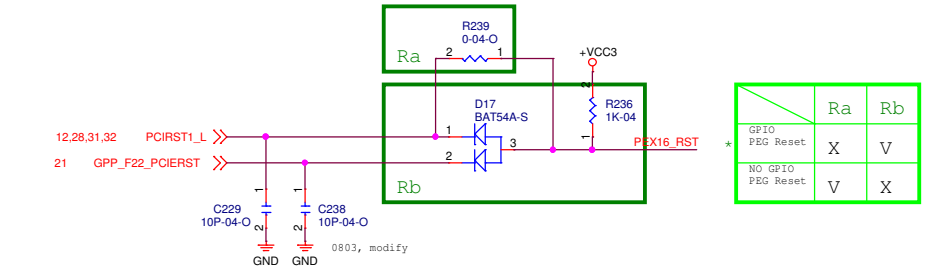
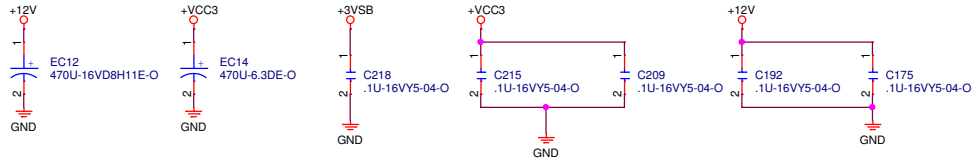
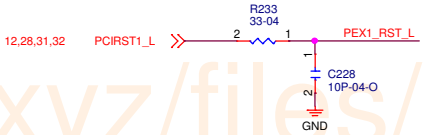
PCIE SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A

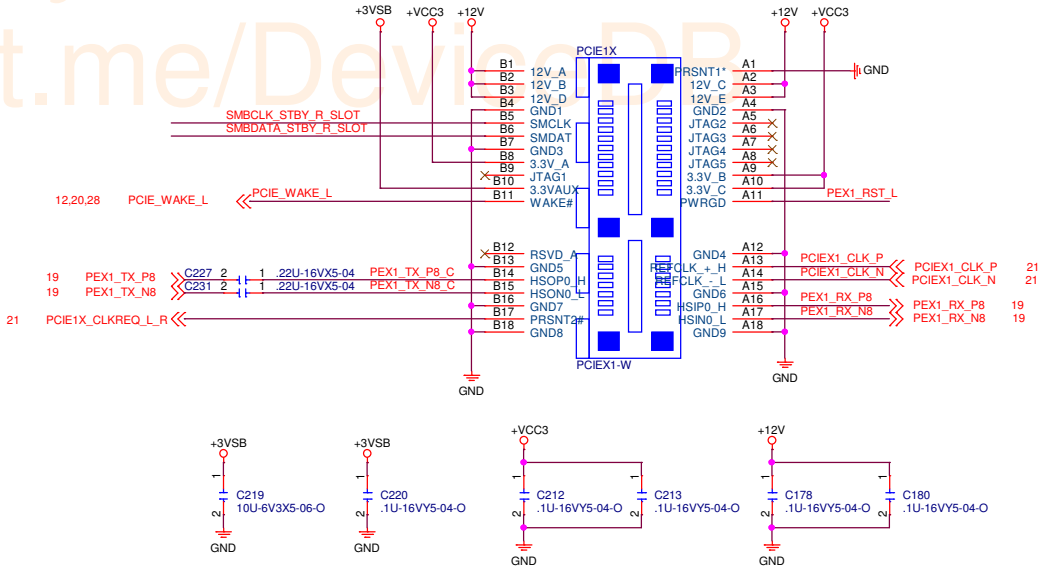


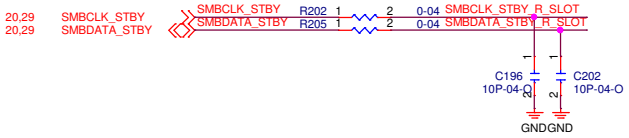


Between PCIEX16 & PCIEX1









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Telegram www.t.me/DeviceDB

Elitegroup Computer Systems	
Title	PCIE*16 / PCIE *1
Size: Custom	Document Number: B36H4-AD
Rev	1.1
Date:	Thursday, March 22, 2018
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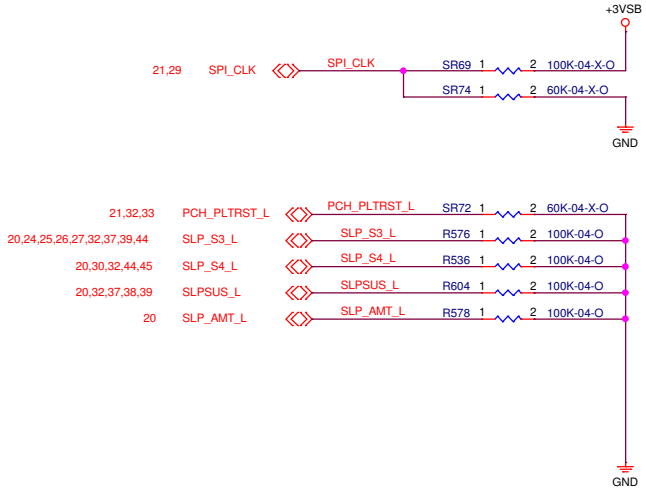
www.DeviceDB.xyz/files/
Telegram: www.t.me/DeviceDB

Elitegroup Computer Systems			
Title: NA			
Size: Custom	Document Number: B36H4-AD		Rev: 1.1
Date: Monday, January 15, 2018	Sheet 13 of 49		

www.DeviceDB.xyz/files/
Telegram: www.t.me/DeviceDB

Elitegroup Computer Systems			
Title: NA			
Size: Custom	Document Number: B36H4-AD		Rev: 1.1
Date: Monday, January 15, 2018	Sheet 14 of 49		



Board Implementation for Critical Signal Glitch-Free Operation

Signal Name	Option 1 (Cap)		Option 2 (Resistor)		Notes
	3.3V Ramp Rate 5-50 ms (3.3V or 1.8V Signaling Mode)	3.3V Ramp Rate < 5ms (3.3V or 1.8V signaling Mode)	3.3V Signaling Mode	1.8V Signaling Mode	
Signals Required Cap or PD resistor					
SLP_S3#; SLP_S4#; SLP_A#; SLP_LAN#; SLP_WLAN#; SLP_SUS#	330 nF	33 nF	100 K	75 K	Cap or pull-down Required
eDP_BKLTEN eDP_VDDEN	330 nF	33 nF	100 K	75 K	Cap or pull-down Required depending on Panel power sequencing spec or power delivery
SPI0_CLK; EXT_PWR_GATE#	NA	NA	100 K	75 K	Pull-up Required
SLP_S0#;	NA	NA	100 K	75 K	Pull-up Required if device monitoring SLP_S0# pre-RSMRST# de-assertion
Signals Required Cap or Resistor Site (Not populated)					
SLP_S5#; SUS_STAT# / ESPI_RESET#	Cap site		Pull-down resistor site		Site for cap or resistor only
PLTRST# HDA_BCLK / I2S0_SCLK HDA_RST# / I2S1_SCLK I2S1_SFRM / SNDW2_CLK	NA		Pull-down resistor site		Site for resistor only

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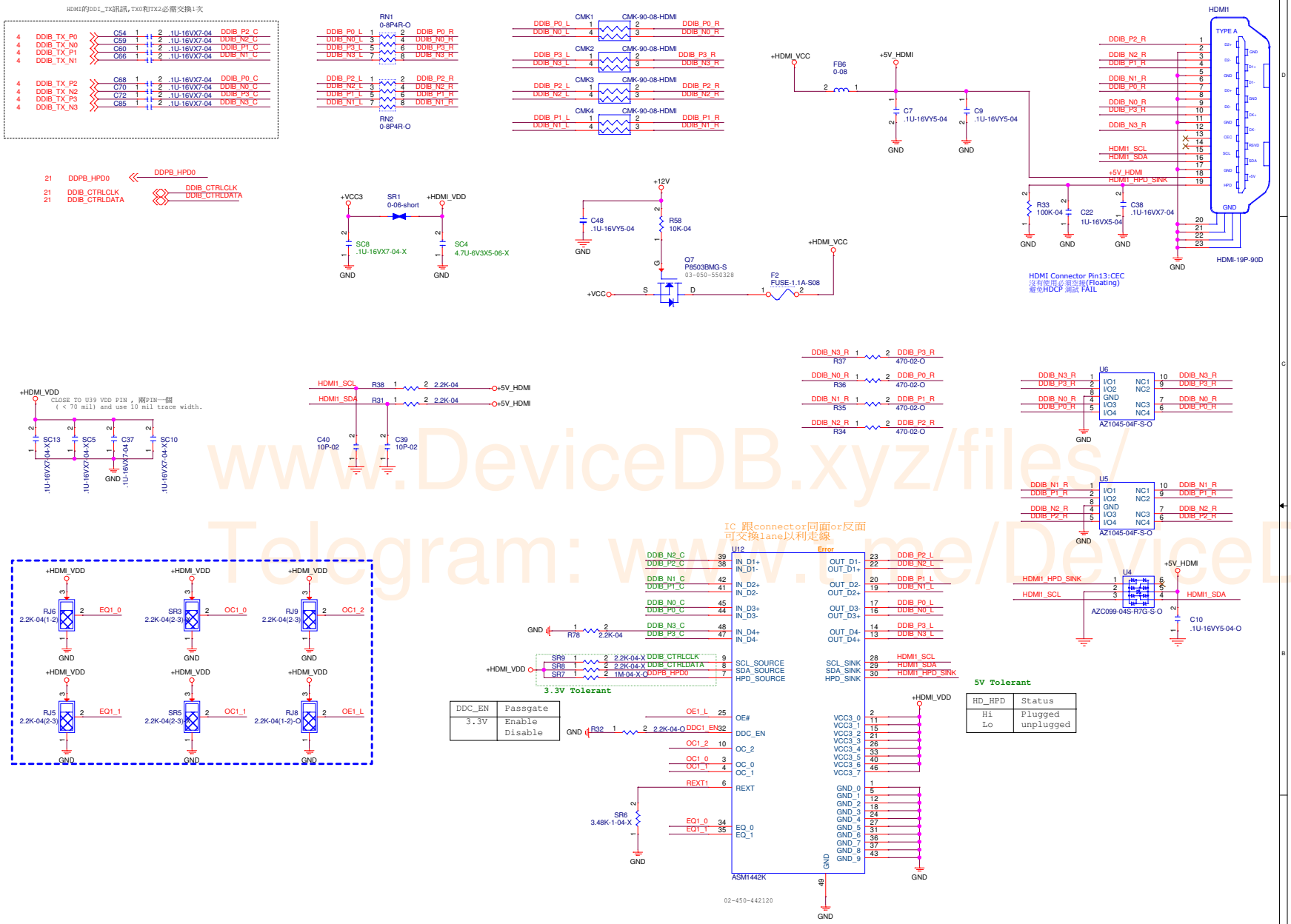
www.t.me/DeviceDB

Elitegroup Computer Systems			
Title: Glitch-free operation			
Size: Custom	Document Number: B36H4-AD		Rev: 1.1
Date: Thursday, March 22, 2018	Sheet 15 of 49		

HDMI1



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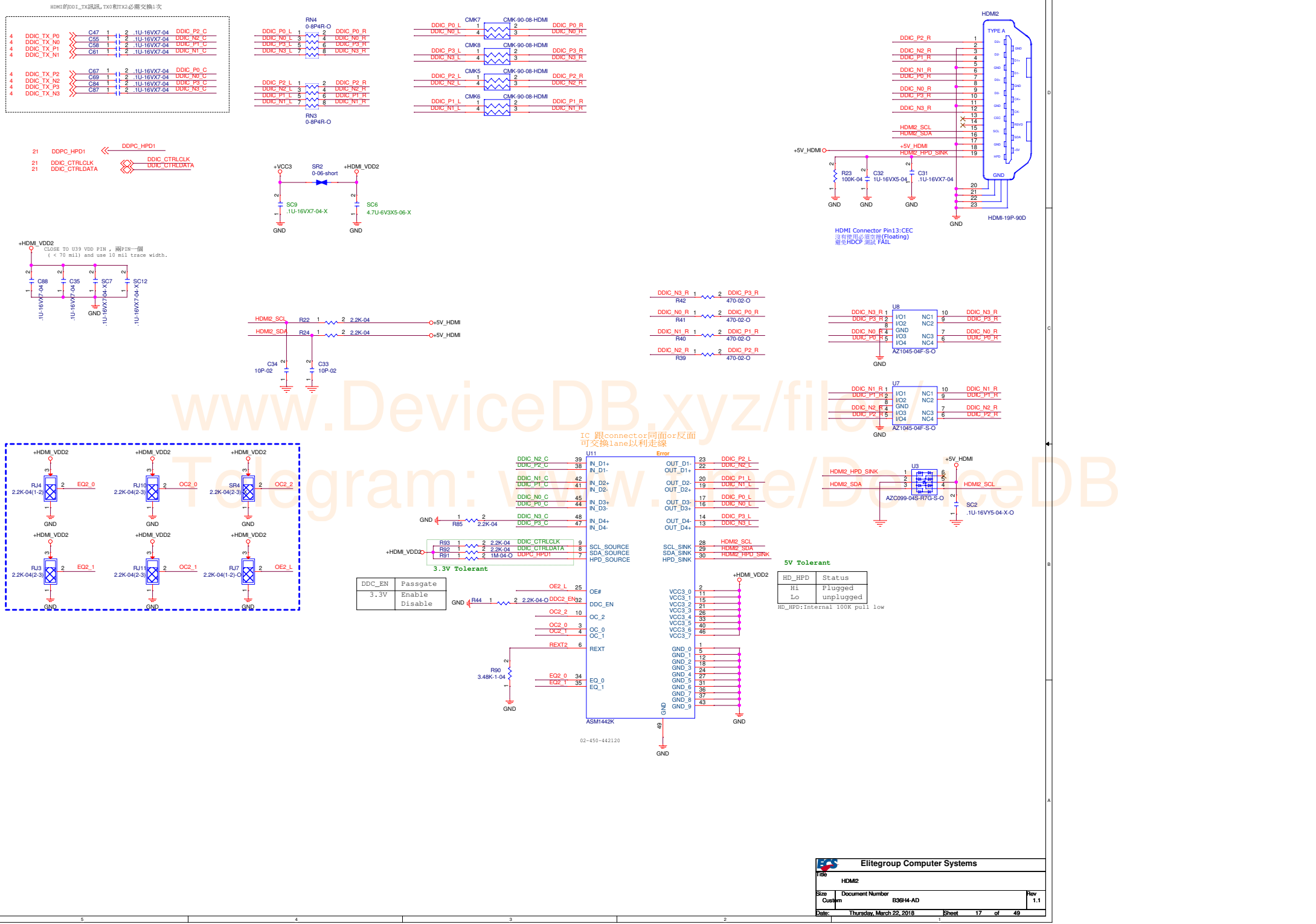
Telegram: www.t.me/DeviceDB

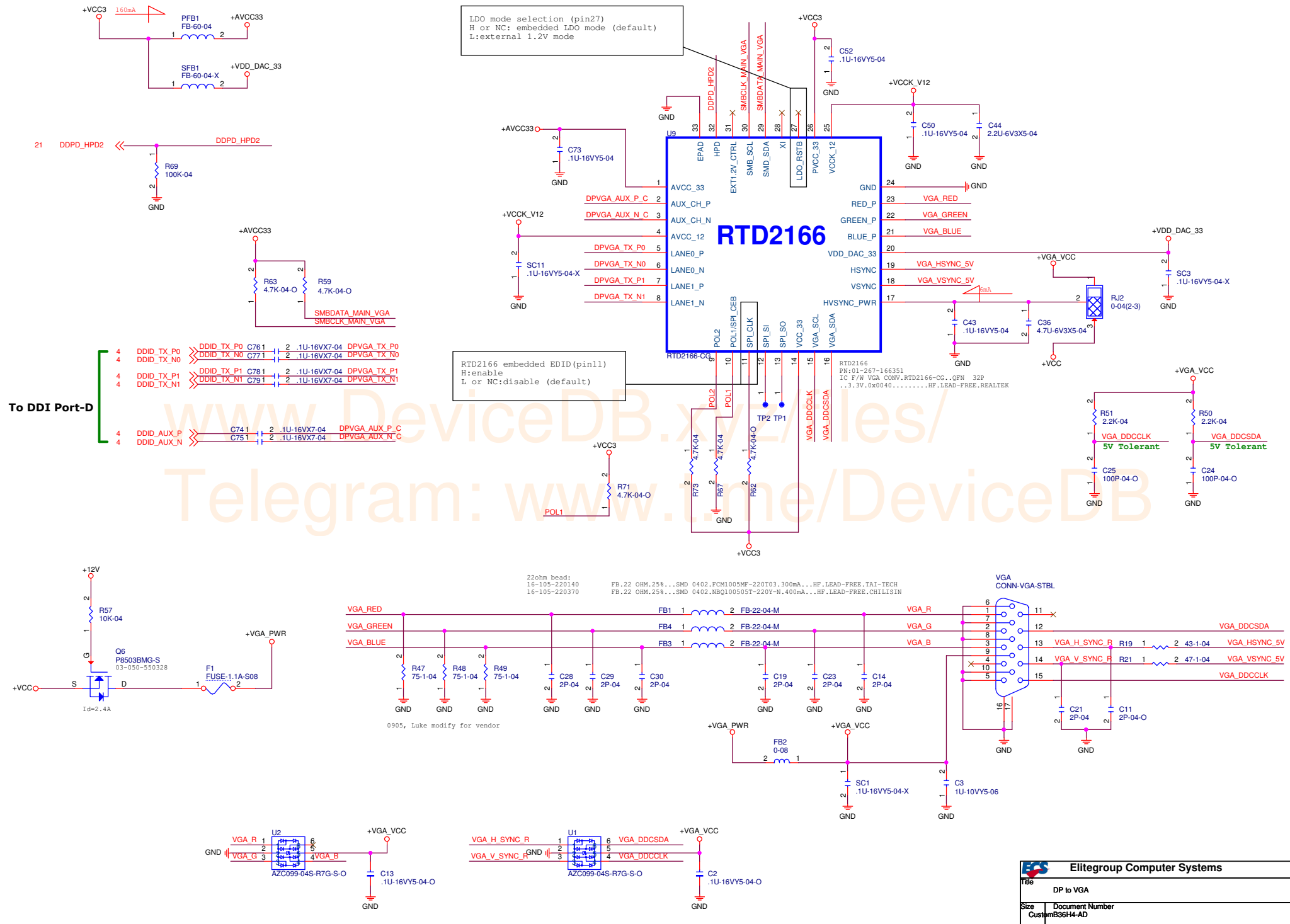
Elitegroup Computer Systems	
Title: HDMI1	
Size: Custom	Document Number: B36H4-AD
Rev: 1.1	
Date: Thursday, March 22, 2018	Sheet 16 of 49

HDMI2



www.DeviceDB.xyz/file/
Telegram: www.t.me/DeviceDB

Elitegroup Computer Systems		
Title: HDMI2		
Size: Custom	Document Number: B36H4-AD	Rev: 1.1
Date: Thursday, March 22, 2018	Sheet 17 of 49	



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Telegram: www.t.me/DeviceDB

Elitegroup Computer Systems	
Title	DP to VGA
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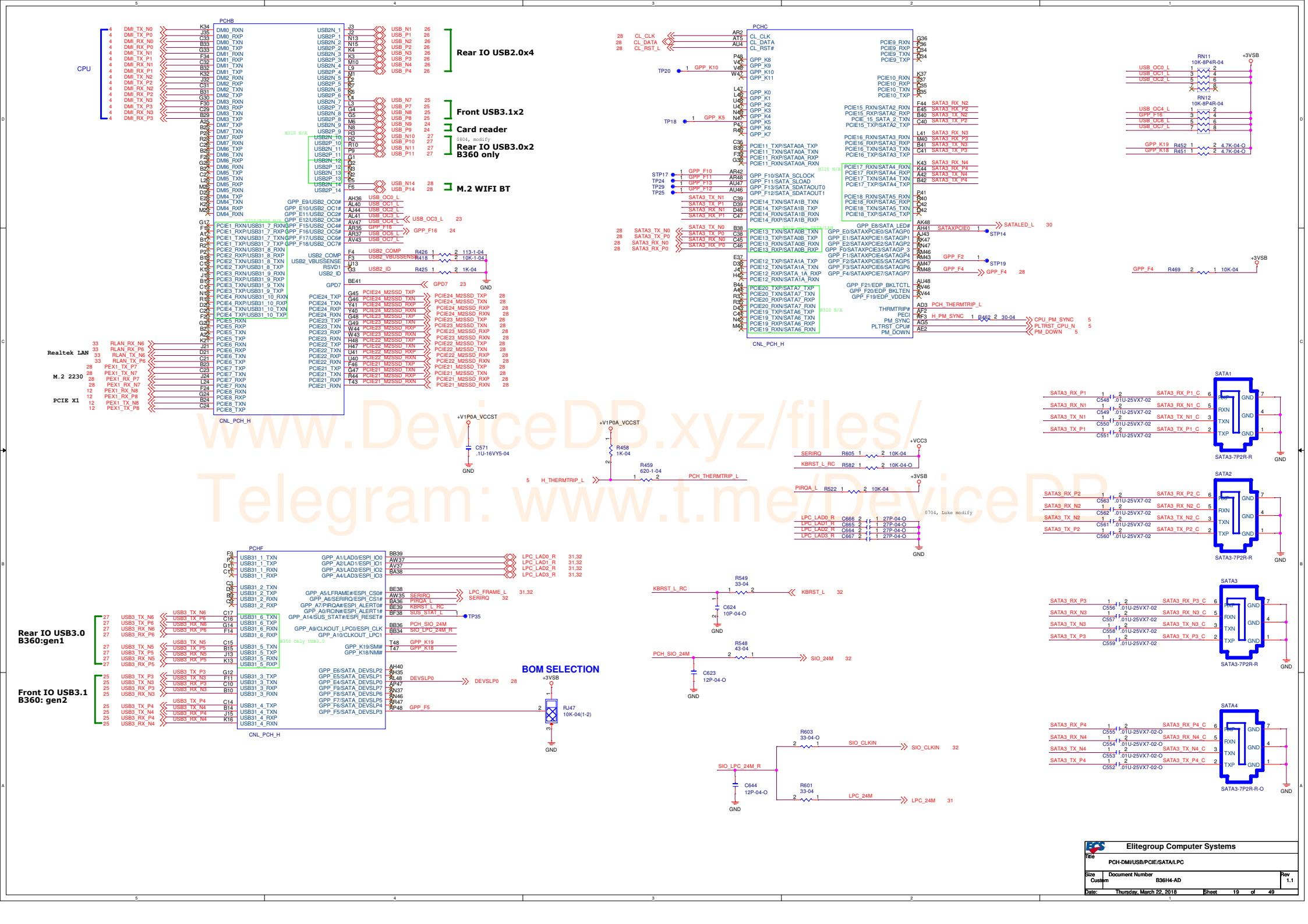

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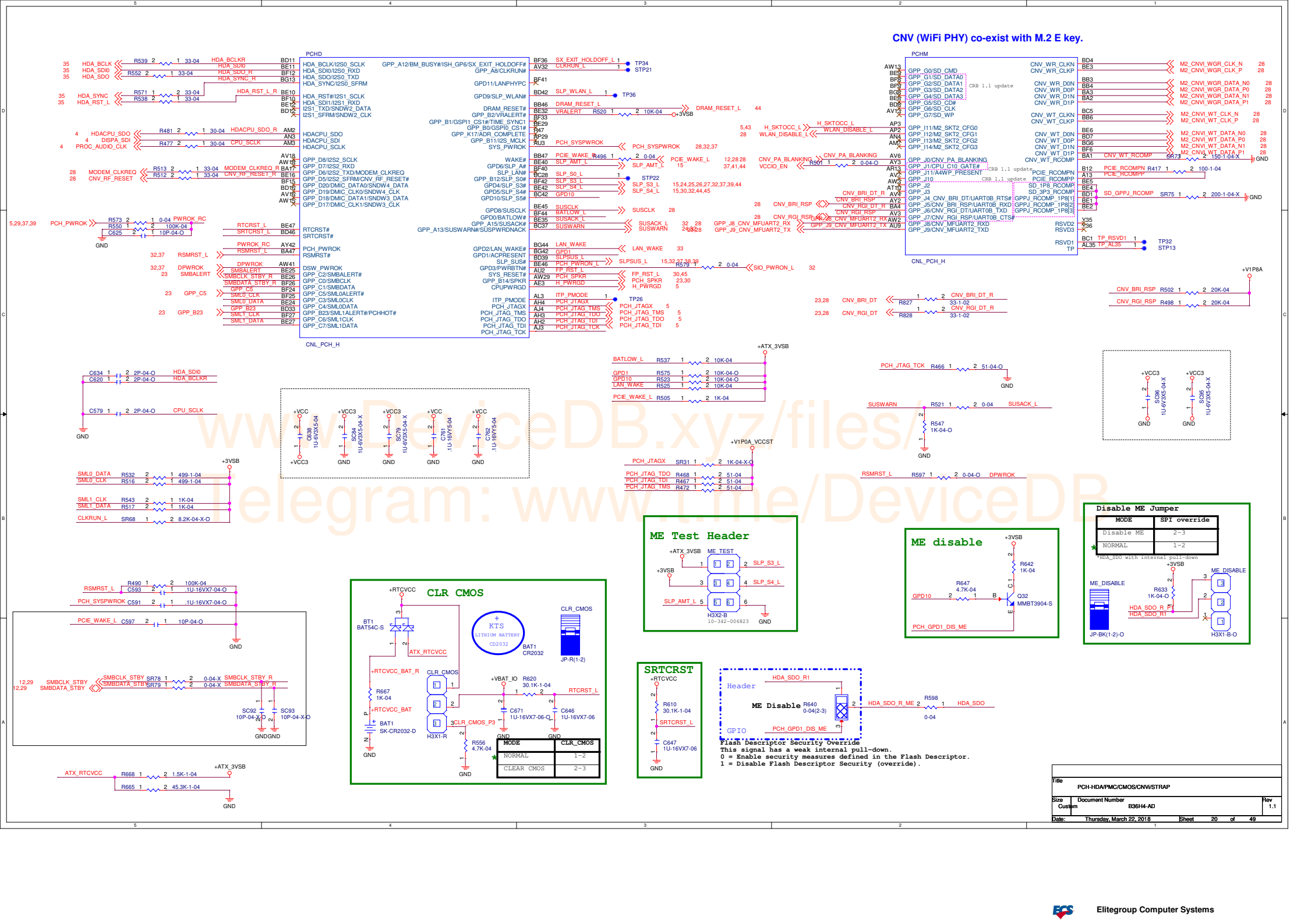
CNV (WiFi PHY) co-exist with M.2 E key.



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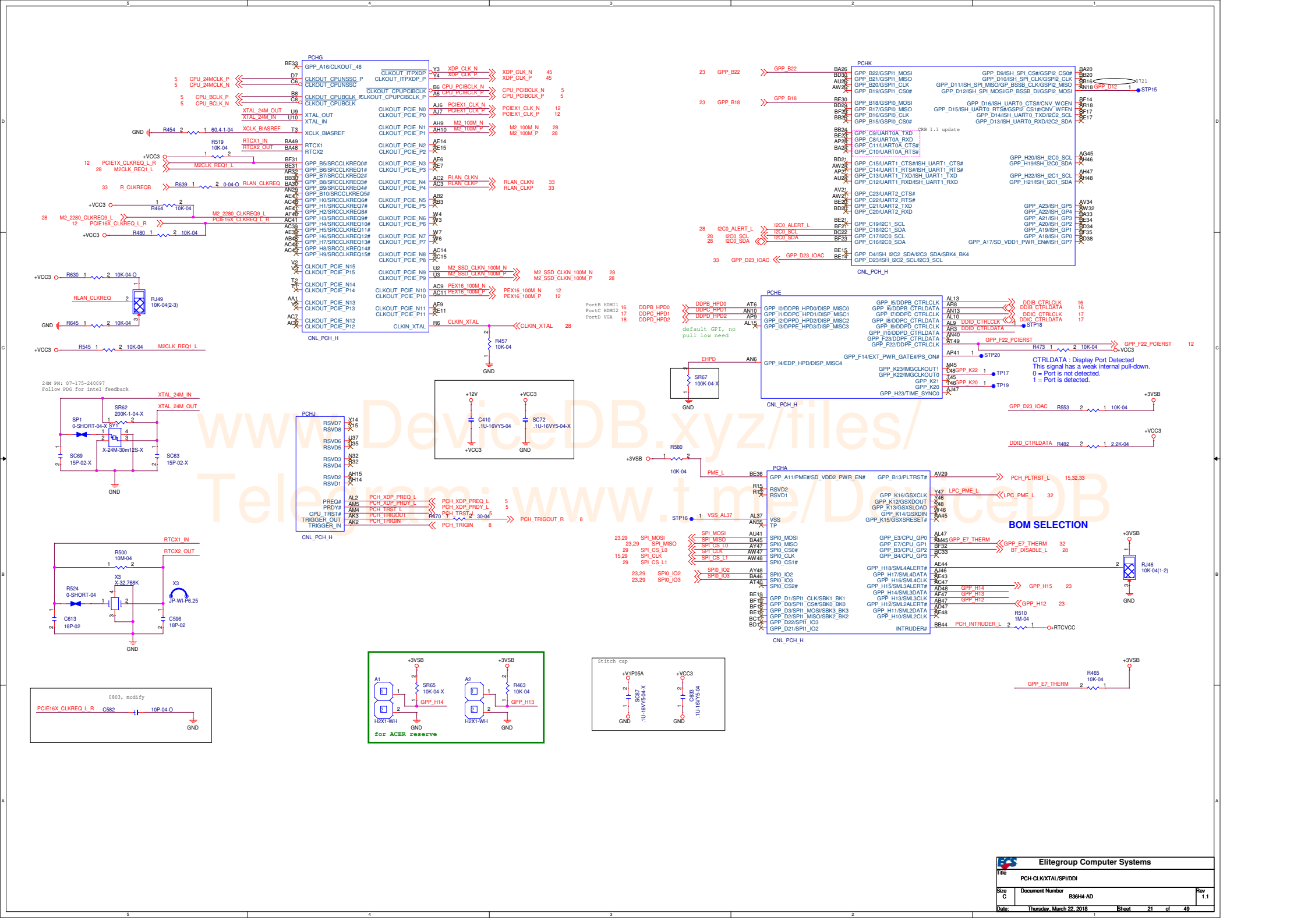
Telegram: www.t.me/DeviceDB


PCHG
PCHK
PCHE
PCHJ
PCHA
CNL_PCH_H
BOM SELECTION
CTRLDATA : Display Port Detected
This signal has a weak internal pull-down.
0 = Port is not detected.
1 = Port is detected.
default GPI, no pull low need
for ACER reserve
Stitch cap
Elitegroup Computer Systems
PCH-CLK/XTAL/SPI/DDI
B36H4-AD
Thursday, March 22, 2018
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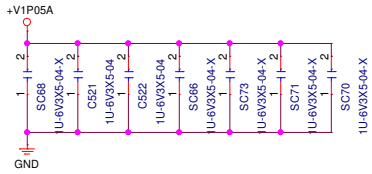

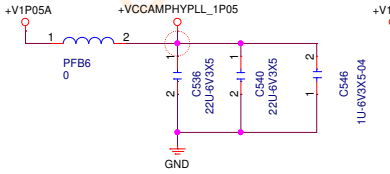

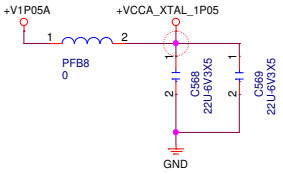

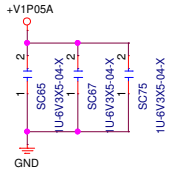

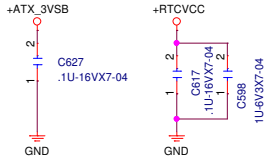

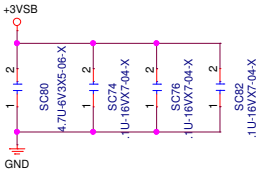

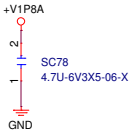

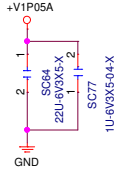

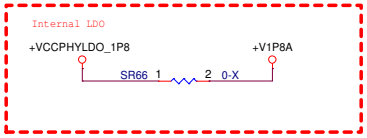

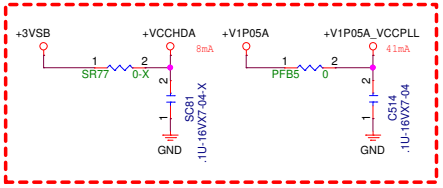

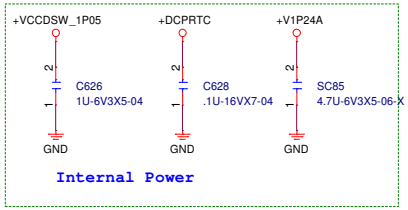

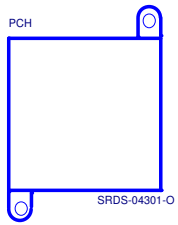

PCH heatsink (T/U phase)
P/N:20-120-013594
HEAT SINK.....SILVER.SRDS-04301-UTS2.SB.31.5*31*1.5mm
....W/PUSH PIN*2,PAD,FOAM....HF.LEAD-FREE.SIXCO

替: 20-120-013593
替: 20-120-013596

08-402-225172
INDUCTOR.2.2uH.10%.100mA.0.33 OHM....SMD 0603..PCH1608F-2R2KT01....LEAD-FREE(RoHS/HF).TAI-TECH

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Elitegroup Computer Systems		
Title: PCH-POWER/GND		
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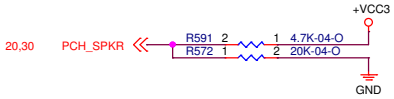
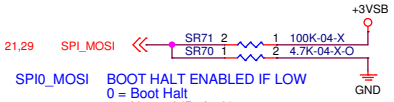
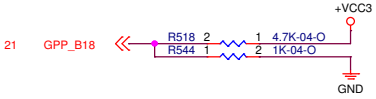


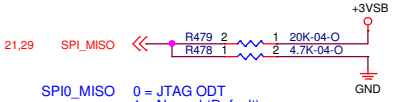
SPKR 0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.
PCH HAS INTERNAL WEAK PD



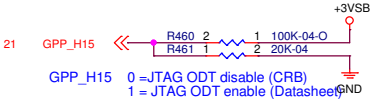
SPI0_MOSI BOOT HALT ENABLED IF LOW
0 = Boot Halt
1 = Normal (Default)
PCH HAS INTERNAL WEAK PU



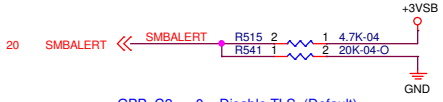
GPP_B18 0 = "Reboot" mode. (Default)
1 = "No Reboot" mode
PCH HAS INTERNAL WEAK PD,
This function is useful when running ITP/XDP



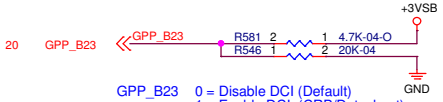
SPI0_MISO 0 = JTAG ODT
1 = Normal (Default)
PCH HAS INTERNAL WEAK PU



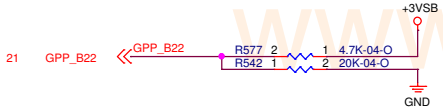
GPP_H15 0 =JTAG ODT disable (CRB)
1 = JTAG ODT enable (Datasheet)



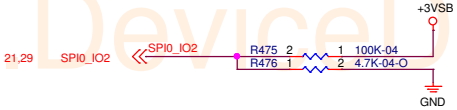
GPP_C2 0 = Disable TLS. (Default)
1 = Enable TLS for AMT.
PCH HAS INTERNAL WEAK PD



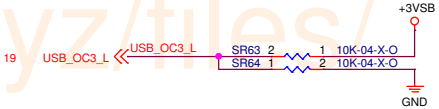
GPP_B23 0 = Disable DCI (Default)
1 = Enable DCI. (CRB/Datasheet)
PCH HAS INTERNAL WEAK PD



GPP_B22 Boot BIOS Destination
0 = SPI(Default)
1 = LPC
PCH HAS INTERNAL WEAK PD

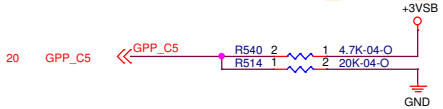


SPI0_IO2 0 = Consent strap enable
1 = Consent strap disable (Default)
PCH HAS INTERNAL WEAK PU

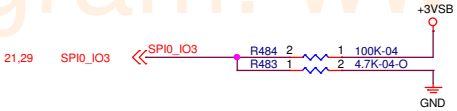


USB_OC3_L DFX TEST MODE
XTAL INPUT
0 = SINGLE ENDED
1 = DIFFERENTIAL

• The pull-down resistor is disabled after RSMRST# de-asserts

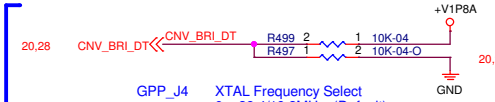


GPP_C5 ESPI/LPC SELECT STRAP
0 = LPC Bus (Default)
1 = eSPI Bus
PCH HAS INTERNAL WEAK PD

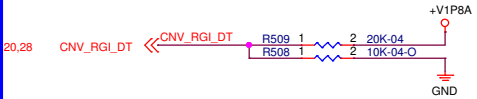


SPI0_IO3 PESONALITY STRAP
0 = Personality strap enable
1 = Personality strap disable (Default)
PCH HAS INTERNAL WEAK PU

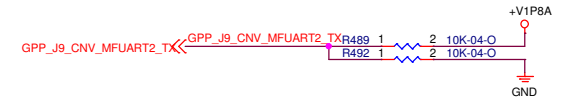
CNVi



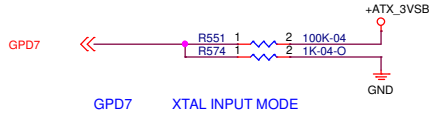
GPP_J4 XTAL Frequency Select
0 = 38.4/19.2MHz. (Default)
1 = 24MHz
PCH HAS INTERNAL 20K PD



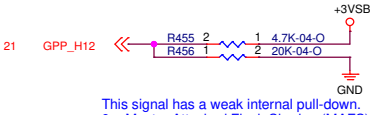
GPP_J6 Modem Reference Clock Source Select
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.



GPP_J9 SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE
0 = VCCPSPI connect to 3.3V. (Default)
1 = VCCPSPI connect to 1.8V.
PCH HAS INTERNAL 20K PD



GPD7 XTAL INPUT MODE
0 = XTAL INPUT IS SINGLE-ENDEDDefault)
1 = XTAL INPUT IS DIFFERENTIAL
PCH HAS INTERNAL 20K PD



This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

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Elitegroup Computer Systems			
Title: PCH STRAP			
Size: Custom	Document Number: B36H4-AD		Rev: 1.1
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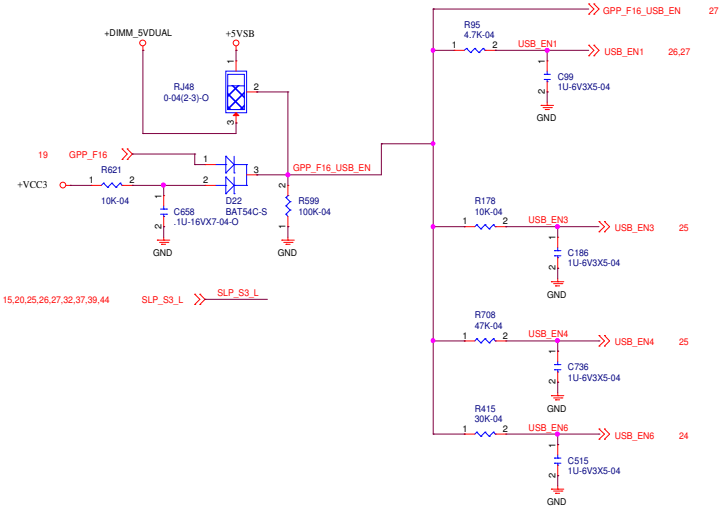
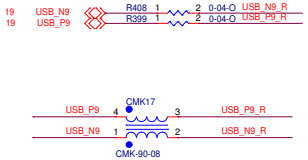
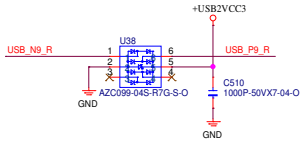
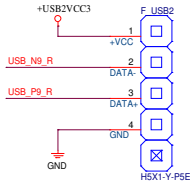


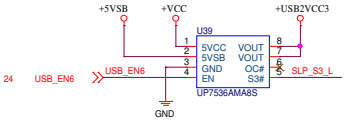
	power switch Enable use	RJ5	D26	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (2-3)	NA	0 Volt	Acer S4 W S5 W/O USB_5VDUAL
	5VSB	0ohm (1-2)	NA	5 Volt	
*	GPIO	NA	Stuff	S4 : 5 Volt S5 : 0 Volt	

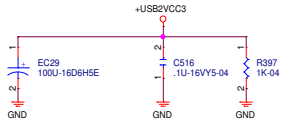
STATUS	S0	S3	S4	S5
GPP_F16	HI	HI	HI	LOW
USB PWR	ON	ON	ON	OFF





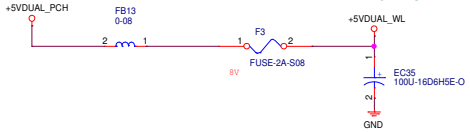


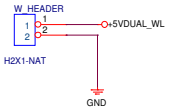


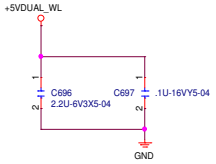


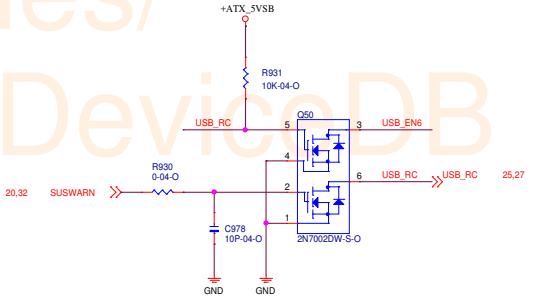
Card Reader

Wireless Charger Header









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Title: ireless Header/Card reader

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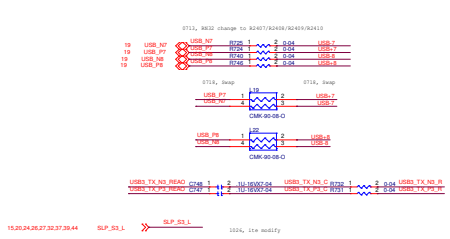
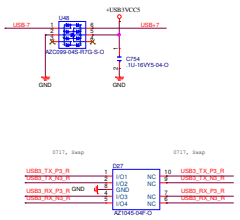
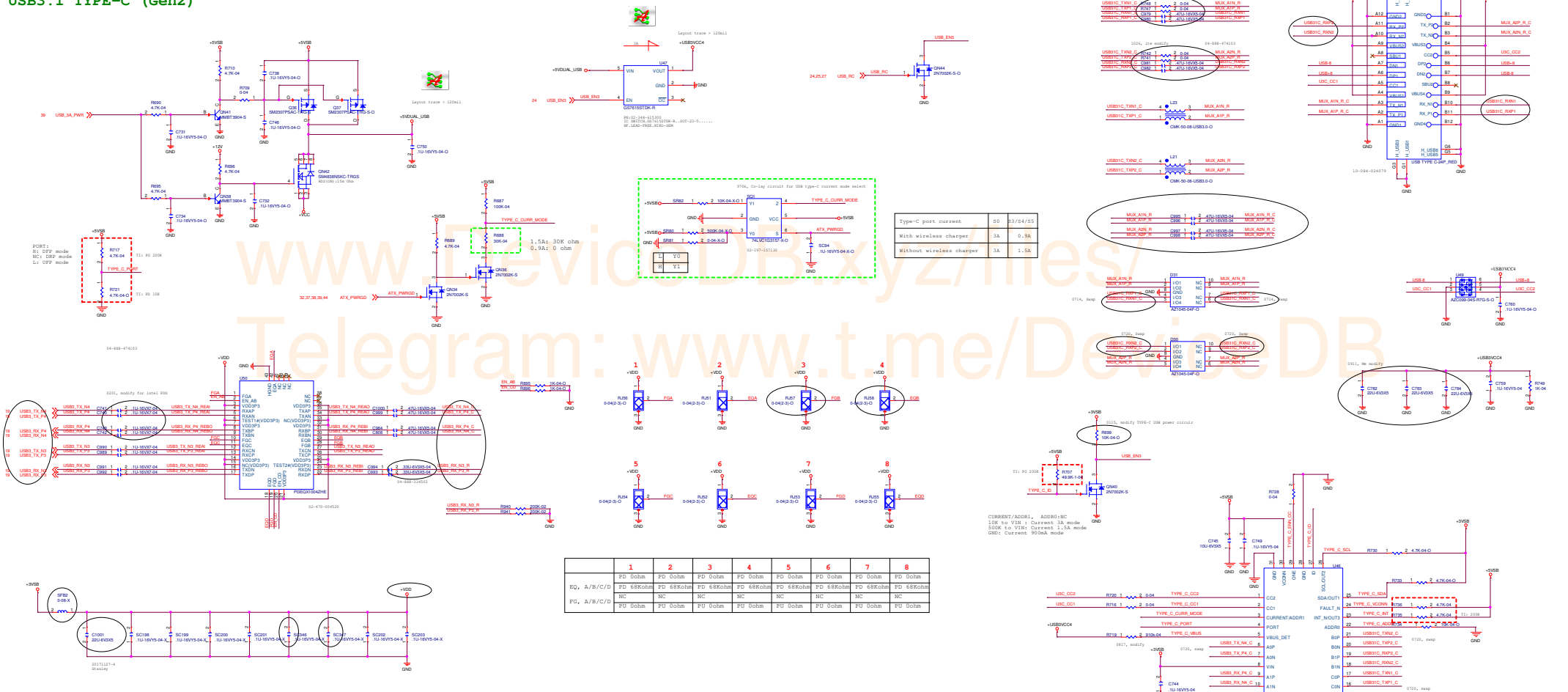
USB3.1(Gen2)



USB3.1 TYPE-A



USB3.1 TYPE-C (Gen2)



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Type-C port current	SO	S3/S4/S5
With wireless charger	3A	0.9A
Without wireless charger	3A	1.5A

	1	2	3	4	5	6	7	8
EQ, A/B/C/D	PD 0ohm	PD 0ohm	PD 0ohm	PD 0ohm	PD 0ohm	PD 0ohm	PD 0ohm	PD 0ohm
	PD 68Kohm	PD 68Kohm	PD 68Kohm	PD 68Kohm	PD 68Kohm	PD 68Kohm	PD 68Kohm	PD 68Kohm
FG, A/B/C/D	NC	NC	NC	NC	NC	NC	NC	NC
	PU 0ohm	PU 0ohm	PU 0ohm	PU 0ohm	PU 0ohm	PU 0ohm	PU 0ohm	PU 0ohm

Equalization Setting:

EQA/B/C/D are the selection pins for the equalization selection

	Equalizer setting (dB)	
EQA/B/C/D	*@2.5GHz*	*@5GHz*
0 (Tie 0Ω to GND)	5.1	10.9
R (Tie Rext to GND)	1.9	6.7
F (Leave Open)	3.5	8.9 (Default)
1 (Tie 0Ω to VDD)	6.8	13.1

Flat Gain Setting:

FGA/B/C/D are the selection pins for the DC gain

	Flat Gain Settings
FGA/B/C/D	*dB*
0 (Tie 0Ω to GND)	-3
R (Tie Rext to GND)	-1.5
F (Leave Open)	0 (Default)
1 (Tie 0Ω to VDD)	+2

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Front USB3.1 TypeA/TypeC

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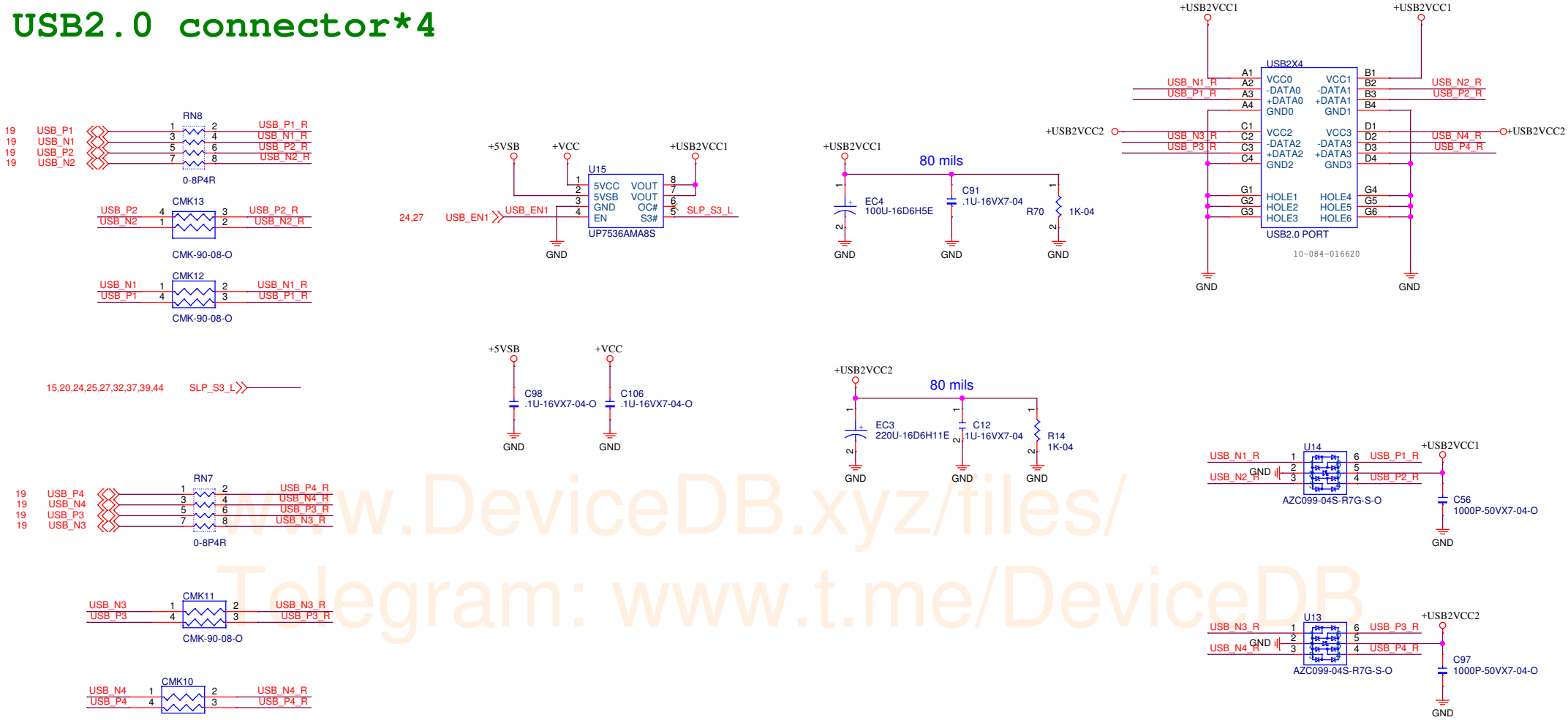
USB2.0 connector*4



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Title: USB2x4 Connector		
Size: B	Document Number: B36H4-AD	Rev: 1.1
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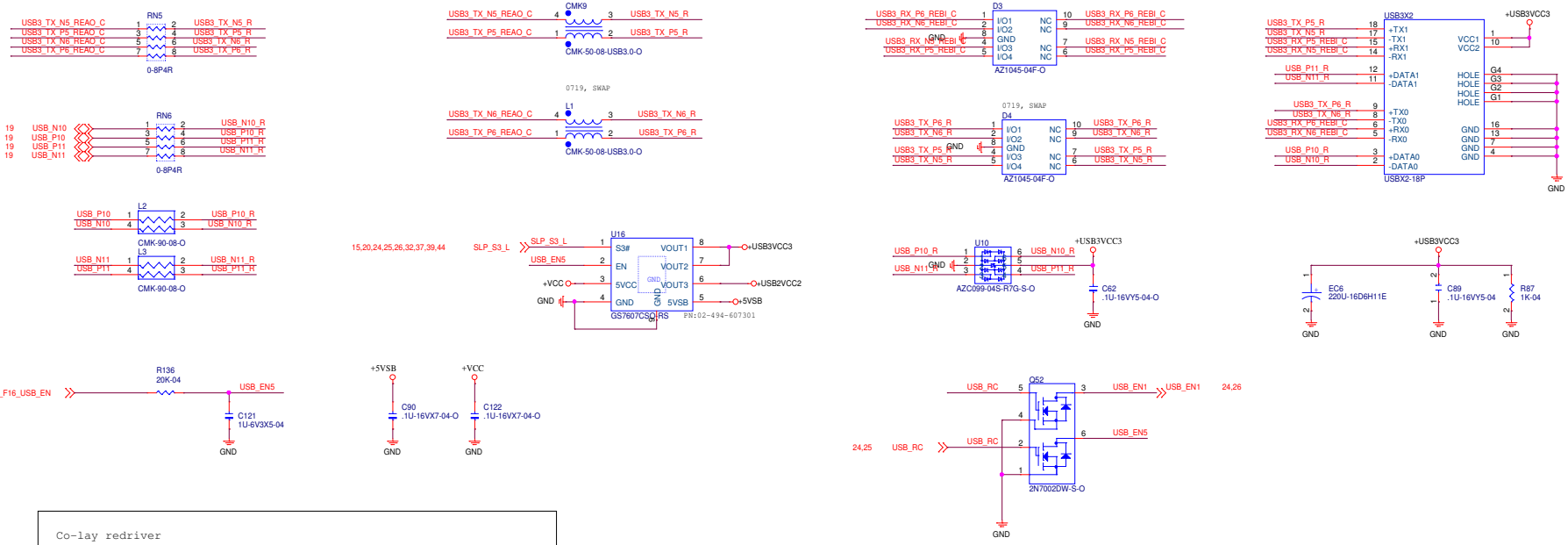

Note:
Pull High 4.7K Ohm
Pull Down 0 ohm

Strapping Table

SW_X	DE_X	Descriptions
0	0	-1.5dB
0	1	0dB
1	0	+1.5dB
1	1	+3dB

Elitegroup Computer Systems		
Title: USB3.0*2 Connector		
Size: C	Document Number: B36H4-AD	Rev: 1.1
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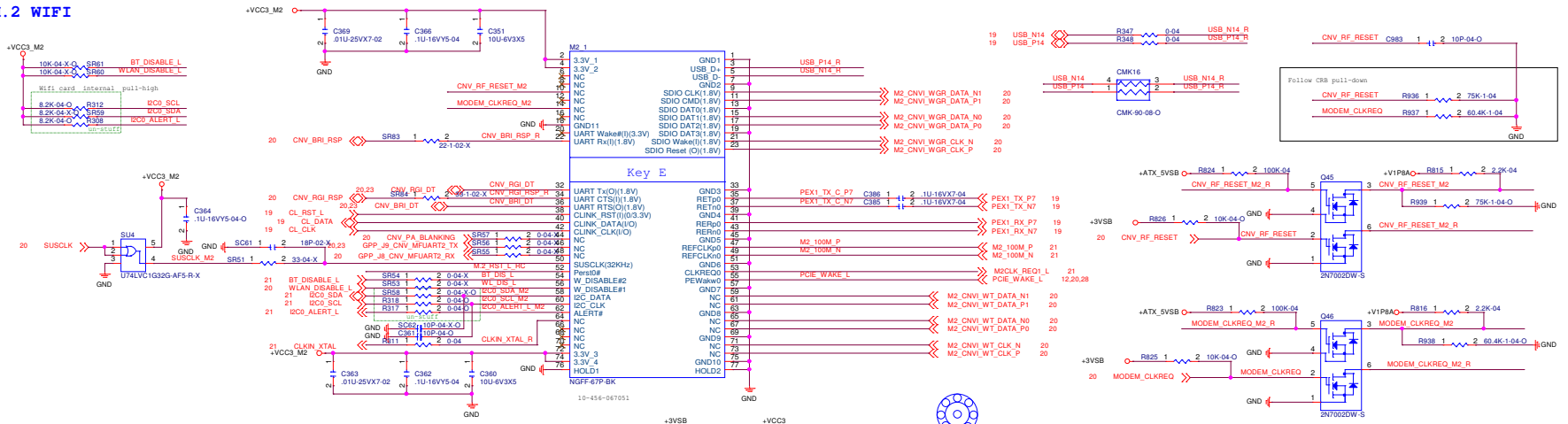
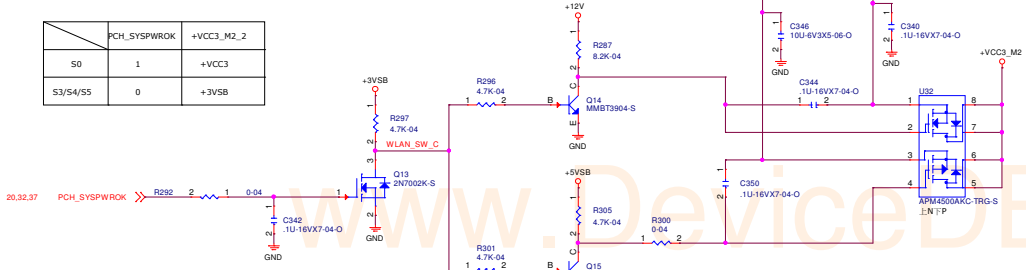
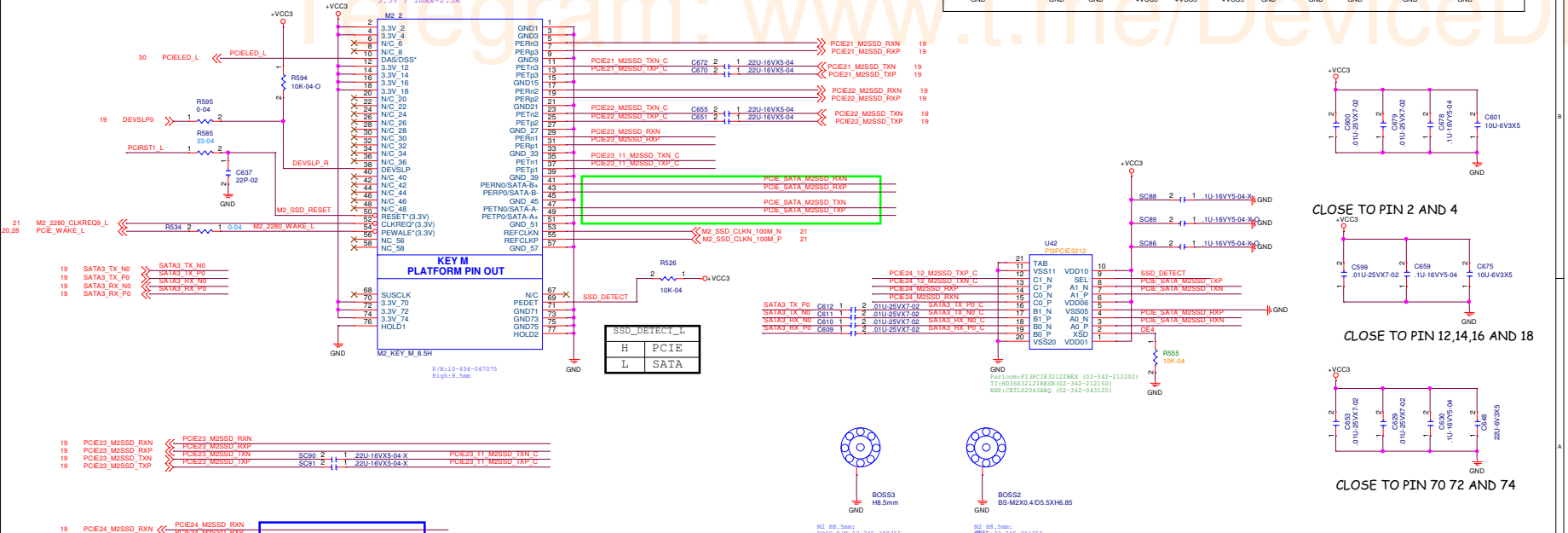
M.2 WIFI



	PCH_SYSPWROK	+VCC3_M2_2
S0	1	+VCC3
S3/S4/S5	0	+3VSB



M.2 SSD



SSD_DETECT_L	
H	PCIE
L	SATA

CLOSE TO PIN 2 AND 4

CLOSE TO PIN 12,14,16 AND 18

CLOSE TO PIN 70 72 AND 74

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Company	Elitegroup Computer Systems
Title	M.2 WLAN/SSD
Size / Custom	Document Number: B36H4-AD
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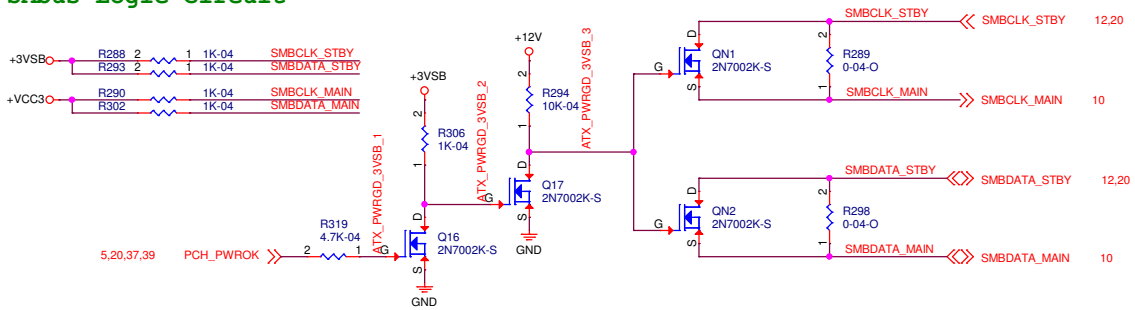
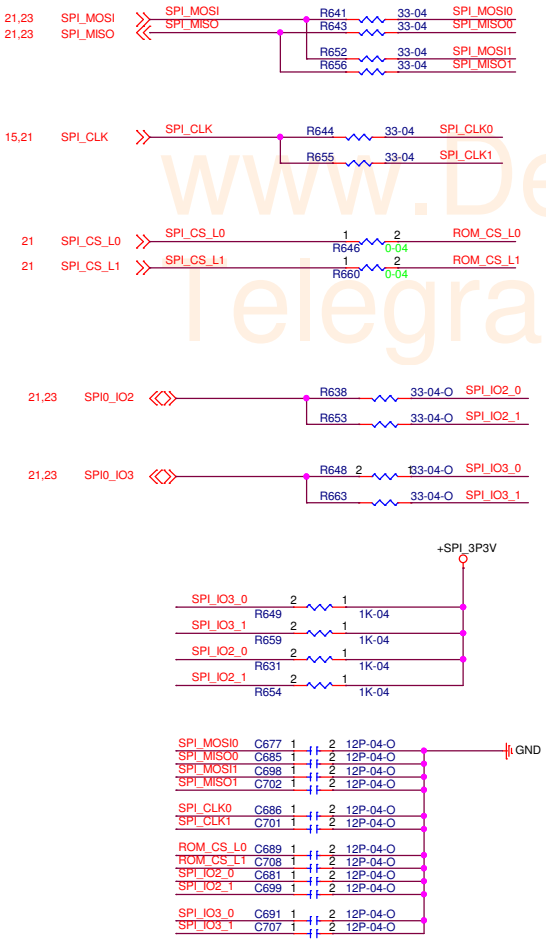
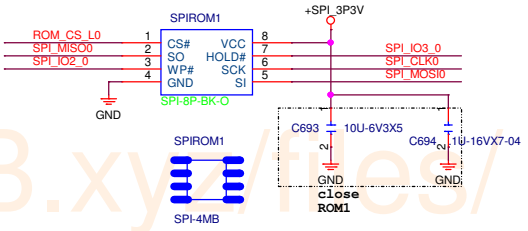
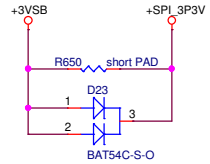
SMbus Logic Circuit

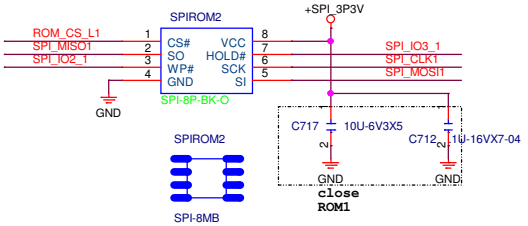


SPI ROM









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Title: SPI/SMbus			
Size: Custom	Document Number: B36H4-AD		Rev: 1.1
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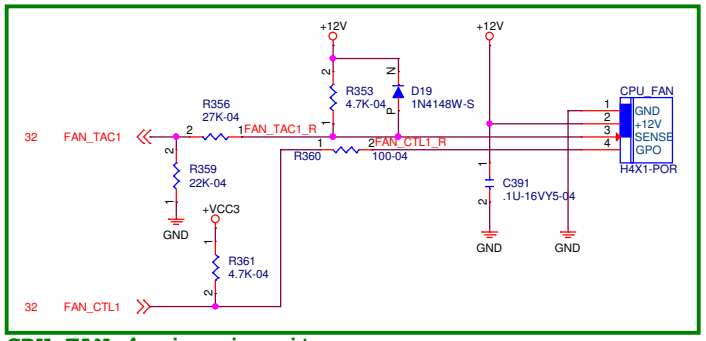
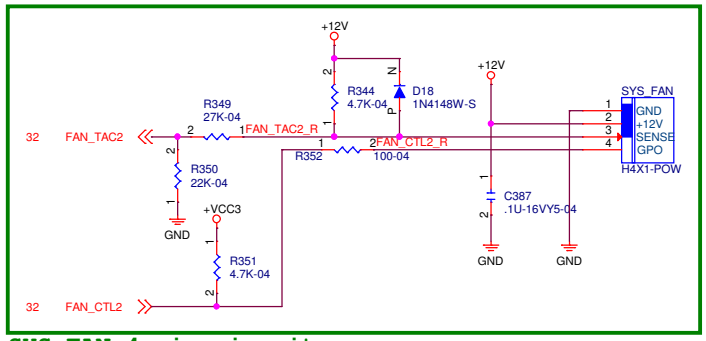
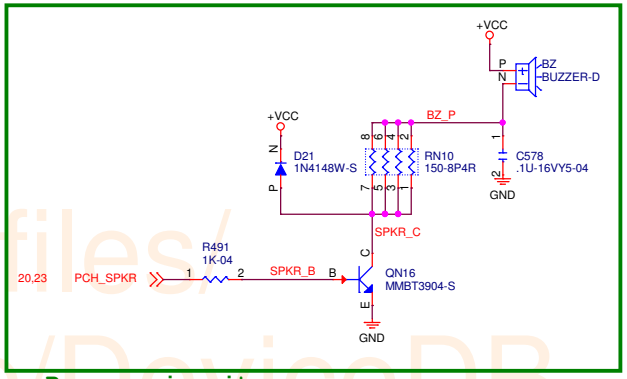


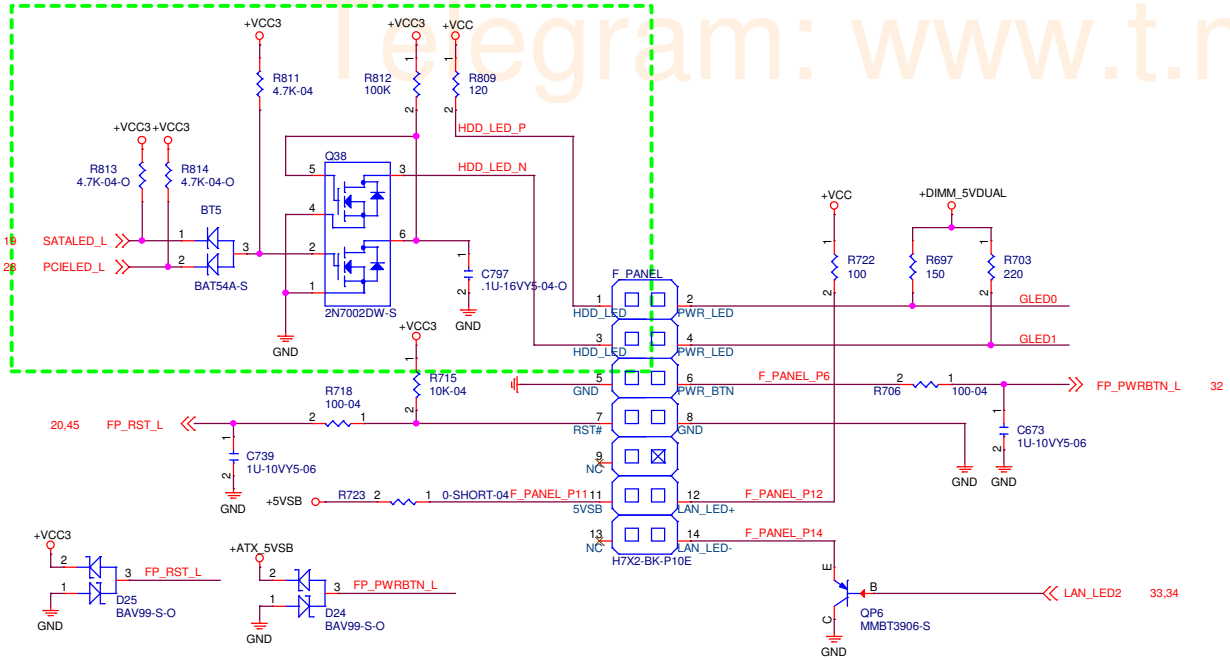
CPU_FAN 4 pin circuit



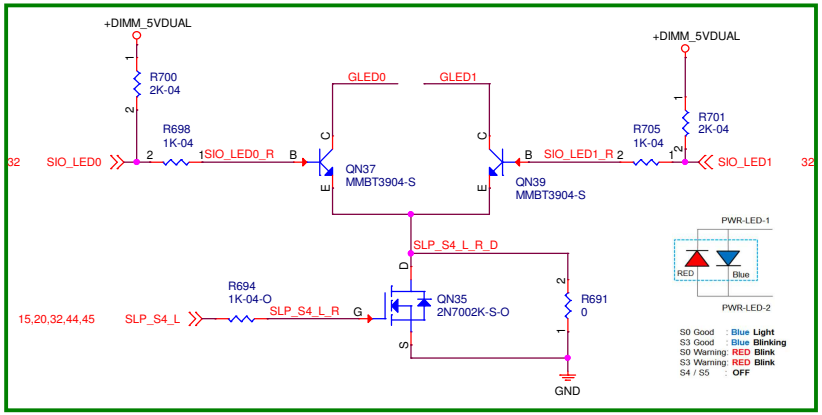
SYS_FAN 4 pin circuit



Buzzer circuit



Front Panel circuit



Power LED circuit

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Title: FAN/Buzzer/F_Panel		
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USB3.1 Gen2 connector re-driver IC

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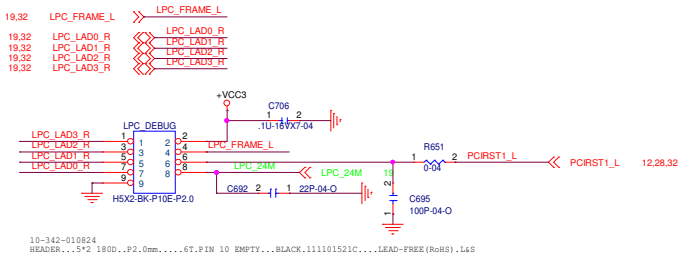
LPC_DEBUG header circuit



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Title: Gen2 Re-driver IC/LPC_debug		
Size: C	Document Number: B36H4-AD	Rev: 1.1
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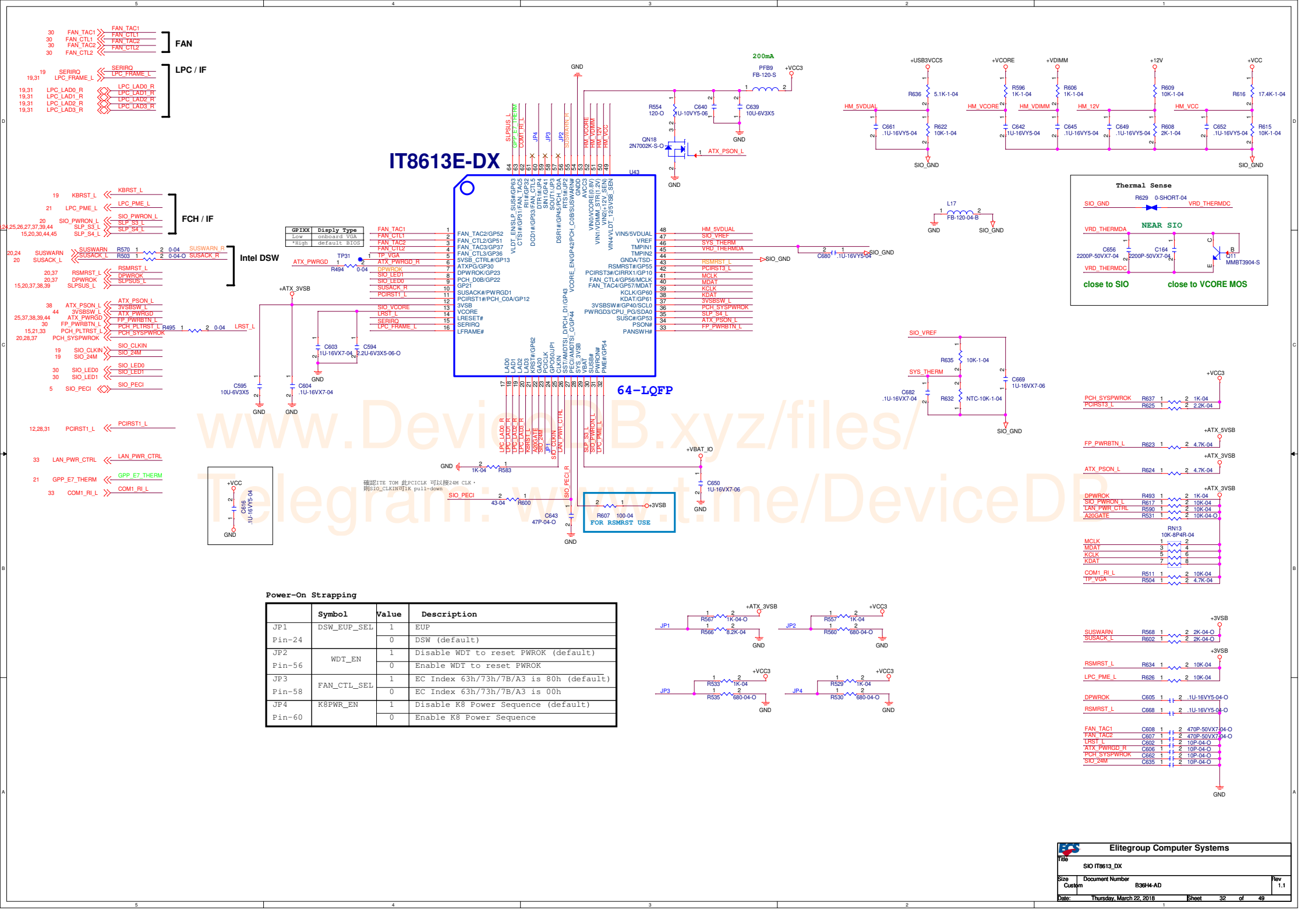

Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-24		0	DSW (default)
JP2	WDT_EN	1	Disable WDT to reset PWROK (default)
Pin-56		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/73h/7B/A3 is 80h (default)
Pin-58		0	EC Index 63h/73h/7B/A3 is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence (default)
Pin-60		0	Enable K8 Power Sequence

GPIXX	Disply Type
Low	onboard VGA
*High	default BIOS

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Title	SIO IT8613_DX
Size	Custom
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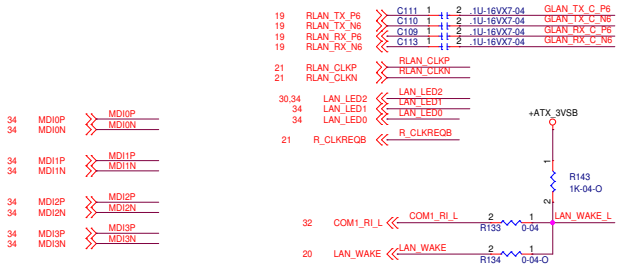
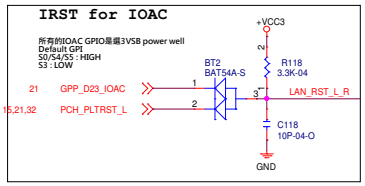
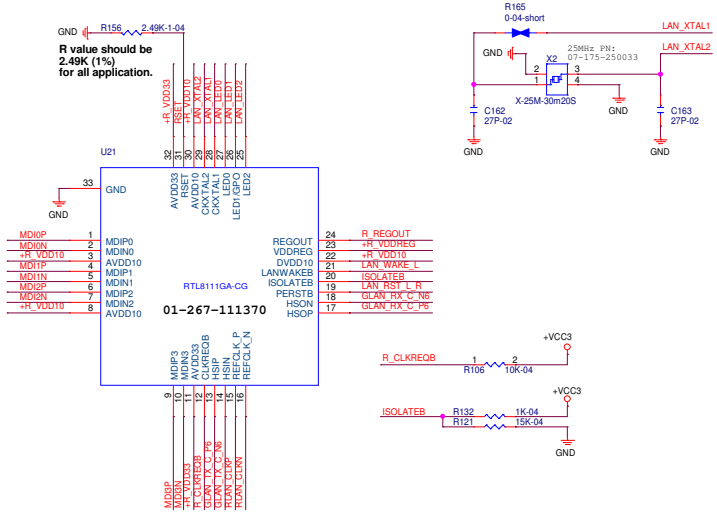
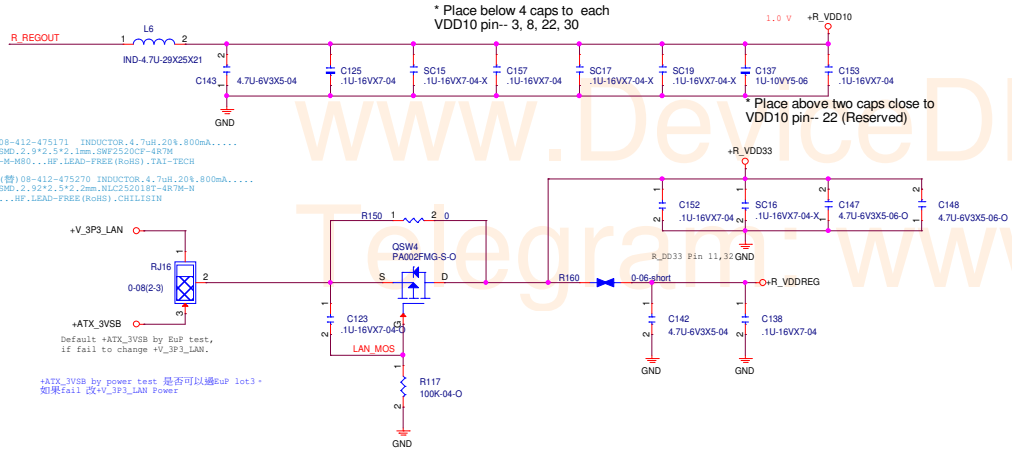






Internal Switching Regulator

8111GA:1V+-5% MAX 300mA



8. Power Sequence

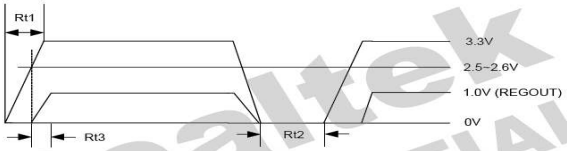


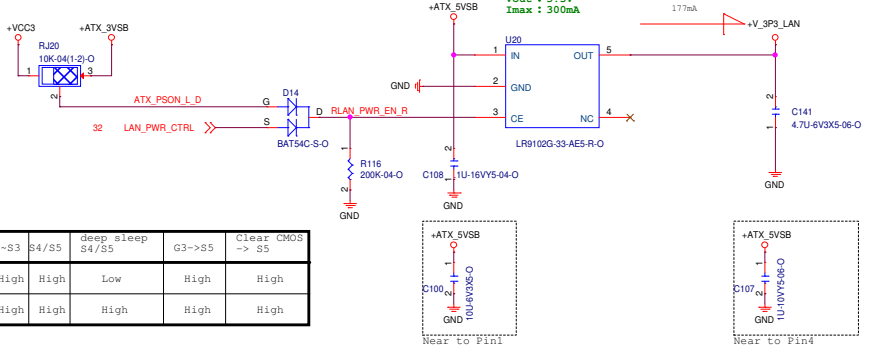
Figure 3. Power Sequence

Table 16. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time.	0.5	-	100	ms
Rt2	3.3V Off Time.	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time.	-	-	15	ms

Note: See the following section for power sequence requirements.

LAN Power Circuit by BIOS



LAN_PWR_CTRL	S0~S3	S4/S5	deep sleep S4/S5	G3->S5	Clear CMOS -> S5
No WoL	High	High	Low	High	High
WoL	High	High	High	High	High

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Realtek CONFIDENTIAL 3

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Size: C	Document Number: B36H4-AD			Rev: 1.1
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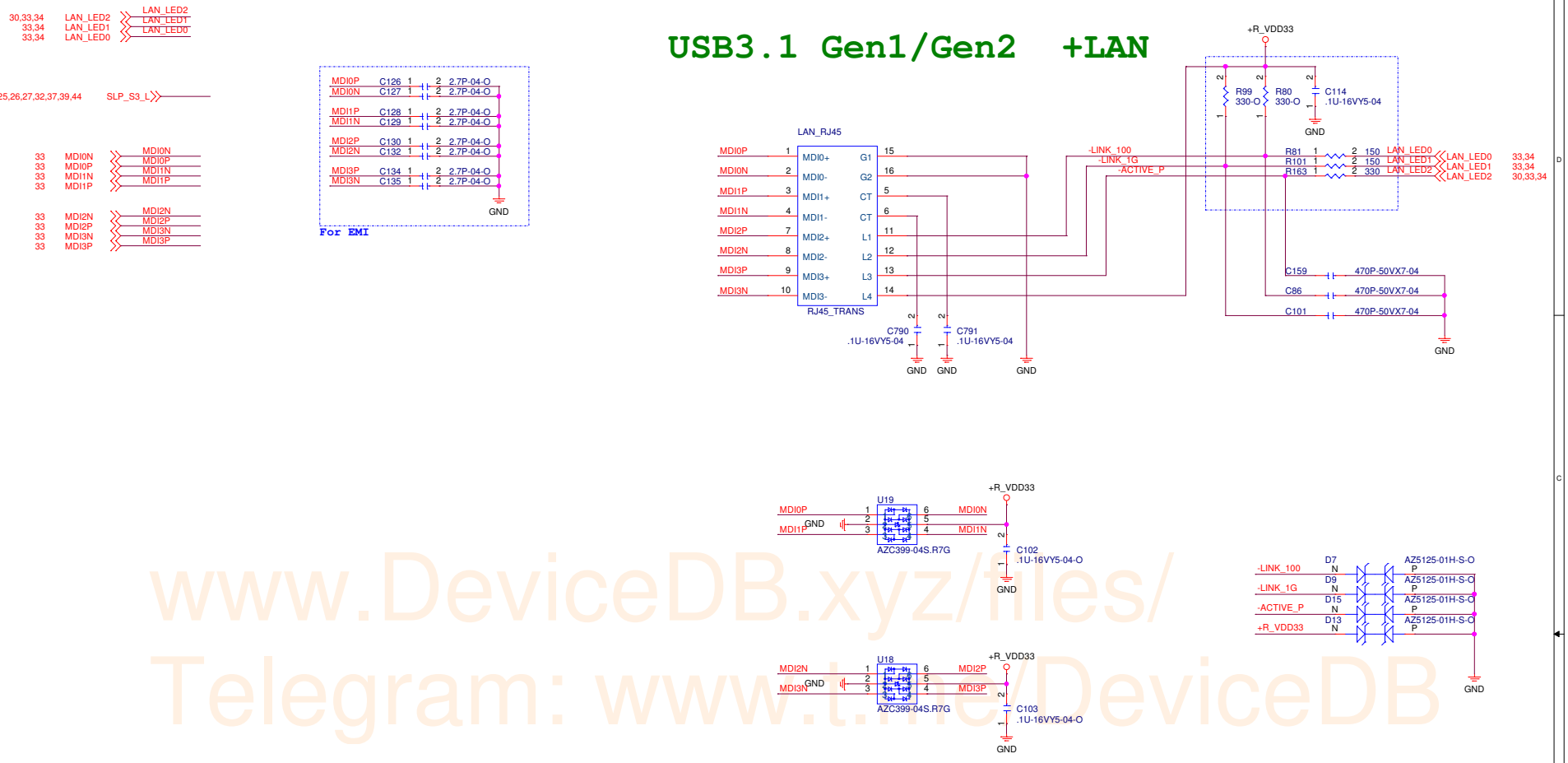
USB3.1 Gen1/Gen2 +LAN



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			S0	S3	S4	S5	G3 to S5
Rear Side (Active / Speed)	Active LED (Single Color)	Access	Blink	Blink	Blink	Blink	
		Not Access	OFF	OFF	OFF	OFF	
	Speed-LED (Dual Color)	Disconnected	OFF	OFF	OFF	OFF	
		1000: ON with Amber Color	ON				
		100: ON with Green Color	ON				
		10: OFF	OFF				

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Size: Custom	Document Number: B36H4-AD		Rev: 1.1
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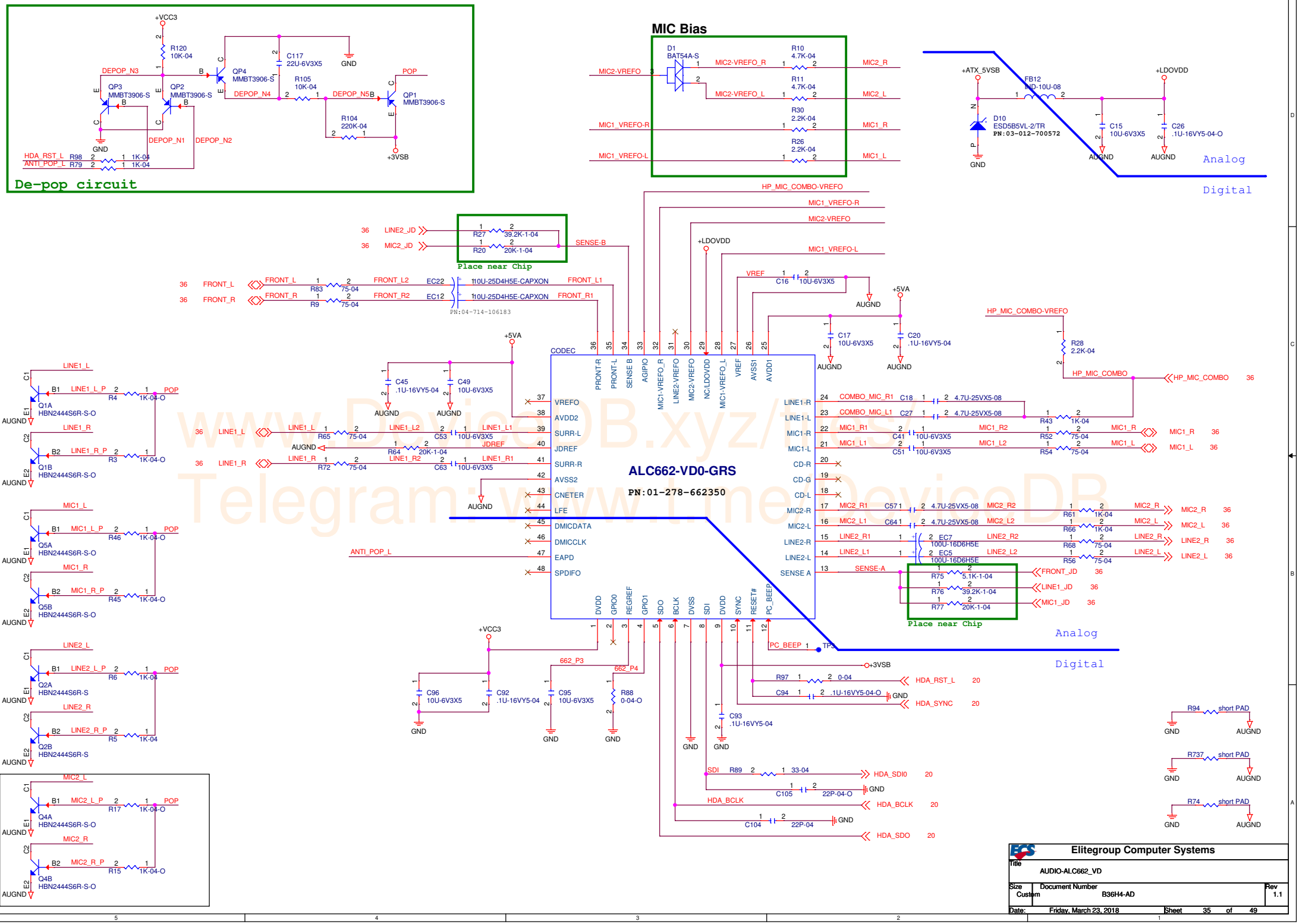

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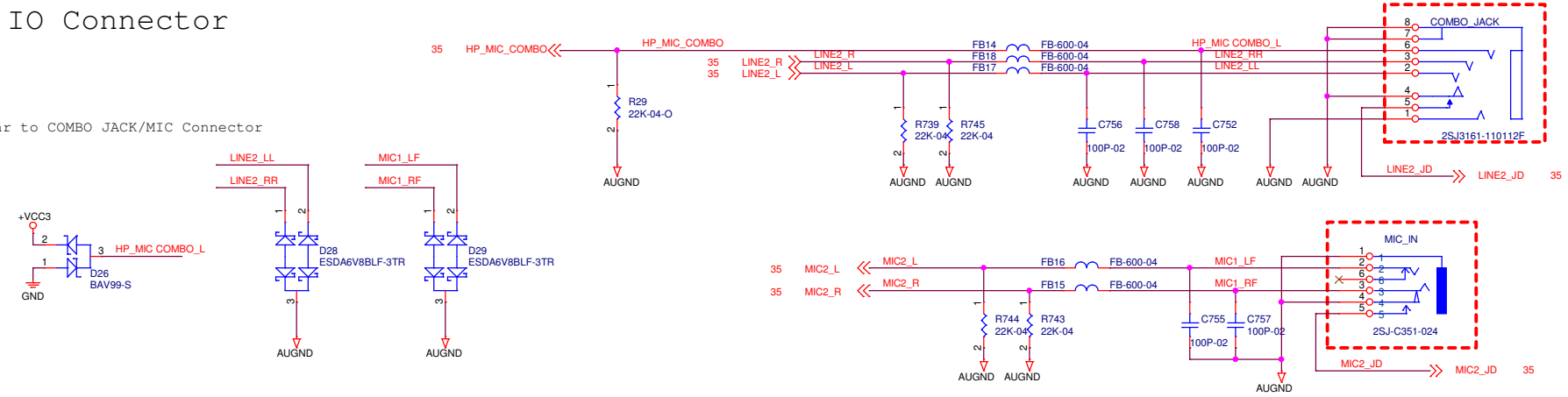
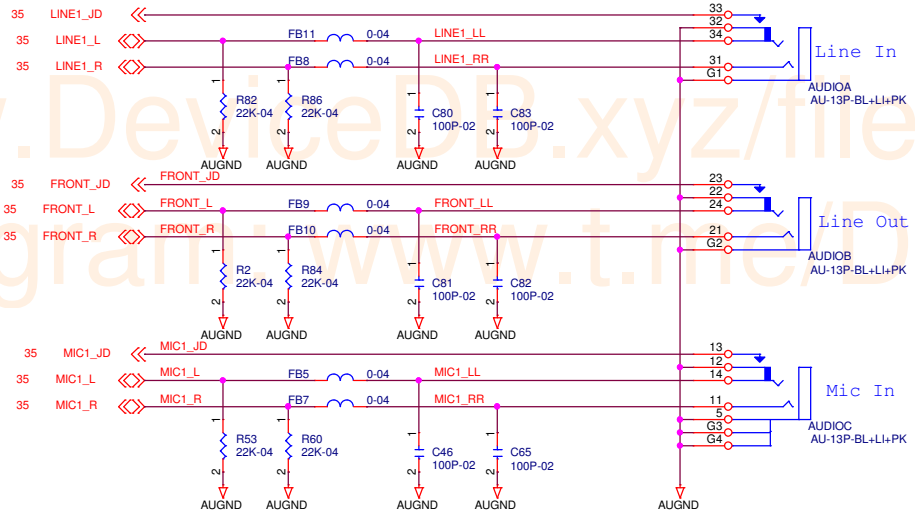
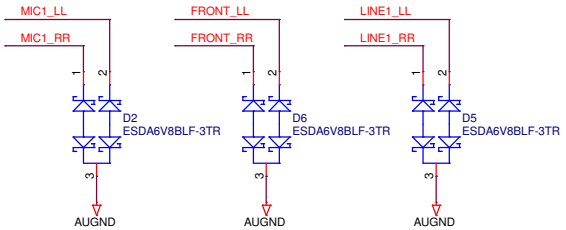
Front IO Connector

Near to COMBO JACK/MIC Connector





A	B	C
	PIN	FUNCTION
LINE IN	3Q	LINE IN-JD
	3P	AUGND
	31	LINE IN_L
	34	LINE IN_R
	G1	AUGND
LINE OUT	2Q	LINE OUT-JD
	2P	AUGND
	21	LINE OUT_L
	24	LINE OUT_R
	G2	AUGND
MIC IN	1Q	MIC IN-JD
	1P	AUGND
	11	MIC IN_L
	14	MIC IN_R
	5	AUGND



PN:03-100-700872
TVS ARRAY..ESDA6V8BLF-3/TR..SOT-23.5V.....LEAD-FREE(RoHS/HF).WILLSEMI

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Title	AUDIO-CONN
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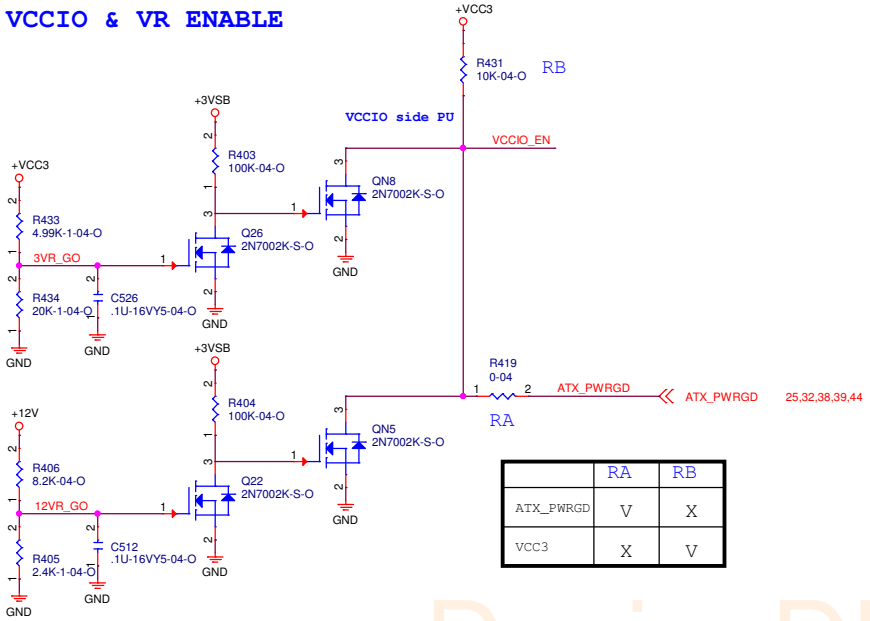
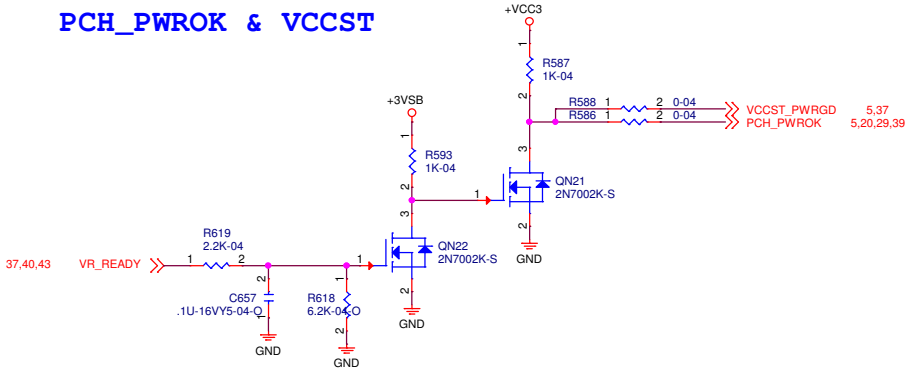
VCCIO & VR ENABLE

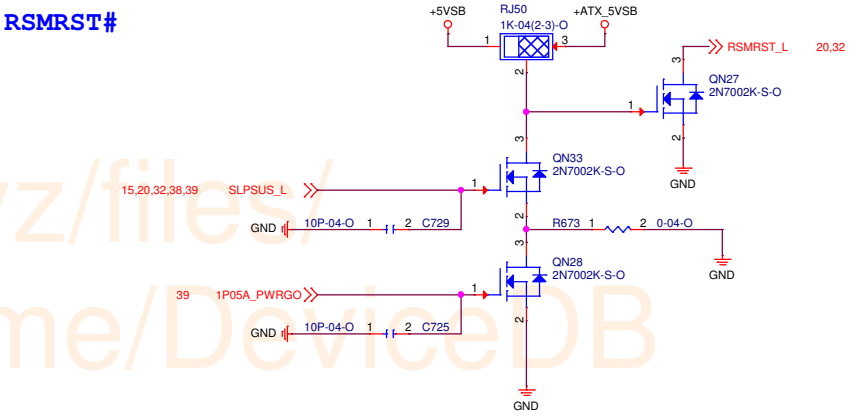


	RA	RB
ATX_PWRGD	V	X
VCC3	X	V

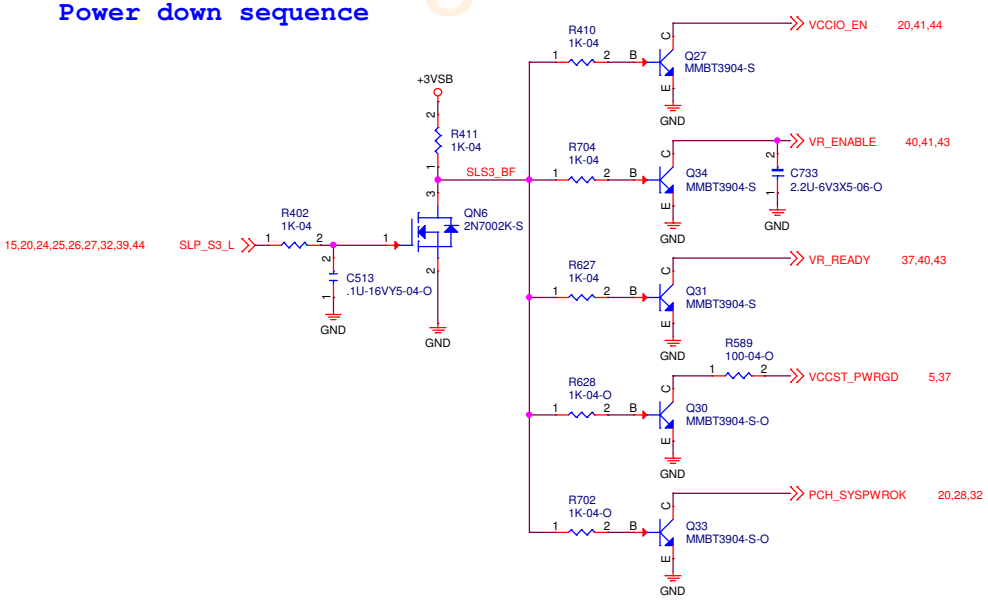
PCH_PWRROK & VCCST



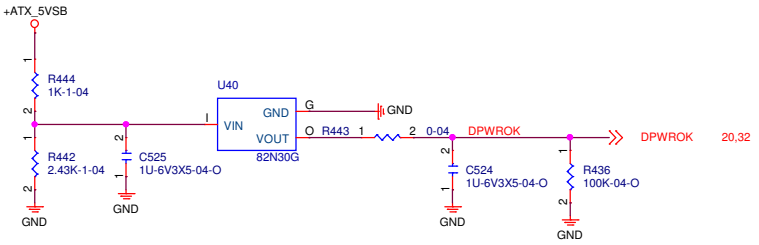
RSMRST#



Power down sequence



DPWROK



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Title	SEQUENCE circuit
Size: Custom	Document Number: B36H4-AD
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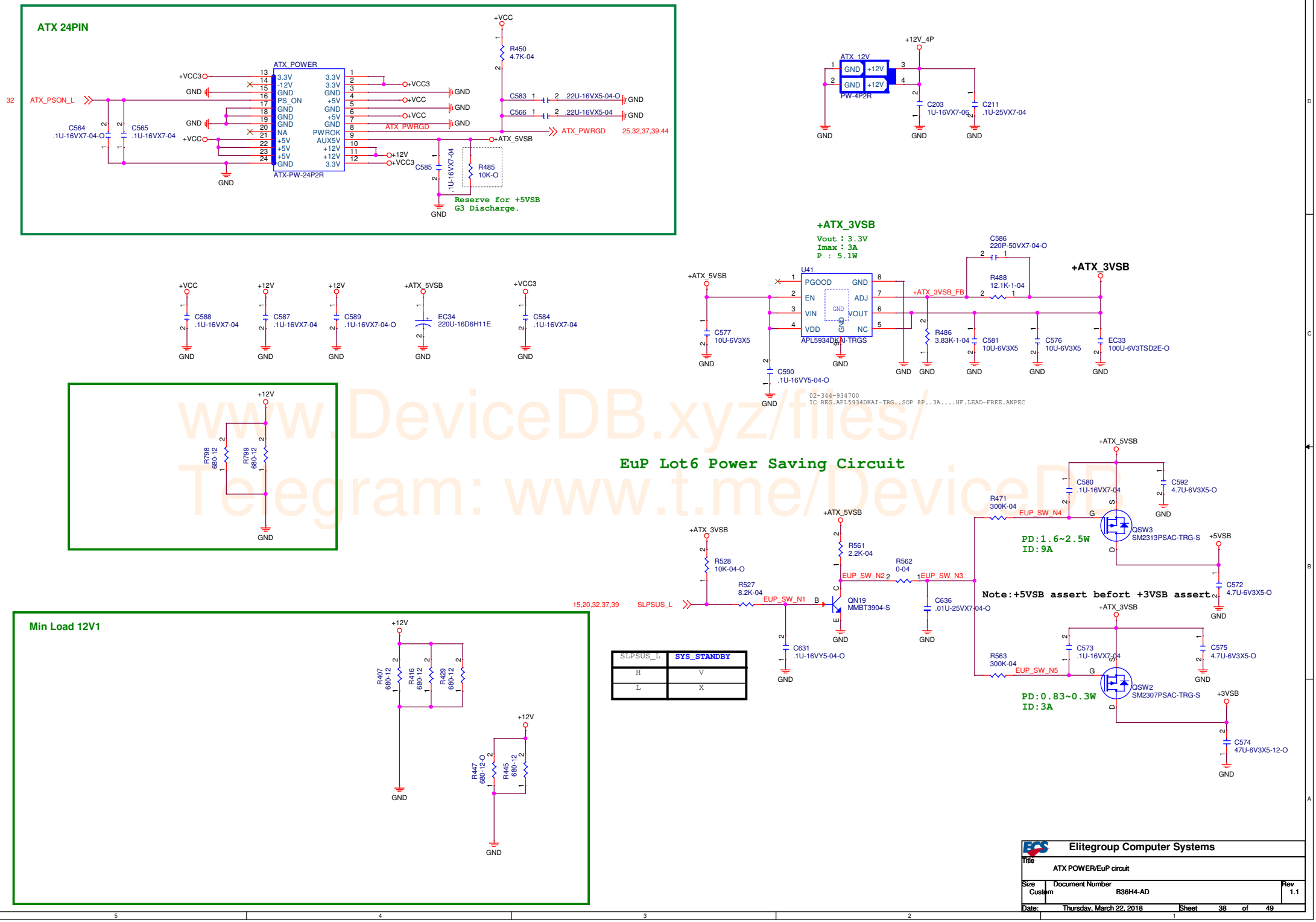

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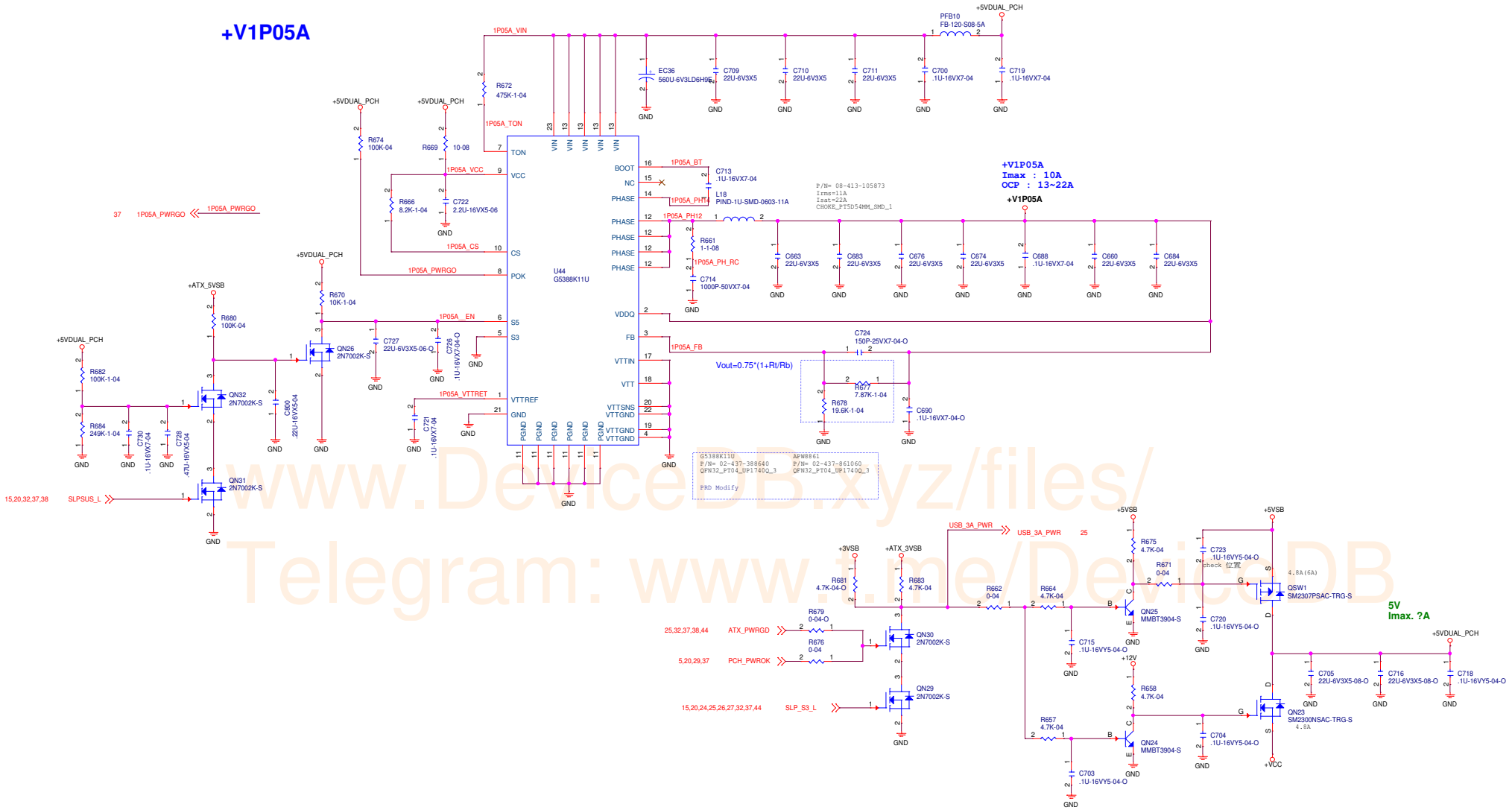
+V1P05A



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Title: DC/DC V1P05A		
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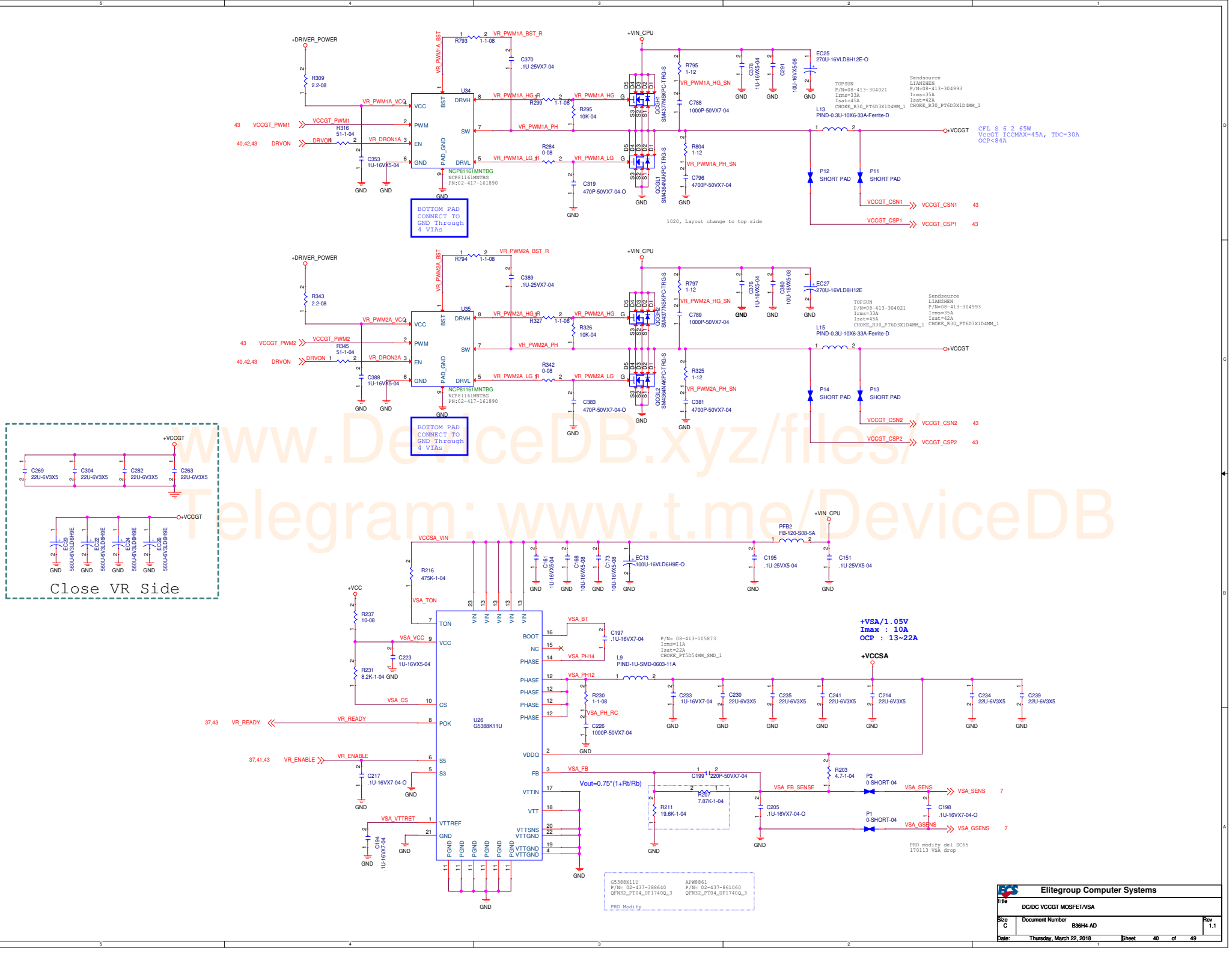

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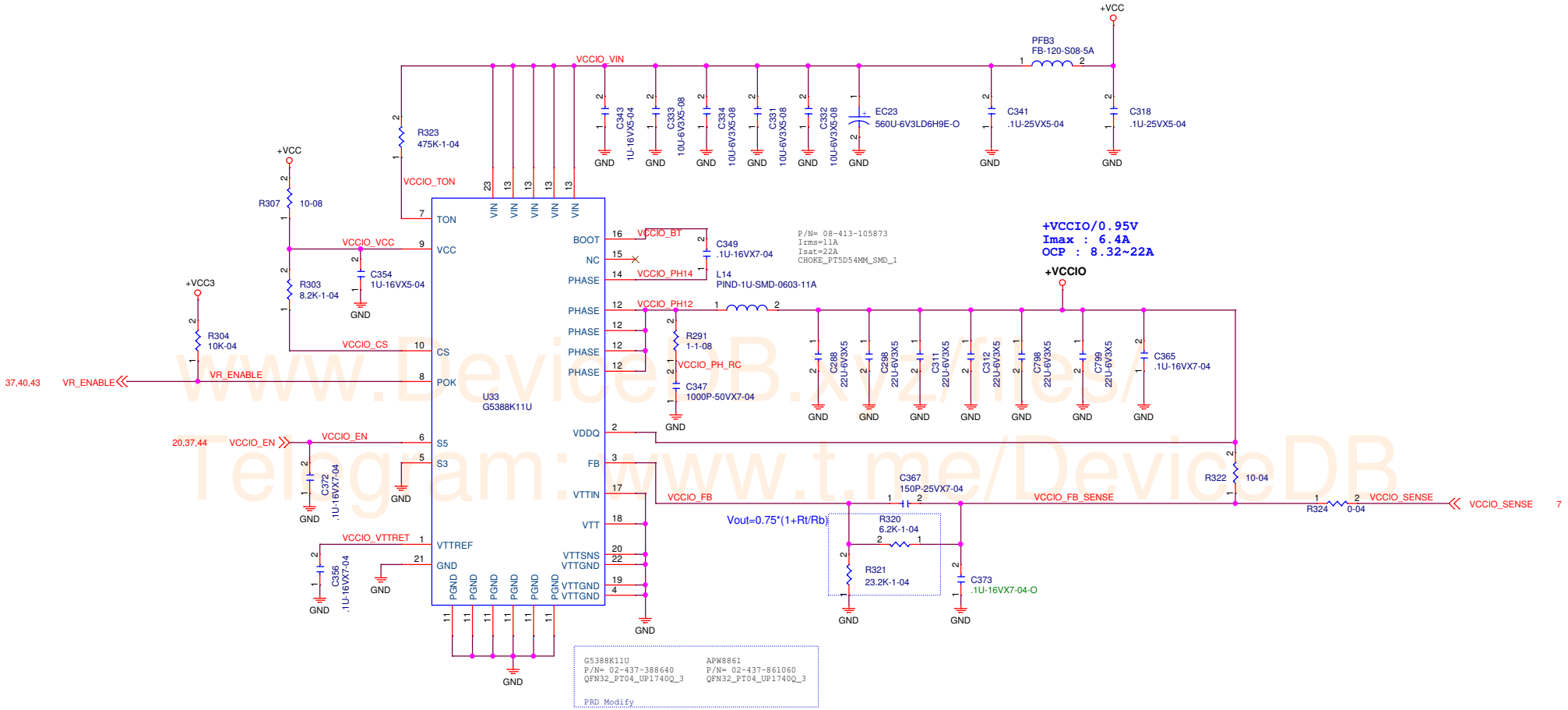

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Title: DC/DC VCCIO		
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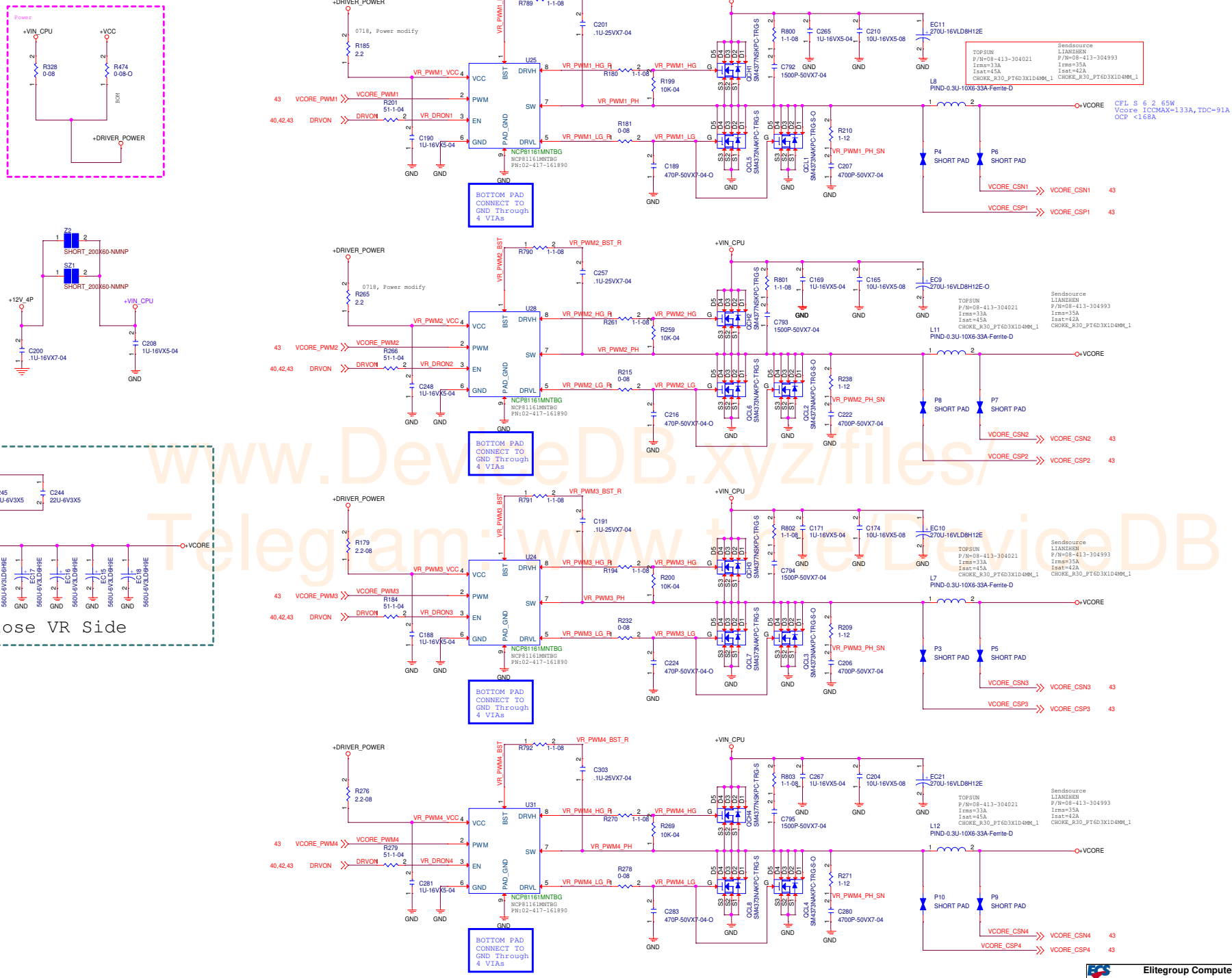

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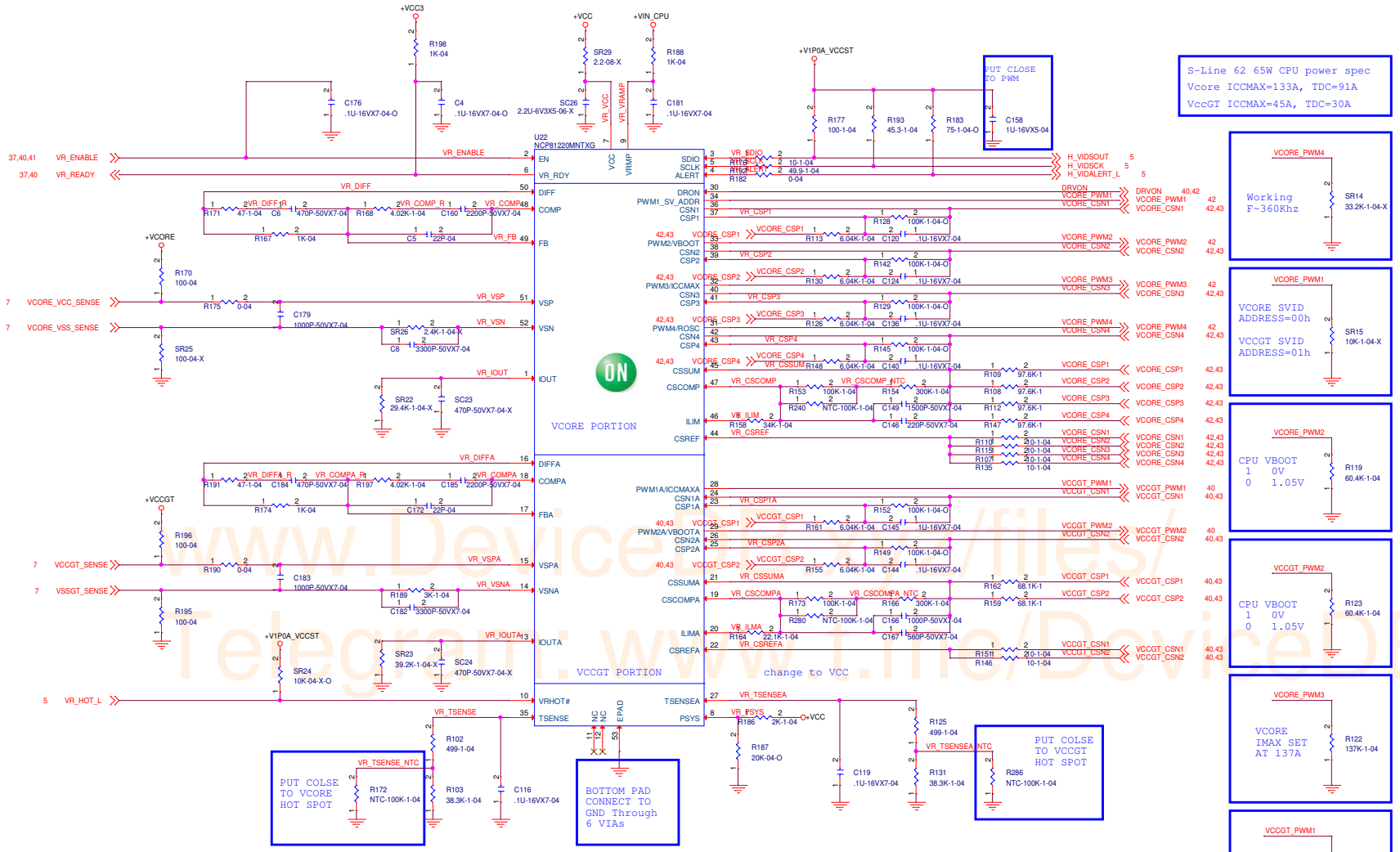
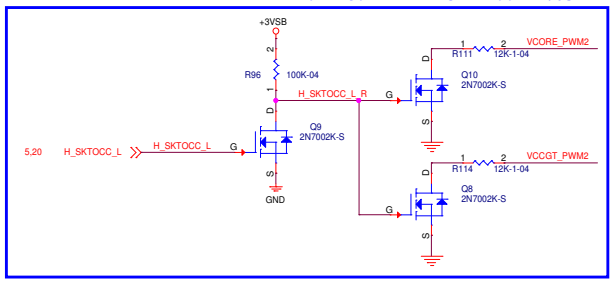


FOR VCORE AND VGT VBOOT=1.05V



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Title	C/DC VCORE/VCCGT PWM IC	
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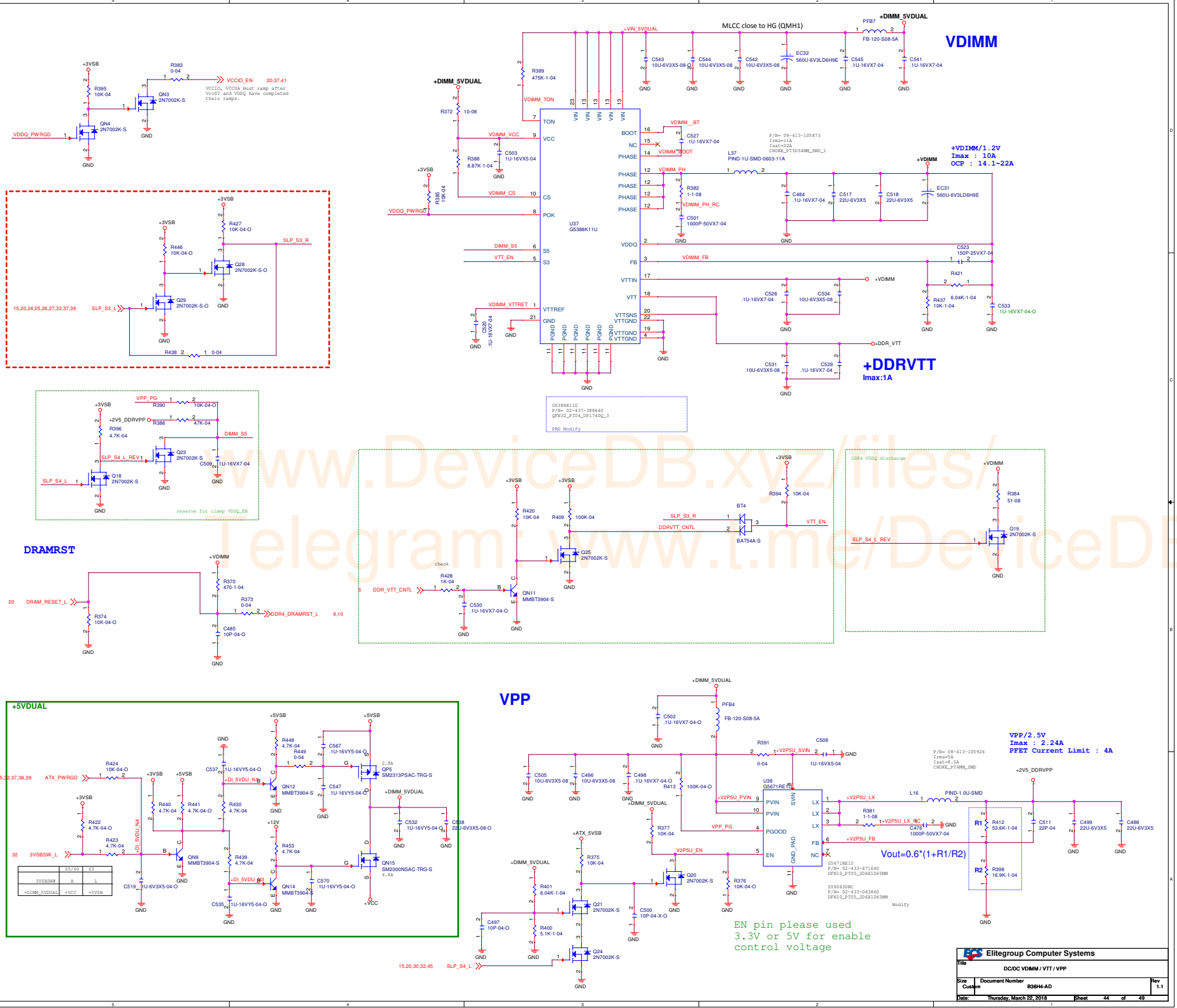

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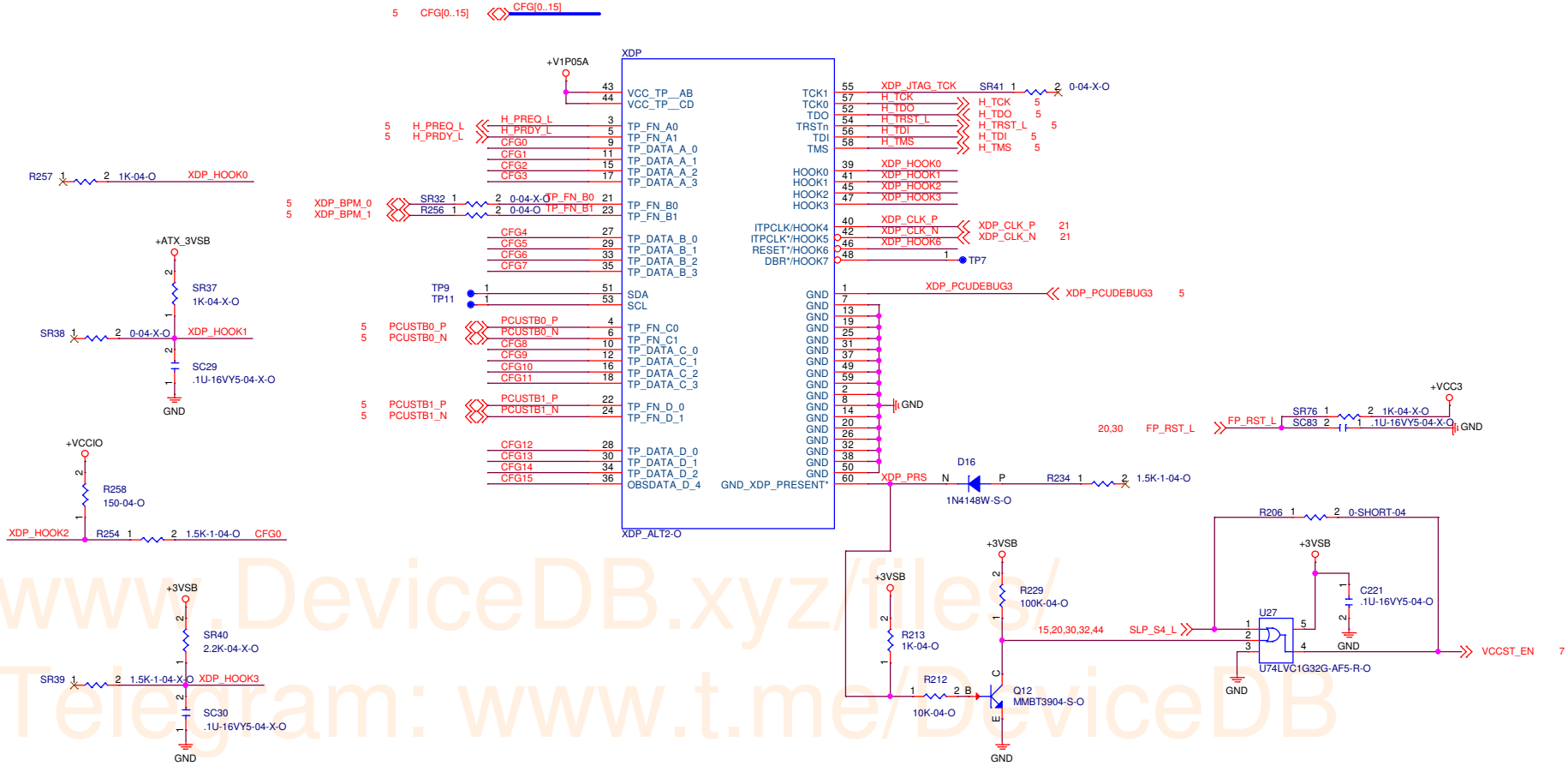

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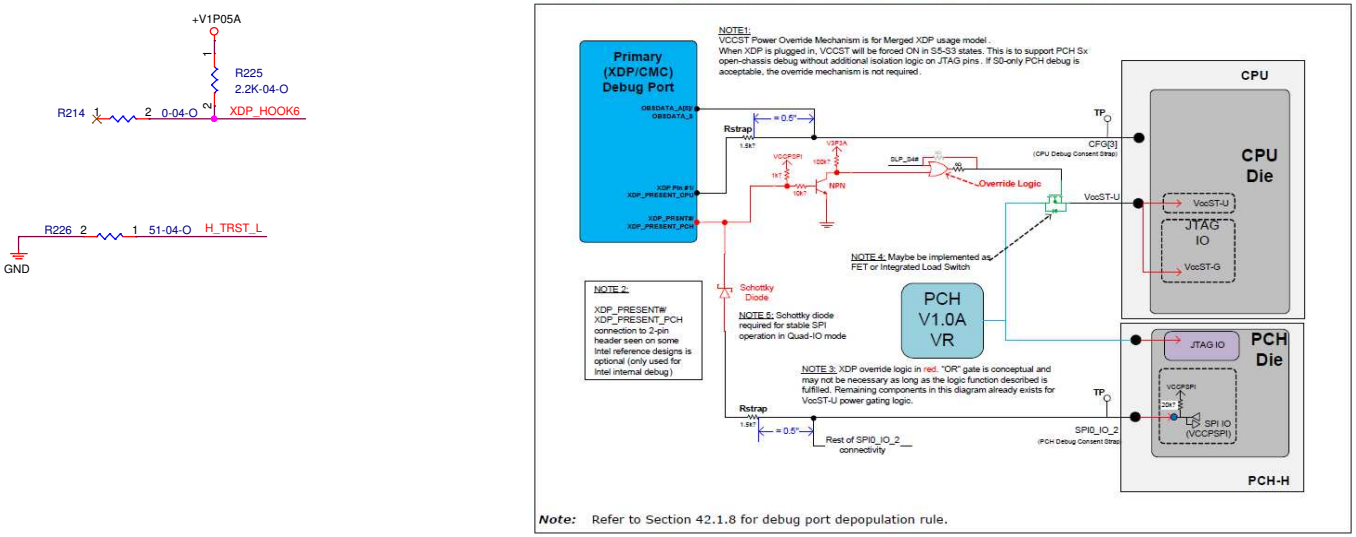
Figure 45-8. Primary Debug Port-XDP_PRESENT# Connectivity



Note: Refer to Section 42.1.8 for debug port depopulation rule.

Elitegroup Computer Systems			
Title: XDP			
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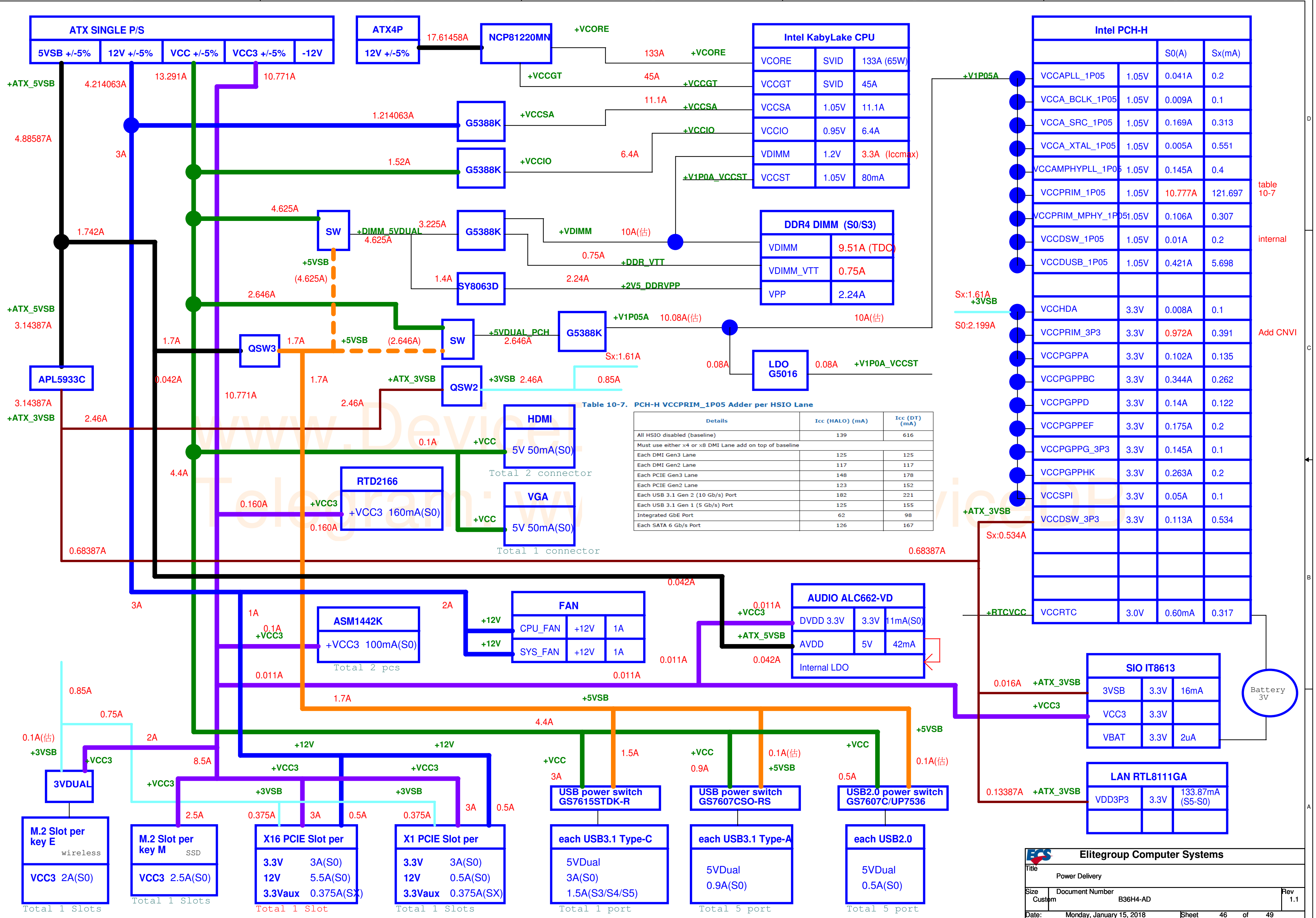

ATX SINGLE P/S
5VSB +/-5%
12V +/-5%
VCC +/-5%
VCC3 +/-5%
-12V
ATX4P
12V +/-5%
17.61458A
NCP81220MN
+VCORE
Intel KabyLake CPU
VCORE SVID 133A (65W)
VCCGT SVID 45A
VCCSA 1.05V 11.1A
VCCIO 0.95V 6.4A
VDIMM 1.2V 3.3A (Iccmax)
VCCST 1.05V 80mA
133A
45A
11.1A
6.4A
+VCCGT
+VCCSA
+VCCIO
+V1P0A_VCCST
G5388K
1.214063A
1.52A
SW
4.625A
+DIMM_5VDUAL
3.225A
+VDIMM
10A(估)
DDR4 DIMM (S0/S3)
VDIMM 9.51A (TDC)
VDIMM_VTT 0.75A
VPP 2.24A
+DDR_VTT
+2V5_DDRVPP
SY8063D
1.4A
2.24A
0.75A
+5VSB
(4.625A)
2.646A
QSW3
1.7A
(2.646A)
+5VDUAL_PCH
G5388K
+V1P05A
10.08A(估)
10A(估)
Sx:1.61A
LDO G5016
0.08A
+V1P0A_VCCST
QSW2
+ATX_3VSB
+3VSB 2.46A
0.85A
HDMI
5V 50mA(S0)
Total 2 connector
+VCC
0.1A
RTD2166
+VCC3 160mA(S0)
0.160A
VGA
5V 50mA(S0)
Total 1 connector
APL5933C
+ATX_5VSB
4.214063A
13.291A
10.771A
4.88587A
3A
1.742A
3.14387A
1.7A
0.042A
4.4A
2.46A
0.68387A
0.042A
Intel PCH-H
S0(A) Sx(mA)
VCCAPLL_1P05 1.05V 0.041A 0.2
VCCA_BCLK_1P05 1.05V 0.009A 0.1
VCCA_SRC_1P05 1.05V 0.169A 0.313
VCCA_XTAL_1P05 1.05V 0.005A 0.551
VCCAMPHYPLL_1P05 1.05V 0.145A 0.4
VCCPRIM_1P05 1.05V 10.777A 121.697
VCCPRIM_MPHY_1P05 1.05V 0.106A 0.307
VCCDSW_1P05 1.05V 0.01A 0.2
VCCDUSB_1P05 1.05V 0.421A 5.698
VCCHDA 3.3V 0.008A 0.1
VCCPRIM_3P3 3.3V 0.972A 0.391
VCCPGPPA 3.3V 0.102A 0.135
VCCPGPPBC 3.3V 0.344A 0.262
VCCPGPPD 3.3V 0.14A 0.122
VCCPGPPEF 3.3V 0.175A 0.2
VCCPGPPG_3P3 3.3V 0.145A 0.1
VCCPGPPHK 3.3V 0.263A 0.2
VCCSPI 3.3V 0.05A 0.1
VCCDSW_3P3 3.3V 0.113A 0.534
VCCRTC 3.0V 0.60mA 0.317
table 10-7
internal
Add CNVI
Sx:1.61A +3VSB
S0:2.199A
Sx:0.534A
+RTCVCC
AUDIO ALC662-VD
DVDD 3.3V 3.3V 11mA(S0)
AVDD 5V 42mA
Internal LDO
0.011A
SIO IT8613
3VSB 3.3V 16mA
VCC3 3.3V
VBAT 3.3V 2uA
Battery 3V
0.016A
LAN RTL8111GA
VDD3P3 3.3V 133.87mA (S5-S0)
0.13387A
ASM1442K
+VCC3 100mA(S0)
Total 2 pcs
FAN
CPU_FAN +12V 1A
SYS_FAN +12V 1A
+12V
2A
1A
0.1A
0.85A
0.75A
0.1A(估)
8.5A
2.5A
0.375A
0.5A
3VDUAL
M.2 Slot per key E
wireless
VCC3 2A(S0)
Total 1 Slots
M.2 Slot per key M
SSD
VCC3 2.5A(S0)
Total 1 Slots
X16 PCIE Slot per
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A(SX)
Total 1 Slot
X1 PCIE Slot per
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A(SX)
Total 1 Slots
USB power switch GS7615STDK-R
USB power switch GS7607CSO-RS
USB2.0 power switch GS7607C/UP7536
1.5A
0.9A
0.1A(估)
each USB3.1 Type-C
5VDual
3A(S0)
1.5A(S3/S4/S5)
Total 1 port
each USB3.1 Type-A
5VDual
0.9A(S0)
Total 5 port
each USB2.0
5VDual
0.5A(S0)
Total 5 port

Table 10-7. PCH-H VCCPRIM_1P05 Adder per HSIO Lane

Details	Icc (HALO) (mA)	Icc (DT) (mA)
All HSIO disabled (baseline)	139	616
Must use either x4 or x8 DMI Lane add on top of baseline		
Each DMI Gen3 Lane	125	125
Each DMI Gen2 Lane	117	117
Each PCIE Gen3 Lane	148	178
Each PCIE Gen2 Lane	123	152
Each USB 3.1 Gen 2 (10 Gb/s) Port	182	221
Each USB 3.1 Gen 1 (5 Gb/s) Port	125	155
Integrated GbE Port	62	98
Each SATA 6 Gb/s Port	126	167

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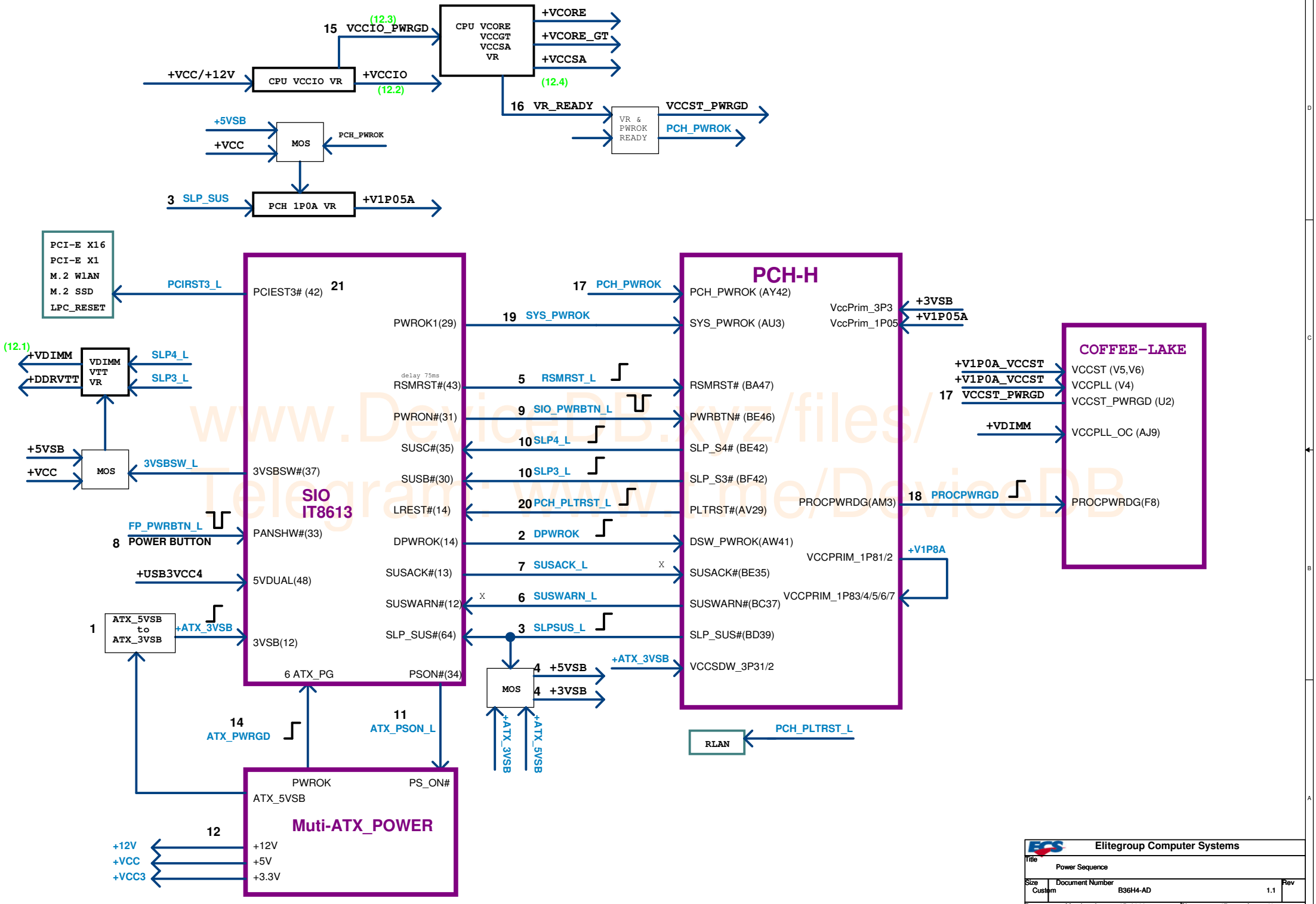

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Elitegroup Computer Systems			
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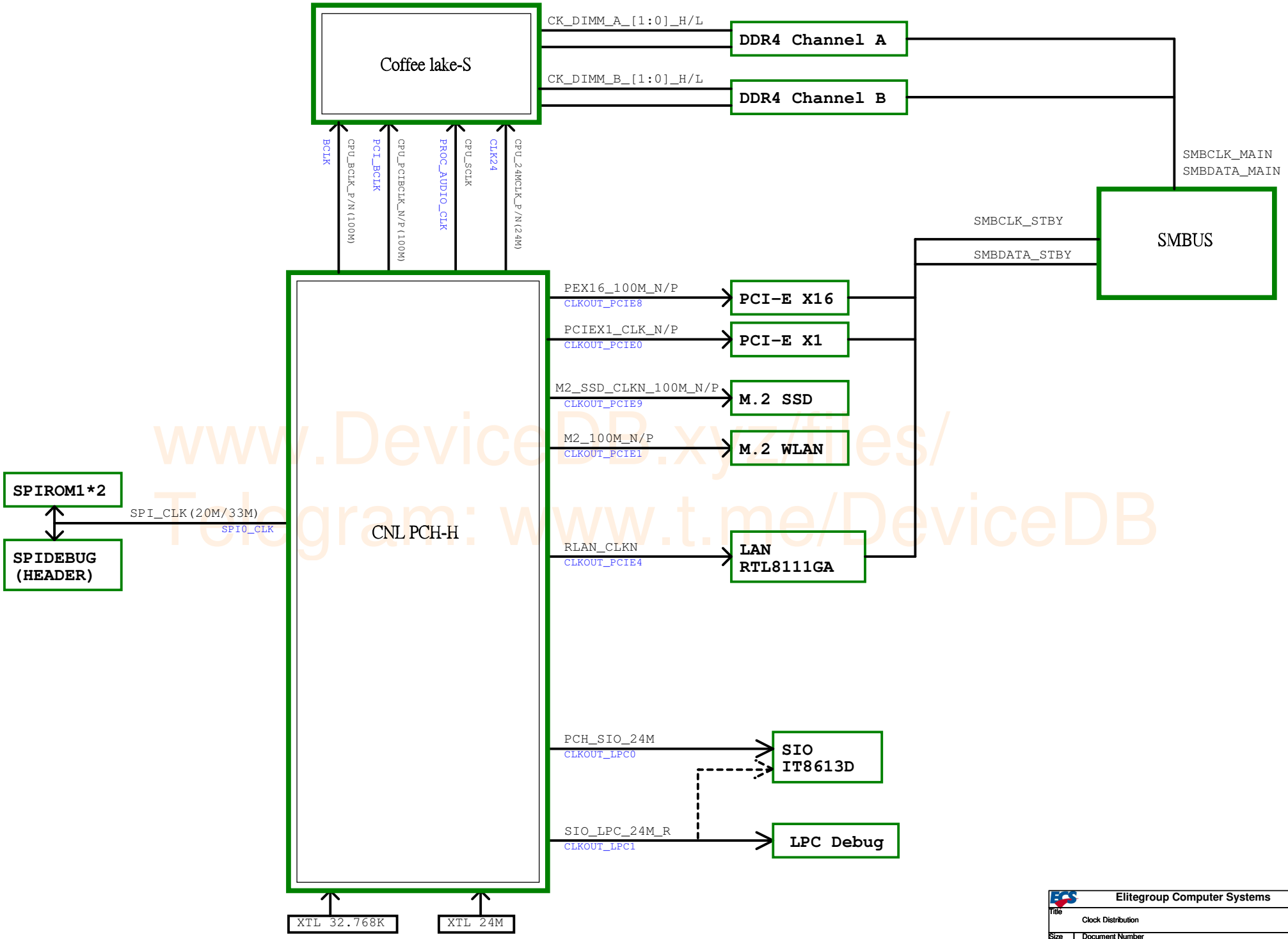

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