

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J113 MLB SCHEMATIC

10 / 03 / 14

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

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ALIASES RESOLVED

Schematic / PCB #'s


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00385	1	SCHEM_MLB,,743A	SCH	CRITICAL	
820-00165	1	PCBF_MLB,,743	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Oct 3 11:36:00 2014

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE
NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE		<PART_DESCRIPTION>	
	Apple Inc.		DRAWING NUMBER <SCH_NUM>
			SIZE D
		REVISION <E4LABEL>	
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BOM Variants						Alternate Parts																																																																																											
<table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>639-00623</td><td>PCBA,MLB,BEST,HY-4GB,X430</td><td>MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_4GB,ALTERNATE</td></tr><tr><td>639-00624</td><td>PCBA,MLB,BEST,HY-8GB,X433</td><td>MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_8GB,ALTERNATE</td></tr><tr><td>639-00625</td><td>PCBA,MLB,BEST,HY-16GB,X433</td><td>MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_16GB</td></tr><tr><td>639-00626</td><td>PCBA,MLB,BEST,SM-4GB,X433</td><td>MLB_CMNPTS,CPU:2.1GHZ,DDR3:SAMSUNG_4GB,ALTERNATE</td></tr><tr><td>639-00627</td><td>PCBA,MLB,BEST,SM-8GB,X433</td><td>MLB_CMNPTS,CPU:2.1GHZ,DDR3:SAMSUNG_8GB,ALTERNATE</td></tr><tr><td>639-00628</td><td>PCBA,MLB,BEST,MI-4GB,X433</td><td>MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_4GB</td></tr><tr><td>639-00629</td><td>PCBA,MLB,BEST,MI-8GB,X433</td><td>MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_8GB</td></tr><tr><td>639-00630</td><td>PCBA,MLB,BEST,MI-16GB,X433</td><td>MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_16GB</td></tr><tr><td>639-00631</td><td>PCBA,MLB,BEST,EL-4GB,X433</td><td>MLB_CMNPTS,CPU:2.1GHZ,DDR3:ELPIDA_4GB</td></tr><tr><td>639-00632</td><td>PCBA,MLB,BEST,EL-8GB,X433</td><td>MLB_CMNPTS,CPU:2.1GHZ,DDR3:ELPIDA_8GB</td></tr><tr><td>639-00633</td><td>PCBA,MLB,BETTER,HY-4GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_4GB,ALTERNATE</td></tr><tr><td>639-00634</td><td>PCBA,MLB,BETTER,HY-8GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_8GB,ALTERNATE</td></tr><tr><td>639-00635</td><td>PCBA,MLB,BETTER,HY-16GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_16GB</td></tr><tr><td>639-00636</td><td>PCBA,MLB,BETTER,SM-4GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_4GB,ALTERNATE</td></tr><tr><td>639-00637</td><td>PCBA,MLB,BETTER,SM-8GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_8GB,ALTERNATE</td></tr><tr><td>639-00638</td><td>PCBA,MLB,BETTER,MI-4GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_4GB</td></tr><tr><td>639-00639</td><td>PCBA,MLB,BETTER,MI-8GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_8GB</td></tr><tr><td>639-00640</td><td>PCBA,MLB,BETTER,MI-16GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_16GB</td></tr><tr><td>639-00641</td><td>PCBA,MLB,BETTER,EL-4GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_4GB</td></tr><tr><td>639-00642</td><td>PCBA,MLB,BETTER,EL-8GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_8GB</td></tr><tr><td>685-00046</td><td>CMN PTS,PCBA,MLB,X433</td><td>MLB_COMMON,J113_MLB</td></tr><tr><td>685-00047</td><td>VCORE FET,REN,X433</td><td>VCORE_FET:REN</td></tr><tr><td>685-00048</td><td>VCORE FET,VSHY,X433</td><td>VCORE_FET:VSHY</td></tr><tr><td>639-00697</td><td>PCBA,MLB,BETTER,EL-16GB,X433</td><td>MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_16GB</td></tr></table>						BOM NUMBER	BOM NAME	BOM OPTIONS	639-00623	PCBA,MLB,BEST,HY-4GB,X430	MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_4GB,ALTERNATE	639-00624	PCBA,MLB,BEST,HY-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_8GB,ALTERNATE	639-00625	PCBA,MLB,BEST,HY-16GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:HYNIX_16GB	639-00626	PCBA,MLB,BEST,SM-4GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:SAMSUNG_4GB,ALTERNATE	639-00627	PCBA,MLB,BEST,SM-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:SAMSUNG_8GB,ALTERNATE	639-00628	PCBA,MLB,BEST,MI-4GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_4GB	639-00629	PCBA,MLB,BEST,MI-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_8GB	639-00630	PCBA,MLB,BEST,MI-16GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:MICRON_16GB	639-00631	PCBA,MLB,BEST,EL-4GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:ELPIDA_4GB	639-00632	PCBA,MLB,BEST,EL-8GB,X433	MLB_CMNPTS,CPU:2.1GHZ,DDR3:ELPIDA_8GB	639-00633	PCBA,MLB,BETTER,HY-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_4GB,ALTERNATE	639-00634	PCBA,MLB,BETTER,HY-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_8GB,ALTERNATE	639-00635	PCBA,MLB,BETTER,HY-16GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_16GB	639-00636	PCBA,MLB,BETTER,SM-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_4GB,ALTERNATE	639-00637	PCBA,MLB,BETTER,SM-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_8GB,ALTERNATE	639-00638	PCBA,MLB,BETTER,MI-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_4GB	639-00639	PCBA,MLB,BETTER,MI-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_8GB	639-00640	PCBA,MLB,BETTER,MI-16GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:MICRON_16GB	639-00641	PCBA,MLB,BETTER,EL-4GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_4GB	639-00642	PCBA,MLB,BETTER,EL-8GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_8GB	685-00046	CMN PTS,PCBA,MLB,X433	MLB_COMMON,J113_MLB	685-00047	VCORE FET,REN,X433	VCORE_FET:REN	685-00048	VCORE FET,VSHY,X433	VCORE_FET:VSHY	639-00697	PCBA,MLB,BETTER,EL-16GB,X433	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_16GB	<table><tr><th>PART NUMBER</th><th>ALTERNATE FOR PART NUMBER</th><th>BOM OPTION</th><th>REF DES</th><th>COMMENTS:</th></tr><tr><td>685-00047</td><td>685-00048</td><td></td><td>ALL</td><td>Remove all to Vshy</td></tr></table> <table><tr><td>333S0704</td><td>333S0700</td><td></td><td>ALL</td><td>Replace (and mark all to Vshy)</td></tr></table>		PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	685-00047	685-00048		ALL	Remove all to Vshy	333S0704	333S0700		ALL	Replace (and mark all to Vshy)
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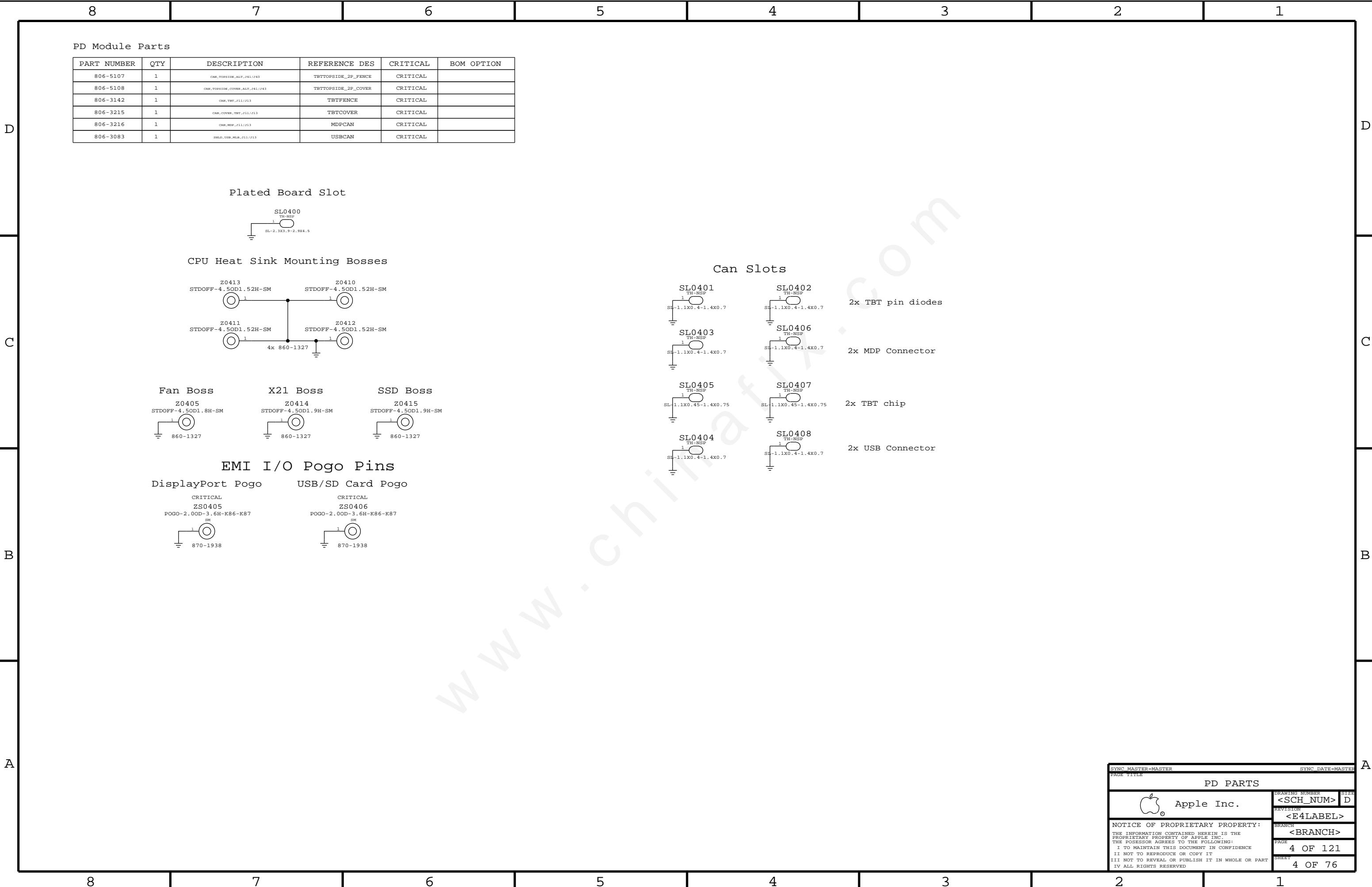
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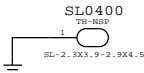
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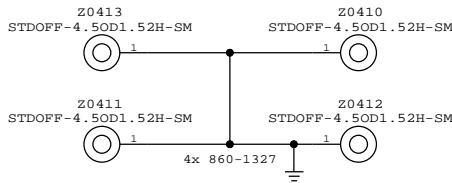
PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-5107	1	CAN, TOPSIDE, ALT, 741/243	TBTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN, TOPSIDE, COVER, ALT, 741/243	TBTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN, TBT, 711/213	TBTFENCE	CRITICAL	
806-3215	1	CAN, COVER, TBT, 711/213	TBTCOVER	CRITICAL	
806-3216	1	CAN, MDP, 711/213	MDPCAN	CRITICAL	
806-3083	1	SHIELD, USB, MLB, 711/213	USBCAN	CRITICAL	

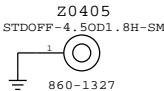
Plated Board Slot



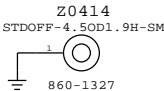
CPU Heat Sink Mounting Bosses



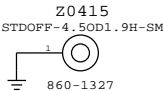
Fan Boss



X21 Boss

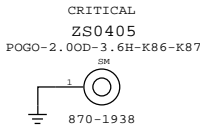


SSD Boss

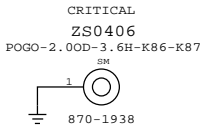


EMI I/O Pogo Pins

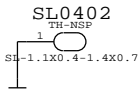
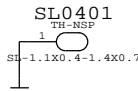
DisplayPort Pogo



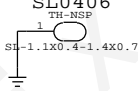
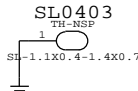
USB/SD Card Pogo



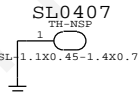
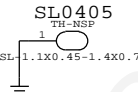
Can Slots



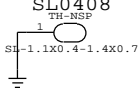
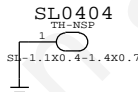
2x TBT pin diodes



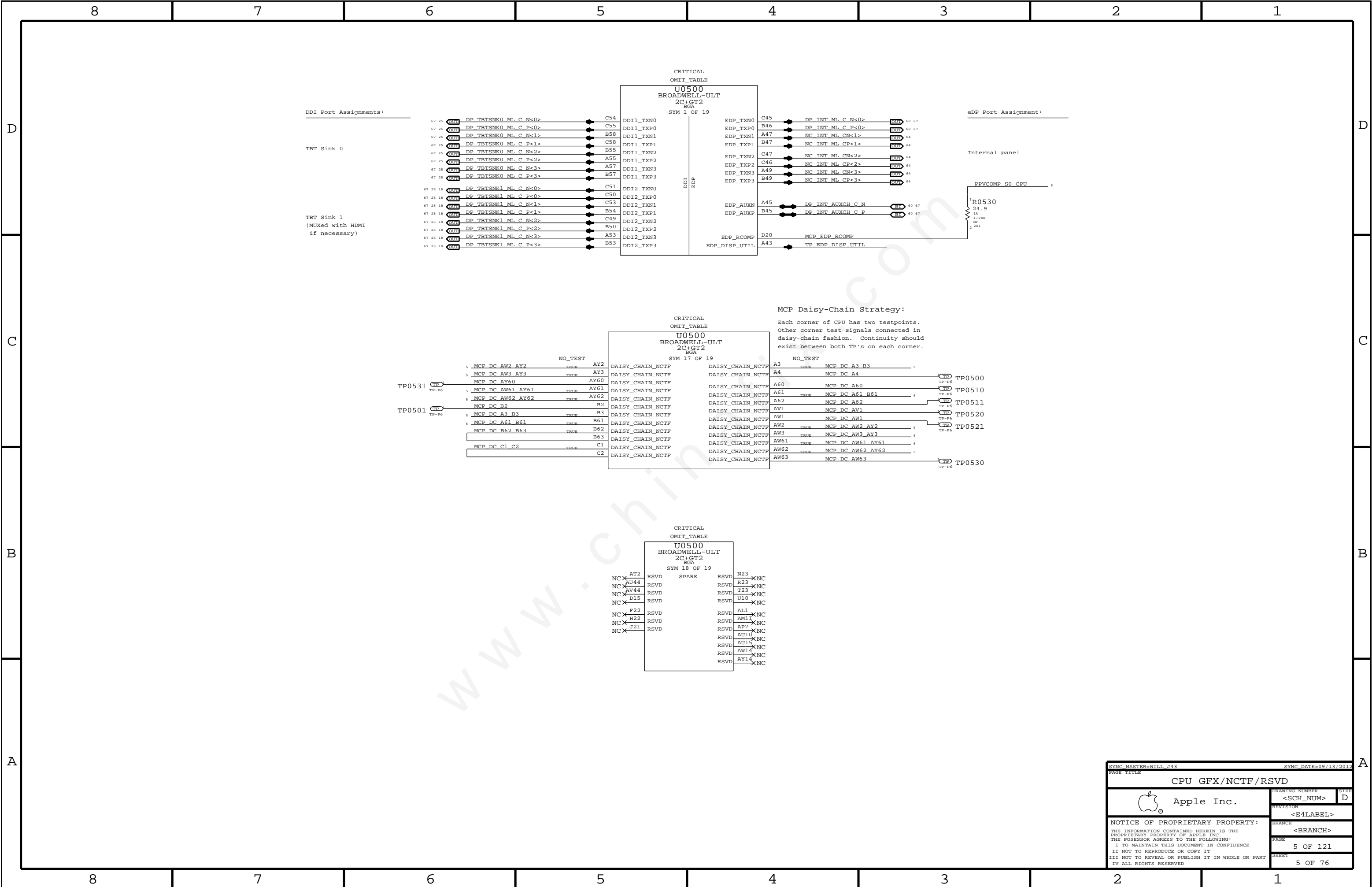
2x MDP Connector



2x TBT chip



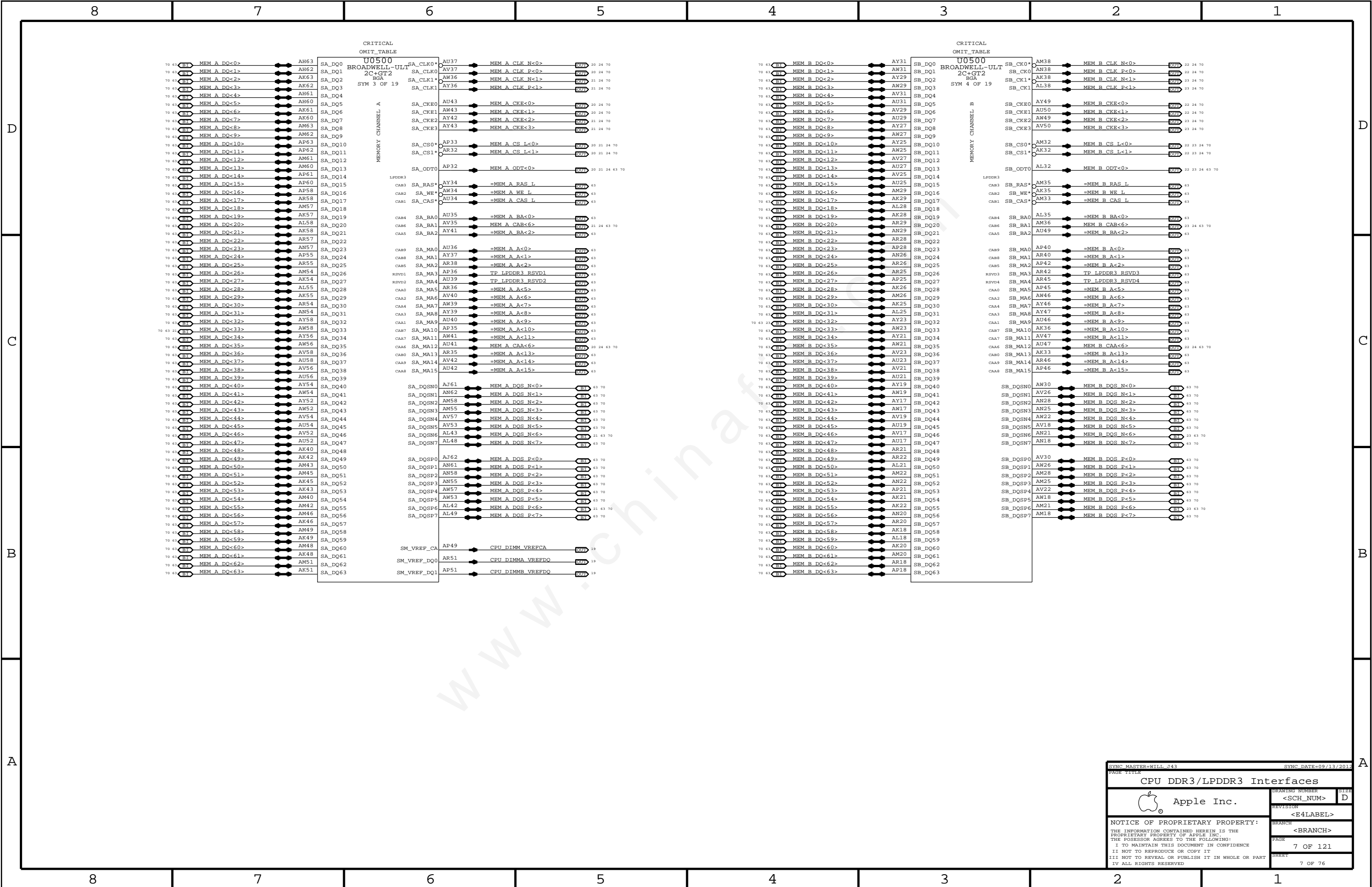
2x USB Connector

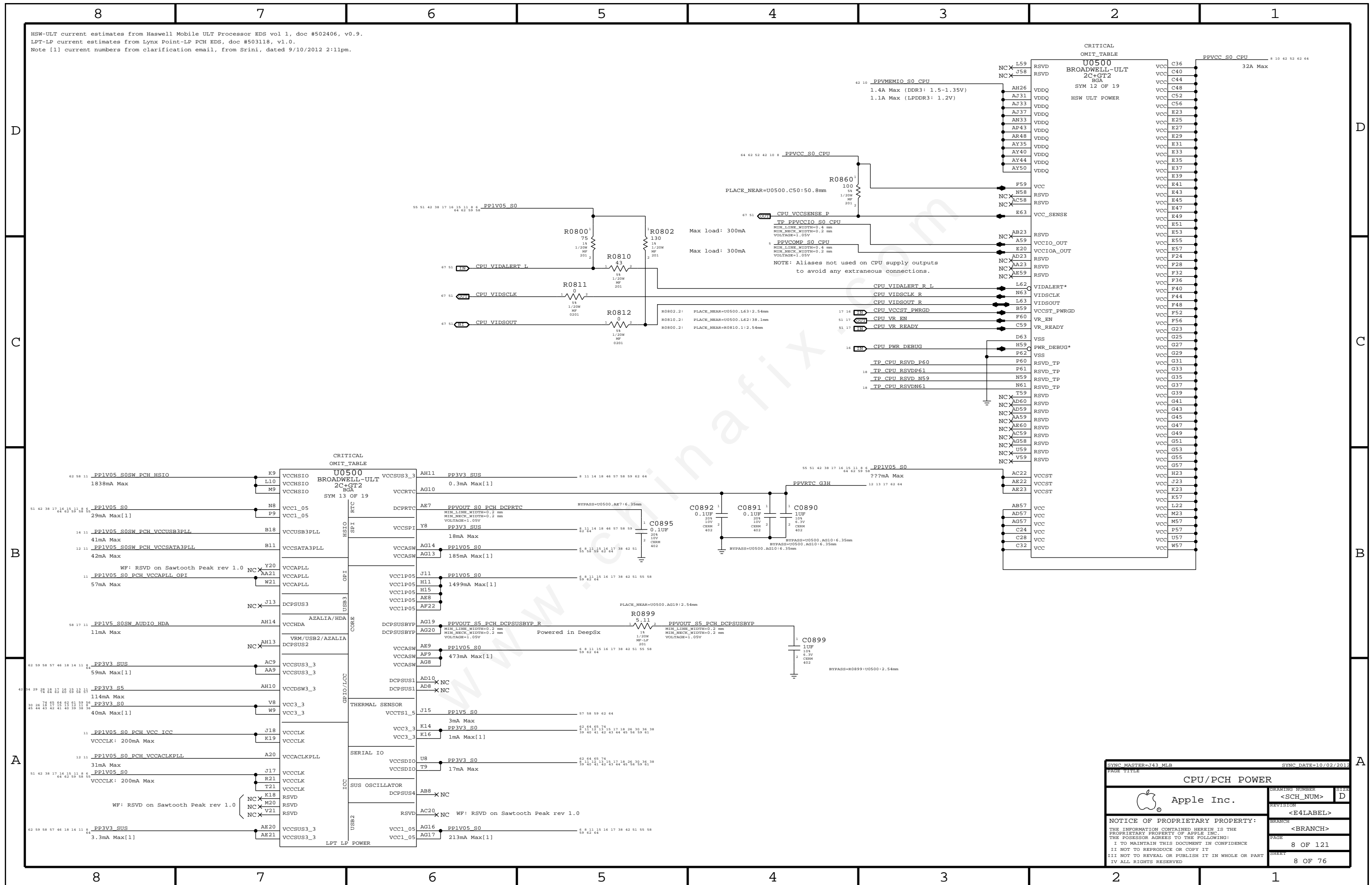


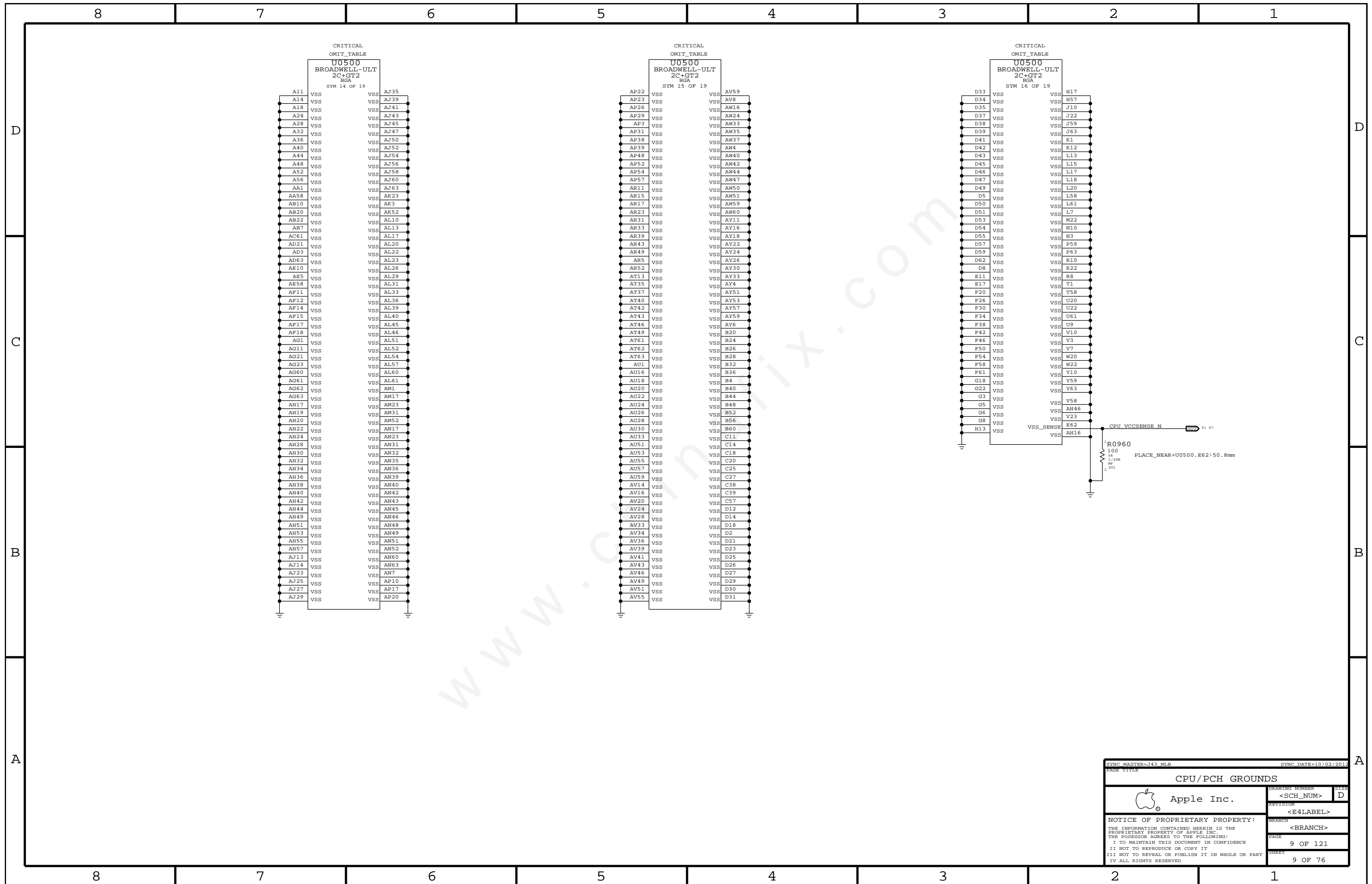


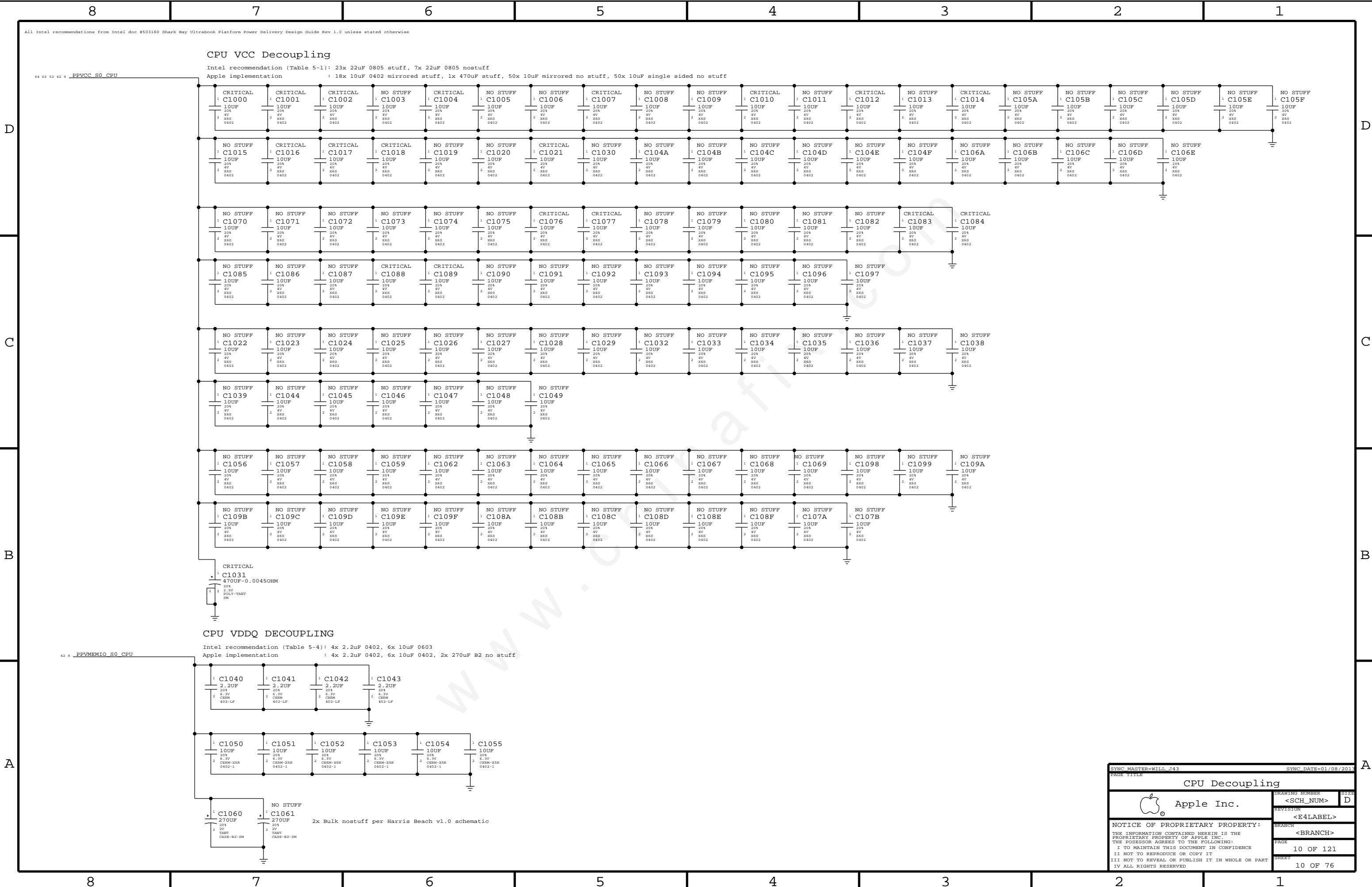
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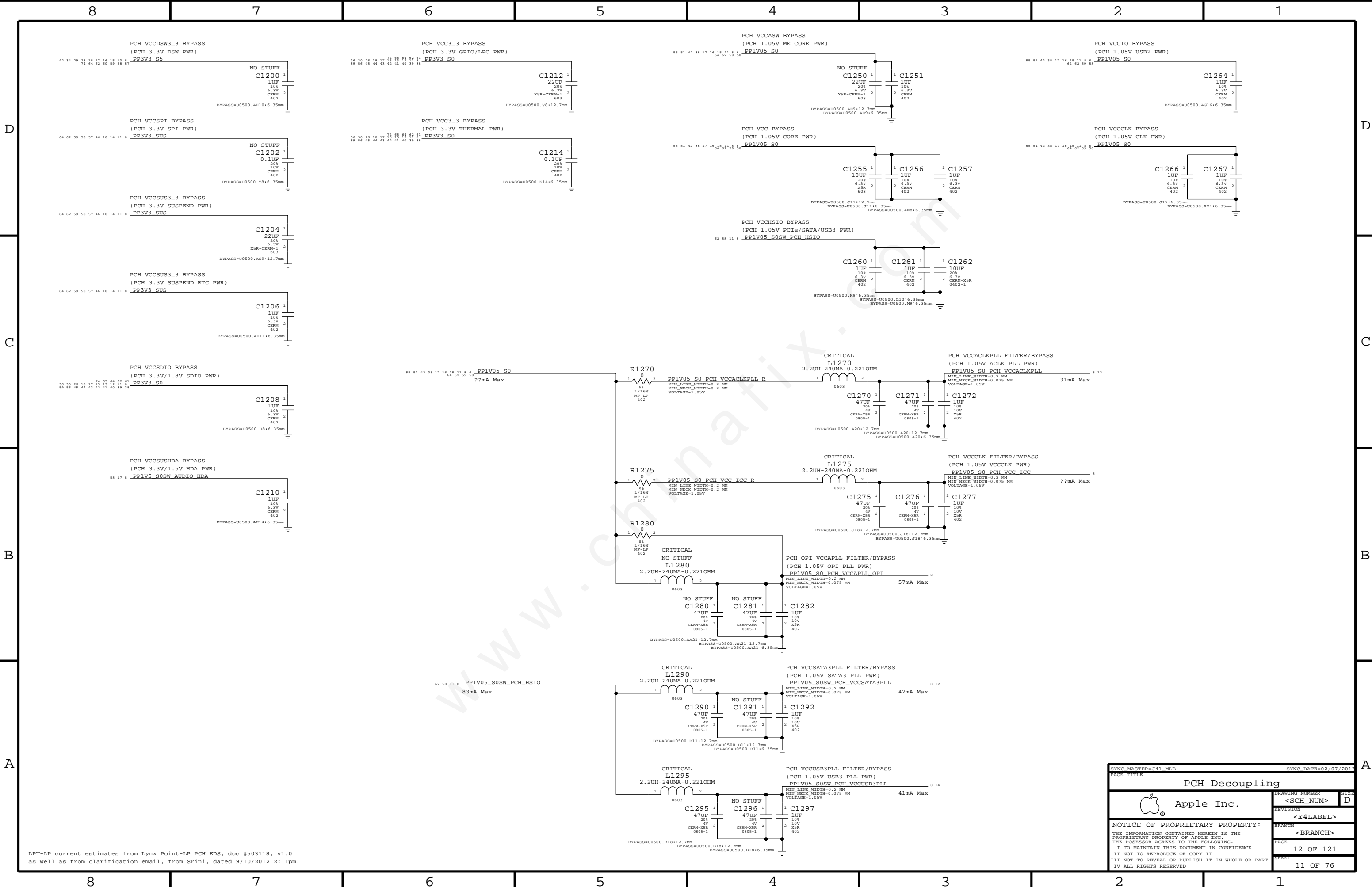













LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0 as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC MASTER=j41 MLB

SYNC DATE=02/07/2013

PAGE TITLE

PCH Decoupling

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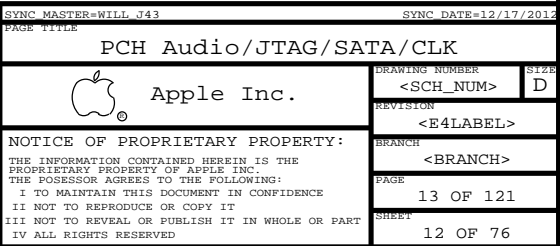
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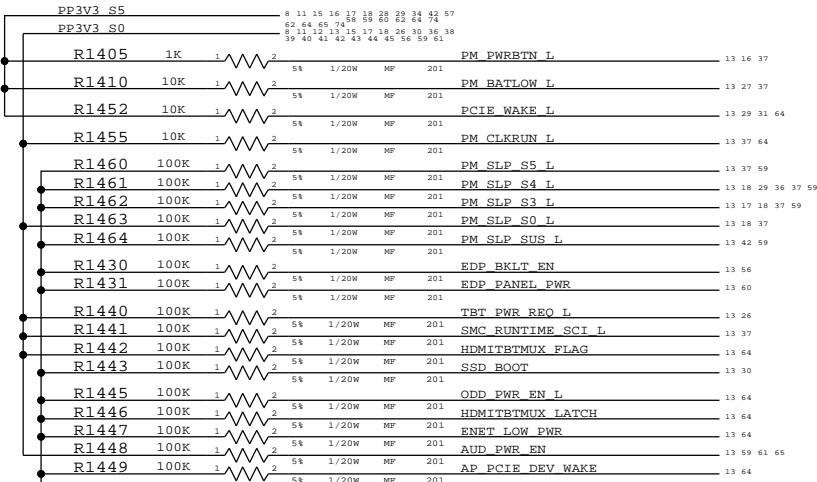
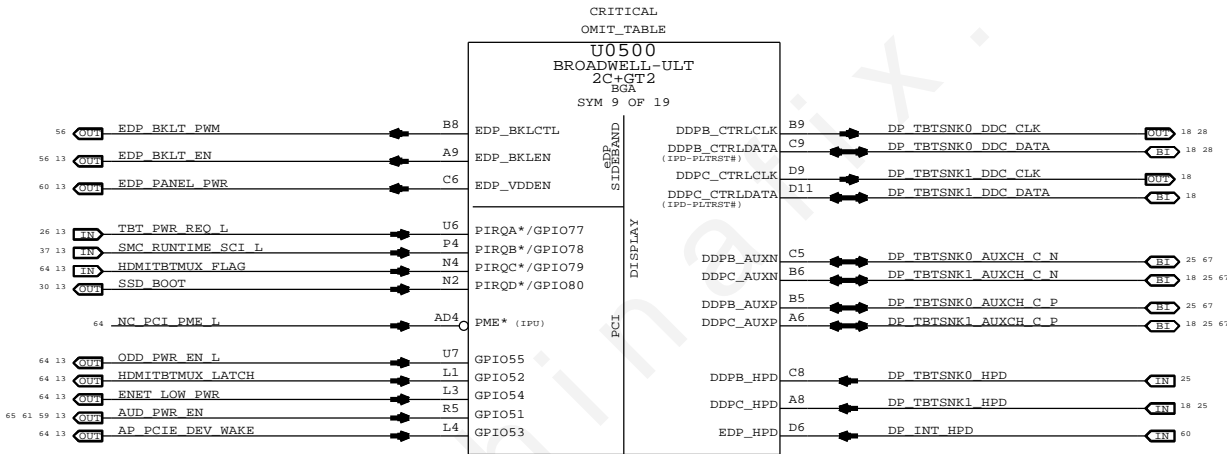
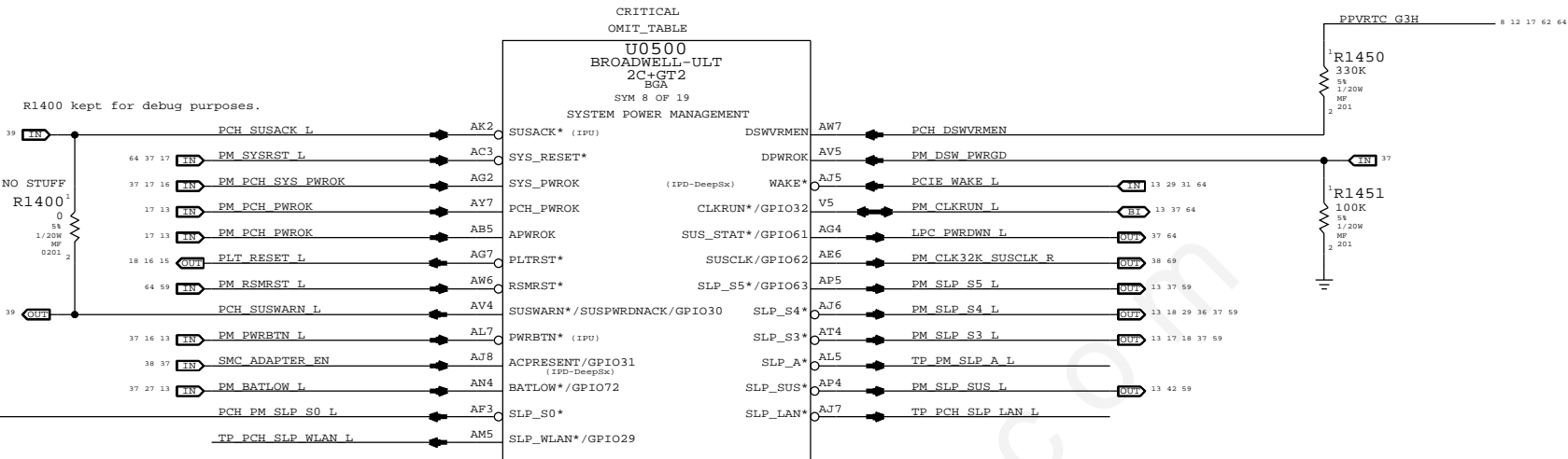
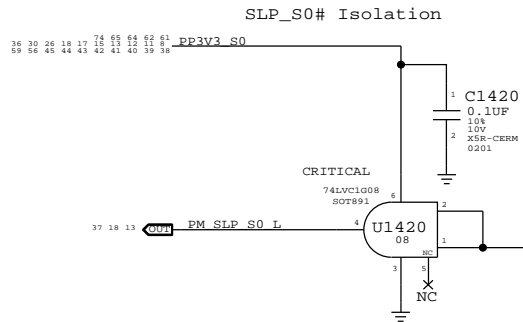
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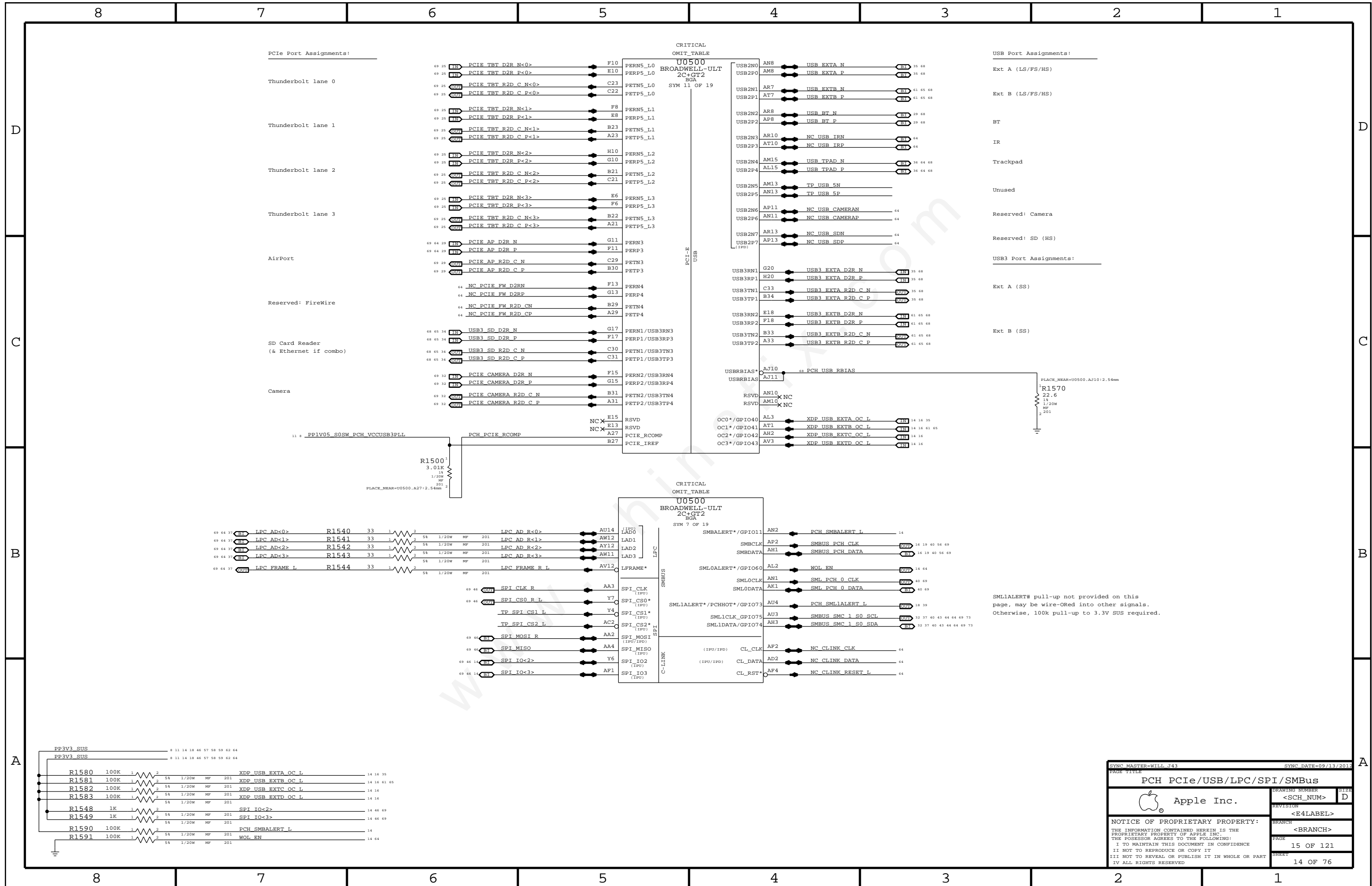
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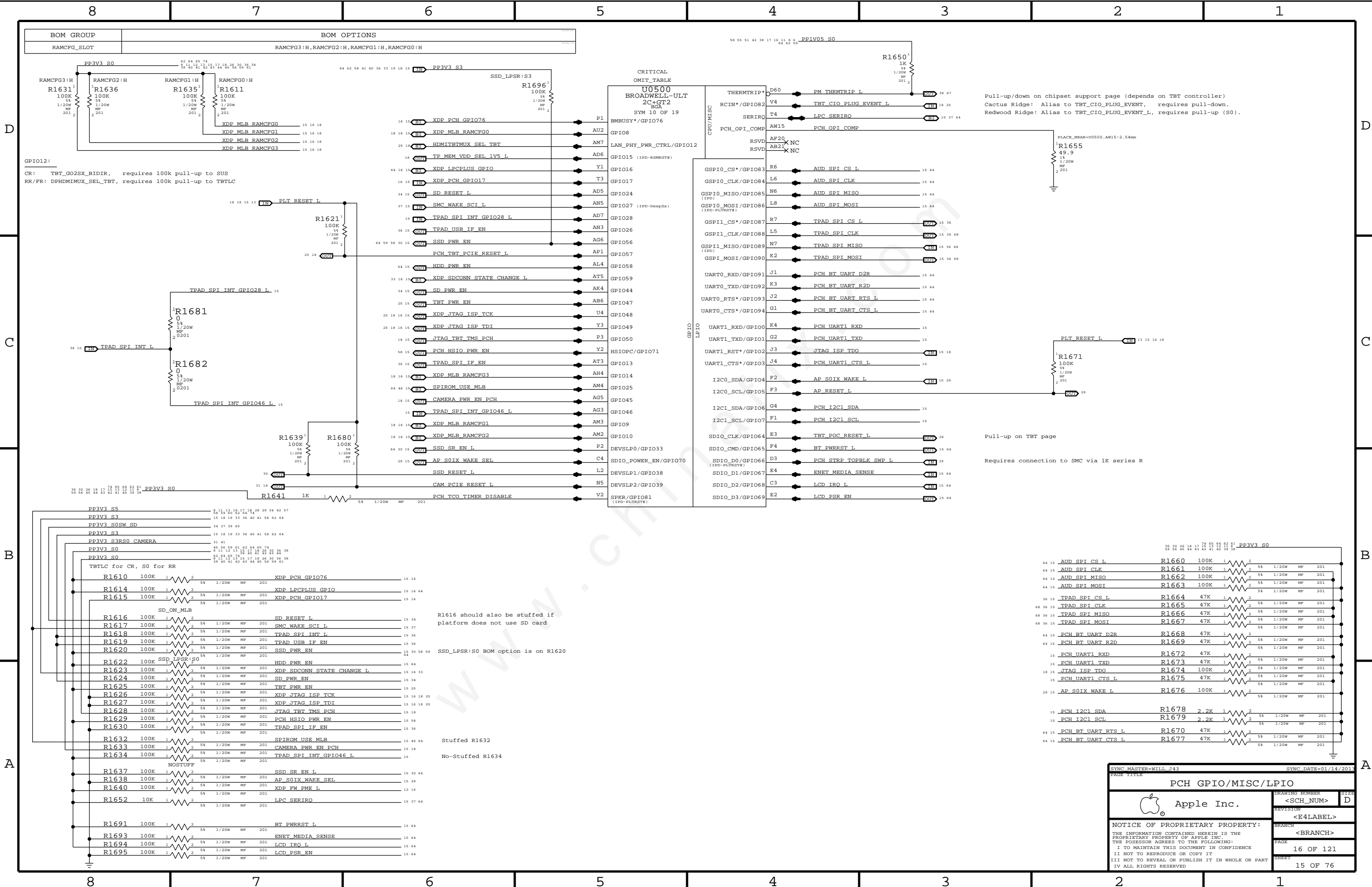
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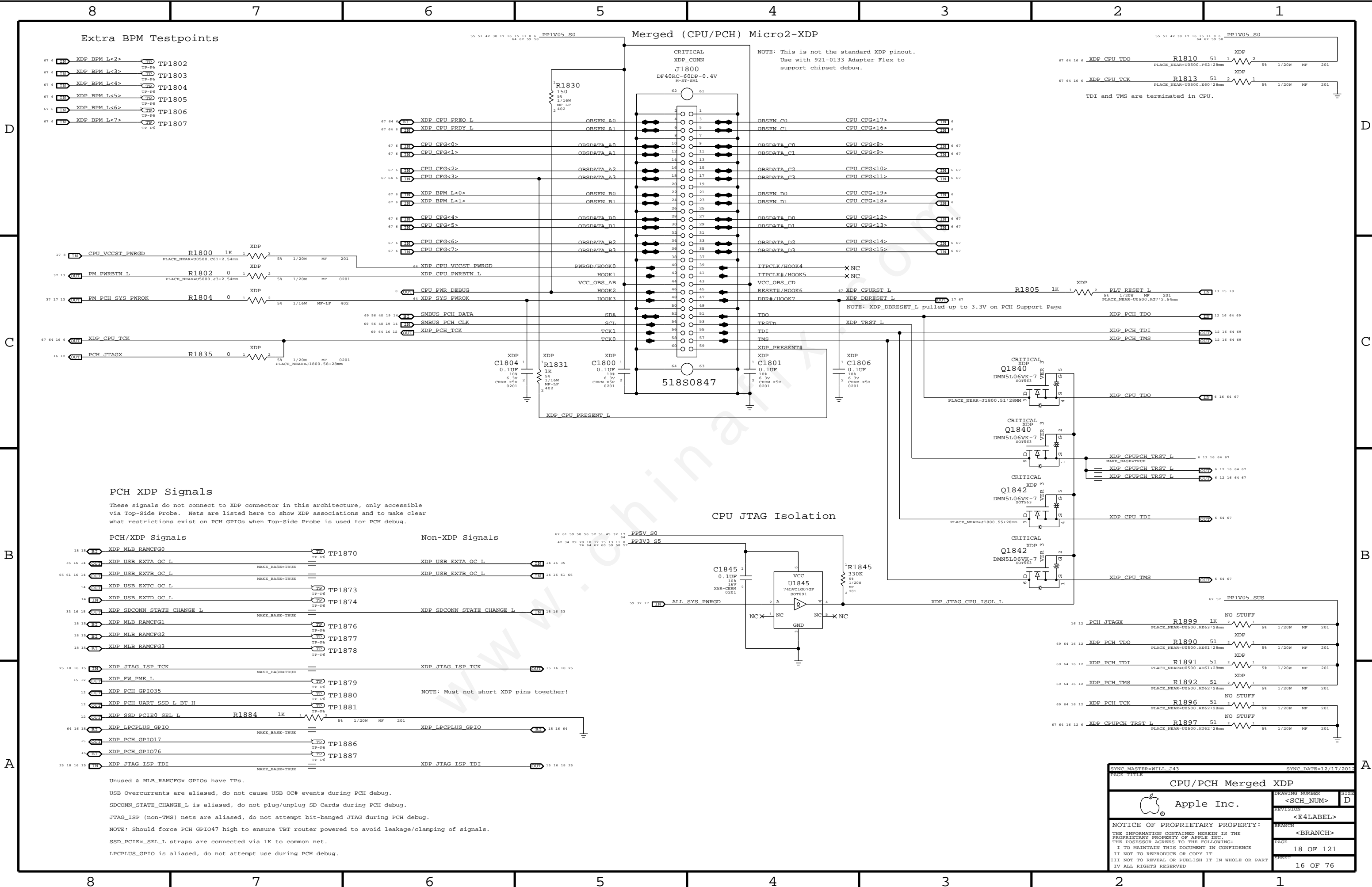




Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

Pull-up on TBT page
Requires connection to SMC via 1K series R

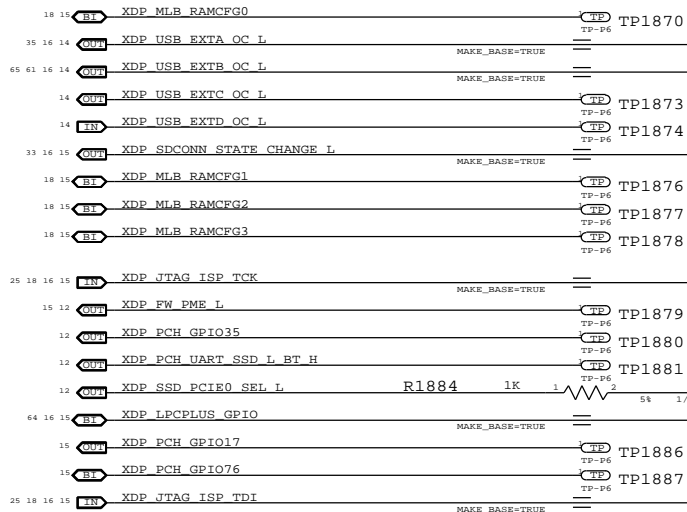
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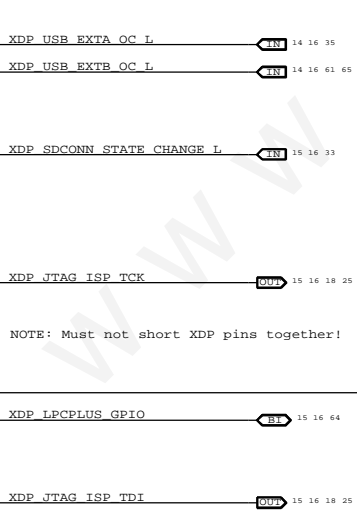
PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals



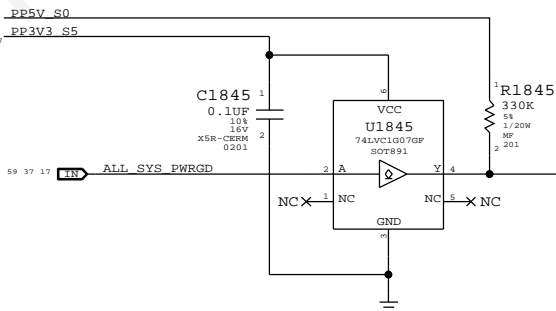
Non-XDP Signals




NOTE: Must not short XDP pins together!

Unused & MLB_RAMCFGx GPIOs have TPs.
USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
SSD_PCIE_SEL_L straps are connected via 1k to common net.
LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation



SYNC MASTER=WILL J43		SYNC DATE=12/17/2012	
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CPU/PCH Merged XDP			
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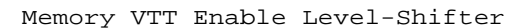
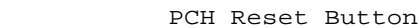
GreenCLK 25MHz Power 18 PP3
Must be powered if any VDDIO is powered.

GreenCLK 25MHz Power
Must be powered if a

CAM XTAL Power
TBT XTAL Power



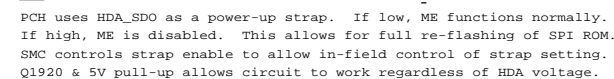
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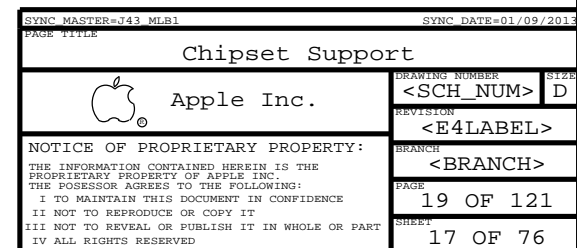
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B



A



Power aliases required by this page:

- =PP3V3_S3_VREFMGRN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:

- =I2C_VREFDAC5_SCL
- =I2C_VREFDAC5_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

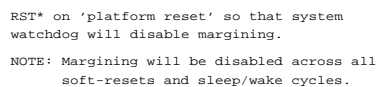
BOM options provided by this page:

- DDRVREF_DAC - Stuffs DAC margining circuit.

FETs for CPU isolation during DAC margining

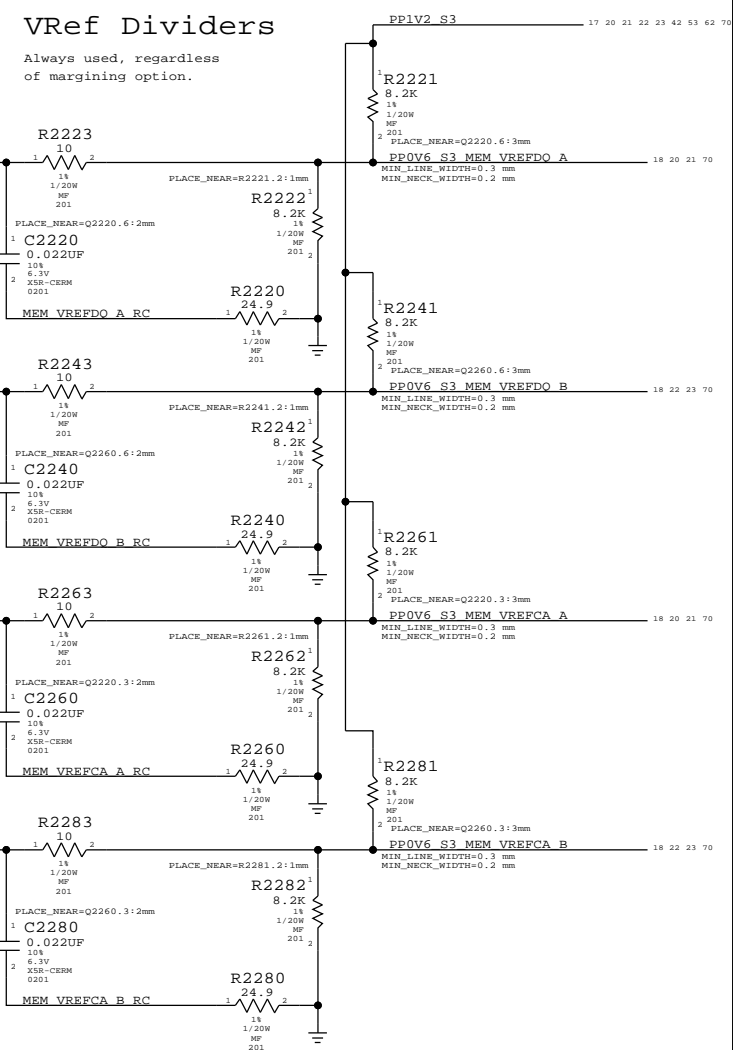
NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.


DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.



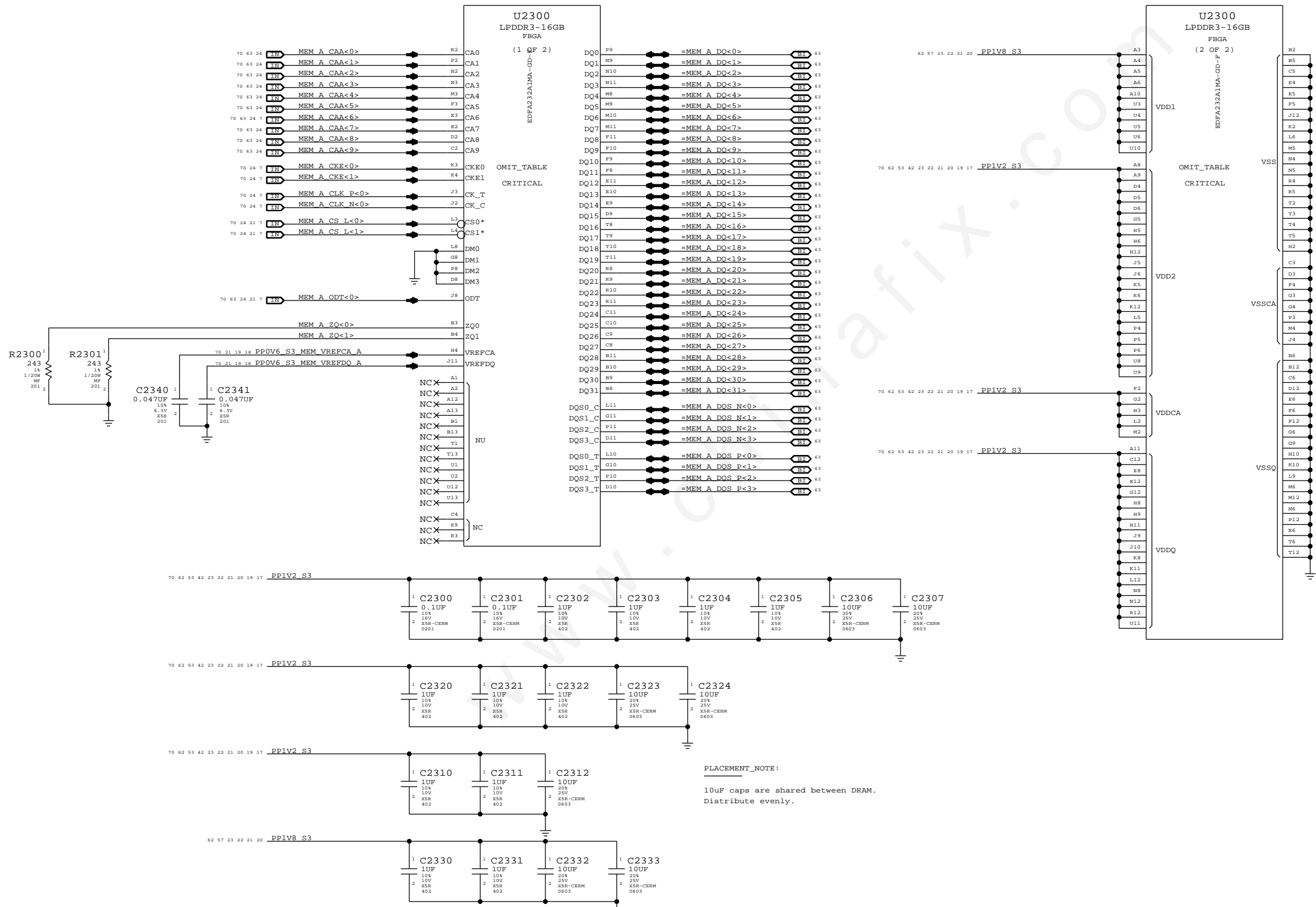
NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

Always used, regardless
of margining option.

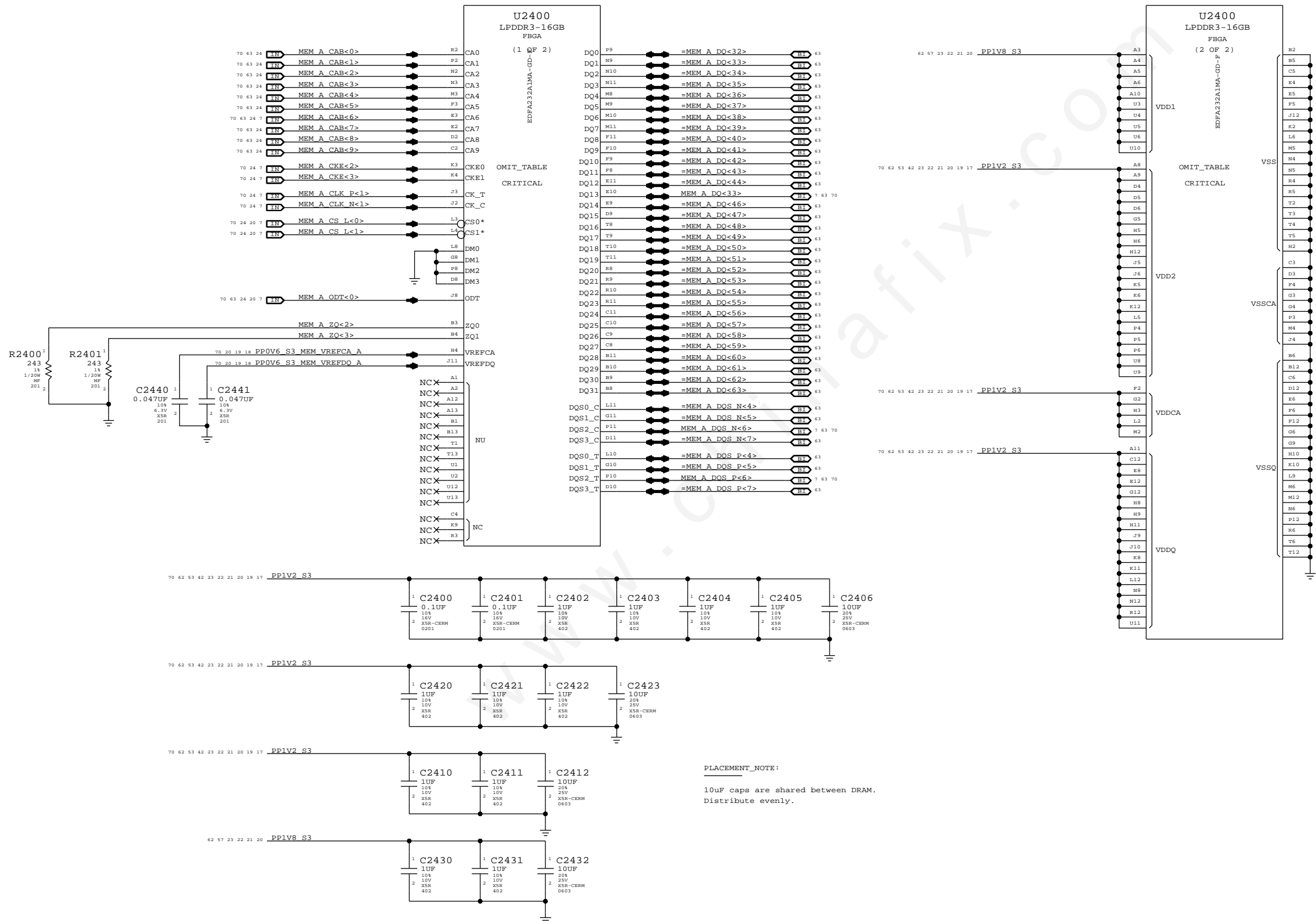


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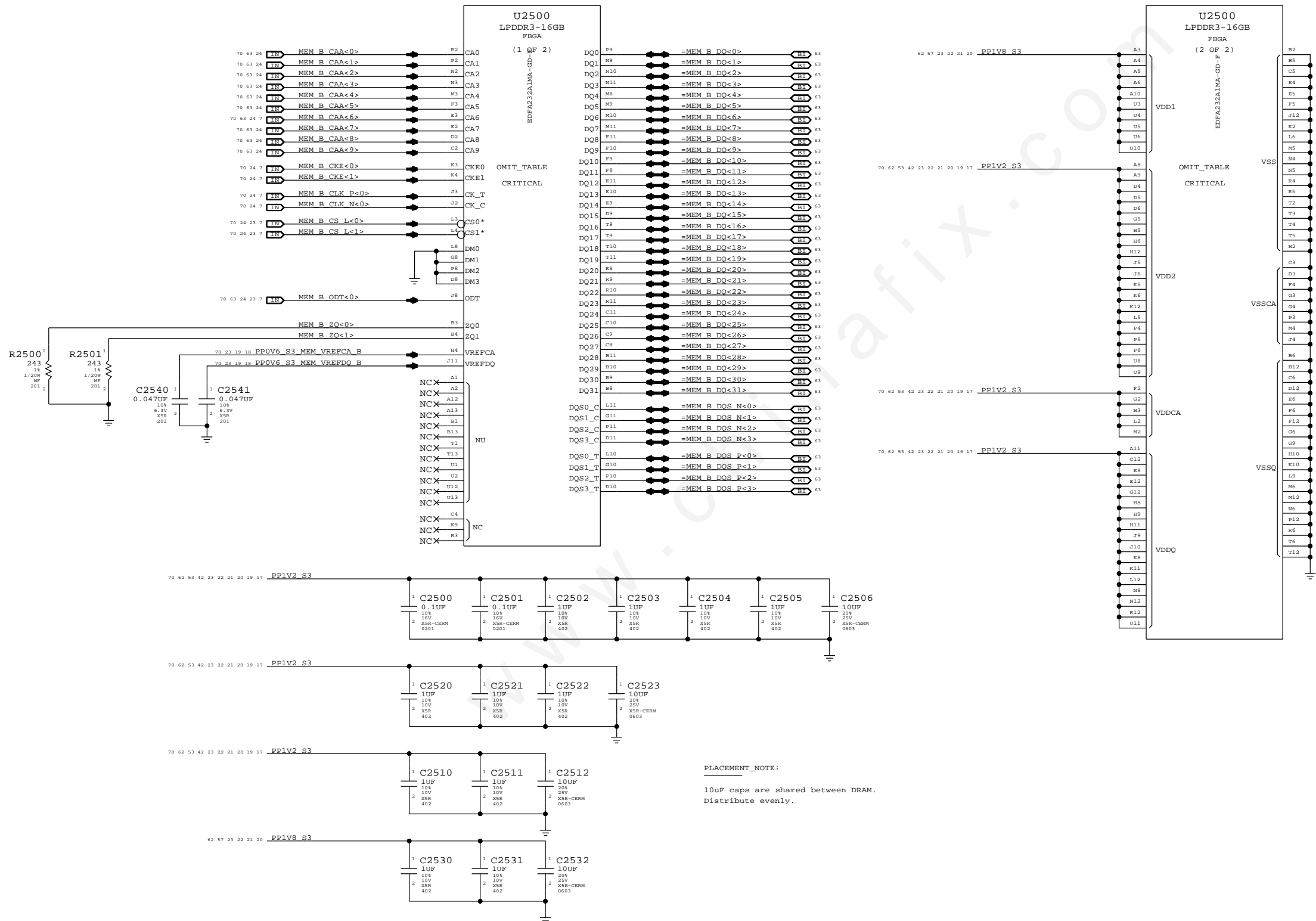
LPDDR3 CHANNEL A (0-31)



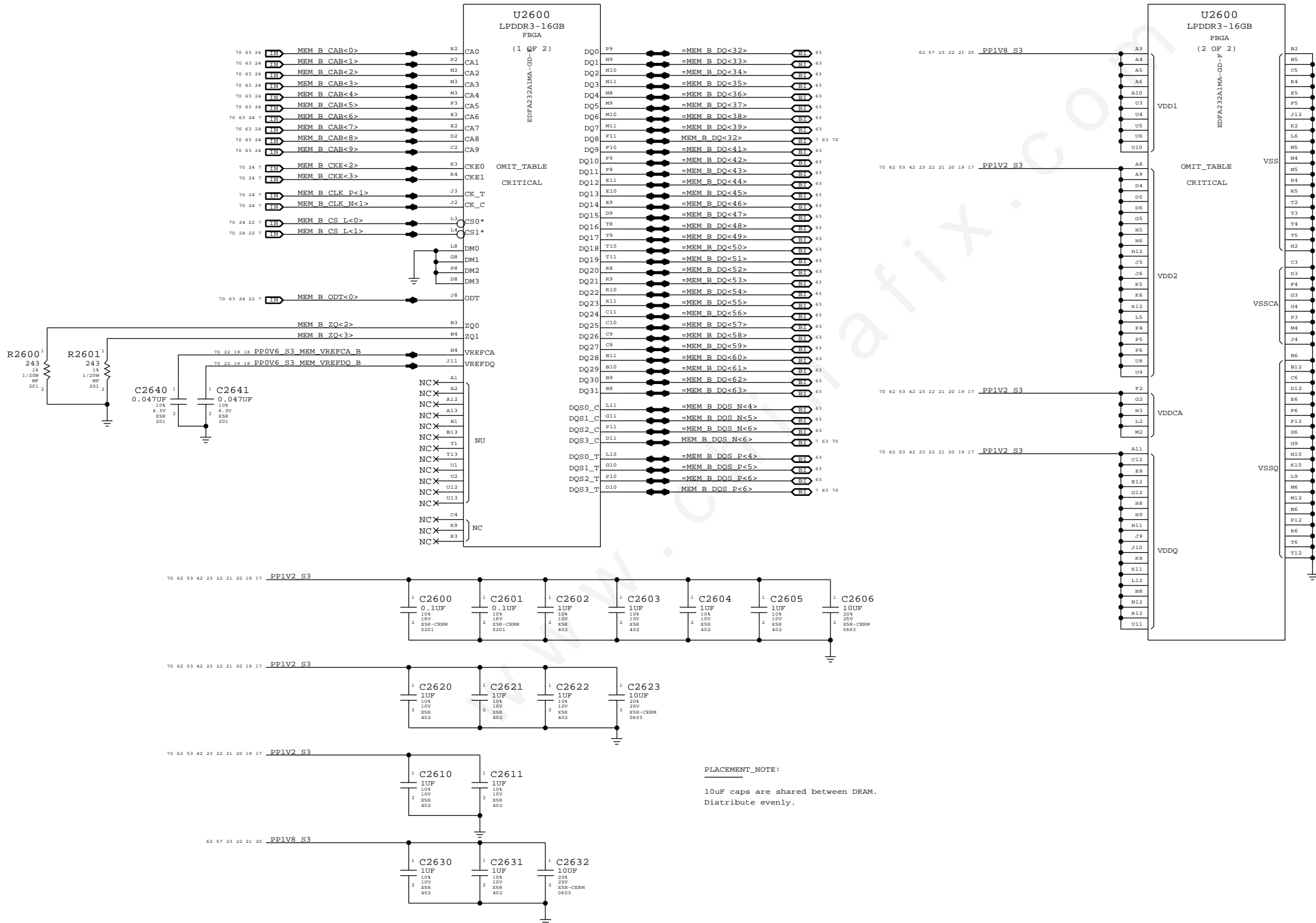
LPDDR3 CHANNEL A (32-63)



LPDDR3 CHANNEL B (0-31)



LPDDR3 CHANNEL B (32-63)

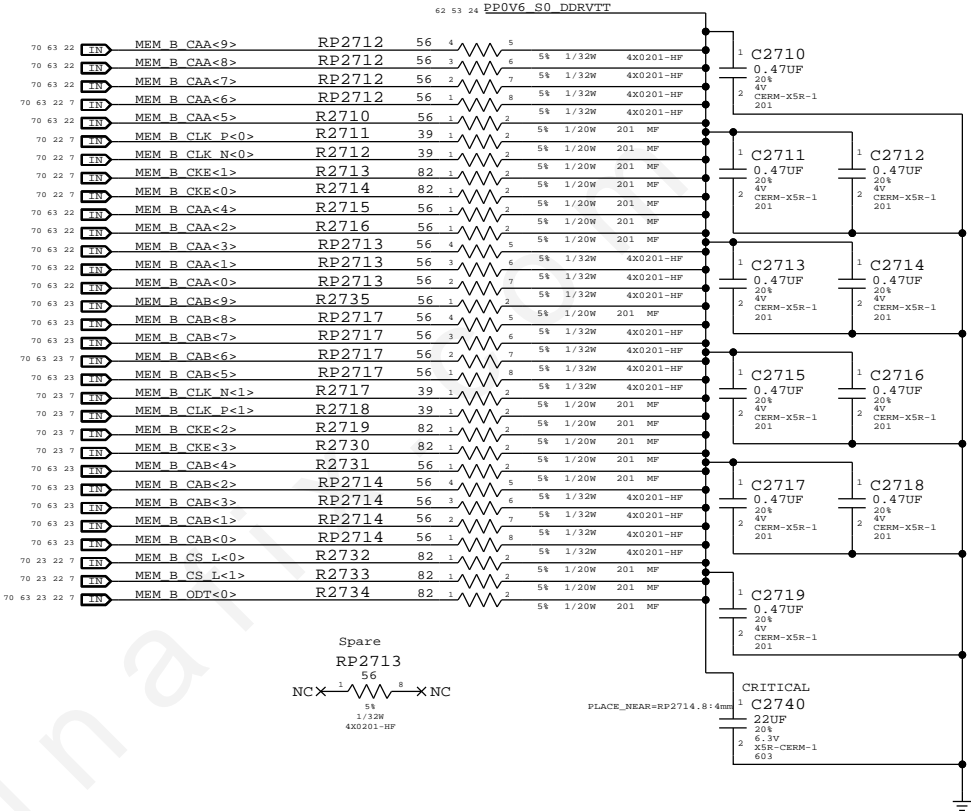
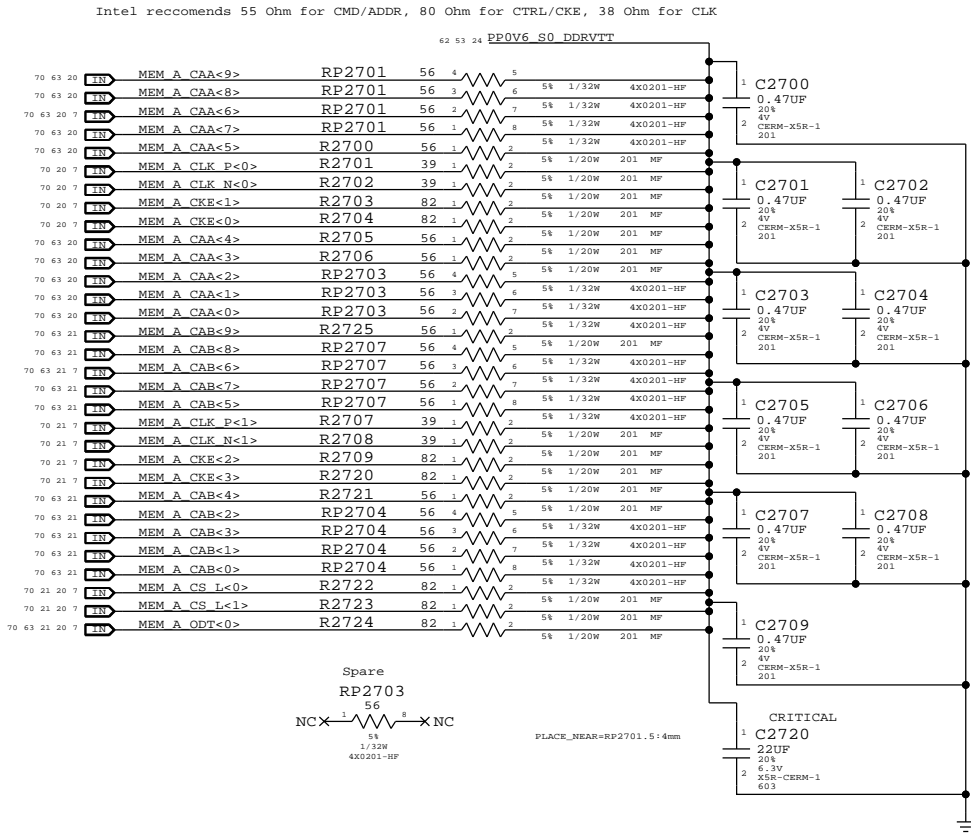


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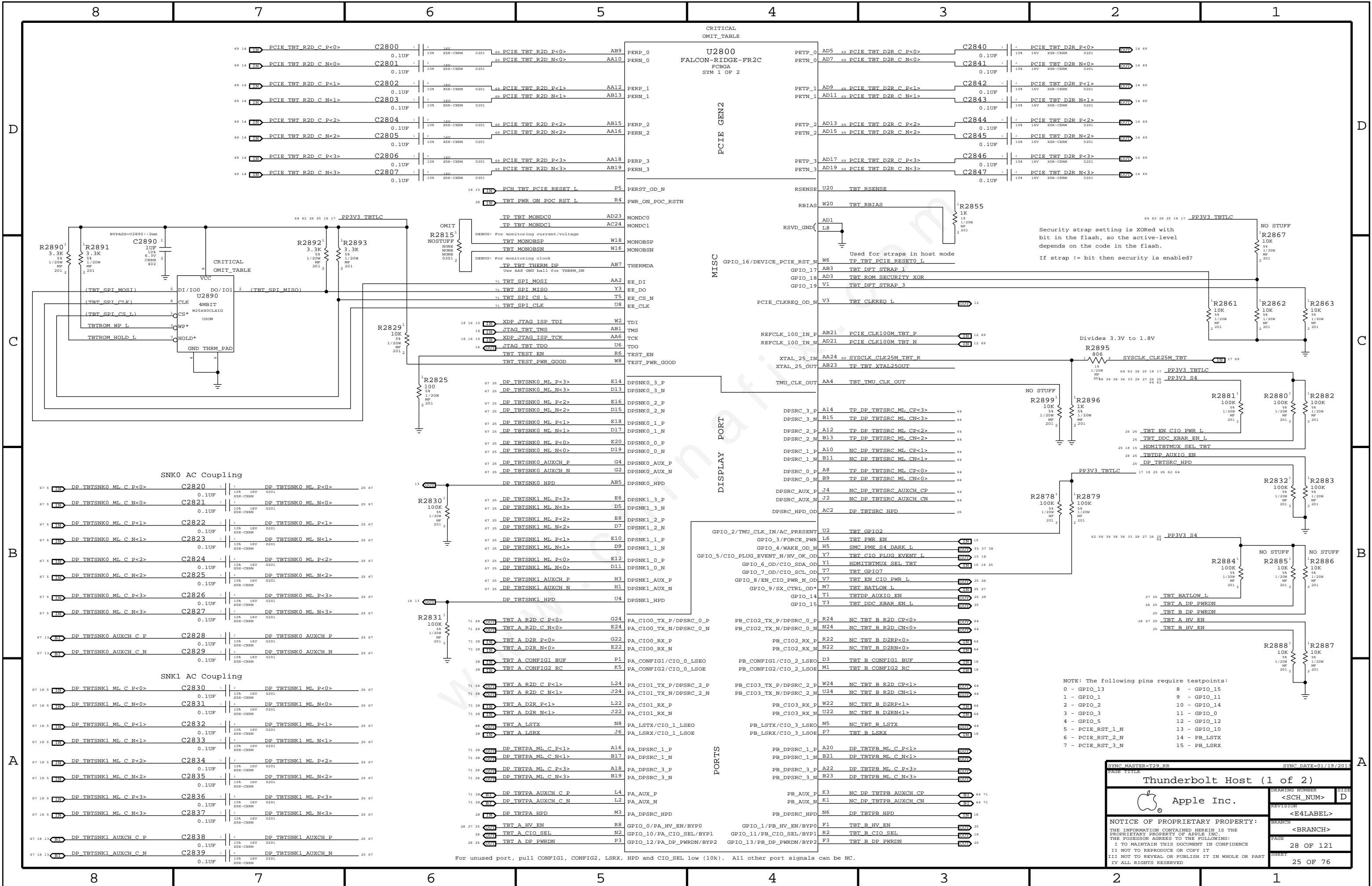


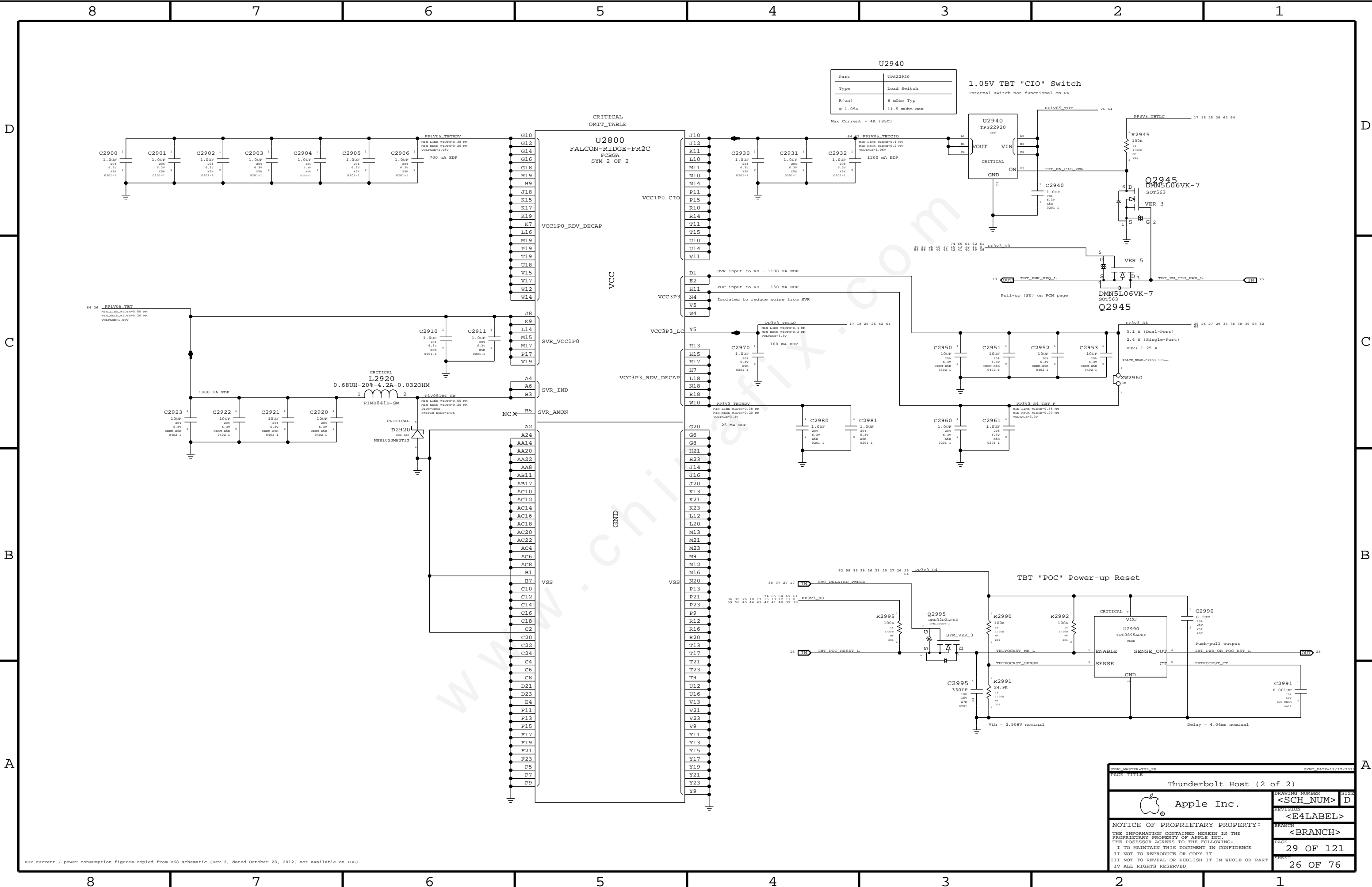
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Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ 11.5 mOhm Max

1.05V TBT "CIO" Switch
Internal switch not functional on RR.

Max Current = 4A (85C)

CRITICAL
OMIT_TABLE
U2800
FALCON-RIDGE-FR2C
FCBGA
SYM 2 OF 2

Q2945
DMN5L06VK-7
SOT563


Q2945
DMN5L06VK-7
SOT563

TBT "POC" Power-up Reset

SYMC PARTSHEET ID: 82

SYMC DATE: 12/17/2015

Thunderbolt Host (2 of 2)

 Apple Inc.

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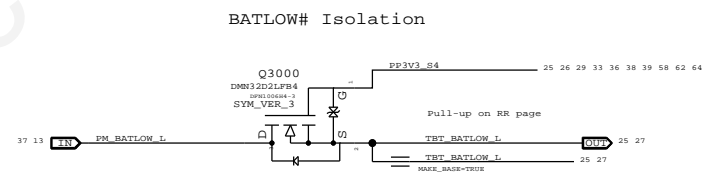
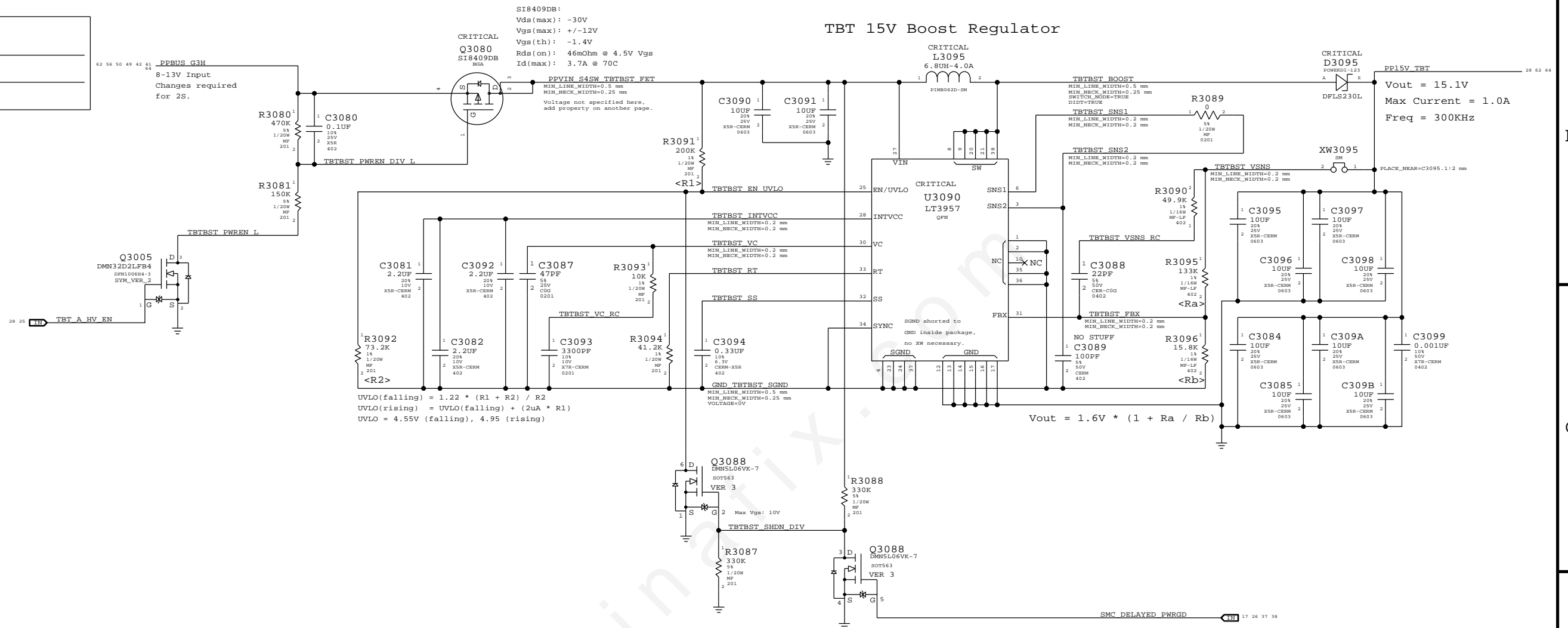
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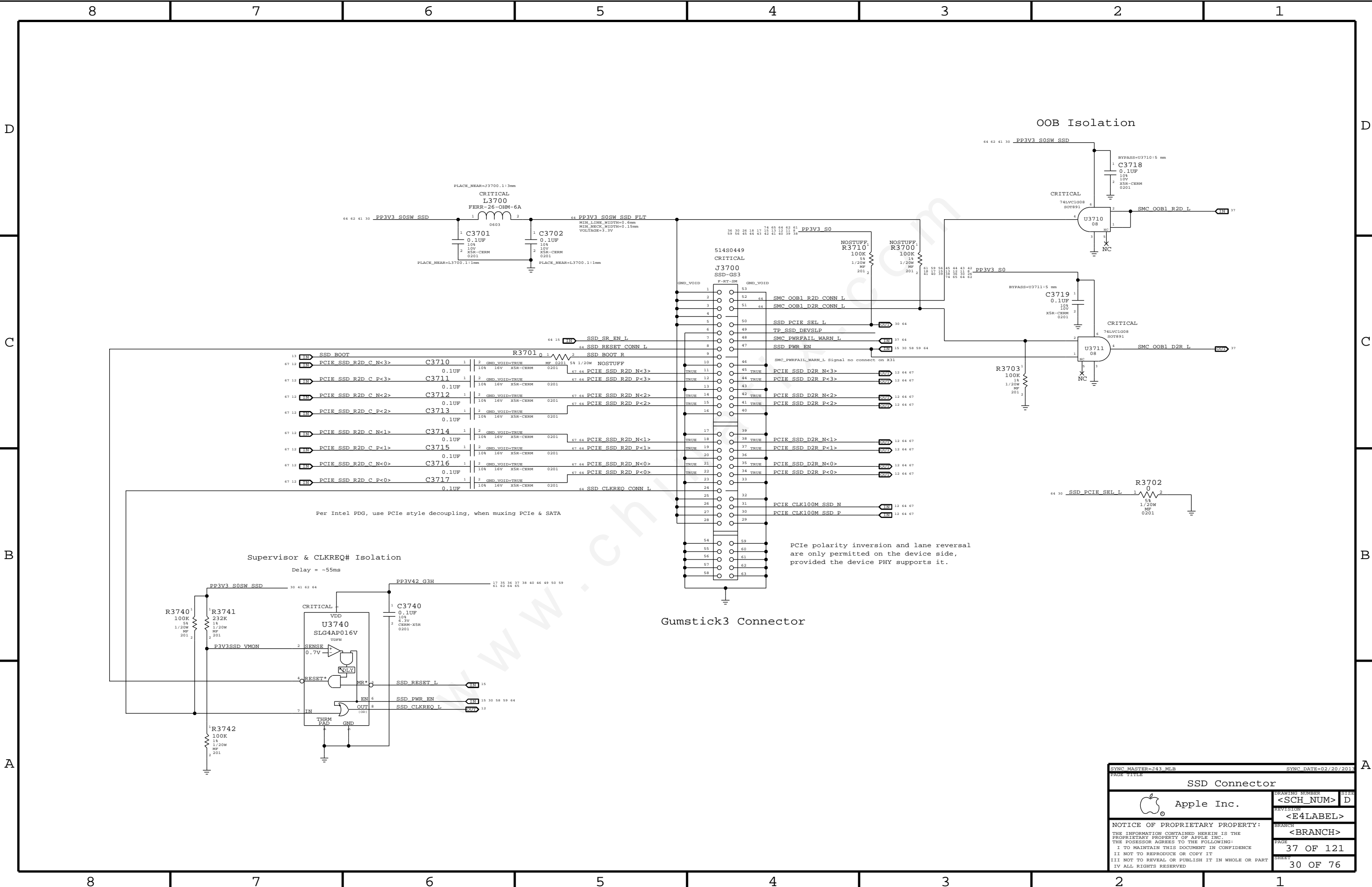
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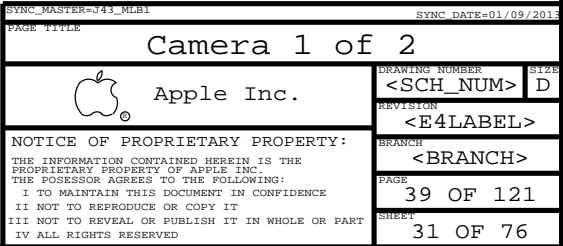
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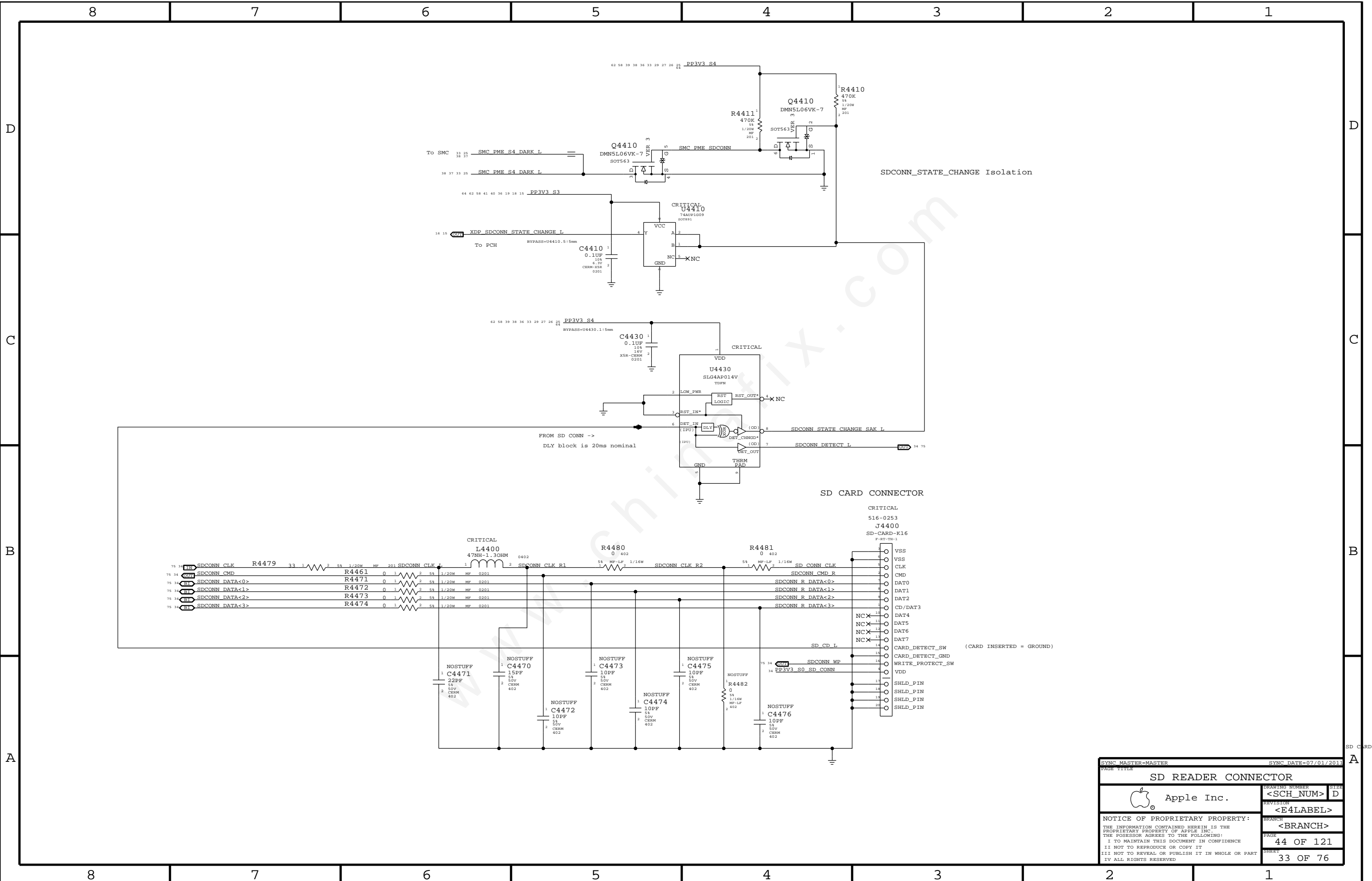
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EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).









3.3V S3 SD Card Switch

U4550
SLG5AP1443V
TDFN
CAP
ON
CRITICAL
GND

U4500
GL3219
LQFN
CRITICAL
OMIT_TABLE

U4590
512KB
W25X05CL
NOSTUFF
VCC
DIO(I00)
DO(I01)
CS*
WP*
HOLD*
GND

Table 1: U4550 Specifications

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ
	17 mOhm Max
Current	2.5A

Table 2: Component Values

Component	Value
C4523	0.1uF
C4524	0.1uF
C4525	1.0uF
C4526	0.1uF
C4527	0.1uF
C4528	2.2uF
C4529	47pF
C4530	100pF
C4531	1.0uF
C4512	0.1uF
C4513	0.1uF
C4518	0.1uF
C4519	0.1uF
C4520	2.2uF
C4521	4.7uF
C4522	1.0uF
C4523	0.1uF
C4524	0.1uF
C4525	1.0uF
C4526	0.1uF
C4527	0.1uF
C4528	2.2uF
C4529	47pF
C4530	100pF
C4531	1.0uF
C4512	0.1uF
C4513	0.1uF
C4518	0.1uF
C4519	0.1uF
C4520	2.2uF
C4521	4.7uF
C4522	1.0uF
C4523	0.1uF
C4524	0.1uF
C4525	1.0uF
C4526	0.1uF
C4527	0.1uF
C4528	2.2uF
C4529	47pF
C4530	100pF
C4531	1.0uF
C4512	0.1uF
C4513	0.1uF
C4518	0.1uF
C4519	0.1uF
C4520	2.2uF
C4521	4.7uF
C4522	1.0uF
C4523	0.1uF
C4524	0.1uF
C4525	1.0uF
C4526	0.1uF
C4527	0.1uF
C4528	2.2uF
C4529	47pF
C4530	100pF
C4531	1.0uF
C4512	0.1uF
C4513	0.1uF
C4518	0.1uF
C4519	0.1uF
C4520	2.2uF
C4521	4.7uF
C4522	1.0uF
C4523	0.1uF
C4524	0.1uF
C4525	1.0uF
C4526	0.1uF
C4527	0.1uF
C4528	2.2uF
C4529	47pF
C4530	100pF
C4531	1.0uF
C4512	0.1uF
C4513	0.1uF
C4518	0.1uF
C4519	0.1uF
C4520	2.2uF
C4521	4.7uF
C4522	1.0uF
C4523	0.1uF
C4524	0.1uF
C4525	1.0uF
C4526	0.1uF
C4527	0.1uF
C4528	2.2uF
C4529	47pF
C4530	100pF
C4531	1.0uF
C4512	0.1uF
C4513	0.1uF
C4518	0.1uF
C4519	0.1uF
C4520	2.2uF
C4521	4.7uF
C4522	1.0uF
C4523	0.1uF
C4524	0.1uF
C4525	1.0uF
C4526	0.1uF
C4527	0.1uF
C4528	2.2uF
C4529	47pF
C4530	100pF
C4531	1.0uF
C4512	0.1uF
C4513	0.1uF
C4518	0.1uF
C4519	0.1uF
C4520	2.2uF
C4521	4.7uF
C4522	1.0uF
C4523	0.1uF
C4524	0.1uF
C4525	1.0uF
C4526	0.1uF
C4527	0.1uF
C4528	2.2uF
C4529	47pF
C4530	100pF
C4531	1.0uF
C4512	0.1uF
C4513	0.1uF
C4518	0.1uF
C4519	0.1uF
C4520	2.2uF
C4521	4.7uF
C4522	1.0uF
C4523	0.1u

3.3V S3 SD Card Switch

U4550
SLG5AP1443V
TDFN
CAP
ON
CRITICAL
GND

U4550
SLG5AP1438V
Type: Load Switch
R(on): 15 mOhm Typ, 17 mOhm Max
Current: 2.5A

U4500
GL3219
LQFN
CRITICAL
OMIT_TABLE

U4590
512KB
USION
W25X05CL
VCC
DIO(I00)
DO(I01)
CS*
WP*
HOLD*
GND

Y4580
25.000MHZ-12PF-20PPM
SM-3.2X2.5MM

SD CONTROLLER (GL3219)

Apple Inc.

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3.3V S3 SD Card Switch

U4550
SLG5AP1443V
TDFN
CAP
ON
CRITICAL
GND

U4550
SLG5AP1438V
Type: Load Switch
R(on): 15 mOhm Typ, 17 mOhm Max
Current: 2.5A

U4500
GL3219
LQFN
CRITICAL
OMIT_TABLE

U4590
512KB
USION
W25X05CL
VCC
DIO(I00)
DO(I01)
CS*
WP*
HOLD*
THRM PAD
GND

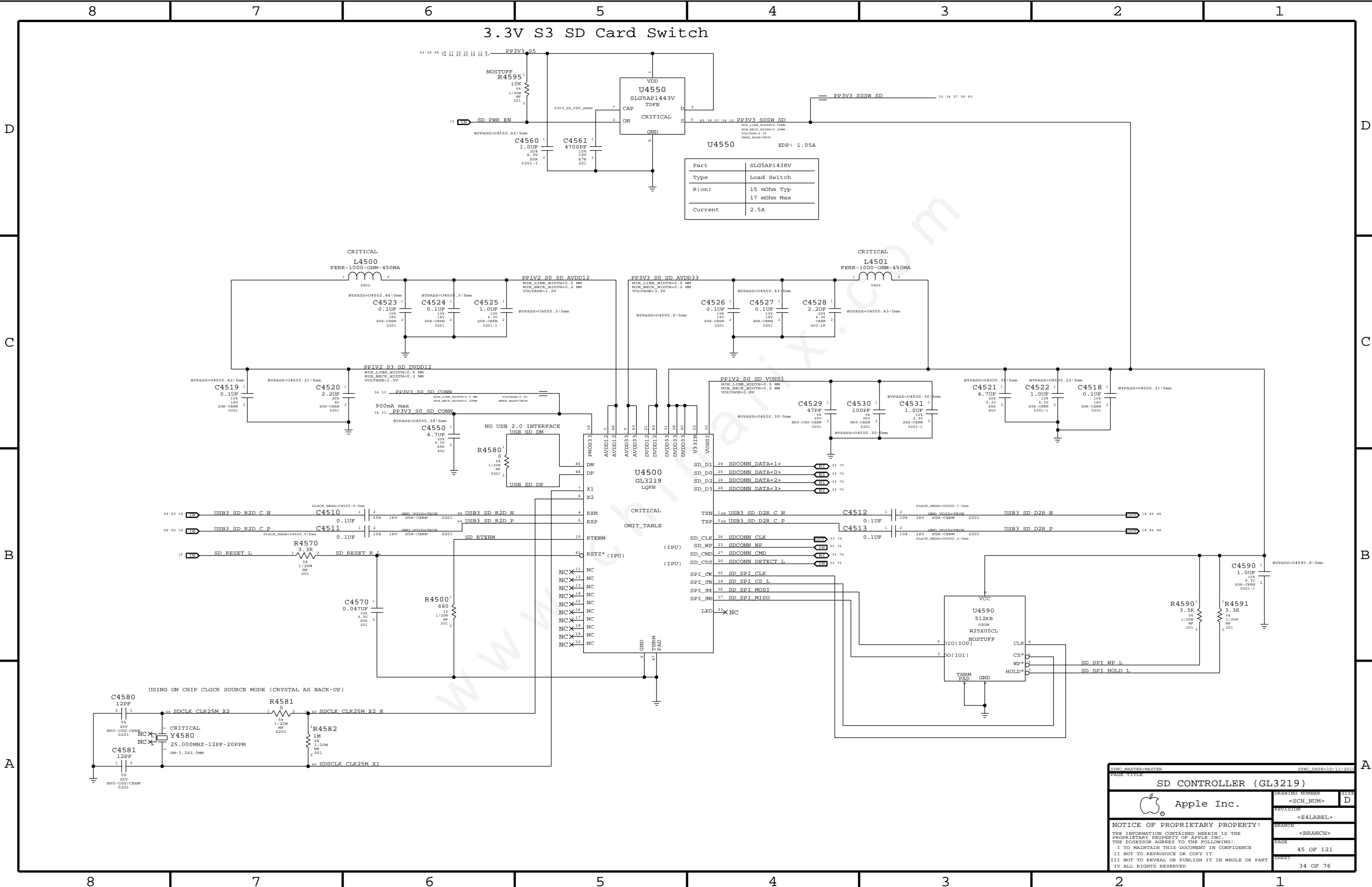
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25.000MHZ-12PF-20PPM
SM-3, 2X2, 5MHZ

SD CONTROLLER (GL3219)

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3.3V S3 SD Card Switch

U4550
SLG5AP1443V
TDFN
CAP
ON
CRITICAL
GND

U4550
SLG5AP1438V
Type: Load Switch
R(on): 15 mOhm Typ, 17 mOhm Max
Current: 2.5A

U4500
GL3219
LQFN
CRITICAL
OMIT_TABLE

U4590
512KB
USION
W25X05CL
VCC
DIO(I00)
DO(I01)
CS*
WP*
HOLD*
THRM PAD
GND

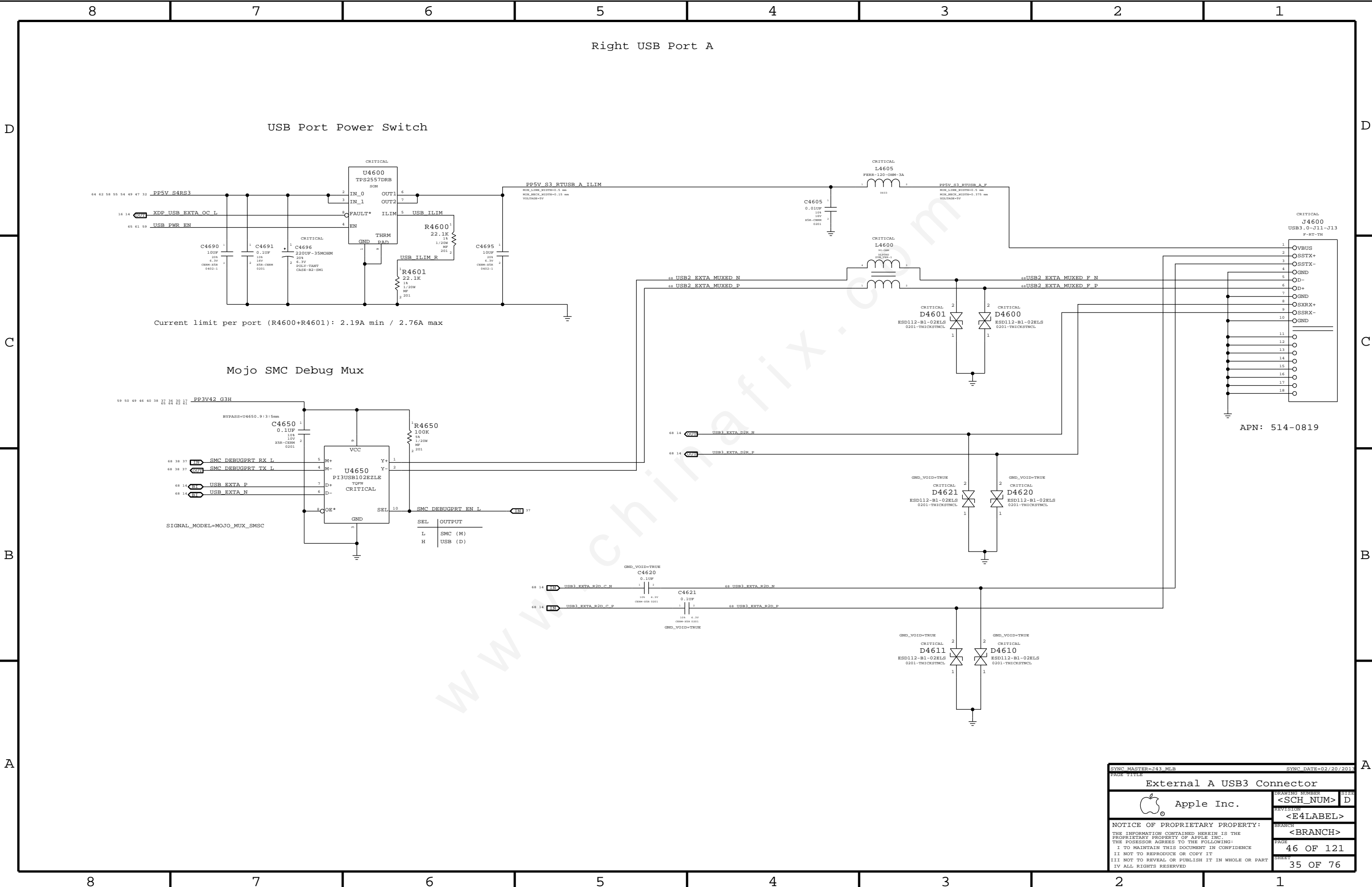
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25.000MHZ-12PF-20PPM
SM-3, 2X2, 5MHZ

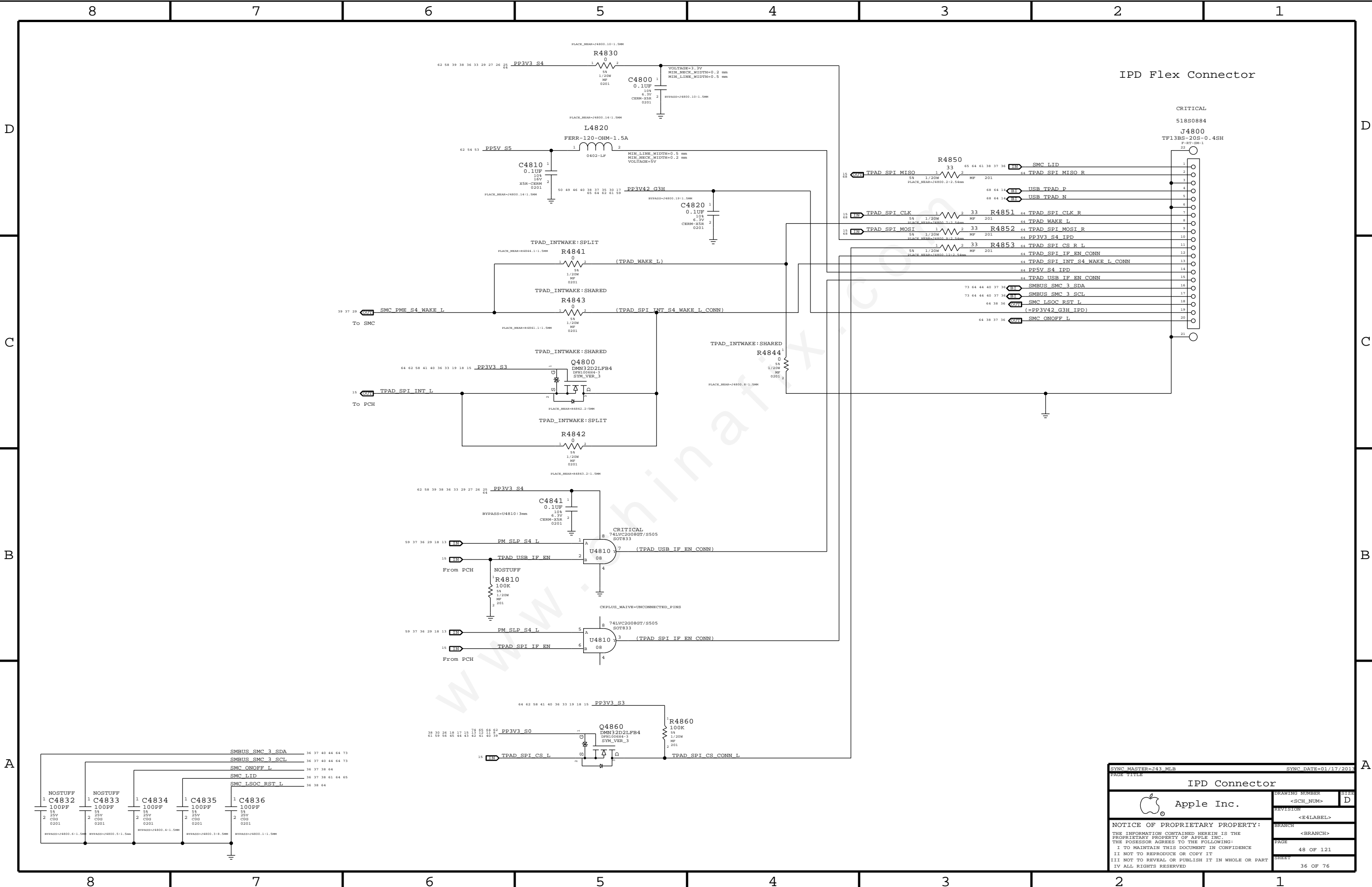
SD CONTROLLER (GL3219)


Apple Inc.

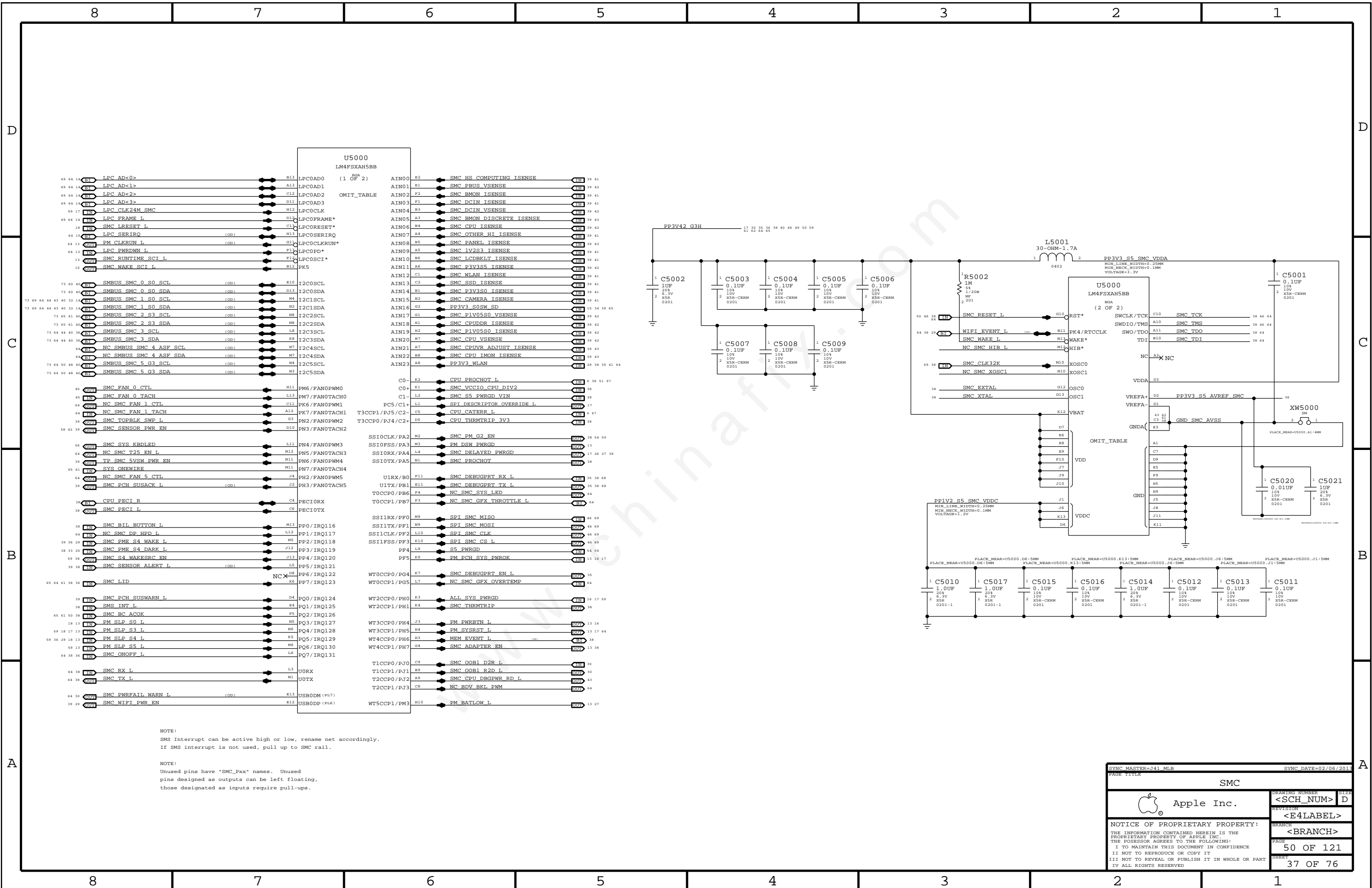
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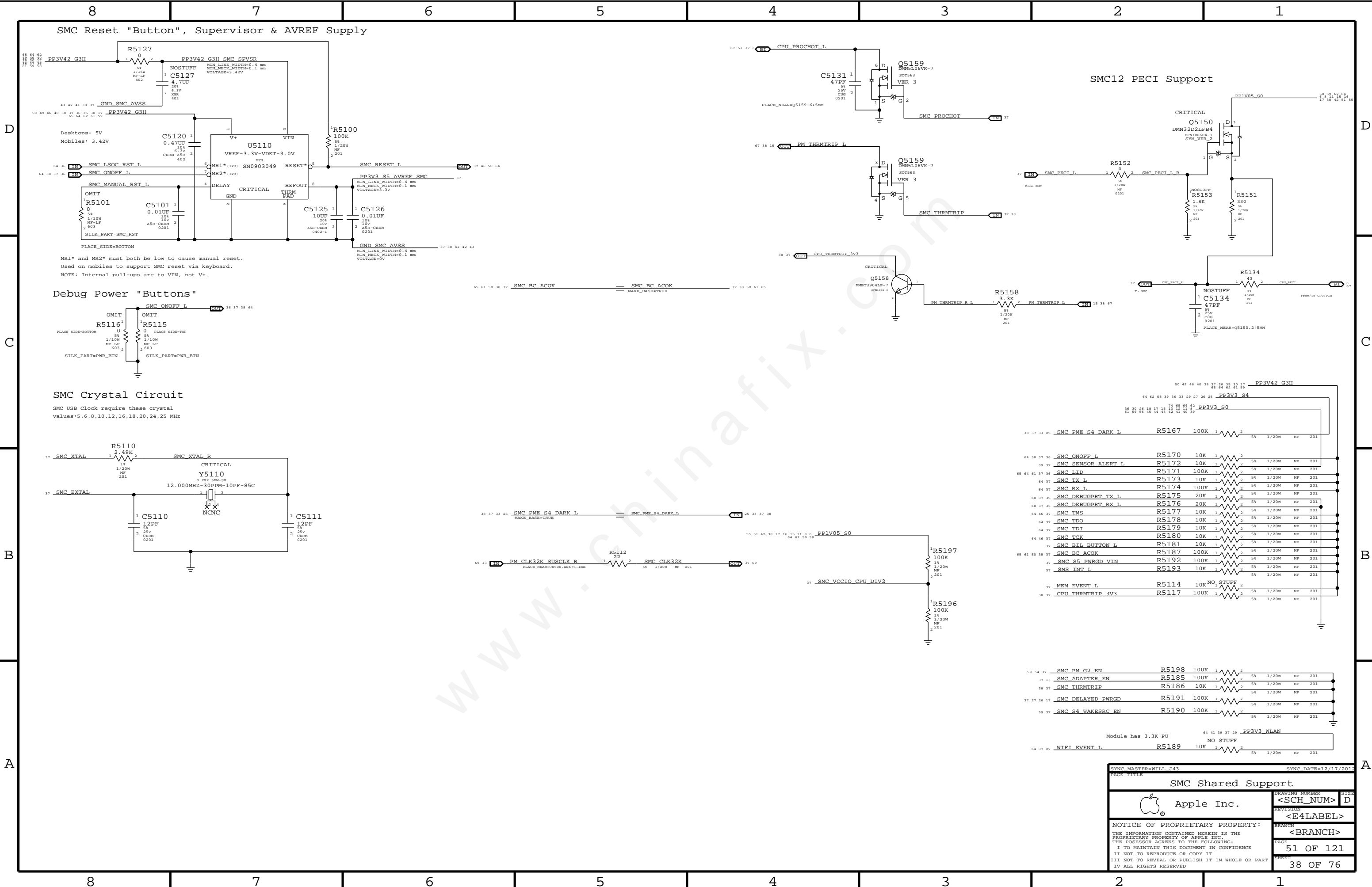
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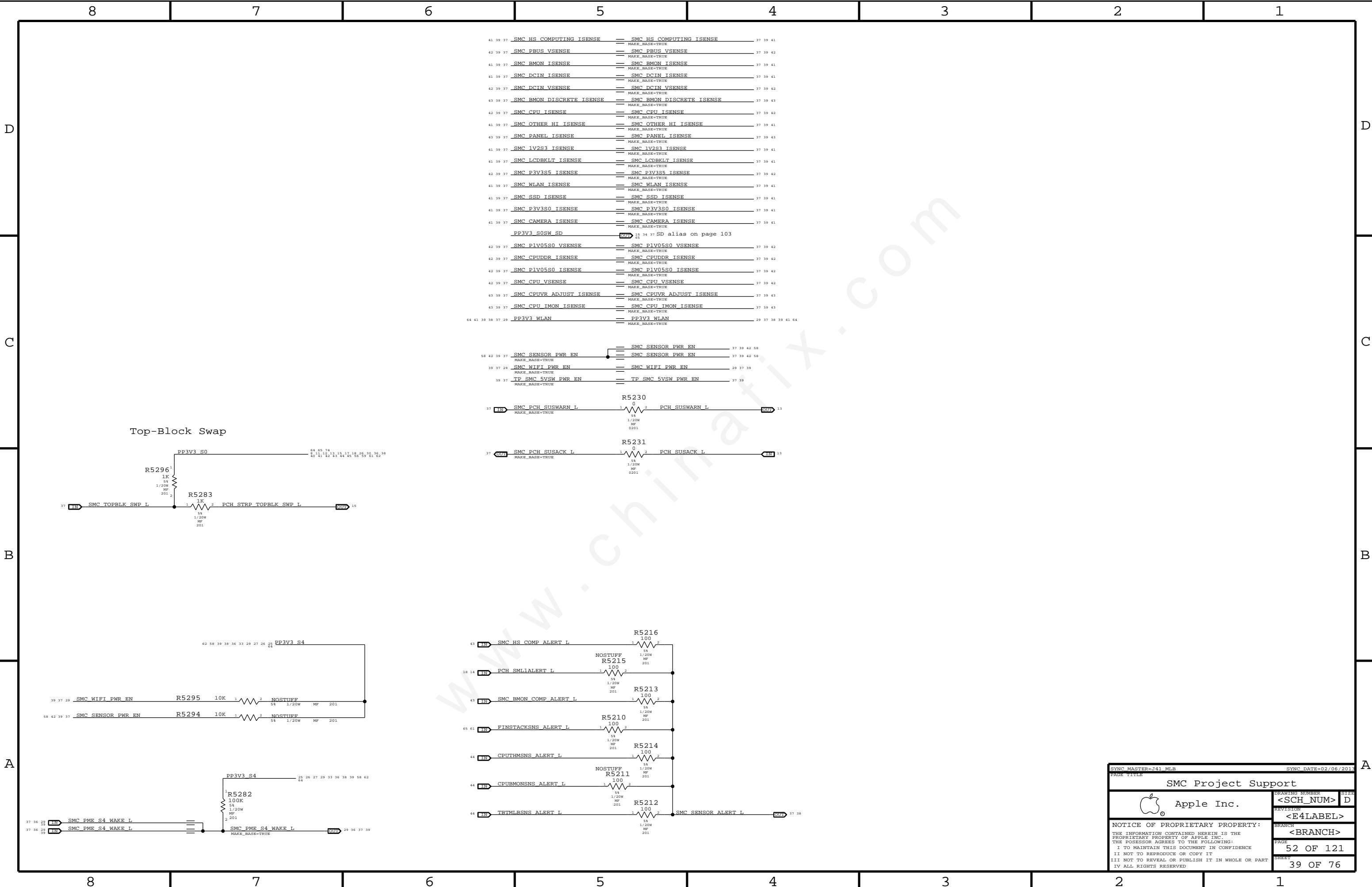


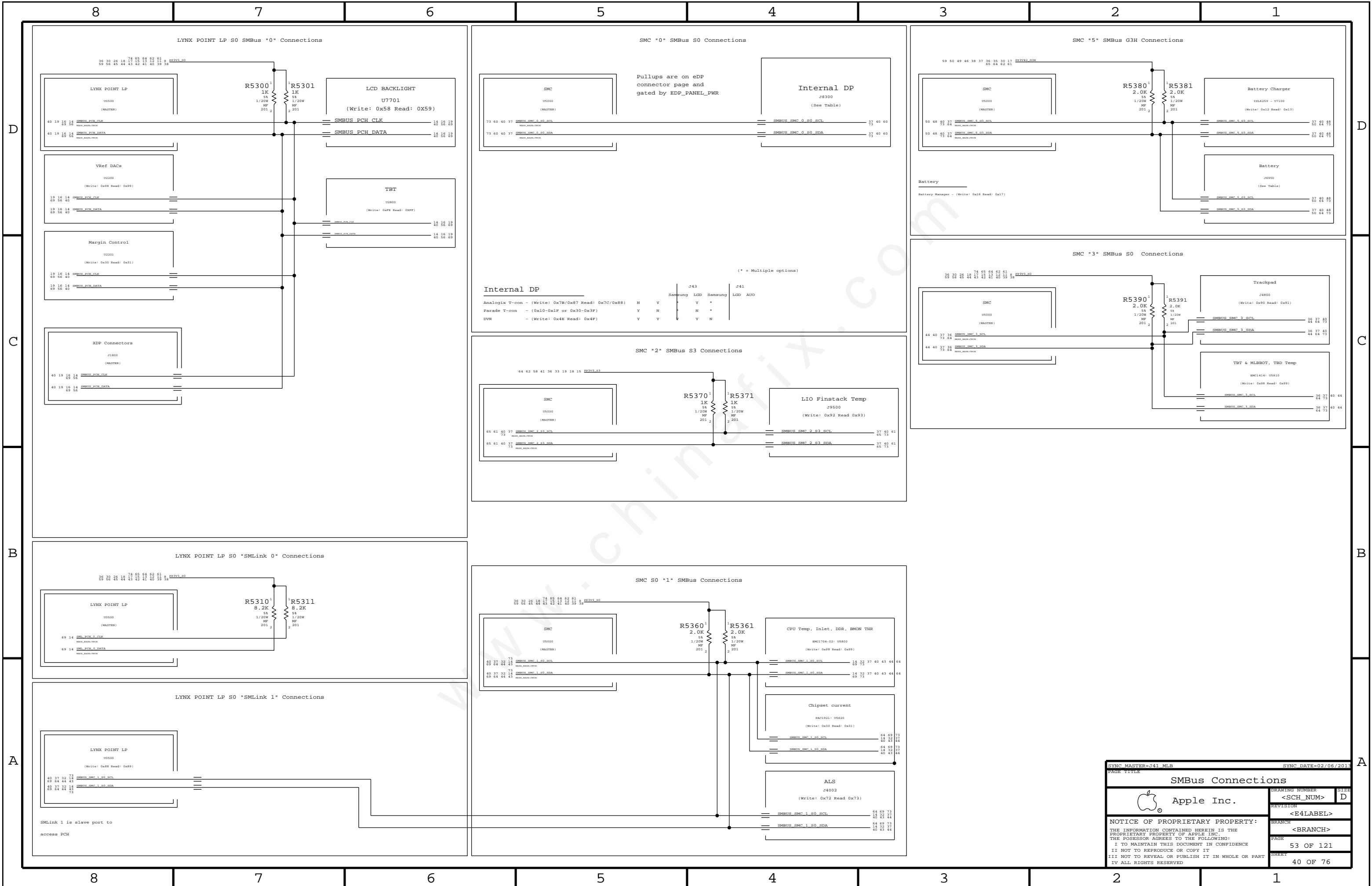
NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

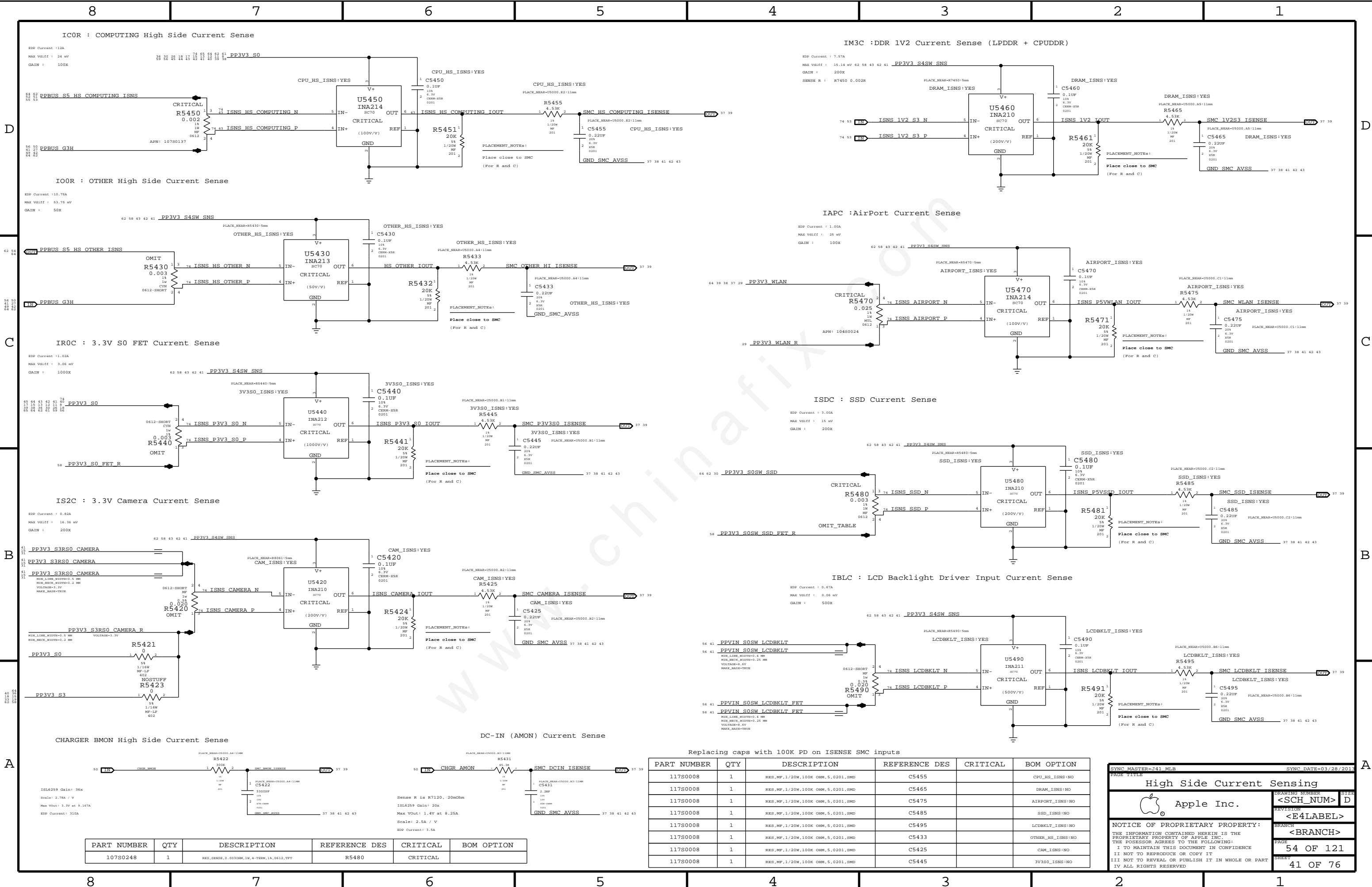
NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
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SMC			
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		BRANCH	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.00300M,1W,4-TERM,1A,0612,TPT	R5480	CRITICAL	

Replacing caps with 100K PD on ISENSE SMC inputs					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5475		SSD_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLT_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

SYNC MASTER=141 MLB

SYNC DATE=03/28/2013

High Side Current Sensing

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SIZE

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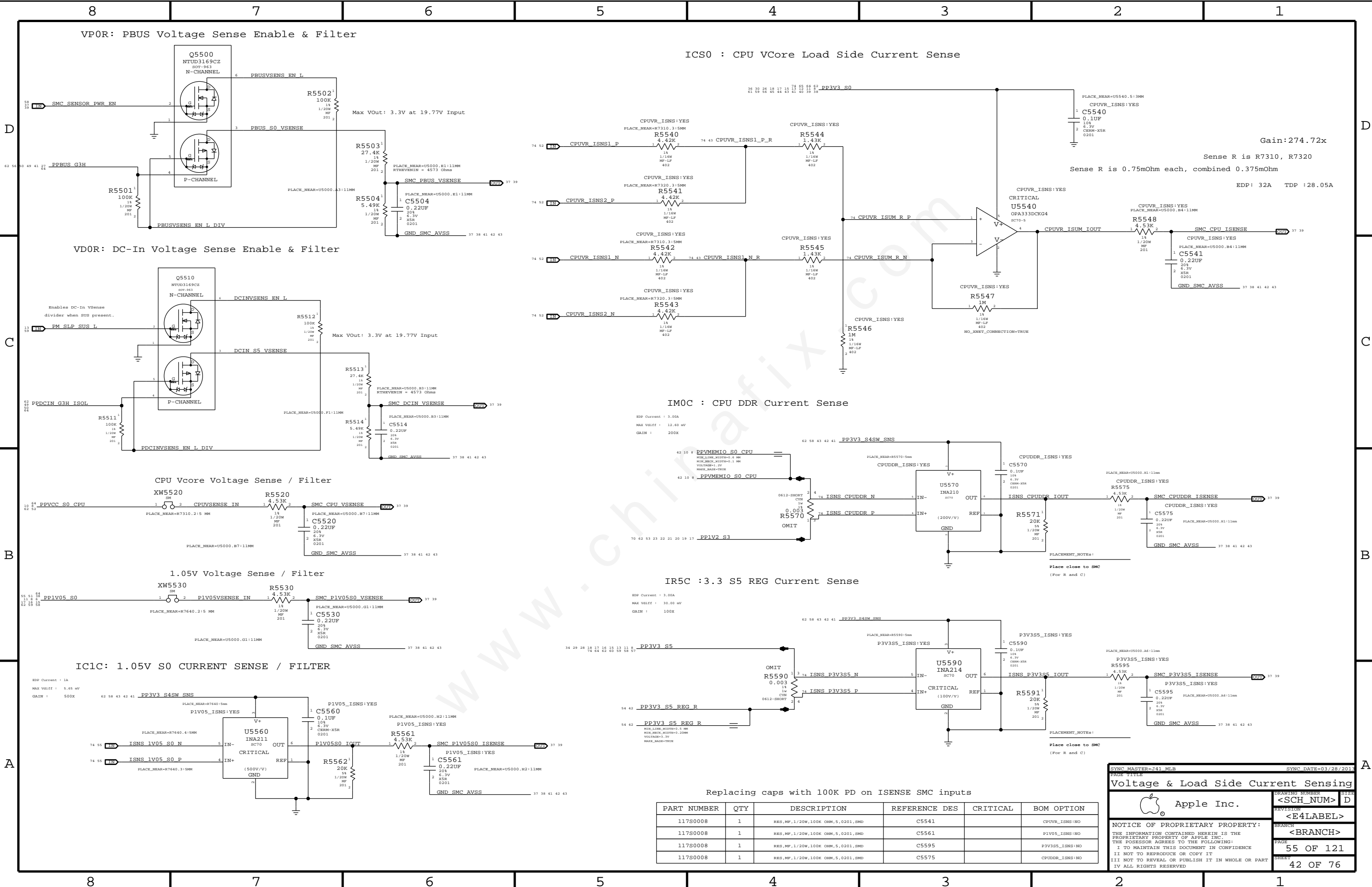
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Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

SYNC MASTER=J41 MLB

SYNC DATE=03/28/2013

Voltage & Load Side Current Sensing

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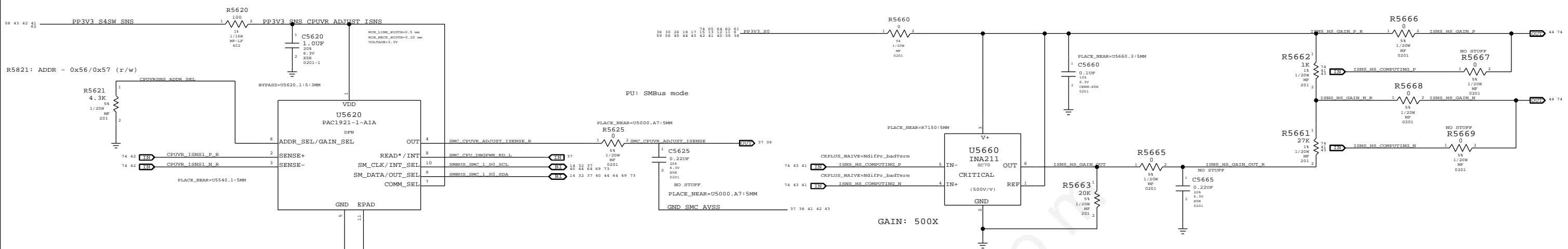
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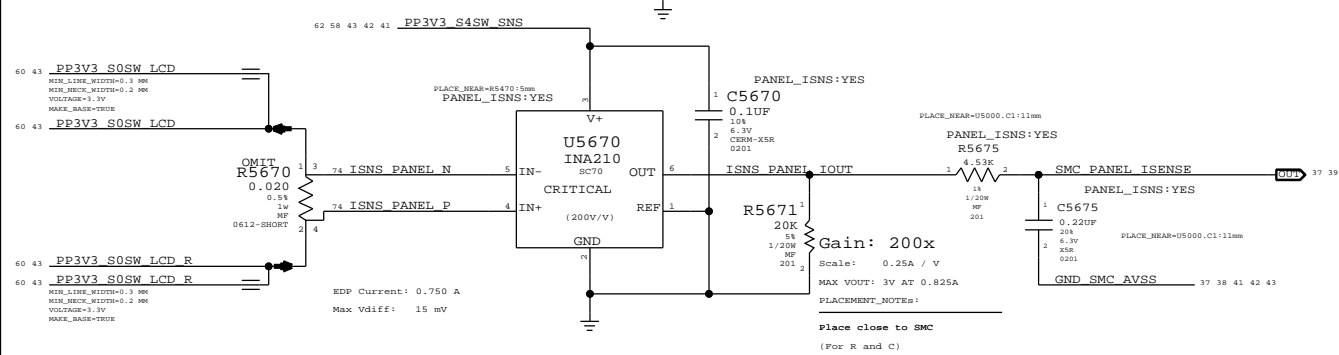
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ICS3 : Adjustable Gain CPU VR Current

Sense Pins gain stage for U5800 (EMC1704)



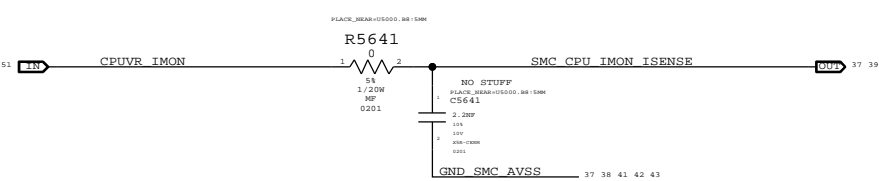
ILDC :LCD Panel Current Sense / Filter



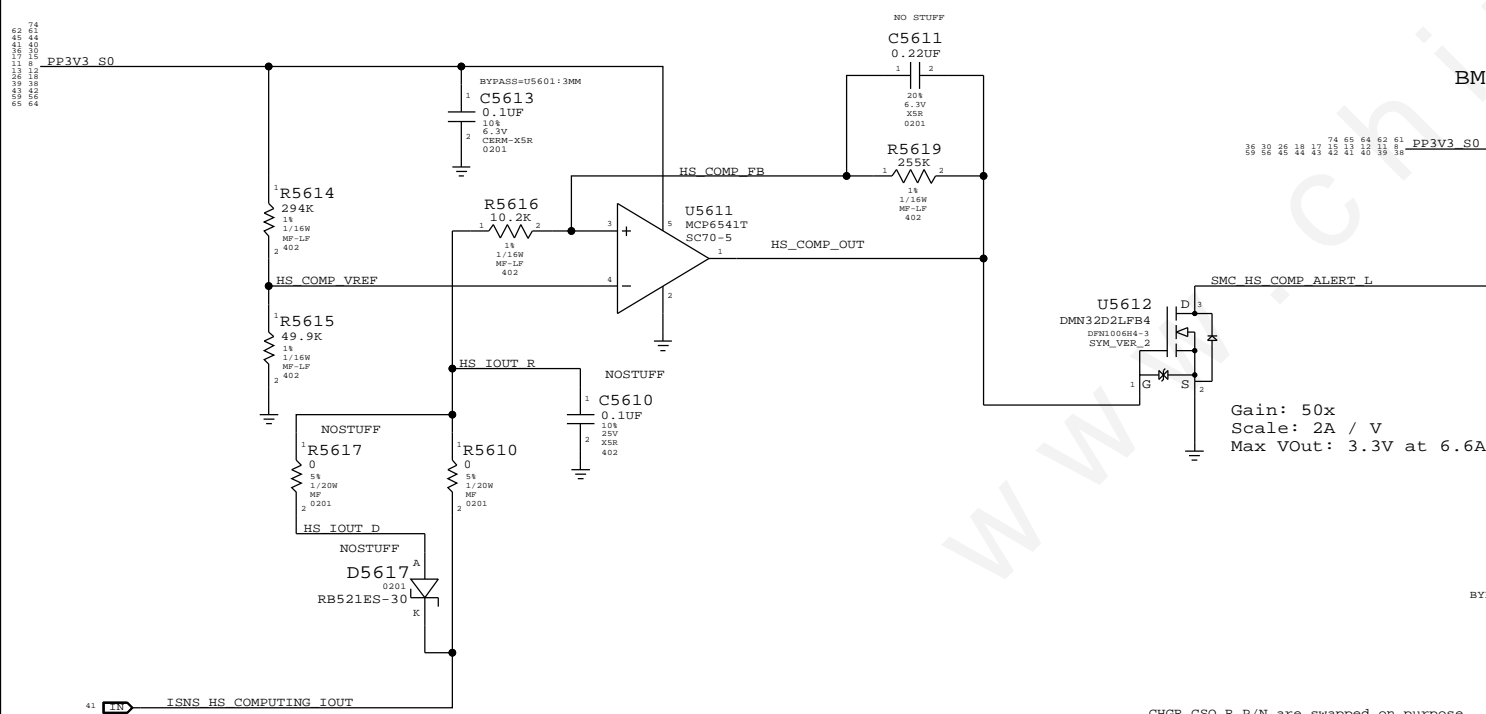
In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800. This will set the mininum current threshold at 0.100mA

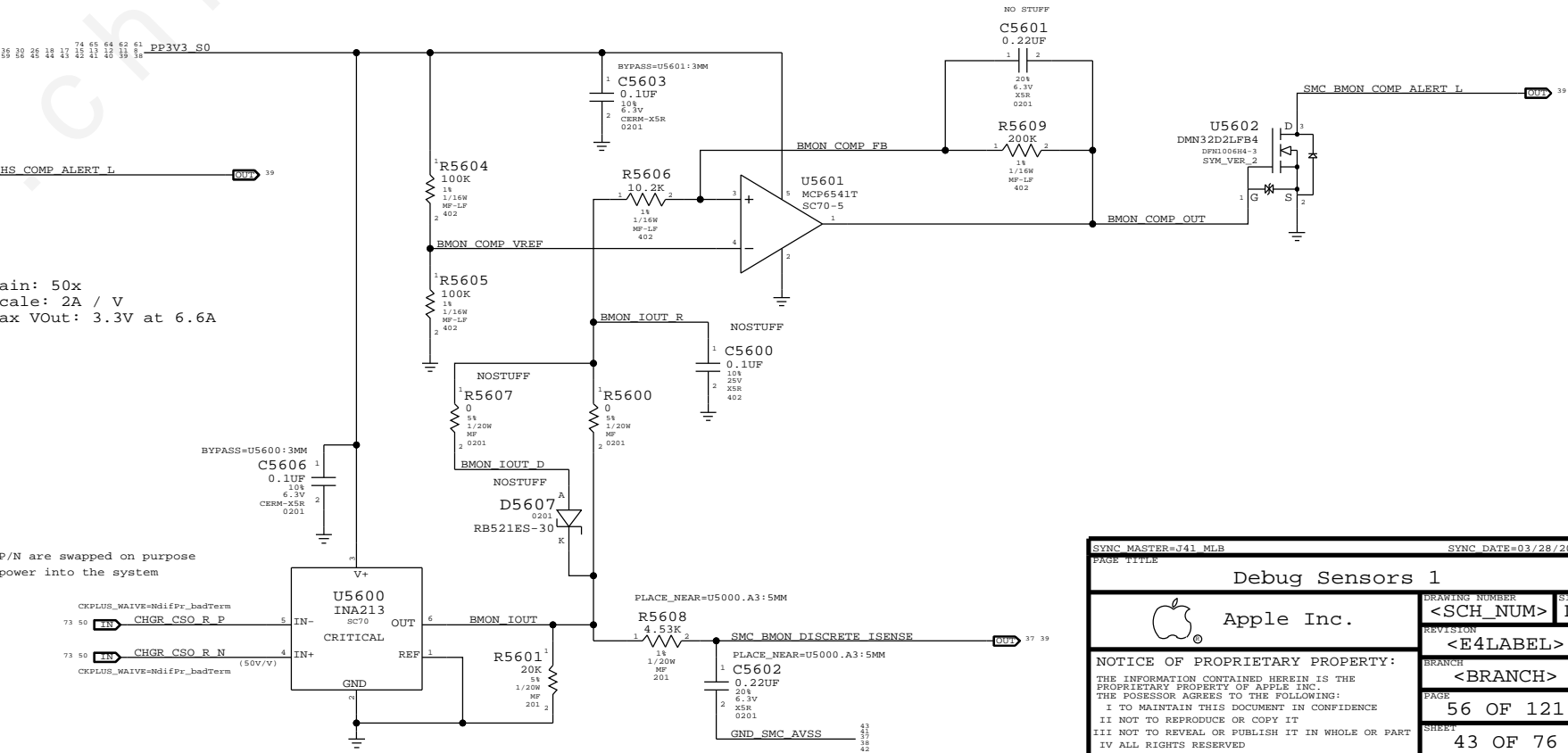
VR IMON Current Sense Filter



Discrete High side Current threshold



BMON : Discrete BMON Current Sense / Filter



Vref = 0.406mV Vth = 0.442 = 1A from Battery
Vtl = 0.290mV = 0.687A from battery
Hysteresis TBD based on RC value changes

Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

CHGR_CSO_R/P/N are swapped on purpose to measure power into the system

Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

SYNC MASTER=J41 MLB

SYNC DATE=03/28/2013

Debug Sensors 1

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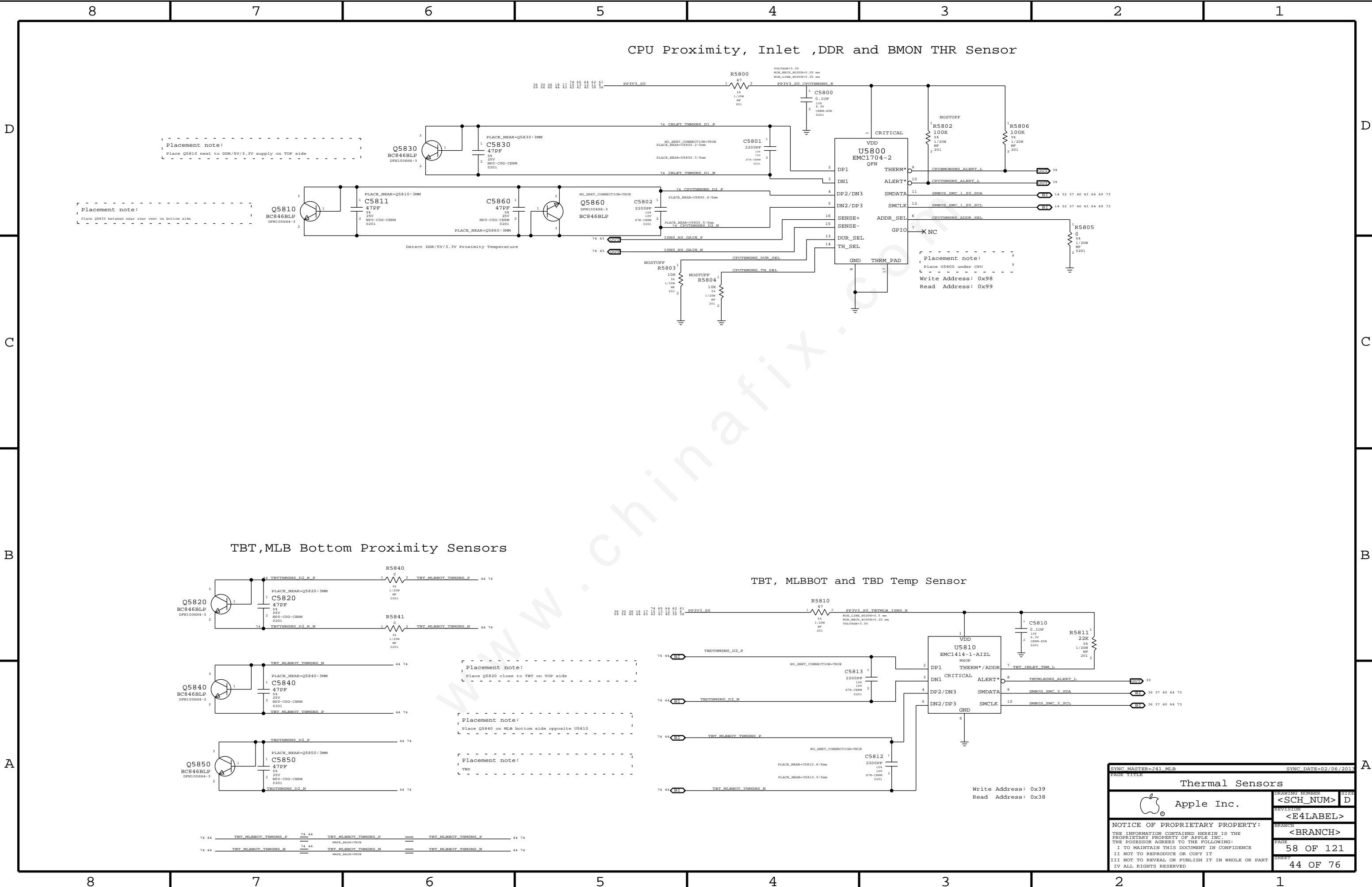
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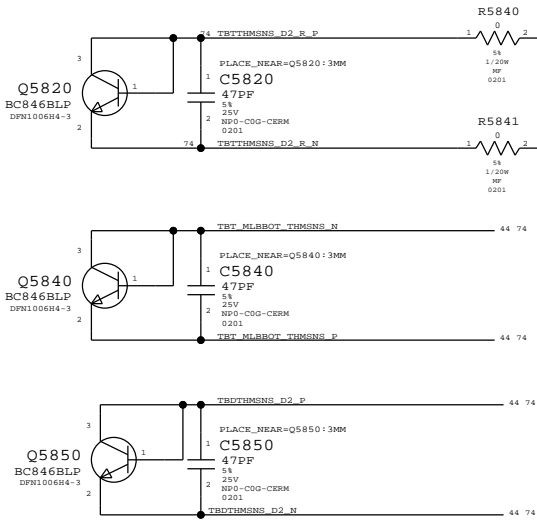
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TBT,MLB Bottom Proximity Sensors

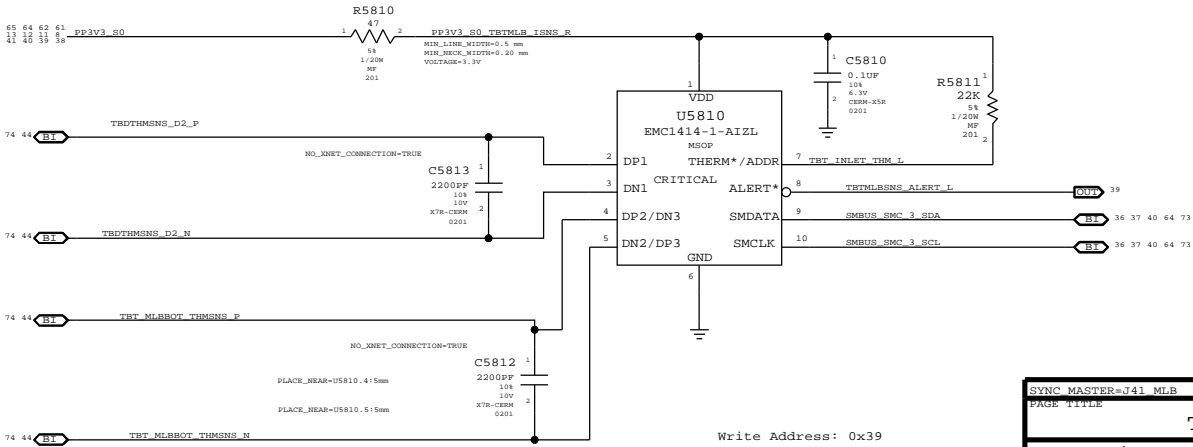


Placement note:
Place Q5820 close to TBT on TOP side


Placement note:
Place Q5840 on MLB bottom side opposite U5810

Placement note:
TBT

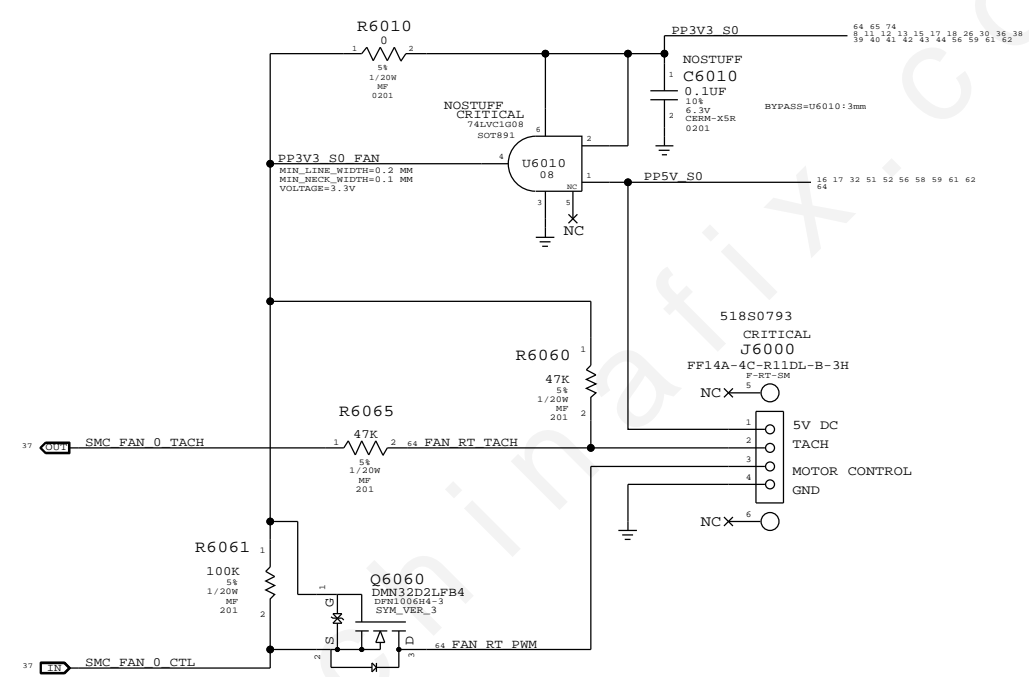
TBT, MLBBOT and TBD Temp Sensor




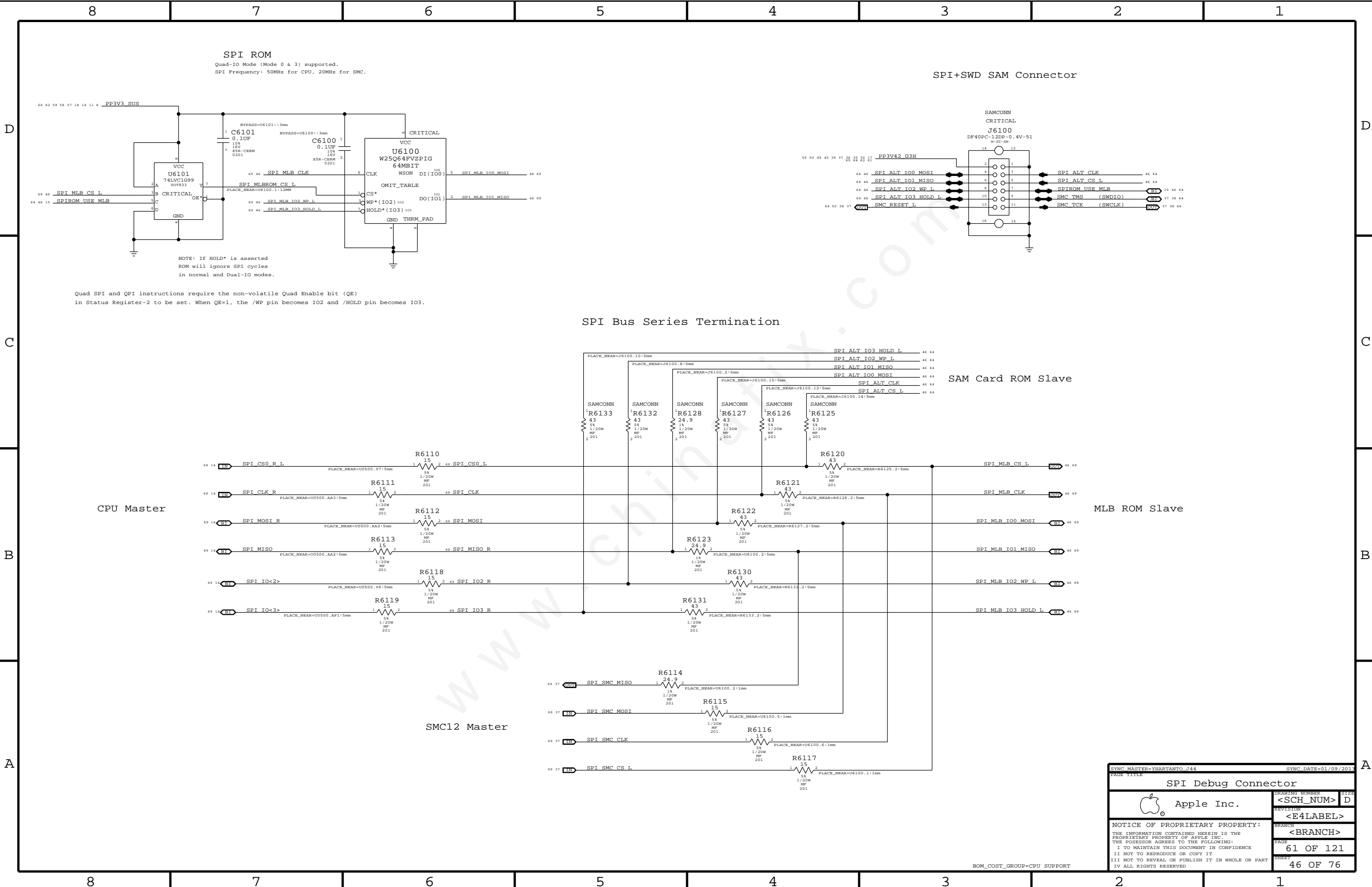
Write Address: 0x39
Read Address: 0x38

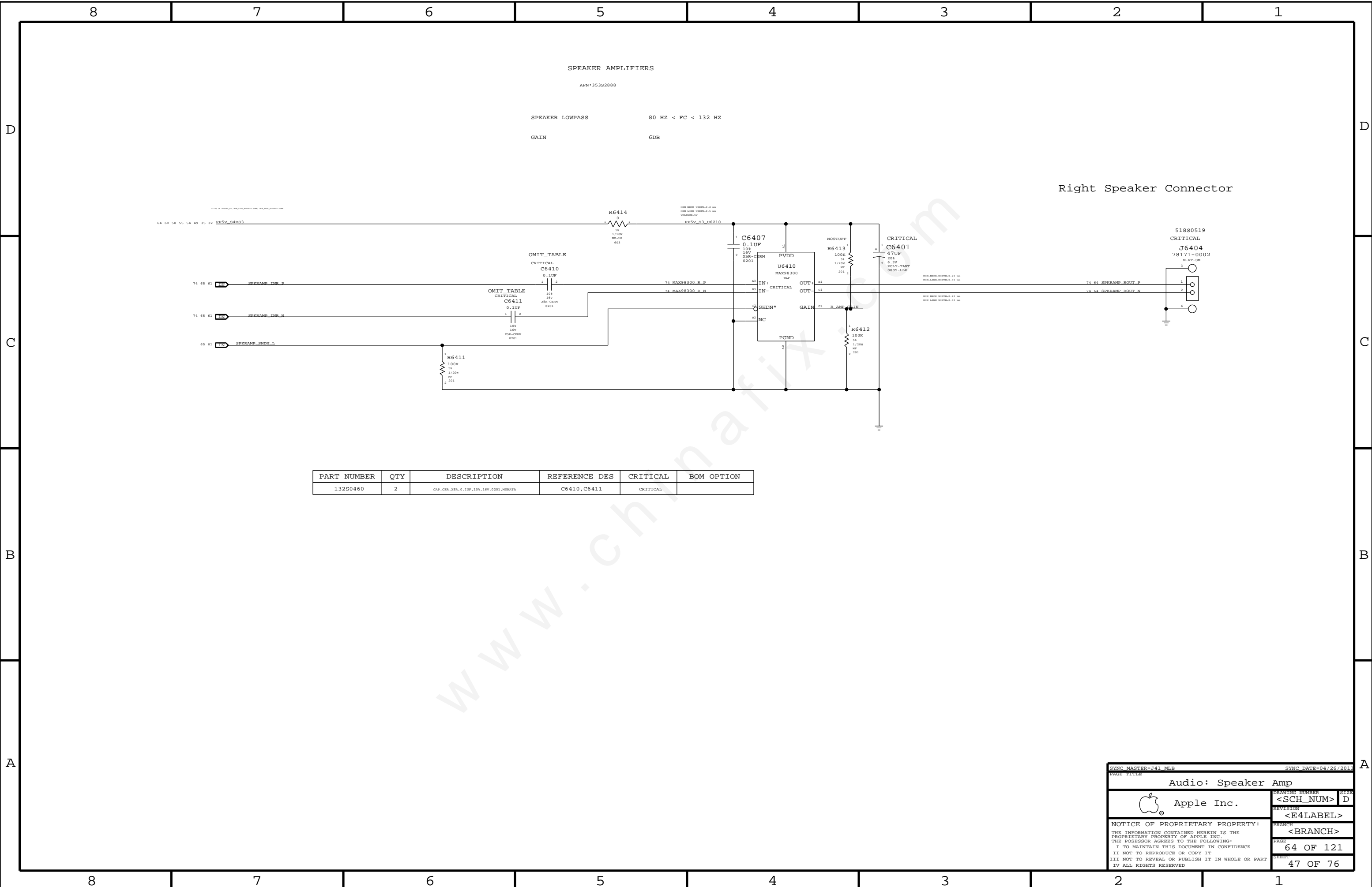
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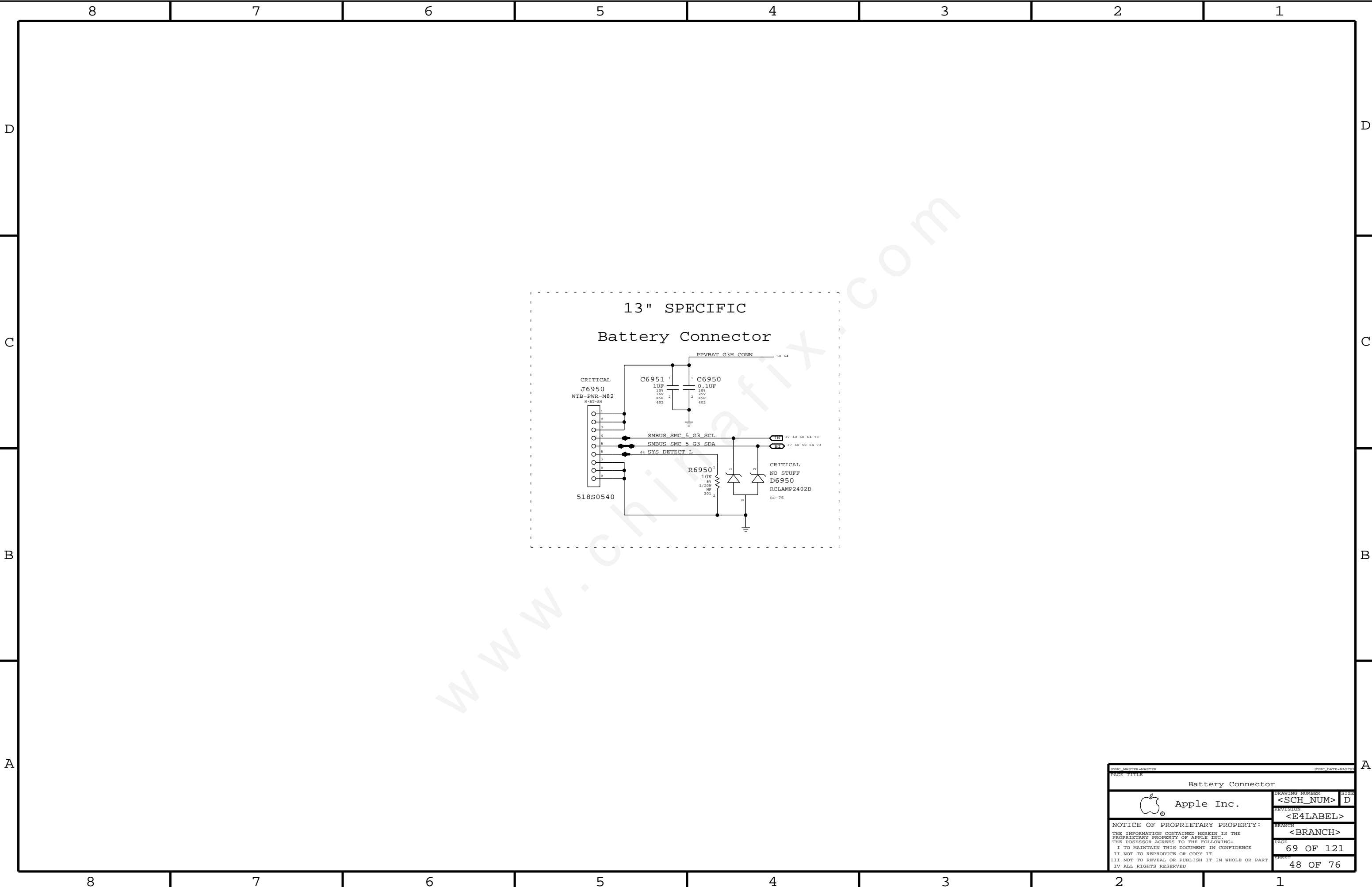
FAN CONNECTOR



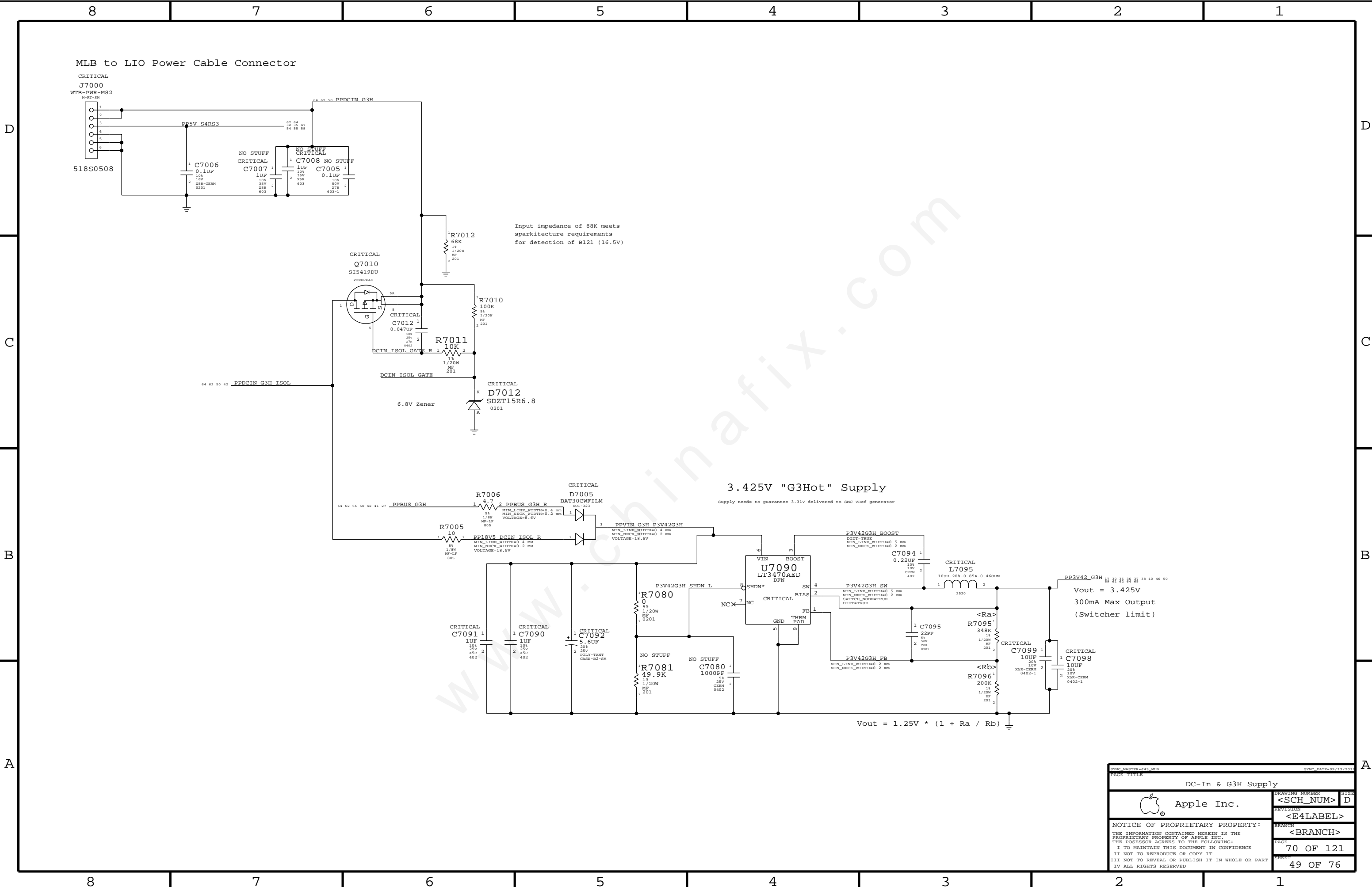
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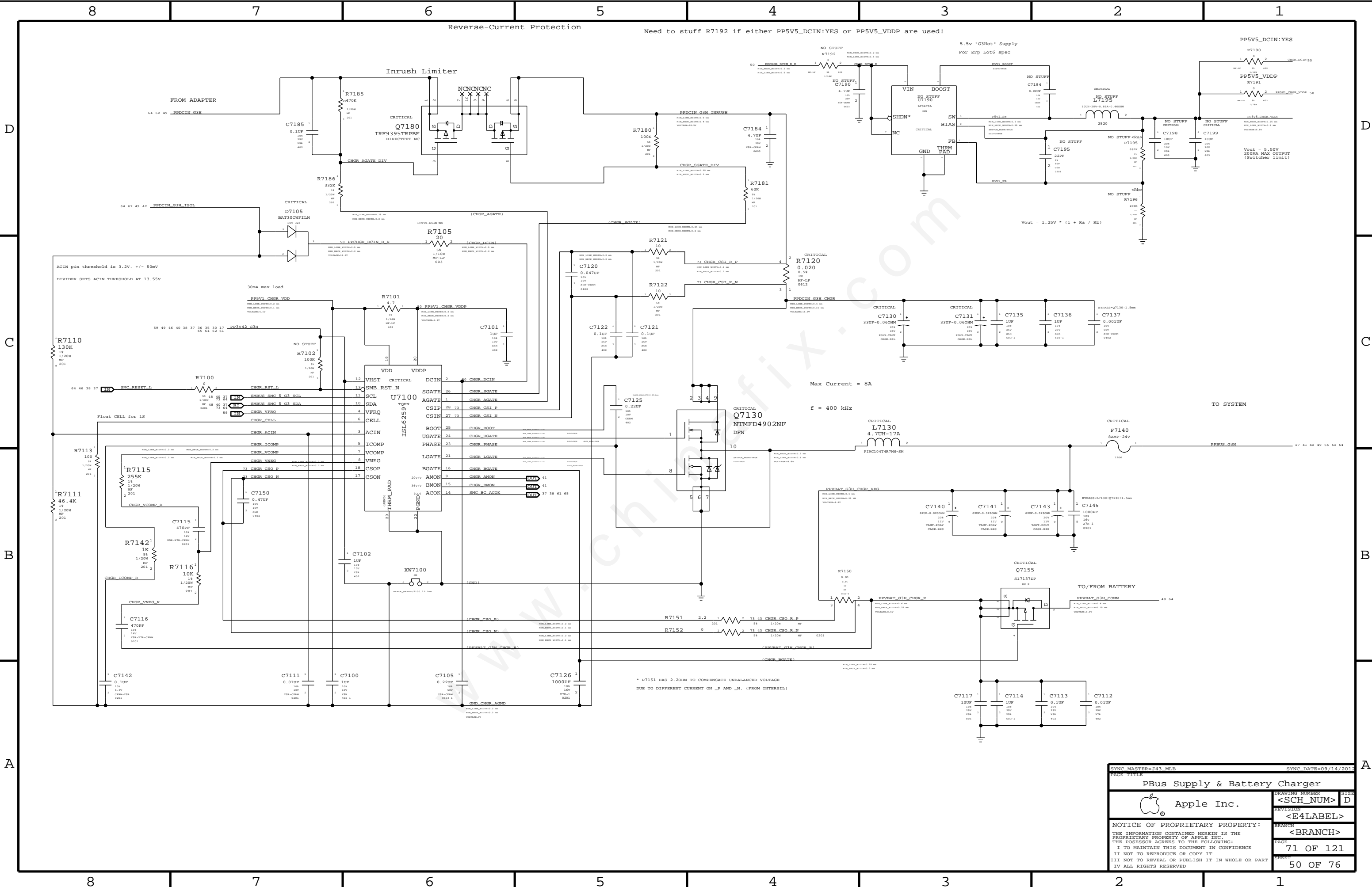



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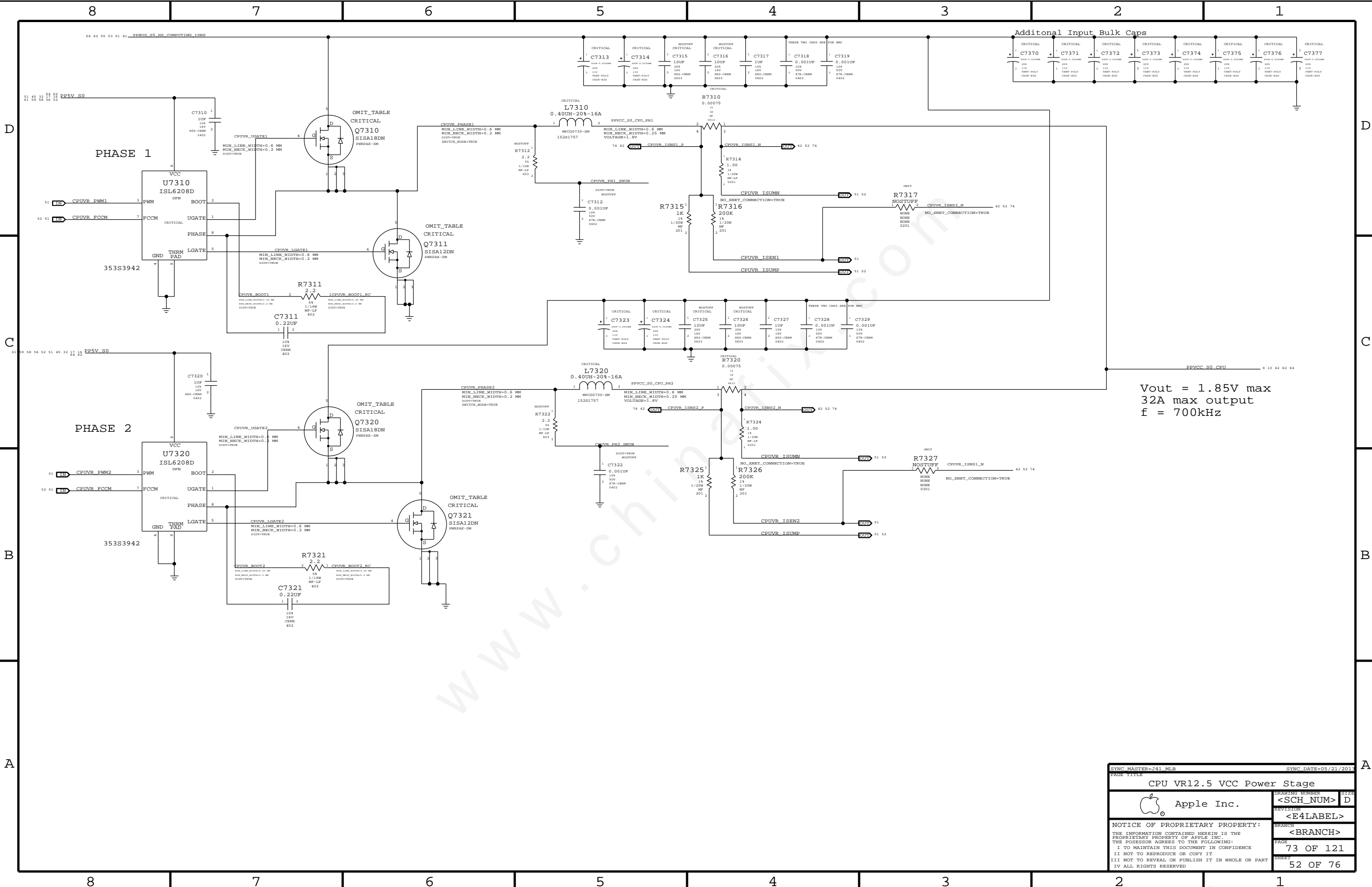
DC-In & G3H Supply


 Apple Inc.

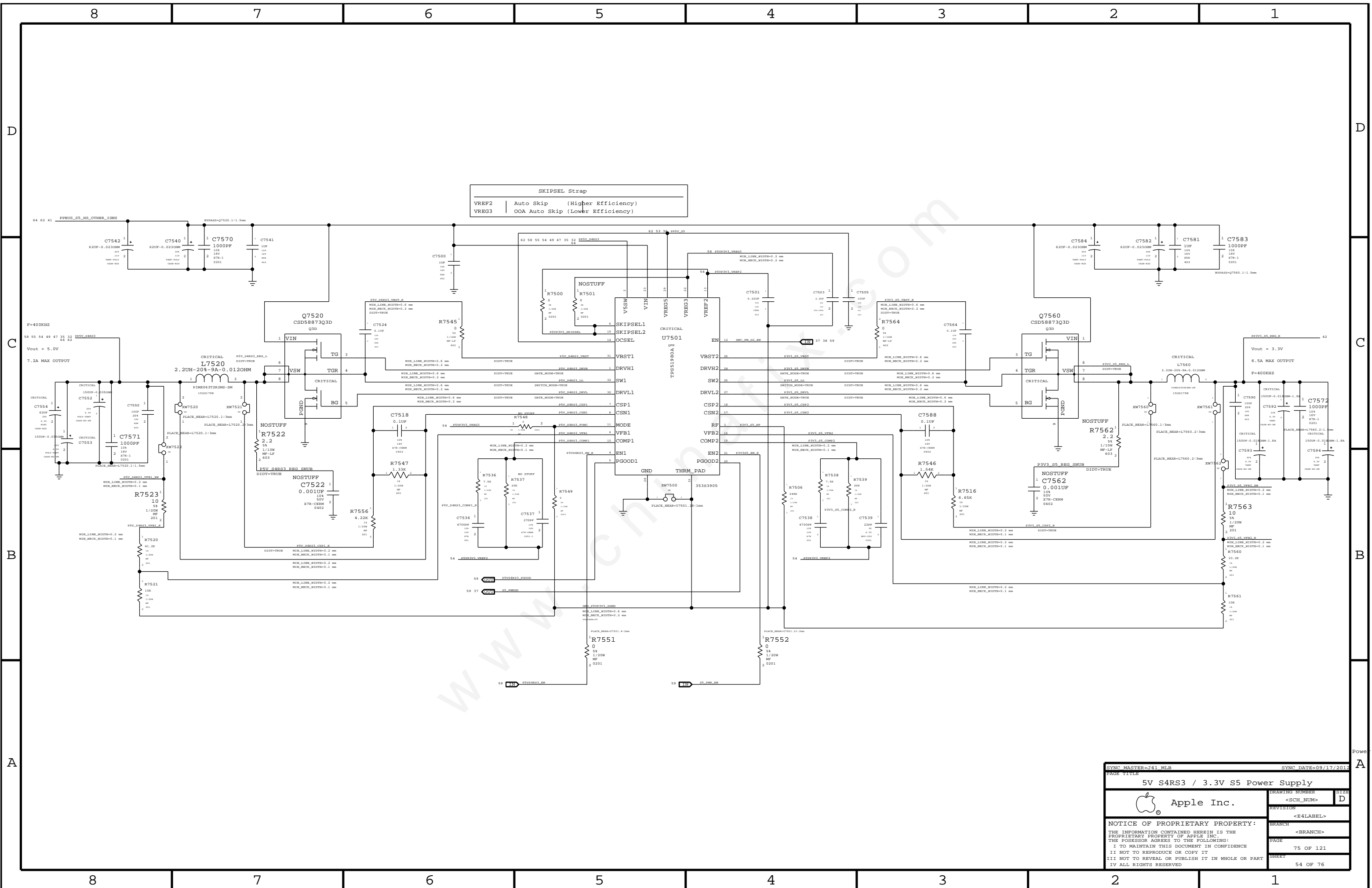
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


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PBus Supply & Battery Charger			
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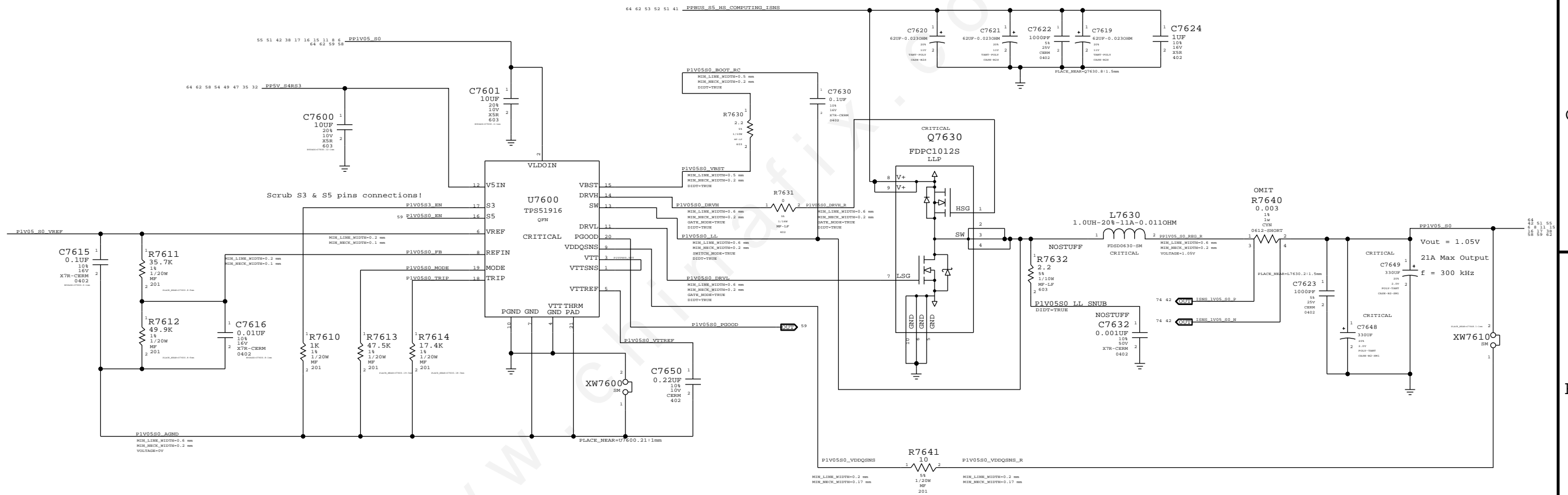



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CPU VR12.5 VCC Power Stage			
 Apple Inc.	DRAWING NUMBER		SIZE
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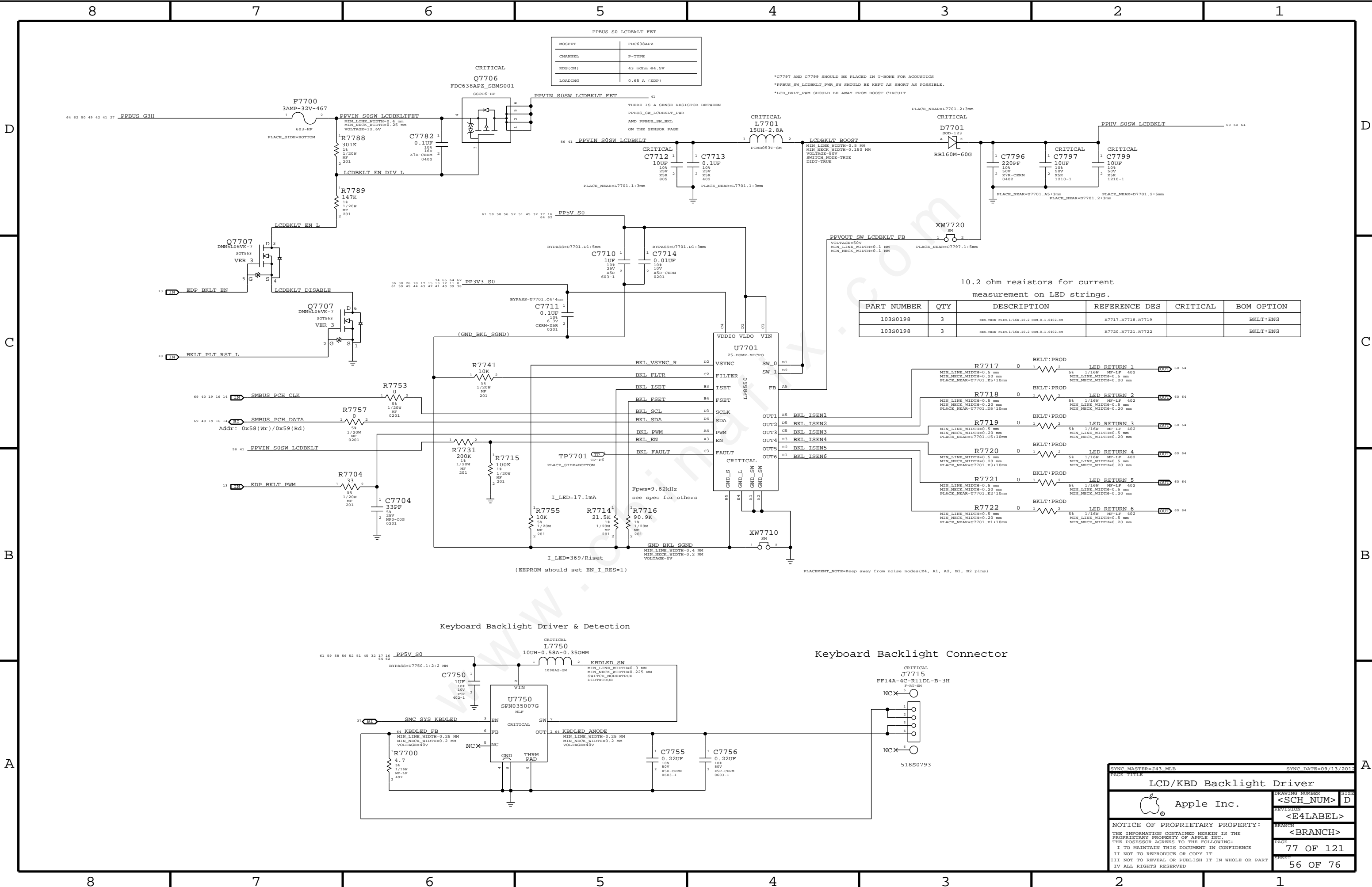


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5V S4RS3 / 3.3V S5 Power Supply			
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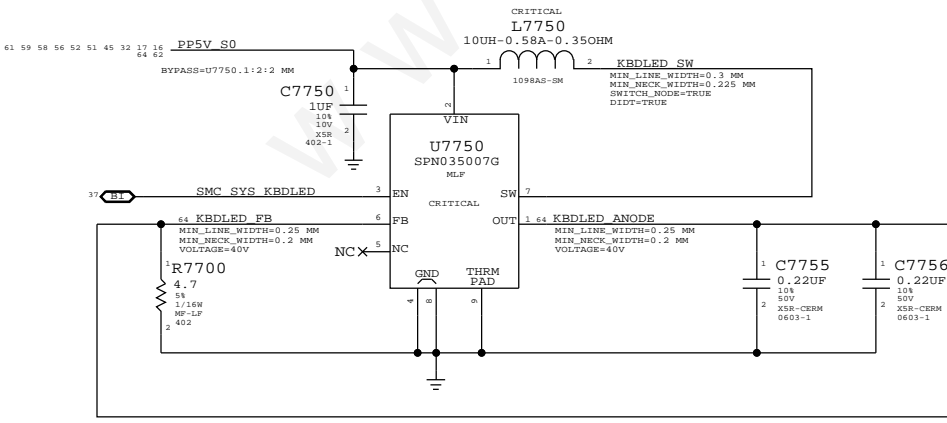
1.05V S0 Regulator



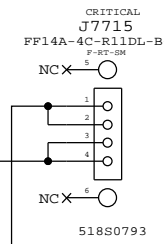
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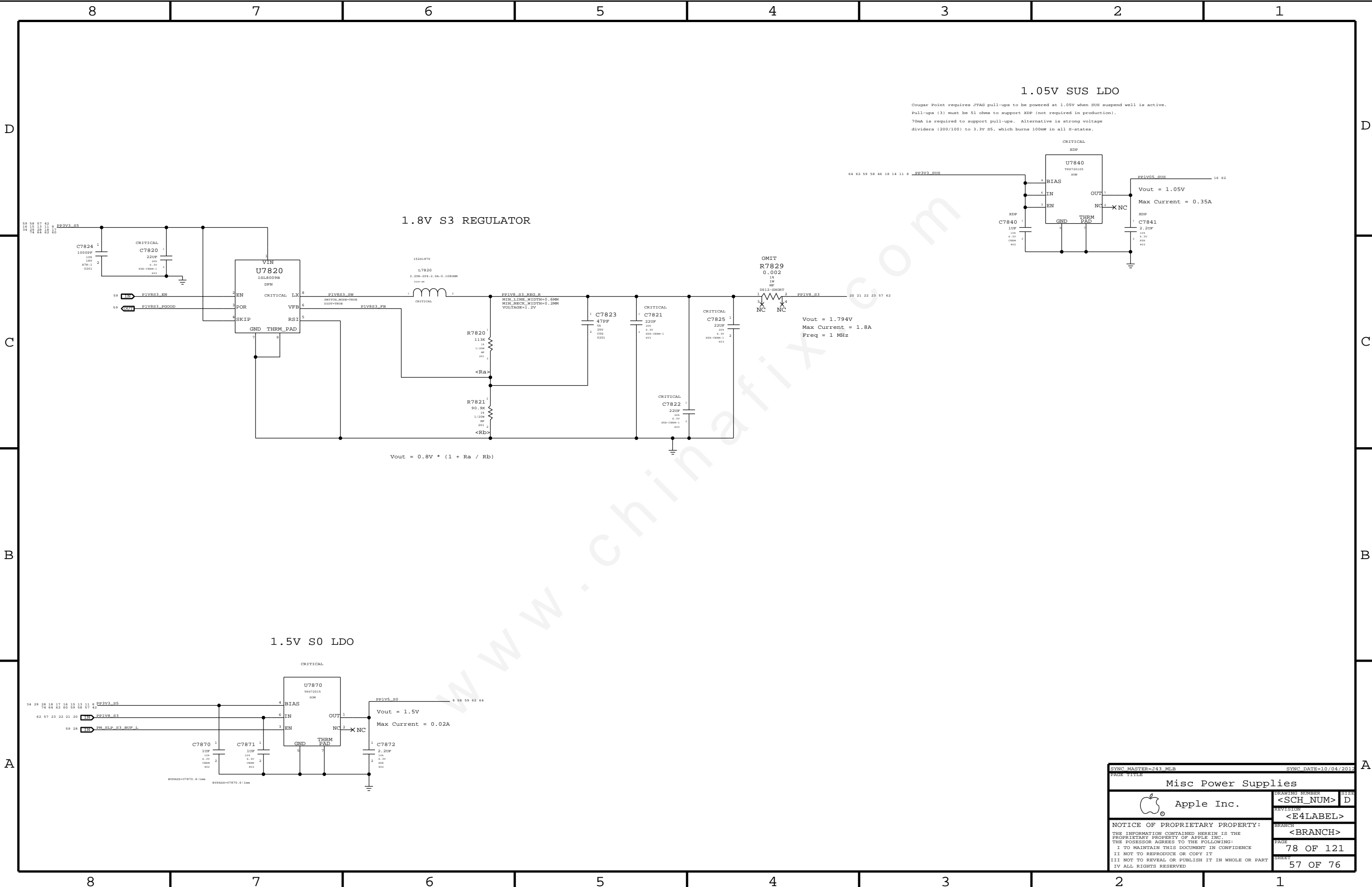


Keyboard Backlight Driver & Detection

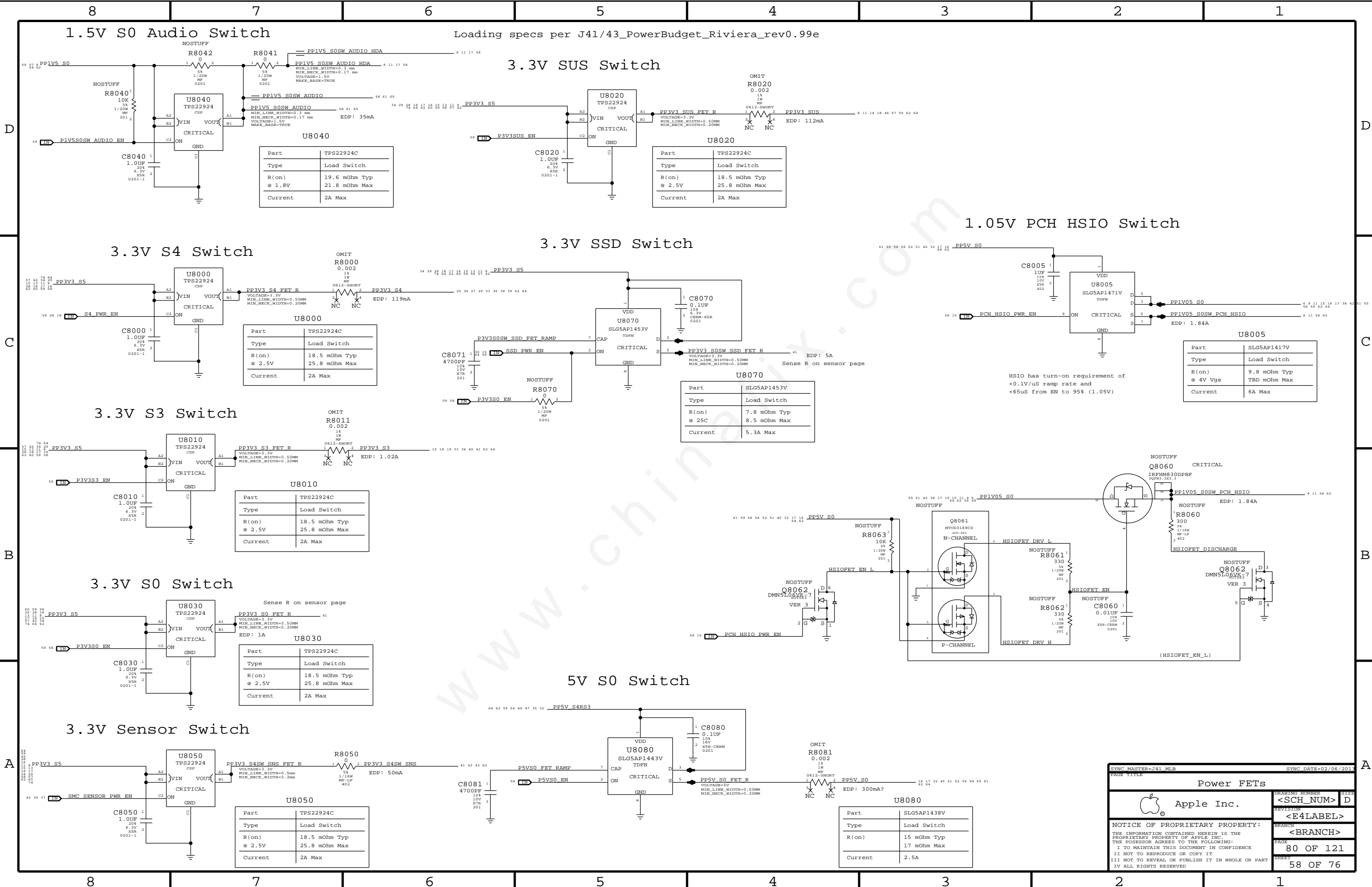


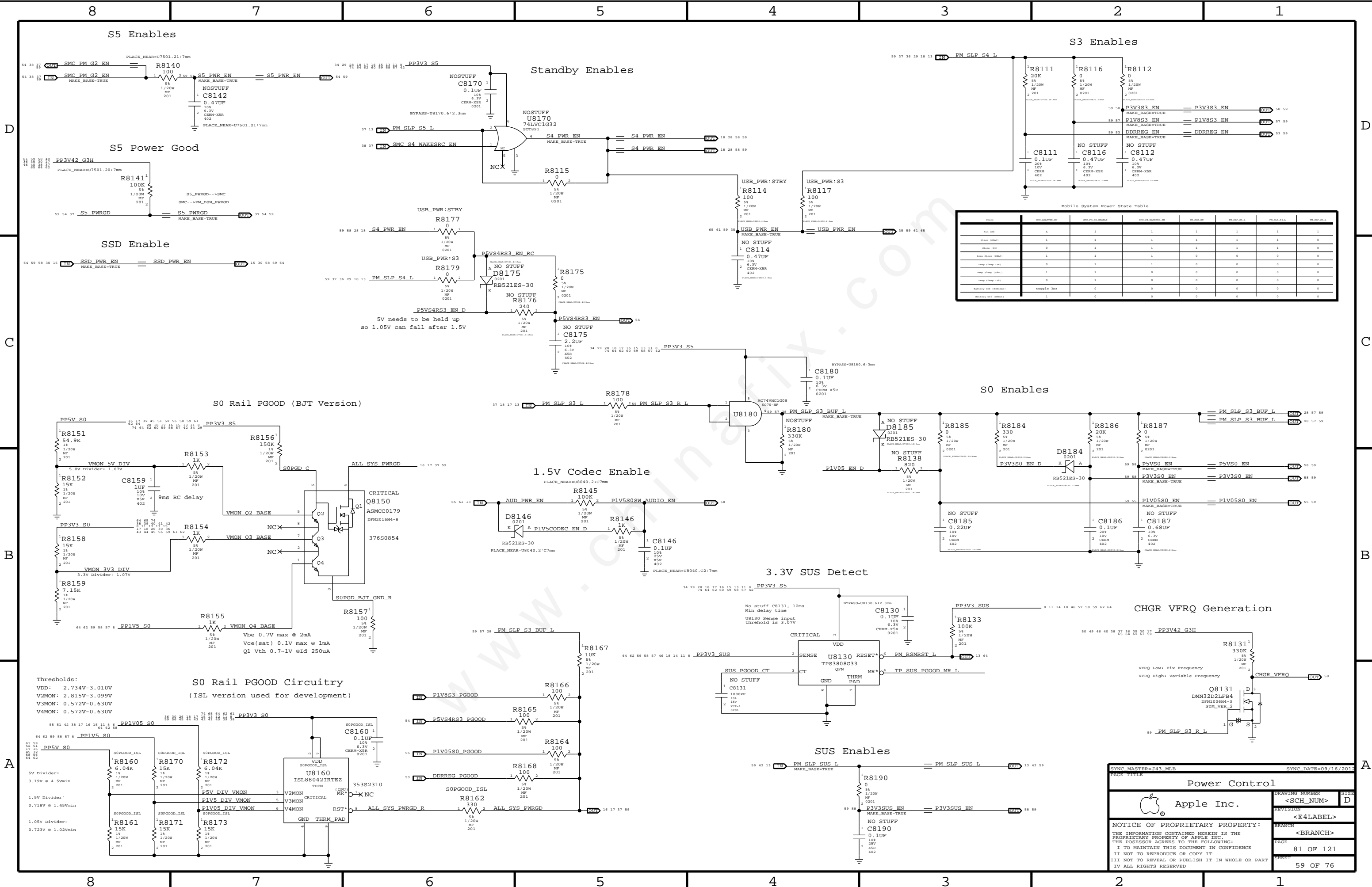
Keyboard Backlight Connector





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REVISION		BRANCH	
<E4LABEL>		<BRANCH>	
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Mobile System Power State Table							
STATE	PMC_ADAPTER_EN	PMC_PMC2_ENABLE	PMC_PMC3_ENABLE	PM_P0S0_EN	PM_P0S1_L	PM_P0S1_L	PM_P0S1_L
Run (001)	X	1	1	1	1	1	1
Standby (000)	1	1	1	1	1	1	0
Sleep (001)	0	1	1	1	1	1	0
Deep Sleep (000)	1	1	1	0	0	0	0
Deep Sleep (001)	0	1	1	0	0	0	0
Deep Sleep (000)	1	1	1	0	0	0	0
Deep Sleep (001)	0	1	1	0	0	0	0
Deep Sleep (000)	1	1	1	0	0	0	0
Workday OFF (000000)	Toggle 1Hz	0	0	0	0	0	0
Workday OFF (000001)	1	0	0	0	0	0	0

SYNC MASTER=J43 MLB

SYNC DATE=09/16/2012

PAGE TITLE

Power Control

Apple Inc.

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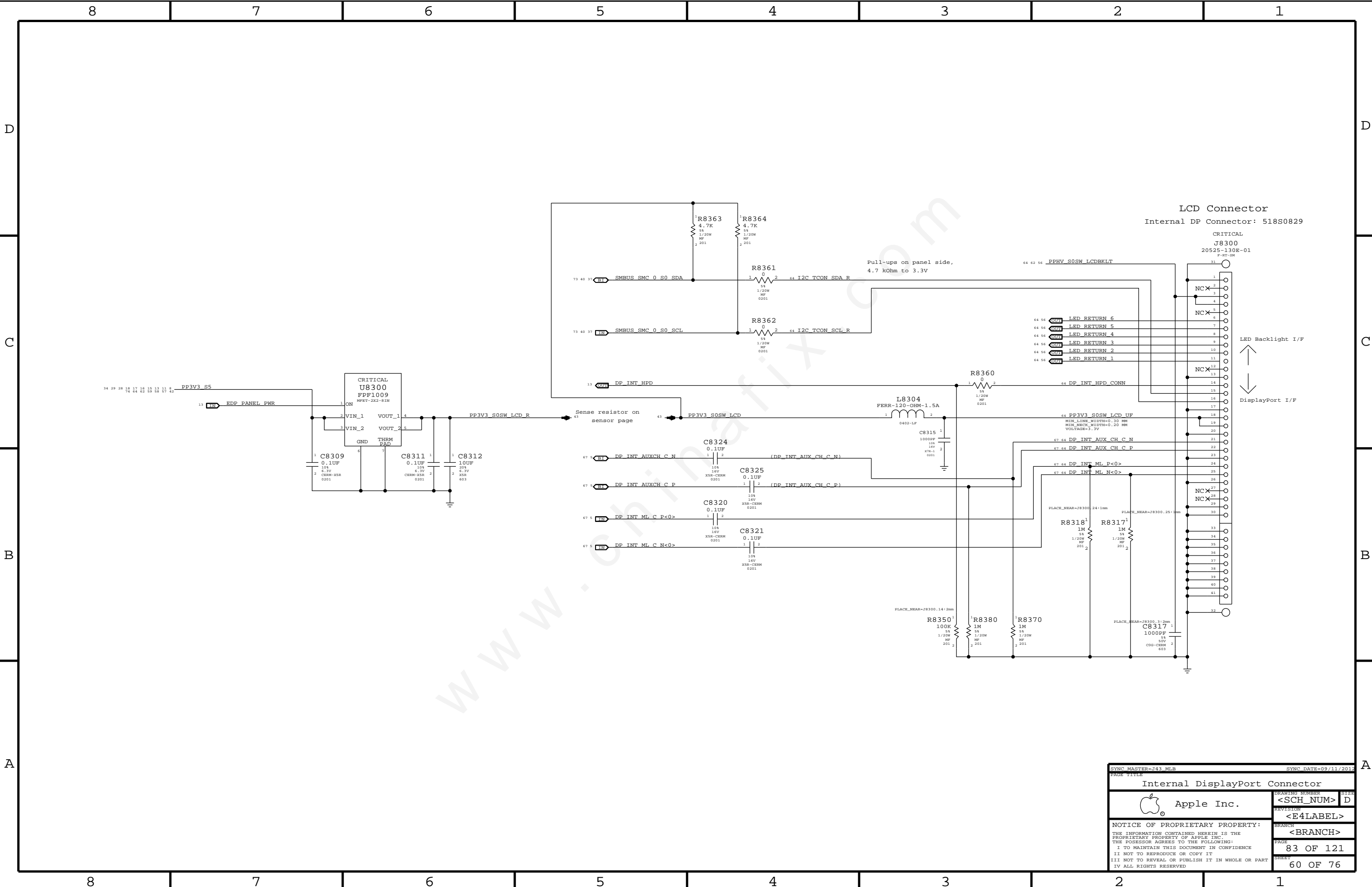
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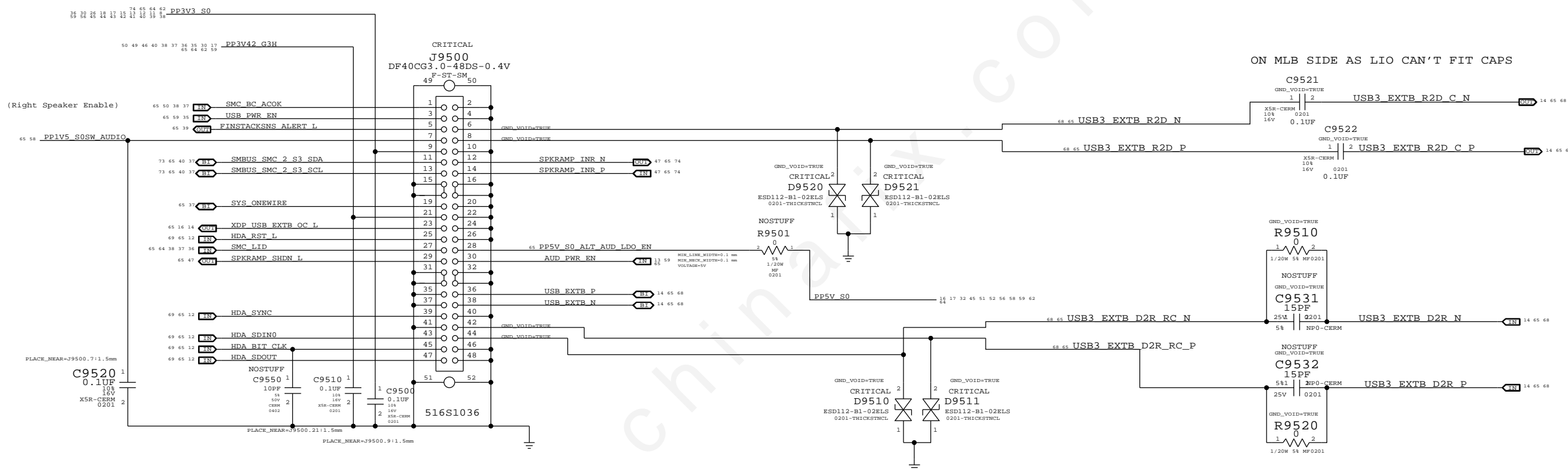
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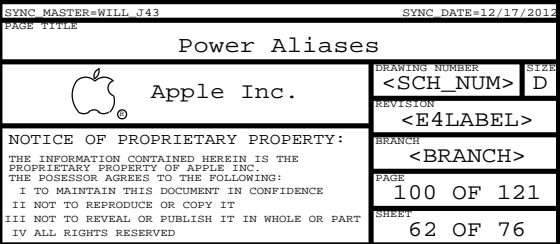
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SYNC MASTER=J43 MLB		SYNC DATE=09/11/2012		
PAGE TITLE				
Internal DisplayPort Connector				
 Apple Inc.	DRAWING NUMBER		SIZE	
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8	7	6	5	4	3	2	1	
Memory Bit/Byte Swizzle								
LPDDR3 Command/Address								
D	MAKE_BASE		MAKE_BASE		MAKE_BASE			
	7	=MEM A A<5>	20	=MEM A A<0>	22	=MEM B B DQ<0>	7 70	
	7	=MEM A A<9>	20	=MEM A A DQ<1>	22	=MEM B B DQ<1>	7 70	
	7	=MEM A A<6>	20	=MEM A A DQ<2>	22	=MEM B B DQ<2>	7 70	
	7	=MEM A A<8>	20	=MEM A A DQ<3>	22	=MEM B B DQ<3>	7 70	
	7	=MEM A A<7>	20	=MEM A A DQ<4>	22	=MEM B B DQ<4>	7 70	
	7	=MEM A BA<2>	20	=MEM A A DQ<5>	22	=MEM B B DQ<5>	7 70	
	70 63 24 20 7	=MEM A CAA<6>	7 20 24 63 70	=MEM A A DQ<6>	22	=MEM B B DQ<6>	7 70	
	7	=MEM A A<11>	20 24 70	=MEM A A DQ<7>	22	=MEM B B DQ<7>	7 70	
	7	=MEM A A<15>	20 24 70	=MEM A A DQ<8>	22	=MEM B B DQ<8>	7 70	
C	7	=MEM A A<14>	20 24 70	20	=MEM A A DQ<9>	22	=MEM B B DQ<9>	7 70
	7	=MEM A A<13>	21 24 70	20	=MEM A A DQ<10>	22	=MEM B B DQ<10>	7 70
	7	=MEM A CAS L	21 24 70	20	=MEM A A DQ<11>	22	=MEM B B DQ<11>	7 70
	7	=MEM A WE L	21 24 70	20	=MEM A A DQ<12>	22	=MEM B B DQ<12>	7 70
	7	=MEM A RAS L	21 24 70	20	=MEM A A DQ<13>	22	=MEM B B DQ<13>	7 70
	7	=MEM A BA<0>	21 24 70	20	=MEM A A DQ<14>	22	=MEM B B DQ<14>	7 70
	7	=MEM A A<2>	21 24 70	20	=MEM A A DQ<15>	22	=MEM B B DQ<15>	7 70
	70 63 24 21 7	=MEM A CAB<6>	7 21 24 63 70	20	=MEM A A DQ<16>	22	=MEM B B DQ<16>	7 70
	7	=MEM A A<10>	21 24 70	20	=MEM A A DQ<17>	22	=MEM B B DQ<17>	7 70
	7	=MEM A A<1>	21 24 70	20	=MEM A A DQ<18>	22	=MEM B B DQ<18>	7 70
B	7	=MEM A A<0>	21 24 70	20	=MEM A A DQ<19>	22	=MEM B B DQ<19>	7 70
	70 63 24 21 20 7	=MEM A ODT<0>	7 20 21 24 63 70	20	=MEM A A DQ<20>	22	=MEM B B DQ<20>	7 70
	63 7	TP LPDDR3 RSVD1	7 63	20	=MEM A A DQ<21>	22	=MEM B B DQ<21>	7 70
	63 7	TP LPDDR3 RSVD2	7 63	20	=MEM A A DQ<22>	22	=MEM B B DQ<22>	7 70
	7	=MEM B B A<5>	22 24 70	20	=MEM A A DQ<23>	22	=MEM B B DQ<23>	7 70
	7	=MEM B B A<9>	22 24 70	20	=MEM A A DQ<24>	22	=MEM B B DQ<24>	7 70
	7	=MEM B B A<6>	22 24 70	20	=MEM A A DQ<25>	22	=MEM B B DQ<25>	7 70
	7	=MEM B B A<8>	22 24 70	20	=MEM A A DQ<26>	22	=MEM B B DQ<26>	7 70
	7	=MEM B B A<7>	22 24 70	20	=MEM A A DQ<27>	22	=MEM B B DQ<27>	7 70
	7	=MEM B BA<2>	22 24 70	20	=MEM A A DQ<28>	22	=MEM B B DQ<28>	7 70
A	70 63 24 22 7	=MEM B CAA<6>	7 22 24 63 70	20	=MEM A A DQ<29>	22	=MEM B B DQ<29>	7 70
	7	=MEM B A<11>	22 24 70	20	=MEM A A DQ<30>	22	=MEM B B DQ<30>	7 70
	7	=MEM B A<15>	22 24 70	20	=MEM A A DQ<31>	22	=MEM B B DQ<31>	7 70
	7	=MEM B A<14>	22 24 70	21	=MEM A A DQ<32>	22	=MEM B B DQ<32>	7 70
	7	=MEM B A<13>	23 24 70	21	=MEM A A DQ<33>	22	=MEM B B DQ<33>	7 70
	7	=MEM B CAS L	23 24 70	21	=MEM A A DQ<34>	22	=MEM B B DQ<34>	7 70
	7	=MEM B WE L	23 24 70	21	=MEM A A DQ<35>	22	=MEM B B DQ<35>	7 70
	7	=MEM B RAS L	23 24 70	21	=MEM A A DQ<36>	22	=MEM B B DQ<36>	7 70
	7	=MEM B BA<0>	23 24 70	21	=MEM A A DQ<37>	22	=MEM B B DQ<37>	7 70
	7	=MEM B A<2>	23 24 70	21	=MEM A A DQ<38>	22	=MEM B B DQ<38>	7 70
Signal Aliases								
Apple Inc.								
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Functional Test Points

NO_TEST Nets

J3501: AirPort / BT Connector

J6000: Fan Connector

Misc Voltages & Control Signals

FUNC_TEST		(Need 6 TPs)	
TRUE	PP3V3 WLAN	29	37 38 39 41
TRUE	WIFI EVENT L	29	37 38
TRUE	PCIE AP R2D N	29	69
TRUE	PCIE AP R2D P	29	69
TRUE	PCIE CLK100M AP N	12	29 69
TRUE	PCIE CLK100M AP P	12	29 69
TRUE	PCIE AP D2R P	14	29 69
TRUE	PCIE AP D2R N	14	29 69
TRUE	PCIE WAKE L	13	29 31
TRUE	AP RESET CONN L	29	
TRUE	AP CLKREQ Q L	29	
TRUE	USB BT CONN P	29	68
TRUE	USB BT CONN N	29	68
TRUE	PP3V3 S4	25	26 27 28 33 36 38
(Need to add 8 GND TPs)			

J3700: SSD Connector

FUNC_TEST		(Need 5 TPs)	
TRUE	PP3V3 S0SW SSD FLT	30	
TRUE	PCIE SSD R2D N<3..0>	30	67
TRUE	PCIE SSD R2D P<3..0>	30	67
TRUE	PP3V3 S0	62	63 64 44 45 56 59 61
TRUE	SSD RESET CONN L	8	11 12 36 38 39 40 41
TRUE	SSD CLKREQ CONN L	62	64 65 74 30
TRUE	SMC OOB1 R2D CONN L	30	
TRUE	SMC OOB1 D2R CONN L	30	
TRUE	SSD PCIE SEL L	30	
TRUE	SSD SR EN L	15	30
TRUE	SMC PWRFAIL WARN L	30	37
TRUE	SSD PWR EN	15	30 58 59
TRUE	PCIE SSD D2R N<3..0>	12	30 67
TRUE	PCIE SSD D2R P<3..0>	12	30 67
TRUE	PCIE CLK100M SSD N	12	30 67
TRUE	PCIE CLK100M SSD P	12	30 67
(Need to add 6 GND TPs)			

J4002: Camera Connector

FUNC_TEST			
TRUE	MIPI CLK CONN N	32	72
TRUE	MIPI CLK CONN P	32	72
TRUE	CAM SENSOR WAKE L CONN	32	
TRUE	MIPI DATA CONN N	32	72
TRUE	MIPI DATA CONN P	32	72
TRUE	SMBUS SMC 1 S0 SDA	14	32 37 40 43 44 69
TRUE	SMBUS SMC 1 S0 SCL	73	32 37 40 43 44 69
TRUE	I2C CAM SCK	31	32
TRUE	I2C CAM SDA	31	32
TRUE	PP5V S3RS0 ALSCAM_F	32	
(Need to add 280 GND TPs)			

J6100: LPC+SPI Connector

FUNC_TEST			
TRUE	SPI ALT IO2 WP L	46	
TRUE	SPI ALT IO3 HOLD L	46	
TRUE	LPC AD<3..0>	14	37 69
TRUE	SPI ALT IO0 MOSI	46	
TRUE	XDP LPCPLUS GPIO	15	16
TRUE	LPCPLUS RESET L	59	
TRUE	SMC TDO	37	38
TRUE	TP SMC TRST L	37	38
TRUE	TP SMC MD1	37	38
TRUE	SMC TX L	37	38
TRUE	SPI ALT IO1 MISO	46	
TRUE	LPC FRAME L	14	37 69
TRUE	SPIROM USE MLB	15	46
TRUE	PM CLKRUN L	13	37
TRUE	SPI ALT CLK	46	
TRUE	SPI ALT CS L	46	
TRUE	LPC SERIRQ	15	37
TRUE	LPC PWRDWN L	13	37
TRUE	SMC TDI	37	38
TRUE	SMC TCK	37	38 46
TRUE	SMC RESET L	37	38 46 50
TRUE	SMC ROMBOOT	37	38
TRUE	SMC RX L	37	38
TRUE	SMC TMS	37	38 46
(Need to add 6 GND TPs)			

J4800: IPD Flex Connector

FUNC_TEST			
TRUE	SMC L1D	36	37 38 61 65
TRUE	TPAD SPI MISO R	36	
TRUE	USB TPAD P	14	36 68
TRUE	USB TPAD N	14	36 68
TRUE	TPAD SPI CLK R	36	
TRUE	TPAD WAKE L	36	
TRUE	TPAD SPI MOSI R	36	
TRUE	PP3V3 S4 IPD	36	
TRUE	TPAD SPI CS R L	36	
TRUE	TPAD SPI IP EN CONN	36	
TRUE	TPAD SPI INT S4 WAKE L CONN	36	
TRUE	PP5V S4 IPD	36	
TRUE	TPAD USB IP EN CONN	36	
TRUE	SMBUS SMC 3 SDA	36	37 40 44 73
TRUE	SMBUS SMC 3 SCL	36	37 40 44 73
TRUE	SMC LSOC RST L	36	38
TRUE	PP3V42 G3H	17	30 35 36 37 38 40 46 49 50
TRUE	SMC ONOFF L	36	37 38
(Need to add 5 GND TPs)			

J7000: DC-In Connector

FUNC_TEST		(Need 4 TPs)	
TRUE	PPDCIN G3H	49	50 62 64
TRUE	PP5V S4RS3	32	35 47 49 54 55 58 62
(Need to add 5 GND TPs)			

J6404: Speaker Connector

FUNC_TEST			
TRUE	SPKRAMP ROUT P	47	74
TRUE	SPKRAMP ROUT N	47	74
(Need to add 3 GND TPs)			

J6950: Battery Connector

FUNC_TEST		(Need 4 TPs)	
TRUE	PPVBAT G3H CONN	48	50
TRUE	SMBUS SMC 5 G3 SCL	37	40 48 50 73
TRUE	SMBUS SMC 5 G3 SDA	37	40 48 50 73
TRUE	SYS DETECT L	48	
(Need to add 4 GND TPs near J7050 and 1 for shield)			

J8300: Internal DP Connector

FUNC_TEST		(Need 2 TPs)	
TRUE	PPHV S0SW LCDCLKLT	56	69 62
TRUE	LED RETURN 6	56	60
TRUE	LED RETURN 5	56	60
TRUE	LED RETURN 4	56	60
TRUE	LED RETURN 3	56	60
TRUE	LED RETURN 2	56	60
TRUE	LED RETURN 1	56	60
TRUE	DP INT HPD CONN	60	
TRUE	I2C TCON SDA R	60	
TRUE	I2C TCON SCL R	60	
TRUE	PP3V3 S0SW LCD UF	60	
TRUE	DP INT AUX CH C N	60	67
TRUE	DP INT AUX CH C P	60	67
TRUE	DP INT ML P<0>	60	67
TRUE	DP INT ML N<0>	60	67
(Need to add 5 GND TPs)			

J7715: KB CLKLT Connector

FUNC_TEST			
TRUE	KBLED ANODE	56	
TRUE	KBLED FB	56	
(Need to add 2 GND TPs)			

J1800: XDP Connector

FUNC_TEST		(Only a subset are needed for PCT HW test fixture)	
TRUE	XDP CPU TCK	6	16 67
TRUE	XDP PCH TCK	12	16 69
TRUE	XDP CPU TDI	6	16 67
TRUE	XDP CPU TDO	6	16 67
TRUE	XDP CPUPECH TRST L	6	12 16 67
TRUE	XDP CPU TMS	6	16 67
TRUE	XDP PCH TMS	12	16 69
TRUE	XDP PCH TDI	12	16 69
TRUE	XDP PCH TDO	12	16 69
TRUE	XDP CPU FREQ L	6	16 67
TRUE	XDP CPU PRDY L	6	16 67
TRUE	XDP CPU VCCST PWRGD	16	
TRUE	PM RSMRST L	13	59
TRUE	XDP SYS PWROK	16	
TRUE	PM SYSRST L	13	37 37
TRUE	CPU CFG<3>	6	16 67
TRUE	PP1V05 S0	6	8 11 15 16 17 38 42 51 55 58
(Need to add 2 GND TPs)			

GND

TRUE	PCH BT UART D2R	15
TRUE	PCH BT UART R2D	15
TRUE	PCH BT UART RTS L	15
TRUE	PCH BT UART CTS L	15
TRUE	AUD SPI CS L	15
TRUE	AUD SPI CLK	15
TRUE	AUD SPI MISO	15
TRUE	AUD SPI MOSI	15
TRUE	HDMI BTMUX LATCH	13
TRUE	HDD PWR EN	15
TRUE	WOL EN	14
TRUE	BT PWRST L	15
TRUE	HDMI BTMUX FLAG	13
TRUE	FW PWR EN	15
TRUE	FW PME L	15
TRUE	ENET MEDIA SENSE	15
TRUE	LCD PSR EN	15
TRUE	LCD IRQ L	15
TRUE	ODD PWR EN L	13
TRUE	ENET LOW PWR	13
TRUE	AUD IP PERIPHERAL DET	13
TRUE	AUD I2C INT L	13
TRUE	AP PCIE DEV WAKE	13

Unused nets with offpage

(Nets with offpages not used on this project)

SYNC MASTER=WILL J43		SYNC DATE=12/17/2012			
PAGE TITLE					
Func Test / No Test					
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J41/J43 Board-Specific Spacing & Physical Constraints							
BOARD LAYERS			BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION	
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA, MEM_TERM		MM	16.2	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP, BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2, ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3, ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4, ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
Single-ended Physical Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2, ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3, ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4, ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2, ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3, ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4, ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2, ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3, ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4, ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2, ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3, ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4, ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
Differential Pair Physical Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL3, ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110MM		0.095 MM	0.095 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP, BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3, ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3, ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL4, ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
Spacing Constraints							
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
1:1_SPACING	*	0.100 MM	?				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
1x_DIELECTRIC	TOP, BOTTOM	0.071 MM	?				
1x_DIELECTRIC	ISL3, ISL10	0.053 MM	?				
1x_DIELECTRIC	ISL4, ISL9	0.050 MM	?				
1x_DIELECTRIC	*	0.090 MM	?				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
DEFAULT	*	0.1 MM	?				
STANDARD	*	=DEFAULT	?				
BGA_P075MM	*	0.075 MM	?				
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET				
*	*	BGA	BGA_P075MM				
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET					
*	BGA	P070MM_BGA					
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL2, ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL3, ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP, BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL3, ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL4, ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD
PCB Rule Definitions							
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SHAPE
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_spacing_type1	NET_spacing_type2	AREA_type	SPACING_rule_Self
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SELF
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP, BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP, BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SELF
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SH
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX20OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX20OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_20OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_20OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	"	=2.5x_DIELECTRIC	?
PCIE_RX2RX	"	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	"	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	"	=4x_DIELECTRIC	?
PCIE_TX2RX	"	=6x_DIELECTRIC	?
PCIE_RX2TX	"	=6x_DIELECTRIC	?
PCIE_20OTHERHS	"	=4x_DIELECTRIC	?
PCIE_20THER	"	=3x_DIELECTRIC	?


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SHORT
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2ZOTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_ZOTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_ZOTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_ZOTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_ZOTHERHS
PCIE_PCH_TX	*	*	PCIE_ZOTHER
PCIE_PCH_RX	*	*	PCIE_ZOTHER

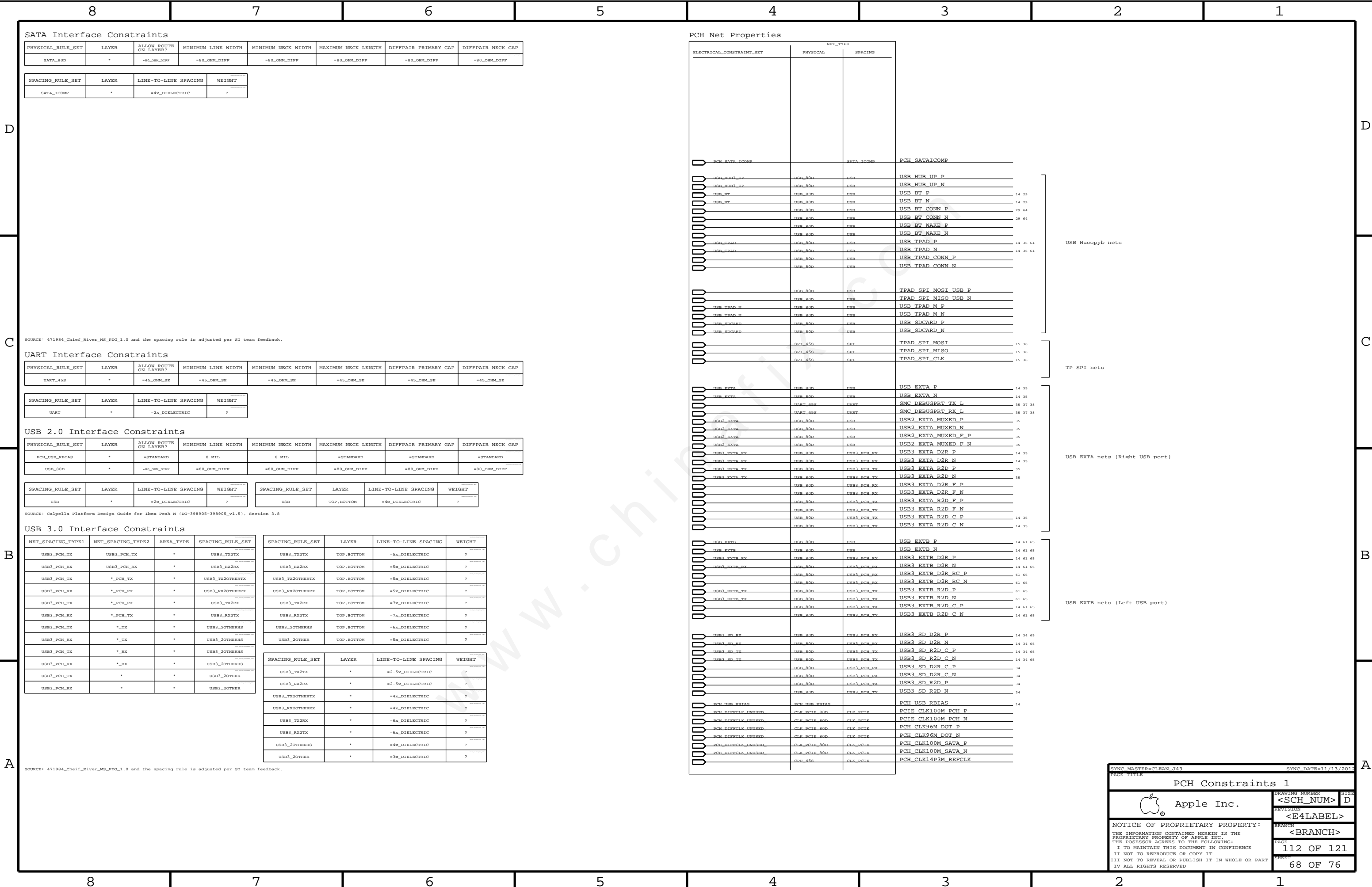
PCIE_RX20THERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_20THERHS	*	=4x_DIELECTRIC	?
PCIE_20THER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 38
	PM_SYNC	CPU_45S	CPU_AGTI	PM_SYNC	
	PM_MEM_PWRGD	CPU_45S	CPU_AGTI	PM_MEM_PWRGD	
		CPU_45S	CPU_ITP	XDP_DBRESET_L	16 17
		CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 16 64
		CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 16 64
		CPU_27BAS	CPU_COMP	EDP_COMP	
		CPU_27BAS	CPU_COMP	CPU_PEG_COMP	
	CPU_SM_RCOMP	CPU_27BAS	CPU_COMP	CPU_SM_RCOMP<0>	6
	CPU_SM_RCOMP	CPU_27BAS	CPU_COMP	CPU_SM_RCOMP<1>	6
	CPU_SM_RCOMP	CPU_27BAS	CPU_COMP	CPU_SM_RCOMP<2>	6
		CPU_45S	CPU_ITP	CPU_CFG<11..0>	6 16 64
	CPU_CATERE_L	CPU_45S	CPU_AGTI	CPU_CATERE_L	6 37
		CPU_45S	CPU_AGTI	CPU_VCCIO_SEL	
	CPU_PROCHOT_1	CPU_45S	CPU_AGTI	CPU_PROCHOT_L	6 37 38 51
	CPU_PWRGD	CPU_45S	CPU_AGTI	CPU_PWRGD	6
	PM_THERMTRIP_1	CPU_45S	CPU_AGTI	PM_THERMTRIP_L	15 38
	DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
	DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
	DEPLL_REF_CLK10M	CLK_PCIE_80D	CLK_PCIE	DEPLL_REF_CLKP	
	DEPLL_REF_CLK10M	CLK_PCIE_80D	CLK_PCIE	DEPLL_REF_CLKN	
	ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
	ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
	ITPXPDP_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXPDP_CLK100M_P	
	ITPXPDP_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXPDP_CLK100M_N	
	ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
	ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
	XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 16 64
	XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 16 64
	XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 16 64
	XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 16 64
	XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUCH_TRST_L	6 12 16 64
	XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<1..0>	6 16
		CPU_45S	CPU_ITP	XDP_BPM_L<7..2>	6 16
		CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	
		CPU_45S	CPU_ITP	CPU_CFG<15..12>	6 16
	CPURST_CUSET_L	CPU_45S	CPU_ITP	XDP_CPURST_L	16
	CPU_VCCSENSE	SENSE_170V_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 51
	CPU_VCCSENSE	SENSE_170V_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 51
	CPU_VCCIOSENSE	SENSE_170V_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
	CPU_VCCIOSENSE	SENSE_170V_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
	CPU_AXG_SENSE	SENSE_170V_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
	CPU_AXG_SENSE	SENSE_170V_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
	CPU_VDDSENSE	CPU_27BAS	CPU_VCCSENSE	CPU_VDDO_SENSE_P	
	CPU_VDDSENSE	CPU_27BAS	CPU_VCCSENSE	CPU_VDDO_SENSE_N	
	CPU_VALSENSE	CPU_27BAS	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
	CPU_VALSENSE	CPU_27BAS	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
	CPU_VALSENSE	CPU_27BAS	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
	CPU_VALSENSE	CPU_27BAS	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
	CPU_VIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 51
	CPU_VIDSCKIN	CPU_45S	CPU_COMP	CPU_VIDSCKIN	8 51
	CPU_VIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 51
	PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
	PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
		PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 64
		PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 64
		PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	
		PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	
	PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 64
	PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 64
	PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 64
	PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 64
1001	DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNKO_ML_P<3..0>	25
1001	DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNKO_ML_N<3..0>	25
1001	DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNKO_ML_C_P<3..0>	5 25
1001	DP_TBT_ML	DP_80D	DP_TX	DP	

DP

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CPU Constraints			
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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_M8_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ihex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_20THERHS
USB3_PCH_RX	*_TX	*	USB3_20THERHS
USB3_PCH_TX	*_RX	*	USB3_20THERHS
USB3_PCH_RX	*_RX	*	USB3_20THERHS
USB3_PCH_TX	*	*	USB3_20THER
USB3_PCH_RX	*	*	USB3_20THER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_20THERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_20THER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_20THERHS	*	=4x_DIELECTRIC	?
USB3_20THER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_M8_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
PCH_SATA_ICOMP	SATA_ICOMP	PCH_SATAICOMP
USB_HUB1_UP	USB_80D	USB_HUB1_UP_P
USB_HUB1_UP	USB_80D	USB_HUB1_UP_N
USB_BT	USB_80D	USB_BT_P
USB_BT	USB_80D	USB_BT_N
USB_80D	USB_80D	USB_BT_CONN_P
USB_80D	USB_80D	USB_BT_CONN_N
USB_80D	USB_80D	USB_BT_WAKE_P
USB_80D	USB_80D	USB_BT_WAKE_N
USB_TPAD	USB_80D	USB_TPAD_P
USB_TPAD	USB_80D	USB_TPAD_N
USB_TPAD	USB_80D	USB_TPAD_CONN_P
USB_80D	USB_80D	USB_TPAD_CONN_N
USB_80D	USB_80D	TPAD_SPI_MOSI_USB_P
USB_80D	USB_80D	TPAD_SPI_MISO_USB_N
USB_TPAD_M	USB_80D	USB_TPAD_M_P
USB_TPAD_M	USB_80D	USB_TPAD_M_N
USB_SDCARD	USB_80D	USB_SDCARD_P
USB_SDCARD	USB_80D	USB_SDCARD_N
SET_45S	SET	TPAD_SPI_MOSI
SET_45S	SET	TPAD_SPI_MISO
SET_45S	SET	TPAD_SPI_CLK
USB_EXT	USB_80D	USB_EXT_P
USB_EXT	USB_80D	USB_EXT_N
USB_45S	USB_45S	SMC_DEBUGPRT_TX_L
USB_45S	USB_45S	SMC_DEBUGPRT_RX_L
USB2_EXT	USB_80D	USB2_EXT_MUXED_P
USB2_EXT	USB_80D	USB2_EXT_MUXED_N
USB2_EXT	USB_80D	USB2_EXT_MUXED_F_P
USB2_EXT	USB_80D	USB2_EXT_MUXED_F_N
USB3_EXT	USB_80D	USB3_EXT_D2R_P
USB3_EXT	USB_80D	USB3_EXT_D2R_N
USB3_EXT	USB_80D	USB3_EXT_R2D_P
USB3_EXT	USB_80D	USB3_EXT_R2D_N
USB3_EXT	USB_80D	USB3_EXT_D2R_F_P
USB3_EXT	USB_80D	USB3_EXT_D2R_F_N
USB3_EXT	USB_80D	USB3_EXT_R2D_F_P
USB3_EXT	USB_80D	USB3_EXT_R2D_F_N
USB3_EXT	USB_80D	USB3_EXT_R2D_C_P
USB3_EXT	USB_80D	USB3_EXT_R2D_C_N
USB_EXTB	USB_80D	USB_EXTB_P
USB_EXTB	USB_80D	USB_EXTB_N
USB3_EXTB	USB_80D	USB3_EXTB_D2R_P
USB3_EXTB	USB_80D	USB3_EXTB_D2R_N
USB3_EXTB	USB_80D	USB3_EXTB_D2R_RC_P
USB3_EXTB	USB_80D	USB3_EXTB_D2R_RC_N
USB3_EXTB	USB_80D	USB3_EXTB_R2D_P
USB3_EXTB	USB_80D	USB3_EXTB_R2D_N
USB3_EXTB	USB_80D	USB3_EXTB_R2D_C_P
USB3_EXTB	USB_80D	USB3_EXTB_R2D_C_N
USB3_SD	USB_80D	USB3_SD_D2R_P
USB3_SD	USB_80D	USB3_SD_D2R_N
USB3_SD	USB_80D	USB3_SD_R2D_C_P
USB3_SD	USB_80D	USB3_SD_R2D_C_N
USB3_SD	USB_80D	USB3_SD_D2R_C_P
USB3_SD	USB_80D	USB3_SD_D2R_C_N
USB3_SD	USB_80D	USB3_SD_R2D_P
USB3_SD	USB_80D	USB3_SD_R2D_N
PCH_USB_RBIAS	PCH_USB_RBIAS	PCH_USB_RBIAS
CLK_PCIE100M	CLK_PCIE100M	CLK_PCIE100M_PCH_P
CLK_PCIE100M	CLK_PCIE100M	CLK_PCIE100M_PCH_N
CLK_PCIE96M	CLK_PCIE96M	CLK_PCIE96M_DOT_P
CLK_PCIE96M	CLK_PCIE96M	CLK_PCIE96M_DOT_N
CLK_PCIE100M	CLK_PCIE100M	CLK_PCIE100M_SATA_P
CLK_PCIE100M	CLK_PCIE100M	CLK_PCIE100M_SATA_N
CLK_PCIE14P3M	CLK_PCIE14P3M	CLK_PCIE14P3M_REFCLK

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP_BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	= 2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.16

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SP1_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF	=0_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
















SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	LPC_AD	LPC_45S	LPC	LPC_AD<3..0>
	LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L
		LPC_45S	LPC	LPCPLUS_RESET_L
	LPC_CLK32M	CLK LPC_45S	CLK LPC	LPC_CLK24M_SMC
		CLK LPC_45S	CLK LPC	LPC_CLK24M_SMC_R
	LPC_CLK32M	CLK LPC_45S	CLK LPC	LPC_CLK24M_LPCPLUS
		CLK LPC_45S	CLK LPC	LPC_CLK24M_LPCPLUS_R
	SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK
	SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA
	SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SMB_PCH_0_CLK
	SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SMB_PCH_0_DATA
	SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL
	SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK
		HDA_45S	HDA	HDA_BIT_CLK_R
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC
		HDA_45S	HDA	HDA_SYNC_R
	HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L
		HDA_45S	HDA	HDA_RST_L
	HDA_SDIO0	HDA_45S	HDA	HDA_SDIO0
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT
		HDA_45S	HDA	HDA_SDOUT_R
	PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R
		CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K
	SPI_CLK	SPI_45S	SPI	SPI_CLK_R
		SPI_45S	SPI	SPI_CLK
	SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R
		SPI_45S	SPI	SPI_MOSI
	SPI_MISO	SPI_45S	SPI	SPI_MISO
		SPI_45S	SPI	SPI_MISO_R
	SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L
		SPI_45S	SPI	SPI_CS0_L
		SPI_45S	SPI	SPI_SMC_CLK
		SPI_45S	SPI	SPI_SMC_MOSI
		SPI_45S	SPI	SPI_SMC_MISO
		SPI_45S	SPI	SPI_SMC_CS_L
		SPI_45S	SPI	SPI_MLB_CLK
		SPI_45S	SPI	SPI_MLB_IO0_MOSI
		SPI_45S	SPI	SPI_MLB_IO1_MISO
		SPI_45S	SPI	SPI_MLB_CS_L
		SPI_45S	SPI	SPI_IO<2>
		SPI_45S	SPI	SPI_IO2_R
		SPI_45S	SPI	SPI_MLB_IO2_WP_L
		SPI_45S	SPI	SPI_IO<3>
		SPI_45S	SPI	SPI_IO3_R
		SPI_45S	SPI	SPI_MLB_IO3_HOLD_L
	PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P
	PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N
		PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P
		PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N
	PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P
	PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N
	PCIE_CLK100M_AP	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_AP_P
	PCIE_CLK100M_AP	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_AP_N
	PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>
	PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>
		PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>
		PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>
	PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>
	PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>
		PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>
		PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>
	PCIE_CLK100M_TBT	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_TBT_P
	PCIE_CLK100M_TBT	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_TBT_N
		CLK PCIE_80D	CLK PCIE	PEG_CLK100M_P
		CLK PCIE_80D	CLK PCIE	PEG_CLK100M_N
	XDP_TDI	PCH_45S	PCH_TPD	XDP_PCH_TDI
	XDP_TDO	PCH_45S	PCH_TPD	XDP_PCH_TDO
	XDP_TMS	PCH_45S	PCH_TPD	XDP_PCH_TMS
	XDP_TCK	PCH_45S	PCH_TPD	XDP_PCH_TCK
	PCIE_CAMERA	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P
	PCIE_CAMERA	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N
		PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P
		PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N
	PCIE_CAMERA	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P
	PCIE_CAMERA	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N
		PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P
		PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N
	PCIE_CLK100M_CAMERA	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_CAMERA_P
	PCIE_CLK100M_CAMERA	CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_CAMERA_N
		CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_CAMERA_C_P
		CLK PCIE_80D	CLK PCIE	PCIE_CLK100M_CAMERA_C_N

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1
	SYSCLK_CLK25M_CB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA
		CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP
		CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R
		CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP
		CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN
		CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN
	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R
	SYSCLK_CLK25M_X1	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R
		CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2
		CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R
		CLK_25M_45S	CLK_25M	SDSClk_CLK25M_X1

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MIPI_8SD	*	=45_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?	MIPI_2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?
MIPI_SCLK	*	=4X_DIELECTRIC	?	MIPI_SCLK	TOP,BOTTOM	=4X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?	MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	*	=2X_DIELECTRIC	?	S2_DATA2SELF	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2X_DIELECTRIC	?	S2_DQS2OWNDATA	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CMD	*	=2X_DIELECTRIC	?	S2_CMD2CMD	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CTRL	*	=2X_DIELECTRIC	?	S2_CMD2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CTRL2CTRL	*	=2X_DIELECTRIC	?	S2_CTRL2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_2OTHERMEM	*	=4X_DIELECTRIC	?	S2_2OTHERMEM	TOP,BOTTOM	=6X_DIELECTRIC	?
S2MEM_2PWR	*	=2X_DIELECTRIC	?	S2MEM_2PWR	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2GND	*	=2X_DIELECTRIC	?	S2MEM_2GND	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2OTHER	*	=6X_DIELECTRIC	?	S2MEM_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 31 32
S2_MEM_CTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 31 32
S2_MEM_CTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 31 32
S2_MEM_CTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 31 32
S2_MEM_DQSD	S2_MEM_85D	S2_MEM_DQSD	MEM_CAM_DQS_P<0> 31 32
S2_MEM_DQSD	S2_MEM_85D	S2_MEM_DQSD	MEM_CAM_DQS_N<0> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 32 64
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 32 64
		S2_MEM_PWB	PP1V35_CAM 31 32
		S2_MEM_PWB	PP0V675_CAM_VREF 31 32
		S2_MEM_PWB	PP0V675_MEM_CAM_VREFCA 32
		S2_MEM_PWB	PP0V675_MEM_CAM_VREFDO 32


DDAA

	8	7	6	5	4	3	2	1	
D	<div>Change List: <RDAR://COMPONENT/508934> J43 HW EE SCHEMATIC PROTO 0 <RDAR://COMPONENT/508937> J43 HW EE SCHEMATIC PROTO 1 <RDAR://COMPONENT/508941> J43 HW EE SCHEMATIC EVT <RDAR://COMPONENT/508945> J43 HW EE SCHEMATIC DVT</div> <div>Kismet: afp://kismet.apple.com/Kismet-Projects/J41-J43</div> <div>Useful Wiki Links: Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design</div> <div>MobileMac HW Radar: <rdar://component/497591> MobileMac HW Task <rdar://component/497587> MobileMac HW Schematic <rdar://component/497585> MobileMac HW New Bugs <rdar://component/497588> MobileMac HW Layout <rdar://component/497590> MobileMac HW Investigation <rdar://component/497589> MobileMac HW Architecture</div> <div>Other Info: Page Allocations - <rdar://problem/11791318> 2012 Schematic Page Allocations</div>								D
C									C
B									B
A									A
	8	7	6	5	4	3	2	1	

SYNC MASTER=J41 MLB

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