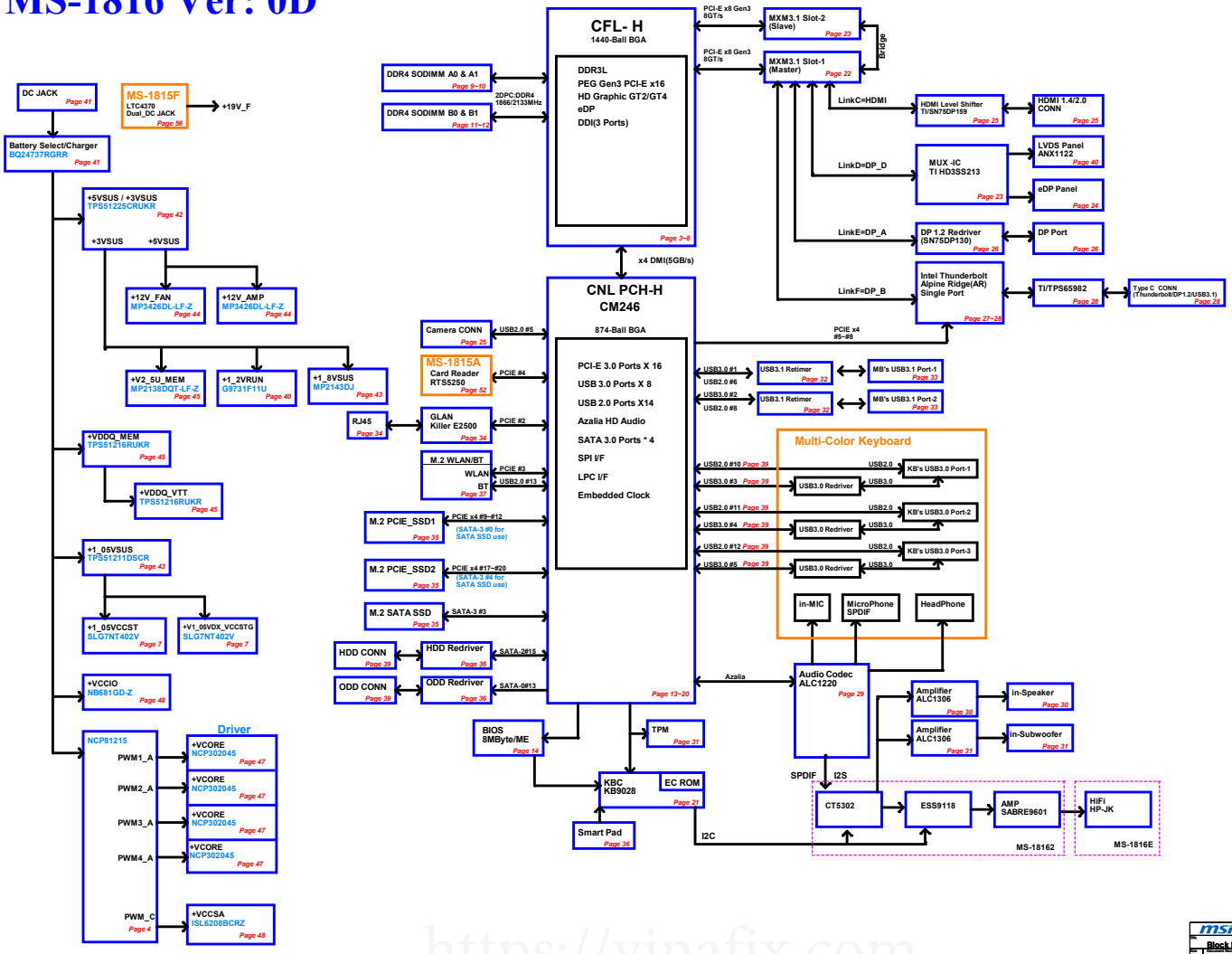
# MS-1816 Ver: 0D

## Intel Coffee Lake H Mobile






MICRO-STAR INT'L CO.,LTD.
Block Diagram
MS-1816
0D

# SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

## Voltage Rails

| Voltage | Description | Control Signal |
|---|---|---|
| PWR_SRC | 19V AC ADAPTER OR BATTERY IN | |
| +5VALW | 5.0V always on power rail | PWR_SRC |
| +3VALW | 3.3V always on power rail | PWR_SRC |
| +5VSUS | 5.0V power rail | SUS_ON |
| +3VSUS | 3.3V power rail | SUS_ON |
| +1V0SUS | 1.0V power rail | 5V3VSUSOK |
| +V2_5U_MEM | 2.5V Memory DDR4 power rail | 5V3VSUSOK |
| +VDDQ_MEM | 1.2V Memory DDR4 power rail | PM_SLP_S4# |
| +VDDQ_VTT | 0.6V DDR4 Termination voltage | VDDQ_VTT_EN |
| +5VRUN | 5V power rail (off in S3-S5) | RUND |
| +3VRUN | 3.3V power rail (off in S3-S5) | RUND |
| +1_2VRUN | 1.1V power rail (off in S3-S5) | PM_SLP_S3# |
| +1_05VRUN | 1.1V power rail (off in S3-S5) | PM_SLP_S3# |
| +12V_FAN | 12V FAN power rail for DGPU | +5VRUN |
| +12V_AMP | 12V Audio Amp APA2619 power rail | +5VSUS |
| CPU/+V1.0U_VCCST | +VCCST: 1.0V Sustain power rail<br>+VCCPLL : 1.0V PLL power rails | +1_2VDIMM_PWRGD |
| CPU/+V1.0DX_VCCSTG | 1.0V Sustain Gated power rail | VCCSTG_EN |
| CPU/+VCORE | 0.55~1.5V Core Voltage for Processor | VR_ON |
| CPU/+VCCSA | 1.05V system Agent power rail | |
| CPU/+VCCIO | 0.95V IO power rail | VCCIO_EN |
| +19V_F | 19V LTC4370 ; Dual_DC JACK | |

## POWER STATES

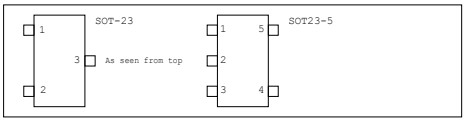
| STATE \ SIGNAL | SLP_S3# | SLP_S4# | SLP_S5# | +V*ALW | +*VSUS | +*VRUN | Clocks |
|---|---|---|---|---|---|---|---|
| S0( Full ON) | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3( Suspend to RAM) | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4( Suspend to Disk) | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | ON | OFF | OFF | OFF |

Note : WHEN AC MODE , System turn on and +V*SUS always keep high

### Net Naming Conventions

**Suffix**
```
#  =  Active Low Signal
```
**Prefix**
```
H  =  Host
M  =  DDR Memory
TP =  Test Point (does not connect anywhere else)
PB = DGPU VRAM
VIAxxx =  Like Test Point, but using VIA.
```

### PCB Footprints



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Title: Platform

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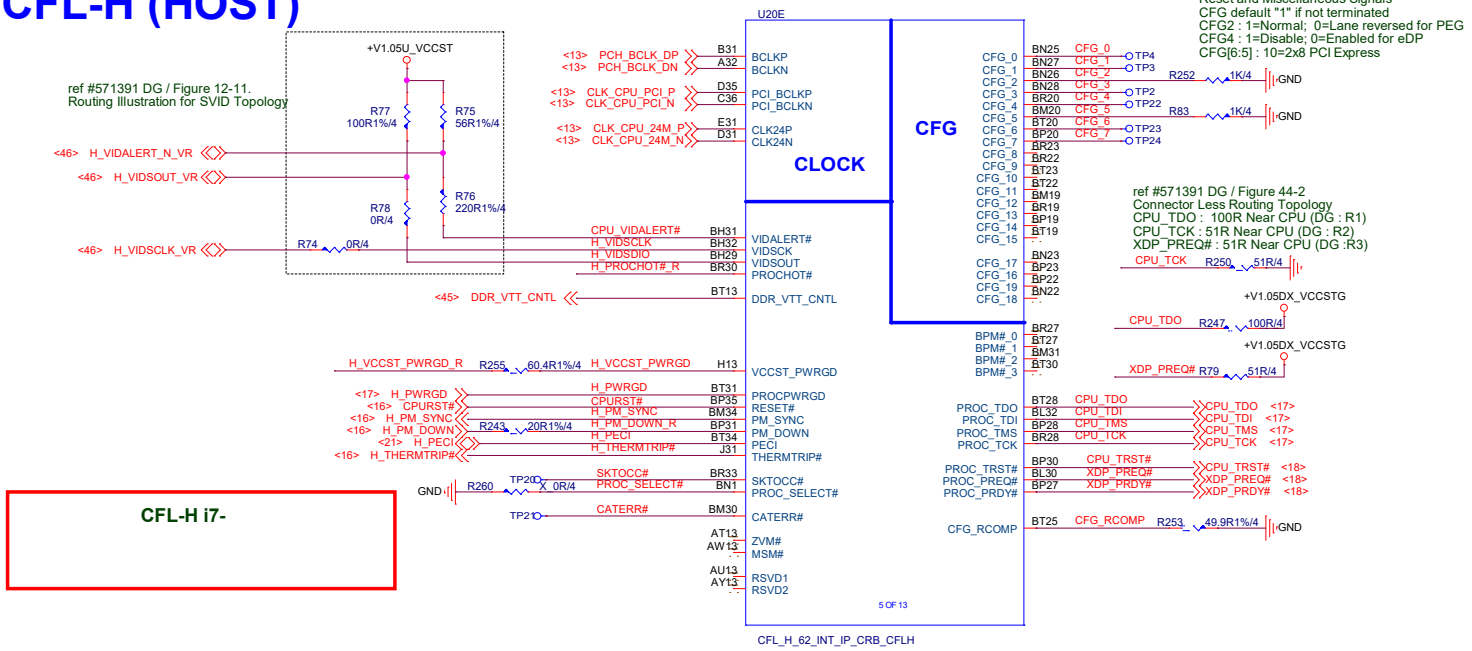
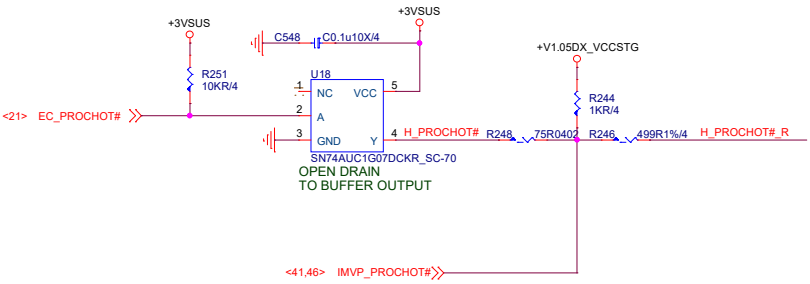
# CFL-H (HOST)

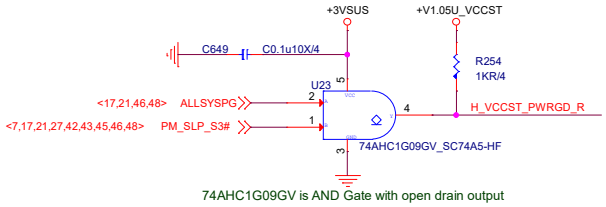



## PROCHOT#




## VCCST_PWRGD

(Level Shifter 3.3V to 1.0V)




74AHC1G09GV is AND Gate with open drain output



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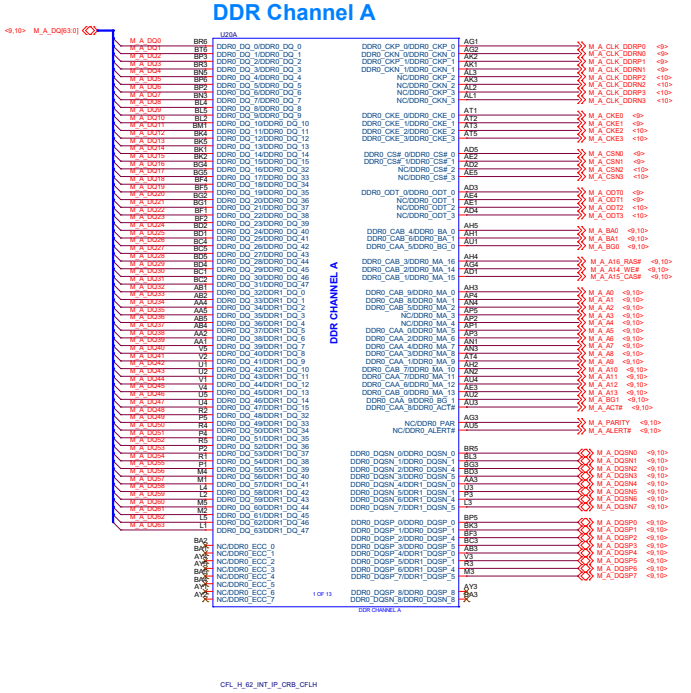
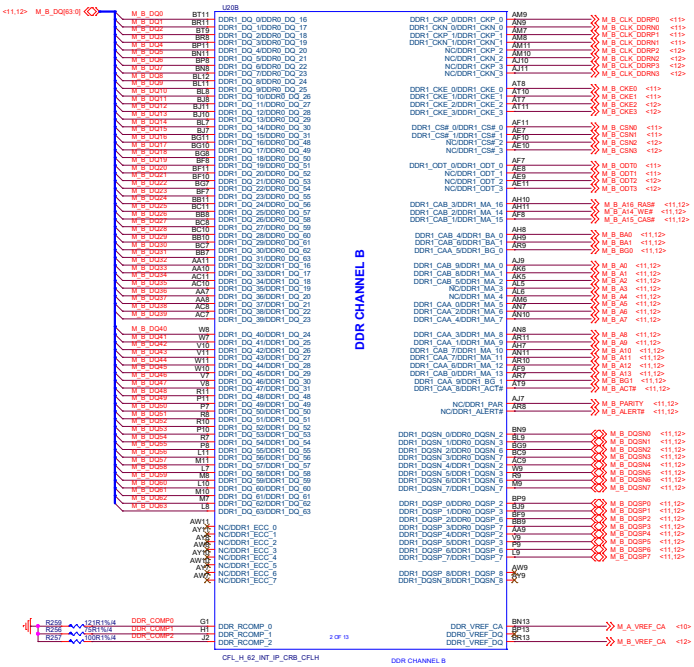
| | | |
|---|---|---|
| Title: CFL-H (HOST) | | |
| Size: Custom | Document Number: MS-18161 | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 3 of 62 | |

# CFL-H (DDR4)

## DDR Channel A




## DDR Channel B




| | |
|---|---|
| Title | CFL-H (DDR4) |
| Size / Document Number | MS-18161 |
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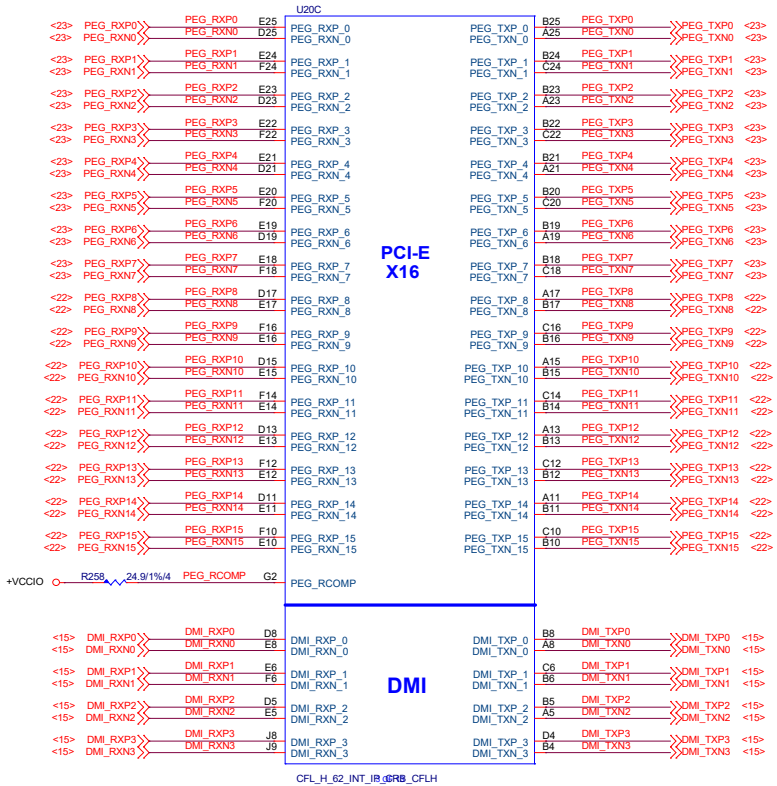
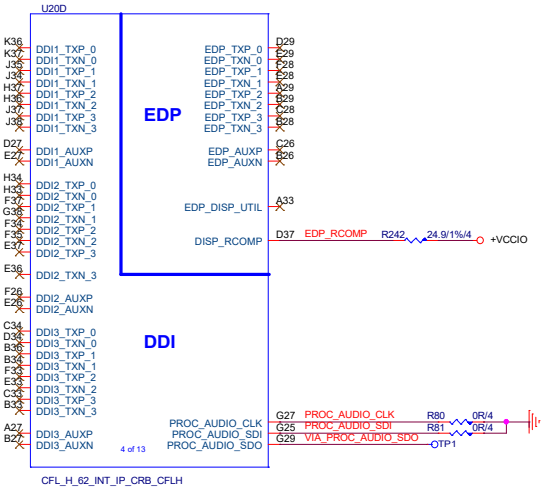
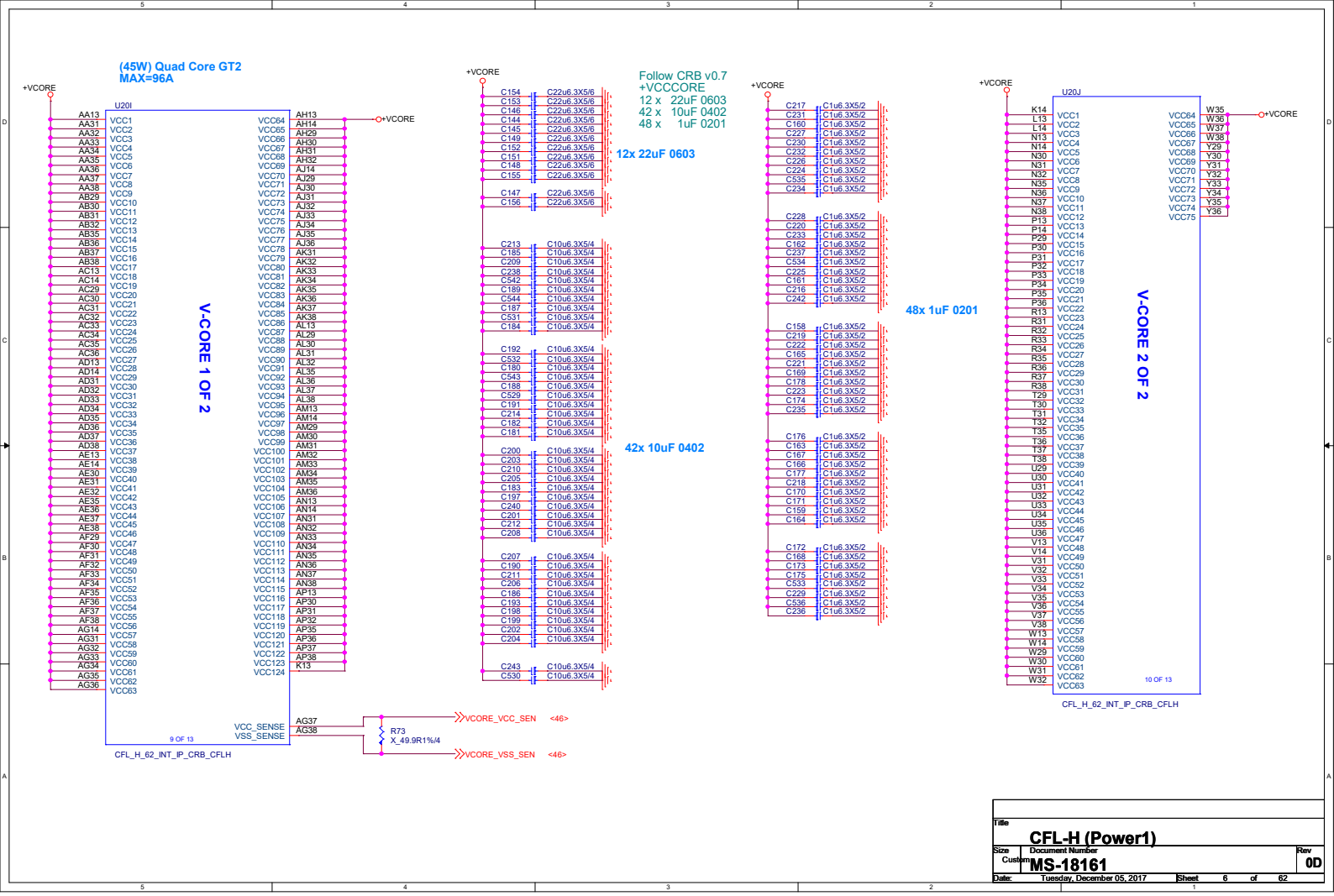
# CFL-H (DMI/Display)



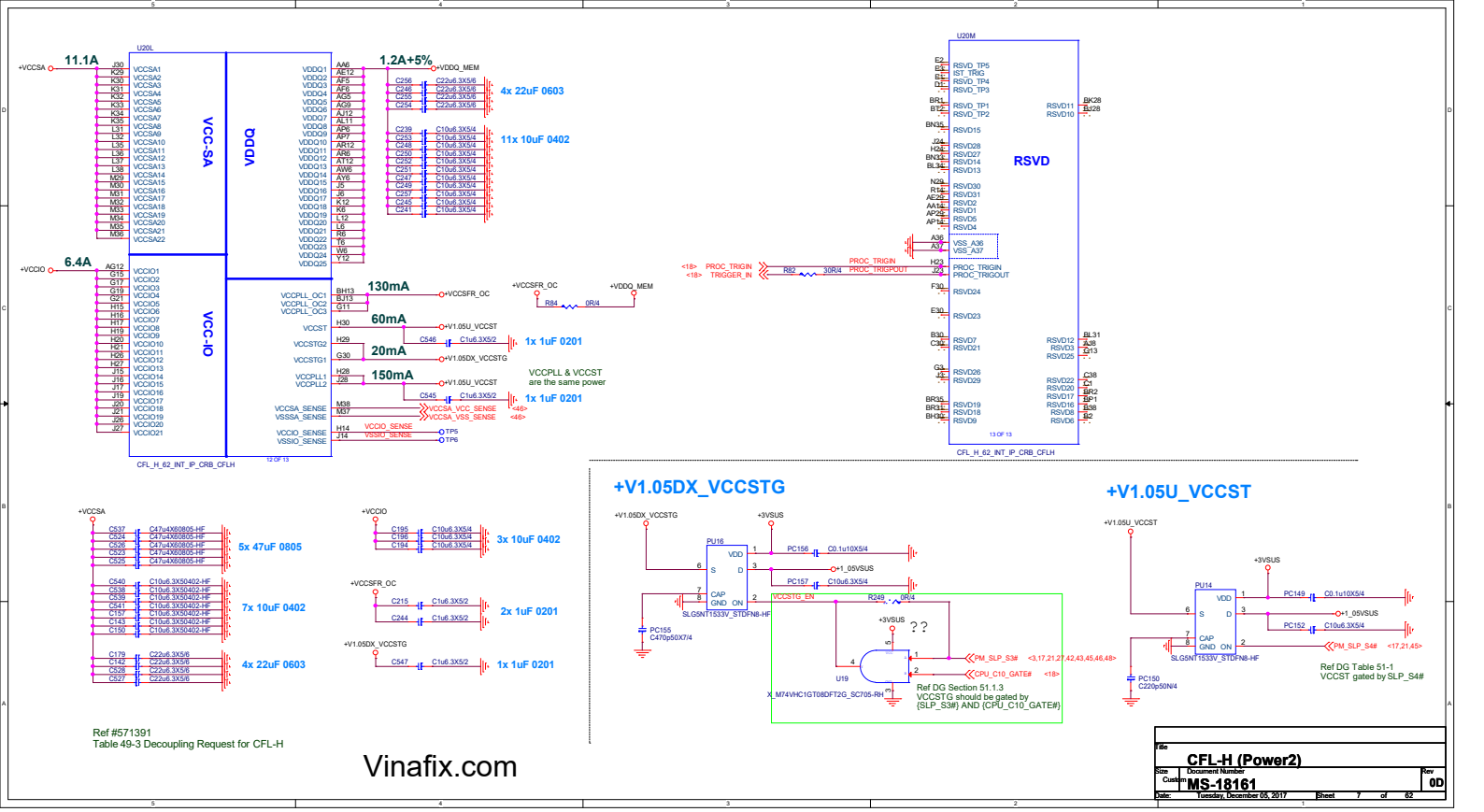



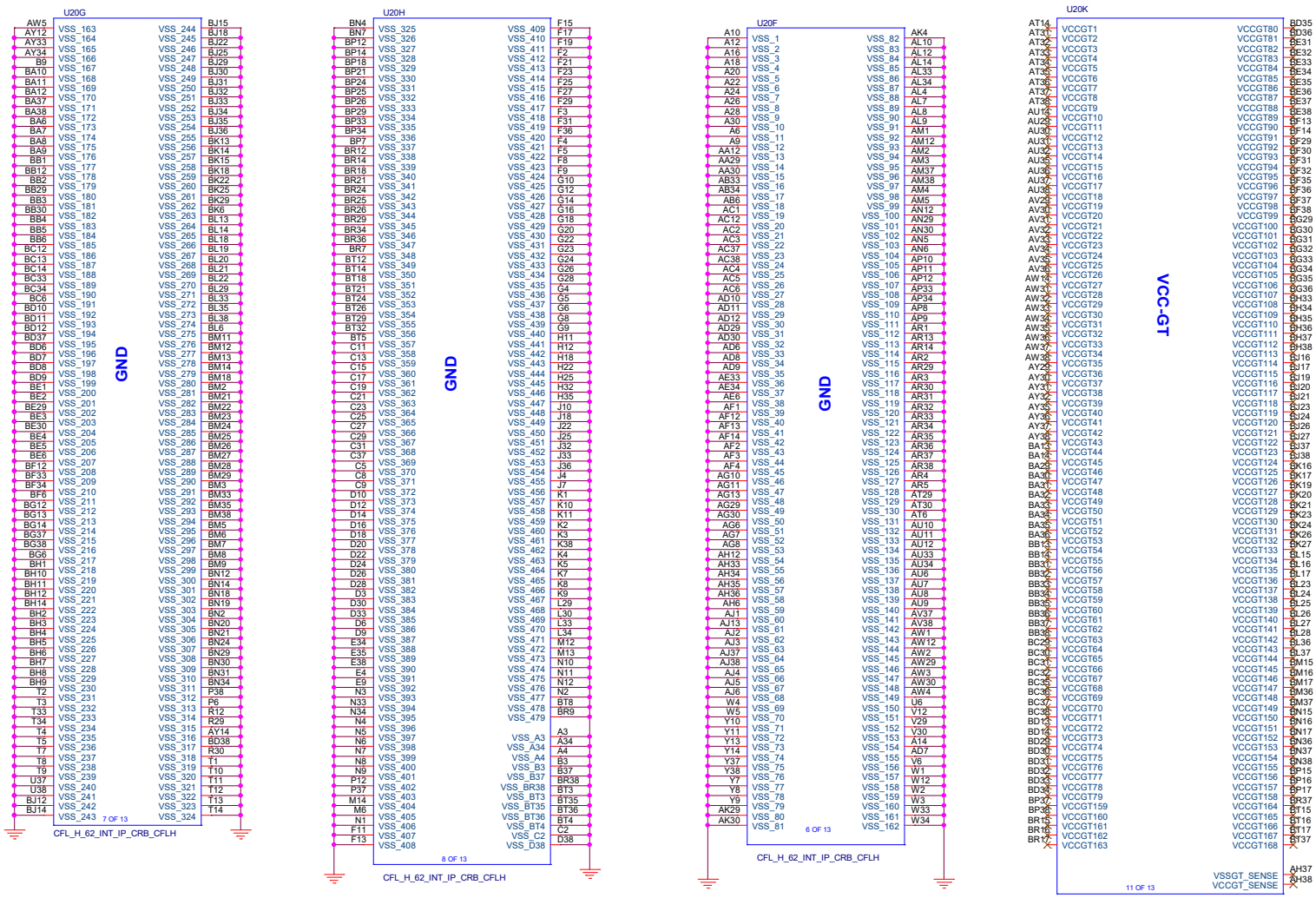

refer #571391 CFL-H DG Chapter 29.1.4
When embedded display audio is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor(~2K), PROC_AUDIO_SDO can be left unconnected.

| | | | |
|---|---|---|---|
| Title | CFL-H (DMI/Display) | | |
| Size: Custom | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 5 of 62 | | |




| | | | |
|---|---|---|---|
| Title | CFL-H (Power1) | | |
| Size: Custom | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 6 of 62 | | |

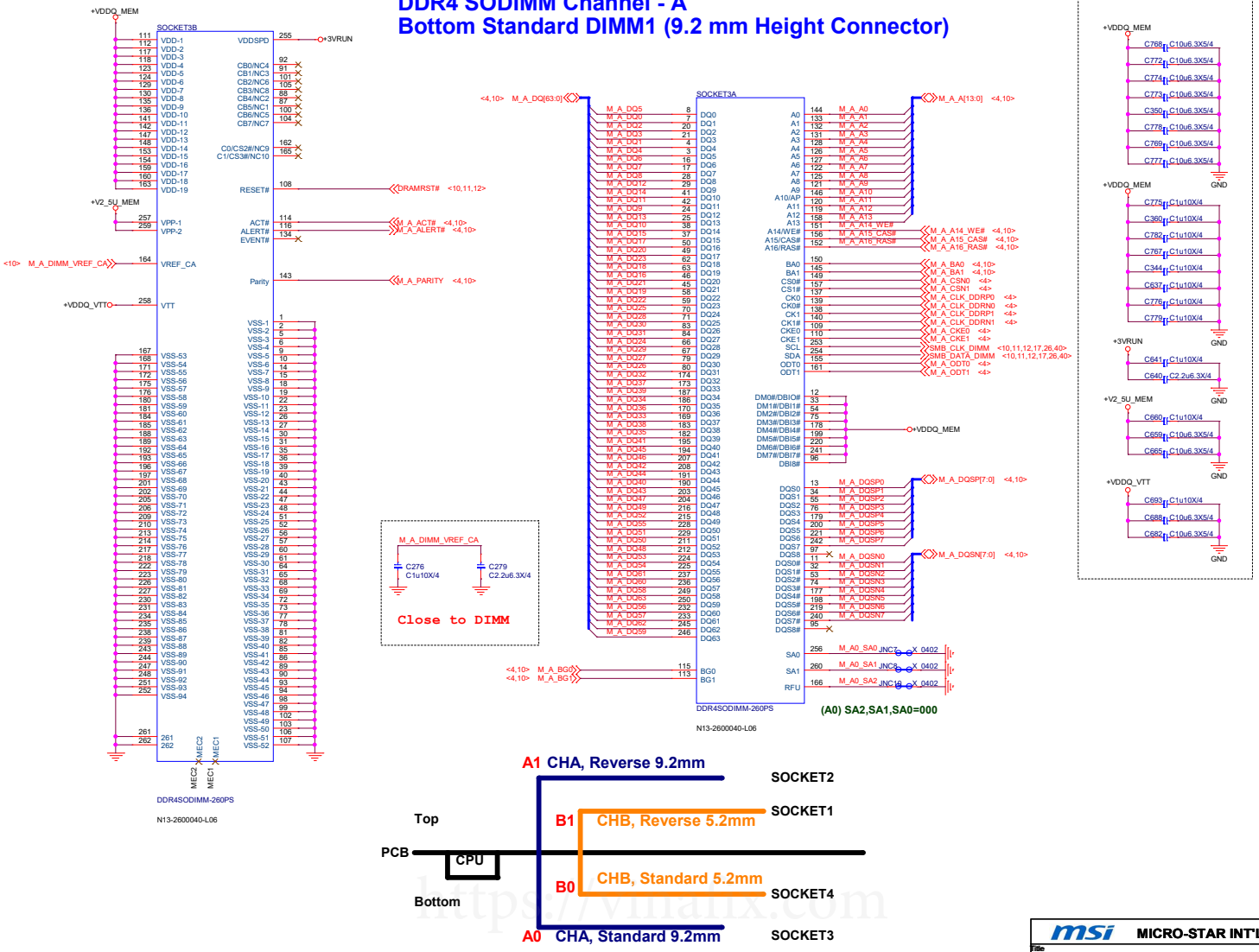






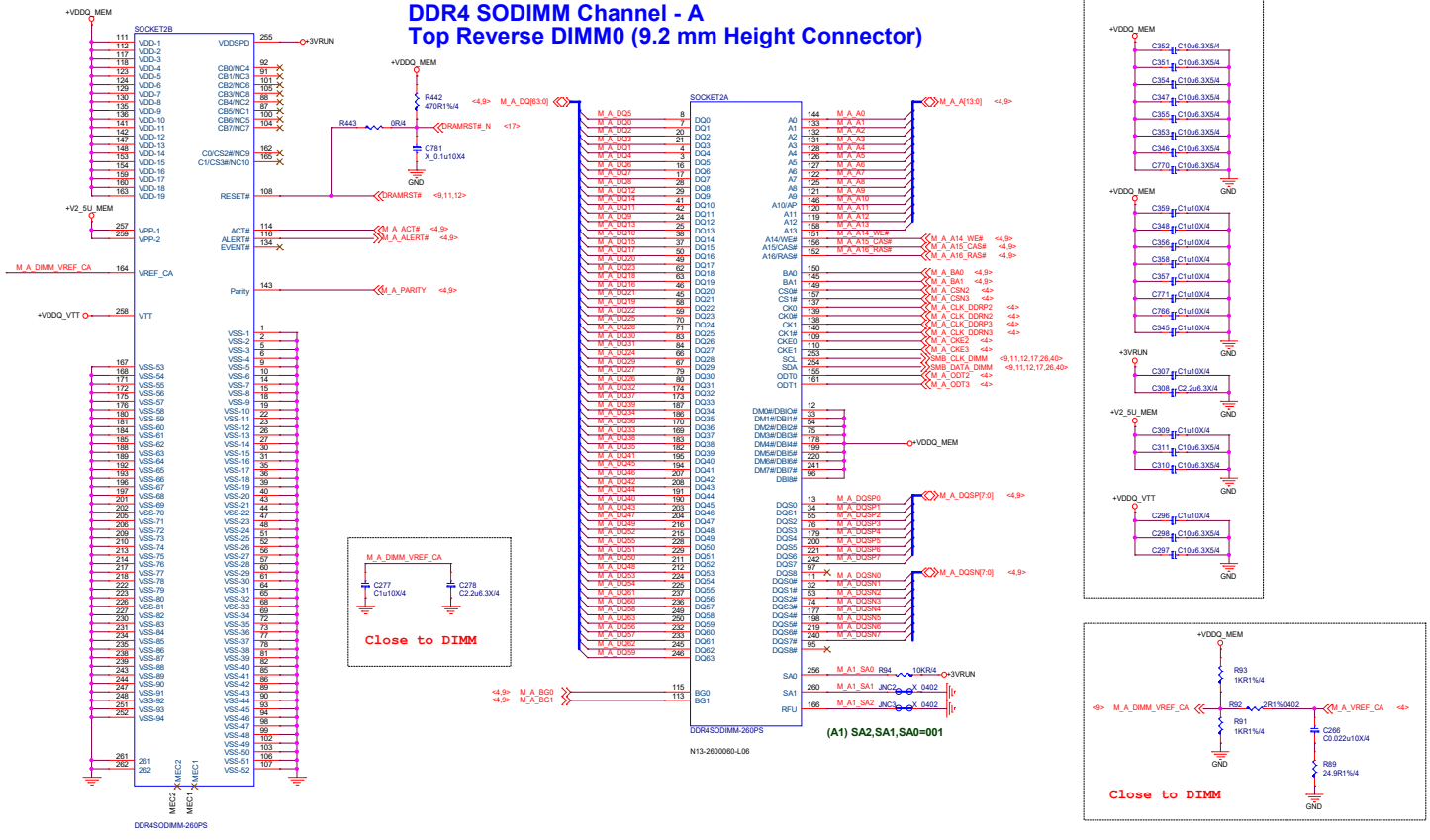

| | | | |
|---|---|---|---|
| Title | CFL-H (VCCGT, GND) | | |
| Size: Custom | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 8 of 62 | | |

# DDR4 SODIMM Channel - A
# Bottom Standard DIMM1 (9.2 mm Height Connector)






| | | | |
|---|---|---|---|
| msi MICRO-STAR INT'L CO.,LTD. | | | |
| Title: DDR4 DIMM1- A1(STD 9.2mm) | | | |
| Size | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 9 of 62 | | |






| | |
|---|---|
| Title | DDR4 DIMM0- A0(RVS 9.2mm) |
| Size | Document Number: MS-18161 |
| Rev | 0D |
| Date: | Tuesday, December 05, 2017 |
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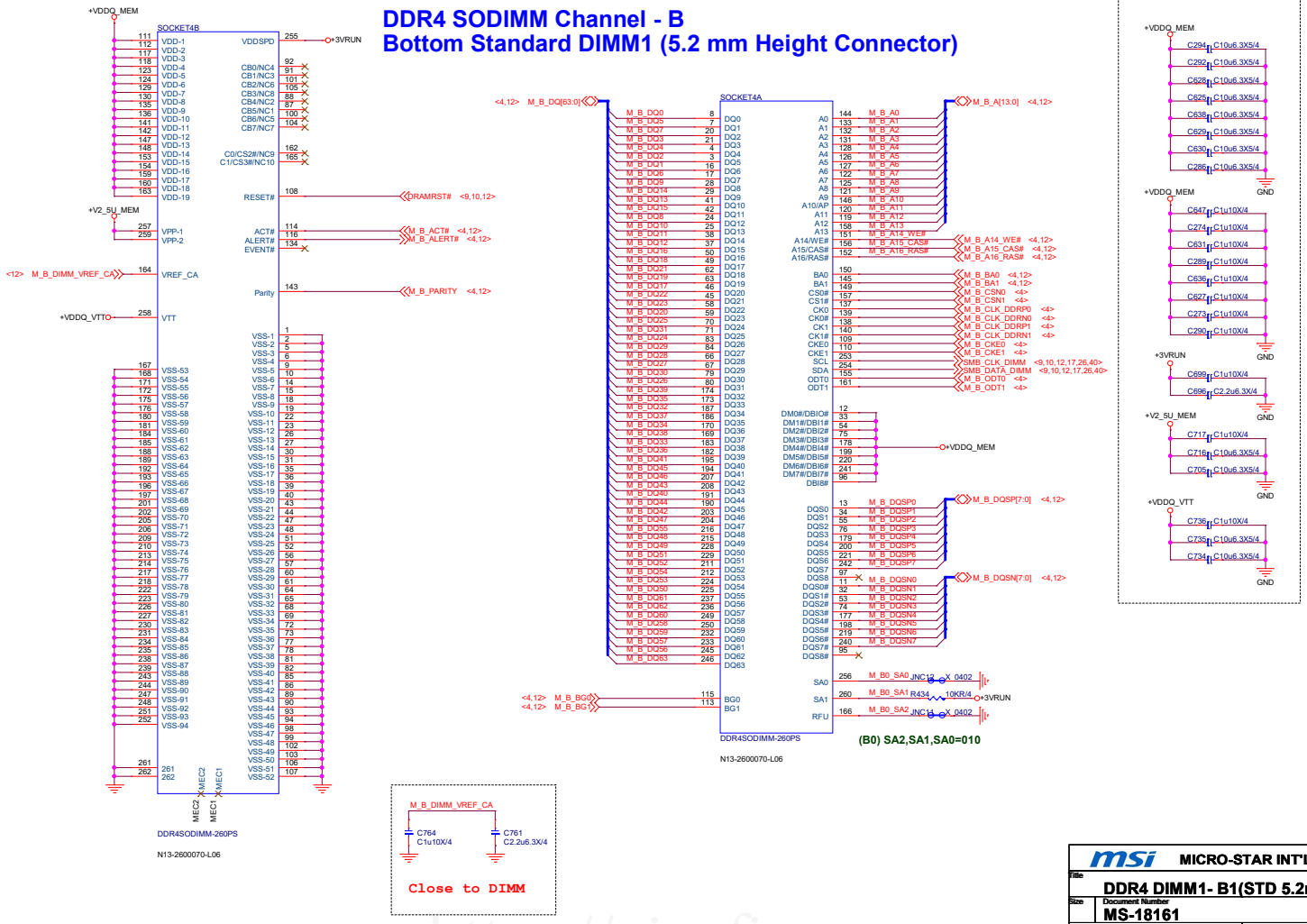
# DDR4 SODIMM Channel - B
# Bottom Standard DIMM1 (5.2 mm Height Connector)




| | |
|---|---|
| Title | DDR4 DIMM1- B1(STD 5.2mm) |
| Company | MICRO-STAR INT'L CO.,LTD. |
| Size | |
| Document Number | MS-18161 |
| Rev | 0D |
| Date: | Tuesday, December 05, 2017 |
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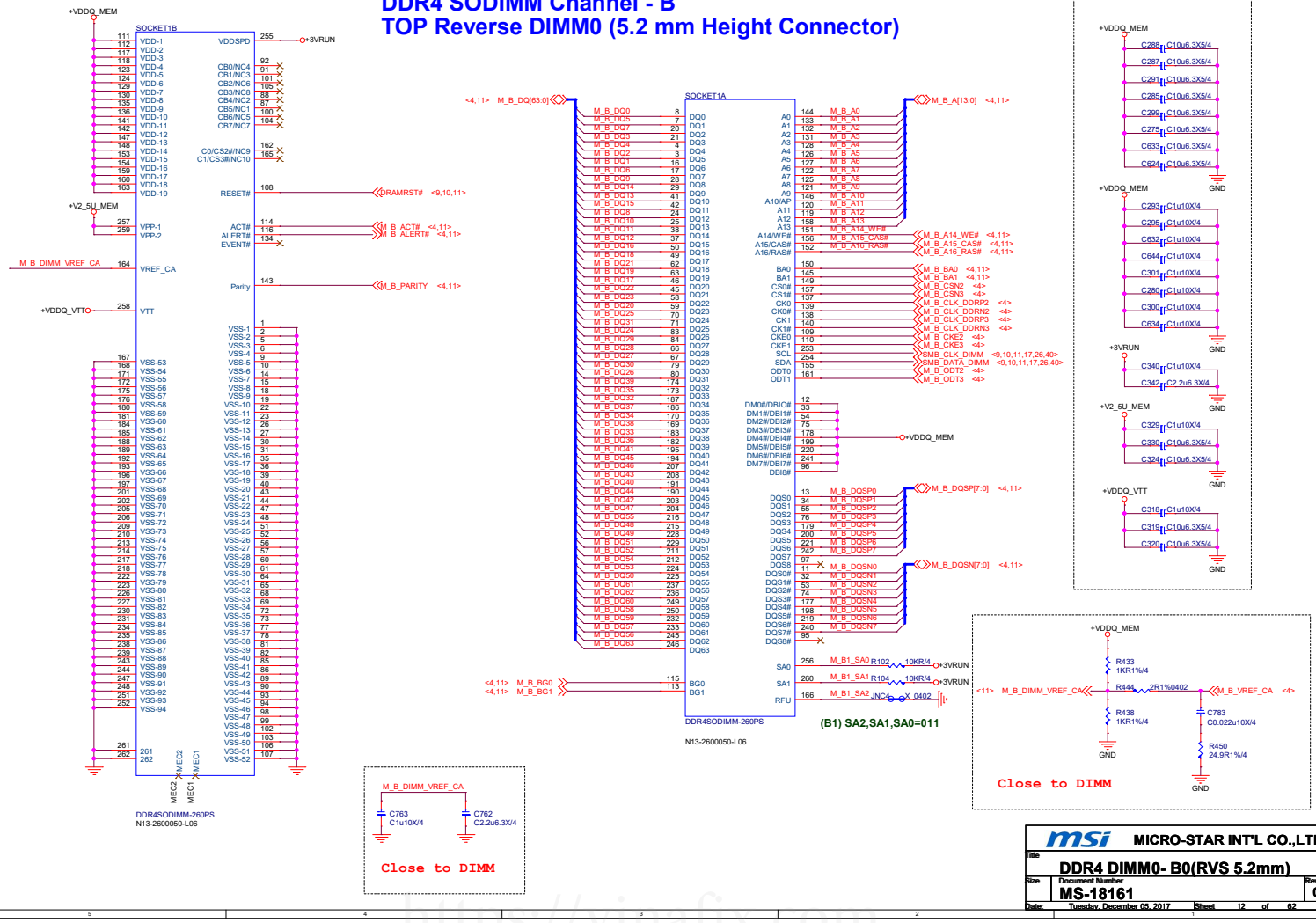
# DDR4 SODIMM Channel - B
# TOP Reverse DIMM0 (5.2 mm Height Connector)




| | | | |
|---|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | | |
| Title | DDR4 DIMM0- B0(RVS 5.2mm) | | |
| Size | Document Number MS-18161 | | Rev 0D |
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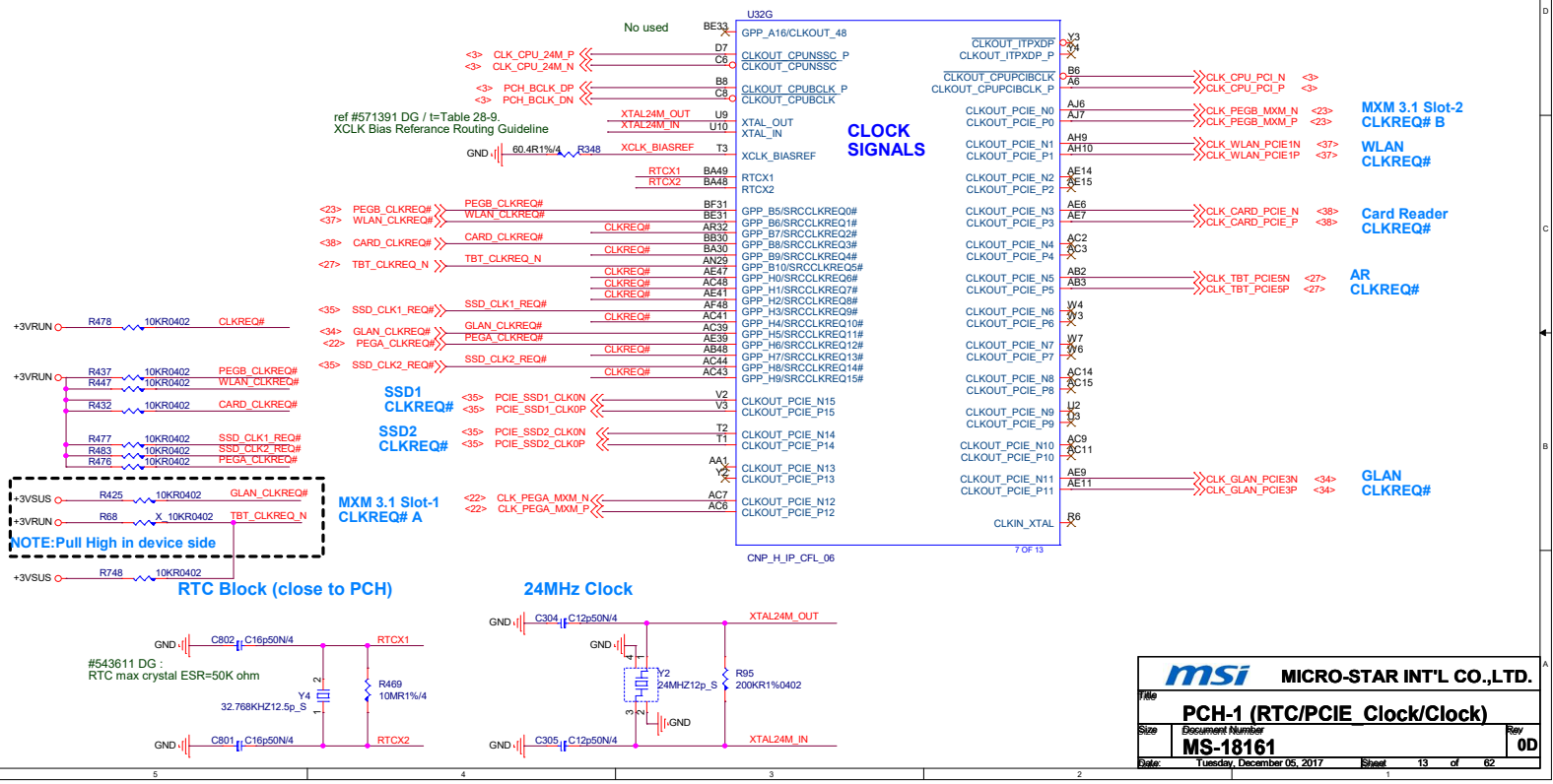
CM238 : B01-CM23805-I06

# PCH-H(RTC/PCIE_Clock/Clock)




## RTC Block (close to PCH)

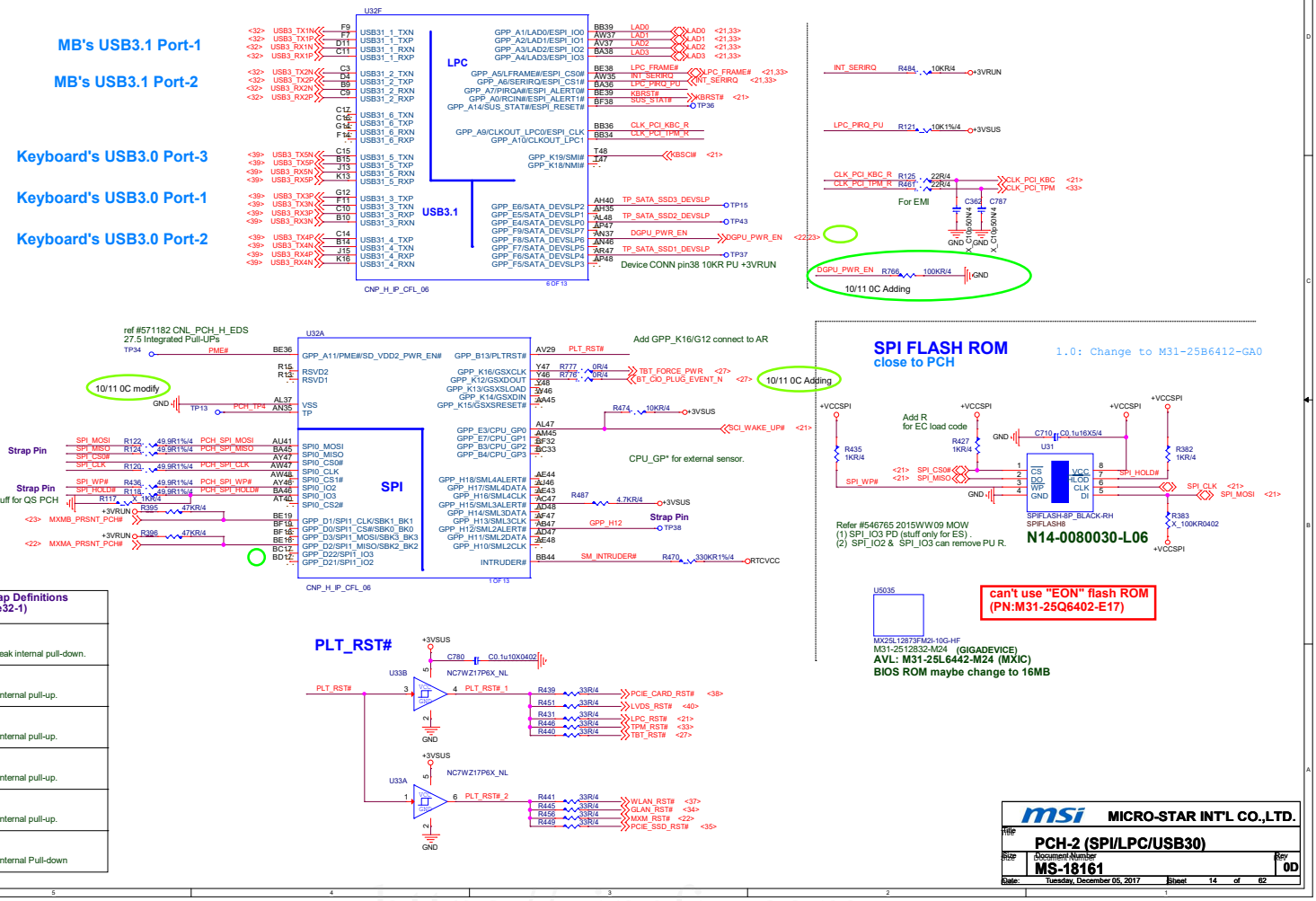



## 24MHz Clock




| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: PCH-1 (RTC/PCIE_Clock/Clock) | | | |
| Size | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 13 of 62 | | |

# PCH-H(SPI/LPC/USB31)




| Functional Strap Definitions (#571182 Table32-1) |
|---|
| **GPP_H12**<br>This signal has a weak internal pull-down. |
| **SPI0_MOSI**<br>This signal has an internal pull-up. |
| **SPI0_MISO**<br>This signal has an internal pull-up. |
| **SPI0_IO2**<br>This signal has an internal pull-up. |
| **SPI0_IO3**<br>This signal has an internal pull-up. |
| **SPI0_CS[2:0]#**<br>This signal has an internal Pull-down |

| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: PCH-2 (SPI/LPC/USB30) | | |
| Size: | Document Number: MS-18161 | Rev: 0D |
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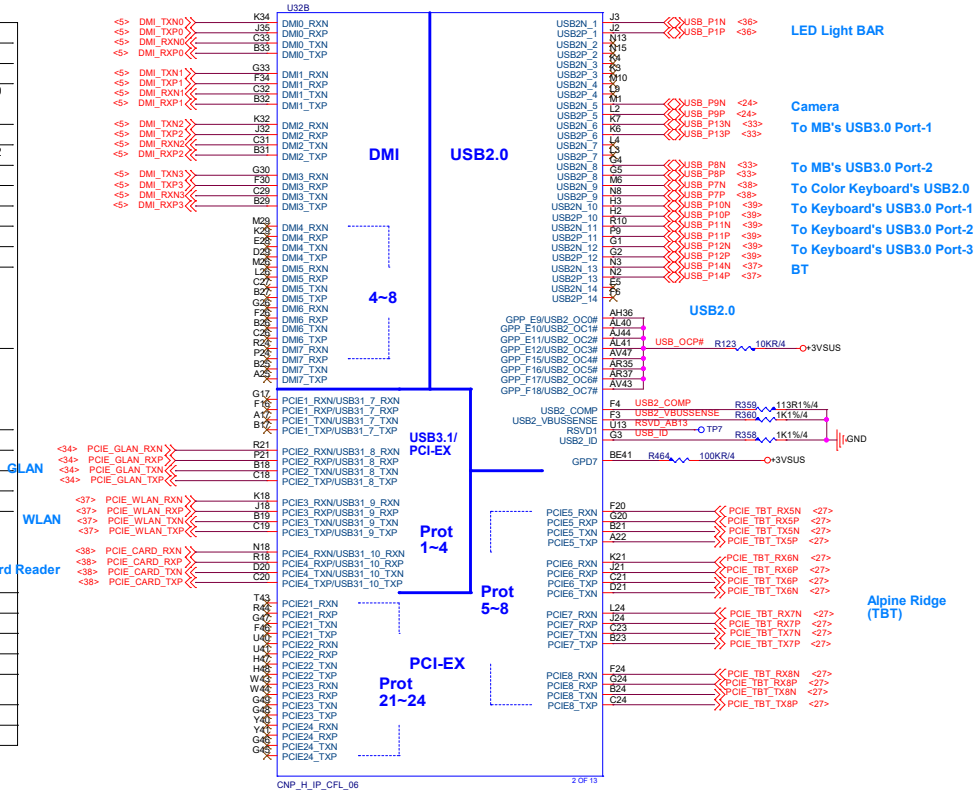
# PCH-H(DMI/PCIE/USB3.1)

## I/O Port Mapping

| Ports Function | | Other | PCIE Storage | | MS-1816 |
|---|---|---|---|---|---|
| USB3 #1 | | | | | USB3.1 (on MB) ; USB2.0 #6 |
| USB3 #2 | | SSIC #1 | | | USB3.1 (on MB) ; USB2.0 #8 |
| USB3 #3 | | SSIC #2 | | | USB3.0 (on KB) ; USB2.0 #10 with iPad Charger |
| USB3 #4 | | | | | USB3.0 (on KB) ; USB2.0 #11 |
| USB3 #5 | | | | | USB3.0 (on KB) ; USB2.0 #12 |
| USB3 #6 | | | | | |
| USB3 #7 | PCIE #1 | | x4 | x2 | |
| USB3 #8 | PCIE #2 | | | | GLAN |
| USB3 #9 | PCIE #3 | | | x2 | WLAN |
| USB3 #10 | PCIE #4 | Gbe | | | CardReader |
| | PCIE #5 | Gbe | x4 | x2 | Intel Alpine Ridge |
| | PCIE #6 | | | | |
| | PCIE #7 | | | x2 | |
| | PCIE #8 | | | | |
| SATA #1 | PCIE #9 | Gbe | x4 | x2 | M.2 PCIE SSD1 (PCIE x4) |
| **SATA #0** | PCIE #10 | | | | M.2 SATA SSD **(SATA #0)** |
| | PCIE #11 | | | x2 | |
| | PCIE #12 | Gbe | | | |
| SATA #0 | PCIE #13 | Gbe | x4 | x2 | ODD |
| SATA #1 | PCIE #14 | | | | |
| SATA #2 | PCIE #15 | | | x2 | HDD |
| SATA #3 | PCIE #16 | | | | SATA SSD |
| **SATA #4** | PCIE #17 | | x4 | x2 | M.2 PCIE SSD2 (PCIE x4) |
| SATA #5 | PCIE #18 | | | | M.2 SATA SSD **(SATA #4)** |
| | PCIE #19 | | | x2 | |
| | PCIE #20 | | | | |
| | PCIE #21 | | x4 | x2 | |
| | PCIE #22 | | | | |
| | PCIE #23 | | | | |
| | PCIE #24 | | | x2 | |
| USB2 #5 | | | | | Camera |
| USB2 #9 | | | | | SSE |
| USB2 #13 | | | | | BT |



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Title: PCH-3 (DMI/PCIE/USB30/USB31)

Size: Document Number: MS-18161 Rev: 0D

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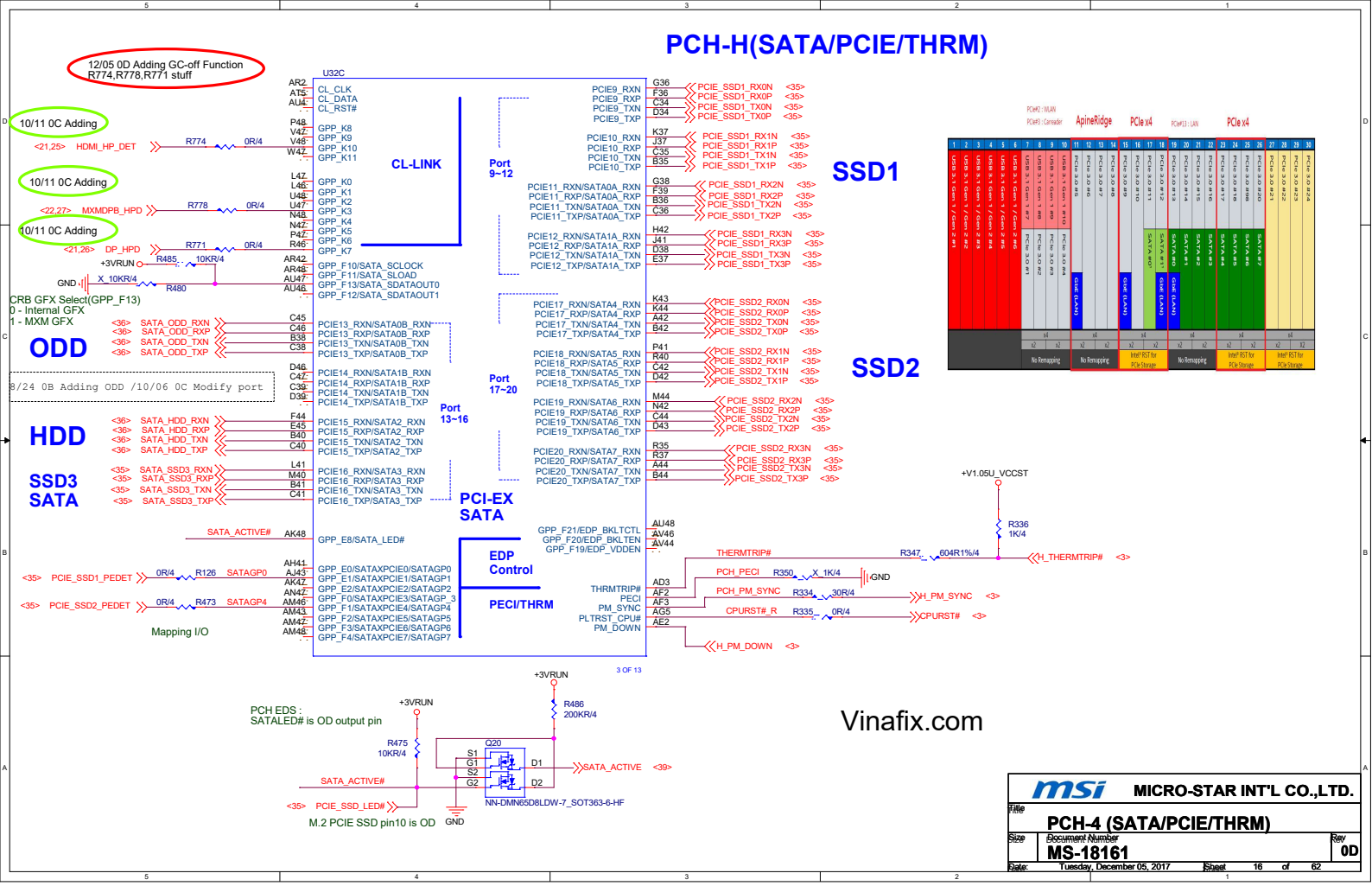
# PCH-H(SATA/PCIE/THRM)







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| | |
|---|---|
| | MICRO-STAR INT'L CO.,LTD. |
| File | PCH-4 (SATA/PCIE/THRM) |
| Size | Document Number: MS-18161 |
| Rev | 0D |
| Date: | Tuesday, December 05, 2017 |
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# PCH-H(HDA/MISC/ACPI/GPIO)

**Functional Strap Definitions (#571182 Table9-1)**

**SPKR / GPP_B14**
The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)

**SMBALERT# / GPP_C2**
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

**SML0ALERT# / GPP_C5**
This signal has a weak internal pull-down.
0 = LPC is selected for EC. (Default)
1 = eSPI Is selected for EC.

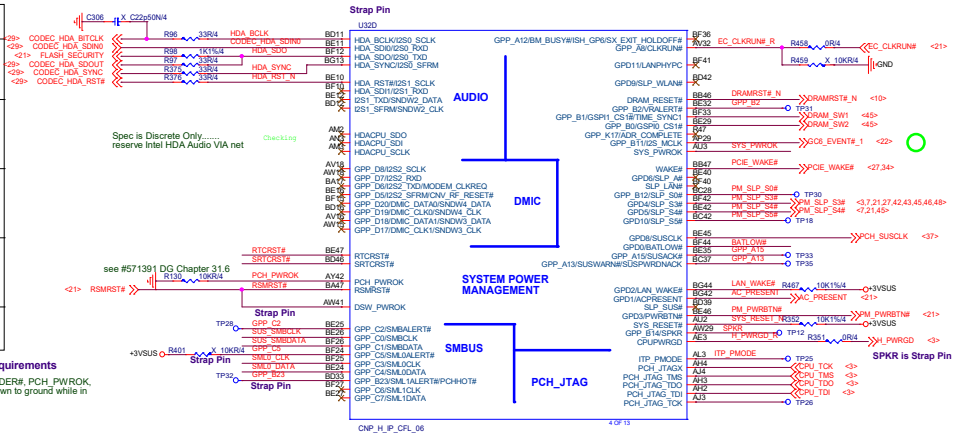
**HDA_SDO**
This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)

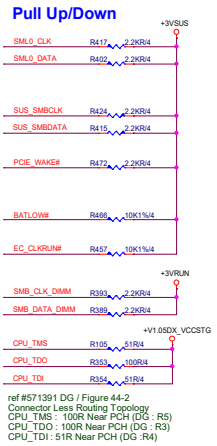
**SML1ALERT# / PCHHOT#/ GPP_B23**
This signal has an internal pull-down.

**#571391 DG Chapter 31.6 :RTC-Well Input Strap Requirements**

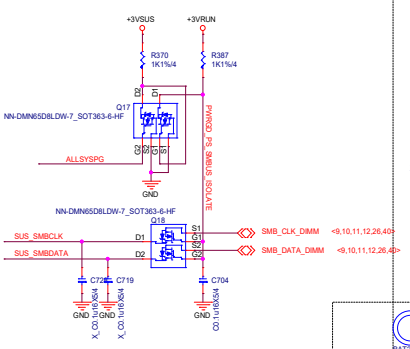
All RTC-well inputs (RSMRST#, RTCRST#, SRTCRST#, INTRUDER#, PCH_PWROK, DSW_PWROK) must be either pulled up to VccRTC or pulled down to ground while in the G3 state.

RSMRST# & DSW_PWROK, PCH_PWROK : PD
RTCRST#, SRTCRST#, INTRUDER# : PU

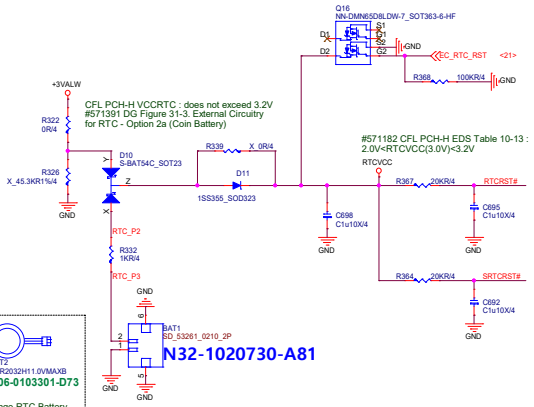


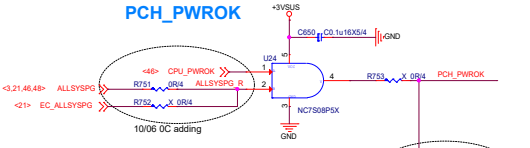

## SMB Isolation



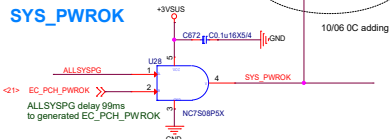

## RTCVCC




## PCH_PWROK




## SYS_PWROK




| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: PCH-5 (HDA/MISC/ACPI/GPIO) | | | |
| Size | Document Number: MS-18161 | | Rev: 0D |
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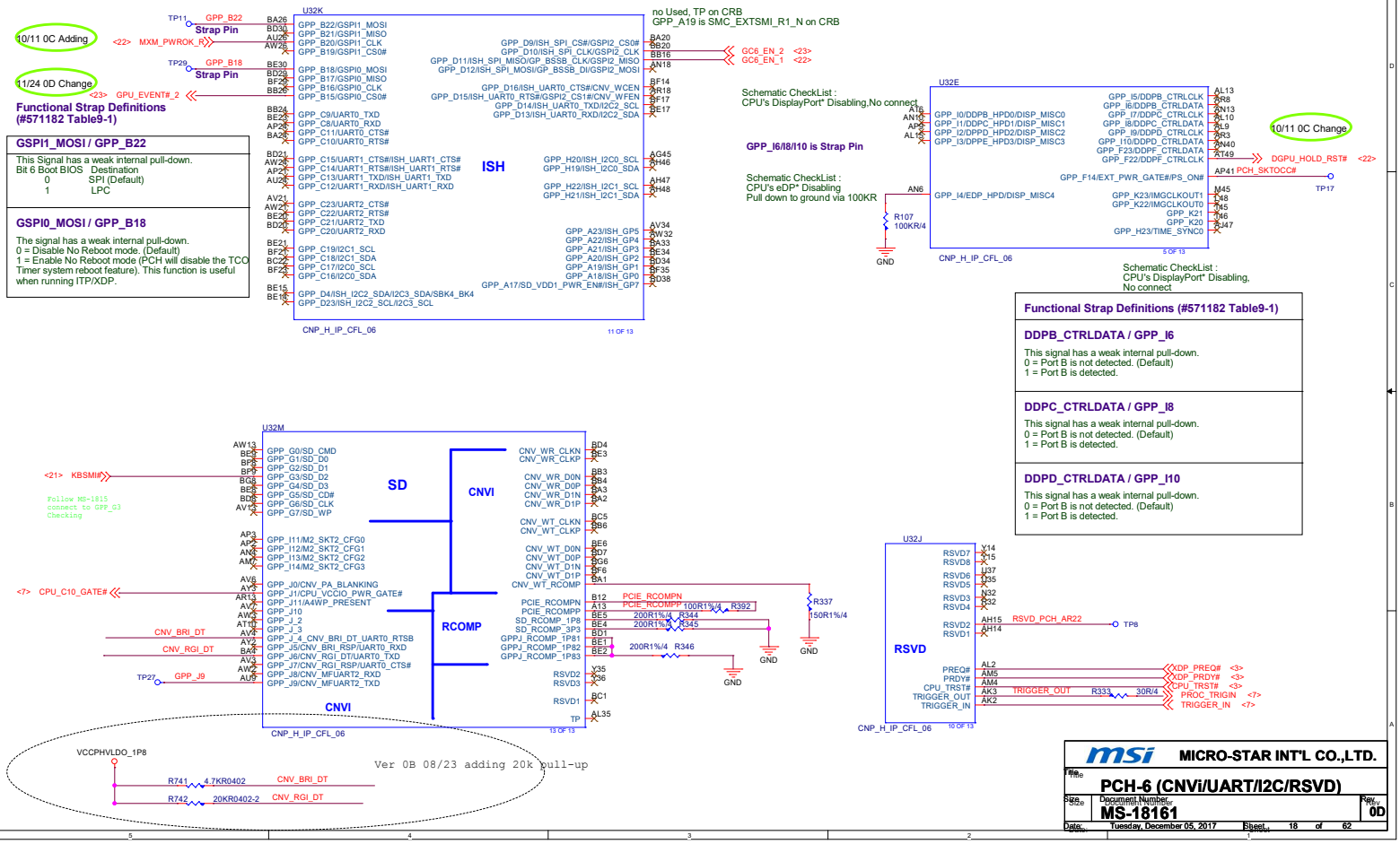
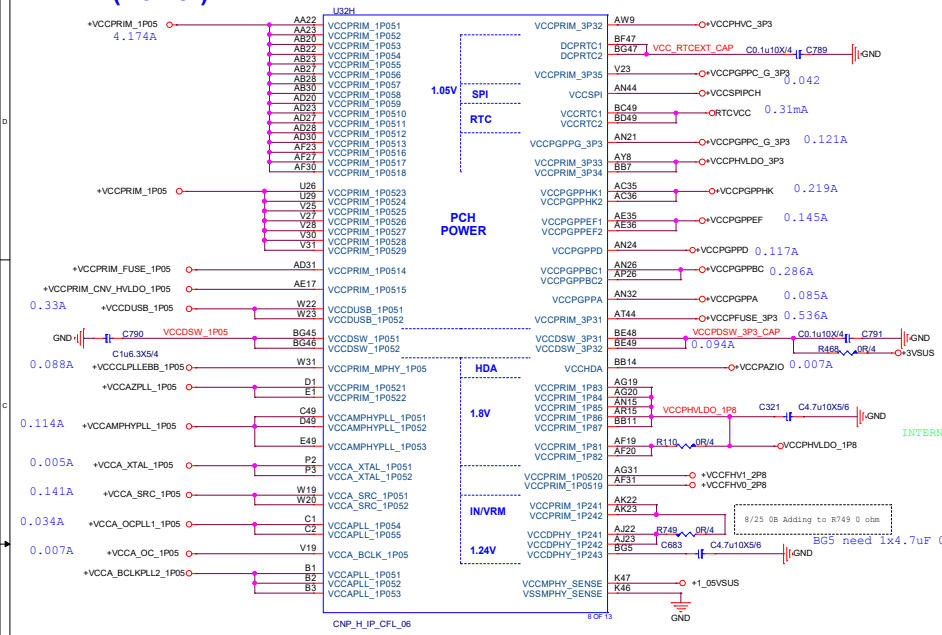
# PCH-H(CNVi/UART/I2C/RSVD)



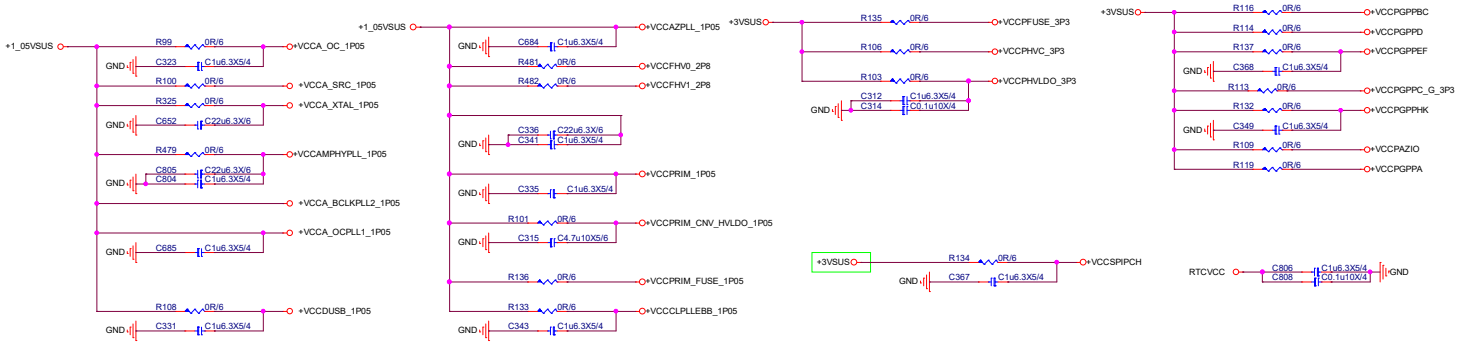

| | | | |
|---|---|---|---|
| Title | PCH-6 (CNVi/UART/I2C/RSVD) | | |
| Size | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | | Sheet 18 of 62 | |

# PCH-H(Power)




## GPIO Group Summary

| GPIO Group | Power Pins | Voltage |
|---|---|---|
| Primary Well Group A (GPP_A) | VCCPGPPA | 1.8V or 3.3V |
| Primary Well Group B (GPP_B)<br>Primary Well Group C (GPP_C) | VCCPGPPBC | 1.8V or 3.3V |
| Primary Well Group D (GPP_D) | VCCPGPPD | 1.8V or 3.3V |
| Primary Well Group E (GPP_E)<br>Primary Well Group F (GPP_F) | VCCPGPPEF | 1.8V or 3.3V |
| Primary Well Group G (GPP_G) | VCCPGPPG_3P3 or VCCPRIM_1P8 | 1.8V or 3.3V |
| Primary Well Group H (GPP_H)<br>Primary Well Group K (GPP_K) | VCCPGPPHK | 1.8V or 3.3V |
| Primary Well Group I (GPP_I) | VCCPRIM_3P3 | 3.3V Only |
| Primary Well Group J (GPP_J) | VCCPRIM_1P8 | 1.8V Only |
| Deep Sleep Well Group (GPD) | VCCDSW_3P3 | 3.3V Only |



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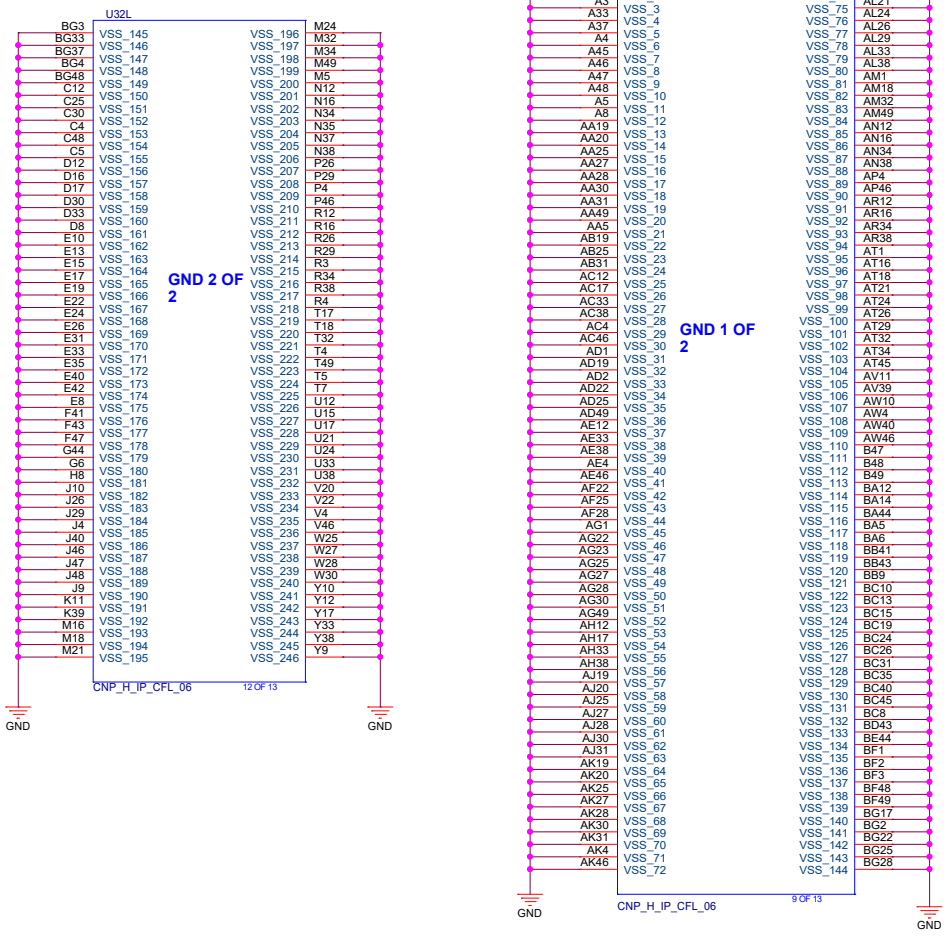
Title: PCH-7 (Power)

Size: | Document Number: MS-18161 | Rev: 0D

Date: Tuesday, December 05, 2017 | Sheet: 19 of 62

# PCH-H(GND)



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| | | |
|---|---|---|
| Title | PCH-8 (GND) | |
| Size | Document Number: MS-18161 | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 20 of 62 | |

# KBC/EC/uP (ENE9028)

**EC Code Note :**

(1)AC_OK=HIGH Active (AC exist)

(2)USB_ENABLE :
Assertion & De-assertion follow RSMRST#

(3)MXM_PWRSR_EN :
Assertion & De-assertion follow ALLSYSPG

## Hardware Reset

RST_SW# — Close to SW — R327 33R/4 — D9 ESD-SFI0402-050E101NP — SW1 SW-TACTB1S-RH-9 N71-0101710-D02

## PU/PD

RSMRST# follow DG modify to 10K

10/11 0C Change

12/05 0D Adding GC-off Function
R773 ; R775 un_stuff

EC pin80 tie to pin81
EC pin82 tie to pin79 for EC request

10/06 0C adding

0B:
remove MXMA_PRSNT_EC# and add GC6_ON
for notifying EC of GC6 states

10/11 0C Change

8/24 Ver 0B Change net Name

U34

### LPC I/F
SERIRQ, LFRAME#, PCICLK, CLKRUN#/GPIO1D, LAD0, LAD1, LAD2, LAD3

### ALLSYSPG
ECRST#, KBRST#/GPIO01, SCI#/GPIO0E, GA20/GPIO00, PCIRST#/GPIO05

### FAN&PWM
PWM0/GPIO0F, PWM1/GPIO10, PWM2/GPIO11, PWM3/GPIO19, FANPWM0/GPIO12, FANPWM1/GPIO13, FANFB0/GPIO14, FANFB1/GPIO15

### IKB
KSO0/GPIO20, KSO1/GPIO21, KSO2/GPIO22, KSO3/GPIO23, KSO4/GPIO24, KSO5/GPIO25/UART_SOUT, KSO6/GPIO26, KSO7/GPIO27/SERIRQ(LPC_Bypass)UART_RTS, KSO8/GPIO28, KSO9/GPIO29, KSO10/GPIO2A, KSO11/CIRTOB/LAD3(LPC_Bypass), KSO12/GPIO2C/LAD2(LPC_Bypass)UART_DTR, KSO13/GPIO2D/LAD1(LPC_Bypass), KSO14/GPIO2E/LAD0(LPC_Bypass), KSO15/GPIO2F, KSO16/GPIO48/UART_SOUT2, KSO17/GPIO49

### ESB
KSI0/GPIO30/E51TXD, KSI1/GPIO31, KSI2/GPIO32, KSI3/GPIO33, KSI4/GPIO34, KSI5/GPIO35, KSI6/GPIO36, KSI7/GPIO37/EDI_DO

GPIO0B/ESB_CLK, GPIO0C/ESB_DAT_O

### CIR
GPIO40/AD6, GPIO41/CIR_RLC_TX/AD7, GPIO3A/OWM, GPIO0D/RLC_TX2

### SPI FLASH
MISO/GPIO05B, MOSI/GPIO5C, SPICLK/GPIO5B, SPICS#/GPIO5A

### PS2 I/F
PSCLK3/GPIO4E, PSDAT3/GPIO4F, PSCLK2/GPIO4C/SCL3, PSDAT2/GPIO4D/SDA3, PSCLK1/GPIO4A/SCL2/SMBD_CLK, PSDAT1/GPIO4B/SDA2/SMBD_DAT

### UART
E51TXD/GPIO16, E51CLK/GPIO17

### LED
GPIO5D, GPIO5E

KB9028Q-C-RH

### POWER/GROUND
VCC_LPC, VCC, VCC-1, VCC-2, VCC-3, VCC0, VCC_IO2, AVCC, AGND, GND, GND-1, GND-2, GND-3, GND-4

+3VALW — C726 C784 C788 C740 C750 (0.1U/10K4)

MXMA_SCL — R448 X 4.7KR0402 — +3VRUN
MXMA_SDA — R452 X 4.7KR0402 — +3VRUN
R492 0R/4 — ACE_I2C_SDA2 <28>
R493 0R/4 — ACE_I2C_SCL2 <28>

### SMBUS
SDA0/GPIO45, SCL0/GPIO44, IEDI_SDA/SDA1/GPIO47, IEDI_SCL/SCL1/GPIO46

EC_SDA <25>, EC_SCL <25>

### AD/DA
DA0/GPIO3C, DA1/GPIO3D, DA2/GPIO3E, DA3/GPIO3F, AD0/GPIO3B, AD1/GPIO39, AD2/GPIO3A, AD3/GPIO3B, AD4/GPIA2, AD5/GPIA3

CAMERA_ON <24>, EAPD <29>, EC_MUTE# <30>

KBIN0, KBIN1, KBIN2, KBIN3, KBIN4, KBIN5

MXM_RUNON_DELAY <22,23>

0B:
Change from BT_PWR_ON to MXM_RUNON_DELAY
for controlling MXM 3V and 5V power

### SDI
GPXIOA00/GPIO60/SHICS#, GPXIOA01/GPIO61/SHICLK, GPXIOA02/GPIO62/SHIDO

ECSSE_SPI_CS <38>, ECSSE_SPI_CLK <38>, ECSSE_SPI_DO <38>

POWER_FAIL,0,GPIO63/GPXIOA03, GPIO64/GPXIOA04, GPIO65/GPXIOA05, VCOUT1/GPIO66/GPXIOA06, VCOUT0/GPIO67/GPXIOA07, GPIO68/GPXIOA08, GPIO69/GPXIOA09, GPIO6A/GPXIOA10, GW/GPIO6B/GPXIOA11, SDIDO/GPIO70/8/GPXIOD00, GPIO79/GPXIOD01, EC_EN#/GPIO7A/GPXIOD02, GPIO7B/GPXIOD03, GPIO7C/GPXIOD04, GPIO7D/GPXIOD05, GPIO7E/GPXIOD06, GPIO7F/PECI

SUS_ON <24,42,43>, CPU_5V_FAN_FB <38>, ADP_ICC <41>, EC_PROCHOT# <3>, EC_RTC_RST <17>, LED_FAN# <38>, LED_CHARGE# <39>, LED_BATLOW# <39>, AC_PRESENT <17>, ECSSE_SPI_DI <38>, AC_OK <41>, LED_SSE <38>, PWR_SW# <38>, HIFIAUDIO_EN <38>, MXM_EC_RST# <23>, PM_PWRBTN# <17>, H_PECI <3>

ADP_ICC_R R390 0R/4

Clear CMOS

AC_OK=HIGH (AC exist)

R423 43R0402 — +3VSUS — For ENE9048, GPIO04 KBSMI# PU3.3V

GPIO04 — MXMB_PRSNT_EC# <23>
PROCHOT#, clk_peri/GPIO08 — SCI_WAKE_UP# <14>
POWER_FAIL1/GPIO18 — EC_PCH_PWROK <17> — **EC_PCH_PWROK**
GPIO50 — LED_WLAN# <39>
GPIO52 — USB_ENABLE <33,39>
WDT_LED#/GPIO54 — LED_PWR# <38>
GPIO56 — RSMRST# <17>
XCLK32K/GPIO57 — PM_SLP_S3# <3,7,17,27,42,43,45,46,48>
GPIO59 — PM_SLP_S4# <7,17,45>

GPIO18 :
ALLSYSPG delay 99ms
to generated EC_PCH_PWROK

10/06 0C adding

EC_ALLSYSPG — LED_CAPS# <39>
GPIO1A/NUMLED# — EC_THE_ID <29,38>
GPIO53/CAPSLED#
GPIO55/SCROLED#

### VCCSPI
+3VSUS — R381 0R/6 — +VCCSPI

### MB ID
+3VALW — R462 10KR0402 — MB_ID — R460 X_0R/4
MXM_ACOK_EC — R463 0R/4 — MB_ID

### For EMI
KBOUT17 EC77 C100p16N0402
KBOUT16 EC78 C100p16N0402

EC74: KBOUT7, KBOUT6, KBOUT5, KBOUT4 — 8p4C-100p50N0402-RH
EC75: KBOUT3, KBOUT2, KBOUT1, KBOUT0 — 8p4C-100p50N0402-RH
EC78: KBOUT11, KBOUT10, KBOUT9, KBOUT8 — 8p4C-100p50N0402-RH
EC79: KBOUT15, KBOUT14, KBOUT13, KBOUT12 — 8p4C-100p50N0402-RH

### KB
CON7 — FPC_S26_7 — FPC26P-B-1PITCH_BLACK-RH — **N5A-26F0340-H06**

KBOUT17..KBOUT0 — KBIN0..KBIN7

RN2 8P4R-10KR0402 — RN3 8P4R-10KR0402

| AC_OK# | MXM_ACOK_EC | MXM Mode |
|---|---|---|
| 0 | 0 | AC |
| 0 | 1 | AC |
| 1 | 0 | AC |
| 1 | 1 | DC |

0B:
for NVIDIA battery boost function

+3VRUN — R323 100KR0402 — MXM_ACOK <22,23>
MXM internal PU 100K to 3.3V

+3VALW — R321 100KR0402 — Q15 N-2N7002CK_SOT23-3-RH — AC_OK
+3VRUN — R316 X_100KR0402 — MXM_ACOK_EC
Q14 NN-DMN65D8LDW-7_SOT363-6-HF — R315 X_0R0402 — AC_OK#



| | | |
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# MXM 3.1 Slot-1

#DG-07875-001 Design Guide
Table 10.1 Standard Configurations

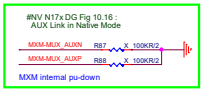
| GB4-256 | **Standard Mode** |
|---|---|
| Link AB | LVDS (Dual Link), DVI (Dual Link) |
| Link C | DisplayPort, HDMI |
| Link D | DisplayPort/eDP |
| Link E | DisplayPort, HDMI, DVI (Single Link or Dual Link with IFPF) |
| Link F | DisplayPort/eDP, DVI (Single Link with IFPE) |

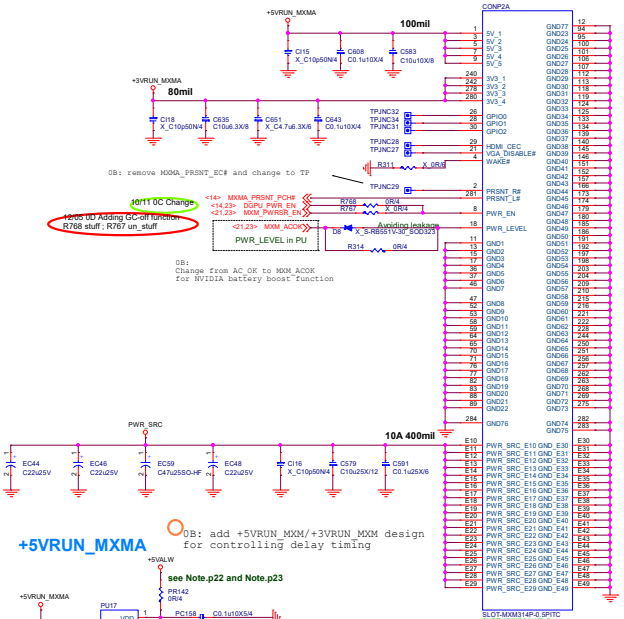
**External (DP)=Link E**

**External (DP)=Link F**
**(To Intel AR's SINK0)**

**External (HDMI)=Link C**

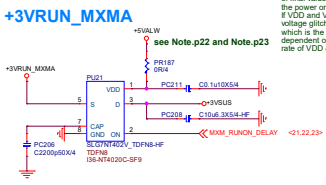
**External (eDP)=Link D**









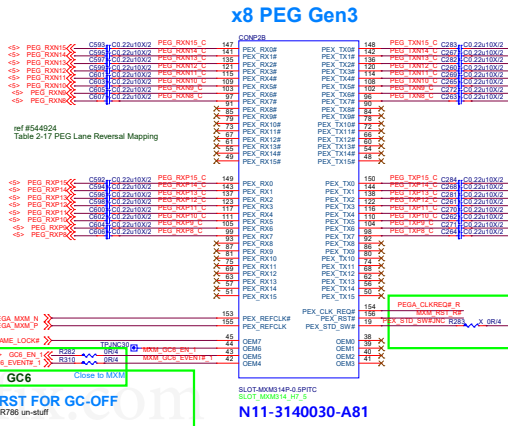

**Note.p22**
SLG7NT402V Turn ON
The normal power on sequence is first VDD, with VD only being applied after VDD is > 1 V, and then ON after VD is at least 90% of final value. The normal power off sequence is the power on sequence in reverse.
If VDD and VD are turned on at the same time then it is possible that a voltage glitch will appear on VS before VDD achieves 1V which is the VT of the main MOSFET. The size of the glitch is dependent on source and drain capacitance loading and the ramp rate of VDD & VD.

**Note.p23 SLG7NT402V Electrical Characteristics**

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | -20 to 70°C | 2.5 | -- | 5.5 | V |
| $I_{DD}$ | Power Supply Current (PIN 1) | when OFF | -- | -- | 1 | µA |
| | | when ON, No load | -- | 70 | 100 | µA |
| $RDS_{ON}$ | Static Drain to Source ON Resistance | $T_A$ 25°C @ 100 mA | -- | 7.8 | 8.5 | mΩ |
| | | $T_A$ 70°C @ 100 mA | -- | 8.5 | 9.6 | mΩ |
| IDS | Operating Current | $V_D$ = 1.0 V to 5.5 V | -- | -- | 4 | A |
| $V_D$ | Drain Voltage | | 1.0 | -- | $V_{DD}$ | V |

**+5VRUN_MXMA**

**+3VRUN_MXMA**





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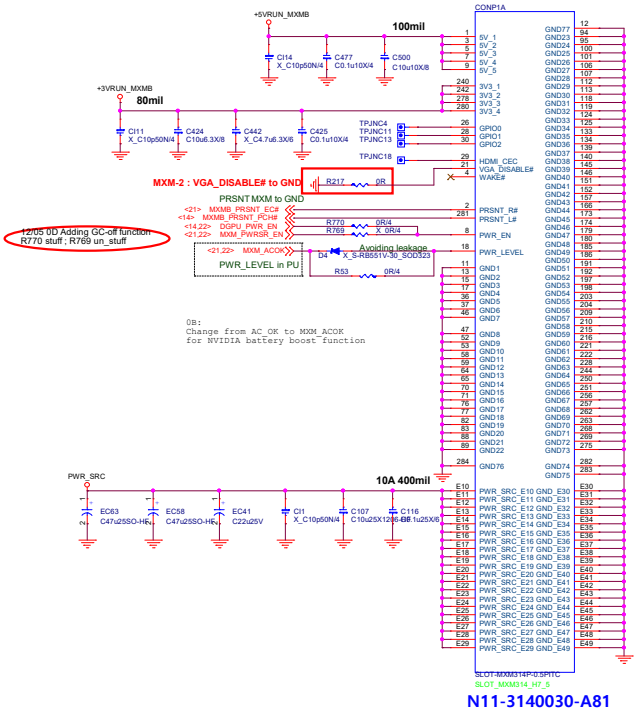
# MXM 3.1 Slot-2

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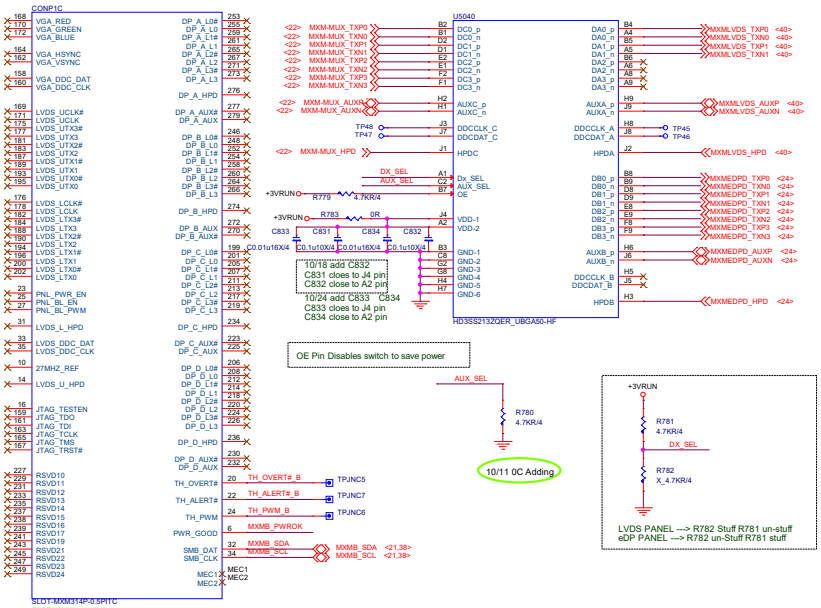


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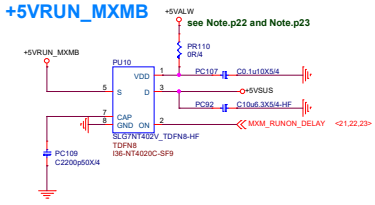
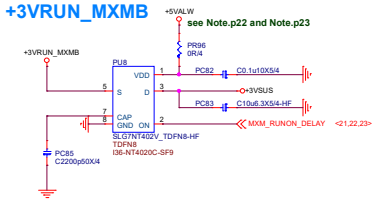
Vinafix.com

## +5VRUN_MXMB

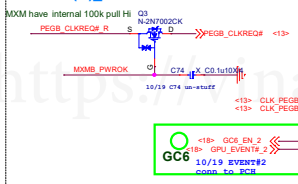



## +3VRUN_MXMB

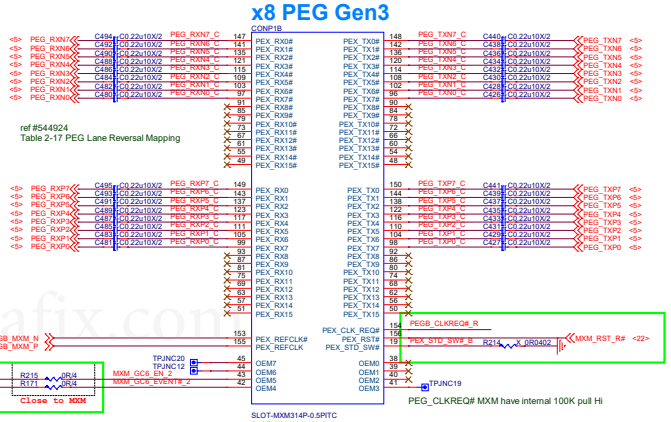



0B: add +5VRUN_MXMB/+3VRUN_MXMB design
for controlling delay timing

## PEG(B)_CLKREQ#




## x8 PEG Gen3

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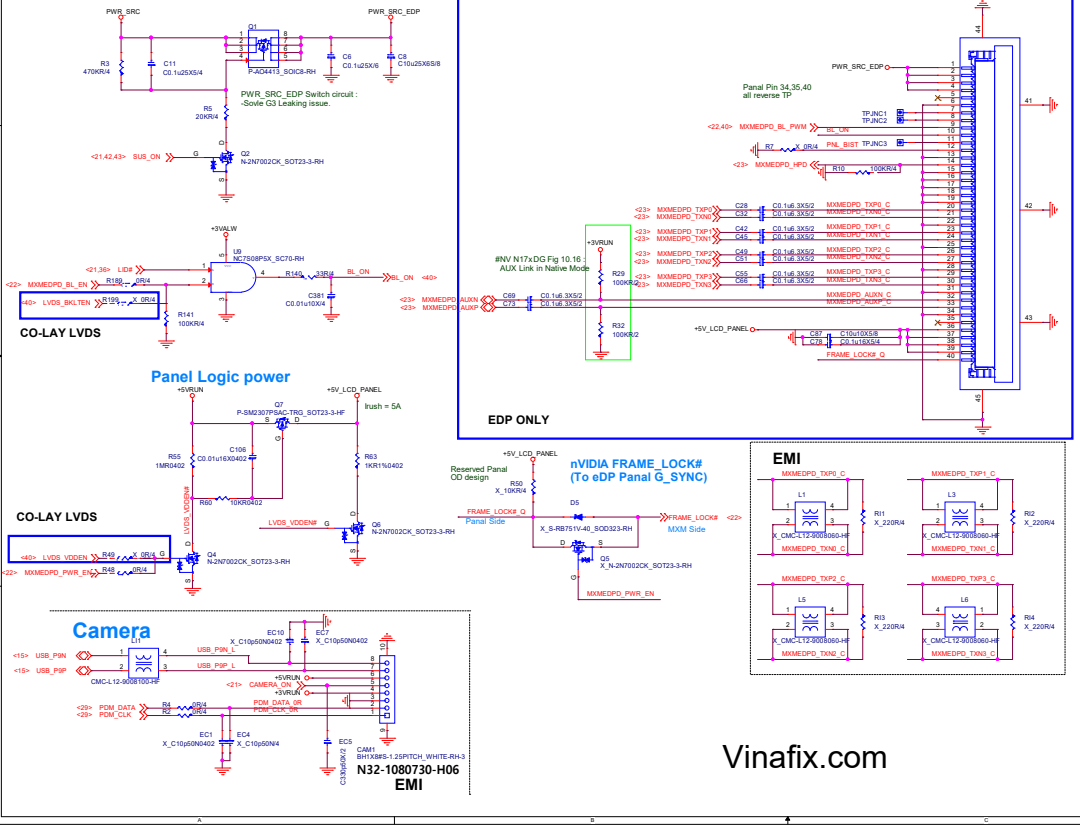
# eDP Panal & Camera




< Table5. Pin Assignment for LCD Module Connector >

| Pin No. | Symbol | Description | I/O |
|---|---|---|---|
| 1 | NC(G_SYNC) | Reserved for LCD manufacturer’s use | P |
| 2 | H_GND | High Speed Ground | - |
| 3 | Lane3_N | Complement Signal Link Lane 3 | O |
| 4 | Lane3_P | True Signal Link Lane 3 | O |
| 5 | H_GND | High Speed Ground | - |
| 6 | Lane2_N | Complement Signal Link Lane 2 | O |
| 7 | Lane2_P | True Signal Link Lane 2 | O |
| 8 | H_GND | High Speed Ground | - |
| 9 | Lane1_1N | Complement Signal Link Lane 1 | O |
| 10 | Lane1_1P | True Signal Link Lane 1 | O |
| 11 | H_GND | High Speed Ground | - |
| 12 | Lane1_0N | Complement Signal Link Lane 0 | O |
| 13 | Lane1_0P | True Signal Link Lane 0 | O |
| 14 | H_GND | High Speed Ground | - |
| 15 | AUX_CH_P | True Signal Auxiliary Channel | I/O |
| 16 | AUX_CH_N | Complement Signal Auxiliary Channel | I/O |
| 17 | H_GND | High Speed Ground | - |
| 18 | LCD_VCC | 5.0VDC | P |
| 19 | LCD_VCC | 5.0VDC | P |
| 20 | LCD_VCC | 5.0VDC | P |
| 21 | LCD_VCC | 5.0VDC | P |
| 22 | BIST | VDC LCD Panel Self Test Enable ( max2.5VDC) | - |
| 23 | LCD_GND | LCD logic and driver ground | - |
| 24 | LCD_GND | LCD logic and driver ground | - |
| 25 | LCD_GND | LCD logic and driver ground | - |
| 26 | LCD_GND | LCD logic and driver ground | - |
| 27 | HPD | HPD signal pin | I/O |
| 28 | BL_GND | Backlight ground | - |
| 29 | BL_GND | Backlight ground | - |
| 30 | BL_GND | Backlight ground | - |
| 31 | BL_GND | Backlight ground | - |
| 32 | BL_ENABLE | 3.3VDC from system | I/O |
| 33 | BL_PWM | PWM Input | I/O |
| 34 | NC(H_SYNC) | Reserved for LCD manufacturer’s use | I/O |
| 35 | NC(DBC) | Reserved for LCD manufacturer’s use | I/O |
| 36 | BL_PWR | 12VDC | P |
| 37 | BL_PWR | 12VDC | P |
| 38 | BL_PWR | 12VDC | P |
| 39 | BL_PWR | 12VDC | P |
| 40 | NC(COLOUR ENI N) | Reserved for LCD manufacturer’s use | I/O |



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LVDS & Conn/CAM

MS-18161 0D

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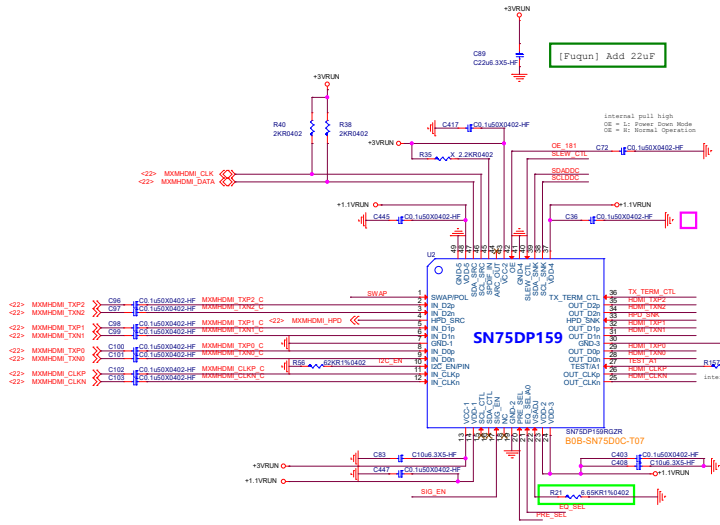
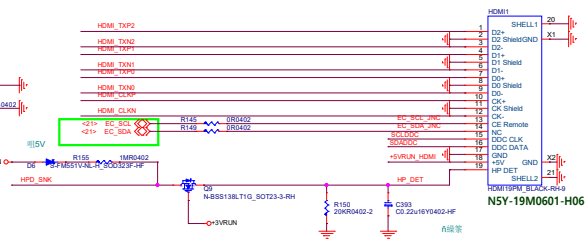
# HDMI(DP159)

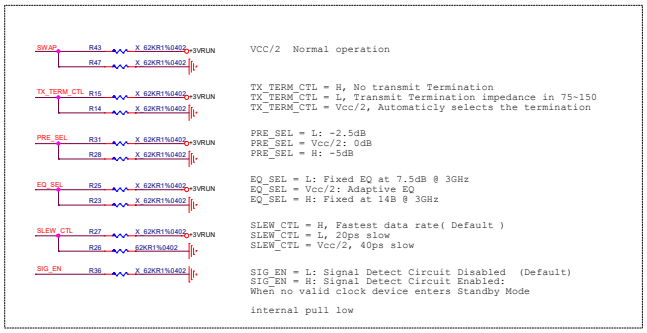


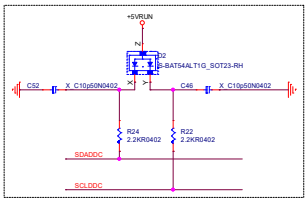

| P159 | NC |
|---|---|
| S181 | Stuff |

## HDMI connector

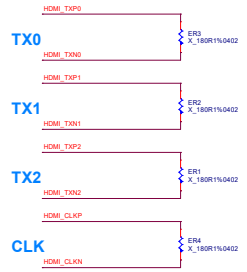
An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.
HPD_SNK Internal PD 150kohm



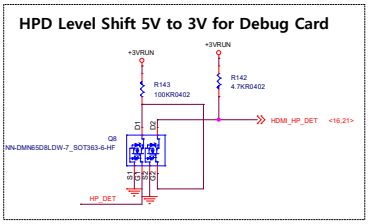



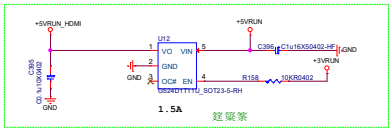




## EMI Close Connector




## HPD Level Shift 5V to 3V for Debug Card



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| Title: | HDMI(DP159) | | |
| Size: C | Document Number: MS-18161 | | Rev.: 0D |
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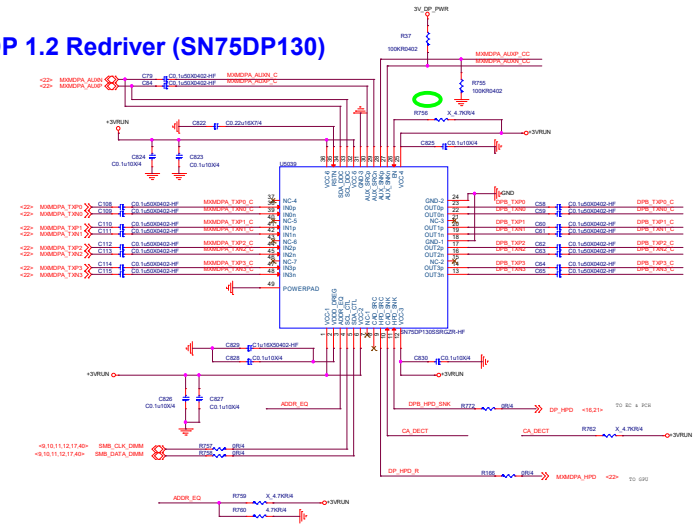
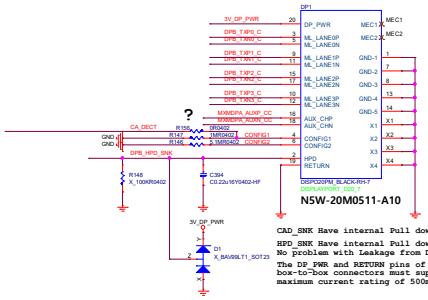
# DP 1.2 Redriver (SN75DP130)



## Display Port



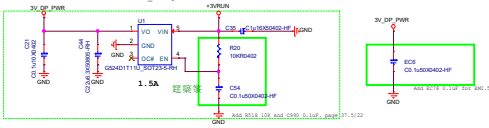
N5W-20M0511-A10

CAD_SNK Have internal Pull down 1Mohm.

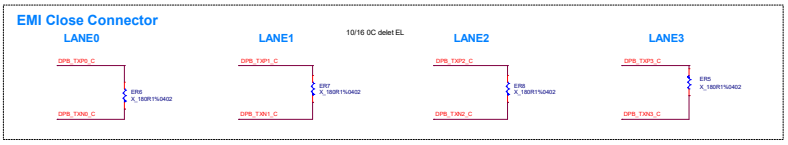
HPD_SNK Have internal Pull down 150kohm. No problem with Leakage from DP device

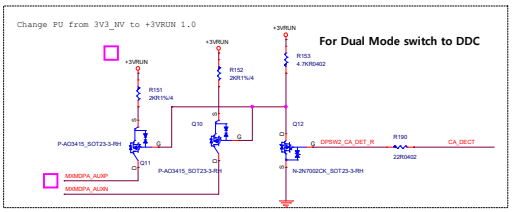
The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.



## EMI Close Connector

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|---|---|---|---|
| Title | MICRO-STAR INT'L CO.,LTD. | | |
| | DP 1.2 (SN75DP130) | | |
| Size | Document Number | | Rev |
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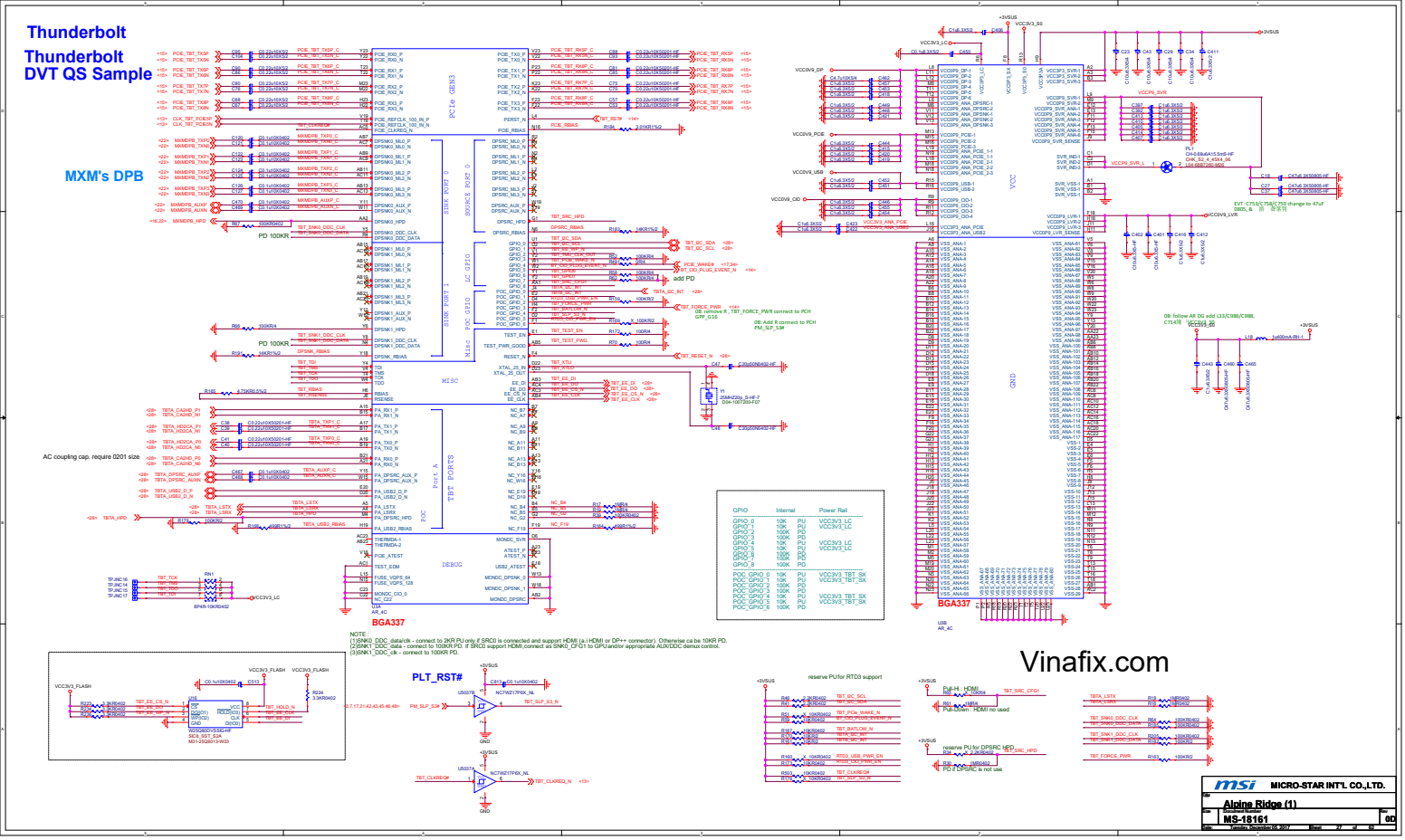
**Thunderbolt**

**Thunderbolt**
**DVT QS Sample**

**MXM's DPB**

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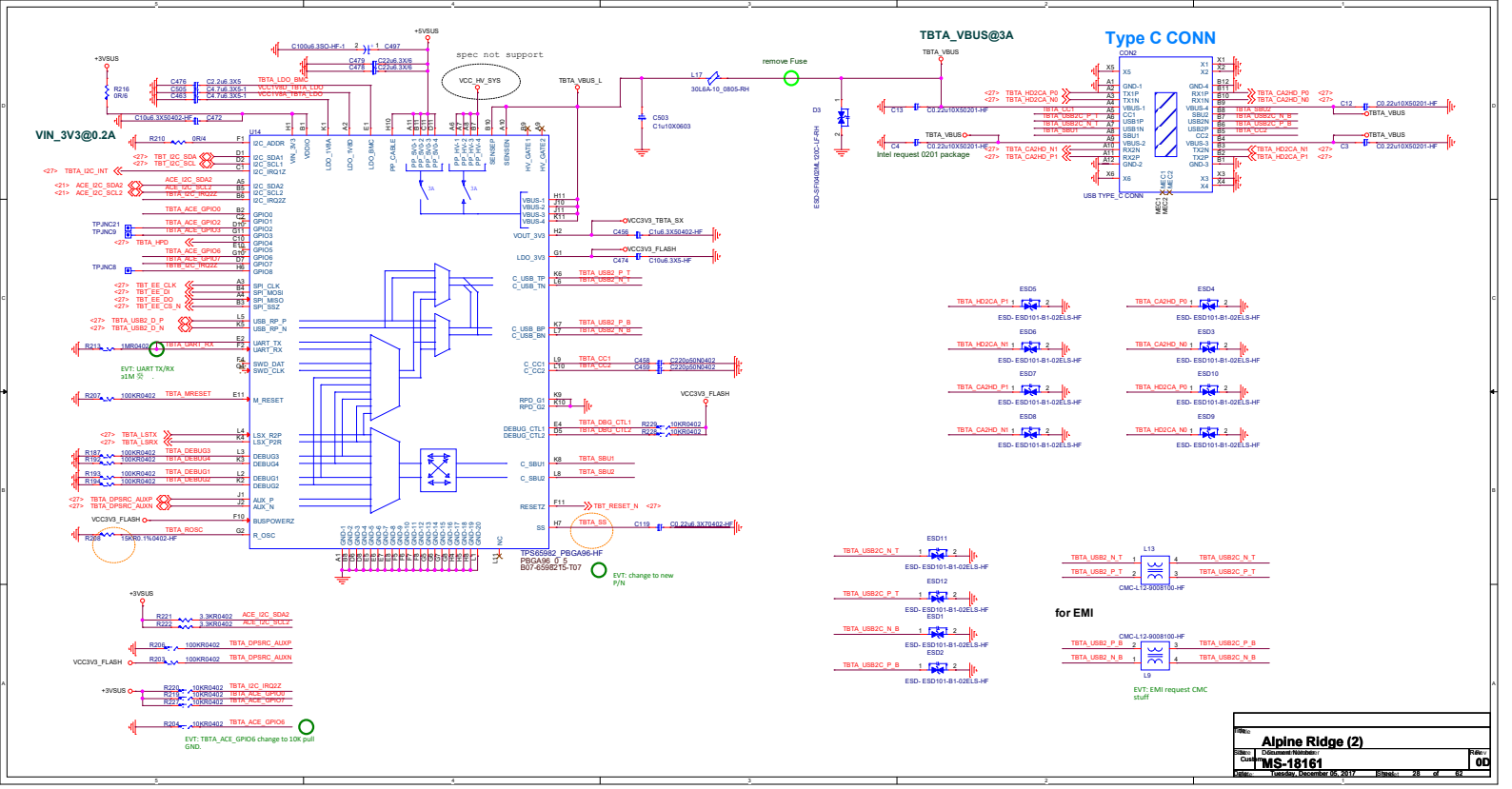
| | |
|---|---|
| Company | MICRO-STAR INT'L CO.,LTD. |
| Title | Alpine Ridge (1) |
| Size | C |
| Document Number | MS-18161 |
| Rev | 0D |
| Date | Tuesday, December 05, 2017 |
| Sheet | 27 of 50 |



# AUDIO(ALC1220)

| ALC1220 | AZ_GPIO3_DSD |
|---|---|
| PCM | H |
| Native DSD | L |
| DOP DSD | L |

8/24 Ver 0B Change net Name

To EC
To EC

To EC
Internal Mic

Impedance DECT
Woffer FOR 17Bx

MIC In

DIGITAL

Analog

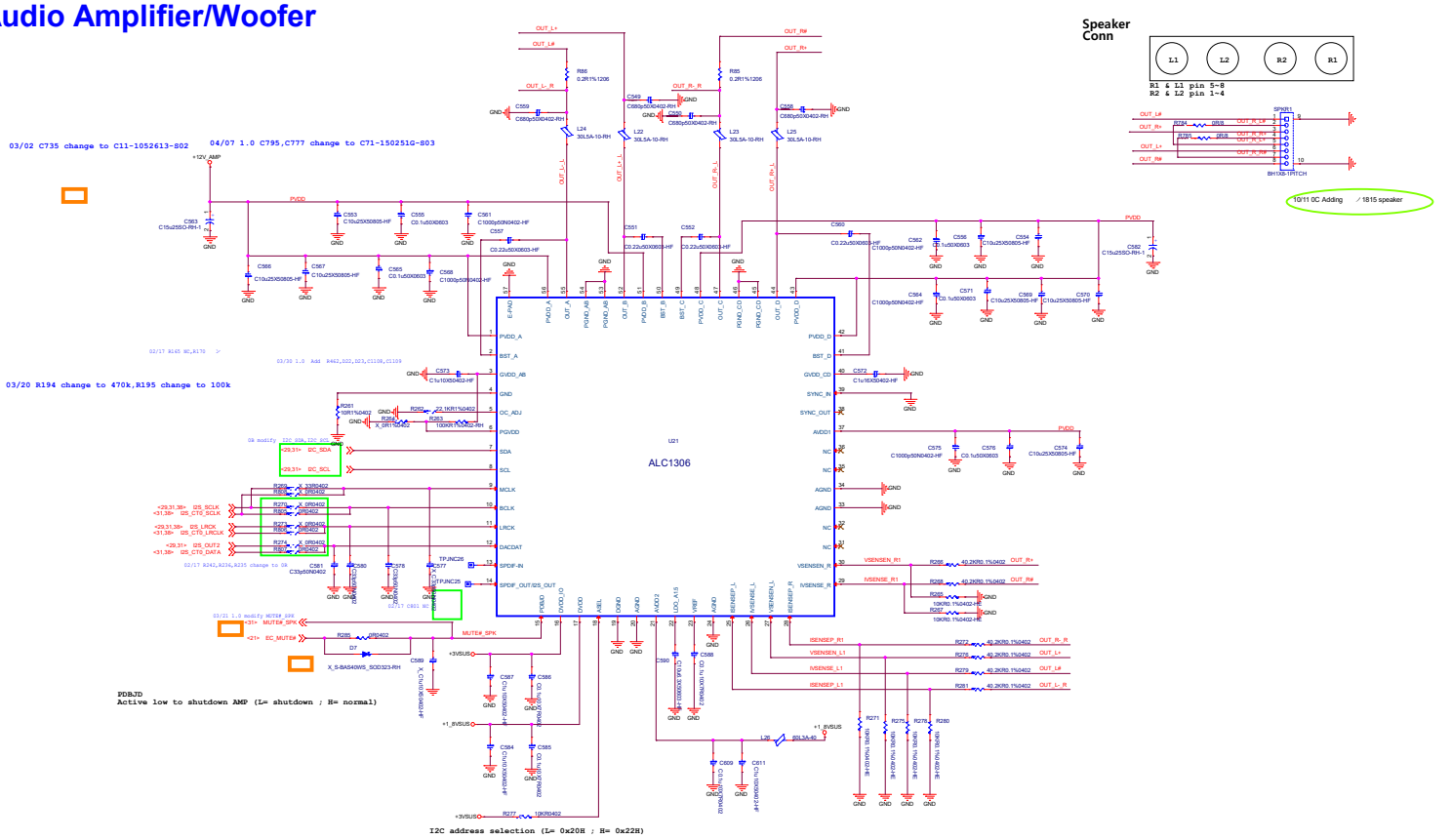
| HP_SEL | | |
|---|---|---|
| 0 | L1 / R1 | Earphone |
| 1 | L2 / R2 | Impedance |

EMI
Close Codec



| | |
|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD. |
| Title | Audio(ALC1220) |
| Size | Custom |
| Document Number | MS-18161 |
| Rev | 0D |
| Date: | Tuesday, December 05, 2017 |
| Sheet | 29 of 62 |

# Audio Amplifier/Woofer

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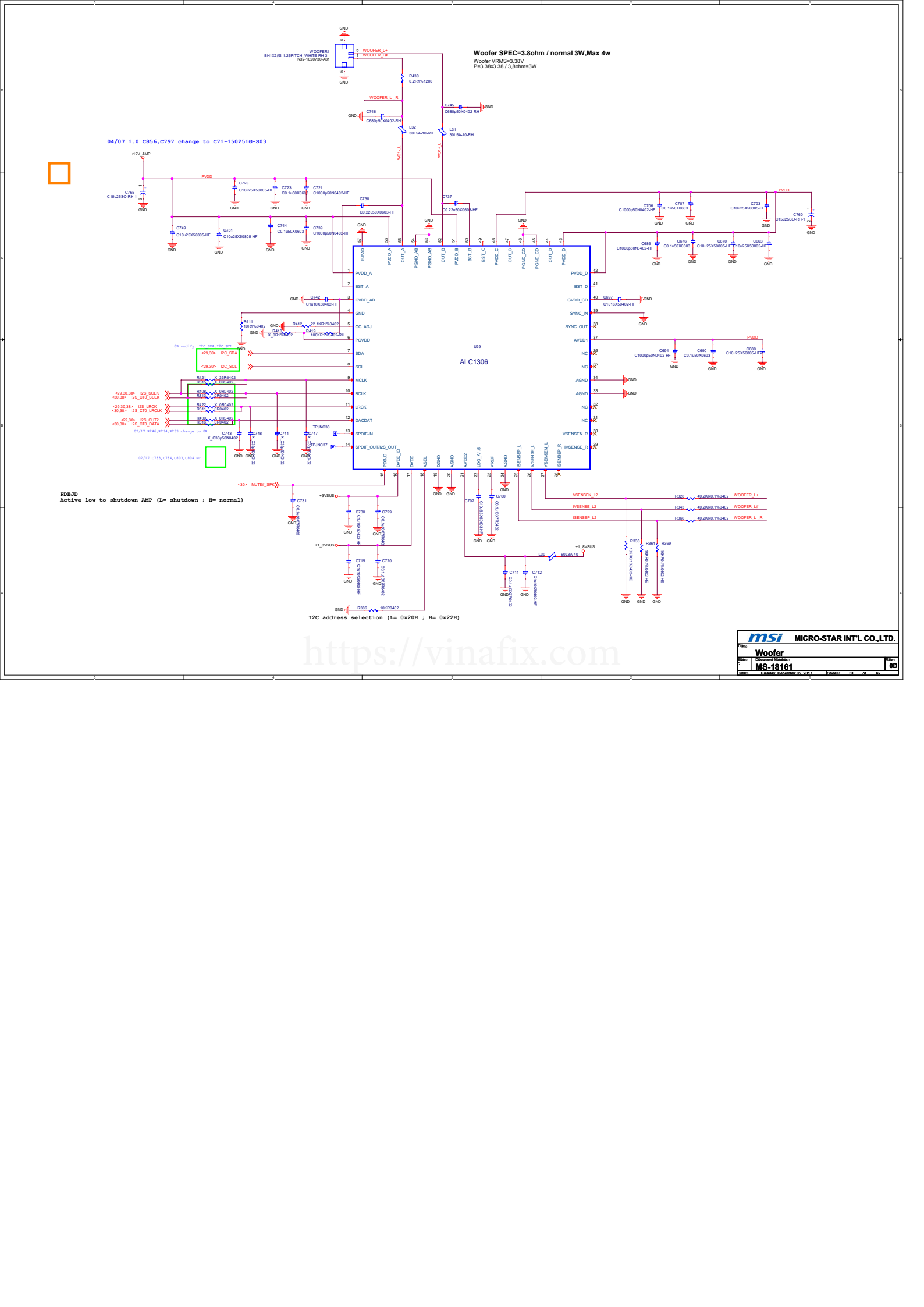
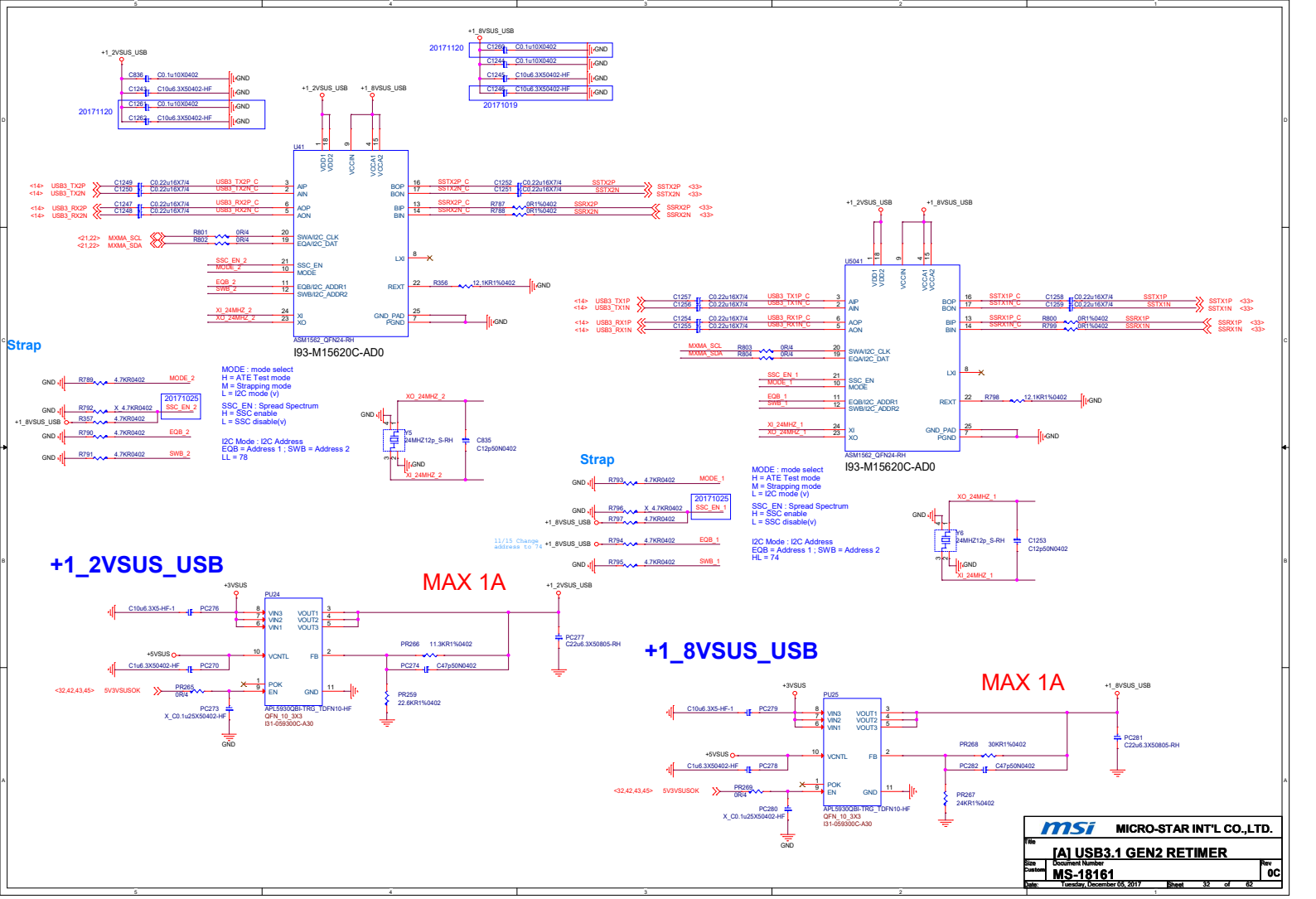
| | | | |
|---|---|---|---|
| Title | Amp(SV3H715/APA2619/APA3010) | | |
| Size | Document Number | | Rev |
| Custom | MS-18161 | | 0D |
| Date: | Tuesday, December 05, 2017 | Sheet 30 of 60 | |






## +1_2VSUS_USB

MAX 1A




## +1_8VSUS_USB

MAX 1A

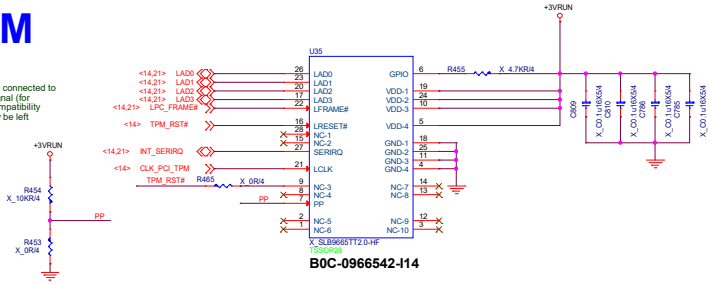





| | |
|---|---|
| MICRO-STAR INT'L CO.,LTD. | |
| Title | [A] USB3.1 GEN2 RETIMER |
| Size / Custom | Document Number: MS-18161 |
| Rev | 0C |
| Date: Tuesday, December 05, 2017 | Sheet 32 of 62 |

# TPM

Pin 9 may be connected to the Reset signal (for backward compatibility 9665) or may be left floating.

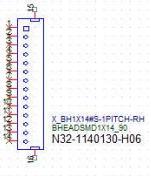



B0C-0966542-I14

For BIOS Debug Port use

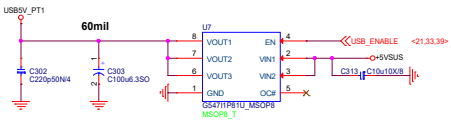

**Note:**

pin1 : LPC_FRAME#
pin2 : LAD3
pin3 : LAD2
pin4 : LAD1
pin5 : LAD0
pin6 : L_LDRQ0
pin7 : CLK_PCIF_PORT80
pin8 : INT_SERIRQ
pin9 : LPC_RST#
pin10 : +5VRUN
pin11 : +3VRUN
pin12 : GND
pin13 : NC
pin14 : GND

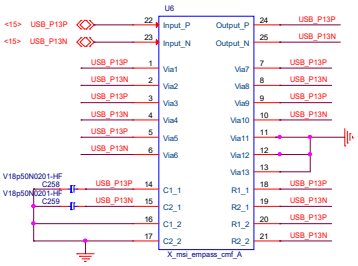


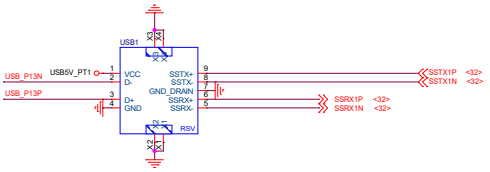

# USB3.1 Port

## MB's USB 3.1 Port-1

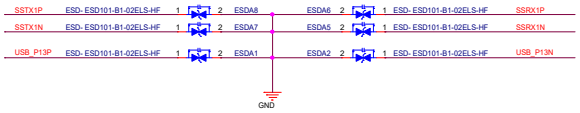



I36-5478102-G07

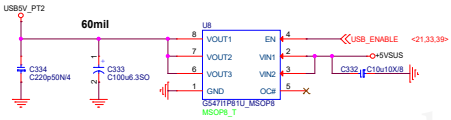


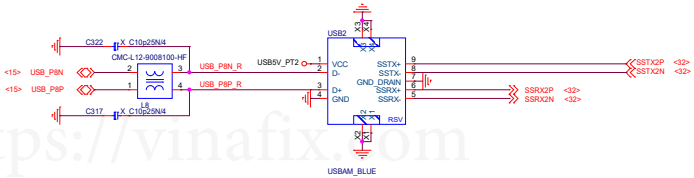

N53-09M0461-AF2



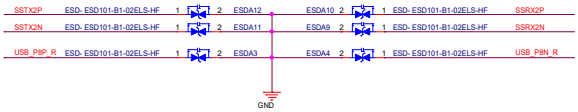

## MB's USB 3.1 Port-2




I36-5478102-G07



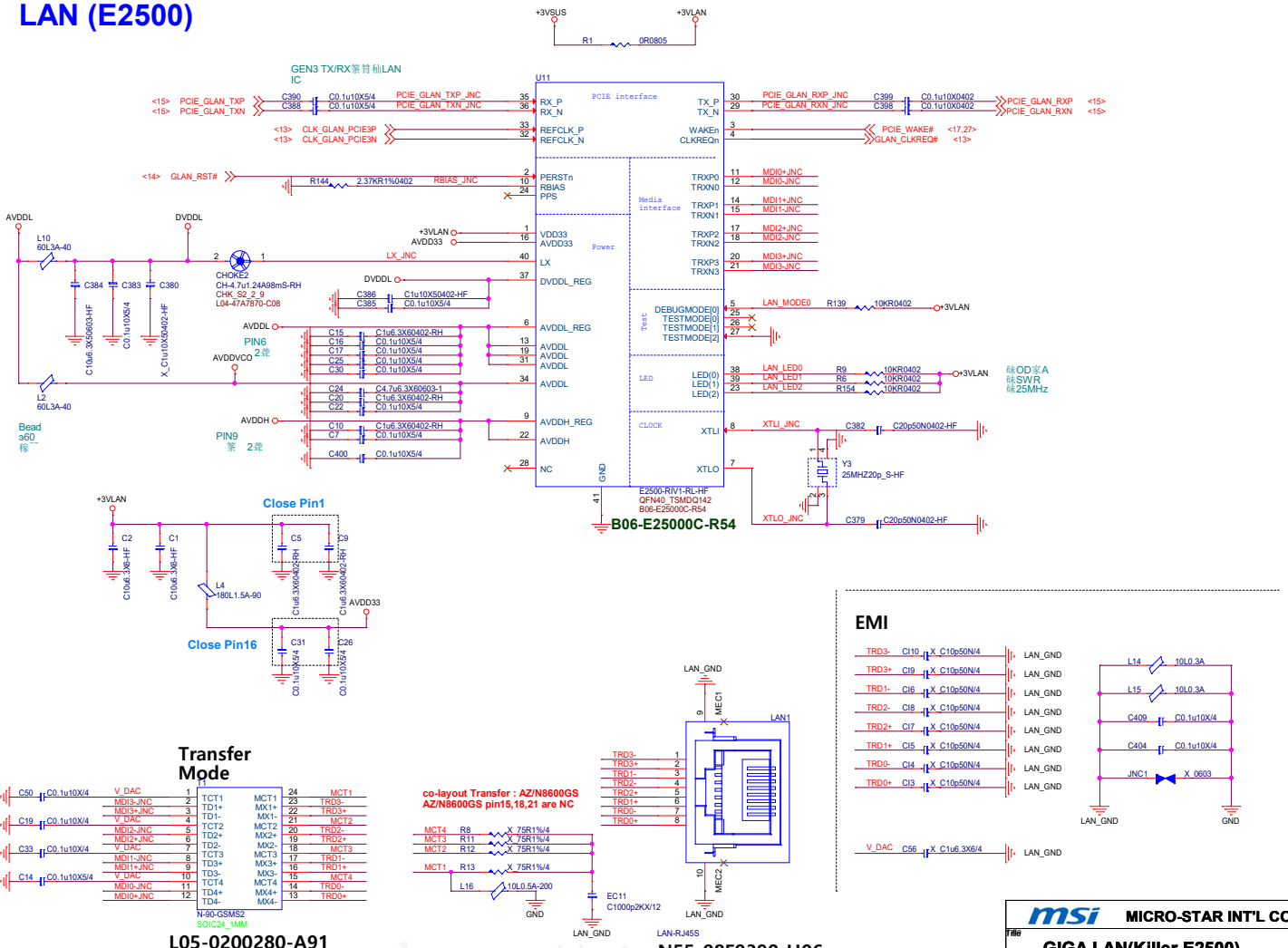

N53-09M0461-AF2






| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: TPM / USB3.0 CONN | | |
| Size | Document Number: MS-18161 | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 33 of 62 | |

# LAN (E2500)




| | | | |
|---|---|---|---|
| Title | GIGA LAN(Killer E2500) | | |
| Size: Custom | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 34 of 62 | | |

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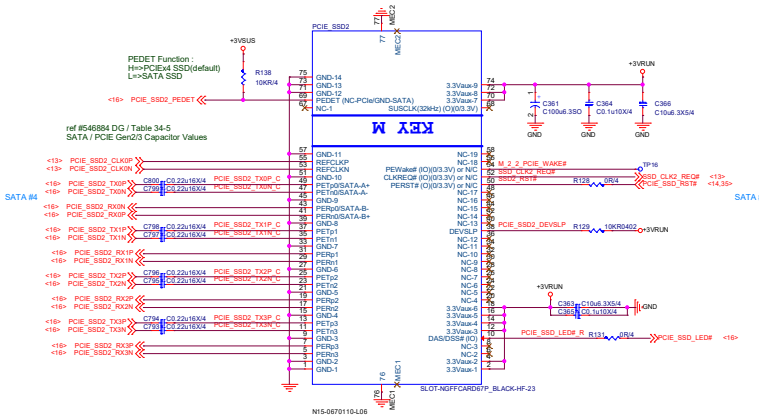
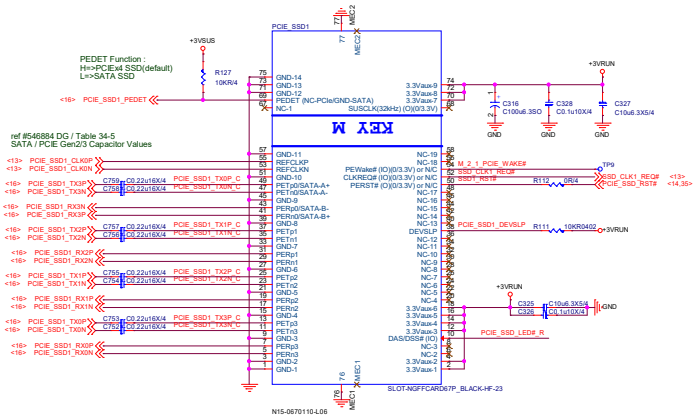
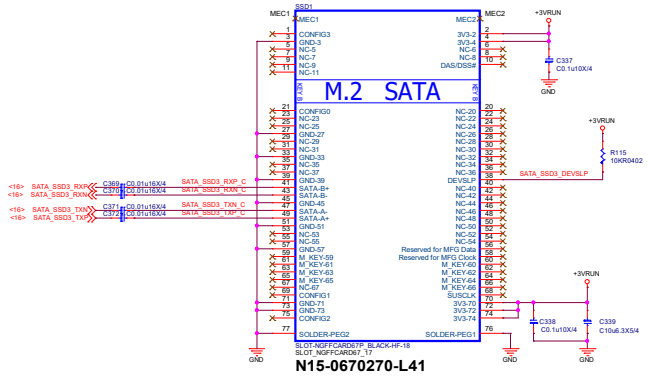
## M.2 PCIE_SSD2 (PCIEx4)




## M.2 PCIE_SSD1 (PCIEx4)

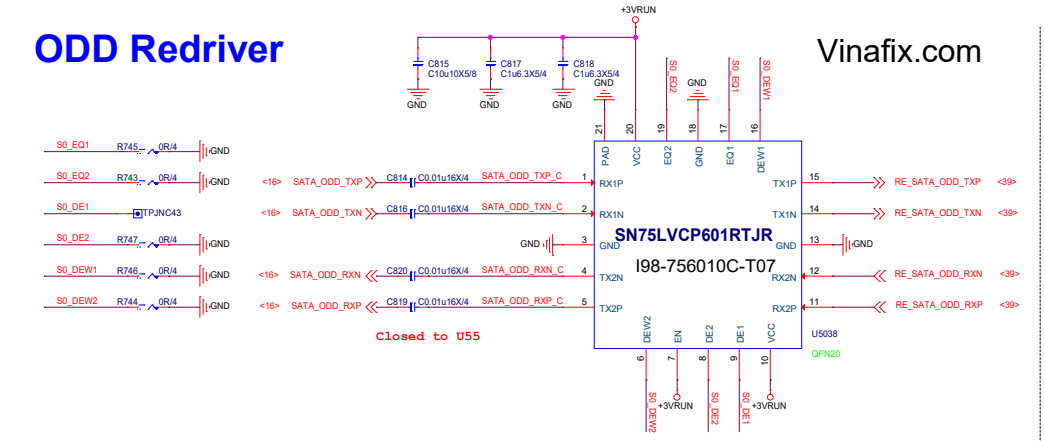



## M.2 SSD1 (SATA)




| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: PCIE M.2 SSD / SATA M2 SSD | | | |
| Size: Custom | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet: 35 | of: 62 | |

# ODD Redriver




Closed to U55

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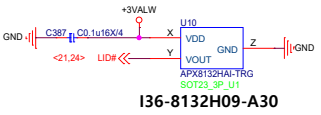
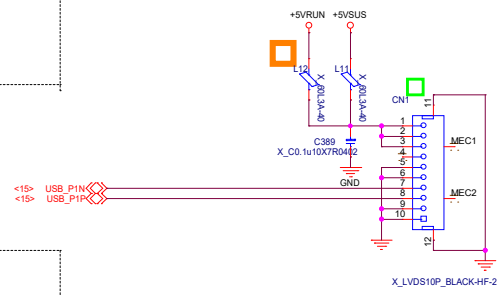
# LID

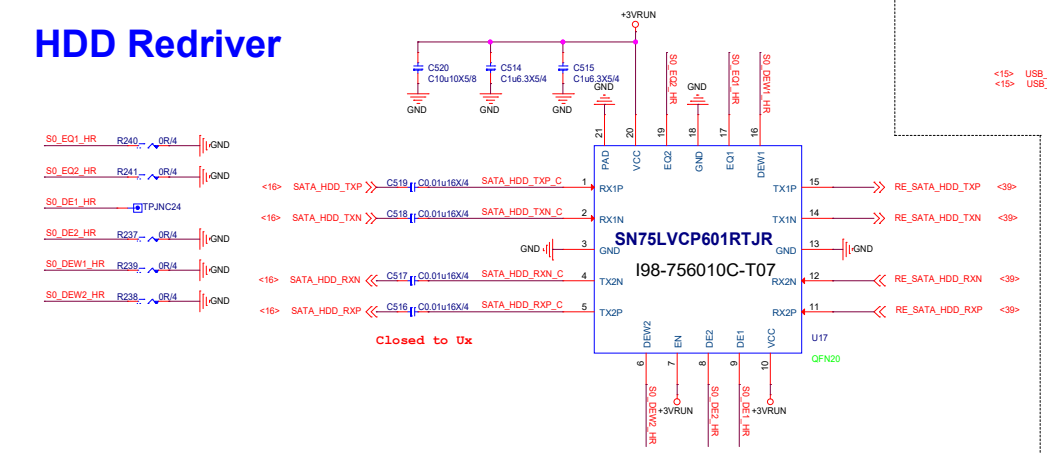



I36-8132H09-A30

# A Side LED



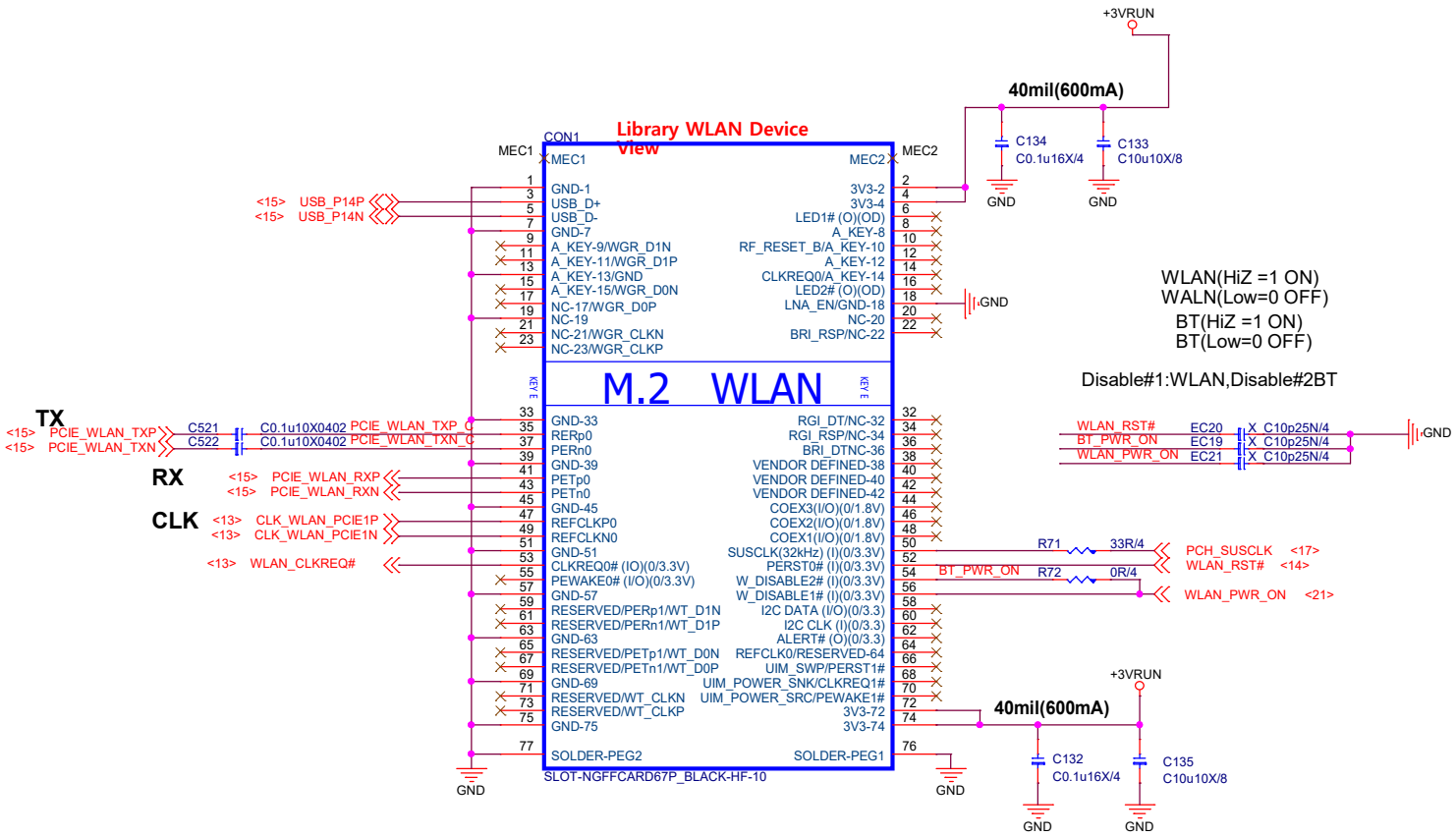

# HDD Redriver




Closed to Ux

| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: ODD,HDD Redriver/LID | | |
| Size | Document Number: MS-18161 | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet: 36 of 62 | |

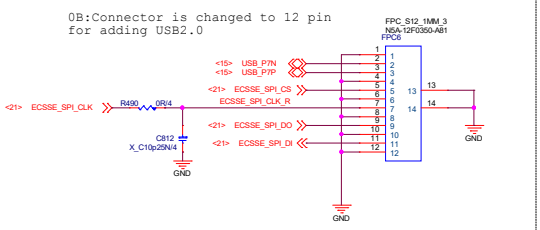
# WLAN/BT



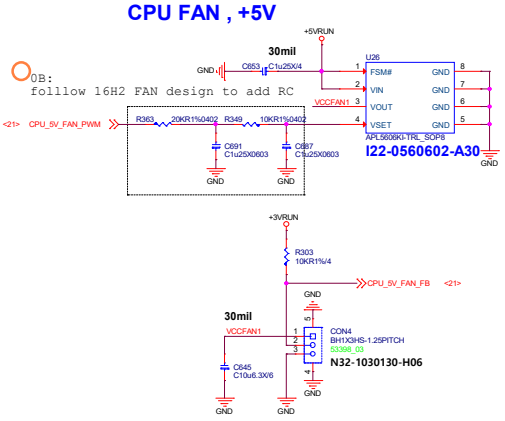



| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: WLAN/BT | | |
| Size | Document Number: MS-18161 | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 37 of 62 | |

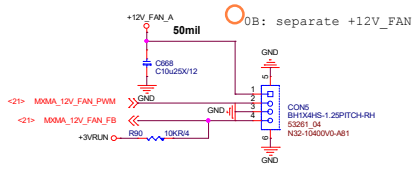
## SSE CONN (To Color Keyboard)



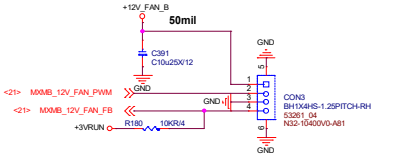

## CPU FAN , +5V



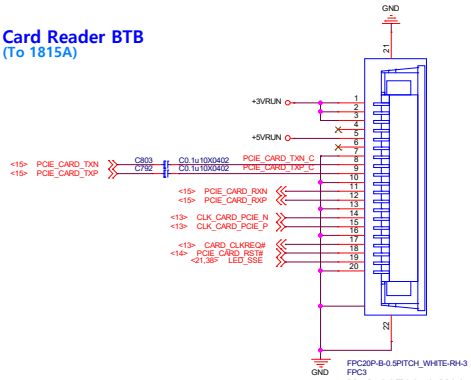

## MXMA(Master) FAN , +12V



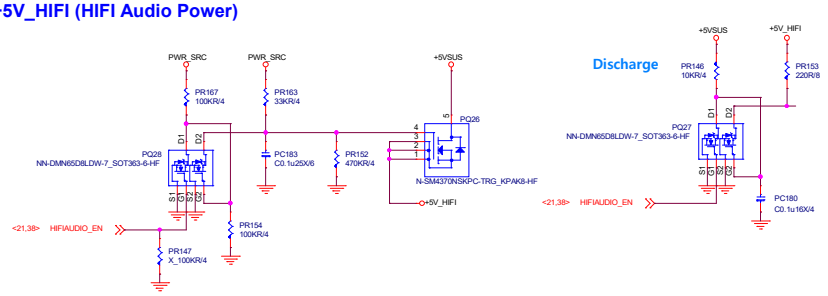

## MXMB(Slave) FAN , +12V



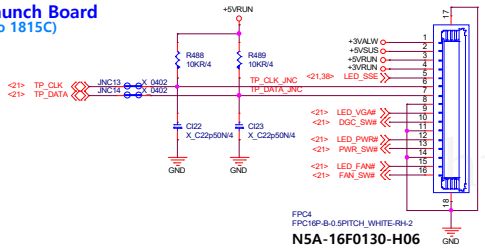

## Card Reader BTB
(To 1815A)



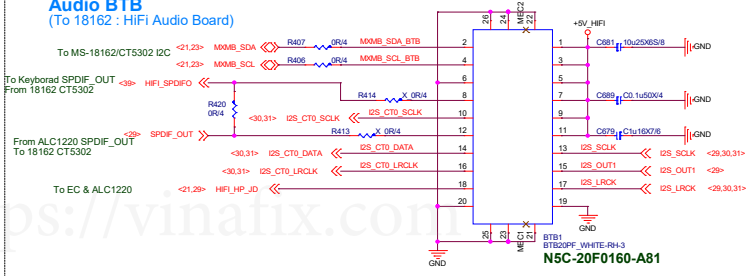

## +5V_HIFI (HIFI Audio Power)




## Launch Board
(To 1815C)



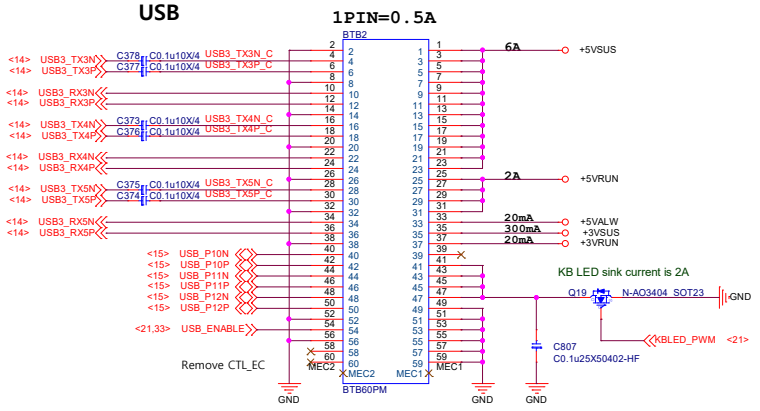

## Audio BTB
(To 18162 : HiFi Audio Board)






| | |
|---|---|
| MICRO-STAR INT'L CO.,LTD. | |
| Title | CardReader BTB/TP Conn/FANs |
| Size | Document Number: MS-18161 |
| Rev | 0D |
| Date: | Tuesday, December 05, 2017 |
| Sheet | 38 of 62 |

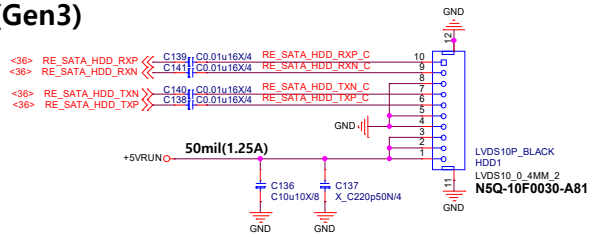
## USB




N5C-60M0110-P01

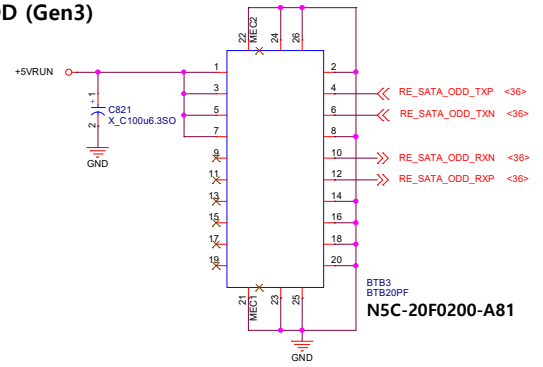
## HDD (Gen3)

1.0: change connector



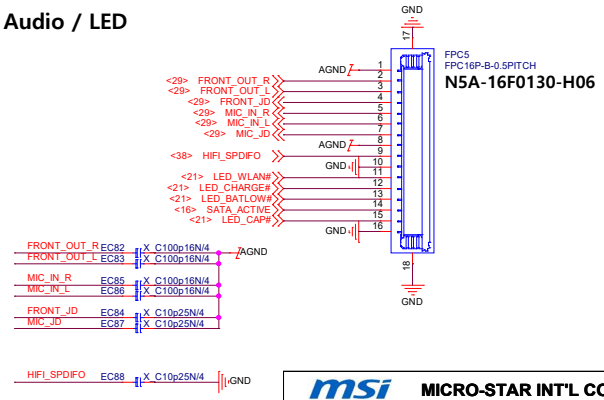

N5Q-10F0030-A81

## ODD (Gen3)




N5C-20F0200-A81

## Audio / LED



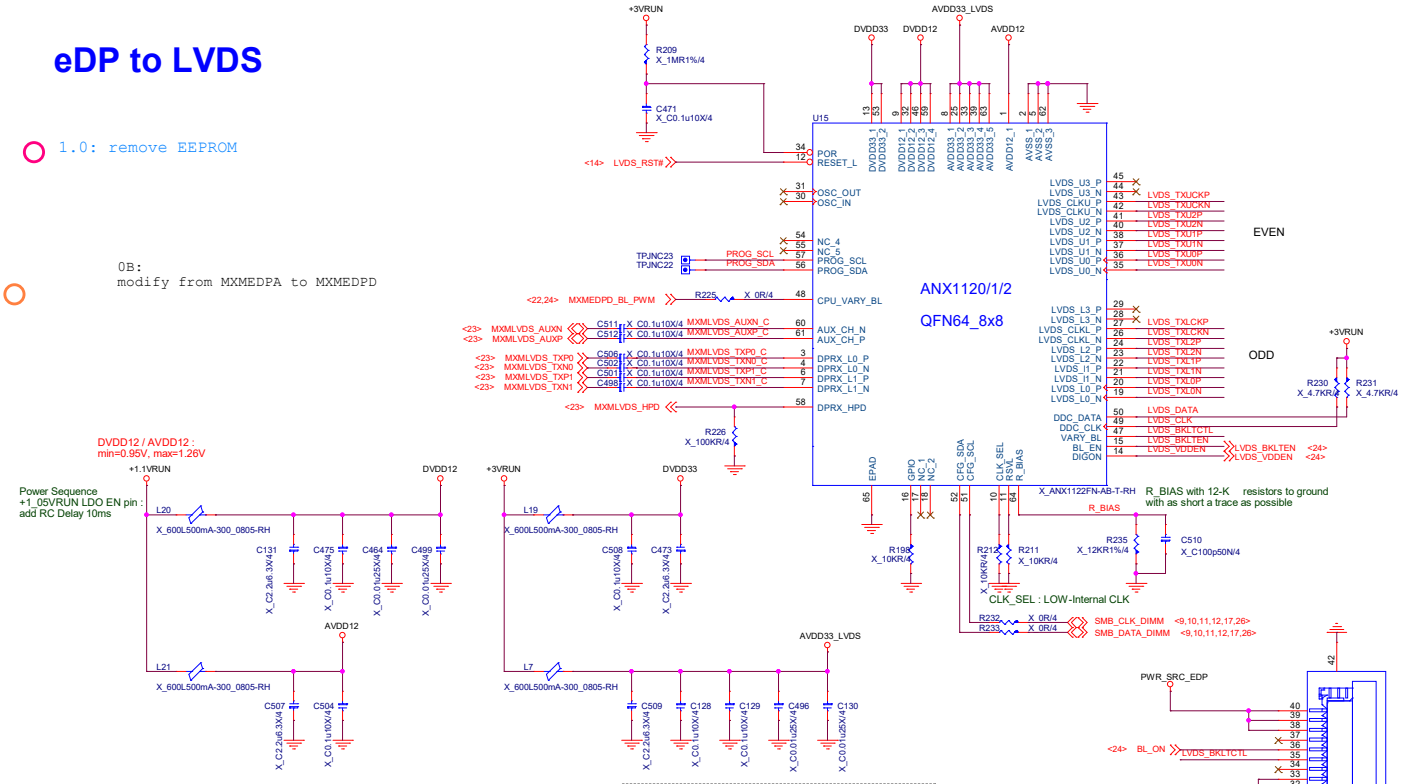

N5A-16F0130-H06

| | | | |
|---|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | | |
| Title | BTB Conn(ODD/Audio/USB/HDD) | | |
| Size | Document Number MS-18161 | | Rev 0D |
| Date: Tuesday, December 05, 2017 | Sheet 39 of 62 | | |

# eDP to LVDS

- 1.0: remove EEPROM

0B:
modify from MXMEDPA to MXMEDPD




DVDD12 / AVDD12 :
min=0.95V, max=1.26V

Power Sequence
+1_05VRUN LDO EN pin :
add RC Delay 10ms




## ANX1122 Power On Sequence

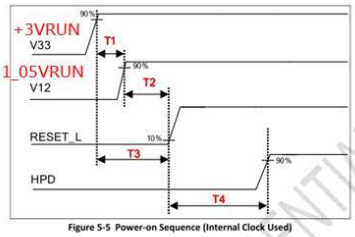
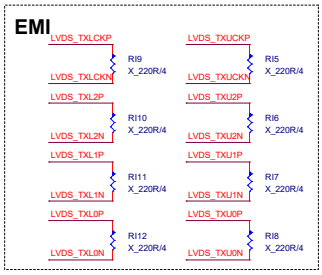


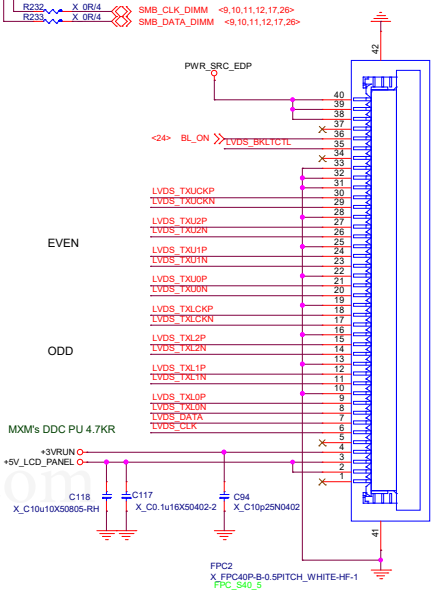

Figure 5-5 Power-on Sequence (Internal Clock Used)

Table 5-2 shows all of the delay times.

Table 5-2 Power-on Sequence Indexes

| Symbol | Min. | Max. | Unit |
|---|---|---|---|
| T1 | 1 | | ms |
| T2 | 1 | | ms |
| T3 | 2 | | ms |
| T4 | 0 | 80 | ms |

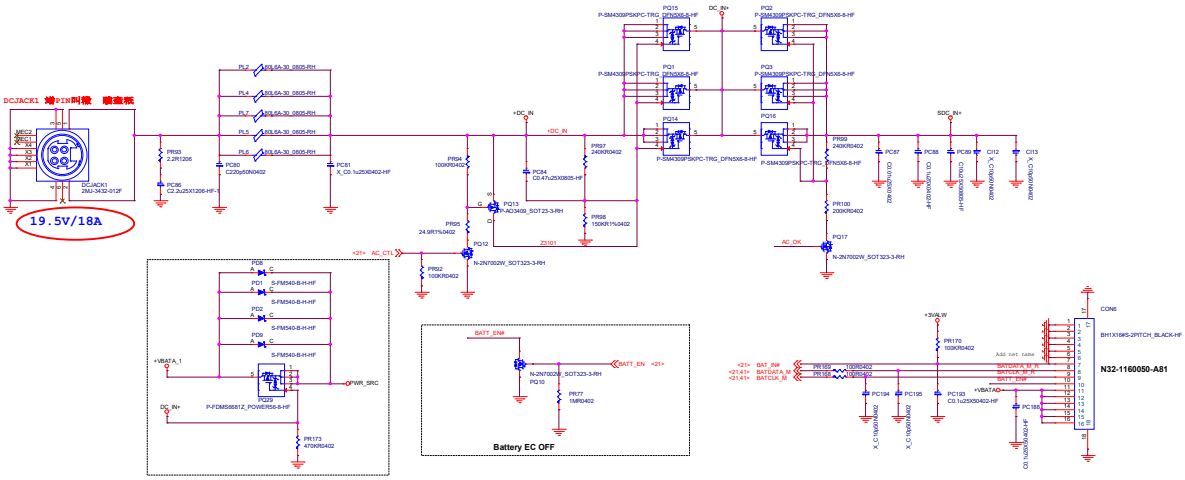


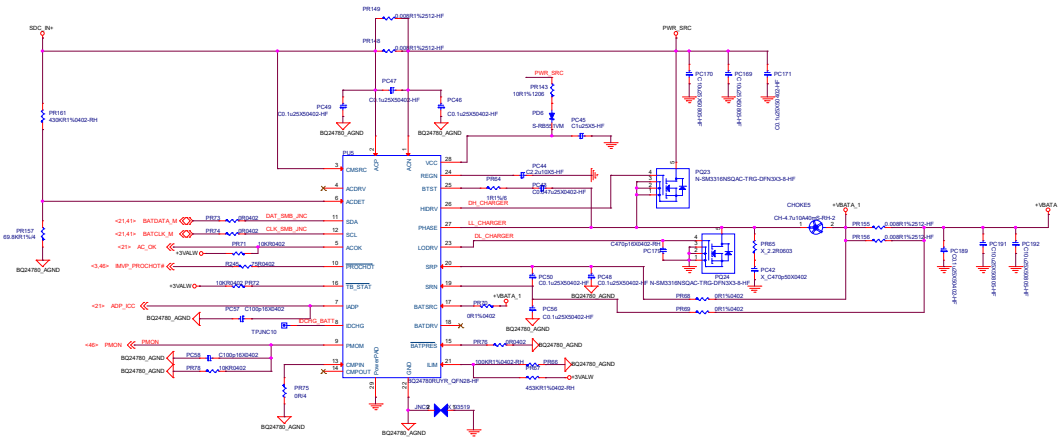



| | | | |
|---|---|---|---|
| Title | eDP to LVDS(ANX1122) | | |
| Size: Custom | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 40 of 62 | | |

## Battery Select

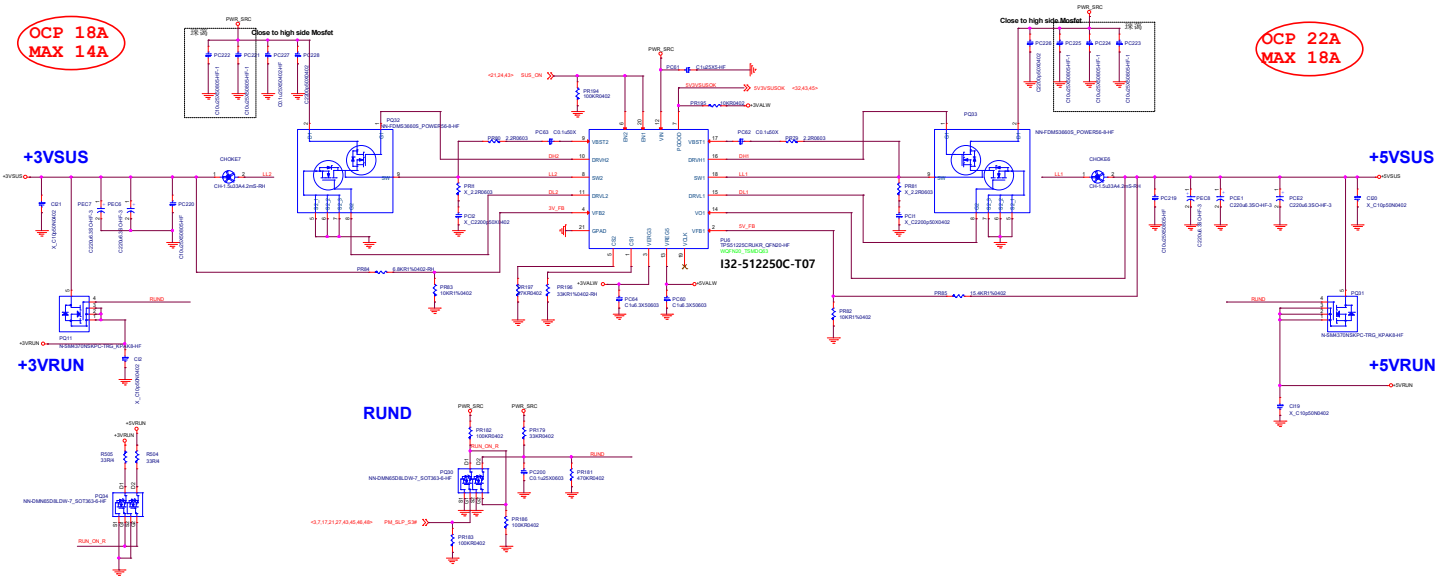



## Battery Charger




| | | | |
|---|---|---|---|
| msi MICRO-STAR INT'L CO.,LTD. | | | |
| Title: Battery select/Charger | | | |
| Size: | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 41 of 60 | | |

# System Power






MICRO-STAR INT'L CO.,LTD.

System Power

MS-18161

0D

Tuesday, December 05, 2017

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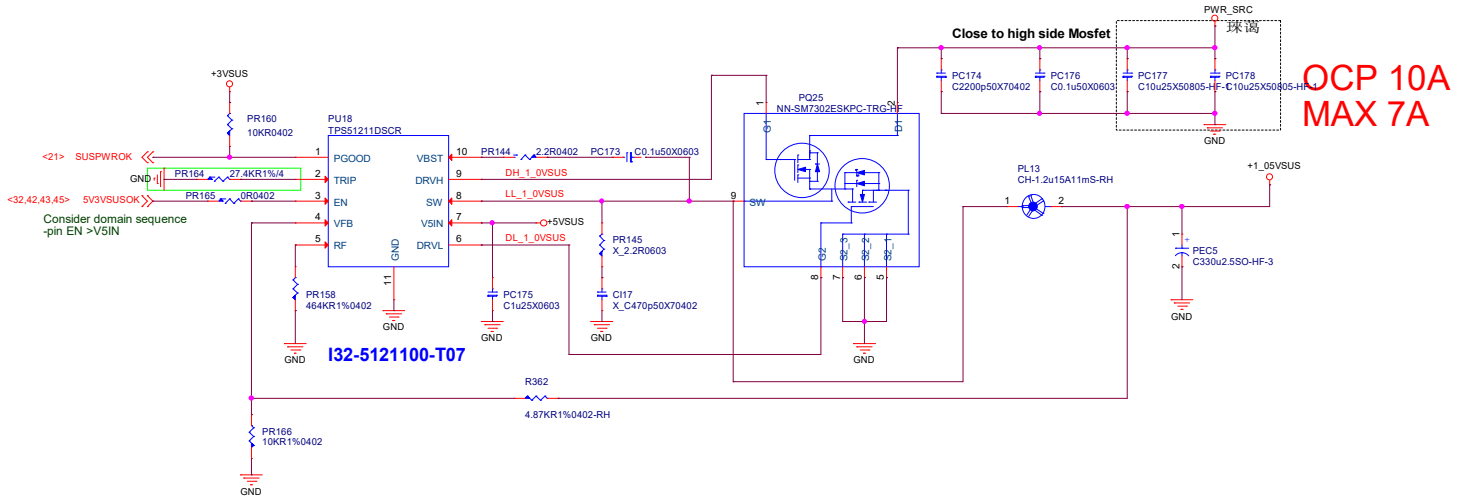
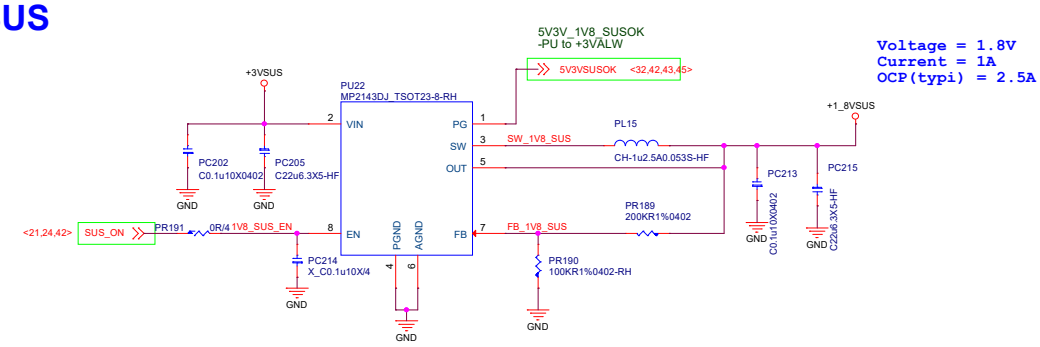
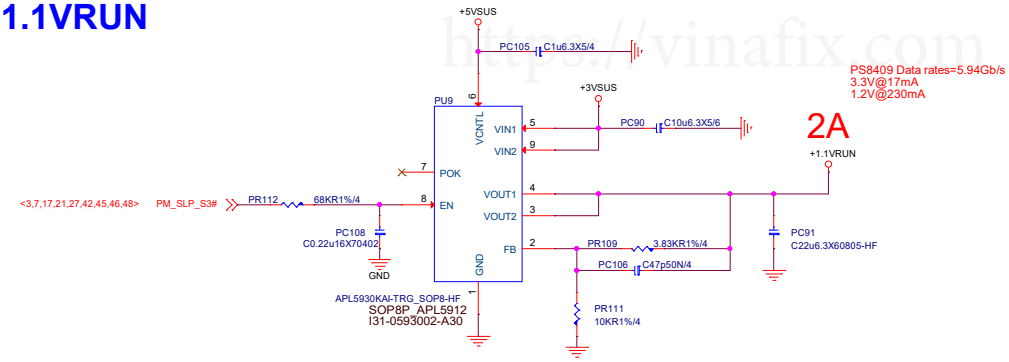
# +1_05VSUS




# +1_8VSUS



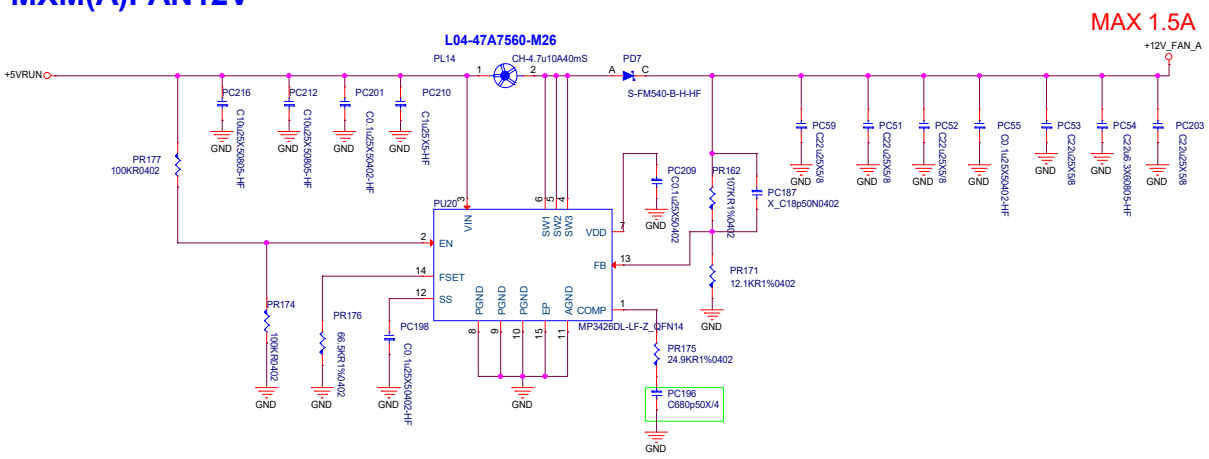

# +1.1VRUN



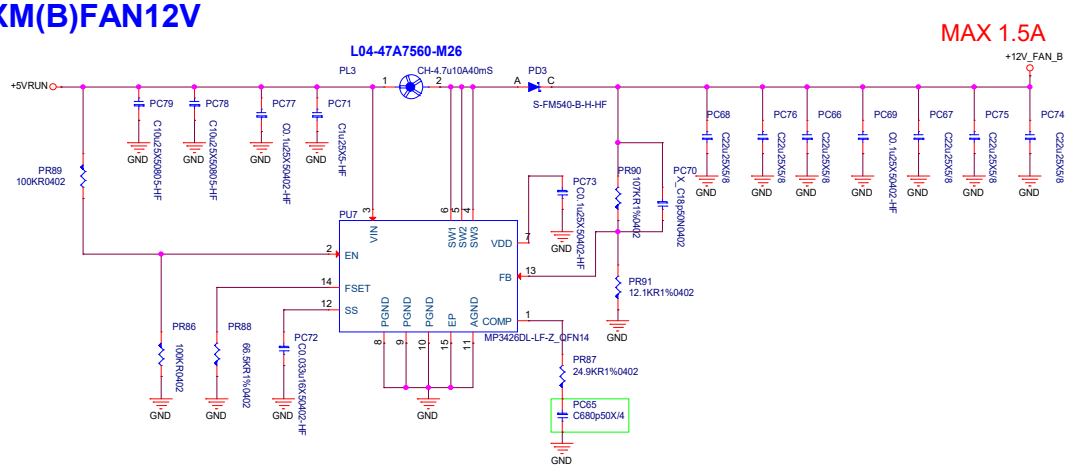



| | | |
|---|---|---|
| Title | +1_05VSUS/+1_8VSUS/+1.1VRUN | |
| Size: Custom | Document Number: MS-18161 | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 43 of 62 | |

# MXM(A)FAN12V

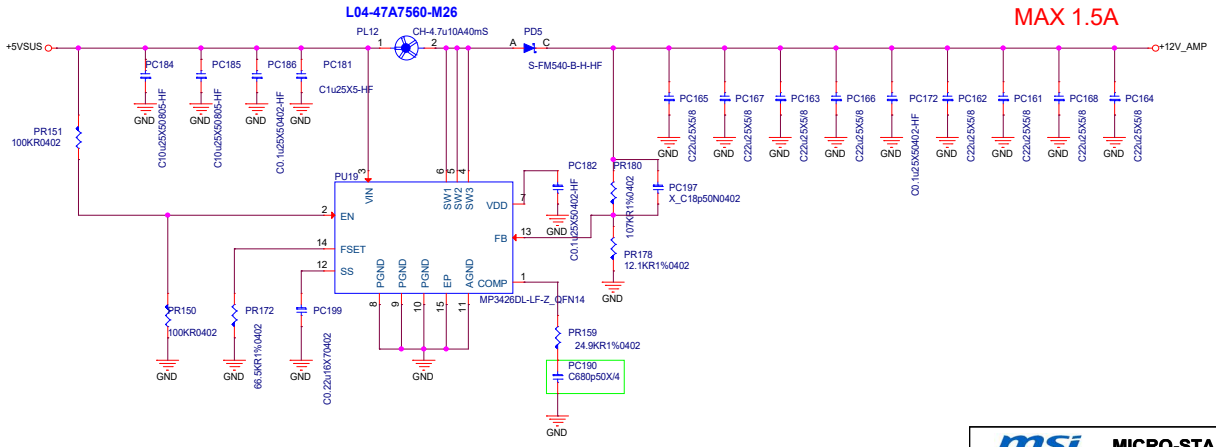



# MXM(B)FAN12V



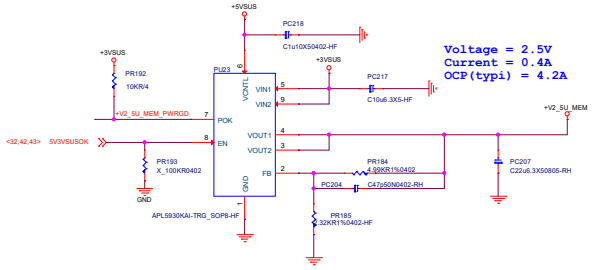



# Audio Amp 12V

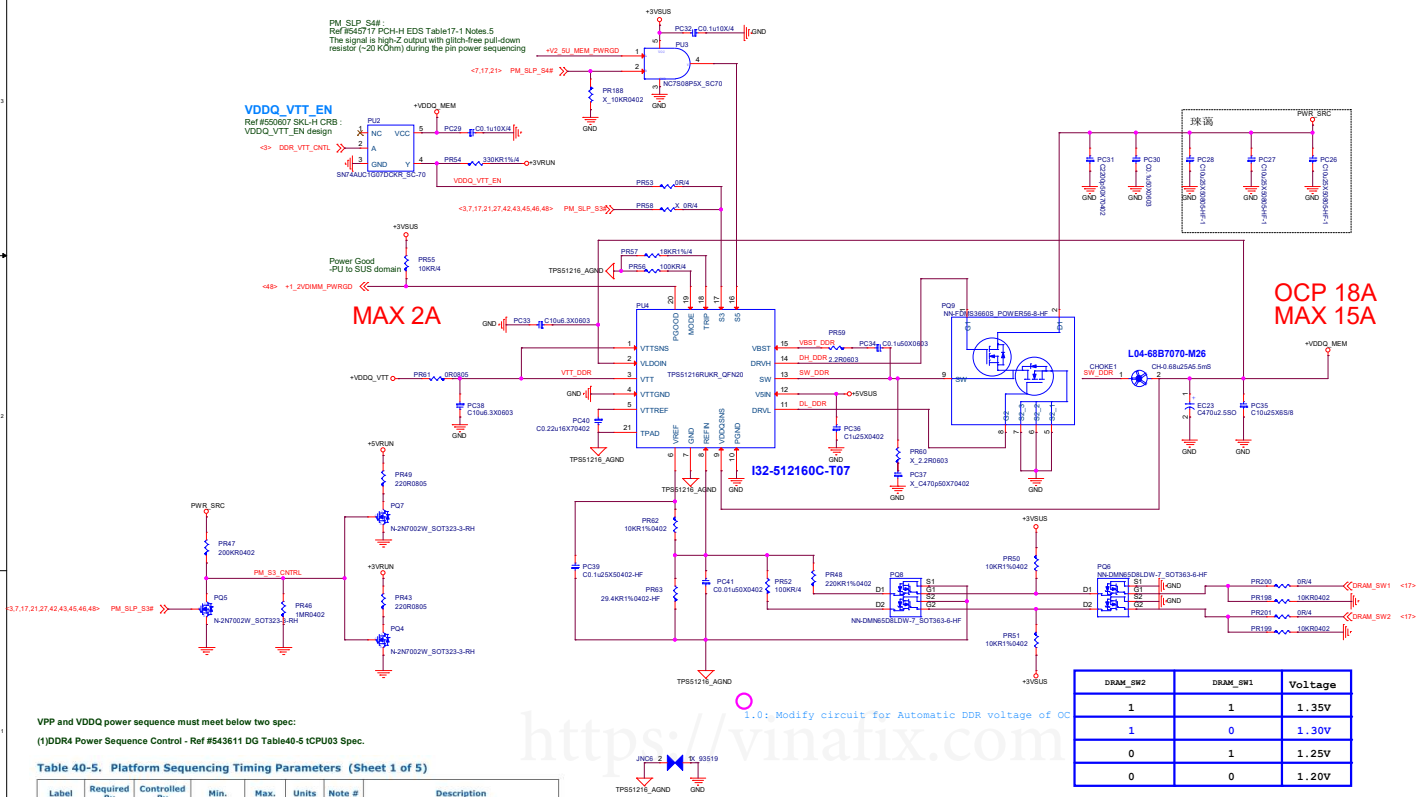



| | | | |
|---|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | | |
| Title: | FAN/+12V_AMP | | |
| Size: | Document Number: MS-18161 | | Rev: 0D |
| Date: | Tuesday, December 05, 2017 | Sheet: 44 of 62 | |

# +V2_5U_MEM (DDR4/Vpp : 2.5V)




# +VDDQ_MEM(1.2V) & +VDDQ_VTT(0.6V)




| DRAM_SW2 | DRAM_SW1 | Voltage |
|---|---|---|
| 1 | 1 | 1.35V |
| 1 | 0 | 1.30V |
| 0 | 1 | 1.25V |
| 0 | 0 | 1.20V |

1.0: Modify circuit for Automatic DDR voltage of OC

**VPP and VDDQ power sequence must meet below two spec:**

**(1)DDR4 Power Sequence Control - Ref #543611 DG Table40-5 tCPU03 Spec.**

**Table 40-5. Platform Sequencing Timing Parameters (Sheet 1 of 5)**

| Label | Required By | Controlled By | Min. | Max. | Units | Note # | Description |
|---|---|---|---|---|---|---|---|
| tCPU03 | CPU | PLT | | 25 | ms | 26 | VDDQ ramping and stable before VCCST stable |

**(2)VPP>VDDQ ; DDR4 Spec : VPP must be greater than or equal to VDD at all times.**



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| | | |
|---|---|---|
| Title: DDR4 Power | | |
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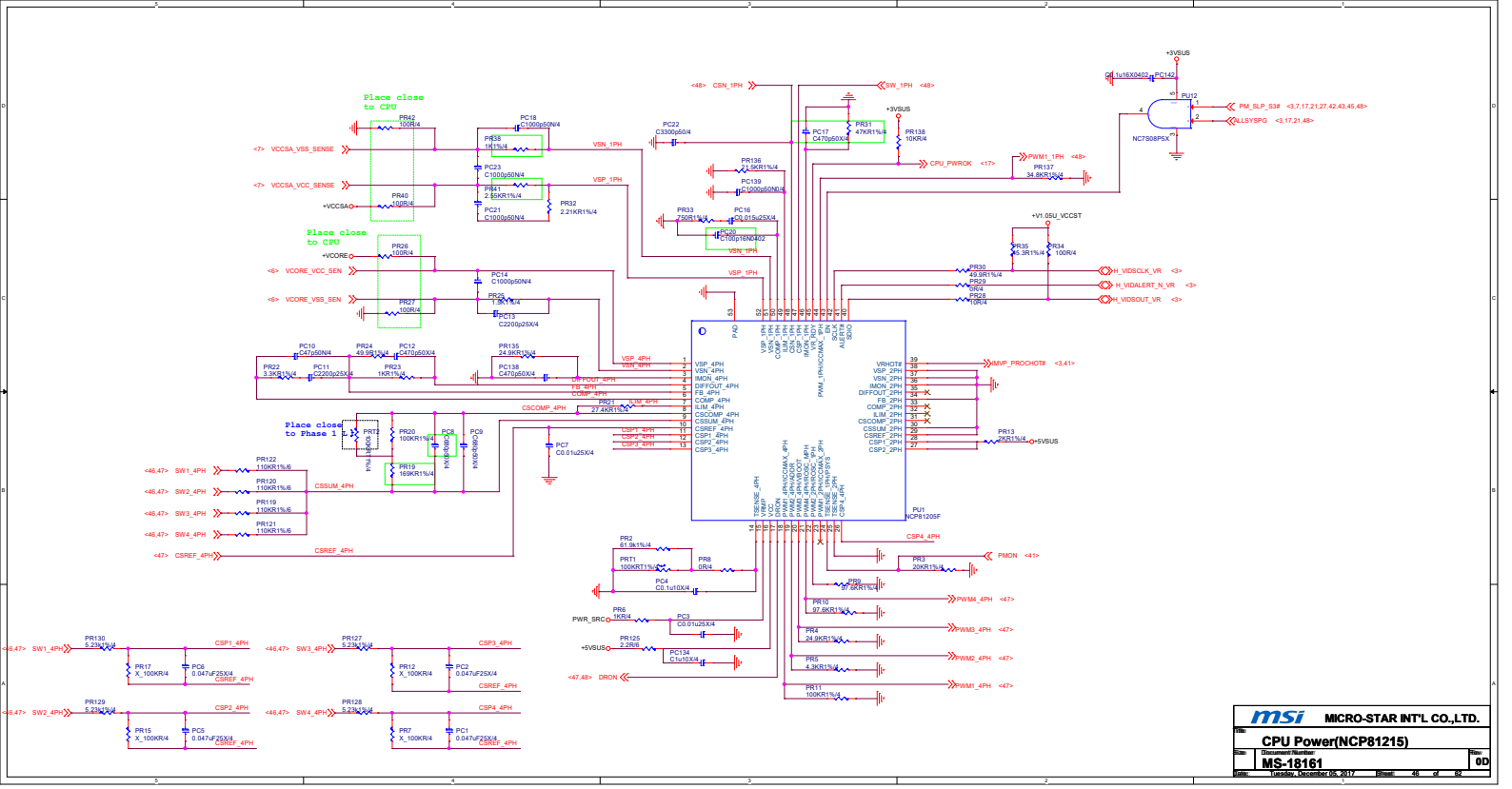
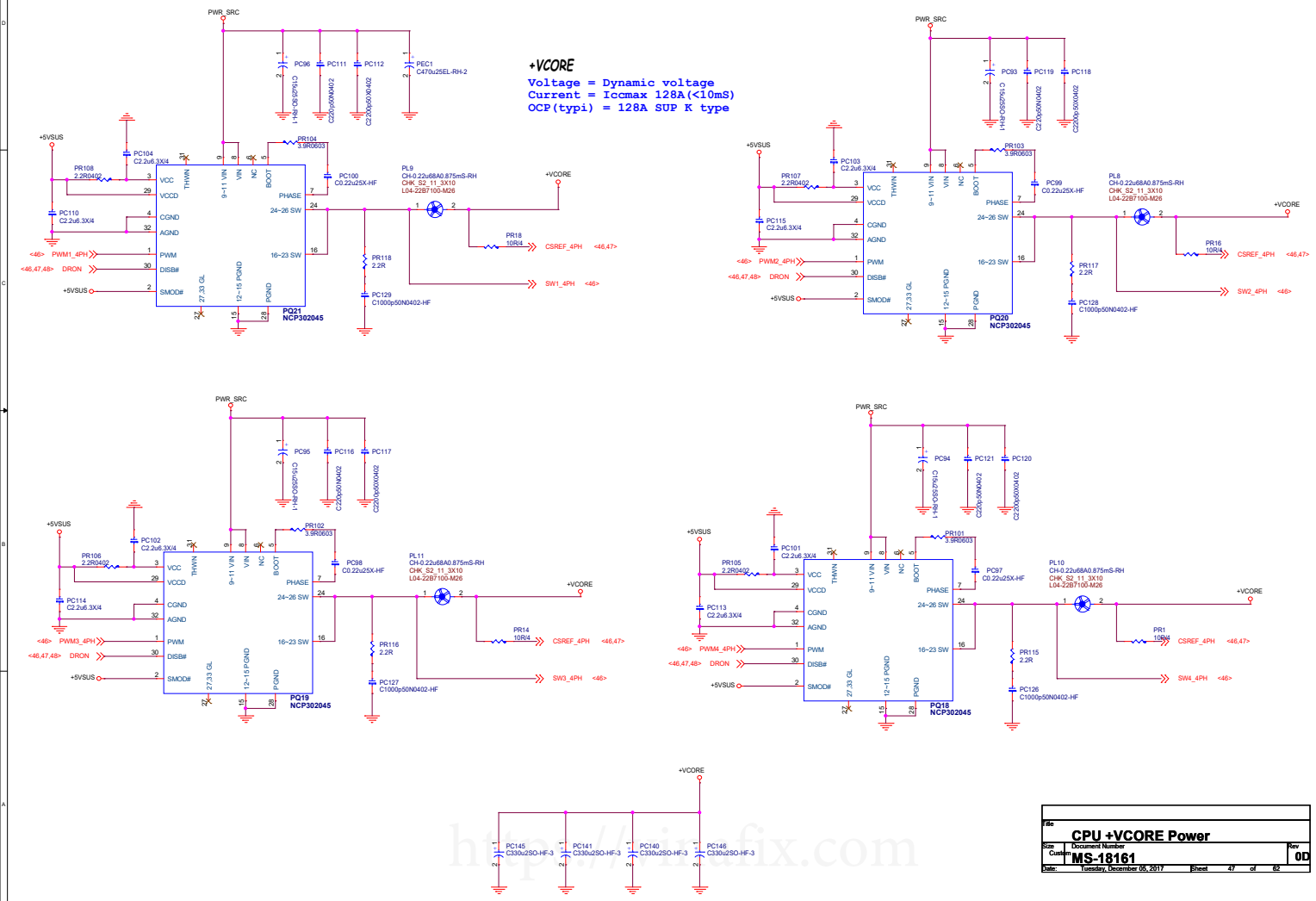


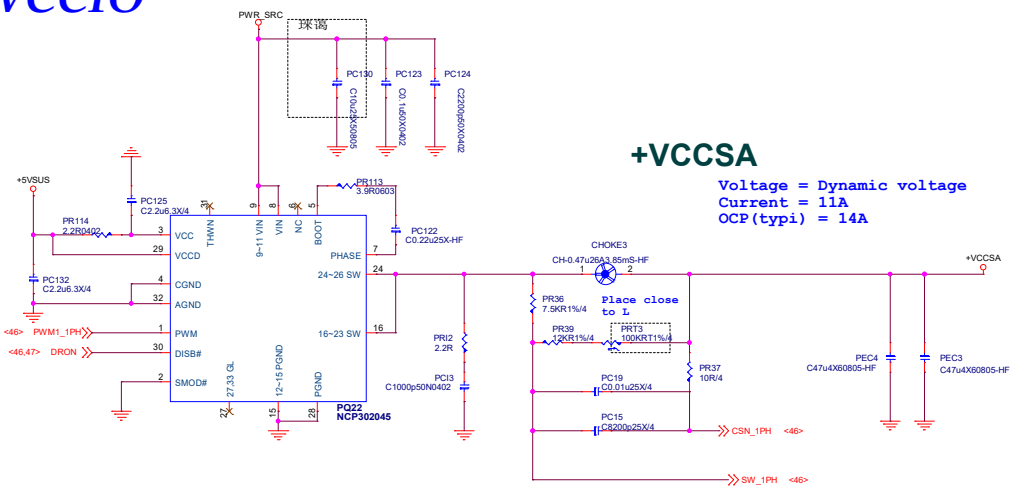
# *Coffee lake H-line*
# *45W IA Core*






| | | | |
|---|---|---|---|
| Title | CPU +VCORE Power | | |
| Size: Custom | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 47 of 62 | | |

# Skylake H-line 42 45W SA Core & VCCIO

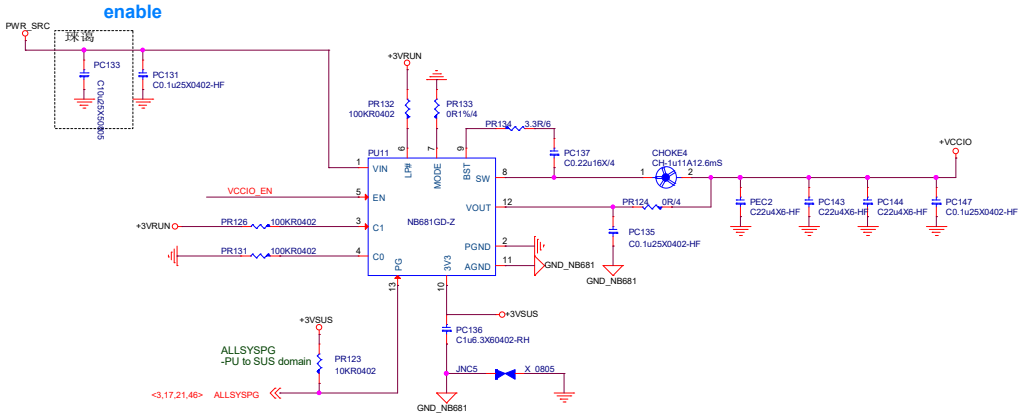



## +VCCSA

Voltage = Dynamic voltage
Current = 11A
OCP(typi) = 14A

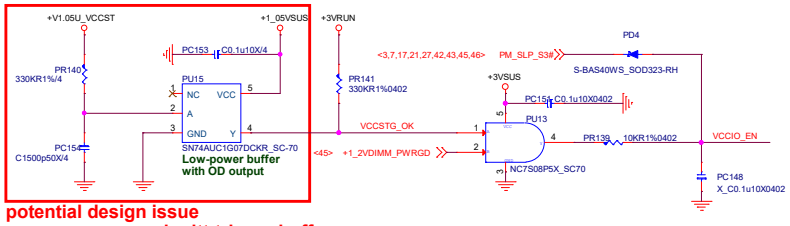
## CPU Core Power VCCIO 0.95V

C0 enable SLP# enable




## VCCIO_EN

Ref #546884 DG Figure 40-4 Notes.14
VCCIO, VCCSA must ramp after VccST, VCCSTG, and VDDQ have completed their ramps.




potential design issue
-remove or use schmitt-trigger buffer

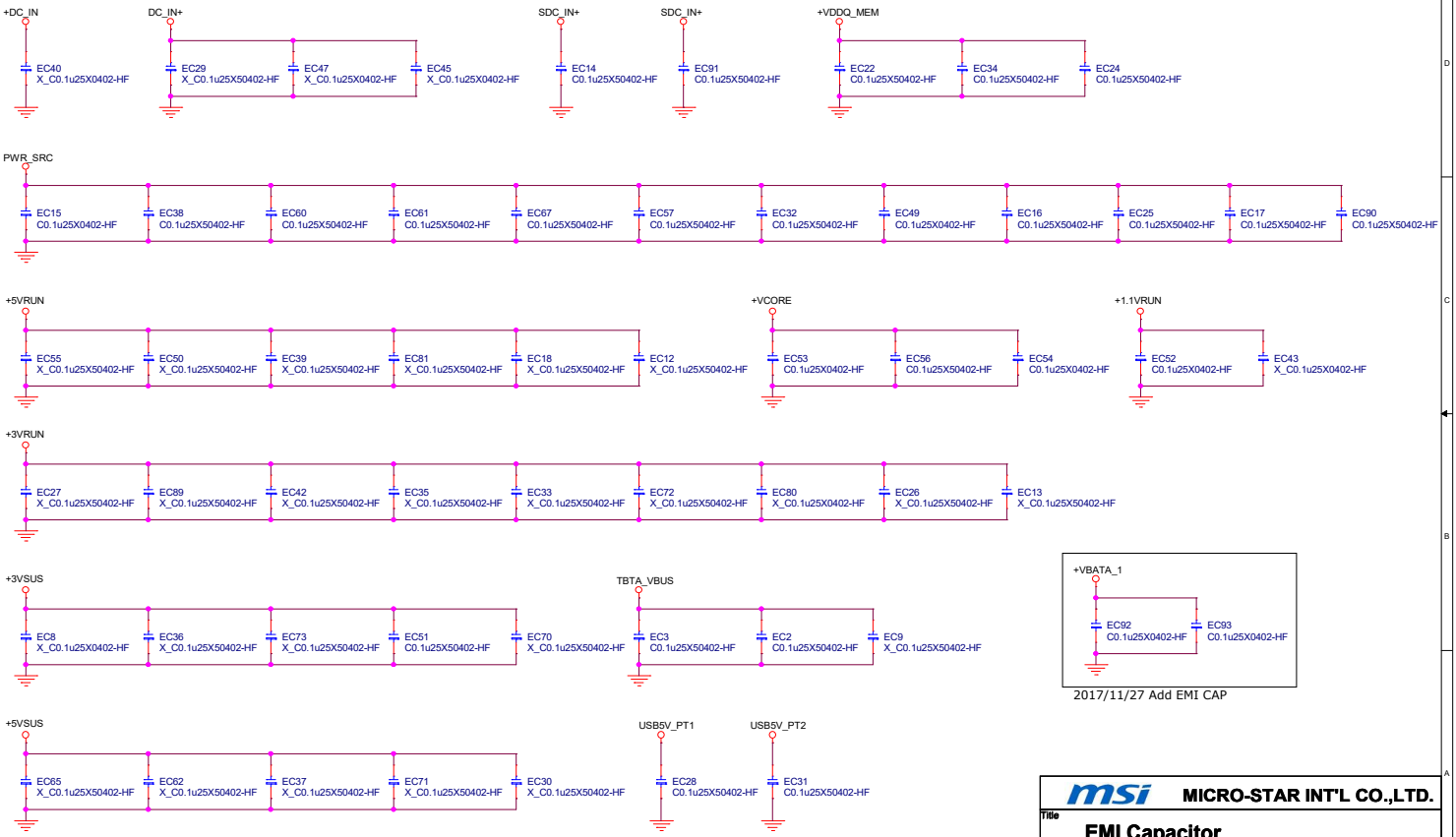
**Table 40-5. Platform Sequencing Timing Parameters (Sheet 1 of 5)**

| Label | Required By | Controlled By | Min. | Max. | Units | Note # | Description |
|---|---|---|---|---|---|---|---|
| tCPU05 | CPU | PLT | 100 | | ns | | VDDQ ramping and stable before VCCSA/ VCCIO ramps |
| tCPU06 | CPU | PLT | 100 | | ns | 27 | VCCST ramping and stable before VCCSA/ VCCIO ramps. |



| | | | |
|---|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | | |
| Title: | CPU Power(+VCCSA/+VCCIO) | | |
| Size: | Document Number: MS-18161 | | Rev: 0D |
| Date: | Tuesday, December 05, 2017 | Sheet: 48 of 62 | |

# EMI Cap




2017/11/27 Add EMI CAP

MICRO-STAR INT'L CO.,LTD.

| | | |
|---|---|---|
| Title | EMI Capacitor | |
| Size | Document Number: MS-18161 | Rev: 0D |
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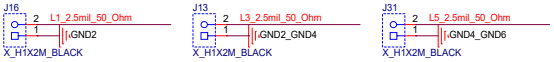
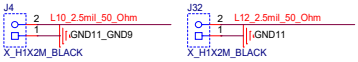
# Impedence

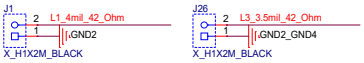
## Impedence Connector No
## PN

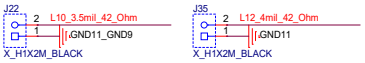
50 ohm



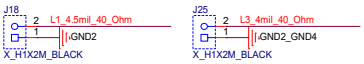



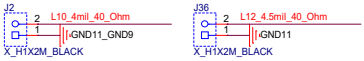

42 ohm



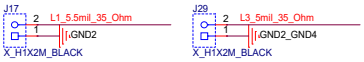



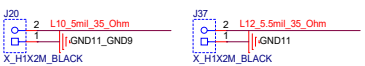

40 ohm



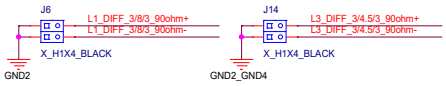



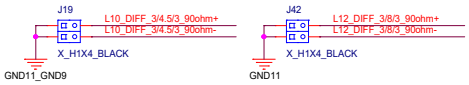

35 ohm



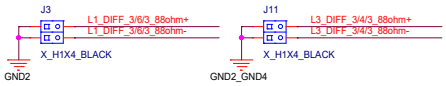



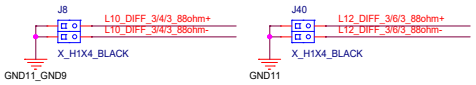

90 ohm



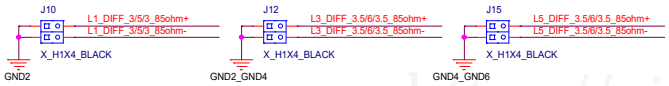



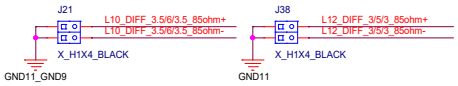

88 ohm



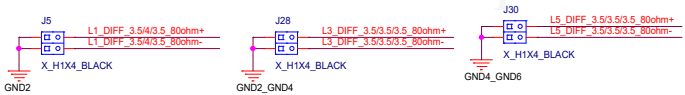



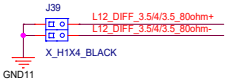

85 ohm



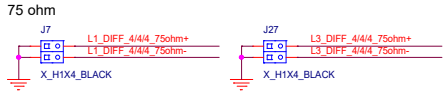



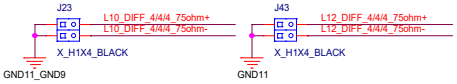

80 ohm




75 ohm






| | | |
|---|---|---|
| Title | Impedence | |
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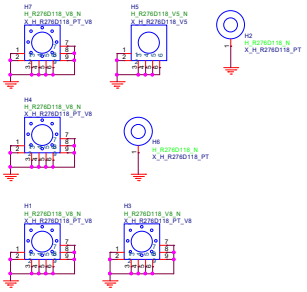
## Screw Hole



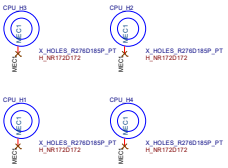
## SSD Stand Off

E2B-1812010-A89

## WLAN Stand off

E2B-1781010-A89

## CPU Hole



## CPU Bracket

60項

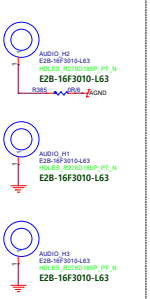
307-8160111-A89

## PCH HEATSINK

60項

E31-0403231-TA9

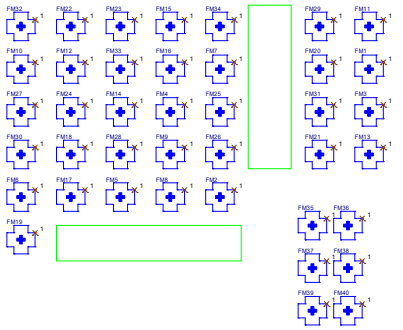
## Audio Stand Off*3



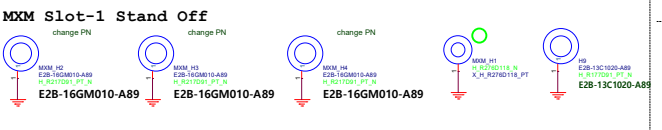
E2B-16F3010-L63

E2B-16F3010-L63

E2B-16F3010-L63



## MXM Slot-1 Stand Off



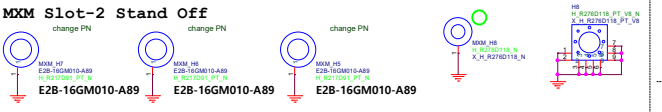
E2B-16GM010-A89

E2B-16GM010-A89

E2B-16GM010-A89

E2B-13C1020-A89

## MXM Slot-2 Stand Off

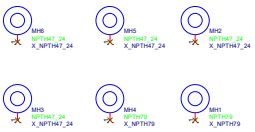


E2B-16GM010-A89

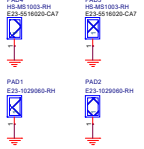
E2B-16GM010-A89

E2B-16GM010-A89

## Hole



## EMI Spring



## USB(MB) Gasket

60項

E2Y-X013211-CA7

## HDMI Gasket

60項

E2Y-X027011-CA7

## RJ45 Mylar

60項

E2P-8123221-G40

## DP Gasket

60項

E2Y-X007911-CA7

## Type C Gasket

60項

E2Y-X011311-CA7

PD0-181610D-H73

(擋　痴紋)

PD0-181610D-T53 廠供

## MP stage to stuff

60項

Y01-RHDMI03-000

60項

G51-N1CO041-A09

## ODD Stand off

E2B-1634020-L63

E2B-1634020-L63

| MICRO-STAR INT'L CO.,LTD. | | |
|---|---|---|
| Title: Screw/ME | | |
| Size: | Document Number: MS-18161 | Rev: 0D |
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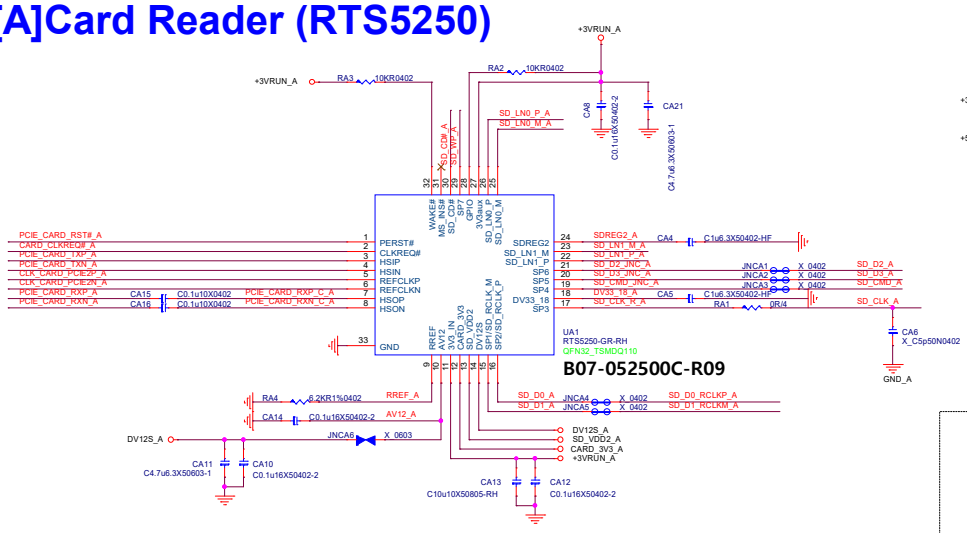
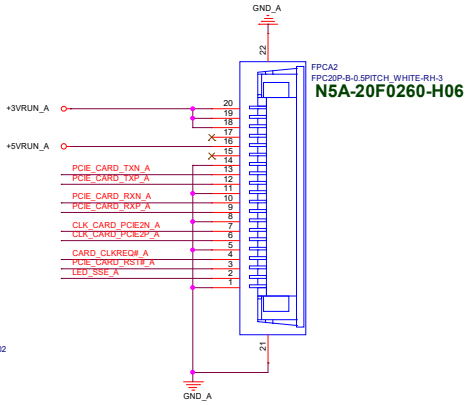
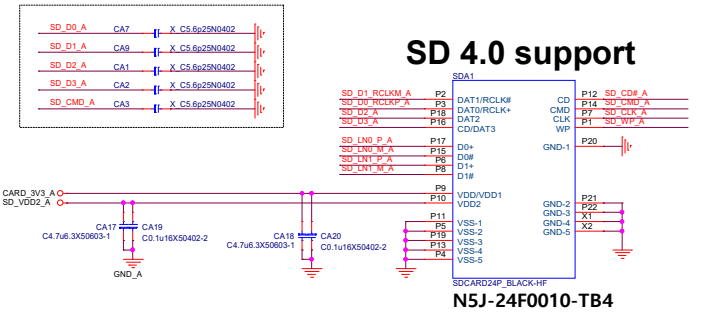
# [A]Card Reader (RTS5250)

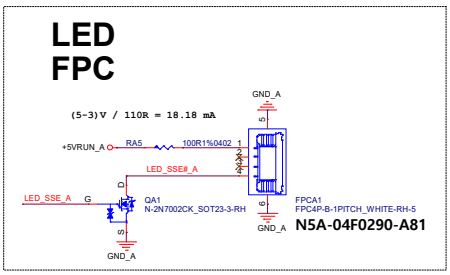


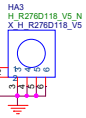

## SD 4.0 support





PD0-1816A0D-H73
PD0-1816A0D-T53

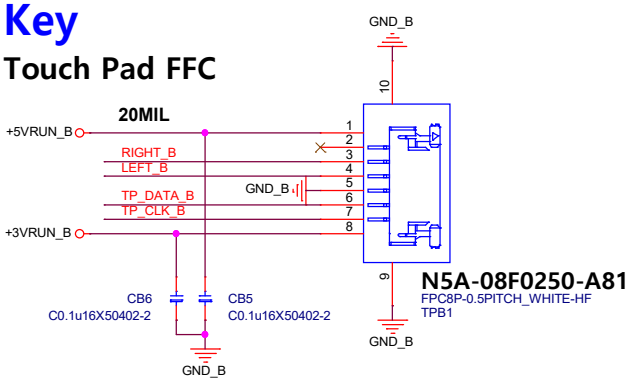





| | | |
|---|---|---|
| msi MICRO-STAR INT'L CO.,LTD. | | |
| Title: [A]Card Reader (RTS5250) | | |
| Size | Document Number: MS-18161 | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 52 of 62 | |

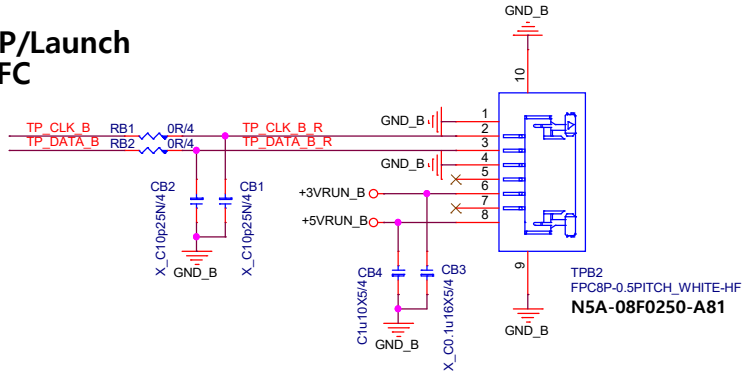
# [B]TP L/R Key

## Touch Pad FFC

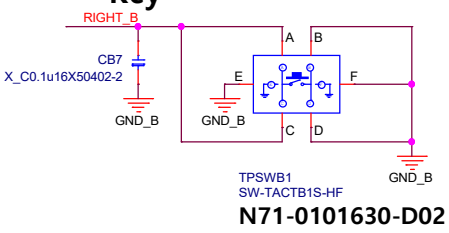


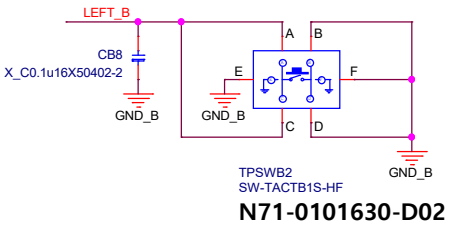

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | VDD | TouchPad Power Supply Current |
| 2 | CLK | Clock |
| 3 | DAT | Data |
| 4 | GND | Ground |
| 5 | LEFT | Left Button Switch |
| 6 | RIGHT | Right Button Switch |

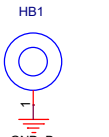
## TP/Launch FFC

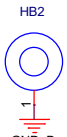


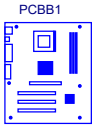

## TP L/R Key




PD0-1816B0D-H73
PD0-1816B0D-T53

## TP Mylar


60顶

E2P-8122721-G40



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| | | |
|---|---|---|
| Title | [B]TP L/R Key | |
| Size | Document Number: MS-18161 | Rev: 0D |
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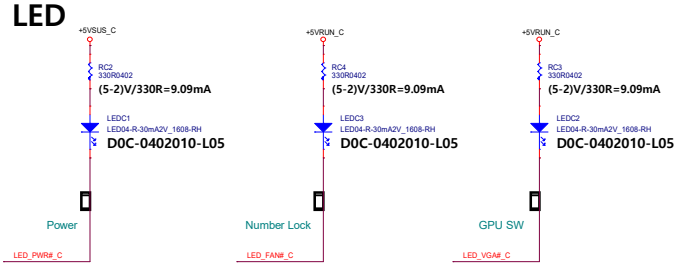
# [C]Launch Board

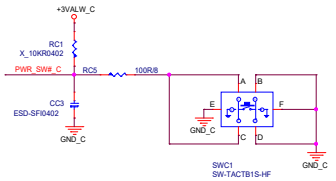
## LED




### EMI

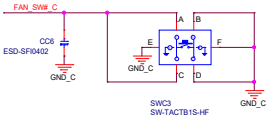

## Function KEY

### Power Key



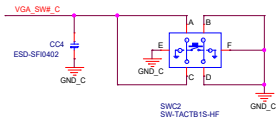

N71-0101630-D02

### Cooler Boost SW



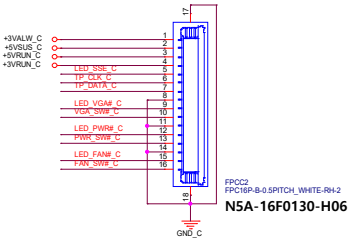

N71-0101630-D02

### Define Panel Backlight SW

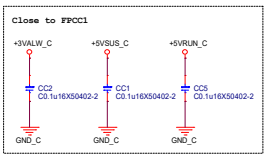



N71-0101630-D02

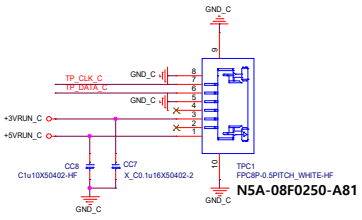
## FFC




N5A-16F0130-H06

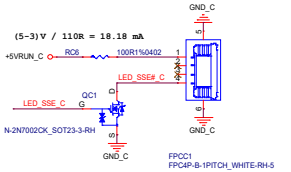



## TP/Launch FFC

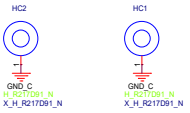



N5A-08F0250-A81

## LED FPC




N5A-04F0290-A81





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| msi | MICRO-STAR INT'L CO.,LTD. | |
| Title | [C]Launch Board | |
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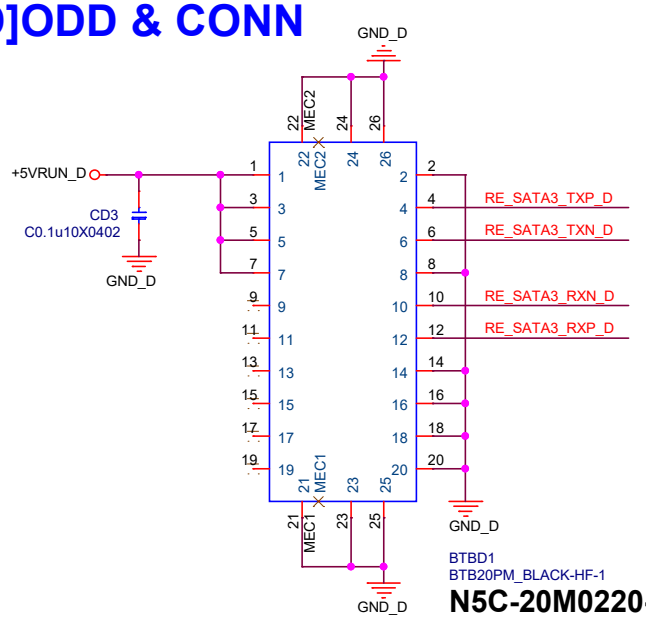
# [D]ODD & CONN




**N5C-20M0220-A81**

HD2

GND_D
H_R177D91_N
X_H_R177D91_N

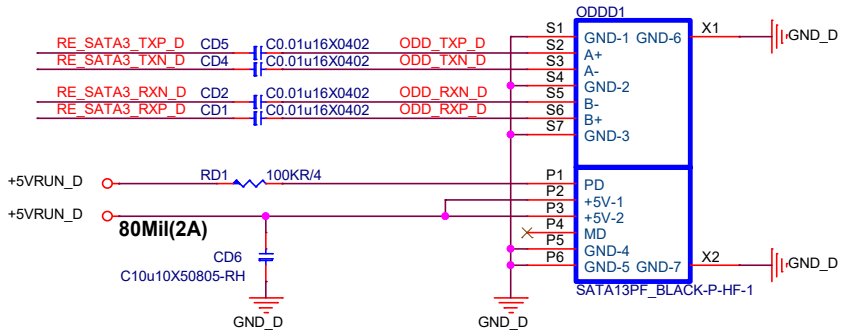
HD1

GND_D
H_R177D91_N
X_H_R177D91_N

Vinafix.com

PCBD1

**PD0-1816D0D-H73**
**PD0-1816D0D-T53**



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|---|---|---|---|
| Title | [D]ODD & CONN | | |
| Size | Document Number MS-1816D | | Rev 0D |
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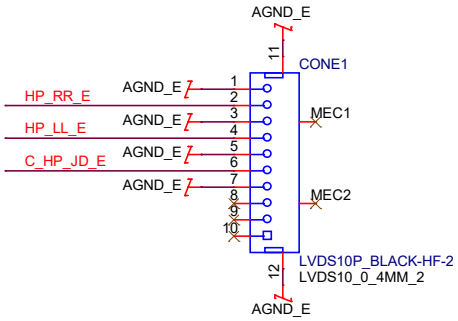
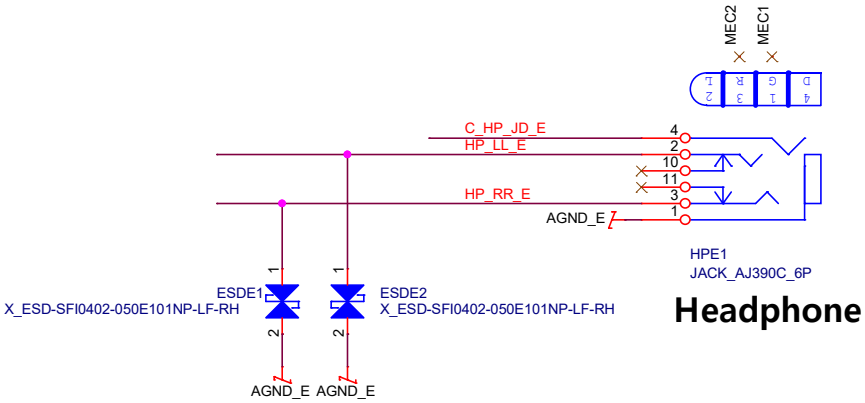
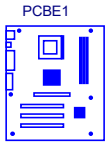
# [E]HiFi Audio CONN/Headphone



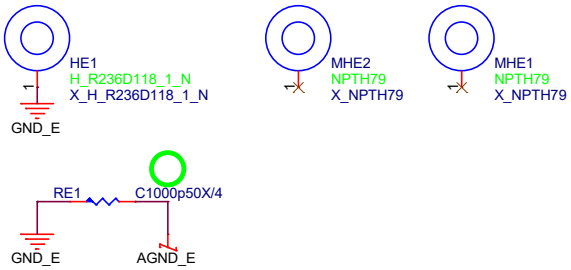

**N5Q-10F0030-A81**




**Headphone**




**PD0-1816E0D-H73**
**PD0-1816E0D-T53**

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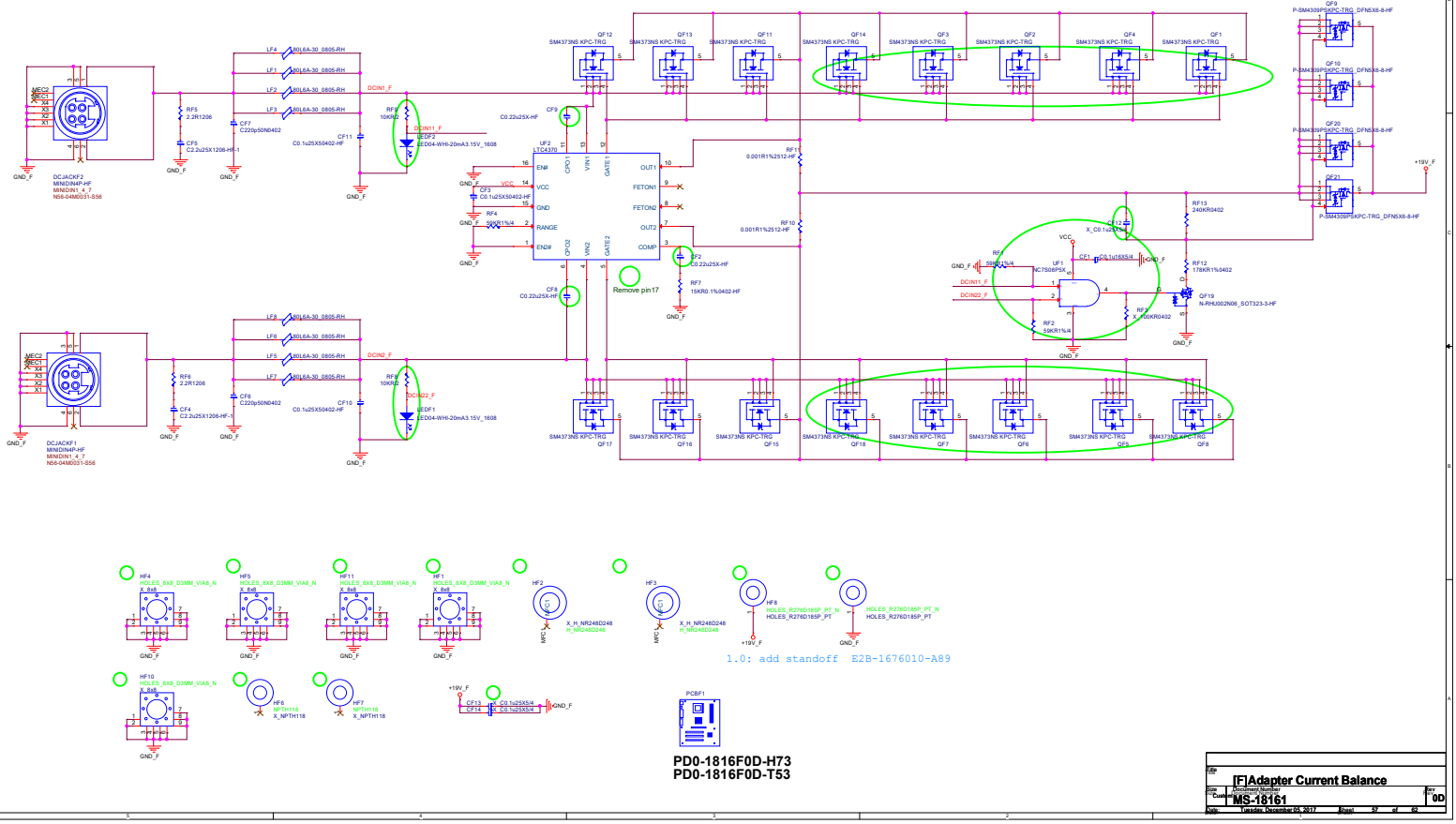
|---|---|---|---|
| Title | [E]HiFi Audio CONN/Headphone | | |
| Size: A | Document Number: MS-18161 | | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 56 of 62 | | |

# [F]Adapter Current Balance







PCBF1

**PD0-1816F0D-H73**
**PD0-1816F0D-T53**

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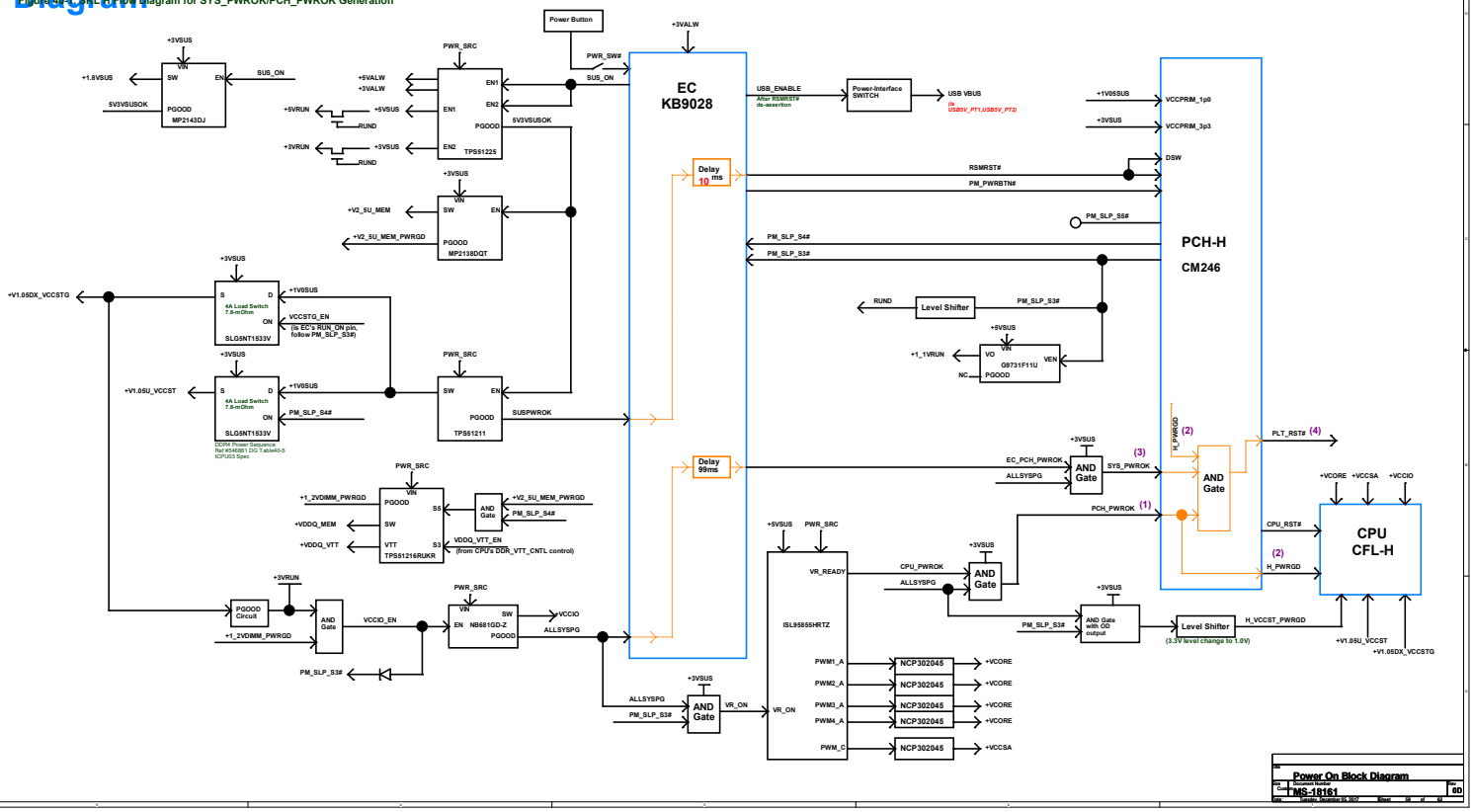
| Title | [F]Adapter Current Balance | |
| Size: C | Document Number: MS-18161 | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 57 of 62 | |

# MS-1816 : CFL-H Mobile Power on Block Diagram

Ref #546884 Chapter49
Figure 49-1 S4L CFlow Diagram for SYS_PWROK/PCH_PWROK Generation




Power On Block Diagram
MS-18161
Date: Tuesday, December 05, 2017
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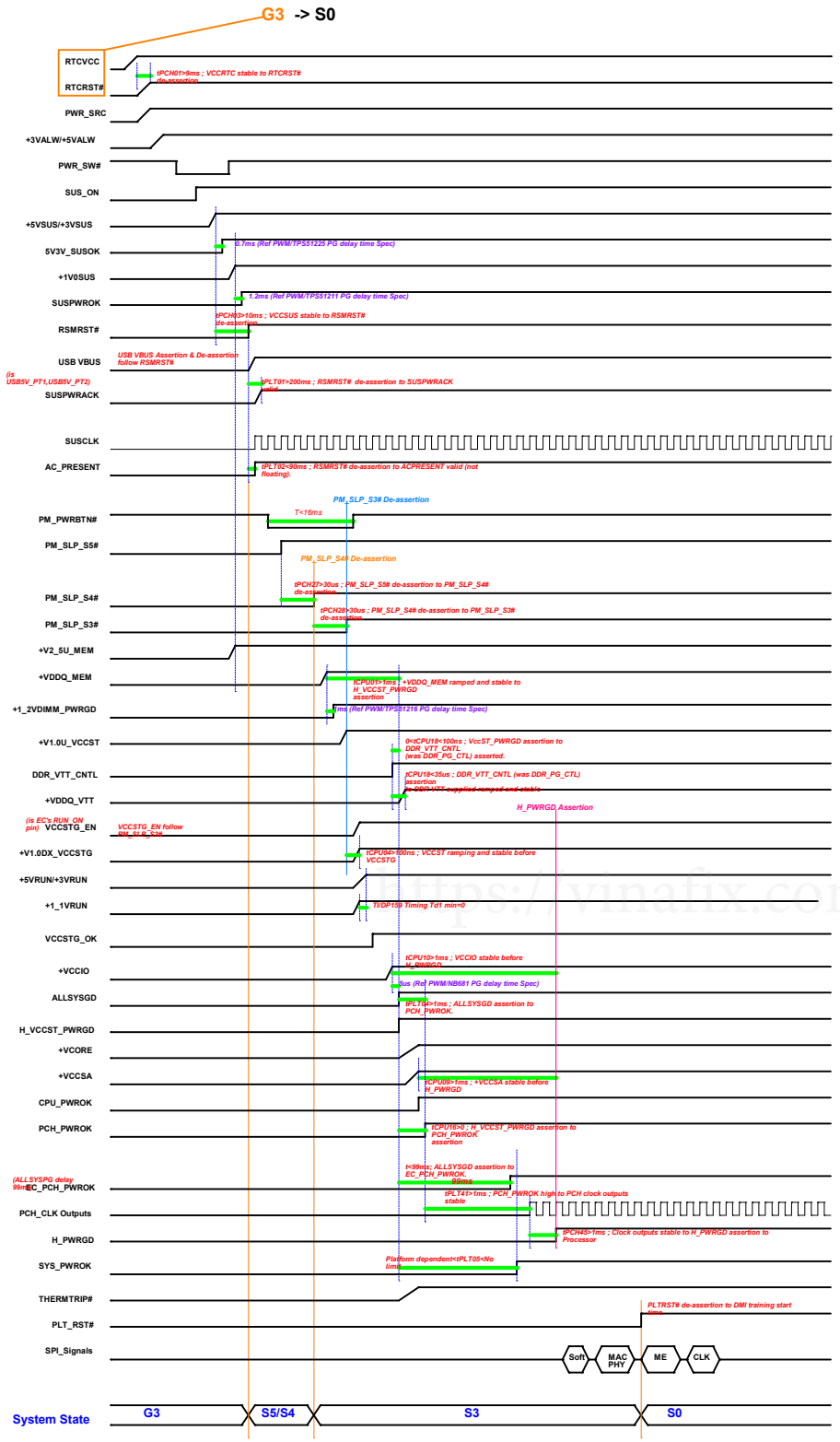
# MS-1816 : CFL-H Mobile Power ON Sequence G3 to S0

Ref: 543611 Chapter40
Figure 40-4. SKL-S Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]
Table 40-5. Platform Sequencing Timing Parameters



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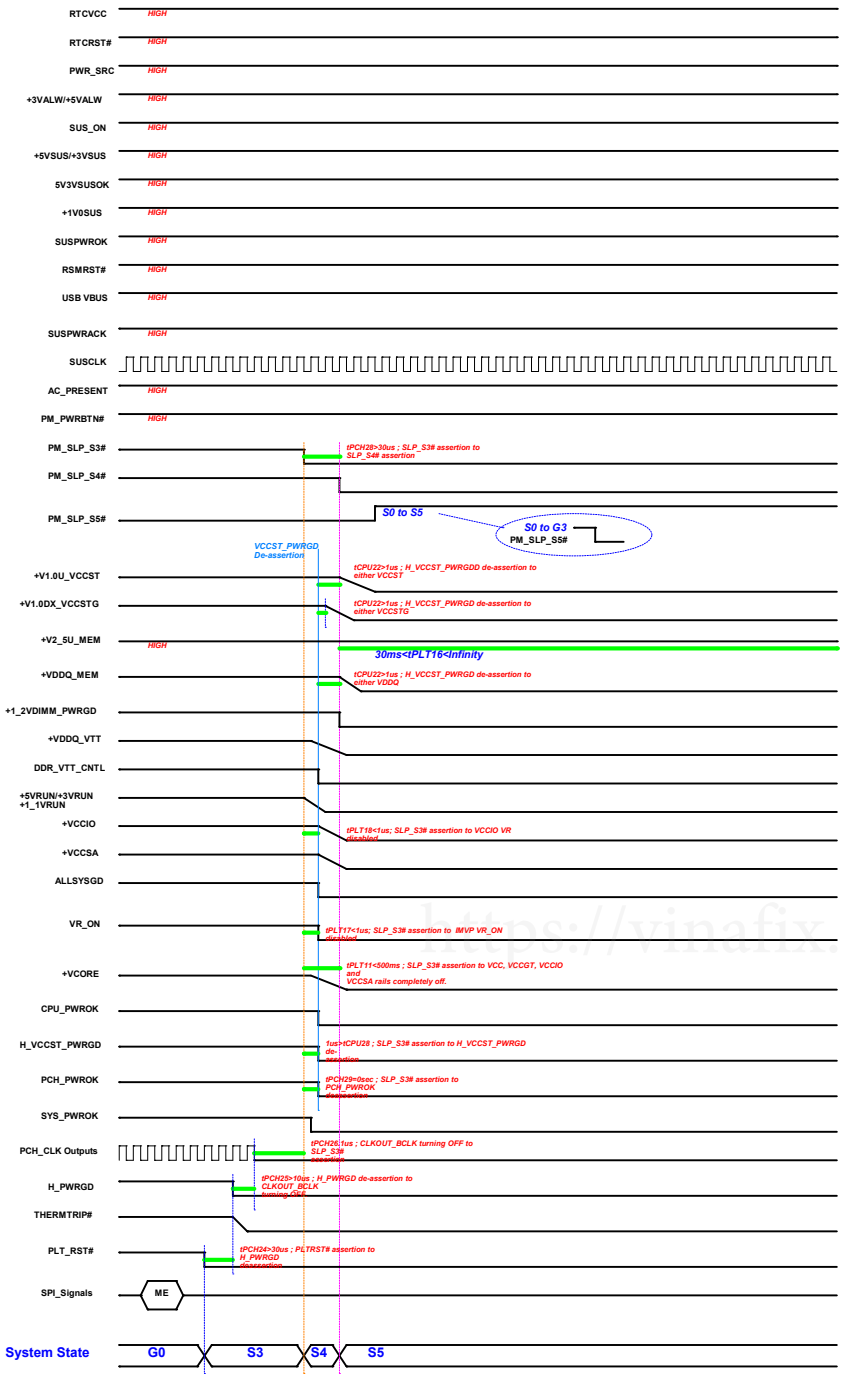
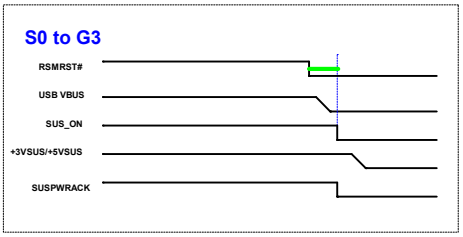
|---|---|---|
| Title | Power On Sequence | |
| Size: Custom | Document Number: MS-18161 | Rev: 0D |
| Date: Tuesday, December 05, 2017 | Sheet 59 of 62 | |

# MS-1816 : CFL-H Mobile Power Down Sequence S0 to S5

Ref 1243611 Chapter40
Figure 40-6. SKL-S Timing Diagram for S0 to G3 [Non-Deep Sx Platform]
Table 40-5. Platform Sequencing Timing Parameters



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|---|---|---|---|
| Title: Power Down Sequence | | | |
| Size: Custom | Document Number: MS-18161 | | Rev: 0D |
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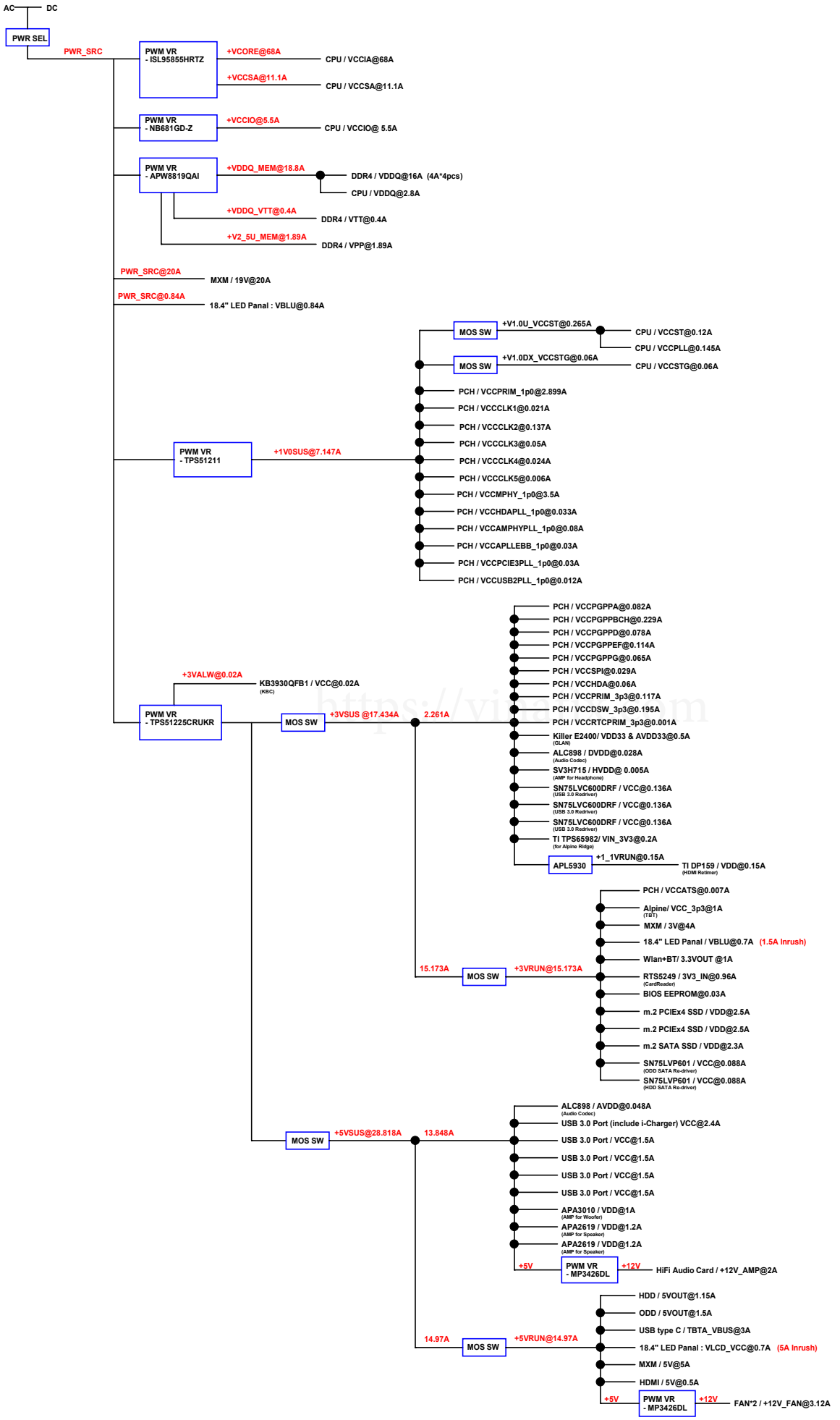
# MS-1816 Power Delivery Chart



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Power Delivery Chart

MS-18161

## ver: 0A

1.2017/08/22 page13 change R95 From 1M ohm to 220K ohm

## ver: 0B

1.2017/08/23 Page18 Adding to CNV_BRI_DT & CNV_RGI_DT net R741 4.7K & R742 20K Pull-up
2.2017/08/23 Page19 Adding to Power NET VCCPHVLDO_1P8
3.2017/08/23 Page30 Change U21.12 pin to I2S_OUT2 NET
4.2017/08/23 Page31 Change U29.12 pin to I2S_OUT2 NET
5.2017/08/23 Page38 Change BTB1.15 pin to I2S_OUT1 NET
6.2017/08/24 Page36 Adding to ODD Redriver IC
7.2017/08/24 Page39 Adding to ODD Connector
8.2017/08/24 Page55 Adding to ODD Function Board
9.2017/08/24 Page13 Adding to TBT_CLKREQ_N Net Pull- up 10K R748 to +3VSUS.
10.2017/08/24 Page51 Change MXM_H8 footprint H_R236D118_1_N to H_R276D118_N
11.2017/08/24 Page51 Change ODD_H1 footprint HOLES_R177D91 to HOLES_R177D91_N
12.2017/08/24 Page51 Change ODD_H2 footprint HOLES_R177D91 to HOLES_R177D91_N
13.2017/08/24 Page55 Change HD1 footprint H_R177D91 to H_R177D91_N
14.2017/08/24 Page55 Change HD2 footprint H_R177D91 to H_R177D91_N
15.2017/08/24 Page21 U34 .123 Pin Change NET AZ_GPIO3_DSD to AZ_GPIO4_PCM
16.2017/08/24 Page29 U22 .56 Pin Change NET AZ_GPIO3_DSD to AZ_GPIO4_PCM
17.2017/08/24 Page51 CPU BRAKET CHANGE PART 307-8160111-A89
18.2017/08/24 All of PCBA change to 0B
19.2017/08/25 Page 19 Adding to R749 0 ohm for PCH Power 1.24V
20.2017/08/25 Page 50 Delete J44 ; J34 ; J33 ; J9 ; J41 Impedence
21.2017/08/28 PU15, PR140, PC154, PC153 Stuff
22.2017/08/28 change U3.1 redriver DC Gain setting

## ver: 0C

1.2017/10/06 Page16 Change ODD SATA_1B to SATA_0B
2.2017/10/06 Page10 Change C781 0.1UF to un_stuff
3.2017/10/06 Page27 Change R169 100K/2 to un_stuff
3.2017/10/06 Page21 Adding to U34 P112 (EC/ENE9028) LED_SSE Net
4.2017/10/06 Page21 AC_PRESENT NET Adding to R750 up HIGH 100K/4 ohm
5.2017/10/06 Page21 U34.P36 Adding to EC_ALLSYSPG NET
6.2017/10/06 Page17 PCH_PWROK function adding to R751 & R752 & R753 & R754 0 ohm For power sequence
7.2017/10/06 Page26 Change SPEC DP1.4 to DP1.2
8.2017/10/11 Page14 Adding U32.AN37 DGPU_PWR_EN For GC-off PCH
9.2017/10/11 Page14 Adding R766 For DGPU_PWR_EN NET Pull_low
10.2017/10/11 Page14 Change TBT_FORCE_PWR NET TO u32.Y47 GPP_K16 GPIO FOLLOW 16K5
11.2017/10/11 Page14 Adding to R777 0_ohm for TBT_FORCE_PWR NET
12.2017/10/11 Page14 Change BT_CIO_PLUG_EVENT_N NET TO U32.Y46 GPP_K12 GPIO FOLLOW 16K5
13.2017/10/11 Page14 Adding to R776 0_ohm for BT_CIO_PLUG_EVENT_N NET
14.2017/10/11 Page16 Adding U32.V48 HDMI_HP_DET NET For GC-off PCH
15.2017/10/11 Page16 Adding to R774 0_ohm for HDMI_HP_DET net un_stuff
16.2017/10/11 Page16 Adding U32.U47 MXMDPB_HPD NET For GC-off PCH
17.2017/10/11 Page16 Adding to R778 0_ohm for MXMDPB_HPD net un_stuff
18.2017/10/11 Page16 Adding U32.R46 DP_HPD NET For GC-off PCH
19.2017/10/11 Page16 Adding to R771 0_ohm for DP_HPD net un_stuff
20.2017/10/11 Page18 Adding U32.AU26 MXM_PWROK_R NET For GC-off PCH
21.2017/10/11 Page18 Adding u32.AT49 DGPU_HOLD_RST# NET For GC_OFF PCH
22.2017/10/11 Page21 Adding R773 0_ohm for GC_OFF
23.2017/10/11 Page21 Adding R775 0_ohm for GC_OFF
24.2017/10/11 Page22 Adding R768 0_ohm for GC_OFF un_stuff
25.2017/10/11 Page22 Adding R767 0_ohm for GC_OFF stuff
26.2017/10/11 Page22 Adding R764 0_ohm for GC_OFF un_stuff
27.2017/10/11 Page22 Adding R765 0_ohm for GC_OFF un_stuff
28.2017/10/11 Page14 Modify U32.AL37 to GND
29.2017/10/12 Page43 PR164 36K to 27.4K for change OCP
30.2017/10/12 Page44 PC196, PC65, PC190 4700P to 680P for change output transient response
31.2017/10/12 Page46 change
PR38 499R to 1K
PR41 2.21K to 2.55K
PR31 49.9K to 47K
PR19 165K to 169K
PC20 15P to 100P
PC17 220P to 470P
PC8 560P to 680P
PU1 NCP81215 to NCP81205F
32.2017/10/13 Page23 edp port adding MUX -IC TI HD3SS213 Differential Switch
33.2017/10/13 Page30 Co-layout Speaker adding R784 & R785 0R ohm/0805
34.2017/10/16 Page23 shift eDP & LVDS lane with AUX IC
35.2017/10/16 Page26 delet EL1, EL2, EL3, EL4
36.2017/10/18 Page23 add C832

## ver: 0C

37.2017/10/19 C74, C648 un-stuff for nV required
38.2017/10/19 R76, R763 stuff for nV required
39.2017/10/19 GPU_EVENT#_2 conn to PCH for nV required
40.2017/10/20 add R786 un-stuff for rework
41.2017/10/20 10/19 R764 uf-stuff,U25 stuff
42.2017/10/25 EC5, EC14, EC9, EC52, EC51, C54 stuff for EMI
43.2017/10/25 add EC90, EC91 stuff for EMI
44.2017/11/3 ALC1220 update to VB2

## ver: 0D

1.2017/10/30 Page 32 USB3.1 GEN2 Change to Re-Timer IC.
2.2017/10/30 Page 21 USB3.1 Re-Timer IC SM BUS LINK to EC.
3.2017/10/30 Page 30 & Page 31 Audio Amp I2S Bus Change to CT5302 IC
4.2017/11/15 Page 32 EQB_1 Pu-High 1.8V
5.2017/11/20 Page 32 add C1260, C1261, C1262
6.2017/11/24 Page 32 PR268 Change to 30K1%
7.2017/11/24 Page 32 PR267 Change to 24K1%
8.2017/11/24 Change Net GPU_EVENT#_2 From Page 17 U32.Aw29 to Page18 U32.BB26
9.2017/11/27 Page 49 Adding to EMI CAP EC92 & EC93 0.1uf_0402
10.2017/11/28 Page 17 Change BAT2 RTC Battery to D06-0103301-D73
11.2017/12/05 Adding to GC-off Function

| 1816-0D | PCH | EC | |
|---|---|---|---|
| DGPU_PWR_EN | R768 stuff | R767 un-stuff | MXM_A ; Page 22 |
| DGPU_PWR_EN | R770 stuff | R769 un-stuff | MXM_B ; Page 23 |
| MXM_PWROK_R | R765 stuff | R320 un-stuff | Page 22 |
| DGPU_HOLD_RST# | R764 ; R786 stuff | R763 ; R309 un-stuff | Page 22 |
| DP_HPD | R771 stuff | R773 un-stuff | DP; Page 16 & 21 |
| MXMDPB_HPD | R778 stuff | | AR; Page 16 |
| HDMI_HP_DET | R774 stuff | R775 un-stuff | HDMI ; Page 16 & 21 |



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