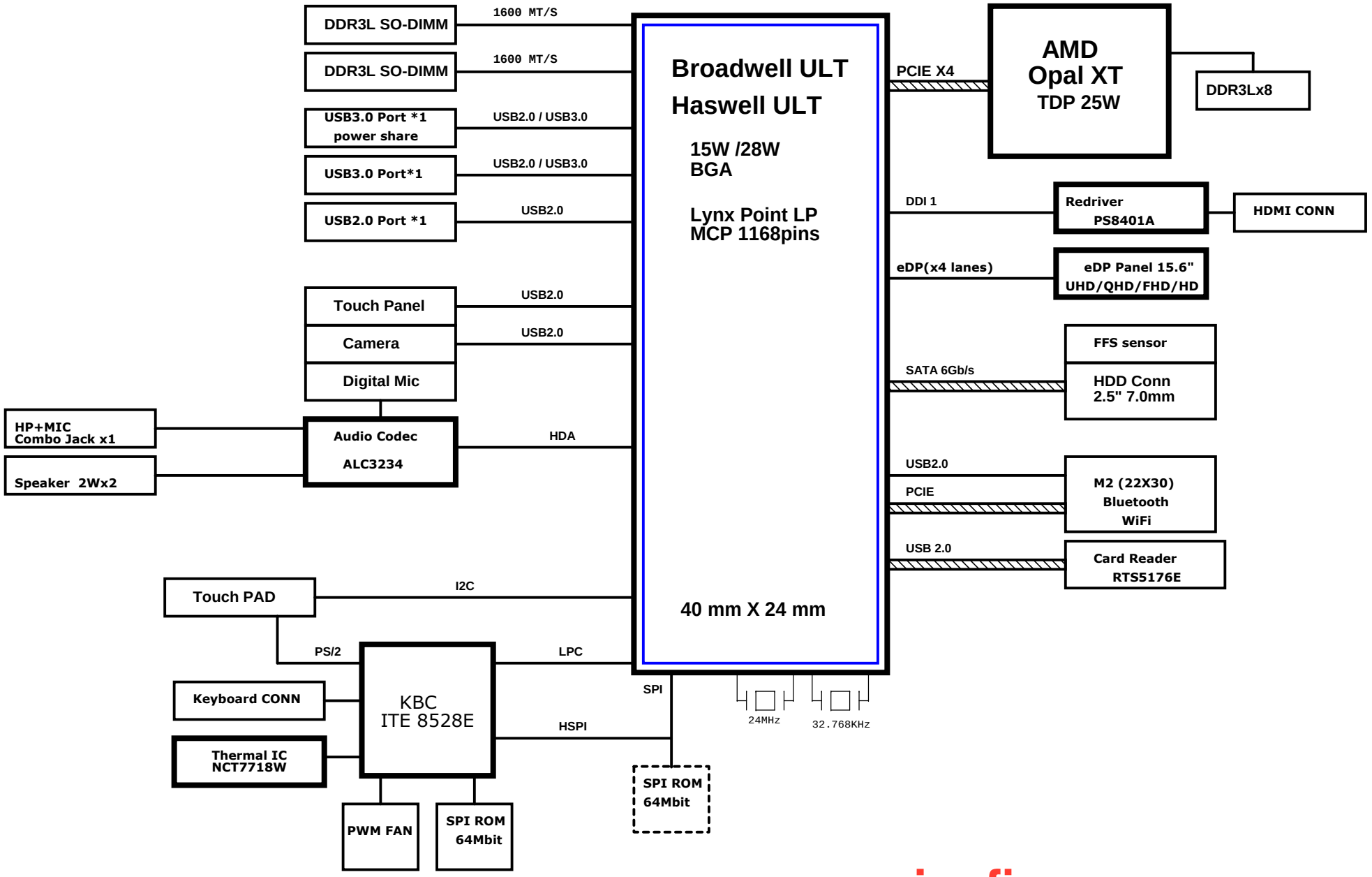
AM6 BLOCK DIAGRAM



Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	Block Diagram	A

Date: Monday, May 05, 2014 Sheet 1 of 58

HSIO Port	USB3.0	PCIE	SATA
1	USB3.0_1 Left Power Share		
2	USB3.0_2 Right		
3	USB3.0_3 X	PCIE1 X	
4	USB3.0_4 X	PCIE2 X	
5		PCIE3 X	
6		PCIE4 WIFI	
7		PCIE5 GPU 4X	
8		PCIE5 GPU 4X	
9		PCIE5 GPU 4X	
10		PCIE5 GPU 4X	
11		PCIE6 X	SATA3 X
12		PCIE6 X	SATA2 X
13		PCIE6 X	SATA1 HDD
14		PCIE6 X	SATA0 X

PCIE CLK
CLK0 X
CLK1 X
CLK2 X
CLK3 WIFI
CLK4 GPU 4X
CLK5 X

USB2.0
USB2.0_0 Left Power Share
USB2.0_1 Right /w 3.0
USB2.0_2 Right
USB2.0_3 Card Reader
USB2.0_4 Camera
USB2.0_5 eTP
USB2.0_6 Blue Tooth
USB2.0_7 X

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Size	Document Number	Rev
	PORT ASSIGNMENT	A

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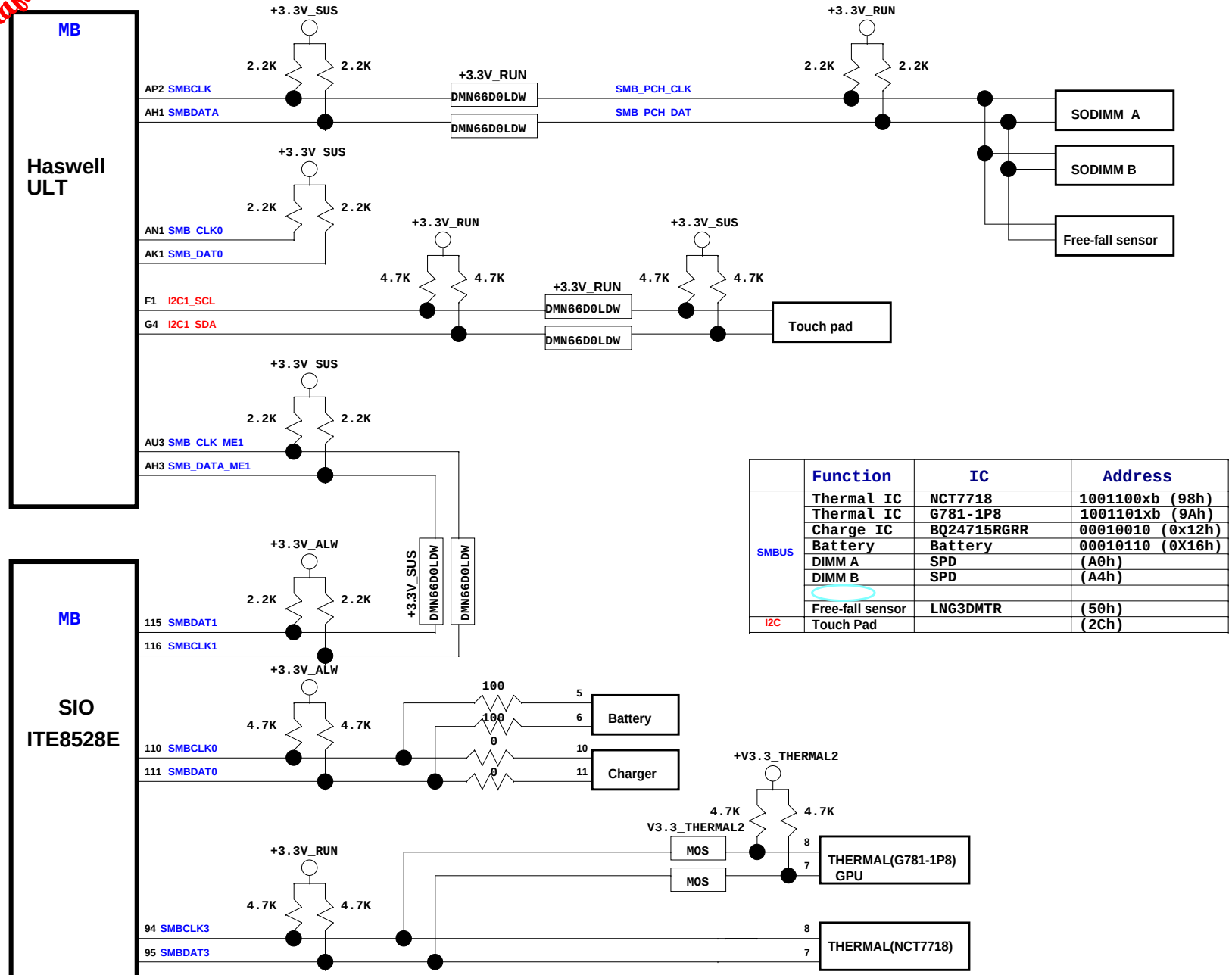

	Function	IC	Address
SMBUS	Thermal IC	NCT7718	1001100xb (98h)
	Thermal IC	G781-1P8	1001101xb (9Ah)
	Charge IC	BQ24715RGRR	00010010 (0x12h)
	Battery	Battery	00010110 (0X16h)
	DIMM A	SPD	(A0h)
	DIMM B	SPD	(A4h)
	Free-fall sensor	LNG3DMTR	(50h)
I2C	Touch Pad		(2Ch)

Quanta Computer Inc.
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Size	Document Number	Rev
	SMBUS	A

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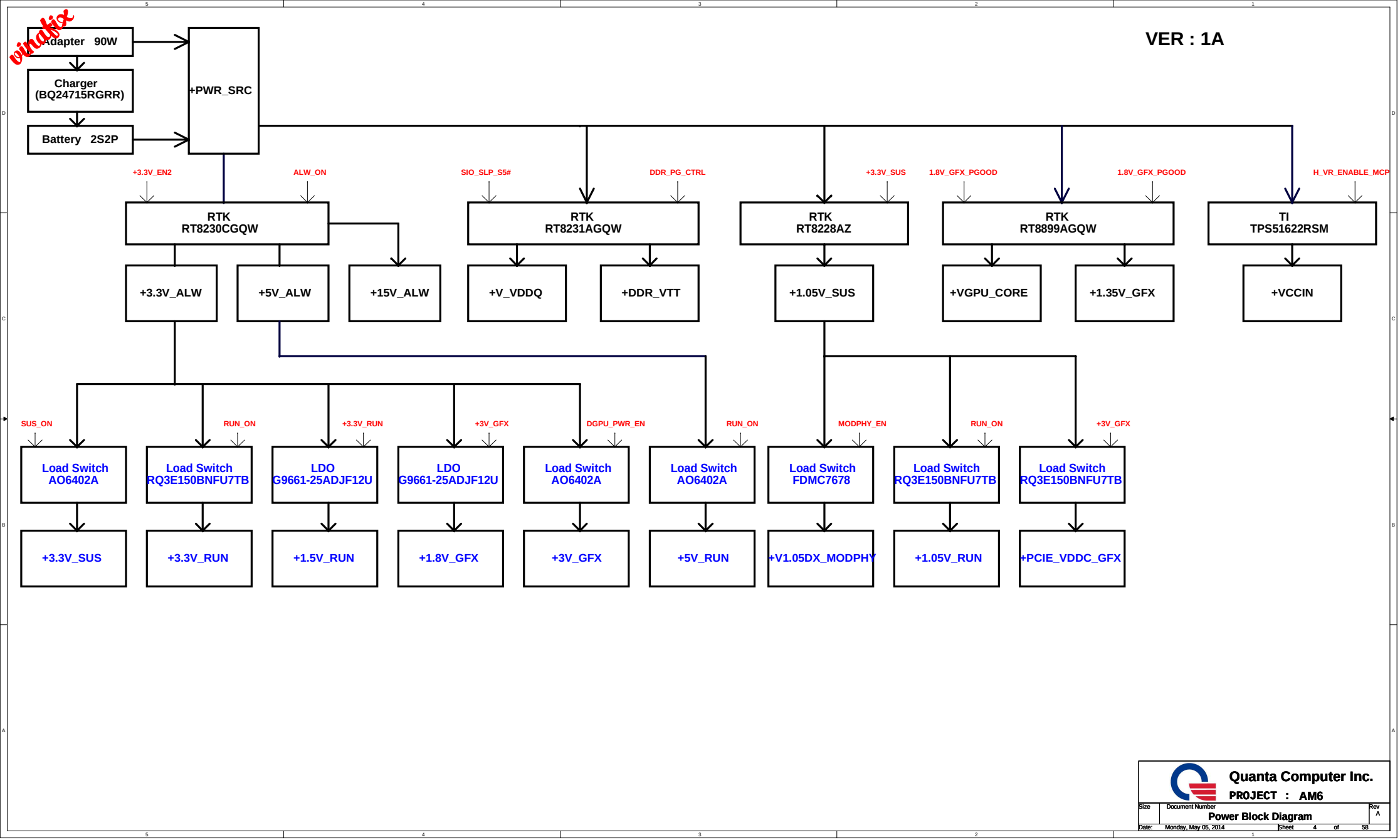

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PROJECT : AM6

Size	Document Number	Rev
	Power Block Diagram	A

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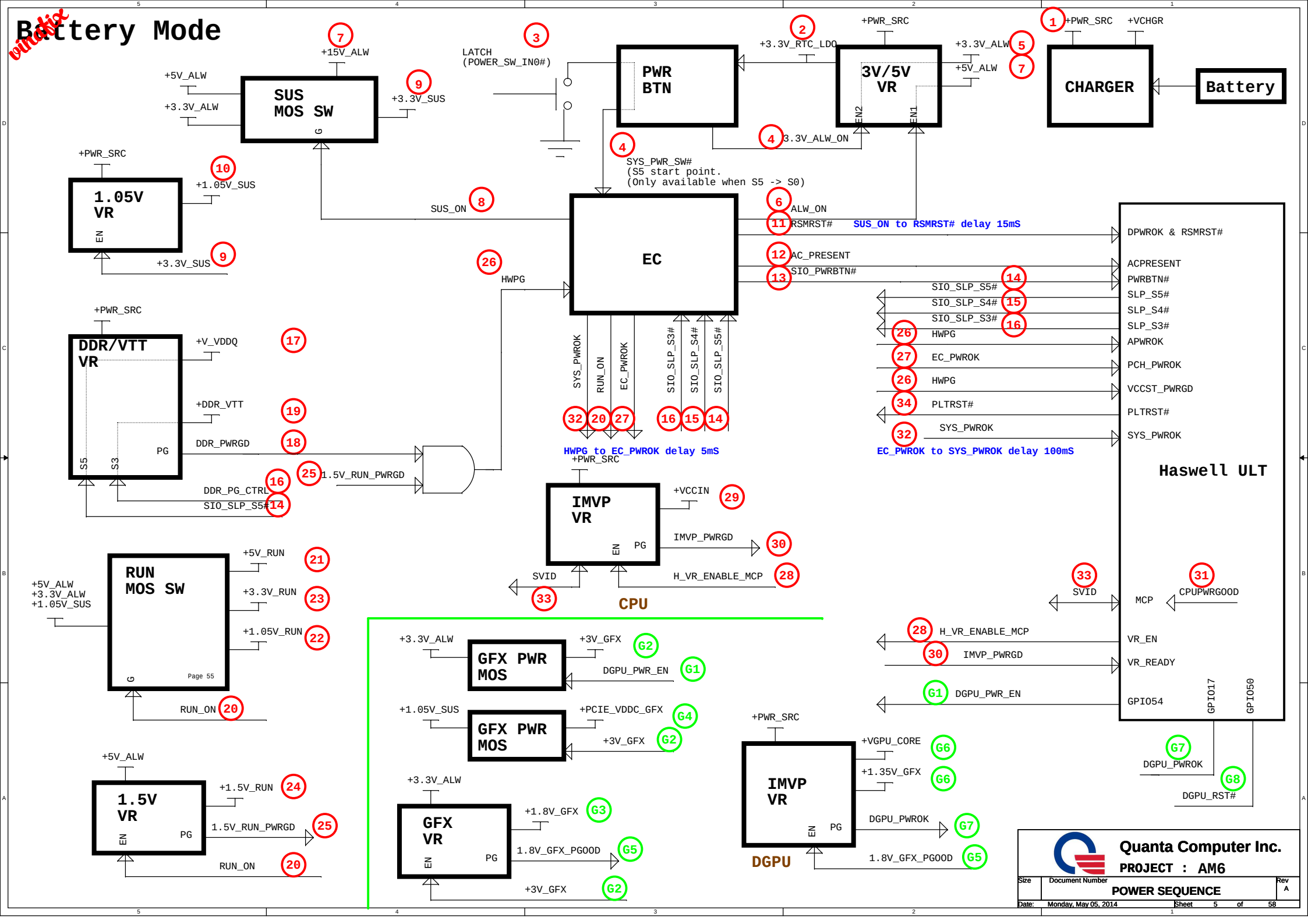
Battery Mode



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Size	Document Number: POWER SEQUENCE
Rev	A
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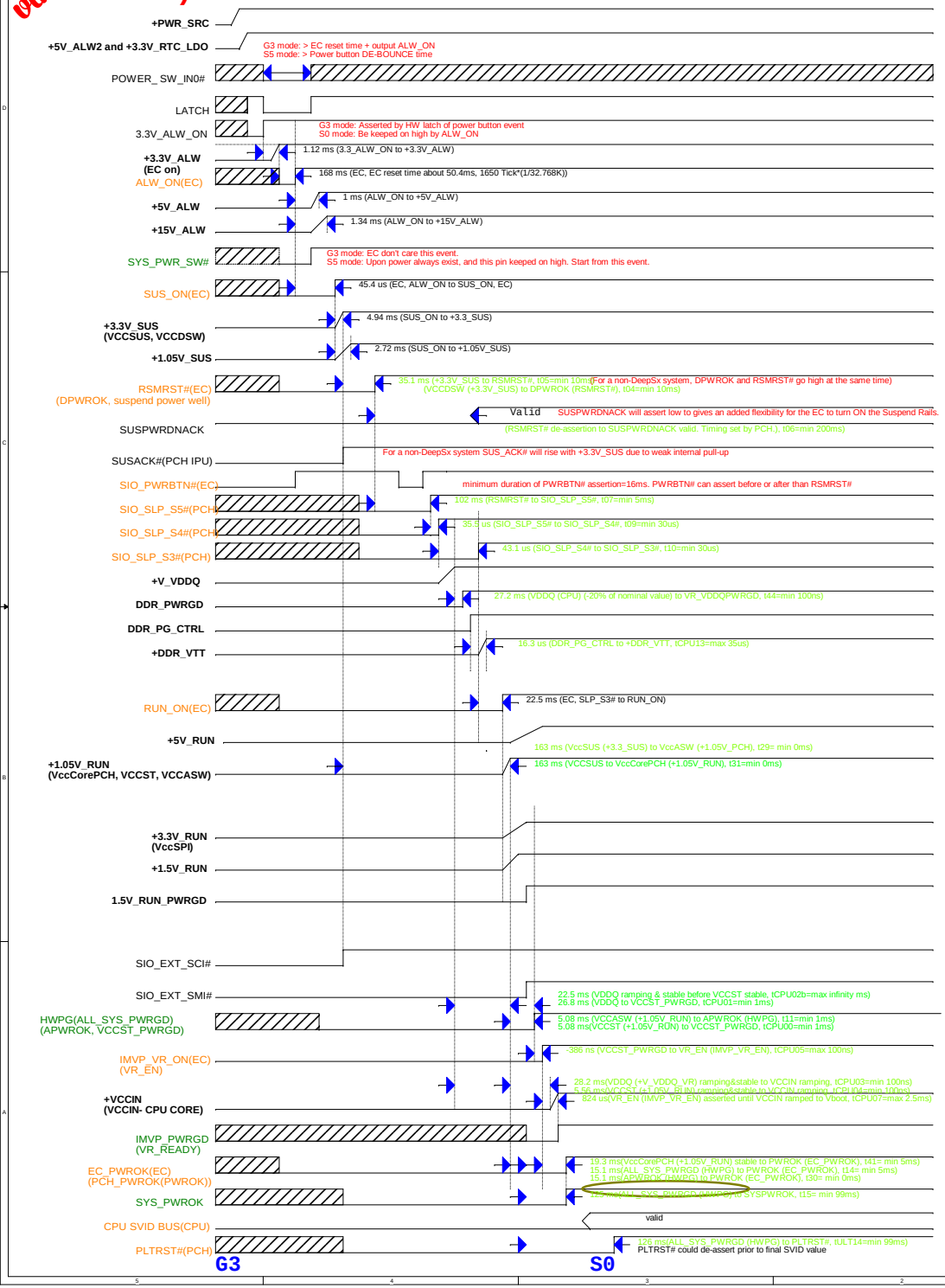
Power Sequence (G3 to S0)

Shark Bay ULT PSS, 490828, Rev1.1



Quanta Computer Inc.
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Size	Document Number	Rev
	G3 to S0	A
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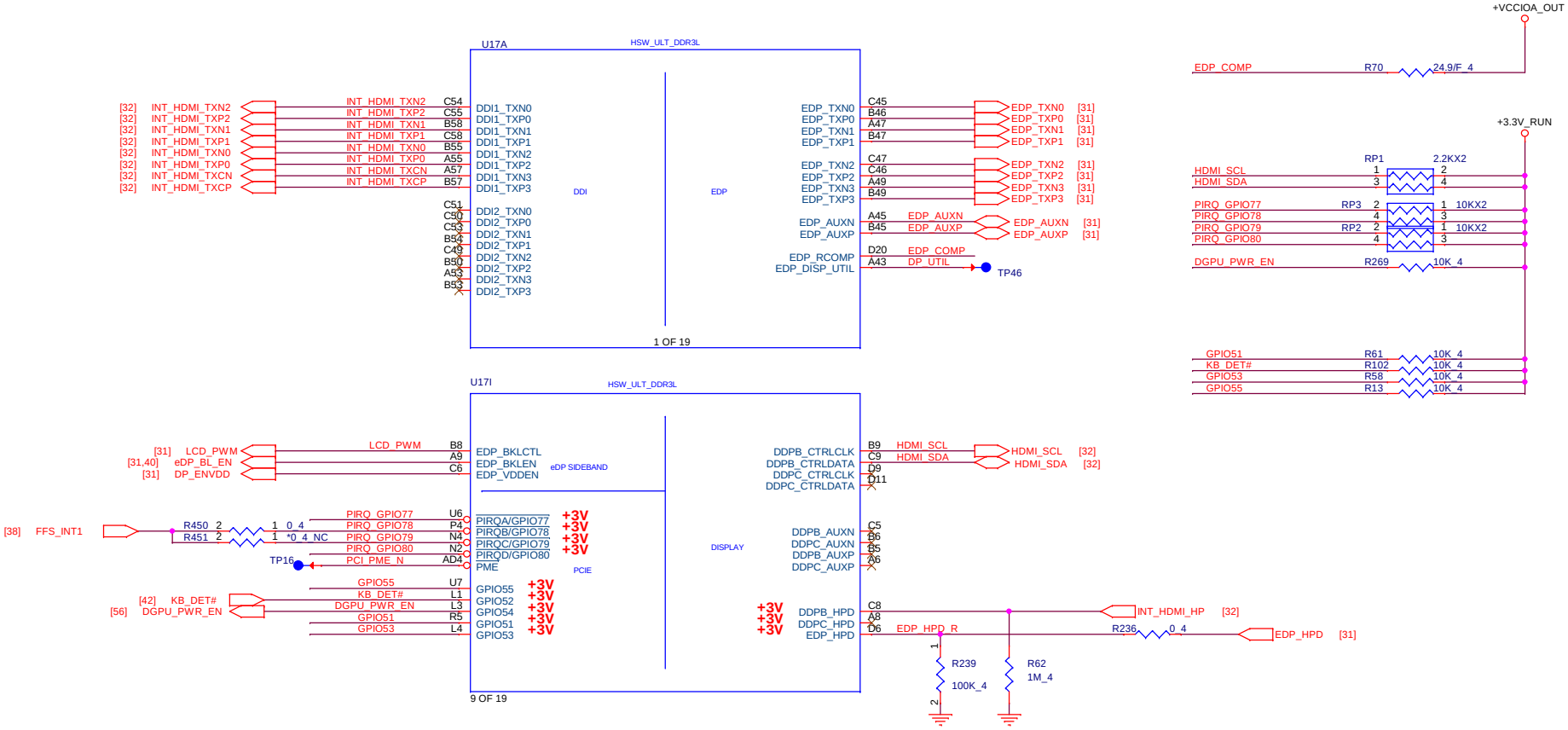
Haswell ULT (DISPLAY)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
DDPB_CTRLDATA	Port B Detected	PCH_PWROK	0 = Port B is not detected. 1 = Port B is detected.	This signal has a weak internal pull-down. IPD 20K is disabled when PLTRST# is de-asserted. PU 2.2K to +3.3V_RUN
DDPC_CTRLDATA	Port C Detected	PCH_PWROK	0 = Port C is not detected. 1 = Port C is detected.	This signal has a weak internal pull-down. IPD 20K is disabled when PLTRST# is de-asserted. NC

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	Haswell ULT 1/12	A

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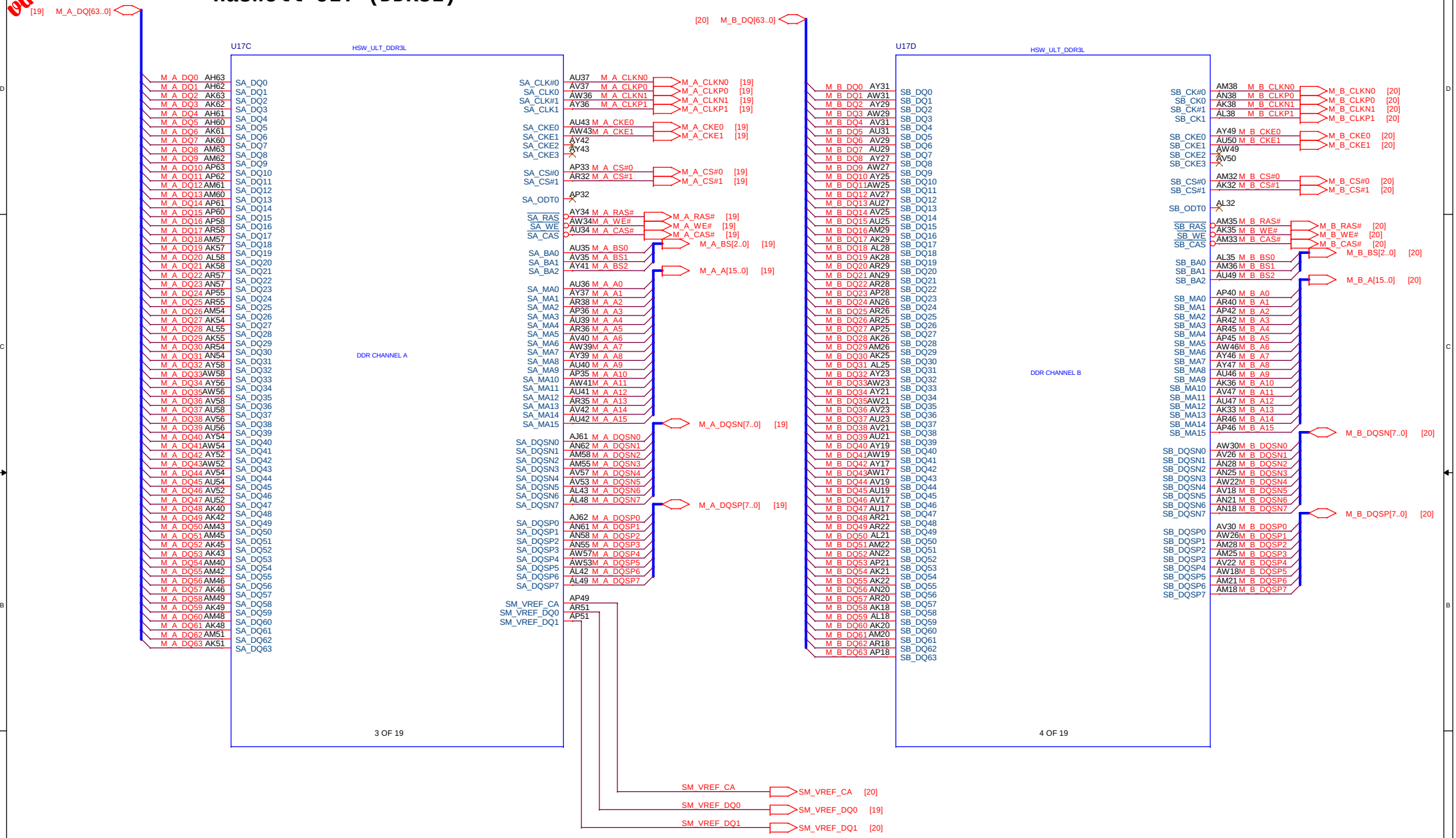
Haswell ULT (DDR3L)



Quanta Computer Inc.		
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Size	Document Number: Haswell ULT 2/12	Rev: A
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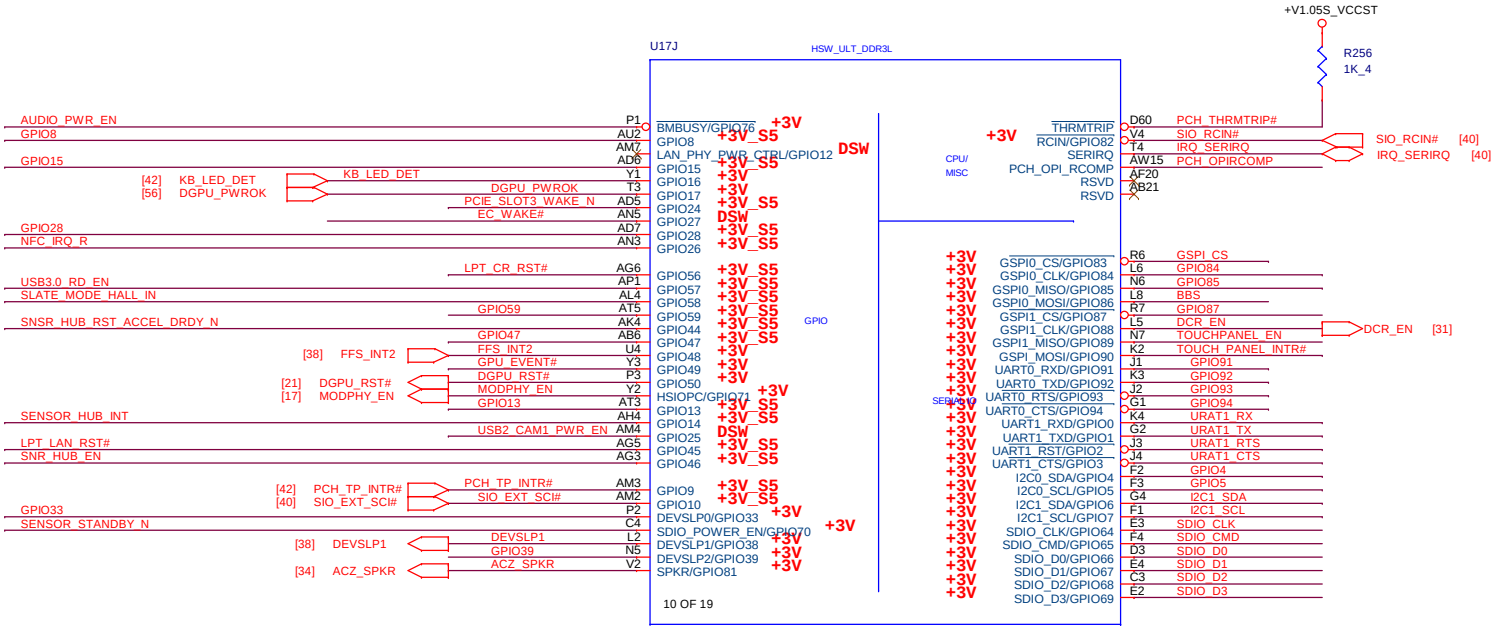
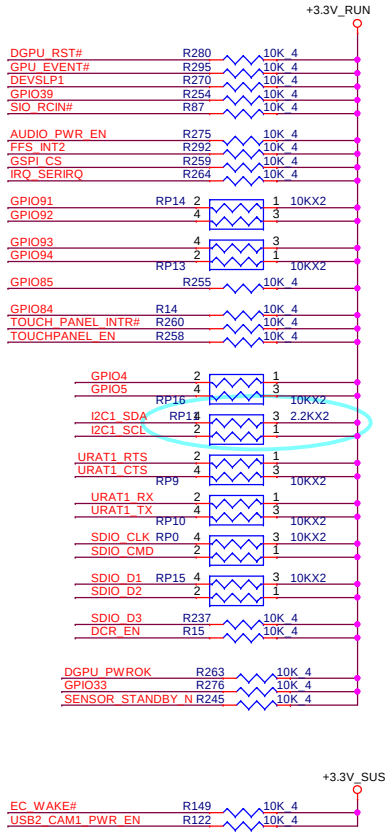
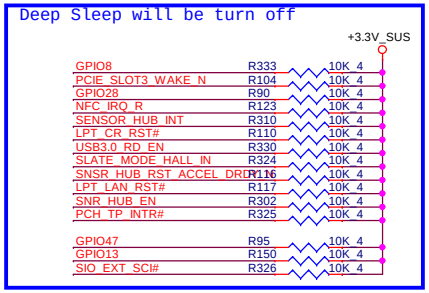
Hasswell ULT(GPIO,LPIO,MISC)

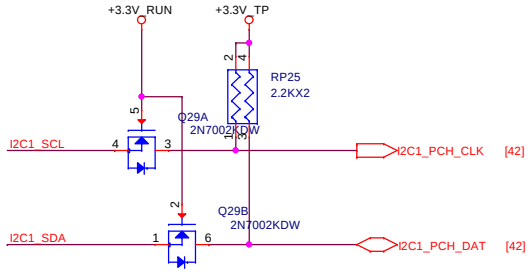


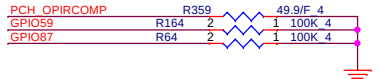


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO15	TLS Confidentiality	RSMRST#	0 = Disable 1 = Enable	This signal has a weak internal pull-down.
SPKR/GPIO81	No Reboot mode	PCH_PWROK	0 = Disable 1 = Enable	This signal has a weak internal pull-down. NA
GSPI0_MOSI/GPIO86	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = SPI 1 = LPC	This signal has a weak internal pull-down.
SDIO_D0/GPIO66	Top Swap Override	PCH_PWROK	0 = Disable 1 = Enable	This signal has a weak internal pull-down.







Deep Sleep will be turn off

+3.3V_SUS R103 *10K_4_NC GPIO15

+3.3V_RUN R265 *1K_4_NC BBS

+V3.3S_1.8S_LPSS_SDIO R21 *1K_4_NC SDIO_D0

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	Haswell ULT 3/12	A

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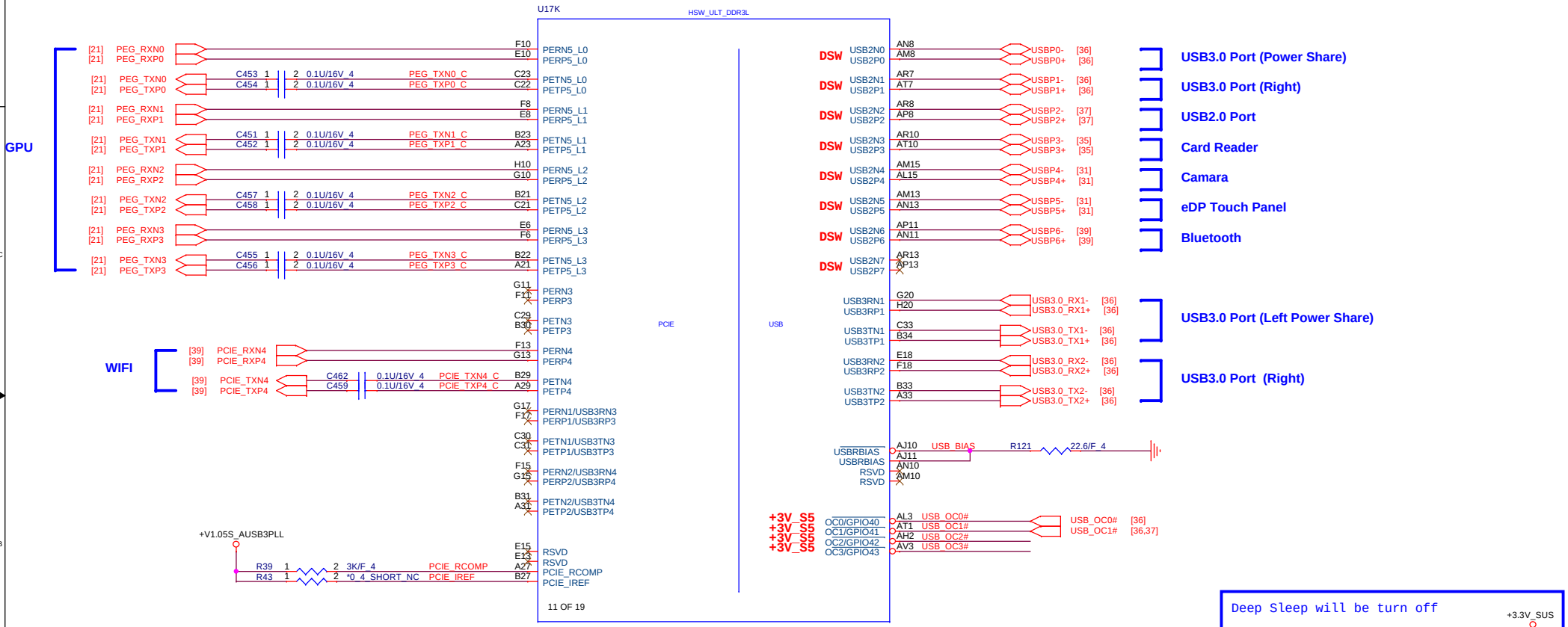
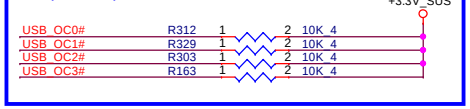
Haswell ULT (PCIE,USB)



Deep Sleep will be turn off



Overcurrent Pin Setting

Pin	Default Port Mapping	AM6 setting
OC0#	Port 0, Port 1	Port 0
OC1#	Port 2, Port 3	Port 1, Port 2
OC2#	Port 4, Port 5	no use
OC3#	Port 6, Port 7	no use

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	Haswell ULT 4/12	A

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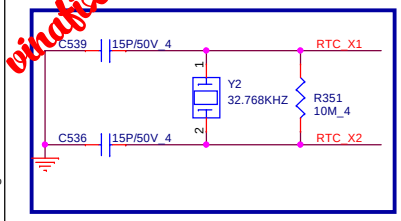
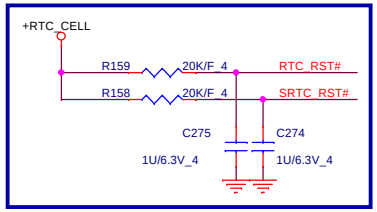
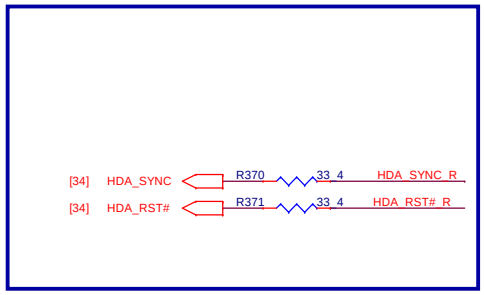
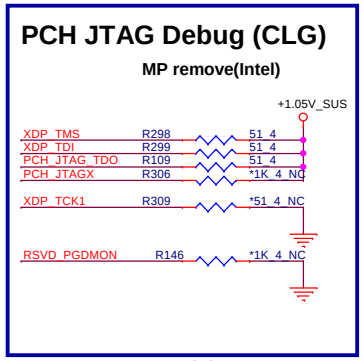
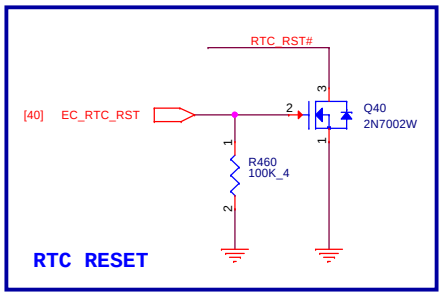
Haswell ULT (RTC, HDA, JTAG, SATA)

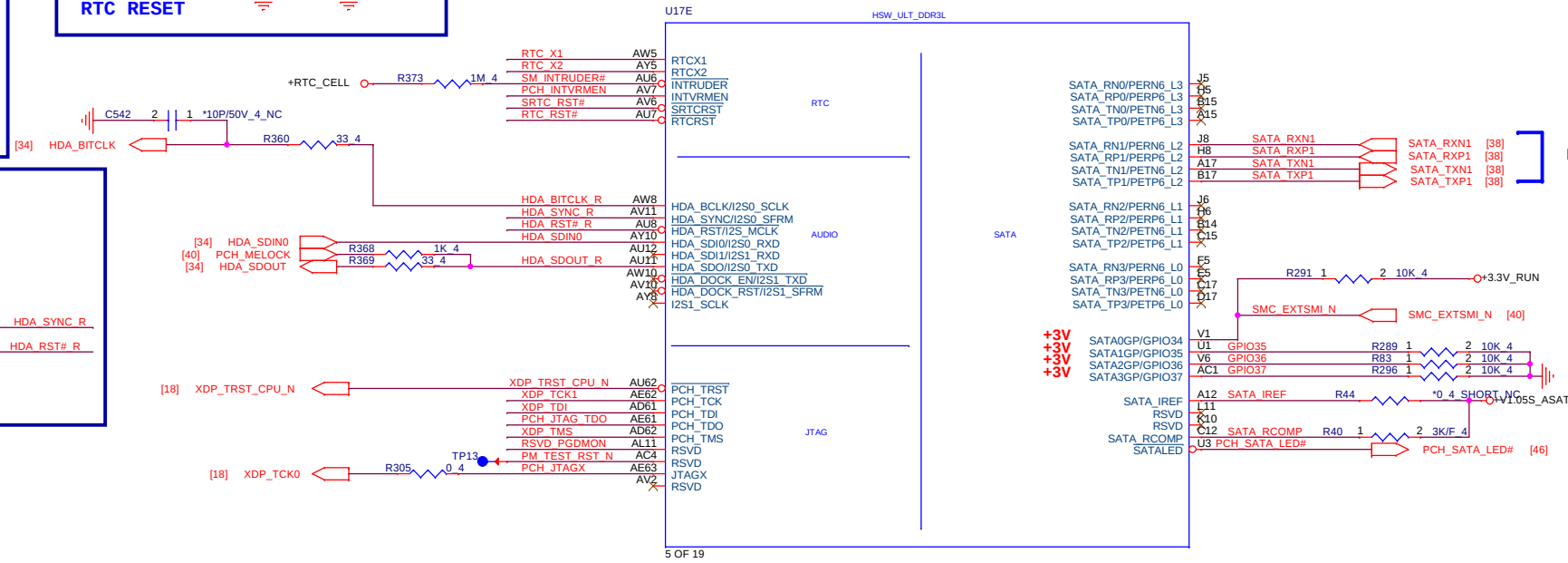












DFXTESTMODE
HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = Security Effect (Int PD) 1 = Can be Override	This signal has a weak internal pull-down. The internal pull-down is disabled after PLTRST# deasserts
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Integrated VRMs disabled. 1 = Integrated VRMs enabled.	+RTC_CELL R157 *330K_4_NC PCH_INTVRMEN R147 330K_4 **An external resistor is required**

Quanta Computer Inc.
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	Haswell ULT 5/12	A

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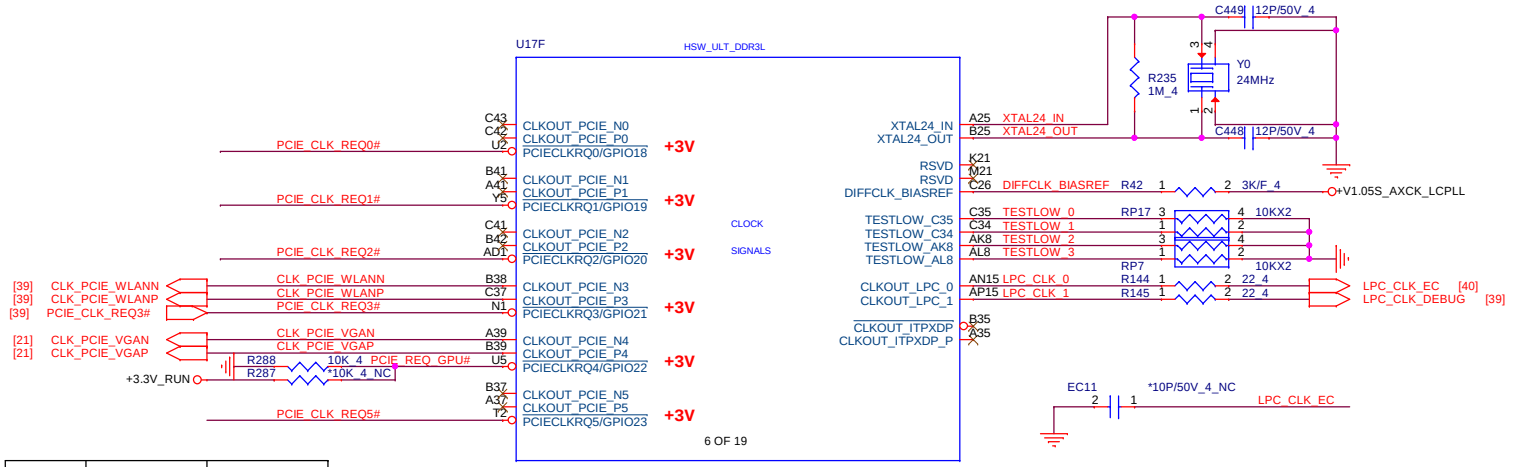
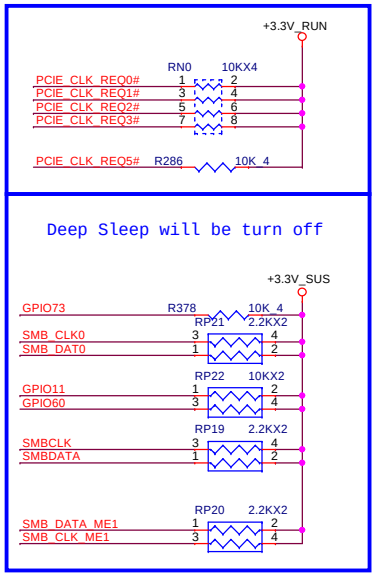
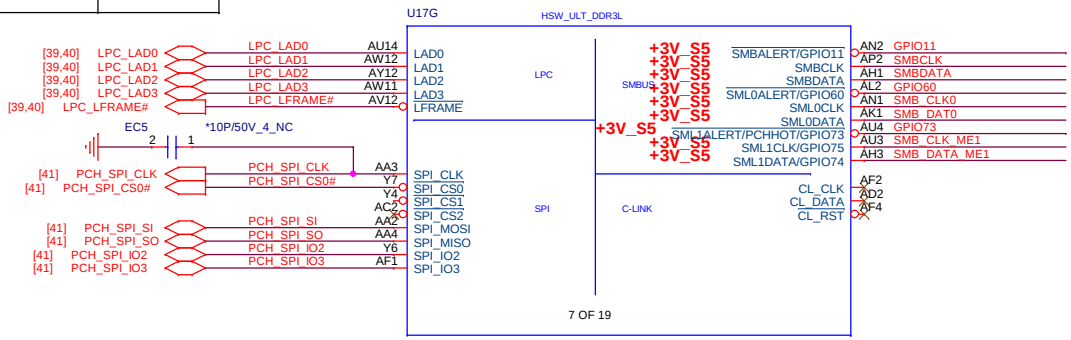
Haswell ULT (CLK)

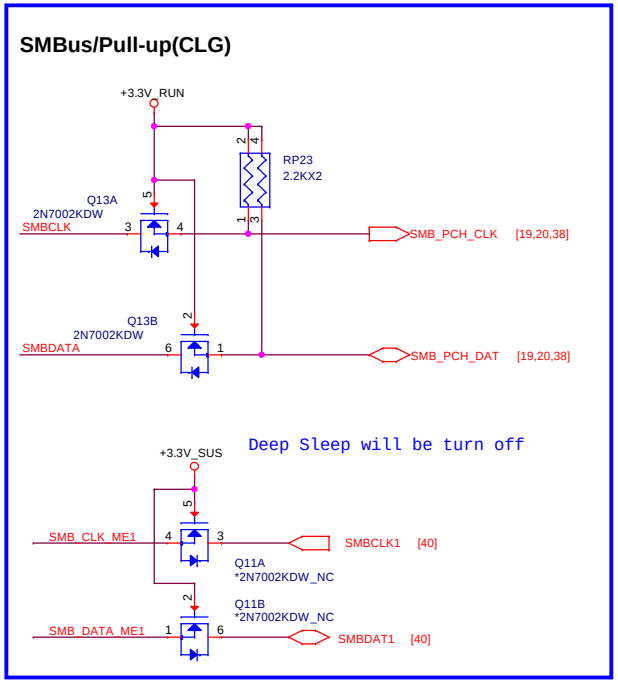




	UMA	Discrete
R288	*10K_4_NC	10K_4
R287	10K_4	*10K_4_NC

Haswell ULT (LPC/SPI/SMB/CLINK)





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	Haswell ULT 6/12	A

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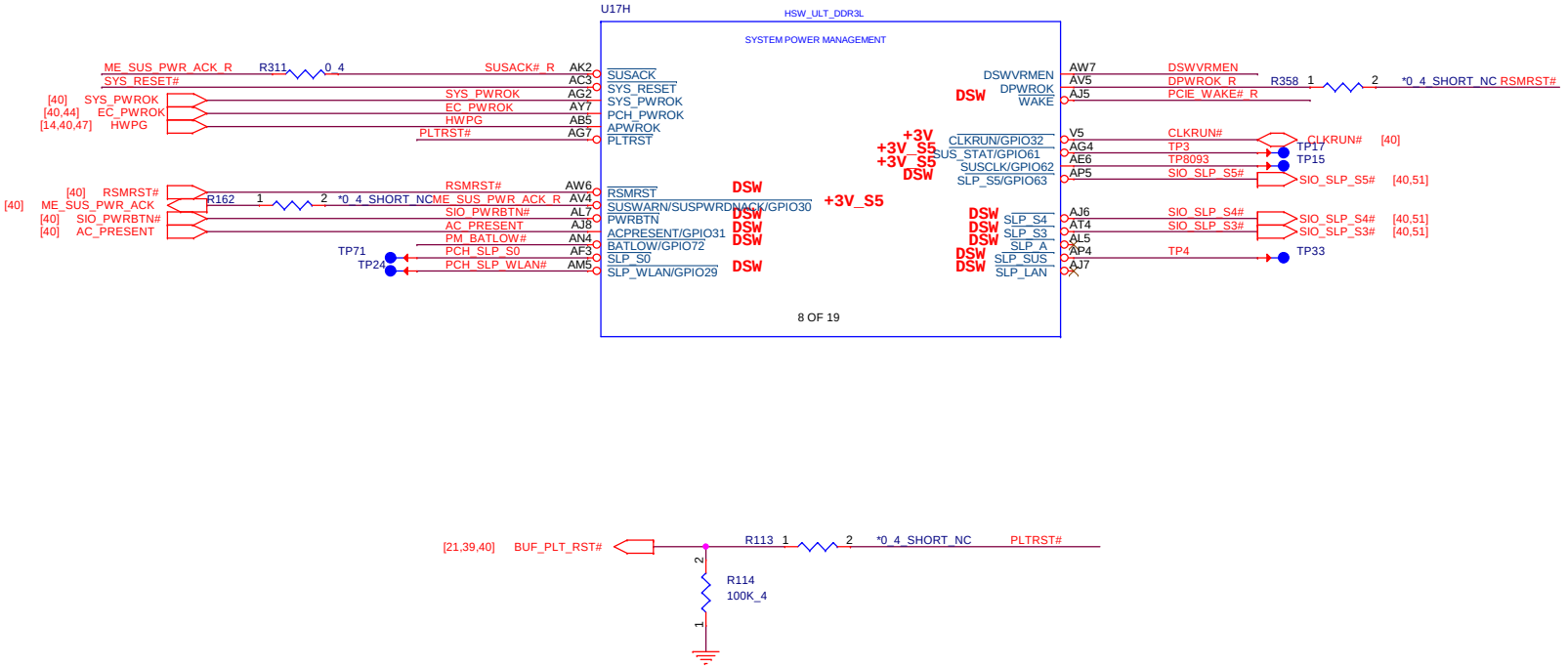
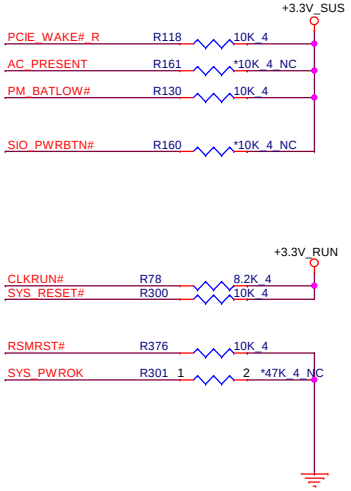
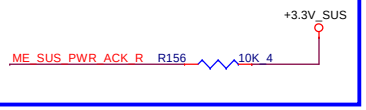
Haswell ULT (SYSTEM POWER MANAGEMENT)



PCH Pull-high/low(CLG)



Deep Sleep will be turn off



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
DSWVRMEN	DeepSx Well On-Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	1. This signal is always sampled. 2. This signal is in the RTC well.

+RTC_CELL 330K_4 R372 DSWVRMEN

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	Haswell ULT 7/12	A

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Haswell ULT MCP(POWER)

CPU VDDQ

Haswell ULT 15W & 28W: 1.4A

6X10UF MLCC
4X2.2UF MLCC

CPU VCC

Haswell ULT 15W : 32A
28W : 40A

24 X 10UF(0603 MLCC)

U17L — HSW_ULT_DDR3L

1.4A

32A

HSW ULT POWER

12 OF 19

VCOMP_OUT(+VCCIOA_OUT) only be used to connect eDP_RCOMP.

+V1.05S_VCCST

SVID ALERT

CLOSE TO CPU

SVID DATA

CLOSE TO CPU

CLOSE TO VR

SVID CLK

CLOSE TO VR

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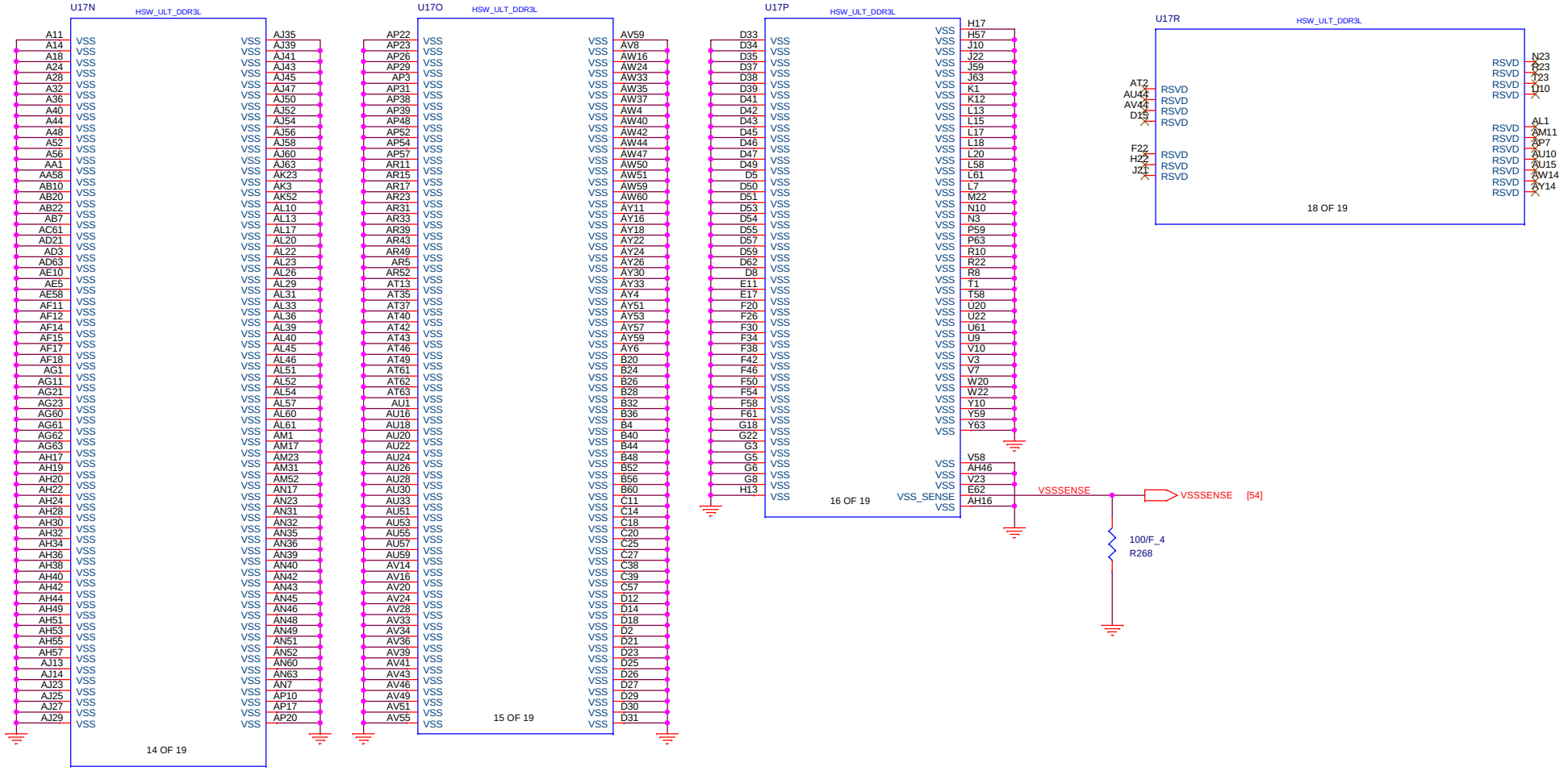
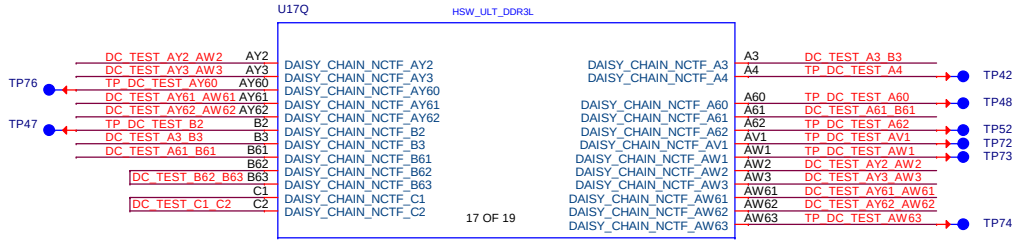
Haswell ULT (GND)





Quanta Computer Inc.		
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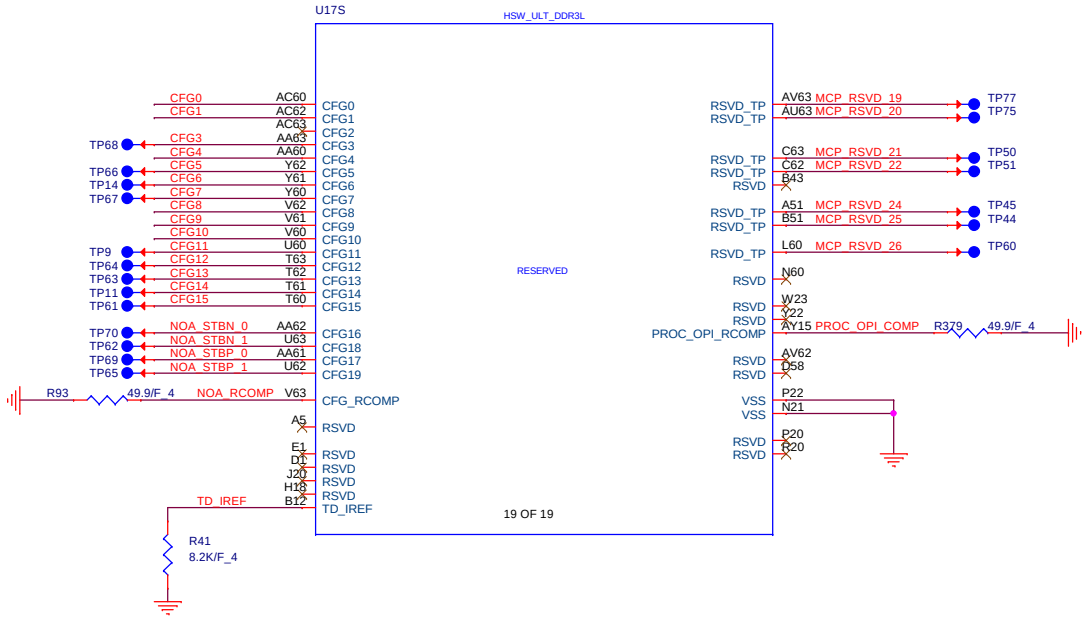

Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	
CFG0 Reserved	(DEFAULT) NORMAL OPERATION		CFG0 R108 *1K_4_NC
CFG1 Reserved	(DEFAULT) NORMAL OPERATION		CFG1 R297 *1K_4_NC
CFG2 Reserved	(DEFAULT) NORMAL OPERATION		
CFG3 MSR Privacy Bit Feature	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	CFG3 R293 *1K_4_NC
CFG4 eDP enable	Disabled	Enabled	CFG4 R107 1K_4
CFG[19:5] Reserved	(DEFAULT) NORMAL OPERATION		CFG8 R92 *1K_4_NC
			CFG9 R294 *1K_4_NC
			CFG10 R100 *1K_4_NC

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	Haswell ULT 10/12	A

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Haswell ULT PCH(POWER)

3.3 SUS: 205mA
1.05 SUS: 2066mA
1.05 RUN: 2578mA
3.3 RUN: 58mA

U17M — HSW_ULT_DDR3L — 13 OF 19

VCCHSIO, VCCHSIO, VCCHSIO	1.838A
VCC1_05	41mA
VCCUSB3PLL	42mA
VCCSATA3PLL	
RSVD, VCCAPLL, VCCAPLL	57mA
DCPSUS3	10mA
VCCHDA	11mA
DCPSUS2	25mA
VCCSUS3_3, VCCSUS3_3	62mA
VCCDSW3_3	119mA
VCC3_3, VCC3_3	
VCCCLK, VCCCLK, VCCACLKPLL, VCCCLK, VCCCLK, VCCCLK, RSVD, RSVD, RSVD, VCCSUS3_3, VCCSUS3_3	185mA, 31mA
RTC: VCCSUS3_3, VCCRTC, DCPRTC	1mA
SPI: VCCSPI	18mA
VCCASW, VCCASW	
CORE: VCC1_05 ×5, DCPSUSBYP, DCPSUSBYP	1.954A
VCCASW ×3	658mA
DCPSUS1, DCPSUS1	109mA
THERMAL SENSOR: VCCTS1_5, VCC3_3, VCC3_3	3mA, 41mA
SERIAL IO: VCCSDIO, VCCSDIO	17mA
SUS OSCILLATOR: DCPSUS4	1mA
USB2: RSVD, VCC1_05, VCC1_05	

Deep Sleep will be turn off — +3.3V_SUS → RTC_CELL

Deep Sleep will be turn off — +3.3V_SUS

Deep Sleep will be turn off — +3.3V_SUS

*C80-->4.7U

boot strap capacitor	VCCDSW3_3 C233 0.47U/6.3V_4 +DCPSUSBYP

1mA

41mA

42mA

*-->4.7U

Q6 FDMC7678 — Q7 AP2319GN-HF — Q5 DMN601WK-7 — Q4A 2N7002KDW — Q4B 2N7002KDW

[9] MODPHY_EN

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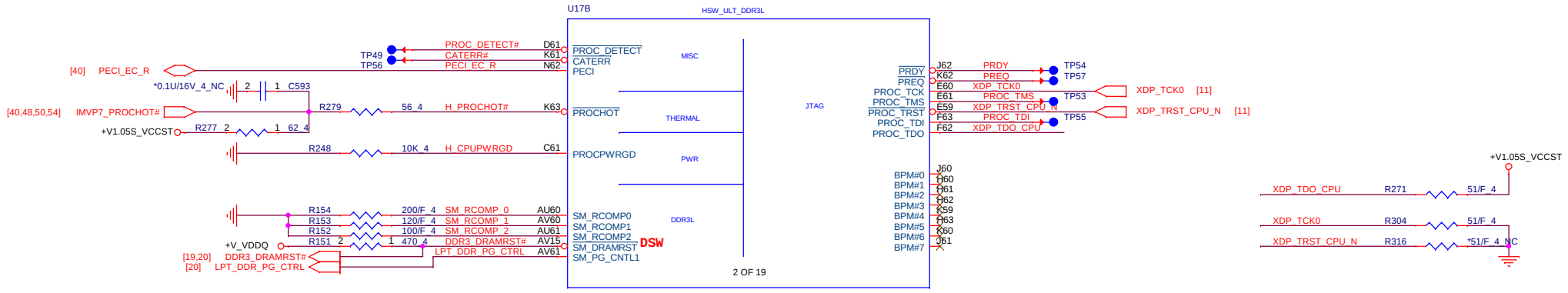

Quanta Computer Inc.		
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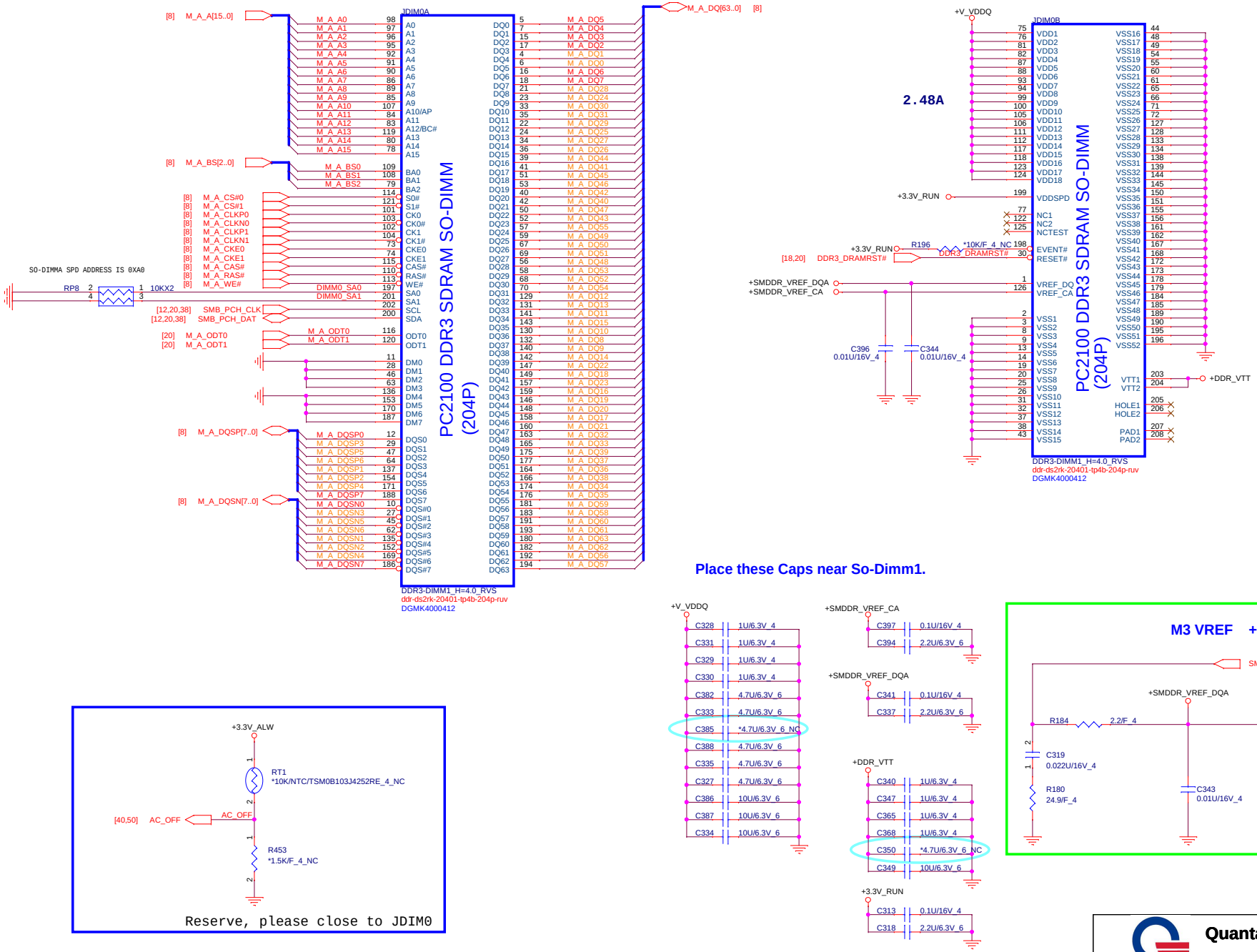

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	DDR3 DIMM1-RVS (4.0H)	A

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JDIM1A — PC2100 DDR3 SDRAM SO-DIMM (204P)

SO-DIMMB SPD ADDRESS IS 0XA4

R182 10K/F_4, R183 10K/F_4 — +3.3V_RUN

[12,19,38] SMB_PCH_CLK
[12,19,38] SMB_PCH_DAT

Pin	Signal	Pin	Signal
98	M_B_A0	5	M_B_DQ0
97	M_B_A1	7	M_B_DQ5
96	M_B_A2	15	M_B_DQ6
95	M_B_A3	17	M_B_DQ7
92	M_B_A4	4	M_B_DQ4
91	M_B_A5	6	M_B_DQ1
90	M_B_A6	16	M_B_DQ3
86	M_B_A7	18	M_B_DQ2
89	M_B_A8	21	M_B_DQ27
85	M_B_A9	23	M_B_DQ24
107	M_B_A10	33	M_B_DQ28
84	M_B_A11	35	M_B_DQ30
83	M_B_A12	22	M_B_DQ26
119	M_B_A13	24	M_B_DQ25
80	M_B_A14	34	M_B_DQ29
78	M_B_A15	36	M_B_DQ31
		39	M_B_DQ39
		41	M_B_DQ33
		51	M_B_DQ34
		53	M_B_DQ38
		40	M_B_DQ36
		42	M_B_DQ32
		50	M_B_DQ35
		52	M_B_DQ37
		57	M_B_DQ43
		59	M_B_DQ40
		67	M_B_DQ47
		69	M_B_DQ42
		56	M_B_DQ44
		58	M_B_DQ41
		68	M_B_DQ46
		70	M_B_DQ45
		129	M_B_DQ56
		131	M_B_DQ61
		141	M_B_DQ60
		143	M_B_DQ58
		130	M_B_DQ59
		132	M_B_DQ57
		140	M_B_DQ62
		142	M_B_DQ63
		147	M_B_DQ8
		149	M_B_DQ13
		157	M_B_DQ10
		159	M_B_DQ11
		146	M_B_DQ12
		148	M_B_DQ9
		158	M_B_DQ14
		160	M_B_DQ15
		163	M_B_DQ21
		165	M_B_DQ16
		175	M_B_DQ18
		177	M_B_DQ19
		164	M_B_DQ20
		166	M_B_DQ17
		174	M_B_DQ22
		176	M_B_DQ23
		181	M_B_DQ49
		183	M_B_DQ52
		191	M_B_DQ53
		193	M_B_DQ48
		180	M_B_DQ50
		182	M_B_DQ51
		192	M_B_DQ54
		194	M_B_DQ55

M_B_DQ[63..0] [8]

M_B_BS[2..0] [8]: M_B_BS0 109, M_B_BS1 108, M_B_BS2 79

M_B_CS#0 [8] 114, M_B_CS#1 [8] 121, M_B_CLKP0 [8] 101, M_B_CLKN0 [8] 103, M_B_CLKP1 [8] 102, M_B_CLKN1 [8] 104, M_B_CKE0 [8] 73, M_B_CKE1 [8] 74, M_B_CAS# [8] 115, M_B_RAS# [8] 110, M_B_WE# [8] 113

DIMM1_SA0 197, DIMM1_SA1 201

M_B_ODT0 116, M_B_ODT1 120

M_B_DQSP[7..0] [8]: M_B_DQSP0 12, M_B_DQSP3 29, M_B_DQSP4 47, M_B_DQSP5 64, M_B_DQSP7 137, M_B_DQSP1 154, M_B_DQSP2 171, M_B_DQSP6 188

M_B_DQSN[7..0] [8]: M_B_DQSN0 10, M_B_DQSN3 27, M_B_DQSN4 45, M_B_DQSN5 62, M_B_DQSN7 135, M_B_DQSN1 152, M_B_DQSN2 169, M_B_DQSN6 186

DDR3-DIMM1_H=4.0_RVS
ddr-ds2rk-20401-tp4b-204p-ruv
DGMK4000412

JDIM1B — PC2100 DDR3 SDRAM SO-DIMM (204P)

+V_VDDQ

Pin	Signal	Pin	Signal
75	VDD1	44	VSS16
76	VDD2	48	VSS17
81	VDD3	49	VSS18
82	VDD4	54	VSS19
87	VDD5	55	VSS20
88	VDD6	60	VSS21
93	VDD7	61	VSS22
94	VDD8	65	VSS23
99	VDD9	66	VSS24
100	VDD10	71	VSS25
105	VDD11	72	VSS26
106	VDD12	127	VSS27
111	VDD13	128	VSS28
112	VDD14	133	VSS29
117	VDD15	134	VSS30
118	VDD16	138	VSS31
123	VDD17	139	VSS32
124	VDD18	144	VSS33
		145	VSS34
199	VDDSPD	150	VSS35
		151	VSS36
77	NC1	155	VSS37
122	NC2	156	VSS38
125	NCTEST	161	VSS39
		162	VSS40
198	EVENT#	167	VSS41
30	RESET#	168	VSS42
		172	VSS43
1	VREF_DQ	173	VSS44
126	VREF_CA	178	VSS45
		179	VSS46
2	VSS1	184	VSS47
3	VSS2	185	VSS48
8	VSS3	189	VSS49
9	VSS4	190	VSS50
13	VSS5	195	VSS51
14	VSS6	196	VSS52
19	VSS7		
20	VSS8	203	VTT1
25	VSS9	204	VTT2
26	VSS10		
31	VSS11	205	HOLE1
32	VSS12	206	HOLE2
37	VSS13		
38	VSS14	207	PAD1
43	VSS15	208	PAD2

2.48A

+3.3V_RUN — R197 *10K/F_4_NC — [18,19] DDR3_DRAMRST#

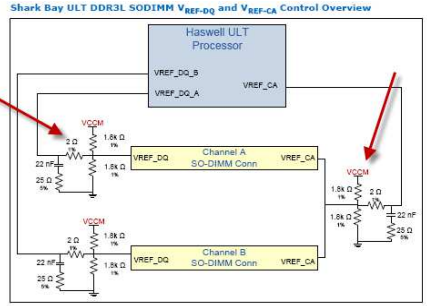
+SMDDR_VREF_DQB
+SMDDR_VREF_CA

C369 0.01U/16V_4, C345 0.01U/16V_4

+DDR_VTT

DDR3-DIMM1_H=4.0_RVS
ddr-ds2rk-20401-tp4b-204p-ruv
DGMK4000412

Figure 91. Shark Bay ULT DDR3L SODIMM V_{REF-DQ} and V_{REF-CA} Control Overview



M3 VREF + M1 VREF

+V_VDDQ

SM_VREF_DQ1 [8]

+SMDDR_VREF_DQB

R177 2.2/F_4

C311 0.022U/16V_4

R178 24.9/F_4

C339 0.01U/16V_4

R179 1.8K/F_4

R181 1.8K/F_4

M3 VREF + M1 VREF

+V_VDDQ

SM_VREF_CA [8]

+SMDDR_VREF_CA

R198 2.2/F_4

C398 0.022U/16V_4

R200 24.9/F_4

C367 0.01U/16V_4

R195 1.8K/F_4

R194 1.8K/F_4

DDR3L SODIMM ODT GENERATION

Q27 — 2N7002KDW

R427 22_4 — +DDR_VTT

DDR_PG_CTRL

R440 2_100K_4 — +5V_ALW

The 74AUP1G07 provides the single non-inverting buffer with open-drain output.

[18] LPT_DDR_PG_CTRL — R437 *0_4_SHORT_NC — R430 *0_4_NC

U24 74AUP1G07GW (NC, A, GND, VCC, Y)

C588 0.1U/16V_4

+V_VDDQ

+5V_ALW — R431 220K/F_4

+V_VDDQ

Q28 DMN601WK-7

DDR_PG_CTRL

[51] DDR_PG_CTRL — R438 2M_4

[19] M_A_ODT0
[19] M_A_ODT1

M_A_ODT0 — R436 66.5/F_4
M_A_ODT1 — R435 66.5/F_4
M_B_ODT0 — R434 66.5/F_4
M_B_ODT1 — R439 66.5/F_4

M_A_B_DIMM_ODT

Place these Caps near So-Dimm2.

+V_VDDQ

C322	1U/6.3V_4
C325	1U/6.3V_4
C383	1U/6.3V_4
C384	1U/6.3V_4
C391	4.7U/6.3V_6
C324	4.7U/6.3V_6
C323	*4.7U/6.3V_6_NC
C390	4.7U/6.3V_6
C392	4.7U/6.3V_6
C326	4.7U/6.3V_6
C321	10U/6.3V_6
C389	10U/6.3V_6
C393	10U/6.3V_6

+SMDDR_VREF_CA

C395	0.1U/16V_4
C400	2.2U/6.3V_6

+SMDDR_VREF_DQB

C336	0.1U/16V_4
C316	2.2U/6.3V_6

+DDR_VTT

C320	1U/6.3V_4
C332	1U/6.3V_4
C364	1U/6.3V_4
C366	1U/6.3V_4
C338	*4.7U/6.3V_6_NC
C346	10U/6.3V_6

+3.3V_RUN

C314	0.1U/16V_4
C315	2.2U/6.3V_6

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	DDR3 DIMM2-RVS (4.0H)	A

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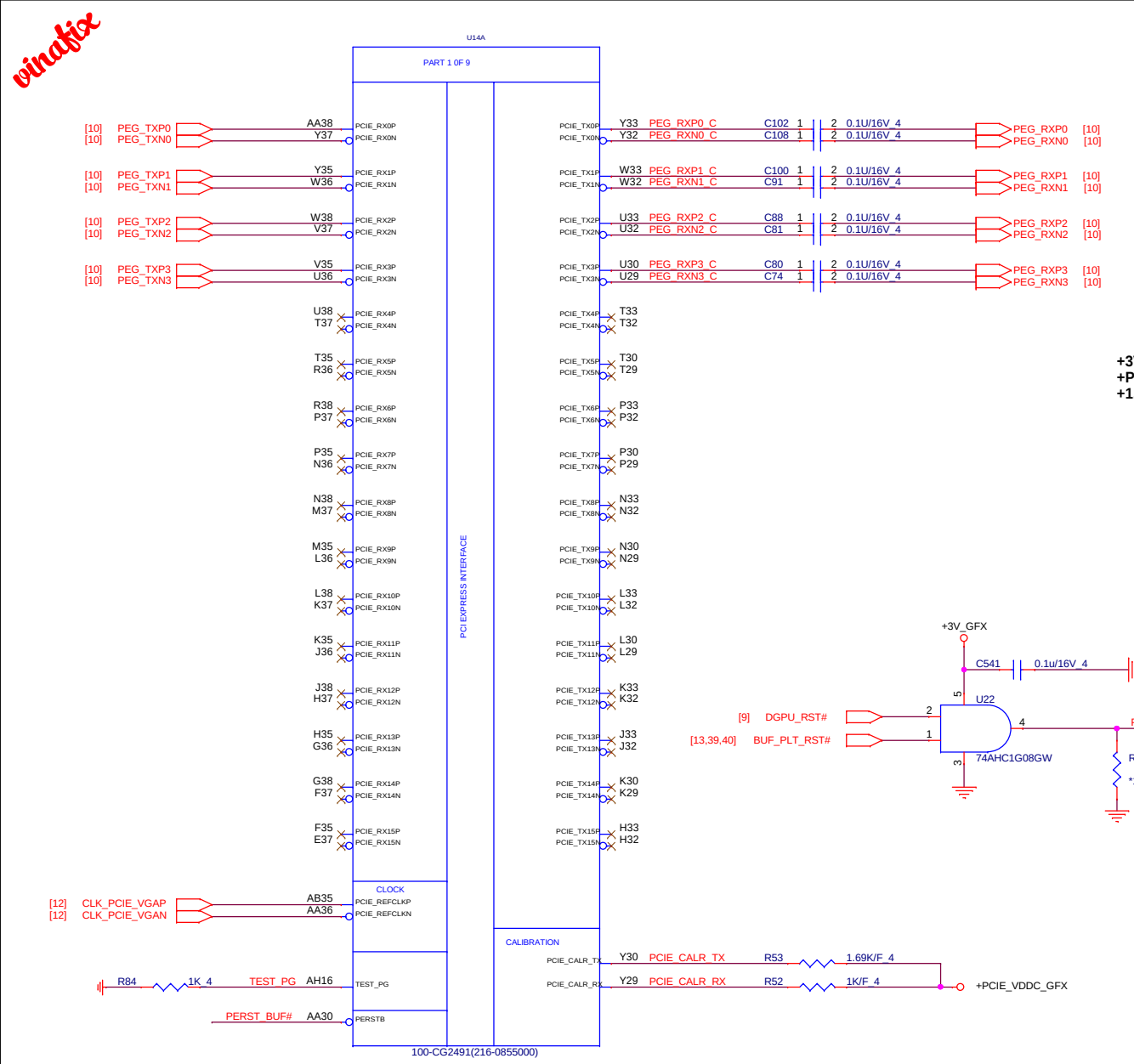
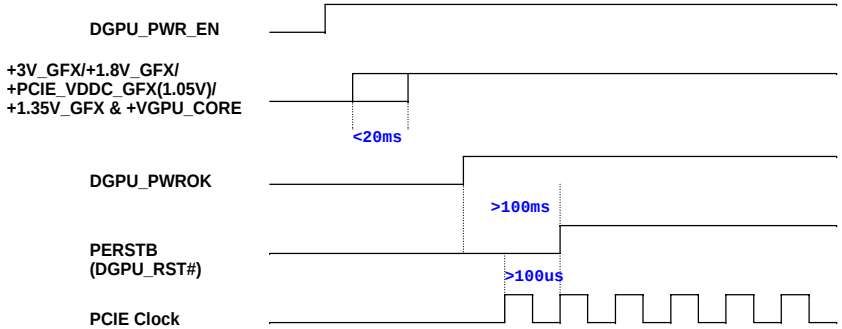
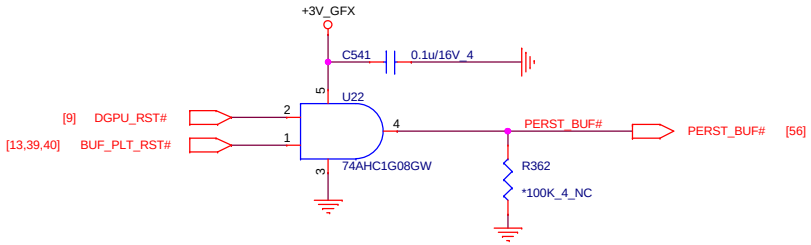


Opal XT Power-on sequence





Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: Opal_XT/PEG*16	Rev: A
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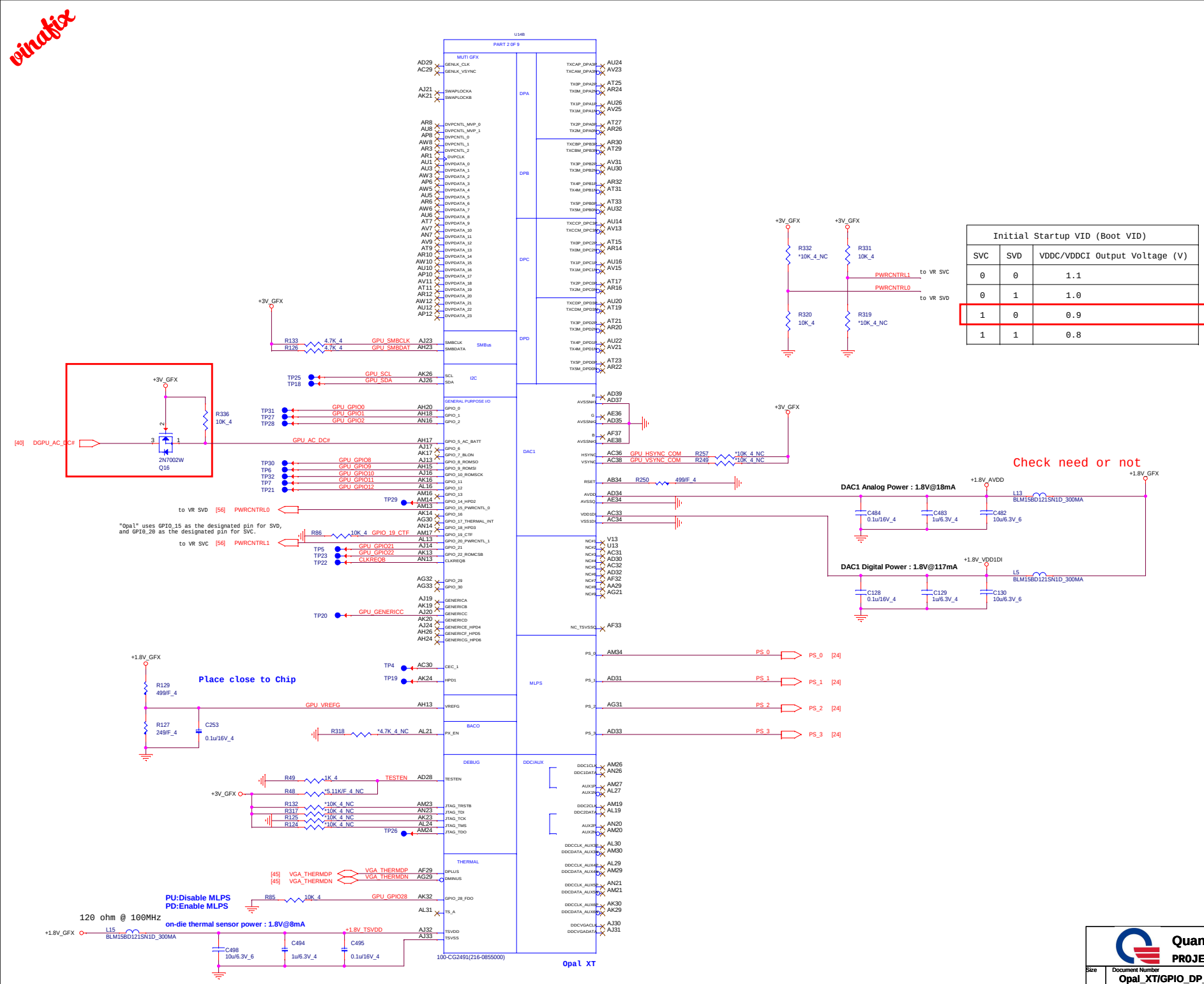

Initial Startup VID (Boot VID)		
SVC	SVD	VDDC/VDDCI Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Quanta Computer Inc.
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Size	Document Number	Rev
	Opal_XT/GPIO_DP_CRT_I2C	A

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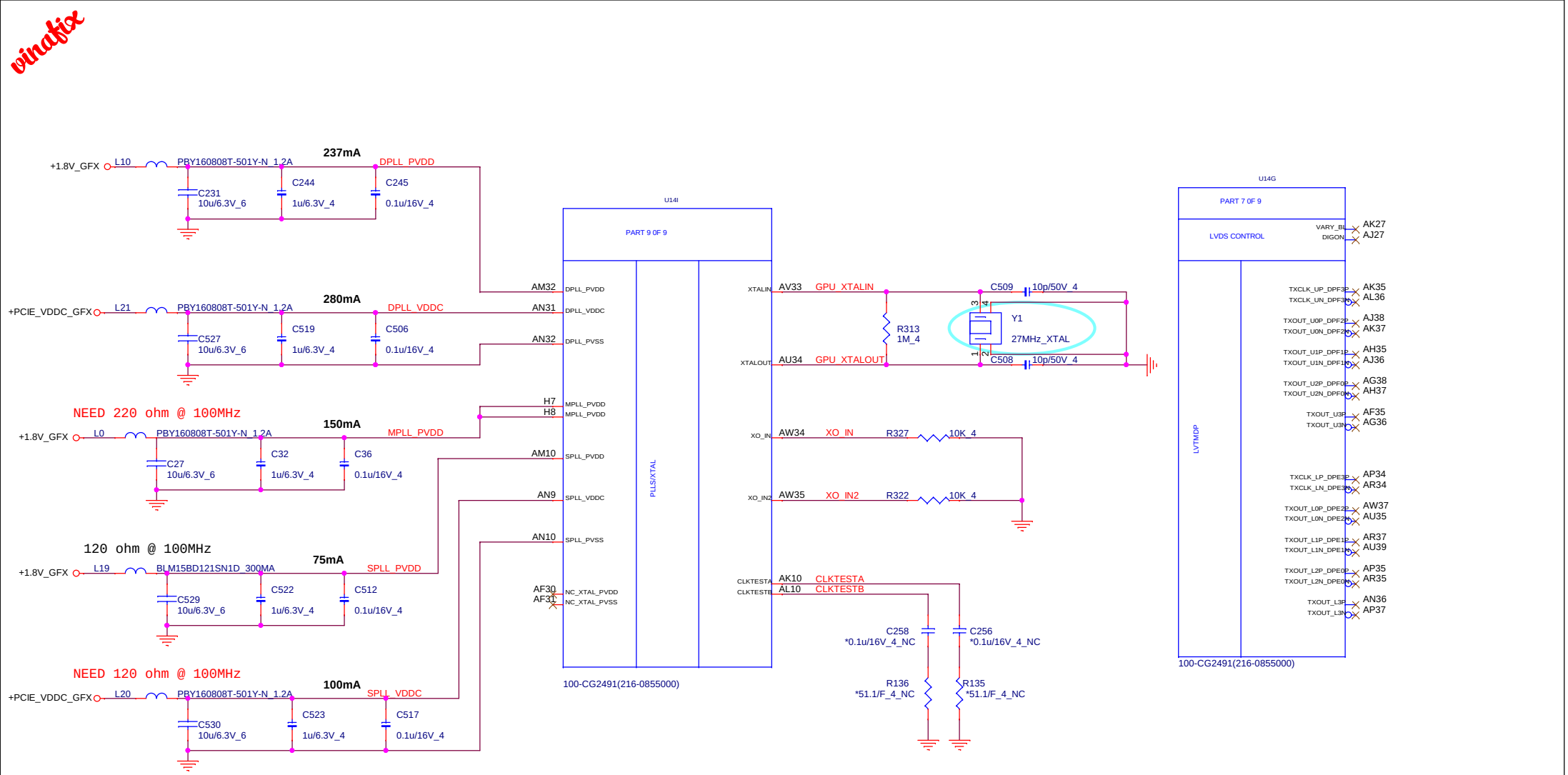

Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	Opal_XT/XTAL_LVDS	A

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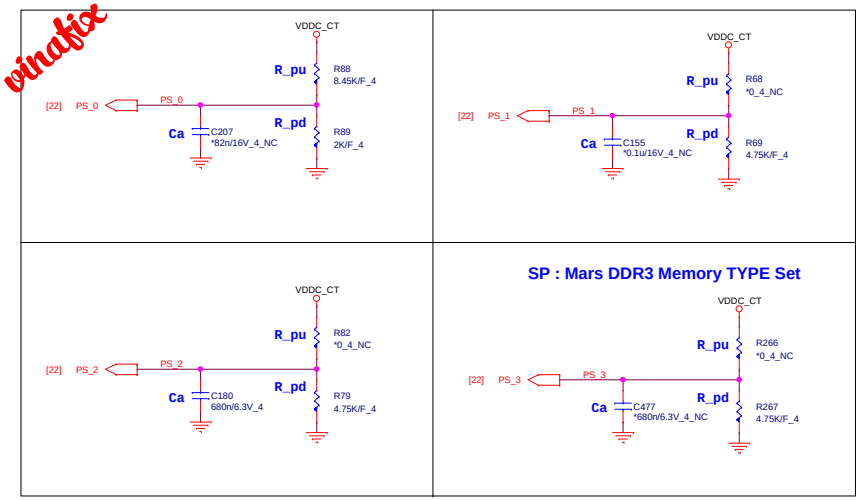

MLPS Bit	Bits [5:1]
PS_0	11001
PS_1	11000
PS_2	00000
PS_3	11XXX

MLPS

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	NA

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

R_pu/R_pd	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

MLPS Bit	Strap Name	AM6 Settings	AM6 Settings	Description	AMD Recommended Settings
PS_0[1]	ROM_CONFIG[0]	1	Memory Aperture Size Select : 256MB	Serial ROM type or Memory Aperture Size Select If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size.	Design dependent, SIZE ROM_CONFIG[2:0] 128MB 000 256MB 001 64MB 010 Reserved 011
PS_0[2]	ROM_CONFIG[1]	0			
PS_0[3]	ROM_CONFIG[2]	0			
PS_0[4]	N/A	1	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	1	All endpoints are usable.	the strap option indicates the number of audio-capable display outputs.	Design dependent
PS_1[1]	STRAP_BIF_GEN3_EN_A	0	PCIe GEN3 is not supported. (use GEN2)	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent
PS_1[2]	STRAP_BIF_CLK_PM_EN	0	The CLKREQB power management capability is disabled	Determines whether or not the PCIe reference clock power management capability 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	0	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1	The transmitter full-swing is enabled	Control the transmitter full-/ half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	1	Tx deemphasis enabled.	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent
PS_2[1]	N/A	0	Reserved.	Reserved.	N/A
PS_2[2]	N/A	0	Reserved.	Reserved.	N/A
PS_2[3]	STRAP_BIOS_ROM_EN	0	Disable the external BIOS ROM device.	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent
PS_2[4]	STRAP_BIF_VGA_DIS	0	Standalone dGPU design	VGA disable determines whether or not the card will be recognized as the system's VGA controller 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	Standalone dGPU design = 0 AMD PowerXpress design = 1
PS_2[5]	N/A	0	Reserved.	Reserved.	N/A
PS_3[1]	BOARD_CONFIG[0]	X	VRAM vendor BOARD_CONFIG[2:0] Hynix 000 default Micron 001 Samsung 010	Board configuration related strapping, such as for memory ID	Design dependent
PS_3[2]	BOARD_CONFIG[1]	X			
PS_3[3]	BOARD_CONFIG[2]	X			
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	1	No usable endpoints.	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	1			

System Memory Aperture size

GPIO9 BIOSROM	SIZE	GPIO13 ROM_CONFIG2	GPIO12 ROM_CONFIG1	GPIO11 ROM_CONFIG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	Reserved	0	1	1

Vendor	Vendor P/N	STN B/S P/N	Size	Opal USE MLPS
Hynix	H5TC4G63AFR-11C (256M*16)	AKD5PGWTW11 * 8	4GB	000
Micron	MT41J256M16HA-093G:E (256M*16)	AKD5PZSTL02 * 8	4GB	001
Samsung	K4W4G1646D-BC1A (256M*16)	AKD5PGWT500 * 8	4GB	010

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	Opal_XT/STRAPS_Thermal	A

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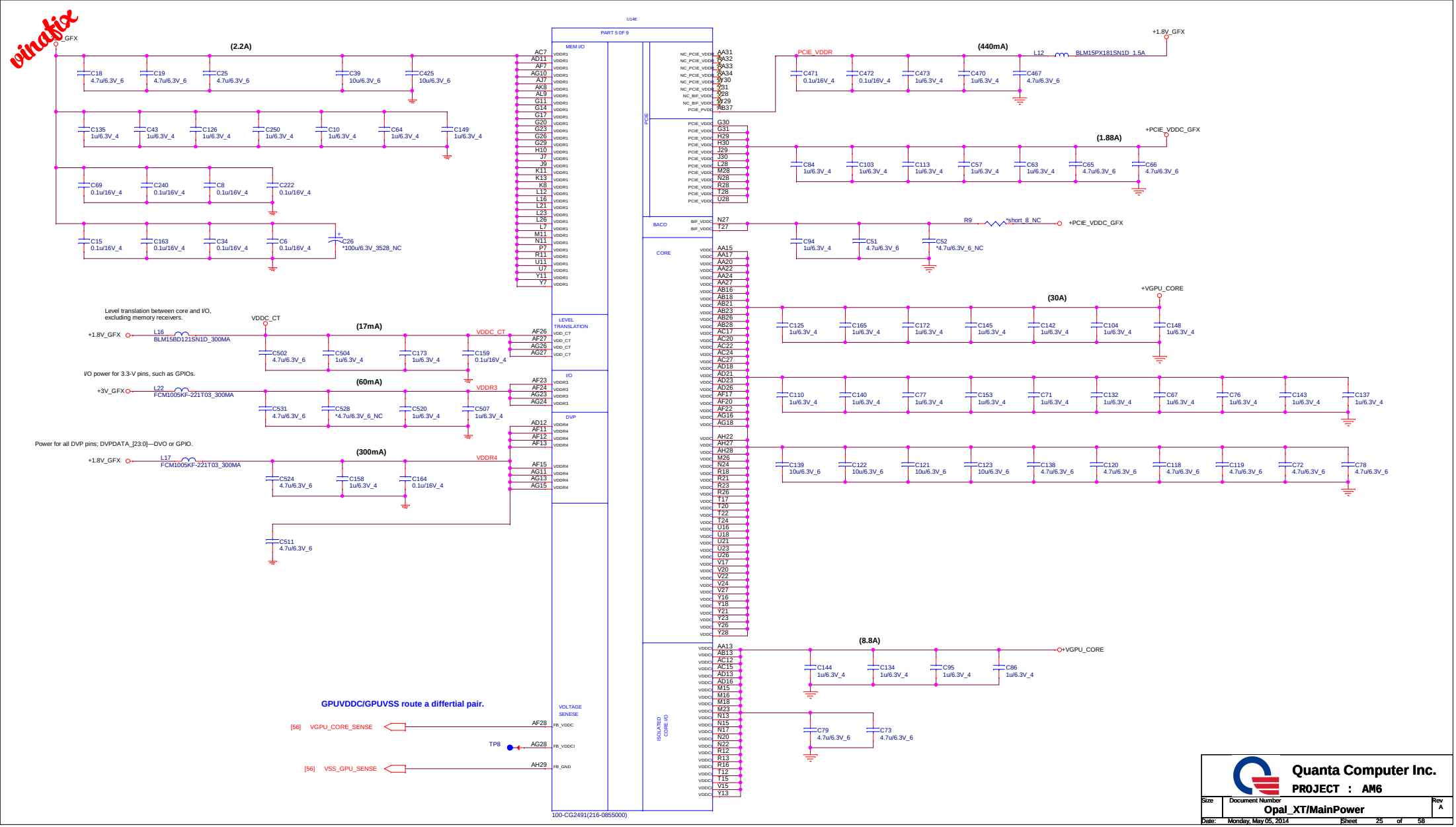
+1.8V_GFX
(2.2A)
C18 4.7u/6.3V_6
C19 4.7u/6.3V_6
C25 4.7u/6.3V_6
C39 10u/6.3V_6
C425 10u/6.3V_6
C135 1u/6.3V_4
C43 1u/6.3V_4
C126 1u/6.3V_4
C250 1u/6.3V_4
C10 1u/6.3V_4
C64 1u/6.3V_4
C149 1u/6.3V_4
C69 0.1u/16V_4
C240 0.1u/16V_4
C8 0.1u/16V_4
C222 0.1u/16V_4
C15 0.1u/16V_4
C163 0.1u/16V_4
C34 0.1u/16V_4
C6 0.1u/16V_4
C26 *100u/6.3V_3528_NC
U14E
PART 5 OF 9
MEM I/O
PCIE
BACO
CORE
LEVEL TRANSLATION
I/O
DVP
VOLTAGE SENSE
ISOLATED CORE I/O
Level translation between core and I/O, excluding memory receivers.
VDDC_CT
(17mA)
L16 BLM15BD121SN1D_300MA
C502 4.7u/6.3V_6
C504 1u/6.3V_4
C173 1u/6.3V_4
C159 0.1u/16V_4
I/O power for 3.3-V pins, such as GPIOs.
+3V_GFX
L22 FCM1005KF-221T03_300MA
(60mA)
C531 4.7u/6.3V_6
C528 *4.7u/6.3V_6_NC
C520 1u/6.3V_4
C507 1u/6.3V_4
Power for all DVP pins; DVPDATA_[23:0]—DVO or GPIO.
L17 FCM1005KF-221T03_300MA
(300mA)
C524 4.7u/6.3V_6
C158 1u/6.3V_4
C164 0.1u/16V_4
C511 4.7u/6.3V_6
GPUVDDC/GPUVSS route a differtial pair.
[56] VGPU_CORE_SENSE
TP8
[56] VSS_GPU_SENSE
100-CG2491(216-0855000)
PCIE_VDDR
(440mA)
L12 BLM15PX181SN1D_1.5A
C471 0.1u/16V_4
C472 0.1u/16V_4
C473 1u/6.3V_4
C470 1u/6.3V_4
C467 4.7u/6.3V_6
+PCIE_VDDC_GFX
(1.88A)
C84 1u/6.3V_4
C103 1u/6.3V_4
C113 1u/6.3V_4
C57 1u/6.3V_4
C63 1u/6.3V_4
C65 4.7u/6.3V_6
C66 4.7u/6.3V_6
R9 *short_8_NC
C94 1u/6.3V_4
C51 4.7u/6.3V_6
C52 *4.7u/6.3V_6_NC
+VGPU_CORE
(30A)
C125 1u/6.3V_4
C165 1u/6.3V_4
C172 1u/6.3V_4
C145 1u/6.3V_4
C142 1u/6.3V_4
C104 1u/6.3V_4
C148 1u/6.3V_4
C110 1u/6.3V_4
C140 1u/6.3V_4
C77 1u/6.3V_4
C153 1u/6.3V_4
C71 1u/6.3V_4
C132 1u/6.3V_4
C67 1u/6.3V_4
C76 1u/6.3V_4
C143 1u/6.3V_4
C137 1u/6.3V_4
C139 10u/6.3V_6
C122 10u/6.3V_6
C121 10u/6.3V_6
C123 10u/6.3V_6
C138 4.7u/6.3V_6
C120 4.7u/6.3V_6
C118 4.7u/6.3V_6
C119 4.7u/6.3V_6
C72 4.7u/6.3V_6
C78 4.7u/6.3V_6
(8.8A)
C144 1u/6.3V_4
C134 1u/6.3V_4
C95 1u/6.3V_4
C86 1u/6.3V_4
C79 4.7u/6.3V_6
C73 4.7u/6.3V_6
Quanta Computer Inc.
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Opal_XT/MainPower
Rev A
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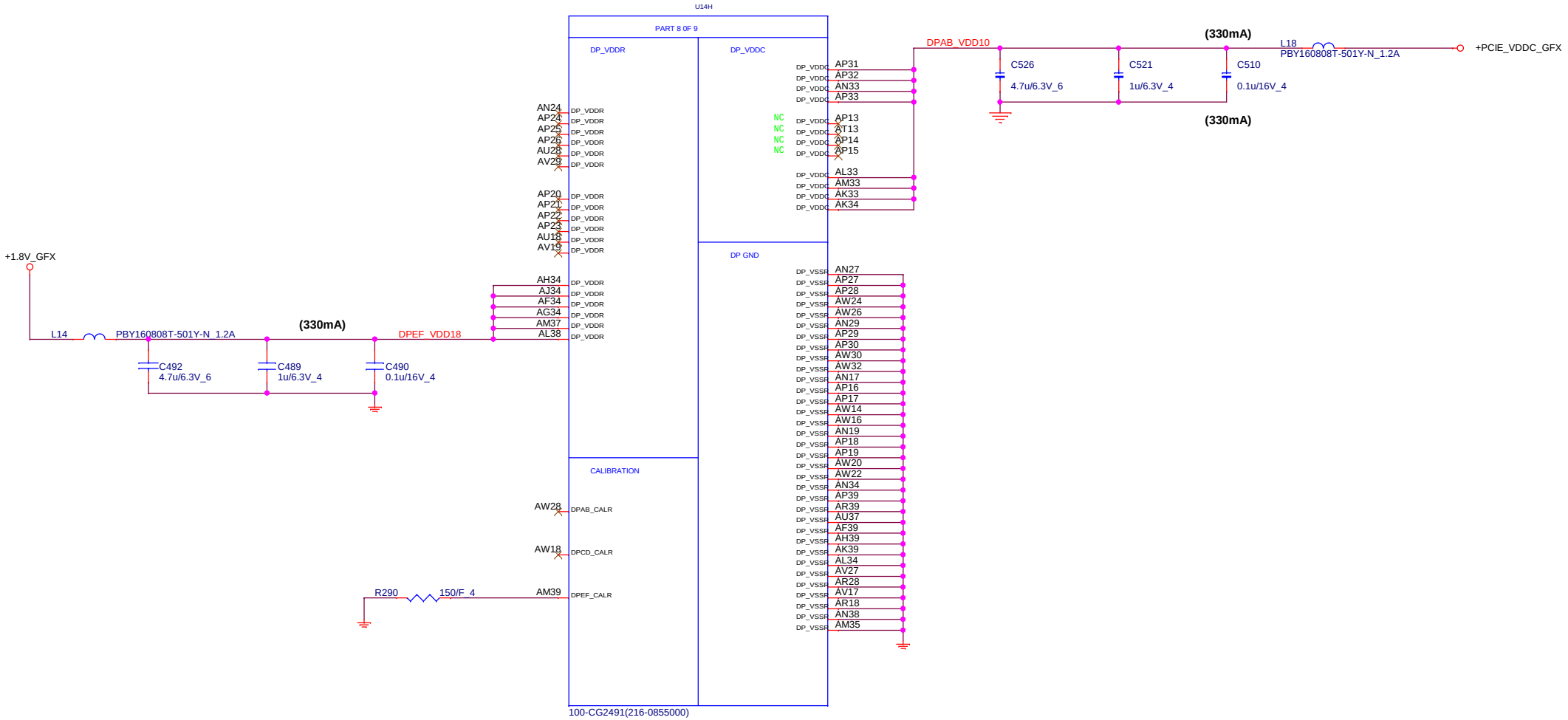

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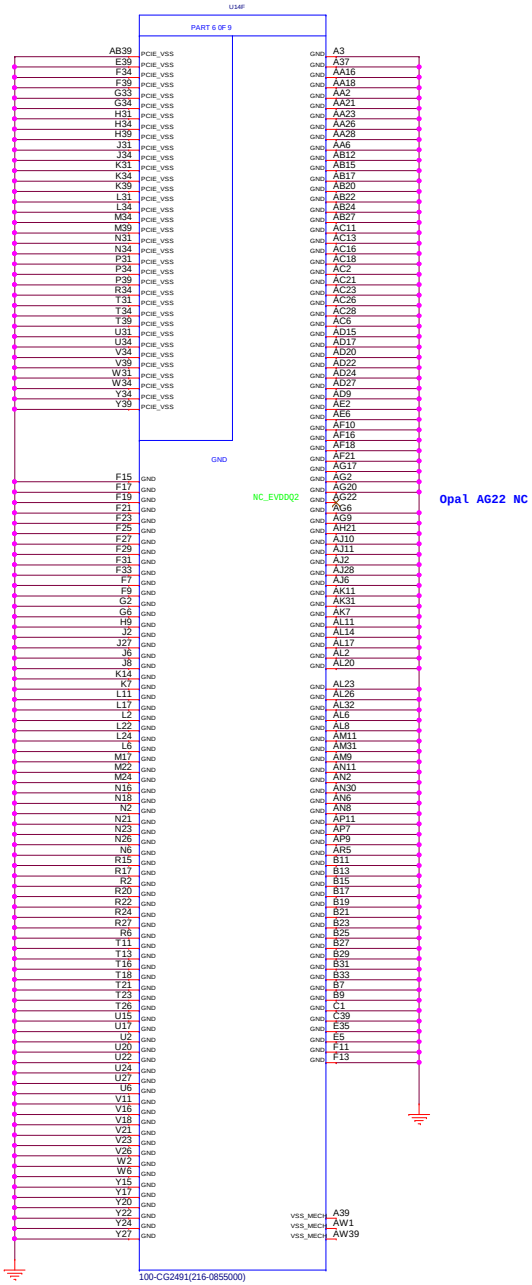
<VGA>



Opal AG22 NC

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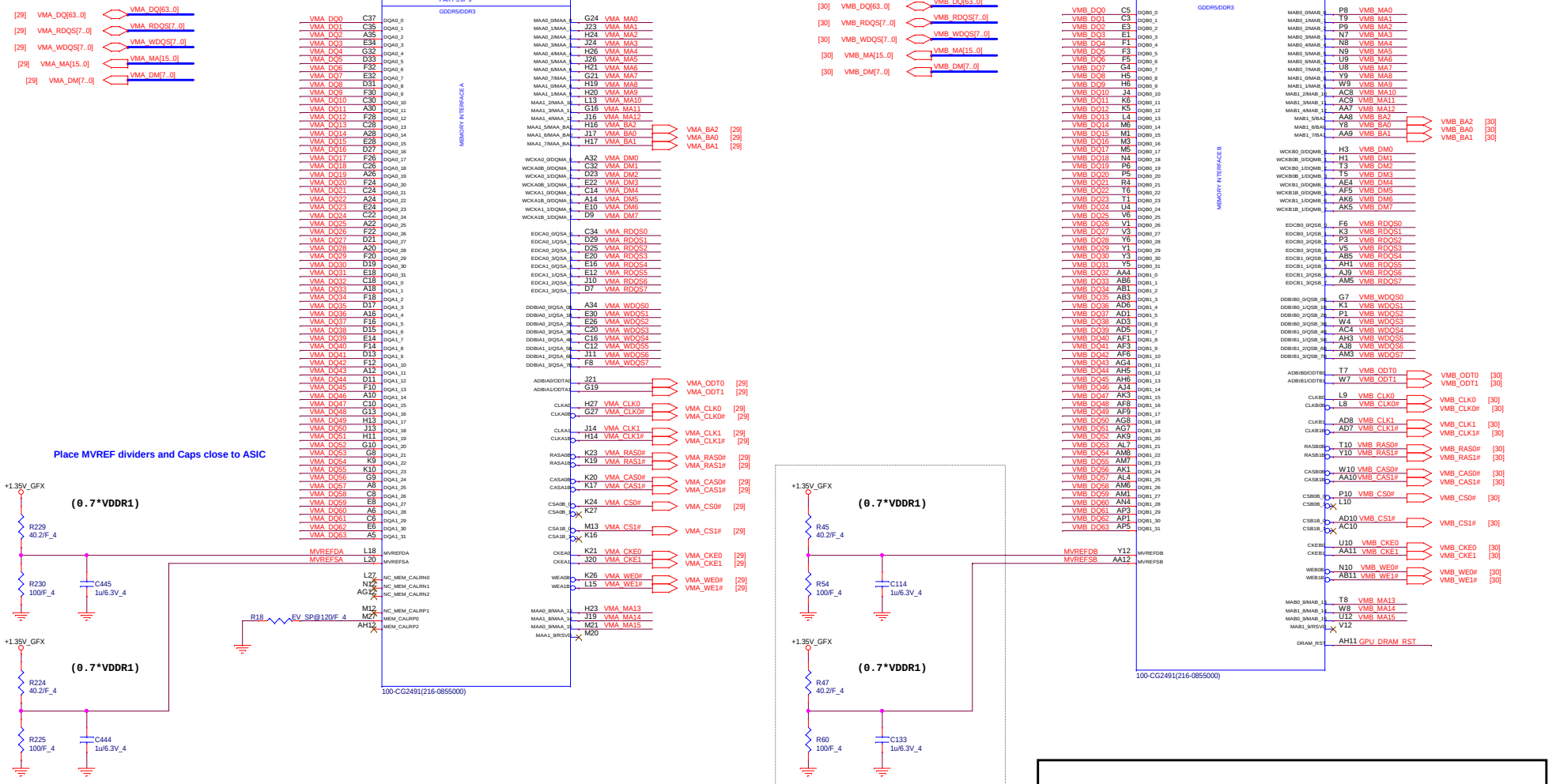
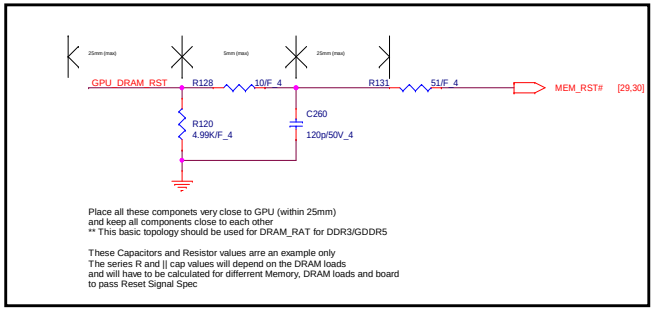
<VGA>





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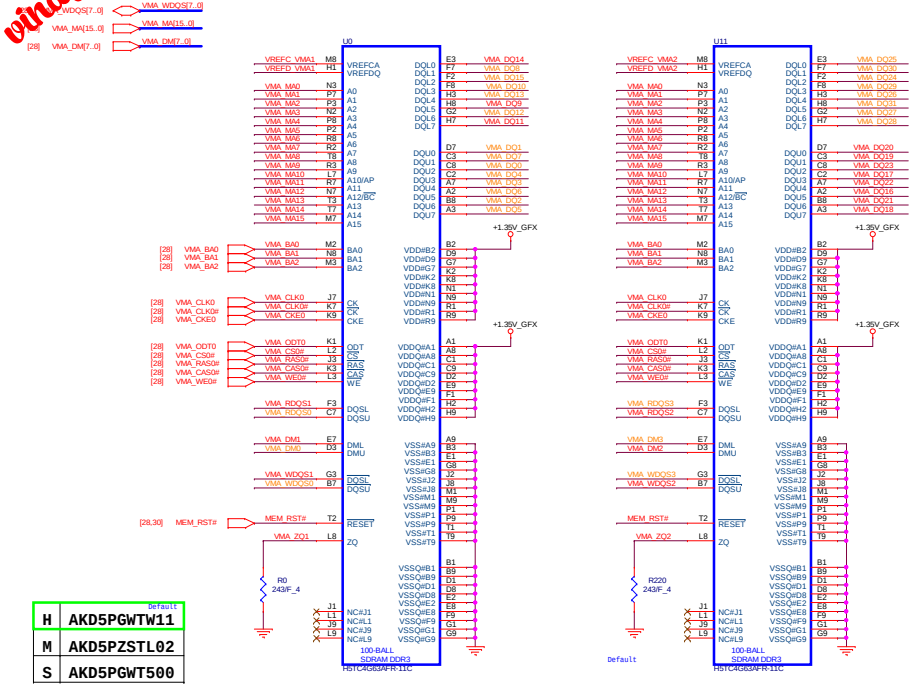
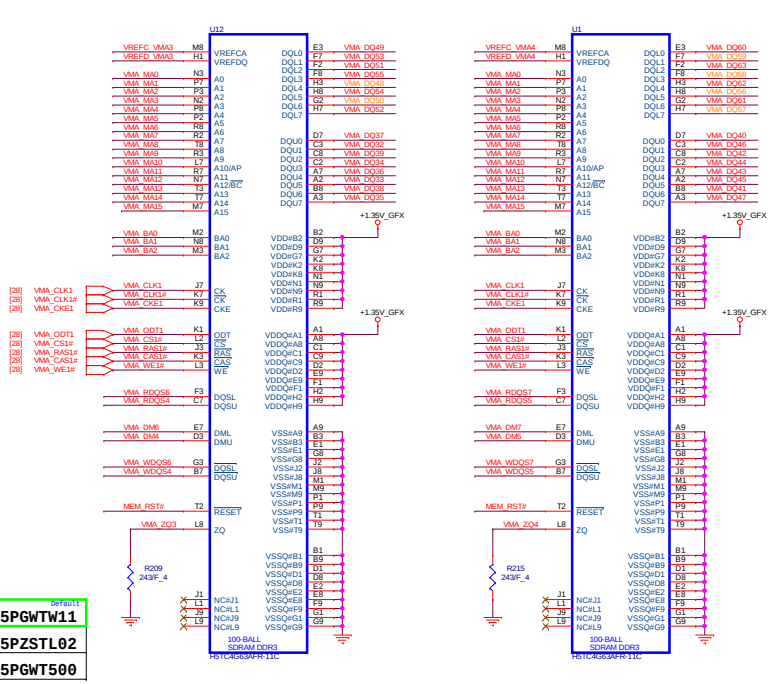
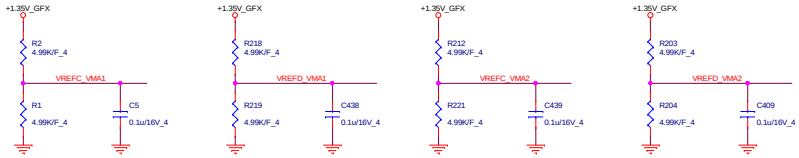
CHANNEL A: 2GB DDR3L (256Mb*16*4pcs)

	Default
H	AKD5PGWTW11
M	AKD5PZSTL02
S	AKD5PGWT500

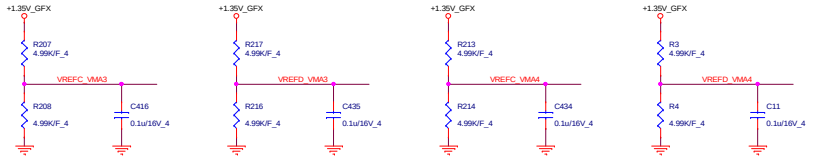




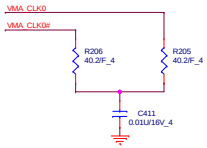
Group-A0 VREF



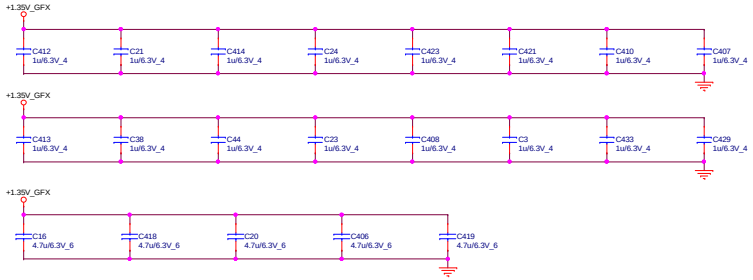
Group-A1 VREF



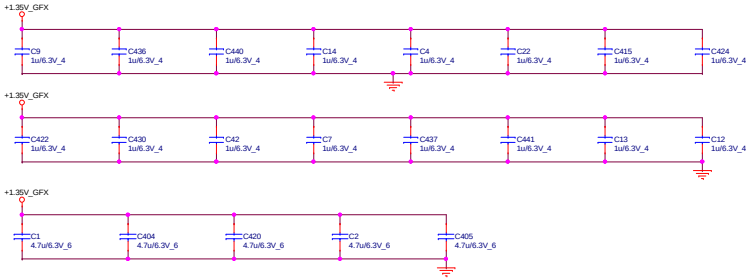
MEM_A0 CLK



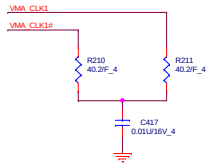
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	Opal_XT/VRAM_A	A

Date: Monday, May 05, 2014 Sheet 29 of 58

CHANNEL B: 2GB DDR3L (256Mb*16*4pcs)

	Default
H	AKD5PGWTW11
M	AKD5PZSTL02
S	AKD5PGWT500

BOT Down

TOP Down

TOP Up

BOT Up

Group-B0 VREF

Group-B1 VREF

MEM_B0 CLK

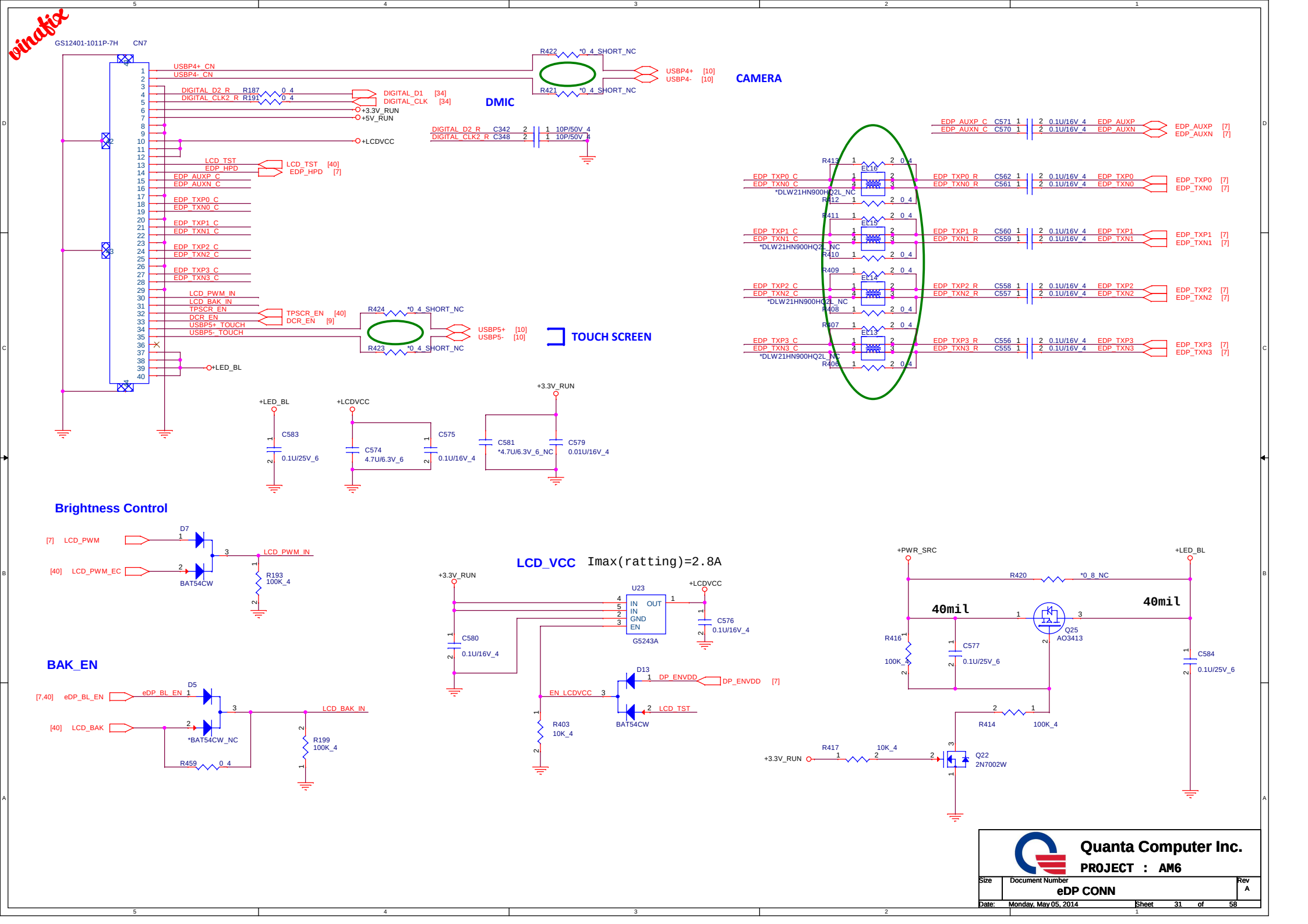
Group-B0 decoupling CAP

Group-B1 decoupling CAP

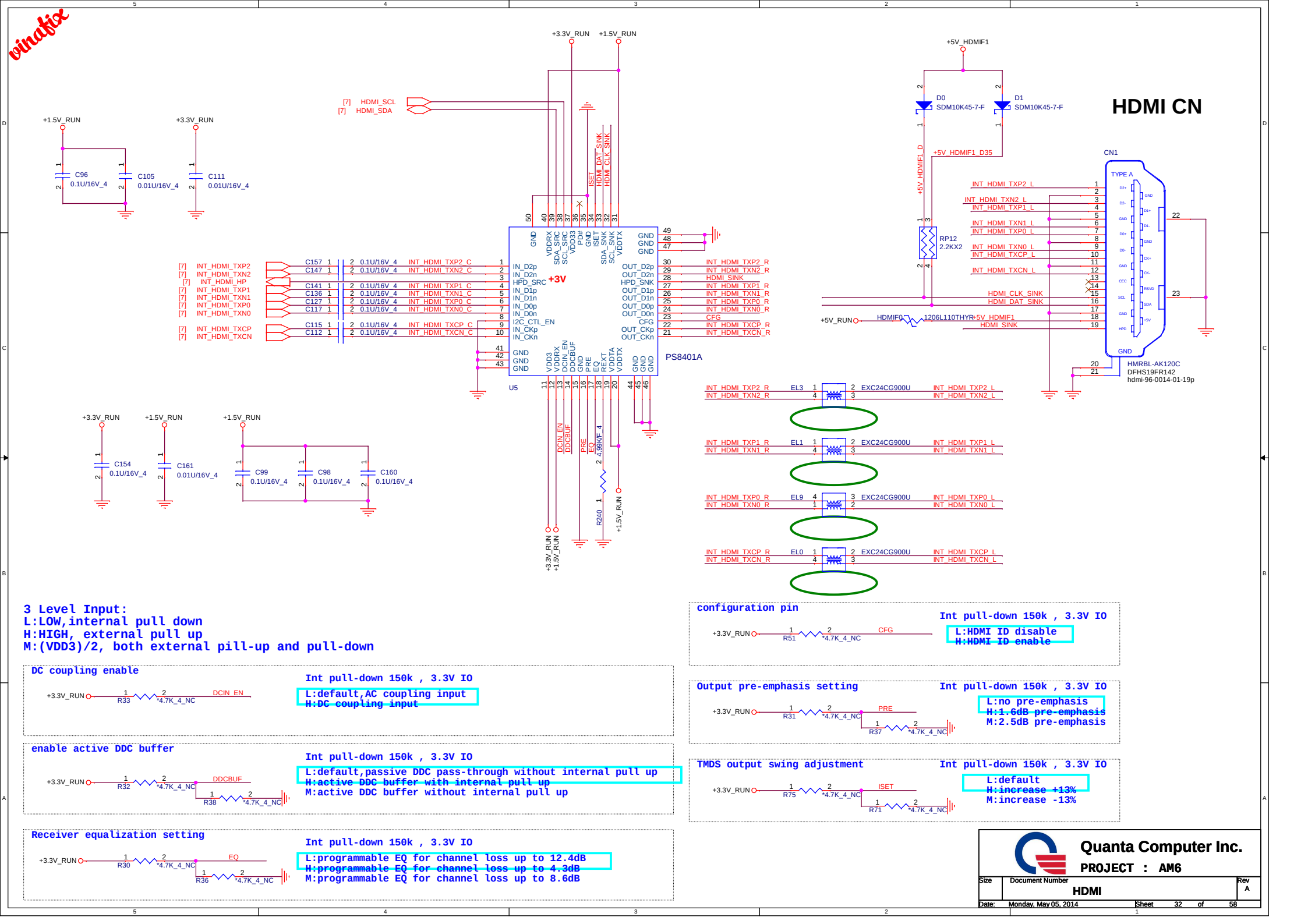
MEM_B1 CLK

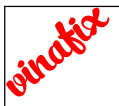
Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	Opal_XT/VRAM_B	A
Date: Monday, May 05, 2014	Sheet 30 of 58	



Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: eDP CONN	Rev: A
Date: Monday, May 05, 2014	Sheet 31 of 58	


HDMI CN
PS8401A
U5
CN1
TYPE A
HMRBL-AK120C
DFHS19FR142
hdmi-96-0014-01-19p
3 Level Input:
L:LOW,internal pull down
H:HIGH, external pull up
M:(VDD3)/2, both external pill-up and pull-down
DC coupling enable
Int pull-down 150k , 3.3V IO
L:default,AC coupling input
H:DC coupling input
enable active DDC buffer
Int pull-down 150k , 3.3V IO
L:default,passive DDC pass-through without internal pull up
H:active DDC buffer with internal pull up
M:active DDC buffer without internal pull up
Receiver equalization setting
Int pull-down 150k , 3.3V IO
L:programmable EQ for channel loss up to 12.4dB
H:programmable EQ for channel loss up to 4.3dB
M:programmable EQ for channel loss up to 8.6dB
configuration pin
Int pull-down 150k , 3.3V IO
L:HDMI ID disable
H:HDMI ID enable
Output pre-emphasis setting
Int pull-down 150k , 3.3V IO
L:no pre-emphasis
H:1.6dB pre-emphasis
M:2.5dB pre-emphasis
TMDS output swing adjustment
Int pull-down 150k , 3.3V IO
L:default
H:increase +13%
M:increase -13%
Quanta Computer Inc.
PROJECT : AM6
Size
Document Number
HDMI
Rev
A
Date: Monday, May 05, 2014
Sheet 32 of 58



H8
*H-C158D158N_NC

H6
*H-C158D158N_NC

H20
*h-o114x98d114x98n_NC

H1
*H-TC236BC197D98P2_NC

H0
*H-TC236BC197D98P2_NC

H7
*H-TC236BC197D98P2_NC

H4
*H-TC236BC197D98P2_NC

H9
*O-AM6-2_NC

H10
*h-c236i158d118p2_NC

H11
*h-c236i158d118p2_NC

H3
*h-c236i158d118p2_NC

H14
*h-c236i158d118p2_NC

H2
*H-TC236BC197D98P2_NC

H13
*O-AM6-1_NC

H12
*H-C118X98D118X98N_NC

H5
*H-C118X98D118X98N_NC

Bracket

HOLE0

*intel-CPU-bracket_NC

H17
H-TC217BC141D141PT

NGFF NUT

NUT

H15
H-TC217BC141D141PT

H16
H-TC217BC141D141PT

H18
H-TC217BC141D141PT

H19
H-TC217BC141D141PT

Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	Hole	A

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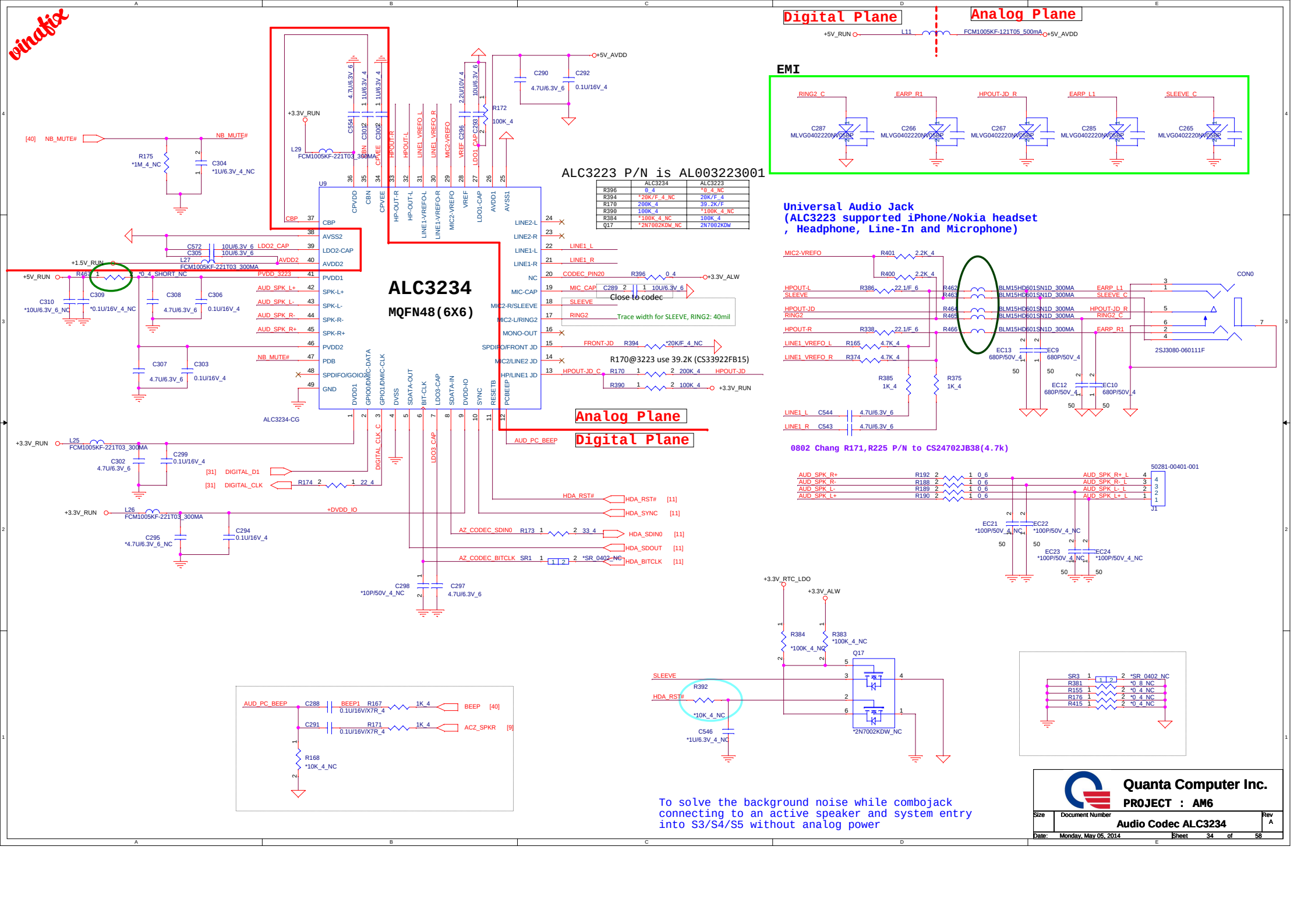
Digital Plane
Analog Plane
+5V_RUN
L11
FCM1005KF-121T05_500mA
+5V_AVDD
EMI
RING2_C
EARP_R1
HPOUT-JD_R
EARP_L1
SLEEVE_C
C287 MLVG0402220NV05BE
C266 MLVG0402220NV05BE
C267 MLVG0402220NV05BE
C285 MLVG0402220NV05BE
C265 MLVG0402220NV05BE
ALC3223 P/N is AL003223001
ALC3234 ALC3223
R396 0_4 *0_4_NC
R394 *20K/F_4_NC 20K/F_4
R170 200K_4 39.2K/F
R390 100K_4 *100K_4_NC
R384 *100K_4_NC 100K_4
Q17 *2N7002KDW_NC 2N7002KDW
ALC3234
MQFN48(6X6)
U9
ALC3234-CG
Universal Audio Jack
(ALC3223 supported iPhone/Nokia headset
, Headphone, Line-In and Microphone)
Close to codec
Trace width for SLEEVE, RING2: 40mil
R170@3223 use 39.2K (CS33922FB15)
0802 Chang R171,R225 P/N to CS24702JB38(4.7k)
2SJ3080-060111F
50281-00401-001
To solve the background noise while combojack
connecting to an active speaker and system entry
into S3/S4/S5 without analog power
Quanta Computer Inc.
PROJECT : AM6
Audio Codec ALC3234
Size
Document Number
Rev A
Date: Monday, May 05, 2014
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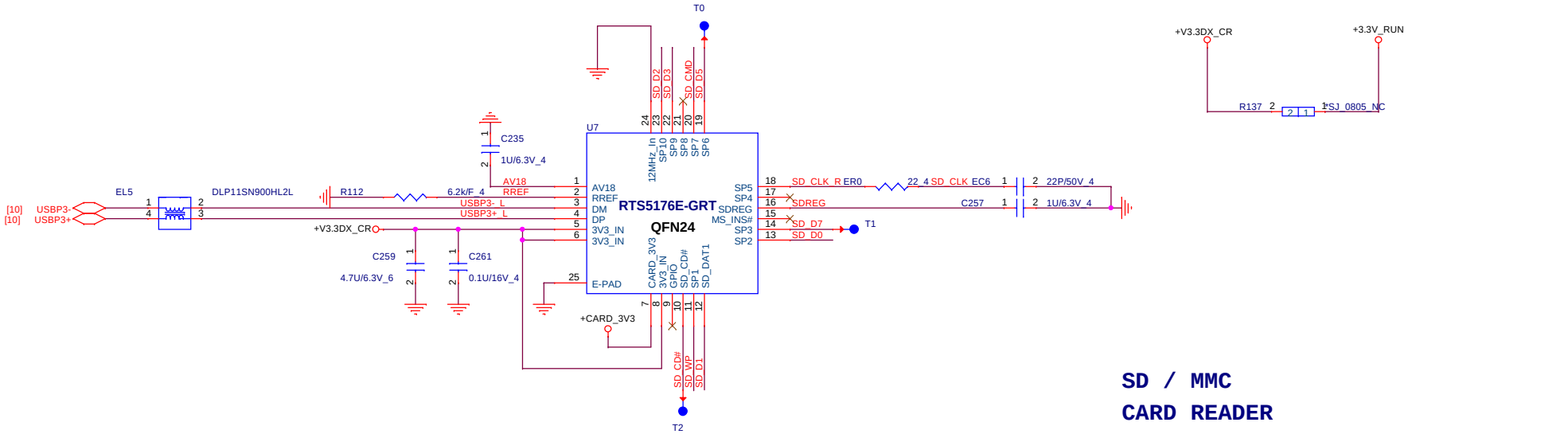
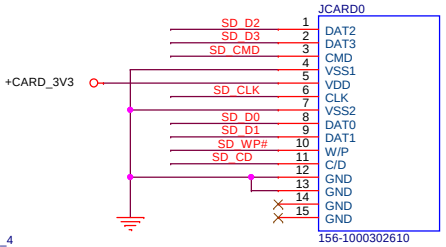


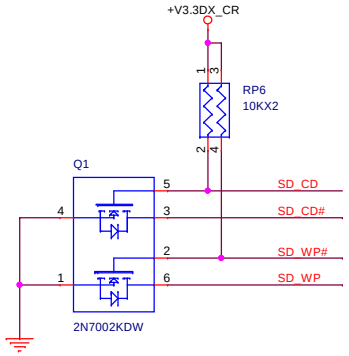
SD / MMC CARD READER



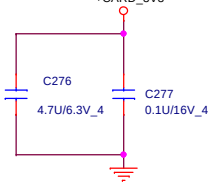
(6)PIN ASSIGNMENTS

PIN NO.	PIN DEFINE	PIN NO.	PIN DEFINE
#1	DAT2	8#	DAT0
2#	CD/DAT3	9#	DAT1
3#	CMD	10#	WP SW
4#	VSS	11#	CD SW
5#	VDD	12#	GND SW
6#	CLK	13#	GND SW
7#	VSS		

C/D and W/P are Normal Close



Place close to Connector



Quanta Computer Inc.		
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Size	Document Number: Card Reader RTS5176E	Rev A
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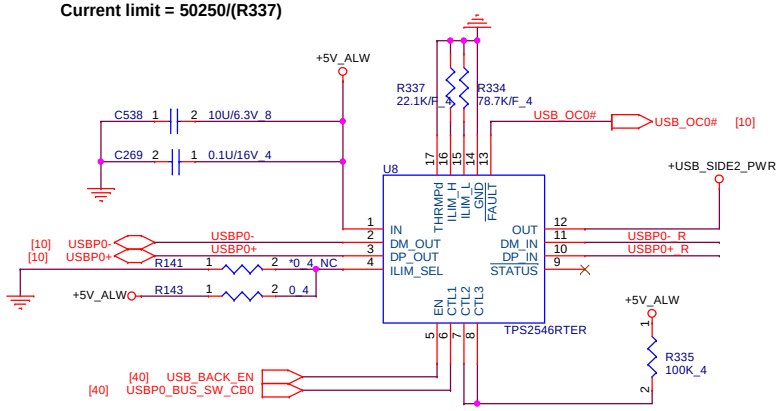
USB3.0 Power Share

USB Power share

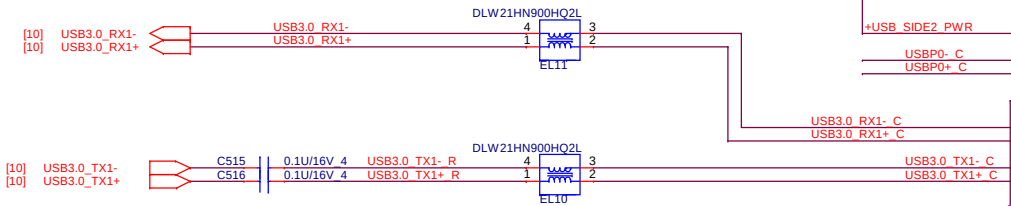
USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.2

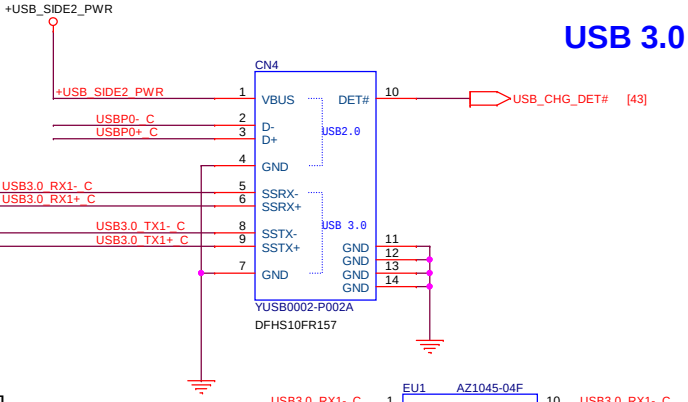
	R337	mA	
OC limitation	100k ohm	504	
	22.1k ohm	2274	Applied Now

Current limit = 50250/(R337)

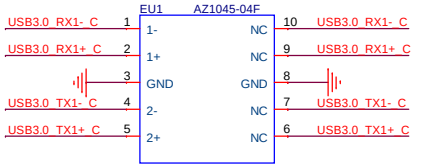


USB3.0/2.0 COMBO X 1

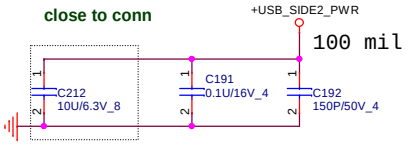


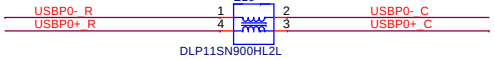


USB 3.0



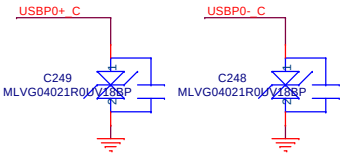
close to conn





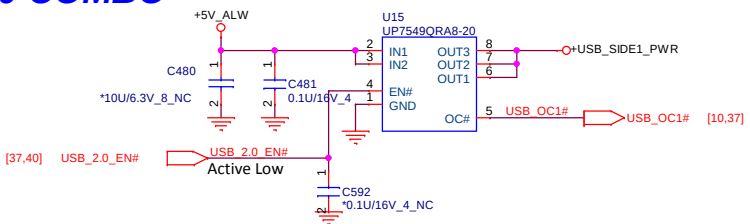
ESD Function

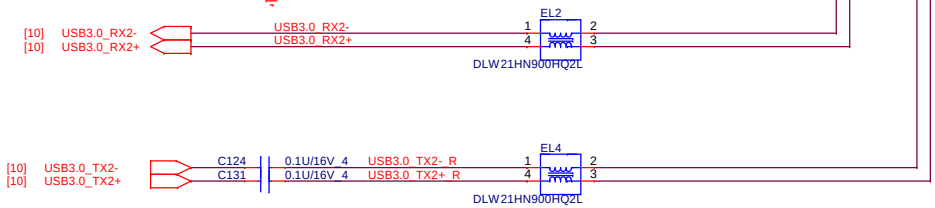
Place ESD diodes as close as USB connector.

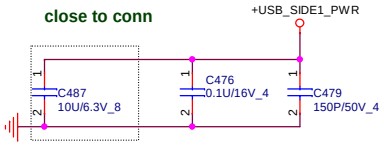


USB3.0/2.0 COMBO

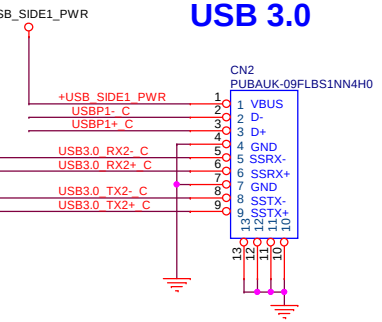
M15 Design Requirement:
I continuous 1.5A ; OC 2.0A

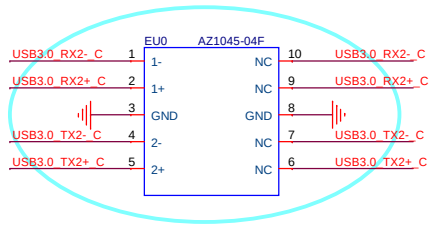






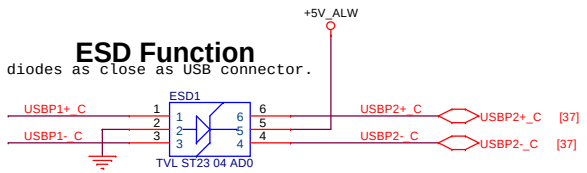
USB 3.0





ESD Function

Place ESD diodes as close as USB connector.



Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: USB3/USB Charger	Rev: A
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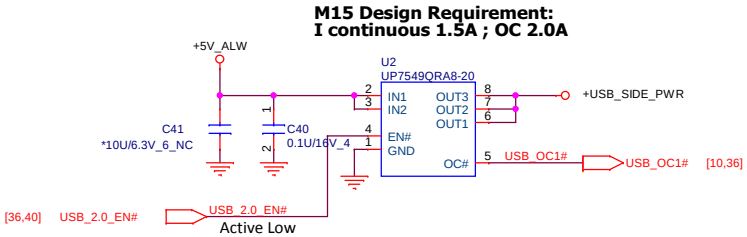
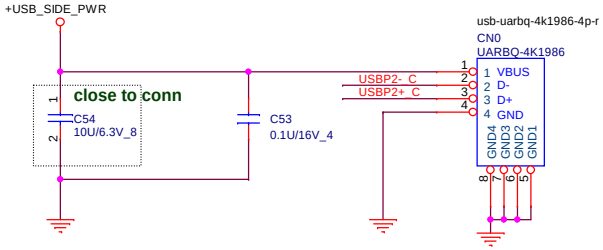
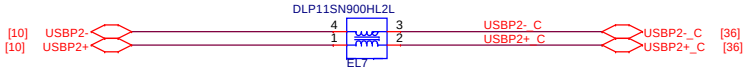
USB2.0 X1







Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: USB2*1	Rev: A
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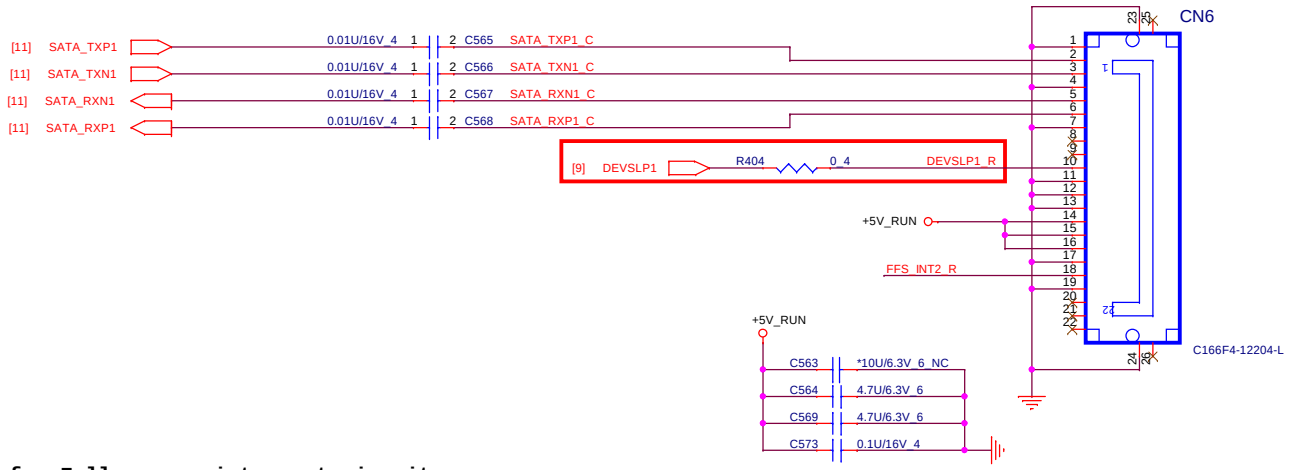
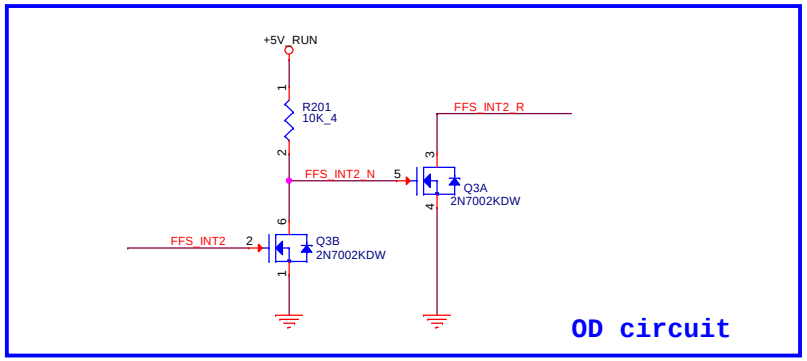
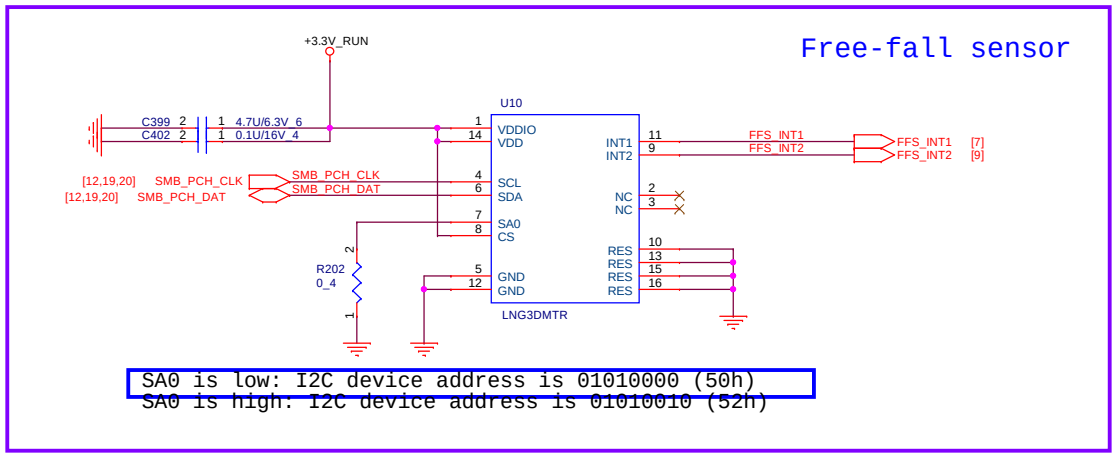
SATA HDD Connector



If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit





Quanta Computer Inc.

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Size	Document Number	Rev
	SATA HDD/Accelerometer	A

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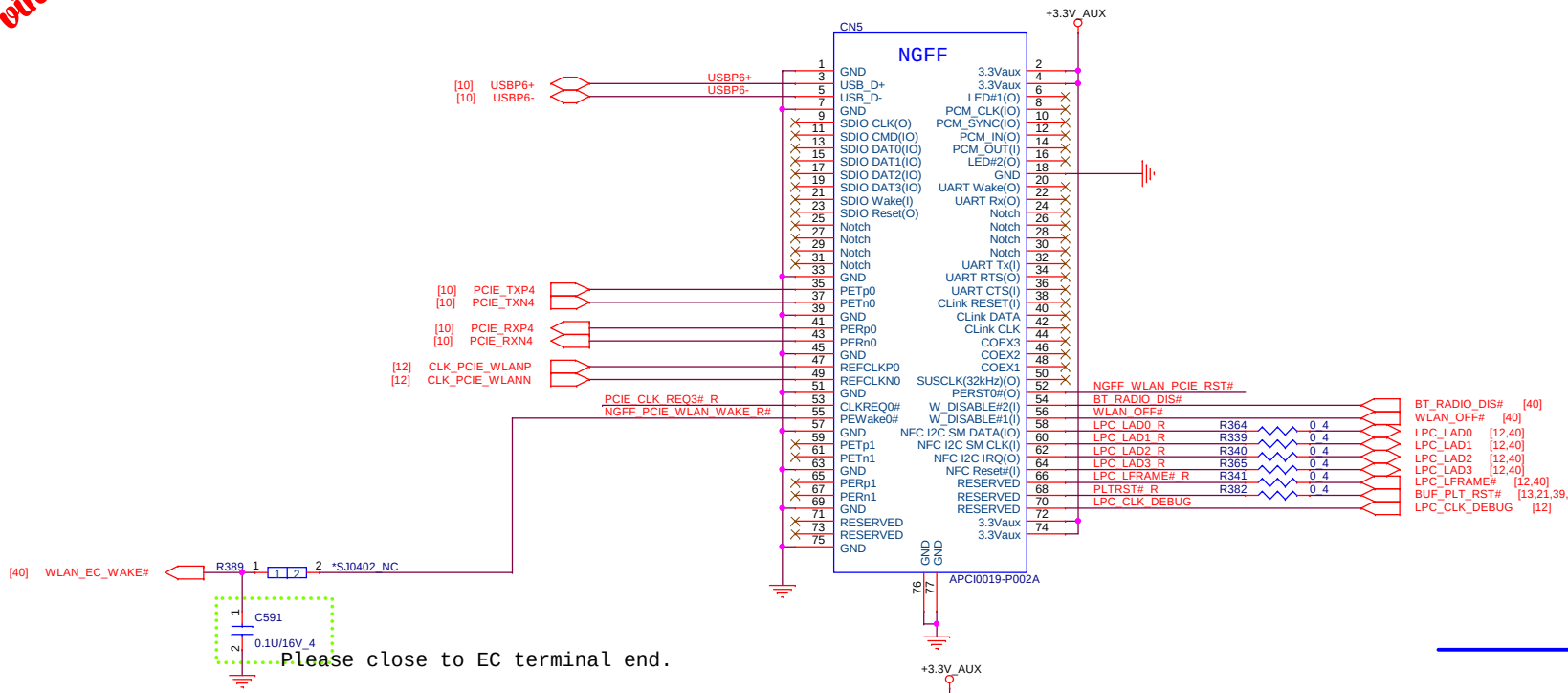
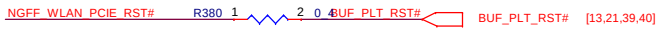
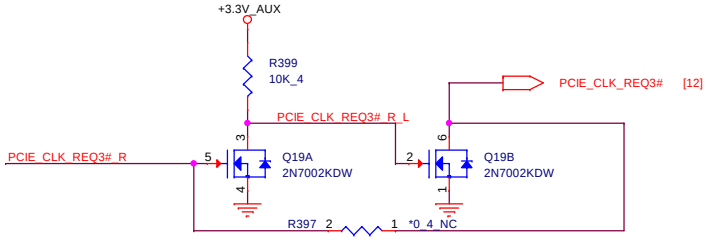
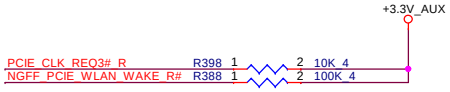
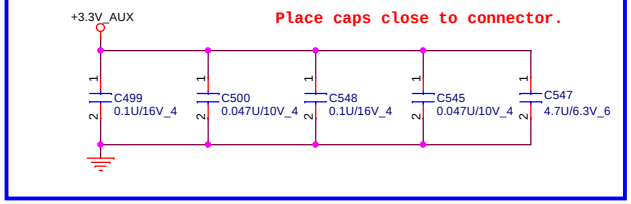
NGFF Wifi/BT connector

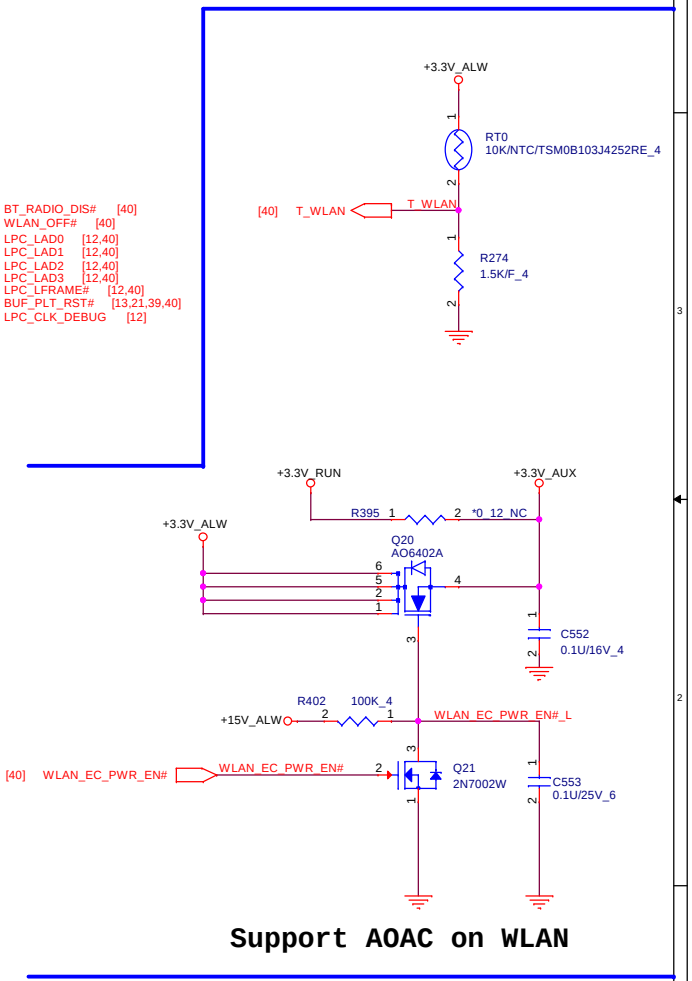












Support AOAC on WLAN

Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	Wifi/BT NGFF	A

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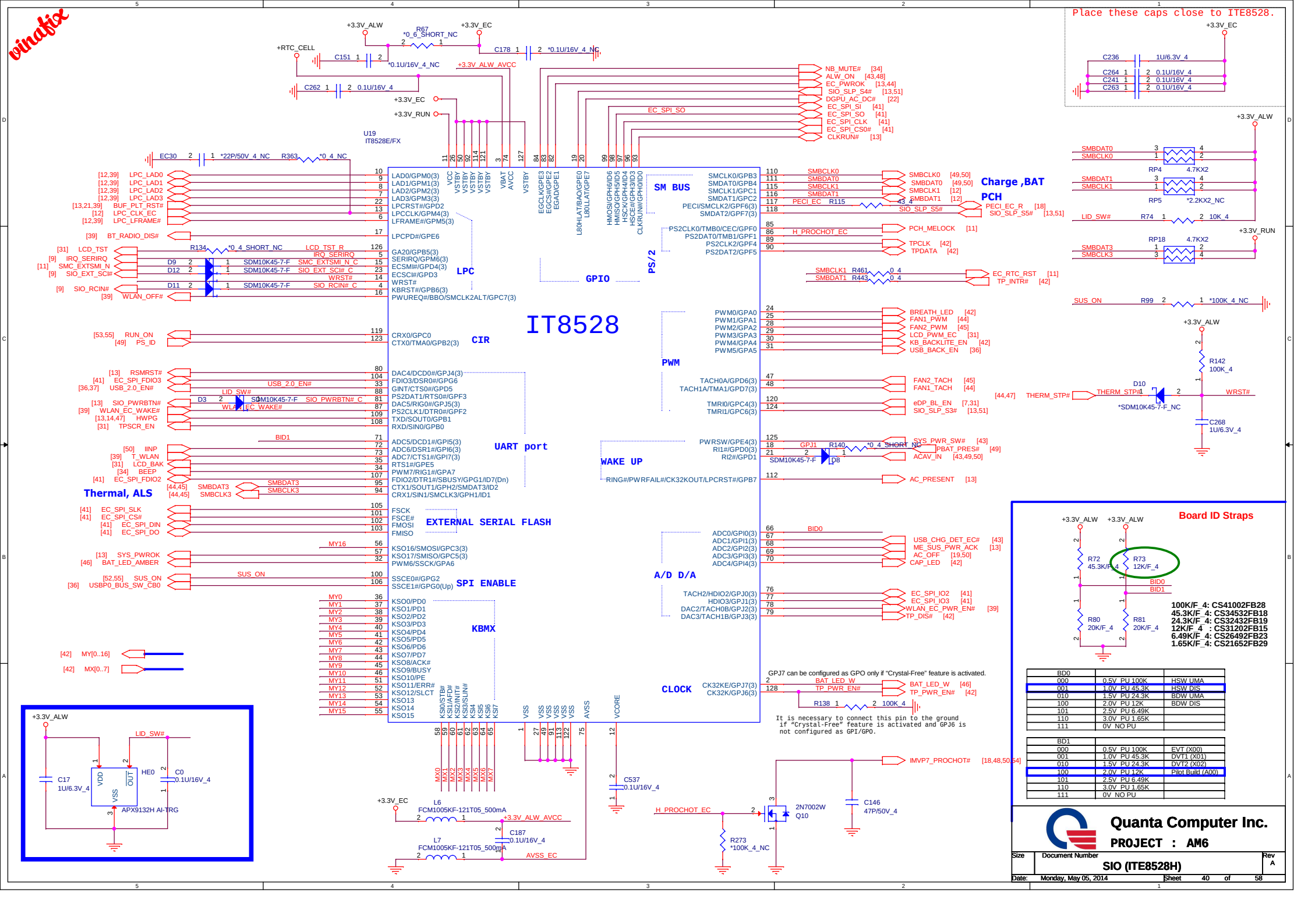
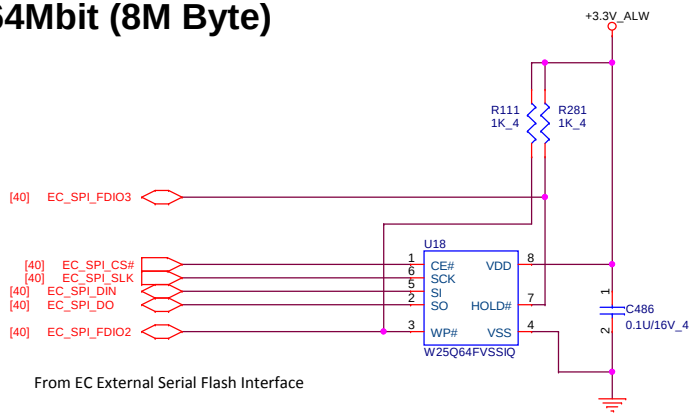


BD0		
000	0.5V PU 100K	HSW UMA
001	1.0V PU 45.3K	HSW DIS
010	1.5V PU 24.3K	BDW UMA
100	2.0V PU 12K	BDW DIS
101	2.5V PU 6.49K	
110	3.0V PU 1.65K	
111	0V NO PU	

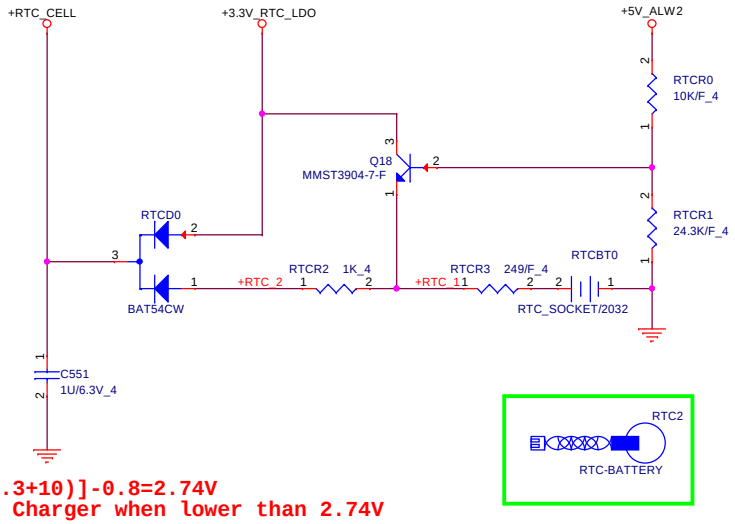
BD1		
000	0.5V PU 100K	EVT (X00)
001	1.0V PU 45.3K	DVT1 (X01)
010	1.5V PU 24.3K	DVT2 (X02)
100	2.0V PU 12K	Pilot Build (A00)
101	2.5V PU 6.49K	
110	3.0V PU 1.65K	
111	0V NO PU	

For EC 64Mbit (8M Byte)



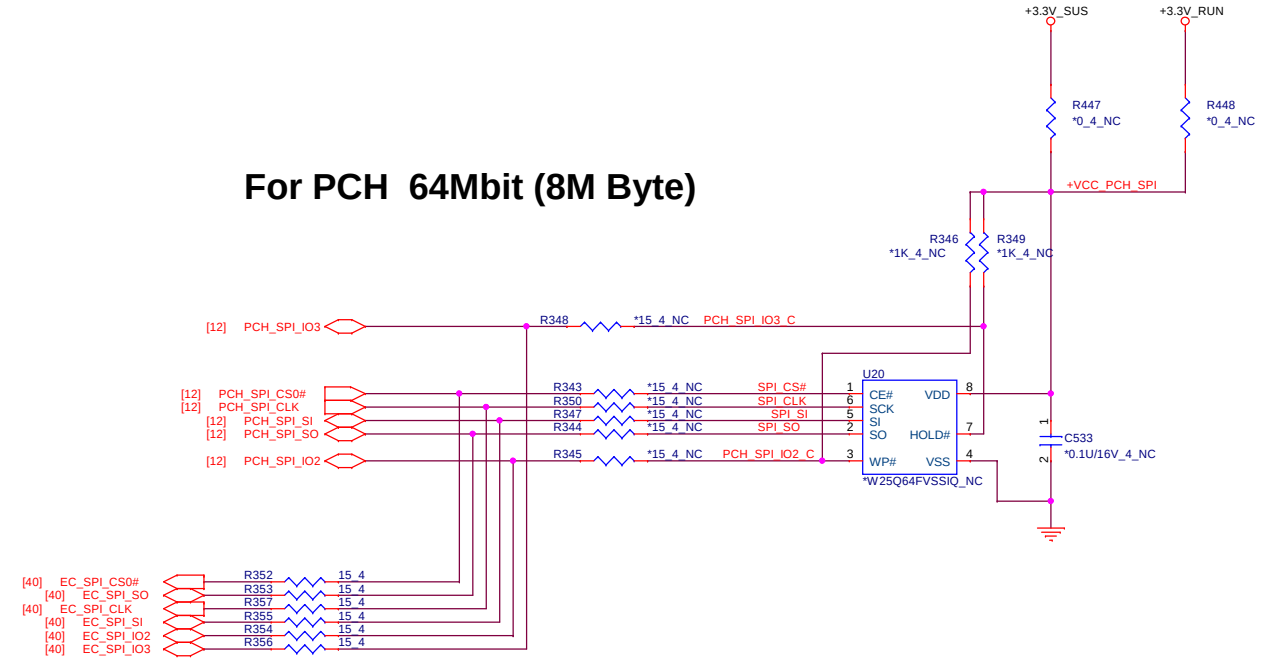
From EC External Serial Flash Interface

RTC BATTERY



5*[24.3/(24.3+10)]-0.8=2.74V
RTC Battery Charger when lower than 2.74V

For PCH 64Mbit (8M Byte)



To EC Slave Interface

Quanta Computer Inc.
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	FLASH / RTC	A
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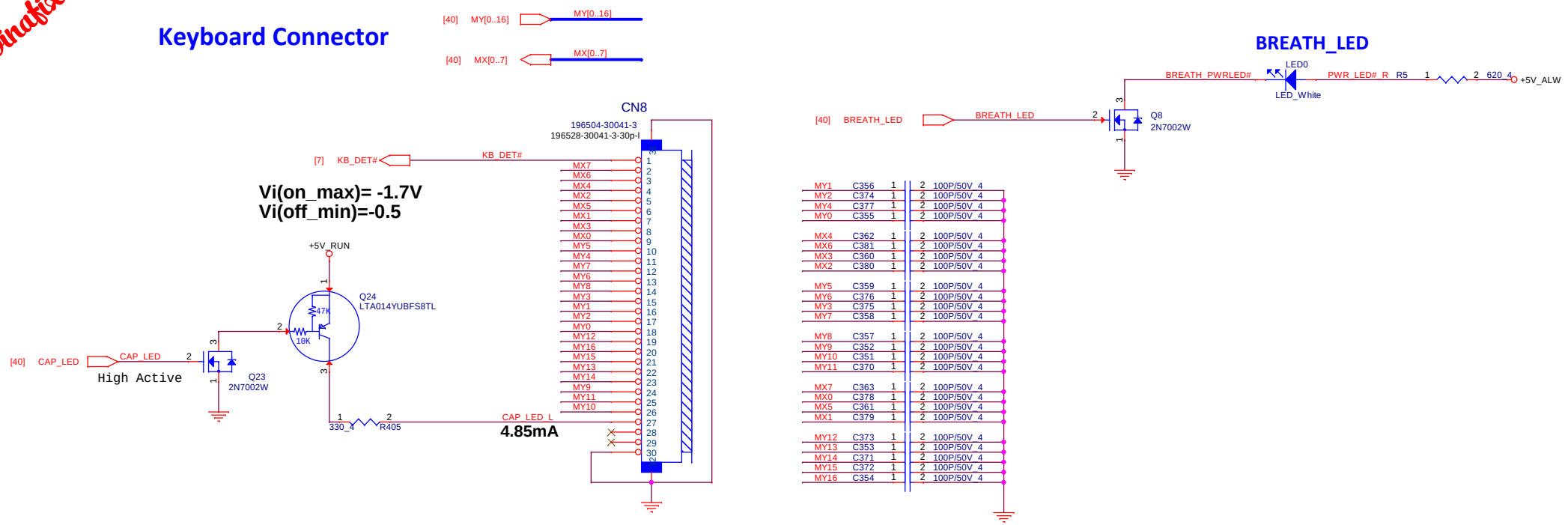
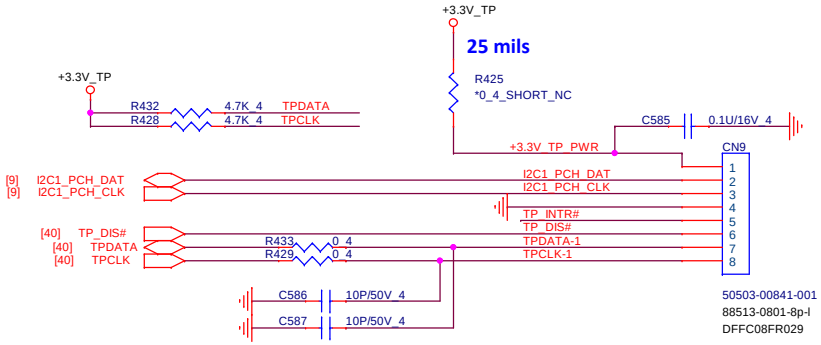
Keyboard Connector

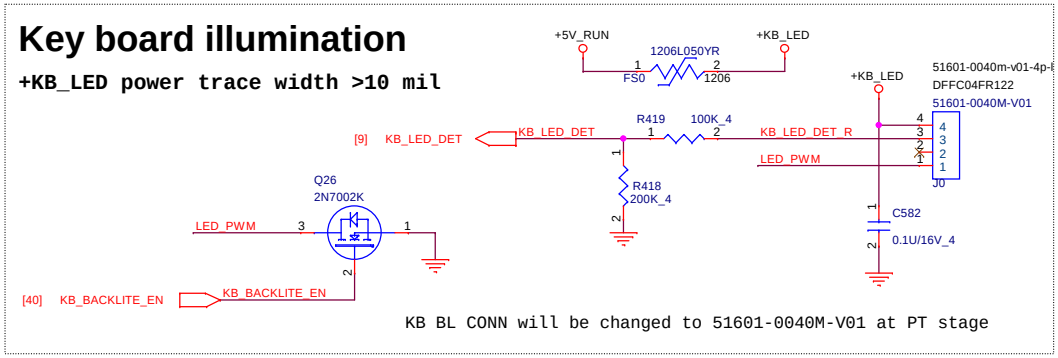


BREATH_LED

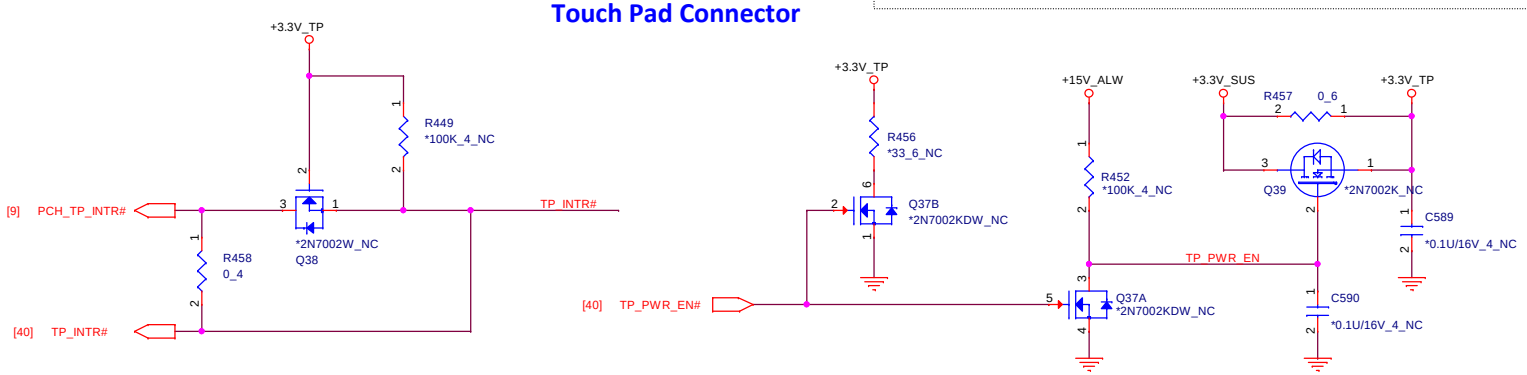


Key board illumination

+KB_LED power trace width >10 mil



Touch Pad Connector



Quanta Computer Inc.

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Size	Document Number	Rev
	KB/CLK Gen/FAN/TP	A

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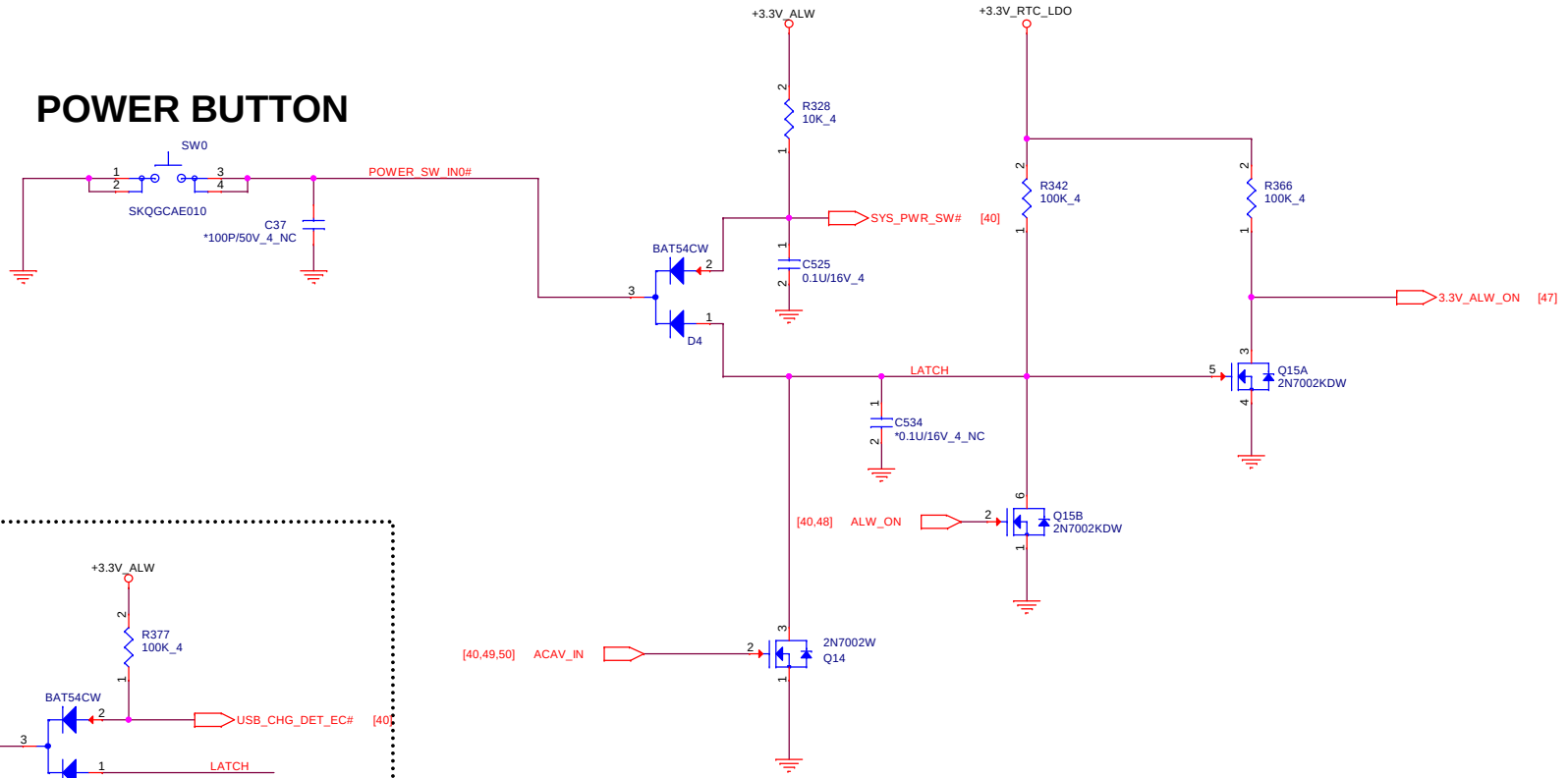
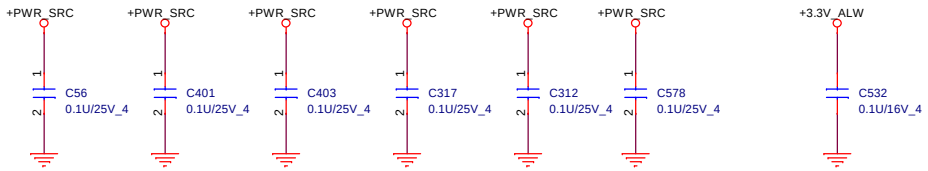
3VALW ON POWER LOGIC

POWER BUTTON



Stitching Capacitors



Quanta Computer Inc.

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Size	Document Number	Rev
	3VALW ON POWER LOGIC	A

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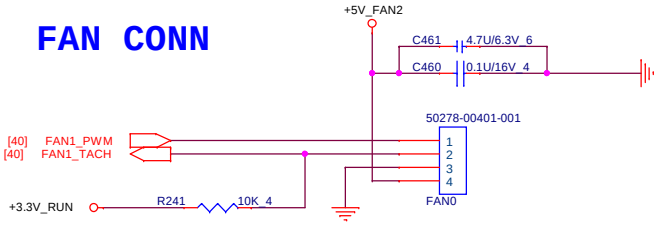
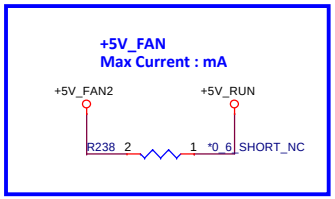
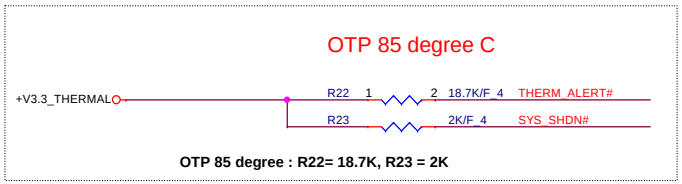
FAN CONN



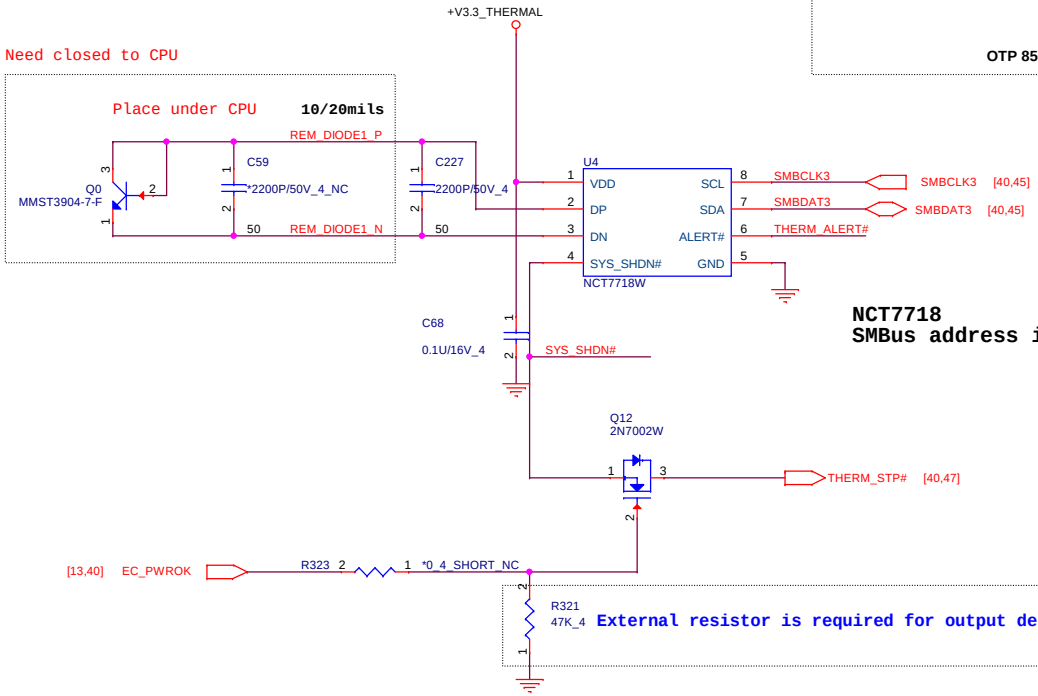


THERMAL IC

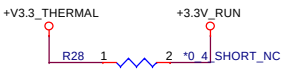


OTP 85 degree : R22= 18.7K, R23 = 2K

SYS_SHD# / ALERT#	2K	7.5K	10.5K	14K	18.7K
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C



NCT7718
SMBus address is 1001100xb (98h) (x is R/W bit).



+V3.3_THERMAL
Max Current :mA

Quanta Computer Inc.
PROJECT : AM6

Size	Document Number	Rev
	FAN & THERMAL	A

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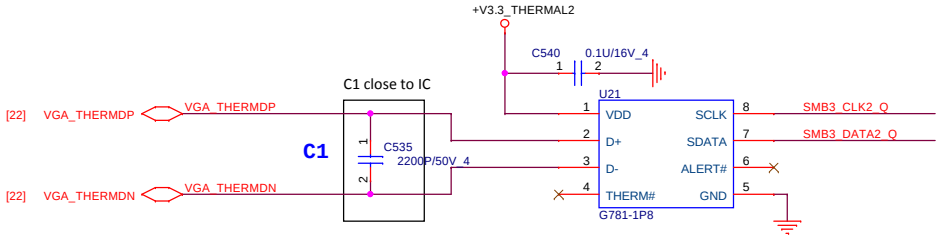
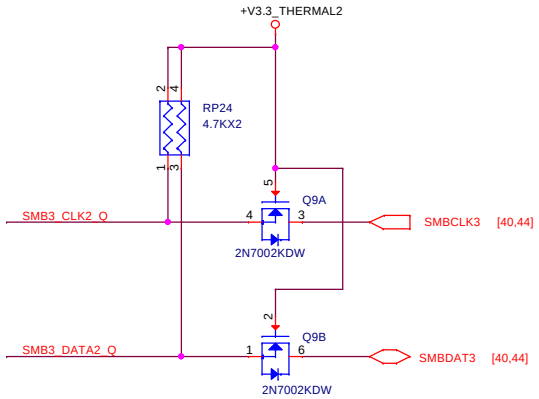
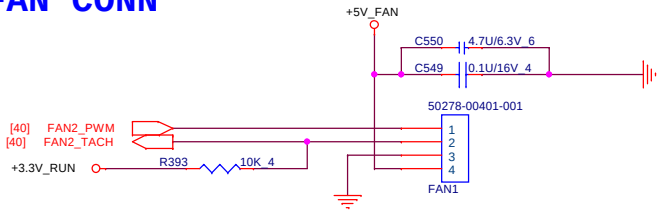
For GPU use

G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).

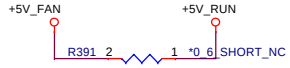


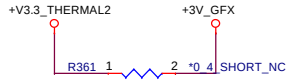


FAN CONN



+5V_FAN
Max Current : mA





+V3.3_THERMAL
Max Current :mA

Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: Thermal GPU	Rev: A
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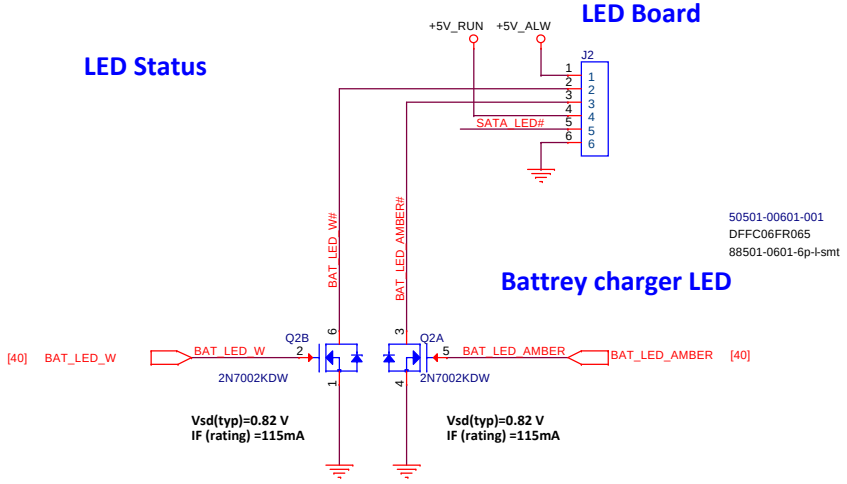
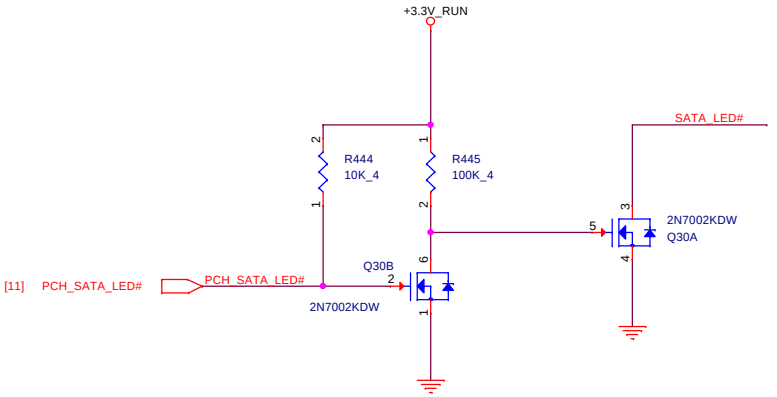
LED Board

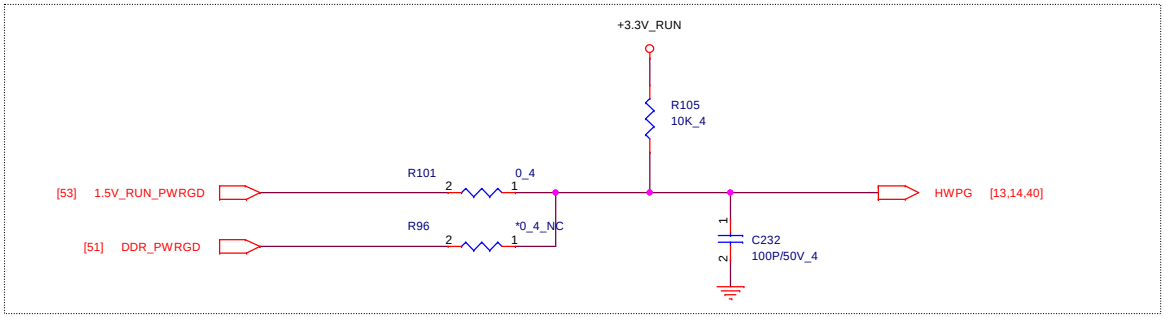
LED Status

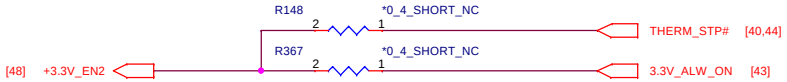


HDD activity LED.



Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: LED	Rev: A
Date: Monday, May 05, 2014	Sheet 46 of 58	





Quanta Computer Inc.

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Size	Document Number	Rev
	System Reset Circuit	A

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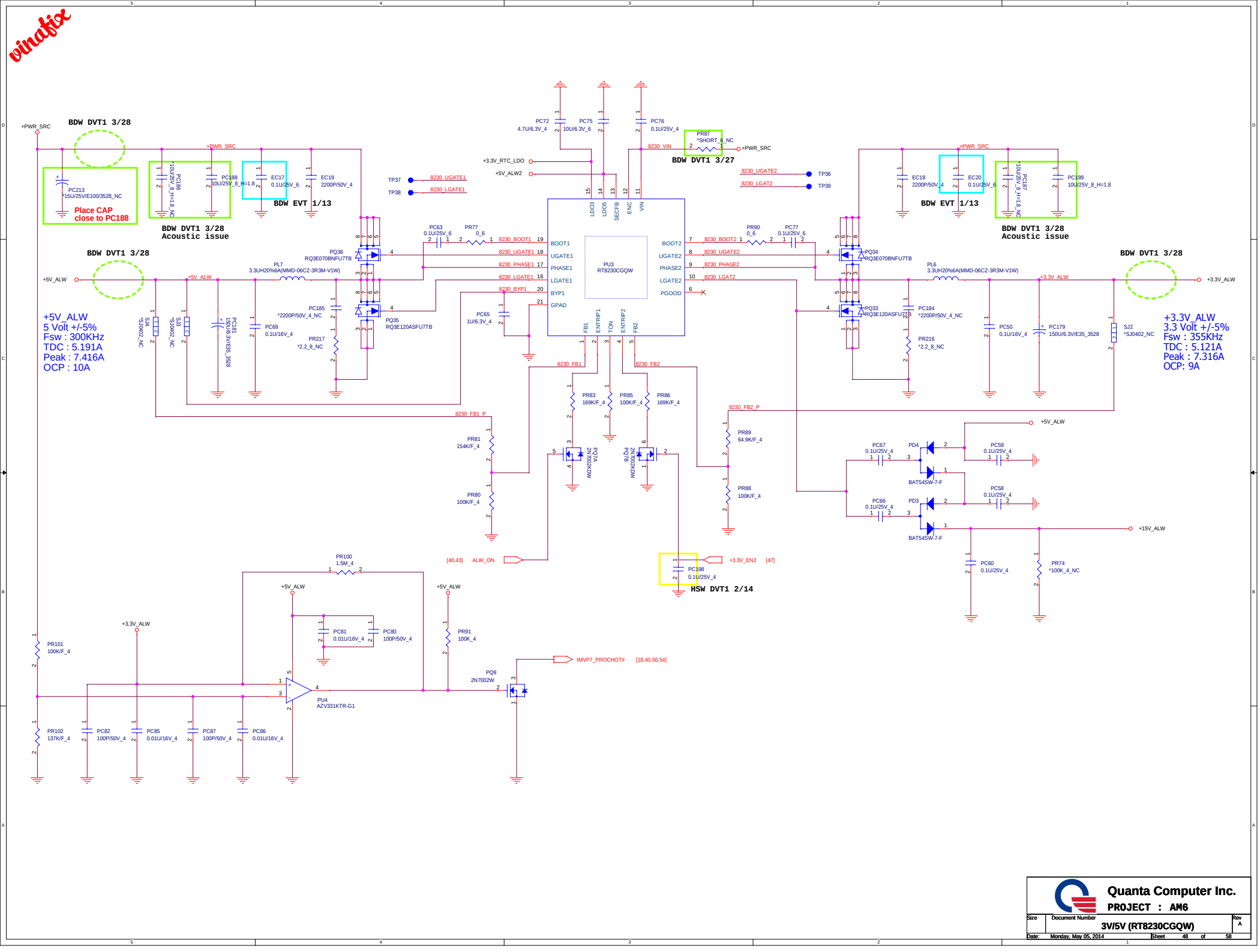

Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	3V/5V (RT8230CGQW)	A

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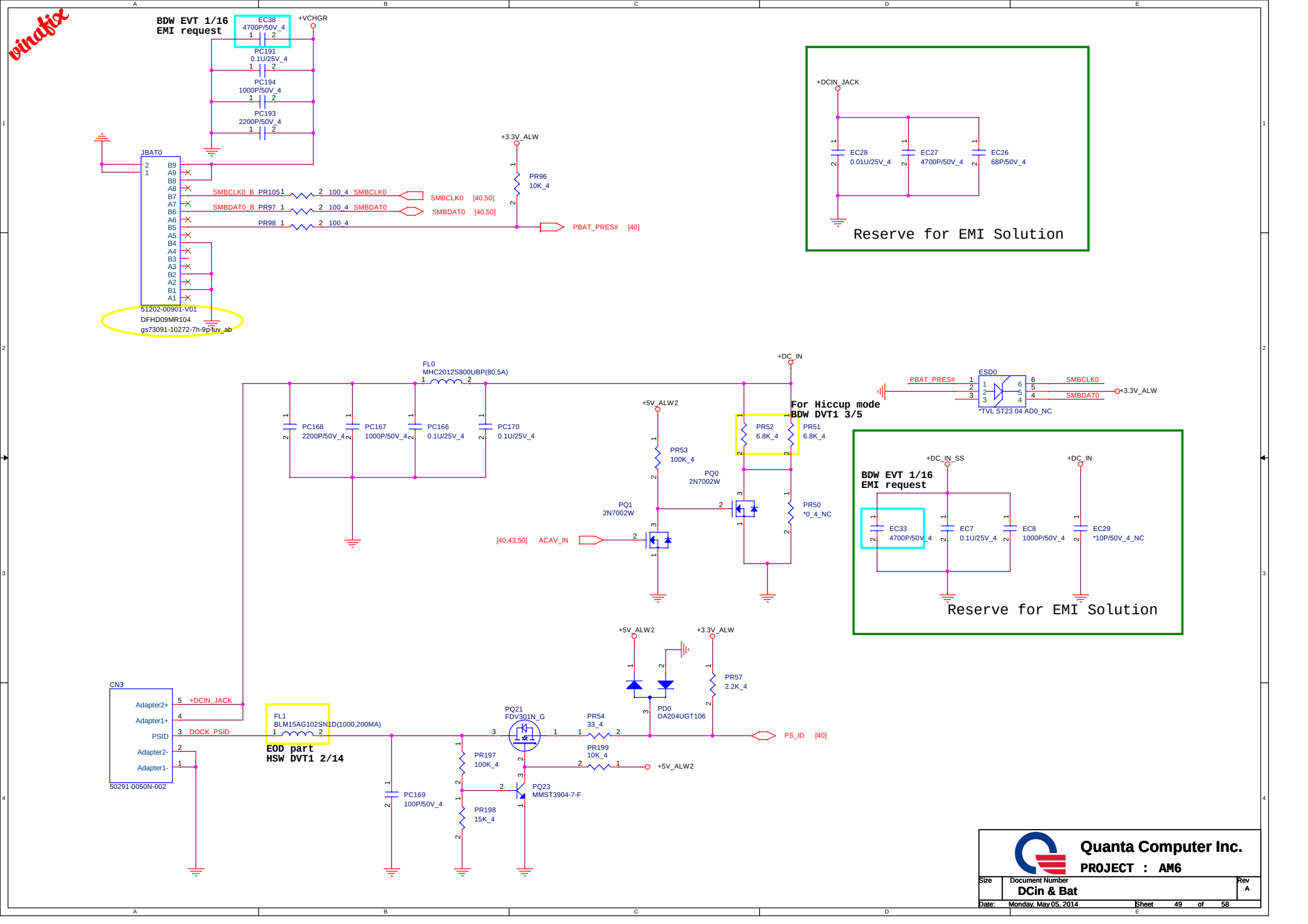

Quanta Computer Inc.

PROJECT : AM6

Size	Document Number	Rev
	DCin & Bat	A

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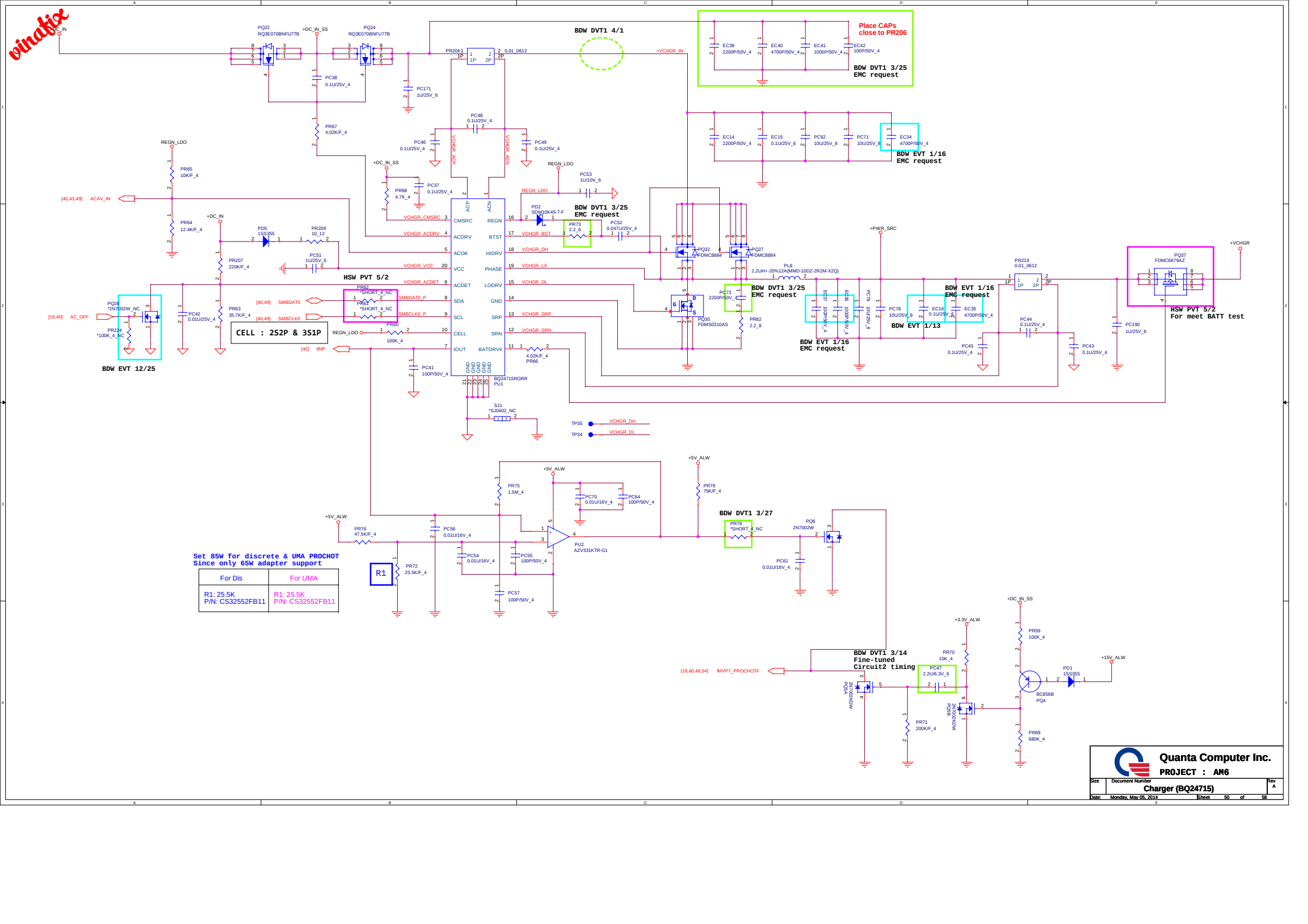
DC_IN
PQ22 RQ3E070BNFU7TB
PQ24 RQ3E070BNFU7TB
+DC_IN_SS
PC38 0.1U/25V_4
PC171 1U/25V_6
PR67 4.02K/F_4
PR2061 0.01_0612
+VCHGR_IN
BDW DVT1 4/1
Place CAPs close to PR206
EC39 2200P/50V_4
EC40 4700P/50V_4
EC41 1000P/50V_4
EC42 100P/50V_4
BDW DVT1 3/25 EMC request
EC14 2200P/50V_4
EC15 0.1U/25V_6
PC62 10U/25V_8
PC71 10U/25V_8
EC34 4700P/50V_4
BDW EVT 1/16 EMC request
PC48 0.1U/25V_4
PC46 0.1U/25V_4
PC49 0.1U/25V_4
VCHGR_ACP
VCHGR_ACN
REGN_LDO
PR65 10K/F_4
PR64 12.4K/F_4
[40,43,49] ACAV_IN
+DC_IN
PR68 4.7K_4
PC37 0.1U/25V_4
PC53 1U/10V_6
PD2 SDM10K45-7-F
BDW DVT1 3/25 EMC request
PR73 2.2_6
PC52 0.047U/25V_4
PD5 1SS355
PR209 10_12
PC51 1U/25V_6
PR207 220K/F_4
HSW PVT 5/2
PR62 *SHORT_4_NC
PR61 *SHORT_4_NC
PR60 100K_4
PR63 35.7K/F_4
PC42 0.01U/25V_4
PQ26 *2N7002W_NC
PR224 *100K_4_NC
[19,40] AC_OFF
BDW EVT 12/25
CELL : 2S2P & 3S1P
[40,49] SMBDAT0
[40,49] SMBCLK0
[40] IINP
VCHGR_CMSRC
VCHGR_ACDRV
VCHGR_ACOK
VCHGR_VCC
VCHGR_ACDET
VCHGR_BST
VCHGR_DH
VCHGR_LX
VCHGR_DL
VCHGR_SRP
VCHGR_SRN
SMBDAT0_P
SMBCLK0_P
CMSRC ACDRV ACOK VCC ACDET SDA SCL CELL IOUT ACP ACN REGN BTST HIDRV PHASE LODRV GND SRP SRN BATDRV#
BQ24715RGRR PU1
PC41 100P/50V_4
4.02K/F_4 PR66
SJ1 *SJ0402_NC
TP35 VCHGR_DH
TP34 VCHGR_DL
PQ32 FDMC8884
PQ27 FDMC8884
PL8 2.2UH+-20%12A(MMD-10DZ-2R2M-X2Q)
PQ30 FDMS0310AS
PR82 2.2_8
PC73 2200P/50V_4
BDW DVT1 3/25 EMC request
+PWR_SRC
PC37 100P/50V_4
PC36 100P/50V_4
PC38 10U/50V_8
PC78 10U/25V_8
EC16 0.1U/25V_4
EC35 4700P/50V_4
BDW EVT 1/16 EMC request
BDW EVT 1/13
BDW EVT 1/16 EMC request
PR219 0.01_0612
PC45 0.1U/25V_4
PC44 0.1U/25V_4
PC43 0.1U/25V_4
PC190 1U/25V_6
PQ37 FDMC6679AZ
+VCHGR
HSW PVT 5/2 For meet BATT test
+5V_ALW
PR75 1.5M_4
PC70 0.01U/16V_4
PC64 100P/50V_4
PR79 75K/F_4
BDW DVT1 3/27
PR78 *SHORT_4_NC
PQ6 2N7002W
PC61 0.01U/16V_4
PR76 47.5K/F_4
PC56 0.01U/16V_4
PC54 0.01U/16V_4
PC55 100P/50V_4
PC57 100P/50V_4
PR72 25.5K/F_4
R1
PU2 AZV331KTR-G1
Set 85W for discrete & UMA PROCHOT
Since only 65W adapter support
For Dis
For UMA
R1: 25.5K
P/N: CS32552FB11
R1: 25.5K
P/N: CS32552FB11
BDW DVT1 3/14 Fine-tuned Circuit2 timing
[18,40,48,54] IMVP7_PROCHOT#
PQ7A 2N7002KW
PQ7B 2N7002KW
PC47 2.2U/6.3V_6
PR70 10K_4
PR71 200K/F_4
+3.3V_ALW
+DC_IN_SS
PR59 100K_4
PR69 680K_4
PD1 1SS355
BC856B PQ4
+15V_ALW
Quanta Computer Inc.
PROJECT : AM6
Size
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Charger (BQ24715)
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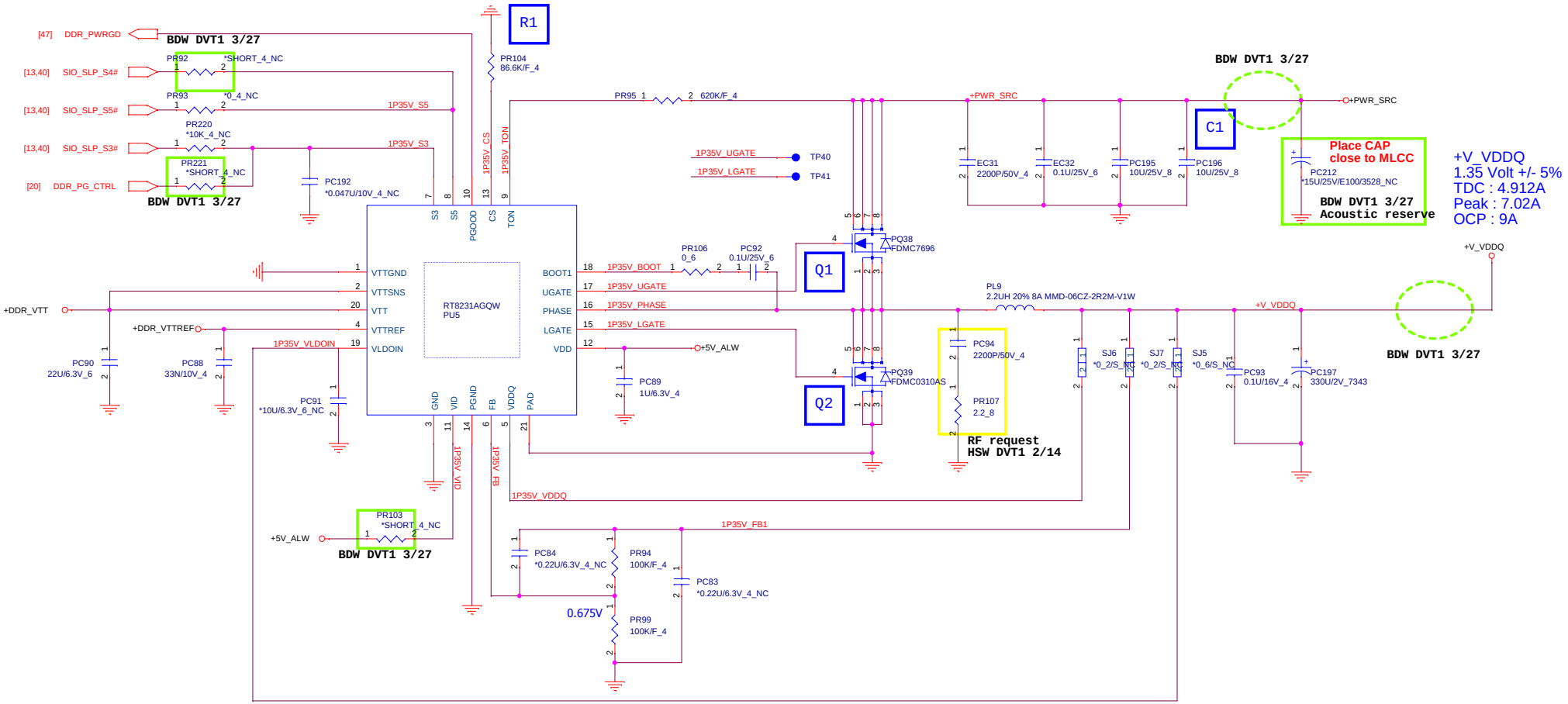
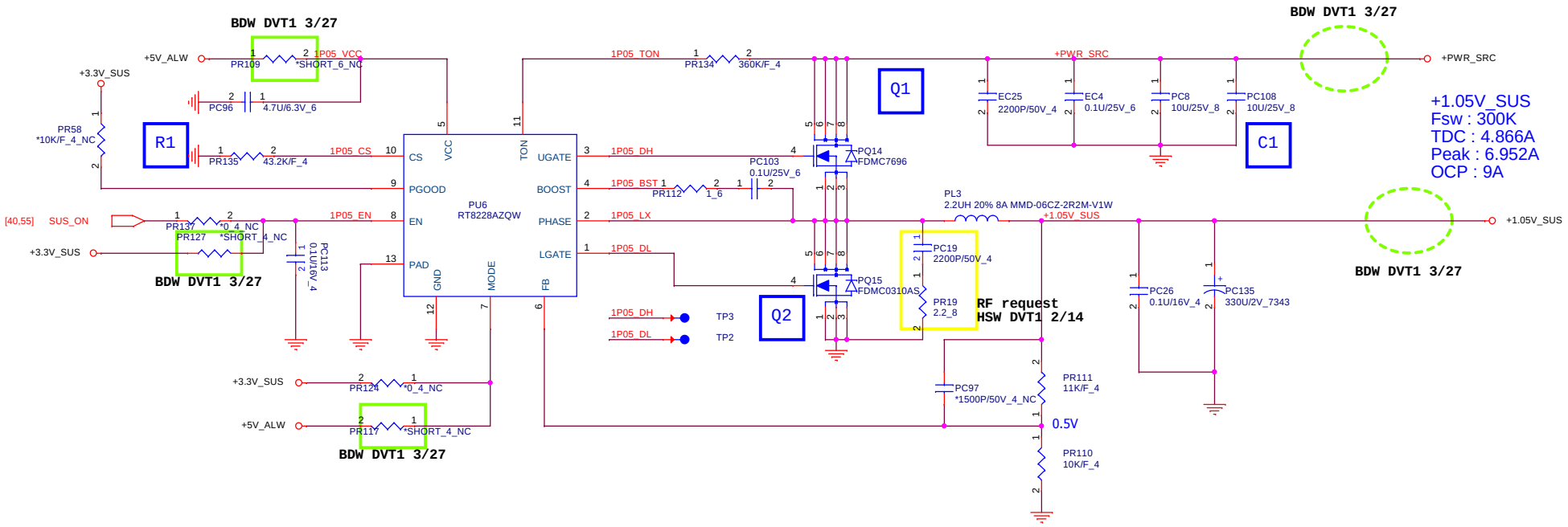
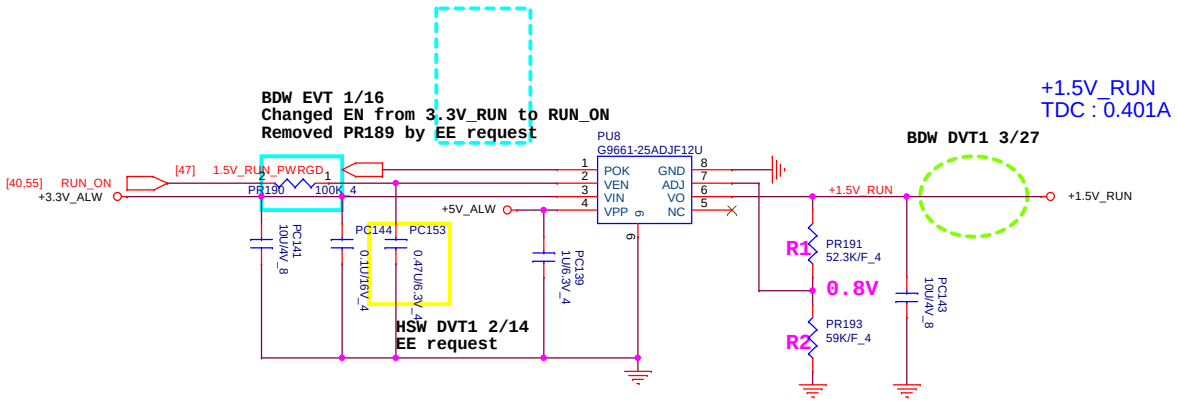


Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: 1.35_DDR/0.675(RT8231)	Rev: A
Date: Monday, May 05, 2014	Sheet 51 of 58	



Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: 1.05V_SUS (RT8228AZ)	Rev: A
Date: Monday, May 05, 2014	Sheet 52 of 58	



Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: +1.5V_RUN (G9661-25ADJF12U)	Rev A
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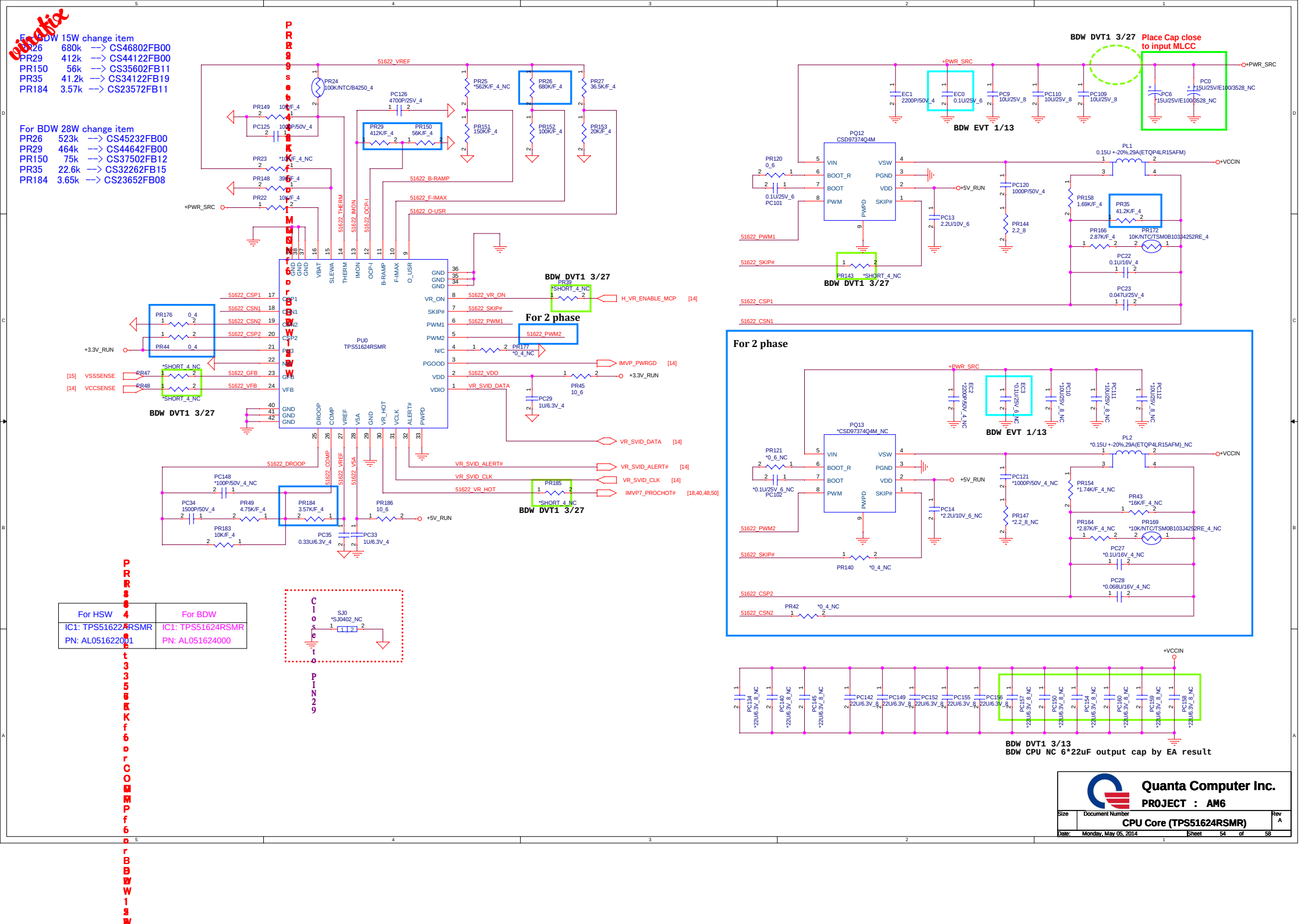
For BDW 15W change item
PR26 680k --> CS46802FB00
PR29 412k --> CS44122FB00
PR150 56k --> CS35602FB11
PR35 41.2k --> CS34122FB19
PR184 3.57k --> CS23572FB11
For BDW 28W change item
PR26 523k --> CS45232FB00
PR29 464k --> CS44642FB00
PR150 75k --> CS37502FB12
PR35 22.6k --> CS32262FB15
PR184 3.65k --> CS23652FB08
PU0 TPS51624RSMR
BDW DVT1 3/27
For 2 phase
BDW EVT 1/13
Place Cap close to input MLCC
PQ12 CSD97374Q4M
PQ13 *CSD97374Q4M_NC
PL1 0.15U +-20%,29A(ETQP4LR15AFM)
PL2 *0.15U +-20%,29A(ETQP4LR15AFM)_NC
For HSW
IC1: TPS51622RSMR
PN: AL051622001
For BDW
IC1: TPS51624RSMR
PN: AL051624000
Close to PIN29
BDW DVT1 3/13
BDW CPU NC 6*22uF output cap by EA result
Quanta Computer Inc.
PROJECT : AM6
CPU Core (TPS51624RSMR)
Size
Document Number
Rev A
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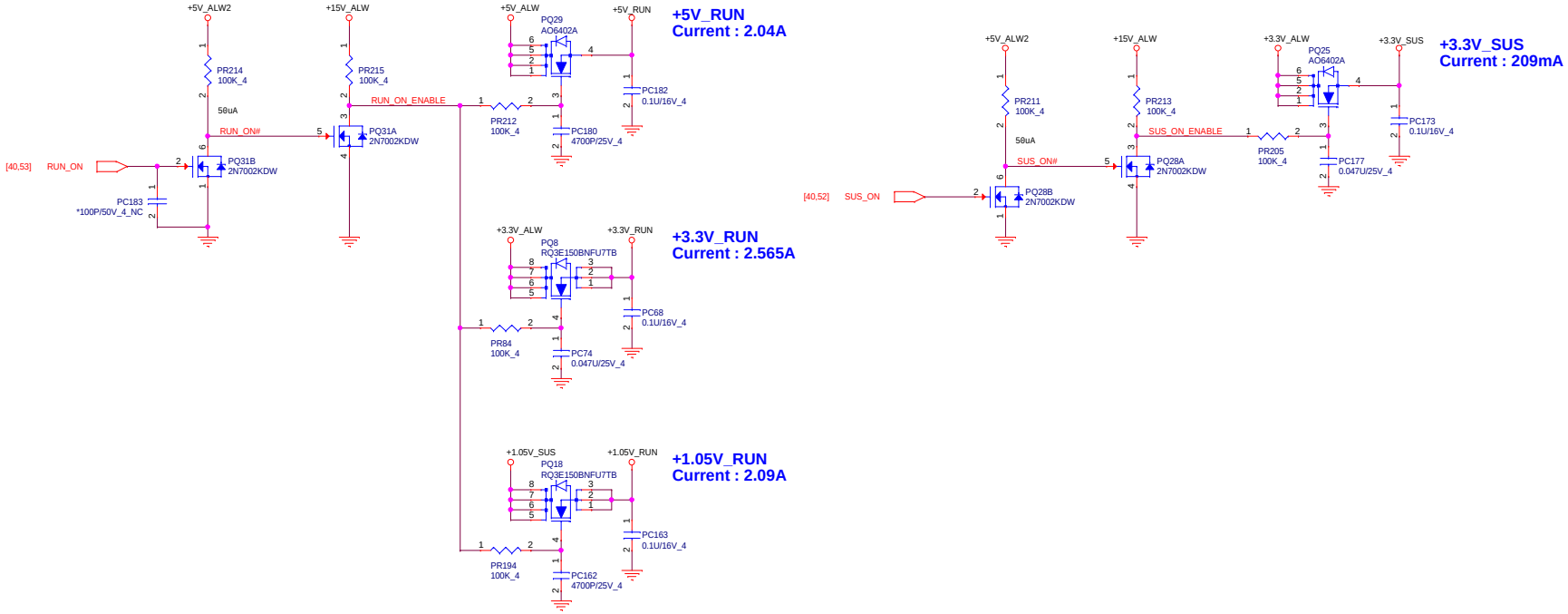

Quanta Computer Inc.		
PROJECT : AM6		
Size	Document Number: SUS_RUN Power Switch	Rev: A
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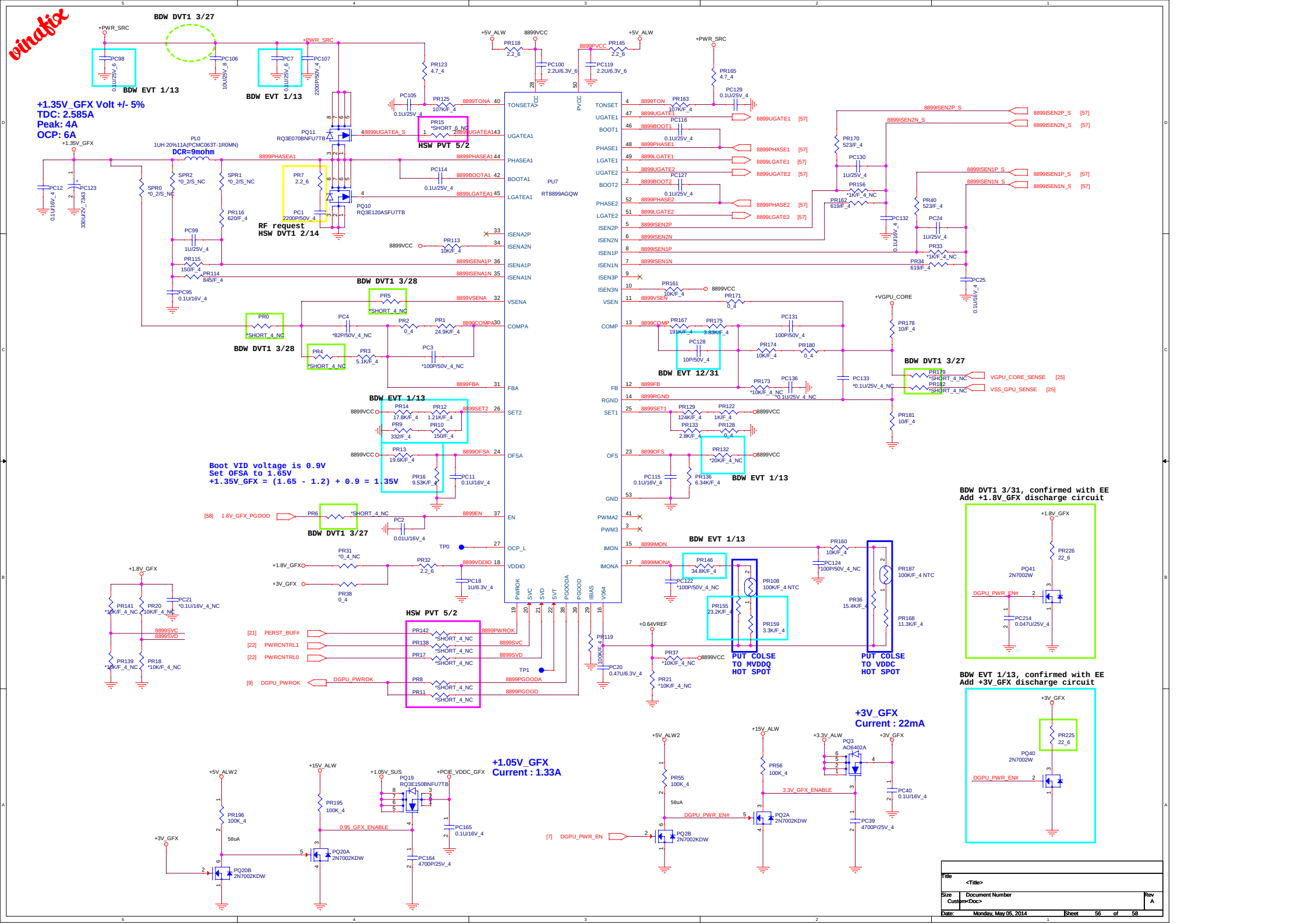
BDW DVT1 3/27
BDW EVT 1/13
+1.35V_GFX Volt +/- 5%
TDC: 2.585A
Peak: 4A
OCP: 6A
DCR=9mohm
RF request
HSW DVT1 2/14
HSW PVT 5/2
BDW DVT1 3/28
BDW EVT 12/31
Boot VID voltage is 0.9V
Set OFSA to 1.65V
+1.35V_GFX = (1.65 - 1.2) + 0.9 = 1.35V
PUT COLSE TO MVDDQ HOT SPOT
PUT COLSE TO VDDC HOT SPOT
BDW DVT1 3/31, confirmed with EE
Add +1.8V_GFX discharge circuit
BDW EVT 1/13, confirmed with EE
Add +3V_GFX discharge circuit
+3V_GFX Current : 22mA
+1.05V_GFX Current : 1.33A
Title
<Title>
Size
Document Number
<Doc>
Rev
A
Date:
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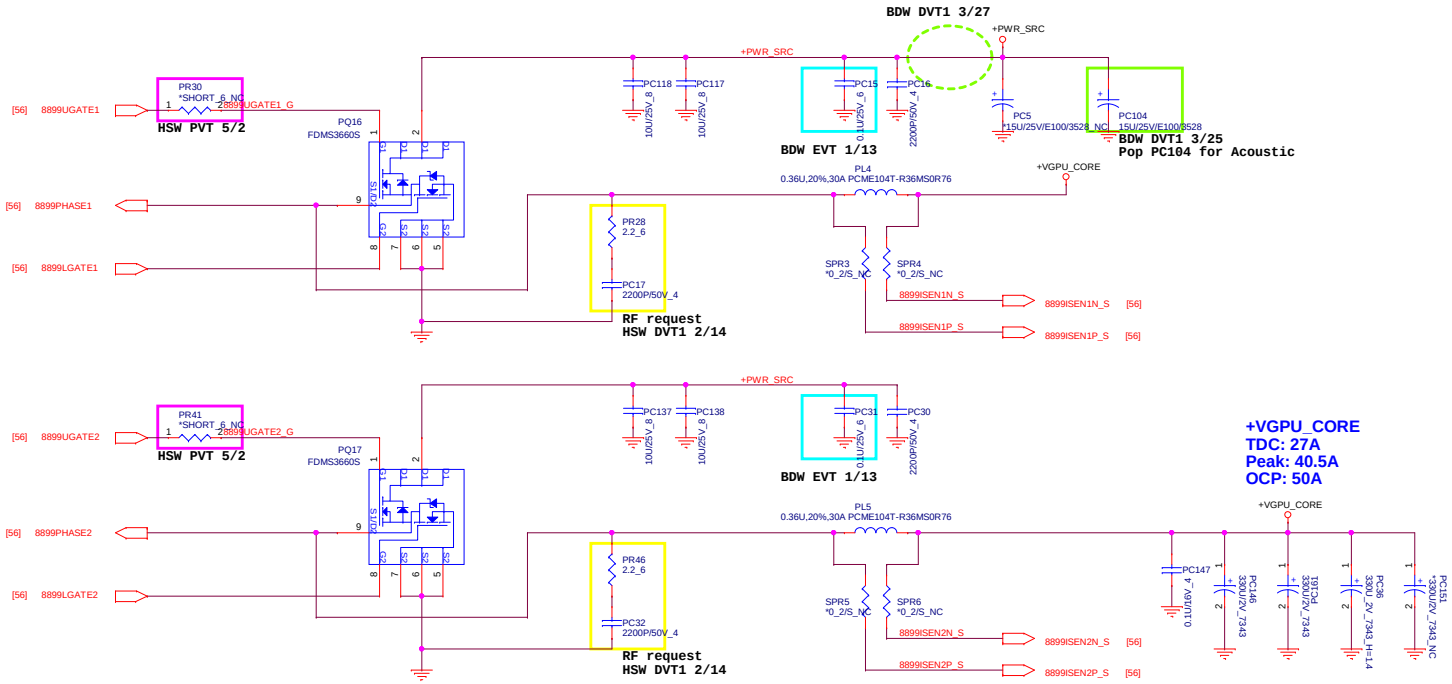

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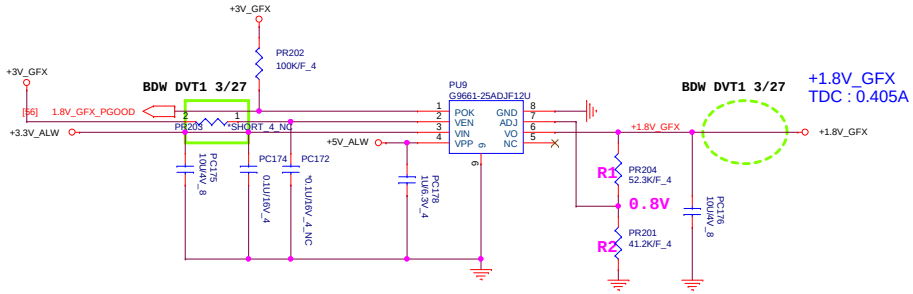
Size	Document Number	Rev
Custom	<Doc>	A
Date: Monday, May 05, 2014	Sheet 57 of 58	



Title	<Title>	
Size: Custom	Document Number: <Doc>	Rev: A
Date: Monday, May 05, 2014	Sheet 58 of 58	