MS-AC751 Ver: 2.1

Intel -SugarBay plamform

CPU:

INTEL-Sandy bridge LGA1155

System Chipset:

INTEL-Cougar Point

OnBoard Chipset:

HD Audio Codec:ALC887

LAN-RTL8111E

SIO: NCT6681D

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

MINIPCI Express (X1) Slot * 2

PWM:

Controller:NCP6131 3+1Phase

Other:

SATA(SATA2-300MB/s) *2

USB2.0 *4

USB3.0 *2

HDMI OUT*1

MICRO-STAR INT'L CO.,LTD

MS-AC75

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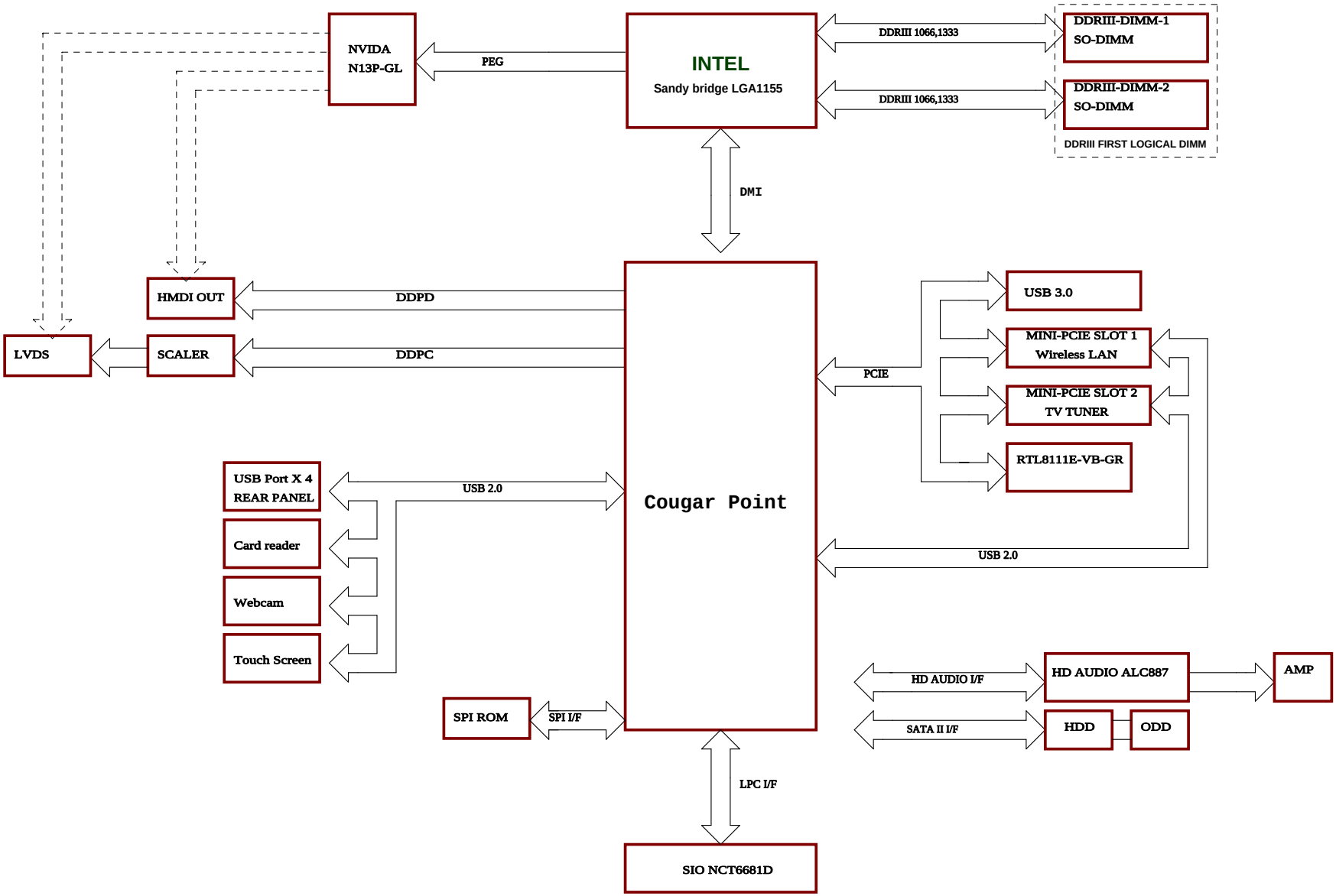
MS-AC77 / AA59 (MS-AC751)



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Size: Custom	Document Description: Block Diagram	Rev: 2.1
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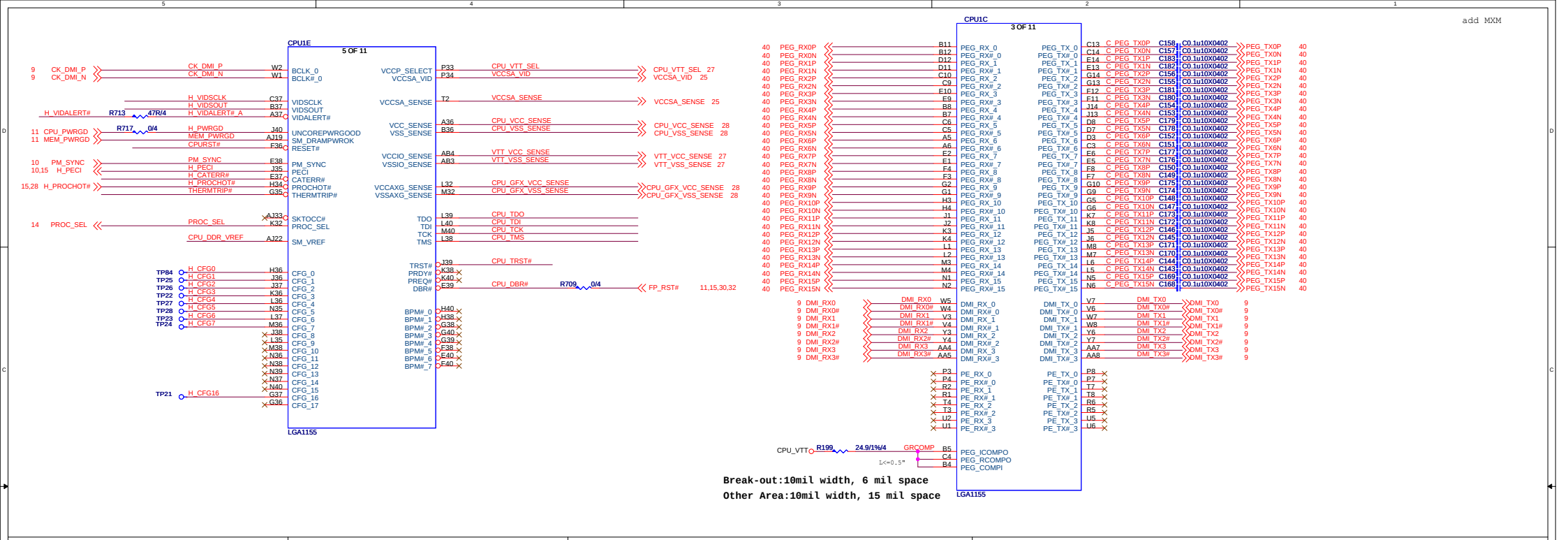

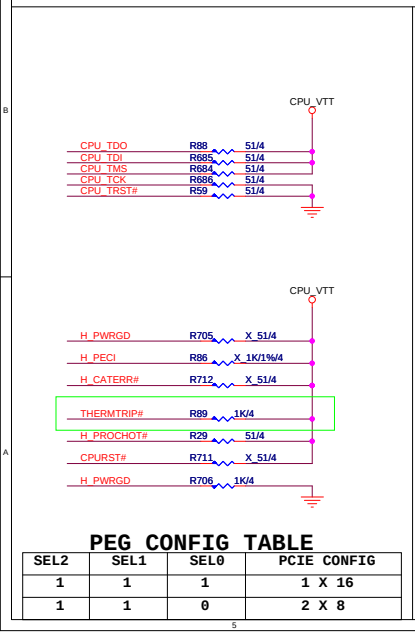

PEG CONFIG TABLE

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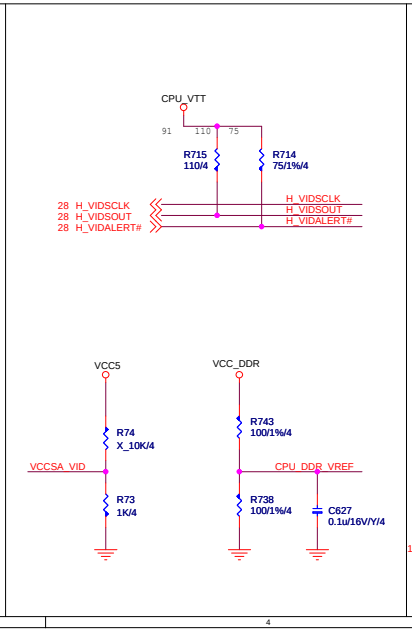
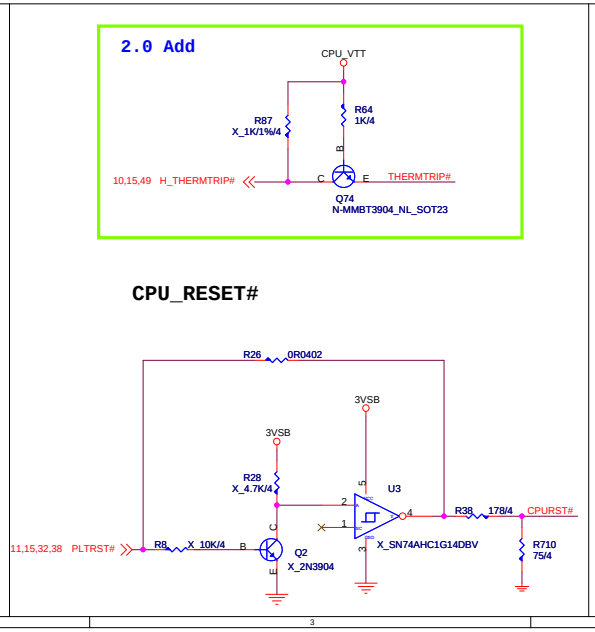
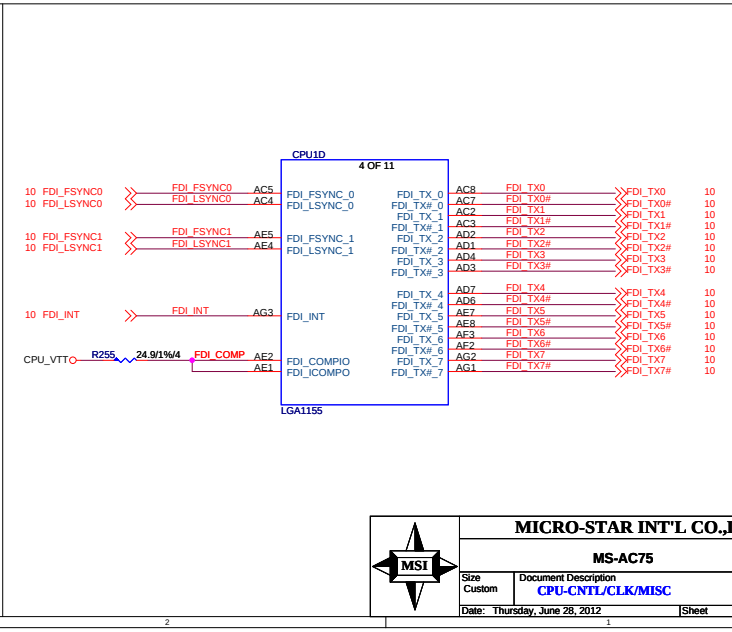
1	1	0	2 X 8







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MS-AC75	
Size: Custom	Document Description: CPU-CNTL/CLK/MISC
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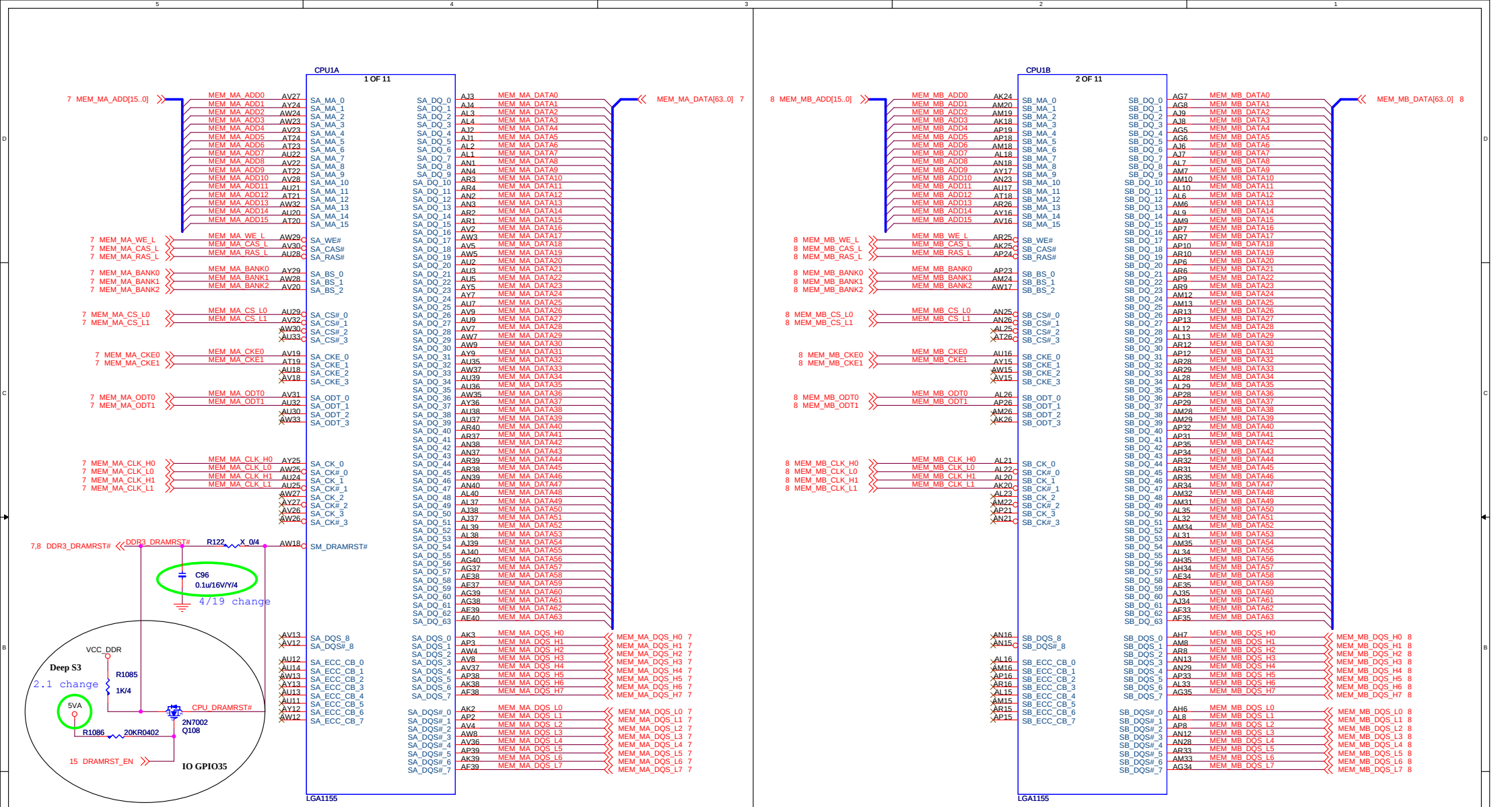

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU-Memory	Rev: 2.1
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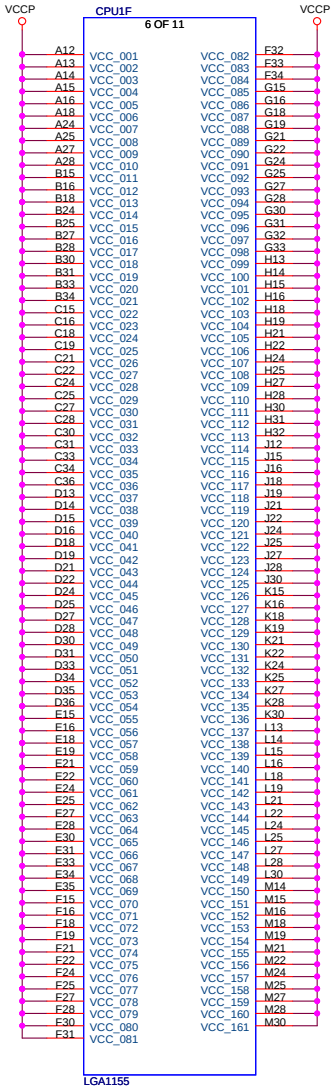
PROCESSOR VDDQ:4.75A

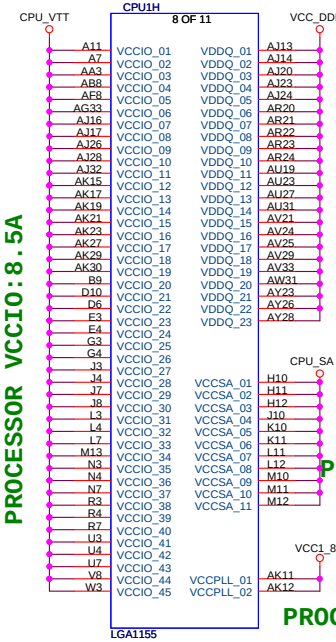
PROCESSOR VAXG:35A

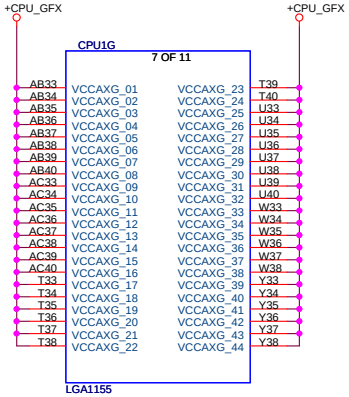
PROCESSOR VCCIO:8.5A

PROCESSOR VCCSA:8.8A

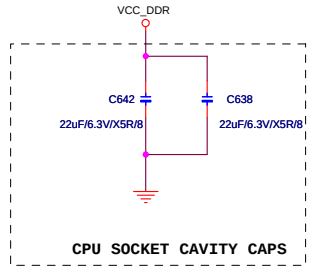
PROCESSOR VCCPLL:1.5A



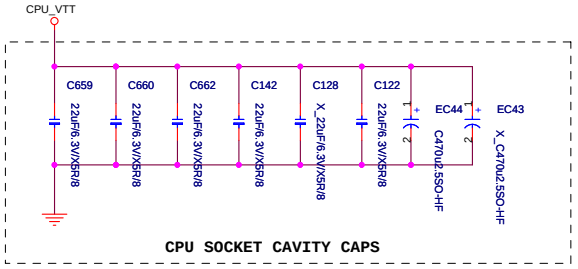


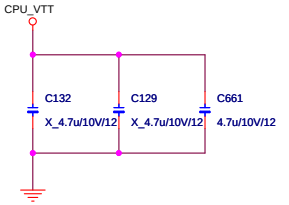


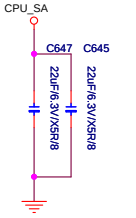
+1.5V_DDR3-Decoupling

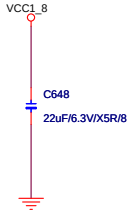


+CPU_VTT Decoupling









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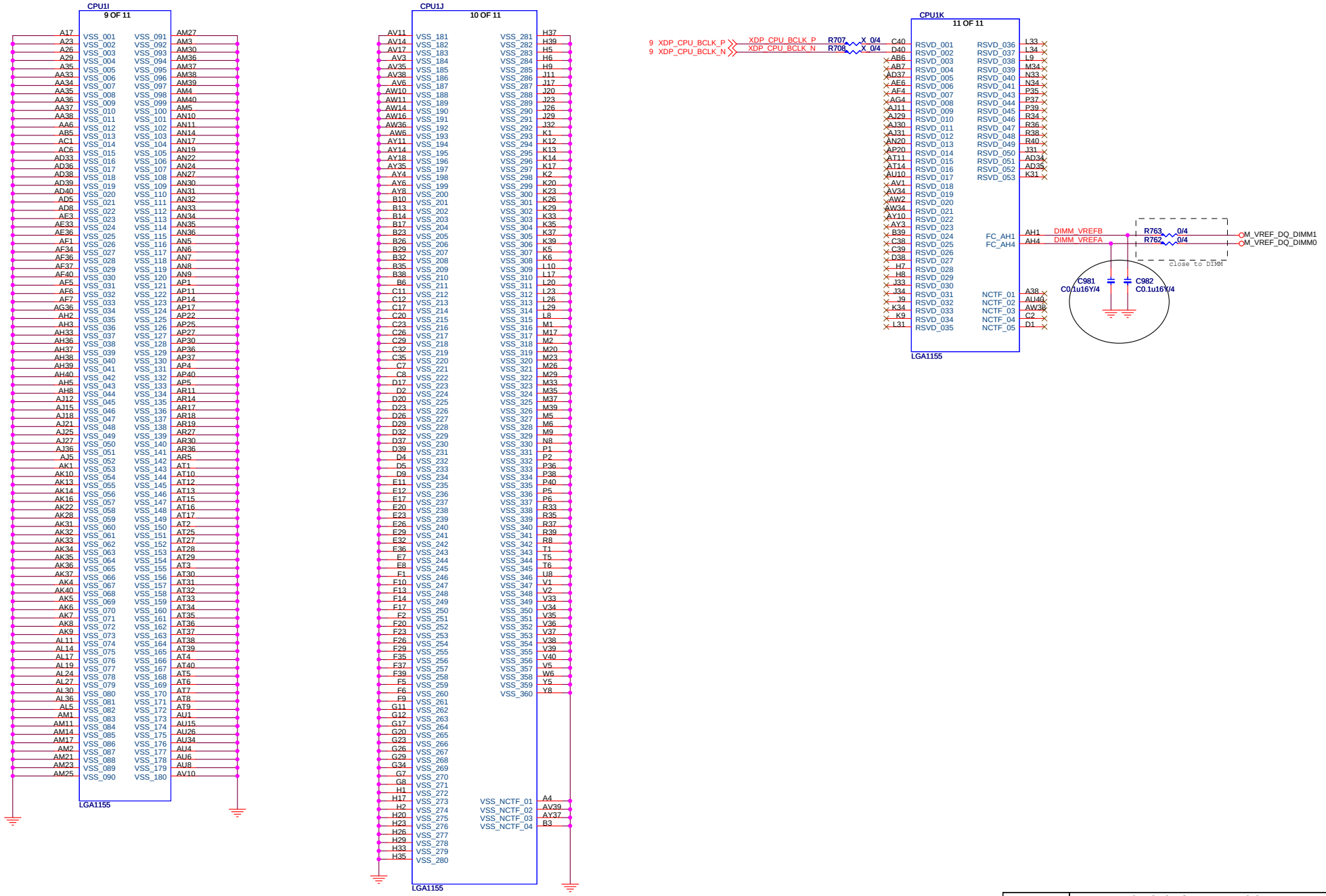

MICRO-STAR INT'L CO.,LTD		
MS-AC75		
Size: Custom	Document Description: CPU-GND	Rev: 2.1
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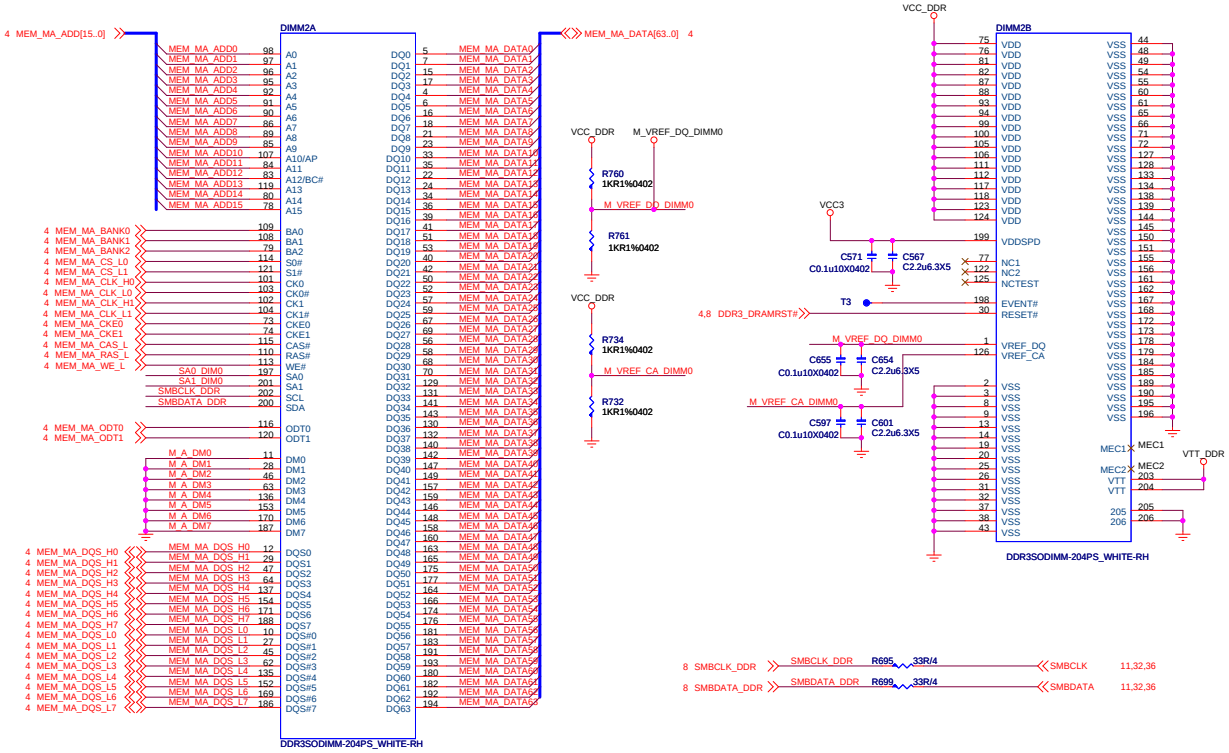
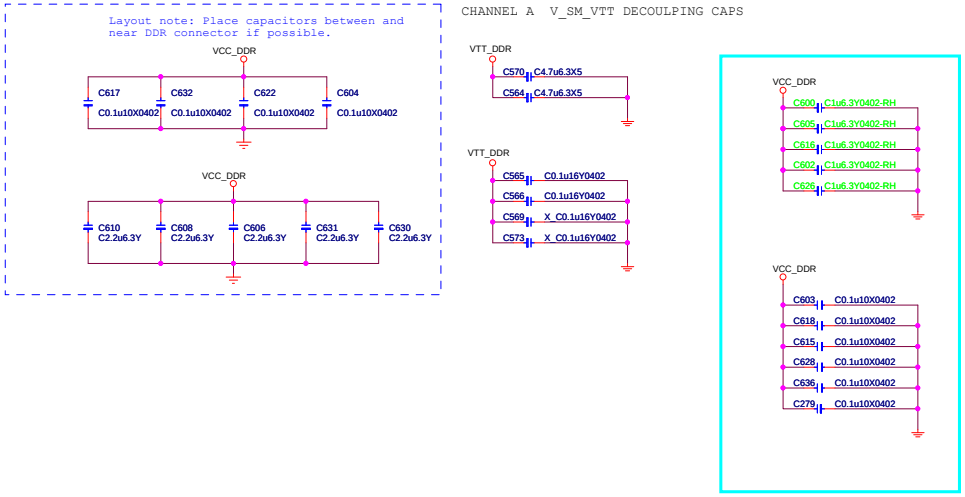
SODIMM#A



ADDRESS: 000
0xA0

H=11mm

CHANNEL A V_SM_VTT DECOULPING CAPS



MICRO-STAR INT'L CO.,LTD		
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Size: C	Document Description: DDR III SODIMM 1	Rev: 2.1
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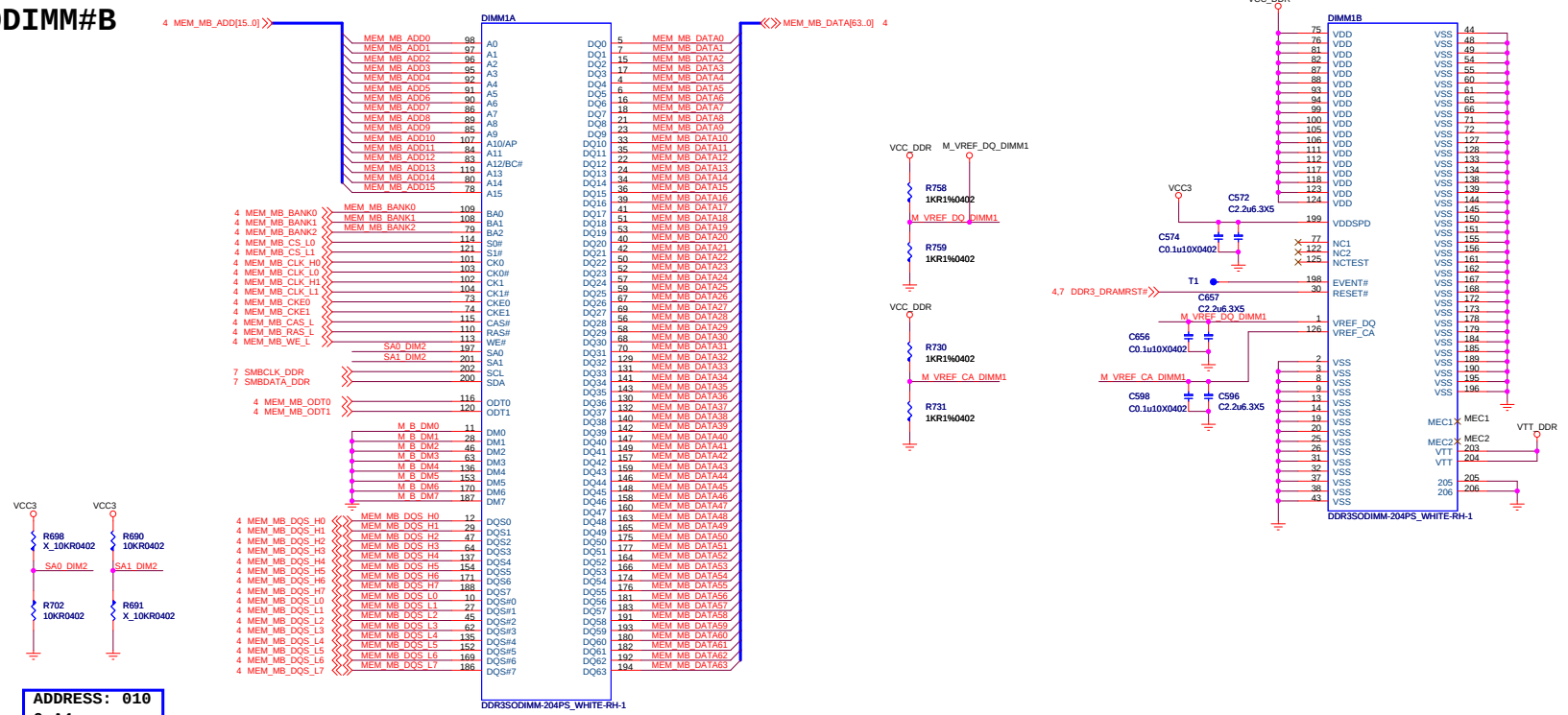
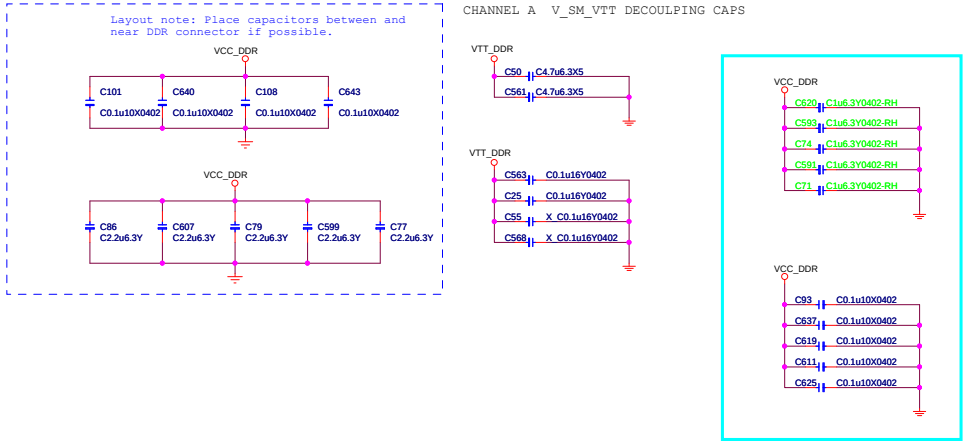
SODIMM#B





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	MS-AC75	
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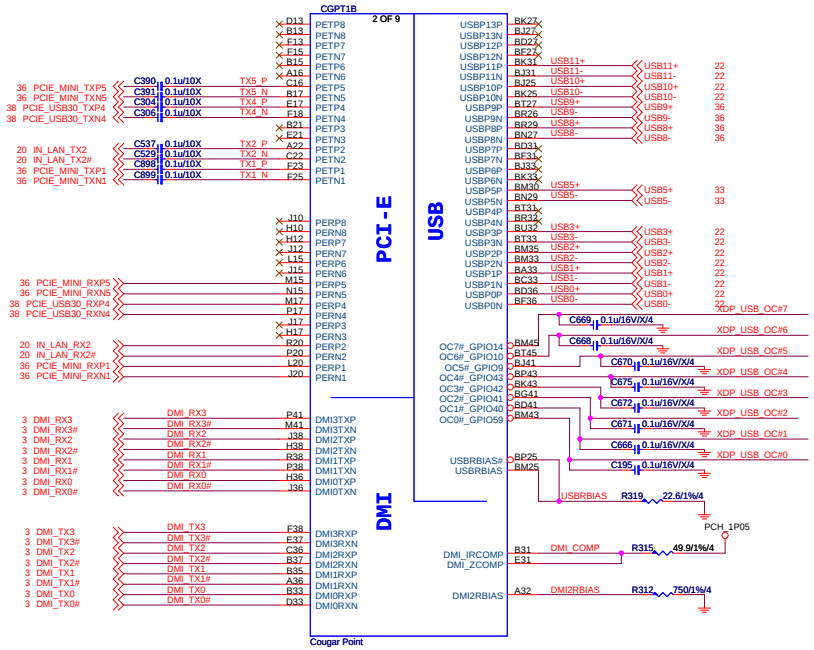
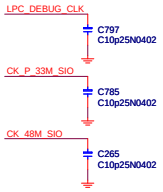
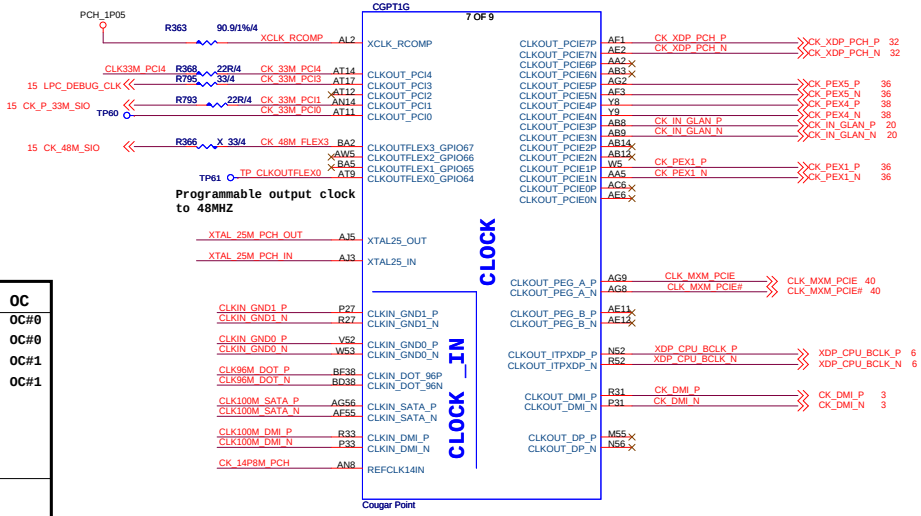
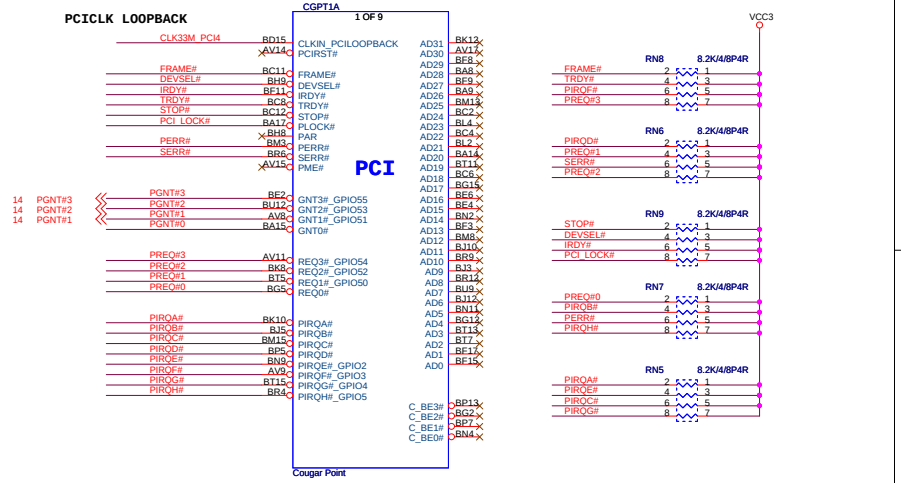
H61 SKU:PCIe ports 7 and 8 are disabled.
H61 SKU:USB ports 6, 7, 12 and 13 are disabled.

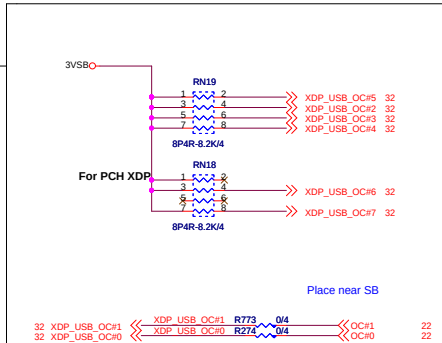


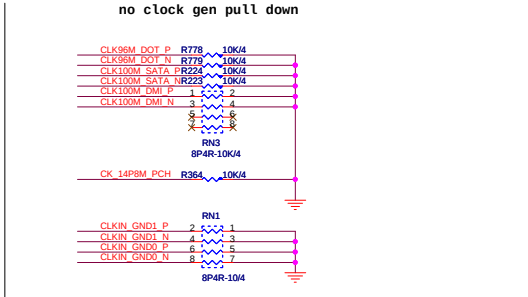


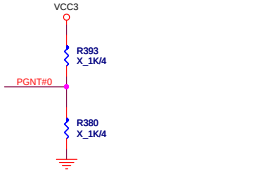
Pair		Device	OC
EHCI#1	0	USB Ext. Port ?	OC#0
	1	USB Ext. Port ?	OC#0
	2	USB Ext. Port ?	OC#1
	3	USB Ext. Port ?	OC#1
	4	-	
	5	Card Reader	
	6	X	
	7	X	
EHCI#2	8	Mini card (WLAN)	
	9	Mini card (TV)	
	10	Webcam	
	11	Touch Screen	
	12	X	
	13	X	

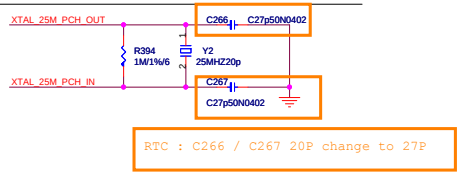












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	MS-AC75
Size: C	Document Description: CP PCI/E/DMI/USB/CLK
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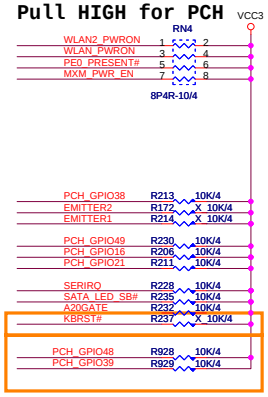
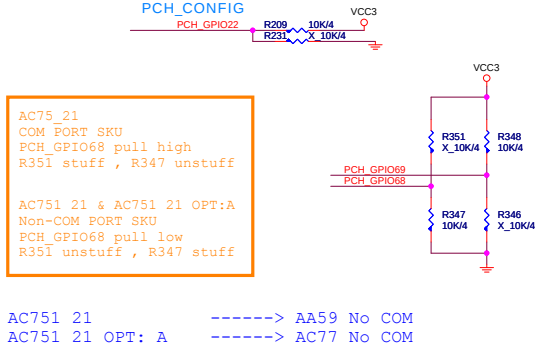
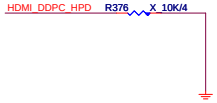
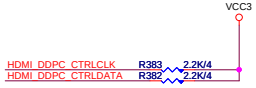
H61 SKU:SATA ports 2 and 3 are disabled.









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Custom	CP SATA/HOST/FAN/GPIO/VGA	2.1

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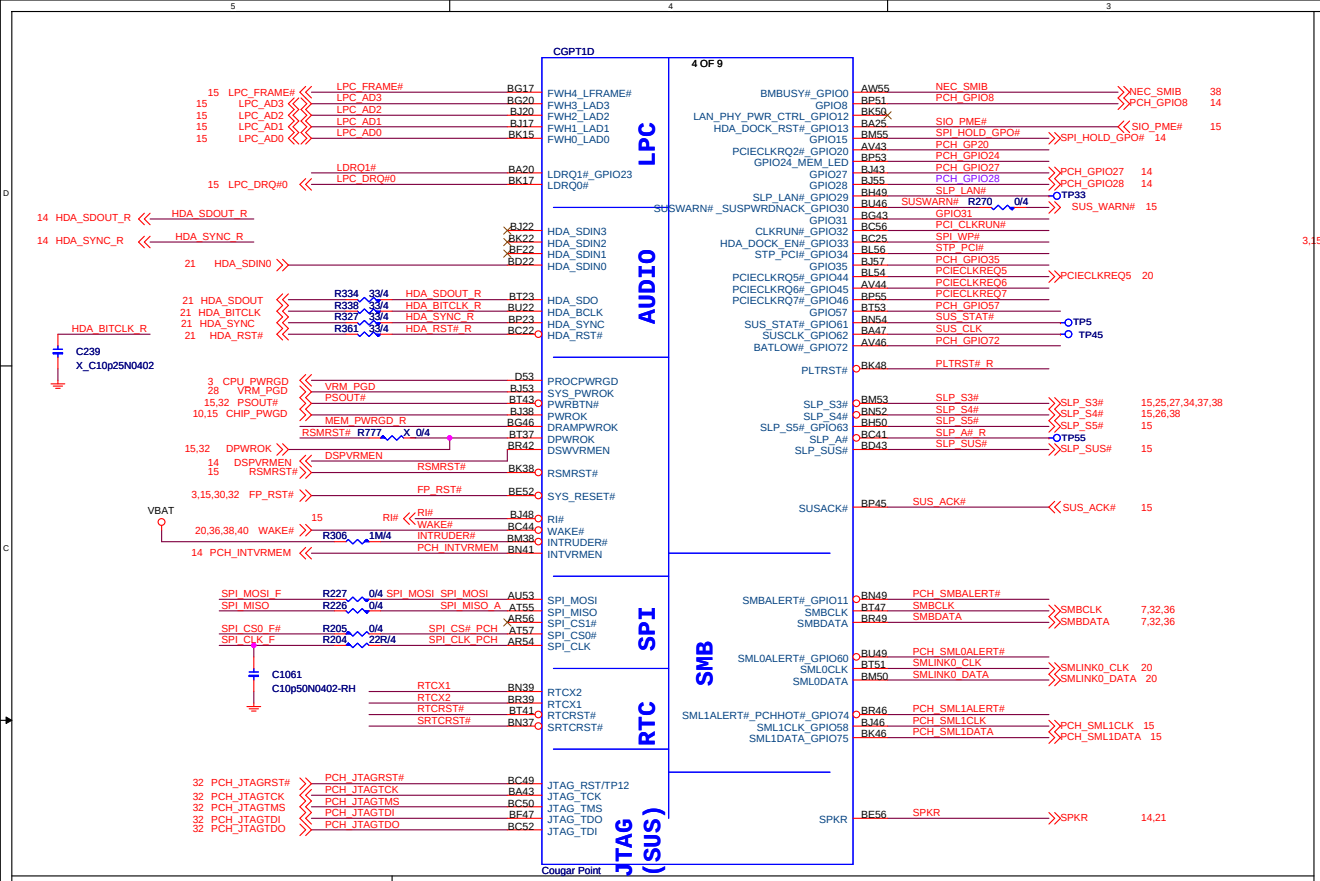

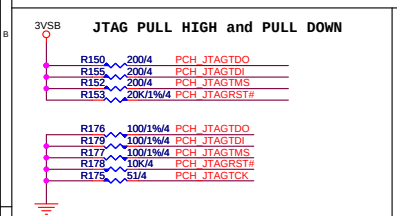

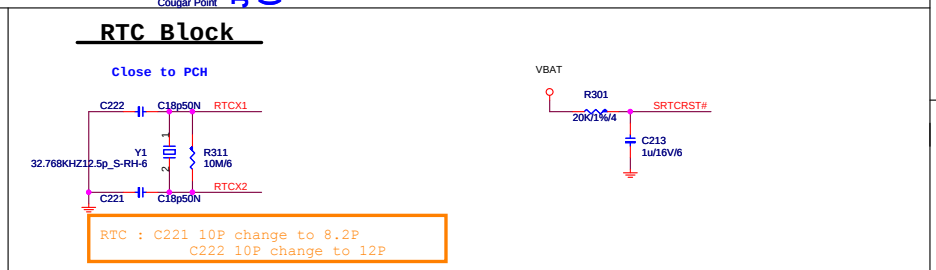

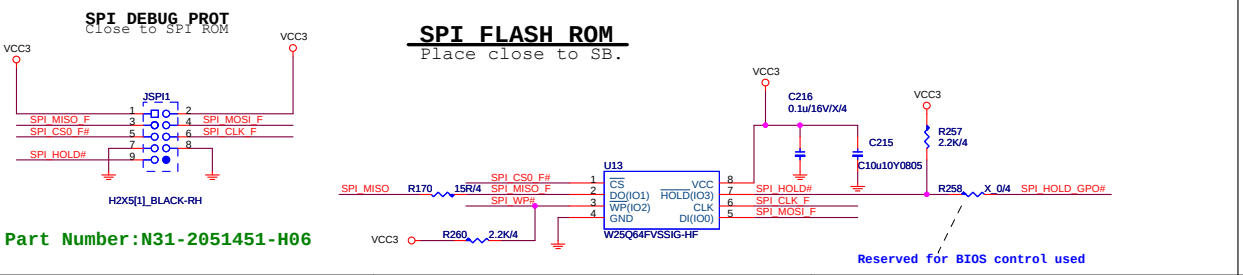

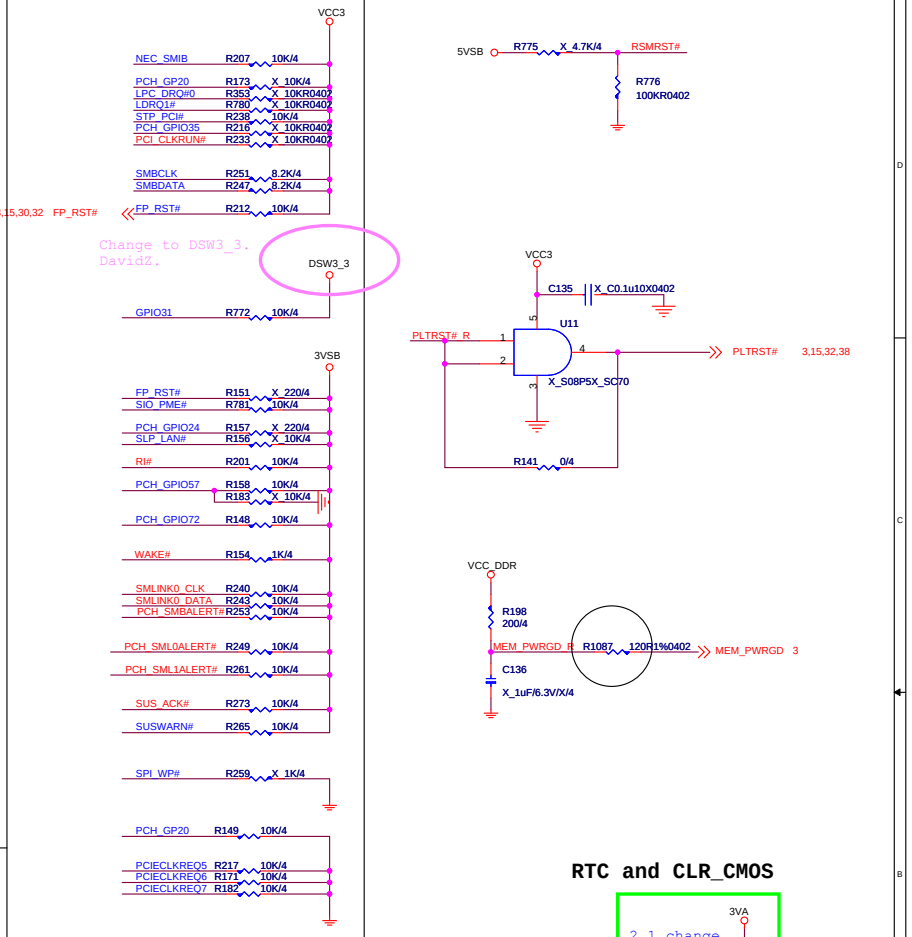

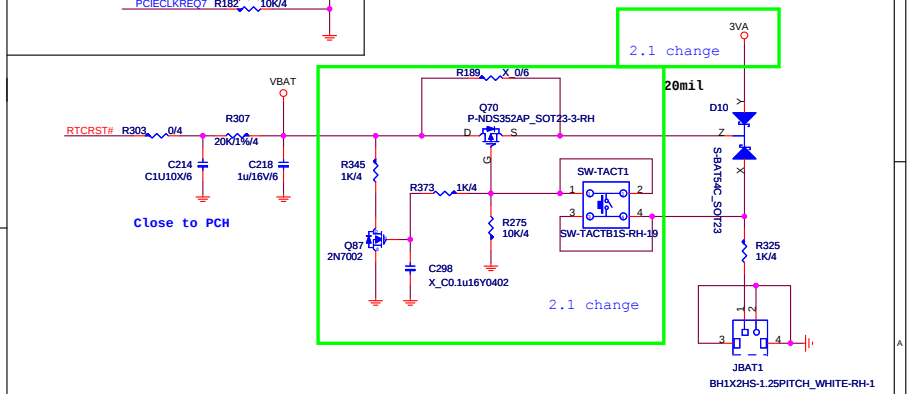

MICRO-STAR INT'L CO.,LTD

MS-AC75

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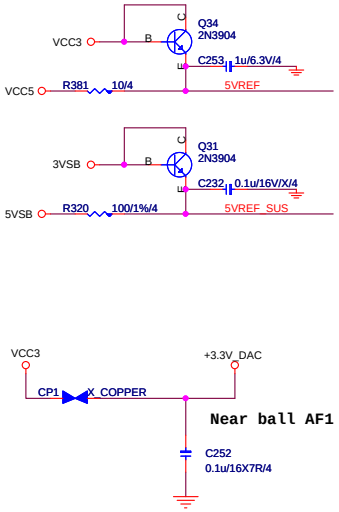
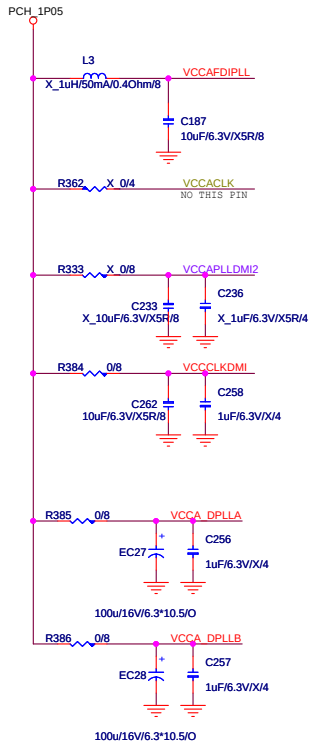
Table 3-7. VCCPLL Decoupling Requirements

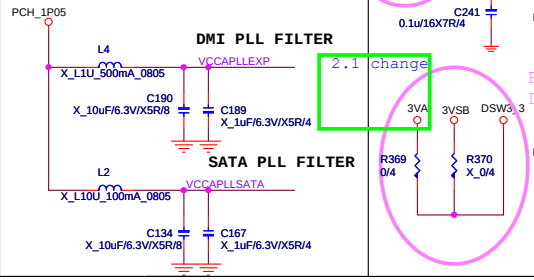
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Electrolytic 220µF	1	77mΩ	3.3nH	Output	North of processor - as close to RM keep-out as possible	1
10µF 0805 X5R	1	3mΩ	0.51nH	Output		1,2,3

Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

5VREF & 5VREF_SUS Sequencing Circuit

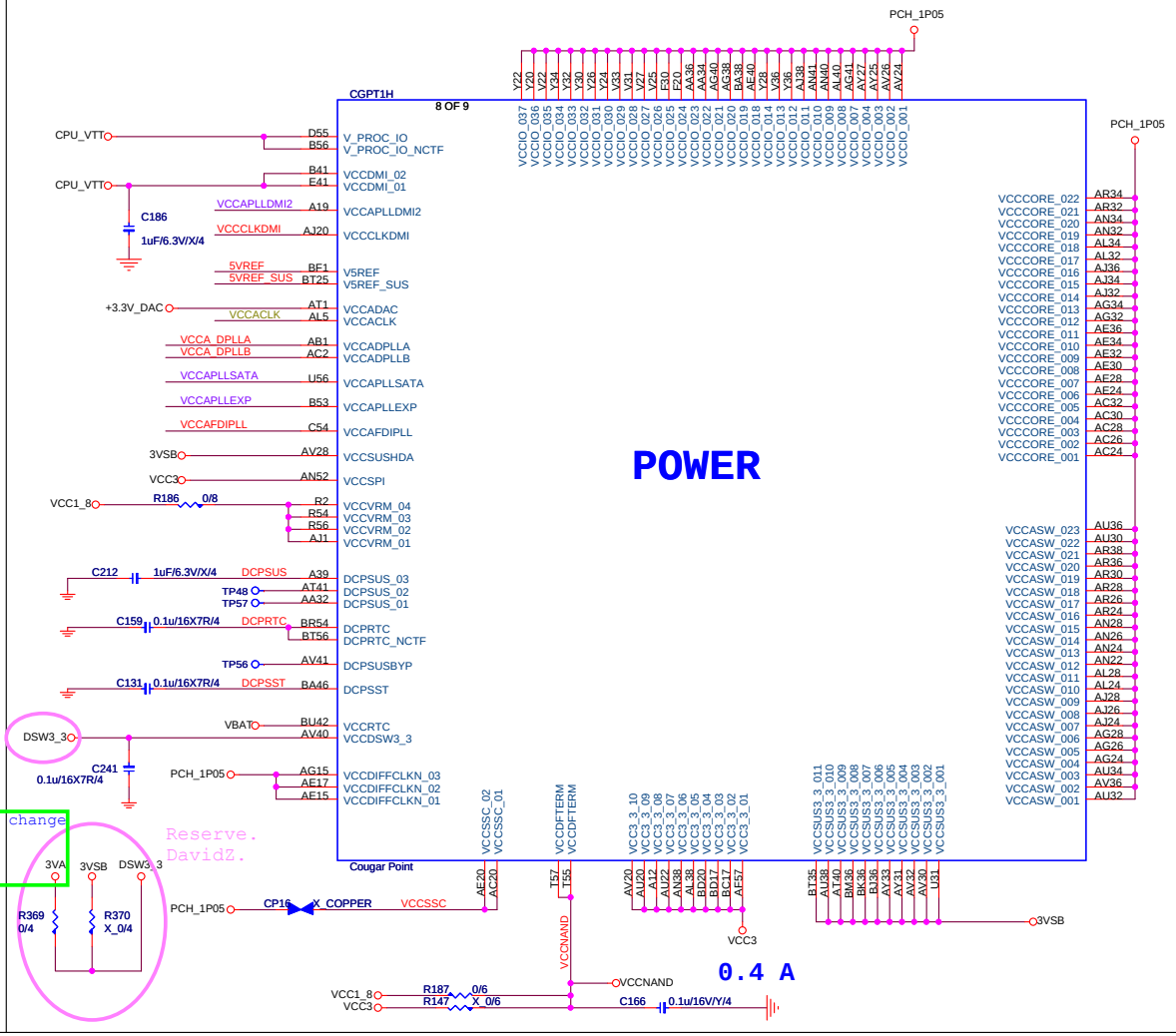




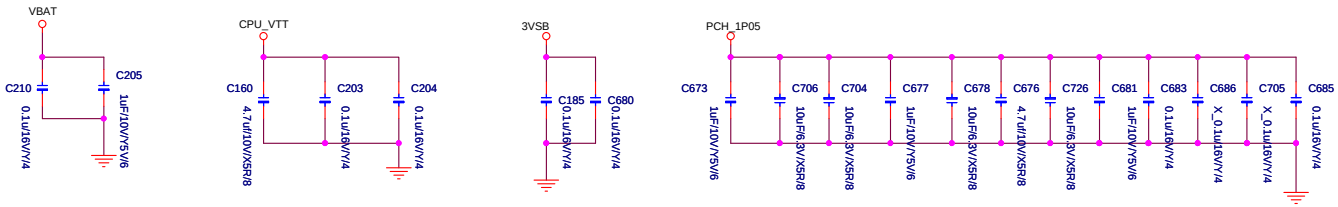


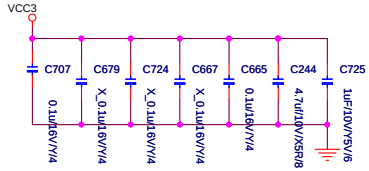
2.1 change

Reserve. DavidZ.



PCH decoupling cap





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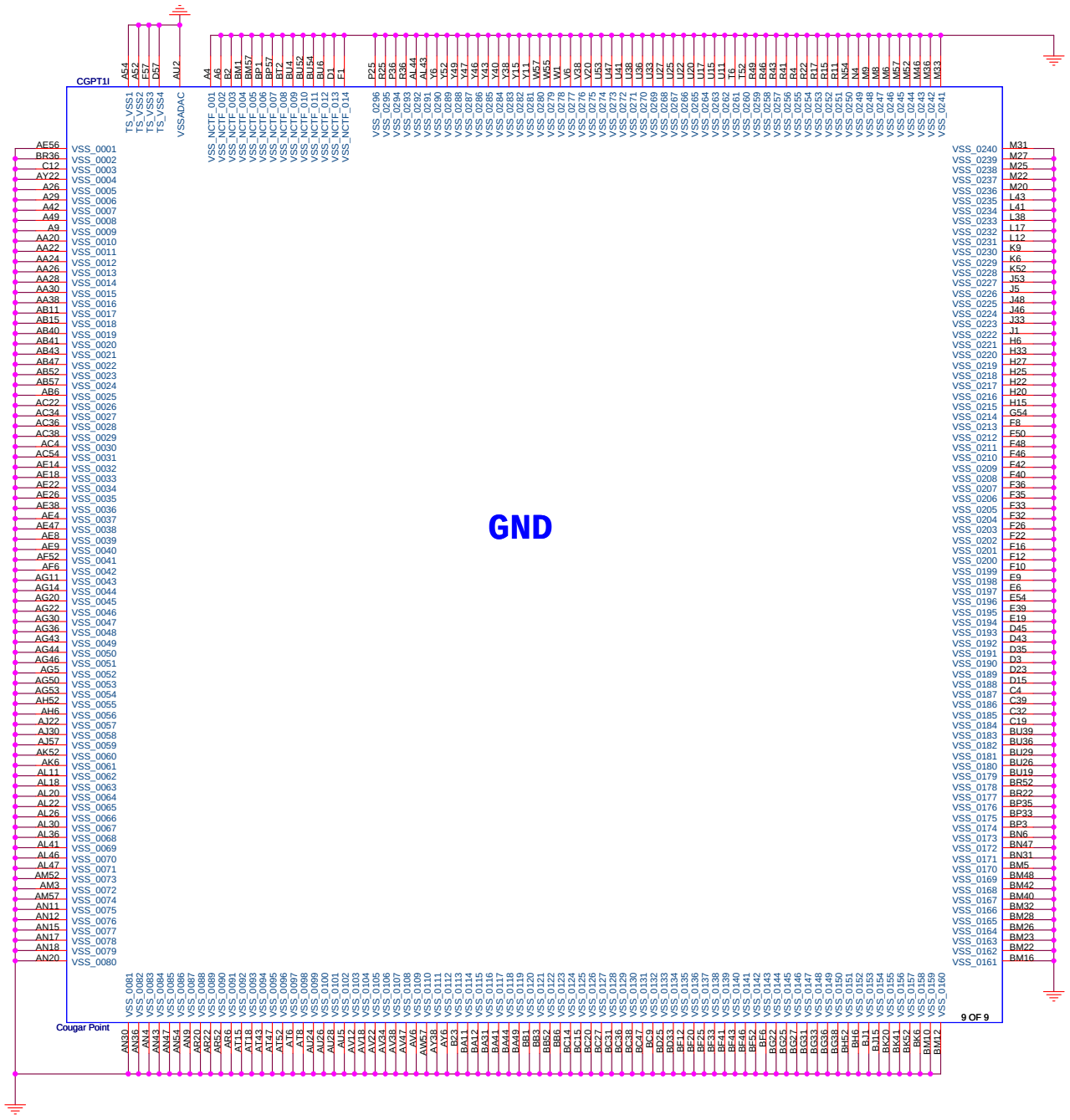
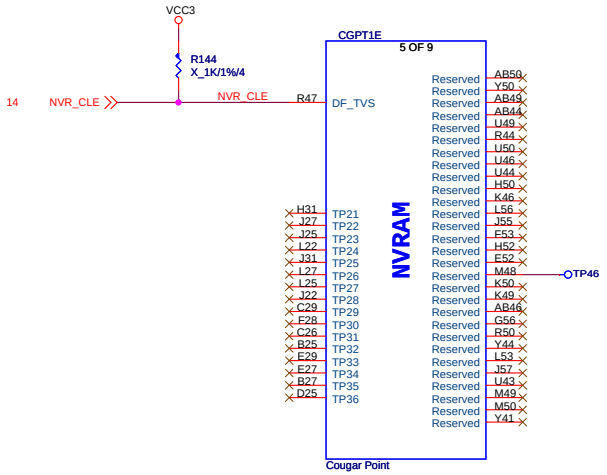


DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



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MS-AC75		
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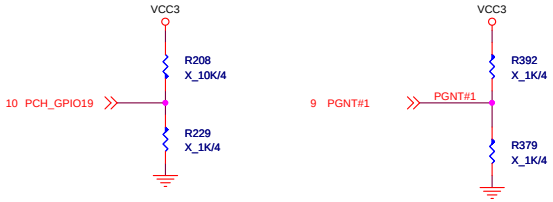
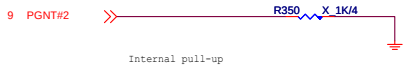
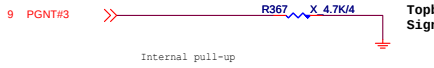
CP REQUIRED STRAPS

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating

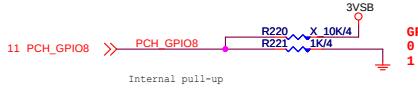




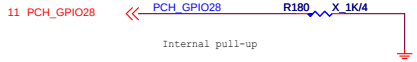
DMI AC/DC MODE
0 : AC
1 : DC *



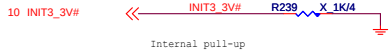
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ????????????????
1 : ???????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

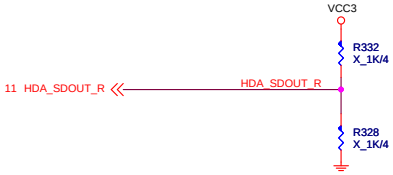
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

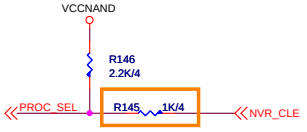
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



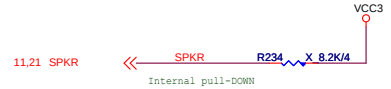
HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY

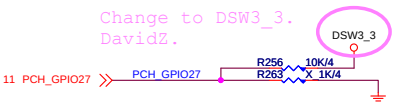


DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



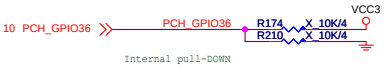
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

Change to DSW3_3.
DavidZ.

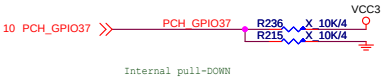


In Deep Sleep Power Well.

If not used,require a weak pull-up(8.2k~10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high



Cougar point EDS PAGE:93 This signal should not be pull high

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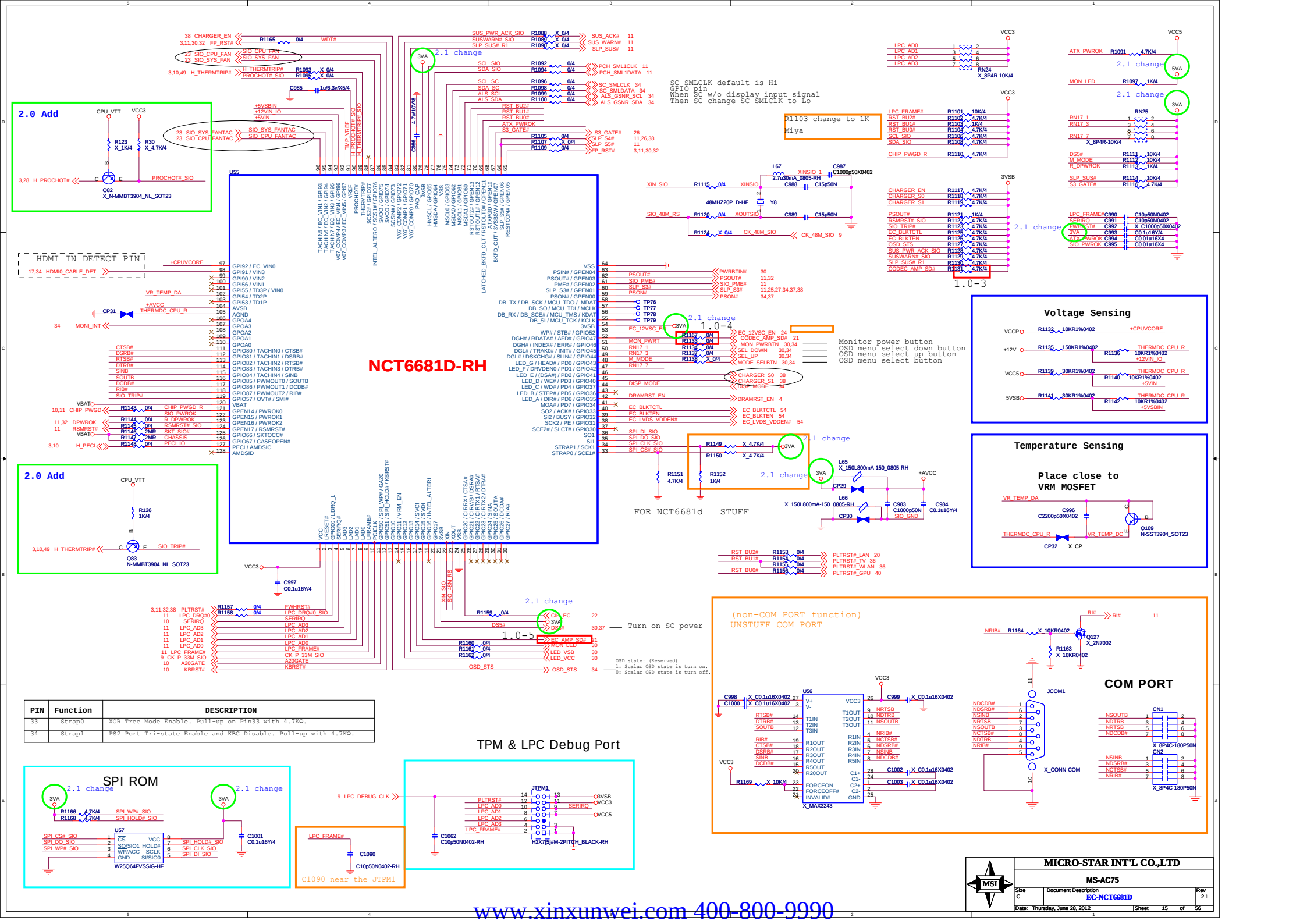

PIN	Function	DESCRIPTION
33	Strap0	XOR Tree Mode Enable. Pull-up on Pin33 with 4.7KΩ.
34	Strap1	PS2 Port Tri-state Enable and KBC Disable. Pull-up with 4.7KΩ.

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Custom	Reserved	2.1

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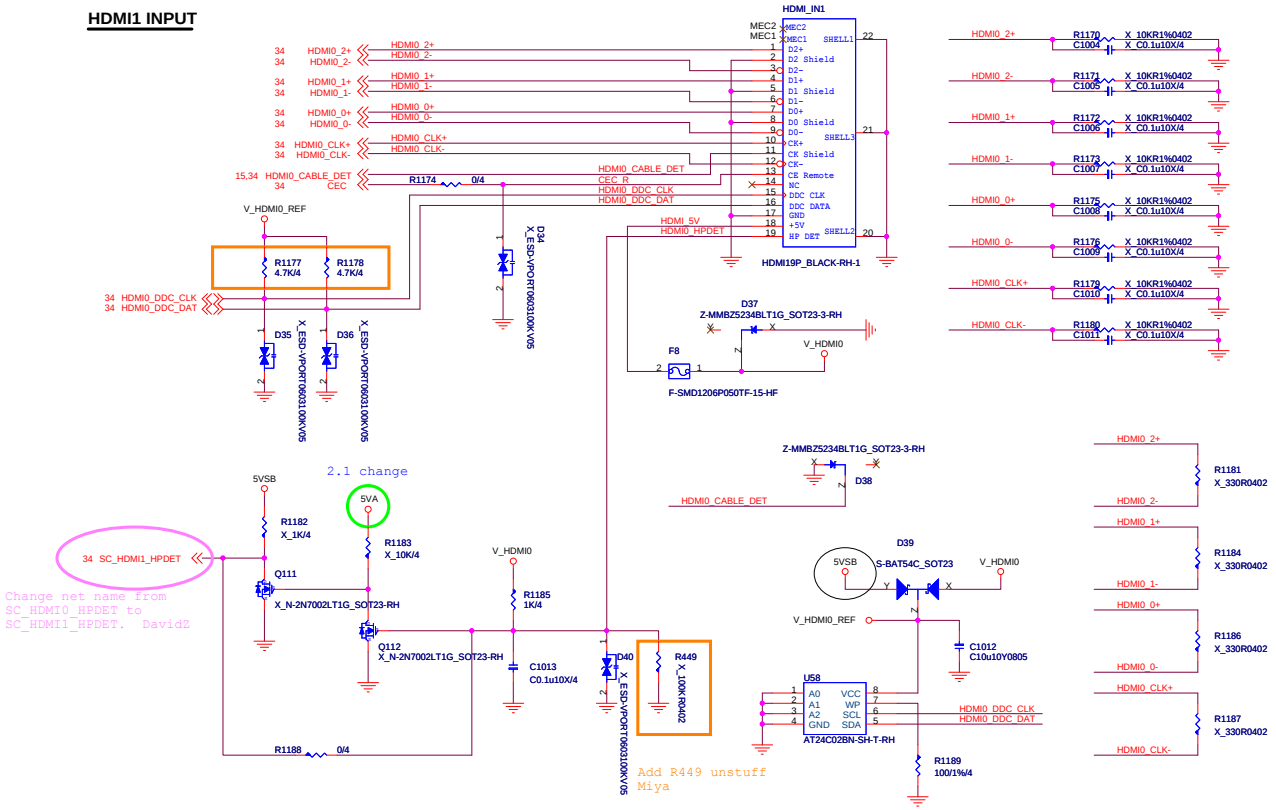
N5Y-19M0221-H06

HDMI1 INPUT



M33-24C02X3-A26

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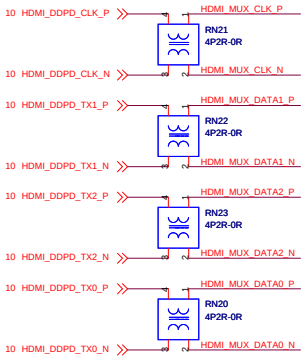
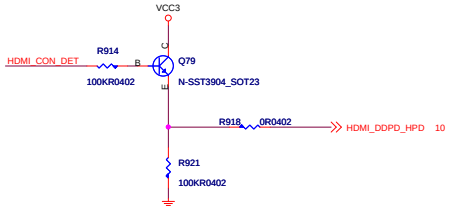
PCH

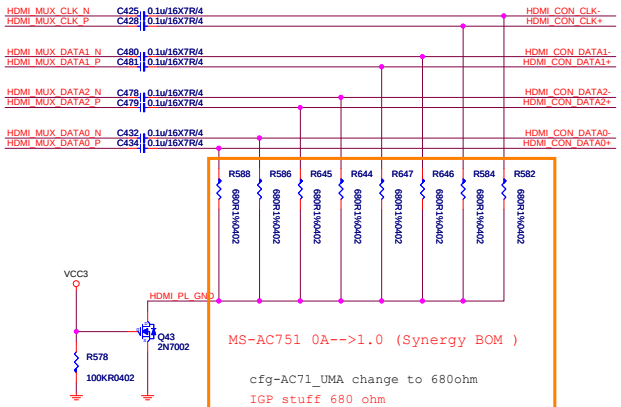
GPIO	Alt Func	Type	POWER	SMI	TOL	DEFAULT	SIGNAL NAME	Pull up or Pull down	BIOS
GPIO0	BMBUSY#	I/O	CORE	Y	3.3V	GPI	NEC_SMIB	Pull-up 10K to VCC3	GPI
GPIO1		I/O	CORE	Y	3.3V	GPI	WLAN2_PWRON		GPO
GPIO2	PIRQE#	I/OD	CORE	Y	5V	GPI	PIRQE#	Pull-up 8.2K to VCC3	No USE
GPIO3	PIRQF#	I/OD	CORE	Y	5V	GPI	PIRQF#	Pull-up 8.2K to VCC3	No USE
GPIO4	PIRQG#	I/OD	CORE	Y	5V	GPI	PIRQG#	Pull-up 8.2K to VCC3	No USE
GPIO5	PIRQH#	I/OD	CORE	Y	5V	GPI	PIRQH#	Pull-up 8.2K to VCC3	No USE
GPIO6		I/O	CORE	Y	3.3V	GPI	BKLT-	Pull-up 10K to VCC3	GPI
GPIO7		I/O	CORE	Y	3.3V	GPI	BKLT+	Pull-up 10K to VCC3	GPI
GPIO8	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	PCH_GPIO8	Pull-down 1K to GND	No USE
GPIO9	OC5#	I/O	Suspend	Y	3.3V	Native	OC5#	Pull-up 10K to 3VSB	Native
GPIO10	OC6#	I/O	Suspend	Y	3.3V	Native	OC6#	Pull-up 10K to 3VSB	Native
GPIO11	SMBALERT#	I/O	Suspend	Y	3.3V	Native	PCH_GPIO11	Pull-up 10K to 3VSB	No USE
GPIO12	LAN_PHY_PWR_CTRL	I/O	Suspend	Y	3.3V	Native	(NC)		No USE
GPIO13	HDA_DOCK_RST#	I/O	Suspend	Y	3.3V	GPI	SIO_PME#		No USE
GPIO14	OC7#	I/O	Suspend	Y	3.3V	Native	OC7#	Pull-up 10K to 3VSB	Native
GPIO15	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	SPI_HOLD_GPO#	Internal pull-down	Straps
GPIO16	SATA4GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO16	Pull-up 10K to VCC3	No USE
GPIO17		I/O	CORE	N	3.3V	GPI	WLAN_PWRON	Pull-up 10K to VCC3	GPO
GPIO19		I/O	CORE	N	3.3V	GPI	PCH_GPIO19	Internal pull-up	Straps
GPIO20	PCIECLKRQ2#	I/O	CORE	N	3.3V	Native	PCH_GP20	Pull-down 10K to GND	Native
GPIO21	SATA0GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO21	Pull-up 10K to VCC3	No USE
GPIO22	SCLOCK	I/O	CORE	N	3.3V	GPI	PCH_GPIO22	Pull-up 10K to VCC3	No USE
GPIO23	LDRQ1#	I/O	CORE	N	3.3V	Native	(NC)		No USE
GPIO24	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PCH_GPIO24	Pull-up 10K to 3VSB	No USE
GPIO25	PCIECLKRQ3#	I/O	Suspend	N	3.3V	Native	USB3_CLKRQ#	Pull-up 10K to 3VSB	Native
GPIO26	PCIECLKRQ4#	I/O	Suspend	N	3.3V	Native	PCIECLKRQ4#	(pull high)	Native
GPIO27	Unmultiplexed	I/O	Deep Sleep	N	3.3V	GPI	DSW_WAKE#	internal pull-up	GPI
GPIO28	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PLL_ODVR_EN	internal pull-up	Straps
GPIO29	SLP_LAN#	I/O	Suspend	N	3.3V	GPI	SLP_LAN#	Pull-up 10K to 3VSB	No USE
GPIO30	SUSPWRDNACK	I/O	Deep Sleep	N	3.3V	Native	SUSPWRACK	Pull-up 10K to 3VSB	Native
GPIO31	ACPRESENT	I/O	Deep Sleep	N	3.3V	GPI	AC_PRESENT	Pull-up 10K to 3VSB	No USE
GPIO32	CLKRUN#	I/O	CORE	N	3.3V	GPO	PM_CLKRUN#	Pull-up 8.2K to VCC3	
GPIO33	HDA_DOCK_EN#	I/O	CORE	N	3.3V	GPO	HDA_DOCK_EN#	Test Pin	No USE
GPIO34	STP_PCI#	I/O	CORE	N	3.3V	GPI	STP_PCI#	Pull-up 10K to VCC3	No USE
GPIO35	(Mobile Only)	I/O	CORE	N	3.3V	GPO	PCH_GPIO35	Test Pin	No USE
GPIO36	SATA2GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO36	Pull-down 10K to GND	Straps
GPIO37	SATA3GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO37	Pull-down 10K to GND	Straps
GPIO38	SLOAD	I/O	CORE	N	3.3V	GPI	PCH_GPIO38	Pull-up 10K to VCC3	No USE
GPIO39	SDATAOUT0	I/O	CORE	N	3.3V	GPI	GFX_DET		GPI
GPIO40	OC1#	I/O	Suspend	N	3.3V	Native	USB_OC1#	(pull high)	Native



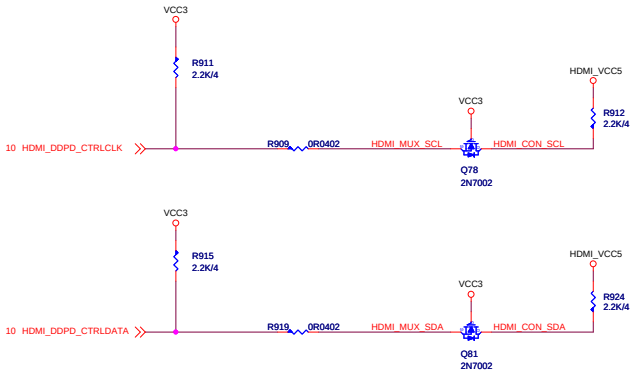


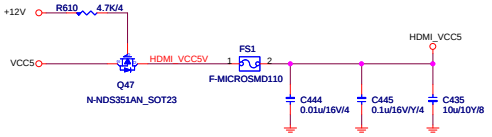
MS-AC751 0A-->1.0 (Synergy BOM)
RN11 , RN12 ,RN14, RN15 unstuff ,
RN20 , RN21 ,RN22, RN23 stuff

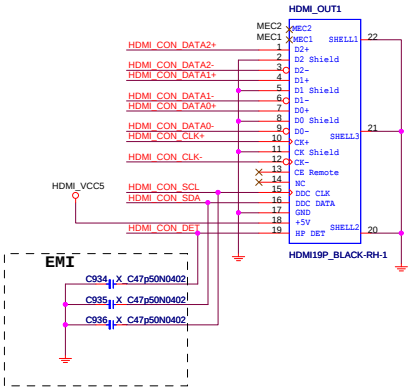
R913 , R910 ,R907, R916 ,R920 unstuff ,
R918 , R911 ,R909, R915 ,R919 stuff



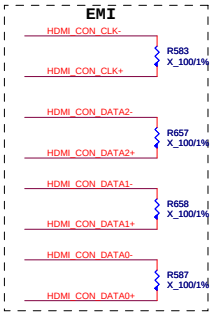
MS-AC751 0A-->1.0 (Synergy BOM)
cfg-AC71_UMA change to 680ohm
IGP stuff 680 ohm
GPU stuff 499 ohm







2011.06.29 EMI test unstuff C934 ,C935 ,C936



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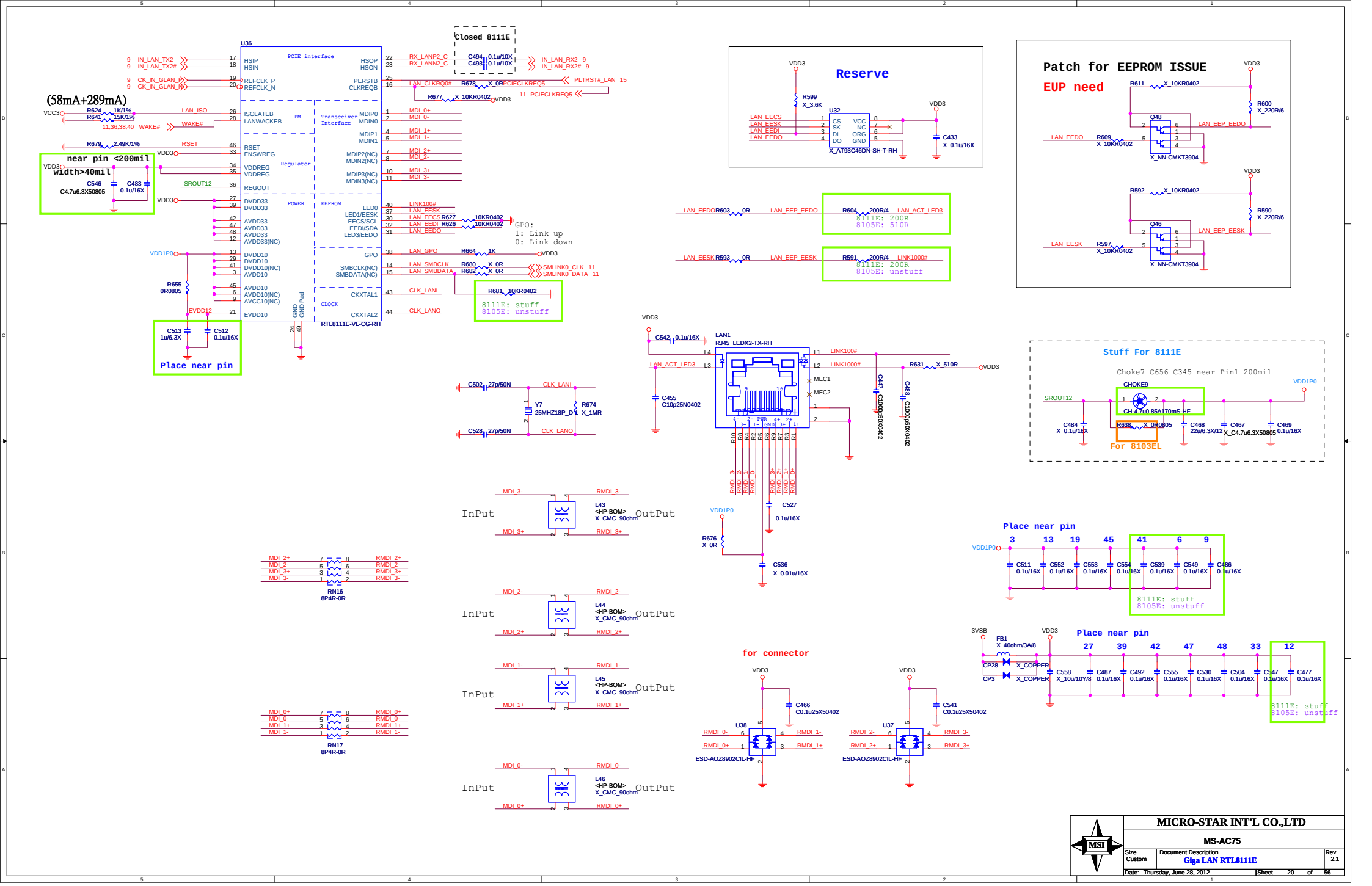

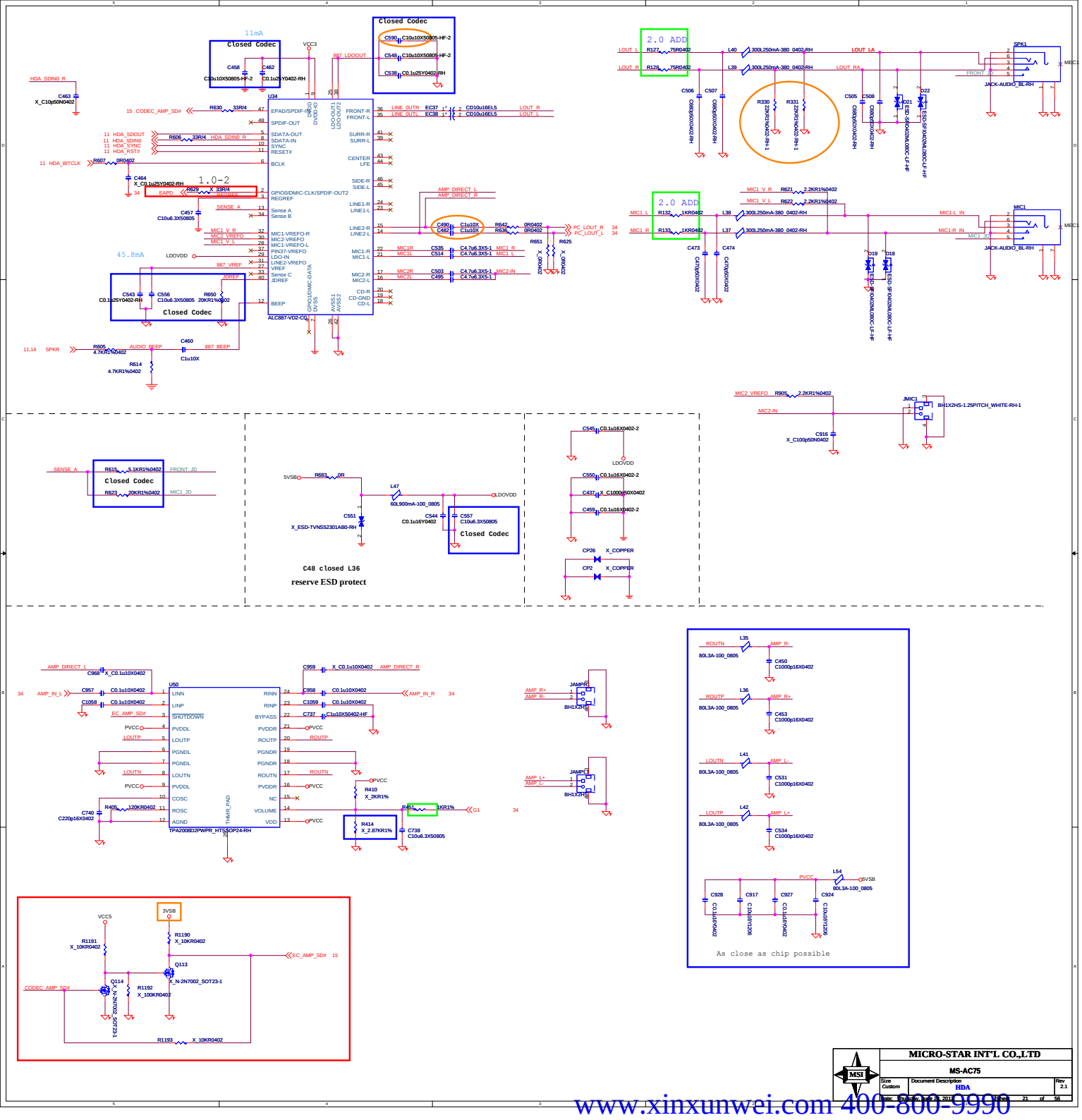
Closed Codec
ALC887-VD2-CG
U34
2.0 ADD
SPK1
MIC1
JACK-AUDIO_BL-RH
Closed Codec
C48 closed L36
reserve ESD protect
U50
TPA2008D2PWPR_HTSSOP24-RH
As close as chip possible
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HDA
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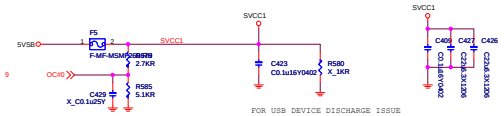
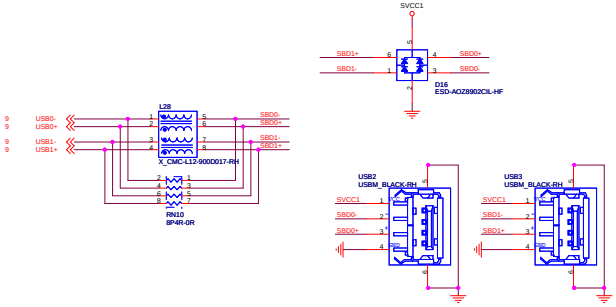
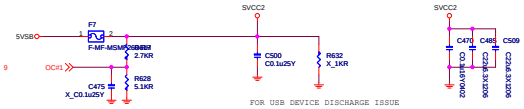
POWER CIRCUIT FOR USB PORT 0,1 (REAR)



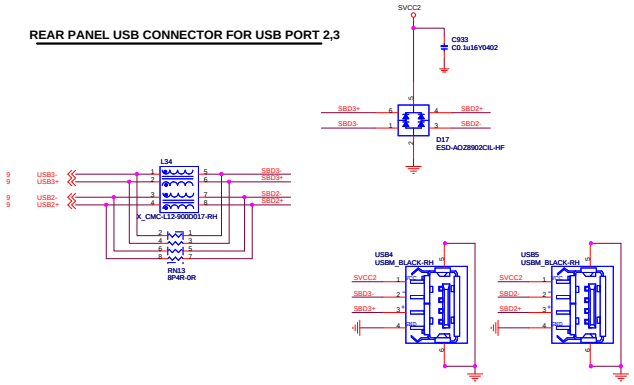
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



POWER CIRCUIT FOR USB PORT 2,3 (REAR)

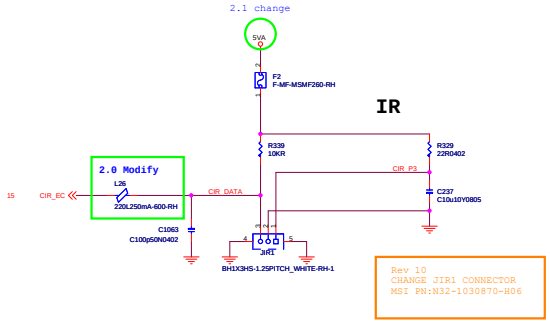


REAR PANEL USB CONNECTOR FOR USB PORT 2,3

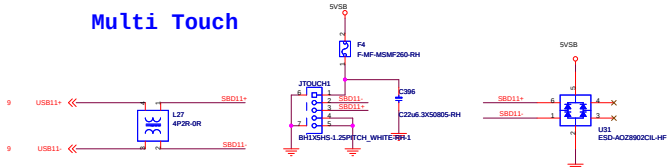


2.1 change

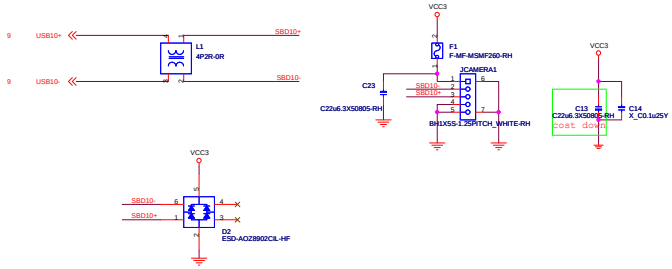
IR



Multi Touch



Webcam



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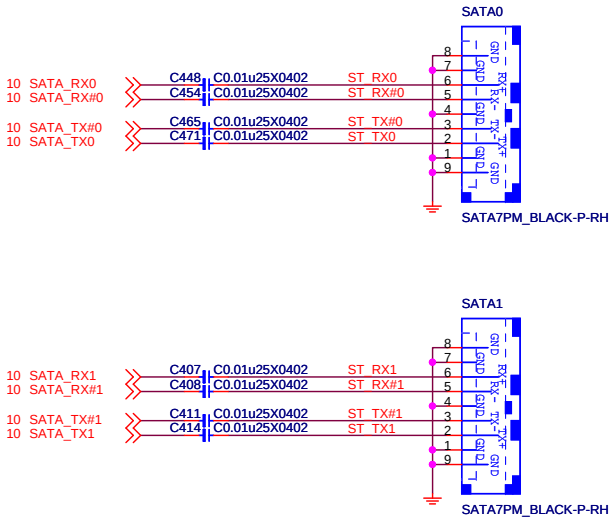
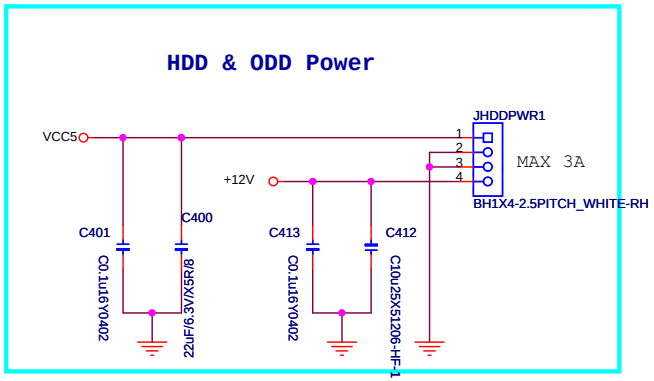
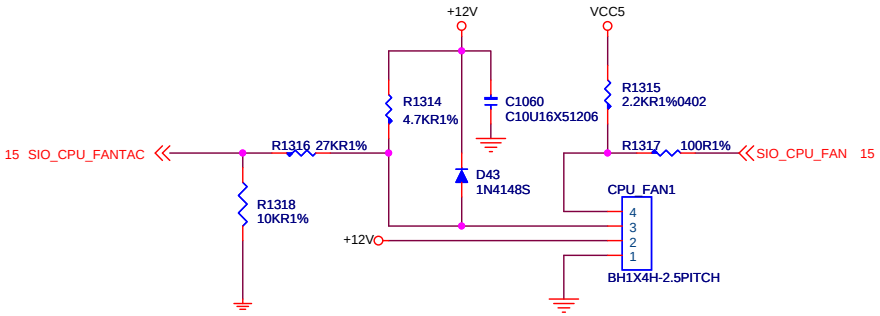
SATA HDD

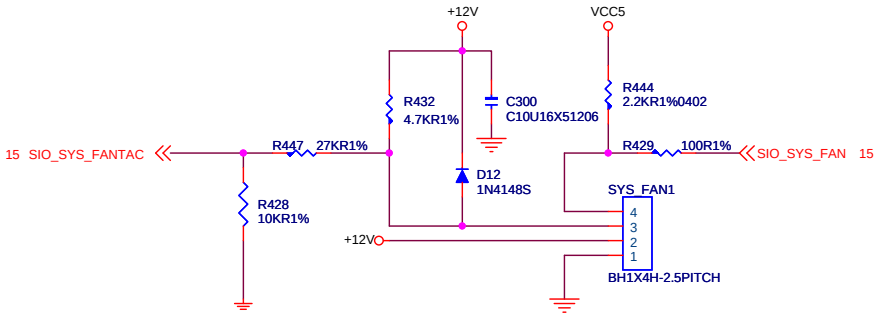




CPU FAN



SYSTEM FAN



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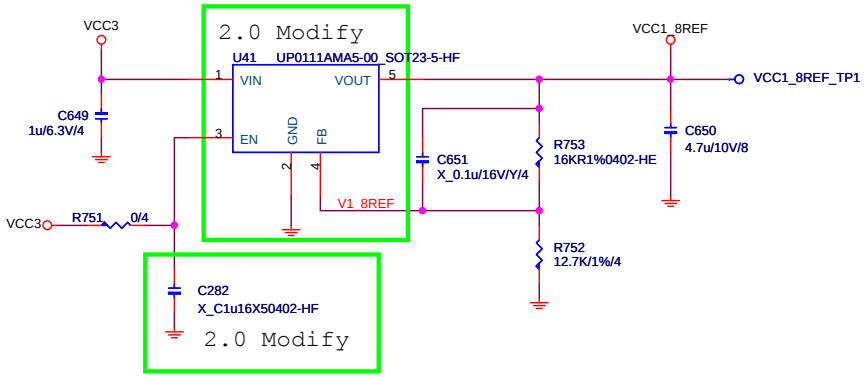
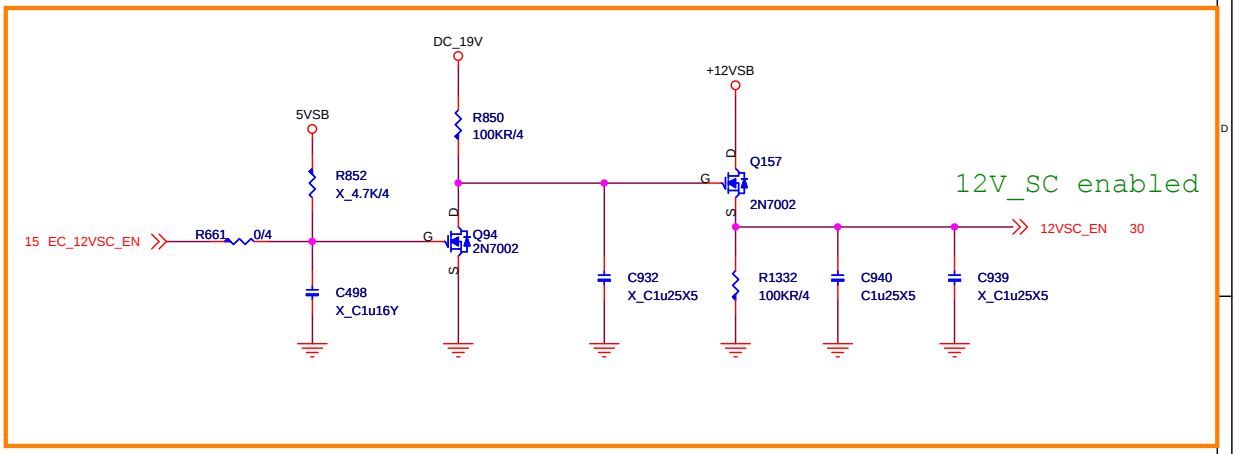
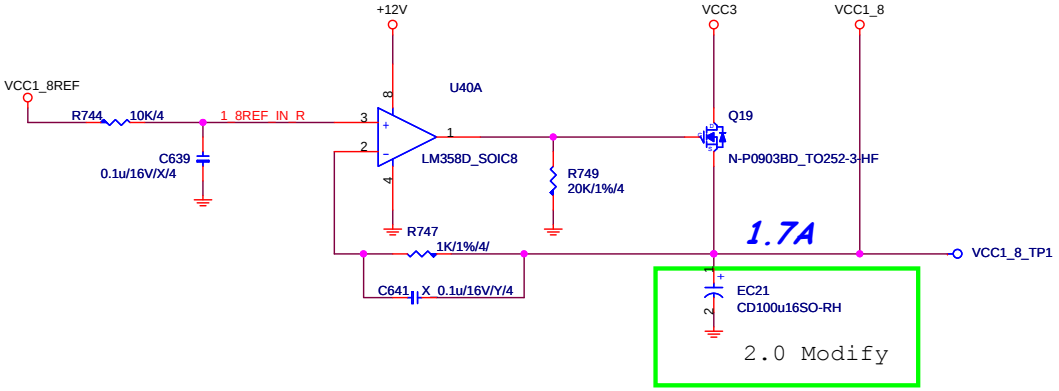
VCC1_8REF

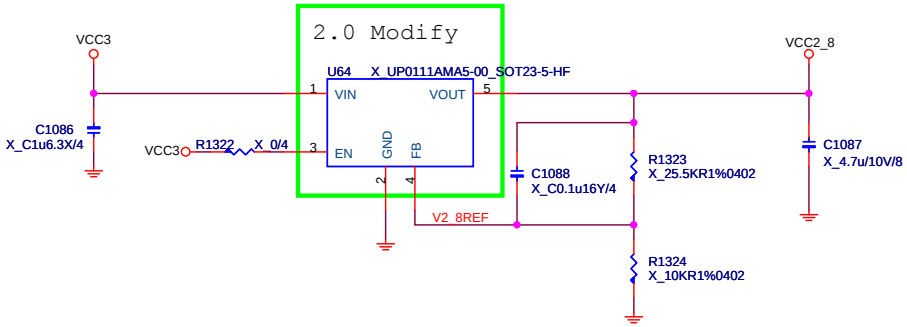




CPU_PLL_1_8



VCC2_8



MS-AC751 0A-->1.0 (unstuff)

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	MS-AC75	
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CPU_SA Power

VTT-->CPU_SA

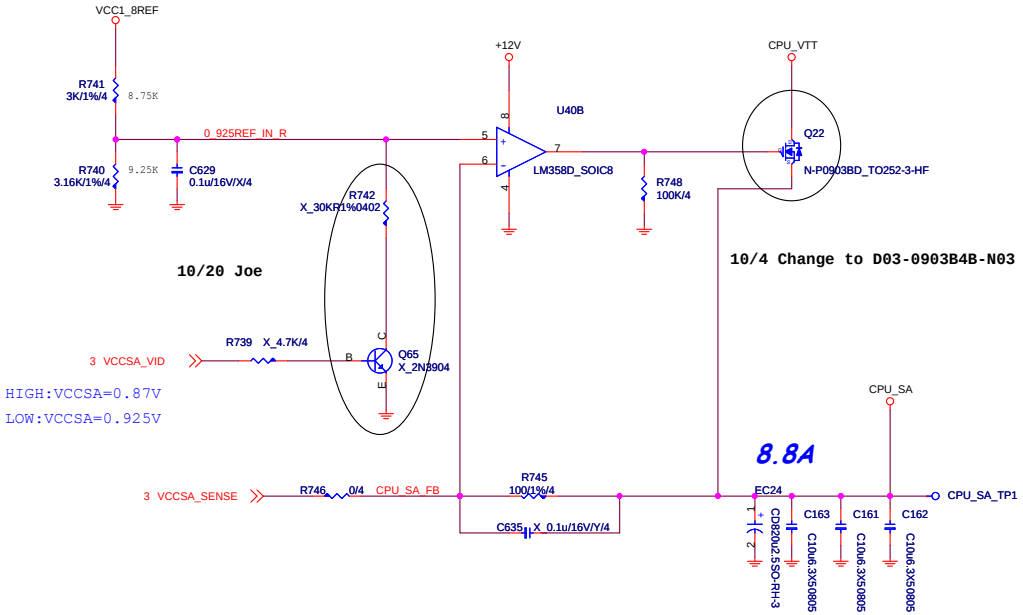
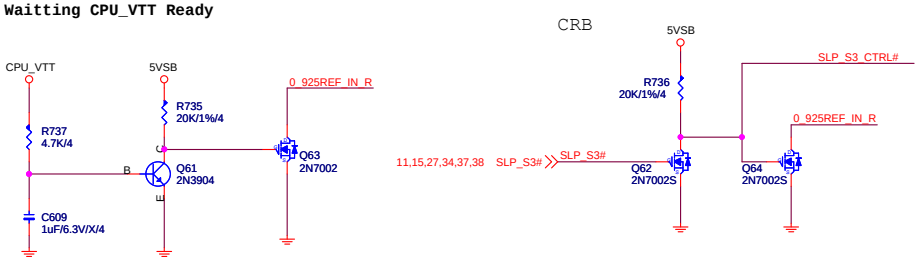


Table 3-10. VCCSA Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	1	7mΩ	1.4nH	Output	As close to RM keep-out as possible	1
10µF 0805 X5R	2	3mΩ	0.51nH	Output	Inside processor socket cavity	1, 2, 3

Waitting CPU_VTT Ready



CP Power

DDR-->PCH

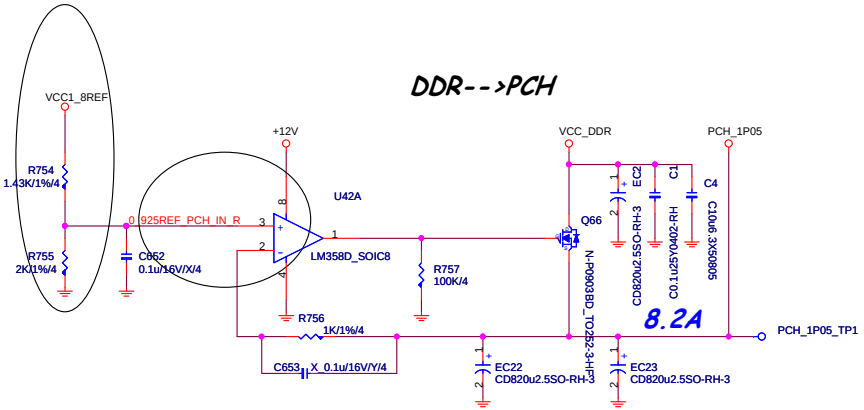
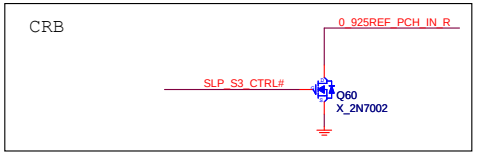


Table 4-1. V1.05A_PCH Plane Decoupling Recommendations

Bulk Decoupling Location	Qty x µF (size)	ESR, m
1.05S rail for VccCore & VccIO (dedicated)(AMT sku)	1x820uF	21mohm (bulk)
1.05A rail for VccASW (dedicated)(AMT sku)	2x22uF MLCC	
1.05S rail merge with 1.05A rail (non- AMT sku)	1X560uF 2x 22uF MLCC	7mohm (bulk)

Note: Bulk electrolytic capacitors (tantalum or aluminum based) render an aggregate ESR that matches the motherboard impedance budget. Other electrolytic capacitors that render motherboard impedance match can be deemed suitable as long as ripple current ratings and attach rate renders Bulk ESR not significantly different that those shown.



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MS-AC75	
Size: Custom	Document Description: CP /CPU_SA POWER
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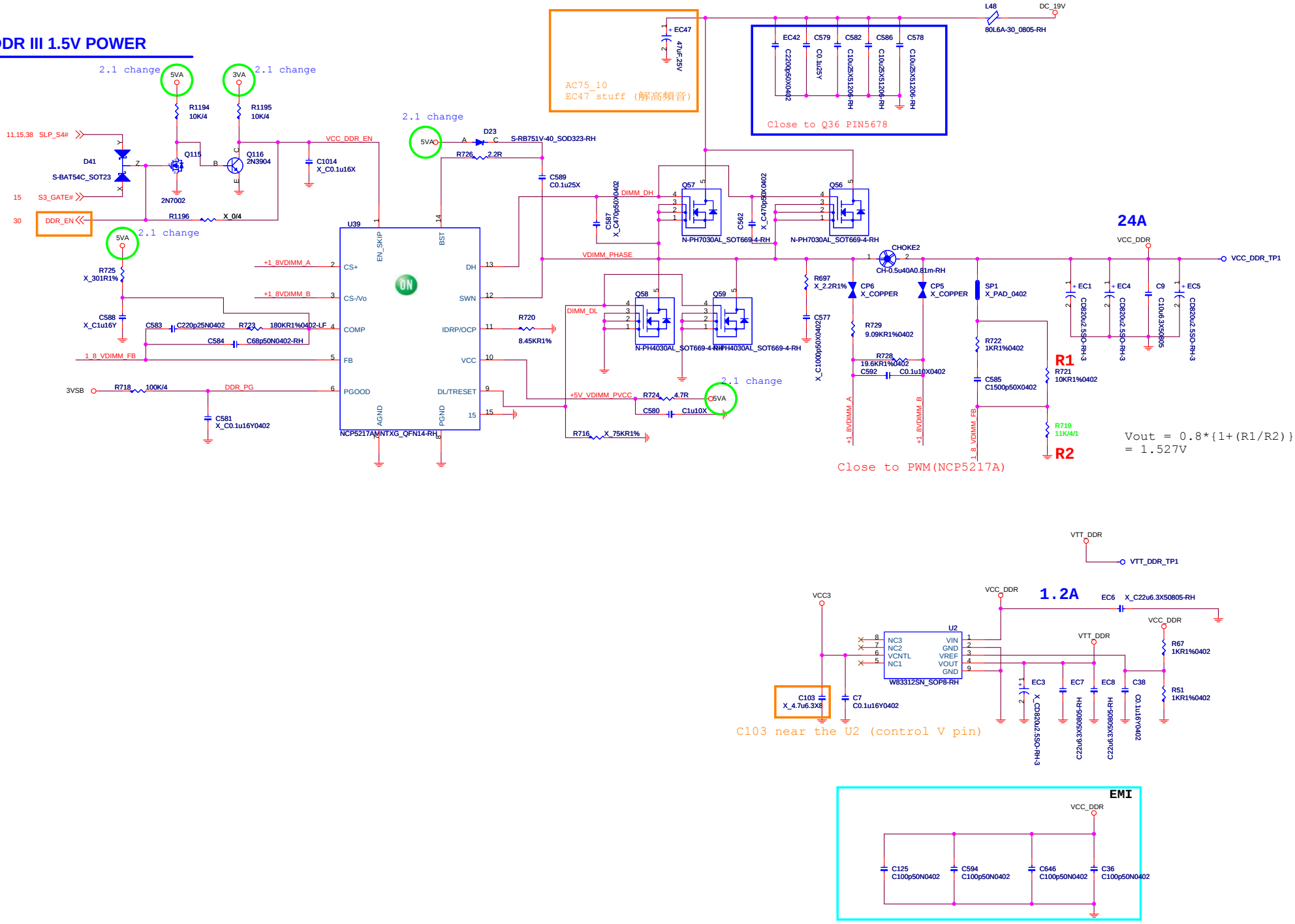
DDR III 1.5V POWER



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-AC75	
Size: Custom	Document Description: DDR POWER-NCP5217A 1-Phase	Rev: 2.1
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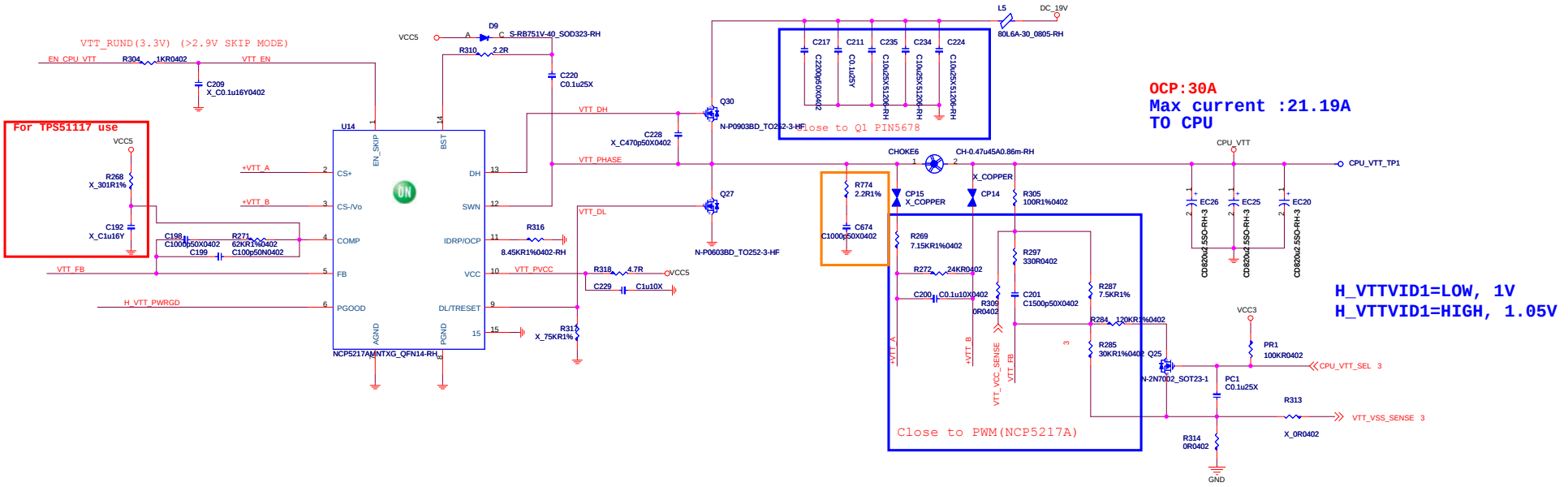

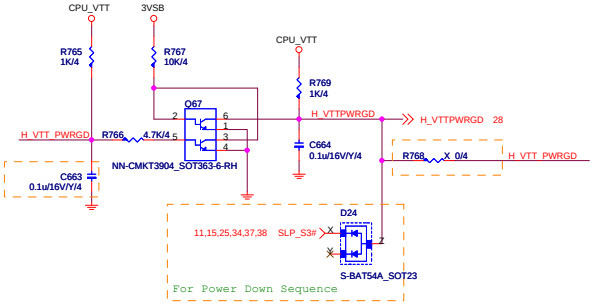

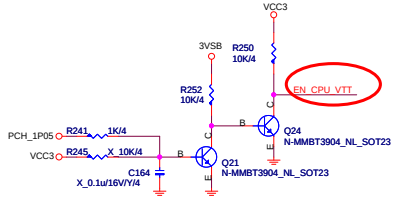

1. Rocest = Iout*DCR/Iocset ; Iocset = 10uA

If DCR = 1m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K

2. Csen = L/Rocset*DCR

If DCR = 1m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

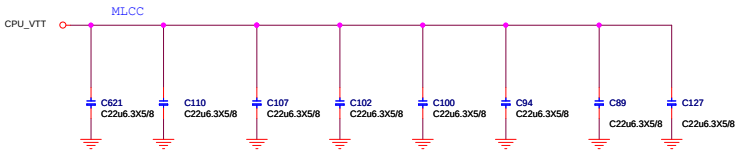

Table 3-6. VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2 3
0805 placeholders	16				Backside	

MICRO-STAR INT'L CO.,LTD		
MS-AC75		
Size: C	Document Description: CPU_VTT - ISL95870B- 1-Phase	Rev: 2.1
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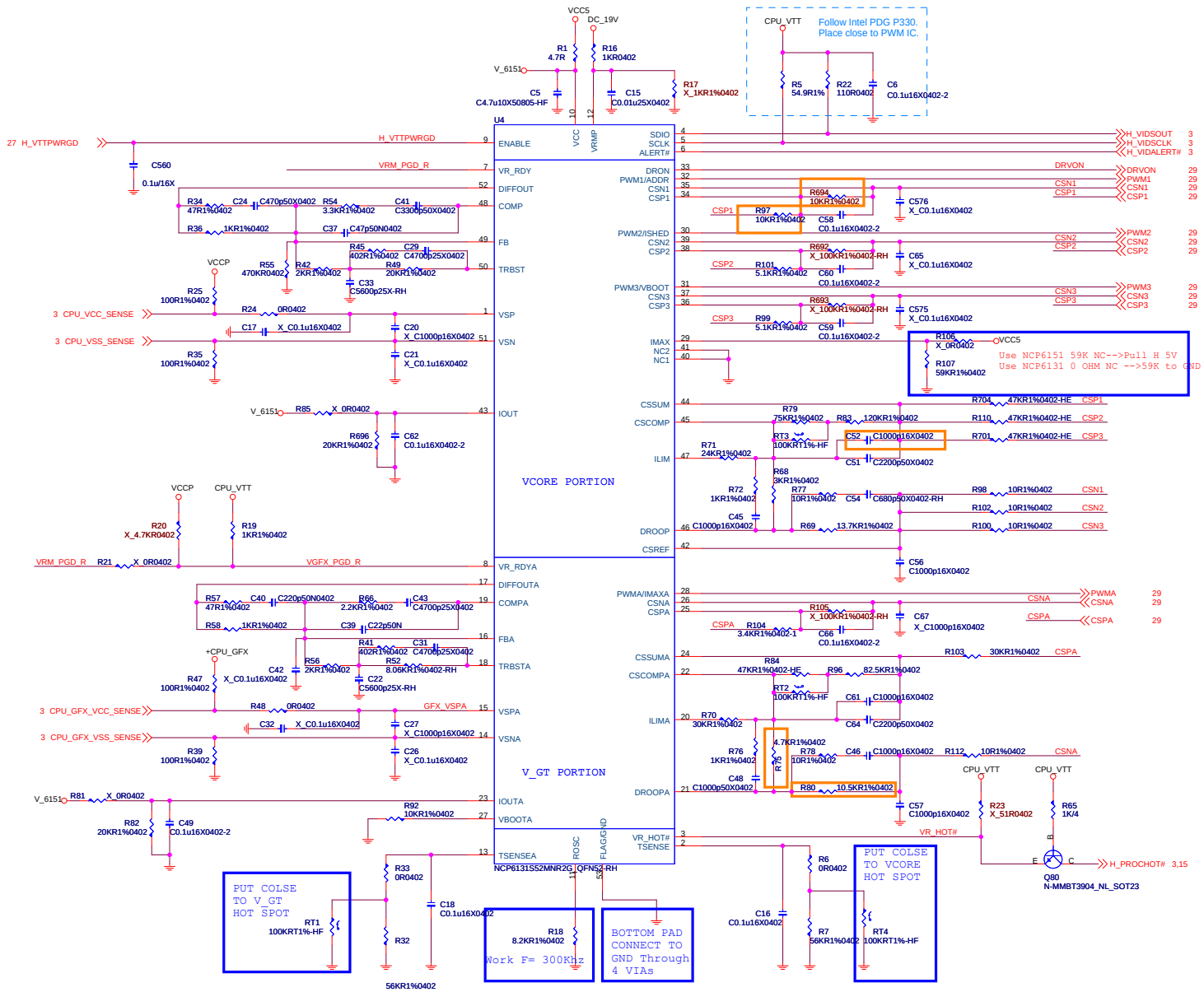
Modulize of NCP6151/NCP6131 COLAY (19V VR12)



BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V

PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

MICRO-STAR INT'L CO.,LTD

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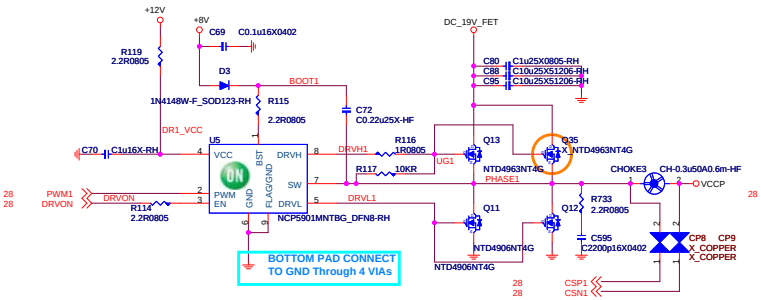
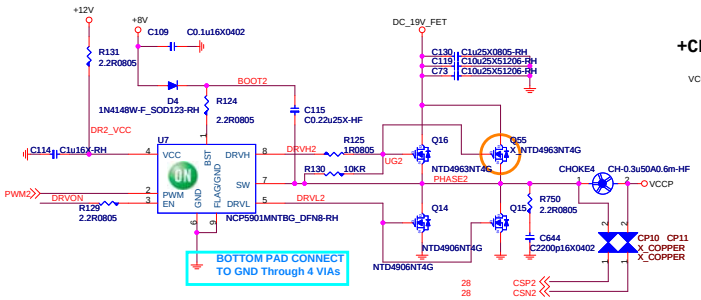
+CPU_VCCP

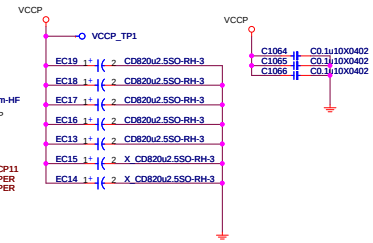
High Side D03-0480900-O05 High Side D03-0903B4B-N03
Low Side D03-0480600-O05 Low Side D03-0603B2B-N03

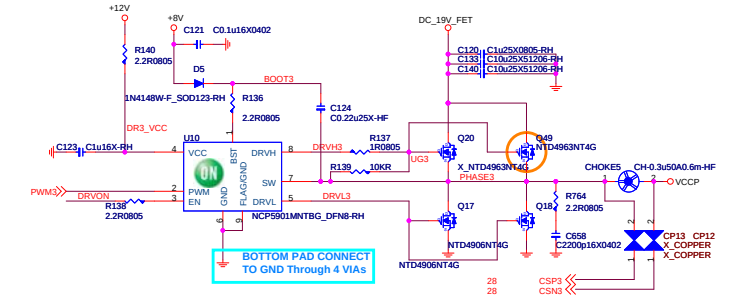
VCCP:75A



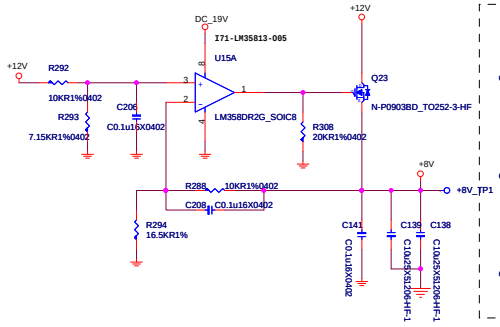


+CPU_VCCP Output Caps

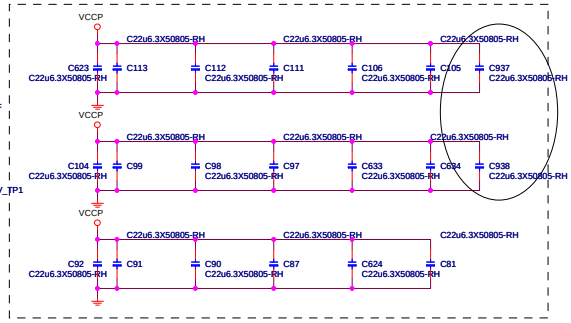




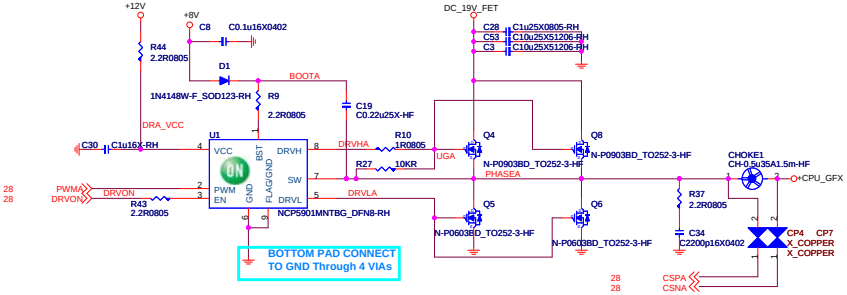
12V to 8V 0.5A



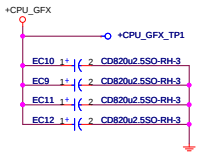
+CPU_VCCP-Decoupling



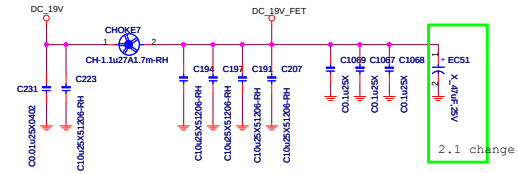
+CPU_GFX



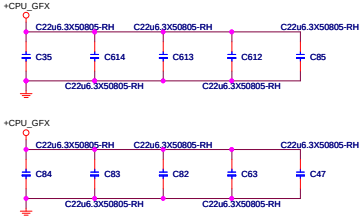
+CPU_GFX Output Caps



+CPU_GFX:35A



+CPU_GFX Decoupling



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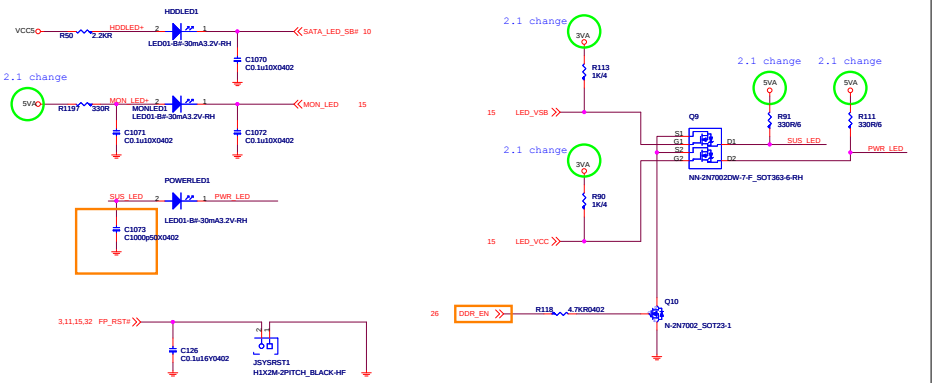
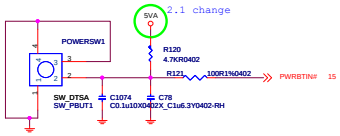
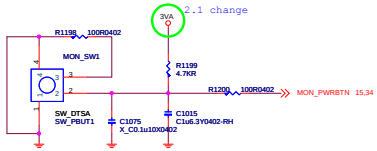


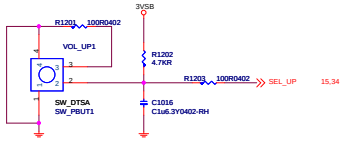
POWER ON/OFF BUTTON

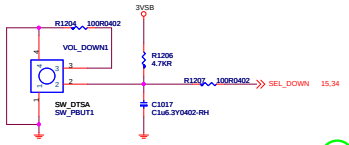


MONITOR ON/OFF BUTTON

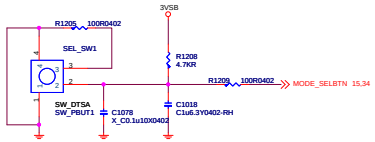


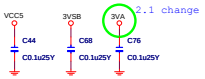
MODE SELECT CONTROL

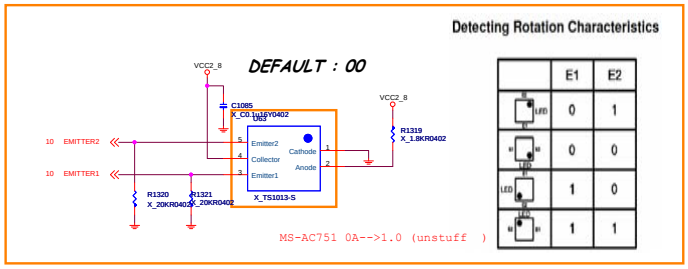


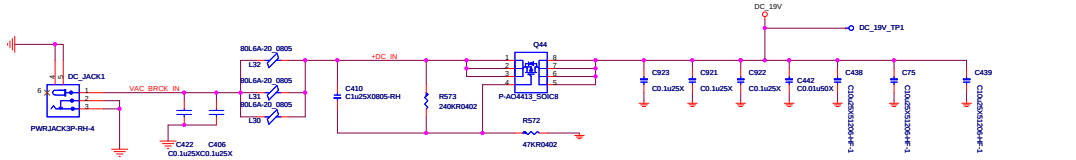


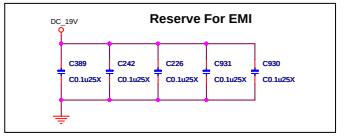
MODE SELECT BUTTON



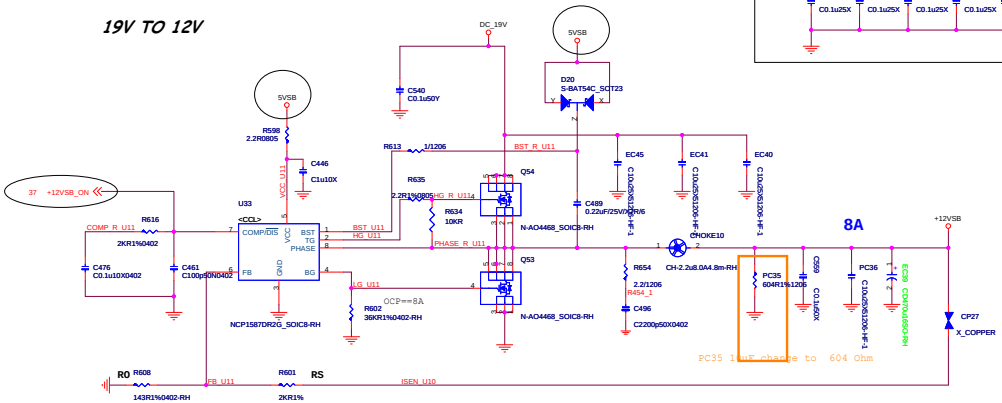








19V TO 12V



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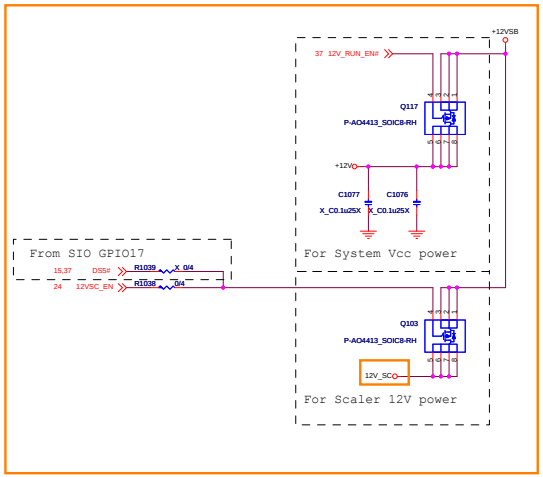
PHASE_R_U11
LG_U11



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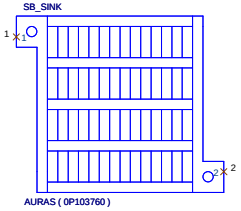
SB_SINK
footprint:HS_37_8X37_8

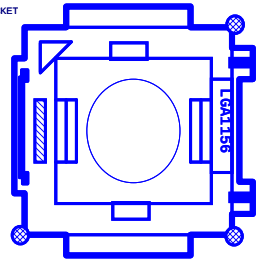
SB_SINK



AURAS (0P103760)

CPU SOCKET

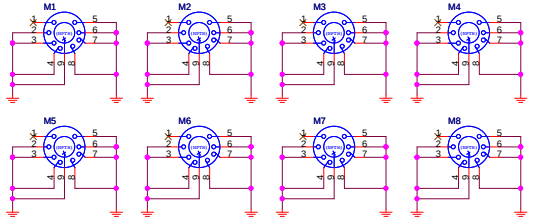
CPU1_X1
CPU SOCKET



MSI P/N E21-AC71010-L06

PCB1 DEL FOR PRE-BOM

Mounting Holes

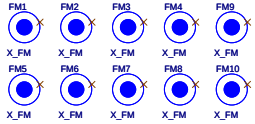


BAT1
BAT-BT-CR2032-RH

CPU_backplate

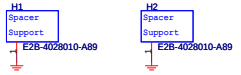
AC71 CPU_backplate

Optical Fiducial Marks-120

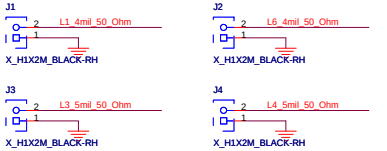


VRM SINK

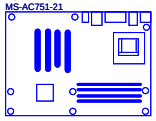
PWM MOSFET heat-pipe stand off.



Single End 50ohm



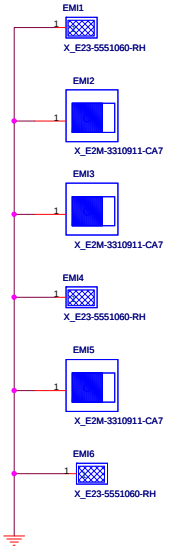
PCB1
MS-AC751-21



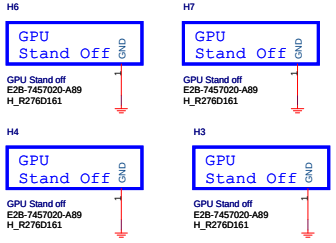
BIOS label

LABEL1

1.0 12/01



GPU Stand off



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Size: Custom	Document Number: MS-AC75	Rev: 2.1
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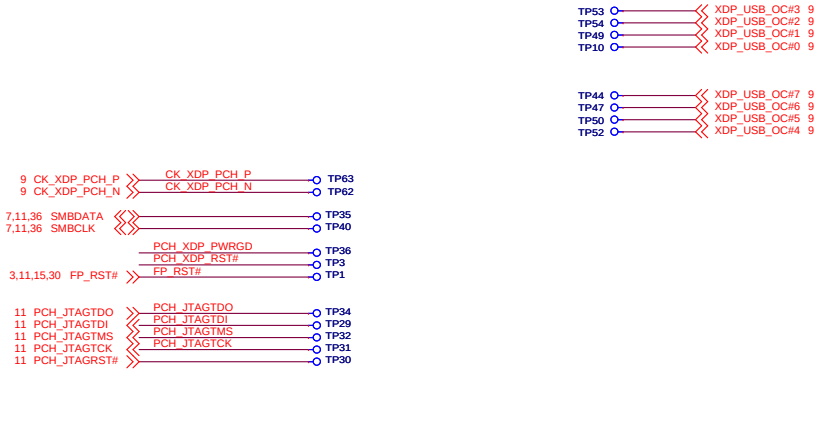
Reserve debug port 5020

PCH XDP



PCH XDP PWRGD/RESET

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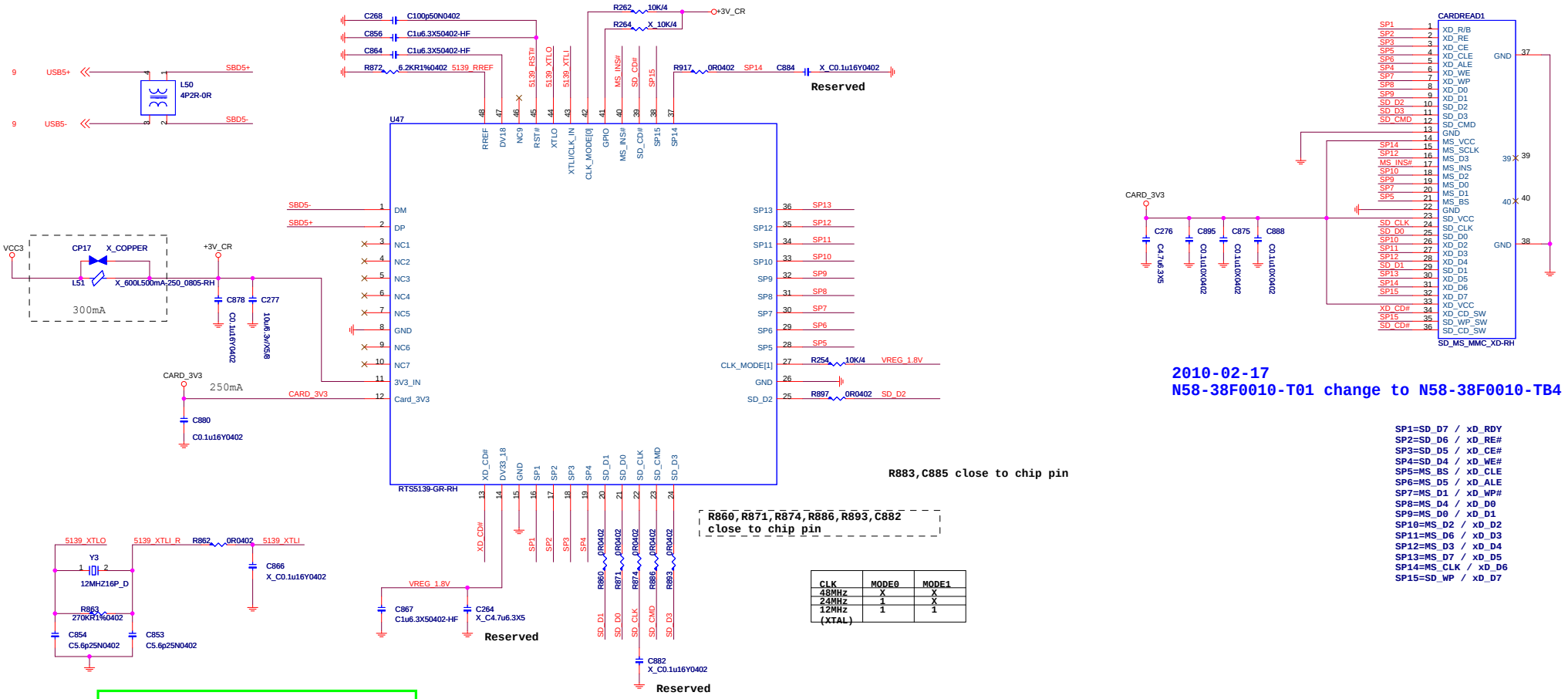
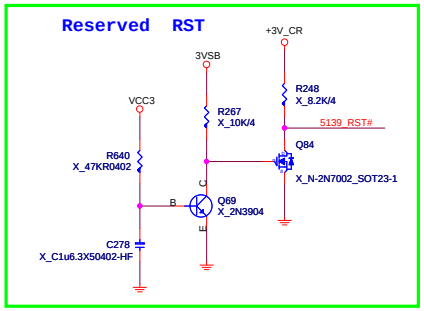


2010-02-17
N58-38F0010-T01 change to N58-38F0010-TB4

SP1=SD_D7 / xD_RDY
SP2=SD_D6 / xD_RE#
SP3=SD_D5 / xD_CE#
SP4=SD_D4 / xD_WE#
SP5=MS_BS / xD_CLE
SP6=MS_D5 / xD_ALE
SP7=MS_D1 / xD_WP#
SP8=MS_D4 / xD_D0
SP9=MS_D0 / xD_D1
SP10=MS_D2 / xD_D2
SP11=MS_D6 / xD_D3
SP12=MS_D3 / xD_D4
SP13=MS_D7 / xD_D5
SP14=MS_CLK / xD_D6
SP15=SD_WP / xD_D7

Reserved RST



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2010-02-17
B07-2482D14-R09 change to B07-2482D04-R09

AMP Volume Controlled by Scaler.DavidZ.

Change net name from SC_HDMI0_HPDET to SC_HDMI1_HPDET. DavidZ

Change net name from TMDS1_HPD to TMDS0_HPD. DavidZ

2.1 change

Change this circuit from pin 64 to pin63. Miya

B07-2482D04-R09

RTD2482D-GR-RH

HDMI IN (HDMI CON)

MS-AC751 0A-->1.0 (Synergy BOM)

IGP stuff 680 ohm

GPU stuff 499 ohm

Add SYS ID pin for System selection. DavidZ.

NO_STUFF

1M(1Mx1bit) SPI ROM

M31-25L1002-M24

M33-24C16D3-S10

2382D=1.2V
130mA

2.0 Modify

UP7707 Spec 600mA

LVDS

PANEL SELECT

	SYS_ID0	SYS_ID1	SYS_ID2	
Samsung	0	0	0	
Chimei	0	0	1	AC77
CPT	0	1	0	
AA59	0	1	1	
X	1	0	0	
X	1	0	1	
X	1	1	0	
X	1	1	1	

AC751 21 ------> AA59
AC751 21 OPT: A ------> AC77
AC751 21 OPT: B ------> AA59 2G
AC751 21 OPT: C ------> AC77 2G

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Size: Custom	Document Description: SCALER(MAIN)
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MICRO-STAR INT'L CO.,LTD	
MS-AC75	
Size: A	Document Description: Reserved
Rev: 2.1	
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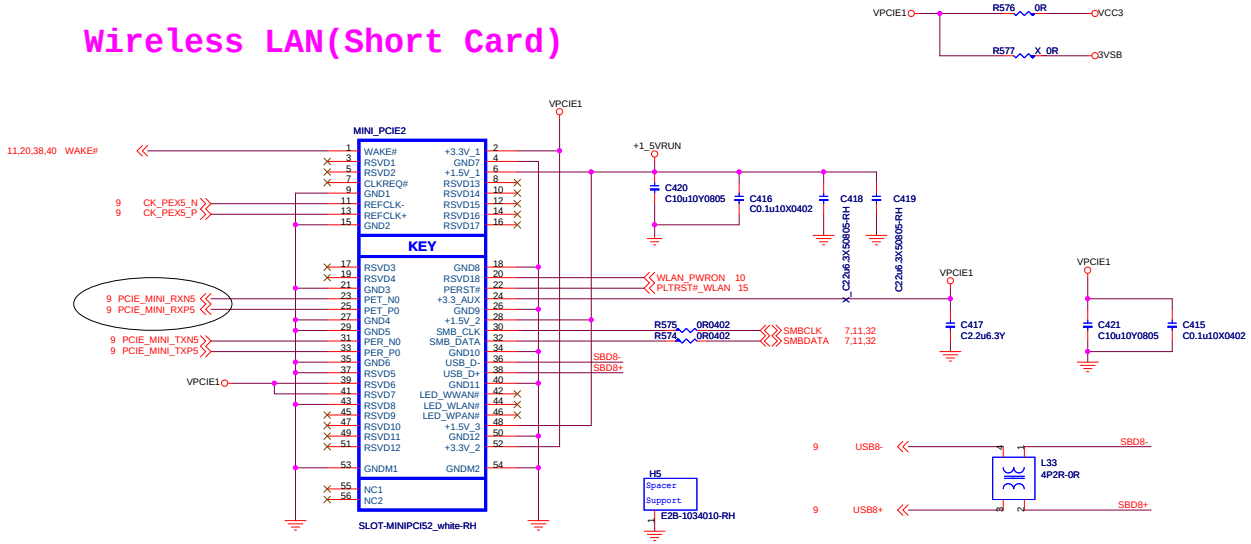
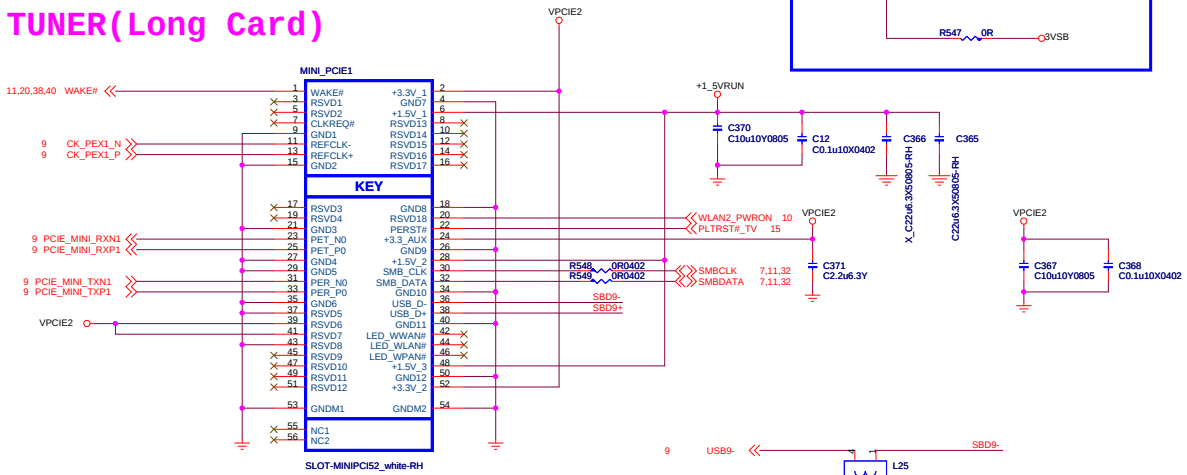
Wireless LAN(Short Card)



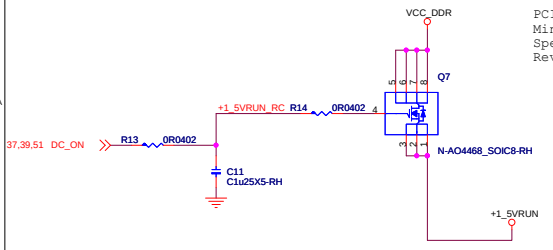
Power change to Normal 3/5

TV TUNER(Long Card)



N11-0520040-A81

PCI ExpressR
Mini Card Electromechanical
Specification
Revision 1.2



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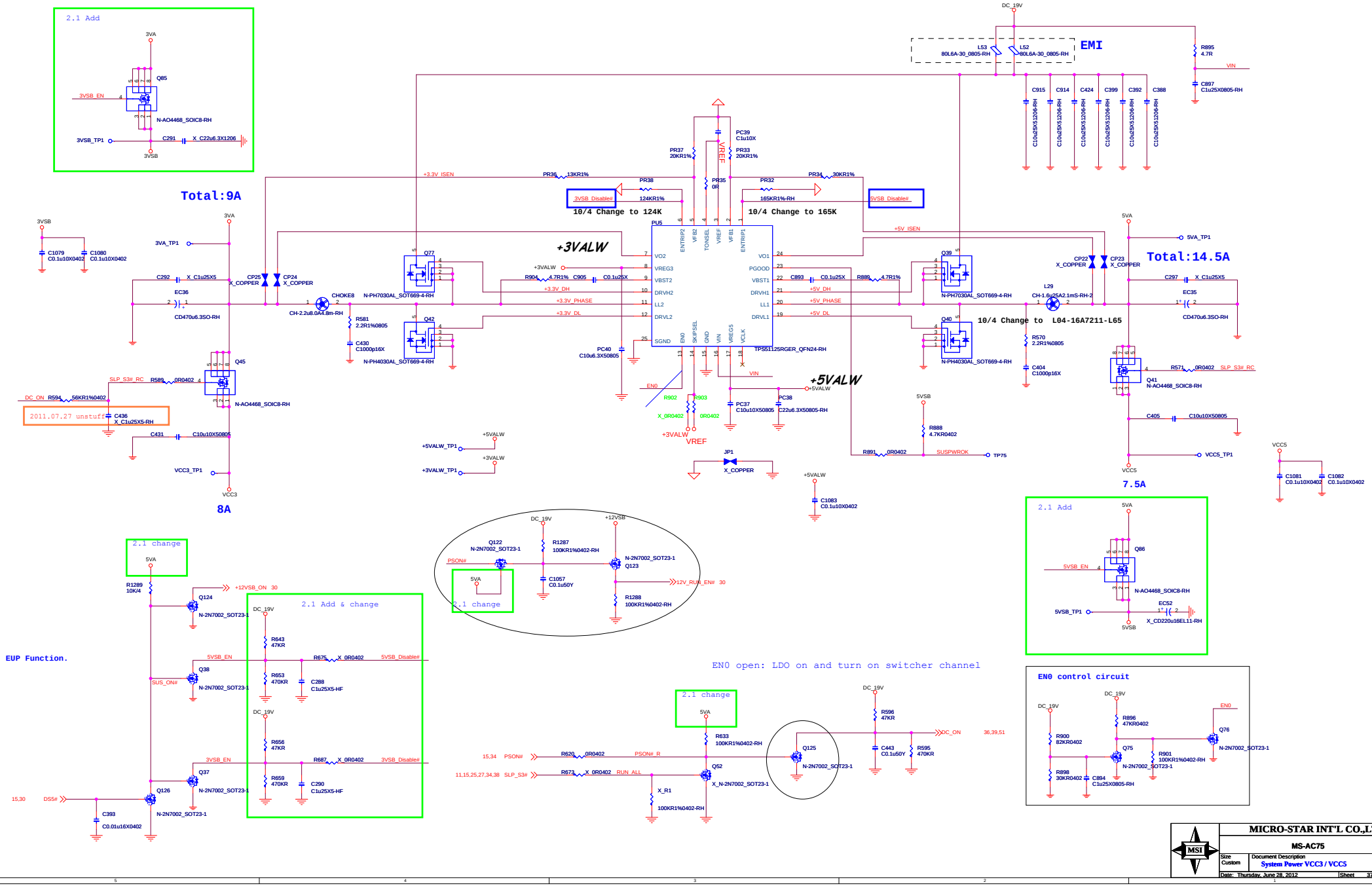
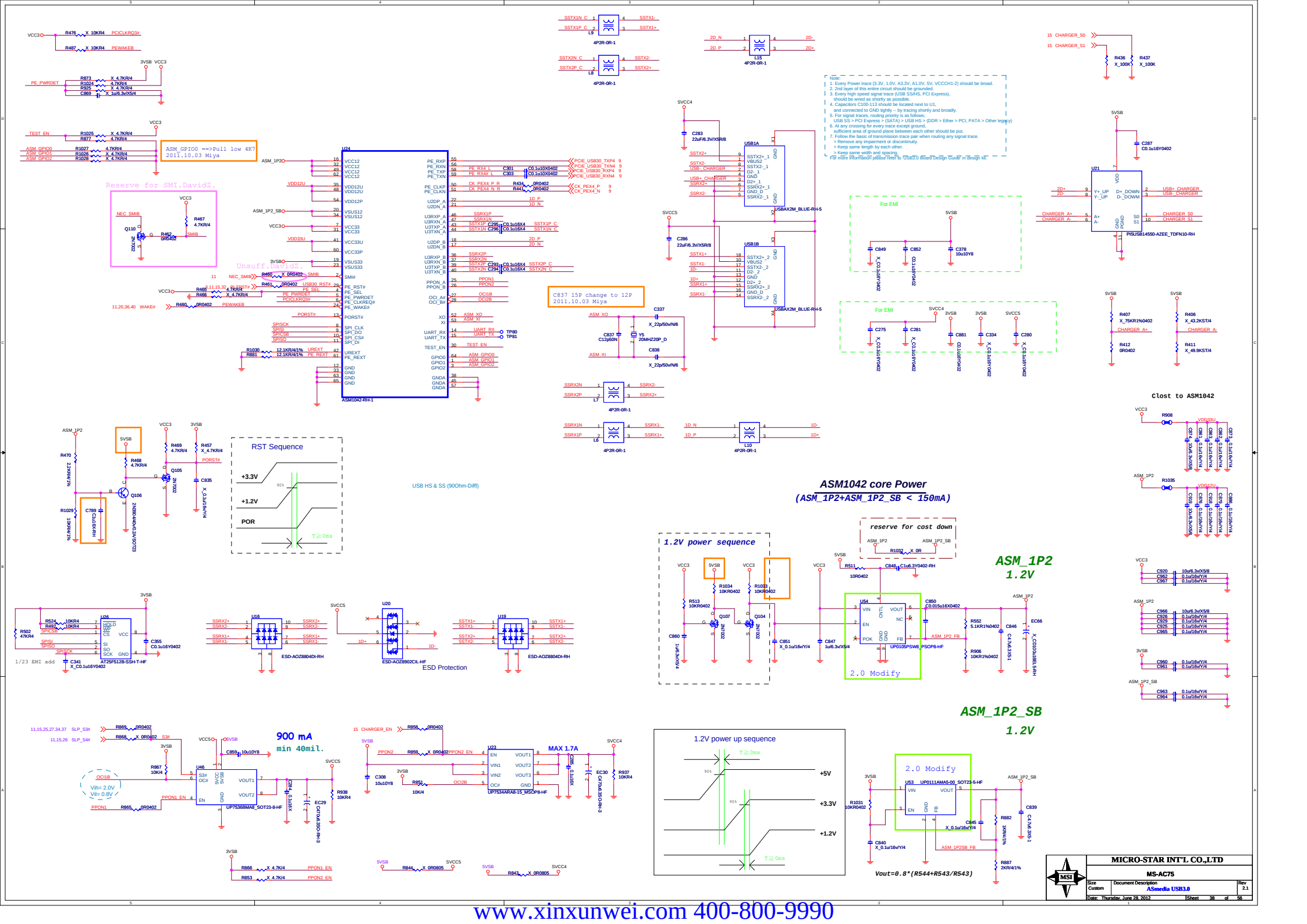
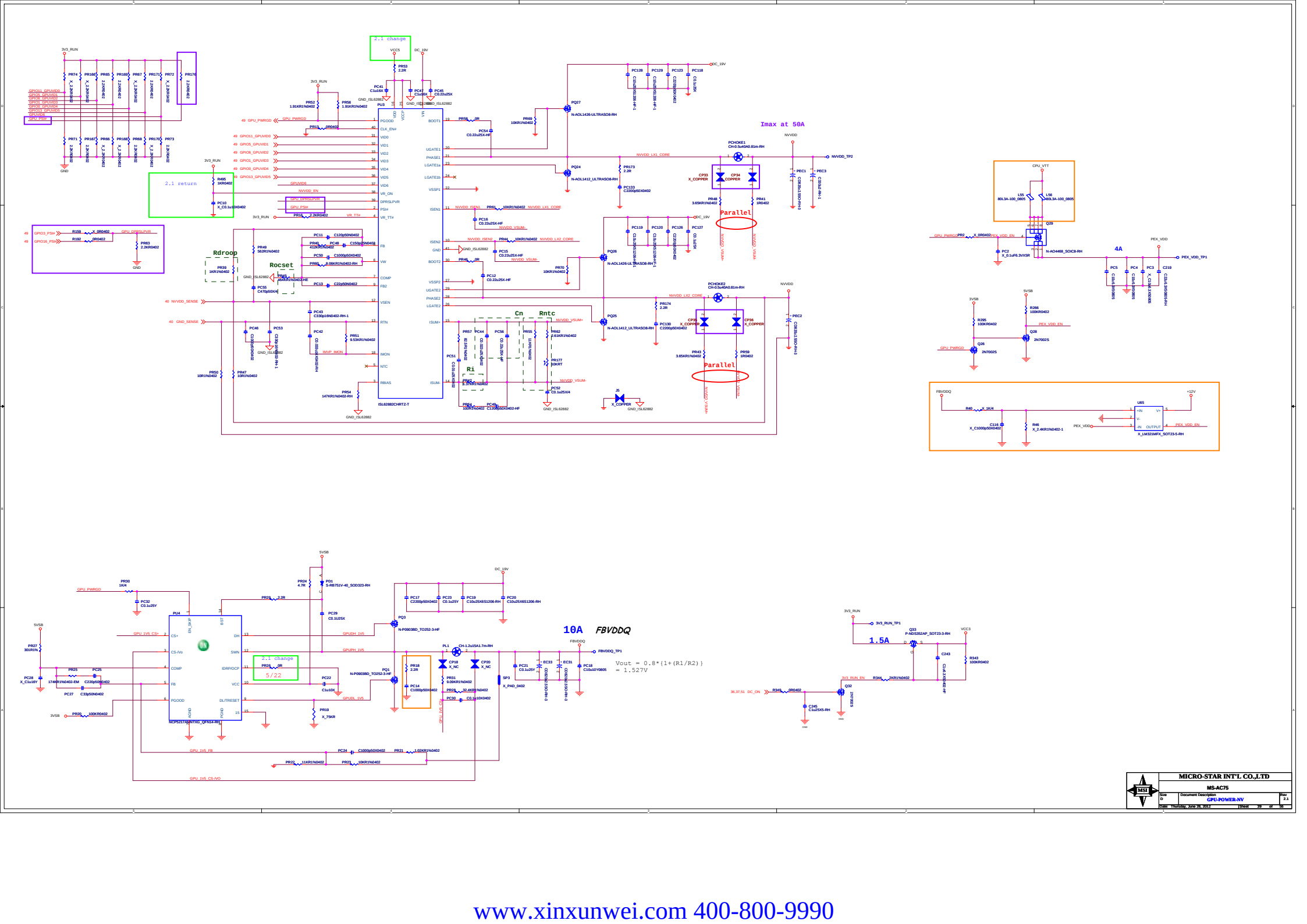
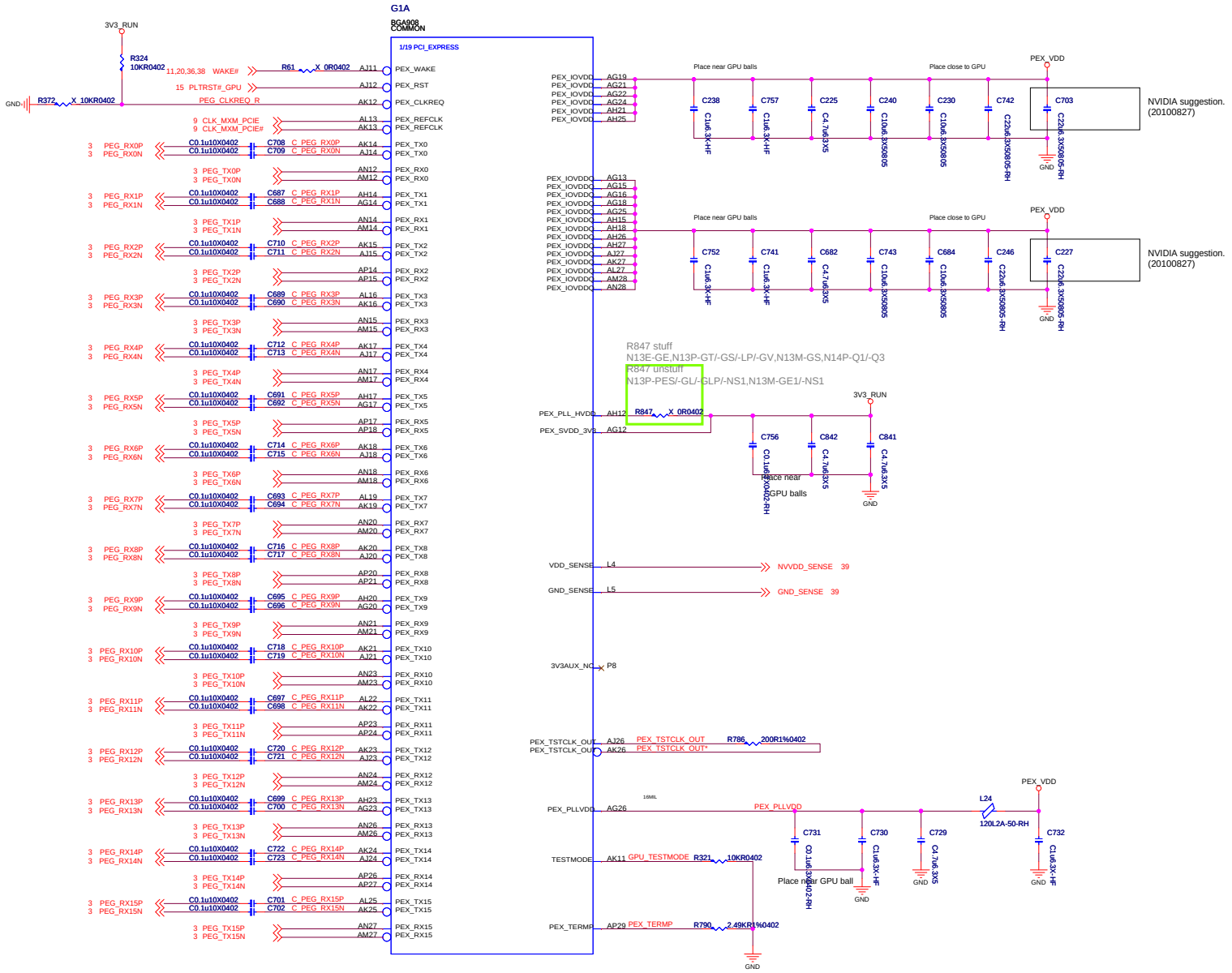
	MS-AC75	
Size: Custom	Document Description: MINI PCIE Slot	Rev: 2.1
Date: Tuesday, June 26, 2012	Sheet 36 of 56	



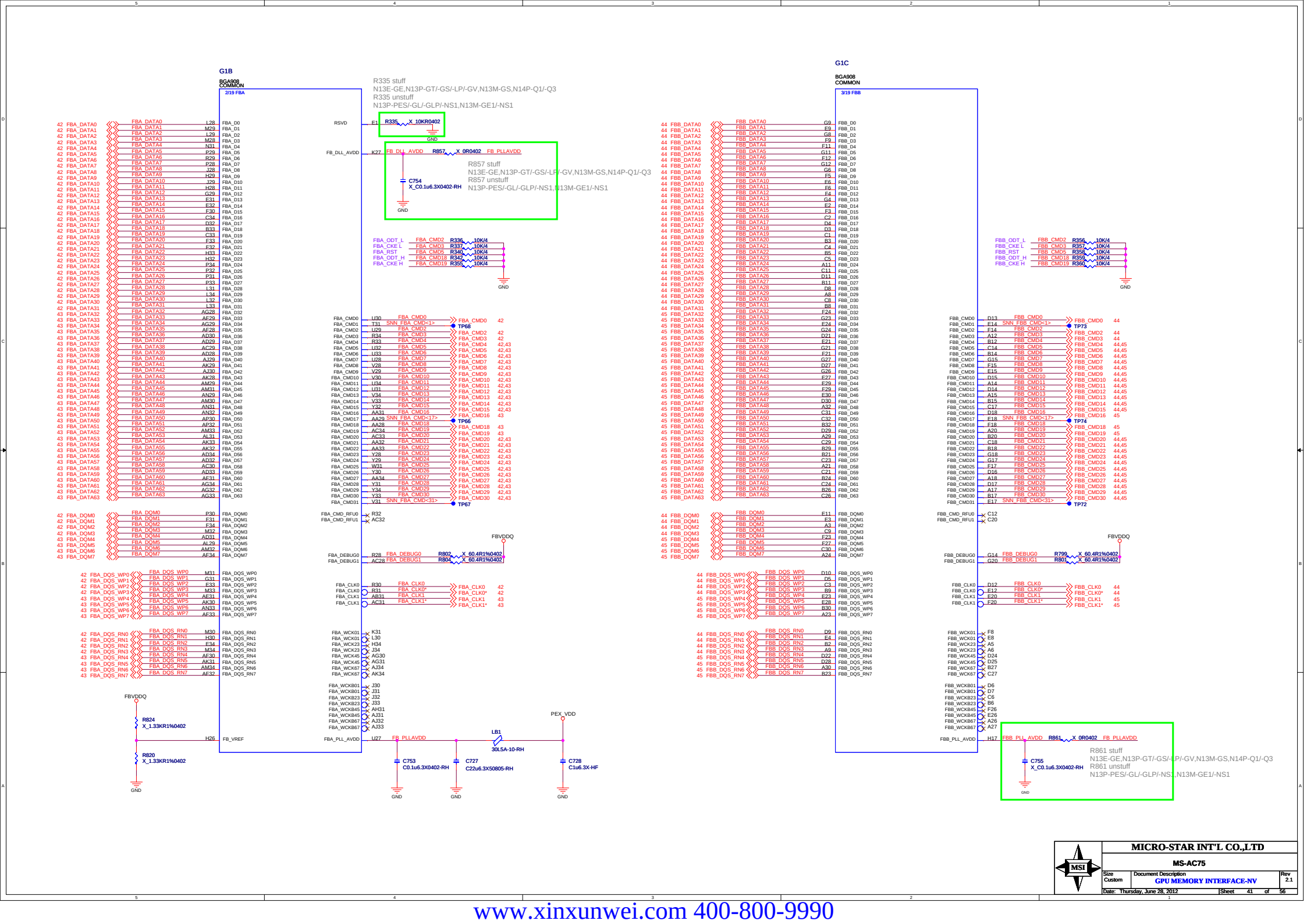


MICRO-STAR INT'L CO.,LTD	
MS-AC75	
Size: Custom	Document Description: ASmedia USB3.0
Rev: 2.1	
Date: Thursday, June 28, 2012	Sheet 38 of 56

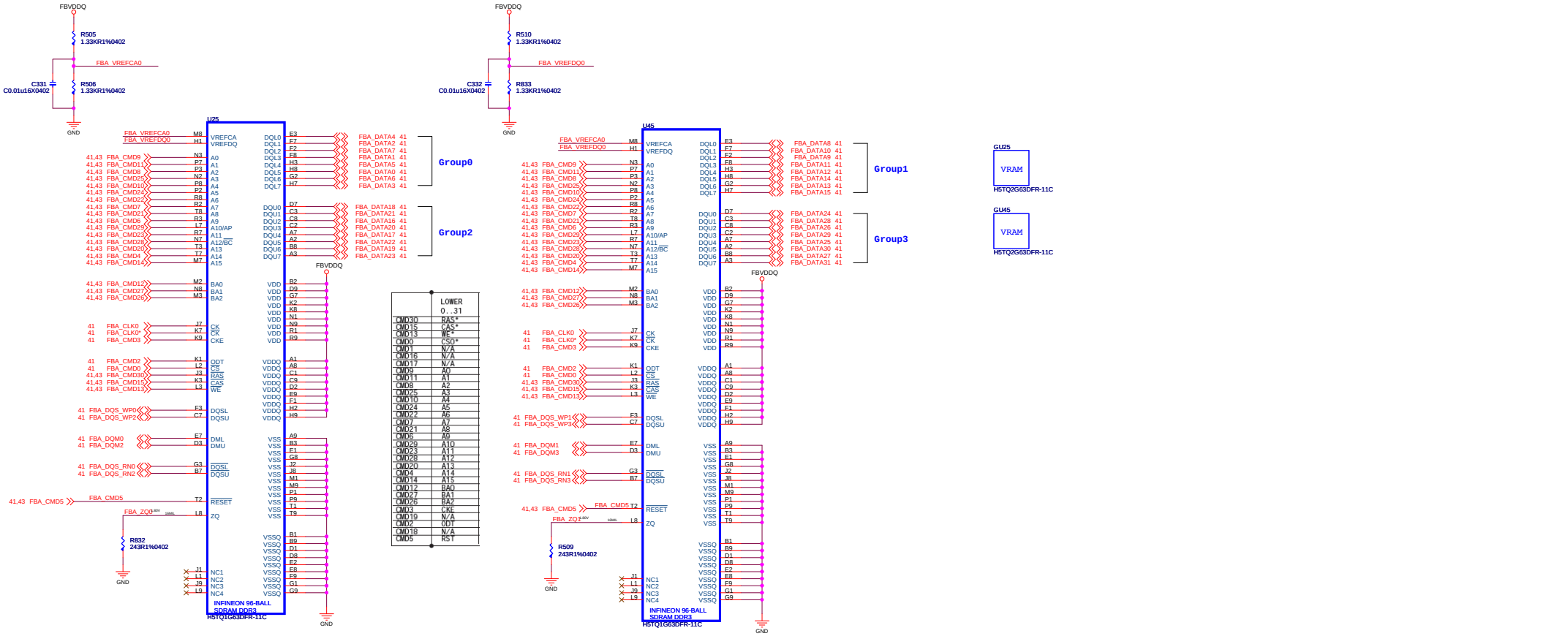




MSI	MICRO-STAR INT'L CO.,LTD	
	MS-AC75	
Size: C	Document Description: PCI EXPRESS INTERFACE-NV	Rev: 2.1
Date: Thursday, June 28, 2012	Sheet 40 of 56	



4. MEMORY PARTITION A LOWER 32 BITS



MEMORY PARTITION A SIGNAL CONSTRAINTS

FBA_CLK0	FBA_CLK0	1	BIDIFF
FBA_CLK0*	FBA_CLK0	1	BIDIFF
FBA_DQS_WP0	FBADQS0	1	BIDIFF
FBA_DQS_RN0	FBADQS0	1	BIDIFF
FBA_DQS_WP1	FBADQS1	1	BIDIFF
FBA_DQS_RN1	FBADQS1	1	BIDIFF
FBA_DQS_WP2	FBADQS2	1	BIDIFF
FBA_DQS_RN2	FBADQS2	1	BIDIFF
FBA_DQS_WP3	FBADQS3	1	BIDIFF
FBA_DQS_RN3	FBADQS3	1	BIDIFF

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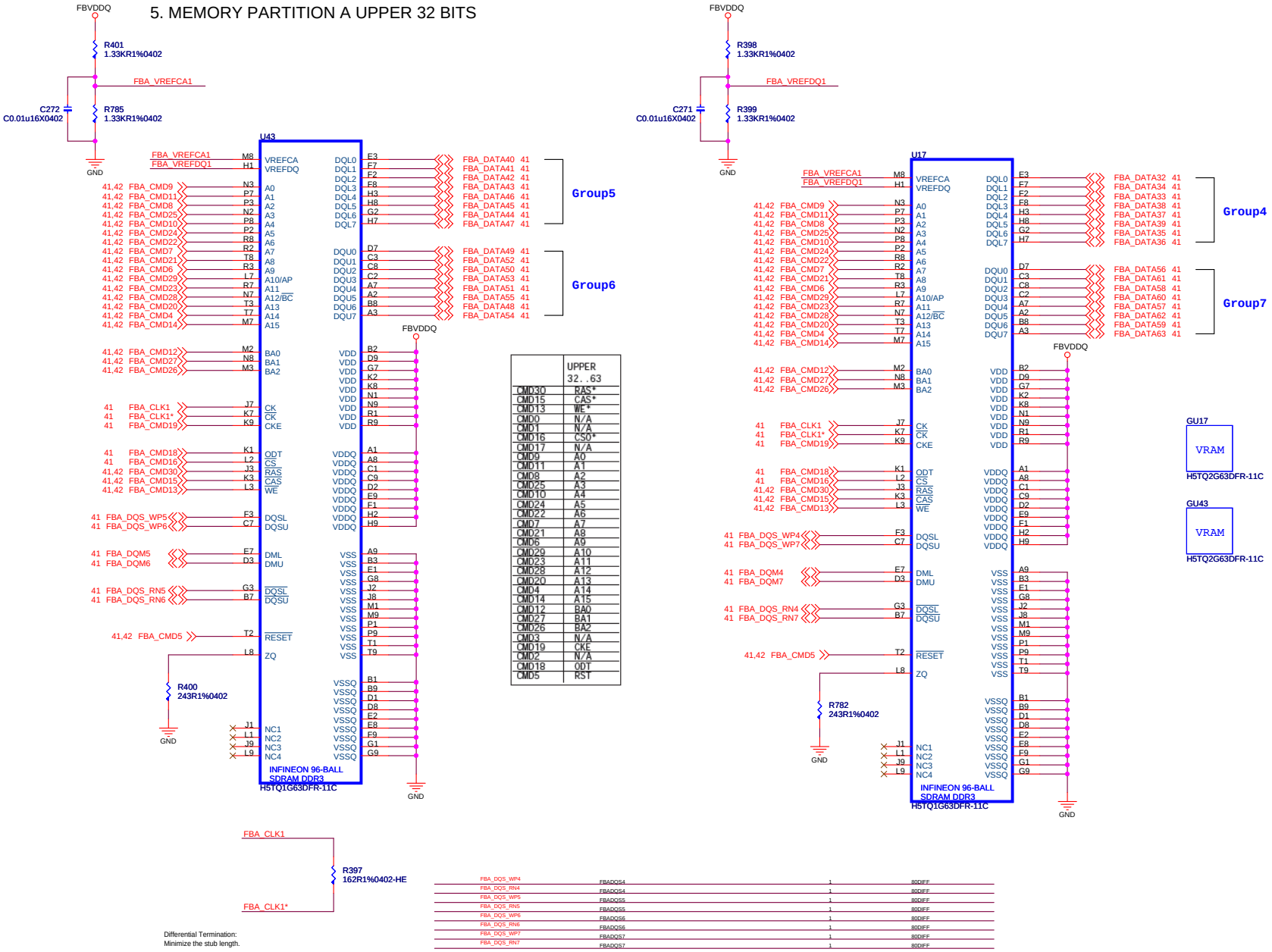
5. MEMORY PARTITION A UPPER 32 BITS



	UPPER 32..63
CMD30	RAS*
CMD15	CAS*
CMD13	WE*
CMD0	N/A
CMD1	N/A
CMD16	CS0*
CMD17	N/A
CMD9	A0
CMD11	A1
CMD8	A2
CMD25	A3
CMD10	A4
CMD24	A5
CMD22	A6
CMD7	A7
CMD21	A8
CMD6	A9
CMD29	A10
CMD23	A11
CMD28	A12
CMD20	A13
CMD4	A14
CMD14	A15
CMD12	BA0
CMD27	BA1
CMD26	BA2
CMD3	N/A
CMD19	CKE
CMD2	N/A
CMD18	ODT
CMD5	RST

FBA_DQS_WP4	FBADQS4	1	80DIFF
FBA_DQS_RN4	FBADQS4	1	80DIFF
FBA_DQS_WP5	FBADQS5	1	80DIFF
FBA_DQS_RN5	FBADQS5	1	80DIFF
FBA_DQS_WP6	FBADQS6	1	80DIFF
FBA_DQS_RN6	FBADQS6	1	80DIFF
FBA_DQS_WP7	FBADQS7	1	80DIFF
FBA_DQS_RN7	FBADQS7	1	80DIFF

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Custom	VRAM-A_UPPER	2.1

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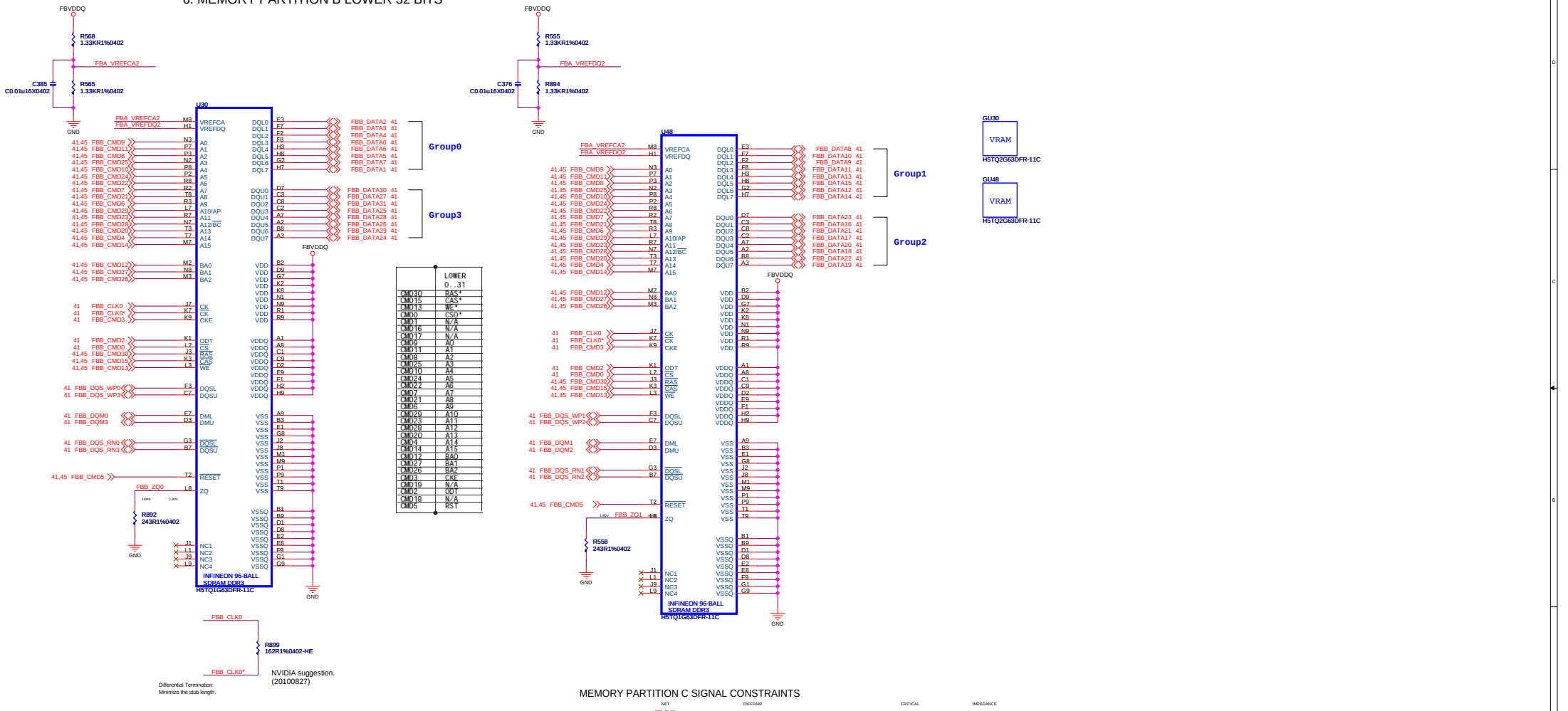
6. MEMORY PARTITION B LOWER 32 BITS



MEMORY PARTITION C SIGNAL CONSTRAINTS

NET	DIFFPAIR	CRITICAL	IMPEDANCE
FBB_CLK0	FBB_CLK0	1	80OHM
FBB_CLK0*	FBB_CLK0	1	80OHM
FBB_DQS_WP0	FBBDQS0	1	80OHM
FBB_DQS_RN0	FBBDQS0	1	80OHM
FBB_DQS_WP1	FBBDQS1	1	80OHM
FBB_DQS_RN1	FBBDQS1	1	80OHM
FBB_DQS_WP2	FBBDQS2	1	80OHM
FBB_DQS_RN2	FBBDQS2	1	80OHM
FBB_DQS_WP3	FBBDQS3	1	80OHM
FBB_DQS_RN3	FBBDQS3	1	80OHM

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Custom	VRAM-B_LOWER	2.1

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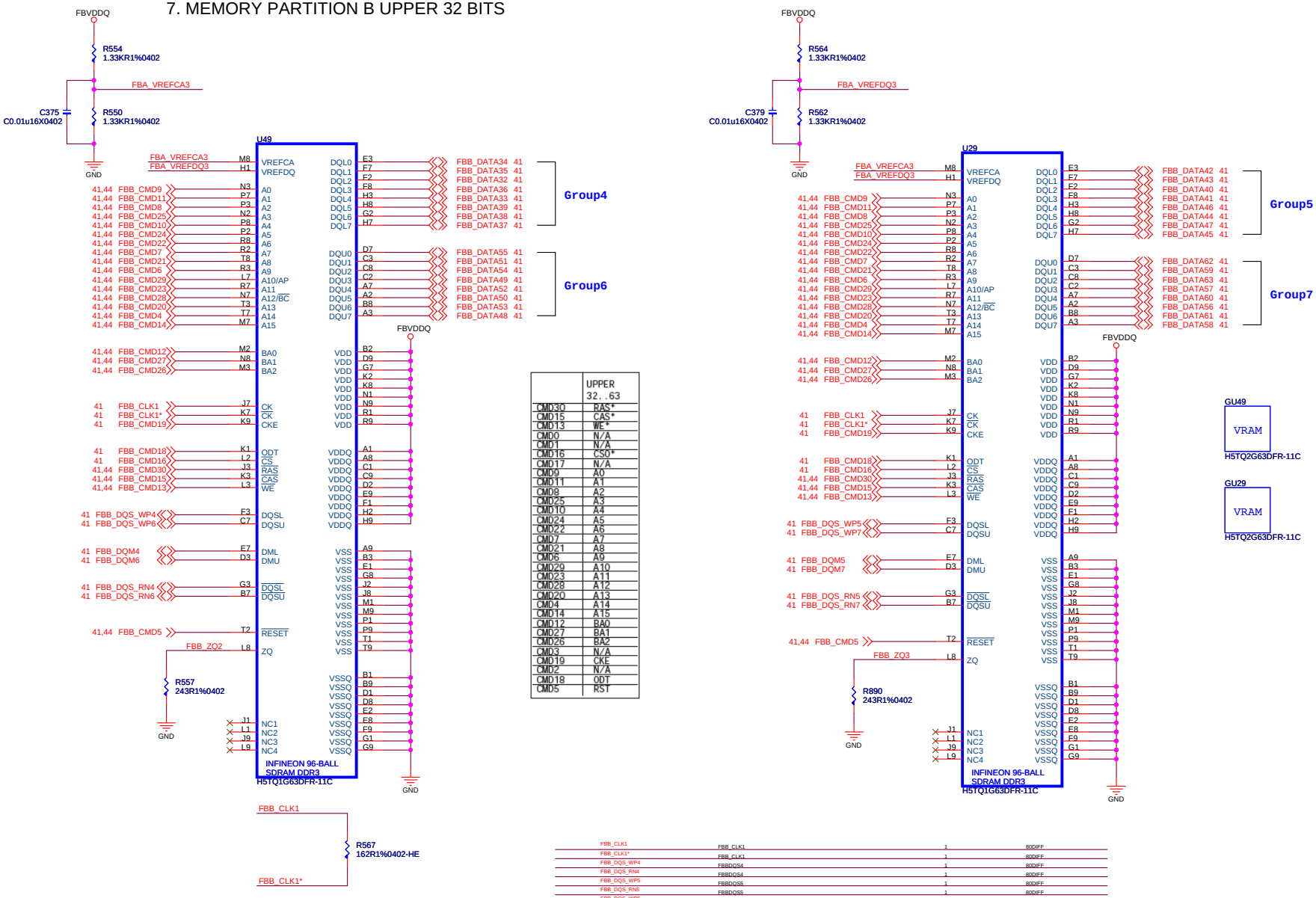
7. MEMORY PARTITION B UPPER 32 BITS



FBB_CLK1	FBB_CLK1	1	80DIFF
FBB_CLK1*	FBB_CLK1	1	80DIFF
FBB_DQS_WP4	FBBDQS4	1	80DIFF
FBB_DQS_RN4	FBBDQS4	1	80DIFF
FBB_DQS_WP5	FBBDQS5	1	80DIFF
FBB_DQS_RN5	FBBDQS5	1	80DIFF
FBB_DQS_WP6	FBBDQS6	1	80DIFF
FBB_DQS_RN6	FBBDQS6	1	80DIFF
FBB_DQS_WP7	FBBDQS7	1	80DIFF
FBB_DQS_RN7	FBBDQS7	1	80DIFF

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Custom	VRAM-A_UPPER	2.1

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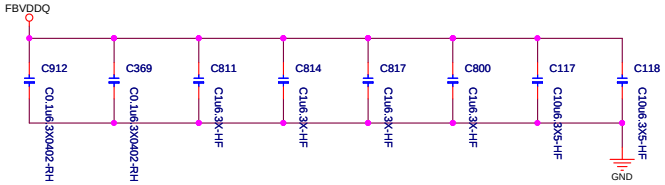
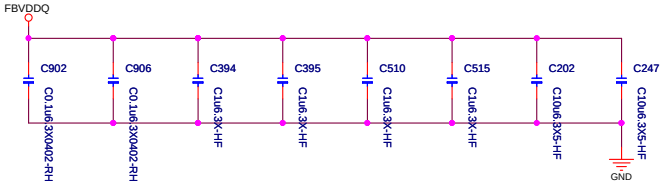
8. MEMORY DECOUPLING CAPS

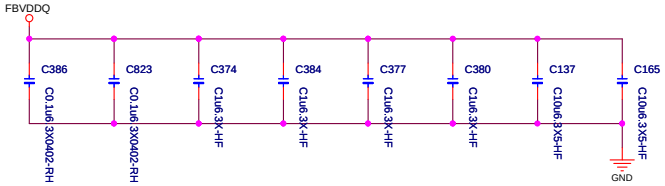
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 0-15



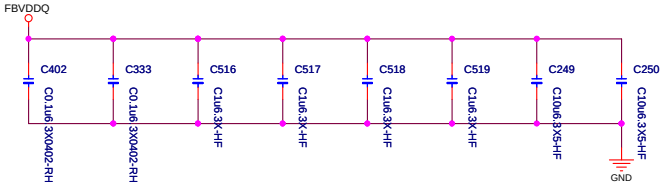
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B LOWER BITS 0-15



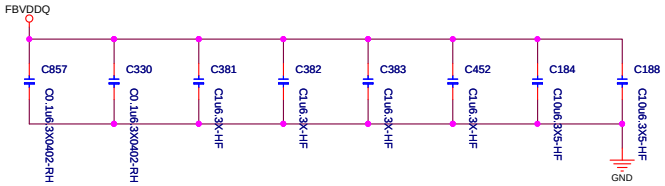
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 16-31



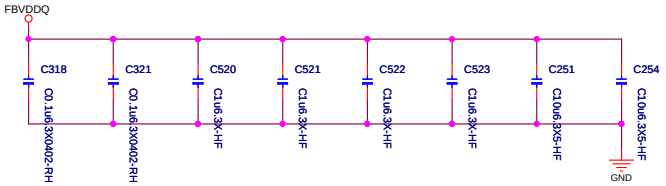
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B LOWER BITS 16-31



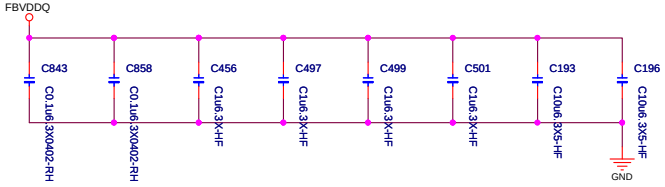
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 32-47



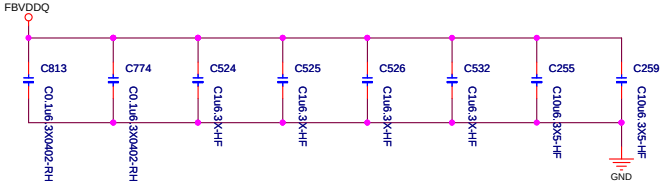
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B UPPER BITS 32-47



DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 48-63



DECOUPLING CAPS FOR ONE MEMORY OF PARTION C UPPER BITS 48-63



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-AC75	
Size: Custom	Document Description: MEMORY DECOUPLING CAPS-NV	Rev: 2.1
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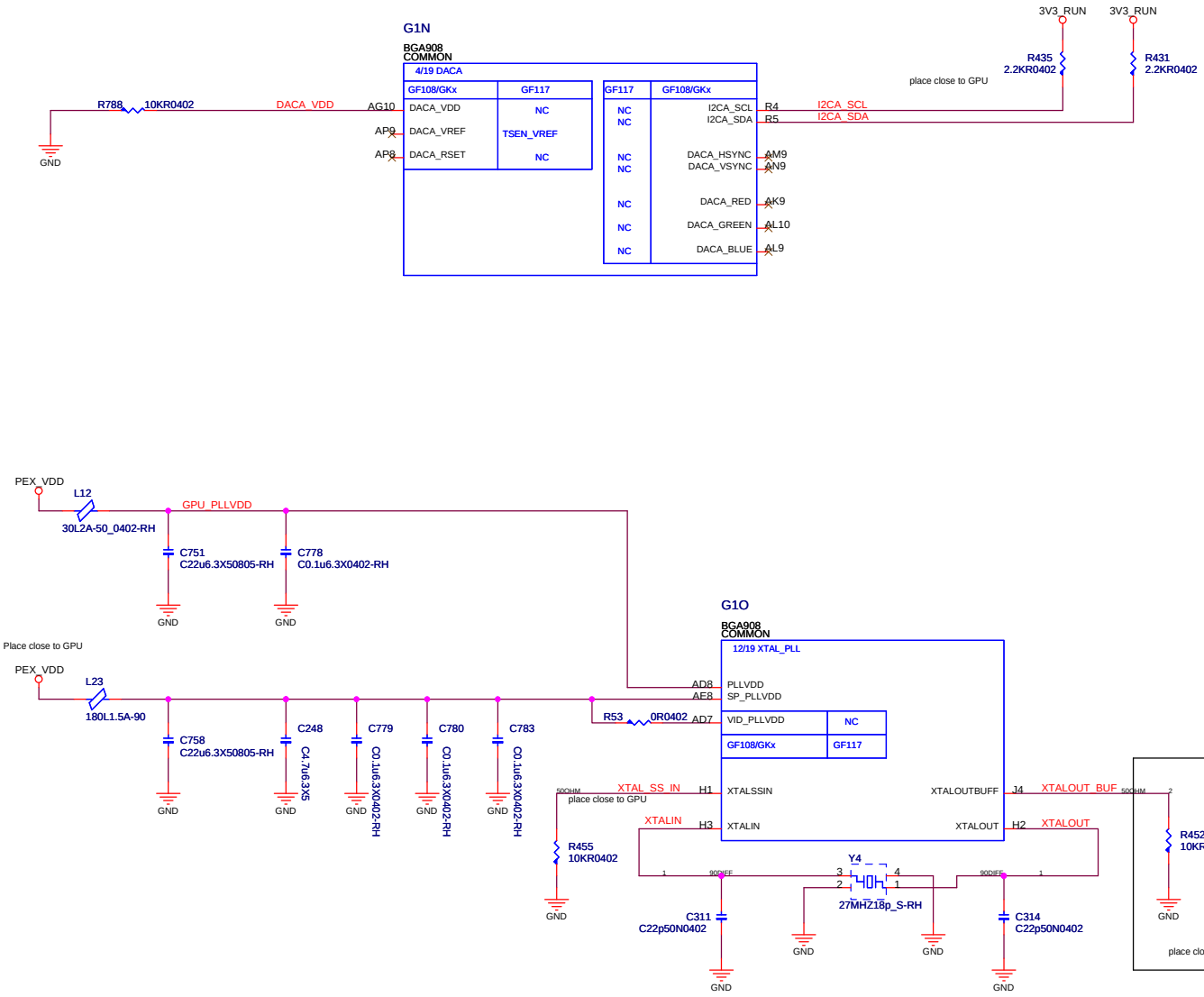
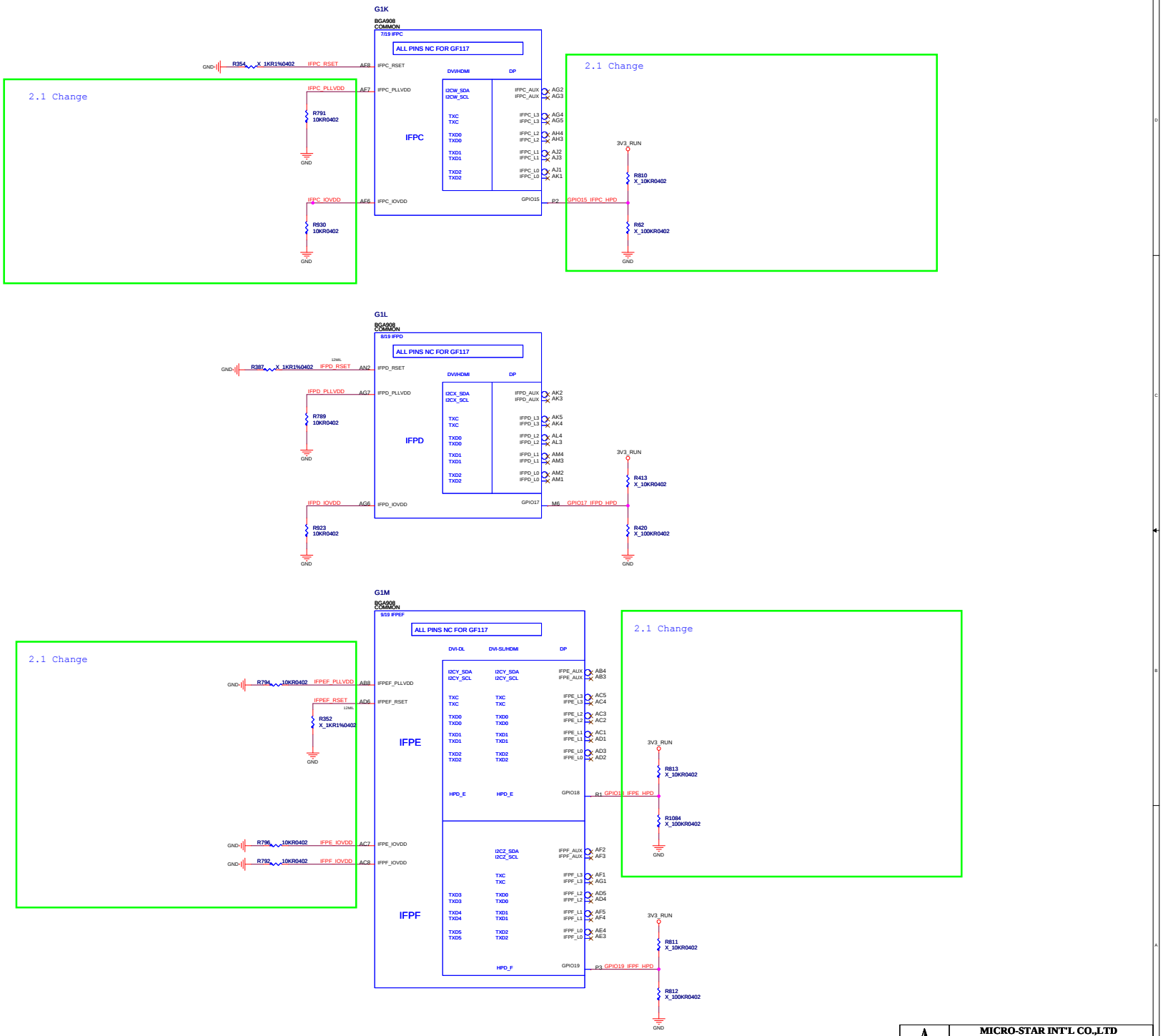
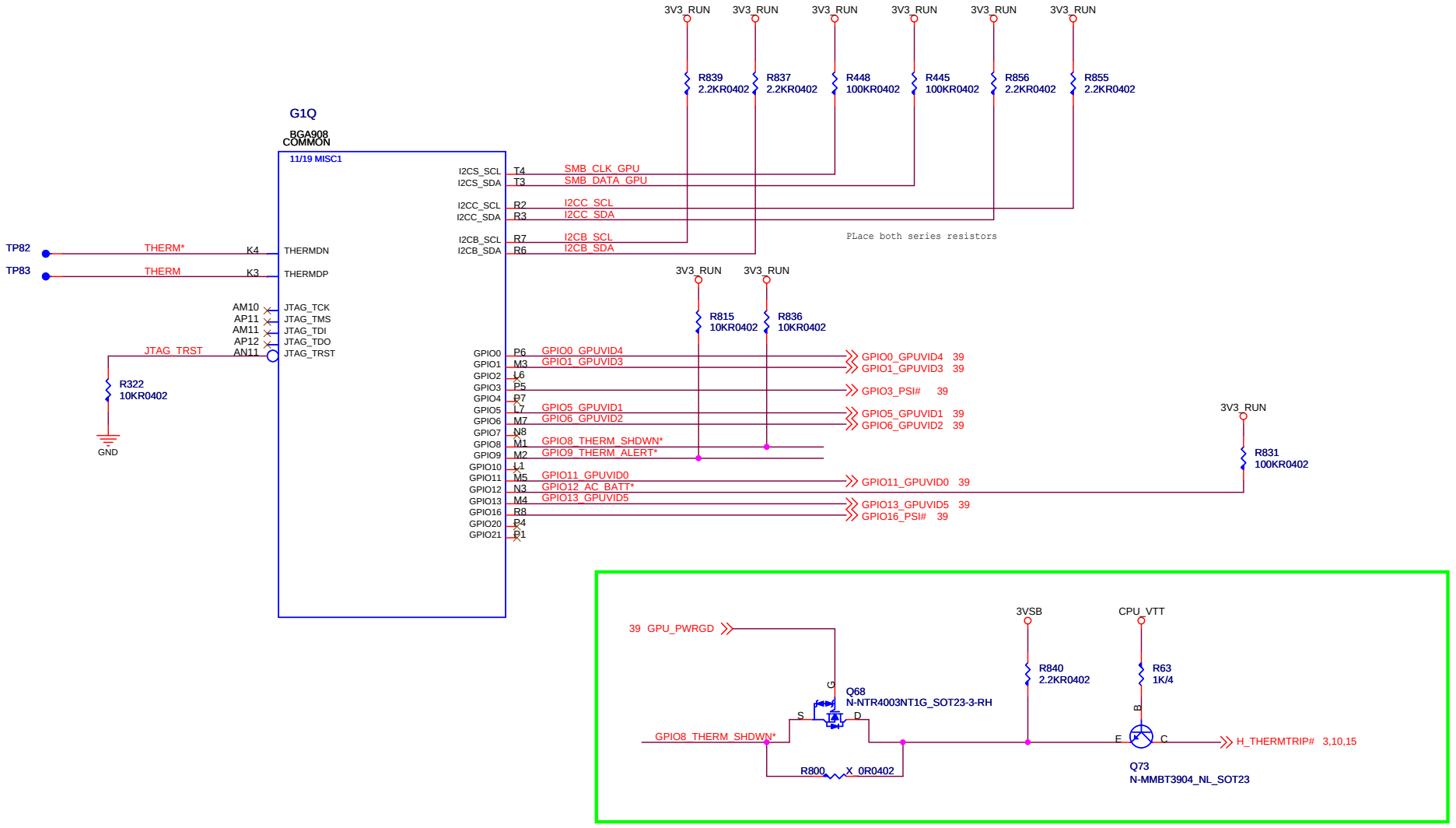


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-AC75	
Size: Custom	Document Description: DAC_A, PLL, CRYSTAL-NV	Rev: 2.1
Date: Thursday, June 28, 2012	Sheet 47 of 56	





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-AC75	
Size B	Document Description: GPIO, JTAG, TEMP SENSOR-NV	Rev 2.1
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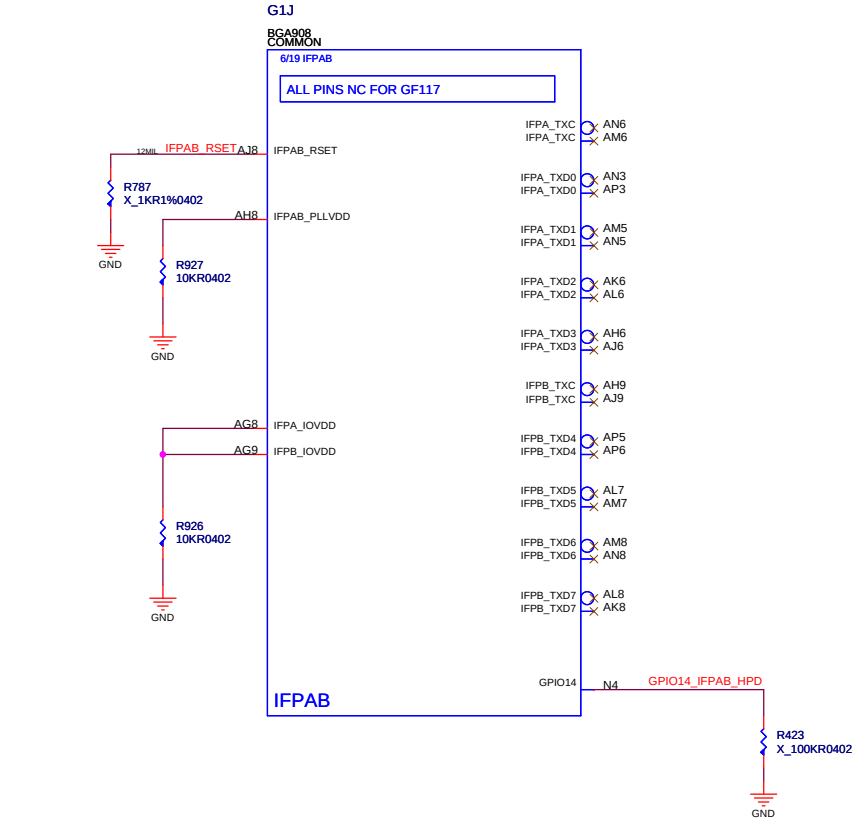
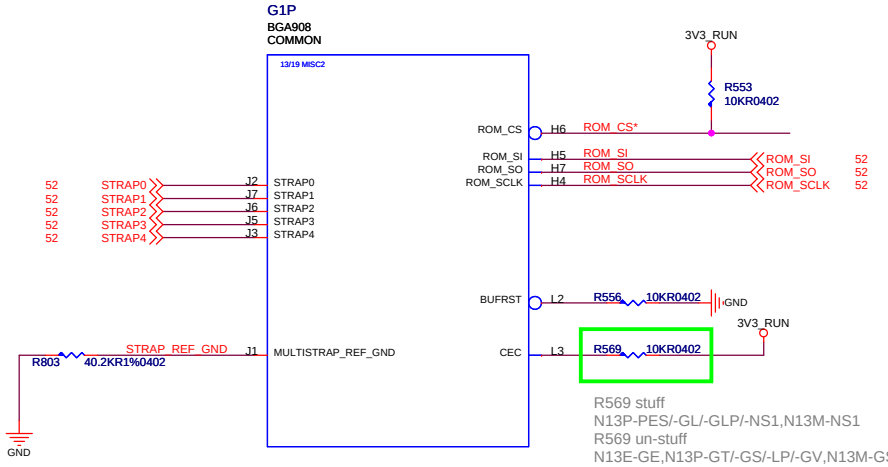
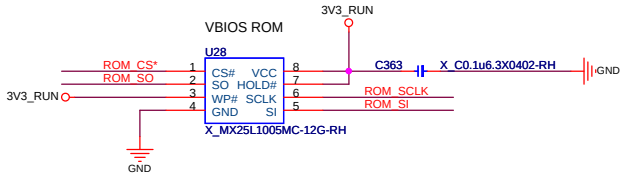




R569 stuff
N13P-PES/-GL/-GLP/-NS1,N13M-NS1
R569 un-stuff
N13E-GE,N13P-GT/-GS/-LP/-GV,N13M-GS/-GE1,N14P-Q1/-Q3



MICRO-STAR INT'L CO.,LTD		
MS-AC75		
Size: Custom	Document Description: LVDS, VBIOS-NV	Rev: 2.1
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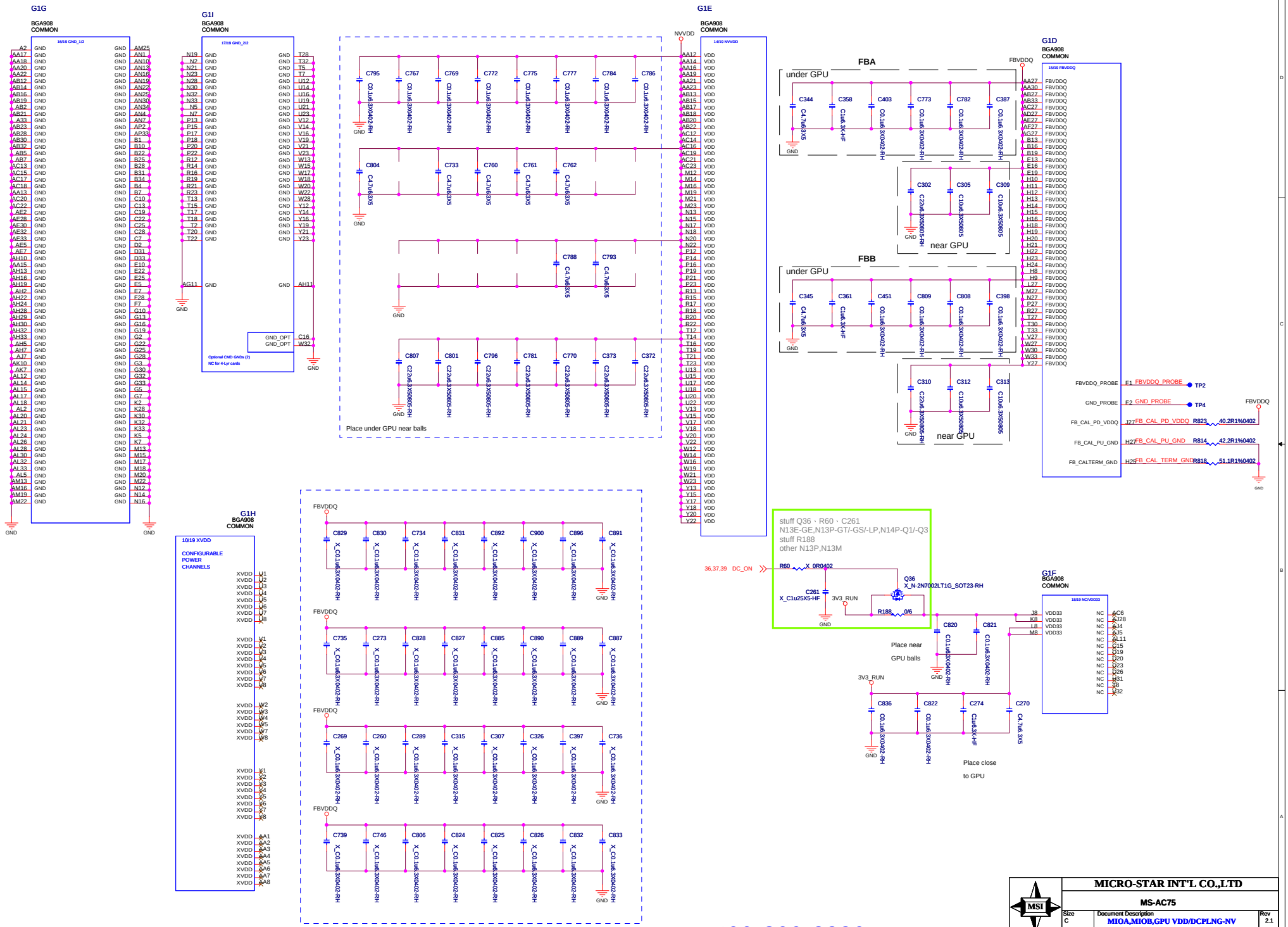

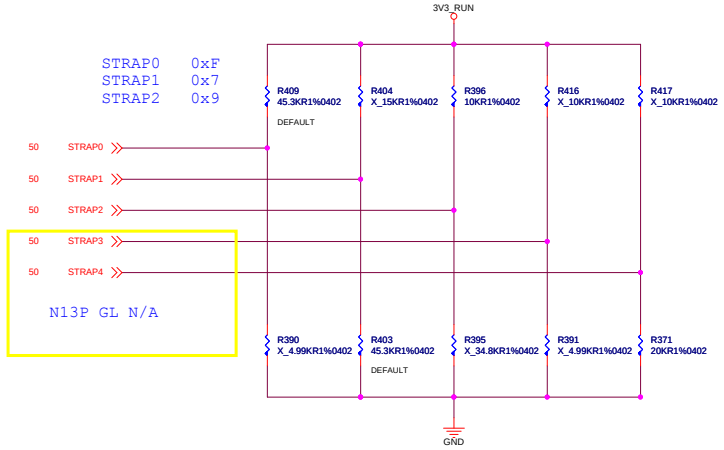

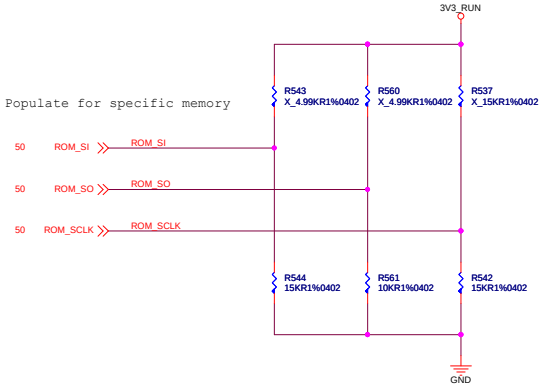

GF108 64Mx16 HYNIX H5TQ1G63DFR-11C Starp 0x2 15K PD

GF108 128Mx16 HYNIX H5TQ2G63DFR-11C Starp 0x5 30.1K PD

GR544
X_30.1KR1%0402

USER_BIT0	Default All SKU(s):
USER_BIT1	0xF = 45K PU
USER_BIT2	LVDS Panel EDID Mode
USER_BIT3	

3GIO_PADCFG_LUT_ADR0	Set at HW reset by the PEX_PADCFG Circuit
3GIO_PADCFG_LUT_ADR1	0x0: Desktop default (normal swing) - 5k PD
3GIO_PADCFG_LUT_ADR2	0x1: Mobile default (low swing) - 10k PD
3GIO_PADCFG_LUT_ADR3	

PCDEVID_3:0] Definitions (Note Actual DEVID set also depends on PCI_DEVID_4)

	GT218	GT216	GF108
PCI_DEVID_0	1000 5K PU GT218-700	1000 5K PU GT216-600	0000 5K PD GF108-630
PCI_DEVID_1	0100 25K PD GT218-730	0100 25K PD GT216-630	
PCI_DEVID_2		1100 25K PU GT216-640	
PCI_DEVID_3		1100 25K PU GT216-950	

VGA_DEVICE	0: 3D DEVICE 1: VGA DEVICE	Set at HW reset by the Device Detect Circuit
SMB_ALT_ADDR	0: Thermal Sensor ADR = 0x9E	0x1 = 10K PD
FB_0_BAR_SIZE	0: Default	
XCLK_417	0: Default	

RAM_CFG[3:0] Definitions

	GF108 64Mx16	GT215/6
RAM_CFG_0	0000 5K PD Reserved	DEFAULT
RAM_CFG_1	0001 10K PD Reserved 0010 15K PD HYNIX 0011 20K PD SAMSUNG	0001 Reserved 0001 64Mx16 128-bit 10K PD Qimonda 0010 64Mx16 128-bit 15K PD Hynix 0011 64Mx16 128-bit 20K PD Samsung 0100 Reserved 0101 32Mx16 128-bit 30K PD Qimonda 0110 32Mx16 128-bit 35K PD Hynix 0111 32Mx16 128-bit 45K PD Samsung * 32Mx16 MAY BE 64Mx16 run at 1/2 density
RAM_CFG_2	GT108 128Mx16	1001 Reserved 1001 64Mx16 64-bit 10K PU Qimonda 1010 64Mx16 64-bit 15K PU Hynix 1011 64Mx16 64-bit 20K PU Samsung 1100 Reserved 1101 128Mx16 64-bit 30K PU Qimonda 1110 128Mx16 64-bit 35K PU Hynix 1111 128Mx16 64-bit 45K PU Samsung
RAM_CFG_3	0100 25k PD Reserved 0101 30k PD Reserved 0110 35k PD HYNIX 0111 45k PD SAMSUNG	

PEX_PLL_EN_TERM100	0: DISABLED	
SLOT_CLK_CONFIG	1: GPU and MCH COMMON REFCLK	0x6 = 35K PD PCDEVID_EXT=0
SUB_VENDOR	1: VBIOS ROM IS PRESENT	0xE = 35K PU PCDEVID_EXT=1
PCI_DEVID_EXT	0: PCDEVID[4] = 0 or 1 (SKU Specific)	

	GND	3V3
4.99K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
24.9K	0100	1100
30.1K	0101	1101
34.8K	0110	1110
45.3K	0111	1111

MICRO-STAR INT'L CO.,LTD

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C	STRAPS, MOUNTING HOLES-NV	2.1

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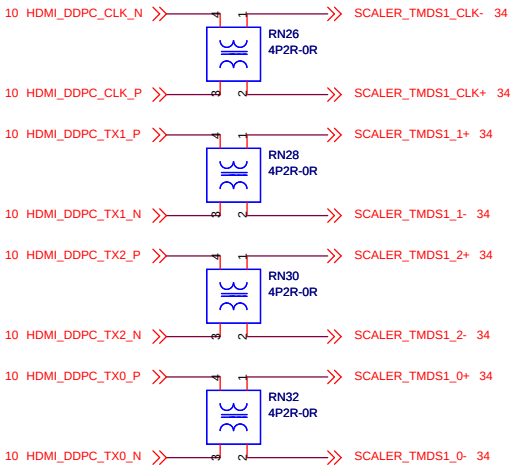
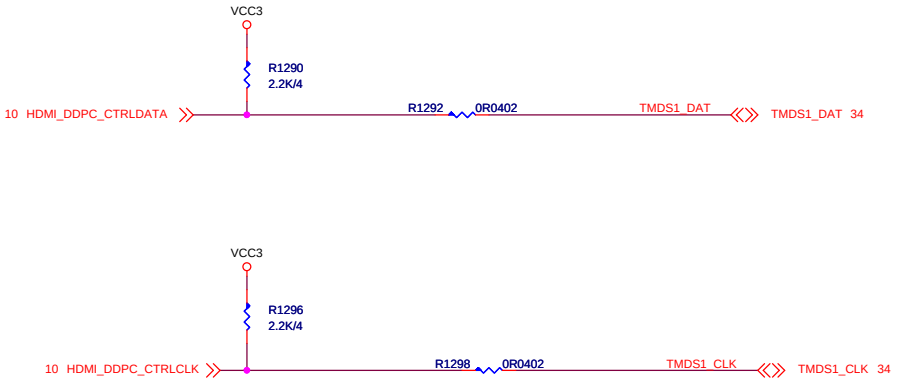
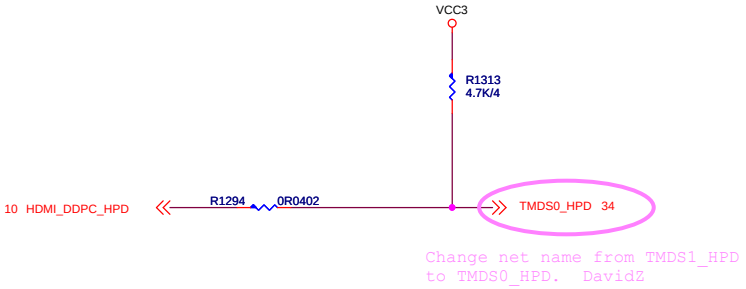


2.1 Change

2.1 Change





MS-AC751 0A-->1.0 (Synergy BOM)
RN27 , RN29 ,RN31, RN33 unstuff ,
RN26 , RN28 ,RN30, RN32 stuff

R1291 , R1293 ,R1297, R1299 ,R1295 unstuff ,
R1290 , R1292 ,R1296, R1298 ,R1294 stuff

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Size	Document Description	Rev
Custom	IGD&NV_SEL	2.1

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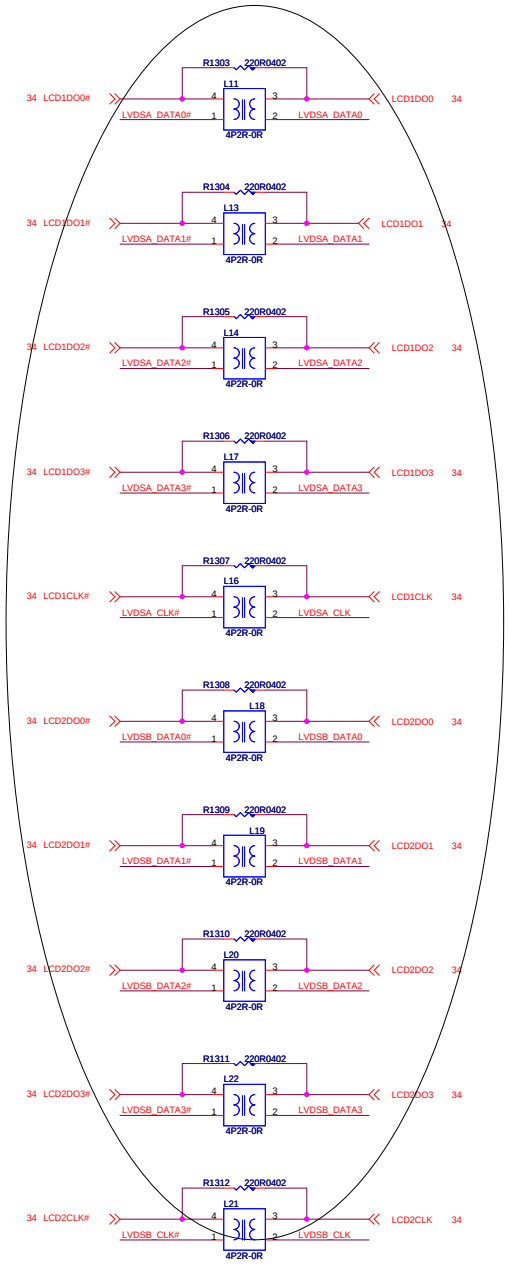

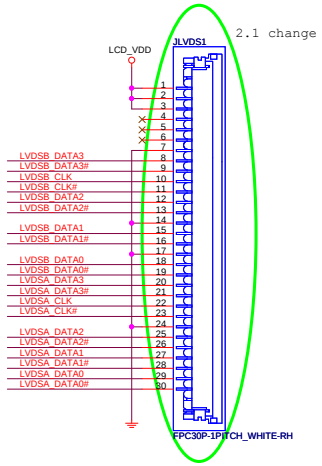

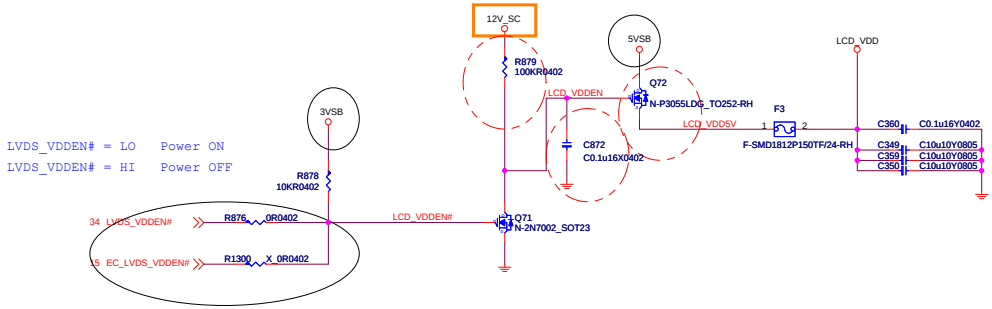

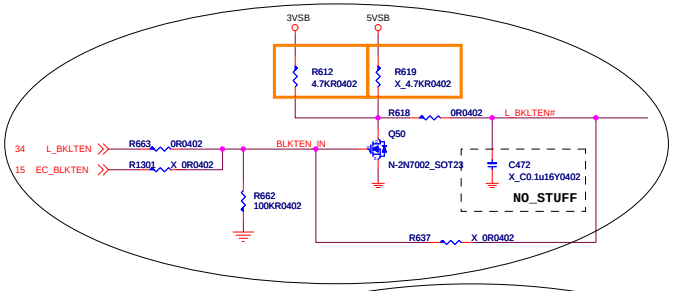

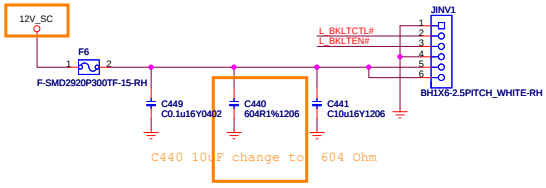

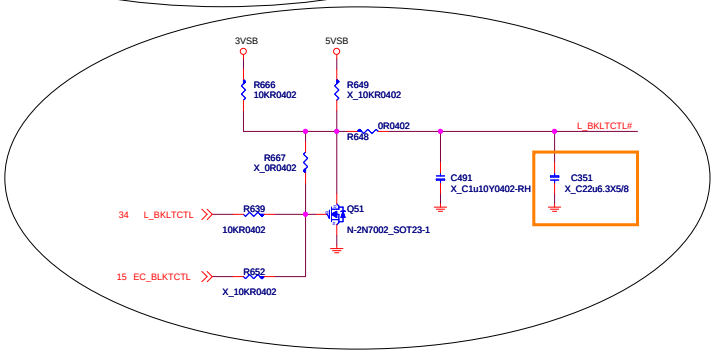

MICRO-STAR INT'L CO.,LTD

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C	LVDS / Interver Connector	2.1

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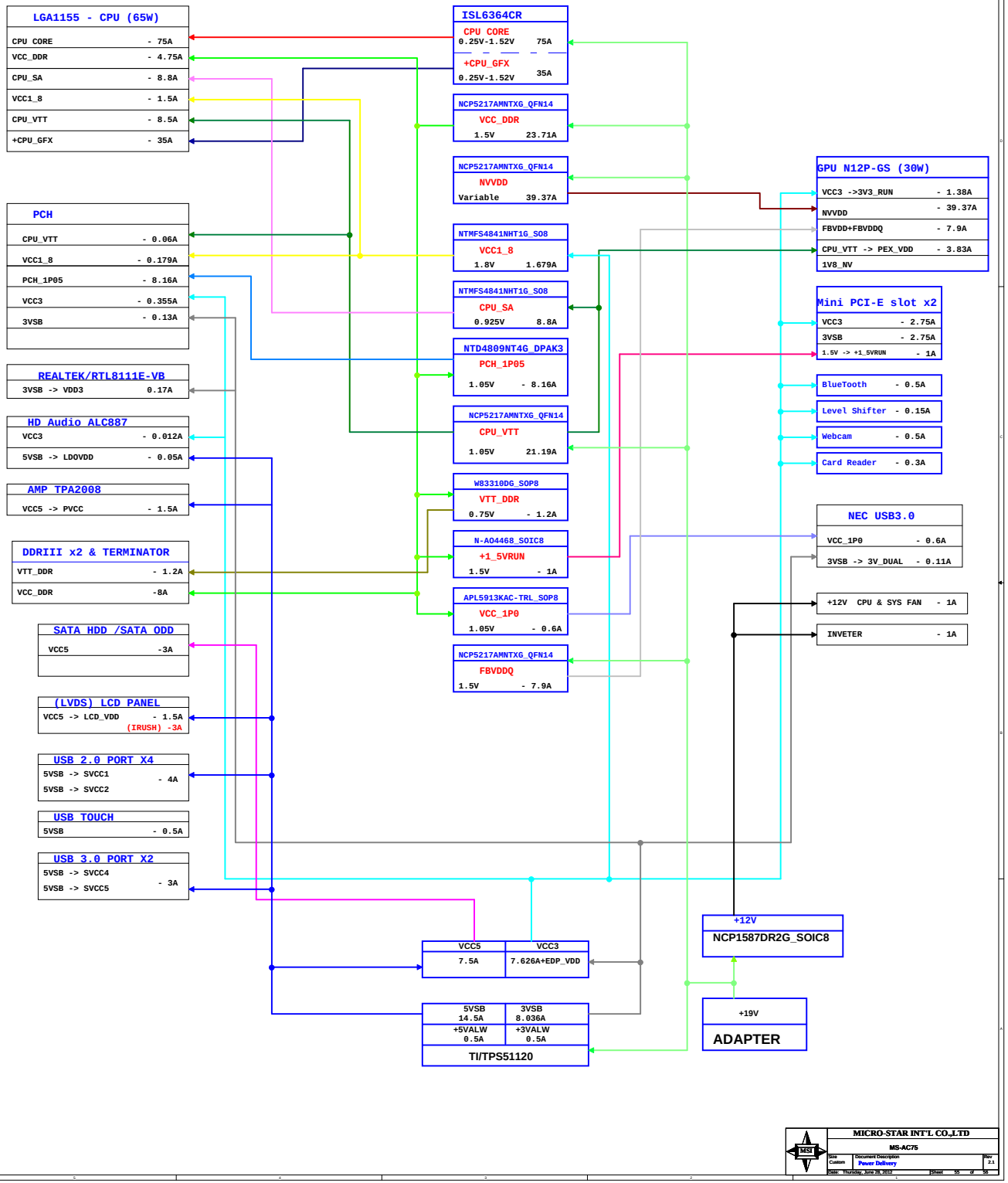

MS-AC751 0A-->1.0

Page 21 Stuff R1022,unstuff R1023.
Page 21 Change net "EAPD" from U34 pin 47 to U34 pin2.
Page 15 Add R1167 and R1131.
Page 15 Add net EC_AMP_SD# on EIO pin18.
Page 21 modify U50 shutdown circuit.
Page 21 Unstuff C451,C452,C532,C533.
Page 21 Change L56 connection from PVCC to 5VSB.
Page 21 Unstuff L55.
Page 21 Change C917 and C928 connection from GND to PGND.

MS-AC751 0A-->1.0 (2011.04.11)
Page 21 Change net: HDMI0_CABLE_DET from pin 64 to pin63.
Page 26 Add C103 near the U2 (control V pin) unstuff
Page 17 Add R449 unstuff
Page 31 EMI5 unstuff (BOM)

MS-AC751 0A-->1.0 (2011.04.11)
Page 15, 24,30,54   Add For Scaler 12V power circuit (12V_SC)
Page 21 Amplifier change back to TI 2008D
Page 26 Add EC47 CAP (C71-5610210-S03)
Page 28 Modify:C52,R75,R80 (Power solution)

MS-AC751 0A-->1.0 (2011.04.18)
Page 26   5VSB change to +5VALW (DDR POWER)
Page 14   R145 4.7K change to 1K
Page 26,30 About power LED can't blink ==>add net: DDR_EN
Page 10 Change sensor EMITTER1,EMITTER2 ==>GPIO6 , GPIO7

MS-AC751 0A-->1.0 (2011.04.20)
Page 15   R1103 4.7K change to 1K
Page 39   Add power(GPU)
Page 15   SIO (NCT6681D) MSI PN:B02-0668104-N62
Page 22   JIR1 Change MSI PN:N32-1030870-H06

MS-AC751 0A-->1.0 (2011.04.22) Reference AA71 SCH, modify the points

Page 54   Add C351 CAP unstuff
Page 26   Add EC51 CAP (預留,MSI料號申請中)
Page 38 power sequence VCC5 change to 5VSB , Add C789 , Delete R477

MS-AC751 0A-->1.0 (2011.04.25)
Page 54 R619 unstuff , R612 stuff

MS-AC751 0A-->1.0 (2011.04.29)
EMI Suggestion:
Page 27,39   R774, C674, PR18, PC14 上件 針對低頻150MHz)
Page 30   C1073 改為1000p 上件 (192MHz)
Page 15   LPC_FRAME# 增加10pF to GND near JTPM1 (192MHz)
Page 31   H1與H2 請改為與GND 連接
Page 15   KBRST issue R1149 unstuff , R1152 stuff 1K Ohm

MS-AC751 0A-->1.0 (2011.05.02)
Page 17   R1177 ,R1178 1.8K Ohm chage to 4.7K Ohm
Page 31   M1-M8 modify footprint :H_R394D157_V8
Page 9   RTC : C266 / C267 20P change to 27P
Page 11   RTC : C221 / C222 12P change to 10P
Page 30   PC35 10uF change to 604 Ohm
Page 34   R1232,R1234 100 Ohm change to 33 Ohm,
Page 29   Q20 unstuff , Q49 stuff
Page 11,15   R777 unstuff , R1144 stuff
Page 10   R237 unstuff
Page 28 Thermal balance solutions R97,R694 change to 10K

MS-AC751 0A-->1.0 (2011.06.10)

Page 24   unstuff POWER VCC2_8
Page 30   unstuff SENSORMODULE
Page 11   C221 10P change to 8.2P ,C222 10P change to 12P
Page 54   C440 10uF change to 604 Ohm

MS-AC751 0A-->1.0 (2011.06.29)

Page 19   unstuff C934 ,C935 ,C936
Page 54   R879 10K change to 100K ,C872 0.01u change to 0.1u (panel issue)
Page 54   PANEL SELECT (SYS_ID0,SYS_ID1,SYS_ID2)

MS-AC751 1.0 --> 2.0

Page 39 ~ 52 GPU change N13P-GL
Page 33 Card Reader change 5139
Page 3、15 Modify THERMTRIP# circuit
Page 21 Modify AUDIO circuit (Add series resistance)
Page 24 Change UPI IC New P/N.
Page 34 Change UPI IC New P/N.
Page 38 Change UPI IC New P/N.
Page 15 Modify PROCHOT# circuit

MS-AC751 2.0 --> 2.1

Page 37 Add 3VA & 5VA for Erp/Eup 0.5W
Page 39 PR26 change to 12Kohm for FBVDDQ OCP (Power team suggest)
Page 28 C48 change to 1000p (Power team suggest)
Page 39 PU3 VDD & VCCP change to VCC5 (Power team suggest)
Page 54 JLVDS1 change to N5A-30F0120-H06
Page 29 EC51 change to C98-4702530-SO8 unstuff
Page 15 Remove COM Port from BOM

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