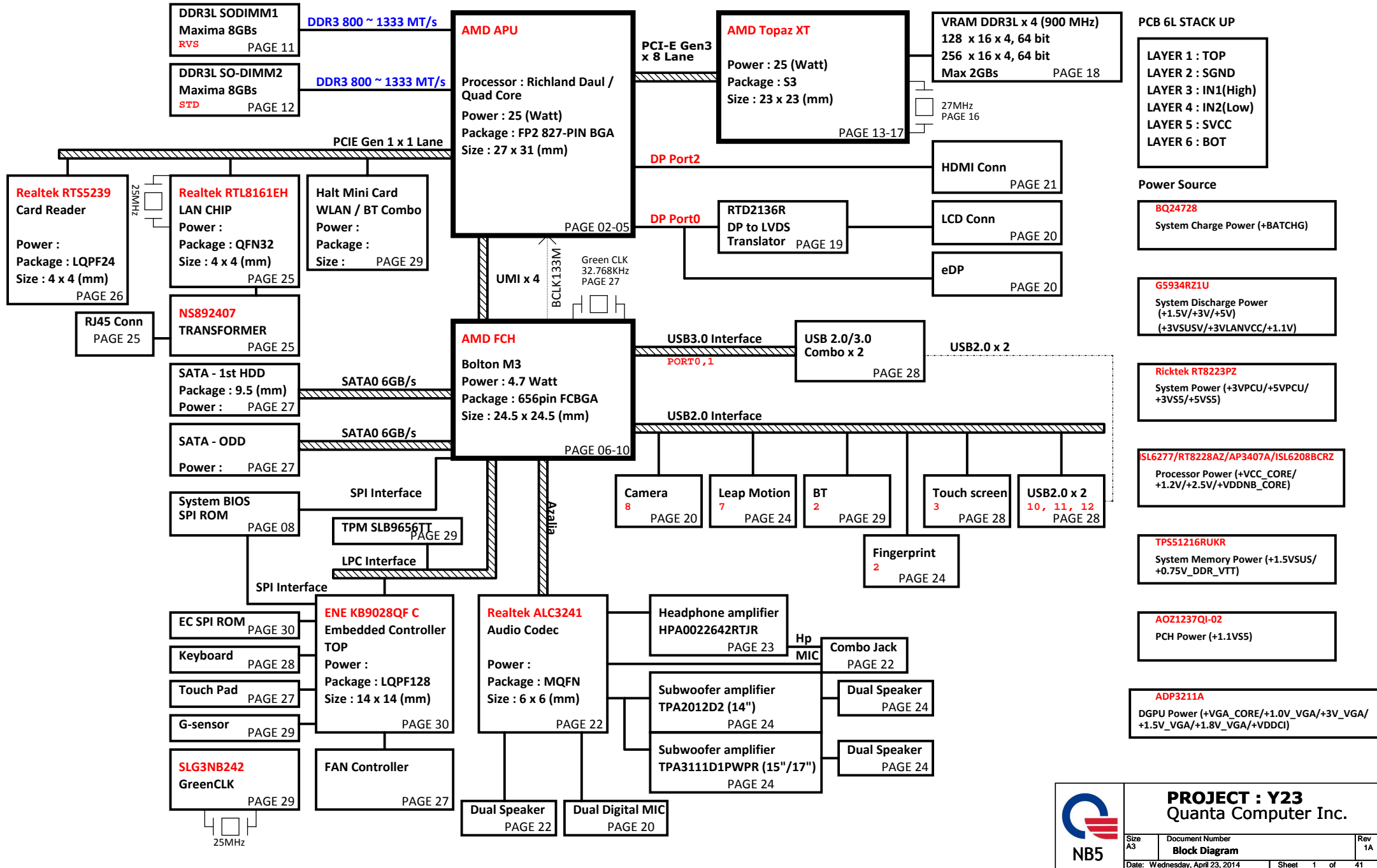


VINE_AMD Richland DIS/UMA (14"/15.6"/17.3")





3



1

1

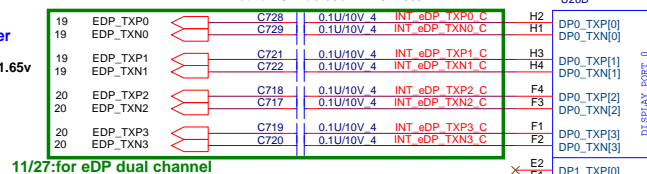
1

1





Display port power 1.5V min 1.2v max : 1.65v



11/27:for eDP dual channel

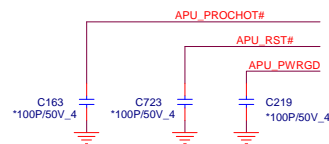
4/19 HDMI change to DP2 for Comal.

DP2 output to
HDMI connector

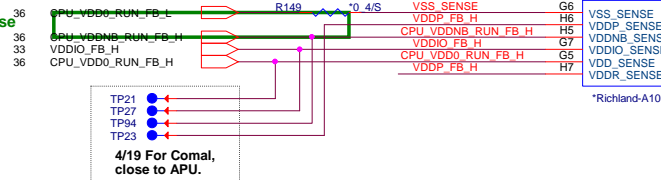
note --HDMI P&N can not swap

Note: CLK_APU_HCLKP/N is 100MHZ SSC

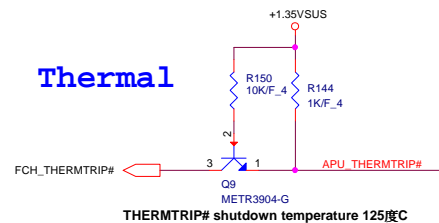
Note: CLK DP NSSCP/N is 100MHZ non-SSC



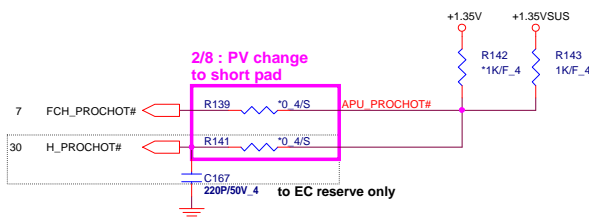
11/27:remove for Power no use³



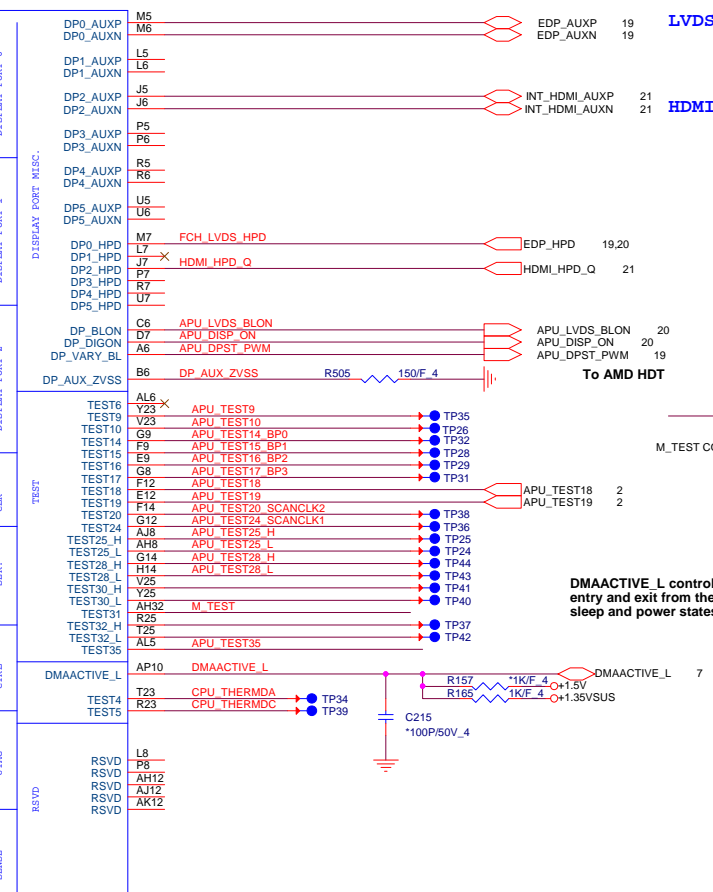
Thermal



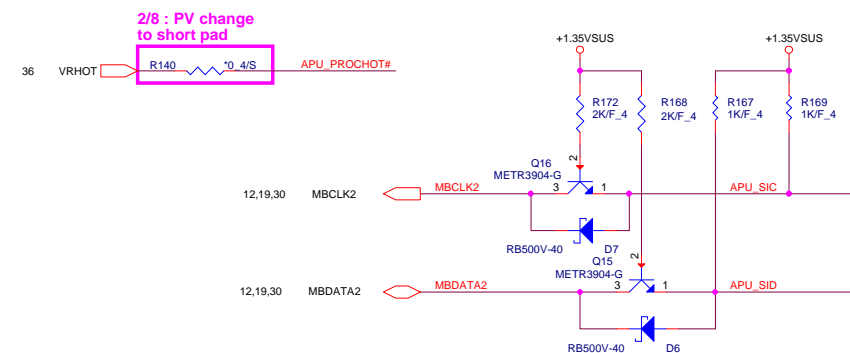
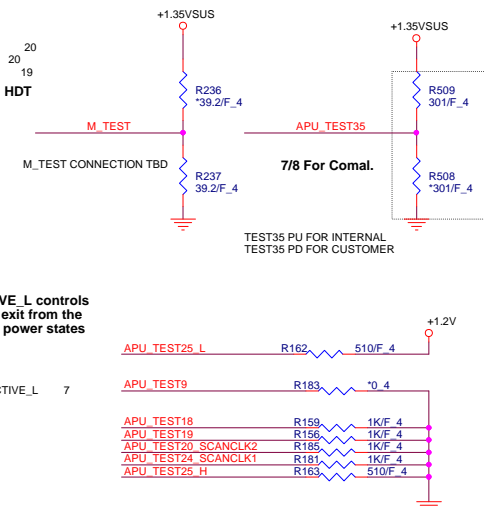
THERMTRIP# shutdown temperature 125°C



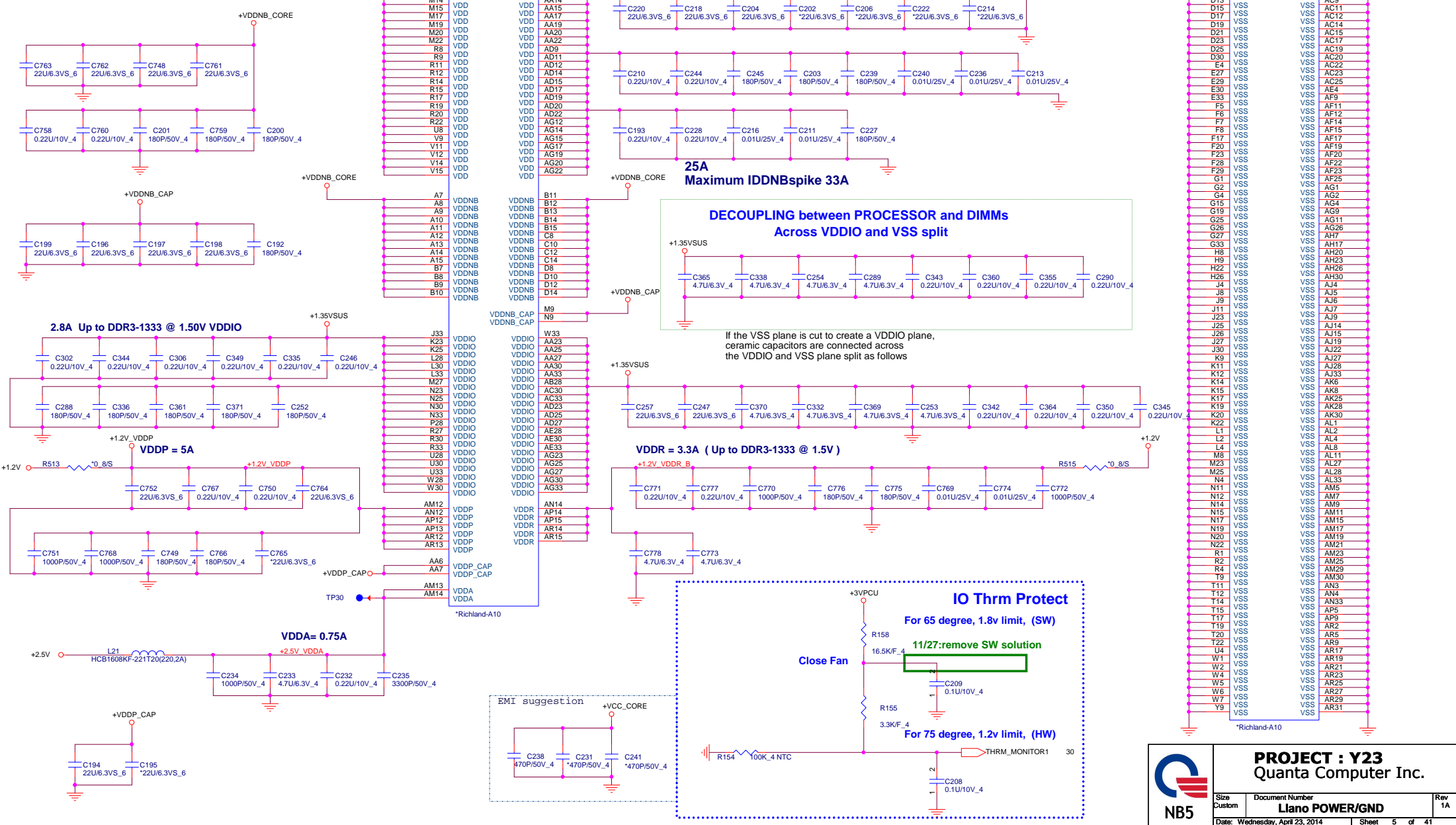
*Richland-A10



DMAACTIVE_L controls entry and exit from the sleep and power states



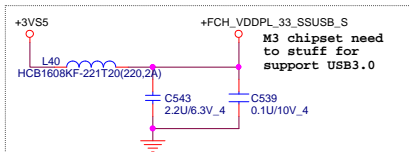
APU POWER TABLE		
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V







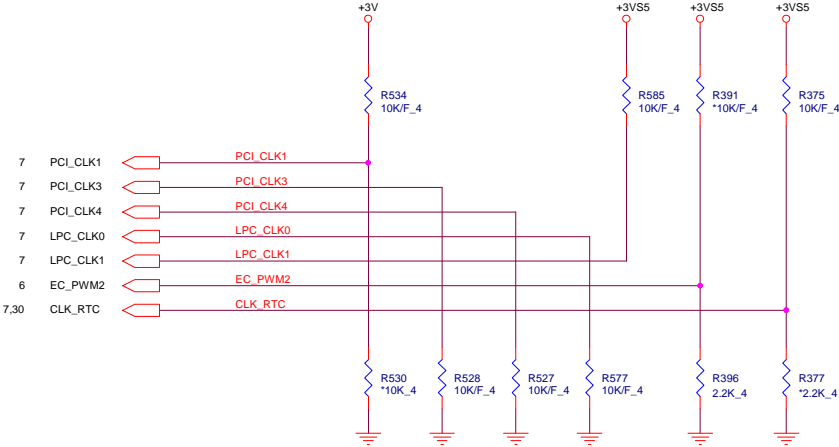
U29C



STRAPS PINS



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

		PCI_CLK1		PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE ENABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE DISABLED

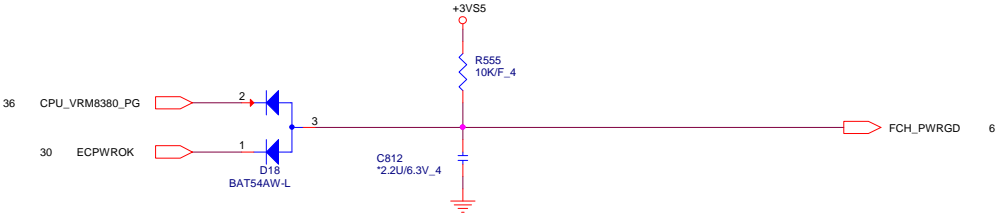
DEBUG STRAPS

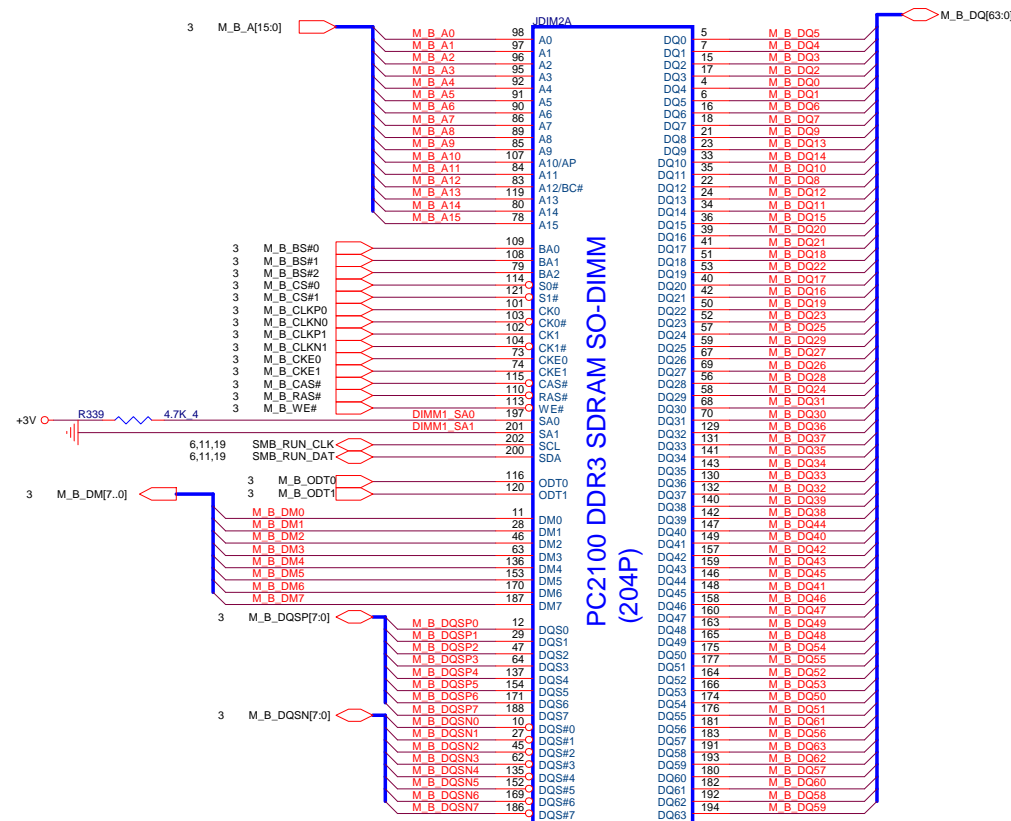
FCH has 15K Internal Pull Up for PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

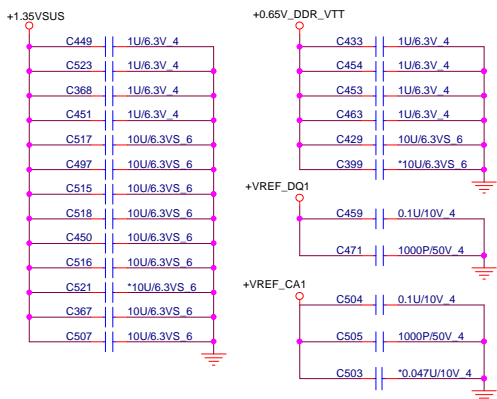
FCH PWRGD



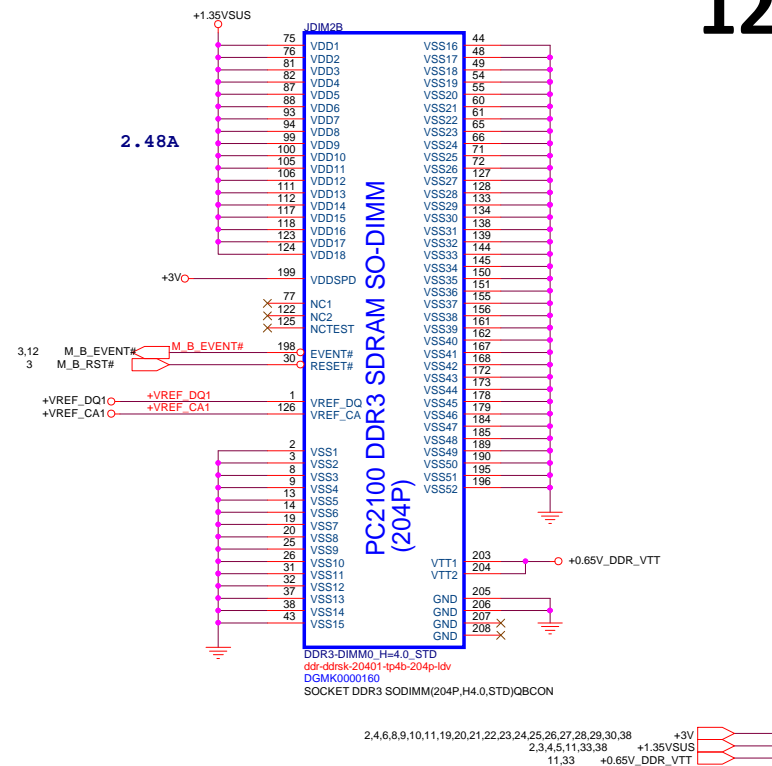
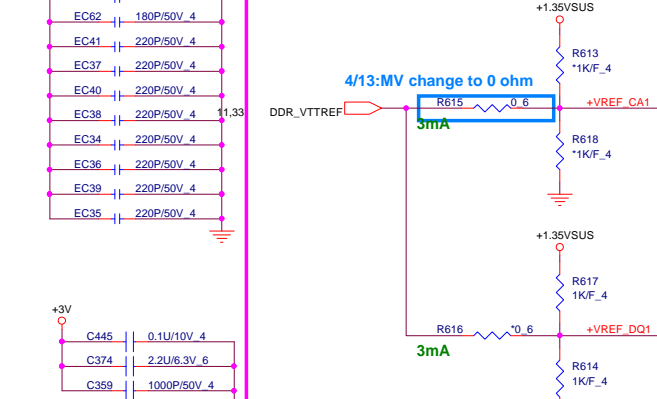


DDR3-DIMM0_H=4.0 STD
ddr-ddrsk-20401-tp4b-204p-ldv
DGMK0000160
SOCKET DDR3 SODIMM(204P,H4.0,STD)QBCCN

Place these Caps near So-Dimm1.

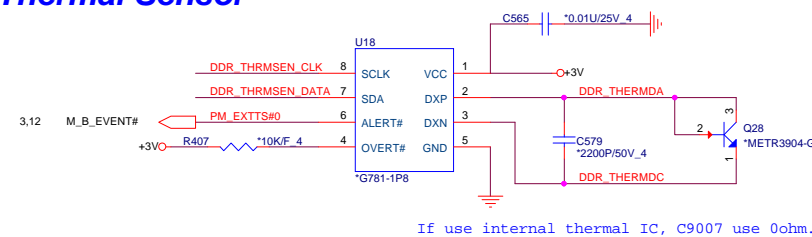


2/7 : PV modify



DDR3 Thermal Sensor

Local Thermal Sensor



If use internal thermal IC, C9007 use 0ohm.

Main:AL000781039

2nd:AL001412005

Main:AL001412003

2nd:AL000431014

G781-1P8(9Ah)

EMC1412-2-ACZL-TR(9Ah)

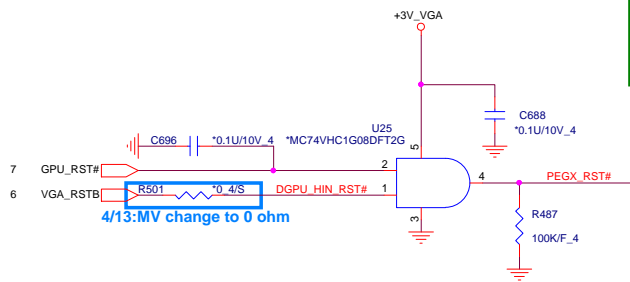
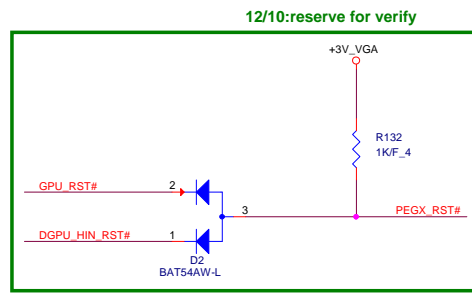
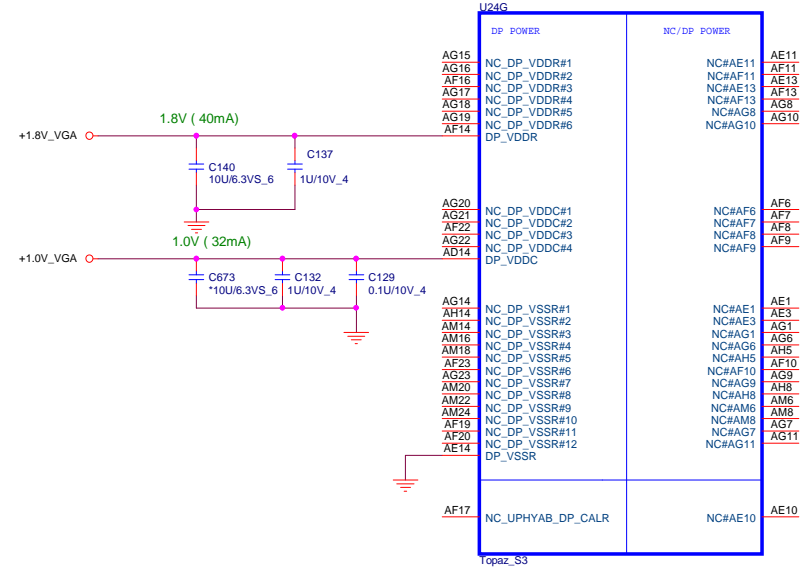
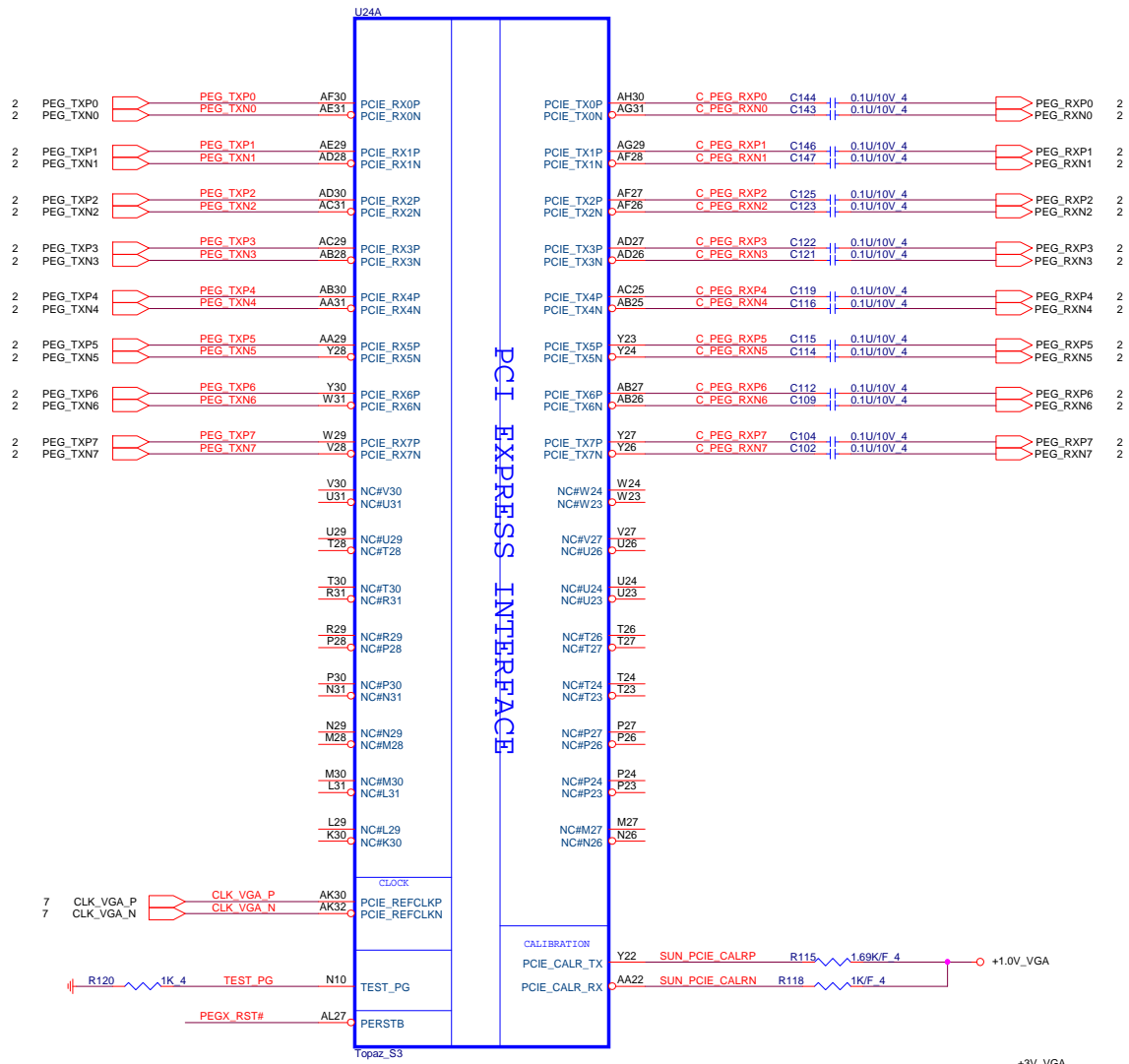
EMC1412-1-ACZL-TR(98h)

TMP431ADGKR(98h)



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 2/2 (4H)	1A
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14,16,30,41 +3V_VGA
14,16,29,39,41 +1.8V_VGA
16,41 +1.0V_VGA

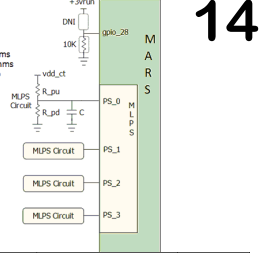
- MPLS Implementation**
- Connect GPIO_28 to I2C1 pulldown to enable MPLS
 - If any of PS_0/1/2/3 is not used, leave "no connect"
 - R_{psu}, R_{pd} and C must be properly populated per tables below
 - Place MPLS circuit components as close to the ASIC as possible
 - Total DC resistance of trace between PS pin and C should be less than 2 ohms
 - Total DC resistance of trace between C and ground should be less than 2 ohms
 - Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (pF)	W (mm)	h (mm)
680	00	00
82	01	01
10	10	10
NC	11	11

Resistor Divider Lookup Table

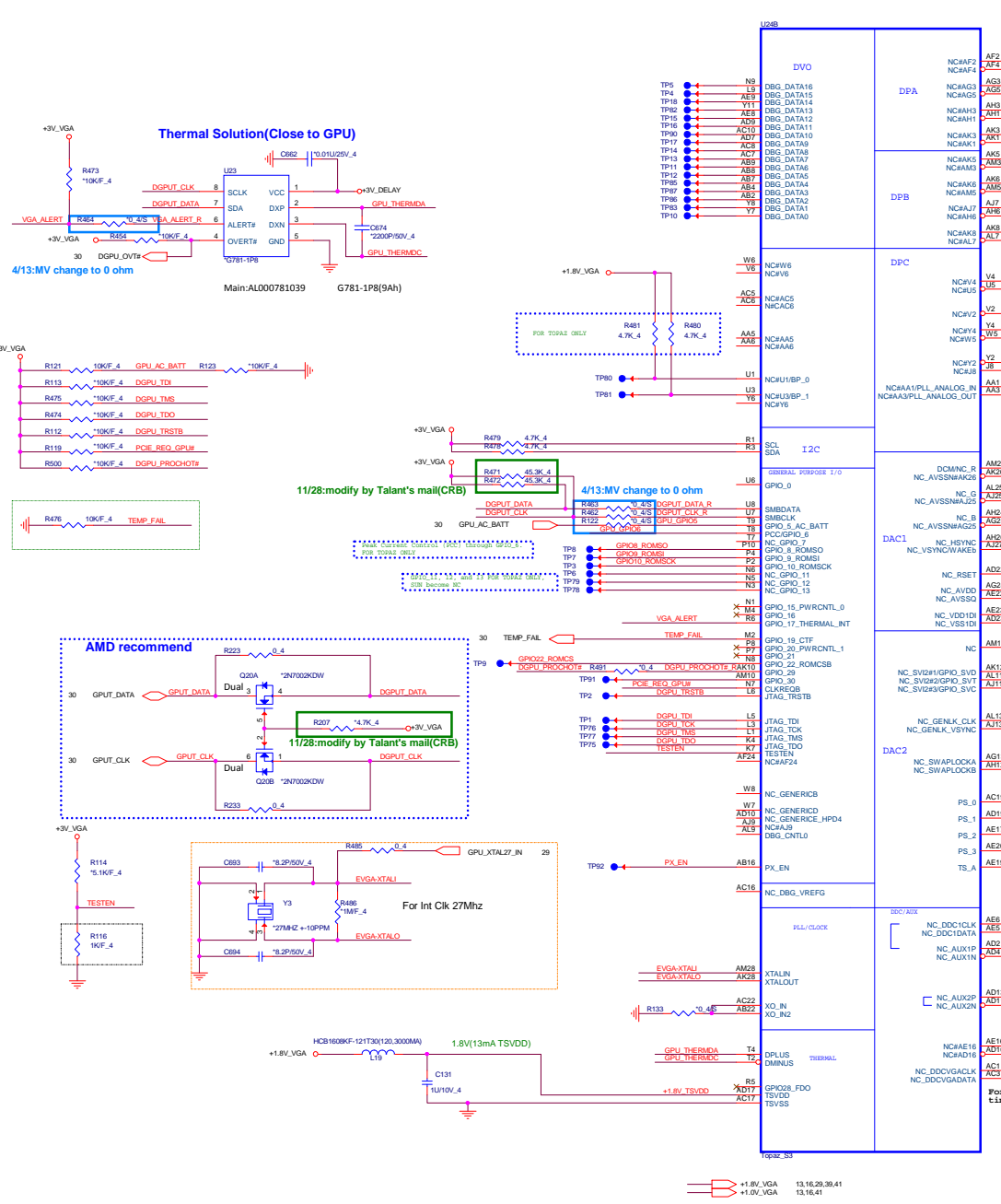
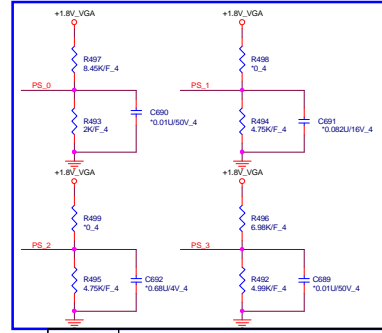
R _{psu} (Ohm)	R _{pd} (Ohm)	W (mm)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3480	10000	110
4750	NC	111

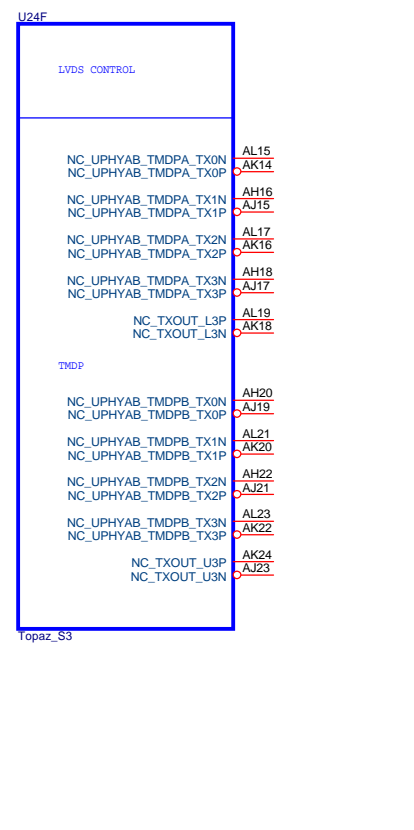
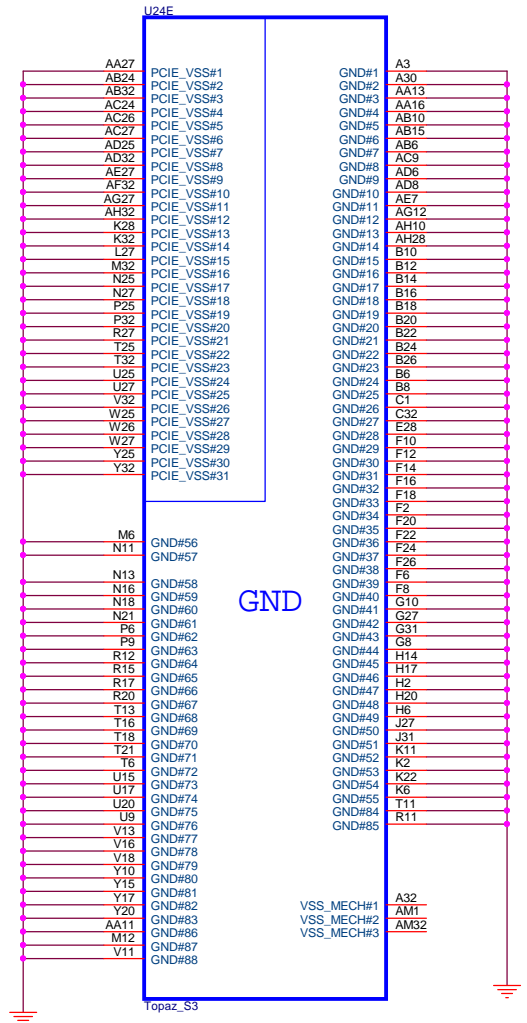


MPLS Bit	Strap Name	Description	Recommended Settings
PS_0[1], PS_0[2], PS_0[3]	ROM_CONFIG[0], ROM_CONFIG[1], ROM_CONFIG[2]	If STRAP BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory aperture size. See Primary Memory Aperture size (p. 25).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIE GEN3 capability. 1 = PCIE GEN3 is supported. 0 = PCIE GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PEN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQ#). 0 = The CLKREQ# power management capability is disabled 1 = The CLKREQ# power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS# transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved.	1
PS_3[1], PS_3[2], PS_3[3]	BOARD_CONFIG[0], BOARD_CONFIG[1], BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1

PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Hynix- F(huma)	128Mb16 *4, 900Mhz	H5TC2G63PFR-11C	NC	4.75K
001	Micron- K die	128Mb16 *4, 900Mhz	M741J128M16J-T93G:K	8.45K	2K
010	Samsung- Q die	128Mb16 *4, 900Mhz	K4W2G1646Q-BC1A	4.53K	2K
011	Hynix- Huma die	256Mb16 *4, 900Mhz	H5TC4G63APR-11C	6.98K	4.99K
100	Samsung- D die	256Mb16 *4, 900Mhz	K4W4G1646D-BC1A	4.53K	4.99K
101	Micron- E	256Mb16 *4, 900Mhz	M741J256M16HA-093G:E	3.24K	5.62K

BIT5 => BIT0
PS0 => 11001
PS1 => 11000
PS2 => 11000
PS3 => 11000

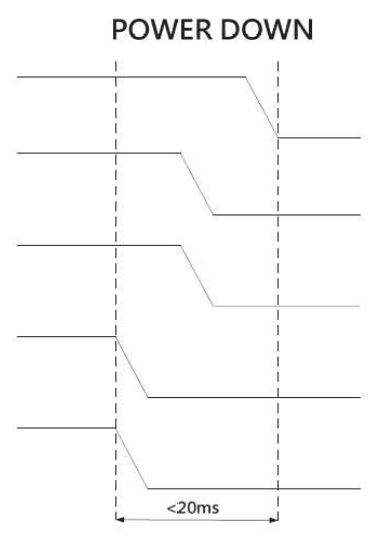
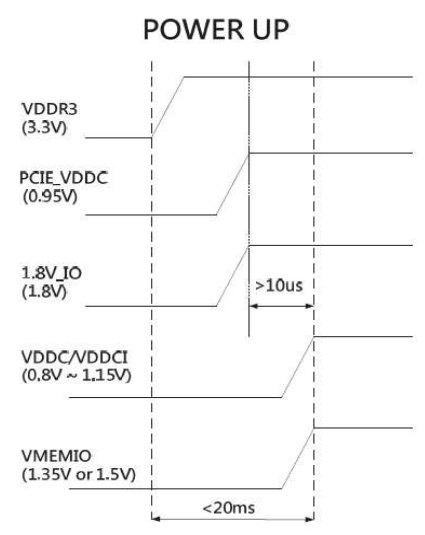


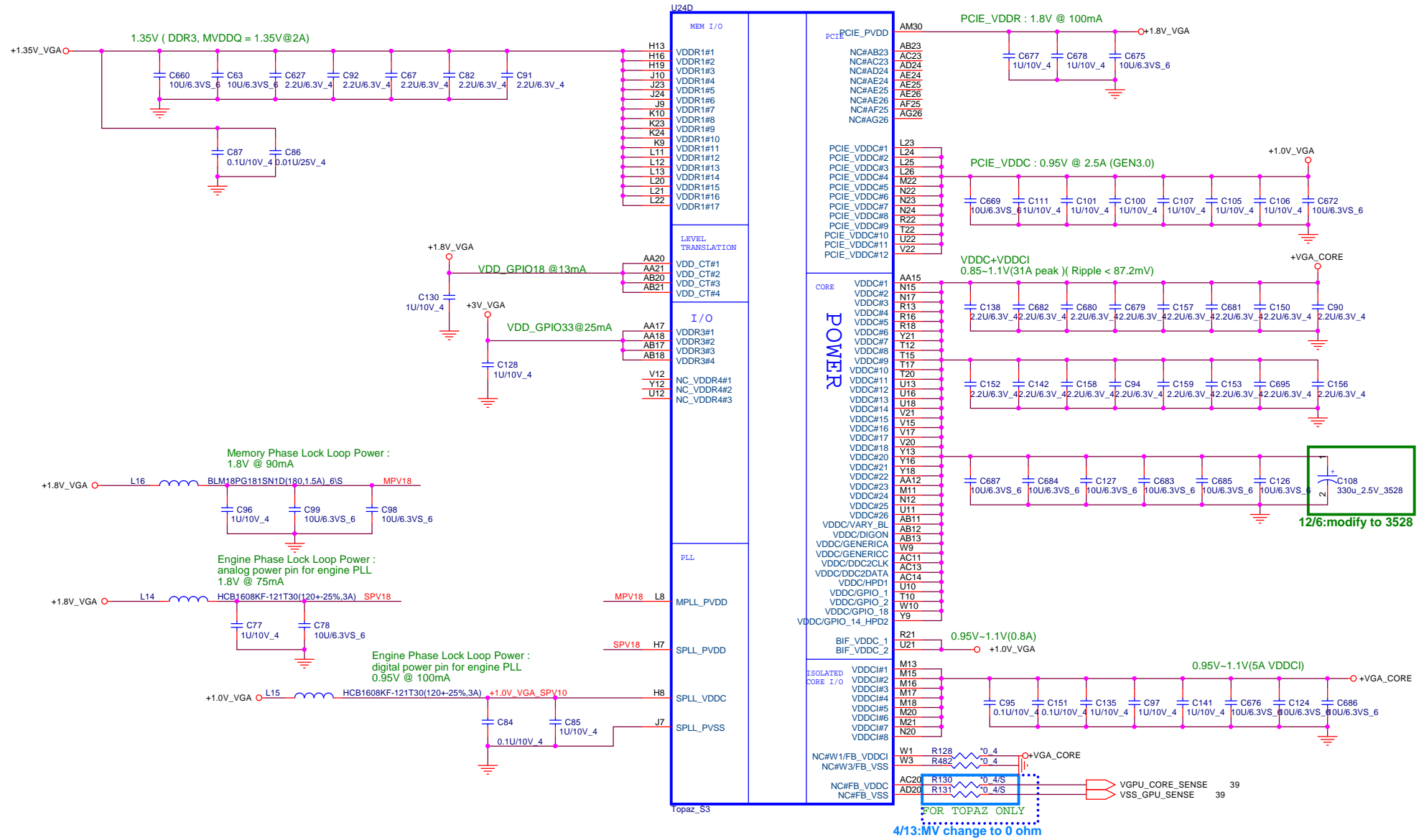


CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

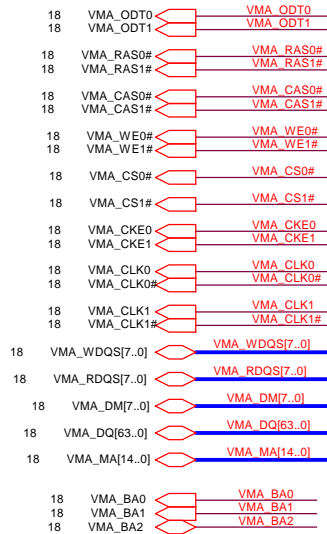
NOTE1: AMD RESERVED CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.				
GPIO21	H2SYNC	GENERICC	GPIO8	GPIO2

POWER UP / POWER DOWN SEQUENCE



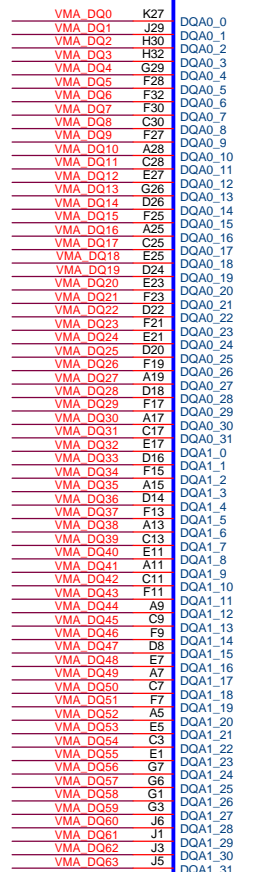


+1.35V_VGA	17,18,39
+1.8V_VGA	13,14,29,39,41
+1.0V_VGA	13,41
+VGA_CORE	39,40

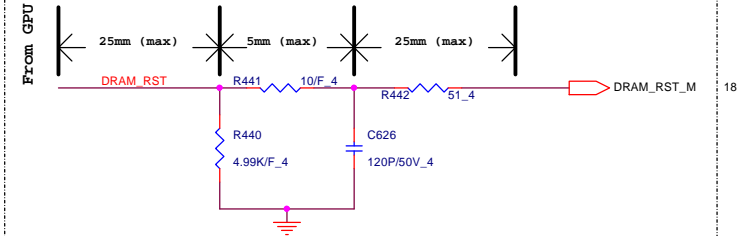
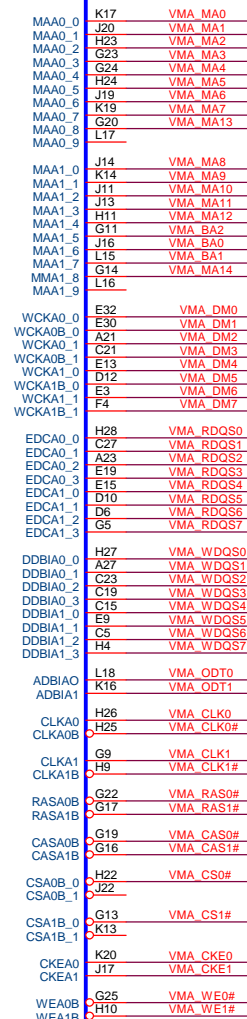


support 1Gbit
VRAM (64M X 16)

U24C

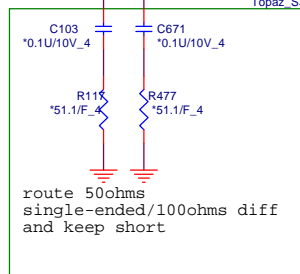
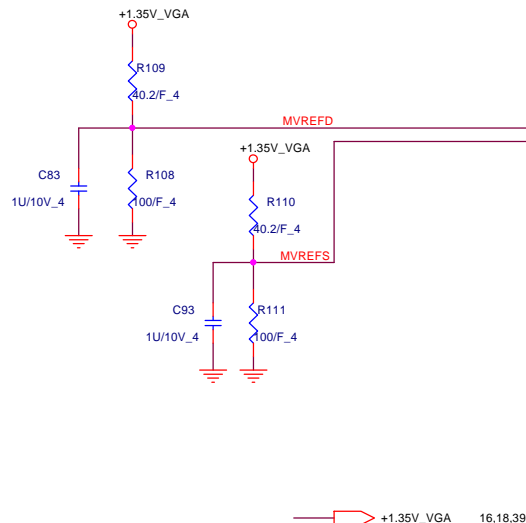


MEMORY INTERFACE



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

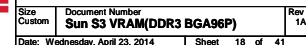


route 50ohms
single-ended/100ohms diff
and keep short

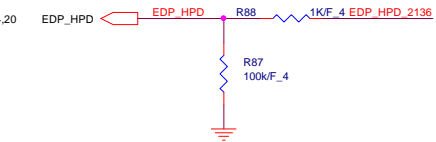
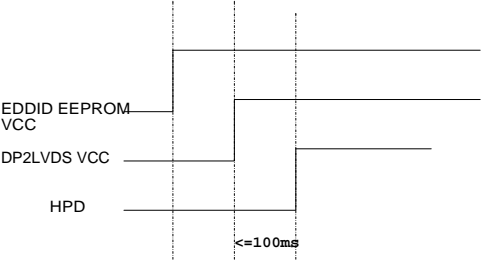


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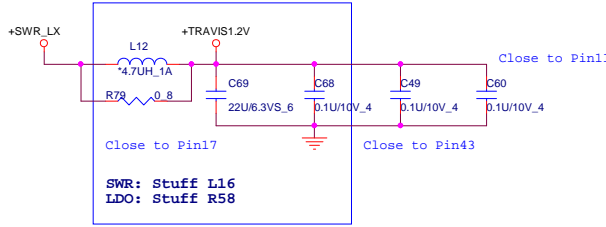
Size	Document Number	Rev
	TPOAZ_S3_MEM_Interface	1A
Date:	Wednesday, April 23, 2014	Sheet 17 of 41



RTD2136S Power Up Sequence




L69: need use CV-4709MN00 for Vendor suggestion
2nd CV-4708MN03



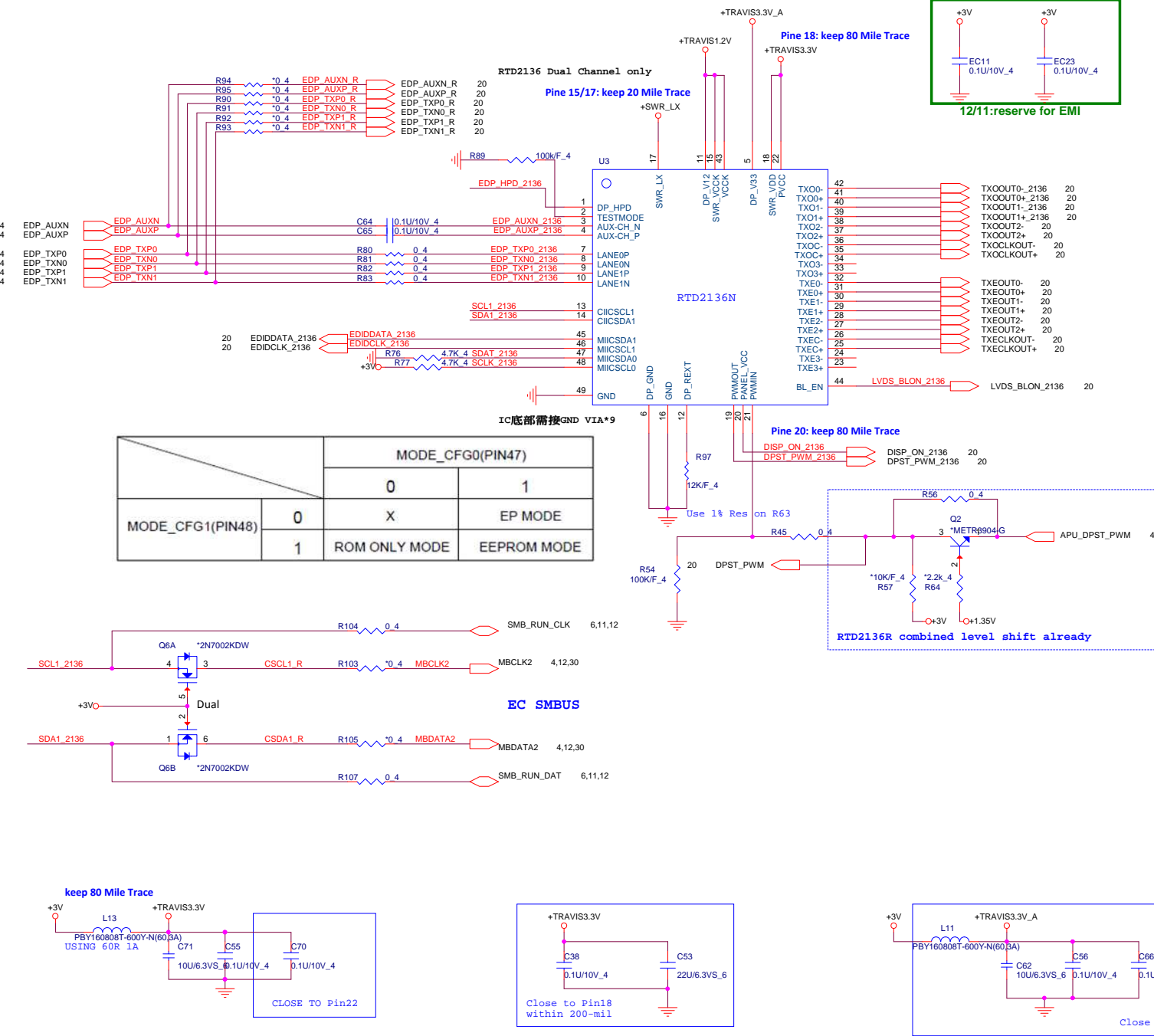
SWR: Stuff L16
LDO: Stuff R58

4,20,36,38 +1.35V
2,4,6,8,9,10,11,12,20,21,22,23,24,25,26,27,28,29,30,38 +3V
2,4,22,24,29,34 +1.5V

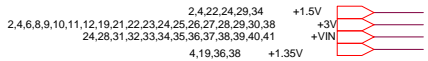
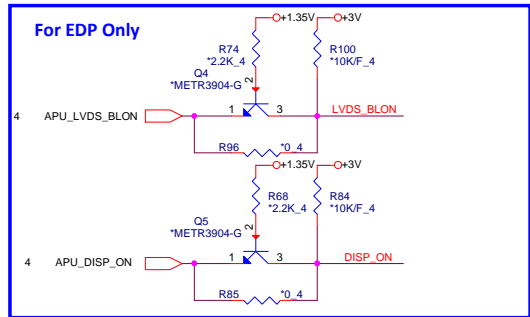
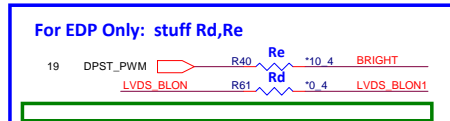
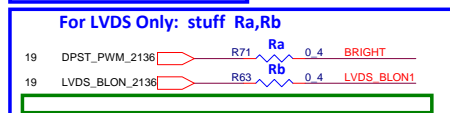
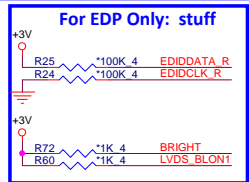
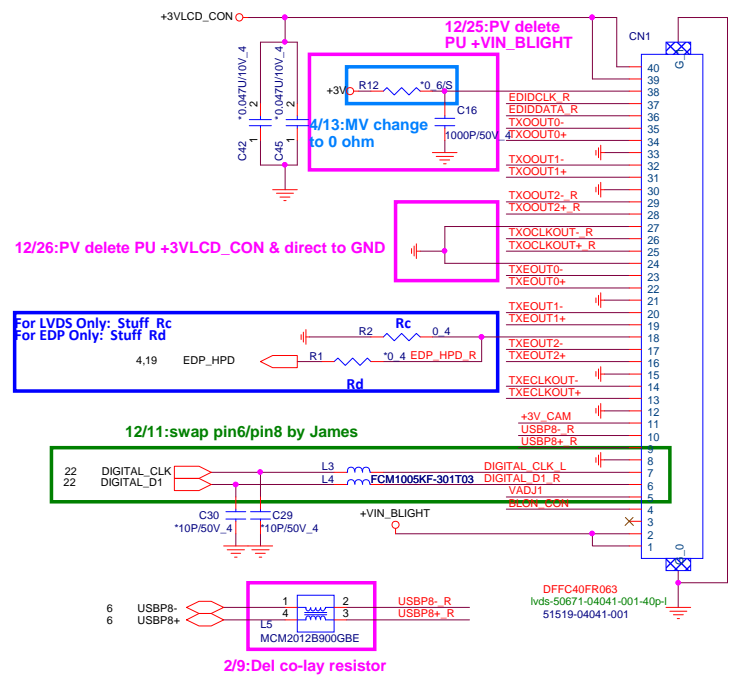
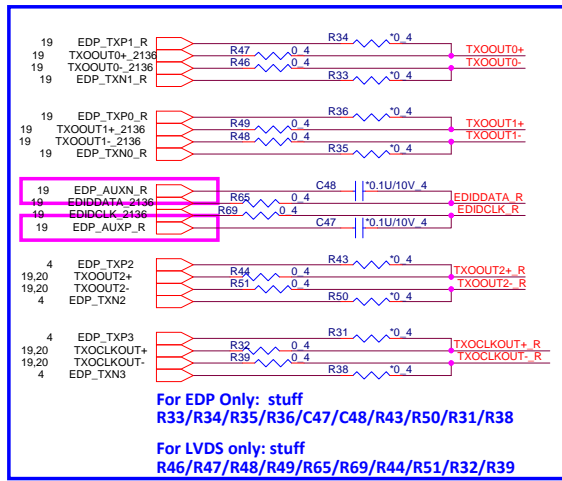
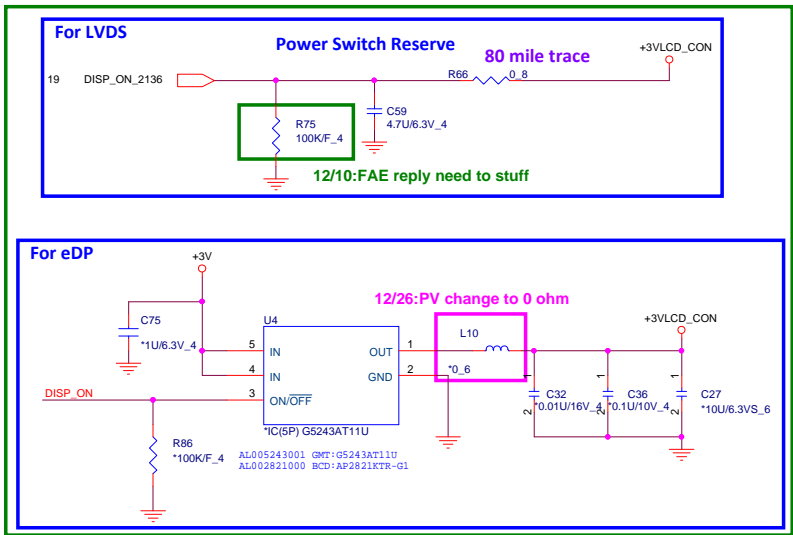
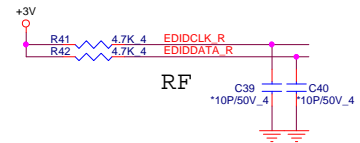
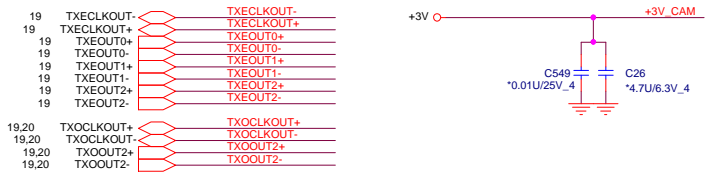
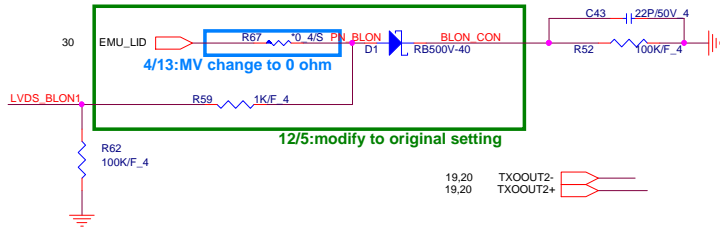


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Size Custom	Document Number	Rev 1A
LVDS converter RTD2136		
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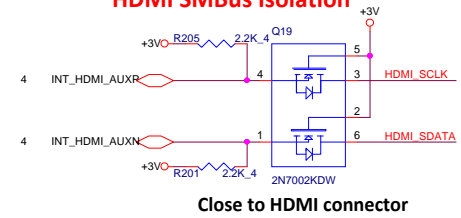


LVDS conn.



HDMI Conn.

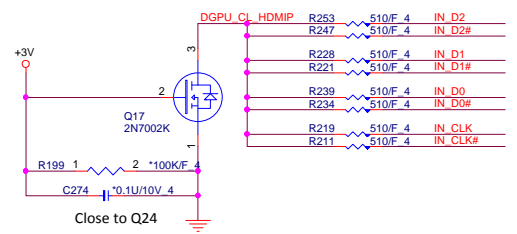
HDMI SMBus Isolation



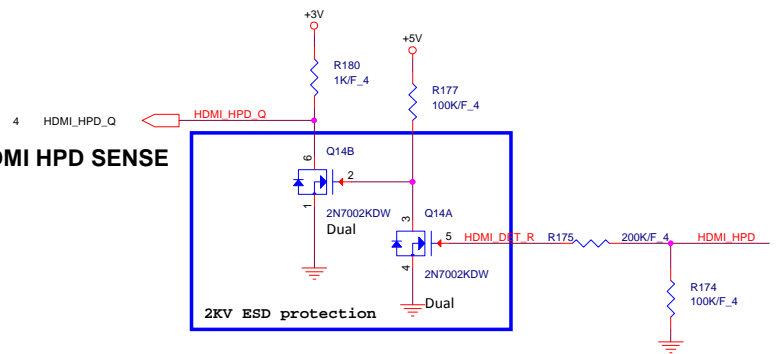
2/9:modify for HDMI fail



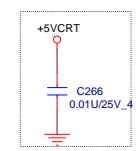
Check list recommend 604 ohm



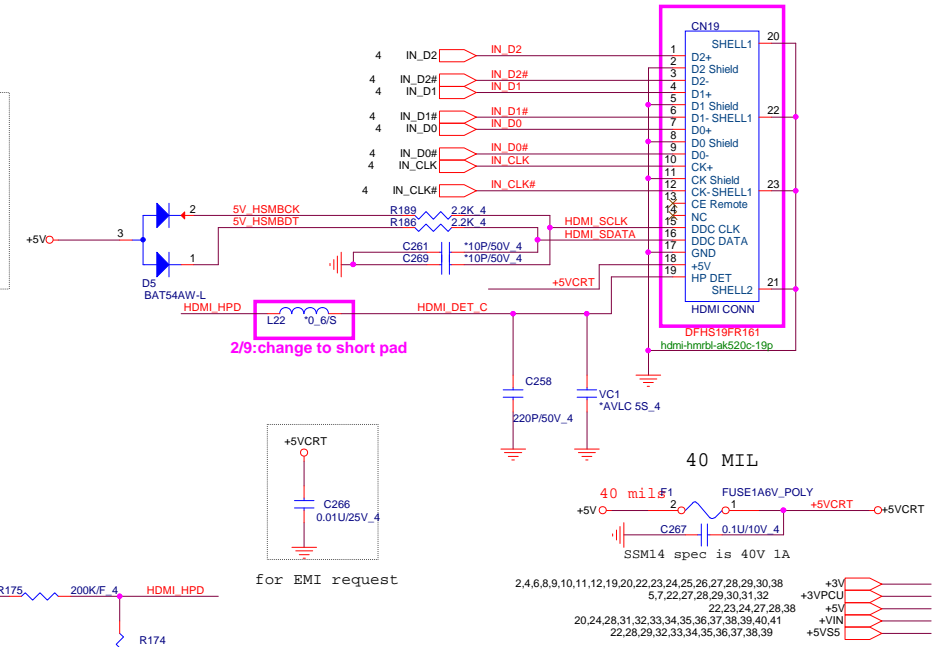
HDMI HPD SENSE



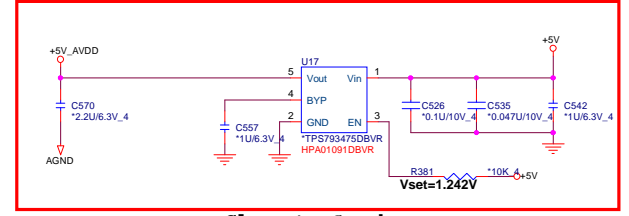
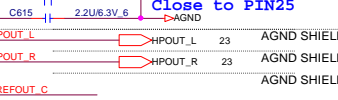
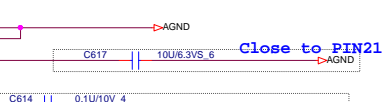
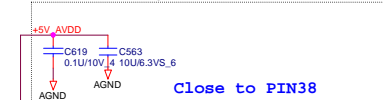
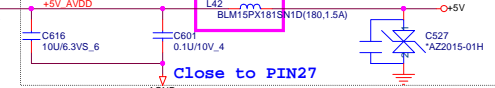
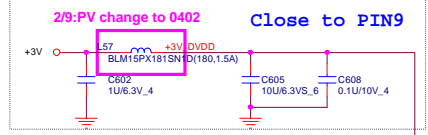
for EMI request



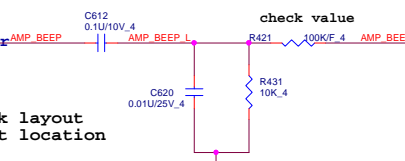
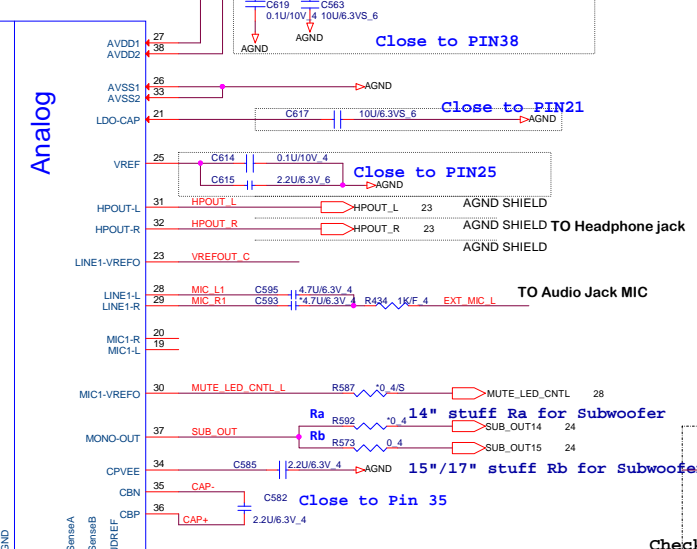
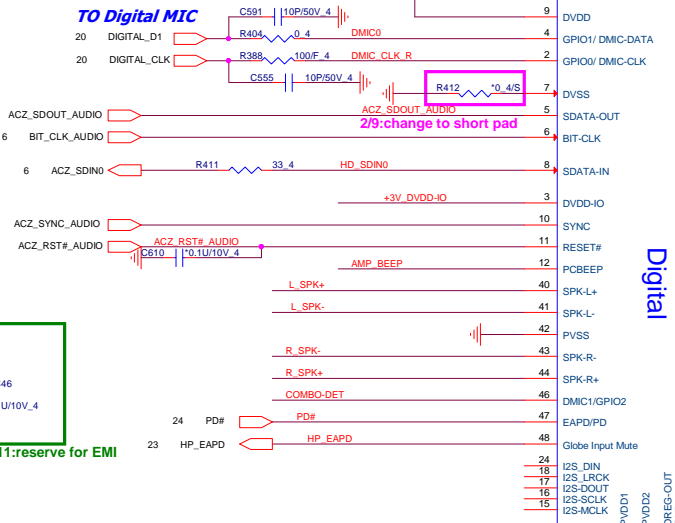
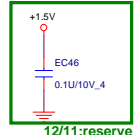
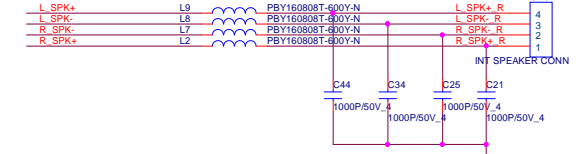
12/26:PV update footprint



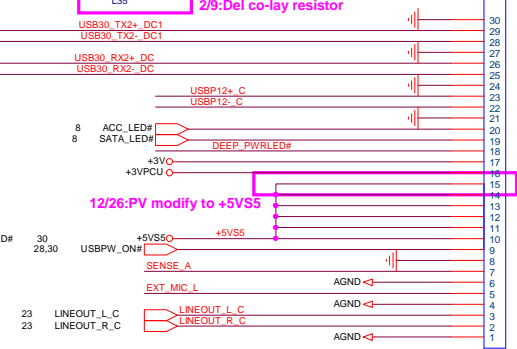
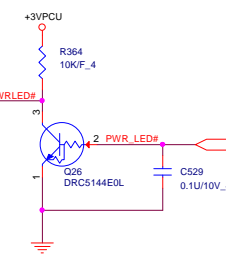
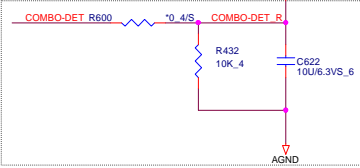
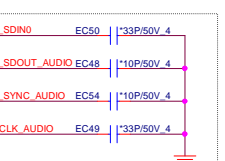
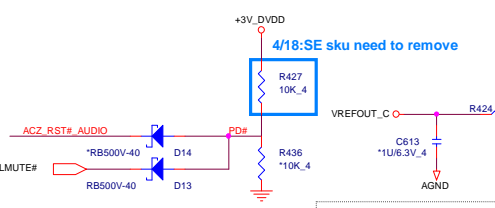
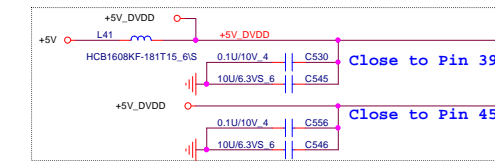
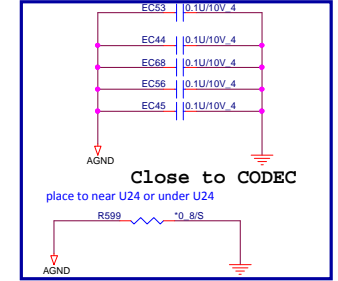
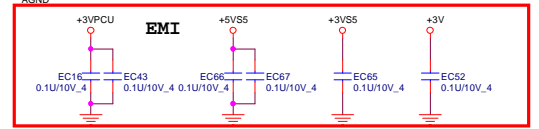
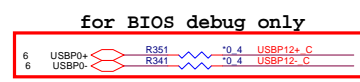
Audio Codec

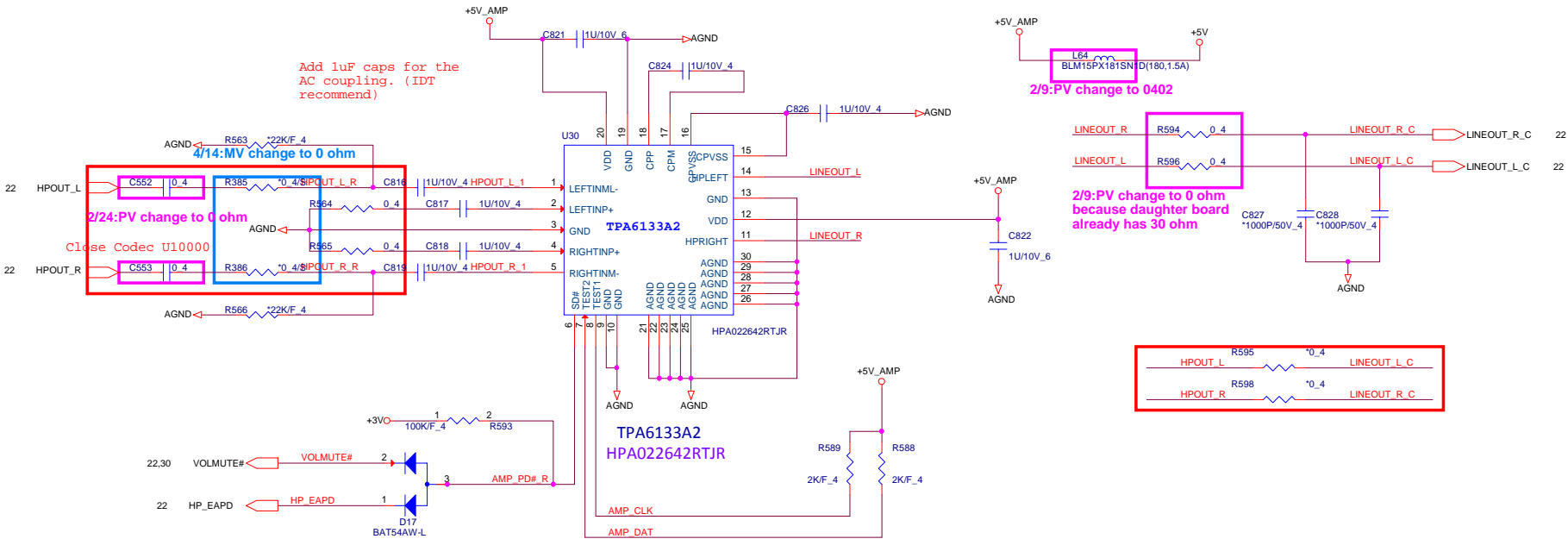


Close to Speaker
Speaker 4 ohm: 40mils

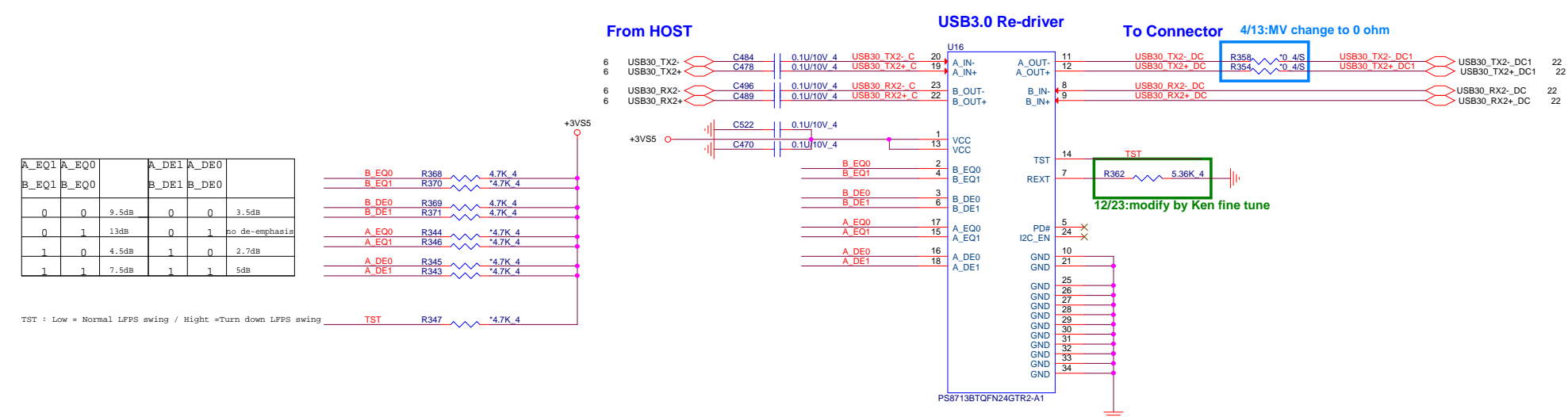


Check layout mount location





USB3.0 re-driver

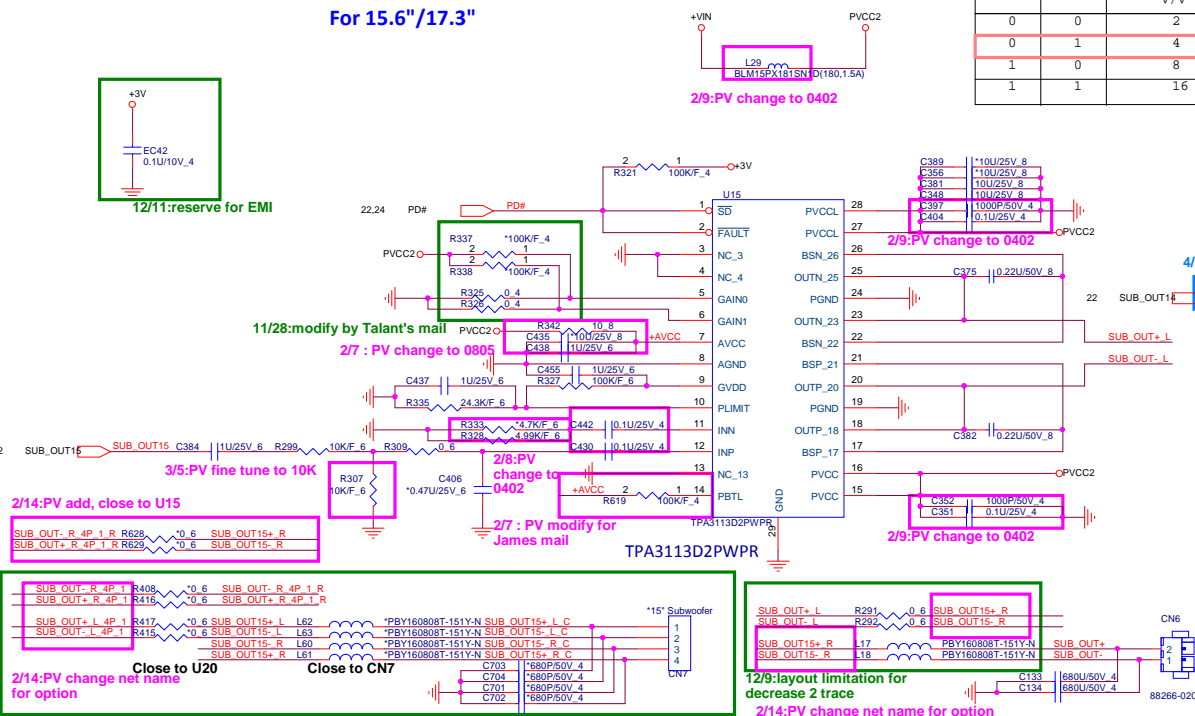


A_EQ1	A_EQ0		A_DE1	A_DE0	
B_EQ1	B_EQ0		B_DE1	B_DE0	
0	0	9.5db	0	0	3.5db
0	1	13db	0	1	no de-emphasis
1	0	4.5db	1	0	2.7db
1	1	7.5db	1	1	5db

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing

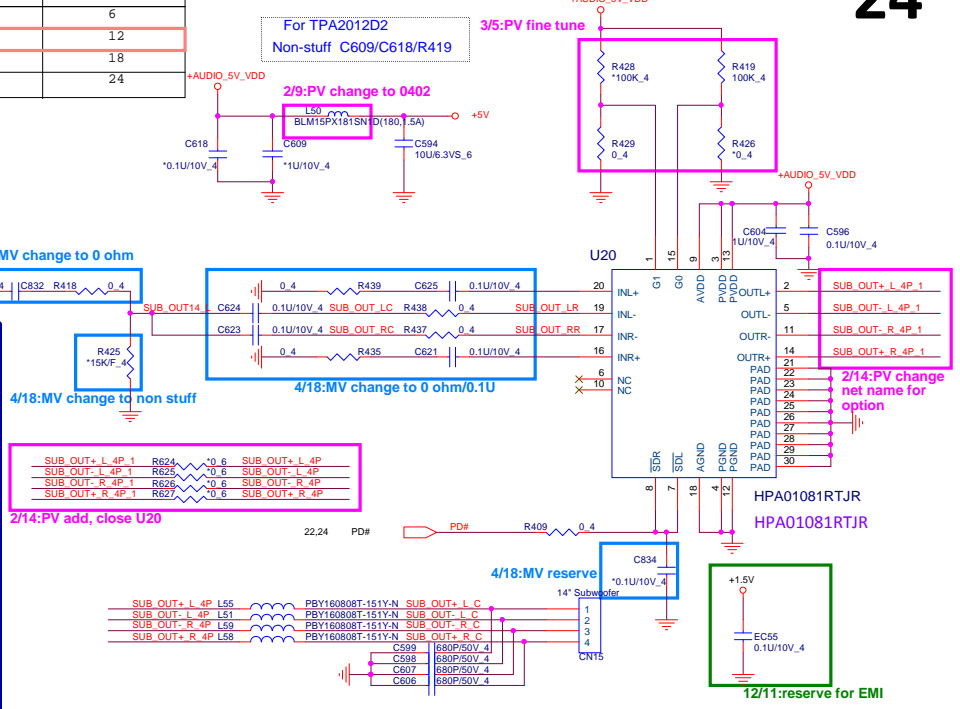
Subwoofer

For 15.6"/17.3"



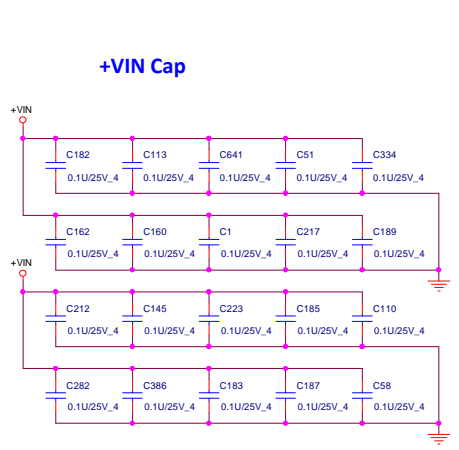
		Amplifier Gain Setting (typ)	
GAIN1	GAIN0	V/V	dB
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24

For 14.0" only

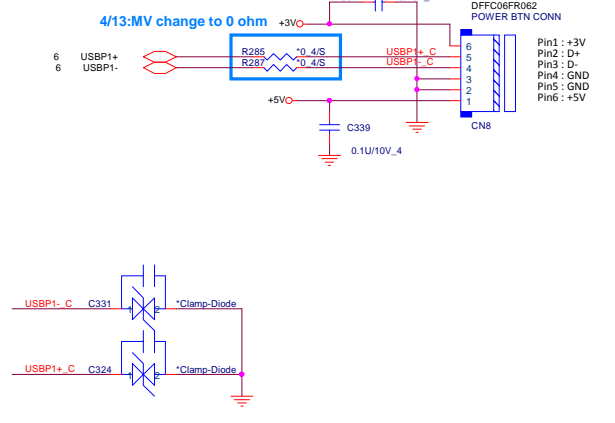


24

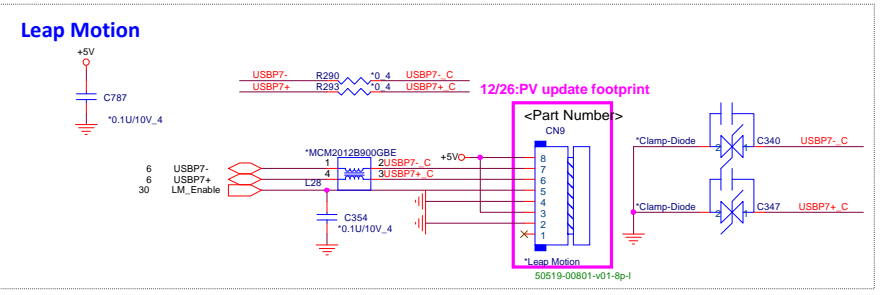
11/29:reserved 15" 4 pin subwoofer CONN



Fingerprint

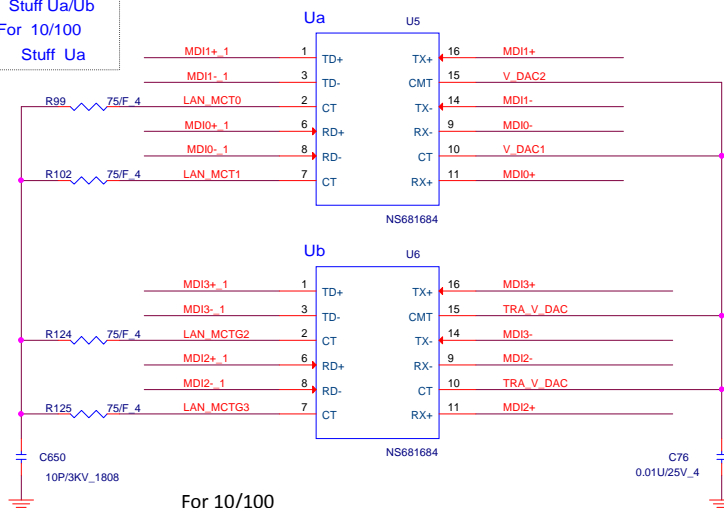
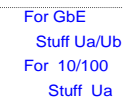
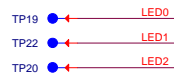


For 17" only



2,4,6,8,9,10,11,12,19,20,21,22,23,25,26,27,28,29,30,38
20,28,31,32,33,34,35,36,37,38,39,40,41

+3V
+5V
+VIN

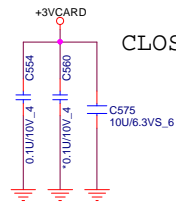
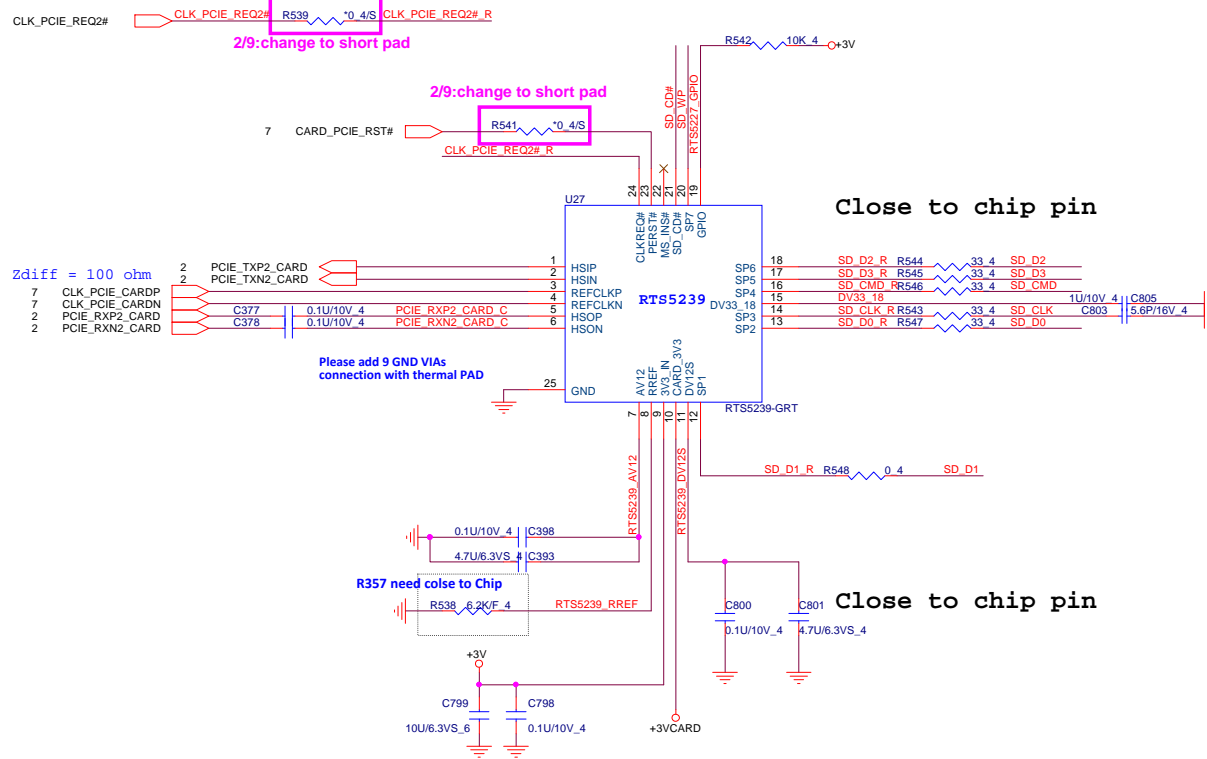


FCE :NS681684 .DB0LE6LAN20

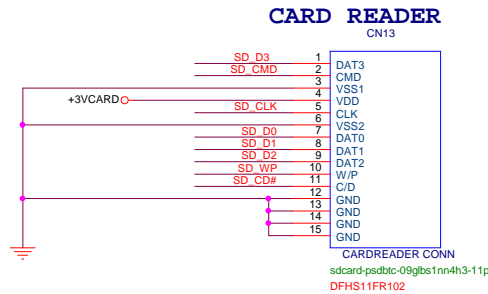


SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

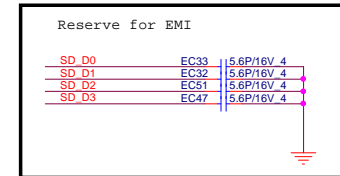
Share Pin



CLOSE CONN

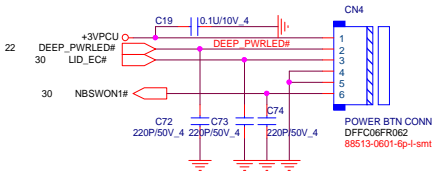


Change footprint to
sdcard-psdbtc-09g1bs1nn4h3-11p

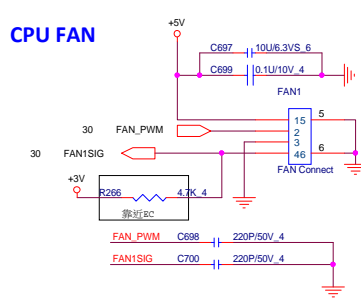


Reserve for EMI

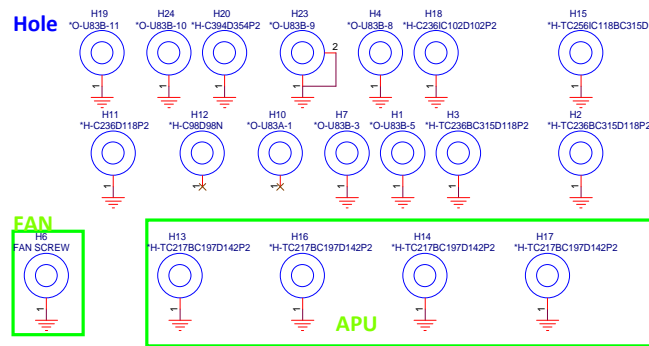
Power Button Connector



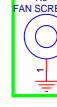
CPU FAN



Hole

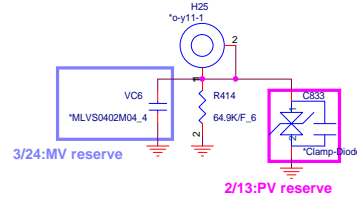
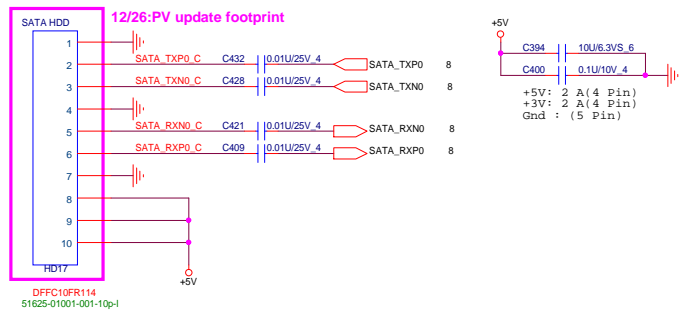


FAN

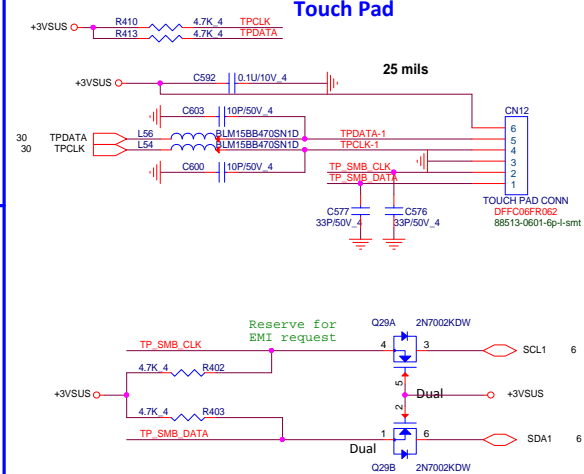


27

SATA HDD Connector(Cable type)

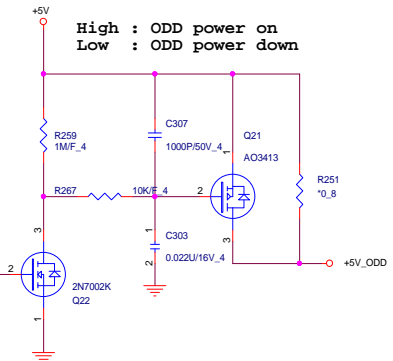
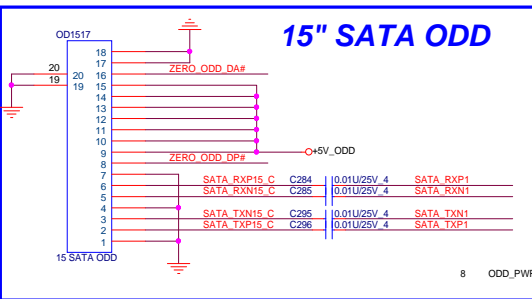
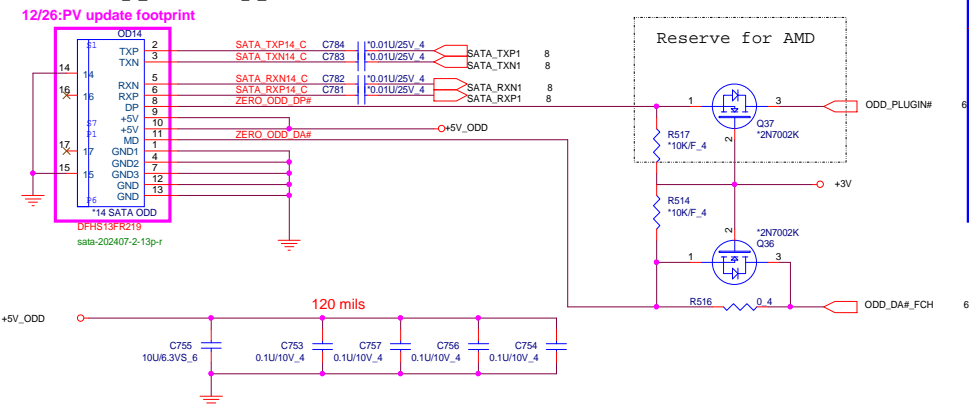


Touch Pad



SATA ODD CONNECTOR

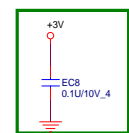
NEW Type Bypass CAP close conn



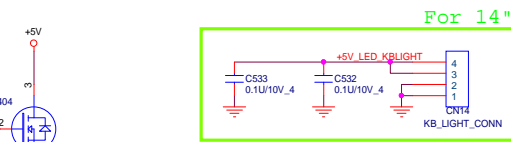
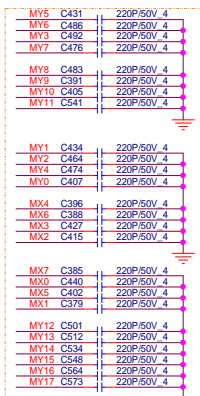
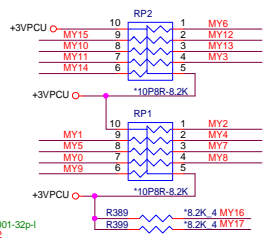
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Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/TP/FAN/HOLE/LID	1A
Date: Wednesday, April 23, 2014	Sheet 27 of 41	

KEYBOARD Con.



12/11:reserve for EMI



For 14"

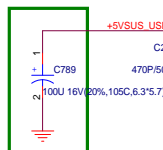
For 15"/17

USB 2.0/3.0 Combo



2/9:Del co-lay resistor

12/26:PV
update
footprint
USB 3.0

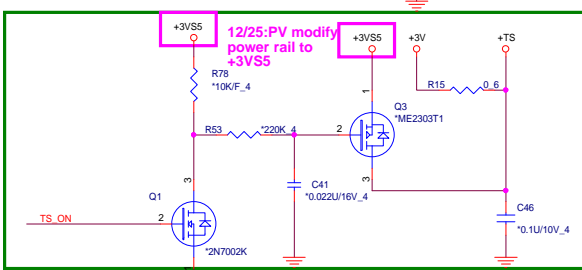


12/6:modify footprint & change to 100u

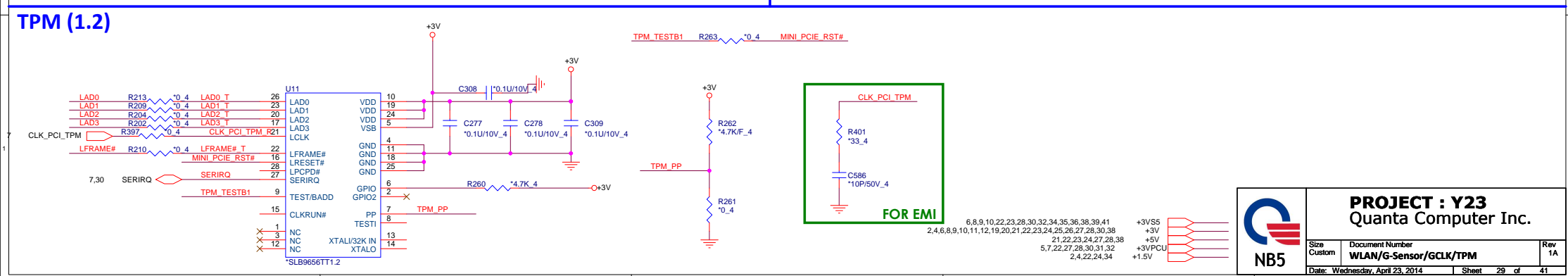
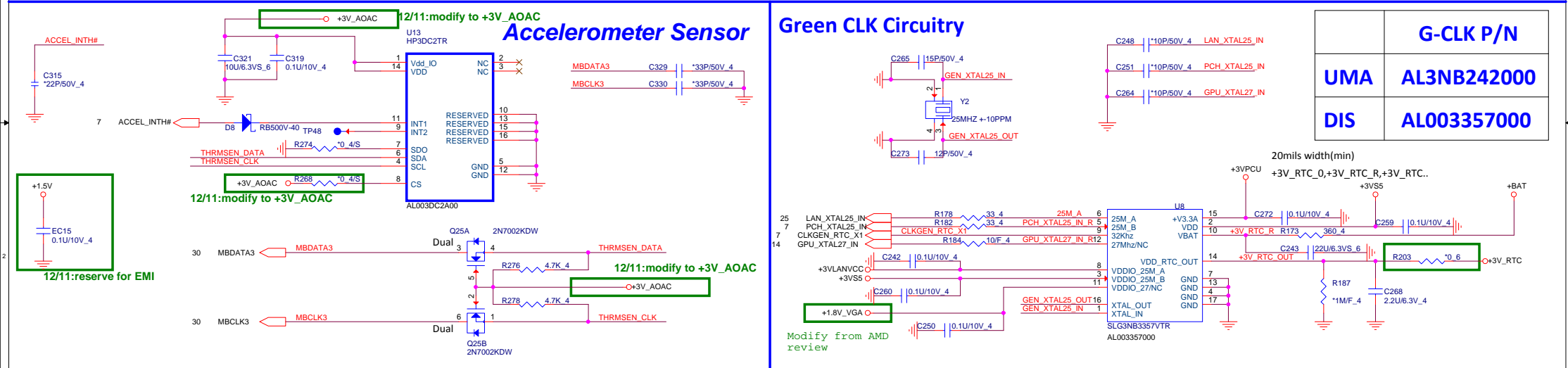
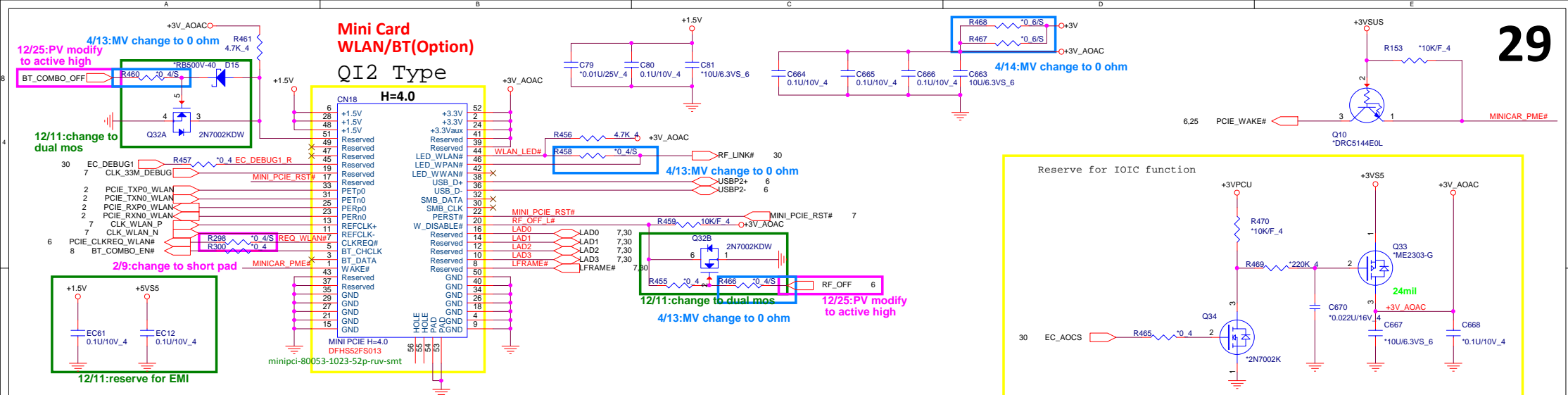
For Envy SKU stuff

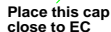
Envy	SKU	no stuff
------	-----	----------

Touch screen



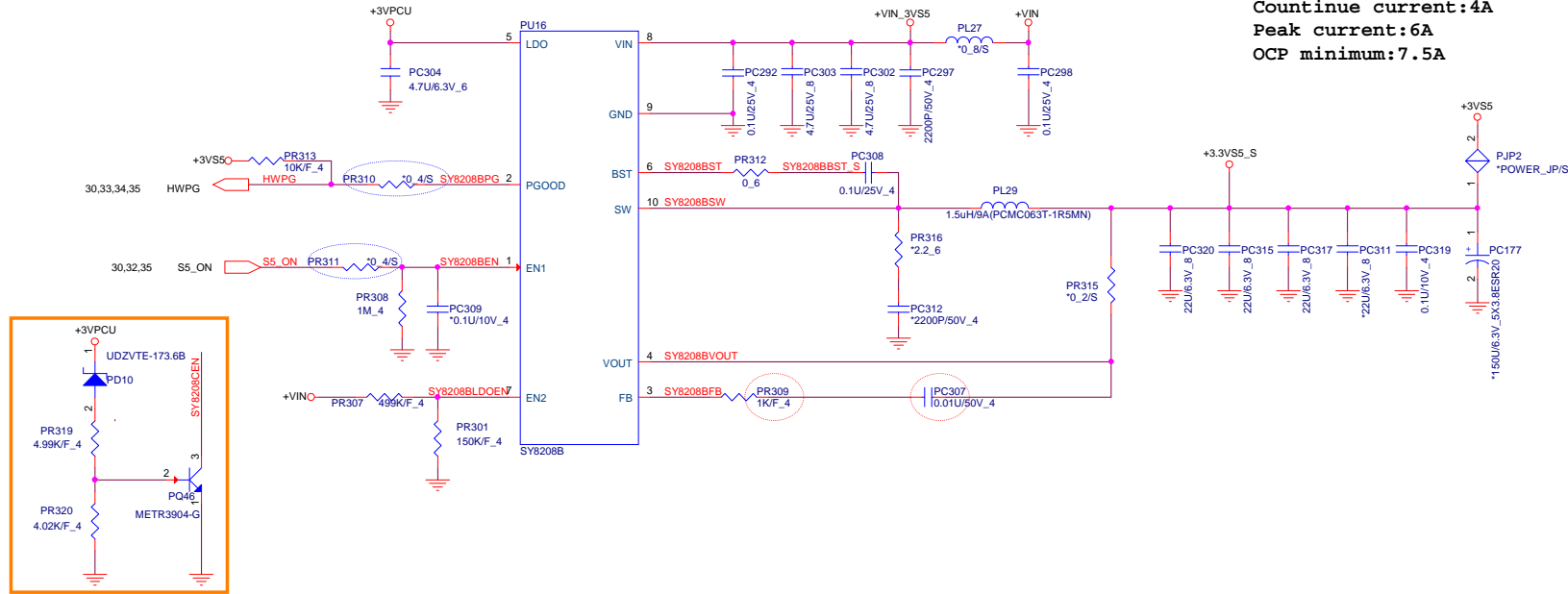
12/12:modify for cost saving





+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

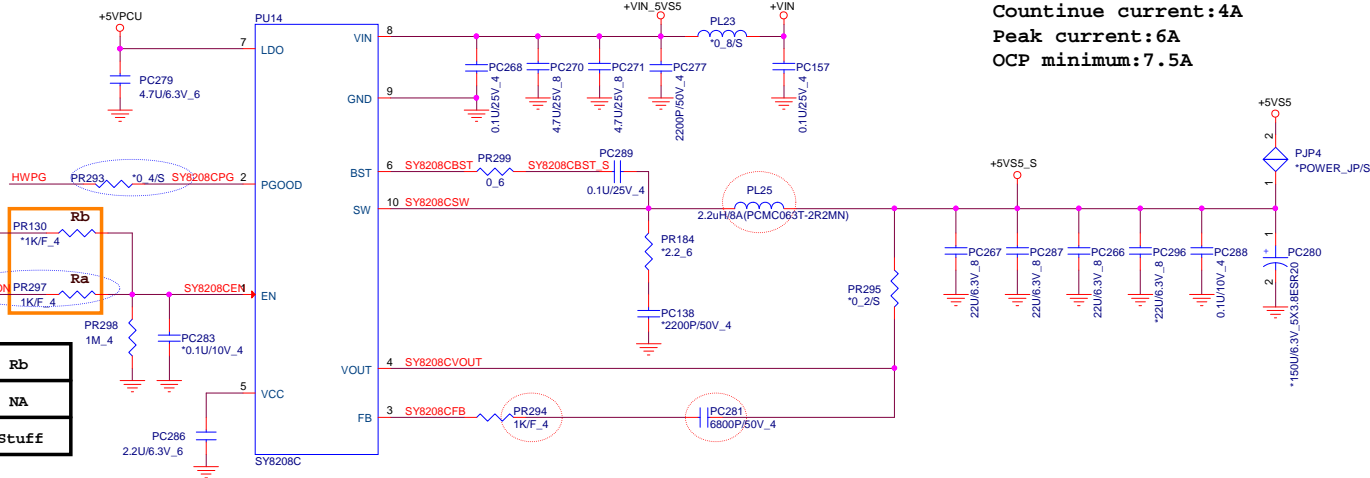
+3VS5 6,8,9,10,22,23,28,29,30,34,35,36,38,39,41
+5VS5 22,28,29,33,34,35,36,37,38,39

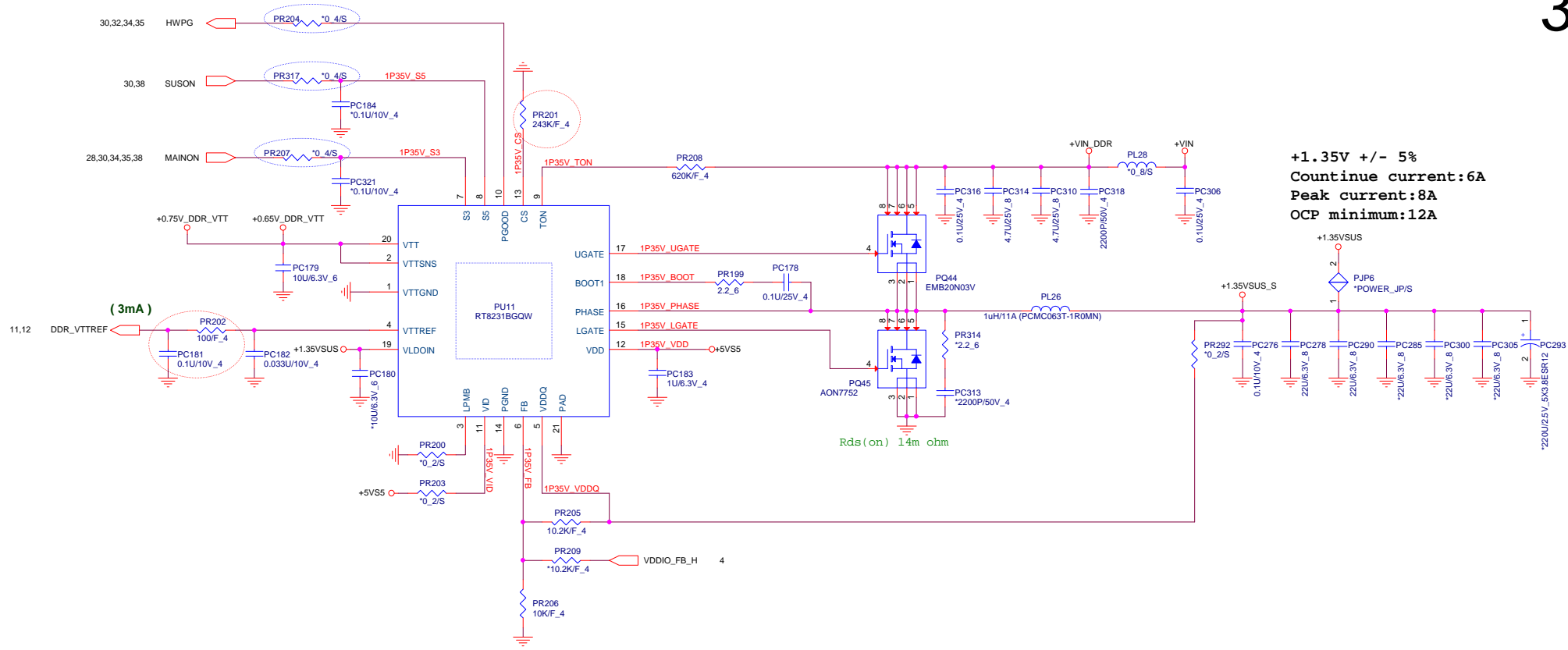


+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

Reserve for USB Charge

USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff





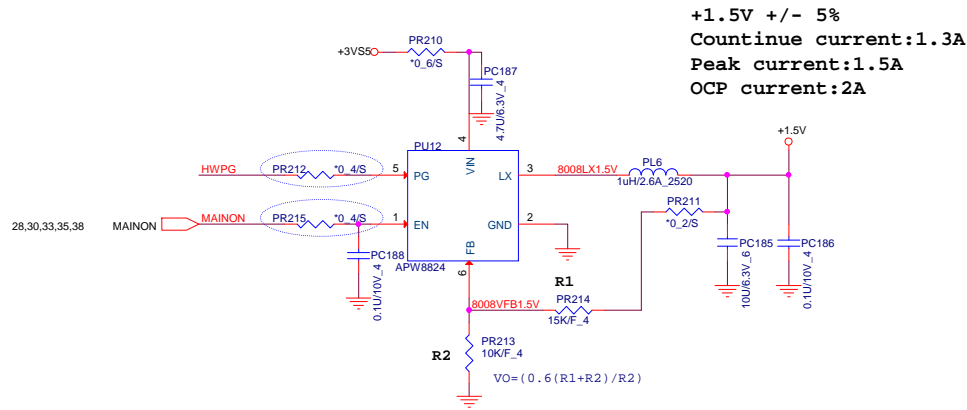
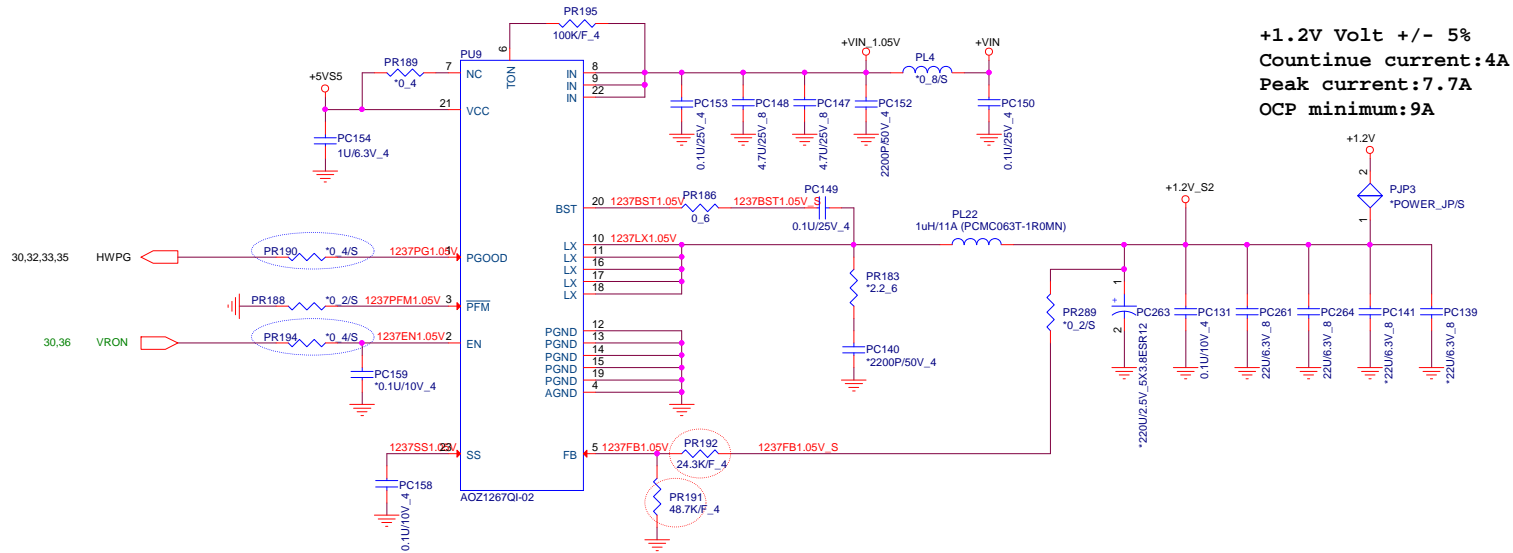
+1.35V +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

+1.35VSUS 2,3,4,5,11,12,38

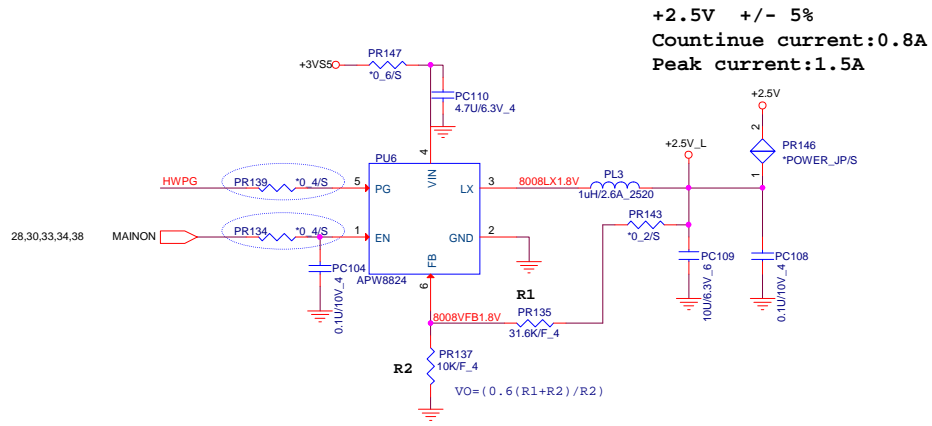
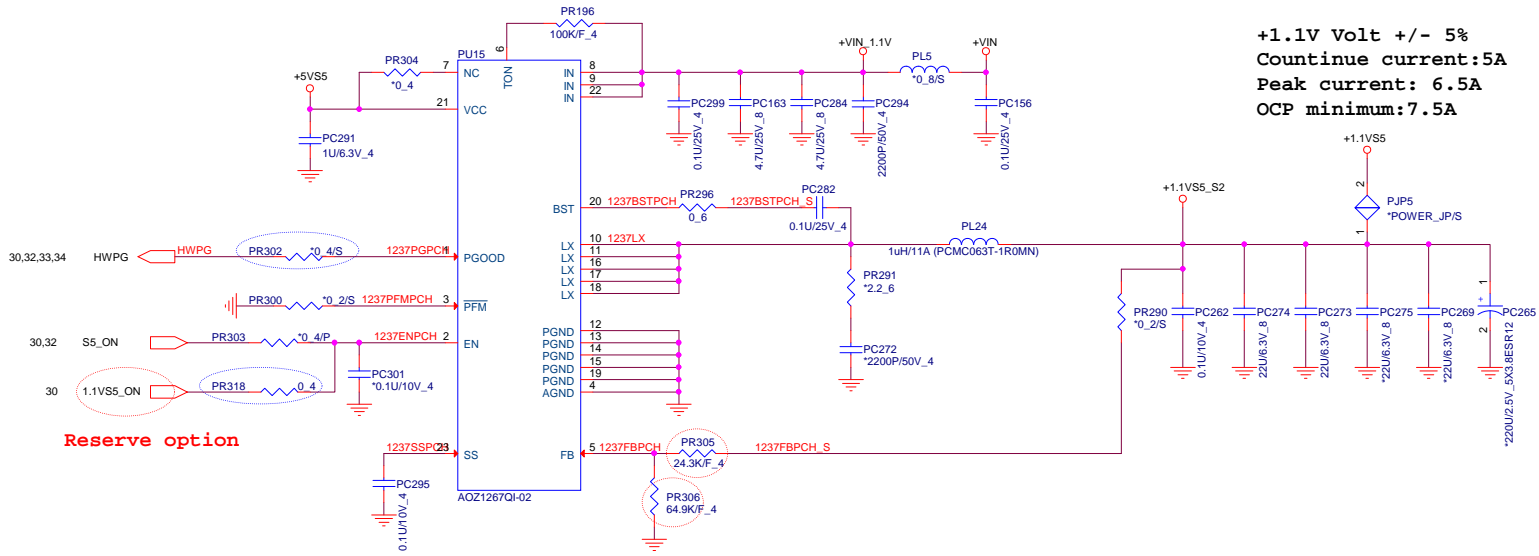


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- +VIN 20,24,28,31,32,33,35,36,37,38,39,40,41
- +3VS5 6,8,9,10,22,23,28,29,30,32,35,36,38,39,41
- +5VS5 22,28,29,32,33,35,36,37,38,39
- +5VPCU 31,32

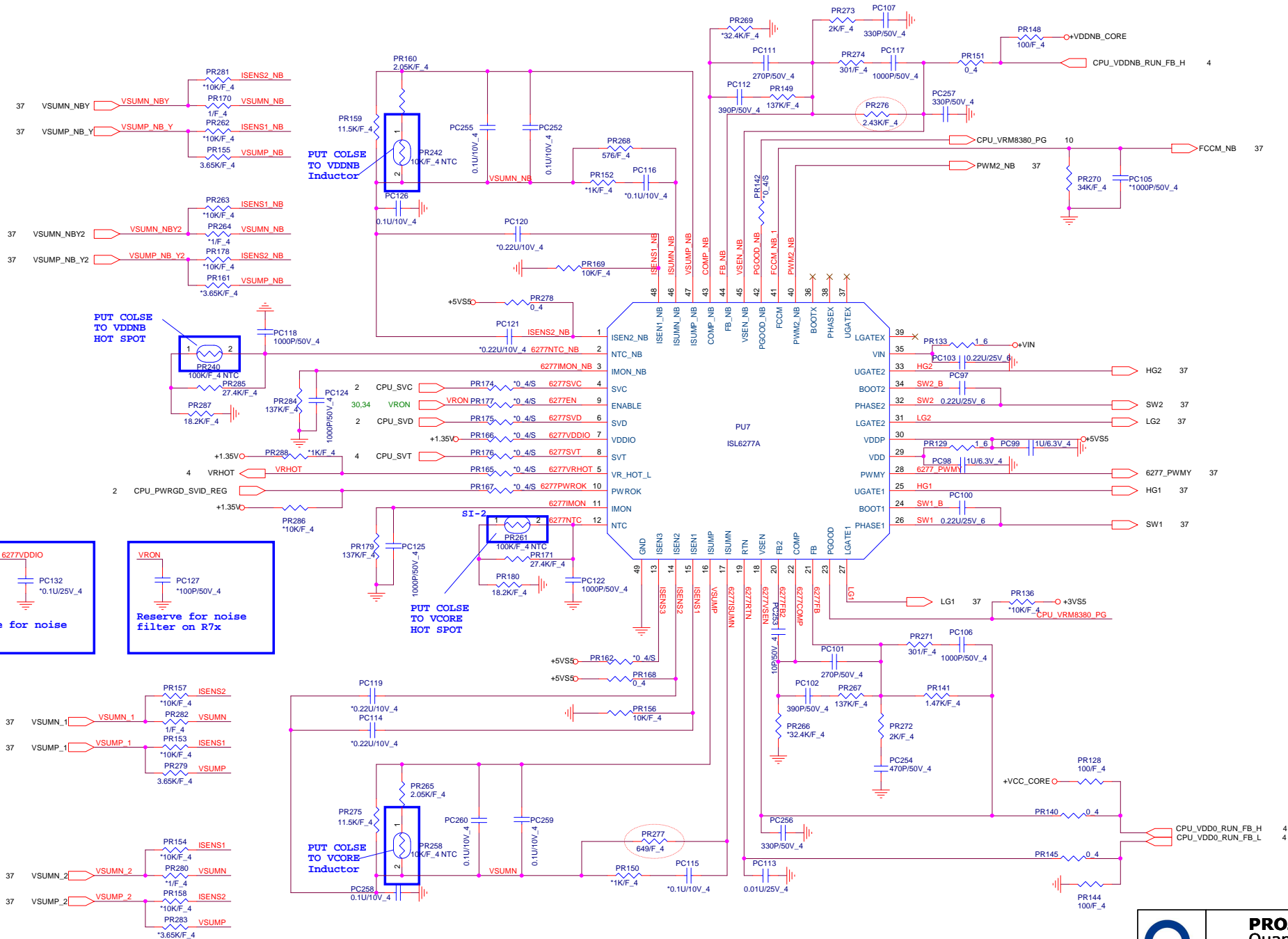


+VIN	20,24,28,31,32,33,34,36,37,38,39,40,41
+3VS5	6,8,9,10,22,23,28,29,30,32,34,36,38,39
+5VS5	22,28,29,32,33,34,36,37,38,39
+1.1VS5	9,38
+5VPCU	31,32

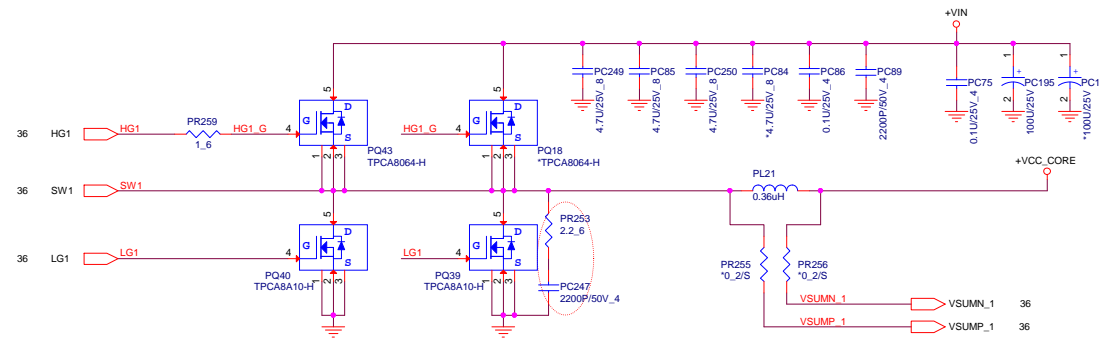


PROJECT : Y23
Quanta Computer Inc.

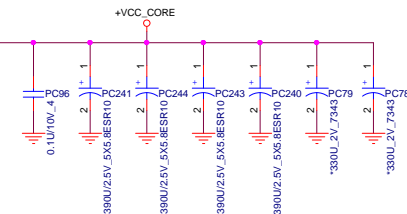
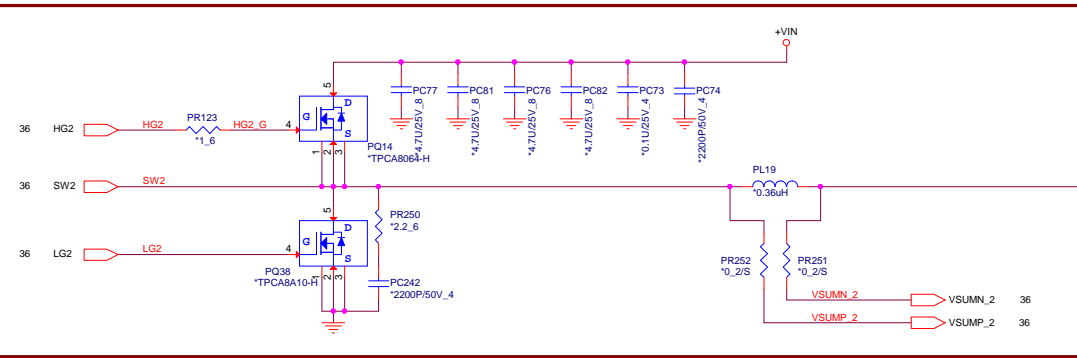
Size Custom	Document Number +1.1VS5 (AOZ1267)/2.5V	Rev 1A
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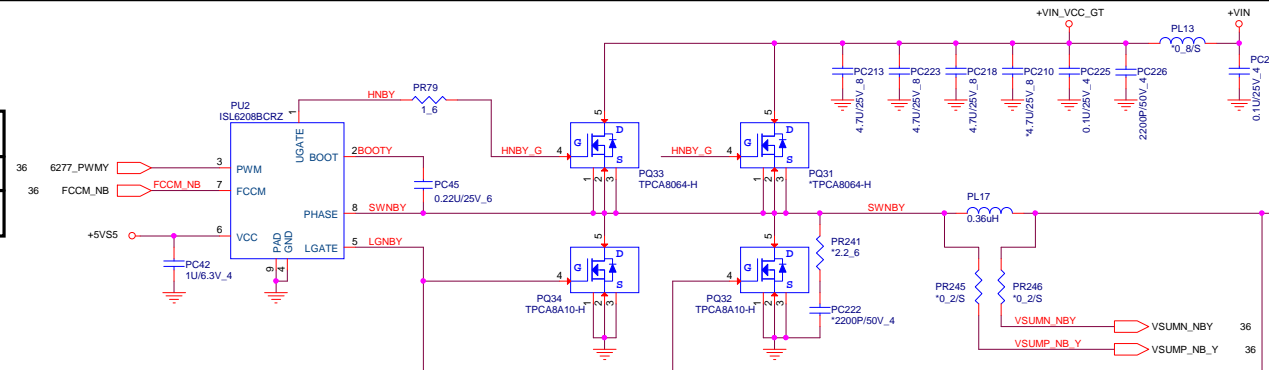
CPU TYPE	MOSFET
25W	1H2L/1phase
19W	1H1L/1phase



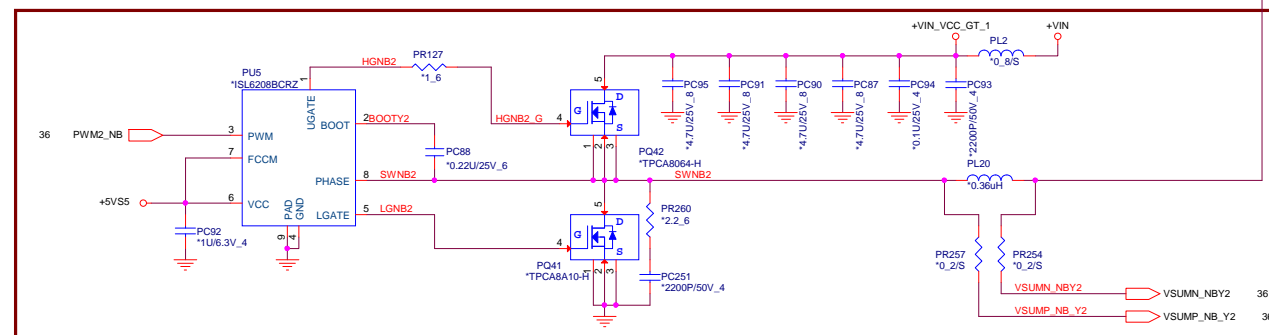
CPU CORE Volt (25W)
Countinue current:20A
Peak current:34A
OCP minimum:39A

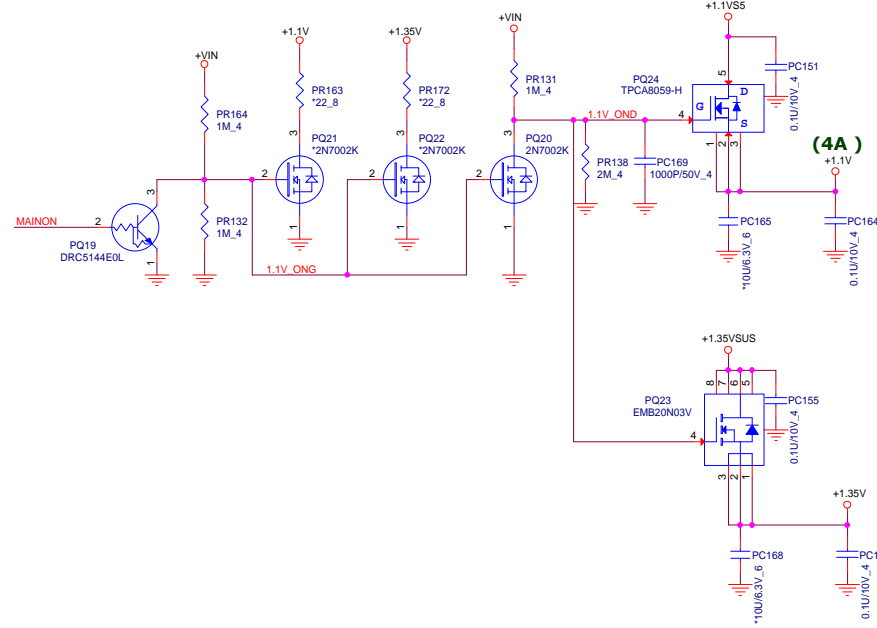
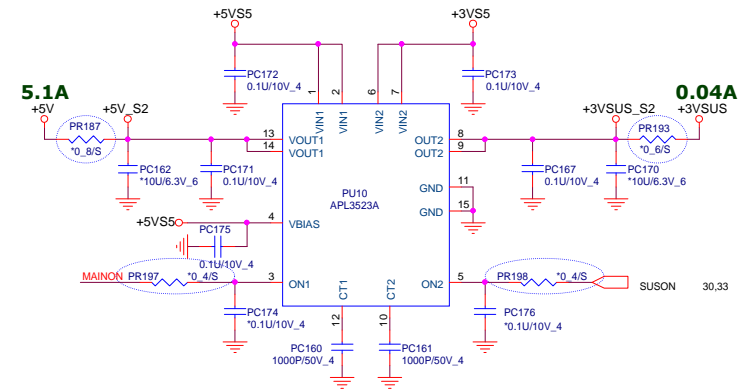
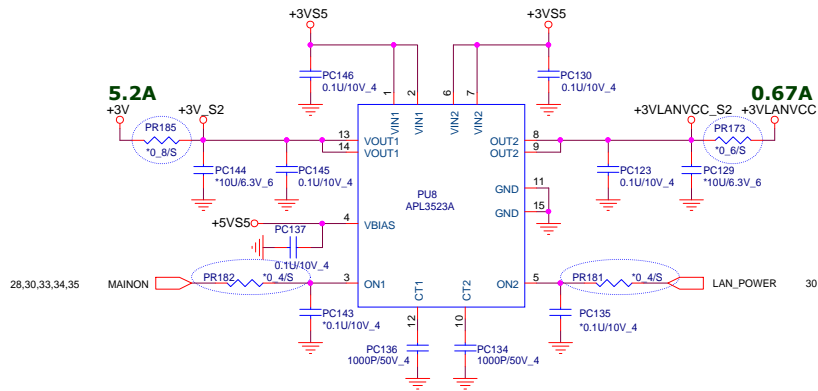


CPU TYPE	MOSFET
25W	1H2L/1phase
19W	1H1L/1phase



VDDNB Volt
Countinue current:14.1A
Peak current:24.1A
OCP minimum:37A





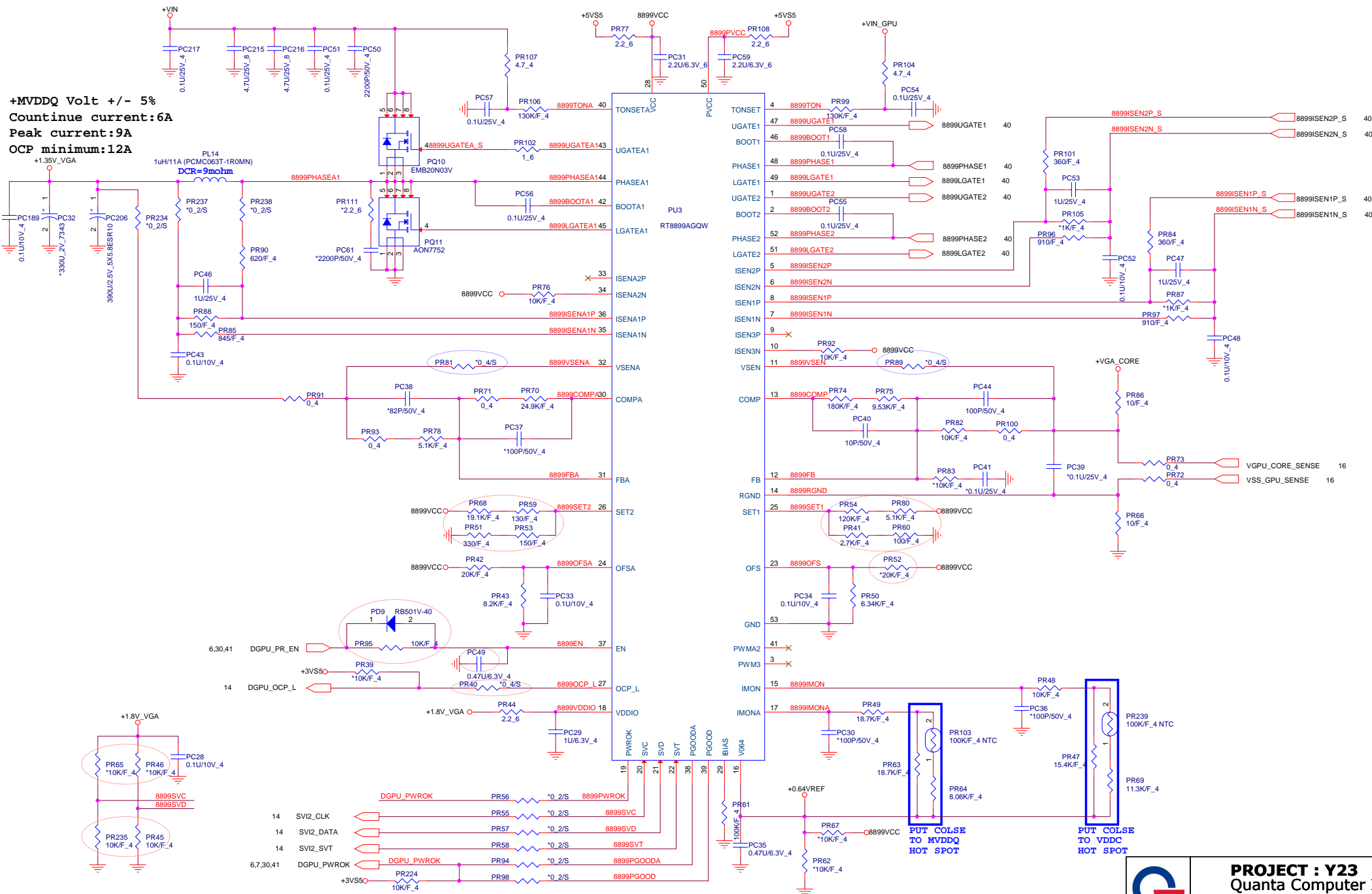
2,4,6,8,9,10,11,12,19,20,21,22,23,24,25,26,27,28,29,30 +3V
21,22,23,24,27,28 +5V
20,24,28,31,32,33,34,35,36,37,39,40,41 +VIN
6,8,9,10,22,23,28,29,30,32,34,35,36,39,41 +3VS5
22,28,29,32,33,34,35,36,37,39 +3VLANVCC
25,29



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Quanta Computer Inc.

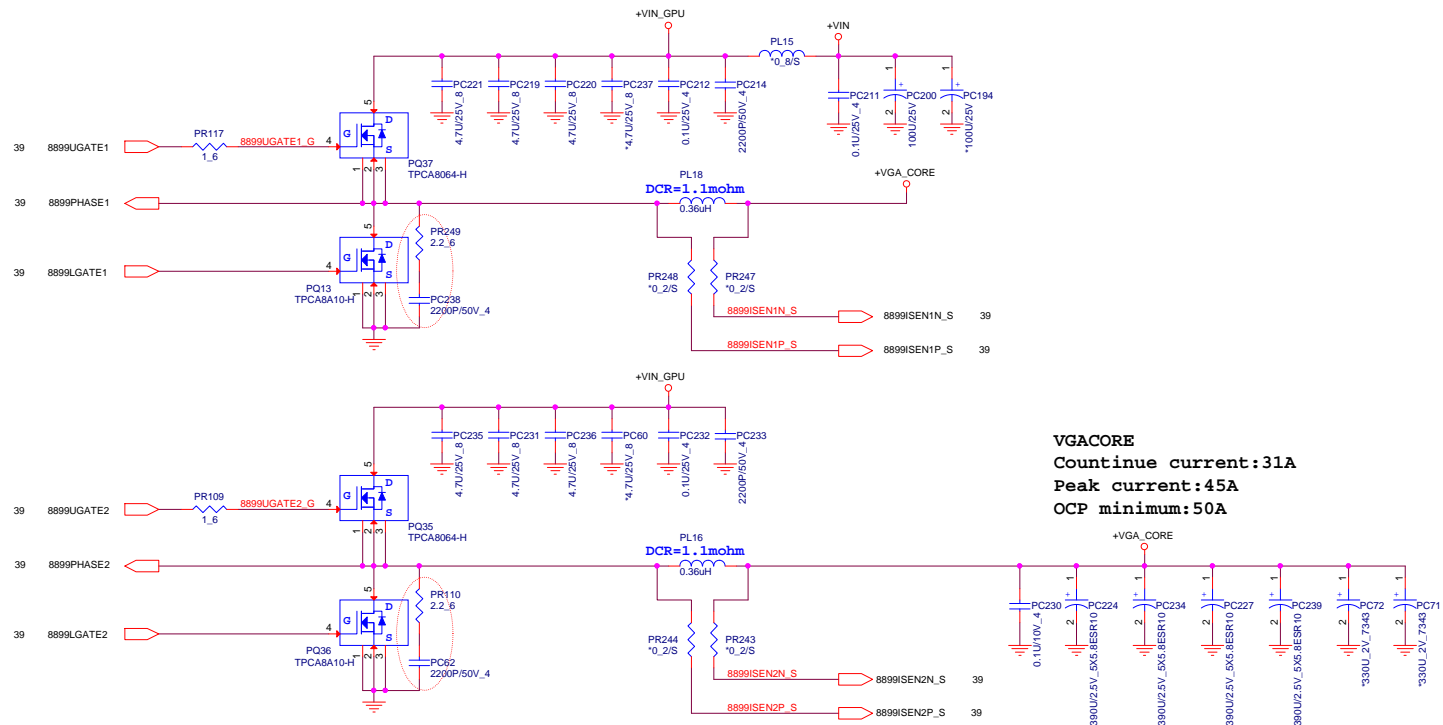
Size Custom	Document Number Dis-charge IC (SLG55448)	Rev 1A
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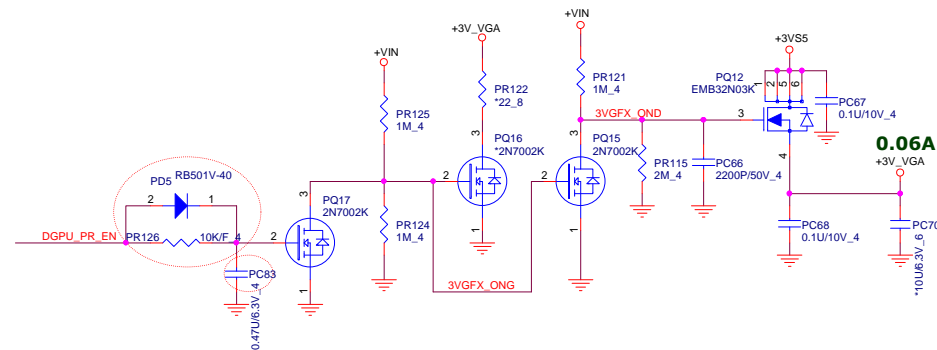
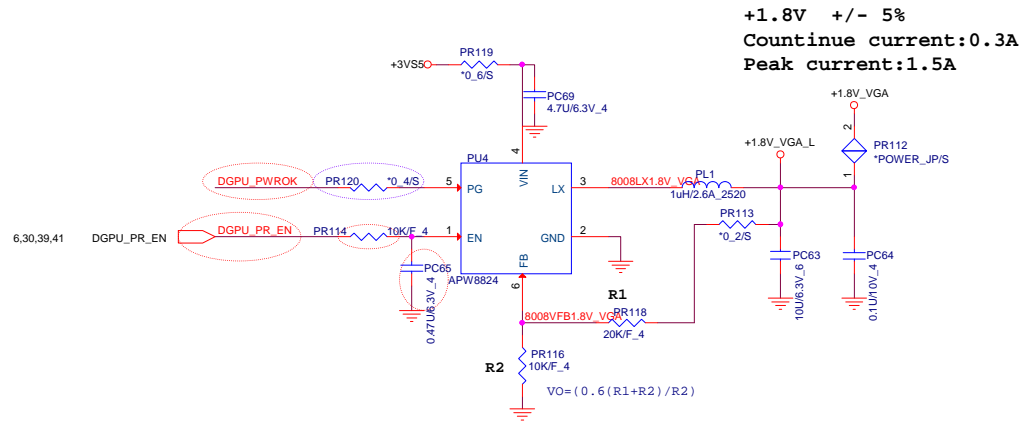
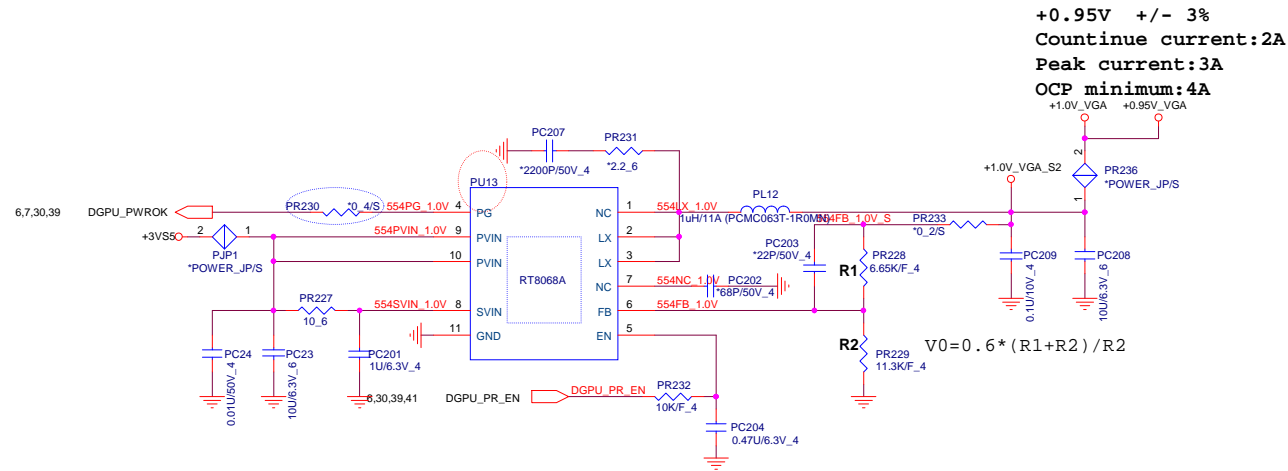
+MVDDQ Volt +/- 5%
Countinue current:6A
Peak current:9A
OCP minimum:12A



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Quanta Computer Inc.

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+3V_VGA 13,14,16,30
 +1.0V_VGA 13,16
 +1.8V_VGA 13,14,16,29,39