X570 UD

Revision : 1.0

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2015.12.30--B.L

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Model Name:X570 UD

Component value change history

Version: 1.0

P-Code: U98126-0

Date	Change Item	Reason
2019/05/31	first release	
	9MX57UD-00-01 BOM	
2019/07/09	9MX57UD-00-10A BOM	
	1.QFR8->X,QFR17上件 2.PM_HS->12SF2-S11013-21R /22R	
	, RMOS->12SP2-S08823-21R / 22R , TMOS->12SP2-S11233-21R / 22R	
	3.MCU1->X 4.M_BIOS Scoket->X 5.WIFI 不上件	
	6.DU1->10TA1-669147-04R,DAJP->X 7.110A->10KS2-040131-02R	

Circuit or PCB layout change for next version

Date	Change Item	Reason
2019/05/28 PCB:0.1	1.PCB first release	
	2.線路由X570 Gaming X Rev1.0修改	
2019/07/05 PCB:1.0	1.文字面Rev0.1 -> 1.0	
	2.Add DC15 , AC9 3.Del IO_1,IO_2	

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Title	BOM & PCB HISTORY	
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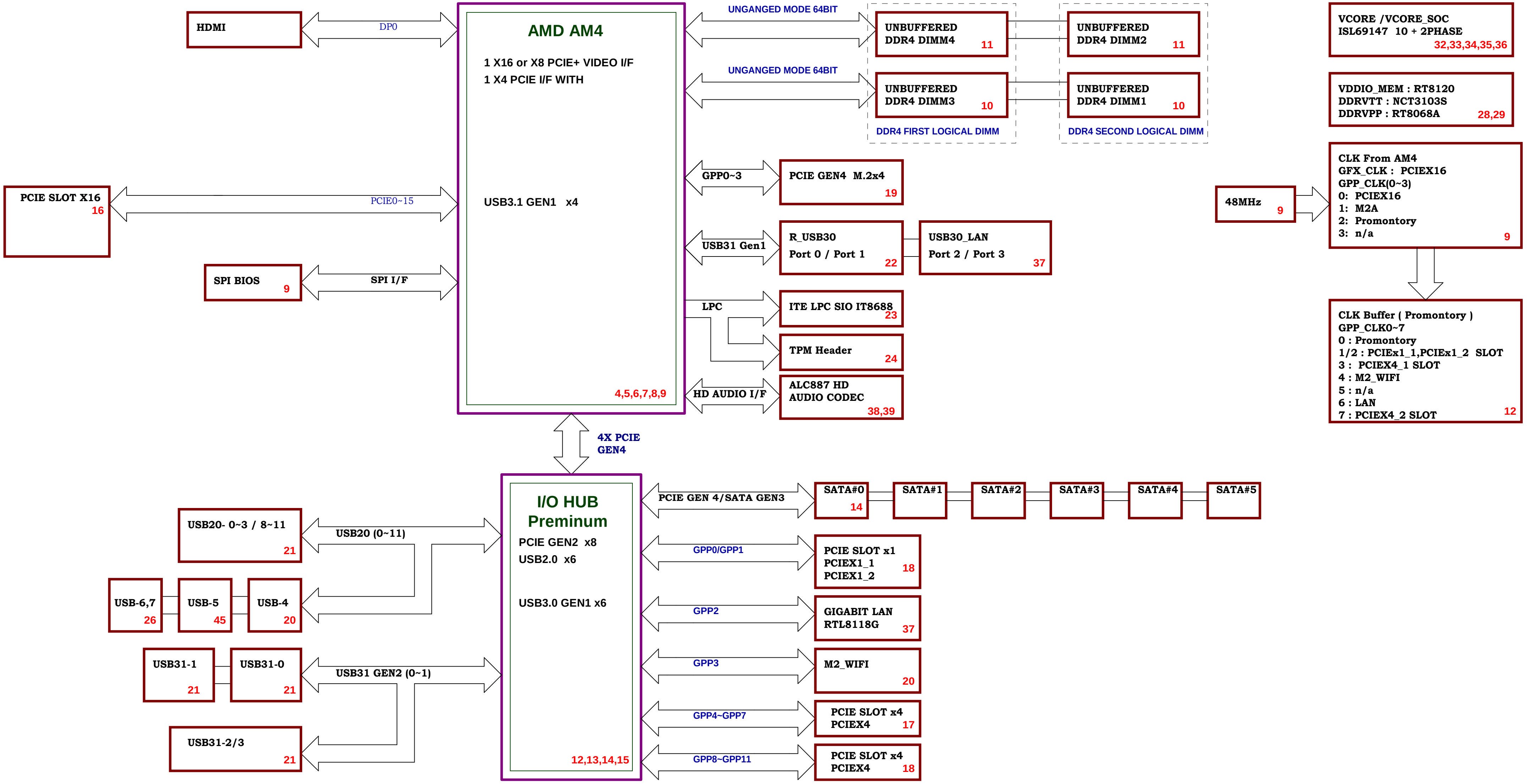

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Title
BLOCK DIAGRAM

Size	Document Number	Rev
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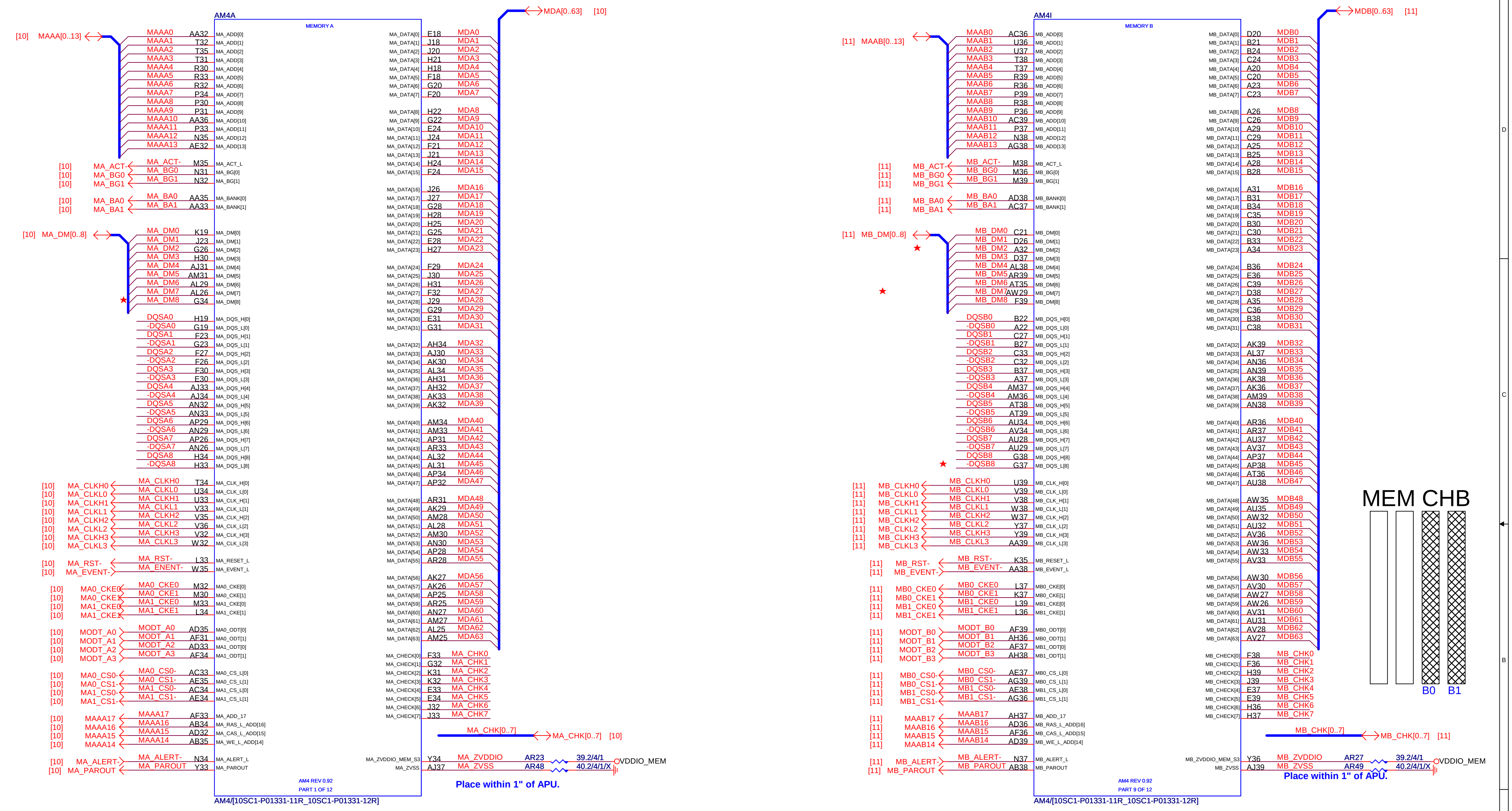

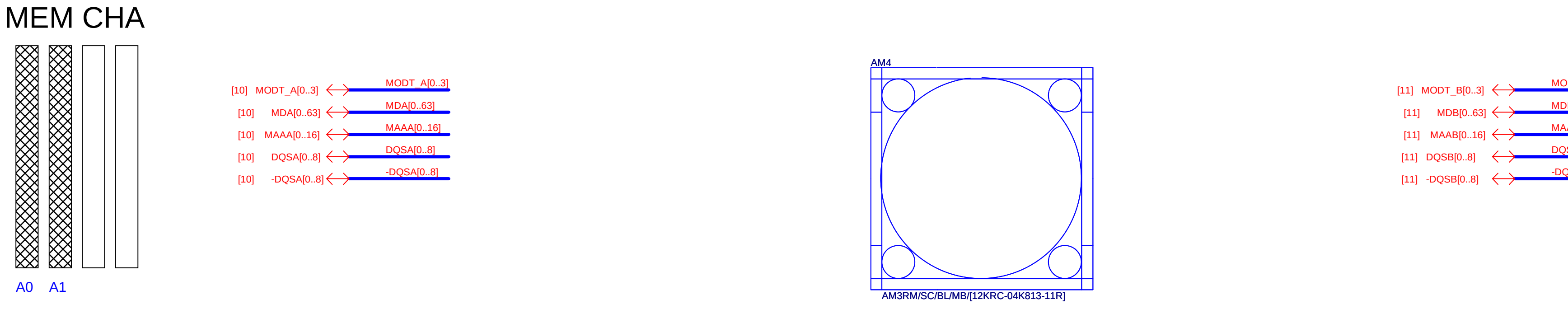

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Title
APU DDR4

Size: Custom
Document Number: **X570 UD**
Rev: **1.0**

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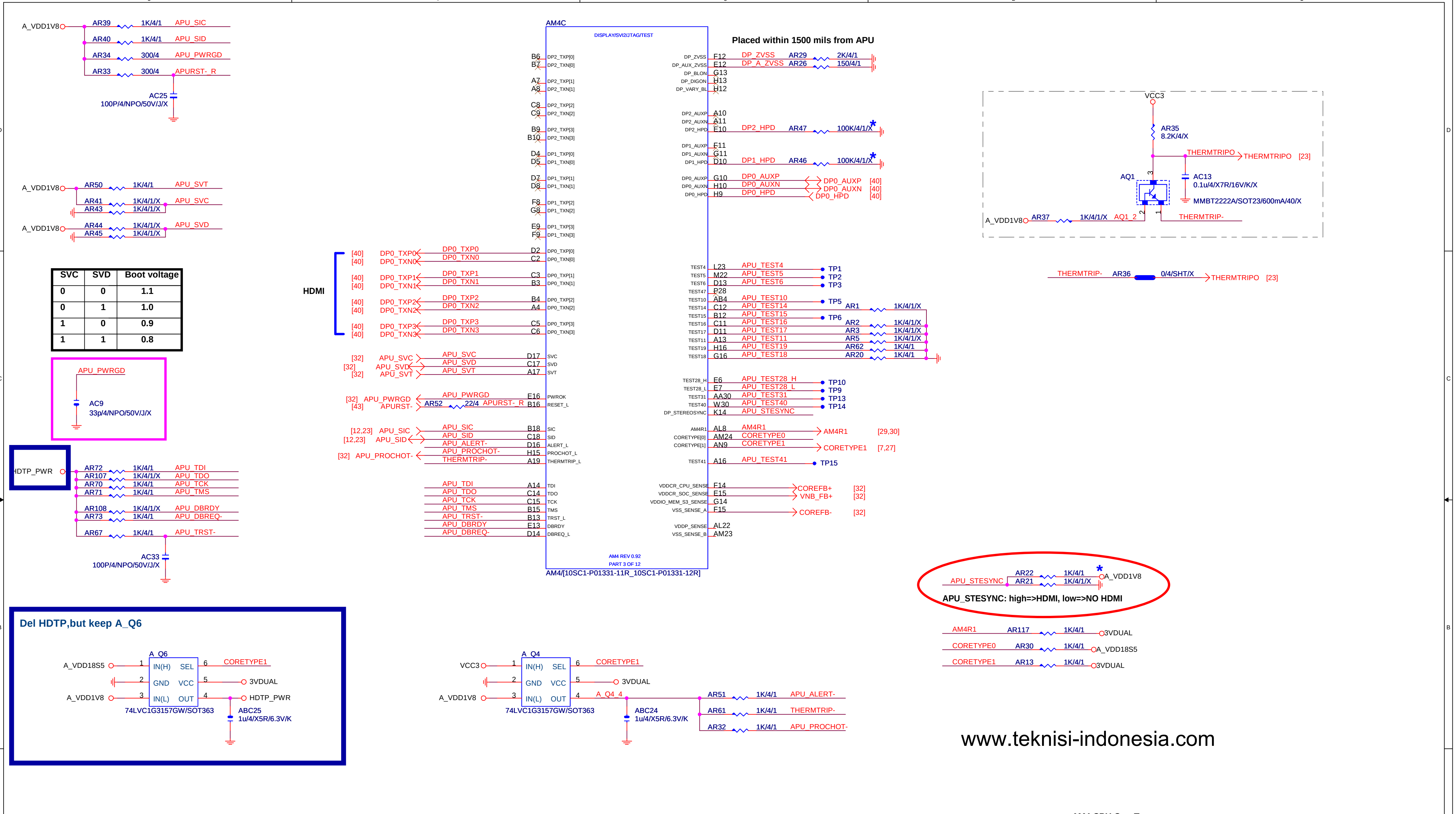

SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

AM4 CPU CoreType

CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h- 6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h- 0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h- 1 Fh	TYPE 3

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Title
CPU CONTROL
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Title
AM4_PCIE LINK, GND

Size Custom
Document Number **X570 UD**
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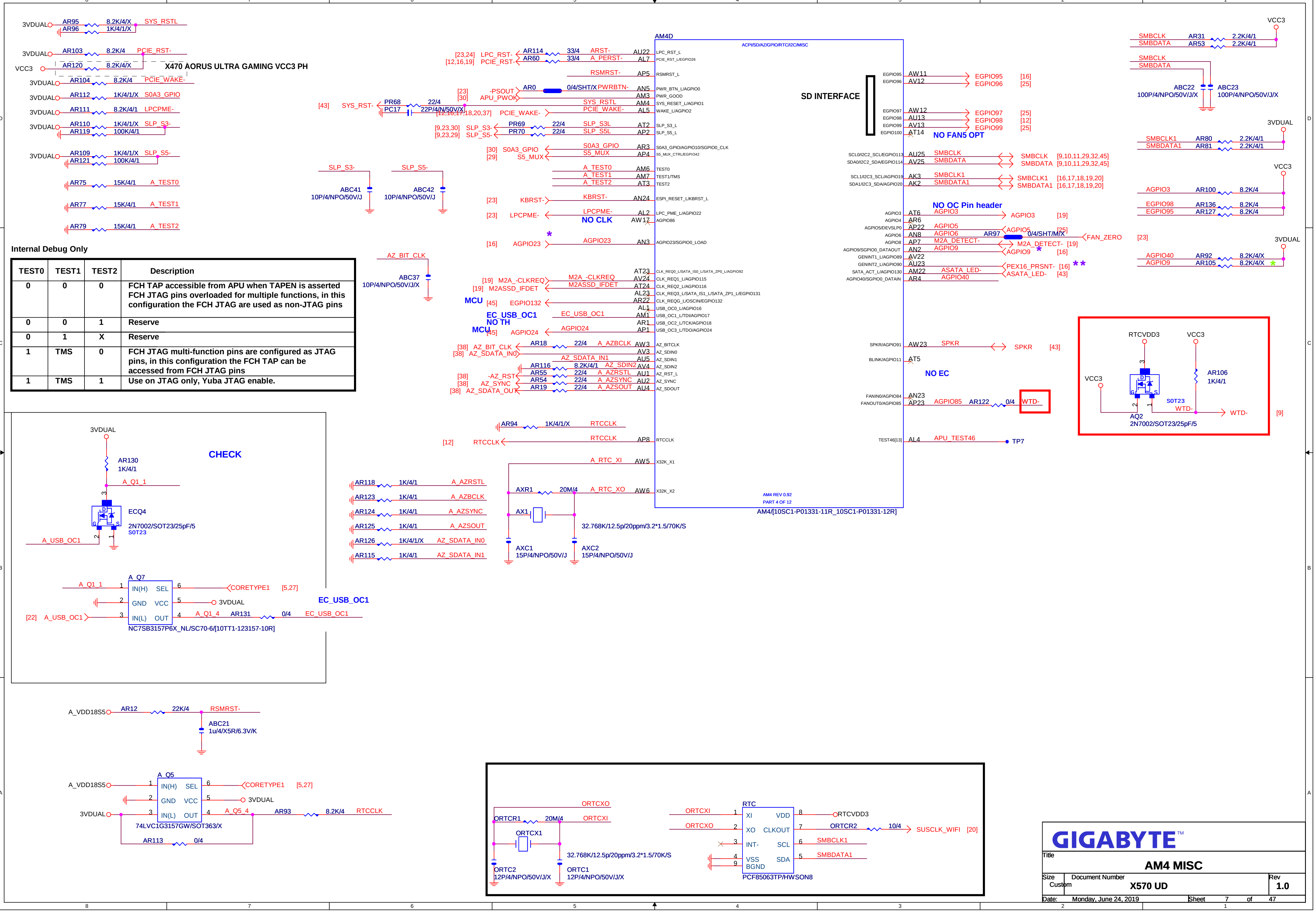

Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP can be accessed from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

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Title
AM4 MISC

Size Custom
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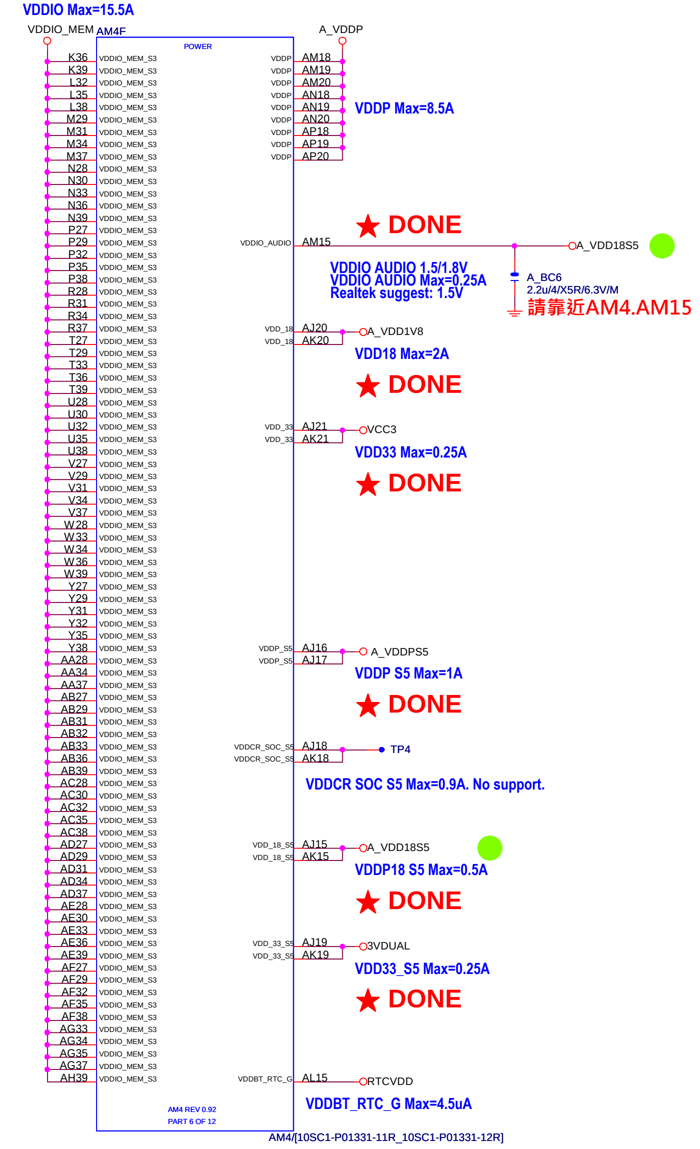
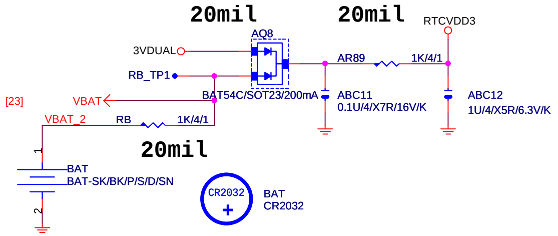
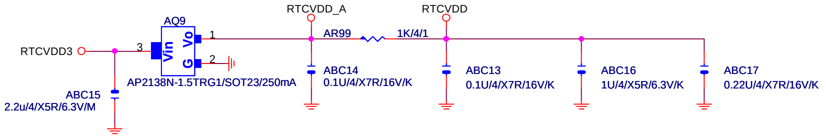


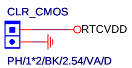
AM4 1.5V, 250mA (A_V15S5)
A_Q1 改接A_VDD18S5 for VDDIO_AUDIO

For STR FAIL ISSUE

`VDDCR_SOC_S5 -->N/A`







CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

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Title
CPU POWER & GND

Size: Custom
Document Number: X570 UD
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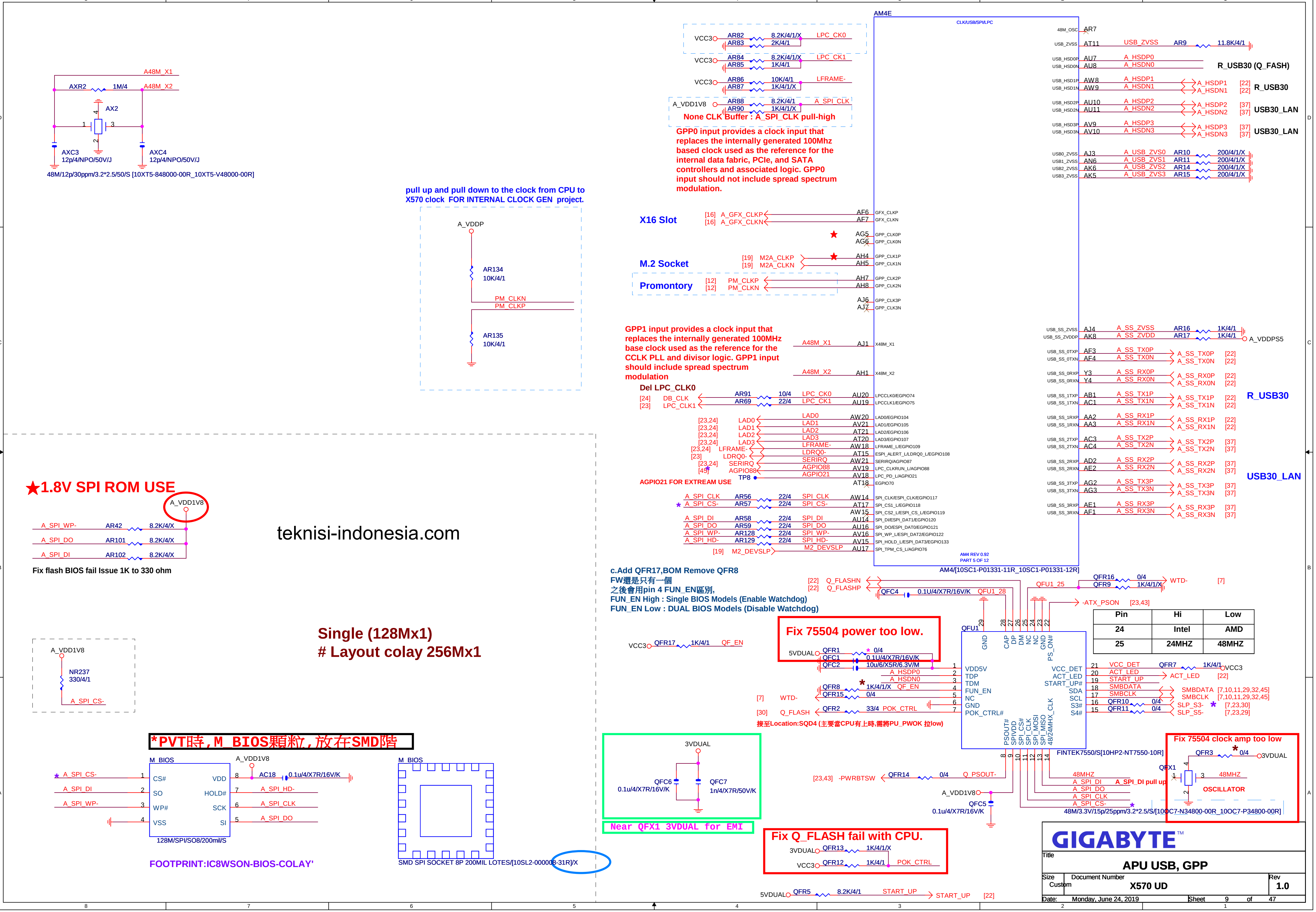

None CLK Buffer : A_SPI_CLK pull-high

GPP0 input provides a clock input that replaces the internally generated 100Mhz based clock used as the reference for the internal data fabric, PCIe, and SATA controllers and associated logic. GPP0 input should not include spread spectrum modulation.

pull up and pull down to the clock from CPU to X570 clock FOR INTERNAL CLOCK GEN project.

GPP1 input provides a clock input that replaces the internally generated 100MHz base clock used as the reference for the CCLK PLL and divisor logic. GPP1 input should include spread spectrum modulation

Del LPC_CLK0

AGPIO21 FOR EXTREAM USE

Fix flash BIOS fail Issue 1K to 330 ohm

teknisi-indonesia.com

c.Add QFR17,BOM Remove QFR8
FW還是只有一個
之後會用pin 4 FUN_EN區別,
FUN_EN High : Single BIOS Models (Enable Watchdog)
FUN_EN Low : DUAL BIOS Models (Disable Watchdog)

Pin	Hi	Low
24	Intel	AMD
25	24MHZ	48MHZ

Fix 75504 power too low.

接至Location:SQD4 (主要當CPU有上時,需將PU_PWOK 拉low)

Fix 75504 clock amp too low

Single (128Mx1)
 # Layout colay 256Mx1

*PVT時,M_BIOS顆粒,放在SMD階

FOOTPRINT:IC8WSON-BIOS-COLAY'

Near QFX1 3VDUAL for EMI

Fix Q_FLASH fail with CPU.

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Title
APU USB, GPP
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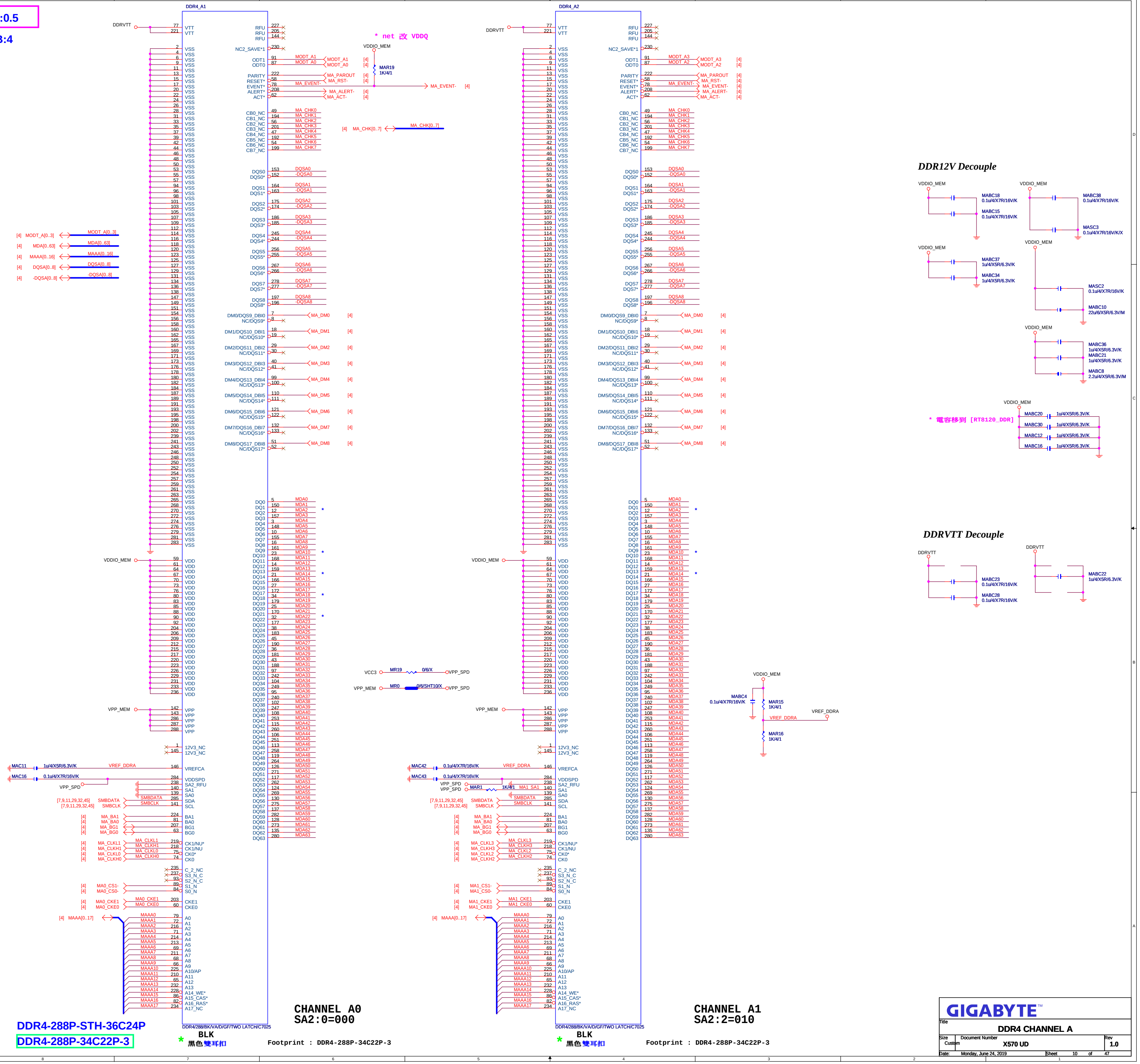
Rev:0.5

PCB:4



CHANNEL A0
SA2:0=000

CHANNEL A1
SA2:2=010

DDR4-288P-STH-36C24P

DDR4-288P-34C22P-3

* BLK
黑色雙耳扣

Footprint : DDR4-288P-34C22P-3

* BLK
黑色雙耳扣

Footprint : DDR4-288P-34C22P-3

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Title	DDR4 CHANNEL A
Size Custom	Document Number X570 UD
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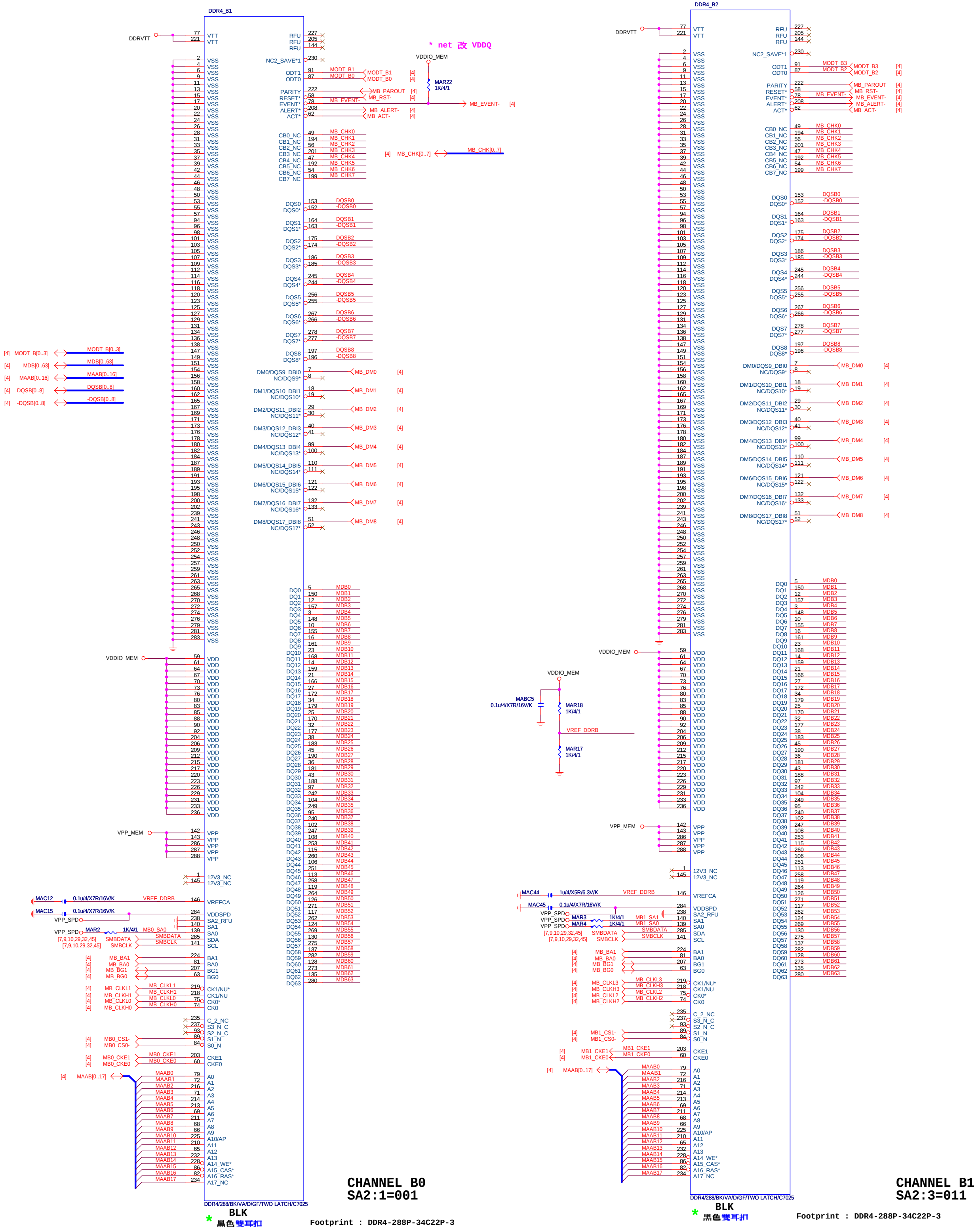

CHANNEL B0
SA2:1=001

Footprint : DDR4-288P-34C22P-3

CHANNEL B1
SA2:3=011

Footprint : DDR4-288P-34C22P-3

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Title
DDR4 CHANNEL B

Size Custom
Document Number X570 UD
Rev 1.0

Date: Monday, June 24, 2019
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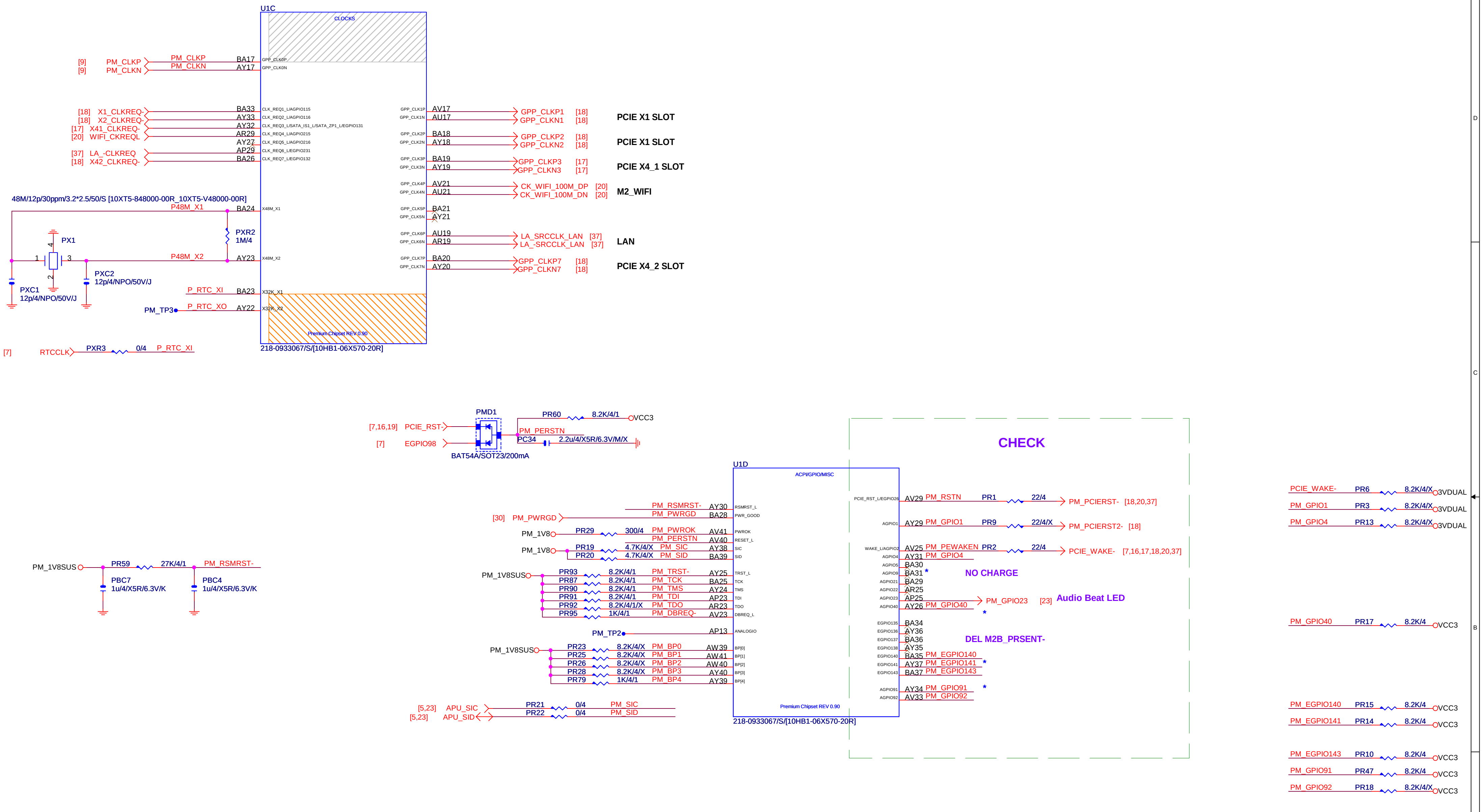

PM_GPIOR11=>1: GPP clock output enabled,0: GPP clock output disabled

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Title
PROMONTORY CPU/CLK/MISC

Size	Document Number	Rev
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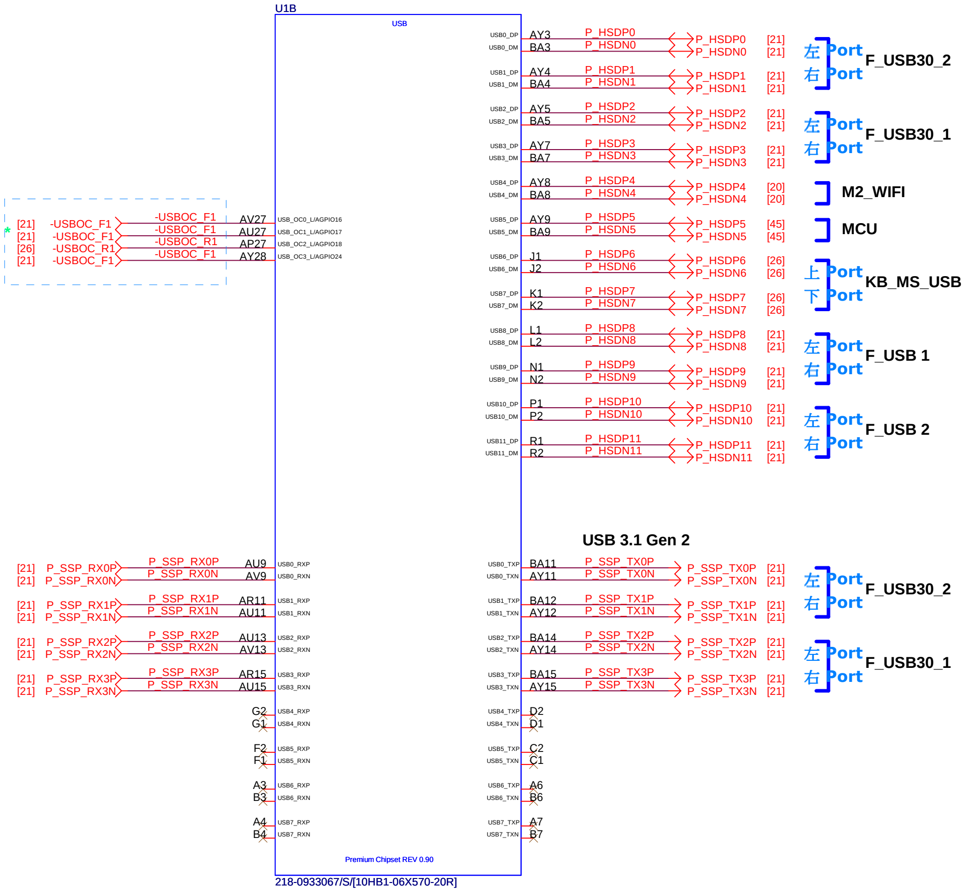

USB Controller 0: USB20 [0:5], USB30 [0:3]

USB Controller 1: USB20 [6:11], USB30 [4:7]

USB30G2	USB20
0	4
1	4
2	5
3	5
4	9
5	8
6	7
7	6

USB30_I211 Lan

F_USB 30_2

F_USB 30_1

FRONT TYPE C

HSD 10

HSD 11

HSD 6

HSD 7

HSD 8

HSD 9

HSD 5

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Title
PM USB

Size: Custom
Document Number: **X570 UD**
Rev: **1.0**

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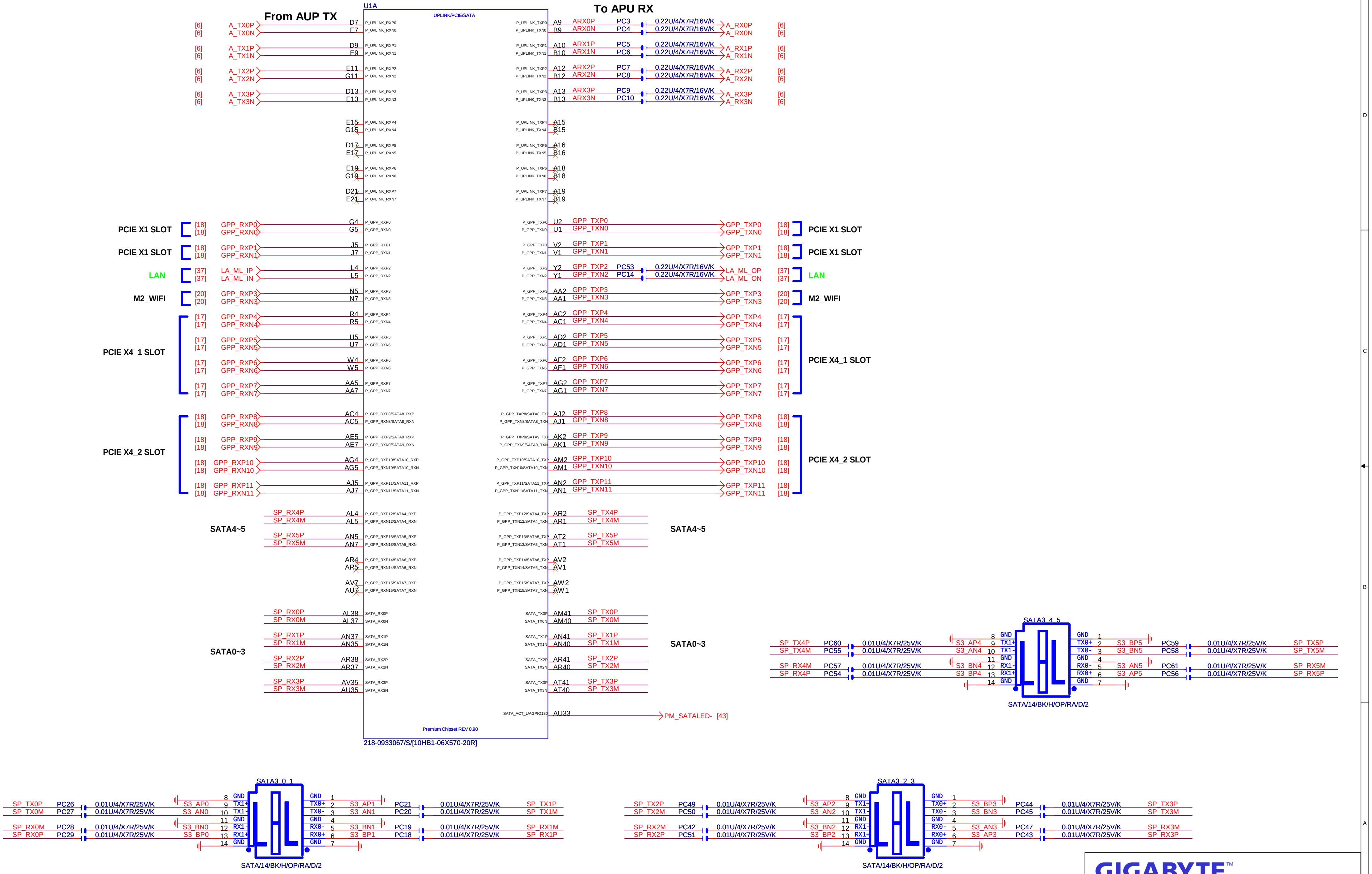

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Title
PM SATA , PCIE

Size	Document Number	Rev
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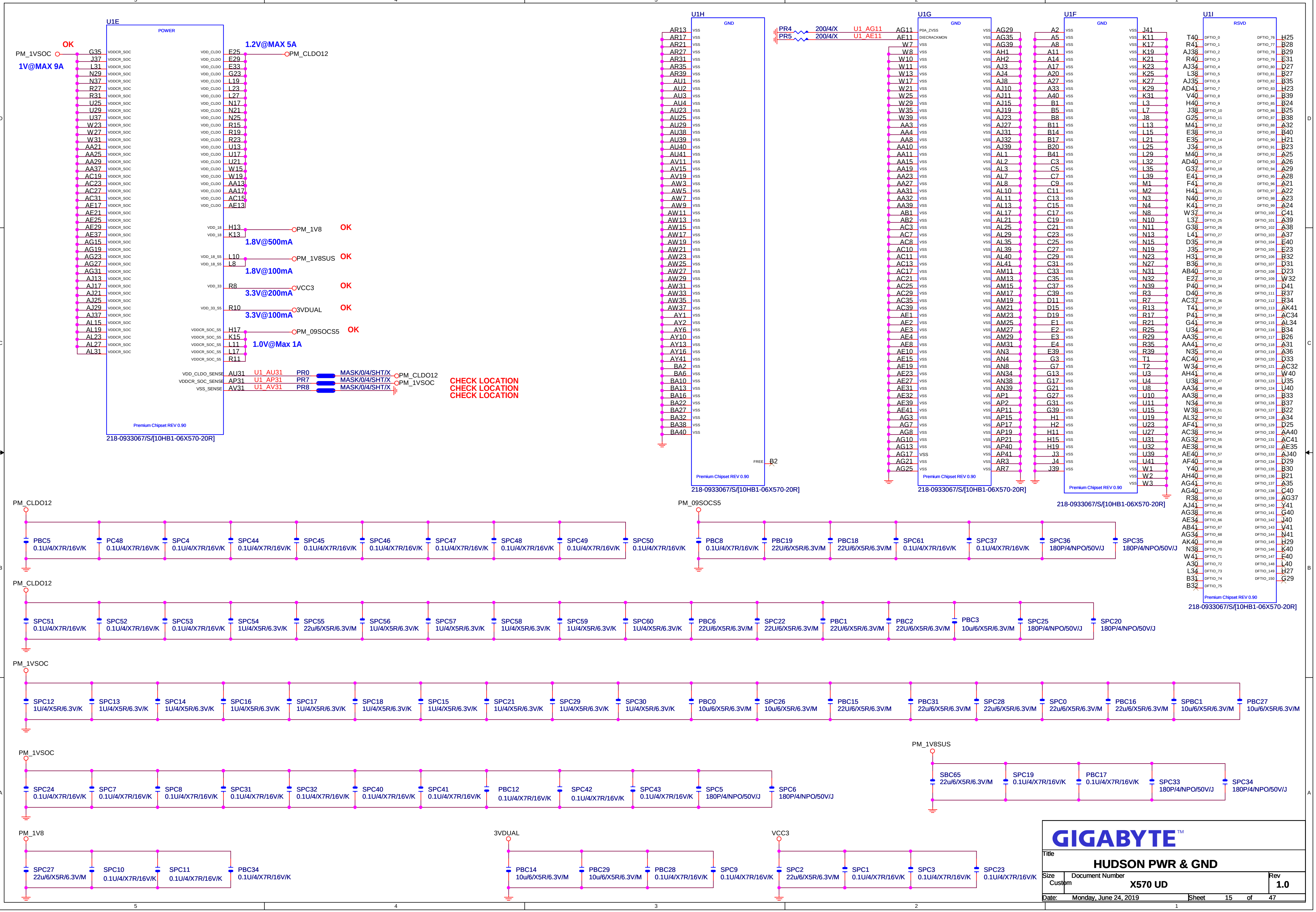

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Title	HUDSON PWR & GND		
Size Custom	Document Number X570 UD		Rev 1.0
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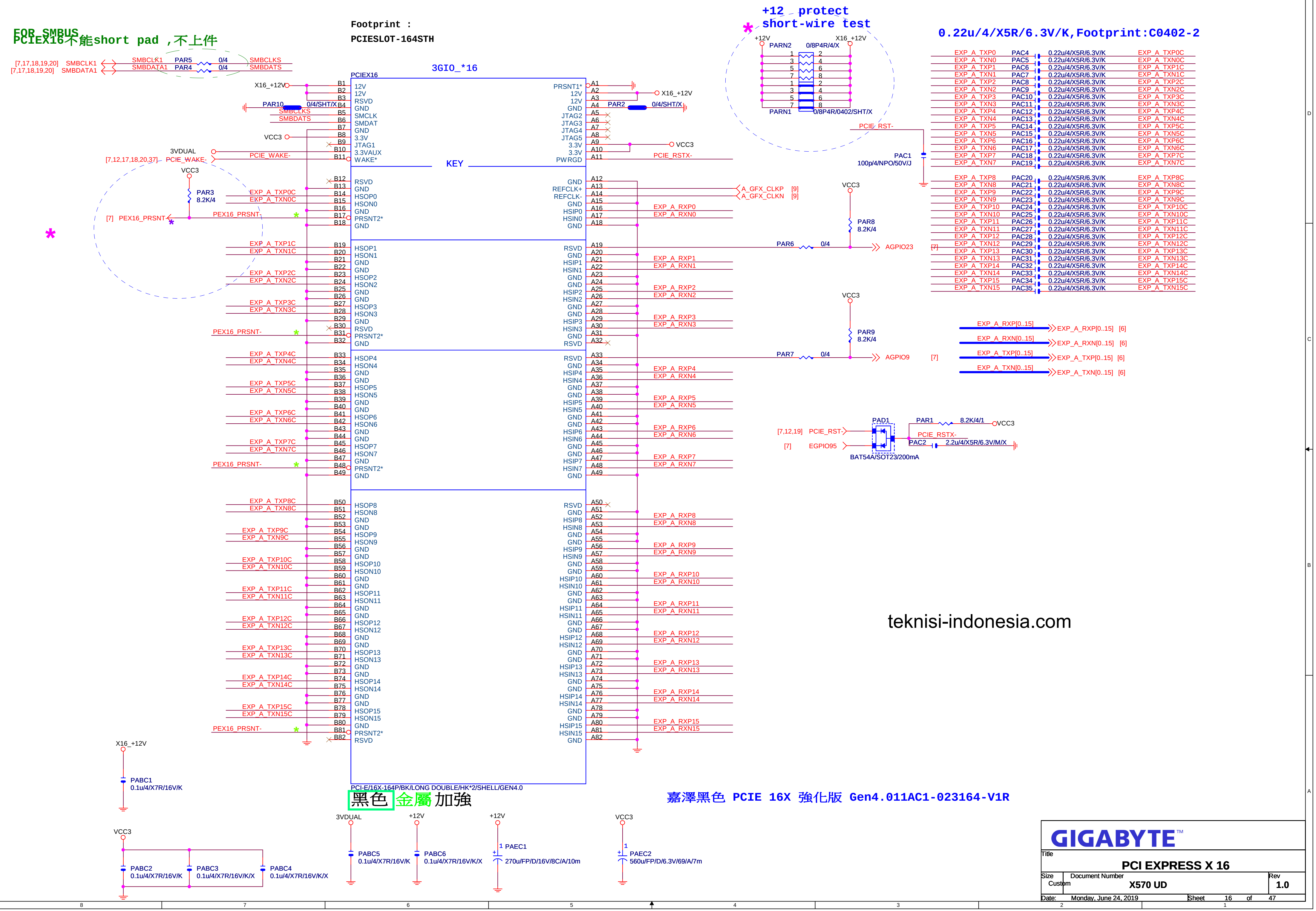

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Title

PCI EXPRESS X 16

Size Custom

Document Number X570 UD

Rev 1.0

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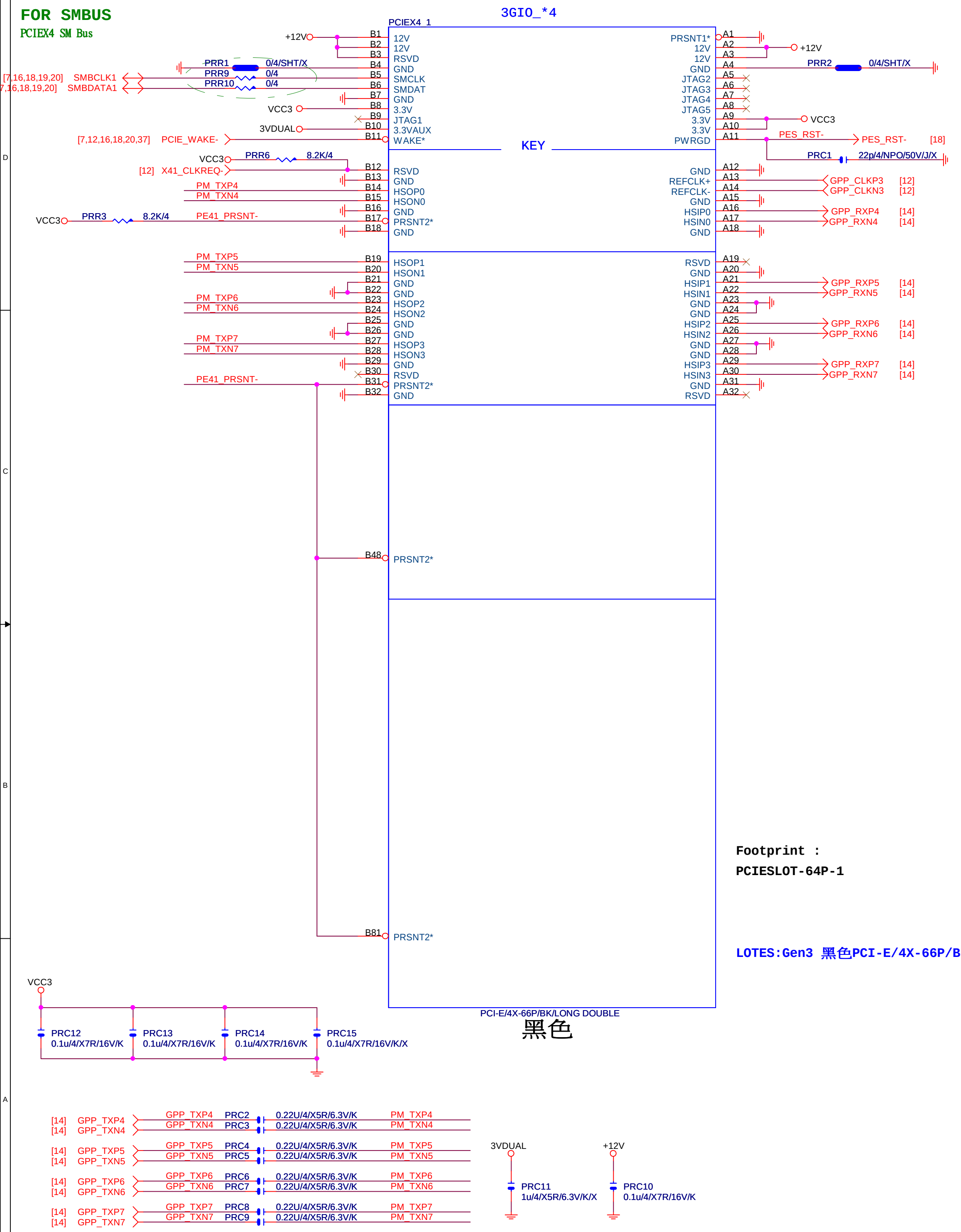

Footprint :
PCIESLOT-64P-1

LOTES:Gen3 黑色PCI-E/4X-66P/BK/LONG DOUBLE :11AC1-023065-17R

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Title
PCIE X4, X1

Size Custom
Document Number X570 UD
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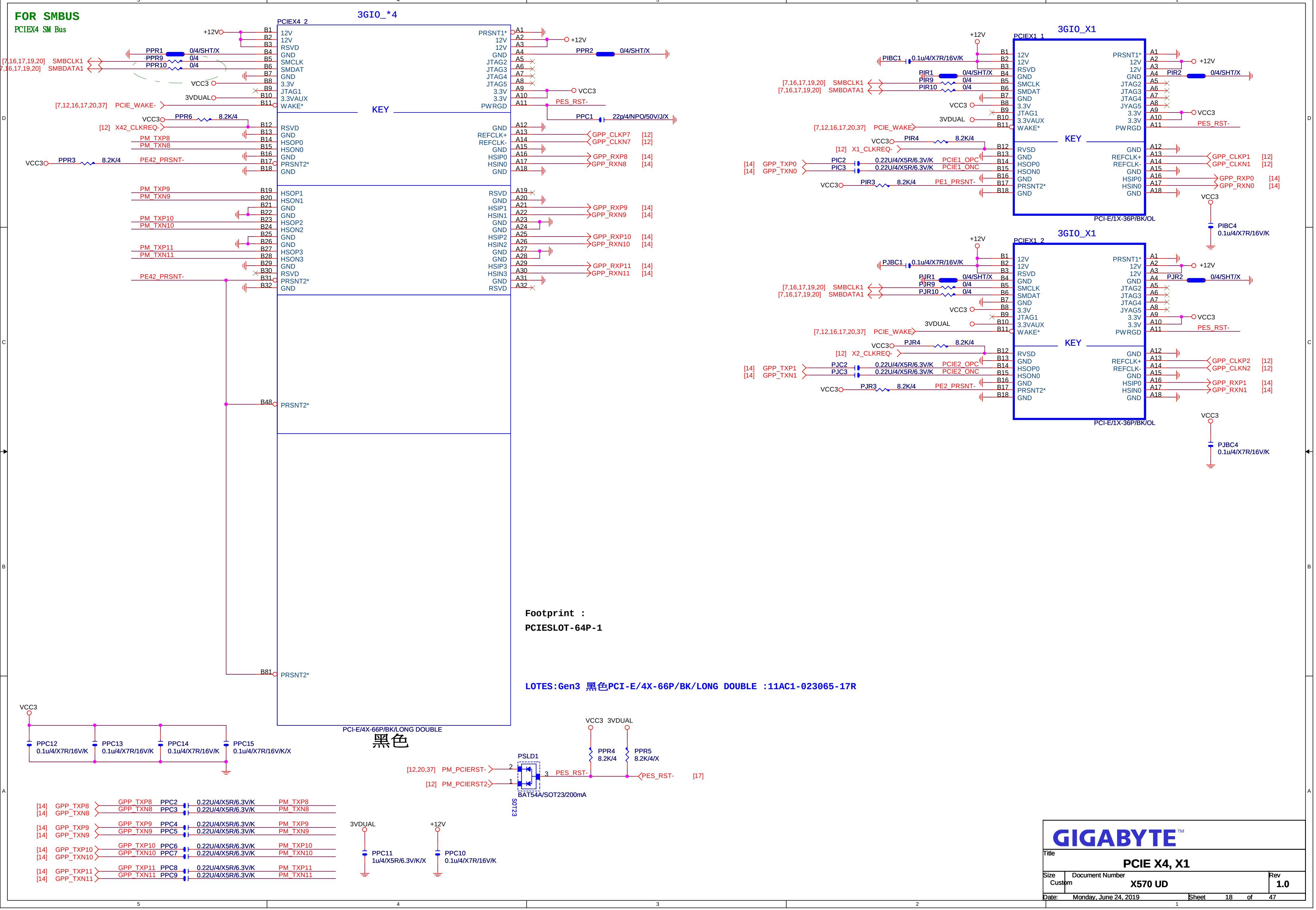

Footprint :
PCIESLOT-64P-1

LOTES:Gen3 黑色PCI-E/4X-66P/BK/LONG DOUBLE :11AC1-023065-17R

GIGABYTE™

Title	PCIE X4, X1	
Size Custom	Document Number X570 UD	Rev 1.0
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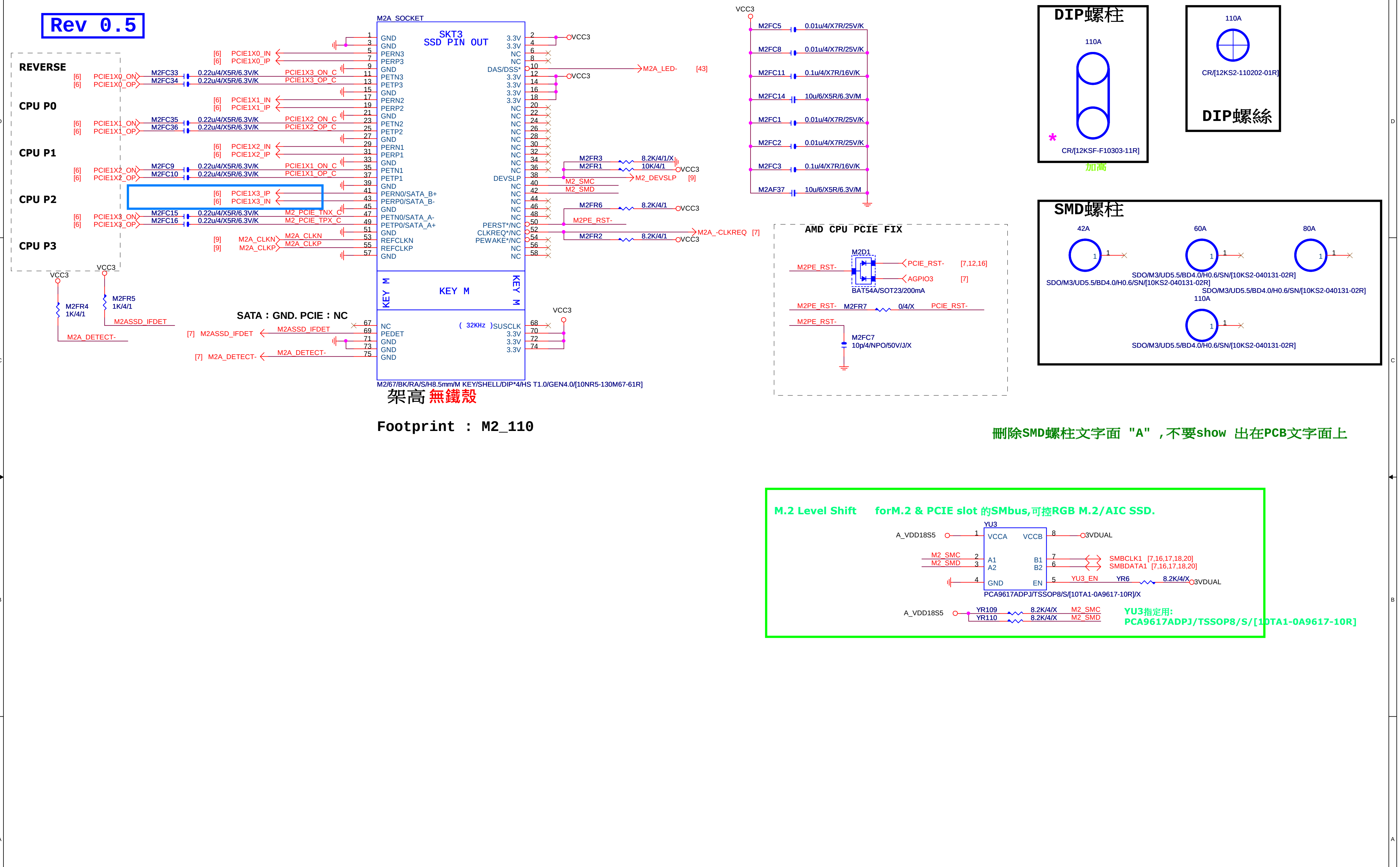

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Title
M.2 SLOT FROM CPU(A)

Size	Document Number	Rev
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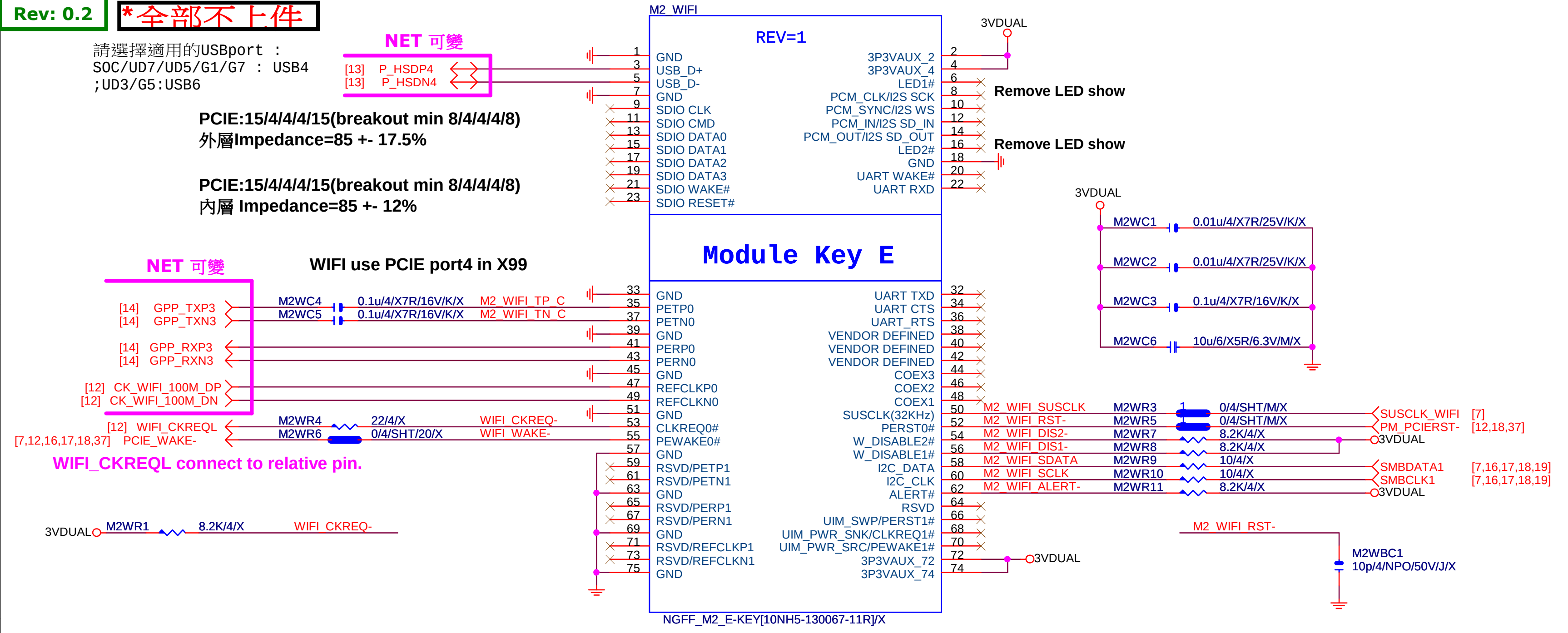
Rev: 0.2

*全部不上件



請選擇適用的USBport :
SOC/UD7/UD5/G1/G7 : USB4
;UD3/G5:USB6

PCIE:15/4/4/4/15(breakout min 8/4/4/4/8)
外層Impedance=85 +- 17.5%

PCIE:15/4/4/4/15(breakout min 8/4/4/4/8)
內層 Impedance=85 +- 12%

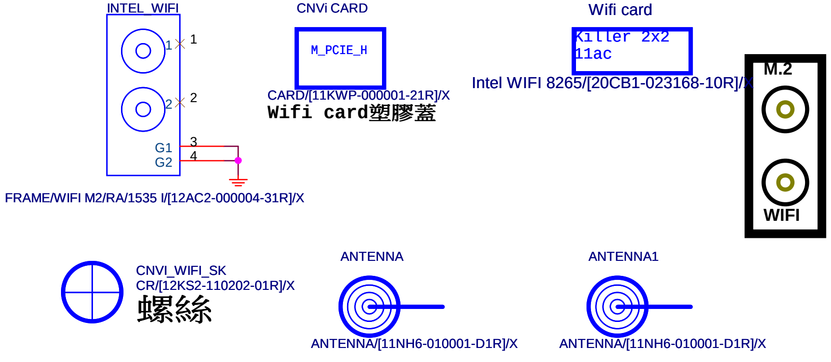
WIFI use PCIE port4 in X99

WIFI_CKREQL connect to relative pin.

FOR M.2 WIFI MODULE @ REAR PANEL

★Update 2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線

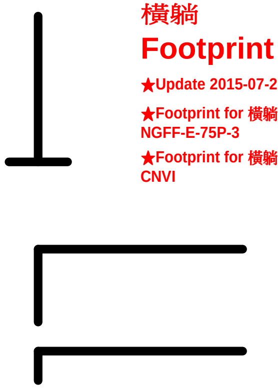


PCIE:15/4/4/4/15(breakout min 8/4/4/4/8)
內層 Impedance=85 +- 12%

直立
Footprint Notice.

★Update 2015-07-22

★Footprint for 直立式 SMD:
WIFI-EKEY
★SMD P/N: 直立式
10NH5-130067-11R.



橫躺
Footprint Notice.

★Update 2015-07-22

★Footprint for 橫躺式高:
NGFF-E-75P-3
★Footprint for 橫躺式矮:
CNVI

Rev:0.6
★ for PCIe mode 預留

★ 橫躺式高SMD
P/N:10NR5-130067-61R
★ 橫躺式矮SMD
P/N:10NR5-130067-22R

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Title	M2_WIFI_E_KEY	
Size B	Document Number X570 UD	Rev 1.0
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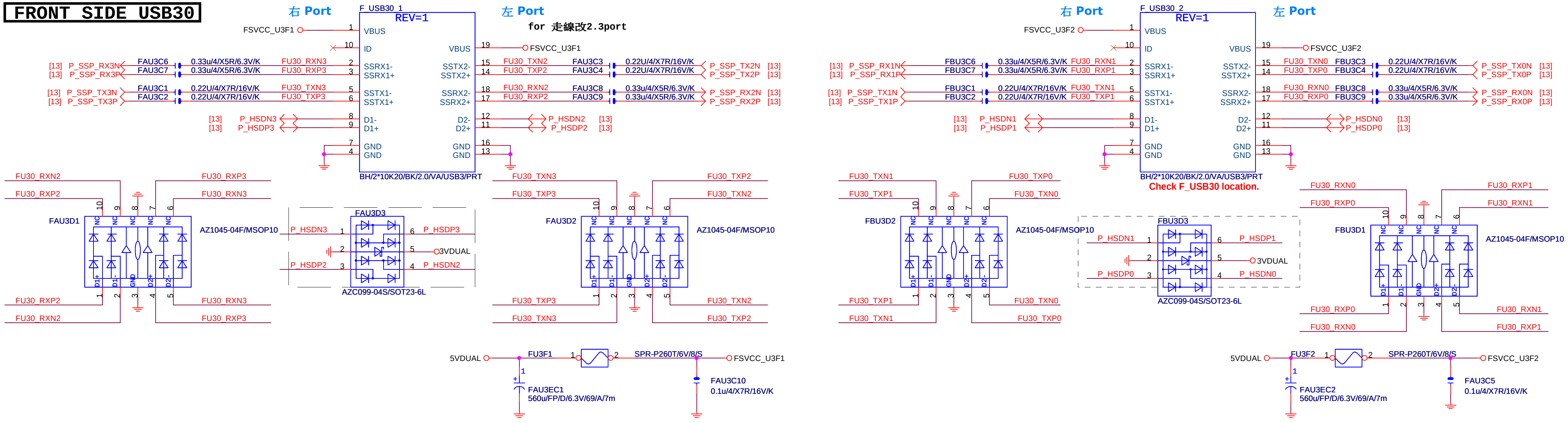
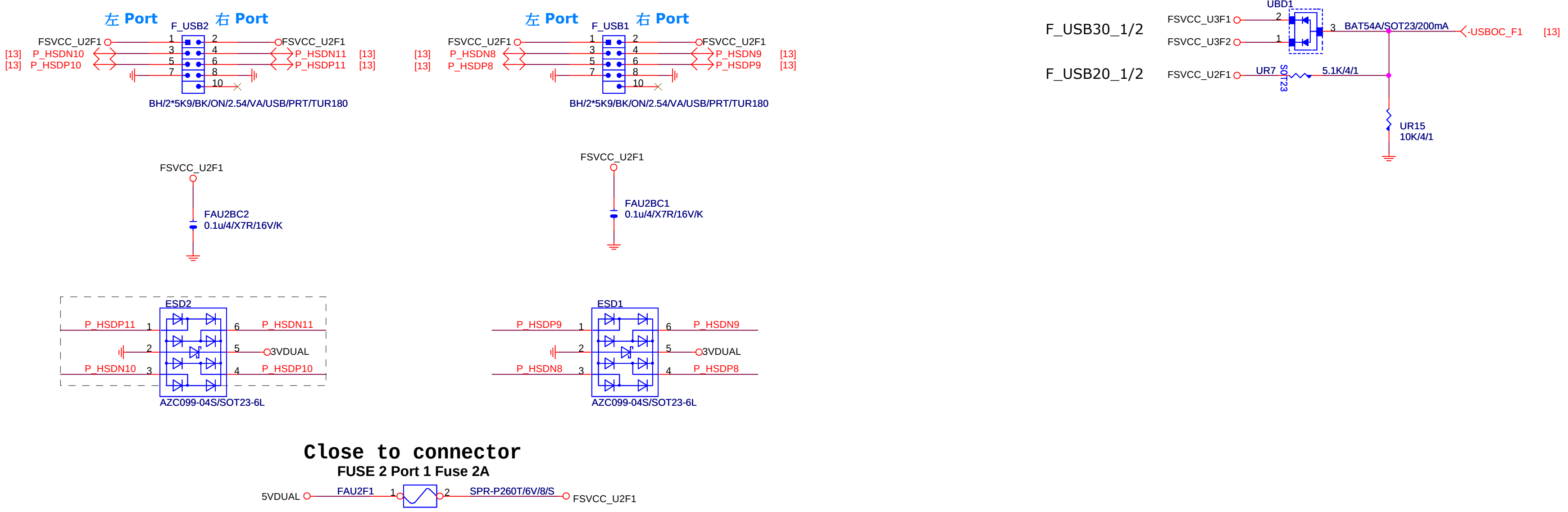
FRONT SIDE USB30



FRONT SIDE USB2

FRONT SIDE USB1



Color markers can be changed by model

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Title
F_ USB30,F_ USB20

Size	Document Number	Rev
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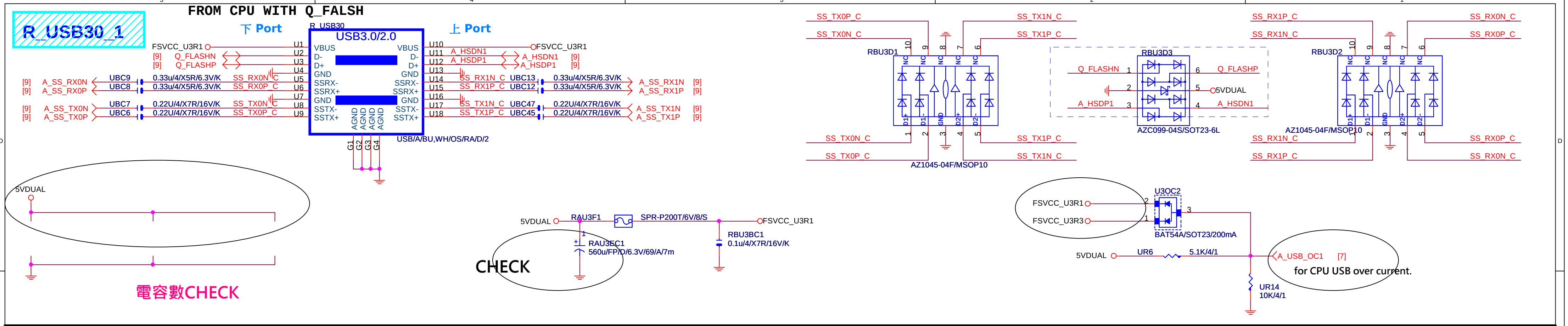

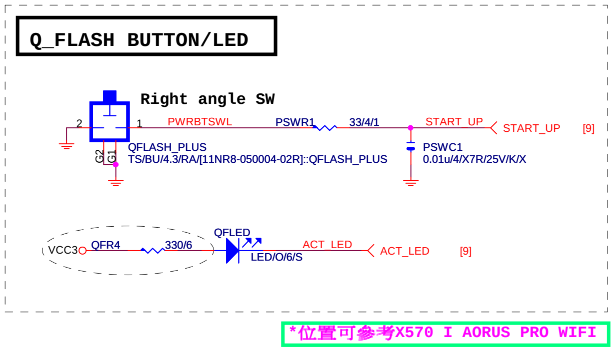

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Title
R_USB30,R_USB20

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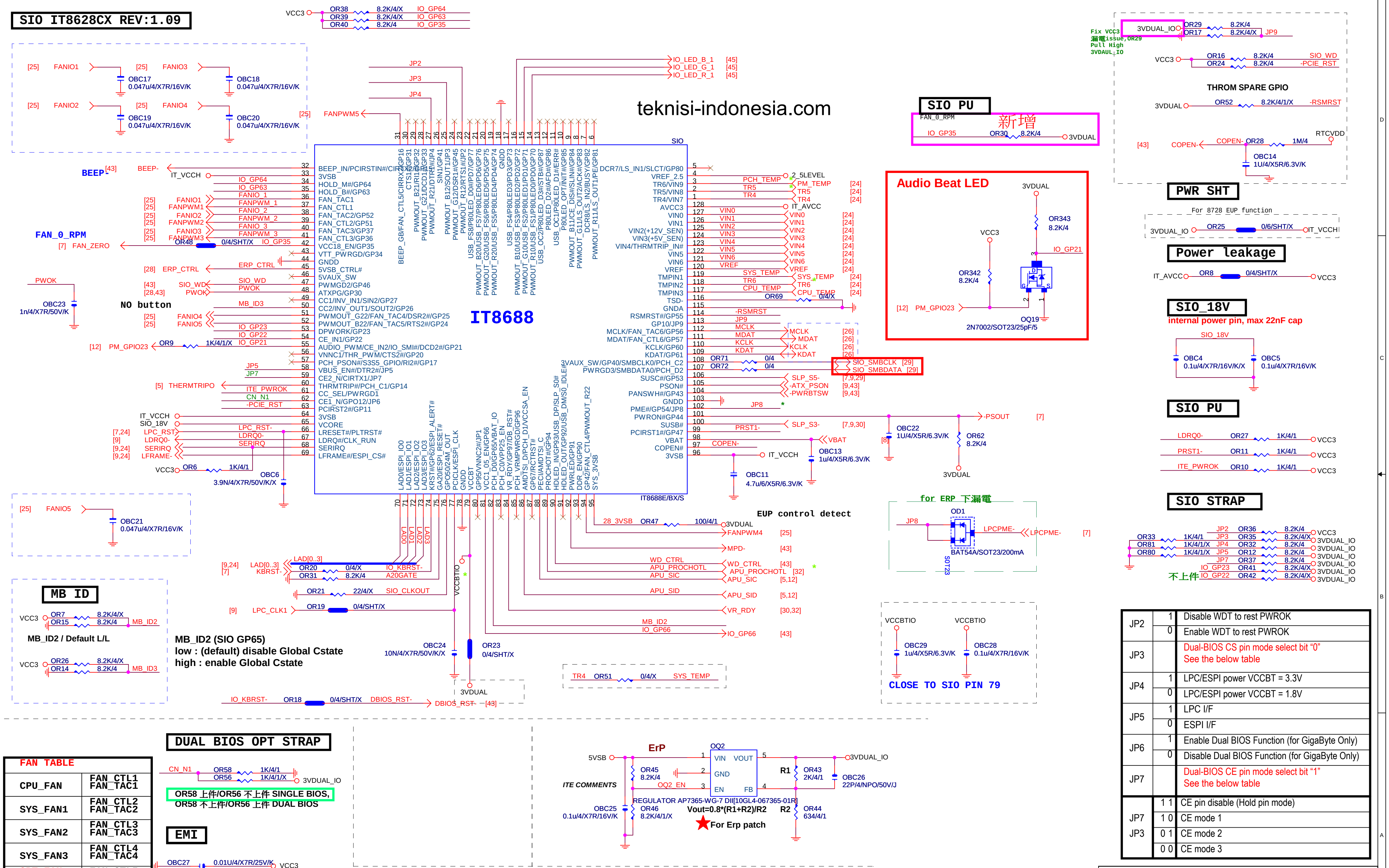
SIO IT8628CX REV:1.09



FAN TABLE

CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7 JP3	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
	0 1	CE mode 2
	0 0	CE mode 3

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Title: IT8688

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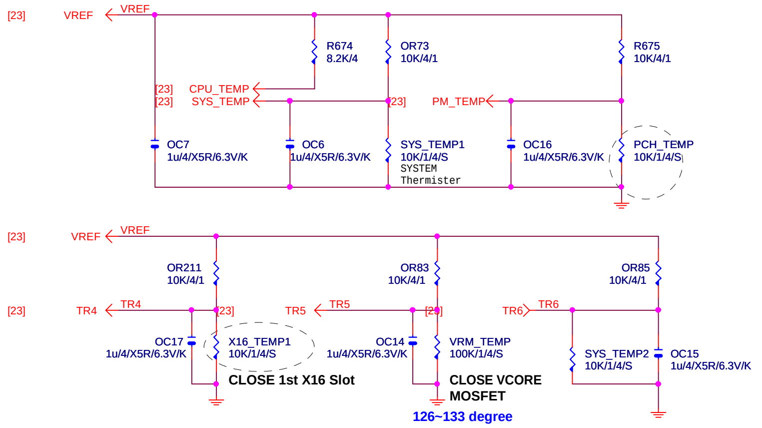
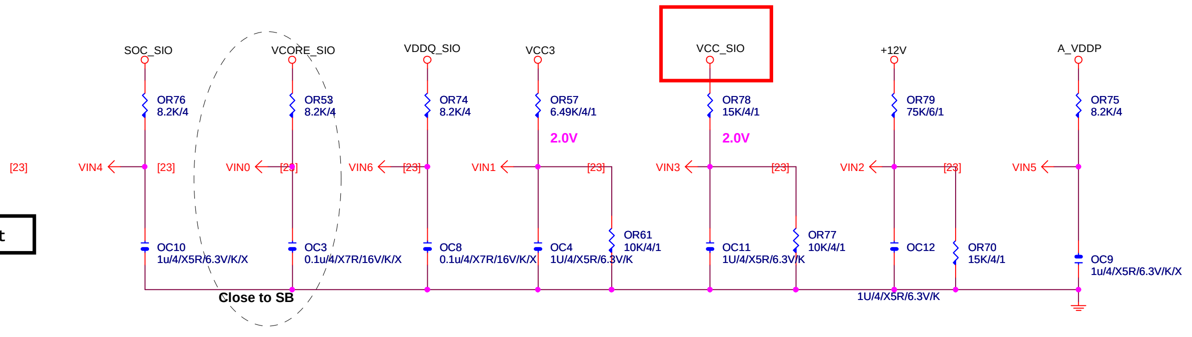
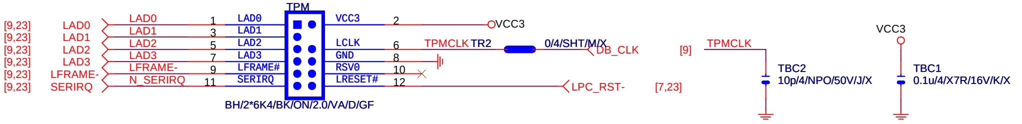
删除clk



Del Thunderbolt





TPM update footprint : TPM2X6-CUT4-1

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Title
HWM, TPM

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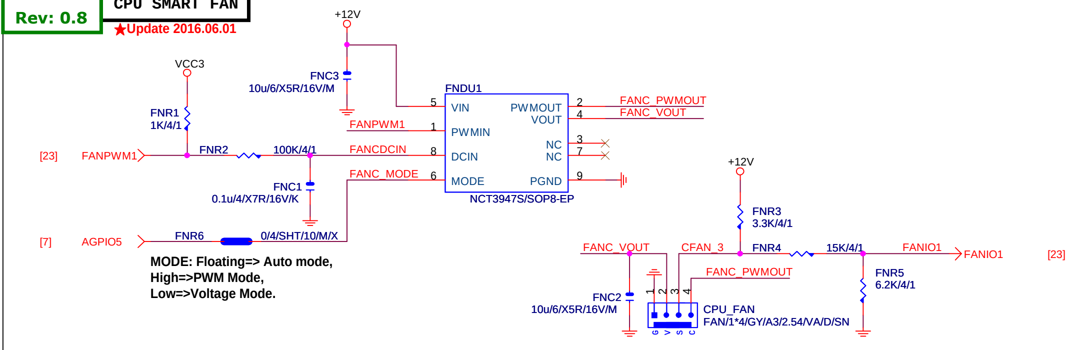
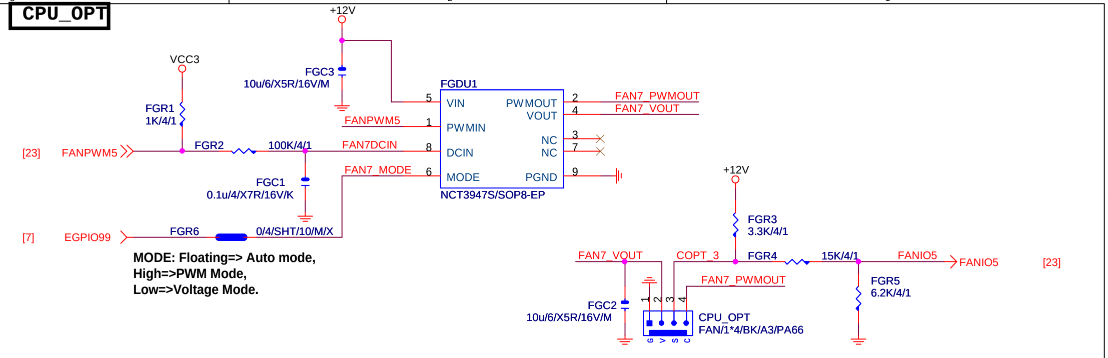
CPU SMART FAN

★Update 2016.06.01



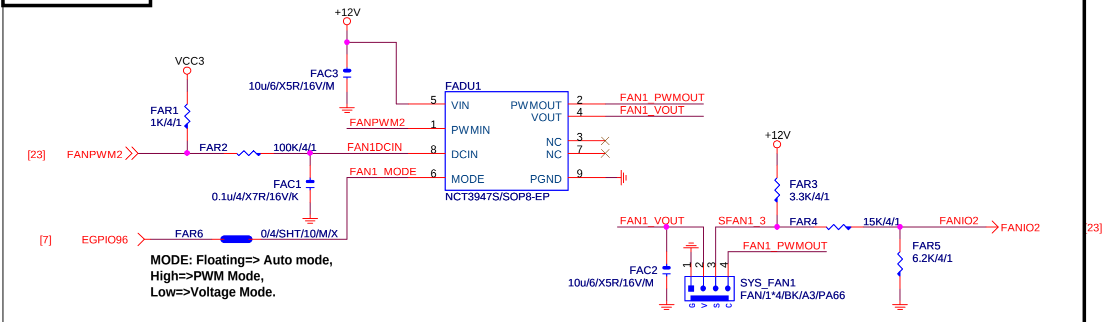
MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

CPU_OPT



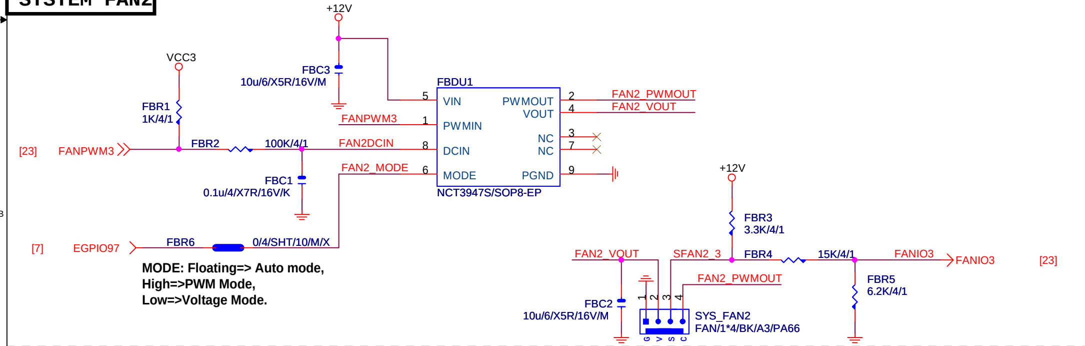
MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

SYSTEM FAN1



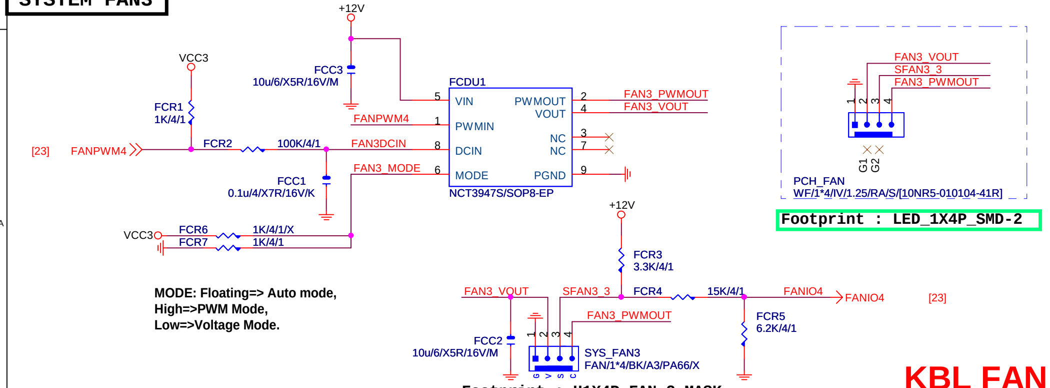
MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

SYSTEM FAN2



MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

SYSTEM FAN3



Footprint : LED_1X4P_SMD-2

MODE: Floating=> Auto mode,
High=>PWM Mode,
Low=>Voltage Mode.

Footprint : H1X4P-FAN-2-MASK

KBL FAN LOCATION MAP REFER TO PAGE.27

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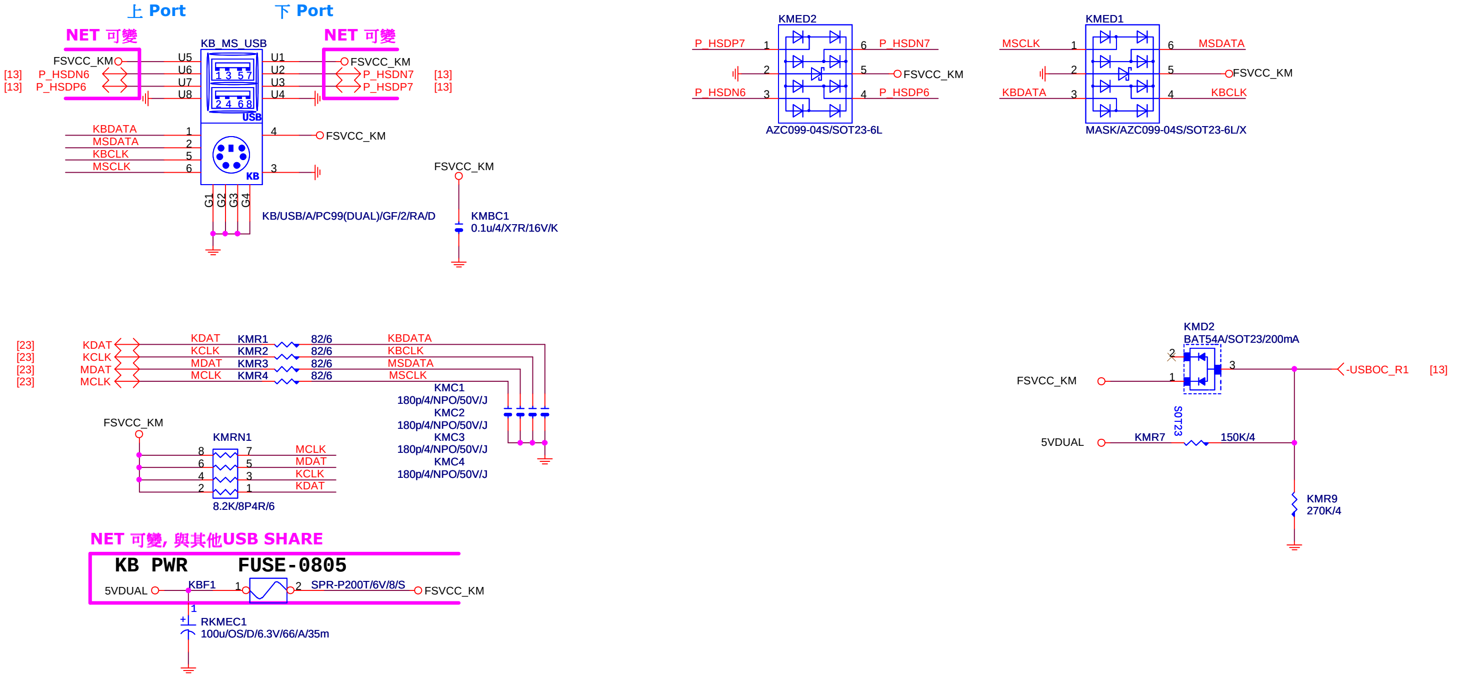
Title	FAN	
Size: Custom	Document Number: X570 UD	Rev: 1.0
Date: Monday, June 24, 2019	Sheet 25 of 47	

Rev: 0.91

KB/MS



GIGABYTE™

Title		
KB_MS_USB		
Size: Custom	Document Number: X570 UD	Rev: 1.0
Date: Monday, June 24, 2019	Sheet 26 of 47	

A_VDDP

A_VDDP 0.9V or 1.05V

CHOKE與CAP料號可變

L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A

FS=290K
OCP=30A

RF: low=>DEM mode, high=>CCM mode.

0.704*(1+RS/R0) = Vout

Remote sense請從最重的負載端點拉回

請放置CHOKE一出來的地方

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

A_VDDPS5

A_VDDPS5 0.9V or 1.05V (1A)

0.8*[(R1+R2)/R1] = Vout =1.121V

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

【技術通報R&D技術通報156】
RT9018(RICHTEK)與NCT3730(NUVOTON),
EM5103GE(EMC)做共用,針對PIN7(FB)分壓阻值部份
(R1/R2)須做修改為100K以上電阻值

PWR SEQ

REV:0.4

A_VDD1V8

A_VDD1V8 1.8V (2A)

L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A

MA_L3,MB_L3, NPL2 footprint to CHOKE6X6MM_SMD-1

上件

teknisi-indonesia.com

A_VDD18S5

A_VDD18S5 1.8V (500mA)

0.8*[(R1+R2)/R1] = Vout

VPP CAP

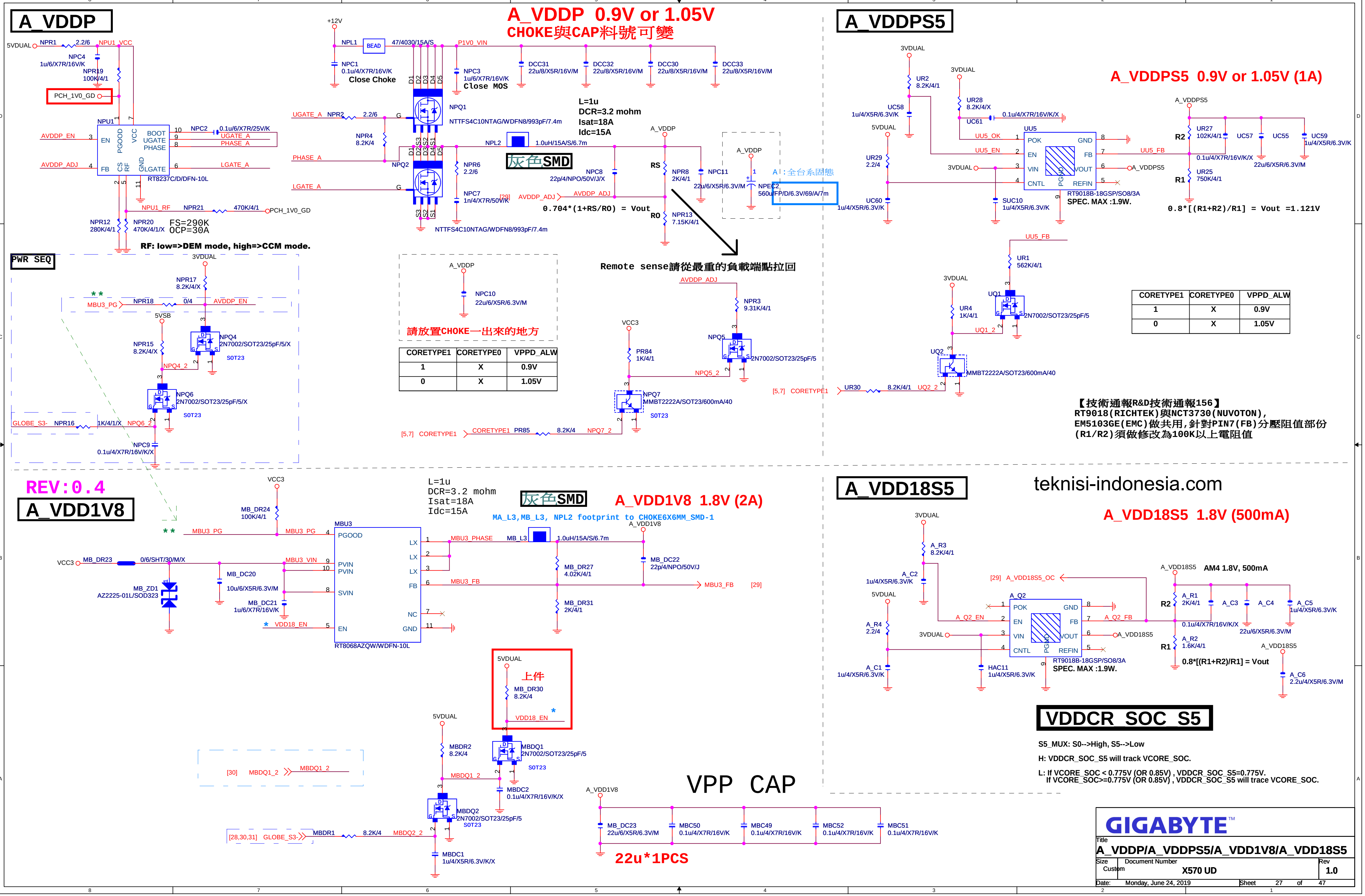
22u*1PCS

VDDCR_SOC_S5

S5_MUX: S0-->High, S5-->Low

H: VDDCR_SOC_S5 will track VCORE_SOC.

L: If VCORE_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.
If VCORE_SOC>=0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCORE_SOC.

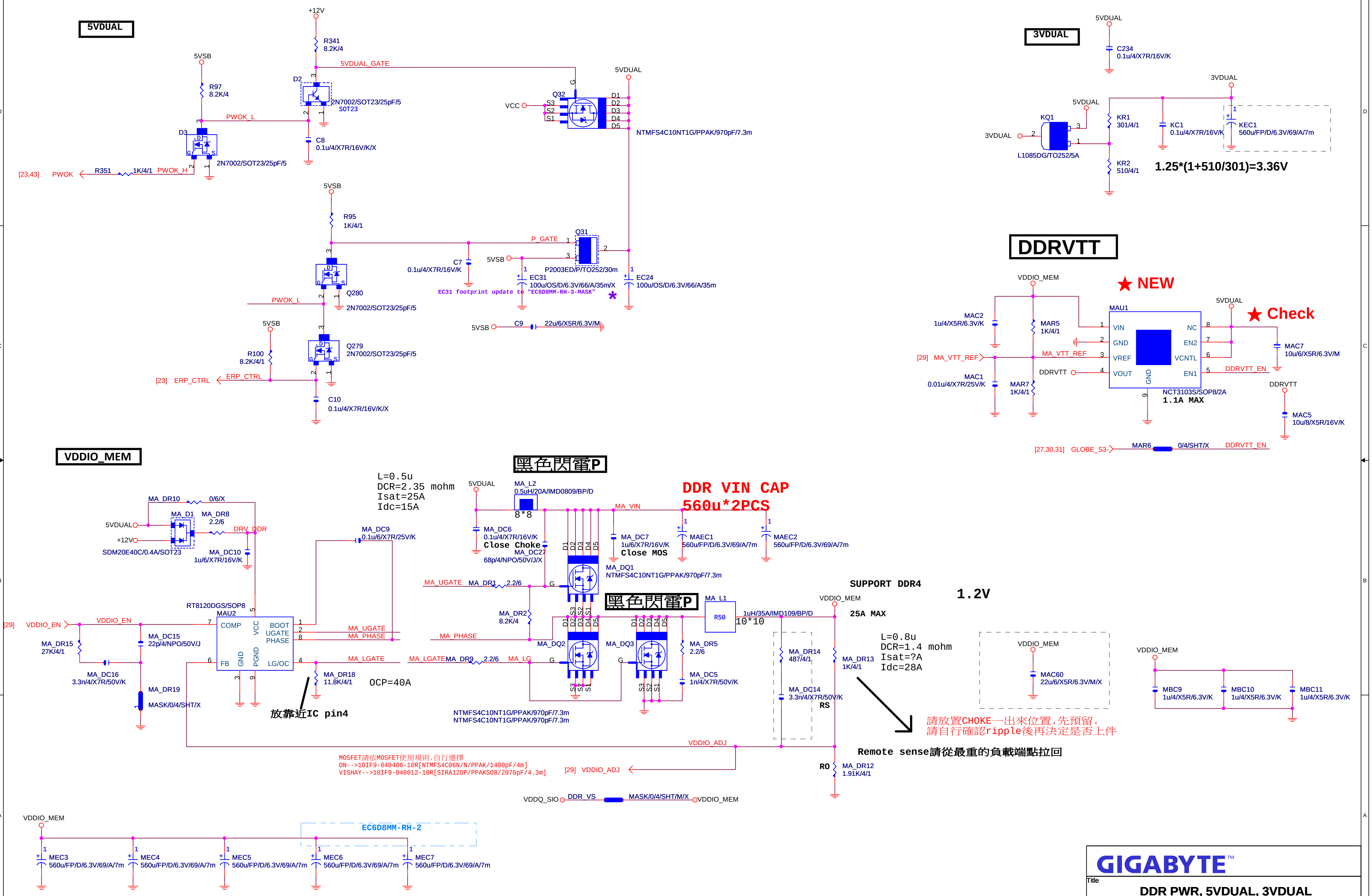


GIGABYTE™

Title
A_VDDP/A_VDDPS5/A_VDD1V8/A_VDD18S5

Size	Document Number	Rev
Custom	X570 UD	1.0

Date: Monday, June 24, 2019 Sheet 27 of 47



MOSFET請依MOSFET使用規則.自行選擇
ON-->10IF9-040406-10R[NTMFS4C06N/N/PPAK/1400pF/4m]
VISHAY-->10IF9-040012-10R[SIRA12DP/PPAKSO8/2070pF/4.3m]

請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件

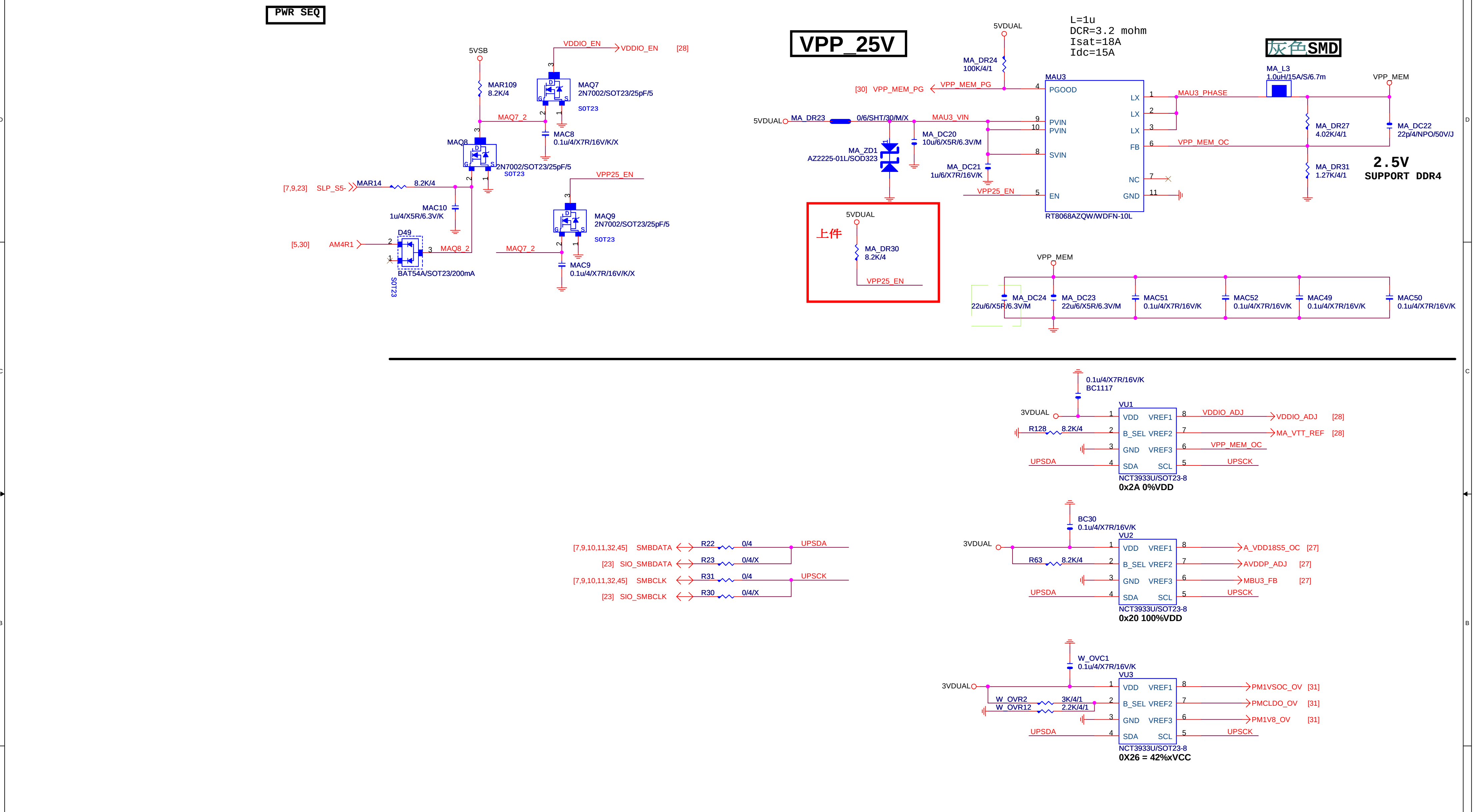
Remote sense請從最重的負載端點拉回

GIGABYTE™

Title
DDR PWR, 5VDUAL, 3VDUAL

Size	Document Number	Rev
Custom	X570 UD	1.0

Date: Monday, June 24, 2019 Sheet 28 of 47



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

GIGABYTE™

Title
VPPMEM

Size: Custom
Document Number: **X570 UD**
Rev: **1.0**

Date: Monday, June 24, 2019
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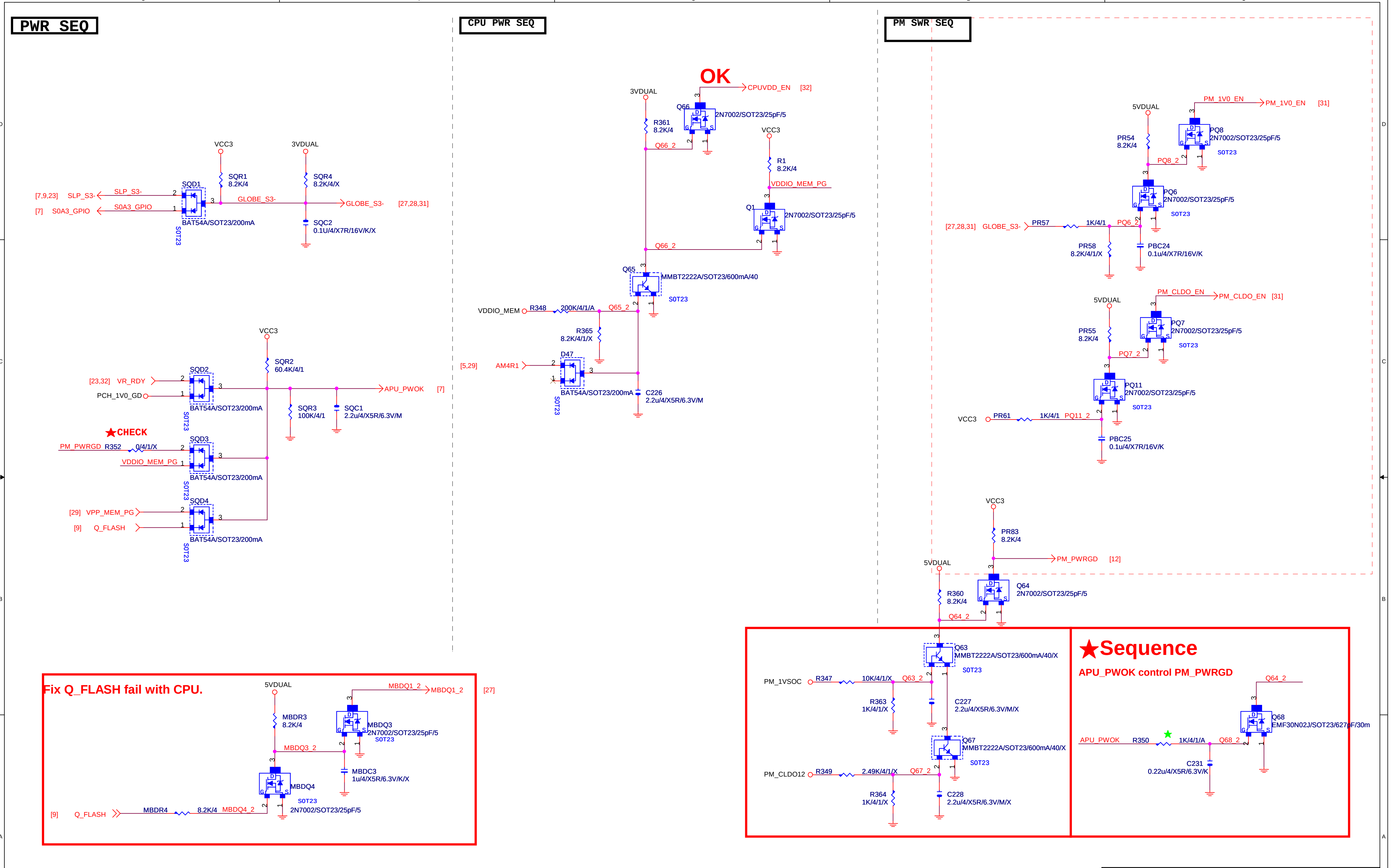


OK

★CHECK

Fix Q_FLASH fail with CPU.

★Sequence

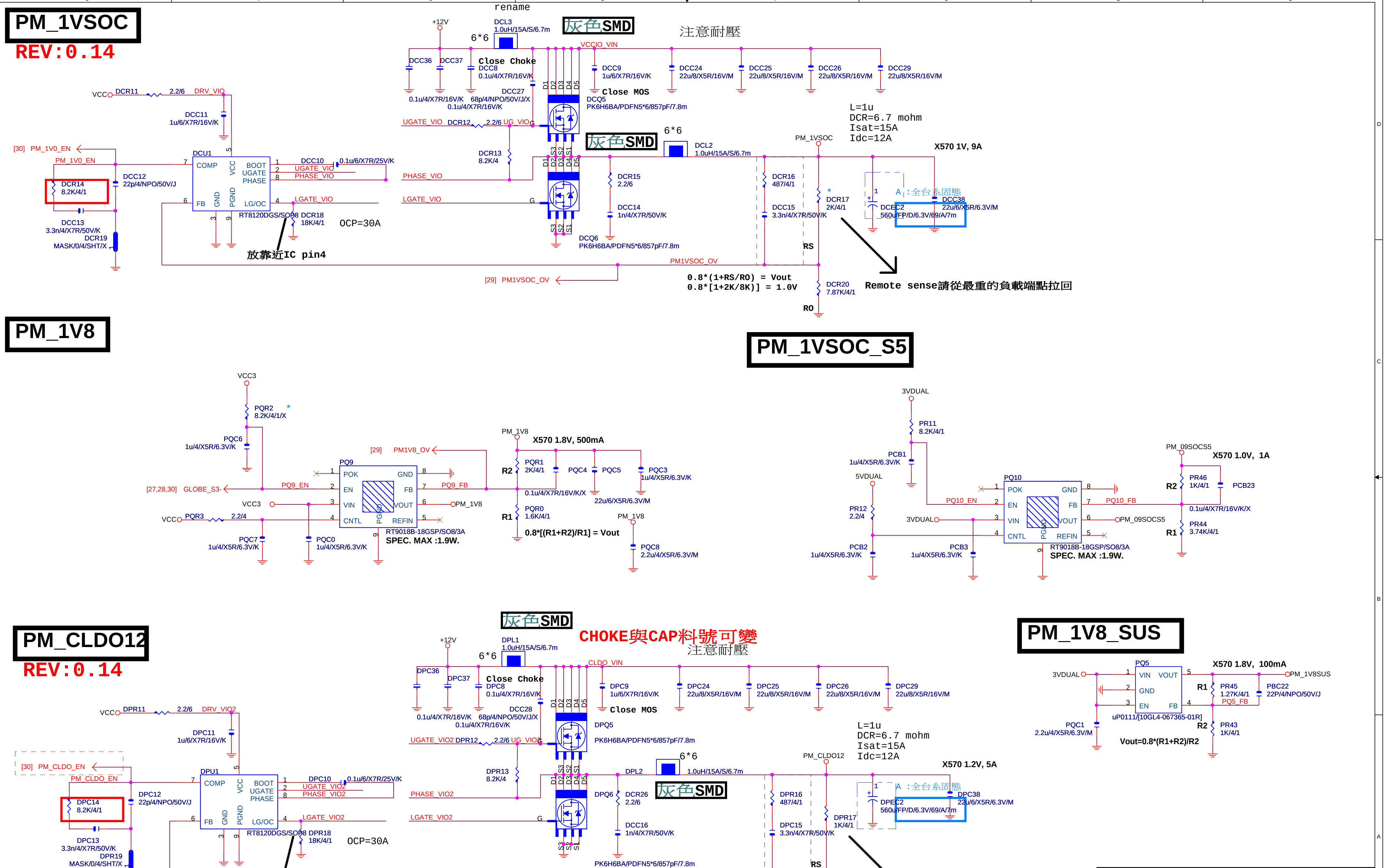
APU_PWOK control PM_PWRGD

GIGABYTE™

Title
POWER SEQUENCE

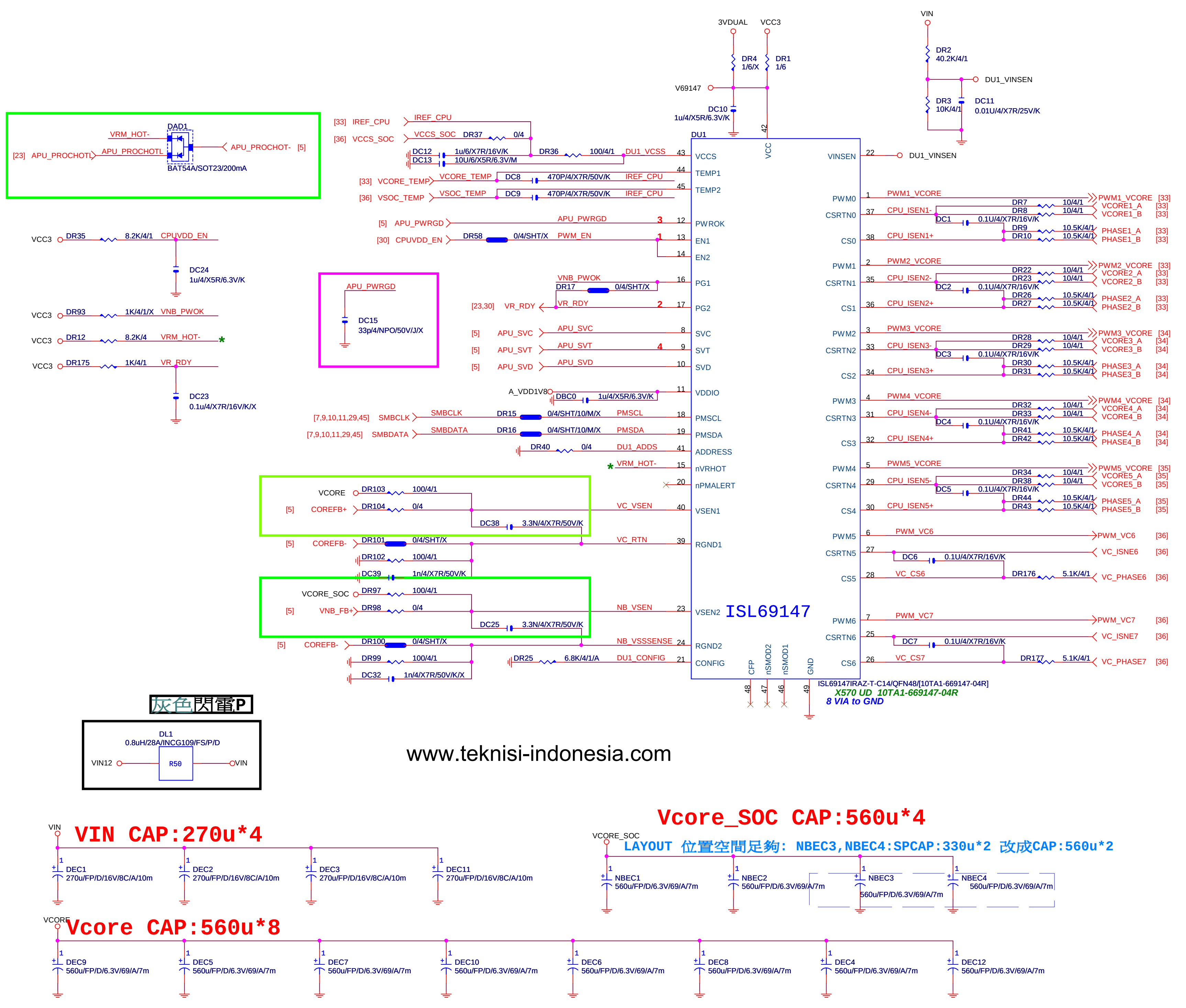
Size	Document Number	Rev
Custom	X570 UD	1.0

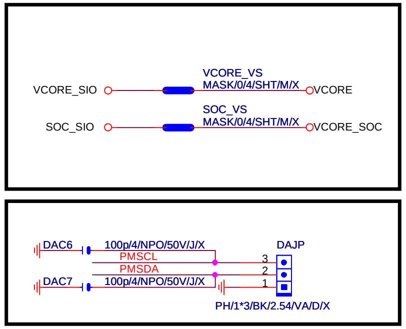
Date: Monday, June 24, 2019 Sheet 30 of 47



GIGABYTE

Title	X570 POWER		
Size Custom	Document Number X570 UD		Rev 1.0
Date: Monday, June 24, 2019		Sheet 31 of 47	





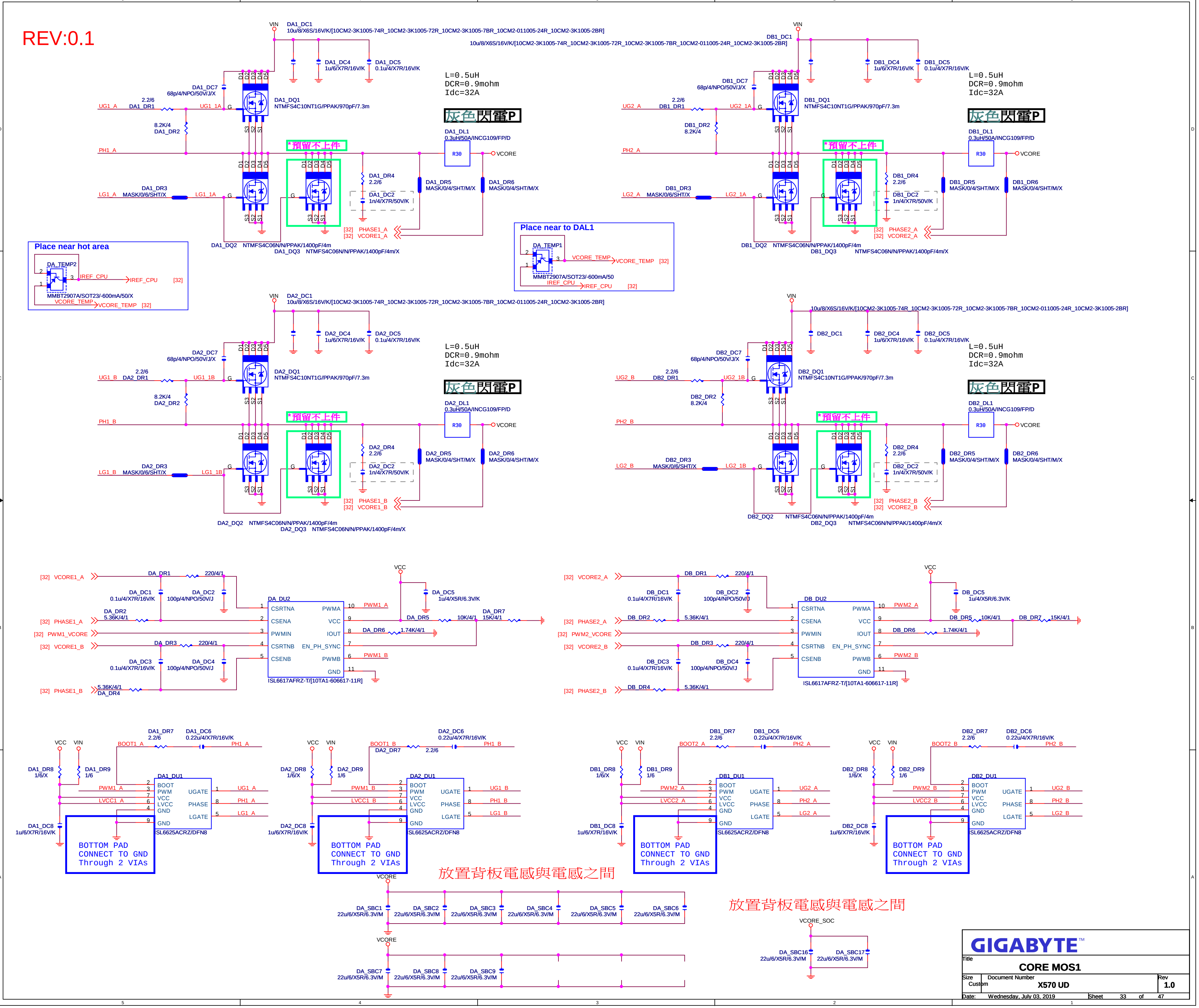
GIGABYTE™

Title
PWM ISL69147

Size	Document Number	Rev
Custom	X570 UD	1.0

Date: Wednesday, July 03, 2019 Sheet 32 of 47

REV:0.1

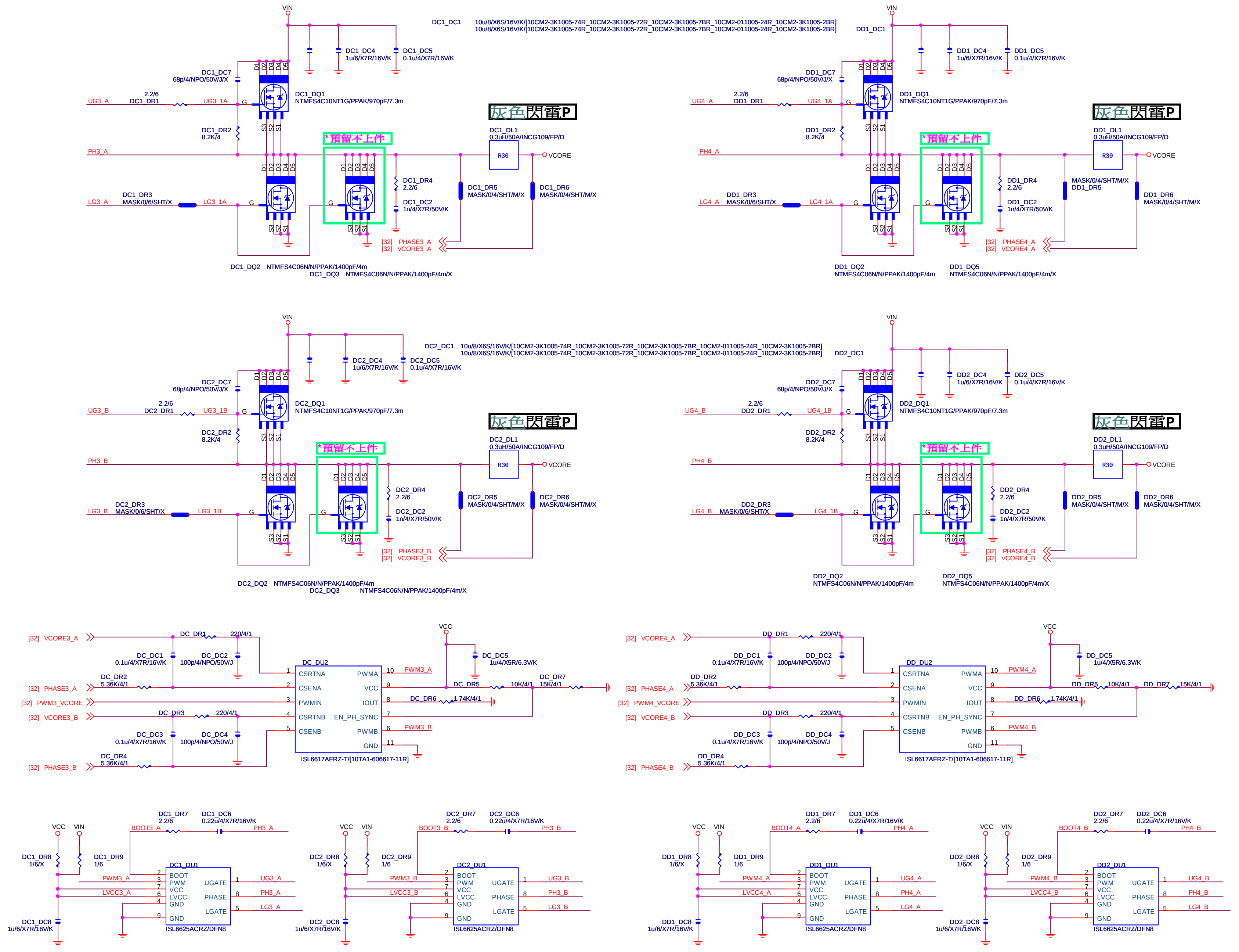


GIGABYTE™

Title
CORE MOS1

Size: Custom
Document Number: X570 UD
Rev: 1.0

Date: Wednesday, July 03, 2019 Sheet 33 of 47



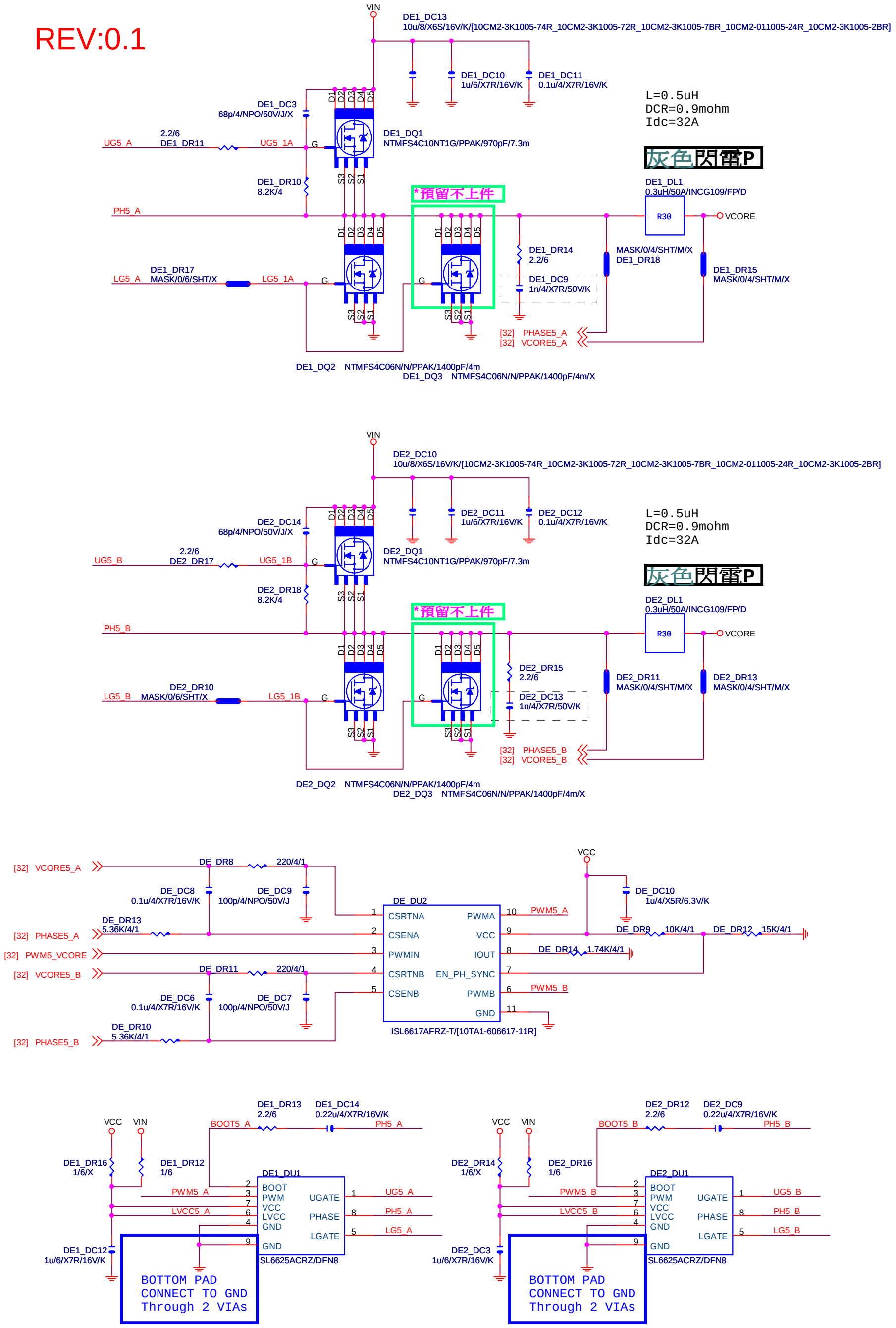
GIGABYTE™

Title
CORE MOS2

Size	Document Number	Rev
Custom	X570 UD	1.0

Date: Wednesday, July 03, 2019 Sheet 34 of 47

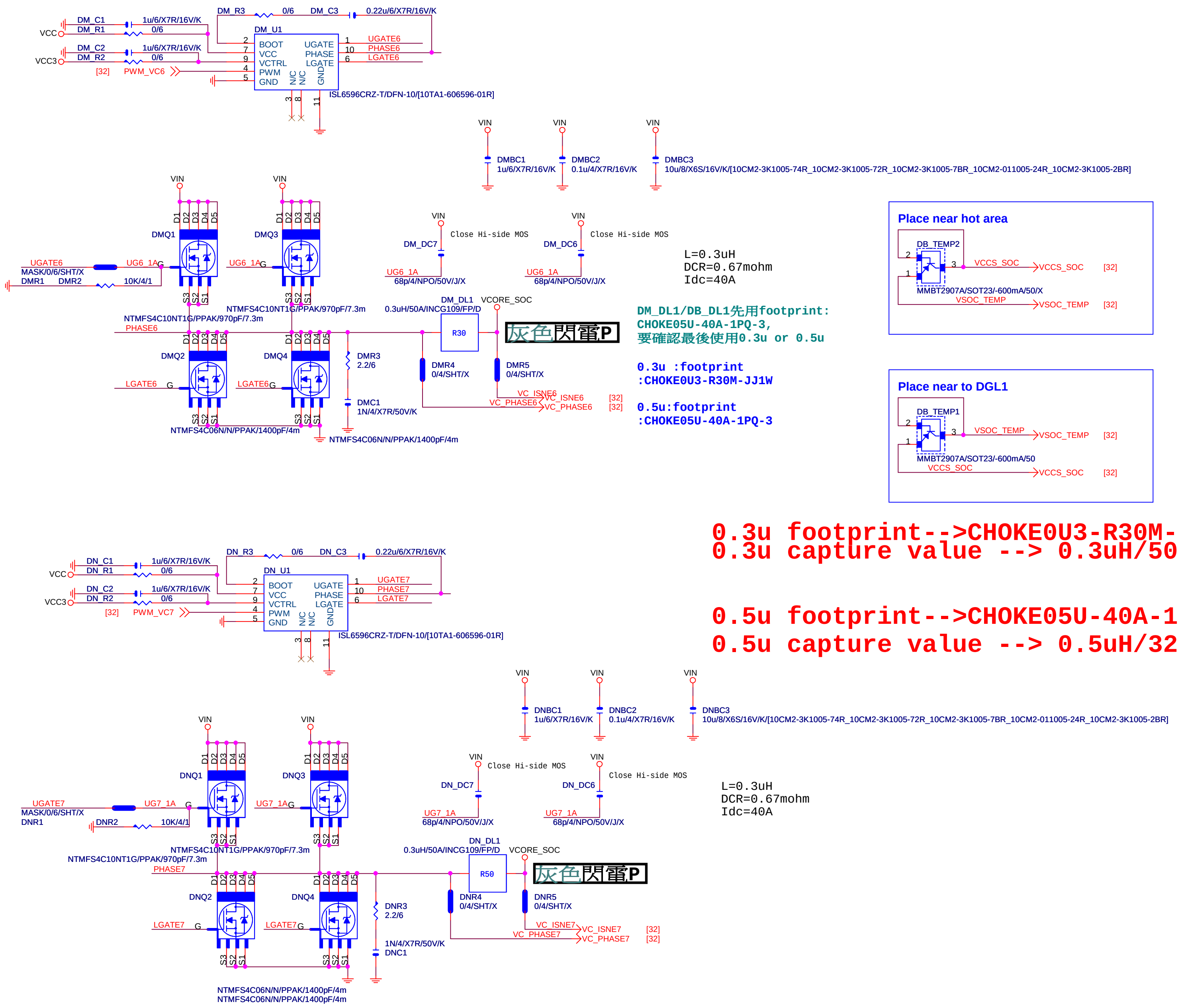
REV:0.1



GIGABYTE™

Title	VCORE MOS3	
Size: Custom	Document Number: X570 UD	Rev: 1.0
Date: Wednesday, July 03, 2019	Sheet 35 of 47	

REV:0.1



L=0.3uH
DCR=0.67mohm
Idc=40A

DM_DL1/DB_DL1先用footprint:
CHOKE05U-40A-1PQ-3,
要確認最後使用0.3u or 0.5u

0.3u :footprint
:CHOKE0U3-R30M-JJ1W

0.5u:footprint
:CHOKE05U-40A-1PQ-3

Place near hot area

DB_TEMP2
MMBT2907A/SOT23/-600mA/50/X
VCCS_SOC → VCCS_SOC [32]
VSOC_TEMP → VSOC_TEMP [32]

Place near to DGL1

DB_TEMP1
MMBT2907A/SOT23/-600mA/50
VSOC_TEMP → VSOC_TEMP [32]
VCCS_SOC → VCCS_SOC [32]

0.3u footprint-->CHOKE0U3-R30M-JJ1W
0.3u capture value --> 0.3uH/50A/INCG109/FP/D

0.5u footprint-->CHOKE05U-40A-1PQ-3
0.5u capture value --> 0.5uH/32A/INCG109/FSI/D

L=0.3uH
DCR=0.67mohm
Idc=40A

GIGABYTE™

Title	SOC MOS
Size: Custom	Document Number: X570 UD
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Date:	Monday, June 24, 2019
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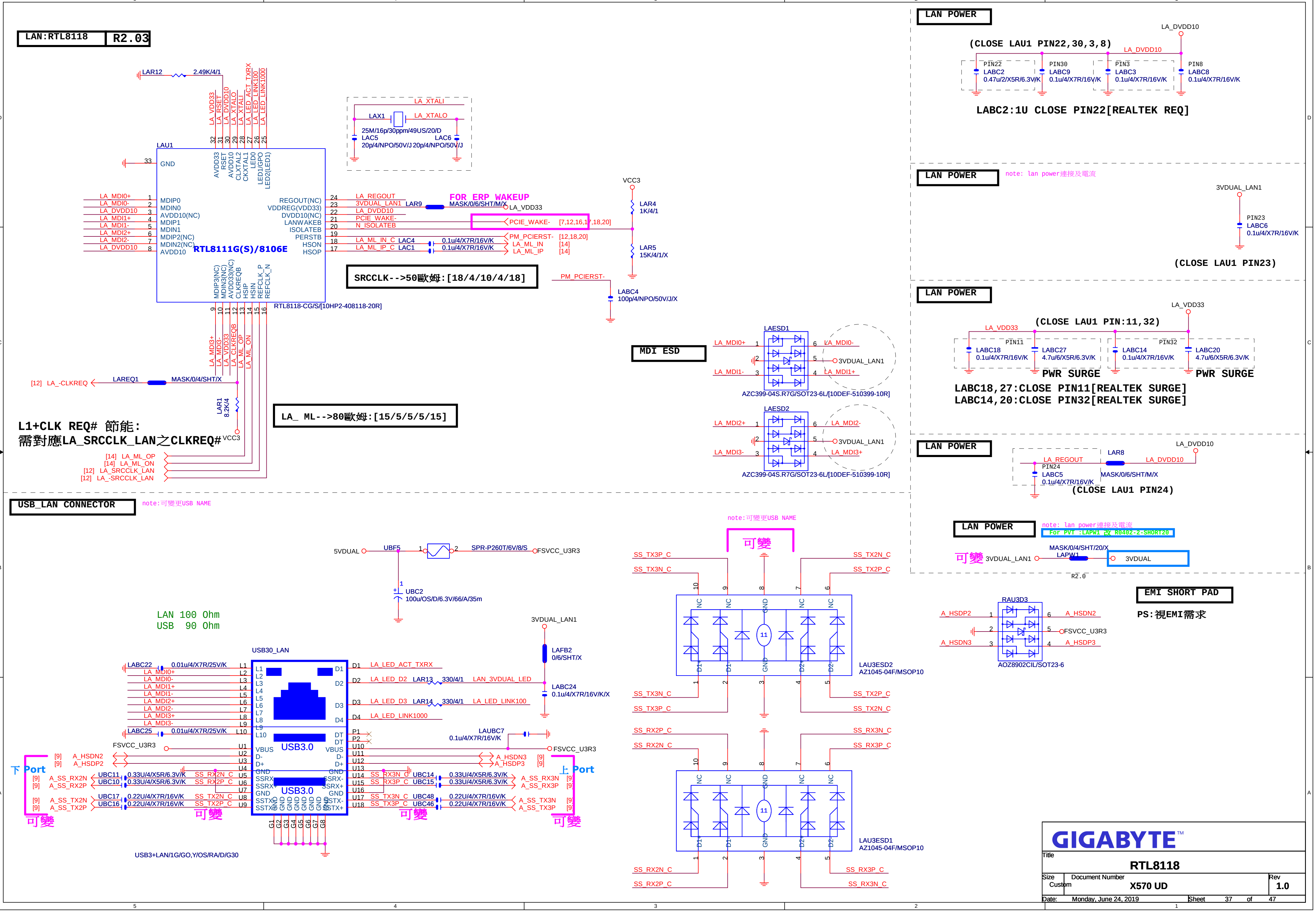

GIGABYTE™

Title
RTL8118

Size: Custom
Document Number: X570 UD
Rev: 1.0

Date: Monday, June 24, 2019
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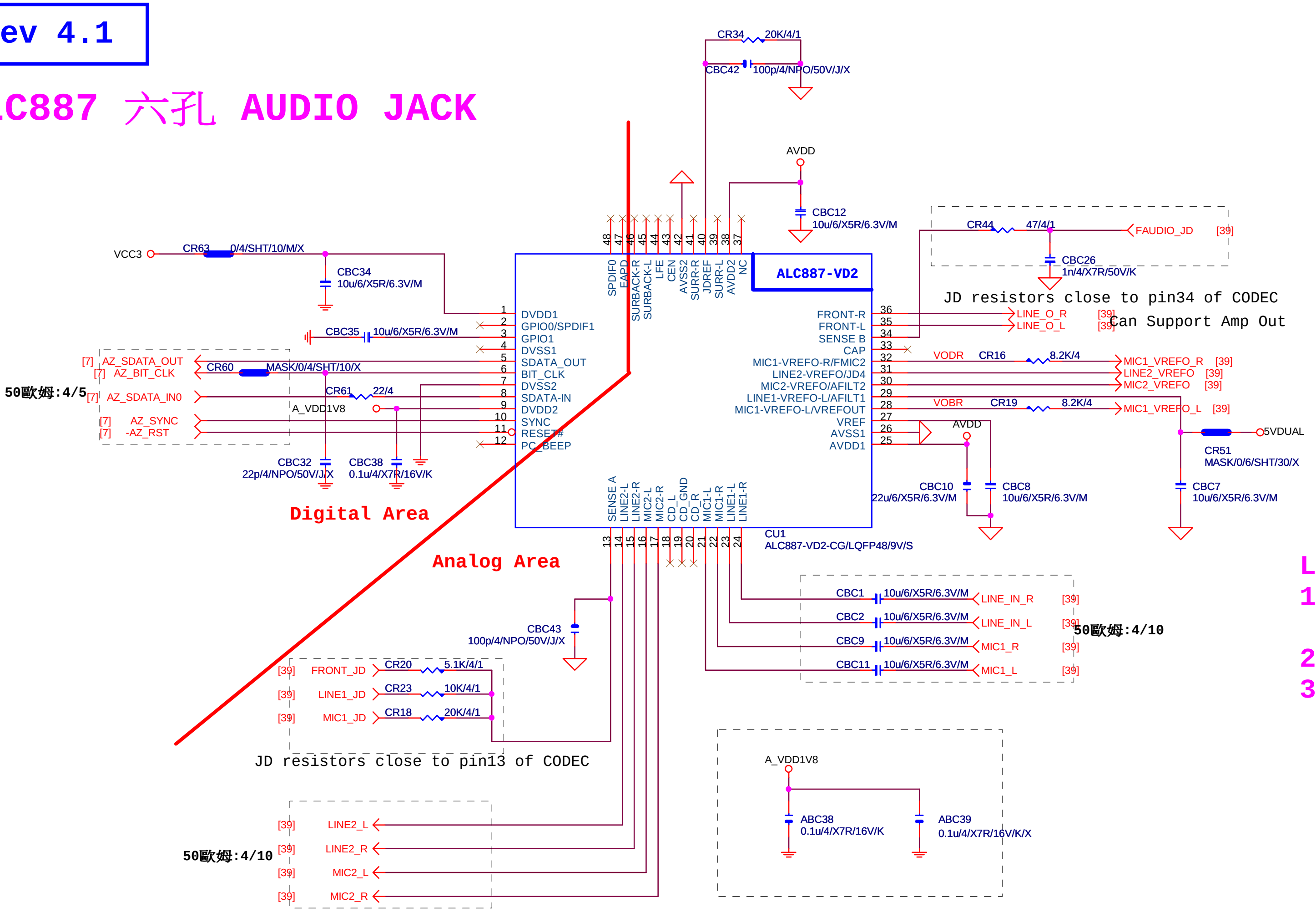
Rev 4.1

ALC887 六孔 AUDIO JACK

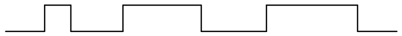


LAYOUT注意:螺絲孔下GND方式
1. MH1空間夠,下DGND
   空間不夠,才改為Isolate
2. MH2一律改為Isolate
3. Codec下方,第二層必須參考GND

○ MH1 DGND	MH2 ○ Isolate

LAYOUT注意:要加

GND切割線



音效區域印刷

BOM OPTION : 1. Chemicon音效電容
2. 金屬外罩 Reserve (LAYOUT上件與否,依照各Model spec)
3. LED Reserve (上件與否和LED顏色,依照各Model spec)

GIGABYTE™

Title
Realtek ALC887

Size Custom
Document Number X570 UD
Rev 1.0

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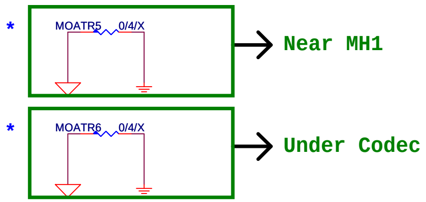
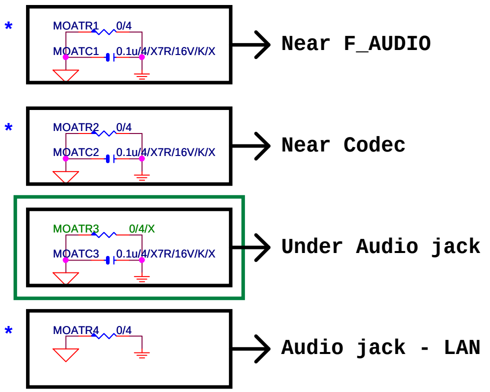
Rev 4.1



增加 for 實驗雜訊issue , 模組 not yet
用大陸反饋配備 ,底噪小聲,先移除

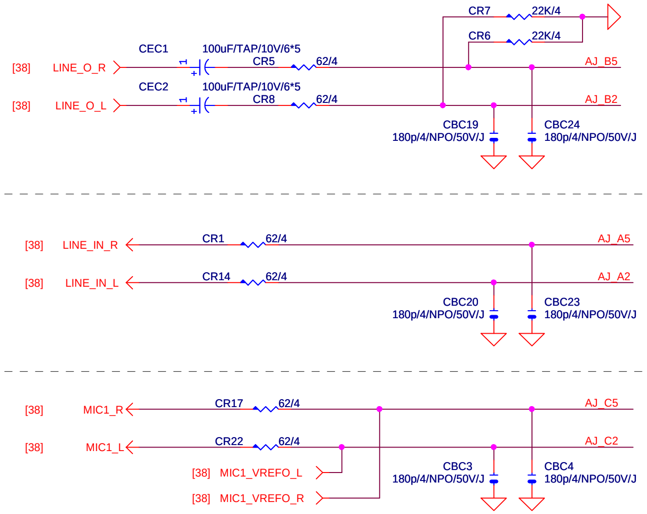


*量產前,MOATR1/MOATR2/MOATR4 ....0ohm改short pad

LINE-OUT

LINE-IN

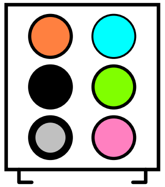
MIC-IN



SURROUND

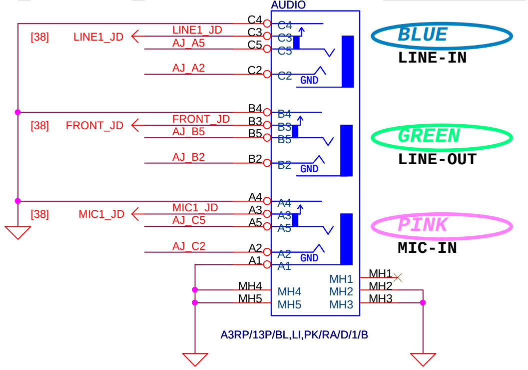
CEN/LFE

AZALIA JACK



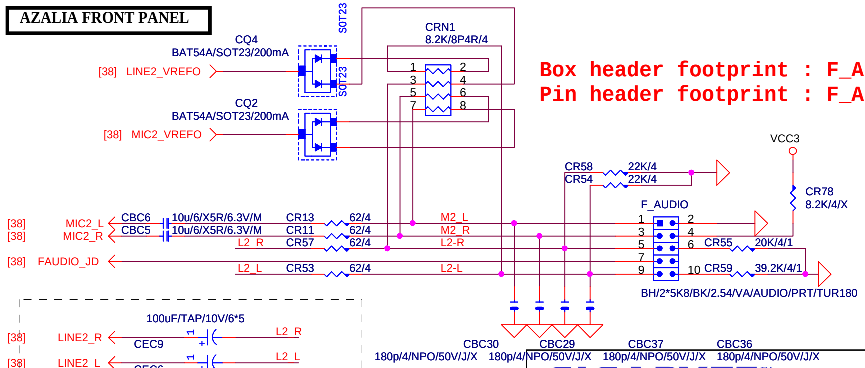
SURR BACK

AZALIA JACK



AZALIA FRONT PANEL

Box header footprint : F_AUDIO
Pin header footprint : F_AUDIO_S



GIGABYTE™

Title
AUDIO JACK

Size: Custom
Document Number: X570 UD
Rev: 1.0

Date: Monday, June 24, 2019
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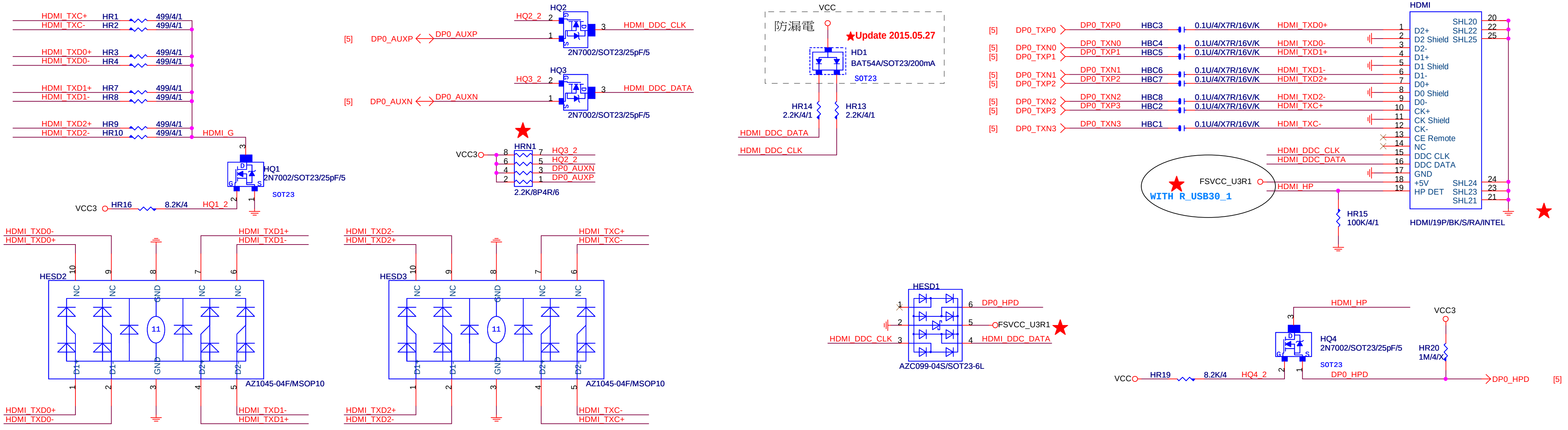


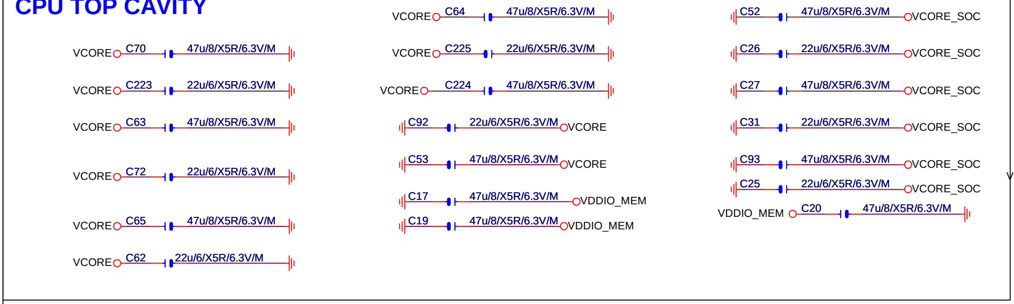
GIGABYTE™

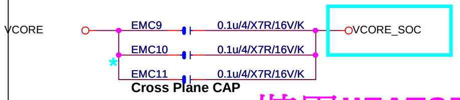
Title
HDMI

Size Custom
Document Number X570 UD
Rev 1.0

Date: Monday, June 24, 2019

CPU TOP CAVITY





裝甲HEATSINK 分成五大部份

*** PCB顏色 : 咖啡黑**

*** 文字面 : 灰色**

*** 圖騰 : 待確認ID**

GIGABYTE™

Title
TOP, ARMOR, HS

Size	Document Number	Rev
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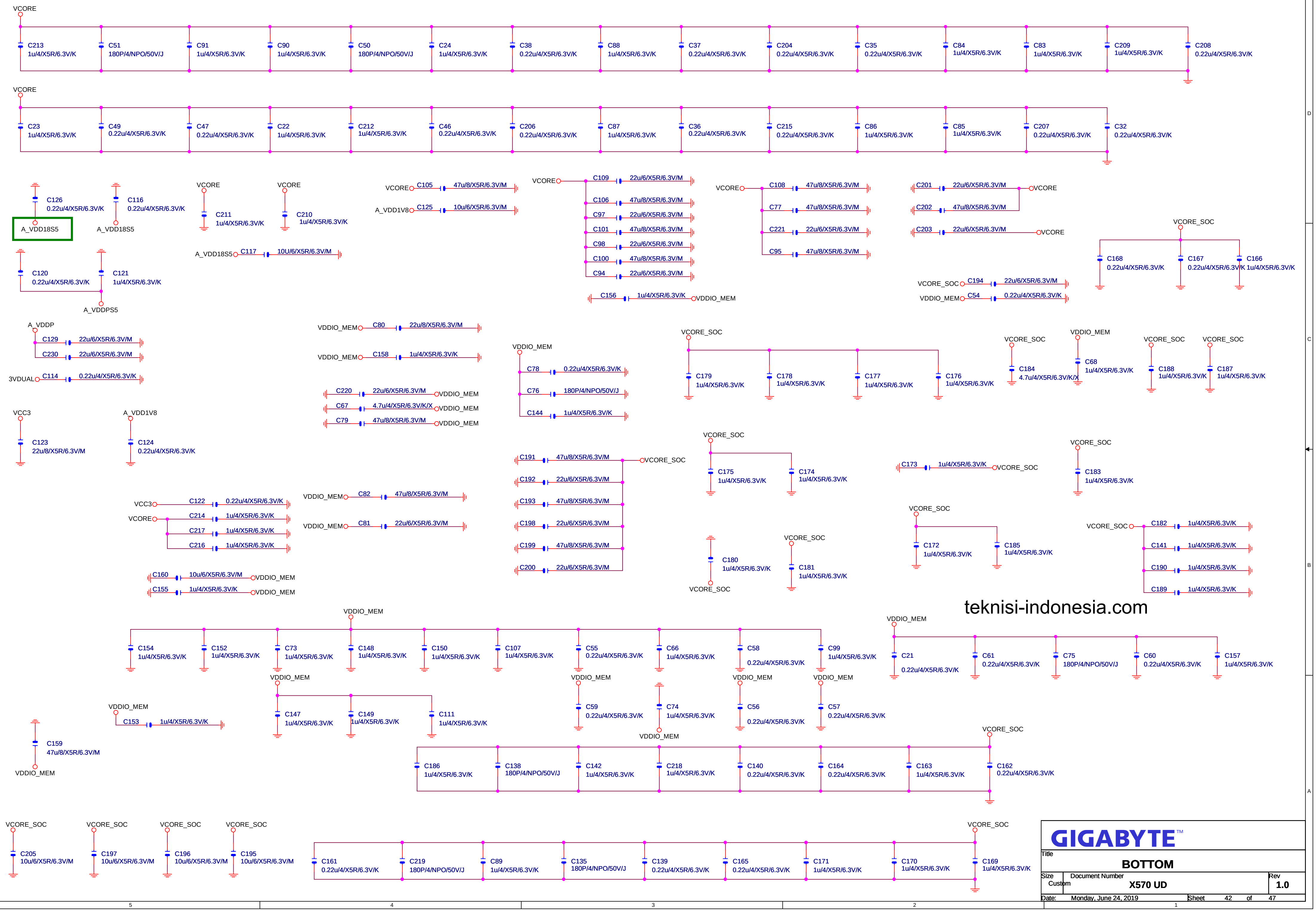

GIGABYTE™

Title	BOTTOM	
Size Custom	Document Number X570 UD	Rev 1.0
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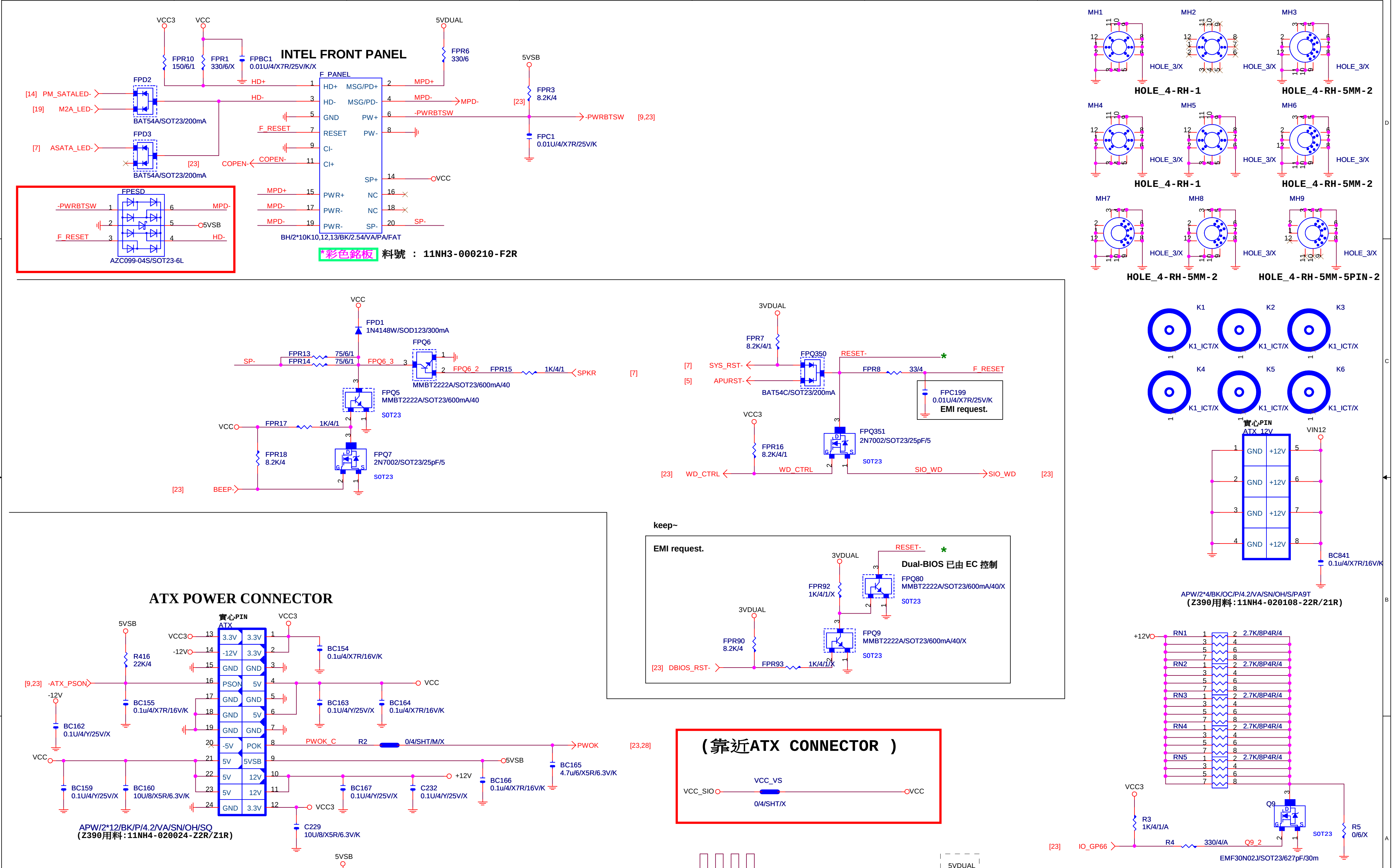

GIGABYTE™

Title
ATX, FRONT PANEL

Size: Custom
Document Number: X570 UD
Rev: 1.0

Date: Wednesday, July 03, 2019
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RGB LED LAYOUT 注意事項 :

1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)

2. 背板 RGB LED 方向整板請統一如下
(整板正極可統一朝下或朝上)

3. 正板 RGB LED 統一方向即可

4. MCU_PW & MCU_PW33電源一律走20mils

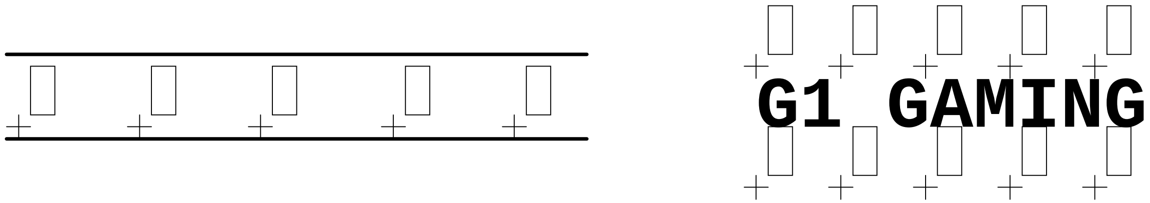
5. ECF1,ECF2,ECF3,ECF5 兩端電源走80mils或用鋪銅方式加粗

6. MCU LED 出pin的走線4mils,如:LED_R_1,LED_G_1,LED_B_1 ......

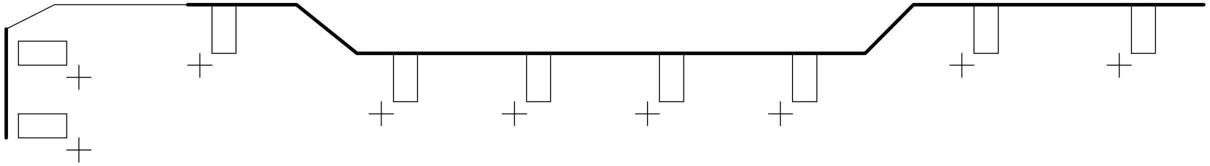
7. LED RGBW rule :W/S=10/5 mils 如:LED_R_11,LED_G_11,LED_B_11..
(包含從晶體到排阻到LED的net)

8. Digital LED NET rule W/S=4/8 mils
GPD0_SDA_B,GPD0_SDA_BB,GPD0_SDA_C,GPD0_SDA_CC

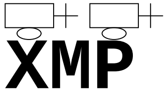
PCB板邊透光model name鏤空+背面 RGB LED



Audio Ground切割線+背面 RGB LED



"XMP"字樣鏤空+背面 RGB測發光 LED



GIGABYTE™
Title
LAYOUT GUIDE
Size Custom
Document Number X570 UD
Rev 1.0
Date: Monday, June 24, 2019
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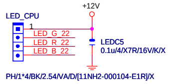
第一區 LED

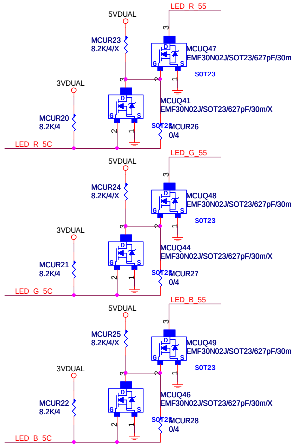
第二區 LED

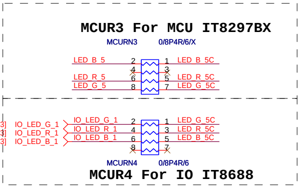
燈條 LED (LED_CPU放在CPU附近位置)



Footprint "PH1X4-FAN-AMD"

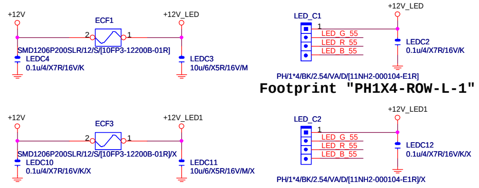
第五區 LED CONTROL





燈條 LED (LED_C1放在PCB左邊板邊位置)

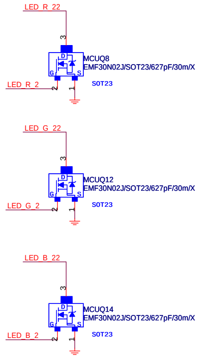
燈條 LED (LED_C2放在PCB右邊板邊位置)

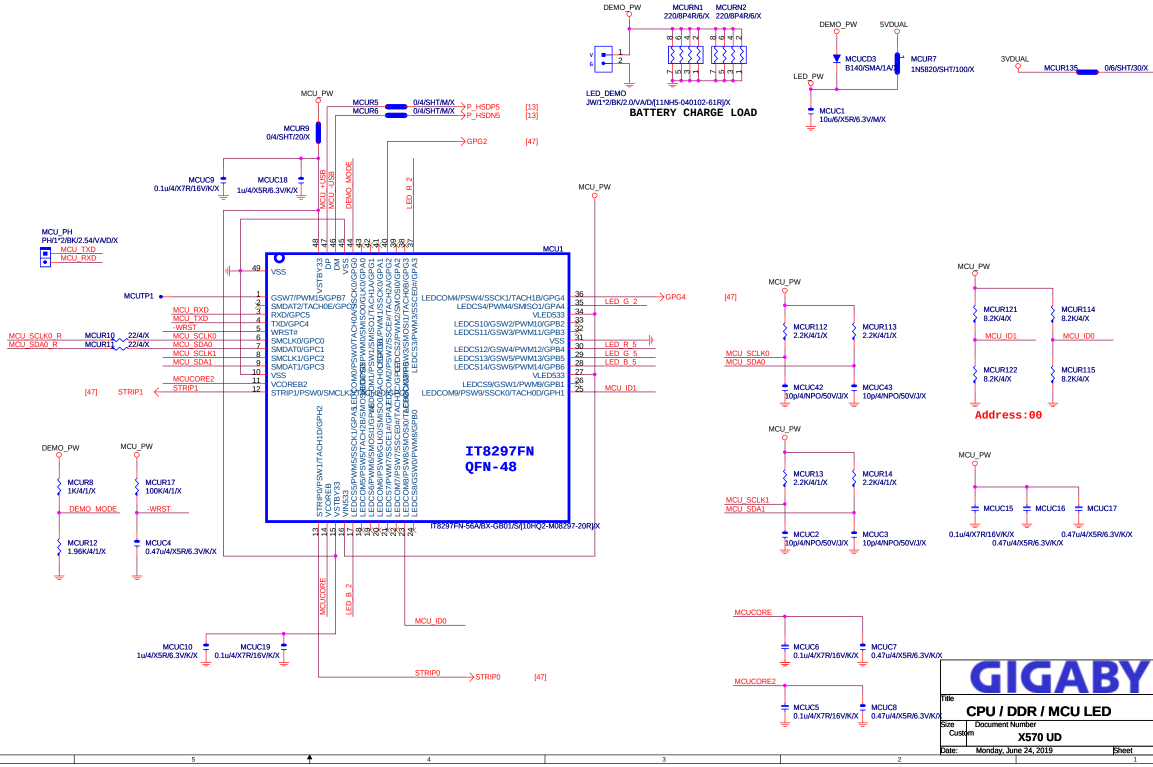


Footprint "PH1X4-ROW-L-1"

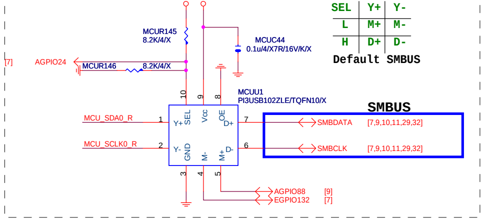
Footprint "PH1X4-ROW-R-1"

第二區 LED CONTROL



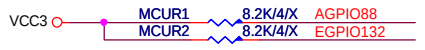


For AMD MCU update



SEL	Y+	Y-
L	M+	M-
H	D+	D-

Default SMBUS



GIGABYTE

Title: CPU / DDR / MCU LED

Size: Custom

Document Number: X570 UD

Rev: 1.0

Date: Monday, June 24, 2019

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Rev 4.0

第三區 LED

第四區 LED

GIGABYTE™

Title
MODEL / PCB /AUDIO/PCIE LED

Size Custom	Document Number **X570 UD**	Rev **1.0**
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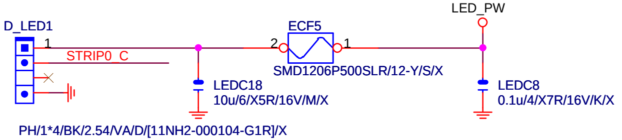
Rev 4.0

第六區 LED (靠近左上板邊位置)

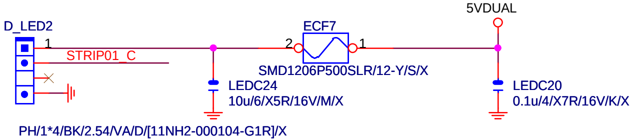
(靠近右下CPU板邊位置)

Digital LED Strip1



Footprint "PH1X4-CUT3-LED-L"

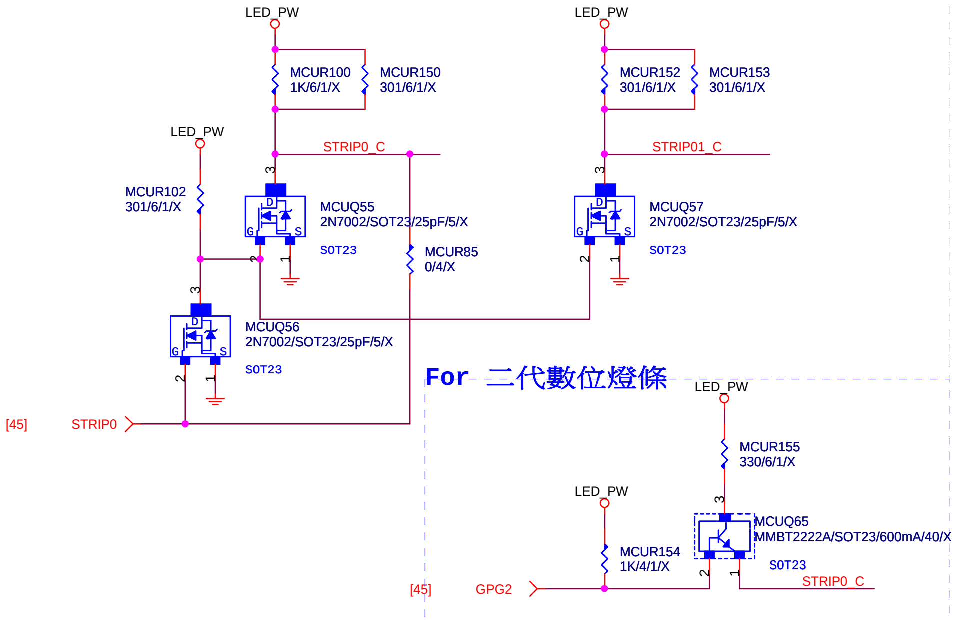
Digital LED Strip2



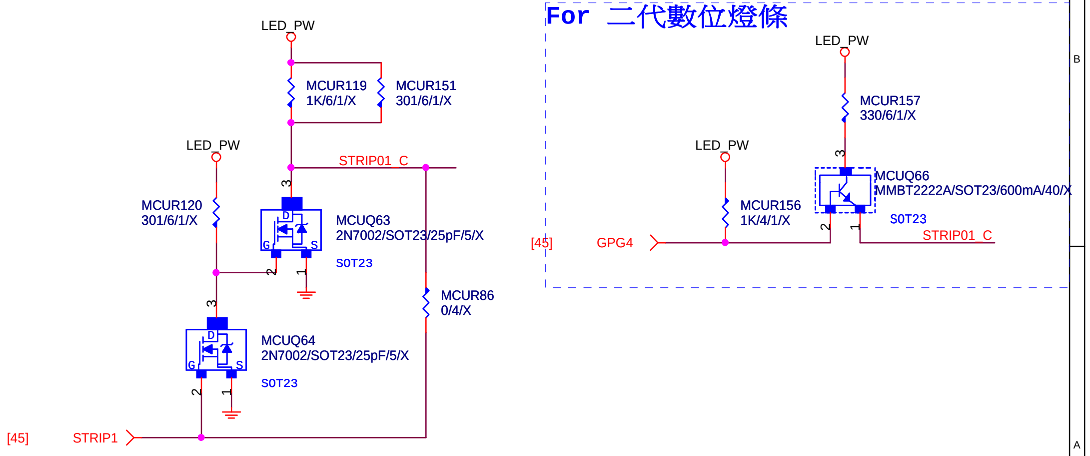
Footprint "PH1X4-CUT3-LED-R"

(for pin-name 與 model-name 同方向)

燈條 Level shift



燈條 Level shift



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