MS-7676

UATX Ver:20

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH

OnBoard Chipset:

Clock Gen:IDT 4105
HD Audio Codec:RTL892
LAN:RTL 8111E 10/100/1000
SIO:FIN71889AD
Flash ROM: 64 Mb SPI (PCH)* 2

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X4) Slot * 1
PCI Express (X1) Slot * 2

PWM:

Controller:VRD12 UPI6234 (6+2-Phase)Dr.MOS

CPU+GPU
Controller:uP6113 Dr.MOS
CPU VTT CPU SA
Controller:uP6103A
DDR PCH

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX4 Front x8(PCH)
USB3.0 RearX2 (NEC uPD720200)
1394 Controller - VT6315N-CE
D-SUB *1
DVI-D PORT*1
HDMI *1
TPM Header *1
COM Header *1
on BOARD BUZZER

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MS-7676

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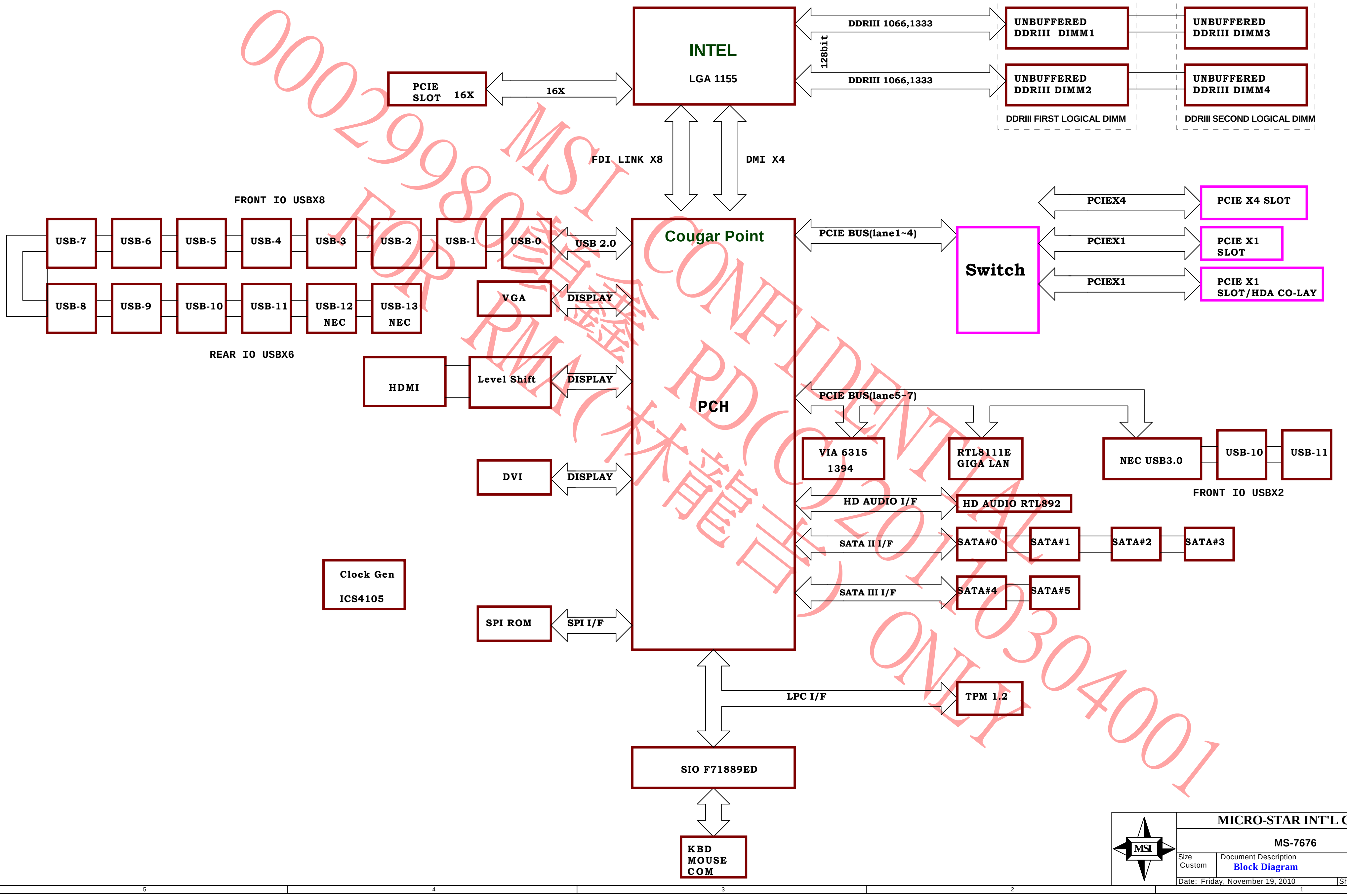
INTEL CONFIDENTIAL



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MS-7676		
Size: Custom	Document Description: Block Diagram	Rev: 20
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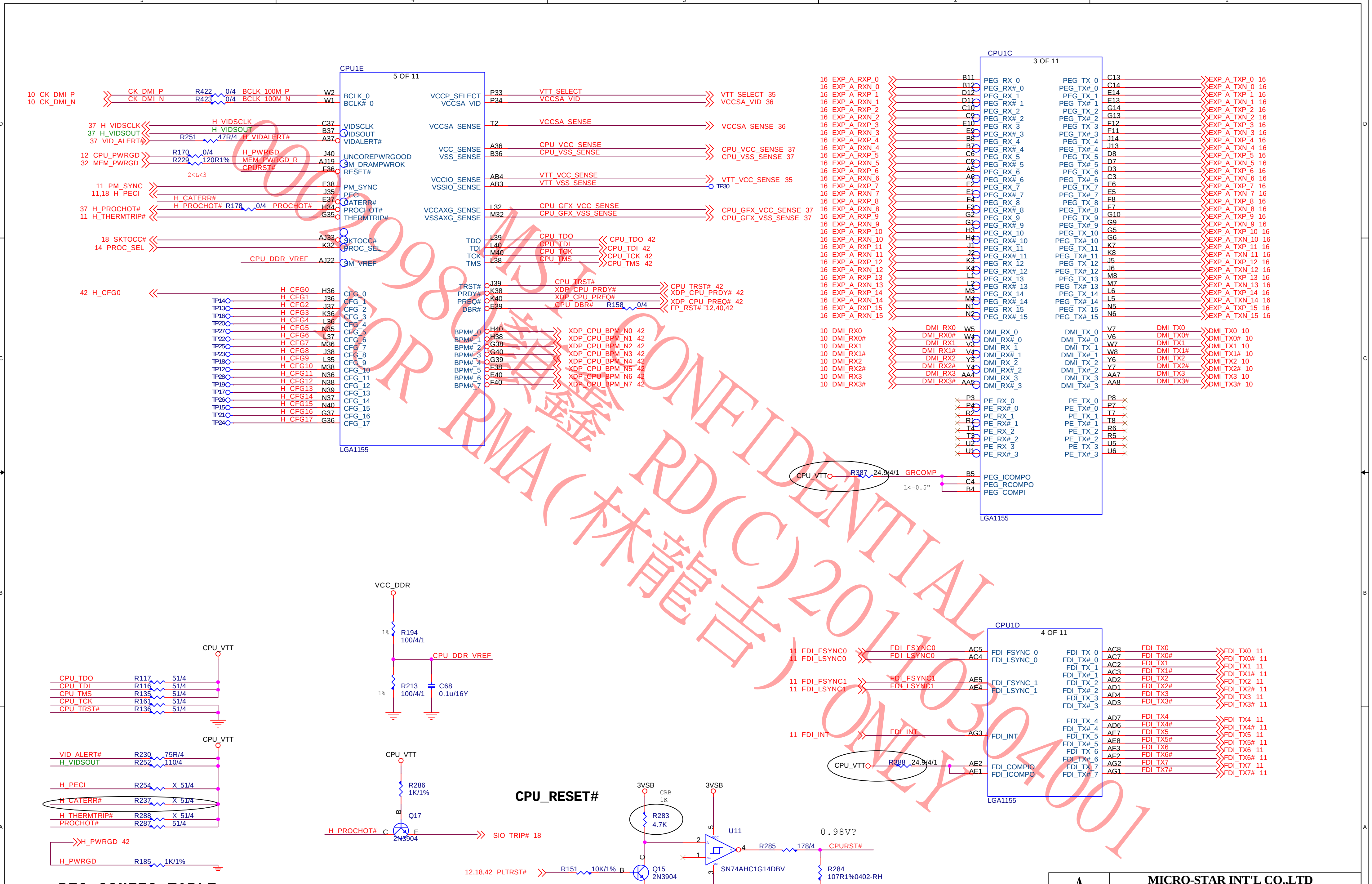

PEG CONFIG TABLE

SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

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Custom	CPU-CLK/Control/MISC/PEG	20

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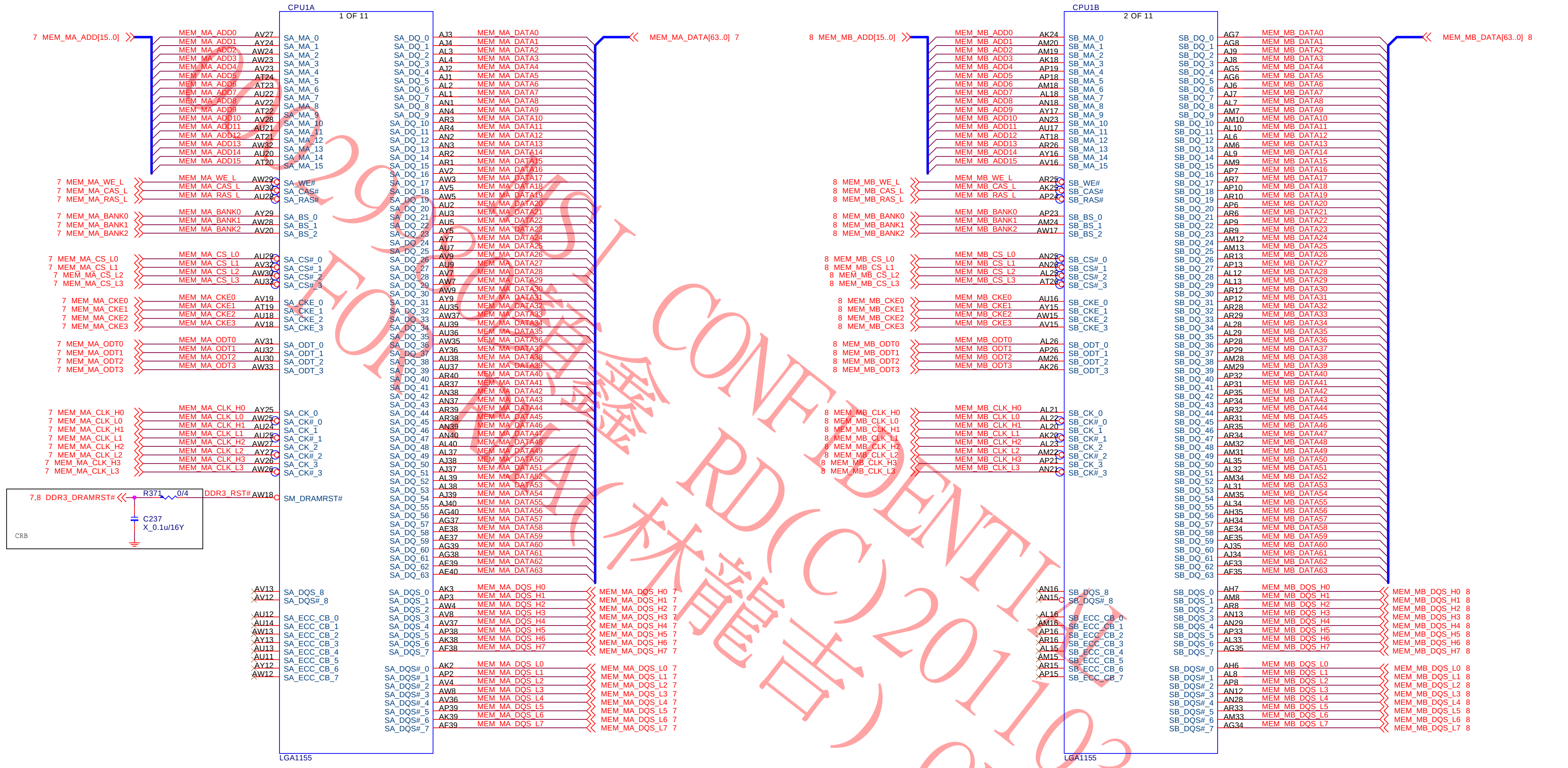

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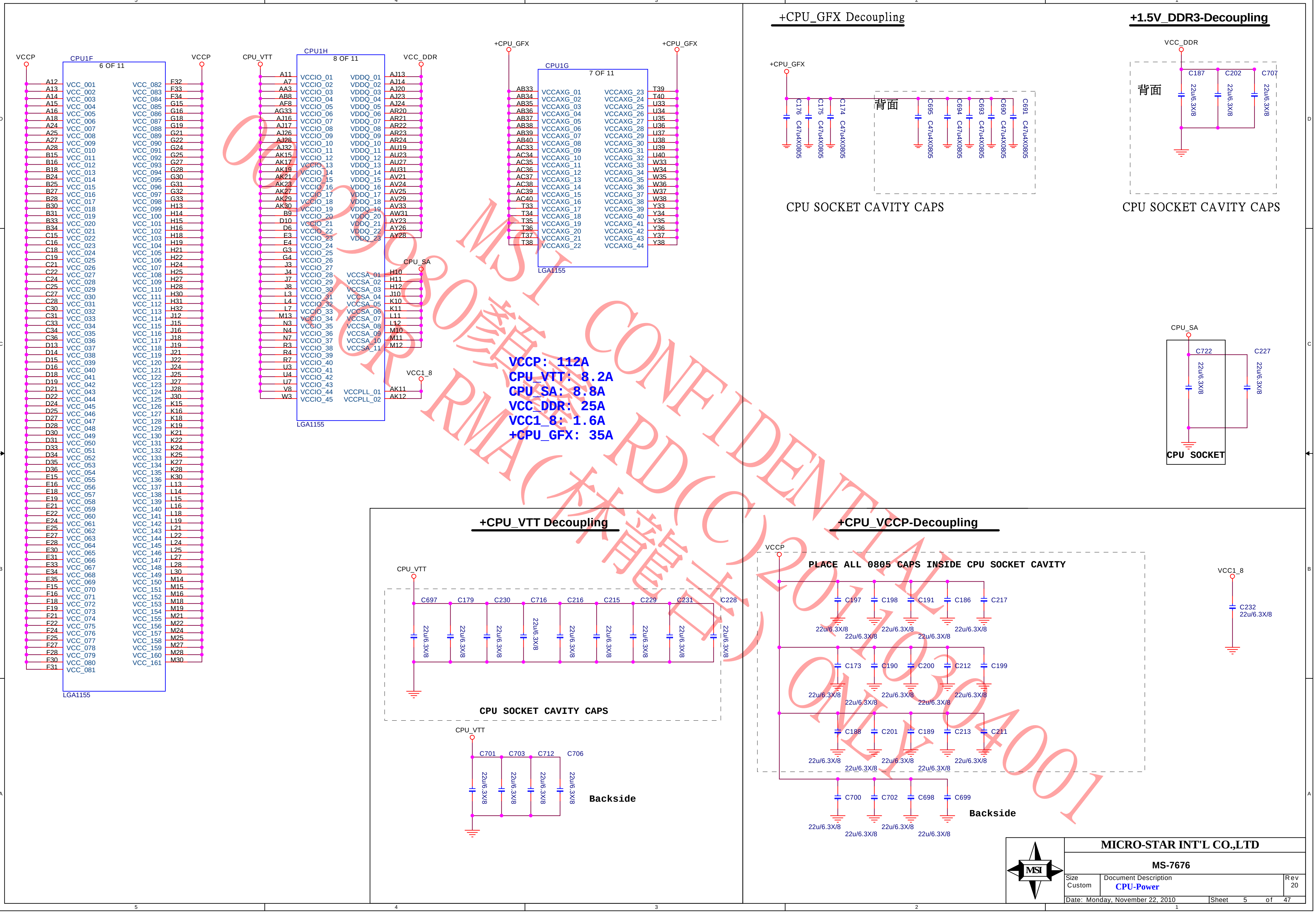

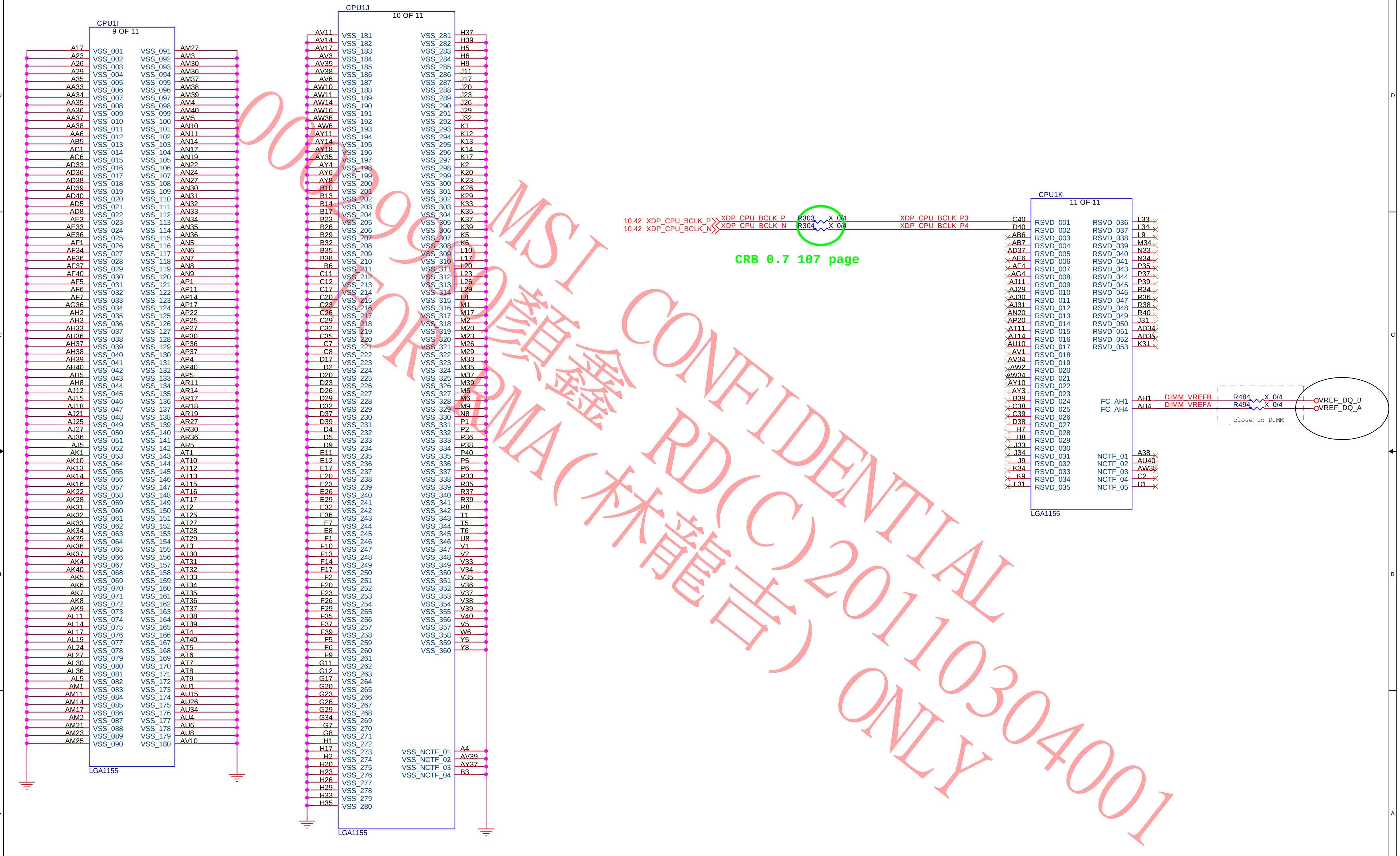

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Size	Document Description	Rev
Custom	CPU-GND	20

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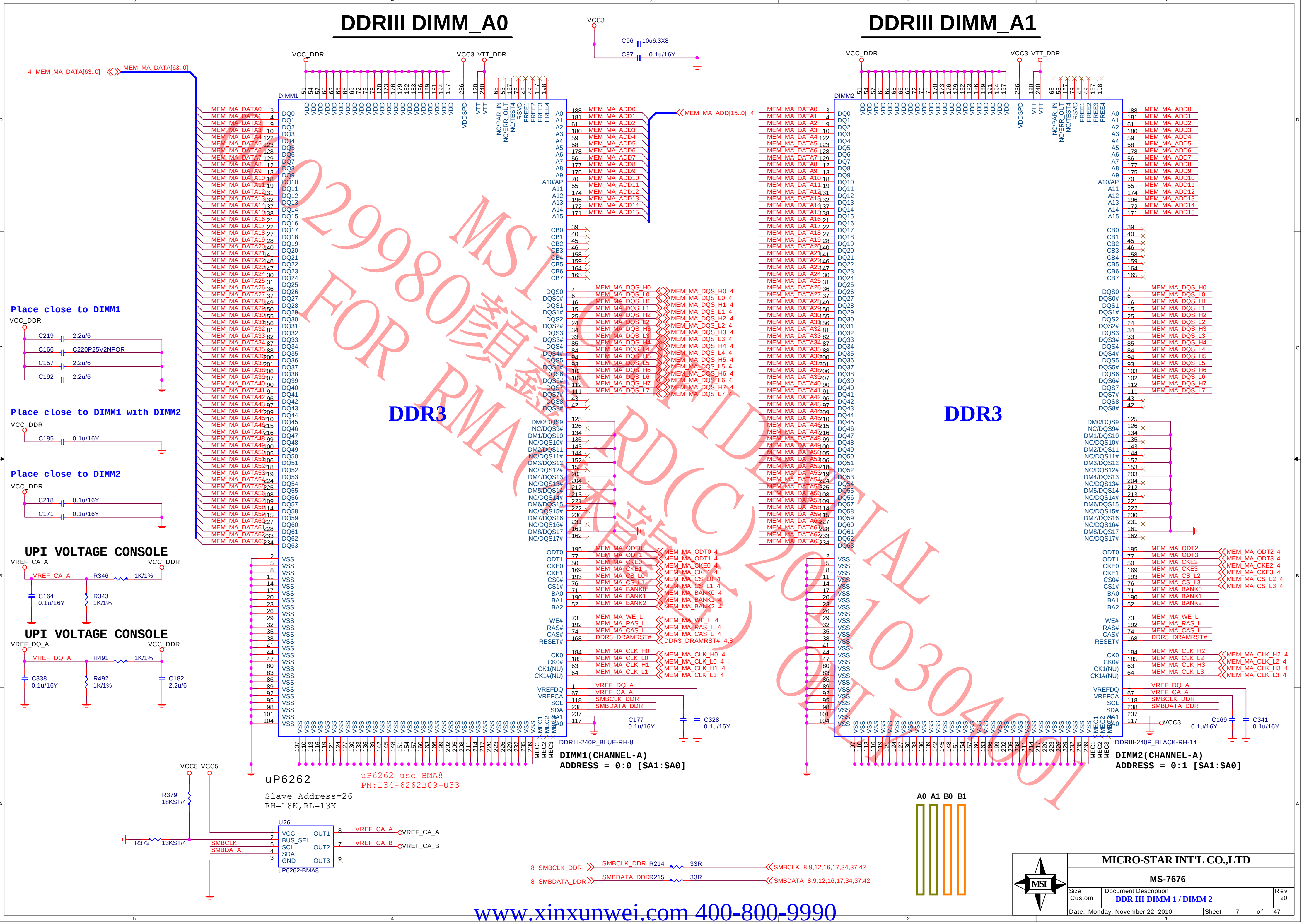
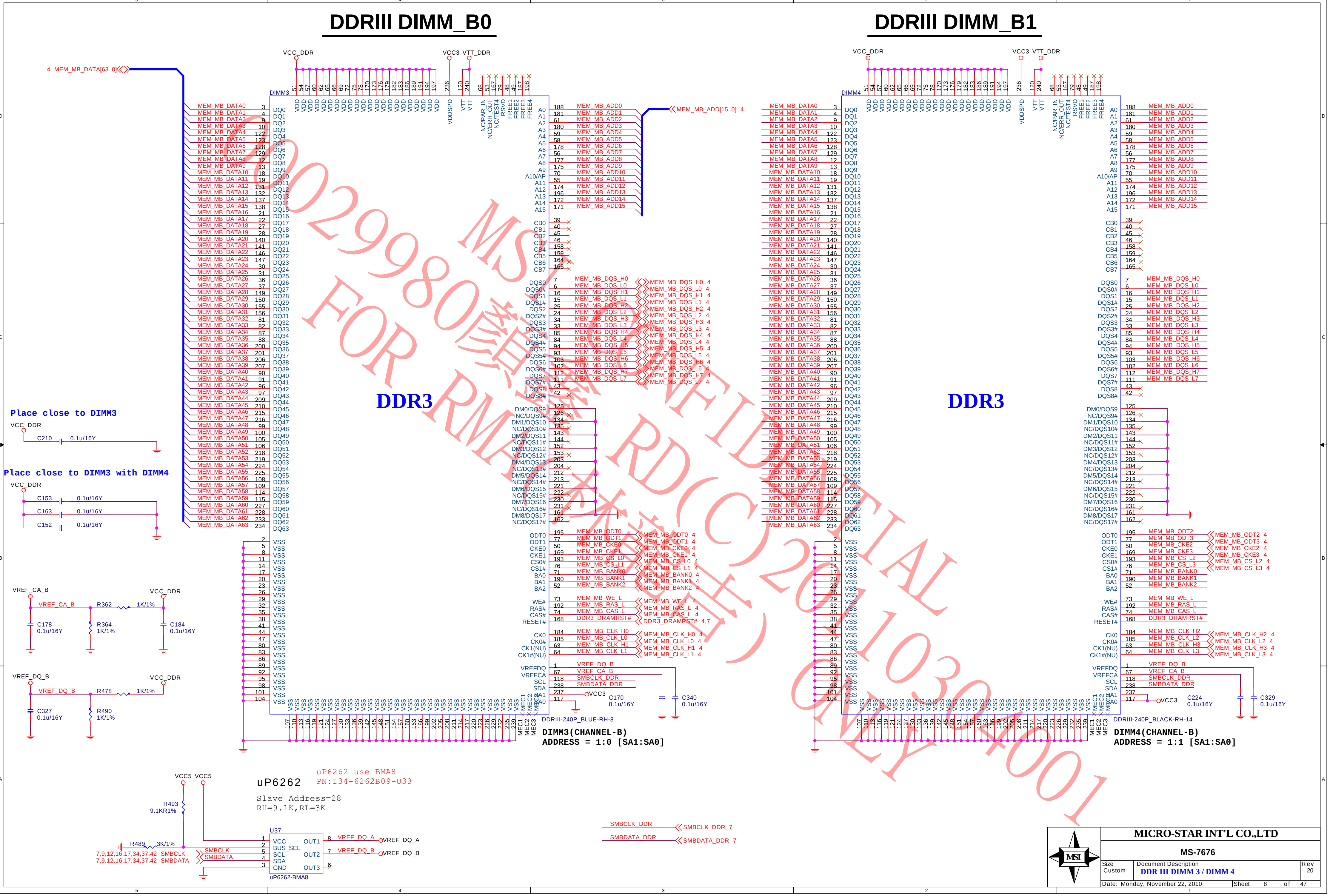
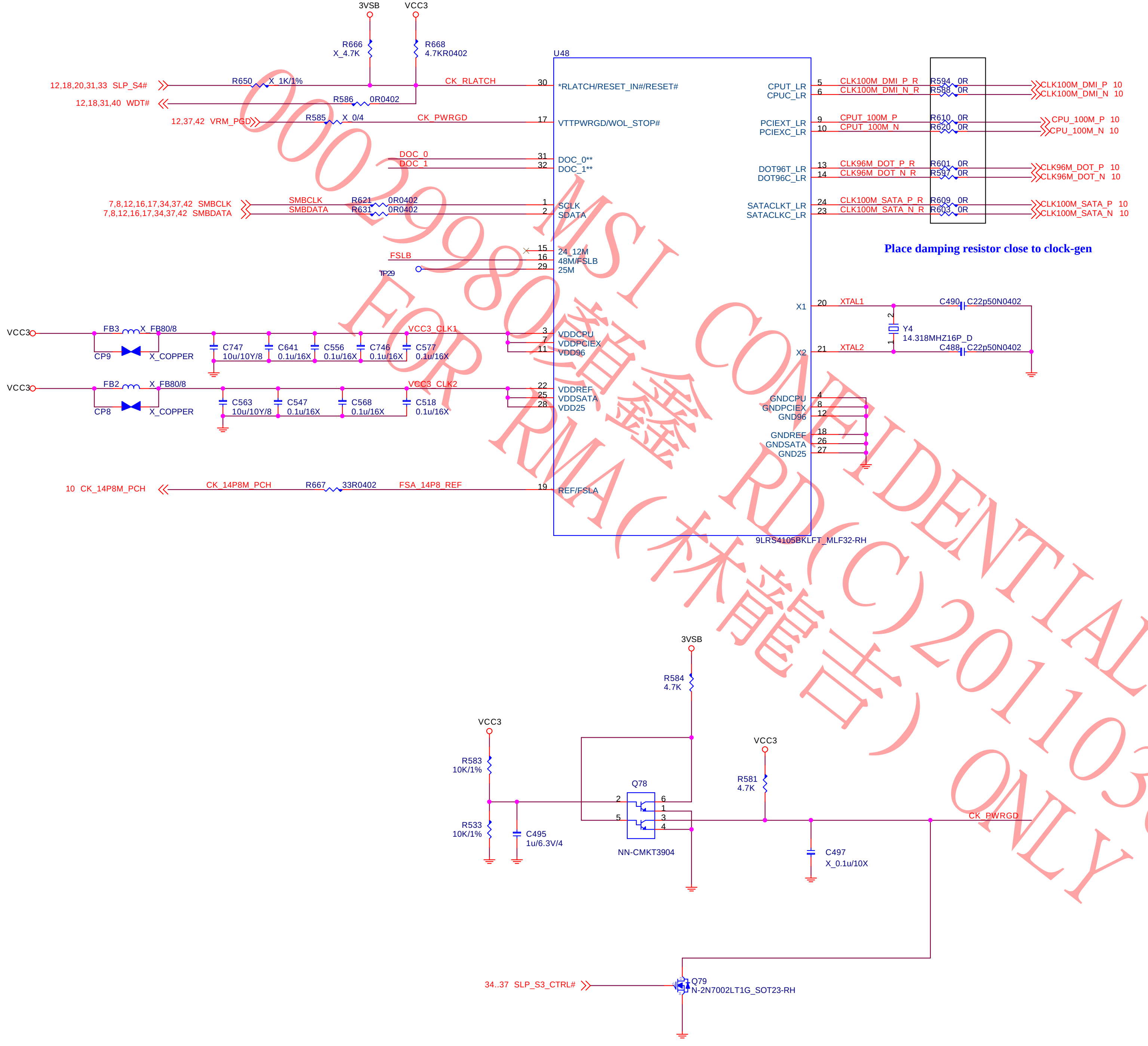
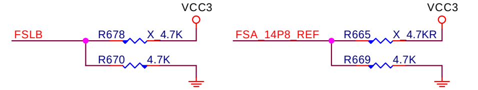






CLOCK GEN STRAPING

FS4 B0b4	FS3 B0b3	FS2 B0b2	FSB B0b1	FSA B0b0	CPU Mhz	Spread %
0	0	0	0	0	100.00	-0.5
0	0	0	0	1	133.33	-0.5
0	0	0	1	0	200.00	-0.5
0	0	0	1	1	166.66	-0.5

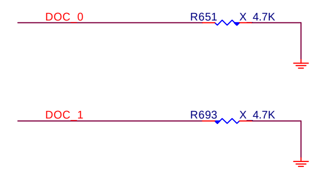


Pin16: 48MHz clock output. / 3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values.

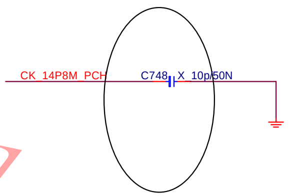
Pin19: 14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.

OC

DOC_0:Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2C.**



EMI



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Size: Custom	Document Description: CLK GEN4105	Rev: 20
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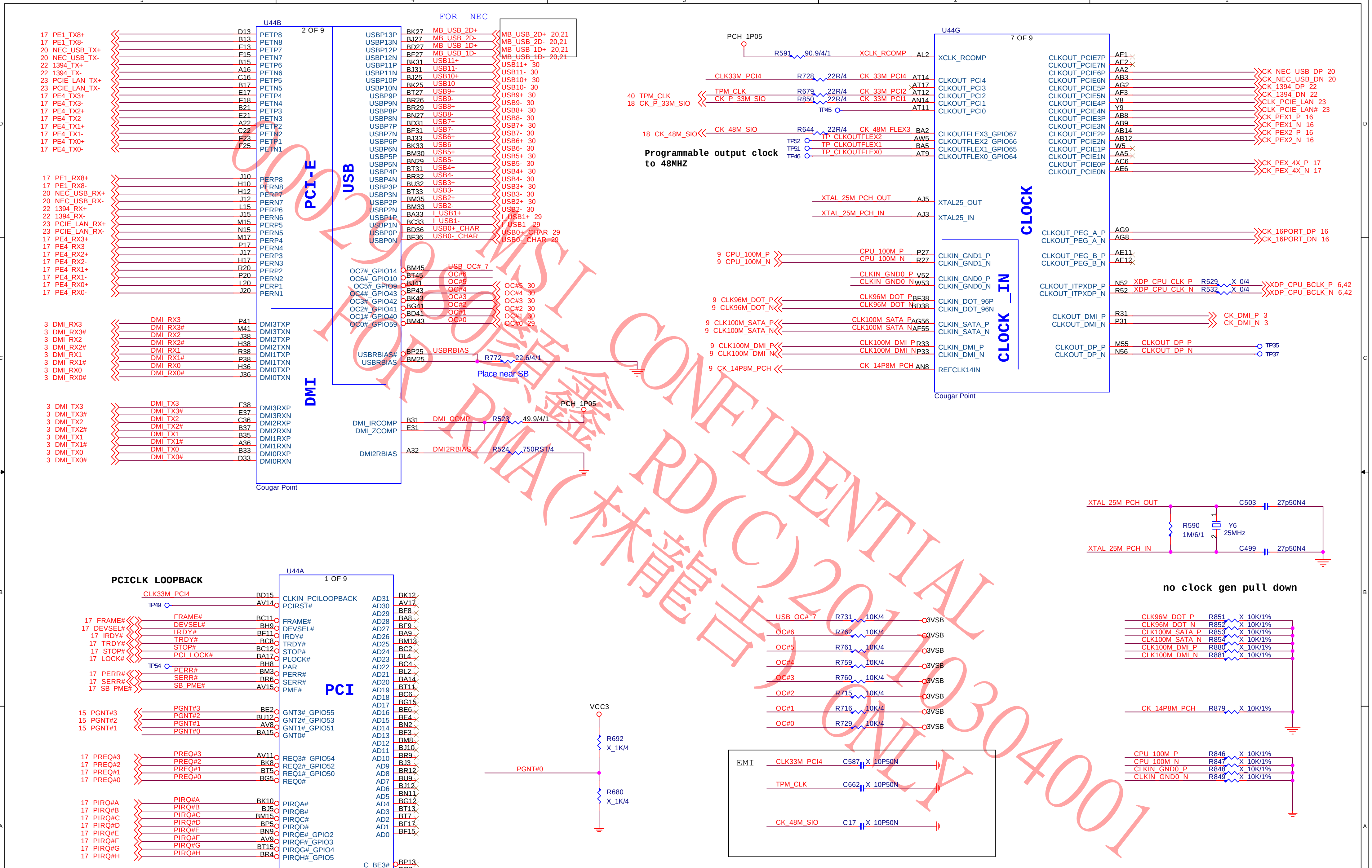

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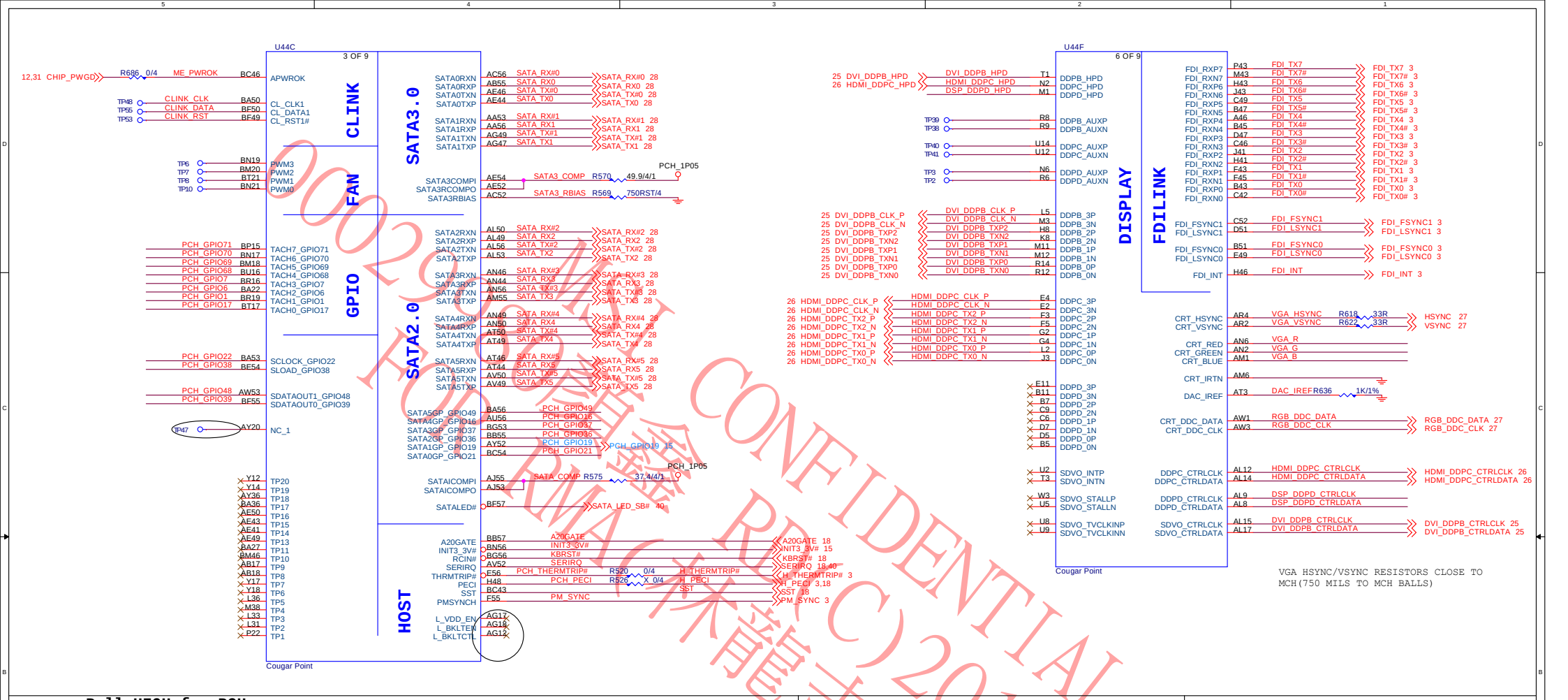

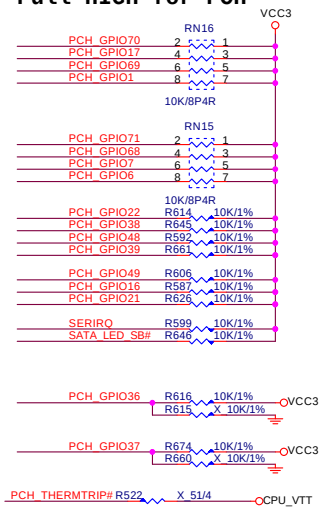

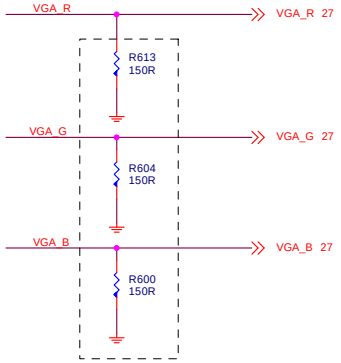

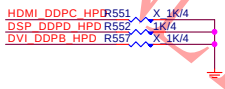

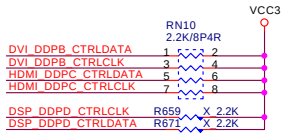

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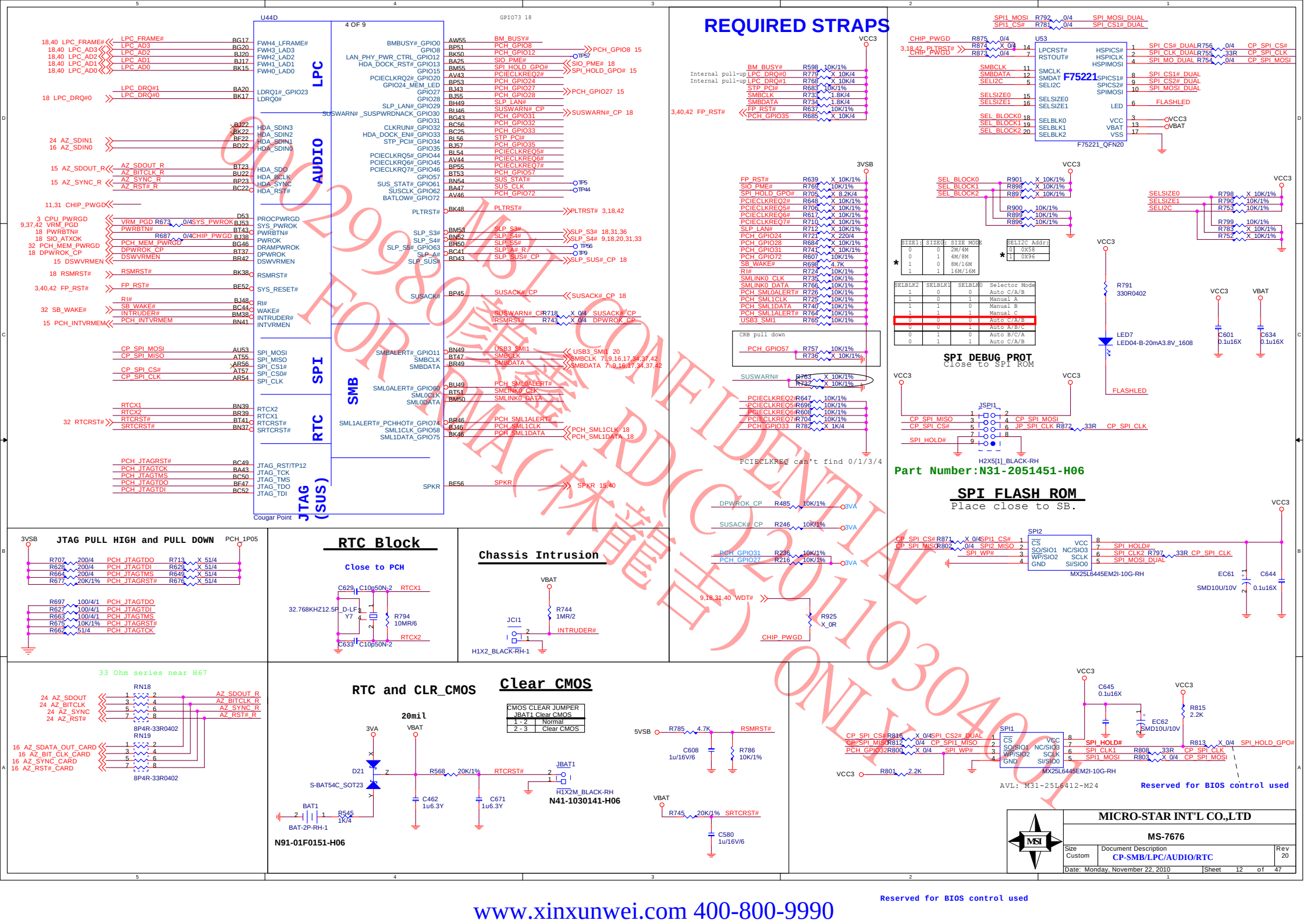
REQUIRED STRAPS
SPI DEBUG PROT
Close to SPI ROM
Part Number:N31-2051451-H06
SPI FLASH ROM
Place close to SB.
JTAG PULL HIGH and PULL DOWN
RTC Block
Close to PCH
Chassis Intrusion
RTC and CLR_CMOS
Clear CMOS
CMOS CLEAR JUMPER
JBAT1 Clear CMOS
1 - 2 Normal
2 - 3 Clear CMOS
N91-01F0151-H06
N41-1030141-H06
MICRO-STAR INT'L CO.,LTD
MS-7676
CP-SMB/LPC/AUDIO/RTC
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Reserved for BIOS control used
www.xinxunwei.com 400-800-9990

Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

PCH_1P05

R514 X_0/8 VCCAFDIPLL
C414 10u6.3X8

R595 X_0/4 VCCACLK
NO THIS PIN

R515 X_0/8 VCCAPLLDMI2
C417 10u6.3X8
C424 1u/6.3V/4

R642 0/8 VCCCLKDMI
C553 10u6.3X8
C554 1u/6.3V/4

R535 0/8 VCCA_DPLLA
EC46 CD100u16SO-RH-2
C460 10u6.3X8
C472 1u/6.3V/4

R572 0/8 VCCA_DPLLB
EC47 CD100u16SO-RH-2
C477 10u6.3X8
C478 1u/6.3V/4

PCH_1P05

DMI PLL FILTER

L21 X_L1U_500mA_0805
VCCAPLLEXP
C418 10u6.3X8
C425 1u/6.3V/4

SATA PLL FILTER

L22 X_L10U_100mA_0805
VCCAPLLSATA
C458 10u6.3X8
C464 1u/6.3V/4

PCH_1P05

U44H
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CPU_VTT
D55 V_PROC_IO
B56 V_PROC_IO_NCTF

CPU_VTT
B41 VCCDMI_02
E41 VCCDMI_01

C428 1u/6.3V/4
VCCAPLLDMI2 A19 VCCAPLLDMI2
VCCCLKDMI AJ20 VCCCLKDMI

5VREF BF1 V5REF
5VREF_SUS BT25 V5REF_SUS

+3.3V_DAC
AT1 VCCADAC
VCCACLK AL5 VCCACLK

VCCA_DPLLA AB1 VCCADPLLA
VCCA_DPLLB AC2 VCCADPLLB

VCCAPLLSATA U56 VCCAPLLSATA
VCCAPLLEXP B53 VCCAPLLEXP
VCCAFDIPLL C54 VCCAFDIPLL

PCH_1P05 R549 X_0/8
3VSB AV28 VCCSUSHDA
VCC3 AN52 VCCSPI
VCC1_8 R548 0/8 R2 VCCVRM_04
R54 VCCVRM_03
R56 VCCVRM_02
AJ1 VCCVRM_01

C427 1u/6.3V/4 DCPSUS A39 DCPSUS_03
TP43 AT41 DCPSUS_02
TP42 AA32 DCPSUS_01

C578 0.1u/10X DCPRTC BR54 DCPRTC
BT56 DCPRTC_NCTF

TP50 AV41 DCPSUSBYP
C520 0.1u/10X DCPSST BA46 DCPSST

3VA C738 0.1u/10X
VBAT BU42
AV40 VCCRTC
VCCDSW3_3

PCH_1P05 AG15 VCCDIFFCLKN_03
AE17 VCCDIFFCLKN_02
AE15 VCCDIFFCLKN_01

VCCSSC_02 AE20
VCCSSC_01 AC20

VCCDFTERM T57
VCCDFTERM T55

VCC3_3_10 AV20
VCC3_3_09 AU20
VCC3_3_08 AU22
VCC3_3_07 AN38
VCC3_3_06 AL38
VCC3_3_05 BD20
VCC3_3_04 BD17
VCC3_3_03 BC12
VCC3_3_02 AE57
VCC3_3_01

VCCSUS3_3_011 BT35
VCCSUS3_3_010 AU38
VCCSUS3_3_009 AT40
VCCSUS3_3_008 BK36
VCCSUS3_3_007 BK36
VCCSUS3_3_006 B136
VCCSUS3_3_005 AY33
VCCSUS3_3_004 AY31
VCCSUS3_3_003 AY32
VCCSUS3_3_002 AY30
VCCSUS3_3_001 U31

3VSB
VCC3

PCH_1P05 CP5 X_COPPER VCCSSC

VCCNAND
VCC1_8 R554 0/6
VCC3 R558 X_0/6
C454 X_0.1u/16Y

Cougar Point

PCH_1P05

VCCCORE_022 AR34
VCCCORE_021 AR32
VCCCORE_020 AN34
VCCCORE_019 AN32
VCCCORE_018 AL34
VCCCORE_017 AL32
VCCCORE_016 AJ36
VCCCORE_015 AJ34
VCCCORE_014 AJ32
VCCCORE_013 AG34
VCCCORE_012 AG32
VCCCORE_011 AE36
VCCCORE_010 AE34
VCCCORE_009 AE32
VCCCORE_008 AE30
VCCCORE_007 AE28
VCCCORE_006 AE24
VCCCORE_005 AC32
VCCCORE_004 AC30
VCCCORE_003 AC28
VCCCORE_002 AC26
VCCCORE_001 AC24

VCCASW_023 AU36
VCCASW_022 AU30
VCCASW_021 AR38
VCCASW_020 AR36
VCCASW_019 AR30
VCCASW_018 AR28
VCCASW_017 AR26
VCCASW_016 AR24
VCCASW_015 AN28
VCCASW_014 AN26
VCCASW_013 AN24
VCCASW_012 AN22
VCCASW_011 AL28
VCCASW_010 AL24
VCCASW_009 AJ28
VCCASW_008 AJ26
VCCASW_007 AJ24
VCCASW_006 AG28
VCCASW_005 AG26
VCCASW_004 AG24
VCCASW_003 AU34
VCCASW_002 AV36
VCCASW_001 AU32

POWER

PCH_1P05: 7.66A
CPU_VTT: 0.058A
VCC1_8: 0.159A
VCC3: 0.697A
3VSB: 0.11A
5VREF: 0.001A
5VREF_SUS: 0.001A

5VREF & 5VREF_SUS Sequencing Circuit

VCC3 Q64 2N3904
C565 1u/6.3V/4
VCC5 R699 10/4 5VREF
C564 0.1u16X

3VSB Q69 2N3904
C605 0.1u16X
5VSB R780 100/4/1 5VREF_SUS
C597 0.1u16X

VCC3 CP4 X_COPPER +3.3V_DAC
Near ball AF1
C536 0.1u/10X

PCH decoupling cap

VBAT C604 C611 1uF/10V/Y5V/6
0.1u/16Y

VCC3 C482 C575 C491 C431 C537 C594 C583 1uF/10V/Y5V/6
0.1u/16Y X_0.1u/16Y 0.1u/16Y 4.7uf/10V/X5R/8

CPU_VTT C412 C421 C429 0.1u/16Y
4.7uf/10V/X5R/8

3VSB C586 C595 0.1u/16Y
0.1u/16Y

PCH_1P05 C729 C402 C411 C734 C410 C457 C735 C733 C731 C737 C736 C732 0.1u/16Y
10u6.3X8 1uF/10V/Y5V/6 10u6.3X8 1uF/10V/Y5V/6 10u6.3X8 4.7uf/10V/X5R/8 10u6.3X8 1uF/10V/Y5V/6 0.1u/16Y X_0.1u/16Y X_0.1u/16Y

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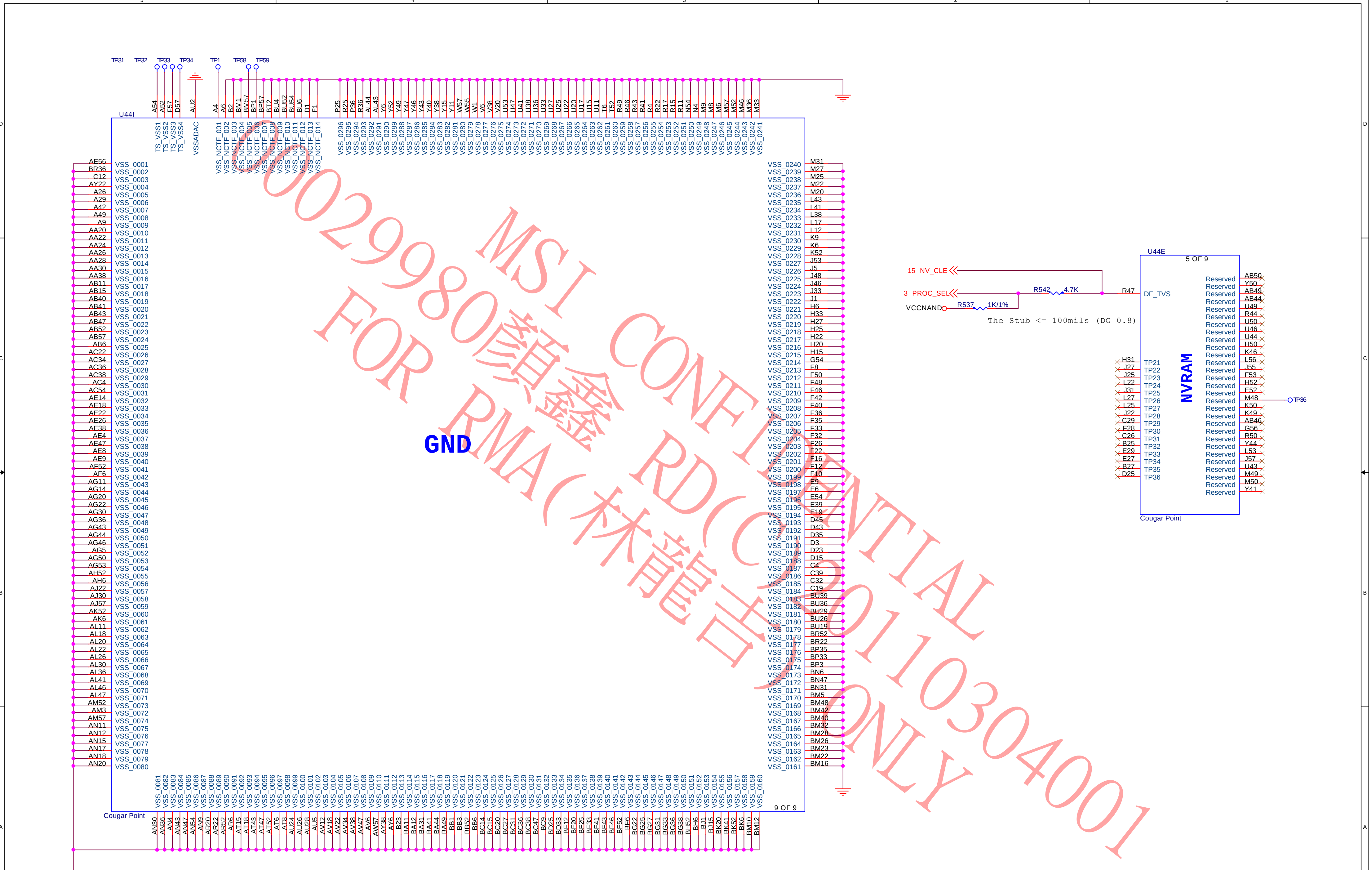

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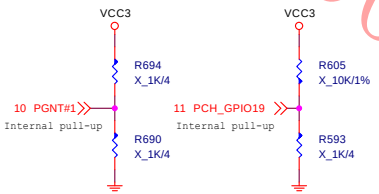
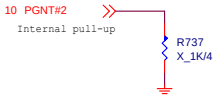
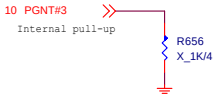
PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

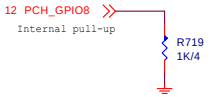




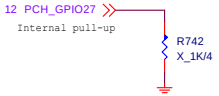
DMI AC/DC MODE
0 : AC
1 : DC *



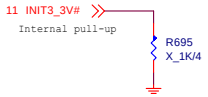
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

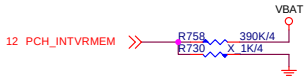


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ????????????????
1 : ???????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

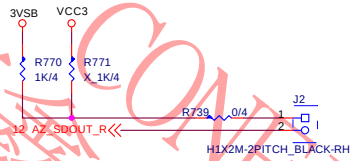


INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

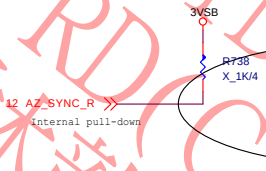
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.



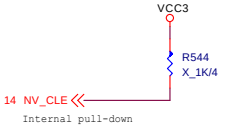
HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

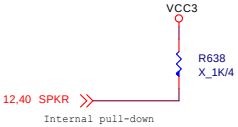


HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

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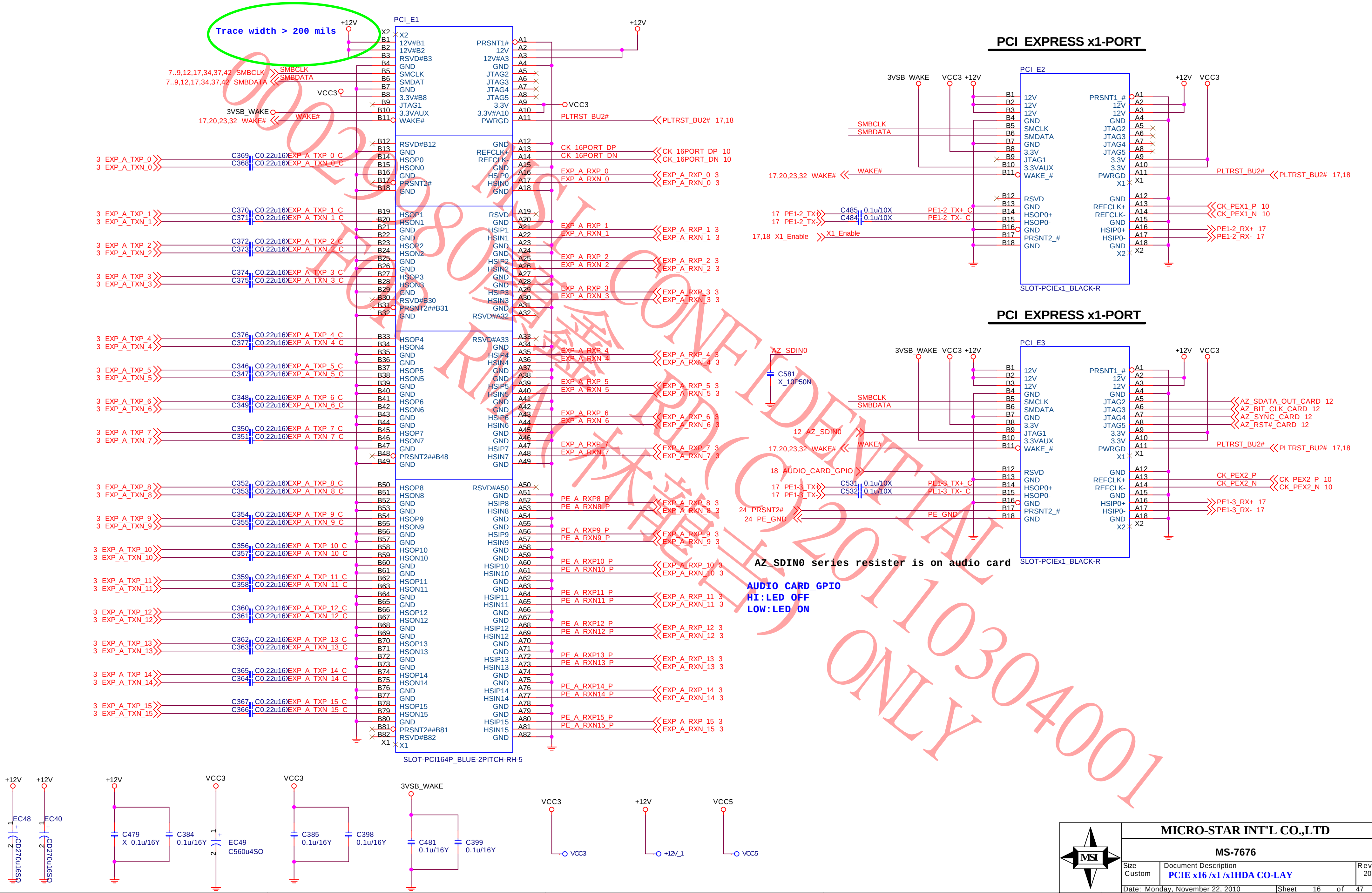
PCI_Express X16 Slot



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Size: Custom	Document Description: PCIE x16 /x1 /x1HDA CO-LAY	Rev: 20
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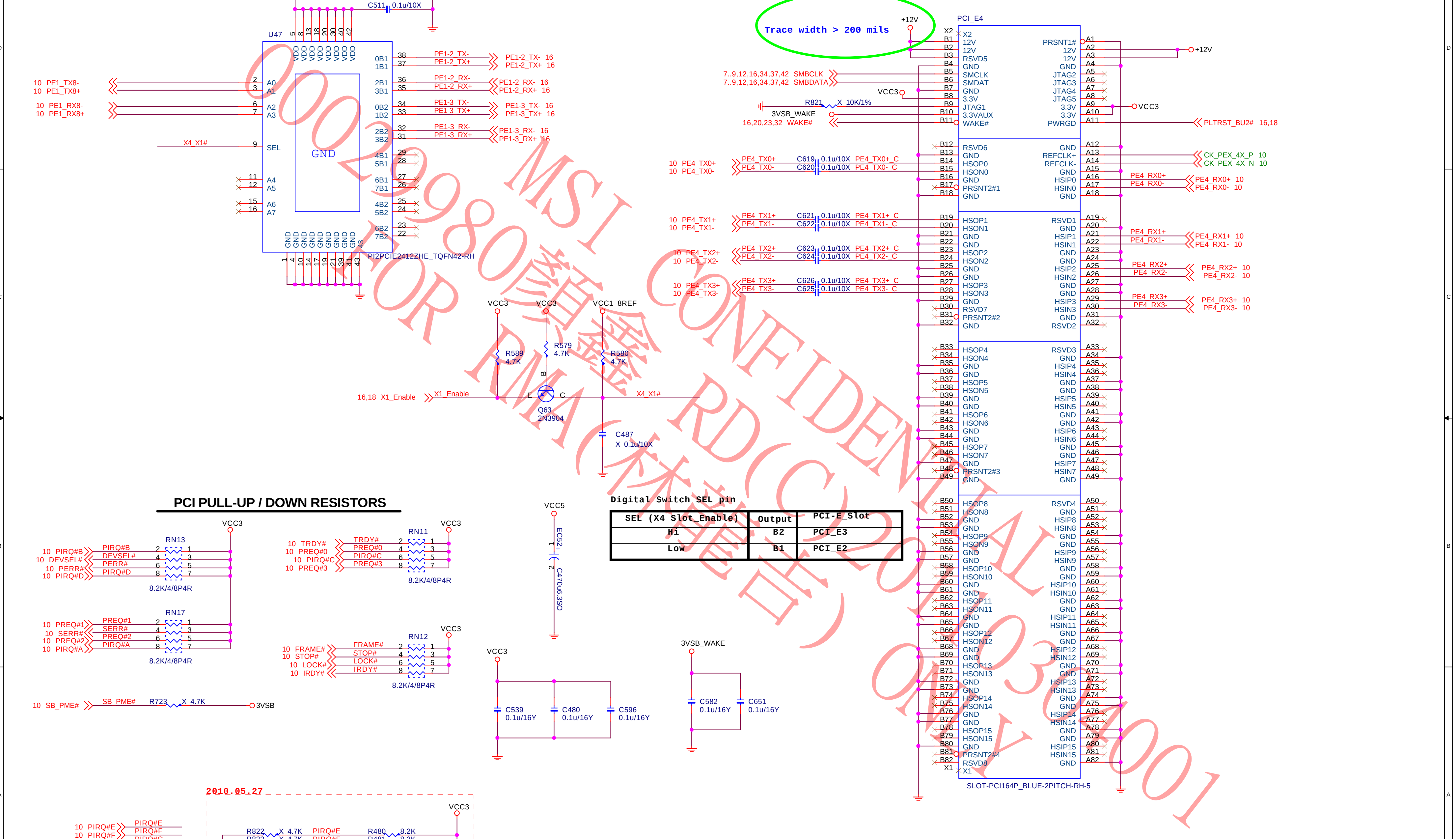
PCI_Express X4 Slot

(Share with PCI_E x1 Slots)



Digital Switch SEL pin

SEL (X4 Slot_Enable)	Output	PCI-E_Slot
Hi	B2	PCI_E3
Low	B1	PCI_E2

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Size: Custom | Document Description: PCIEx4 Slots | Rev: 20

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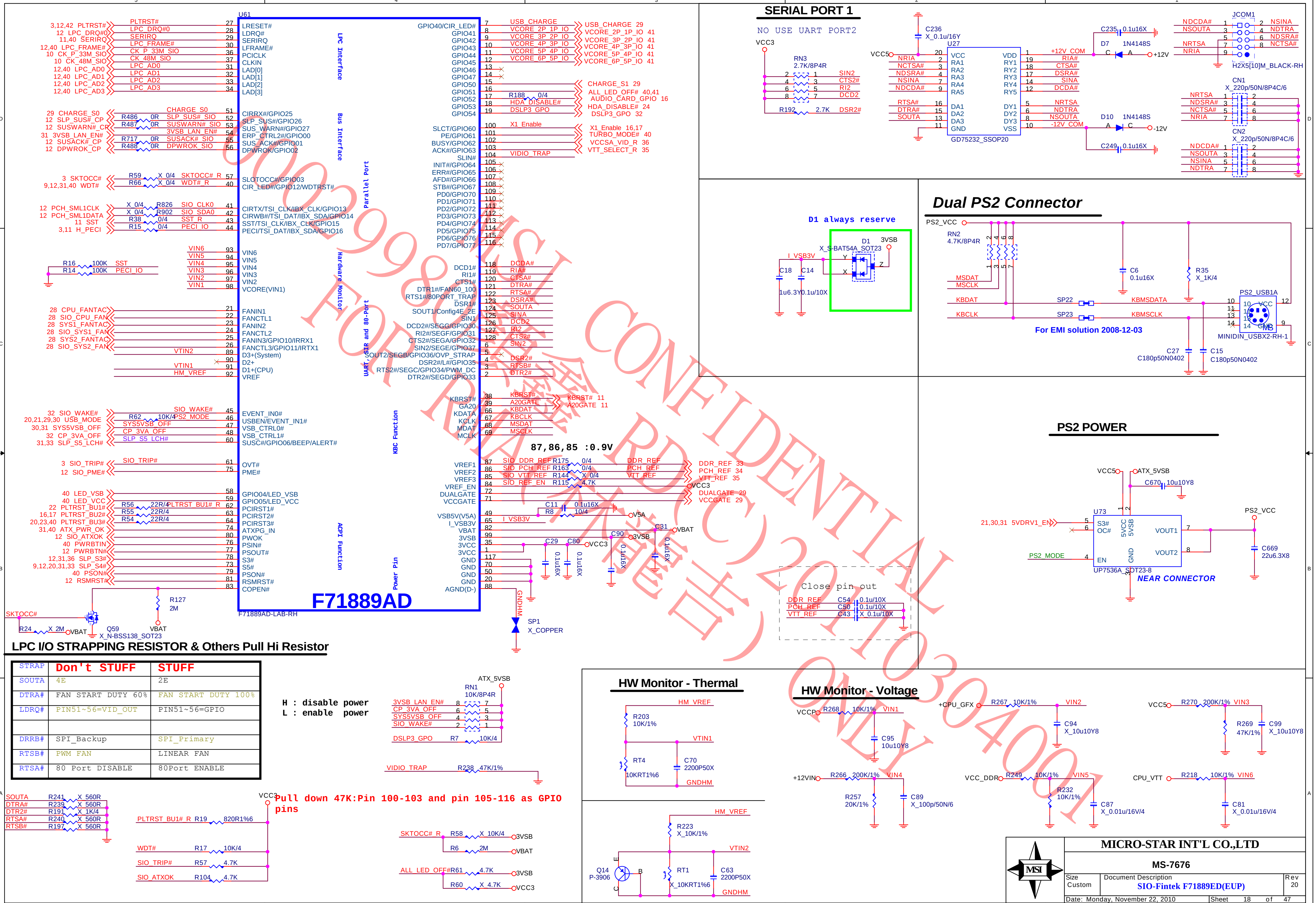

LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
LDRQ#	PIN51~56=VID_OUT	PIN51~56=GPIO
DRRB#	SPI_Backup	SPI_Primary
RTSB#	PWM FAN	LINEAR FAN
RTSA#	80 Port DISABLE	80Port ENABLE

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Size: Custom | Document Description: SIO-Fintek F71889ED(EUP) | Rev 20

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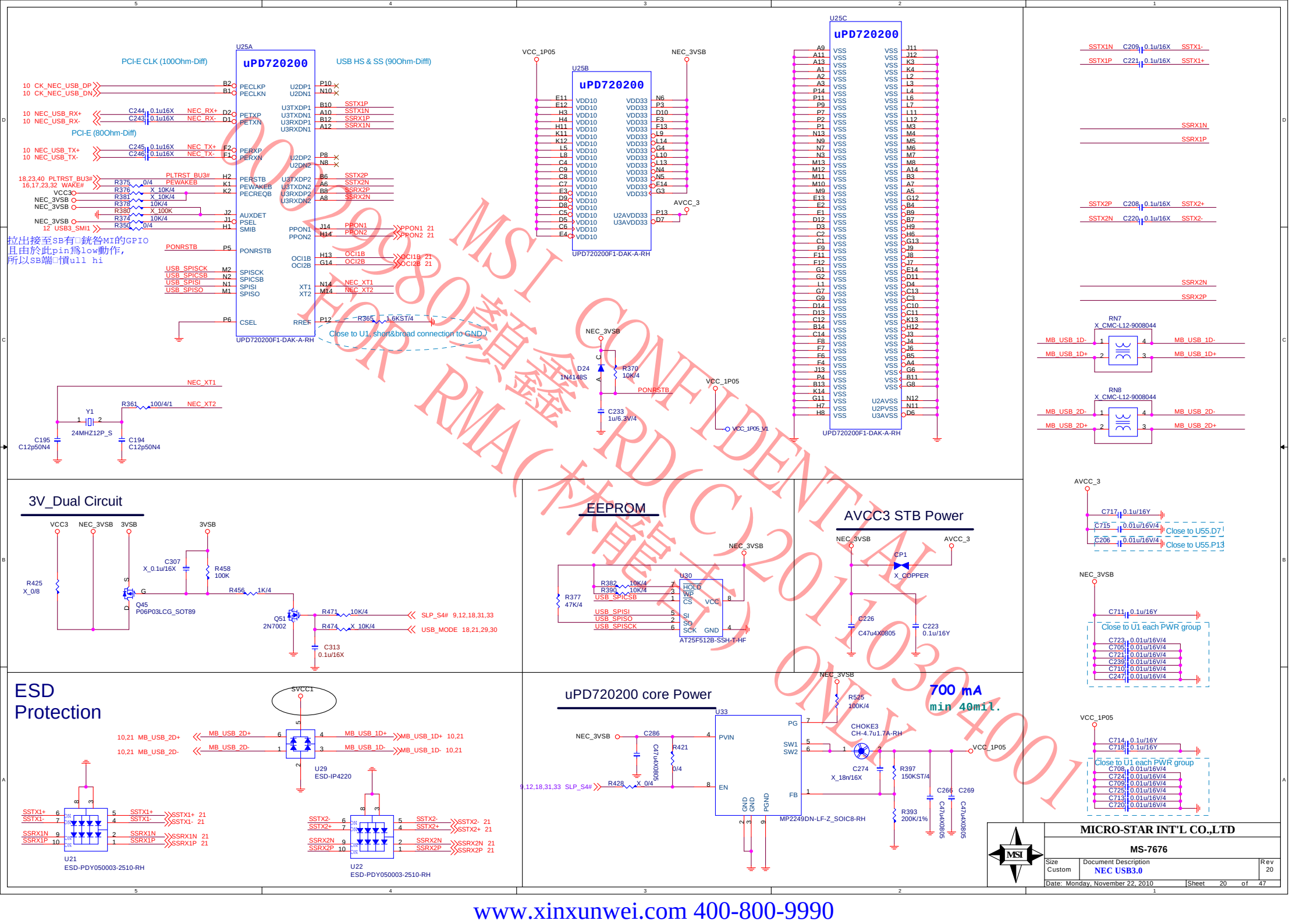
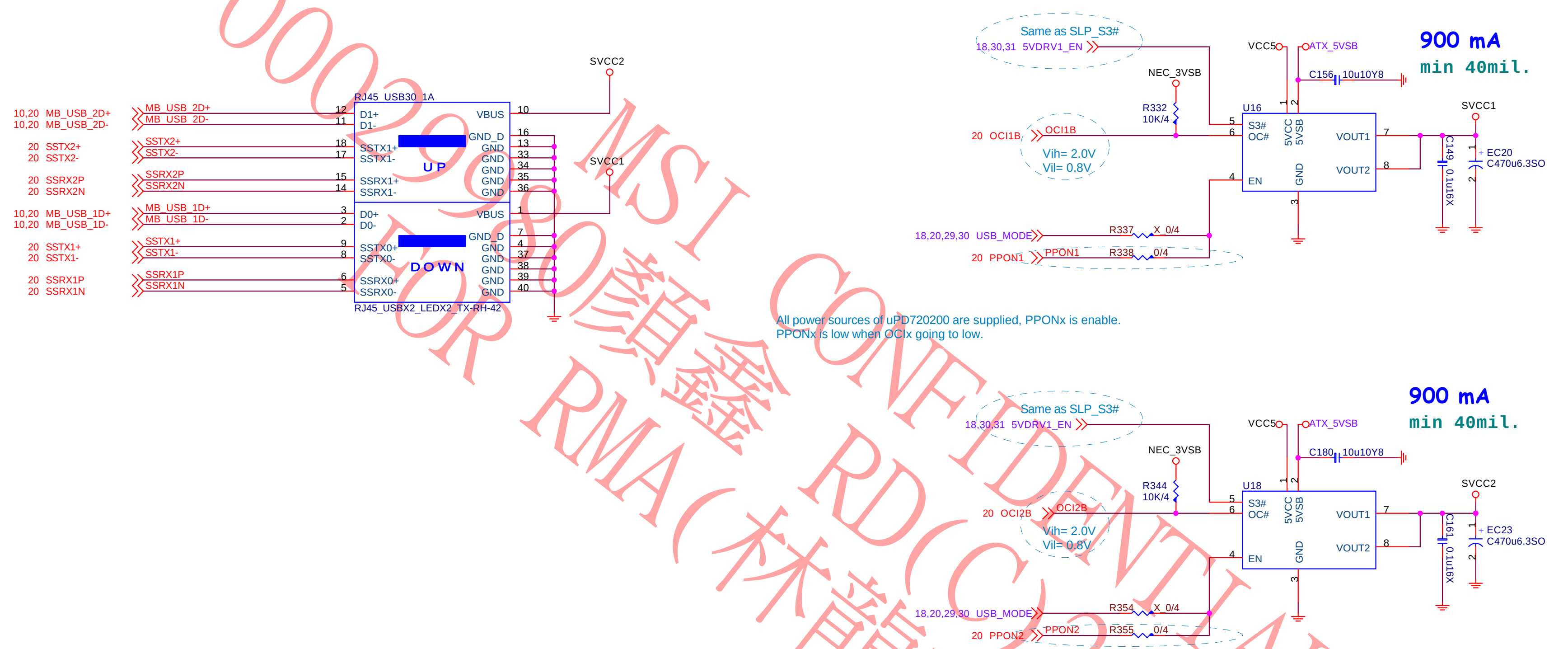
Size	Document Description	Rev
Custom	MARVELL SATA 6G	20

Date: Friday, November 19, 2010 Sheet 19 of 47


PCI-E CLK (100Ohm-Diff)
USB HS & SS (90Ohm-Diff)
PCI-E (80Ohm-Diff)
uPD720200
U25A
U25B
U25C
UPD720200F1-DAK-A-RH
拉出接至SB有銹咎MI的GPIO
且由於此pin爲low動作,
所以SB端憤ull hi
Close to U1, short&broad connection to GND
3V_Dual Circuit
EEPROM
AVCC3 STB Power
ESD
Protection
uPD720200 core Power
700 mA
min 40mil.
MICRO-STAR INT'L CO.,LTD
MS-7676
NEC USB3.0
Date: Monday, November 22, 2010
Sheet 20 of 47
www.xinxunwei.com 400-800-9990



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Size	Document Description	Rev
Custom	NEC USB3.0 POWER & CONNECT	20

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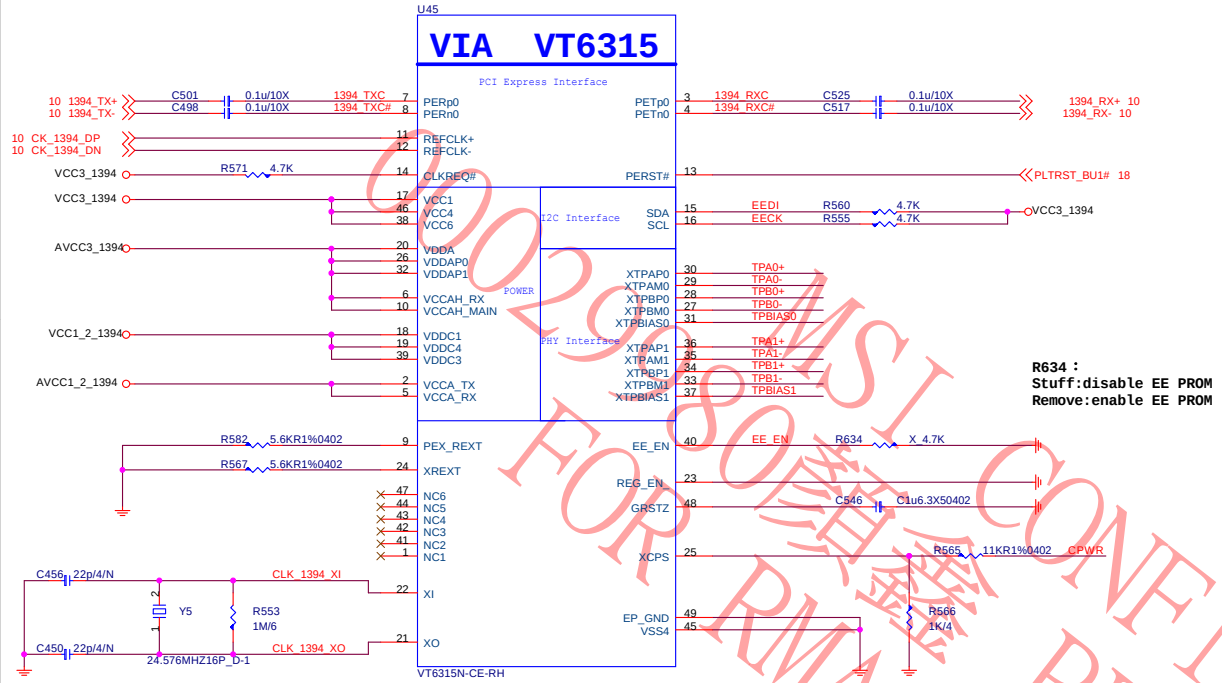
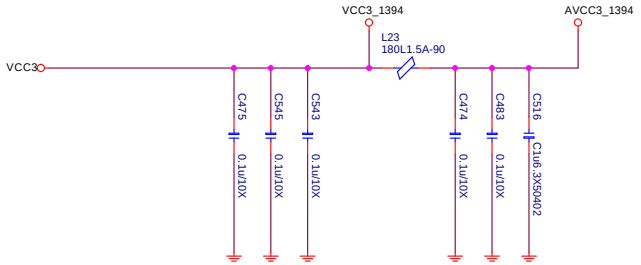
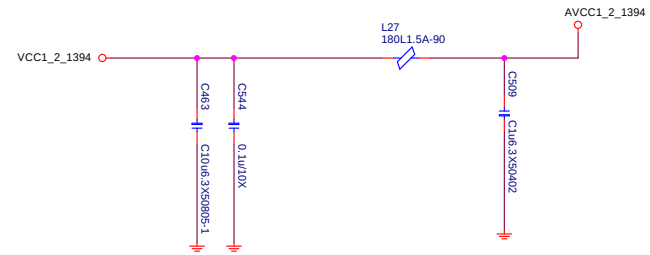
1394 CONTROLLER



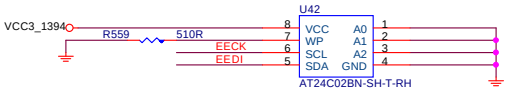
R634 :
Stuff:disable EE PROM
Remove:enable EE PROM



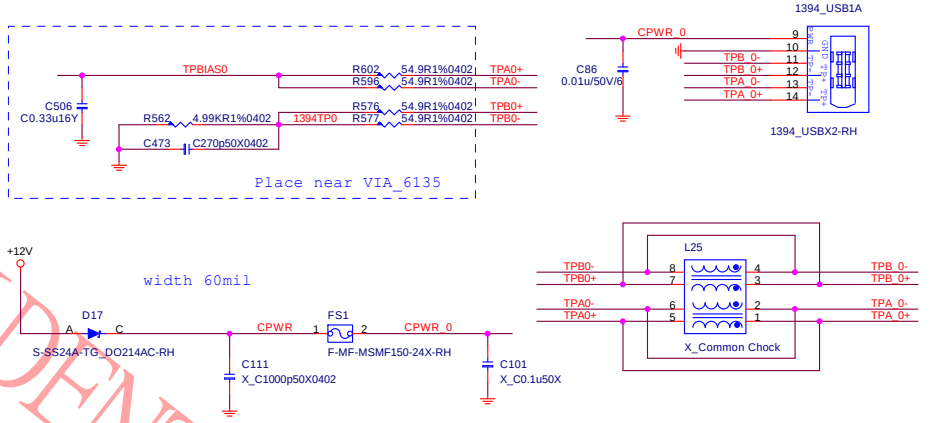
close to chip of all Cap.



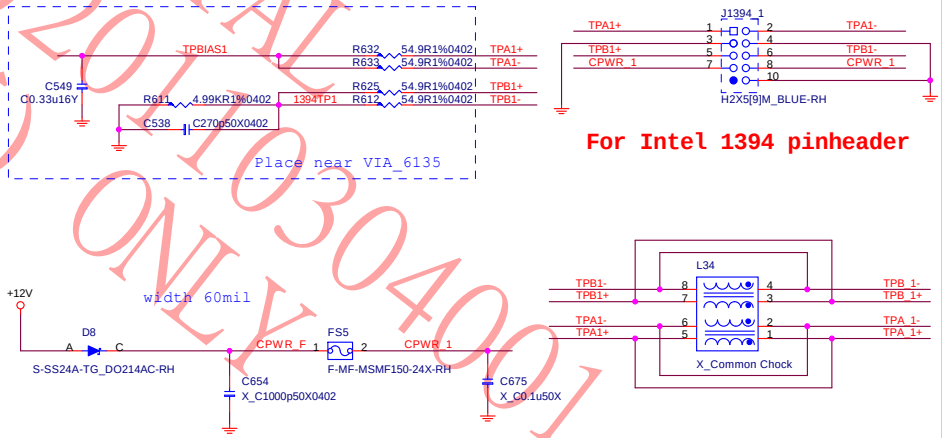
EE PROM



Rear 1394 port



Front 1394 pin header



For Intel 1394 pinheader

MICRO-STAR INT'L CO.,LTD	
MS-7676	
Size: Custom	Document Description: 1394 Controller - VT6315N-CE
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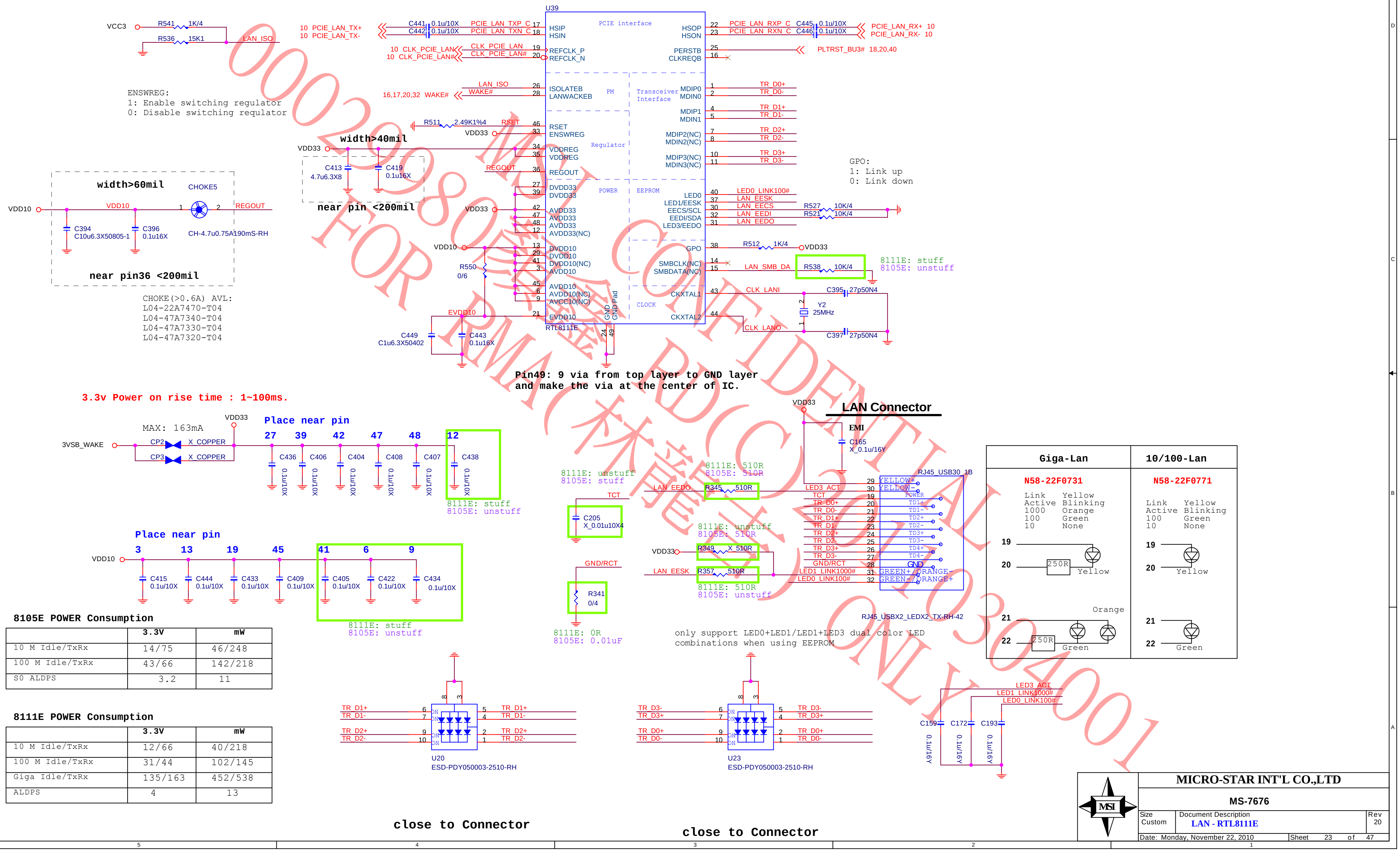
RTL8111E Giga LAN

RTL8105E 10/100M LAN



Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow Active Blinking 1000 Orange 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

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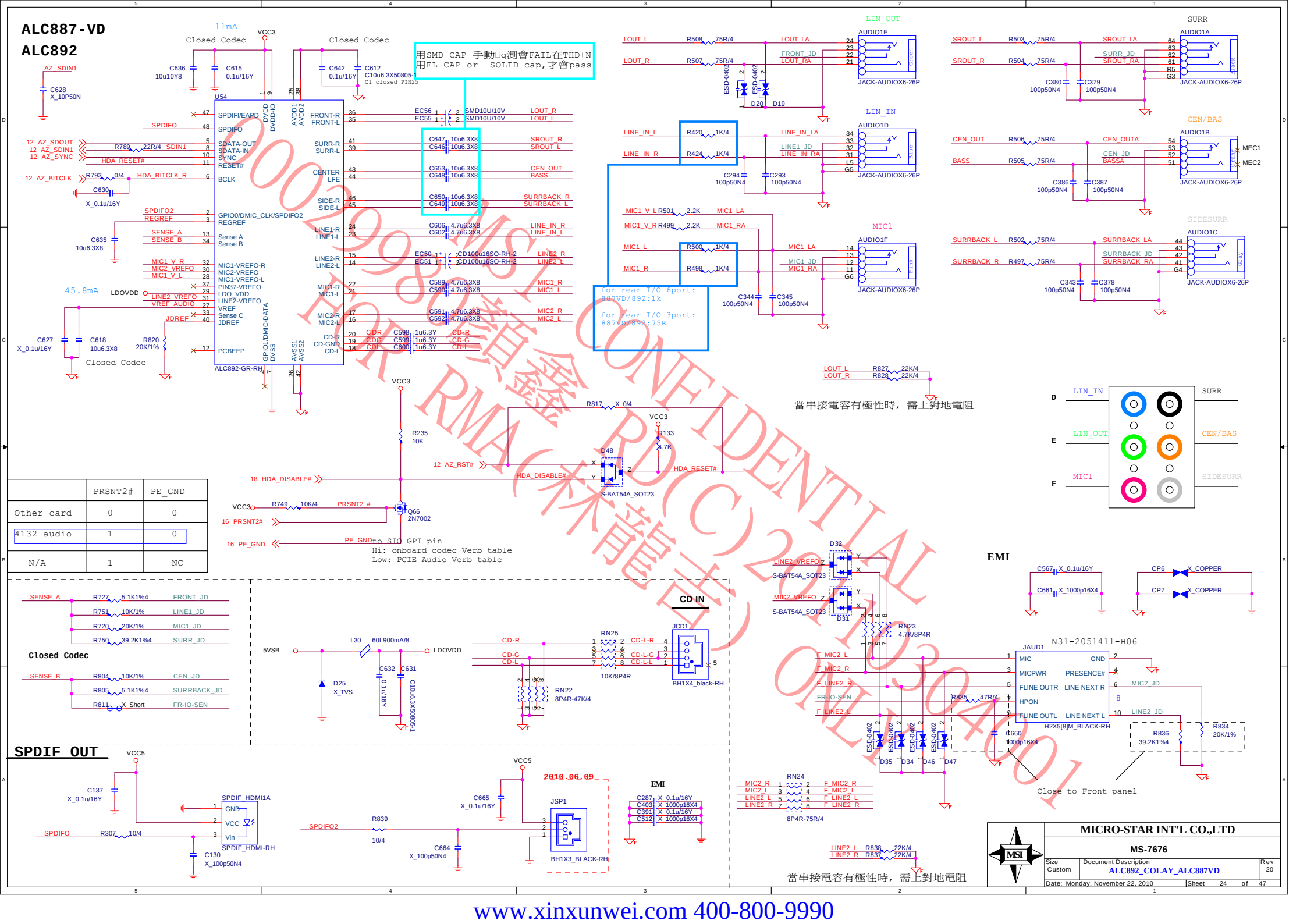
ALC887-VD
ALC892



	PRSNT2#	PE_GND
Other card	0	0
4132 audio	1	0
N/A	1	NC

PE_GND to SIO GPI pin
Hi: onboard codec Verb table
Low: PCIE Audio Verb table

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MS-7676	
Size: Custom	Document Description: ALC892_COLAY_ALC887VD
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DVI level shifter

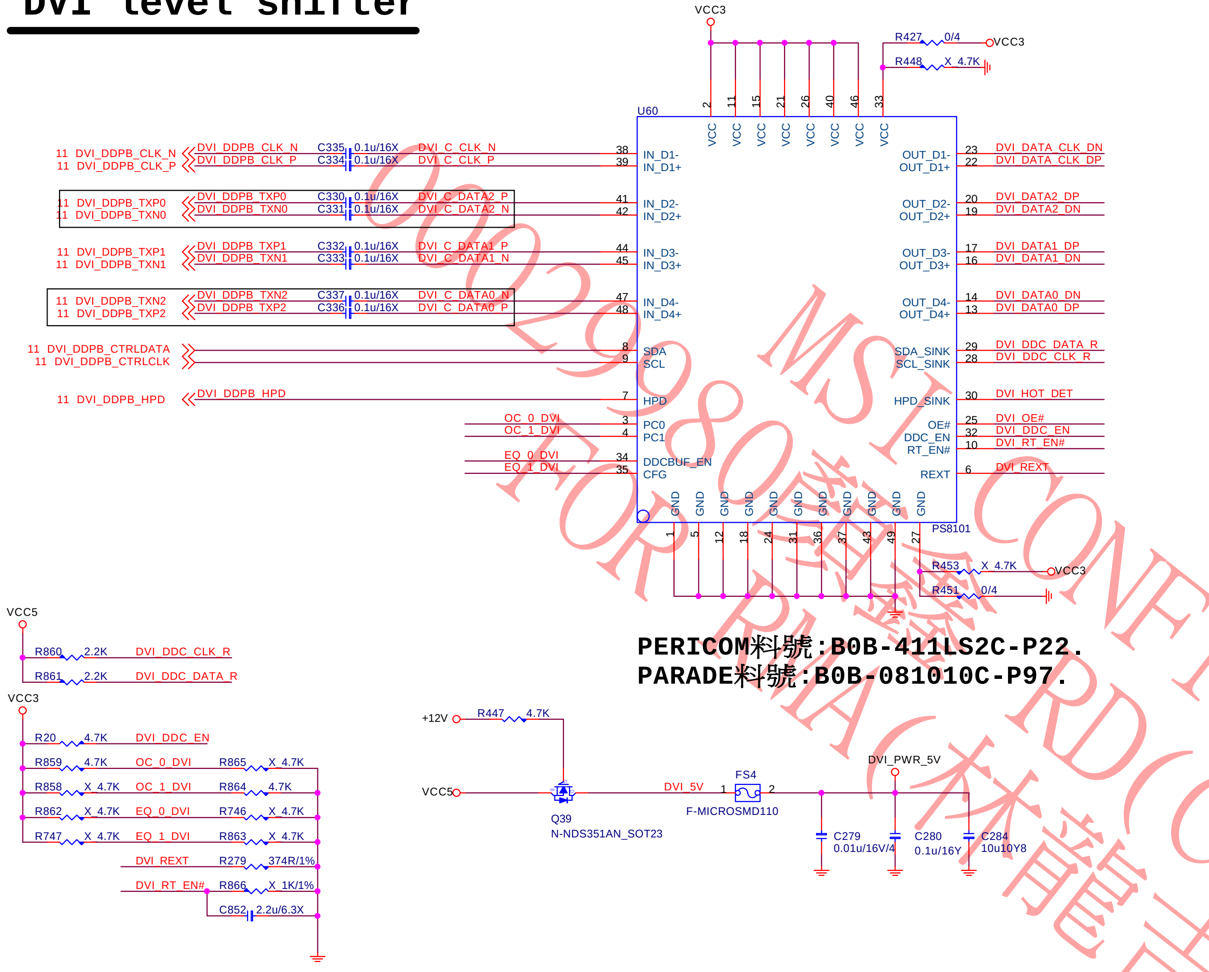
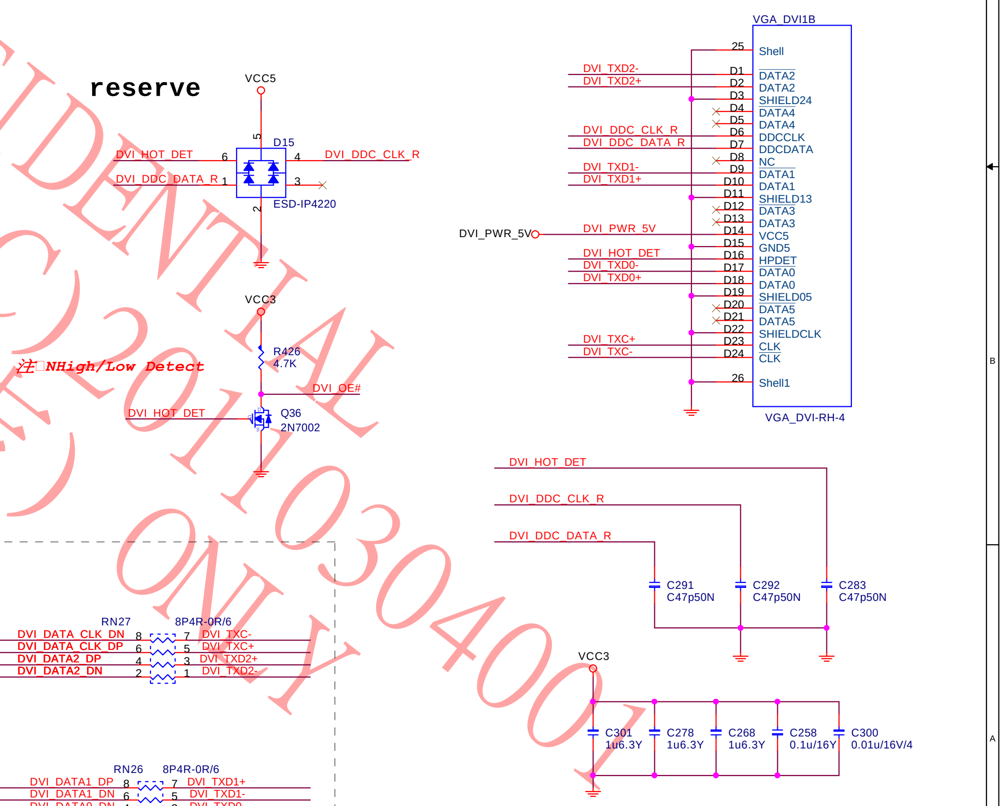
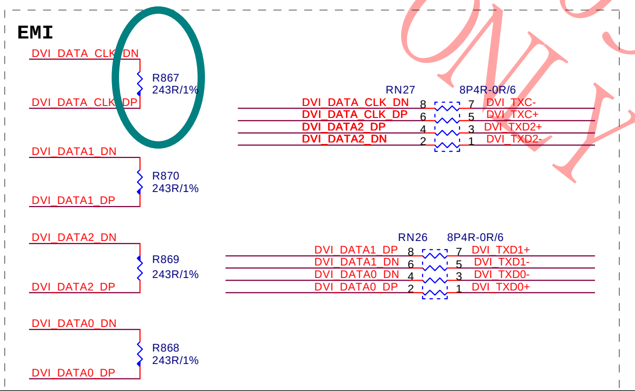


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	





	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

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HDMI level shifter

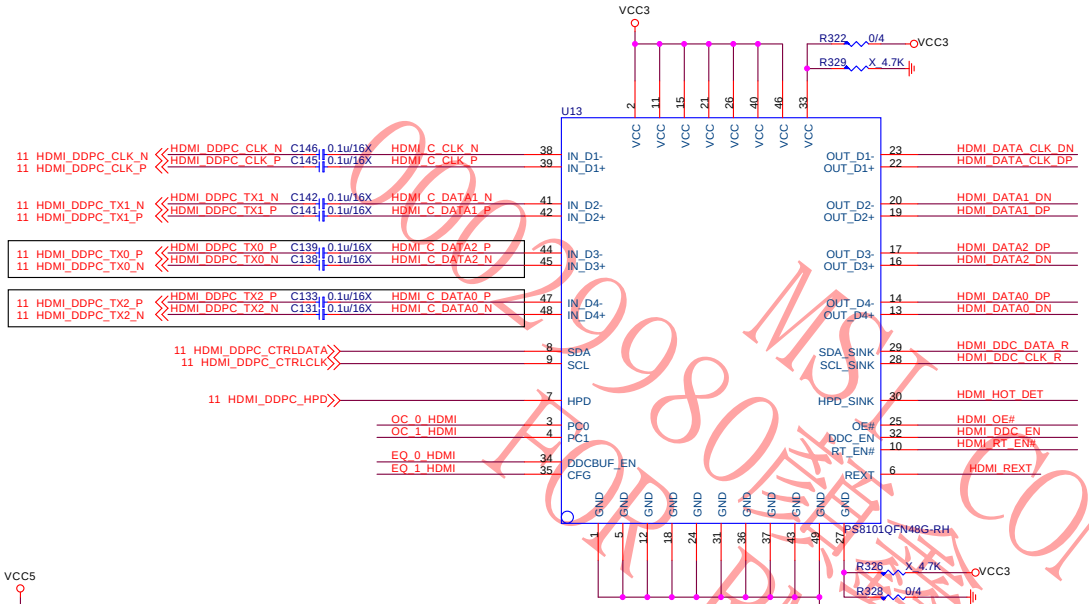
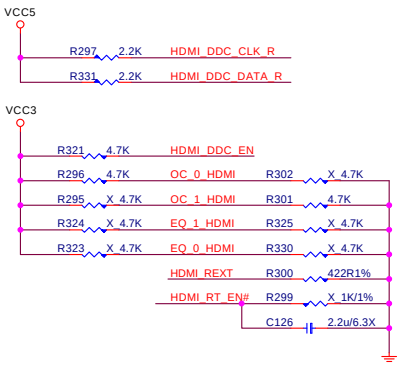
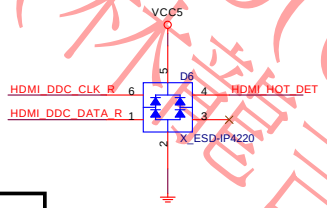


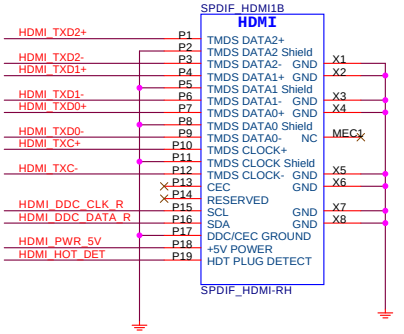
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

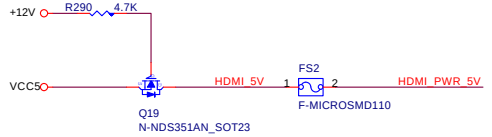
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	

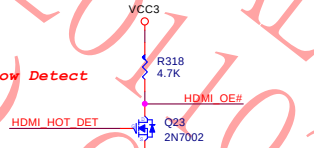


reserve

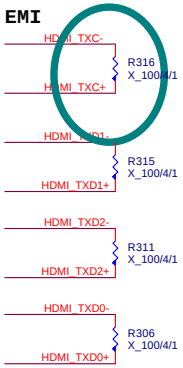


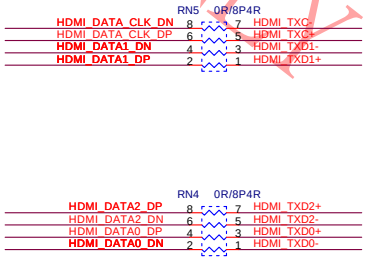


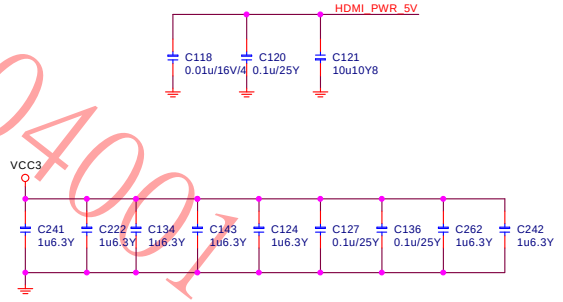




注 NHigh/Low Detect







	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

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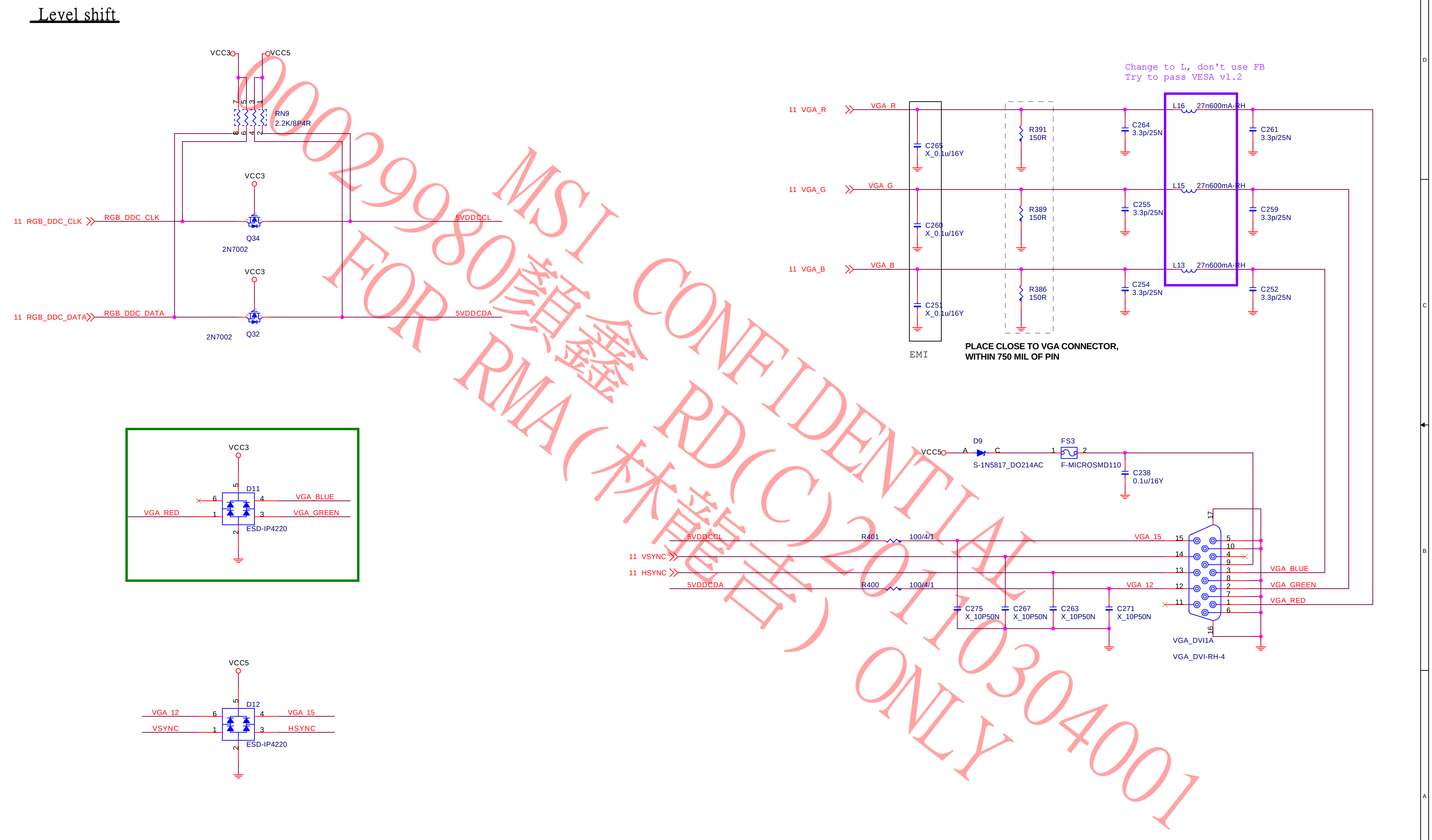
D-Sub



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Custom	VGA	20

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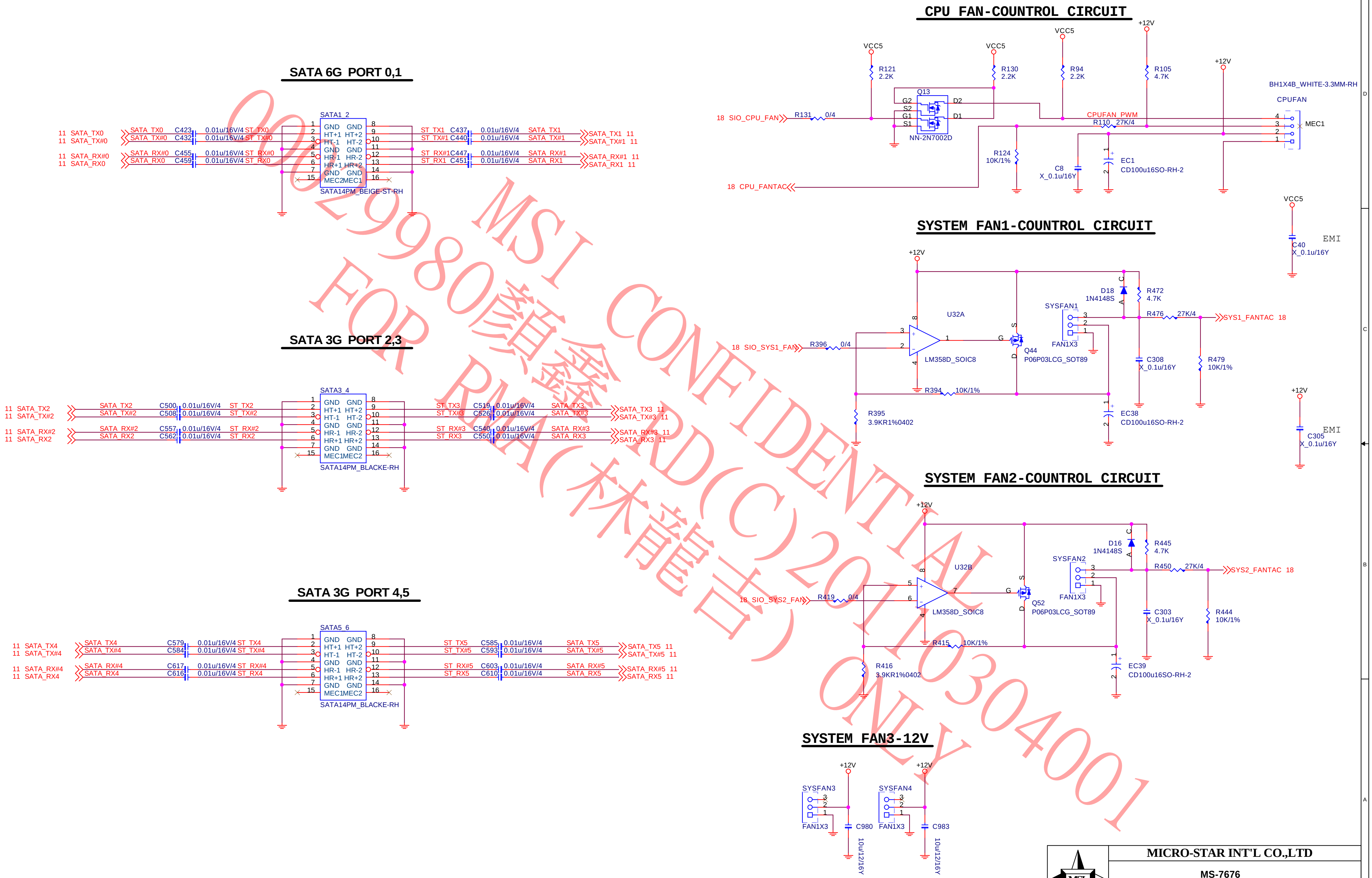

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: SATA / FAN Control	Rev: 20
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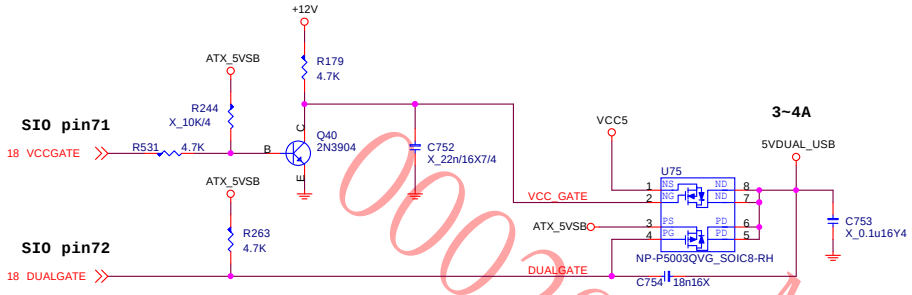
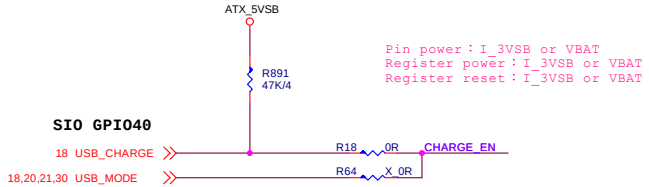
5VDUAL_USB



SIO GPIO40 Pin7 (I_VSB3V)

USB_CHARGE: (OD)
0: Don't support USB charge and resume.
1: Support USB charge and resume.

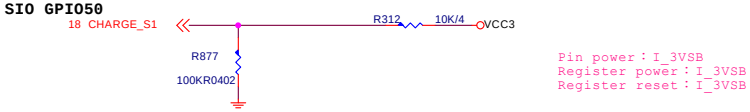
Power plug in , H/W default support USB charge.

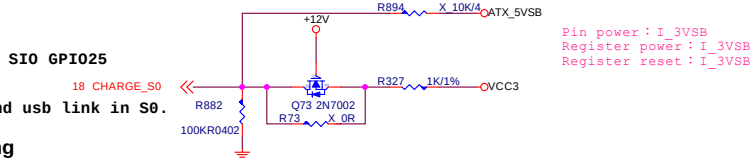


SIO GPIO25 (I_VSB3V)
SIO GPIO50 (I_VSB3V)

CHARGE_S1: (PUSH PULL)
CHARGE_S0: (OPEN DRAIN ONLY)

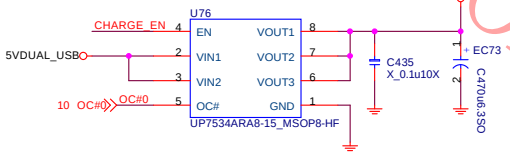
	S0	S1
AUTO:	0	0
DCP :	0	1
A :	1	0
Y :	1	1





USB POWER FOR PORT 0 for USBCharging

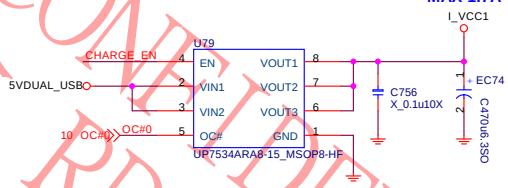
MAX 1.7A

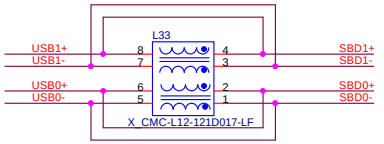


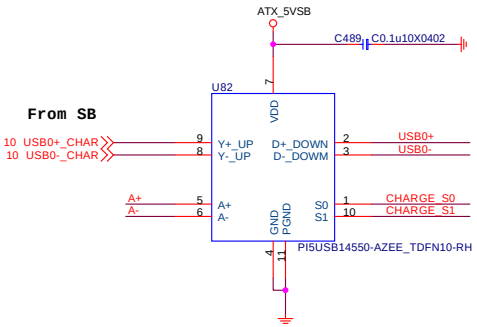
H/W default support auto charging in S3/S4/S5 and usb link in S0.

USB POWER FOR PORT 1 for USBCharging

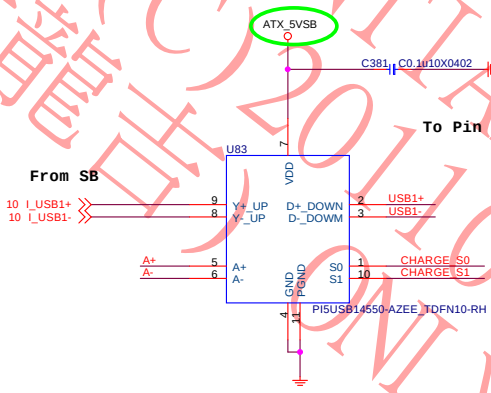
MAX 1.7A



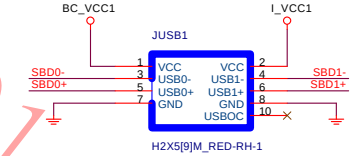


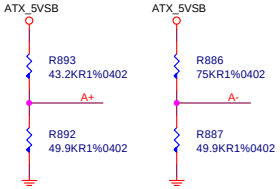


S1	0		0	1
S0	0		1	1
Mode	AUTO		A	Y



PI5USB14550 has internal EDS diode.





A type
2.70V< D+ <3.1 V，
1.85V< D- < 2.1V。
For i-Pad / i-Phone 4G charges current up to 1.6A.

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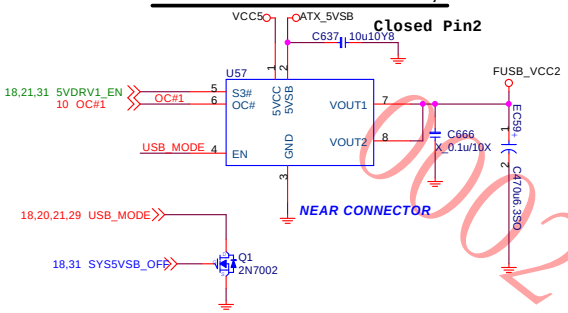
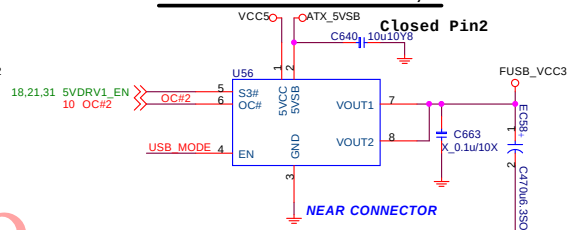
Front USB Connector

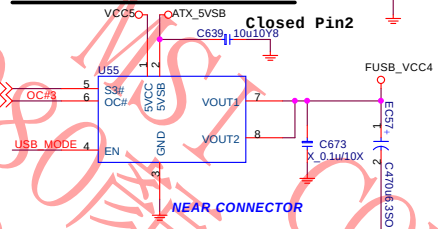
USB POWER REAL PORT 2,3



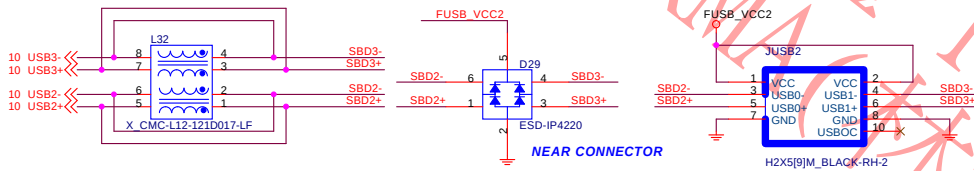
USB POWER FOR PORT 4,5



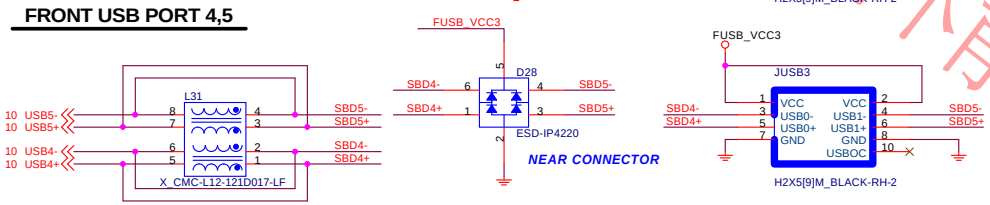
USB POWER FOR PORT 6,7



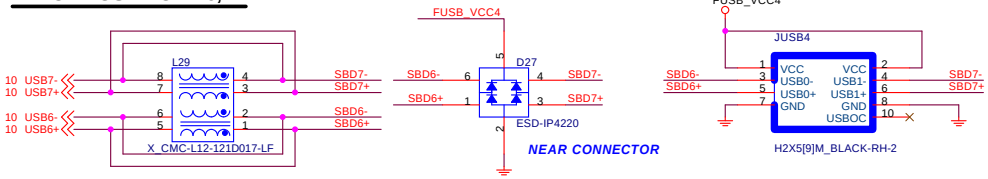
FRONT USB PORT 2,3



FRONT USB PORT 4,5

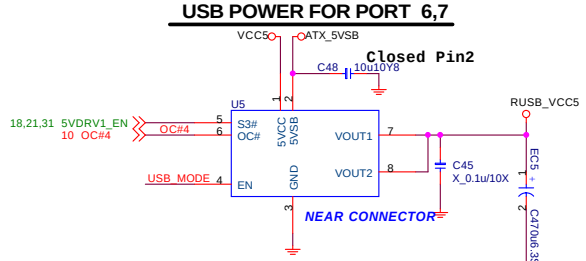


FRONT USB PORT 6,7

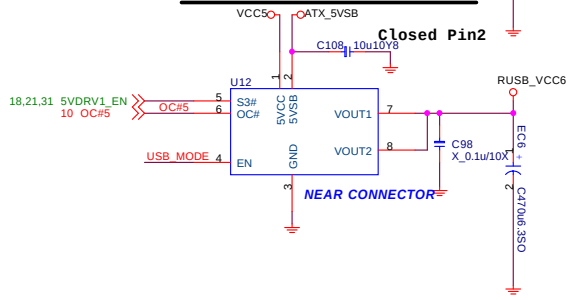


Rear USB Connector

USB POWER FOR PORT 6,7

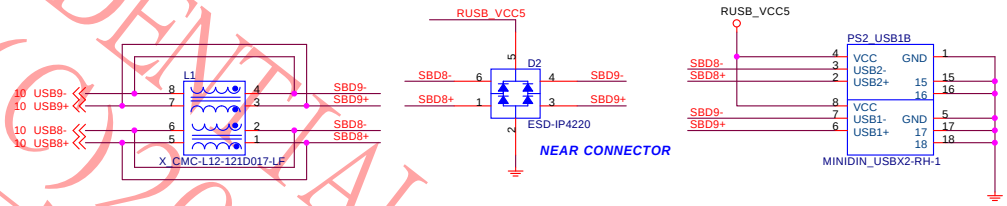


USB POWER FOR PORT 8,9

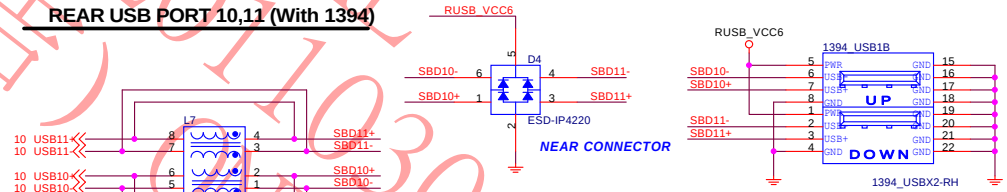


USB_MODE for USB voltage
H:Follow 5VSB
L:Always off

REAR USB PORT 8,9 (With PS2)



REAR USB PORT 10,11 (With 1394)



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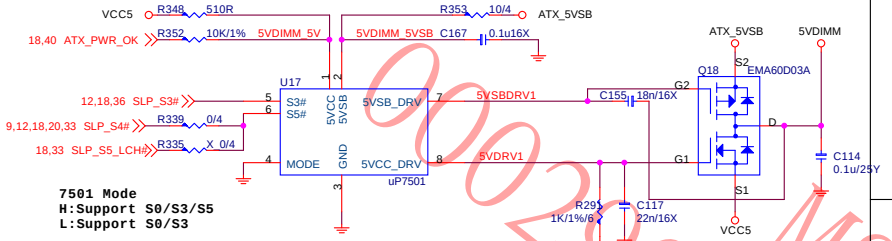
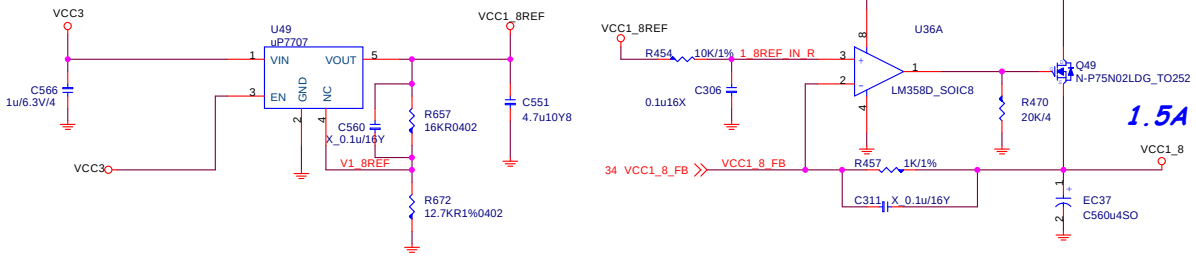
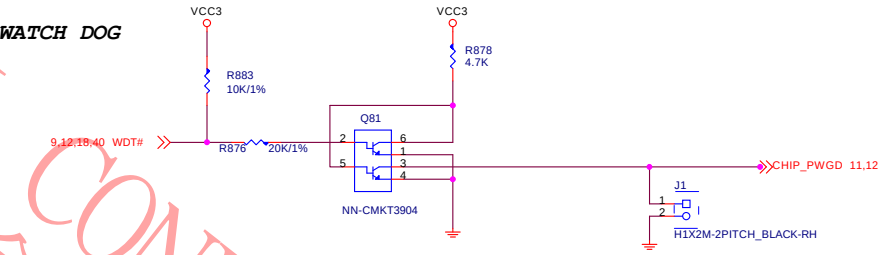
5VDIMM FOR DDR

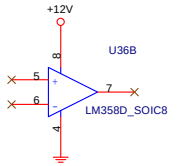


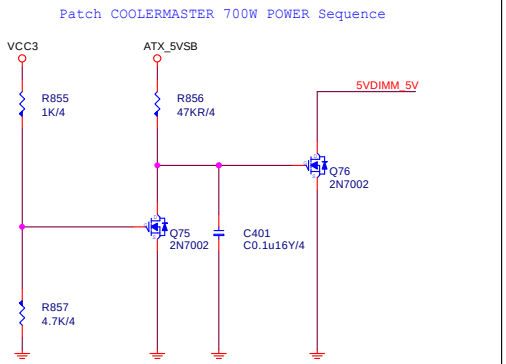
VCC1_8REF



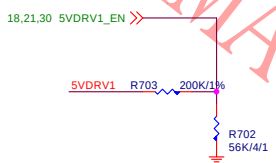
WATCH DOG



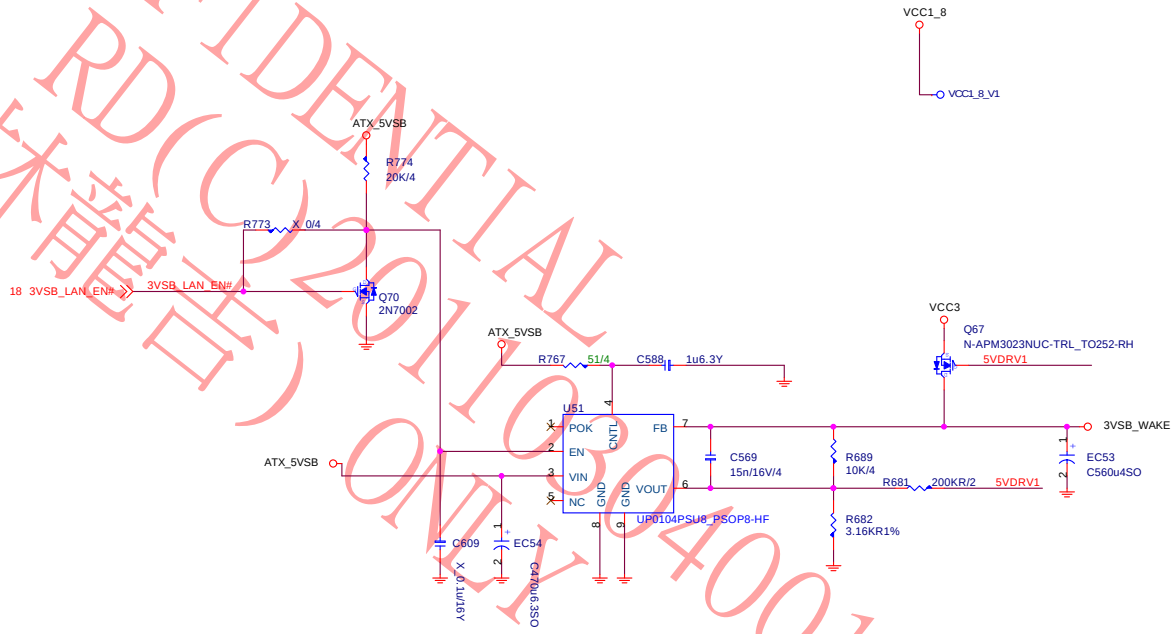




USB MODE

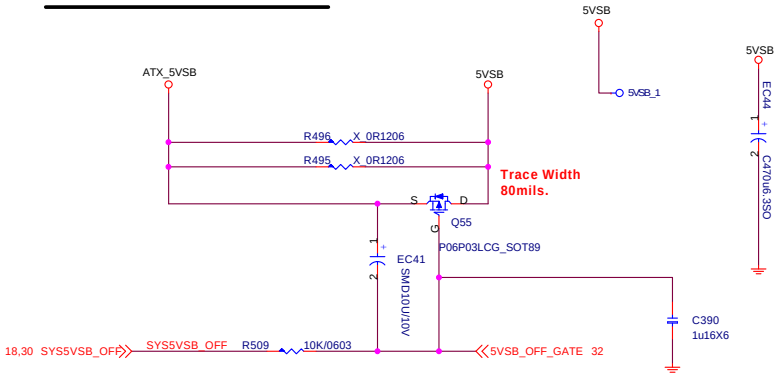


3VSB_WAKE



3VSB supply to PCH and other device. Turn off when Deep S3/S5.
+3VSB_WAKE supply to PCI Slot and LAN power.Turn off when Deep S3/S5 w/o WOL.

5VSB Power Switch



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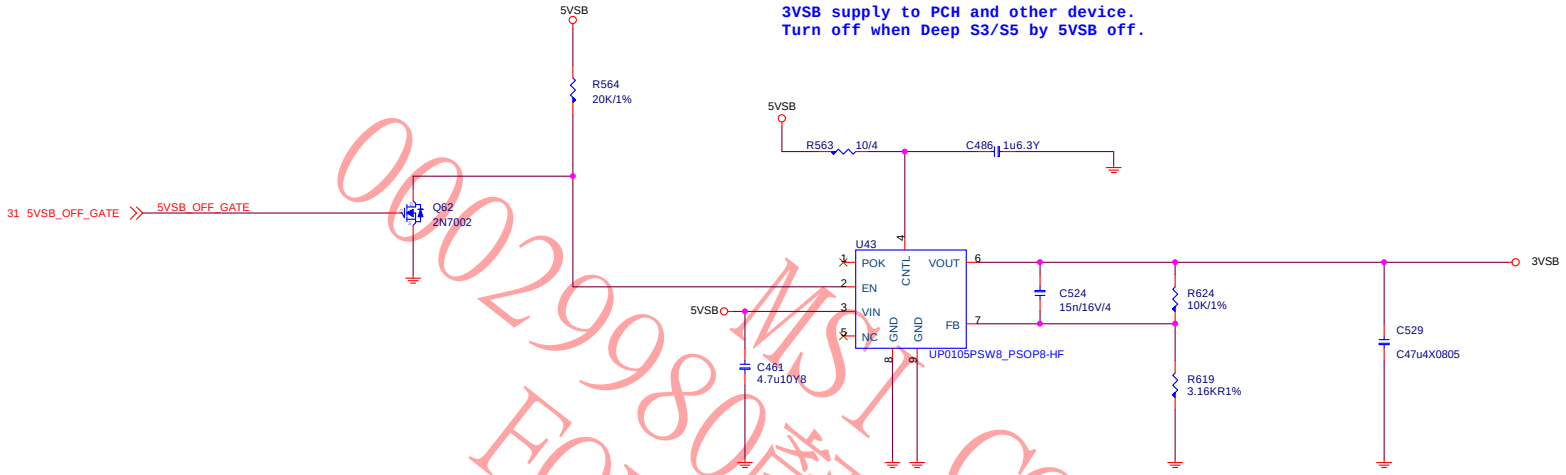
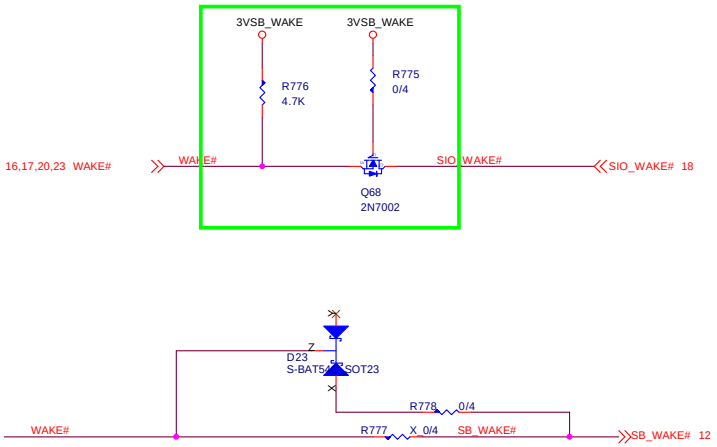
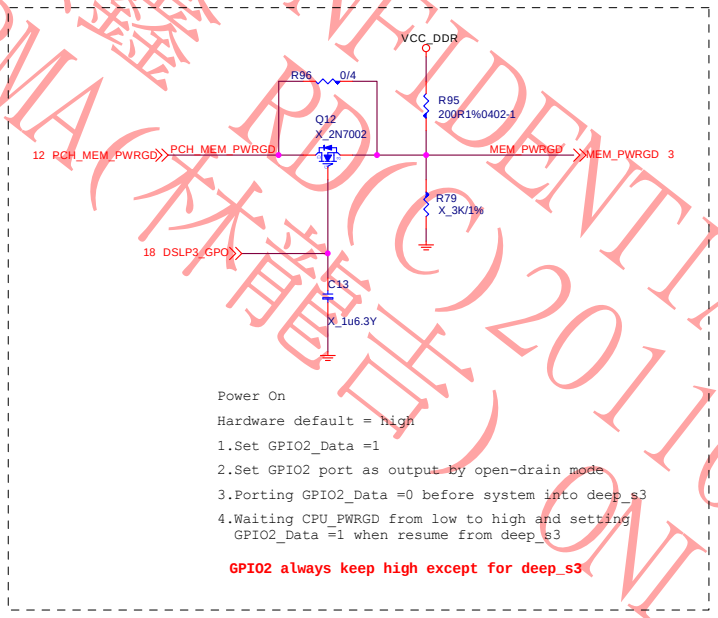
Deep Mode WOL LAN Power CTRL Circuit

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.

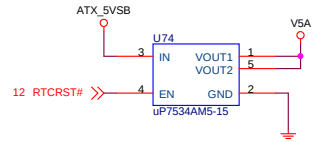


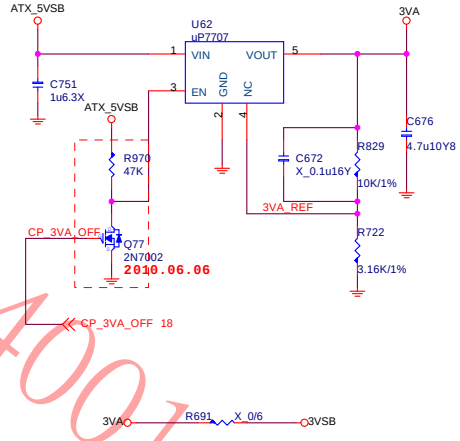
LAN/PCIE/PCI Wake Up CTRL Circuit





RTCRST patch circuit for
clr-CMOS PCH will wake up issue





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DDR Power:1.5V

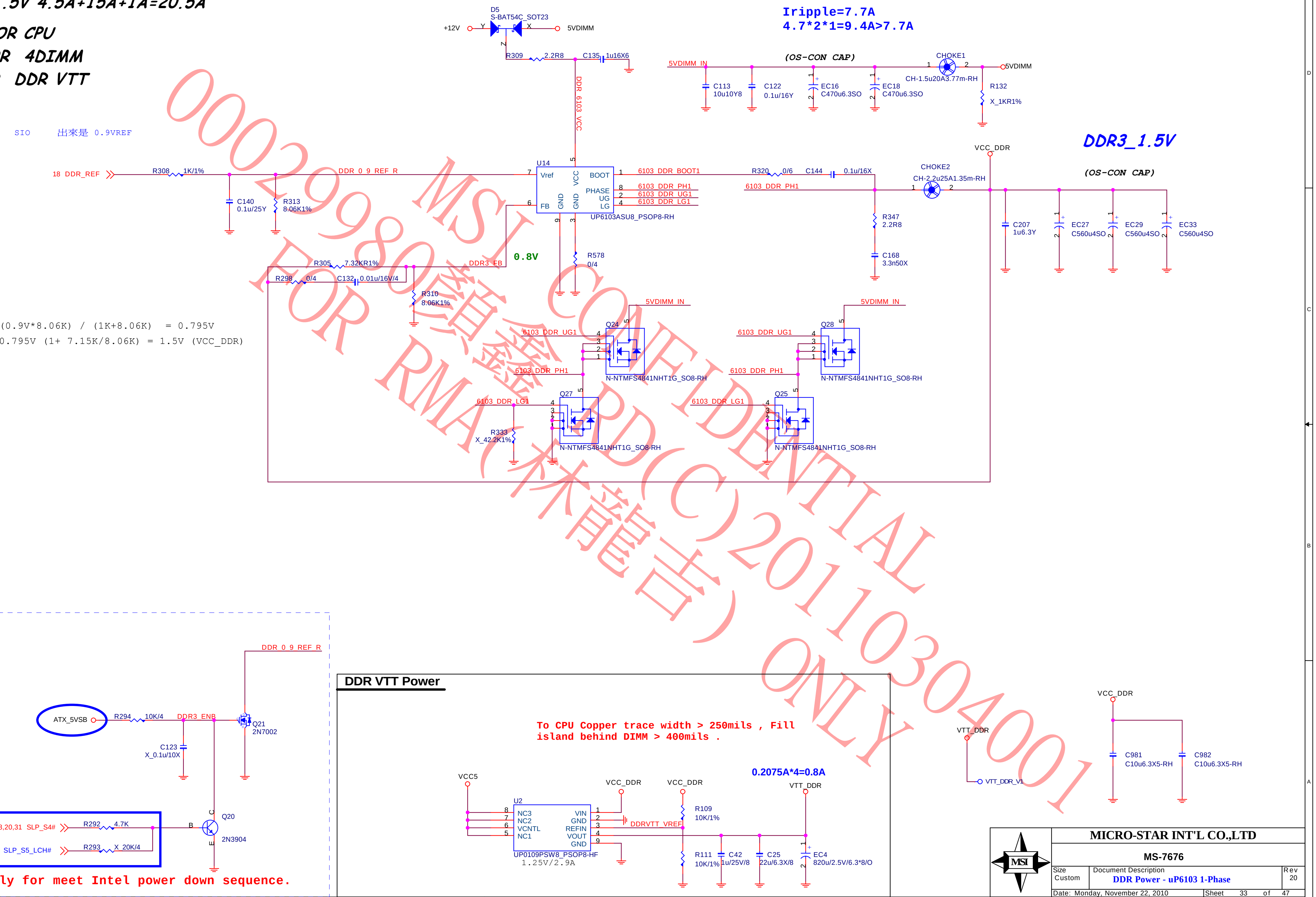
DDR3_1.5V 4.5A+15A+1A=20.5A

4.5A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

SIO 出來是 0.9VREF

Iripple=7.7A
4.7*2*1=9.4A>7.7A

(0.9V*8.06K) / (1K+8.06K) = 0.795V
0.795V (1+ 7.15K/8.06K) = 1.5V (VCC_DDR)



P.S. Only for meet Intel power down sequence.

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PCH Power:1.05V

PCH Core 6.2A+1.8A=8A

6.2A FOR PCH

1.8A FOR ME CORE

Iripple=1.80A
5.08*1=5.08A>1.80A

8A

SIO 出來是 0.9VREF

FOR SIO REF

0.9V

UPI VOLTAGE CONSOLE

uP6262

Slave Address=20
RH=10K,RL=NC

CRB

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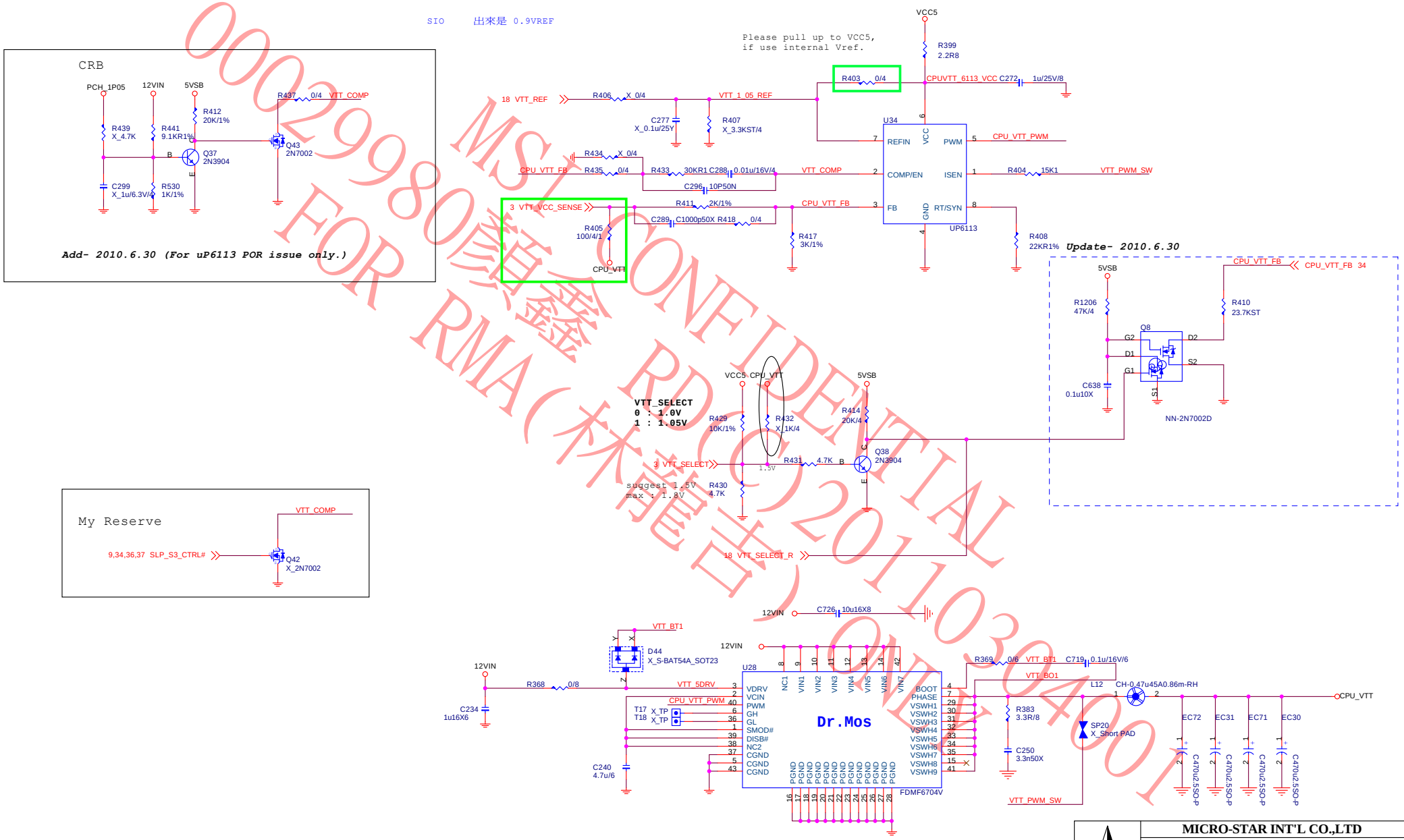
CPU_VTT:1.05/1.00

CPU VTT 8.5A

8.5A FOR CPU



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Size: Custom	Document Description: CPU_VTT - uP6113- 1-Phase
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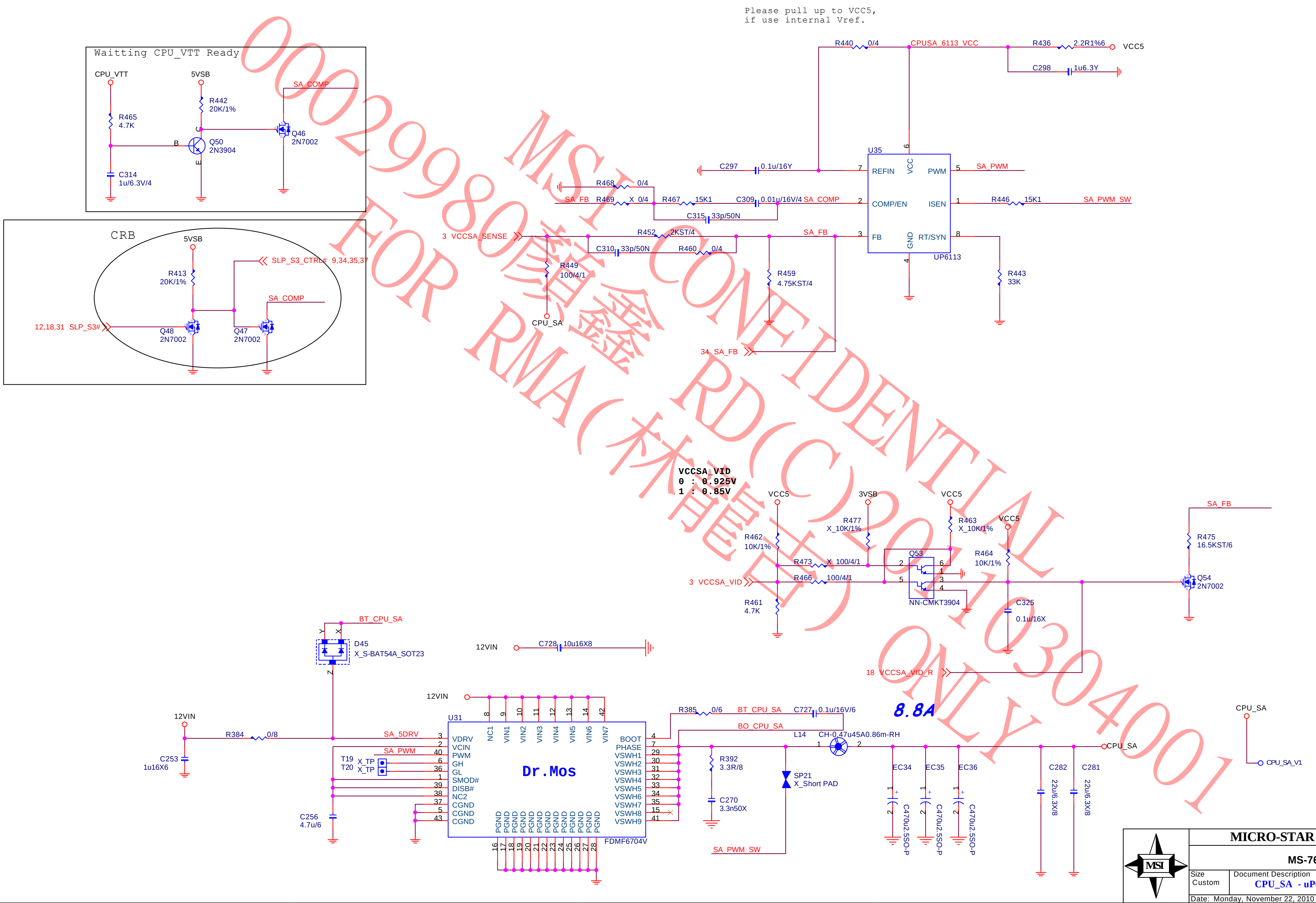
CPU_SA:0.925/0.85

SA Core =8.8A



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Size	Document Description	Rev
Custom	CPU_SA - uP6113 1-Phase	20

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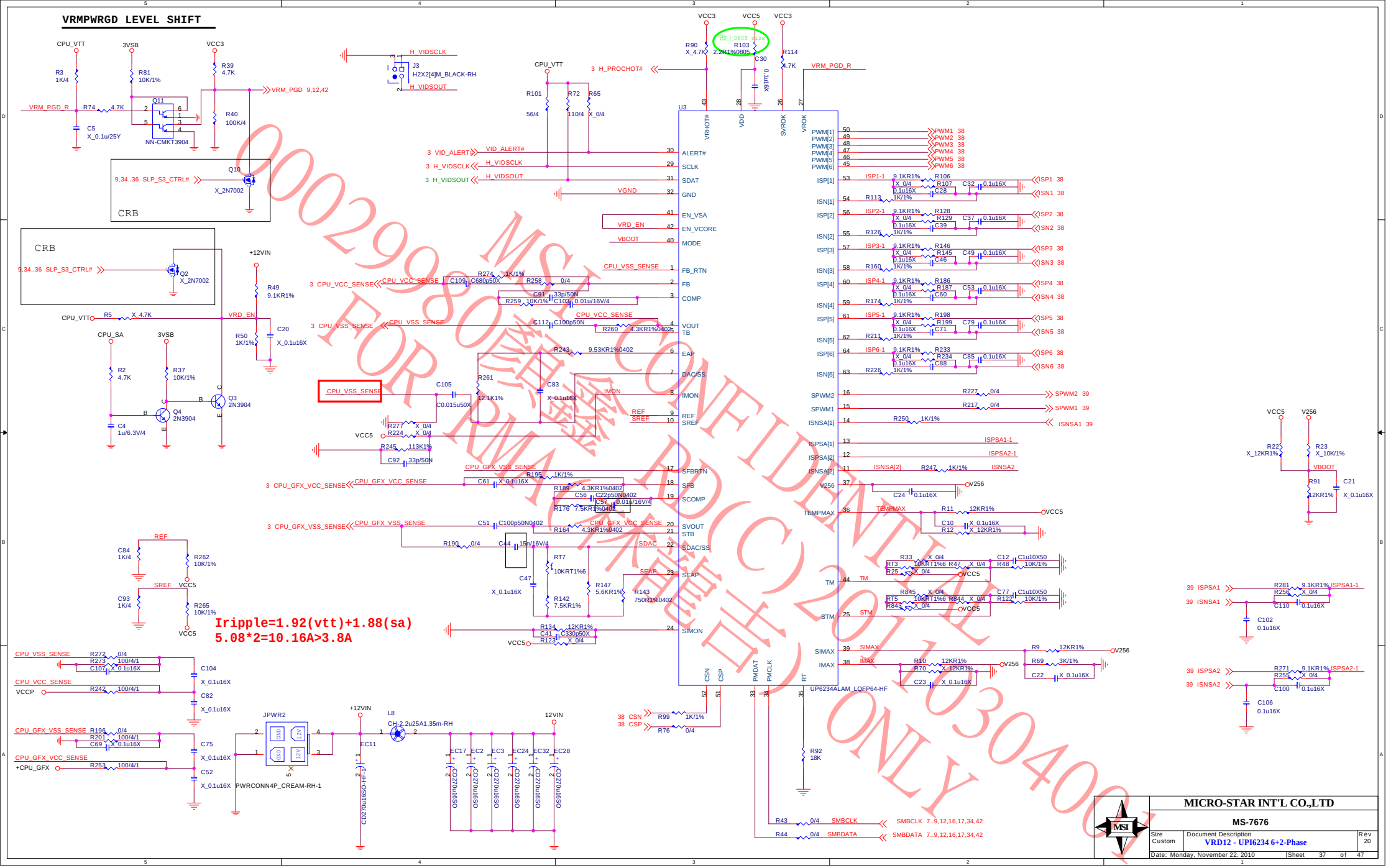

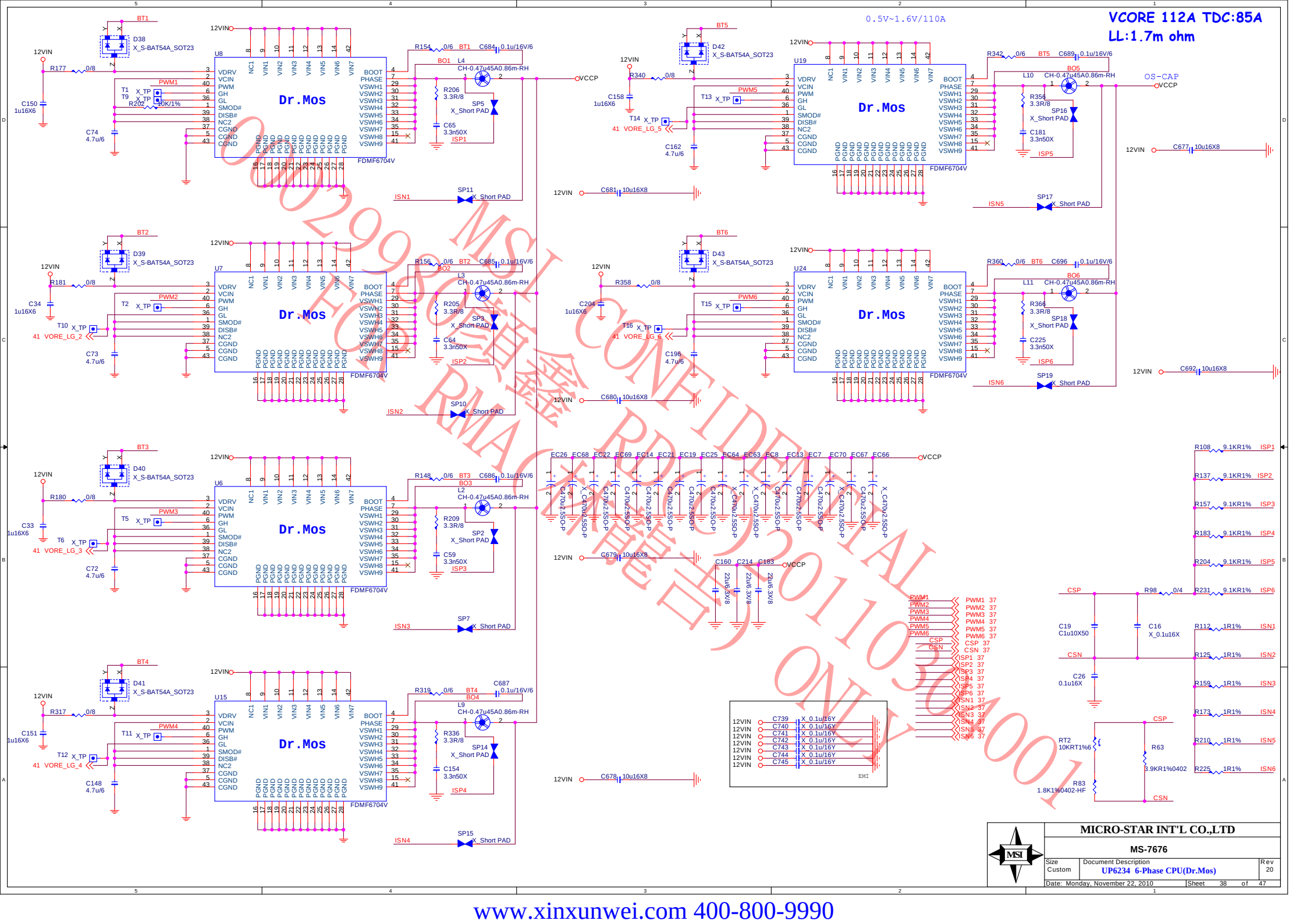
VCORE 112A TDC:85A
LL:1.7m ohm
0.5V~1.6V/110A
Dr.Mos
FDMF6704V
U8
U19
U7
U24
U6
U15
VCCP
OS-CAP
EMI
MICRO-STAR INT'L CO.,LTD
MS-7676
UP6234 6-Phase CPU(Dr.Mos)
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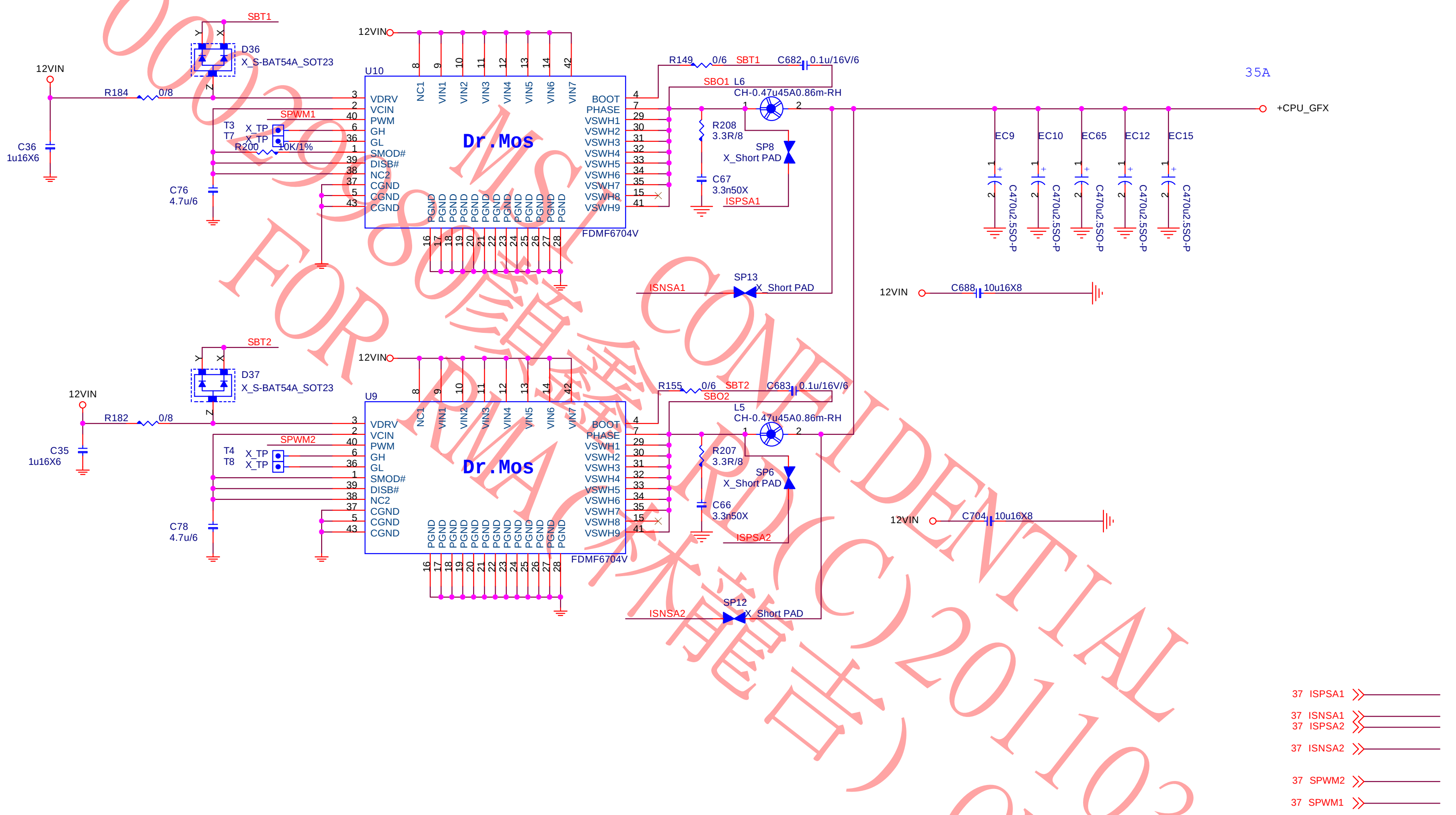
www.xinxunwei.com 400-800-9990



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Size	Document Description	Rev
Custom	UP6234 2-Phase GPU(Dr.Mos)	20

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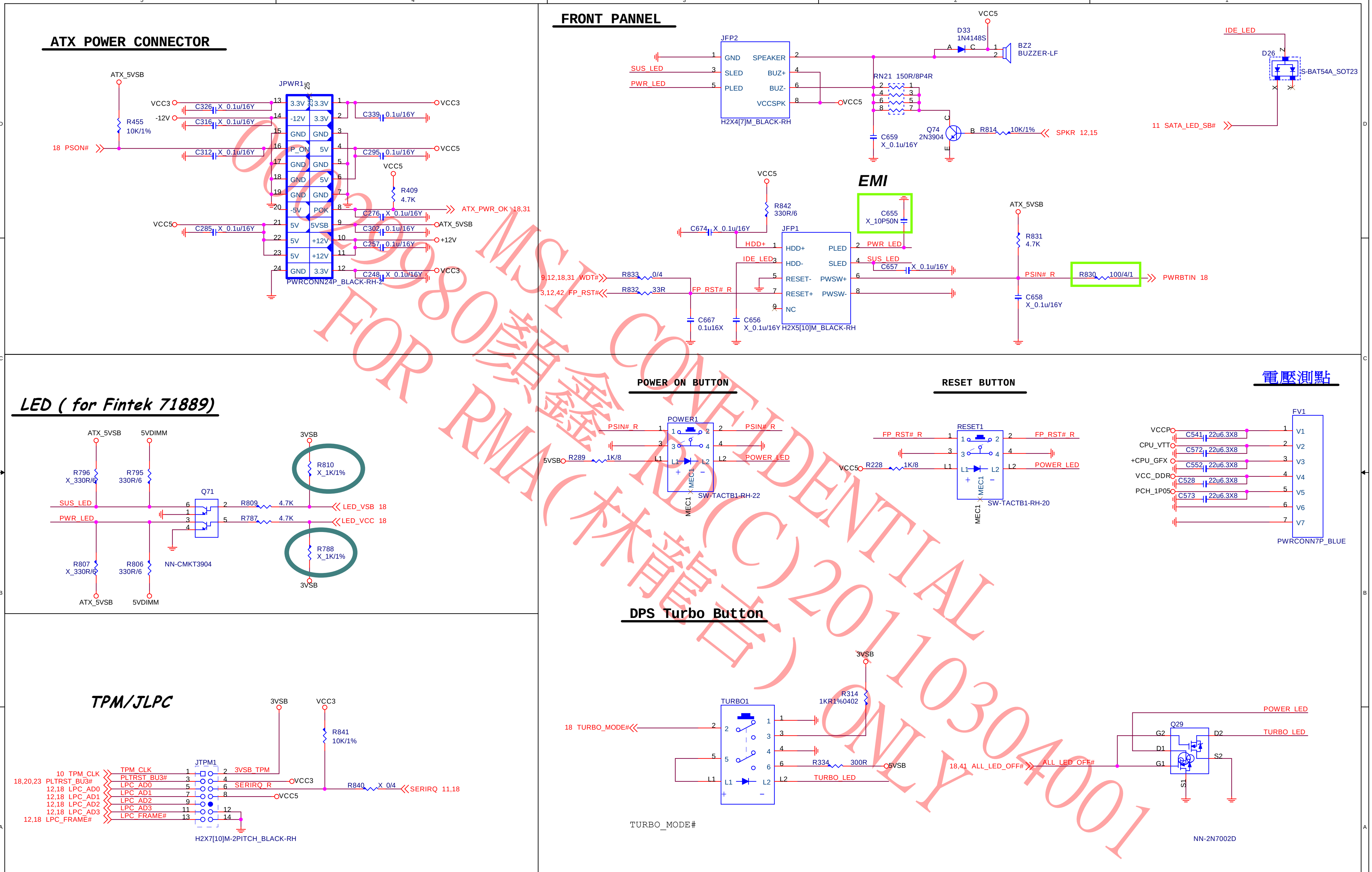

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Size: Custom | Document Description: ATX PWR-Connector & Front Panel & EMI | Rev: 20

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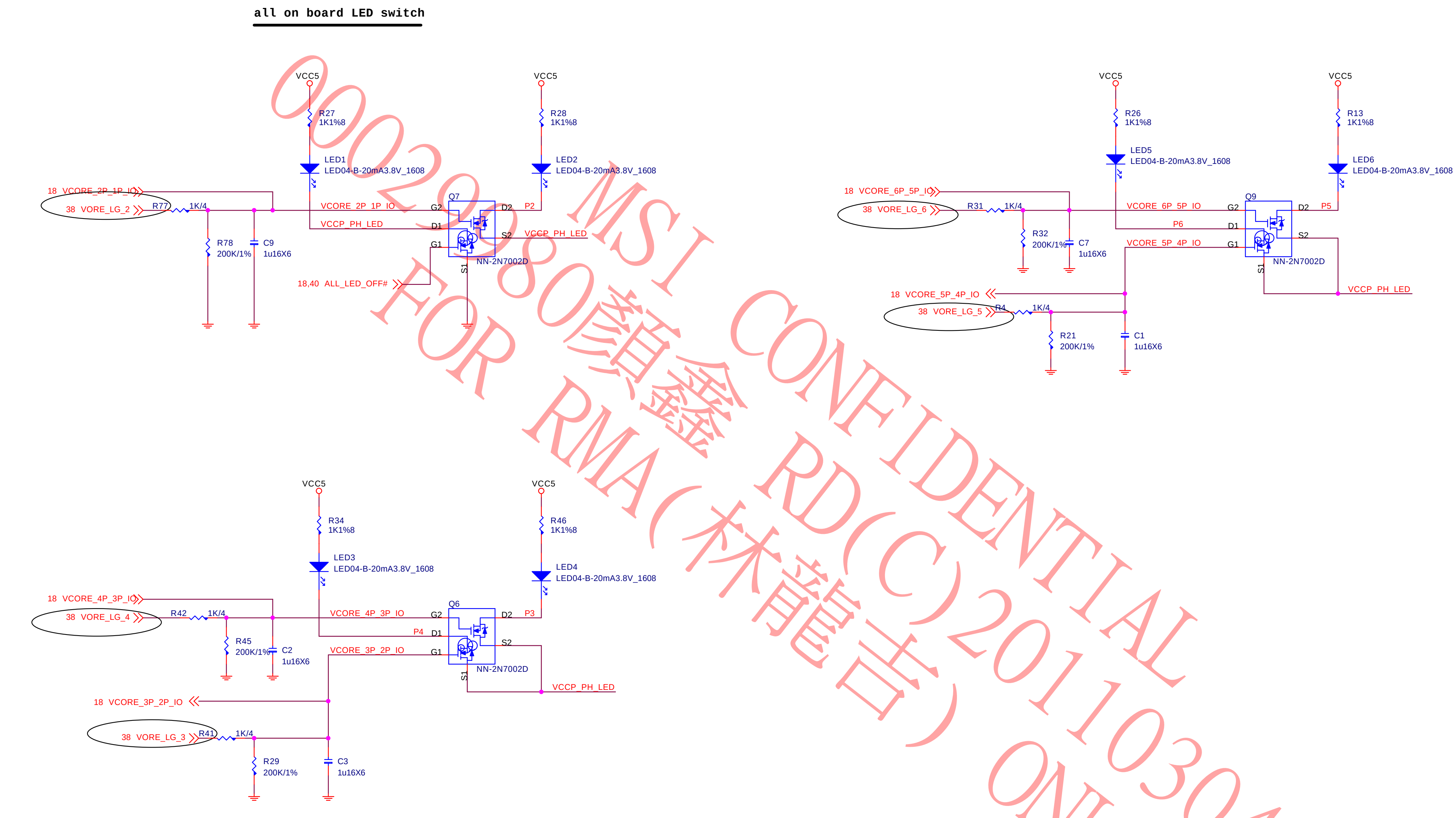
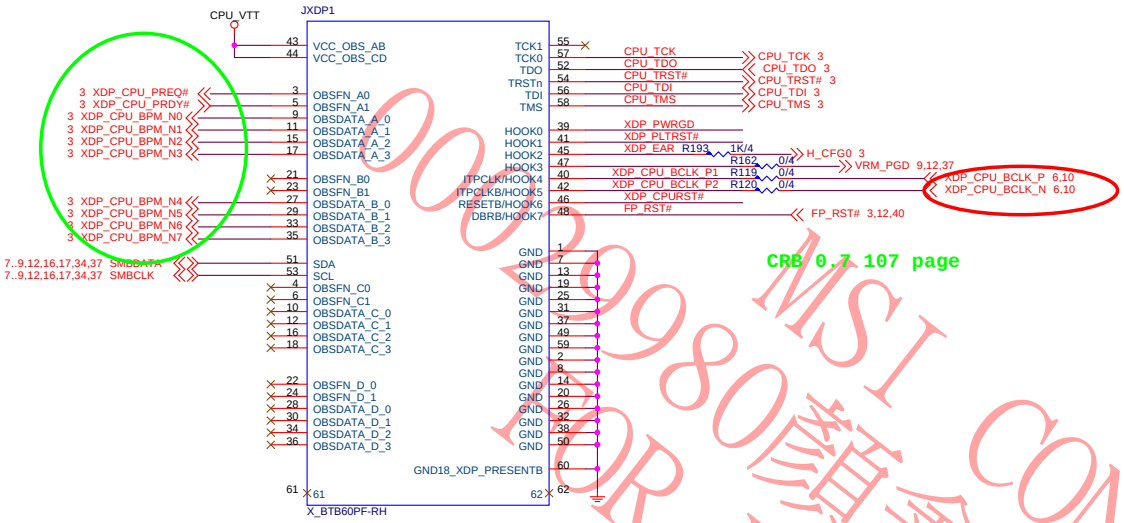
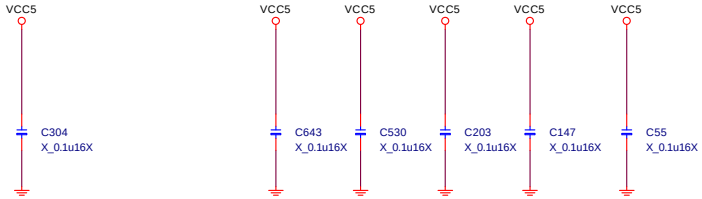


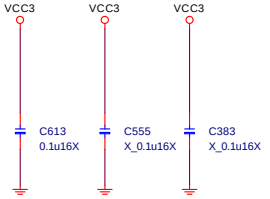
Reserve debug port 5020



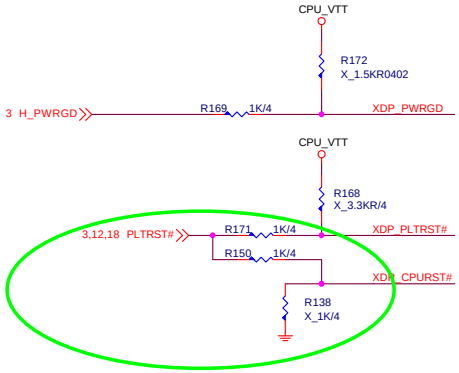
CRB 0.7 107 page

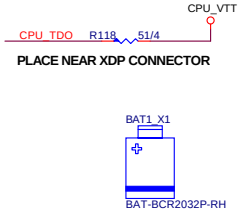
PCH XDP





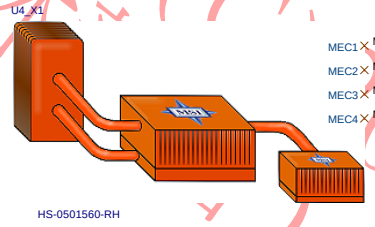
PCH XDP PWRGD/RESET



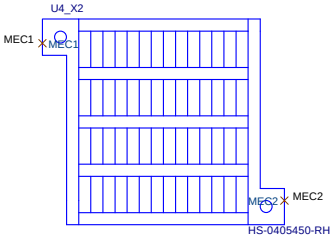


PK0-0767611-E48競華,27,寶安恩斯邁廠(MSIS)
PK0-0767611-G37,精成,27,寶安恩斯邁廠(MSIS)

CPU Heat-pipe

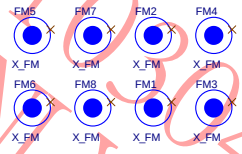


Heat-Sink PCH

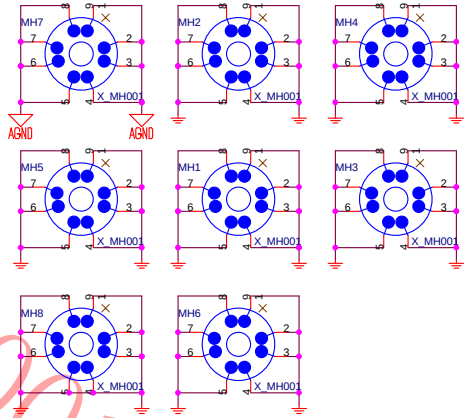


Simulation

Optical Fiducial Marks-120



Mounting Holes



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