Cottonwood Schematic
Broadwell-ULT

2014-06-09
REV : A00

DY : None Installed

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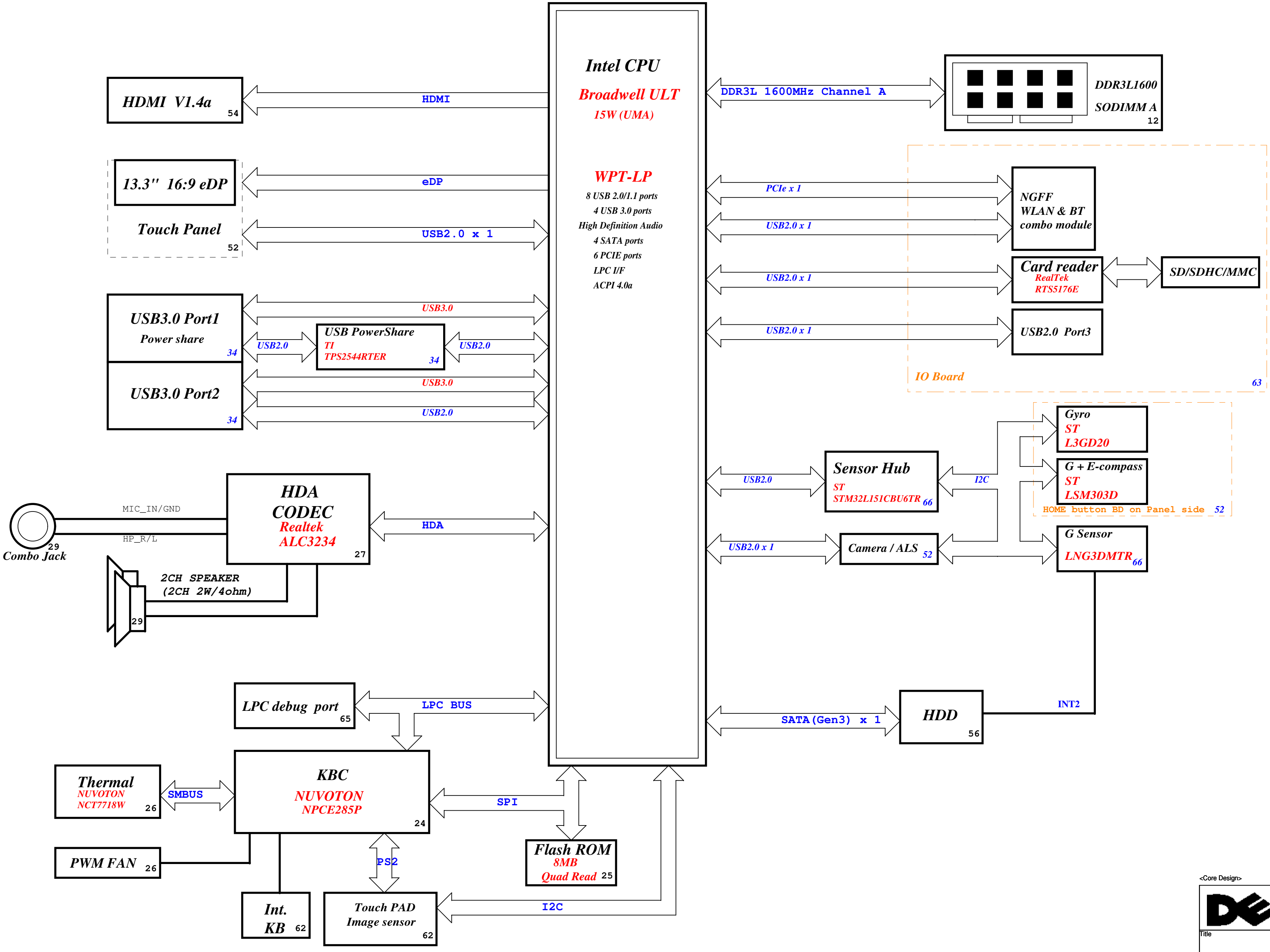
Title		
Cover Page		
Size: A3	Document Number: Cottonwood	Rev: A00
Date: Tuesday, June 17, 2014	Sheet 1 of 104	

Cottonwood Block Diagram

Project code:4PD01V010001
PCB P/N: 13321
Revision: A00



CHARGER	44
BQ24770RUYR-GP	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	45
TPS51225RUKR-GP	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power	46,47
TPS51624RSMR-GP	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR3L SUS	49
TPS51716RUKR-GP	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0

CPU 1.05V	48
SY8208DQNC-GP-U	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

CPU 1D5V_S0	51
TLV70215DBVR-GP	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

Switches	36 83
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Signal

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Title	Block Diagram	
Size C	Document Number: Cottonwood	Rev A00
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Title	(Reserved)	
Size A4	Document Number Cottonwood	Rev A00
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SSID = CPU

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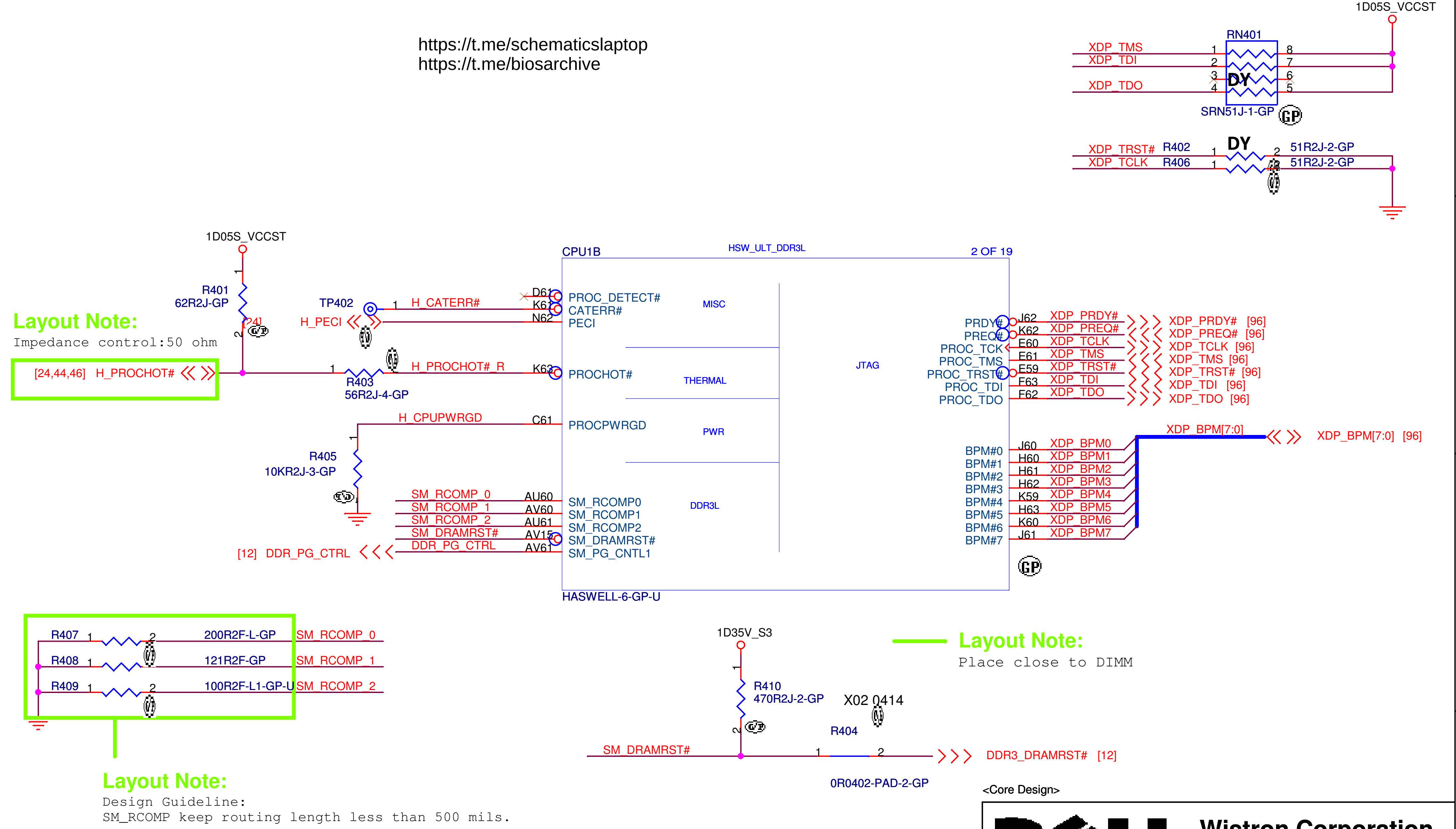

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Title: **CPU (THERMAL/MISC/PM)**

Size: A4 | Document Number: **Cottonwood** | Rev: **A00**

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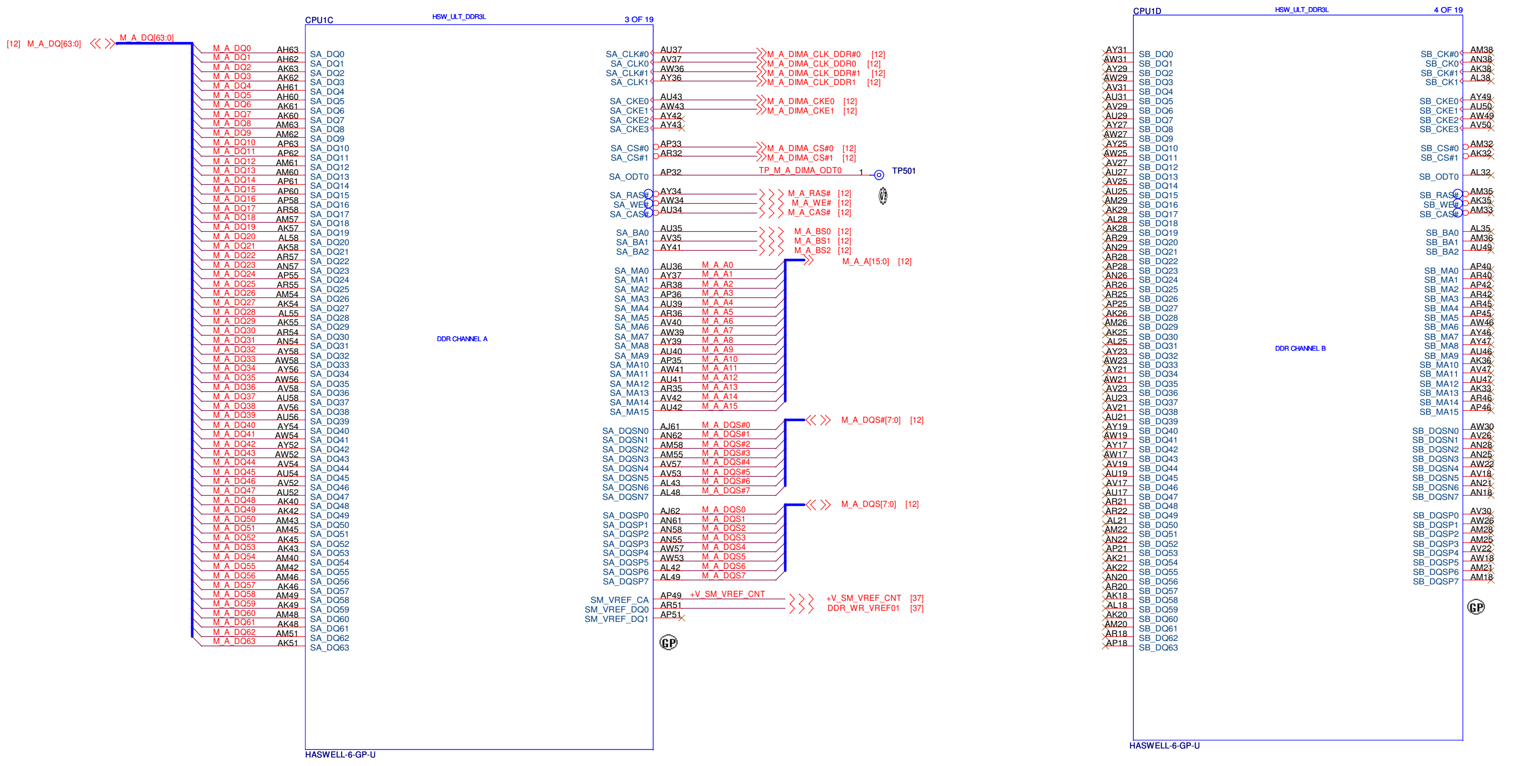
SSID = CPU

DDR3L ball type: Non-Interleaved Type



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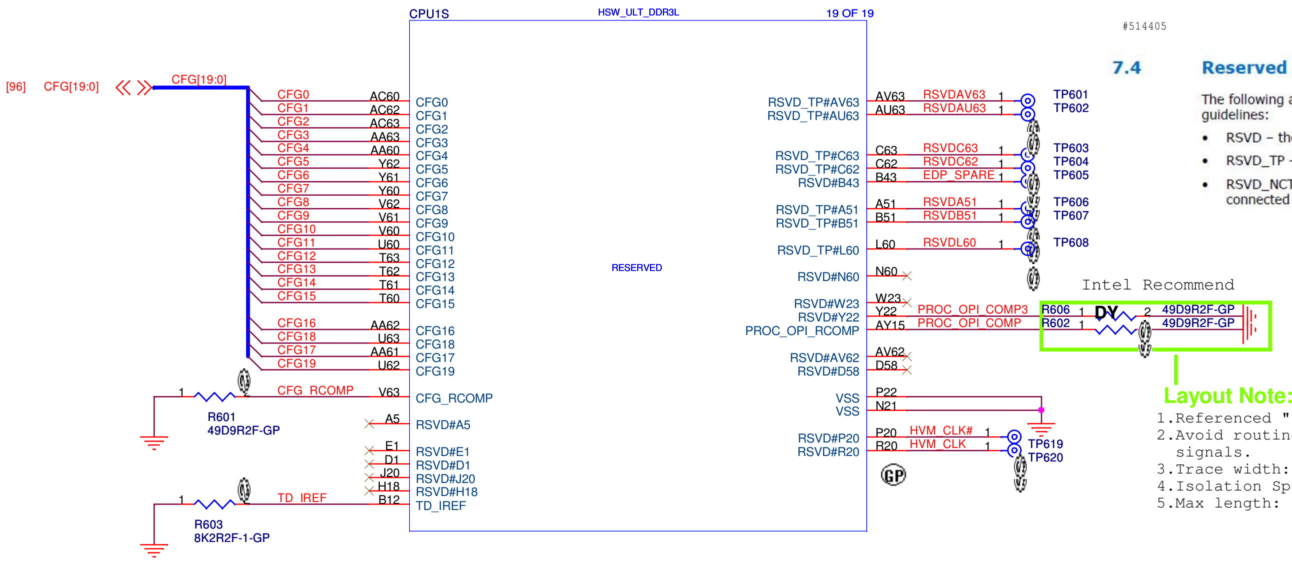
Title	CPU (DDR)
Size A2	Document Number: Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 5 of 104

SSID = CPU



#514405

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

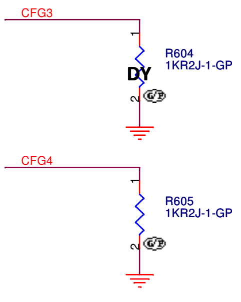
- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

#514405 **PCH strap pin:**

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired. • **CFG[2:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • **CFG[3]: MSR Privacy Bit Feature** — 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting — 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **CFG[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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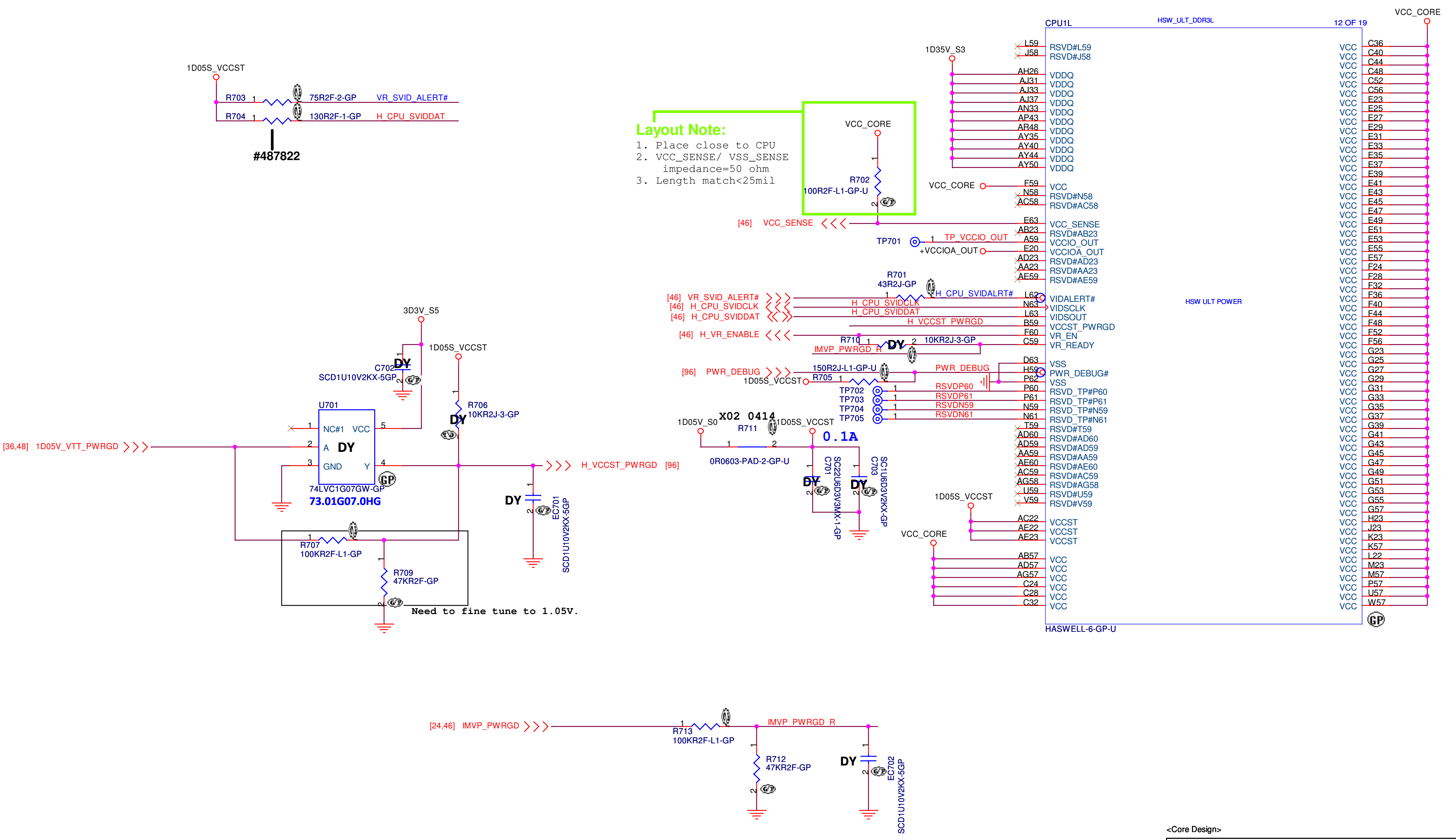
Title	CPU (CFG)	
Size: A3	Document Number: Cottonwood	Rev: A00
Date: Tuesday, June 17, 2014	Sheet 6 of 104	

SSID = CPU



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Title		
CPU (VCC CORE)		
Size: A3	Document Number: Cottonwood	Rev: A00
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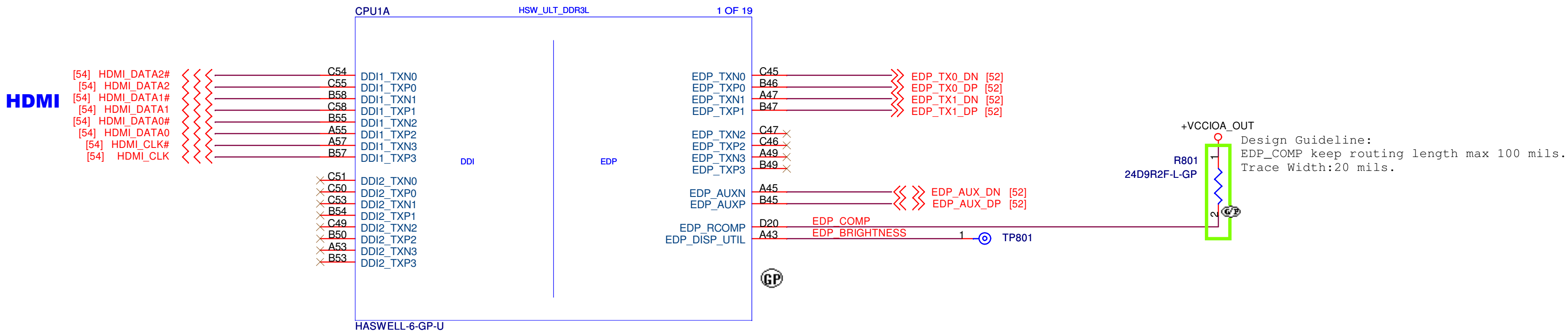
SSID = CPU



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Title: **CPU (DDI/EDP)**

Size	Document Number	Rev
A3	Cottonwood	A00

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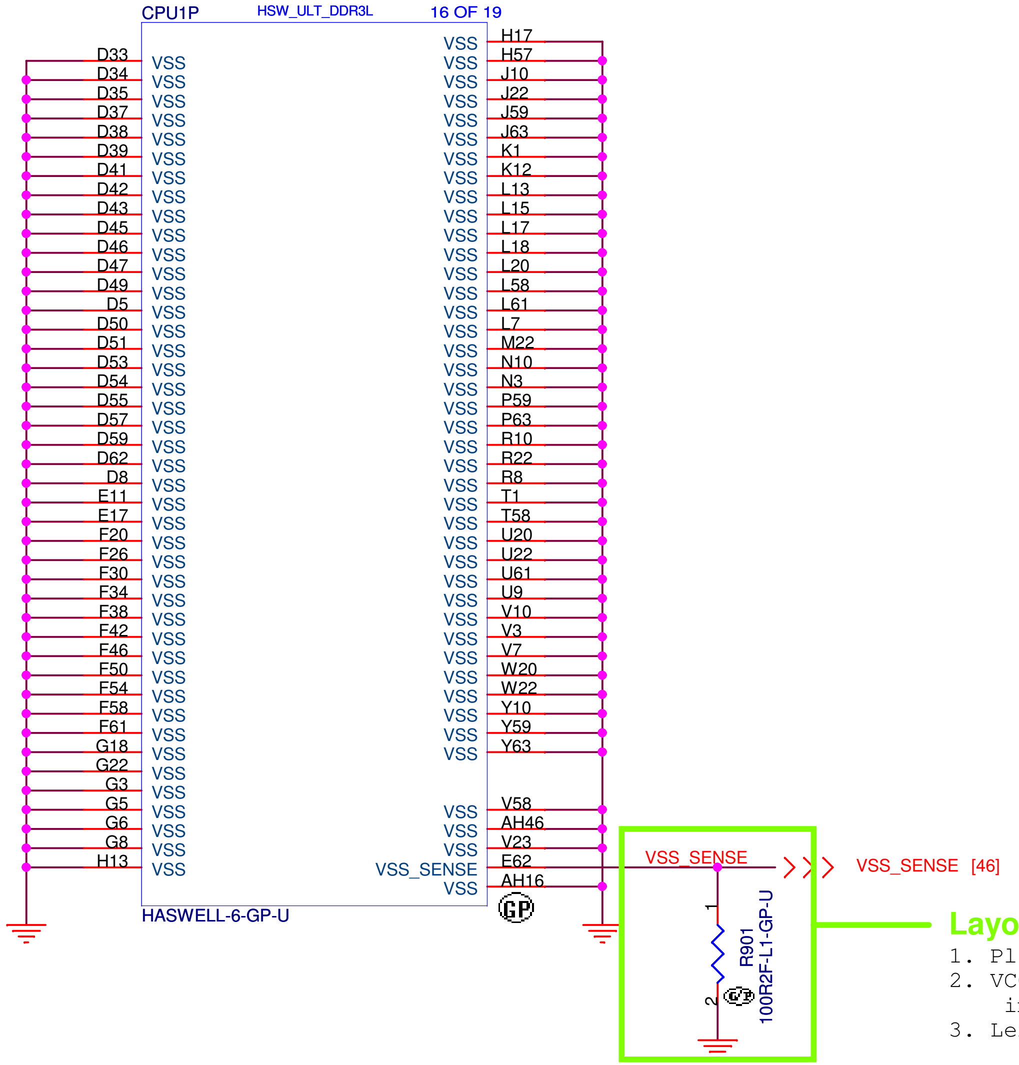
5 4 3 2 1

SSID = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

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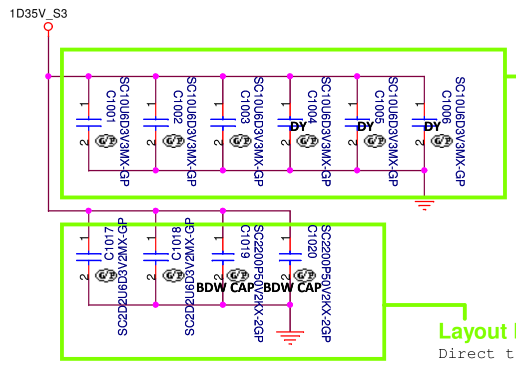
DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	**CPU (VSS)**		
Size A4	Document Number **Cottonwood**		Rev **A00**
Date: Tuesday, June 17, 2014		Sheet 9 of 104	

5 4 3 2 1

SSID = CPU



Layout Note:
As close to CPU as possible

Layout Note:
Direct tie to CPU VccIn/Vss balls

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Title		
CPU (Power CAP1)		
Size: A3	Document Number: Cottonwood	Rev: A00
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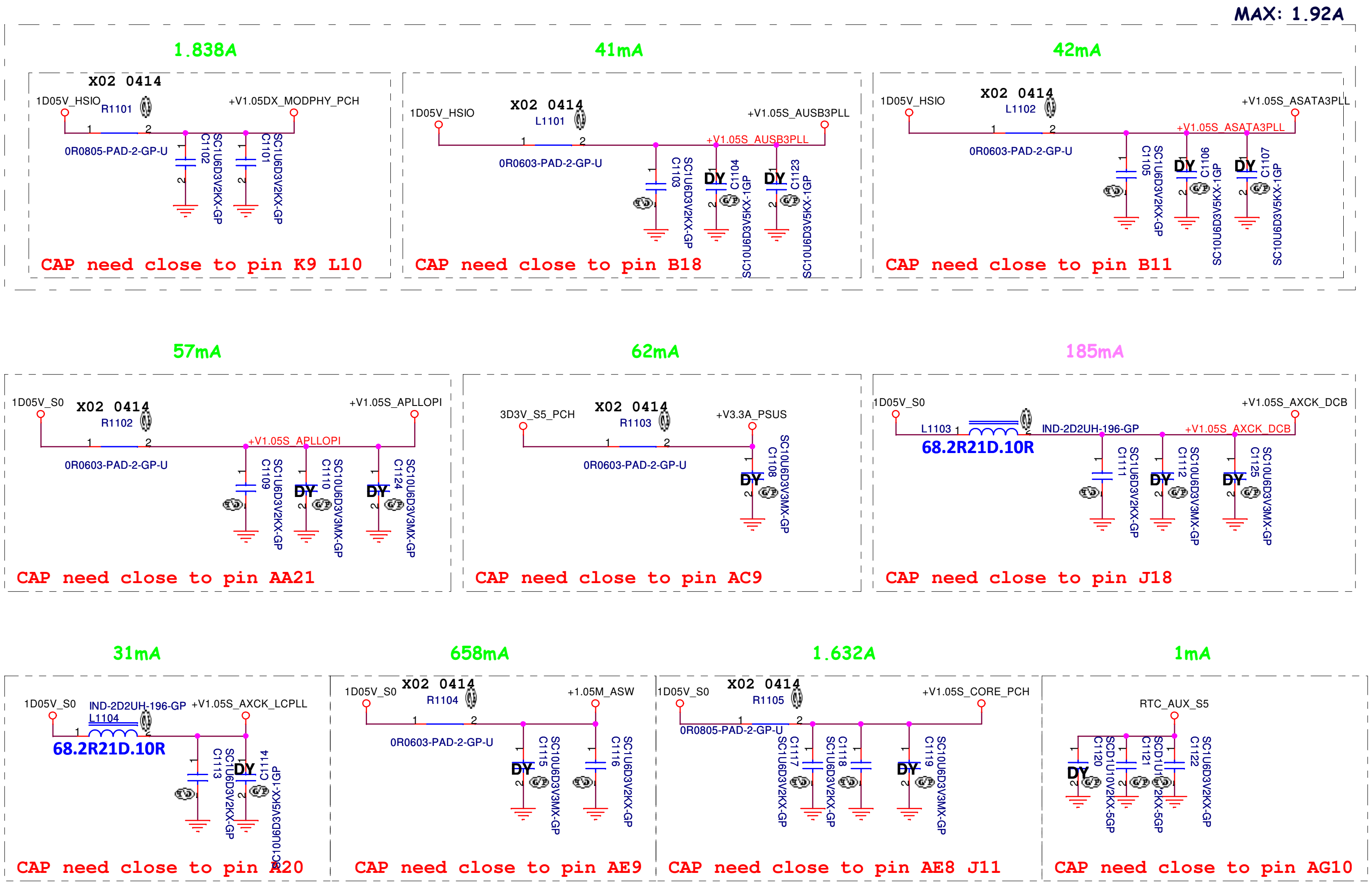

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Title: CPU (Power CAP2)		
Size: A3	Document Number: Cottonwood	Rev: A00
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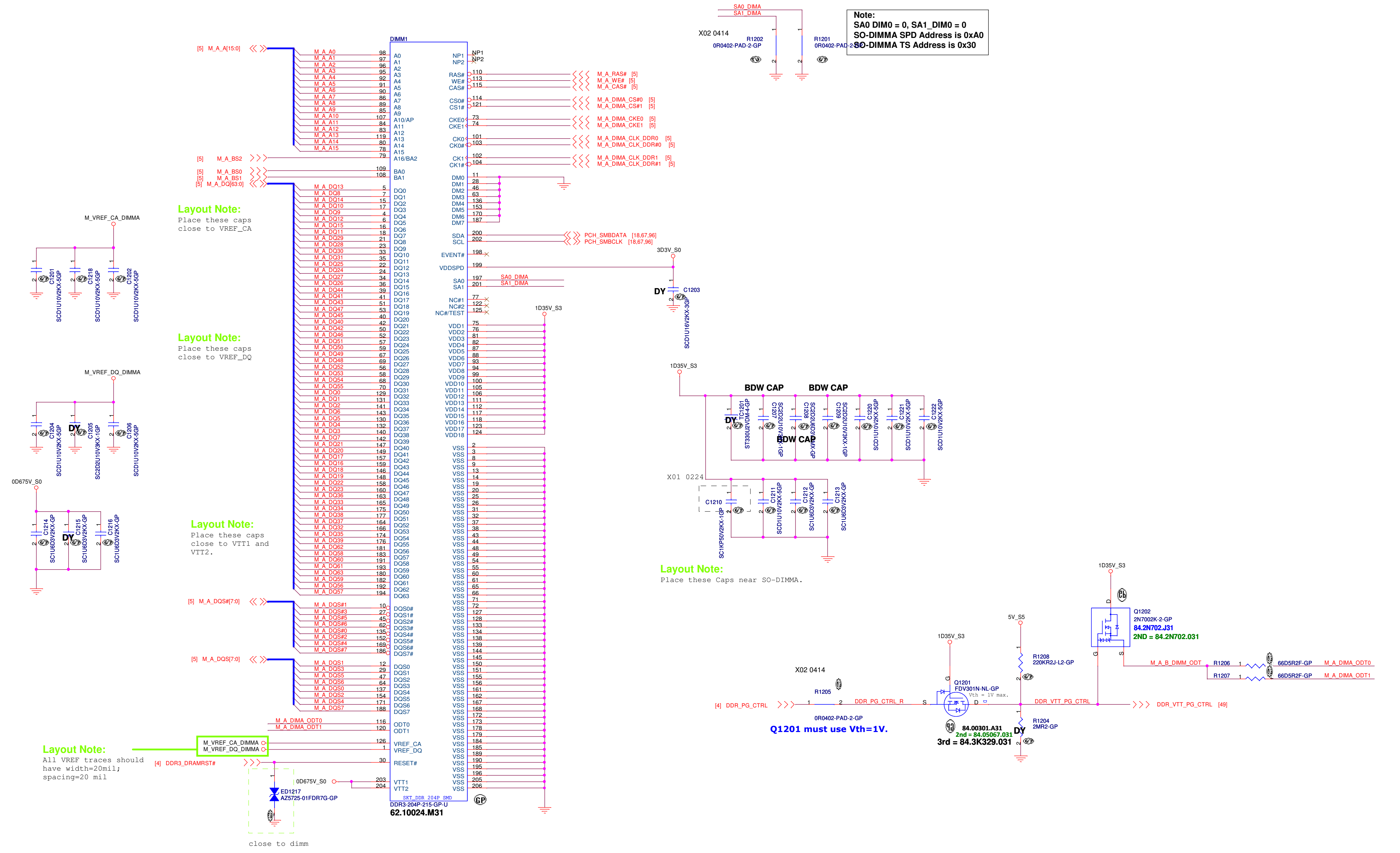
SSID = MEMORY



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Title		
DDR3-SODIMM1		
Size: A2	Document Number: Cottonwood	Rev: A00
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Title	(Reserved)DDR3-SODIMM2	
Size A3	Document Number Cottonwood	Rev A00
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Title	(Reserved)_SODIMM _SODIMM4	
Size A4	Document Number Cottonwood	Rev A00
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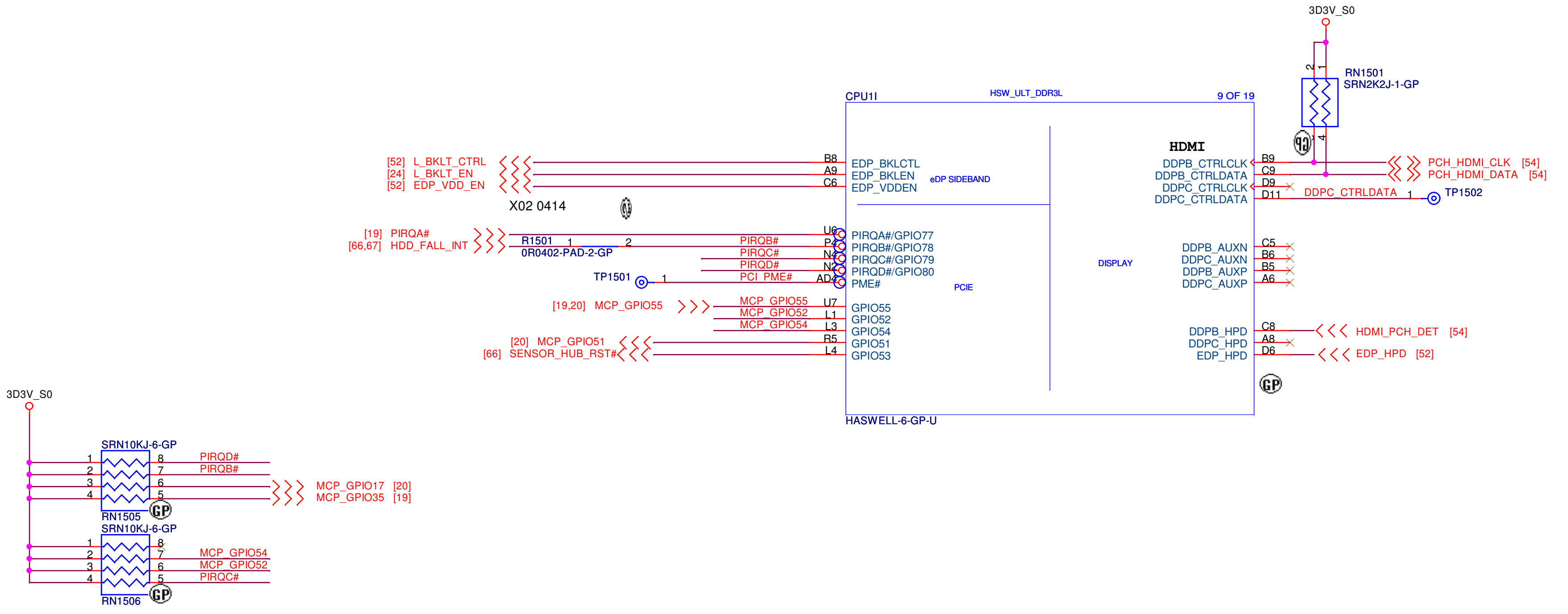
SSID = CPU



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Title: PCH (EDP/GPIO/DDI)

Size	Document Number	Rev
A3	Cottonwood	A00

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SSID = PCH

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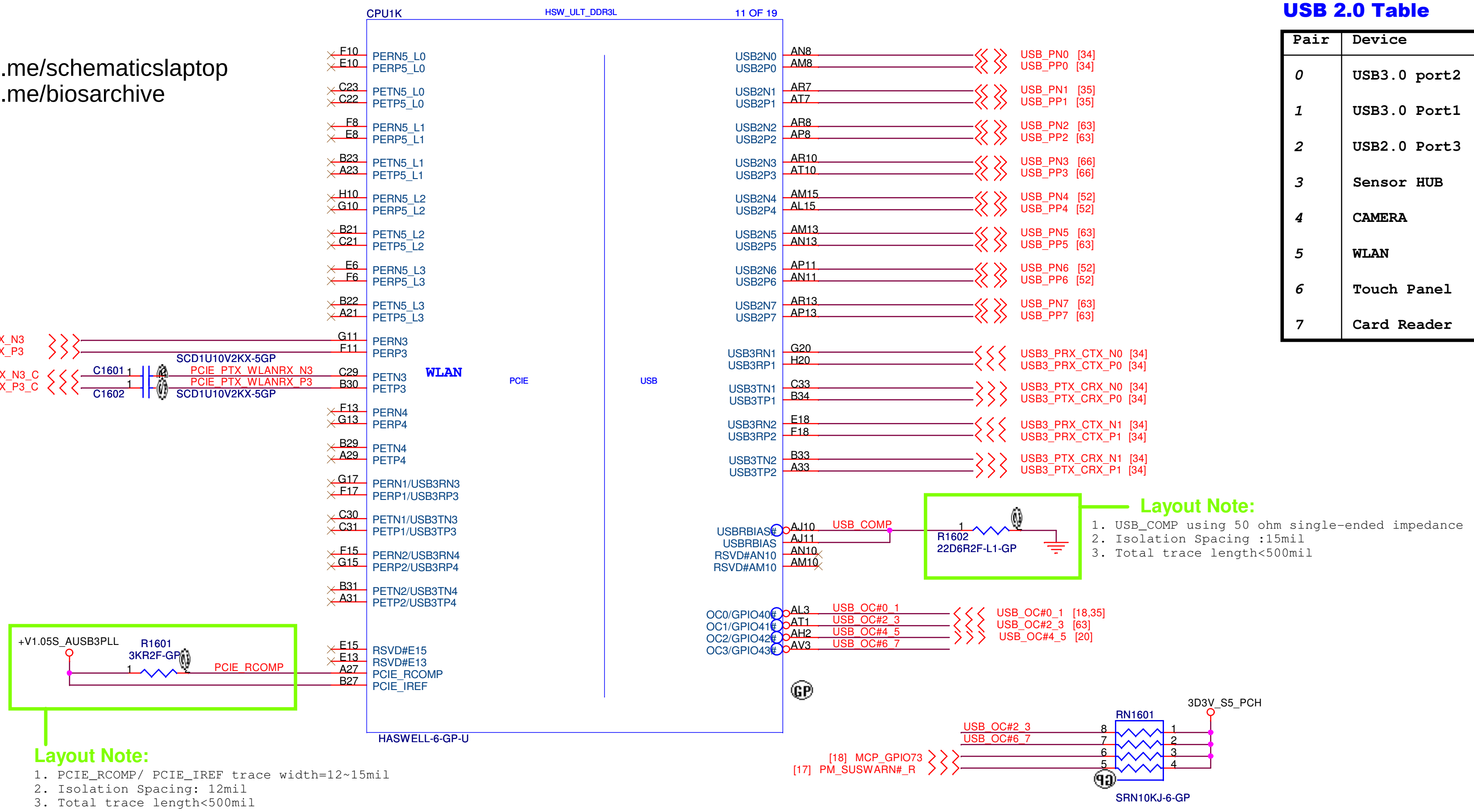

USB 2.0 Table

Pair	Device
0	USB3.0 port2
1	USB3.0 Port1 (Debug Port)
2	USB2.0 Port3 (IOBD)
3	Sensor HUB
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	N/A	
5 (L0~L3)	N/A	
6 (L3)	HDD	SATA0
6 (L2)	N/A	SATA1
6 (L0~L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3 / PCIe* Port 1 SSD	USB 3.0 Port 4 / PCIe* Port 2 SSD	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD GPU	PCIe* Port 5 Lane 1 SSD GPU	PCIe* Port 5 Lane 2 GPU	PCIe* Port 5 Lane 3 GPU	SATA 6Gb/s Port 3 / PCIe* Port 6 Lane 0 SSD	SATA 6Gb/s Port 2 / PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1 / PCIe* Port 6 Lane 2	SATA 6Gb/s Port 0 / PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3 / PCIe* Port 1 SSD	USB 3.0 Port 4 / PCIe* Port 2 SSD	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD GPU	PCIe* Port 5 Lane 1 SSD GPU	PCIe* Port 5 Lane 2 GPU	PCIe* Port 5 Lane 3 GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0

SSID = PCH

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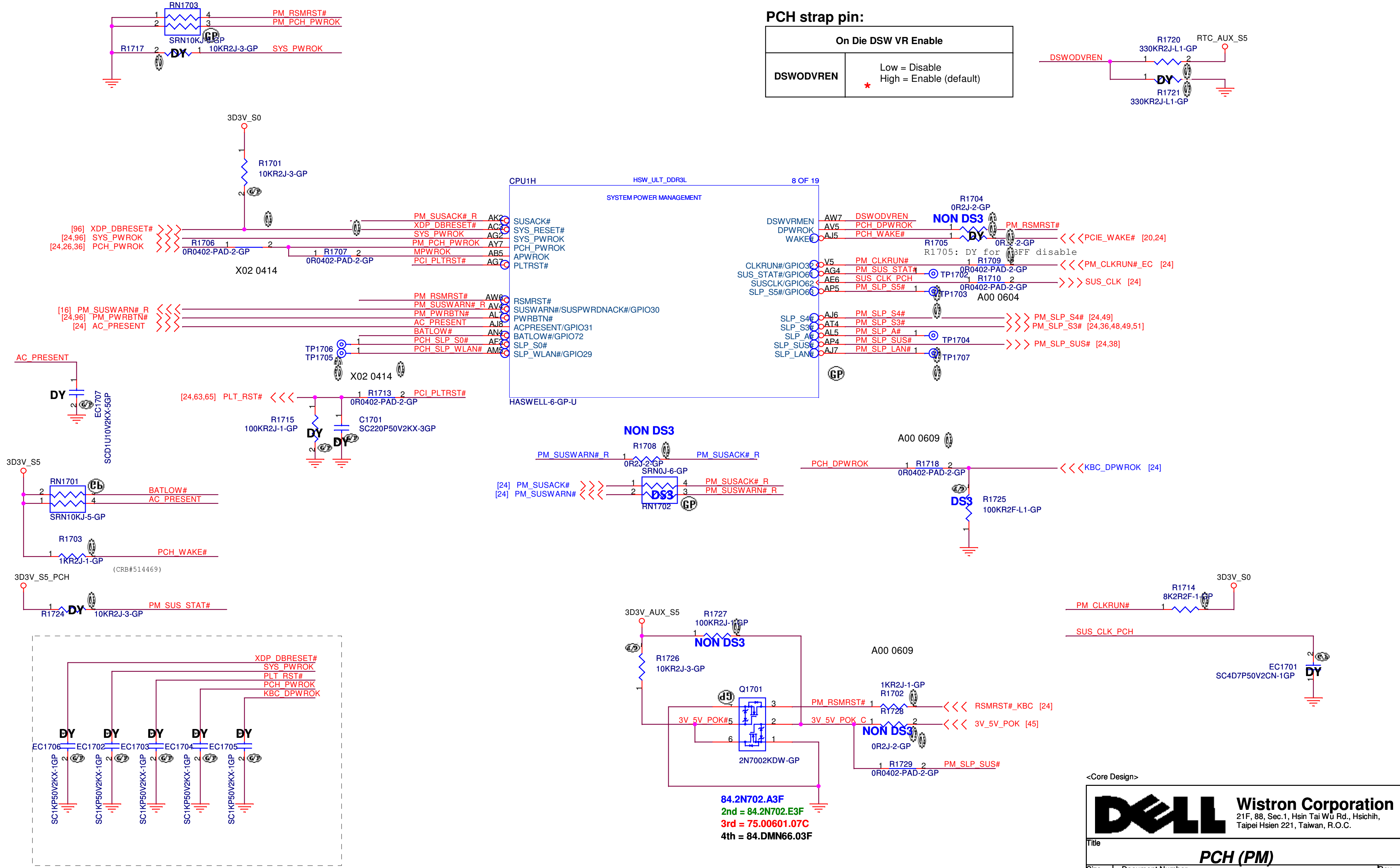
PCH strap pin:

On Die DSW VR Enable	
DSWODVREN	Low = Disable * High = Enable (default)



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Title	PCH (PM)	
Size: A3	Document Number: Cottonwood	Rev: A00
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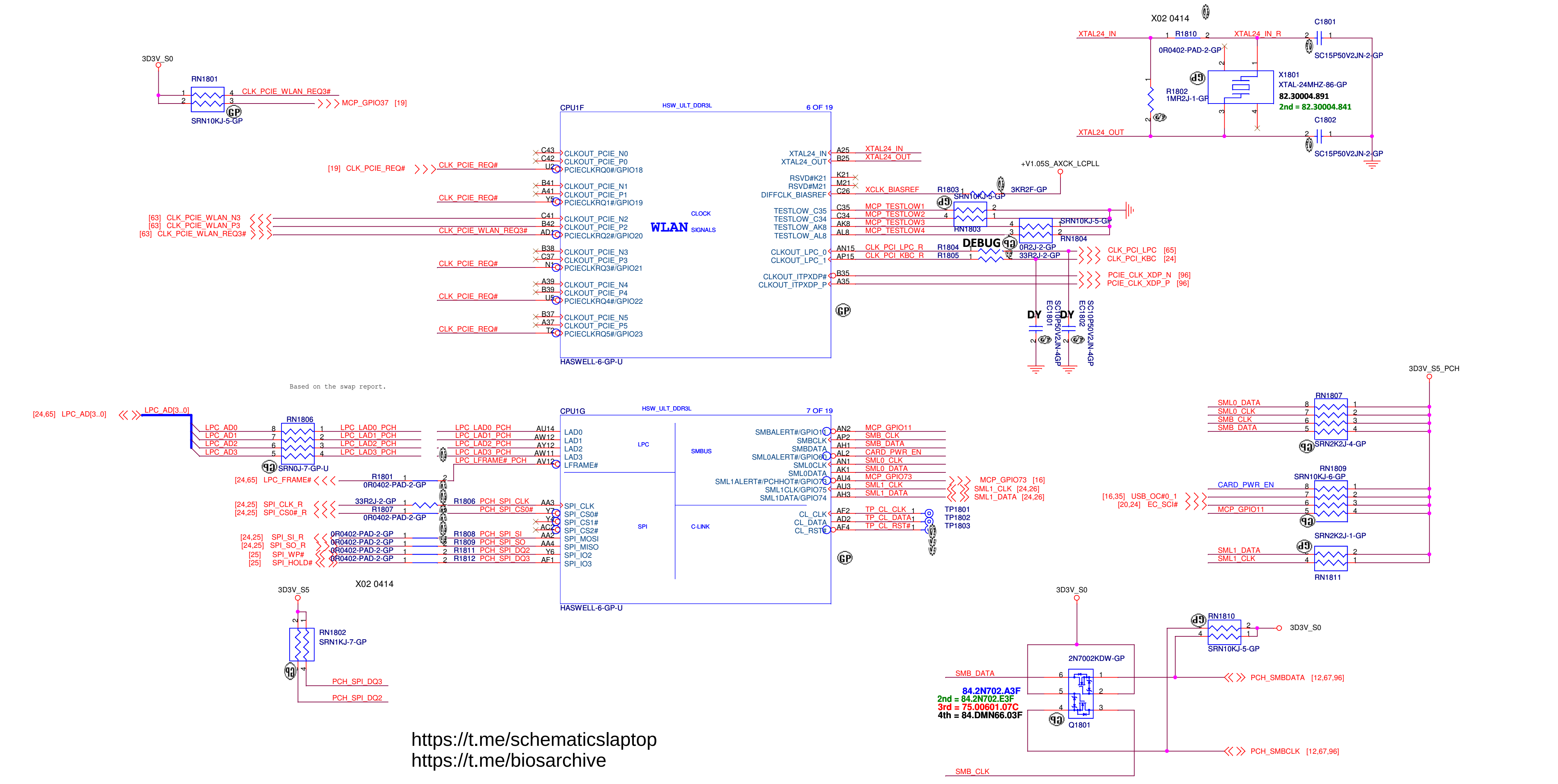
SSID = PCH



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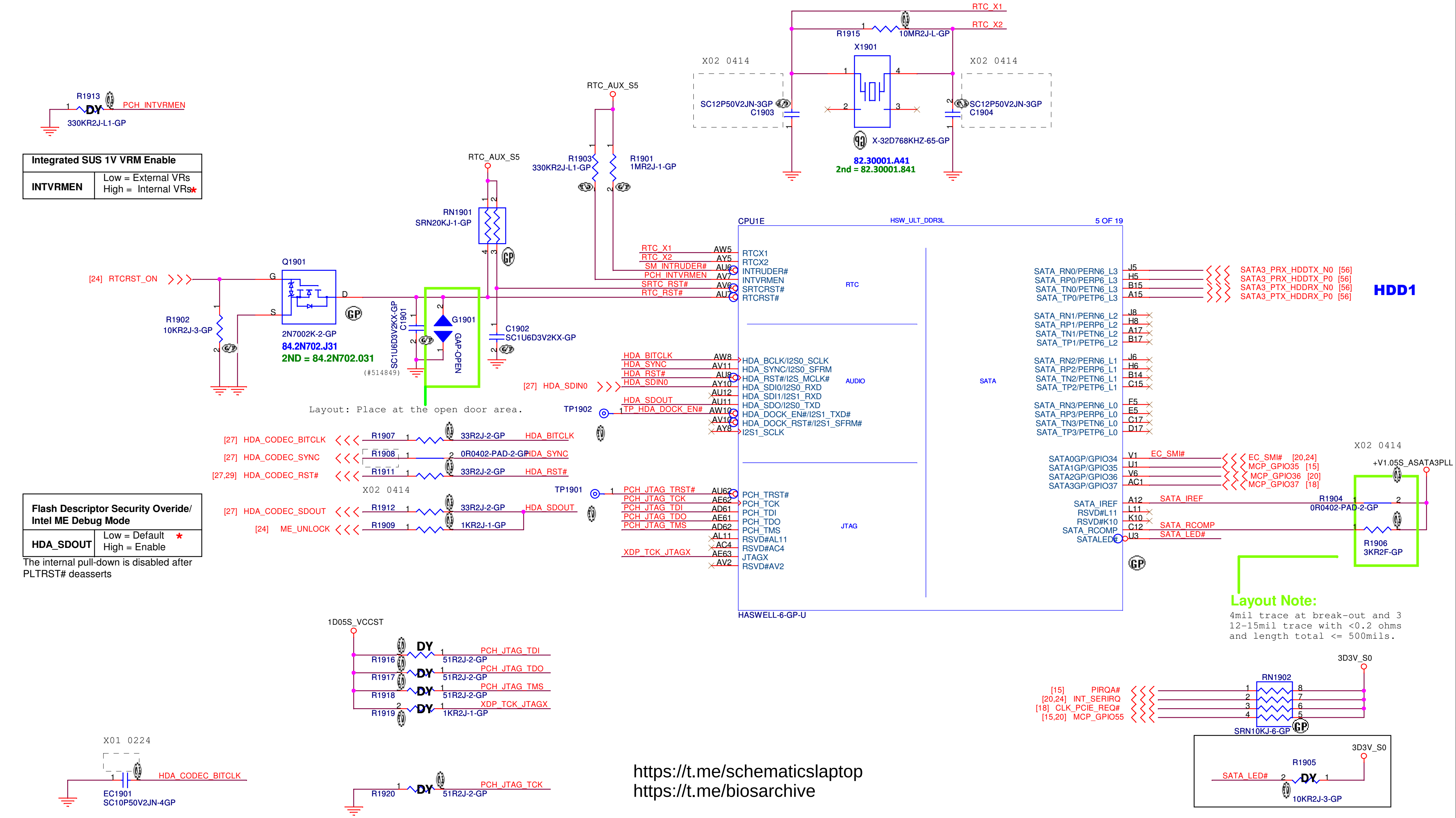
Title: PCH (CLOCK/SMBUS/CL/LPC/SPI)

Size: Custom | Document Number: Cottonwood | Rev: A00

Date: Tuesday, June 17, 2014 | Sheet 18 of 104

SSID = CPU



Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs *

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Layout Note:
4mil trace at break-out and 3 12-15mil trace with <0.2 ohms and length total <= 500mils.

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Title	PCH (RTC/SATA/HDA/JTAG)	
Size A3	Document Number: Cottonwood	Rev A00
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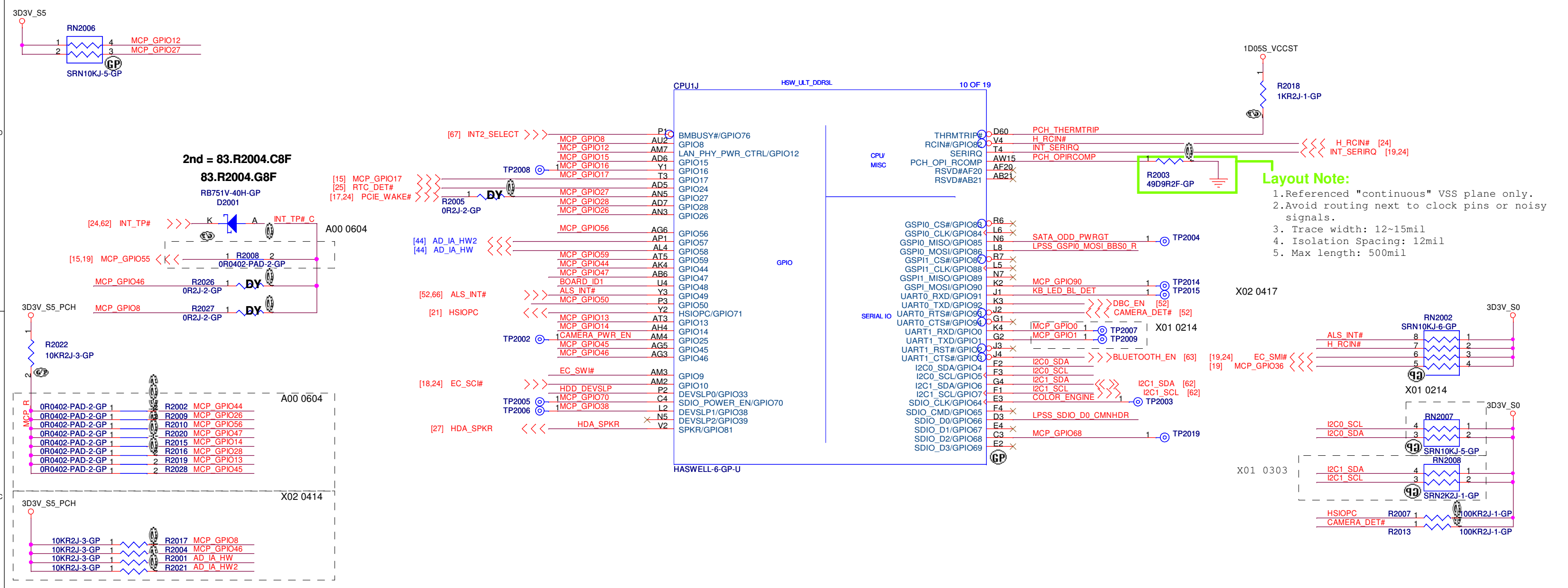
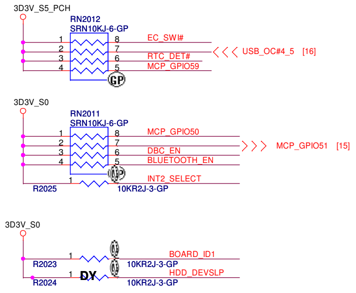
SSID = CPU



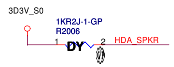
Layout Note:
1.Referenced "continuous" VSS plane only.
2.Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PCH strap pin:

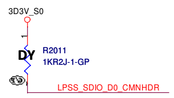
NO REBOOT	
HDA_SPKR	★ Low = Disable (Default) High = Enable

The internal pull-down is disabled after PLTRST# deasserts



Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode (Default) ★ Low = Disable "Top-Block swap" mode

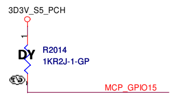
The internal pull-down is disabled after PLTRST# deasserts



Need SW double confirm if that's needed Top-Block swap

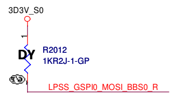
TLS Confidentiality	
GPIO15	★Low = Disable Intel ME Crypto TLS High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.



Boot BIOS Strap Bit BBS	
Boot BIOS Destination	★ Low = SPI High = LPC

The internal pull-down is disabled after PLTRST# deasserts



Need double confirm, GPIO table set to GPI if that's needed PH or PL

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Title		
CPU (GPIO/MISC)		
Size A2	Document Number Cottonwood	Rev A00
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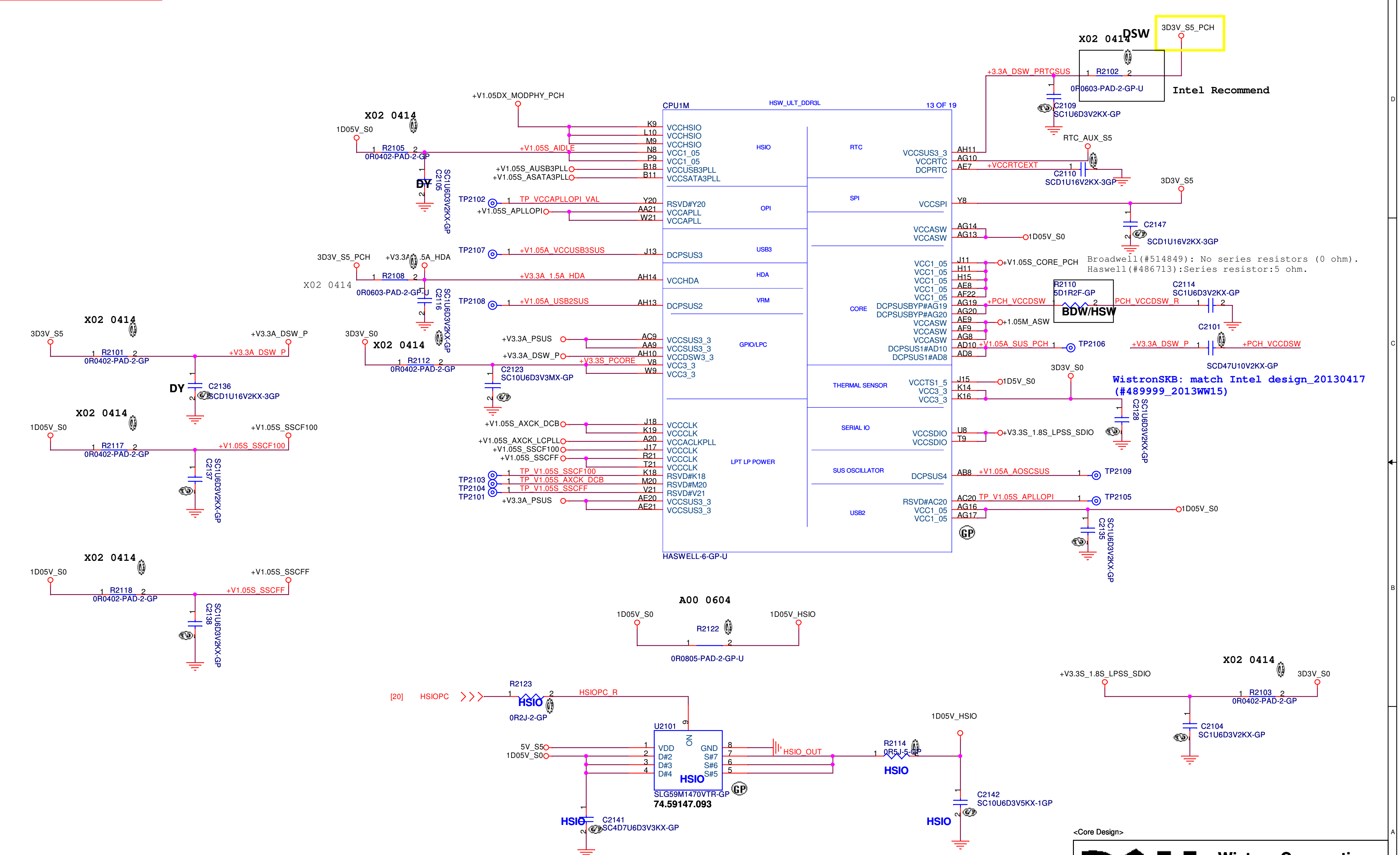
SSID = CPU



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Title: CPU (POWER2)

Size	Document Number	Rev
A3	Cottonwood	A00

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SSID = PCH

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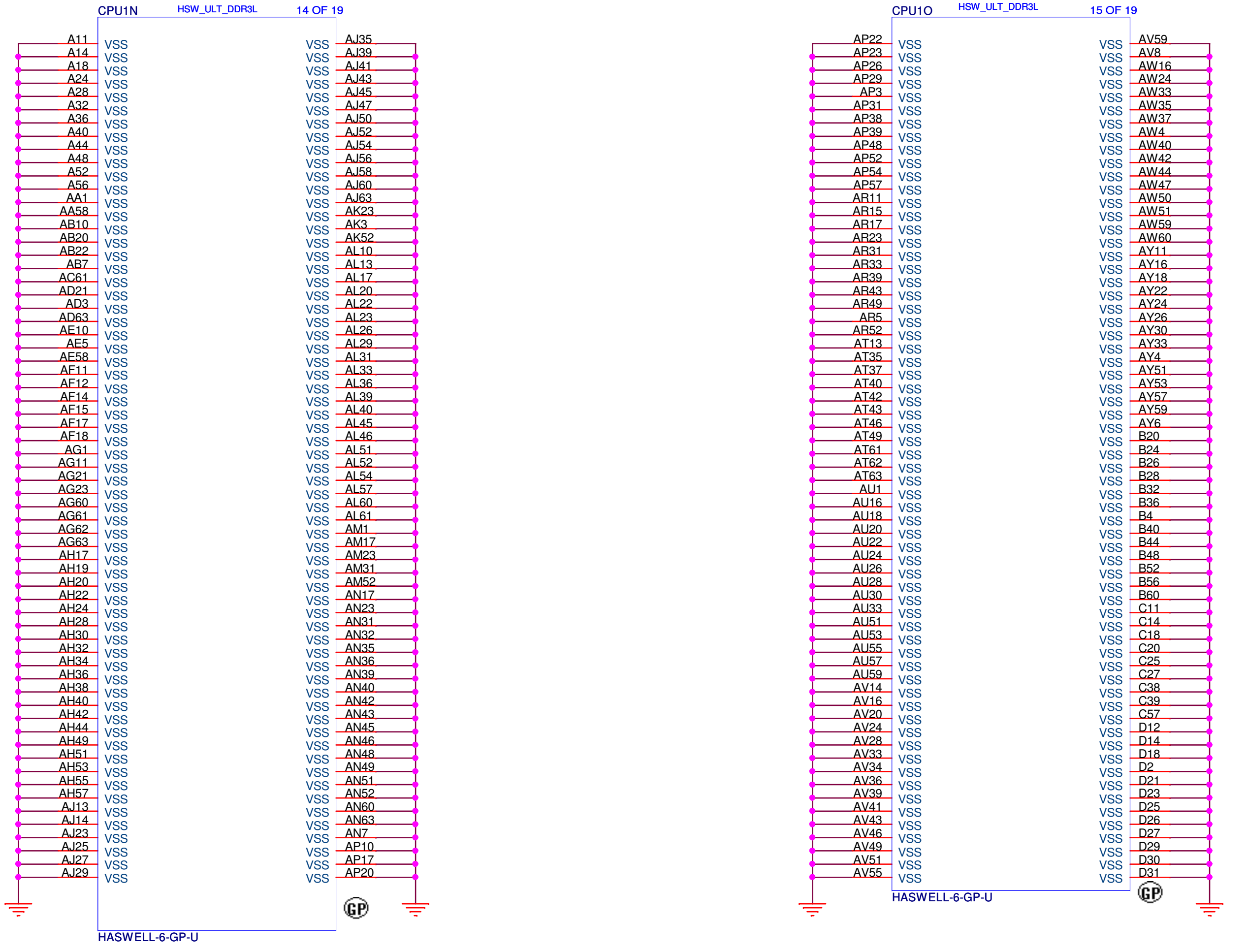
Title: **CPU (RSVD)**		
Size: A4	Document Number: **Cottonwood**	Rev: **A00**
Date: Tuesday, June 17, 2014	Sheet 22 of 104	

SSID = PCH



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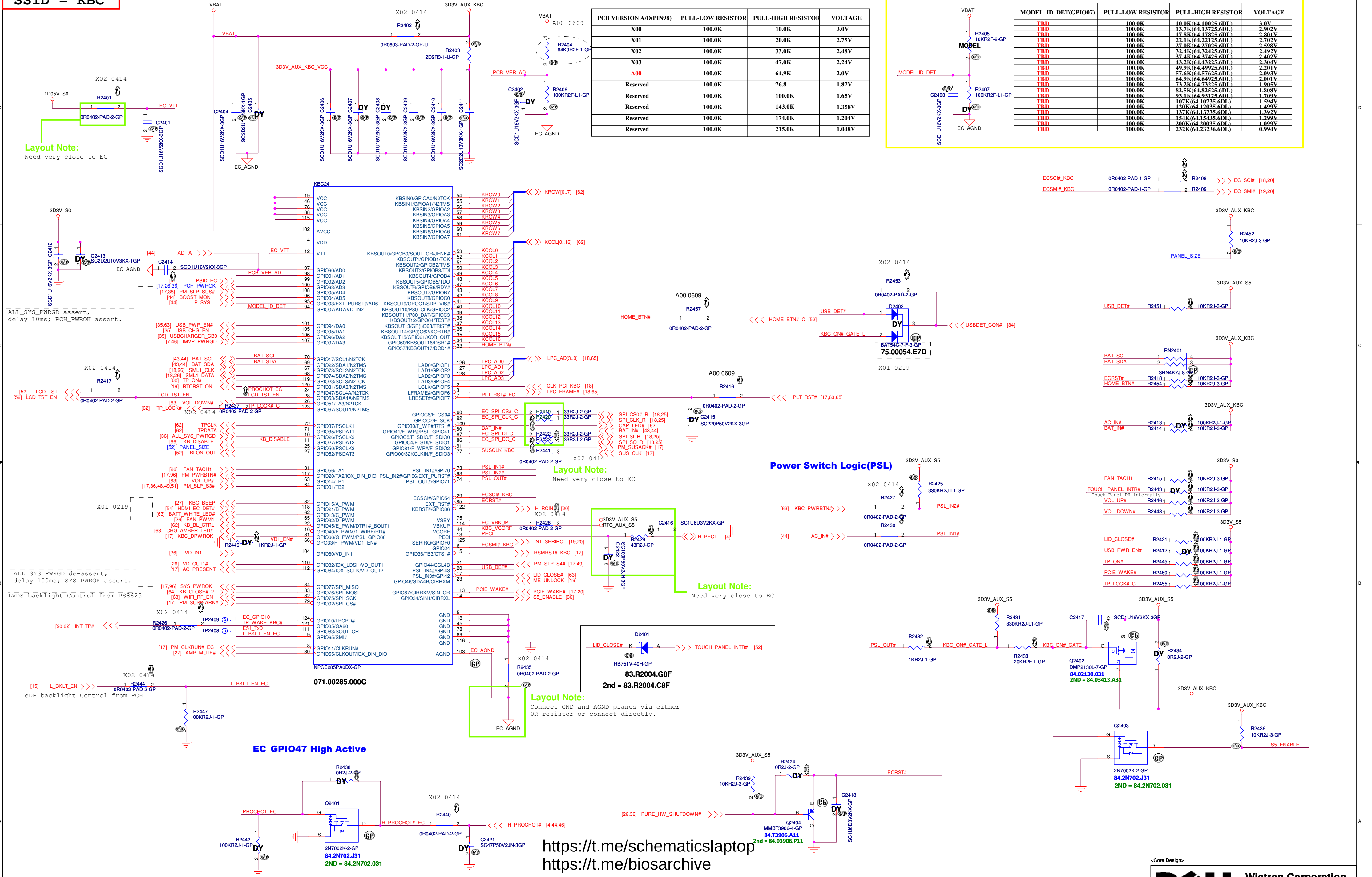
Title	*CPU(VSS)*	
Size A3	Document Number *Cottonwood*	Rev *A00*
Date: Tuesday, June 17, 2014	Sheet 23 of 104	

SSID = KBC



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
TBD	100.0K	10.0K(64.10025.6DL)	3.0V
TBD	100.0K	13.7K(64.13725.6DL)	2.902V
TBD	100.0K	17.8K(64.17825.6DL)	2.801V
TBD	100.0K	22.1K(64.22125.6DL)	2.702V
TBD	100.0K	27.0K(64.27025.6DL)	2.598V
TBD	100.0K	32.4K(64.32425.6DL)	2.492V
TBD	100.0K	37.4K(64.37425.6DL)	2.402V
TBD	100.0K	43.2K(64.43225.6DL)	2.304V
TBD	100.0K	49.9K(64.49925.6DL)	2.201V
TBD	100.0K	57.6K(64.57625.6DL)	2.093V
TBD	100.0K	64.9K(64.64925.6DL)	2.001V
TBD	100.0K	73.2K(64.73225.6DL)	1.905V
TBD	100.0K	82.5K(64.82525.6DL)	1.808V
TBD	100.0K	93.1K(64.93125.6DL)	1.709V
TBD	100.0K	107K(64.10735.6DL)	1.594V
TBD	100.0K	120K(64.12035.6DL)	1.499V
TBD	100.0K	137K(64.13735.6DL)	1.392V
TBD	100.0K	154K(64.15435.6DL)	1.299V
TBD	100.0K	200K(64.20035.6DL)	1.099V
TBD	100.0K	232K(64.23236.6DL)	0.994V

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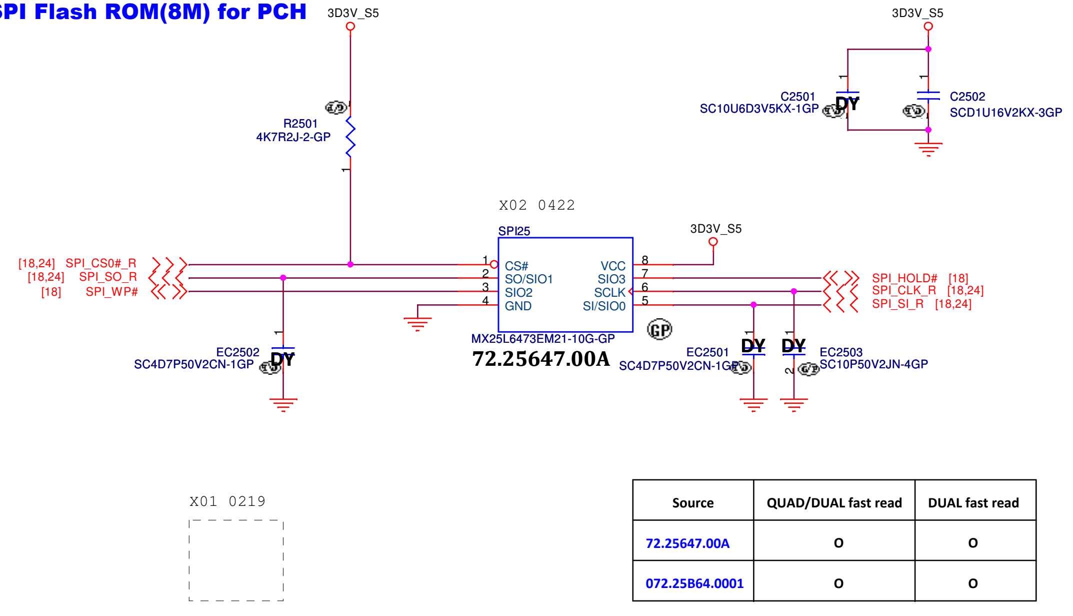
Title: KBC Nuvoton NPCE885

Size: Custom | Document Number: Cottonwood | Rev: A00

Date: Tuesday, June 17, 2014 |

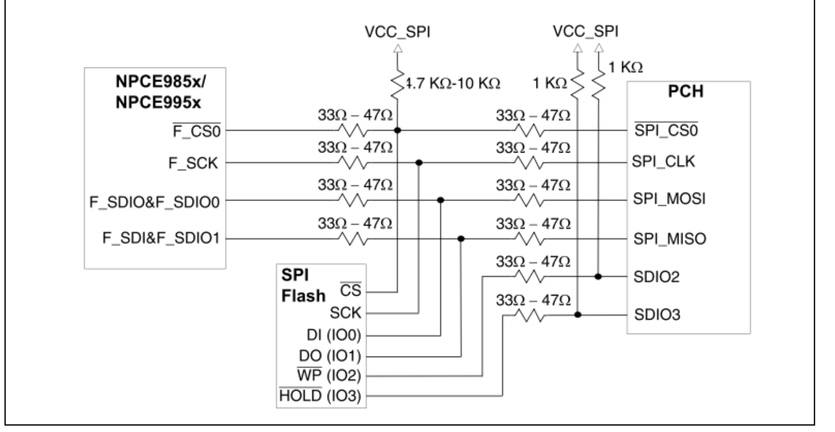
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



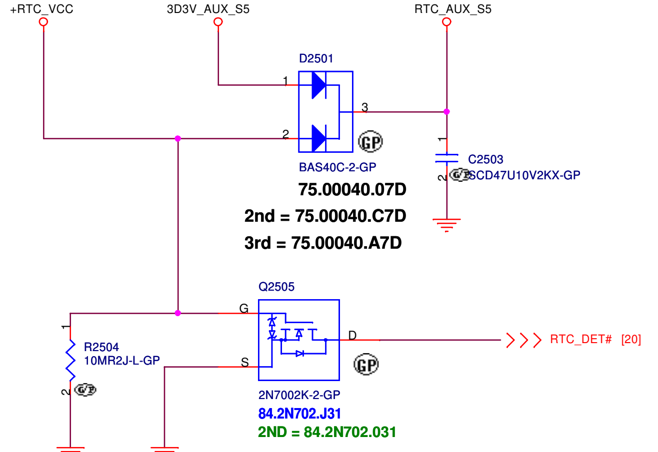
Source	QUAD/DUAL fast read	DUAL fast read
72.25647.00A	O	O
072.25B64.0001	O	O

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



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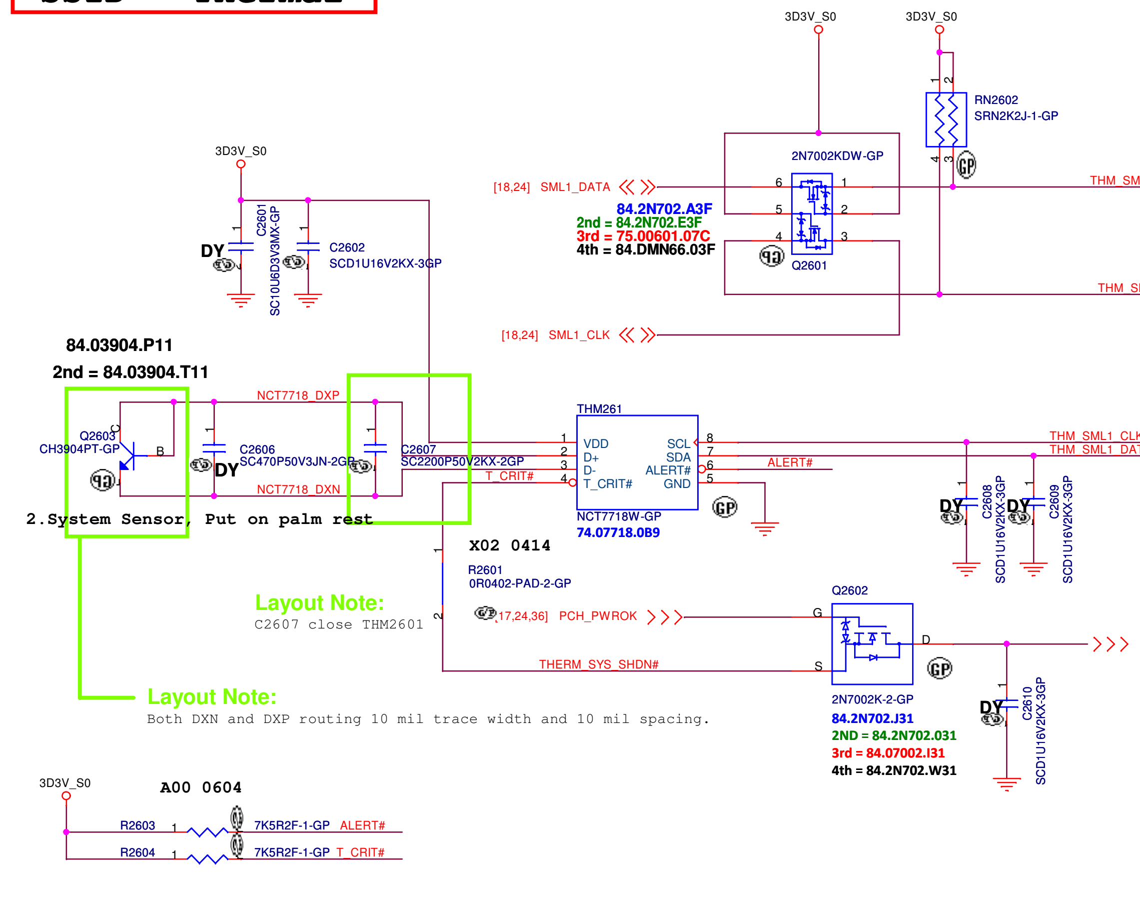
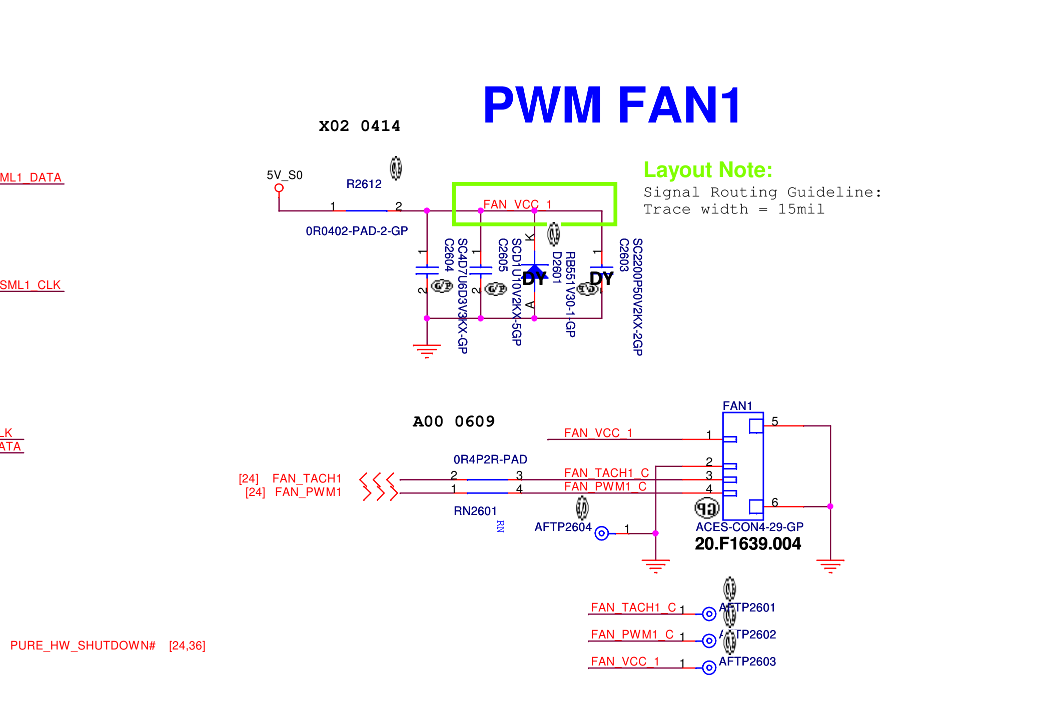
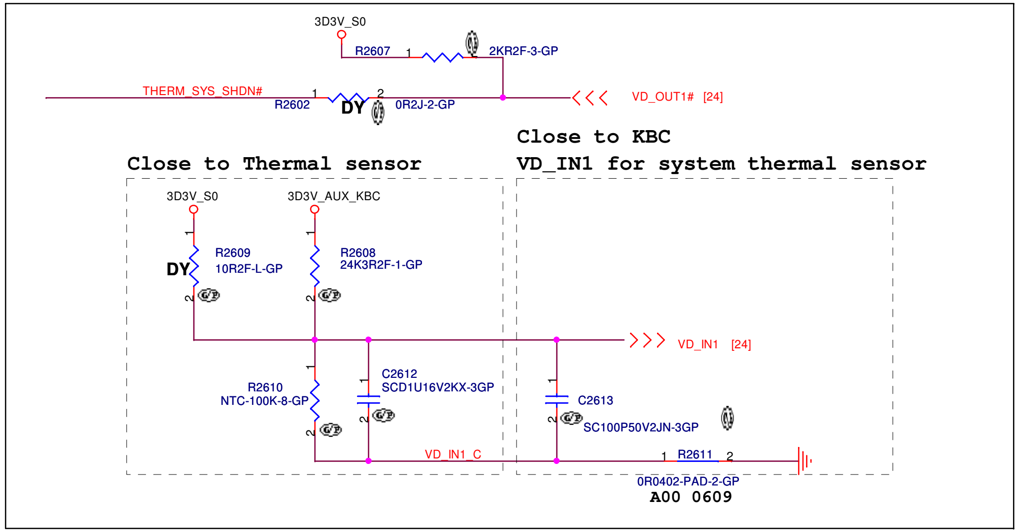
https://t.me/biosarchive

SSID = Thermal





KBC T8



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

https://t.me/schematicslaptop
https://t.me/biosarchive

<Core Design>

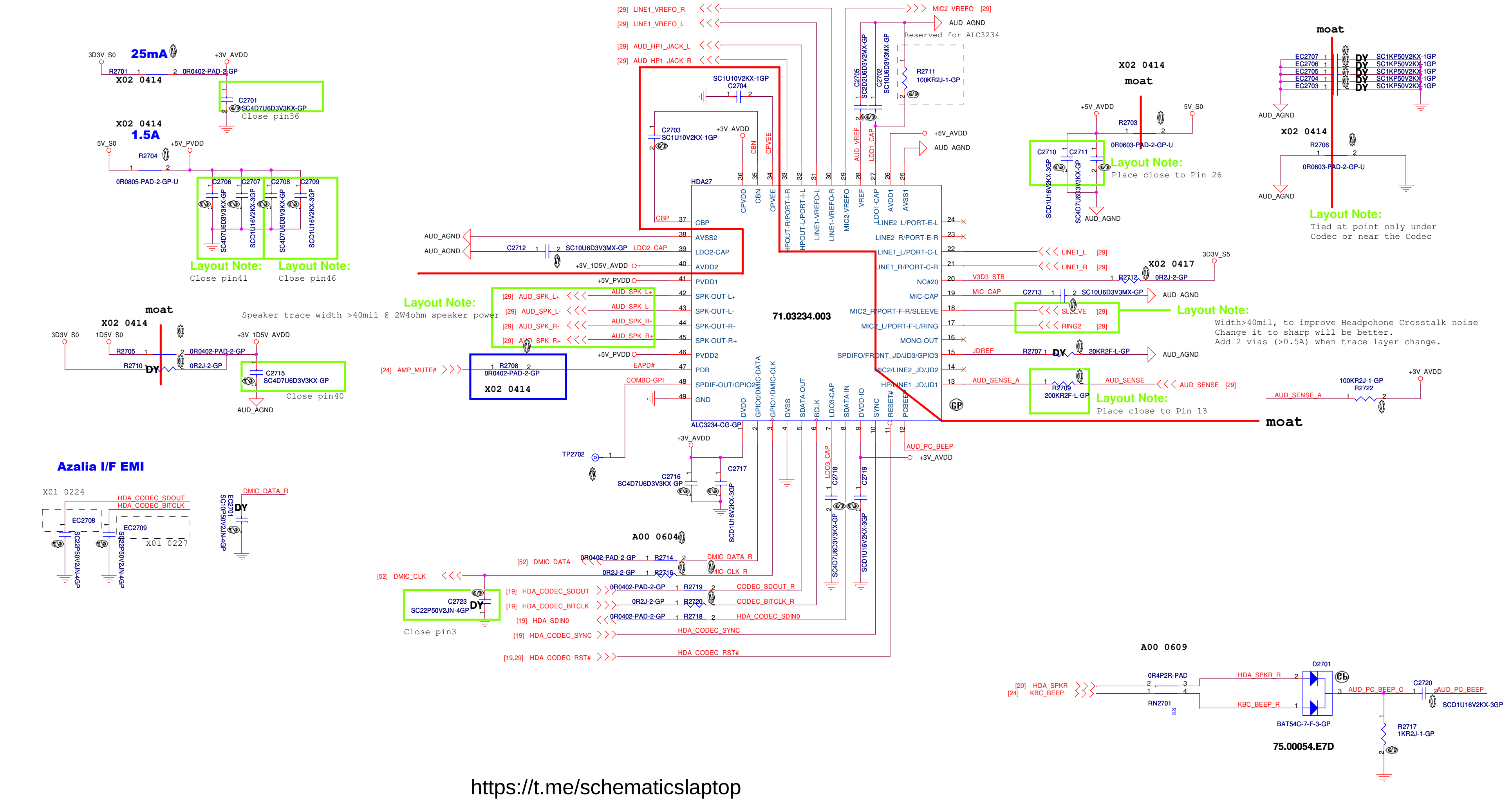
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: A3 | Document Number: Cottonwood | Rev: A00

Date: Tuesday, June 17, 2014 | Sheet 26 of 104

SSID = AUDIO



https://t.me/schematicslaptop
https://t.me/biosarchive

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Codec ALC3223	
Size A2	Document Number Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 27 of 104	

SSID = AUDIO

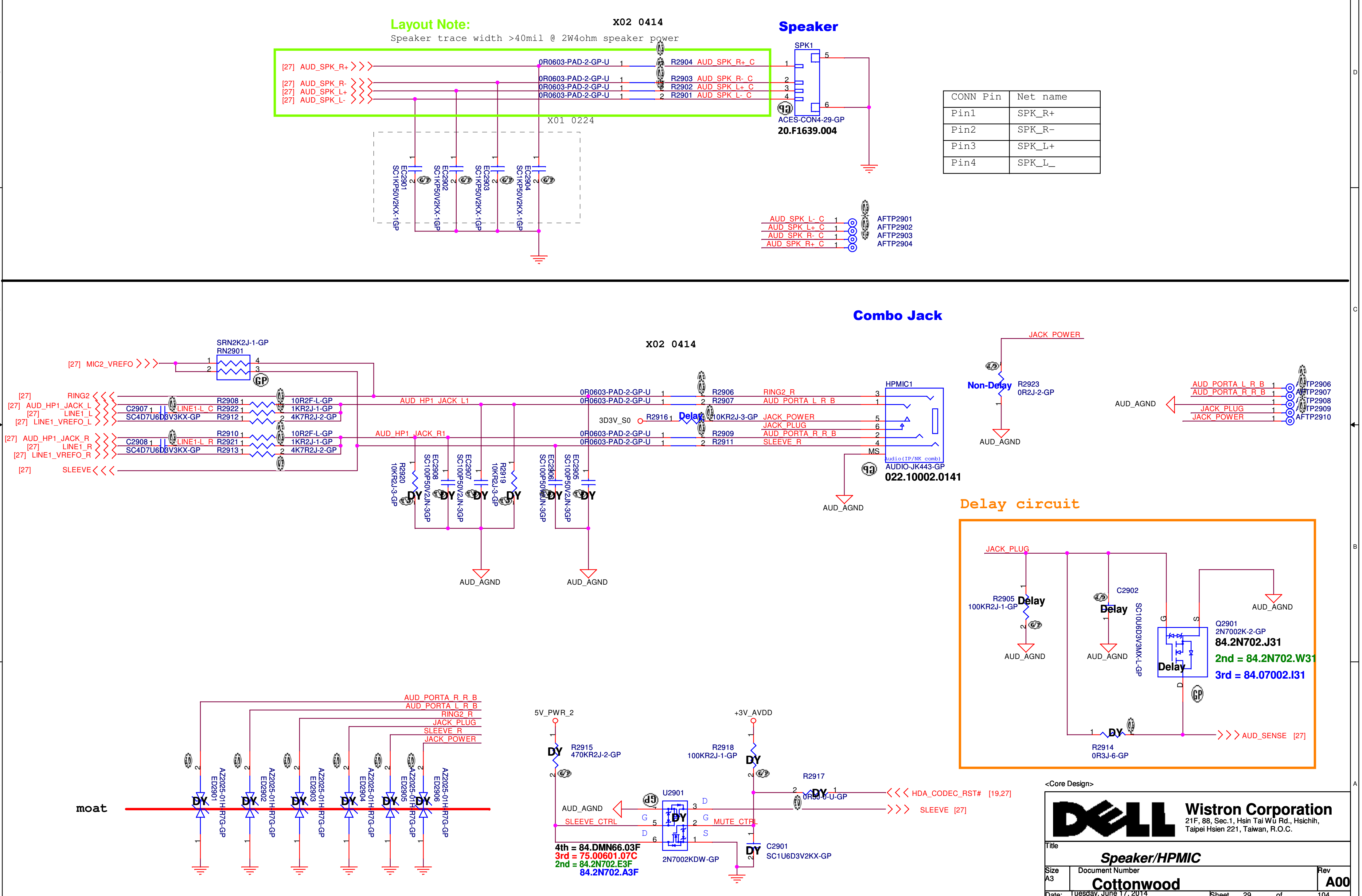
(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AUDIO AMP		
Size: A3	Document Number: Cottonwood	Rev: A00
Date: Tuesday, June 17, 2014	Sheet 28 of 107	

SSID = AUDIO



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC

Size: A3 | Document Number: Cottonwood | Rev: A00

Date: Tuesday, June 17, 2014 | Sheet 29 of 104

5 4 3 2 1

D

C

(Blanking)

B

A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN RTL8111/RTL8106	
Size A2	Document Number Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 30 of 104	

5 4 3 2 1

SSID = LOM

(Blanking)

<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: XFOM&RJ45		
Size: A3	Document Number: Cottonwood	Rev: A00
Date: Tuesday, June 17, 2014	Sheet 31 of 104	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)Card Reader	
Size A4	Document Number Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 32 of 104	

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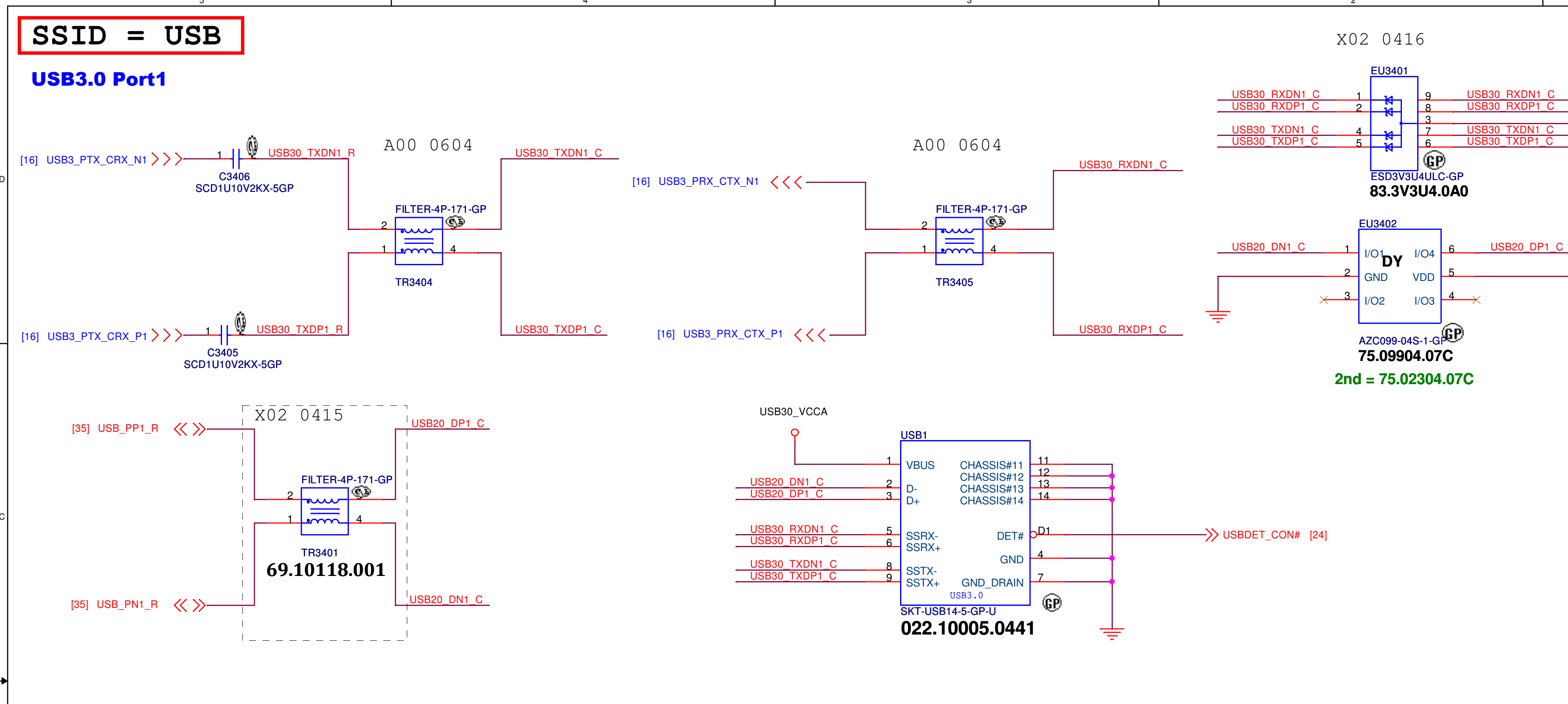
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)	
Size: A3	Document Number: Cottonwood	Rev: A00
Date: Tuesday, June 17, 2014	Sheet 33 of 104	

SSID = USB

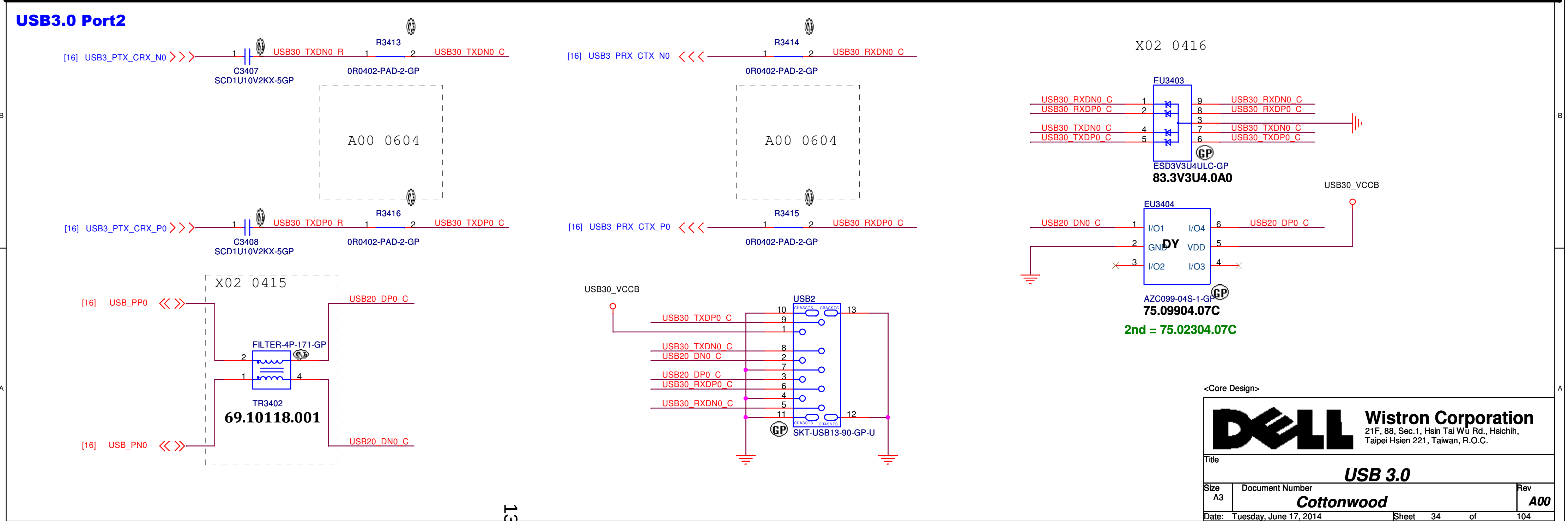
USB3.0 Port1



USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

USB3.0 Port2

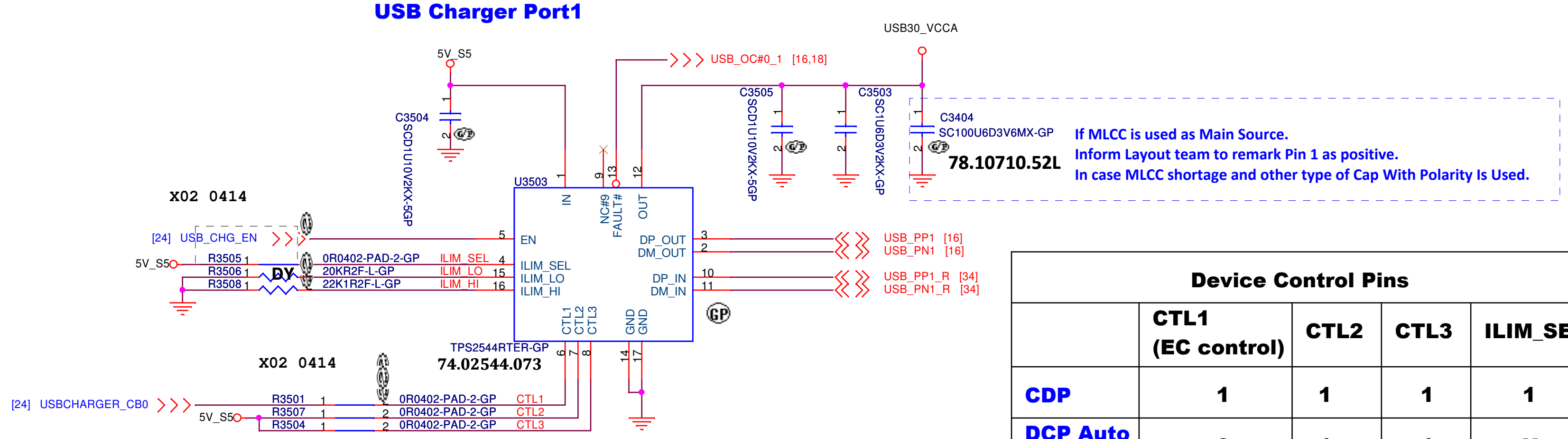


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

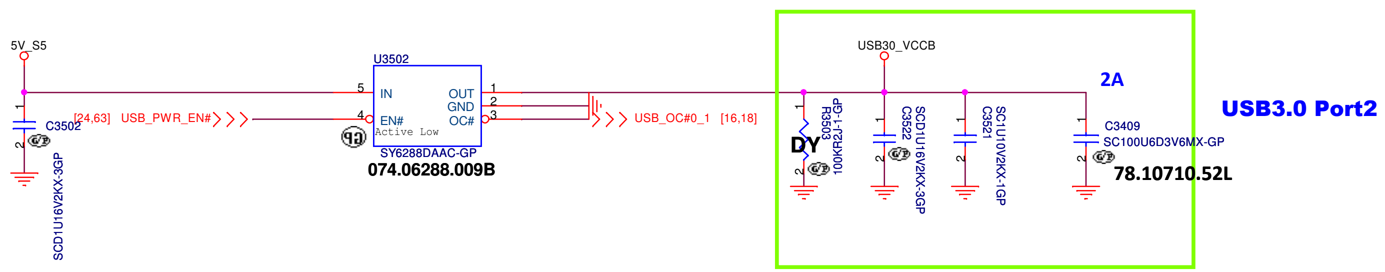
Title	USB 3.0	
Size: A3	Document Number: Cottonwood	Rev: A00
Date: Tuesday, June 17, 2014	Sheet 34 of 104	

USB Charger Port1



Device Control Pins				
	CTL1 (EC control)	**CTL2**	**CTL3**	**ILIM_SEL**
CDP	**1**	**1**	**1**	**1**
DCP Auto	**0**	**1**	**1**	**X**

Layout Note: Close CON1



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https://t.me/biosarchive

<Core Design>

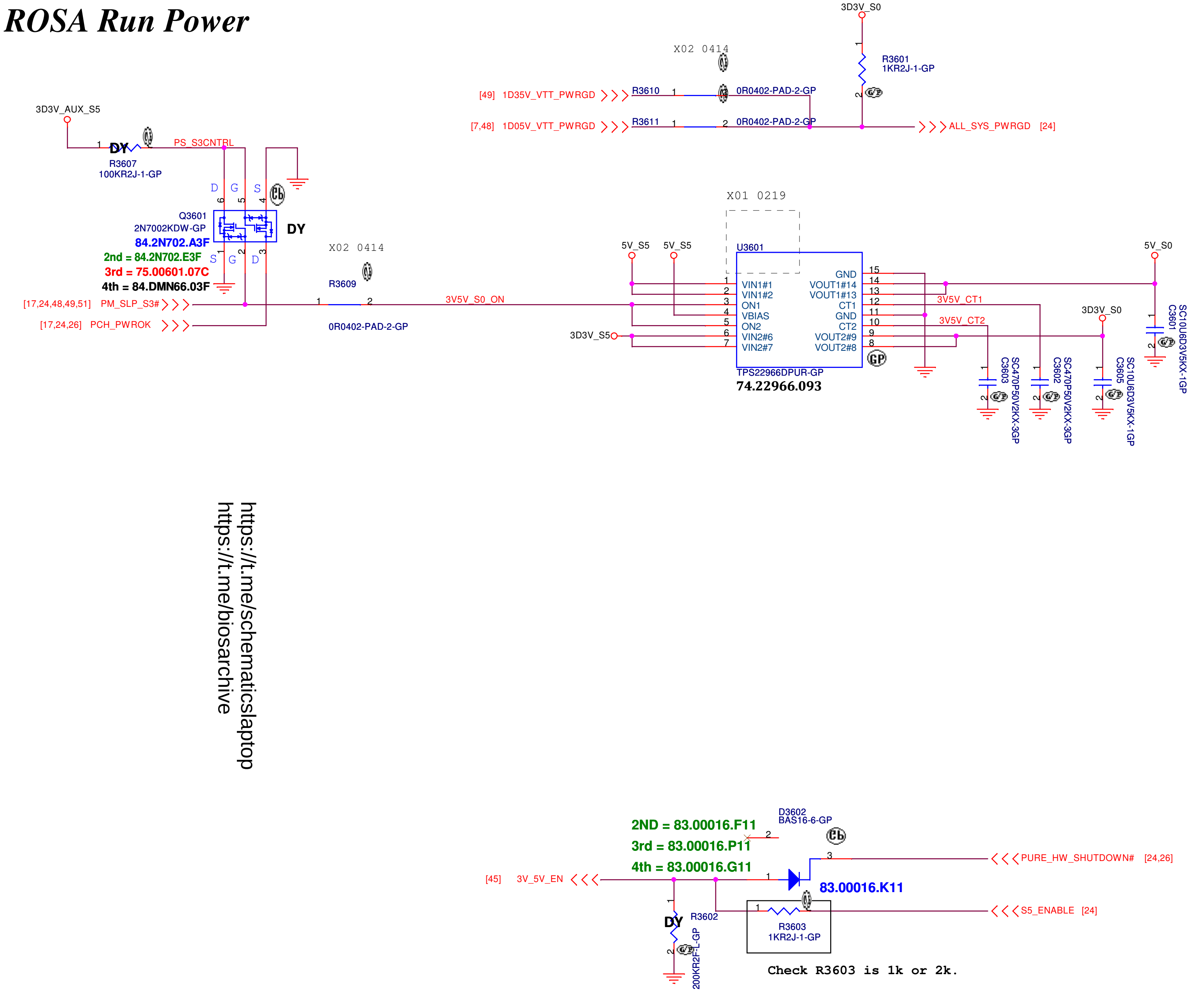
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB Power SW	
Size	Document Number: Cottonwood	Rev: A00
Date: Tuesday, June 17, 2014	Sheet 35 of 104	

SSID = Reset.Suspend

ROSA Run Power

Power Good



Check R3603 is 1k or 2k.

5V_S0

5V_S0 Comsumption
Peak current 5A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

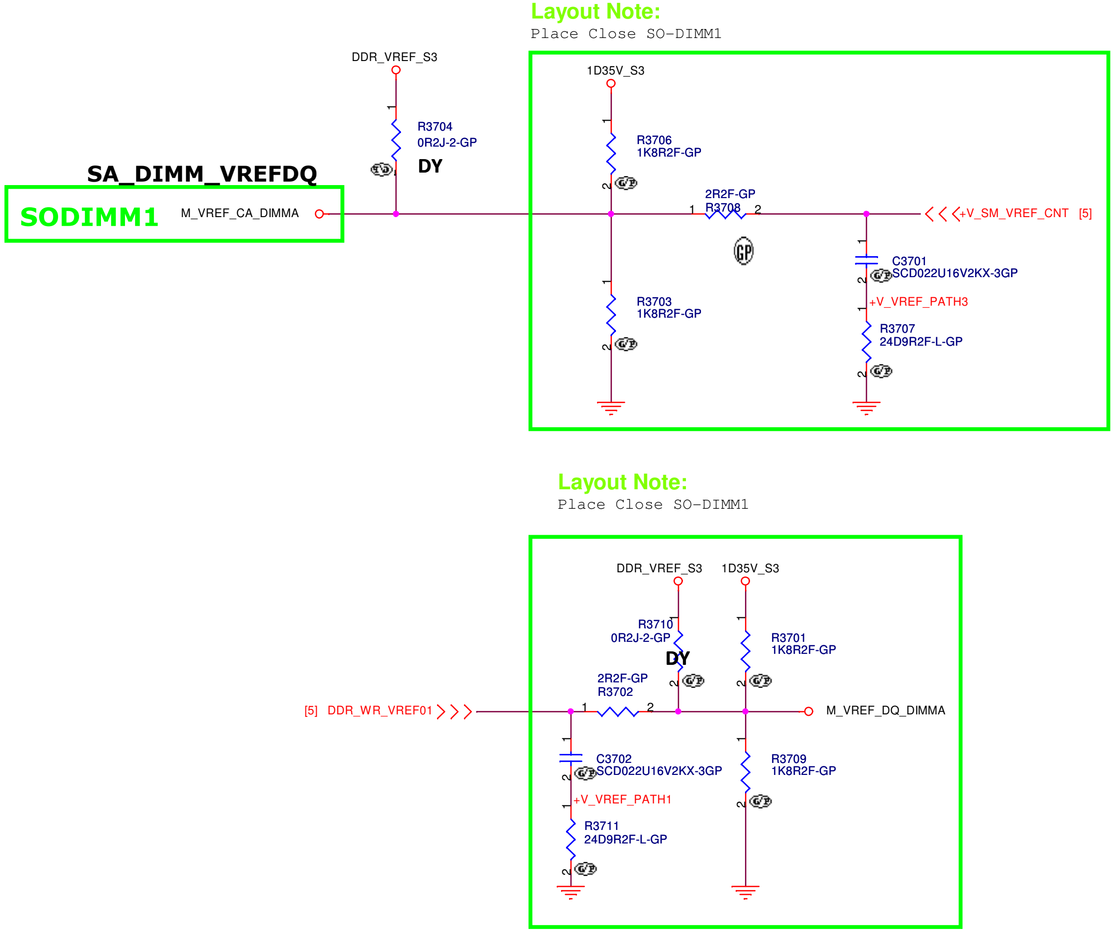
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size: A3 | Document Number: Cottonwood | Rev: A00

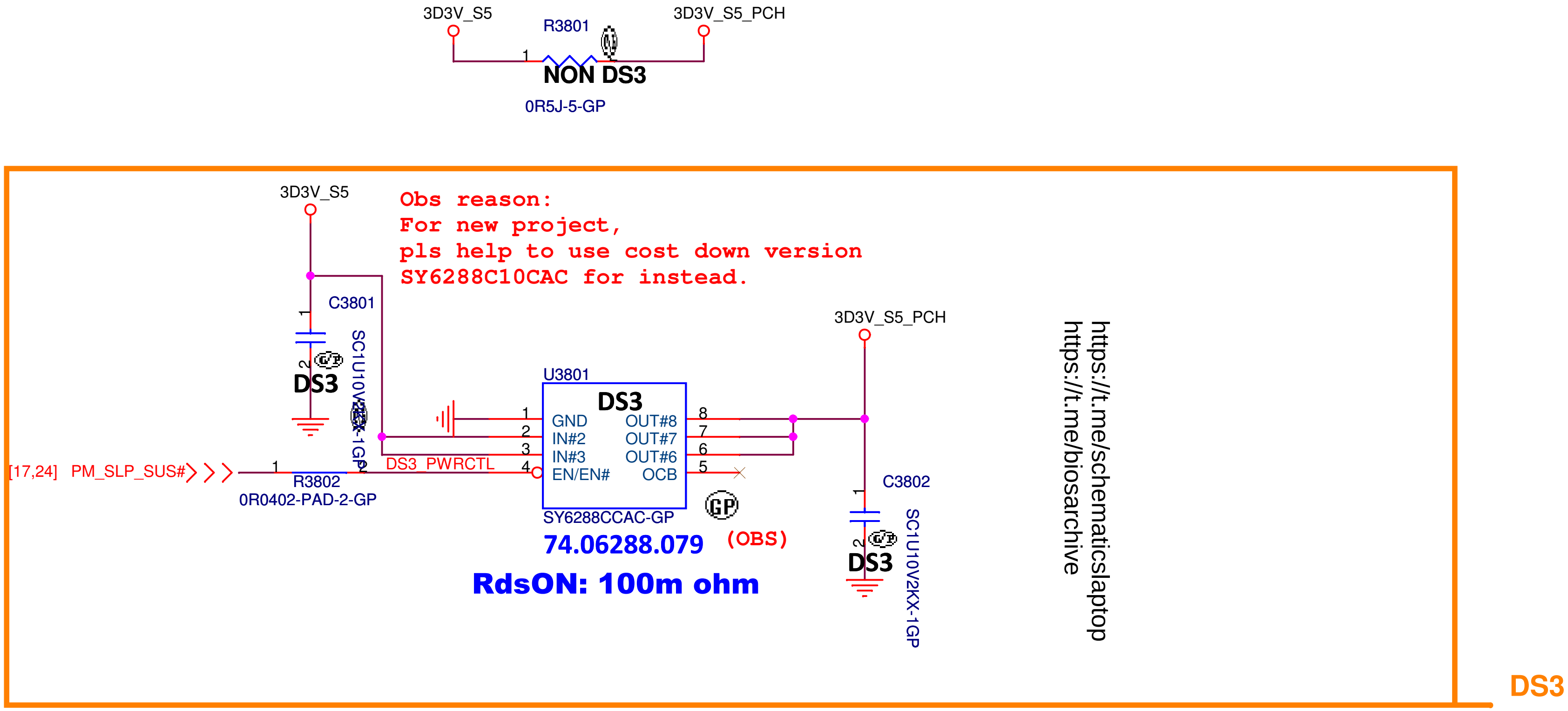
SSID = Reset.Suspend



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	S3 Reduction Circuit	
Size A3	Document Number Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 37 of 104	



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**DSW**	
Size A4	Document Number **Cottonwood**	Rev **A00**
Date: Tuesday, June 17, 2014	Sheet 38 of 104	

5 4 3 2 1

D C B A

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved) 1D05_M	
Size A4	Document Number Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 39 of 104	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Reserved**	
Size A4	Document Number **Cottonwood**	Rev **A00**
Date: Tuesday, June 17, 2014	Sheet 40 of 104	

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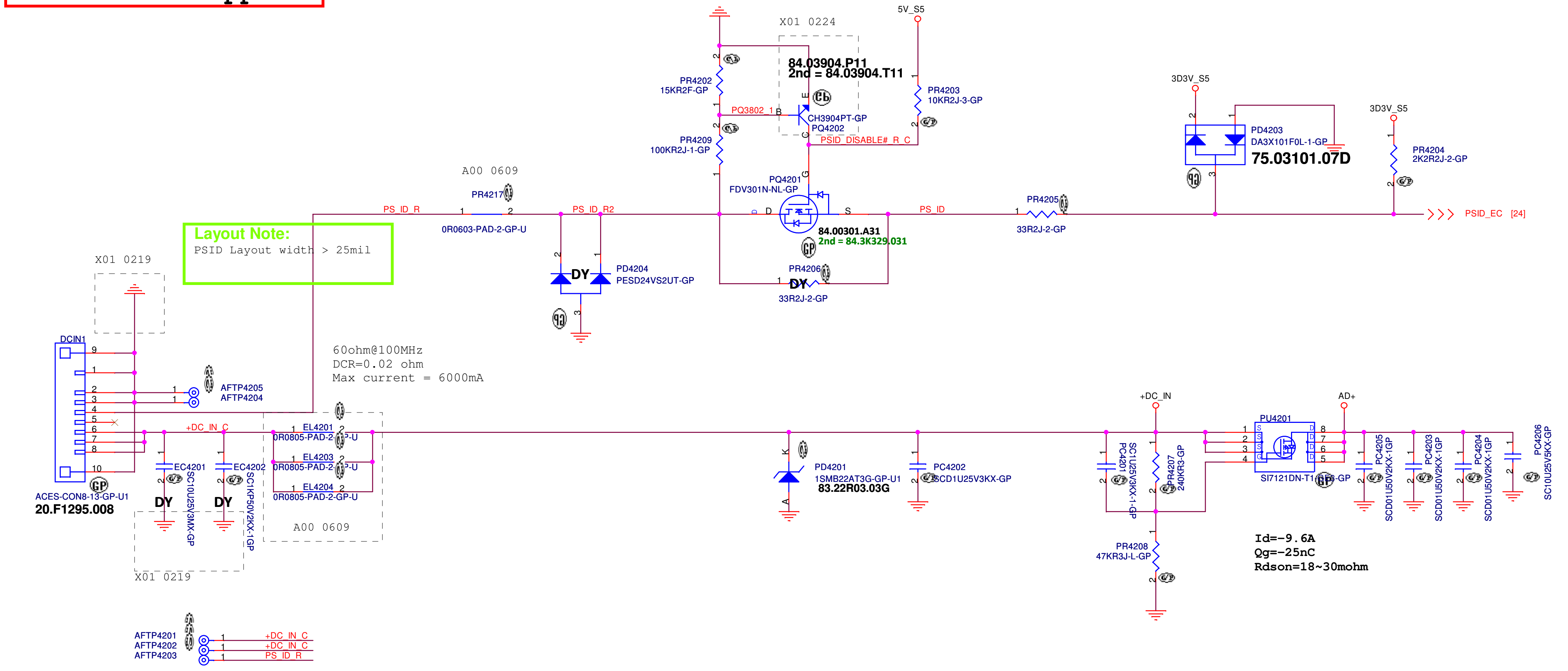
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size A4	Document Number Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 41 of 104	

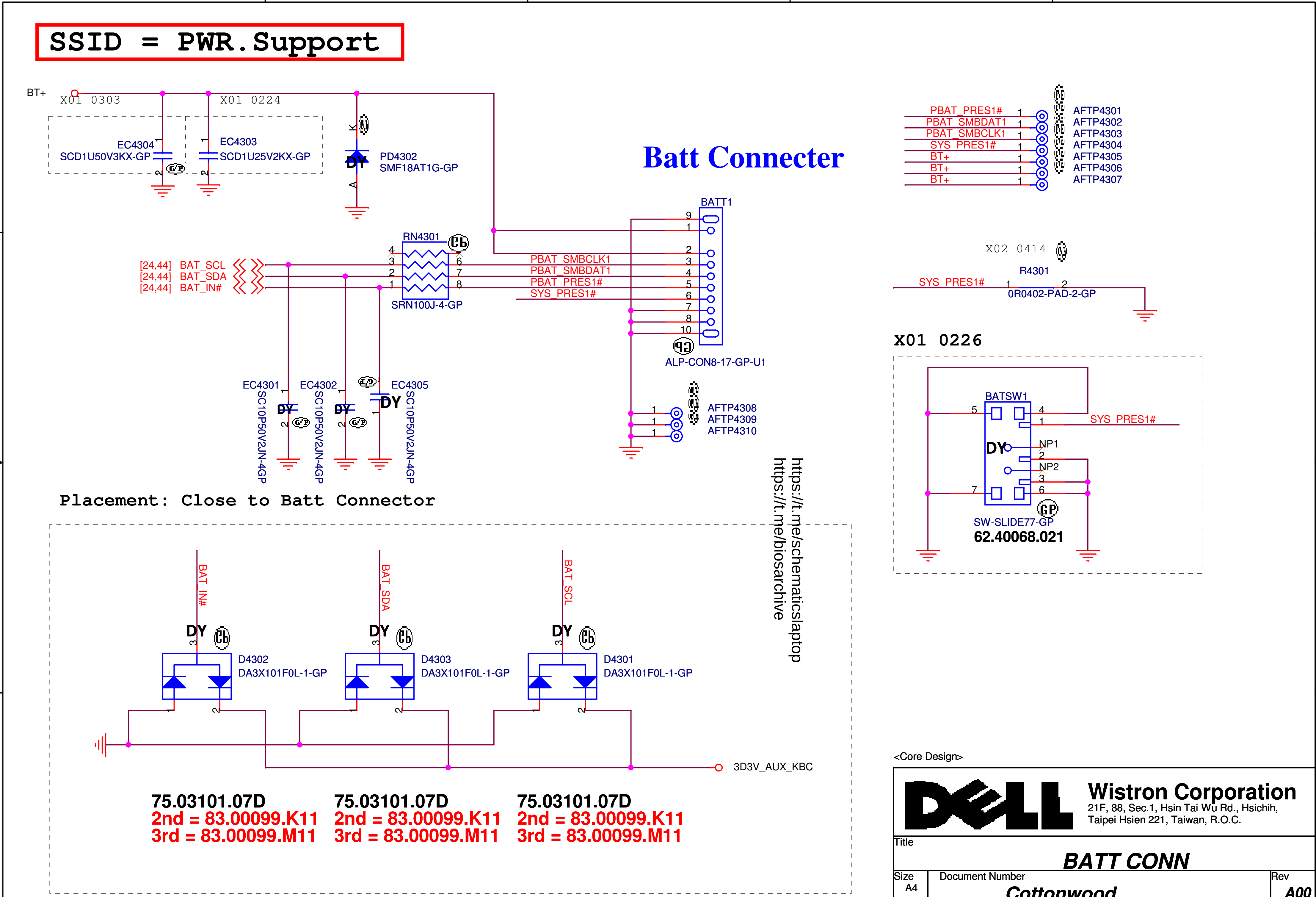
SSID = PWR.Support



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN	
Size A3	Document Number: Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 42 of 104	

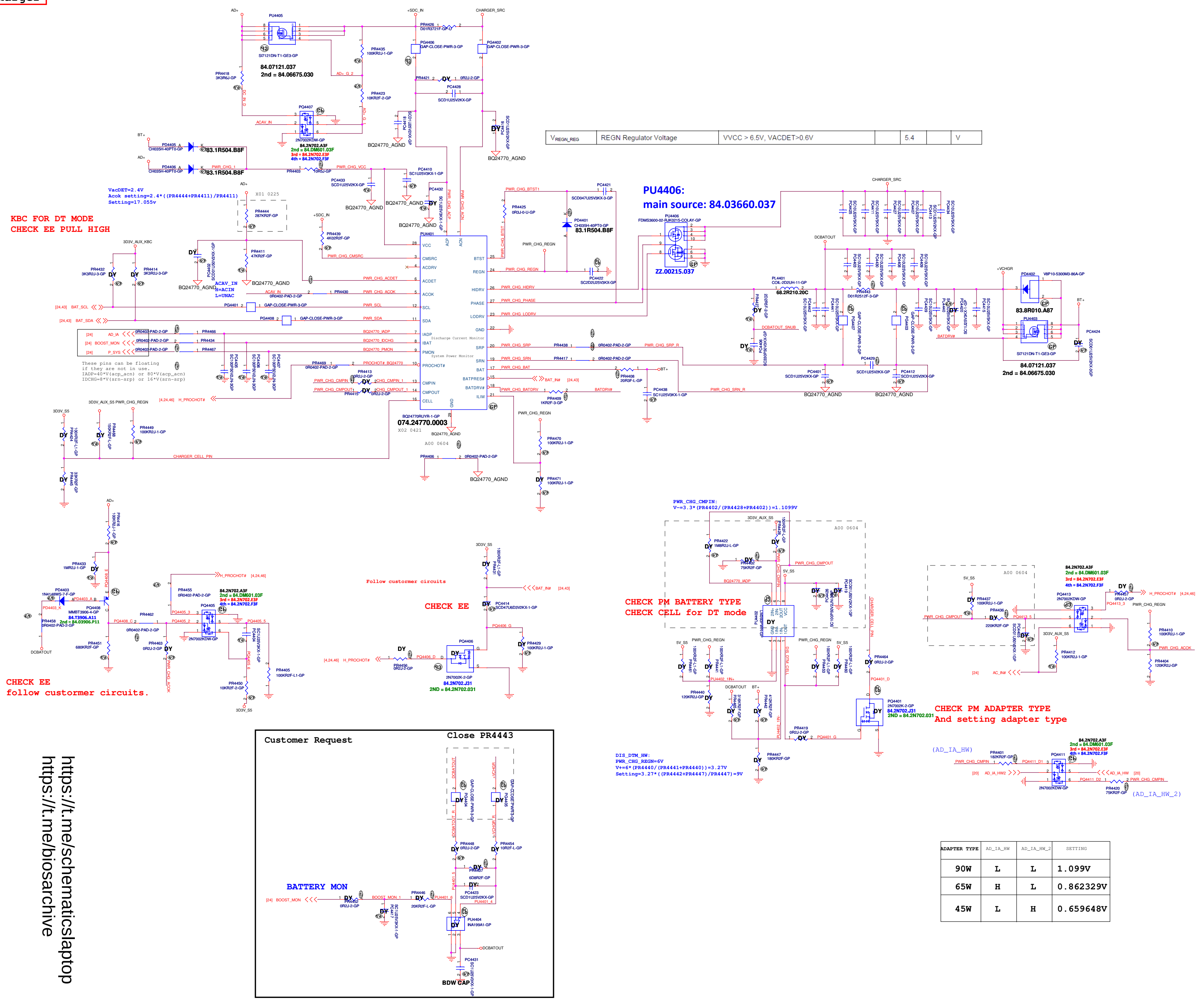


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT CONN	
Size A4	Document Number Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 43 of 104	

SSID = Charger



V_{REGN_REG}	REGN Regulator Voltage	VVCC > 6.5V, VACDET>0.6V		5.4		V

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

<Core Design>

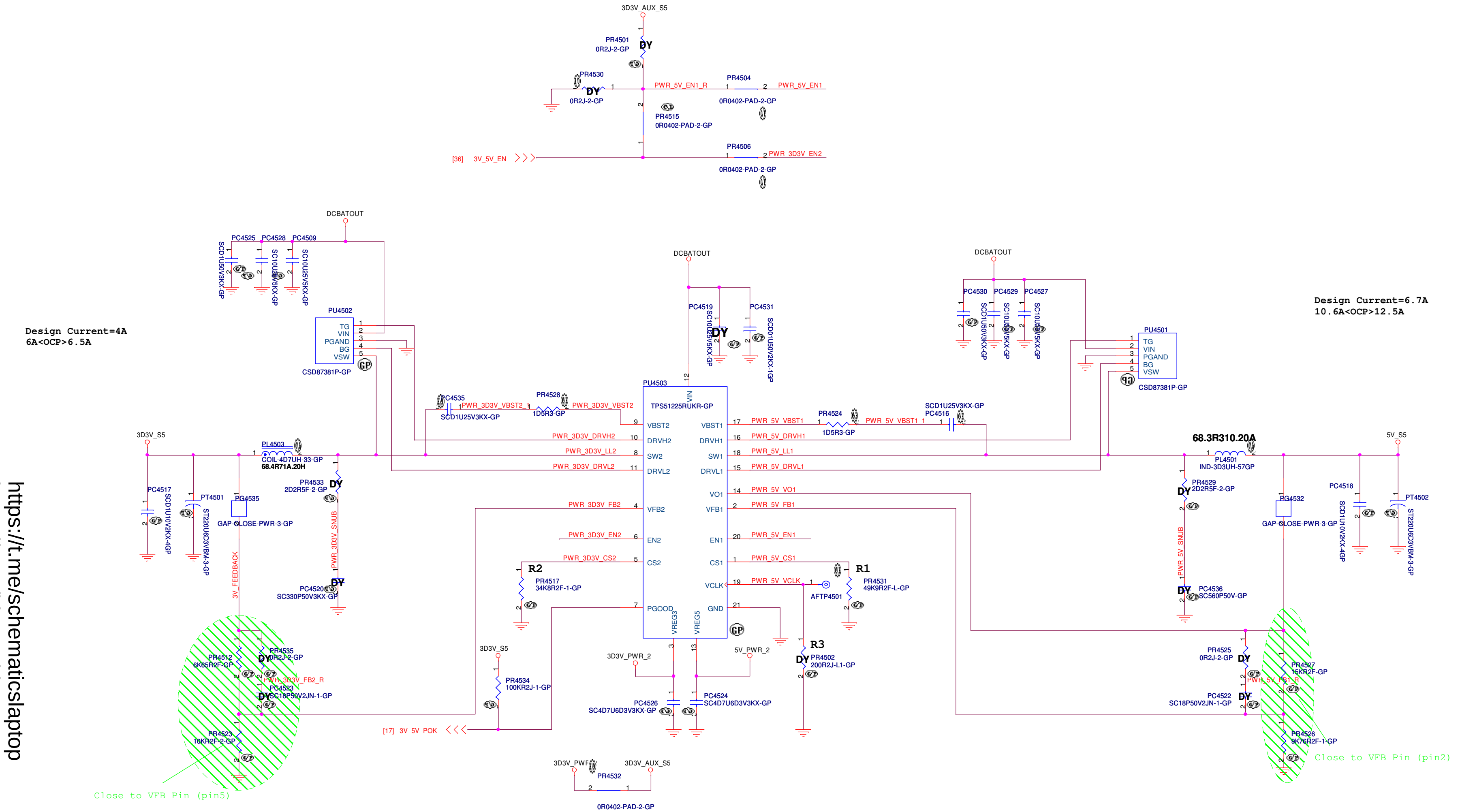
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 044P_CHARGER(BQ24770)

Size: A1 Document Number Rev: A00

Date: Tuesday, June 17, 2014 Sheet 44 of 102

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 4.7UH PCMB063T-4R7MS Cyntec 28mohm/33mohm Isat =6.5Arms 68.4R71A.20H
O/P capCHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
R1	100K	20K
R2	64.9K	13K
R3	DY	200

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

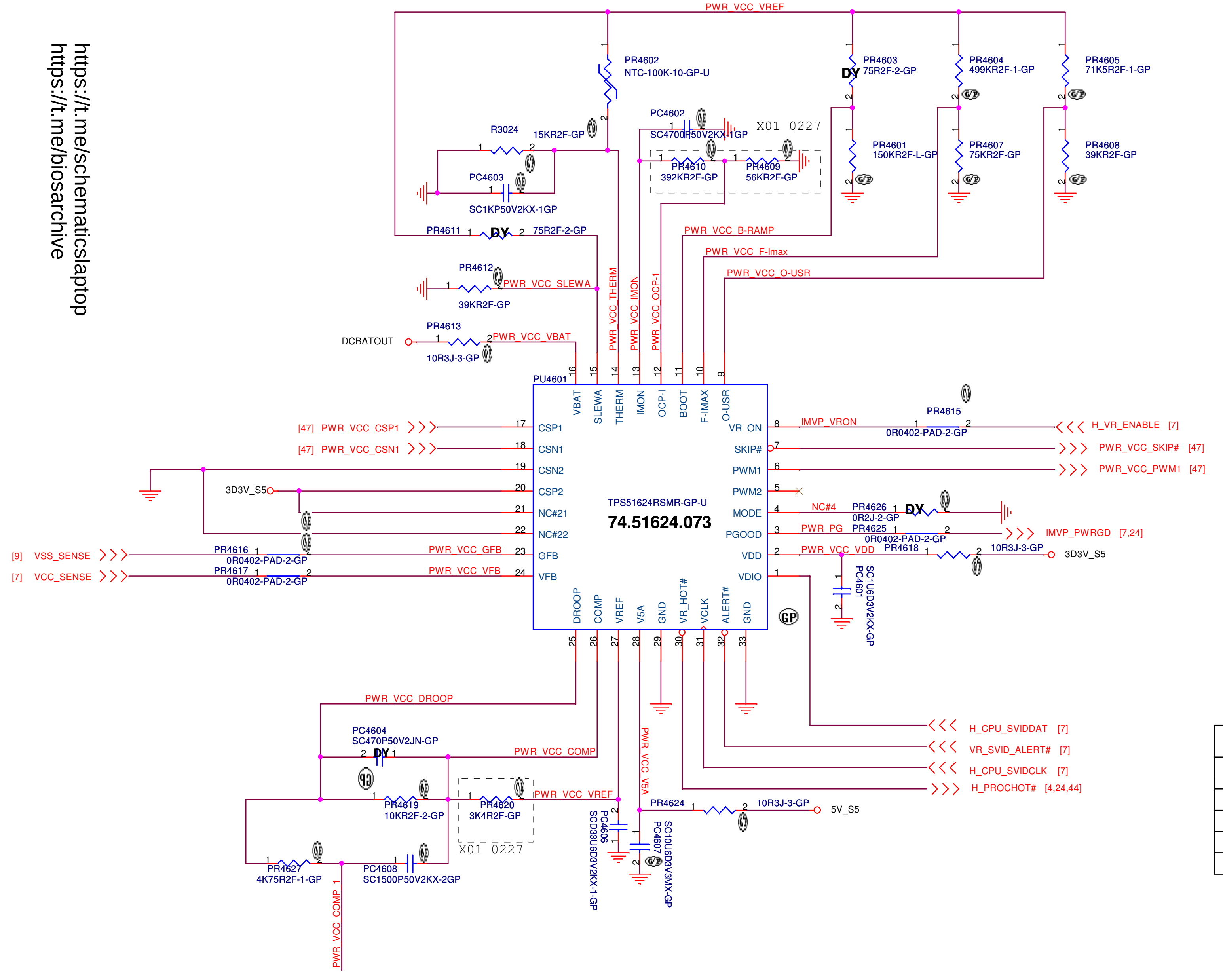
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

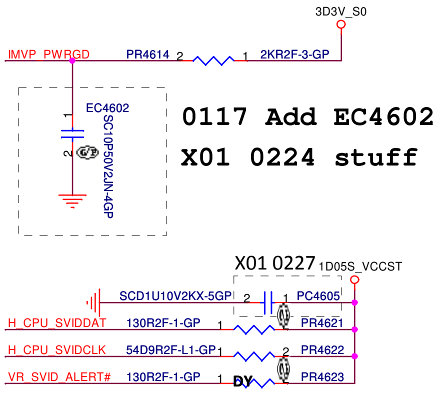
Title: *TPS51225_5V/3D3V*

Size: A2 | Document Number: Cottonwood | Rev: A00

Date: Tuesday, June 17, 2014 | Sheet 45 of 102

SSID = CPU.Regulator





		28W	15W
Fsw	PR4604	392K	1M
Fsw	PR4607	75K	150K
OCP	PR4609	150k	75K
IMON	PR4610	680K	422K
Load line	PR4620	2.8K	3K

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

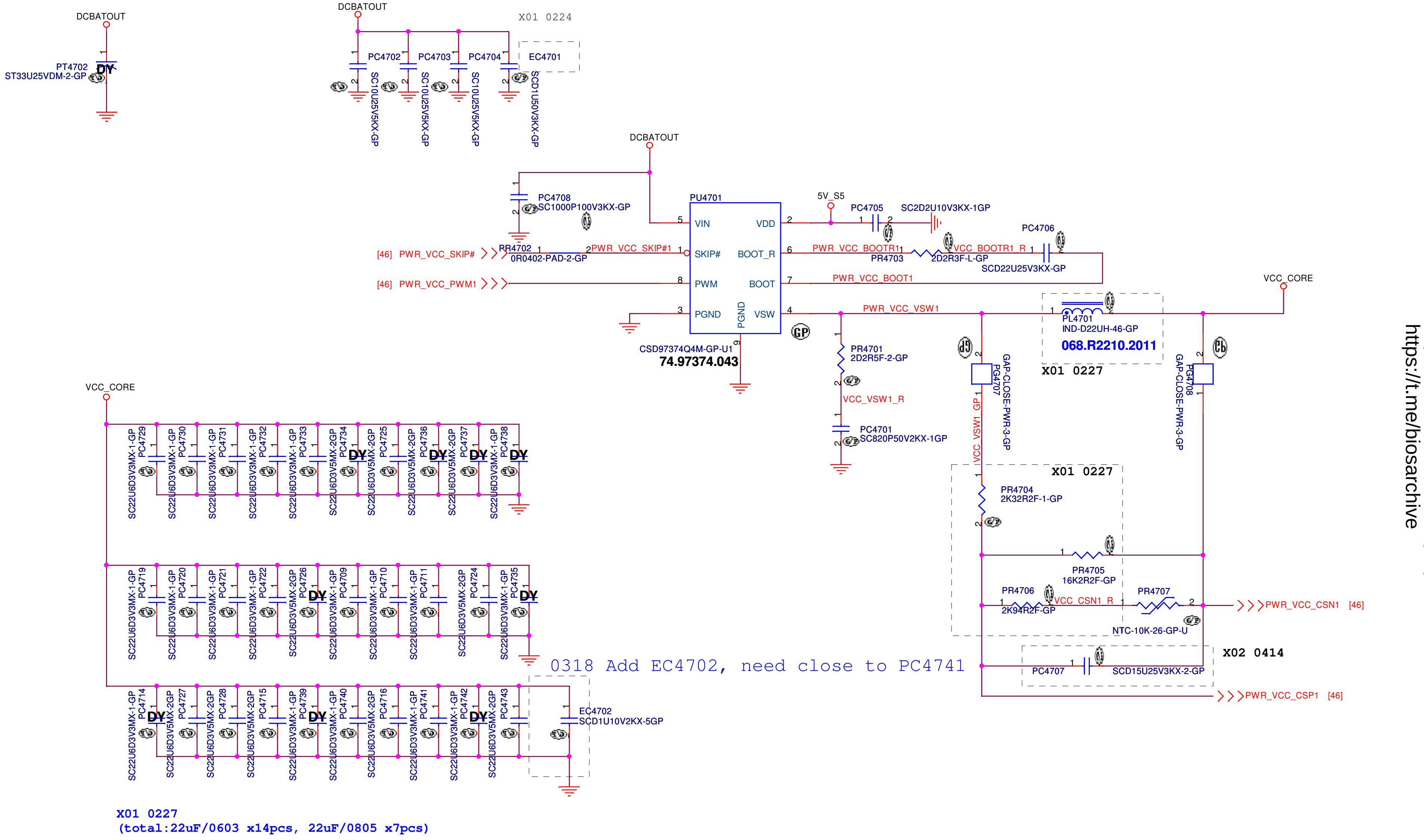
Title: 046P_TPS51624_CPUCORE(1/2)

Size: A3 | Document Number: Cottonwood | Rev: A00

Date: Tuesday, June 17, 2014 | Sheet 46 of 102

SSID = CPU.Regulator

For acoustic noice



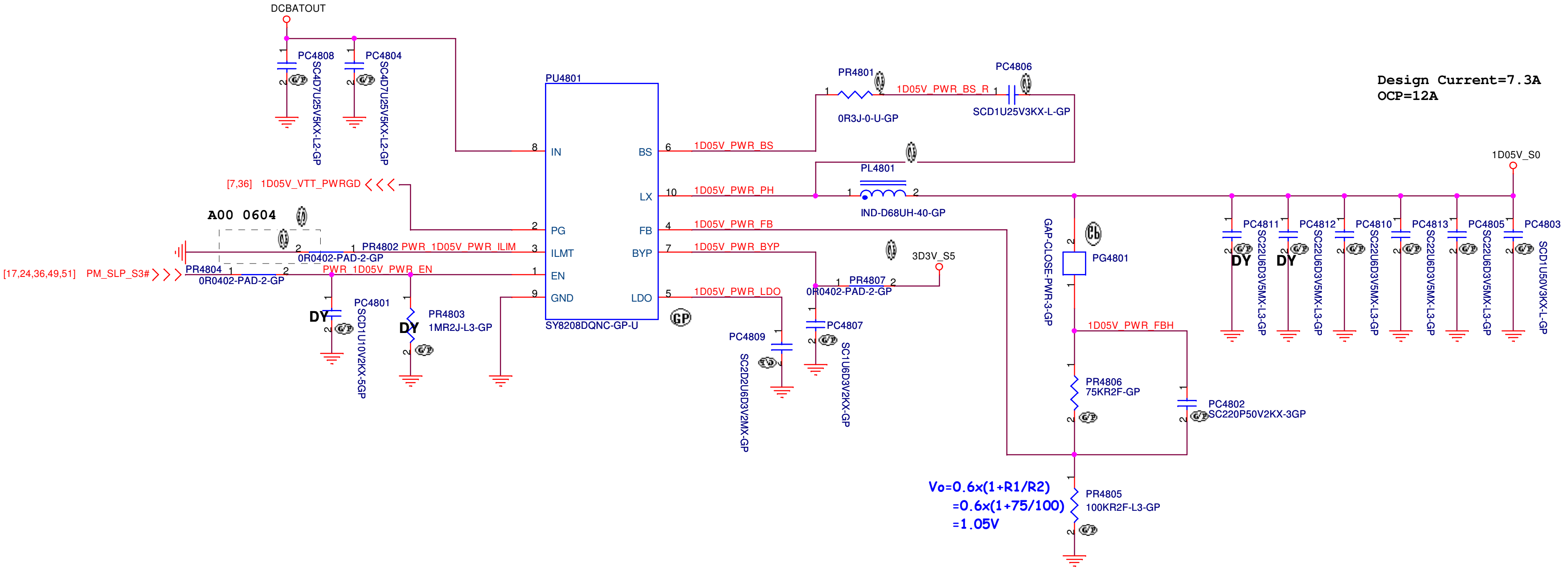
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	047P_TPS51624_CPUCORE(2/2)
Size	A3
Document Number	Cottonwood
Rev	A00
Date:	Tuesday, June 17, 2014
Sheet	47 of 102

SSID = PWR.Plane.Regulator_1p05v

SY8208D for 1D05V



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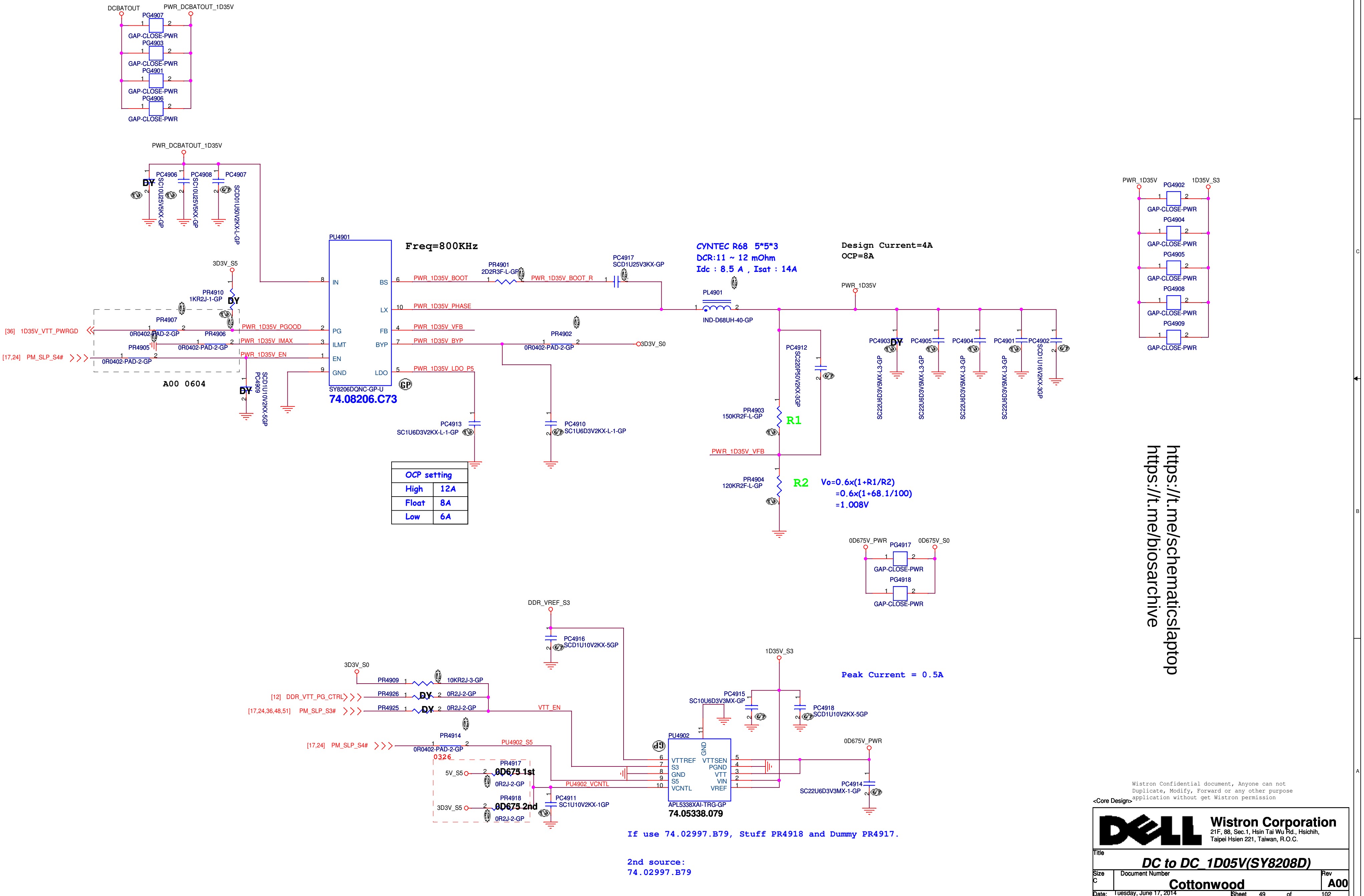
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	SY8208DQNC_1D05V	
Size A3	Document Number Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 48 of 104	

SY8206D for 1D35V



OCP setting	
High	12A
Float	8A
Low	6A

If use 74.02997.B79, Stuff PR4918 and Dummy PR4917.

2nd source:
74.02997.B79

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC_1D05V(SY8208D)

Size: C | Document Number: Cottonwood | Rev: A00

Date: Tuesday, June 17, 2014 | Sheet 49 of 102

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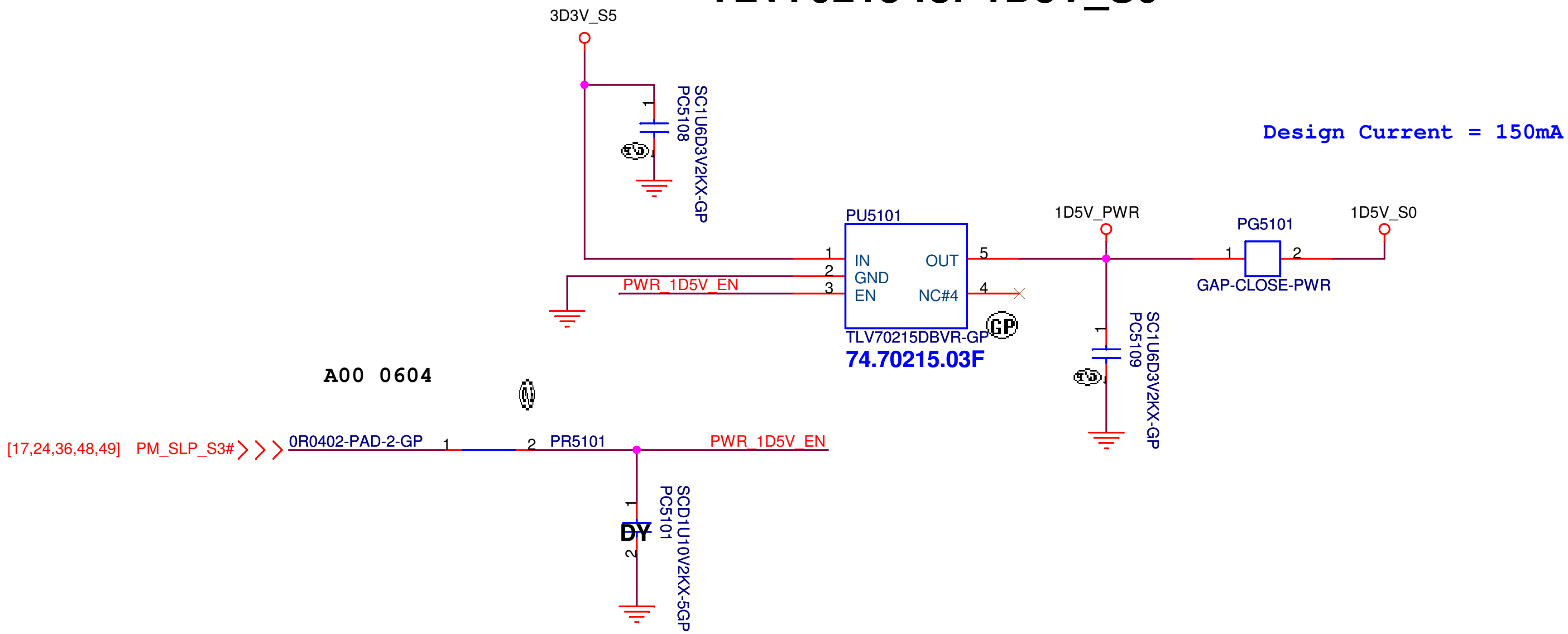
<Core Design>

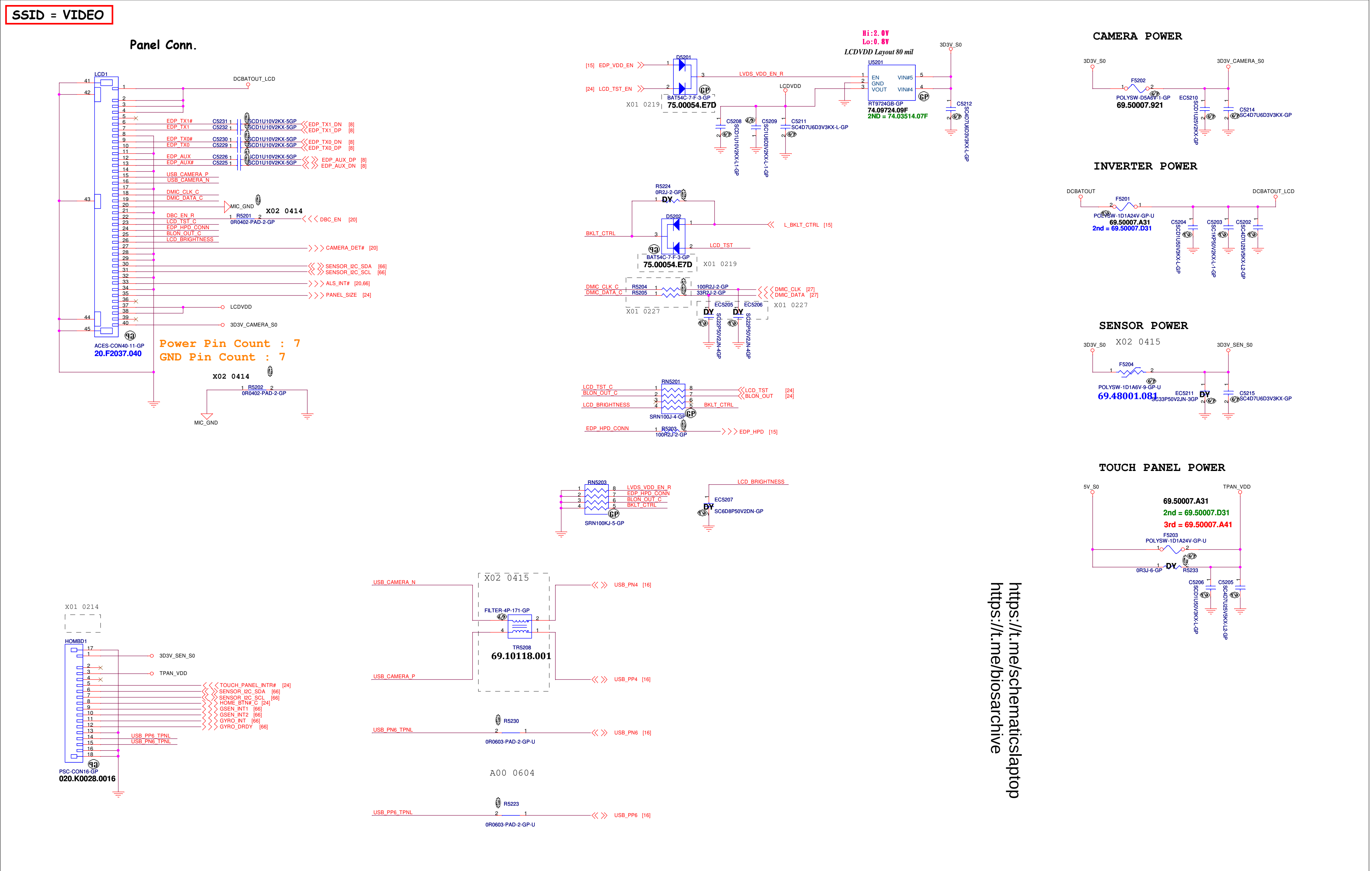
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved		
Size: A3	Document Number: Cottonwood	Rev: A00
Date: Tuesday, June 17, 2014	Sheet 50 of 104	

SSID = PWR.Plane.Regulator_1p5v

TLV70215 for 1D5V_S0





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD Connector
Size	A2
Document Number	Cottonwood
Rev	A00
Date:	Tuesday, June 17, 2014
Sheet	52 of 102

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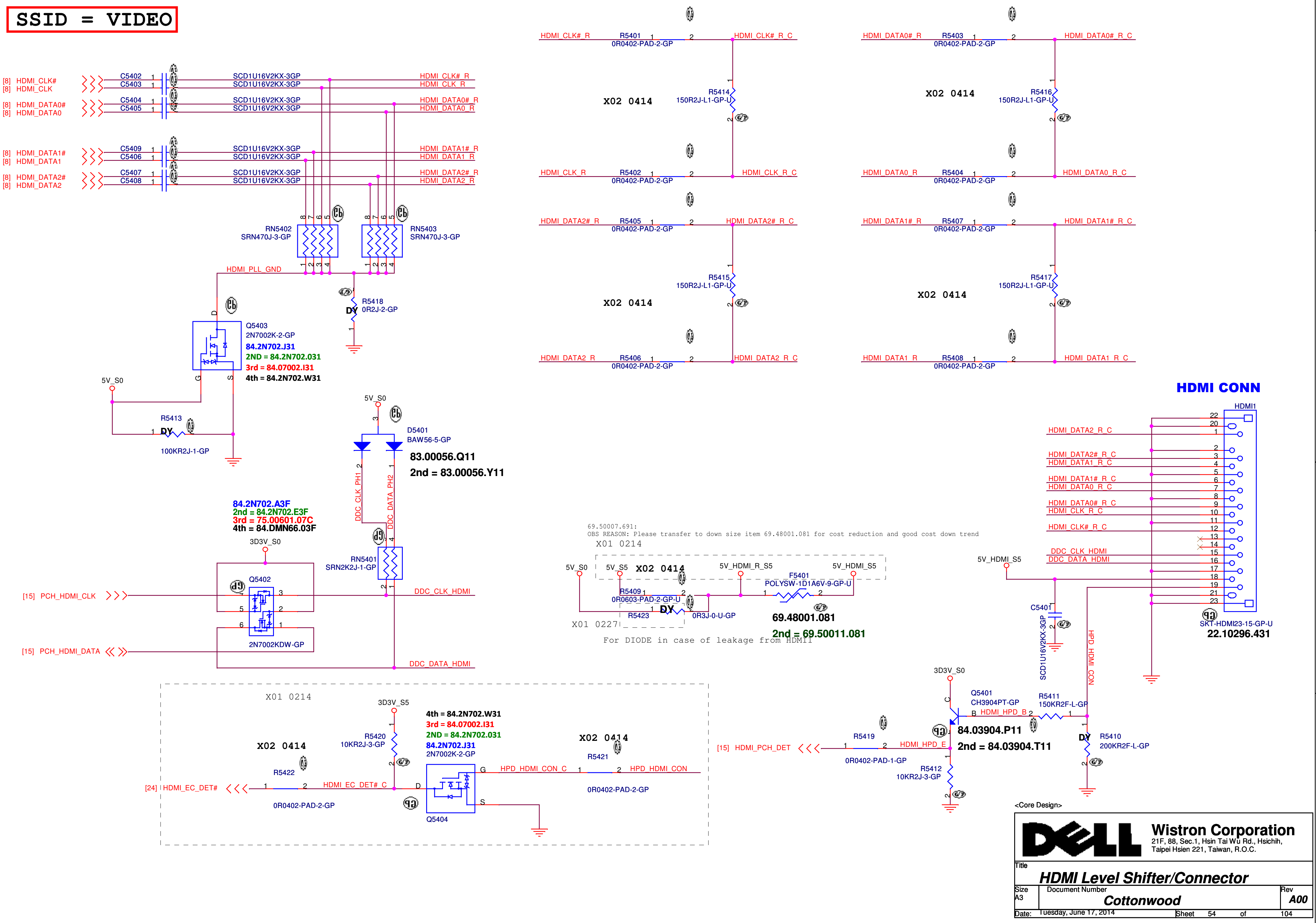
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)	
Size A3	Document Number Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 53 of 104	



SSID = VIDEO
[8] HDMI_CLK#
[8] HDMI_CLK
[8] HDMI_DATA0#
[8] HDMI_DATA0
[8] HDMI_DATA1#
[8] HDMI_DATA1
[8] HDMI_DATA2#
[8] HDMI_DATA2
C5402 C5403 C5404 C5405 C5409 C5406 C5407 C5408
SCD1U16V2KX-3GP
HDMI_CLK#_R
HDMI_CLK_R
HDMI_DATA0#_R
HDMI_DATA0_R
HDMI_DATA1#_R
HDMI_DATA1_R
HDMI_DATA2#_R
HDMI_DATA2_R
RN5402
SRN470J-3-GP
RN5403
SRN470J-3-GP
HDMI_PLL_GND
R5418
0R2J-2-GP
DY
Q5403
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31
5V_S0
R5413
DY
100KR2J-1-GP
5V_S0
D5401
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.Y11
DDC_CLK_PH1
DDC_DATA_PH2
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F
3D3V_S0
Q5402
2N7002KDW-GP
RN5401
SRN2K2J-1-GP
[15] PCH_HDMI_CLK
[15] PCH_HDMI_DATA
DDC_CLK_HDMI
DDC_DATA_HDMI
HDMI_CLK#_R R5401 0R0402-PAD-2-GP HDMI_CLK#_R_C
R5414 150R2J-L1-GP-U
X02 0414
HDMI_CLK_R R5402 0R0402-PAD-2-GP HDMI_CLK_R_C
HDMI_DATA2#_R R5405 0R0402-PAD-2-GP HDMI_DATA2#_R_C
R5415 150R2J-L1-GP-U
X02 0414
HDMI_DATA2_R R5406 0R0402-PAD-2-GP HDMI_DATA2_R_C
HDMI_DATA0#_R R5403 0R0402-PAD-2-GP HDMI_DATA0#_R_C
R5416 150R2J-L1-GP-U
X02 0414
HDMI_DATA0_R R5404 0R0402-PAD-2-GP HDMI_DATA0_R_C
HDMI_DATA1#_R R5407 0R0402-PAD-2-GP HDMI_DATA1#_R_C
R5417 150R2J-L1-GP-U
X02 0414
HDMI_DATA1_R R5408 0R0402-PAD-2-GP HDMI_DATA1_R_C
HDMI CONN
HDMI1
HDMI_DATA2_R_C
HDMI_DATA2#_R_C
HDMI_DATA1_R_C
HDMI_DATA1#_R_C
HDMI_DATA0_R_C
HDMI_DATA0#_R_C
HDMI_CLK_R_C
HDMI_CLK#_R_C
DDC_CLK_HDMI
DDC_DATA_HDMI
5V_HDMI_S5
SKT-HDMI23-15-GP-U
22.10296.431
69.50007.691:
OBS REASON: Please transfer to down size item 69.48001.081 for cost reduction and good cost down trend
X01 0214
5V_S0
5V_S5
X02 0414
5V_HDMI_R_S5
5V_HDMI_S5
F5401
POLYSW-1D1A6V-9-GP-U
R5409
0R0603-PAD-2-GP-U
R5423
DY
0R3J-0-U-GP
69.48001.081
2nd = 69.50011.081
X01 0227
For DIODE in case of leakage from HDMI
C5401
SCD1U16V2KX-3GP
HPD_HDMI_CON
3D3V_S0
Q5401
CH3904PT-GP
HDMI_HPD_B
R5411
150KR2F-L-GP
84.03904.P11
2nd = 84.03904.T11
[15] HDMI_PCH_DET
R5419
0R0402-PAD-1-GP
HDMI_HPD_E
R5412
10KR2J-3-GP
DY
R5410
200KR2F-L-GP
X01 0214
3D3V_S5
R5420
10KR2J-3-GP
4th = 84.2N702.W31
3rd = 84.07002.I31
2ND = 84.2N702.031
84.2N702.J31
2N7002K-2-GP
X02 0414
X02 0414
R5421
HPD_HDMI_CON_C
HPD_HDMI_CON
0R0402-PAD-2-GP
R5422
[24] HDMI_EC_DET#
HDMI_EC_DET#_C
0R0402-PAD-2-GP
Q5404
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Level Shifter/Connector
Size A3
Document Number
Cottonwood
Rev A00
Date: Tuesday, June 17, 2014
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)DP to VGA Converter	
Size A3	Document Number Cottonwood	Rev A00
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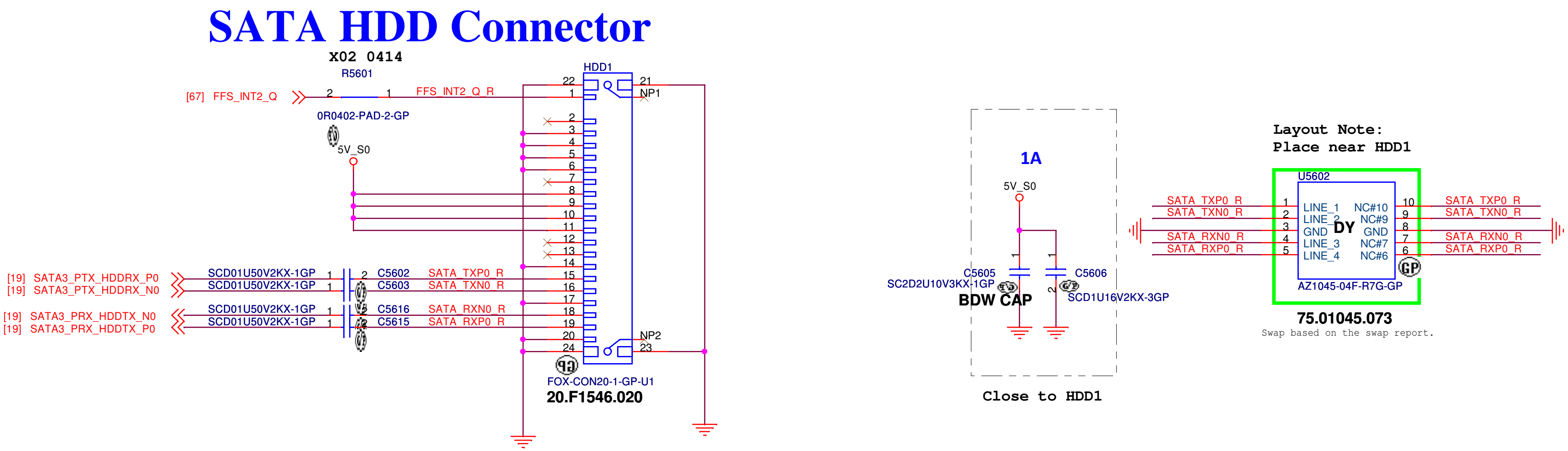
SSID = SATA



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD		
Size: A3	Document Number: Cottonwood	Rev: A00
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SSID = ESATA

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<Core Design>

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Title: WLAN (NGFF) CONN		
Size: A4	Document Number: Cottonwood	Rev: A00
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A B C D E

4

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3

2

1

<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title ***Reserved***		
Size A4	Document Number ***Cottonwood***	Rev ***A00***
Date: Tuesday, June 17, 2014	Sheet 59 of 104	

A B C D E

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SSID = User.Interface

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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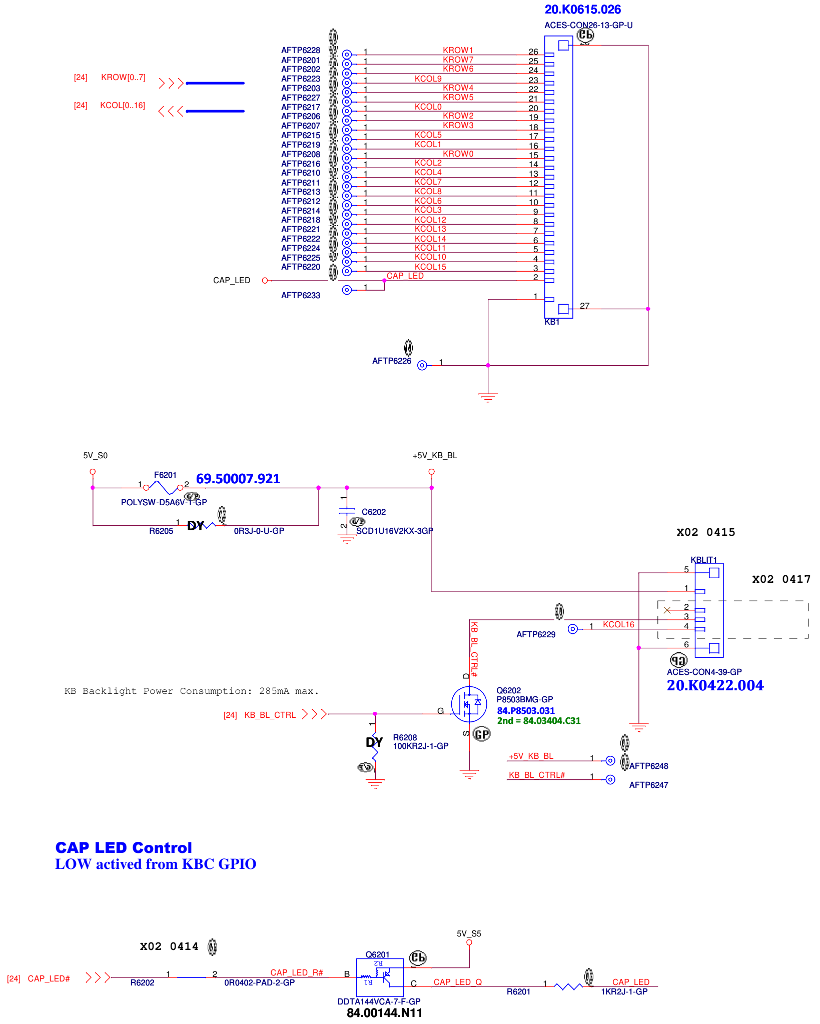
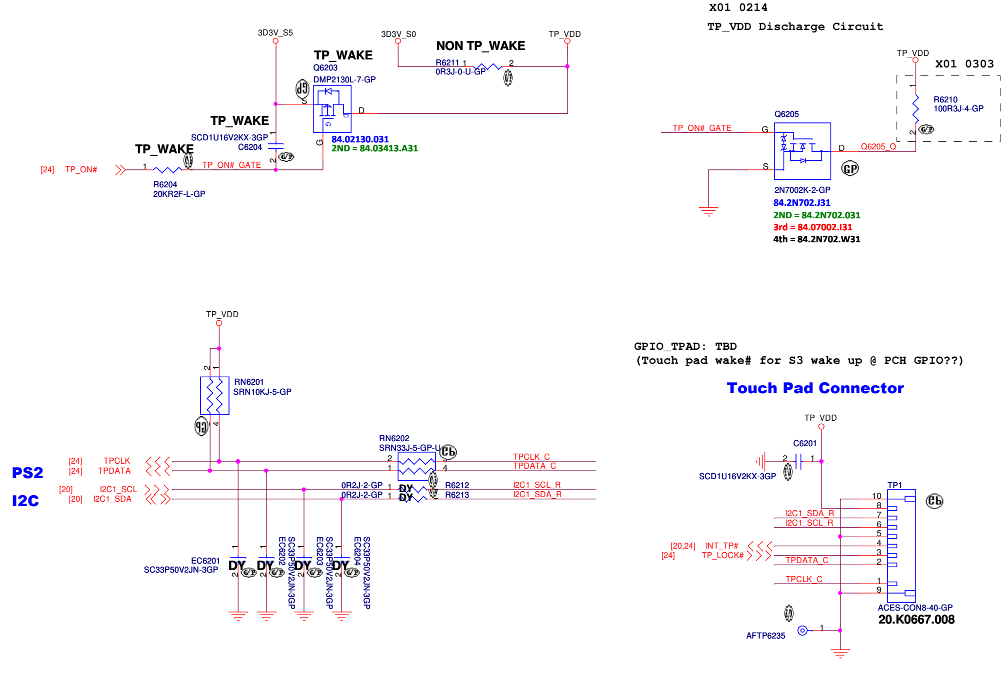
Title	LED Bard/Power Button	
Size: A4	Document Number: Cottonwood	Rev: A00
Date: Tuesday, June 17, 2014	Sheet 61 of 104	

SSID = KBC

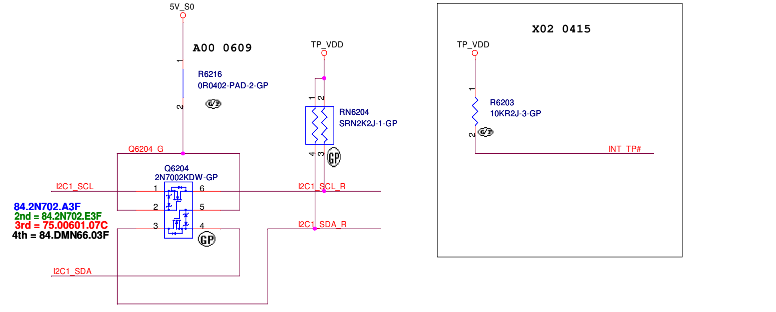
Keyboard



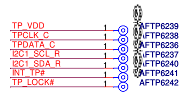
Touch.Pad



Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)



<Core Design>

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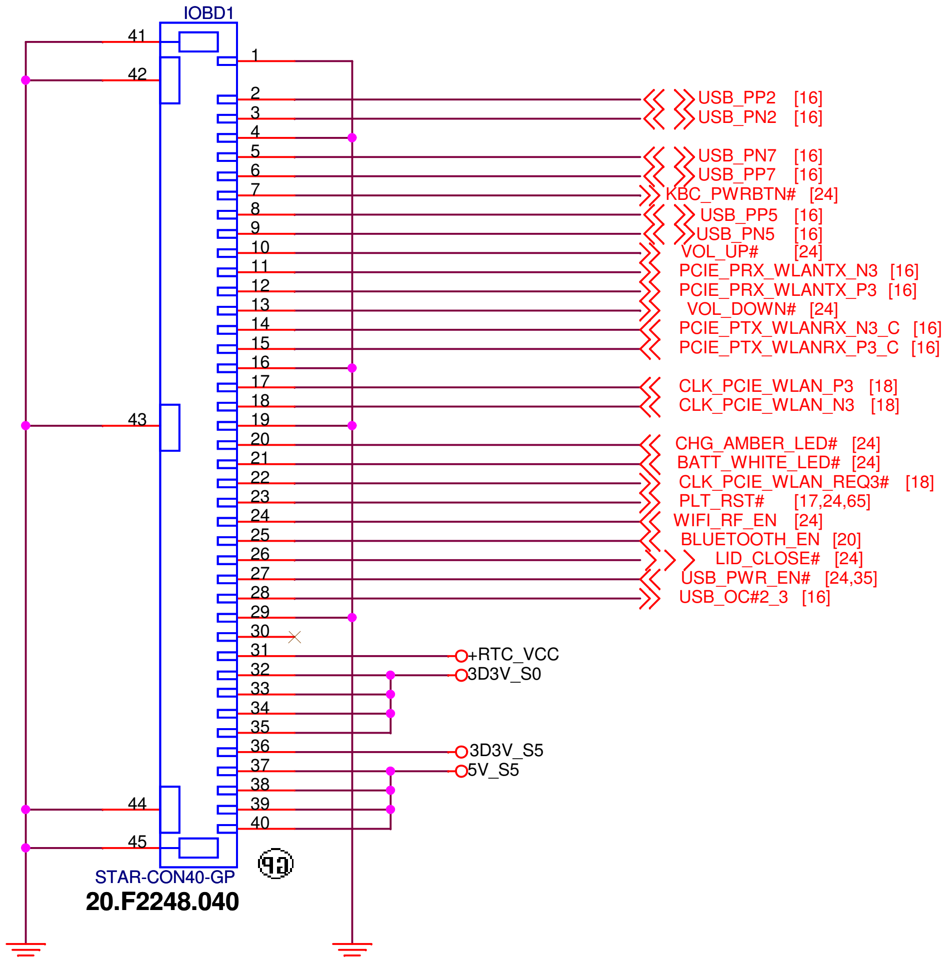
Title	Key Board/Touch Pad	
Size A2	Document Number Cottonwood	Rev A00
Date: Tuesday, June 17, 2014	Sheet 62 of 104	



Power Pin Count : 10

GND Pin Count :5

<Core Design>

Wistron Corporation

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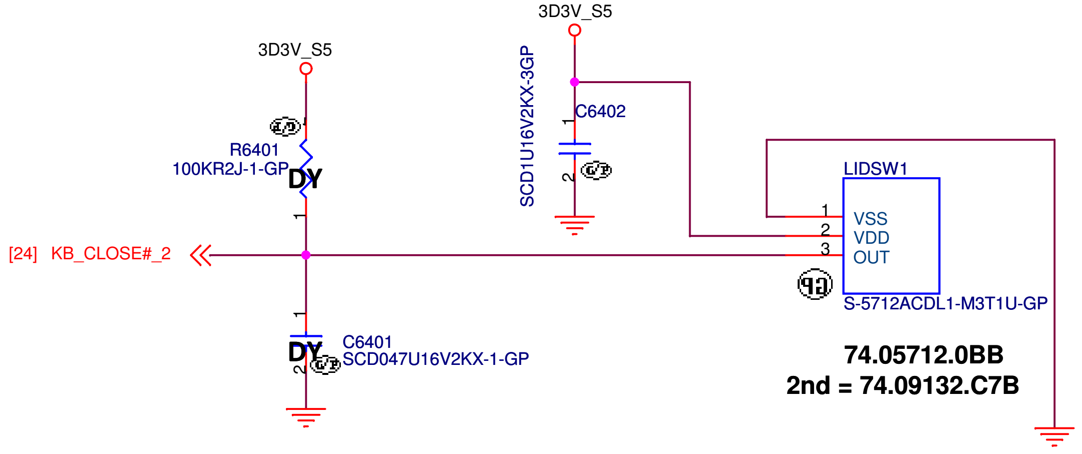
Title: IO Board Connector

Size: A4 | Document Number: Cottonwood | Rev: A00

Date: Tuesday, June 17, 2014 | Sheet 63 of 104

SSID = User.Interface



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor		
Size: A4	Document Number: Cottonwood	Rev: A00
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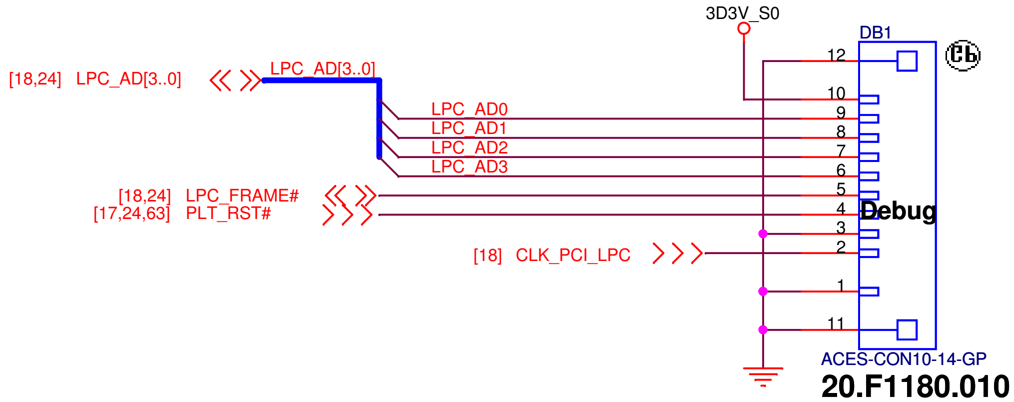
SSID = DEBUG PORT

Debug Connector



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

X01 0214

<Core Design>

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Title	*Dubug connector*	
Size A4	Document Number *Cottonwood*	Rev *A00*
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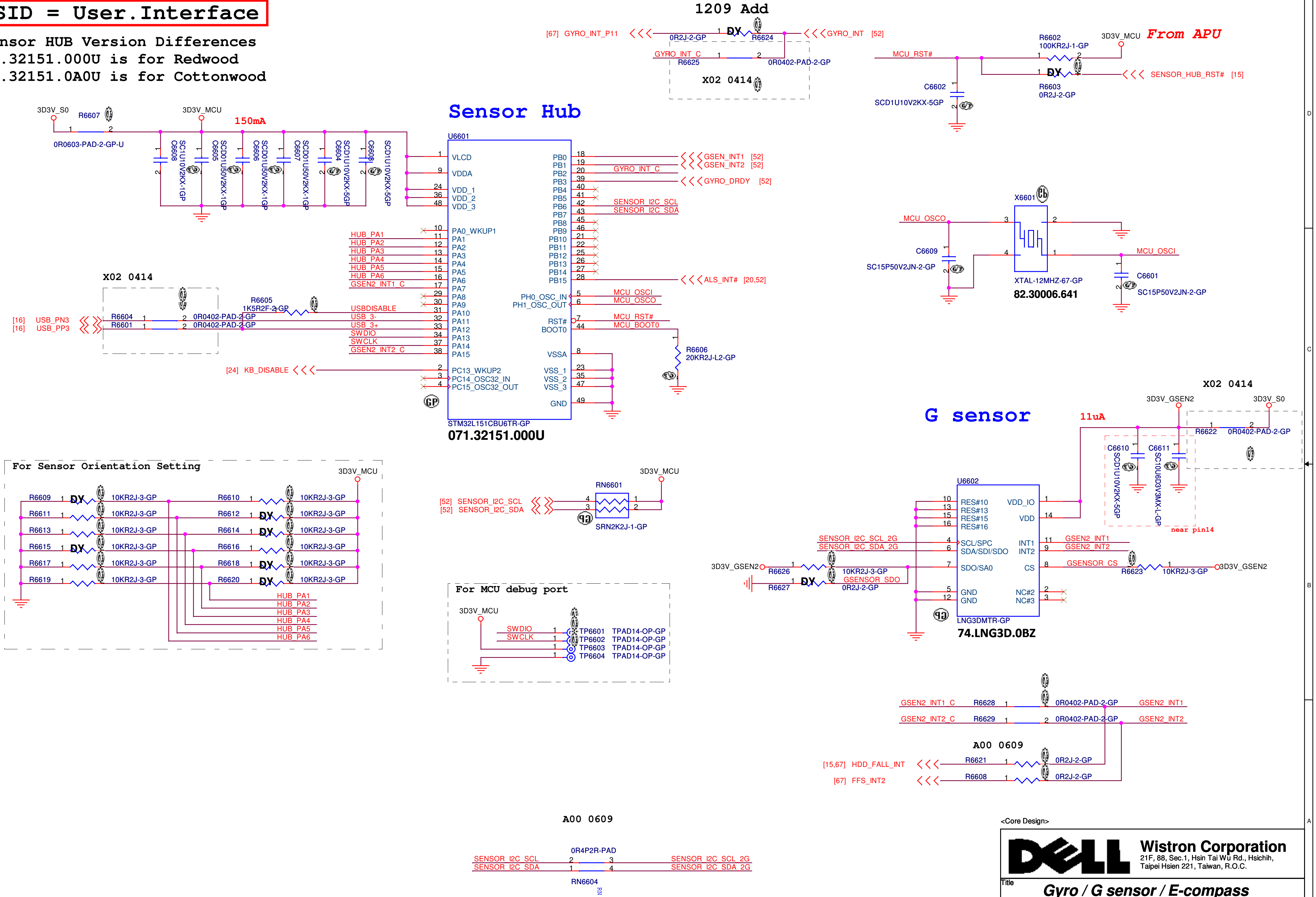
SSID = User.Interface

*Sensor HUB Version Differences
071.32151.000U is for Redwood
071.32151.0A0U is for Cottonwood



<Core Design>

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Title	Gyro / G sensor / E-compass		
Size A3	Document Number: Cottonwood		Rev A00
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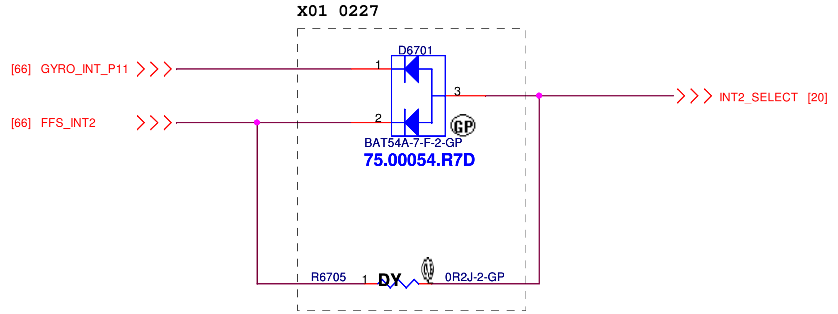
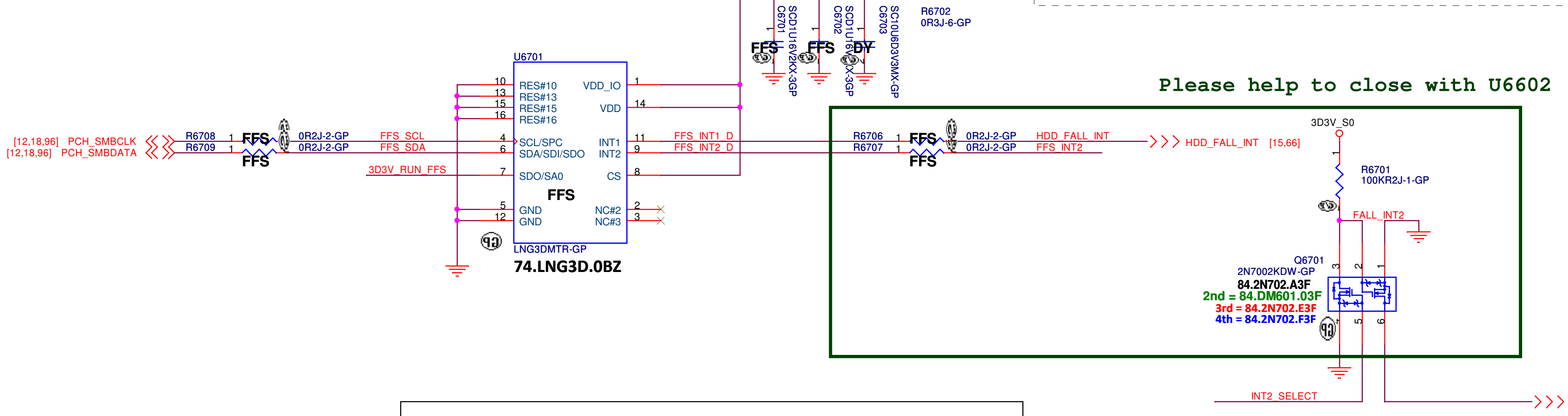


Free Fall Sensor



Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title	Reserved	
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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	RESERVED	
Size A3	Document Number Cottonwood	Rev A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**USB3.0 PORT**	
Size A3	Document Number **Cottonwood**	Rev **A00**
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5 4 3 2 1

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<Core Design>

DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A3	Document Number ***Cottonwood*** / Rev ***A00***
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5 4 3 2 1

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<Core Design>

Wistron Corporation
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Title	Reserved	
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<Core Design>

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Title		
Reserved		
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU Memory(2/5)	
Size A2	Document Number Cottonwood	Rev A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU_DP/LVDS/CRT/GPIO(3/5)	
Size A2	Document Number Cottonwood	Rev A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU_POWER(4/5)	
Size Custom	Document Number Cottonwood	Rev A00
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(Blanking)

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU-VRAM1,2 (1/4)	
Size A3	Document Number Cottonwood	Rev A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU-VRAM5,6 (3/4)	
Size A3	Document Number Cottonwood	Rev A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	GPU-VRAM7,8 (4/4)	
Size A3	Document Number Cottonwood	Rev A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	RT8812_VGACORE	
Size A2	Document Number Cottonwood	Rev A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
	Reserved		
Size: A3	Document Number: Cottonwood		Rev: A00
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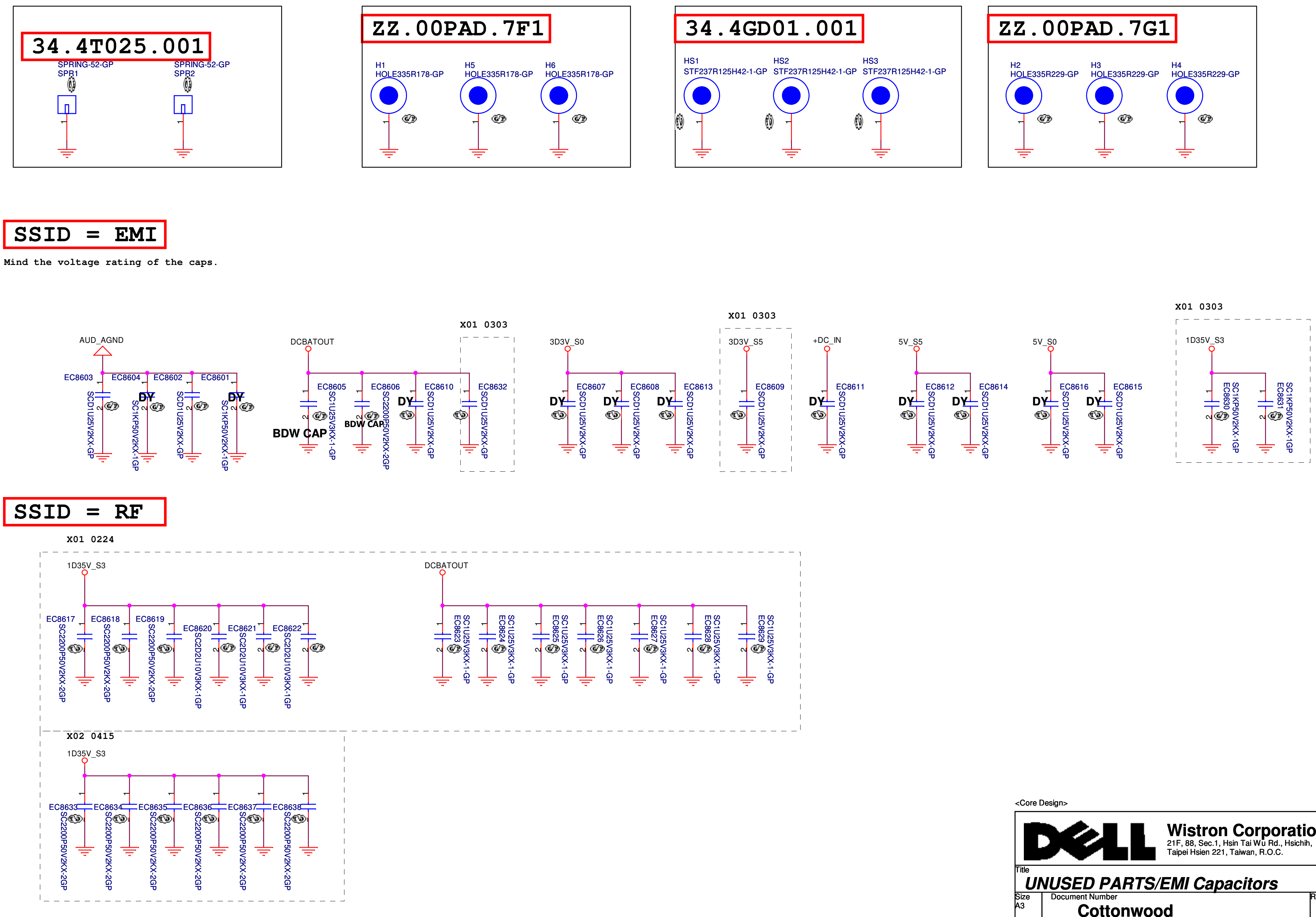
SSID = Mechanical

SSID = EMI

Mind the voltage rating of the caps.

SSID = RF



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	UNUSED PARTS/EMI Capacitors	
Size A3	Document Number Cottonwood	Rev A00
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<Core Design>

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Title		
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<Core Design>

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)Finger Print	
Size A4	Document Number Cottonwood	Rev A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Free Fall Sensor	
Size A3	Document Number Cottonwood	Rev A00
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<Core Design>

Wistron Corporation
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Title		
Reserved		
Size: A3	Document Number: Cottonwood	Rev: A00
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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Reserved		
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5 4 3 2 1

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Express Card		
Size: A3	Document Number: Cottonwood	Rev: A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	LVDS_Switch	
Size A3	Document Number Cottonwood	Rev A00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	CRT_Switch	
Size A3	Document Number Cottonwood	Rev A00
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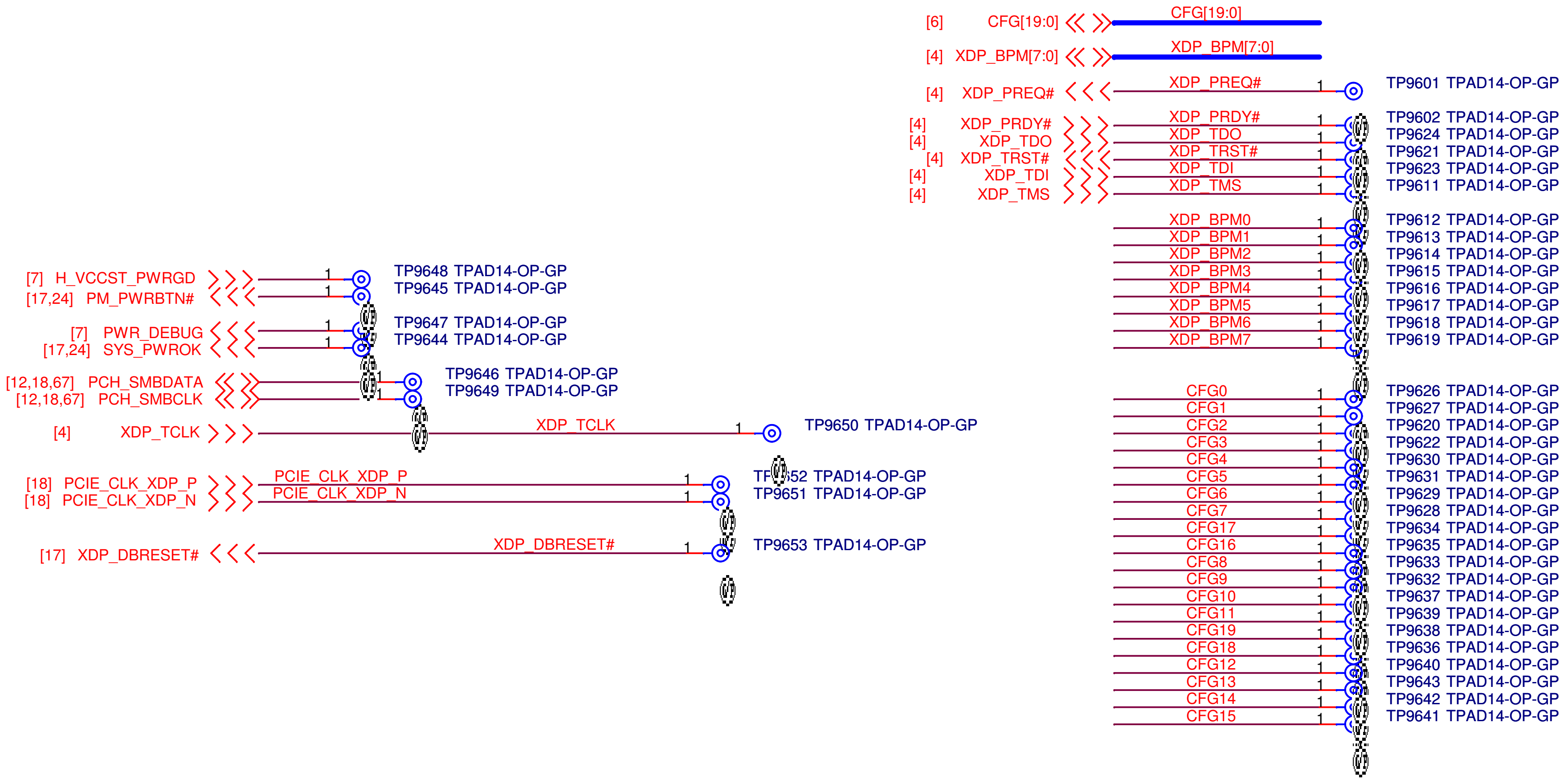
SSID = XDP

CPU XDP



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **CPU/PCH XDP**

Size	Document Number	Rev
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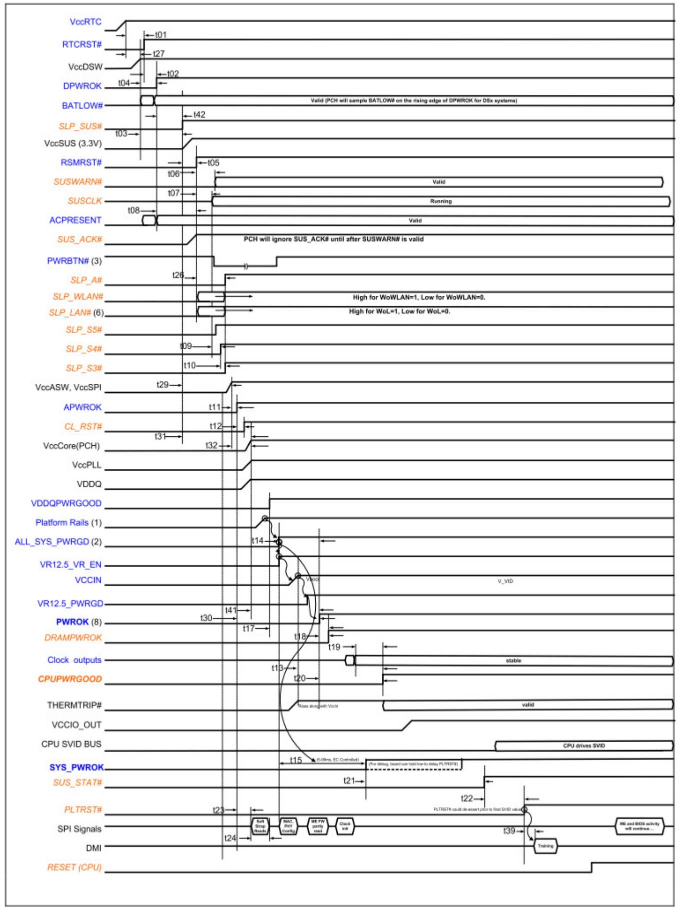
Shark Bay Platform Power Sequence



(DC mode)

Red Words: Controlled by EC GPIO

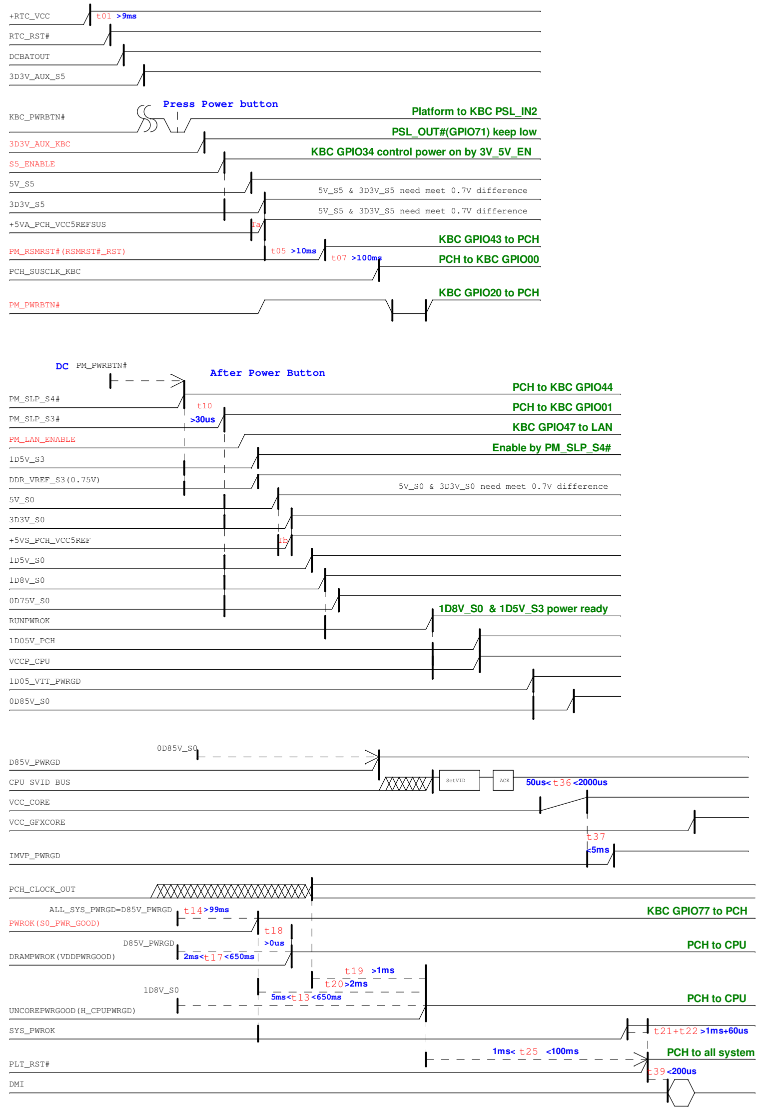
Sense the power button status

VREF_Sus must be powered up before VccSus3_3, or after VccSus3_3 within 0.7 V. Also, VREF_Sus must power down after VccSus3_3, or before VccSus3_3 within 0.7 V.

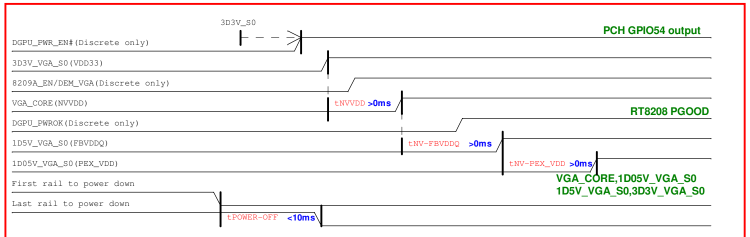
In case of a non-Deep S4/S5 Platform timing t42 should be added to t07 which will make it 100mS minimum.

VREF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, VREF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.



N14P-GT Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

<Core Design>

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Title	Power Sequence				
Size A1	Document Number Cottonwood				Rev A00
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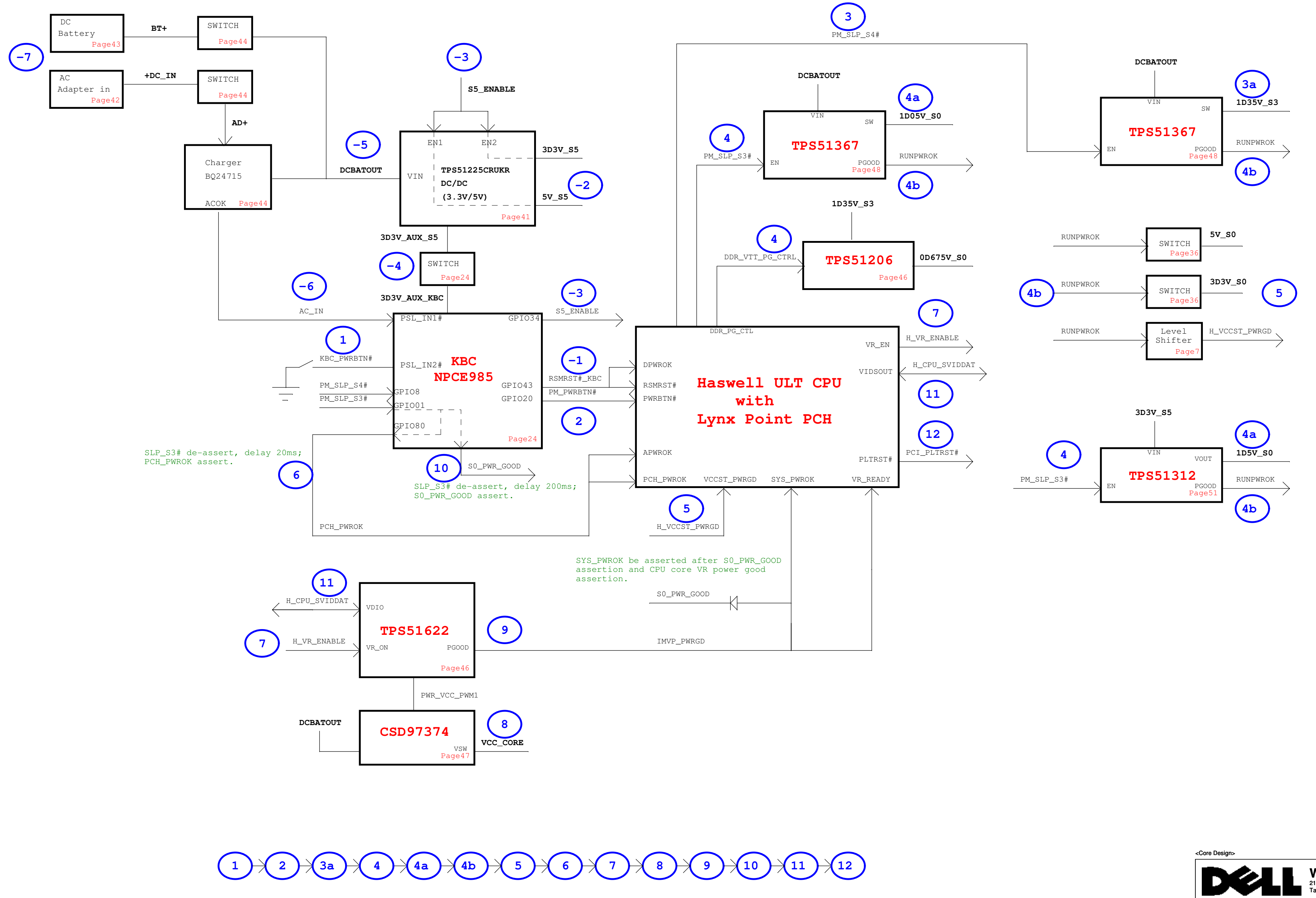
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



<Core Design>

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Title: Power Sequence Diagram

Size: A2 | Document Number: Cottonwood | Rev: A00

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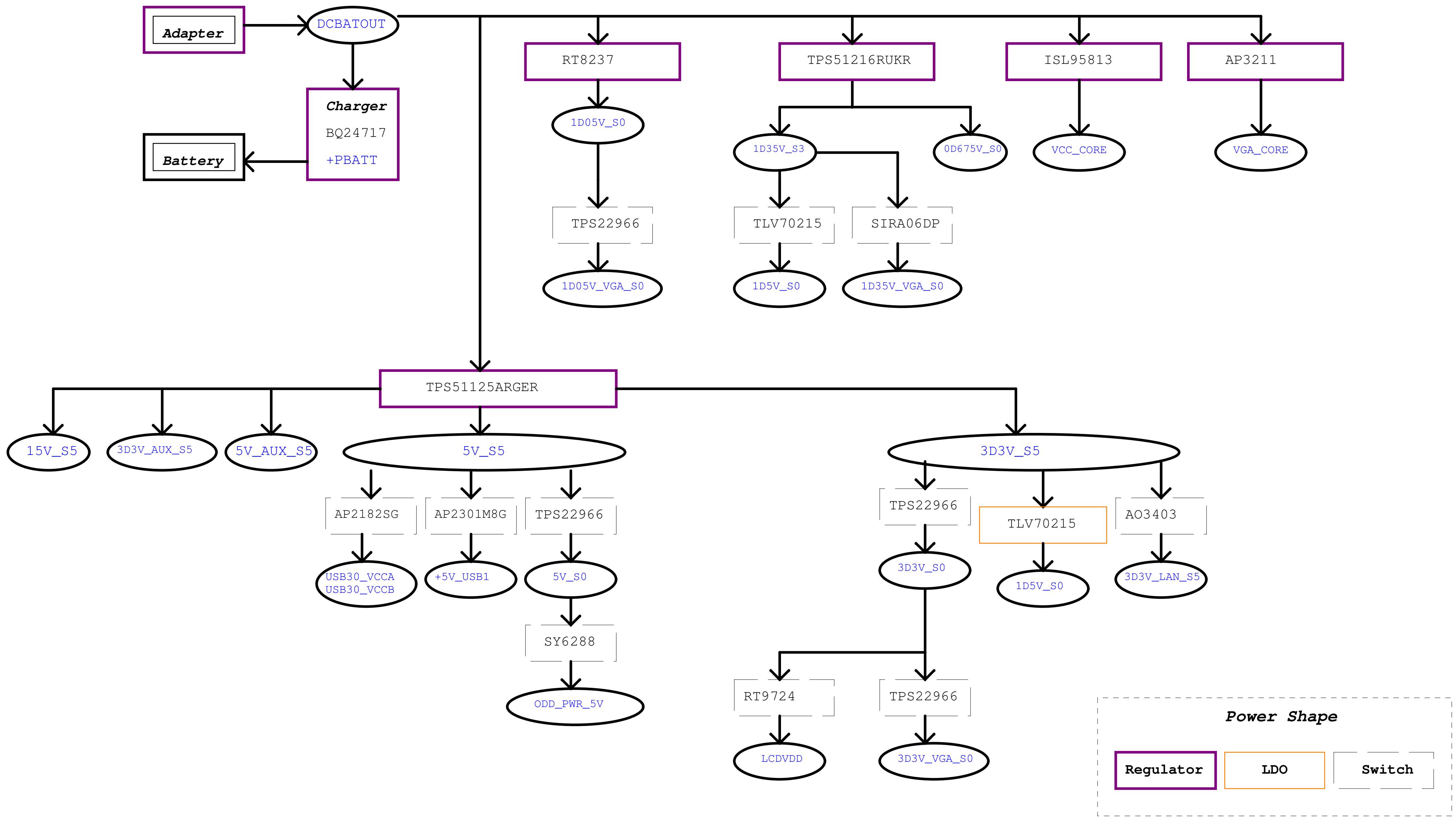

<Core Design>

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Title		
Power Block Diagram		
Size: A3	Document Number: **Cottonwood**	Rev: **A00**
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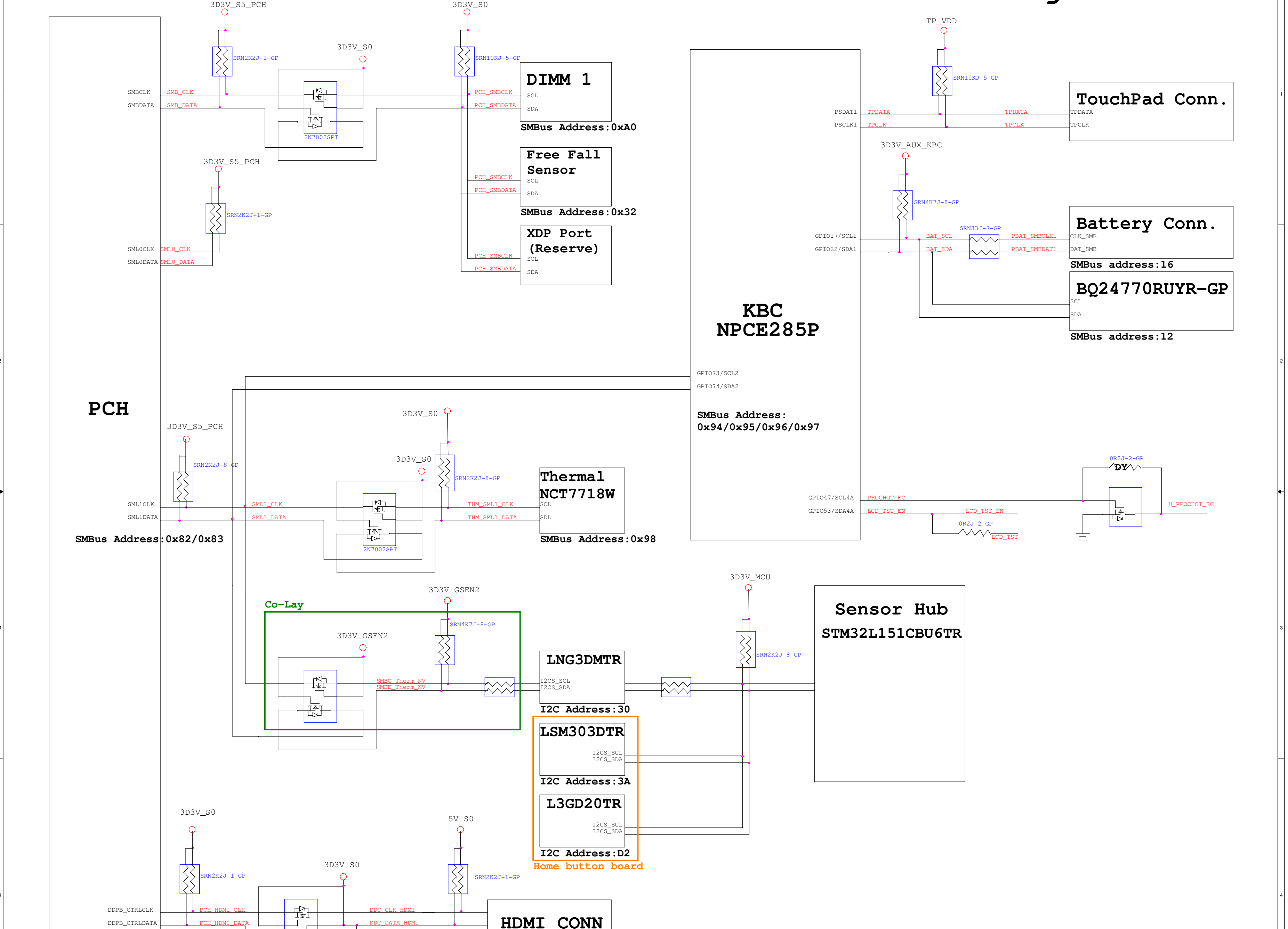
PCH SMBus Block Diagram

KBC SMBus Block Diagram



<Core Design>

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Title	SMBUS Block Diagram	
Size: Custom	Document Number: Cottonwood	Rev: A00
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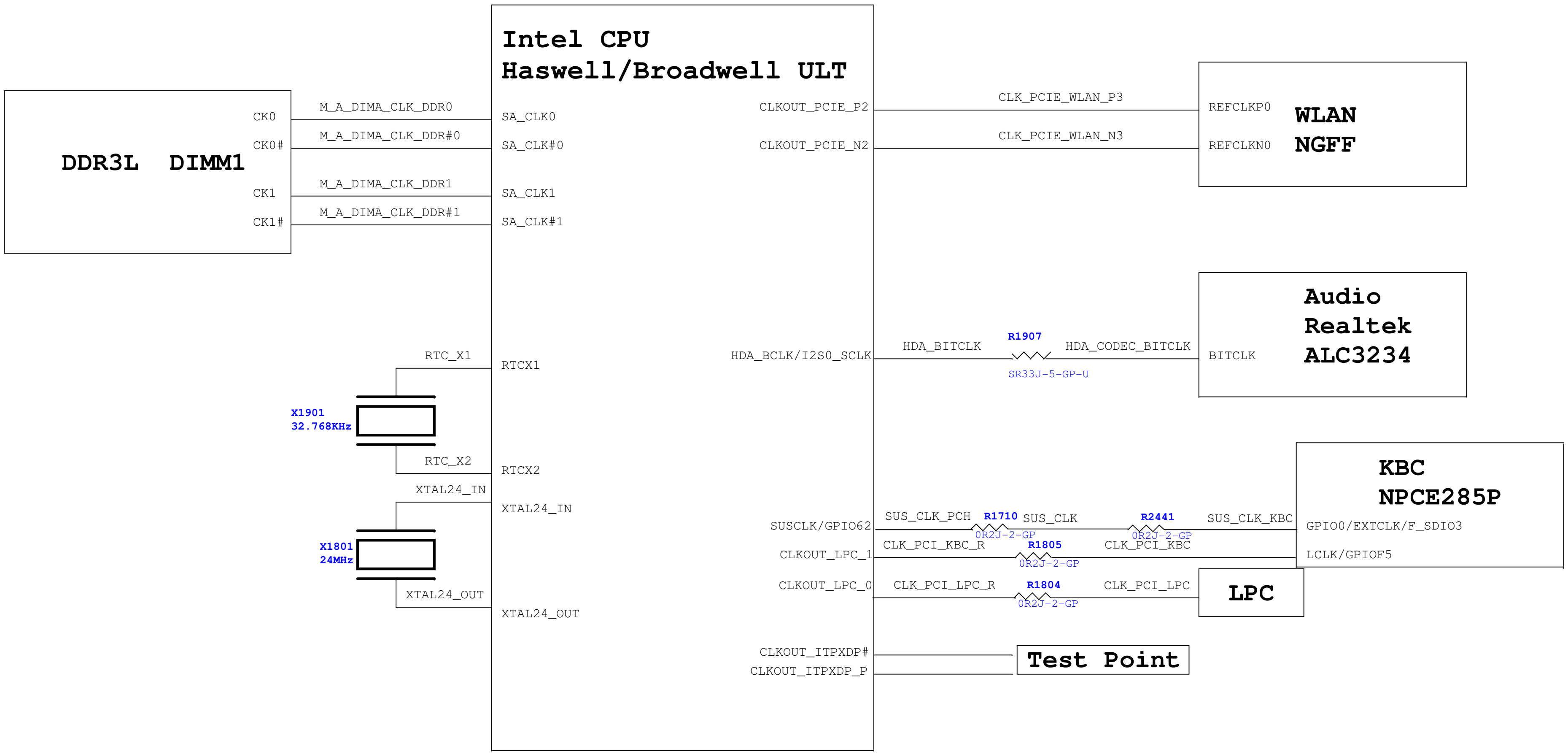
CLK Block Diagram



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CLK Block Diagram

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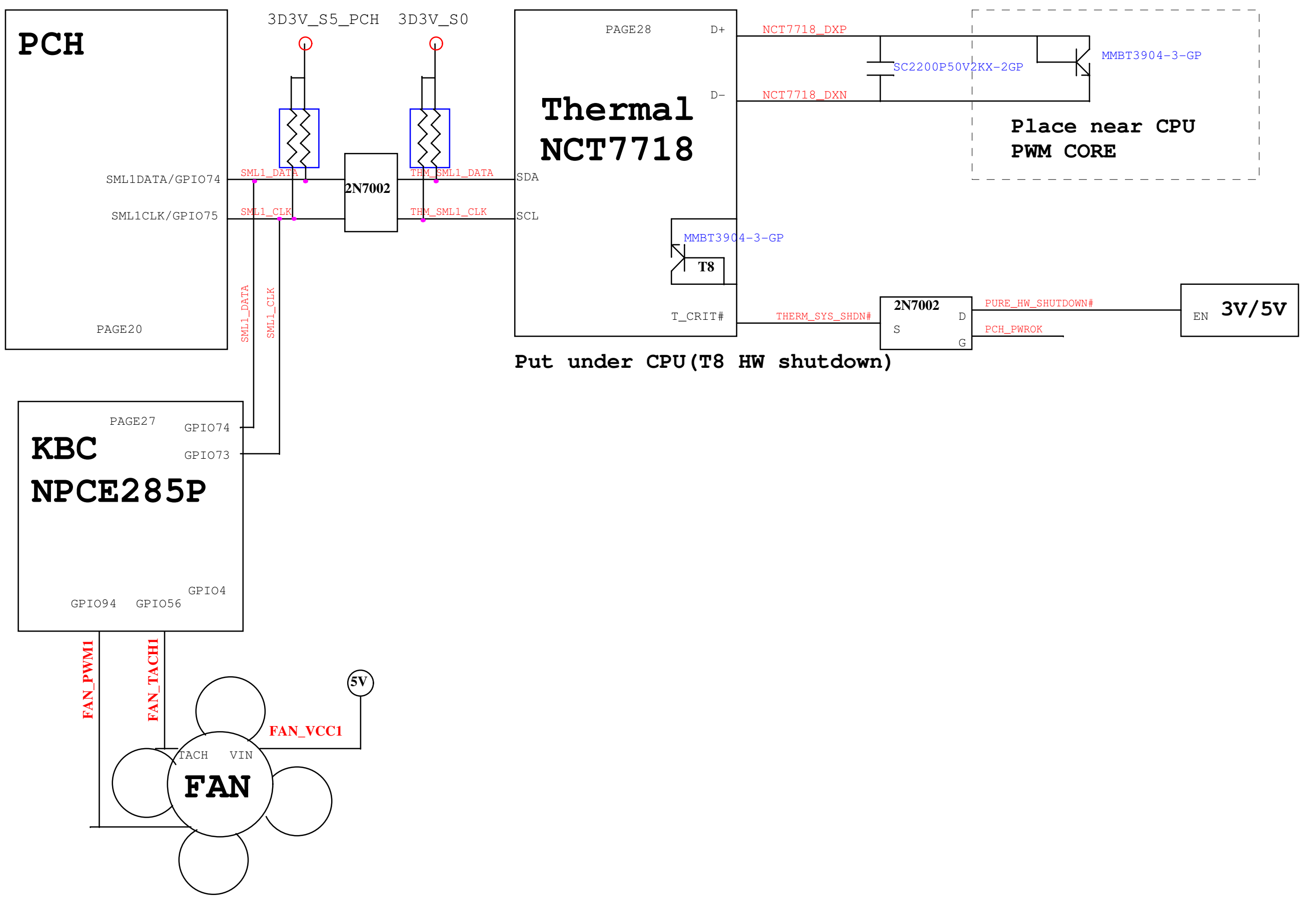
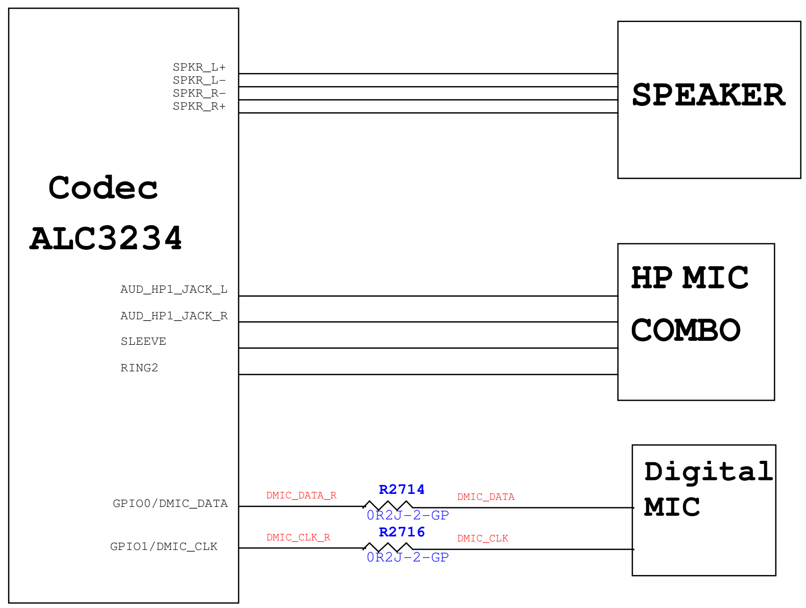
Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Title	Thermal/Audio Block Diagram	
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Change notes –

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **Change History**

Size: A3 | Document Number: **Cottonwood** | Rev: **A00**

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VERSION	DATA	PAGE	Change Iteam

<Core Design>

DELL

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Change History

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