MS-7676

UATX Ver:0C

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH

OnBoard Chipset:

Clock Gen:IDT 4106
HD Audio Codec:RTL892
LAN:RTL 8111E 10/100/1000
SIO:FIN71889AD
Flash ROM: 64 Mb SPI (PCH)* 2

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X4) Slot * 1
PCI Express (X1) Slot * 2

PWM:

Controller:VRD12 UPI6234 (6+2-Phase)Dr.MOS

CPU+GPU
Controller:uP6113 Dr.MOS
CPU VTT CPU SA
Controller:uP6103A
DDR PCH

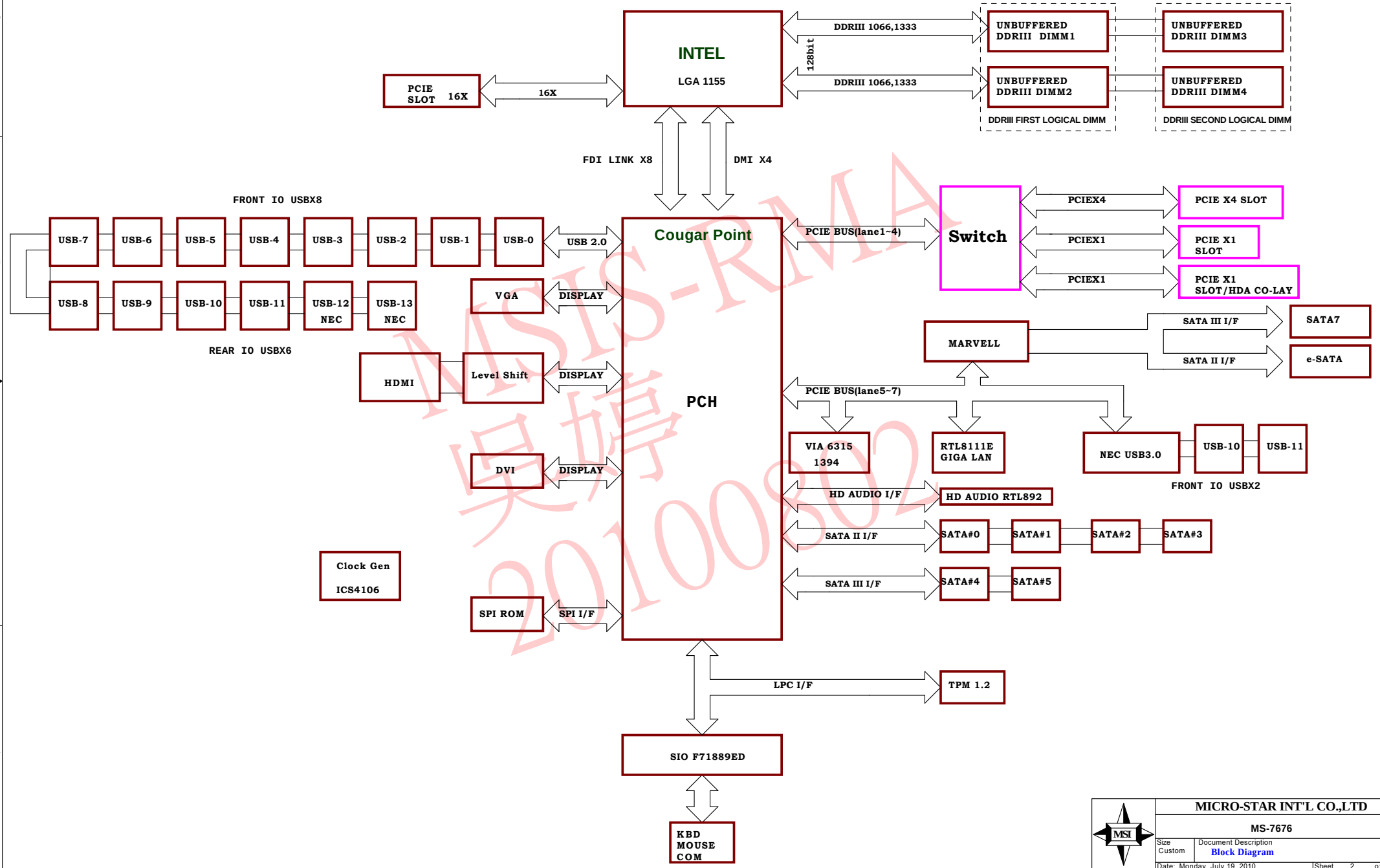
ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)
SATA3.0X1 + e-SATA X1(MARVELL)
USB2.0 RearX4 Front x8(PCH)
USB3.0 RearX2 (NEC uPD720200)
1394 Controller - VT6315N-CE
D-SUB *1
DVI-D PORT*1
HDMI *1
TPM Header *1
COM Header *1
on BOARD BUZZER

MICRO-STAR INT'L CO.,LTD
MS-7676
Size: Custom | Document Description: Cover Sheet | Rev: 0C
Date: Monday, July 19, 2010 | Sheet 1 of 47



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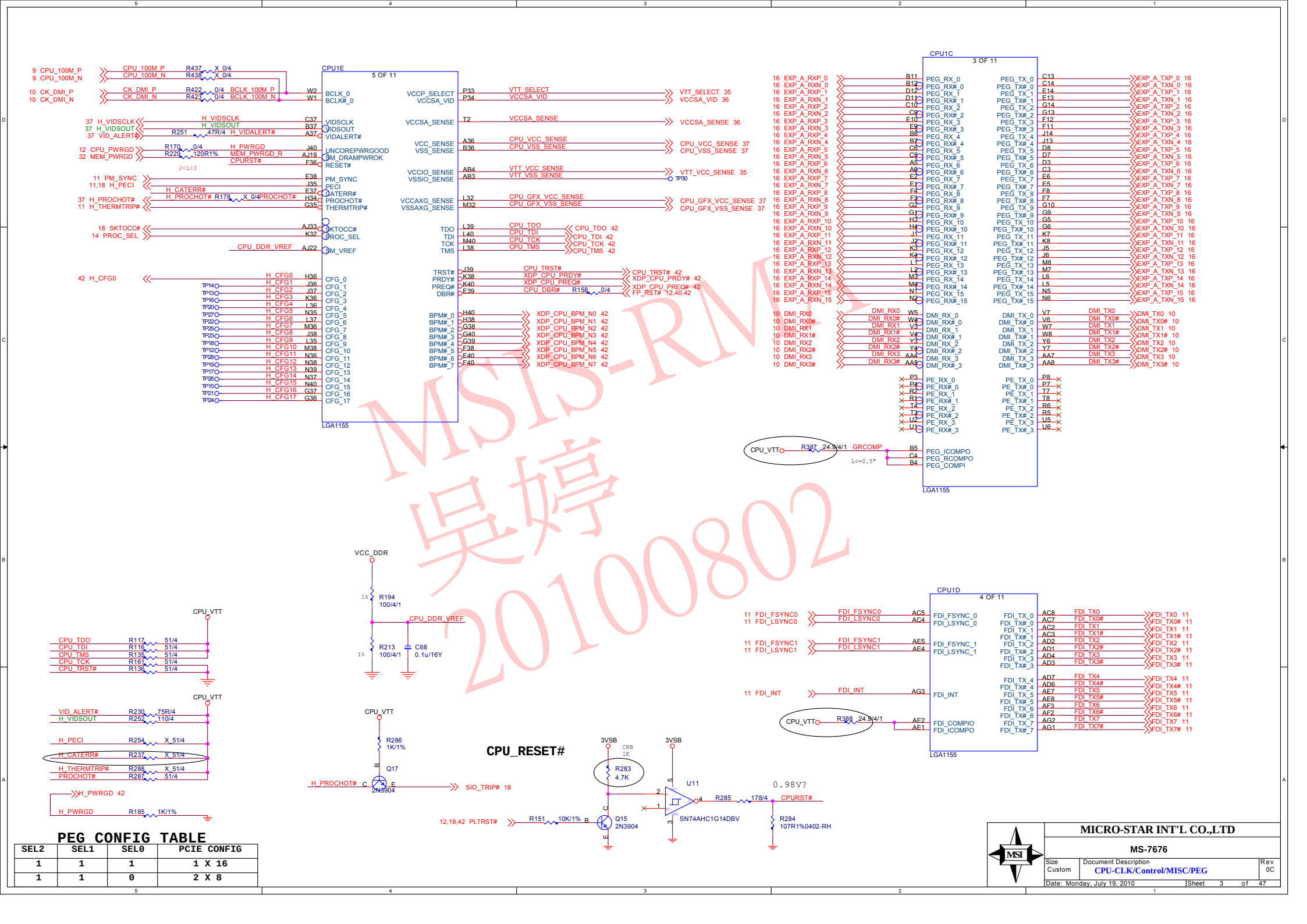
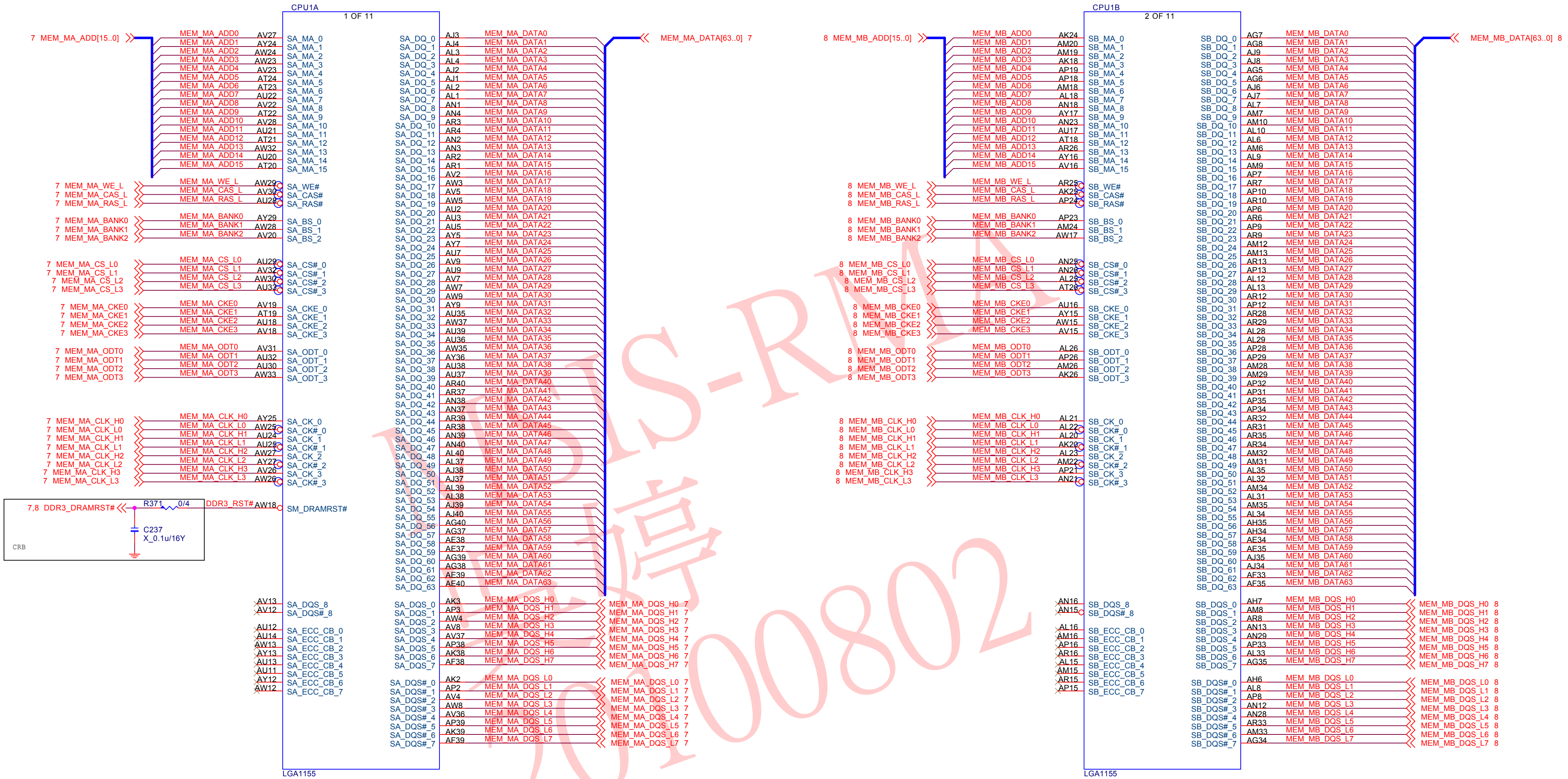
MS-7676

Size: Custom | Document Description: Block Diagram | Rev: 0C

Date: Monday, July 19, 2010 | Sheet 2 of 47


CPU1E
5 OF 11
LGA1155
CPU1C
3 OF 11
LGA1155
CPU1D
4 OF 11
LGA1155
CPU_RESET#
PEG CONFIG TABLE
SEL2 SEL1 SEL0 PCIE CONFIG
1 1 1 1 X 16
1 1 0 2 X 8
MSI-RMA
吴婷
20100802
MICRO-STAR INT'L CO.,LTD
MS-7676
CPU-CLK/Control/MISC/PEG
Rev 0C
Monday, July 19, 2010
Sheet 3 of 47



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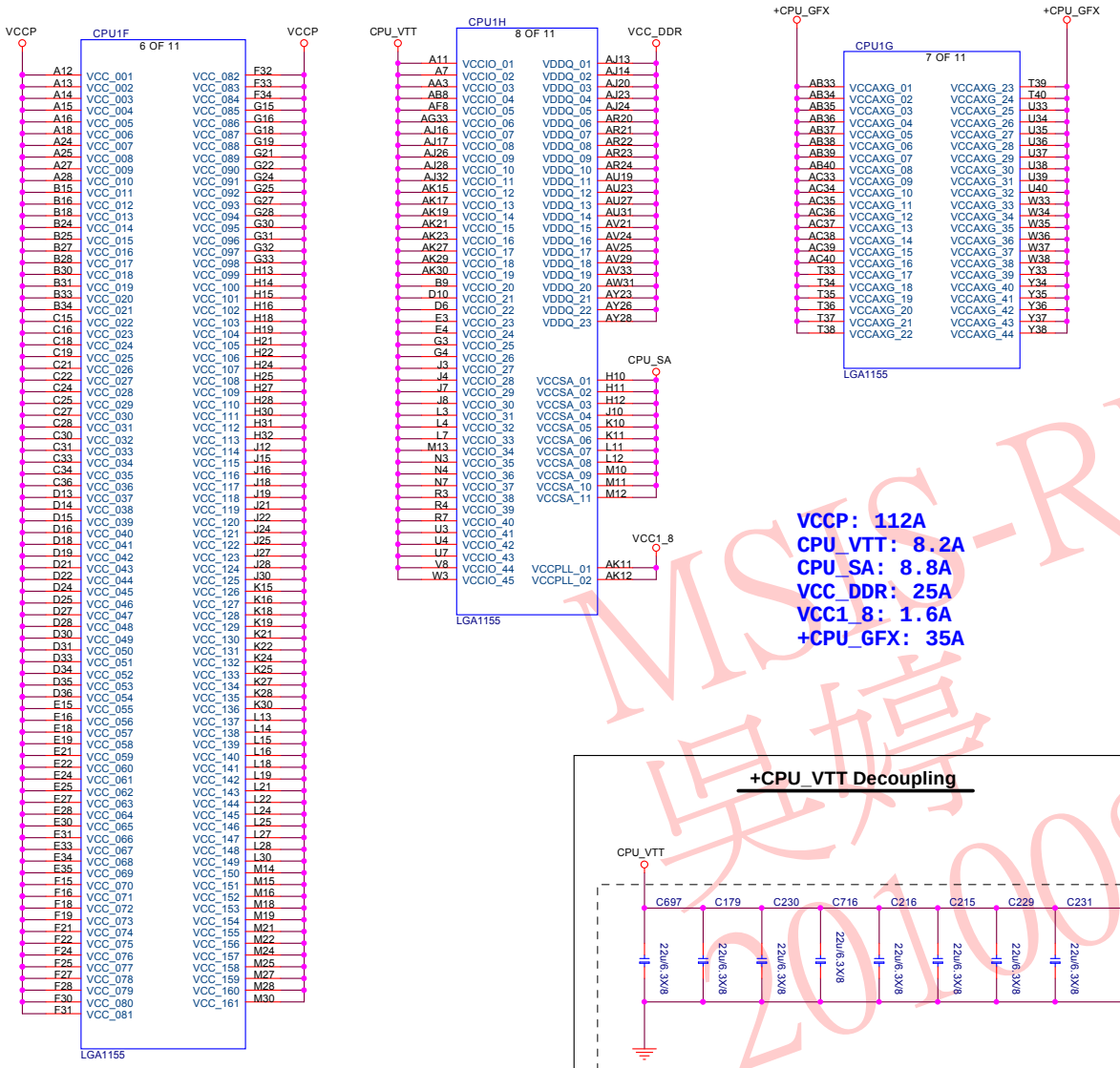
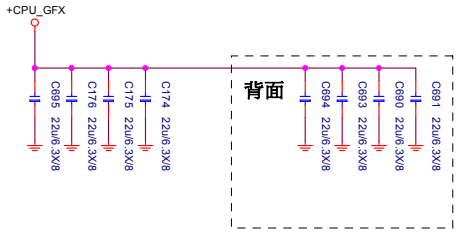
MS-7676

Size	Document Description	Rev
Custom	CPU-Memory	0C

Date: Monday, July 19, 2010 Sheet 4 of 47

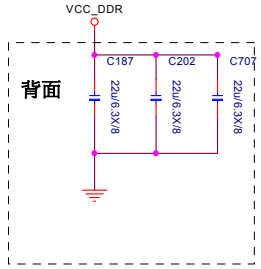


+CPU_GFX Decoupling

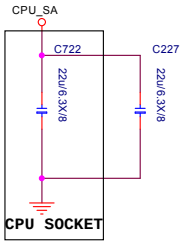


CPU SOCKET CAVITY CAPS

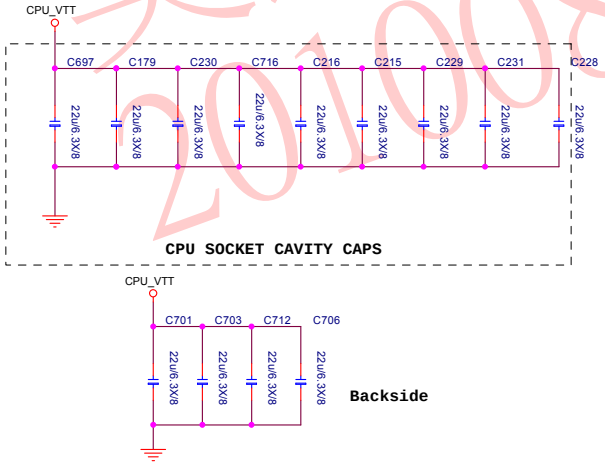
+1.5V_DDR3-Decoupling



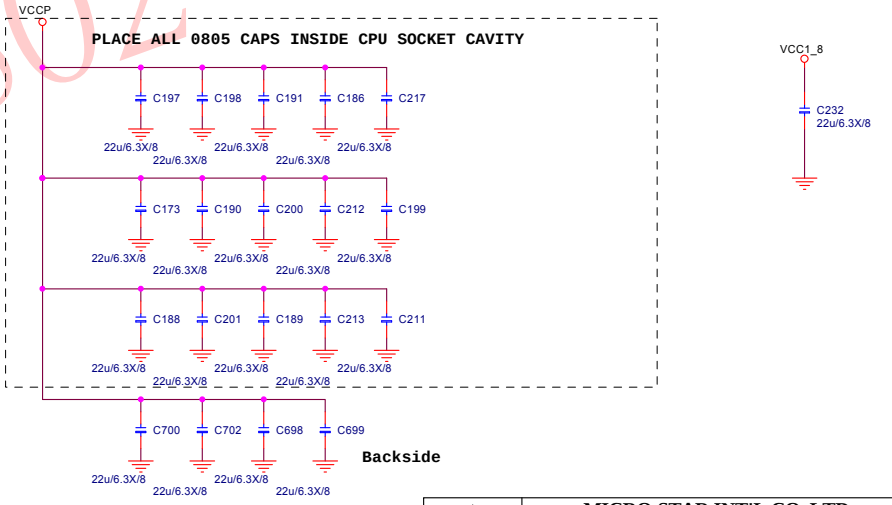
CPU SOCKET CAVITY CAPS



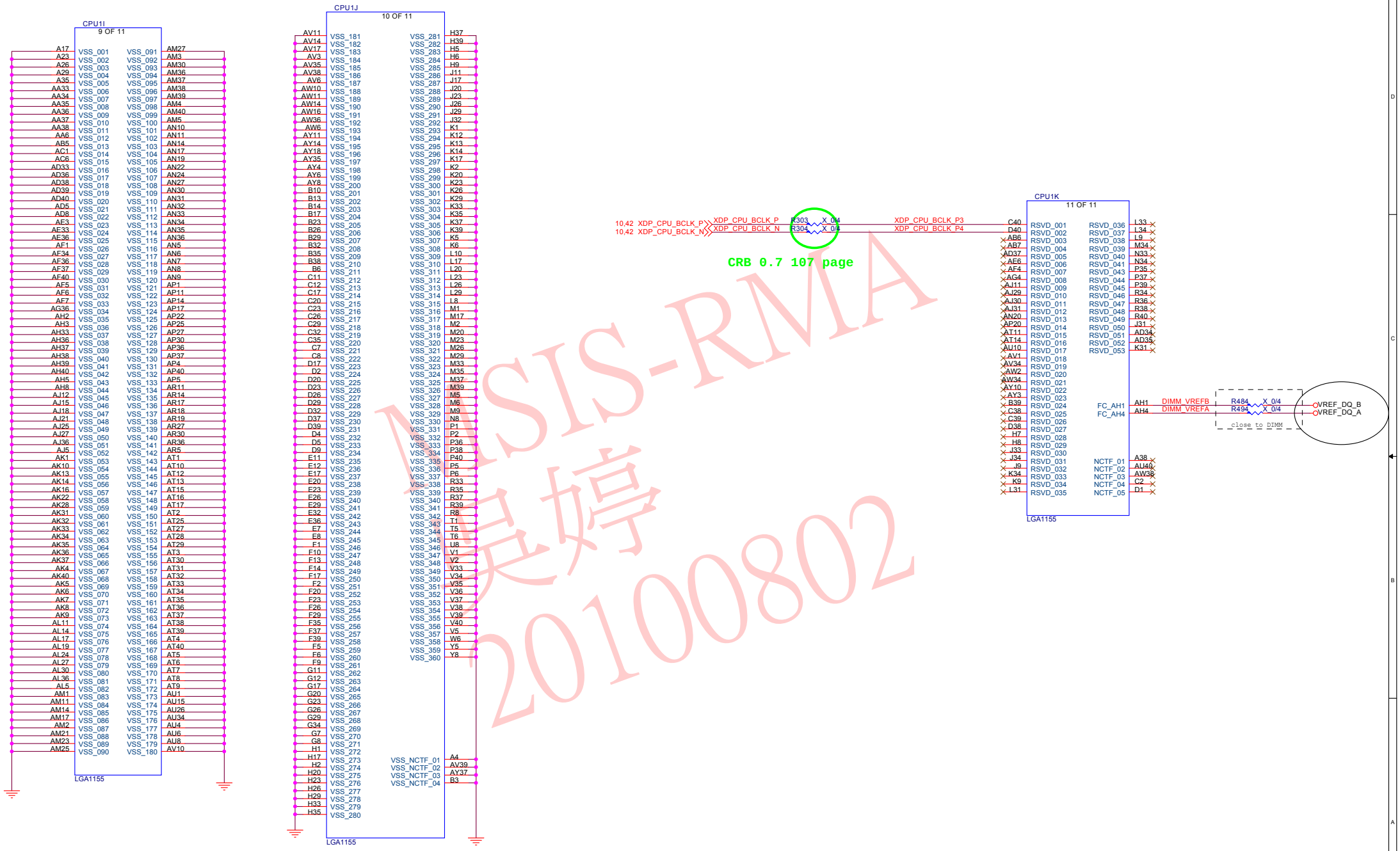
+CPU_VTT Decoupling



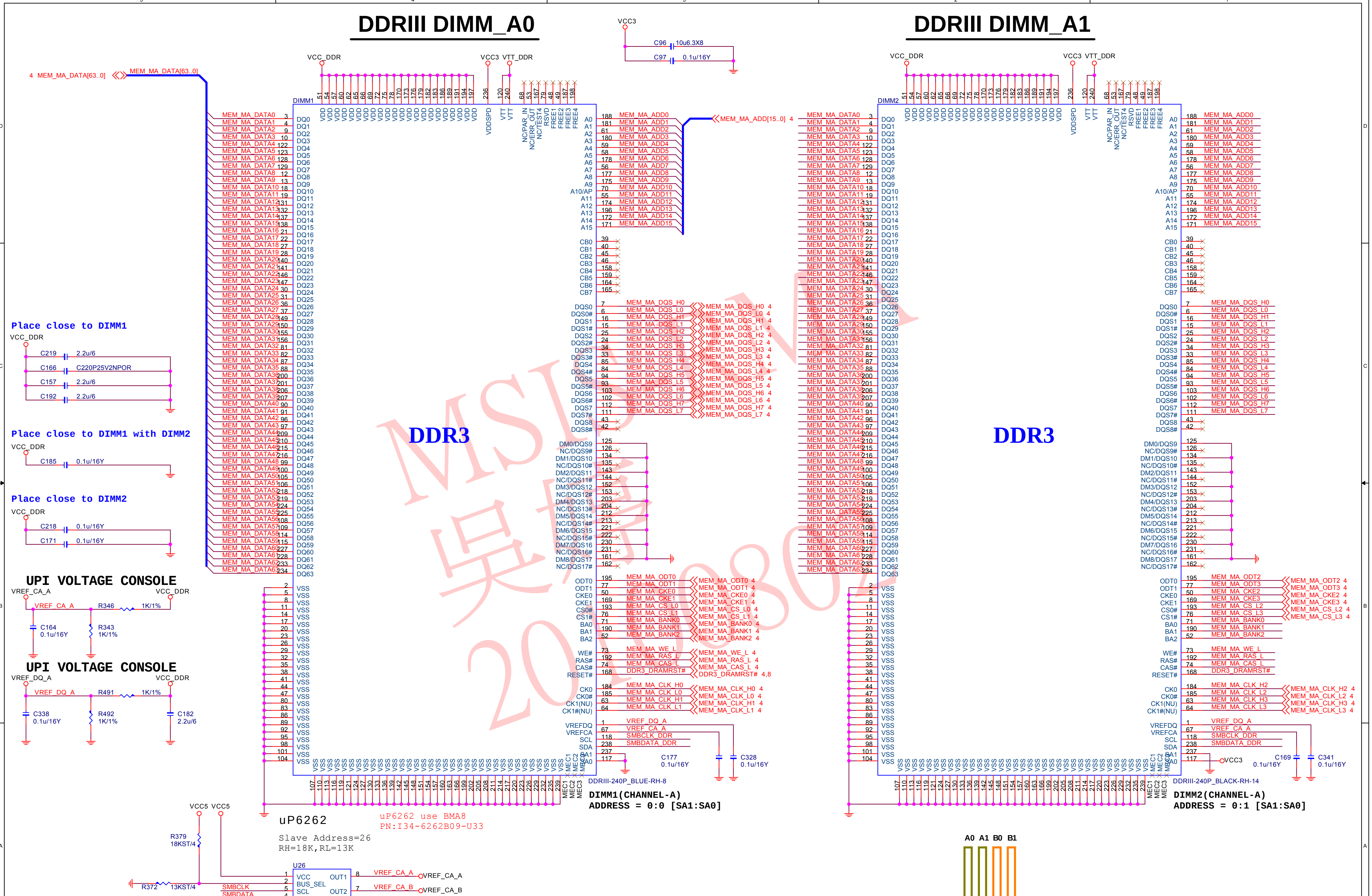
+CPU_VCCP-Decoupling



MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size: Custom	Document Description: CPU-Power	Rev: 0C
Date: Monday, July 19, 2010	Sheet 5 of 47	

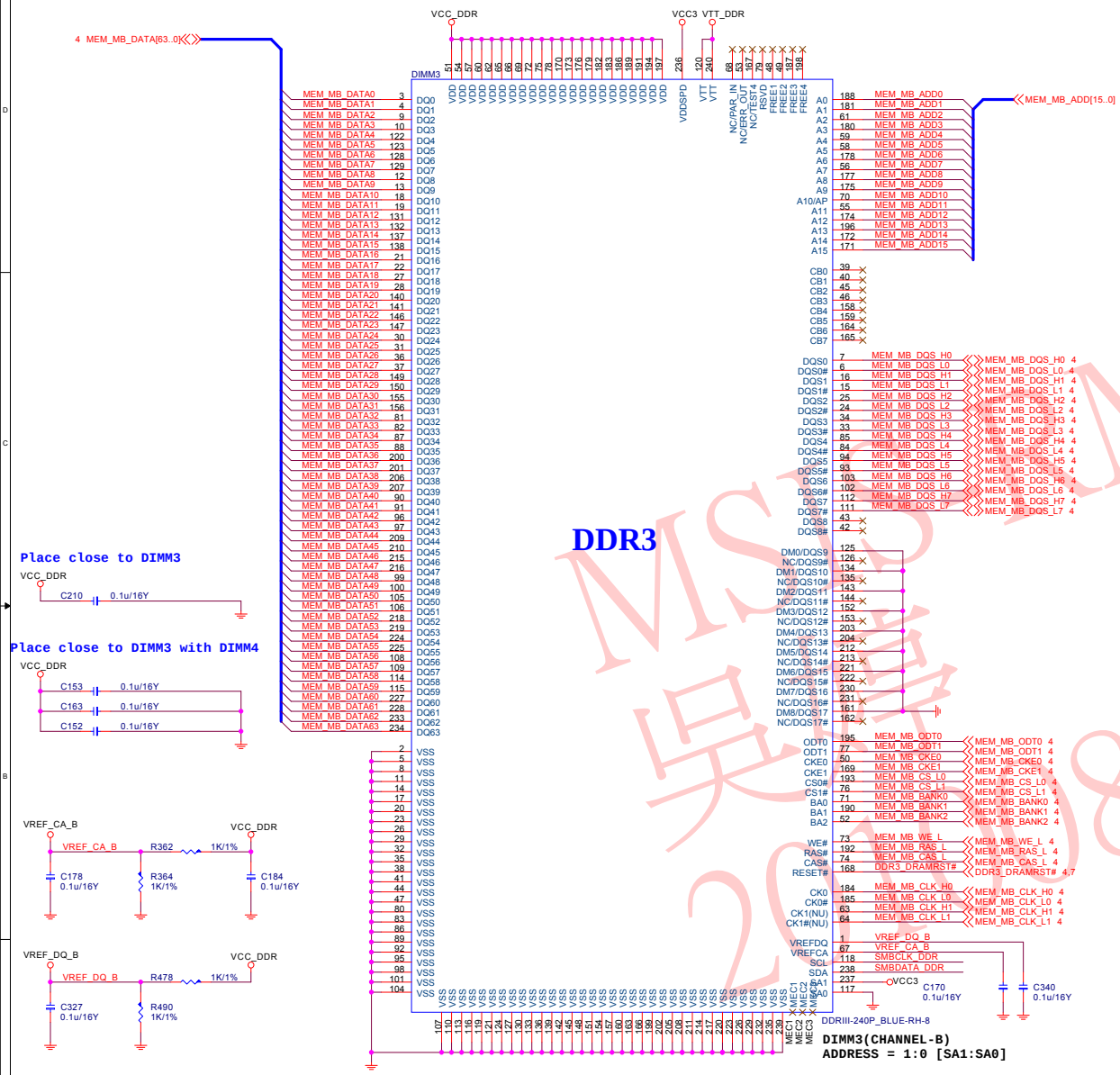


MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size: Custom	Document Description: CPU-GND	Rev: 0C
Date: Monday, July 19, 2010	Sheet 6 of 47	

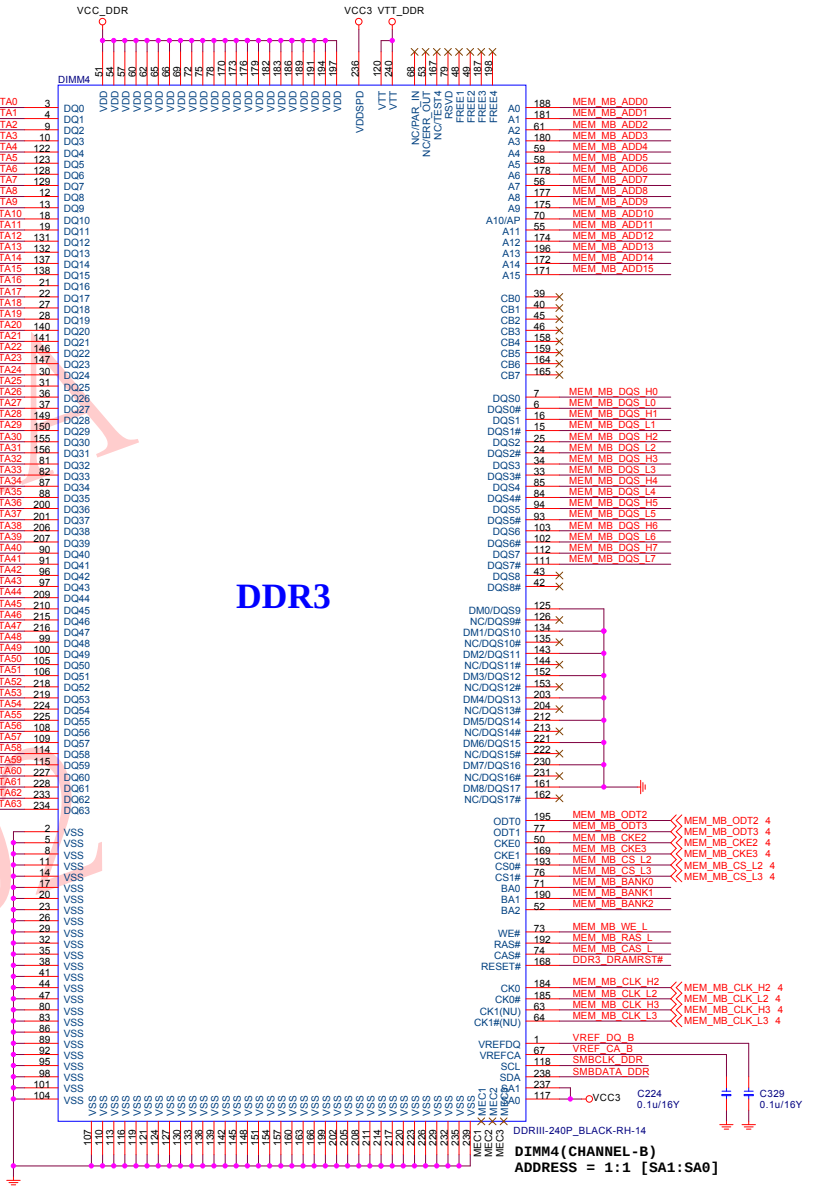

DDRIII DIMM_A0
DDRIII DIMM_A1
VCC3
C96 10u6.3X8
C97 0.1u/16Y
VCC_DDR
VCC3 VTT_DDR
4 MEM_MA_DATA[63..0]
MEM_MA_DATA[63..0]
MEM_MA_ADD[15..0] 4
DIMM1
DIMM2
DDR3
Place close to DIMM1
C219 2.2u/6
C166 C220P25V2NPOR
C157 2.2u/6
C192 2.2u/6
Place close to DIMM1 with DIMM2
C185 0.1u/16Y
Place close to DIMM2
C218 0.1u/16Y
C171 0.1u/16Y
UPI VOLTAGE CONSOLE
VREF_CA_A
R346 1K/1%
C164 0.1u/16Y
R343 1K/1%
VREF_DQ_A
R491 1K/1%
C338 0.1u/16Y
R492 1K/1%
C182 2.2u/6
DDRIII-240P_BLUE-RH-8
DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
DDRIII-240P_BLACK-RH-14
DIMM2(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
C177 0.1u/16Y
C328 0.1u/16Y
C169 0.1u/16Y
C341 0.1u/16Y
VCC5 VCC5
R379 18KST/4
R372 13KST/4
uP6262
Slave Address=26
RH=18K,RL=13K
uP6262 use BMA8
PN:I34-6262B09-U33
U26
uP6262-BMA8
VREF_CA_A
VREF_CA_B
8 SMBCLK_DDR
8 SMBDATA_DDR
R214 33R
R215 33R
SMBCLK 8,9,12,16,17,34,37,42
SMBDATA 8,9,12,16,17,34,37,42
A0 A1 B0 B1

MICRO-STAR INT'L CO.,LTD	
MS-7676	
Size: Custom	Document Description: DDR III DIMM 1 / DIMM 2
Rev: 0C	
Date: Monday, July 19, 2010	Sheet 7 of 47

DDRIII DIMM_B0



DDRIII DIMM_B1



VCC5 VCC5

R493 9.1KR1%

R489 3K/1%

uP6262

uP6262 use BMA8

PN:I34-6262B09-U33

Slave Address=28

RH=9.1K,RL=3K

U37

VCC BUS_SEL SCL SDA GND

OUT1 OUT2 OUT3

VREF_DQ_A VREF_DQ_B

SMBCLK SMBDATA

7,9,12,16,17,34,37,42 SMBCLK

7,9,12,16,17,34,37,42 SMBDATA

uP6262-BMA8

SMBCLK_DDR SMBCLK_DDR 7

SMBDATA_DDR SMBDATA_DDR 7

MICRO-STAR INT'L CO.,LTD

MS-7676

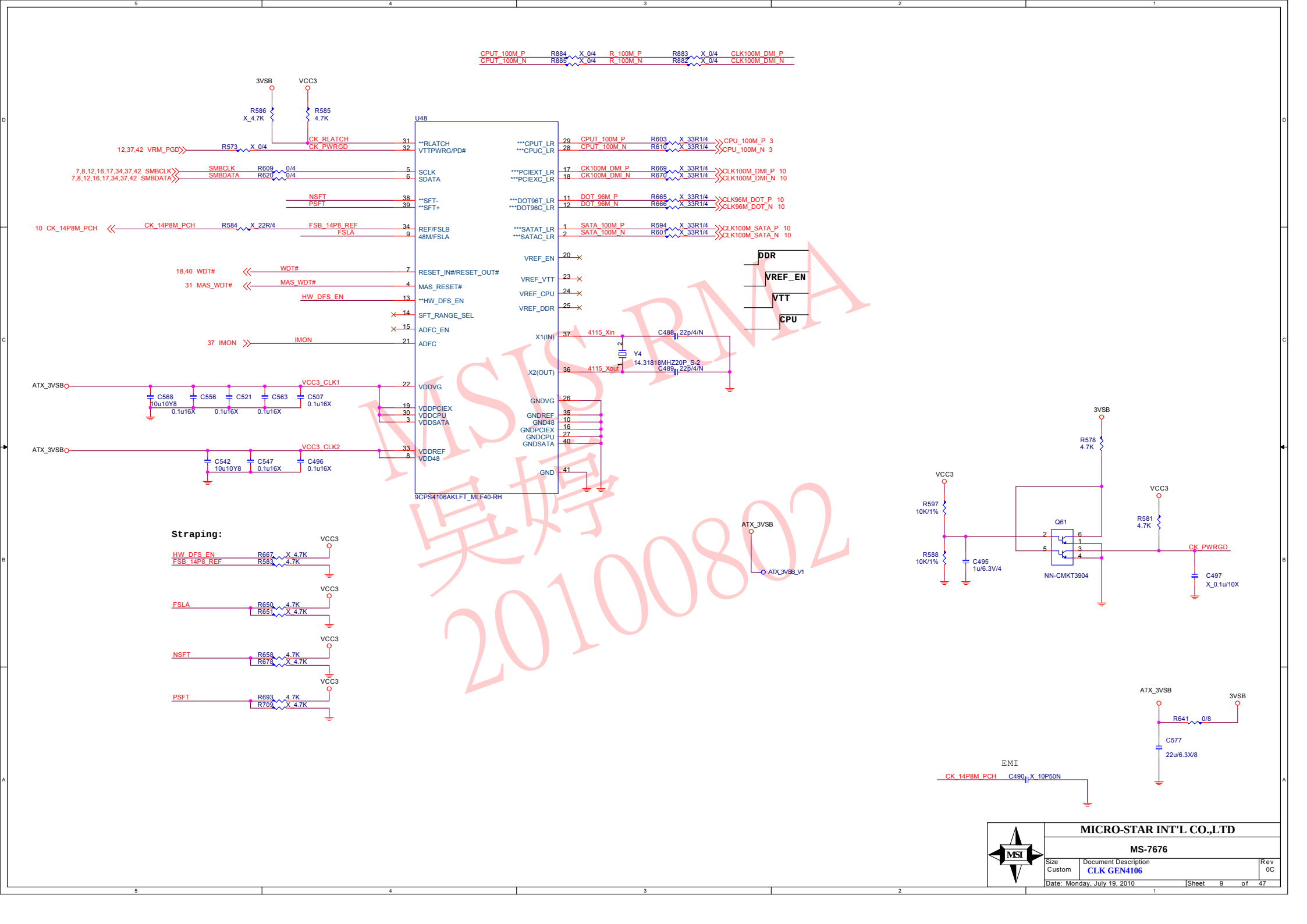
Size: Custom

Document Description: DDR III DIMM 3 / DIMM 4

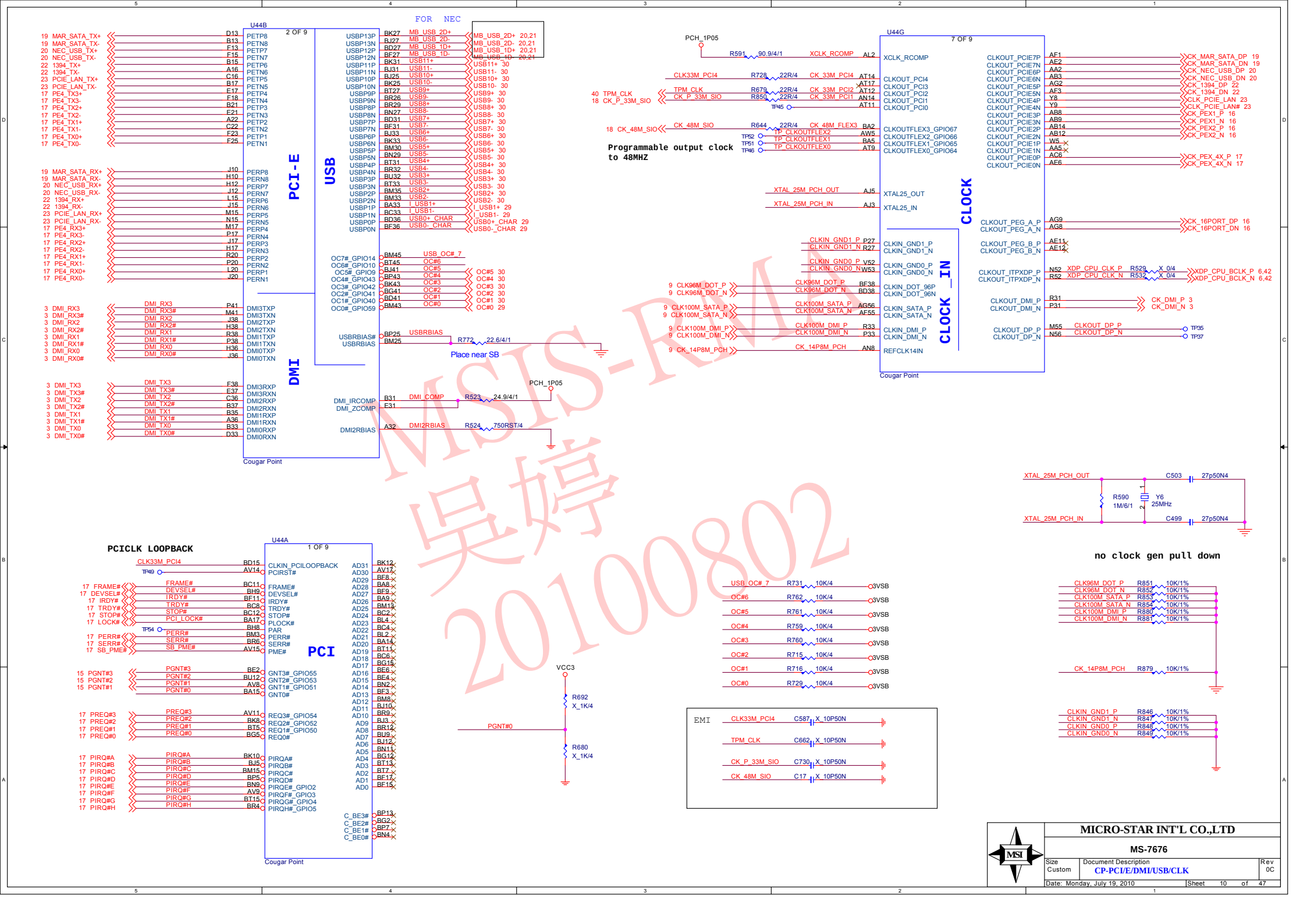
Rev: 0C

Date: Monday, July 19, 2010

Sheet 8 of 47



MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size: Custom	Document Description: CLK GEN4106	Rev: 0C
Date: Monday, July 19, 2010	Sheet 9 of 47	



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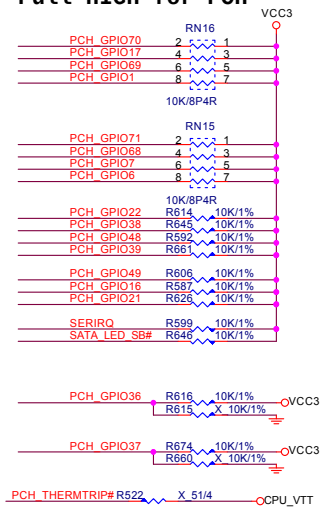
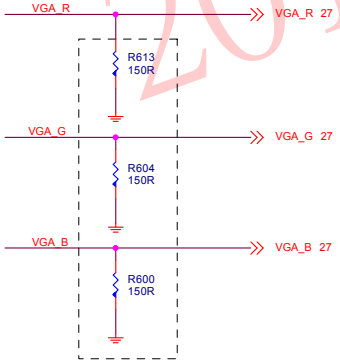
MS-7676	
Size: Custom	Document Description: CP-PCI/E/DMI/USB/CLK
Rev: 0C	
Date: Monday, July 19, 2010	Sheet 10 of 47

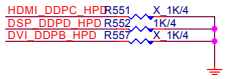
Pull HIGH for PCH



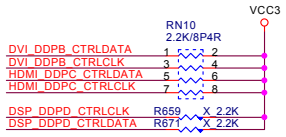


Close to PCH within 250 mils.

No VGA(pull down)



Enable VGA(CTRLCLK/DATA Pull High)

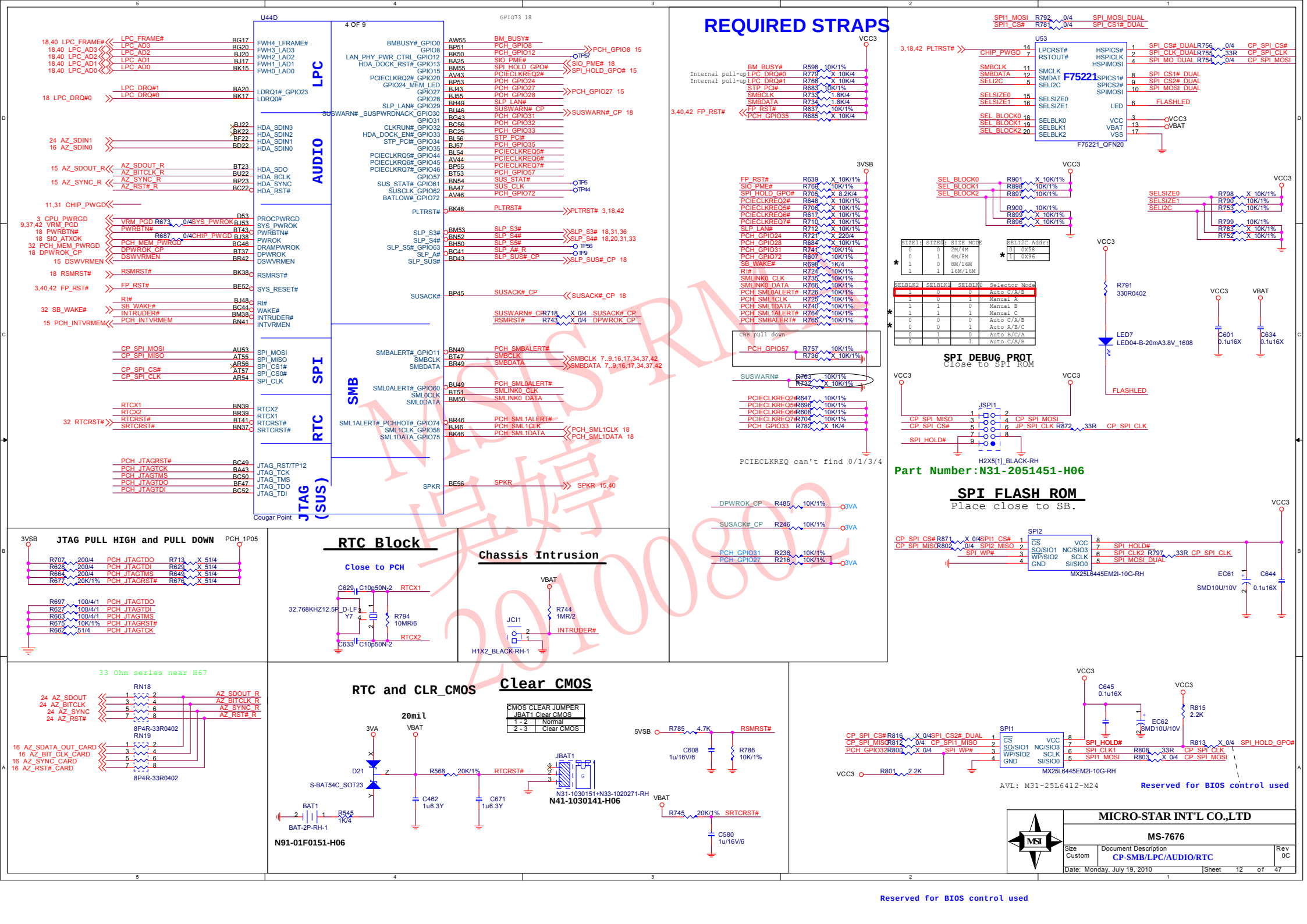


MICRO-STAR INT'L CO.,LTD

MS-7676

Size	Document Description	Rev
Custom	CP-SATA/HOST/FAN/GPIO/VGA	0C

Date: Monday, July 19, 2010 Sheet 11 of 47



Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

PCH_1P05

R514 X_0/8 VCCAFDIPLL
C414 10u6.3X8

R595 X_0/4 VCCACLK
NO THIS PIN

R515 X_0/8 VCCAPLLDMI2
C417 10u6.3X8
C424 1u/6.3V/4

R642 0/8 VCCCLKDMI
C553 10u6.3X8
C554 1u/6.3V/4

R535 0/8 VCCA_DPLLA
EC46 CD100u16SO-RH-2
C460 10u6.3X8
C472 1u/6.3V/4

R572 0/8 VCCA_DPLLB
EC47 CD100u16SO-RH-2
C477 10u6.3X8
C478 1u/6.3V/4

PCH_1P05

DMI PLL FILTER

L21 X_L1U_500mA_0805
VCCAPLLEXP
C418 X_10u6.3X8
C425 1u/6.3V/4

SATA PLL FILTER

L22 X_L10U_100mA_0805
VCCAPLLSATA
C458 X_10u6.3X8
C464 1u/6.3V/4

U44H
8 OF 9
Cougar Point

CPU_VTT
D55 V_PROC_IO
B56 V_PROC_IO_NCTF

CPU_VTT
B41 VCCDMI_02
E41 VCCDMI_01

C428 1u/6.3V/4
VCCAPLLDMI2 A19 VCCAPLLDMI2
VCCCLKDMI AJ20 VCCCLKDMI

5VREF BF1 V5REF
5VREF_SUS BT25 V5REF_SUS

+3.3V_DAC AT1 VCCADAC
VCCACLK AL5 VCCACLK

VCCA_DPLLA AB1 VCCADPLLA
VCCA_DPLLB AC2 VCCADPLLB

VCCAPLLSATA U56 VCCAPLLSATA
VCCAPLLEXP B53 VCCAPLLEXP
VCCAFDIPLL C54 VCCAFDIPLL

PCH_1P05 R549 X_0/8
3VSB AV28 VCCSUSHDA
VCC3 AN52 VCCSPI
VCC1_8 R548 0/8
R2 VCCVRM_04
R54 VCCVRM_03
R56 VCCVRM_02
AJ1 VCCVRM_01

C427 1u/6.3V/4 DCPSUS A39 DCPSUS_03
TP43 AT41 DCPSUS_02
TP42 AA32 DCPSUS_01

C578 0.1u/10X DCPRTC BR54 DCPRTC
BT56 DCPRTC_NCTF

TP50 AV41 DCPSUSBYP

C520 0.1u/10X DCPSST BA46 DCPSST

3VA
C738 0.1u/10X
VBAT BU42 VCCRTC
AV40 VCCDSW3_3

PCH_1P05 AG15 VCCDIFFCLKN_03
AE17 VCCDIFFCLKN_02
AE15 VCCDIFFCLKN_01

PCH_1P05 CP5 X_COPPER VCCSSC
AE20 VCCSSC_02
AC20 VCCSSC_01

T67 VCCDFITERM
T55 VCCDFITERM
VCCNAND

AV20 VCC3_3_10
AU20 VCC3_3_09
AU22 VCC3_3_08
AN38 VCC3_3_07
AL38 VCC3_3_06
BD20 VCC3_3_05
BD17 VCC3_3_04
BC17 VCC3_3_03
AE57 VCC3_3_02
VCC3_3_01

VCC3

BT35 VCCSUS3_3_011
AU38 VCCSUS3_3_010
AT40 VCCSUS3_3_009
BA36 VCCSUS3_3_008
BK36 VCCSUS3_3_007
BJ36 VCCSUS3_3_006
AY33 VCCSUS3_3_005
AY31 VCCSUS3_3_004
AY32 VCCSUS3_3_003
AV30 VCCSUS3_3_002
U31 VCCSUS3_3_001

3VSB

VCC1_8 R554 0/6
VCC3 R558 X_0/6
VCCNAND
C454 X_0.1u/16Y

PCH_1P05

VCCCORE_022 AR34
VCCCORE_021 AR32
VCCCORE_020 AN34
VCCCORE_019 AN32
VCCCORE_018 AL34
VCCCORE_017 AL32
VCCCORE_016 AJ36
VCCCORE_015 AJ34
VCCCORE_014 AJ32
VCCCORE_013 AG34
VCCCORE_012 AG32
VCCCORE_011 AE36
VCCCORE_010 AE34
VCCCORE_009 AE32
VCCCORE_008 AE30
VCCCORE_007 AE28
VCCCORE_006 AE24
VCCCORE_005 AC32
VCCCORE_004 AC30
VCCCORE_003 AC28
VCCCORE_002 AC26
VCCCORE_001 AC24

VCCASW_023 AU36
VCCASW_022 AU30
VCCASW_021 AR38
VCCASW_020 AR36
VCCASW_019 AR30
VCCASW_018 AR28
VCCASW_017 AR26
VCCASW_016 AR24
VCCASW_015 AN28
VCCASW_014 AN26
VCCASW_013 AN24
VCCASW_012 AN22
VCCASW_011 AL28
VCCASW_010 AL24
VCCASW_009 AJ28
VCCASW_008 AJ26
VCCASW_007 AJ24
VCCASW_006 AG28
VCCASW_005 AG26
VCCASW_004 AG24
VCCASW_003 AU34
VCCASW_002 AV36
VCCASW_001 AU32

POWER

PCH_1P05: 7.66A
CPU_VTT: 0.058A
VCC1_8: 0.159A
VCC3: 0.697A
3VSB: 0.11A
5VREF: 0.001A
5VREF_SUS: 0.001A

5VREF & 5VREF_SUS Sequencing Circuit

VCC3 Q64 2N3904 B C E
C565 1u/6.3V/4
VCC5 R699 10/4 5VREF
C564 0.1u16X

3VSB Q69 2N3904 B C E
C605 0.1u16X
5VSB R780 100/4/1 5VREF_SUS
C597 0.1u16X

VCC3 CP4 X_COPPER +3.3V_DAC
Near ball AF1
C536 0.1u/10X

PCH decoupling cap

VBAT C604 C611 1uF/10V/Y5V/6 0.1u/16Y

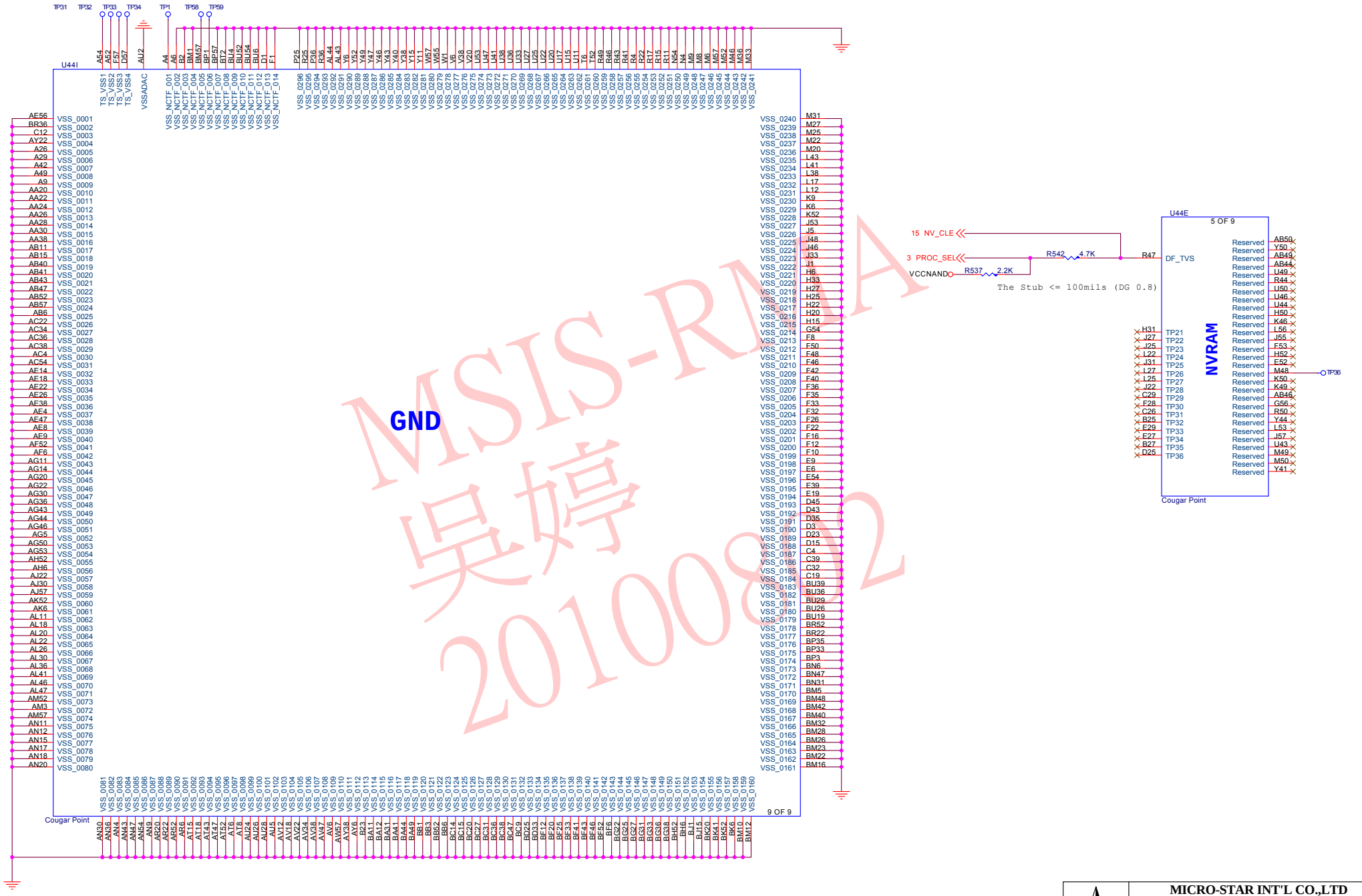
VCC3 C482 C575 C491 C431 C537 C594 C583 1uF/10V/Y5V/6
0.1u/16Y X_0.1u/16Y X_0.1u/16Y 0.1u/16Y 4.7uf/10V/X5R/8

CPU_VTT C412 C421 C429 0.1u/16Y 0.1u/16Y
4.7uf/10V/X5R/8

3VSB C586 C595 0.1u/16Y 0.1u/16Y

PCH_1P05 C729 C402 C411 C734 C410 C457 C735 C733 C731 C737 C736 C732 0.1u/16Y
10u6.3X8 1uF/10V/Y5V/6 10u6.3X8 1uF/10V/Y5V/6 4.7uf/10V/X5R/8 1uF/10V/Y5V/6 X_0.1u/16Y X_0.1u/16Y
1uF/10V/Y5V/6 10u6.3X8 10u6.3X8 0.1u/16Y

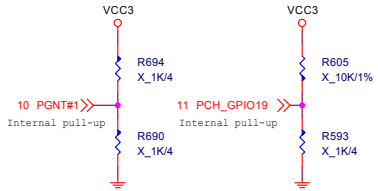
MICRO-STAR INT'L CO.,LTD
MS-7676
Size: Custom
Document Description: CP-POWER
Rev: 0C
Date: Monday, July 19, 2010
Sheet 13 of 47

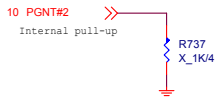


MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size: Custom	Document Description: CP-GND/NVRAM	Rev: 0C
Date: Monday, July 19, 2010	Sheet 14 of 47	

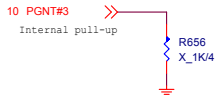
PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

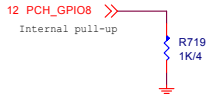




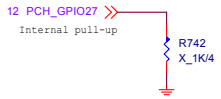
DMI AC/DC MODE
0 : AC
1 : DC *



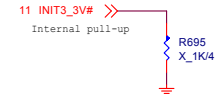
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

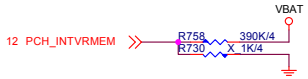


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ????????????????
1 : ???????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

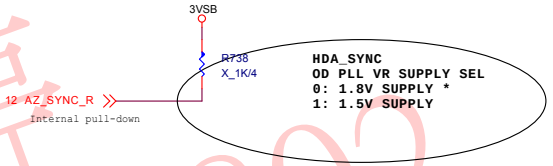
When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

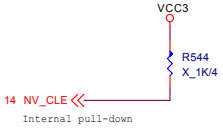
HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

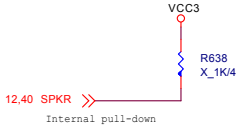


HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

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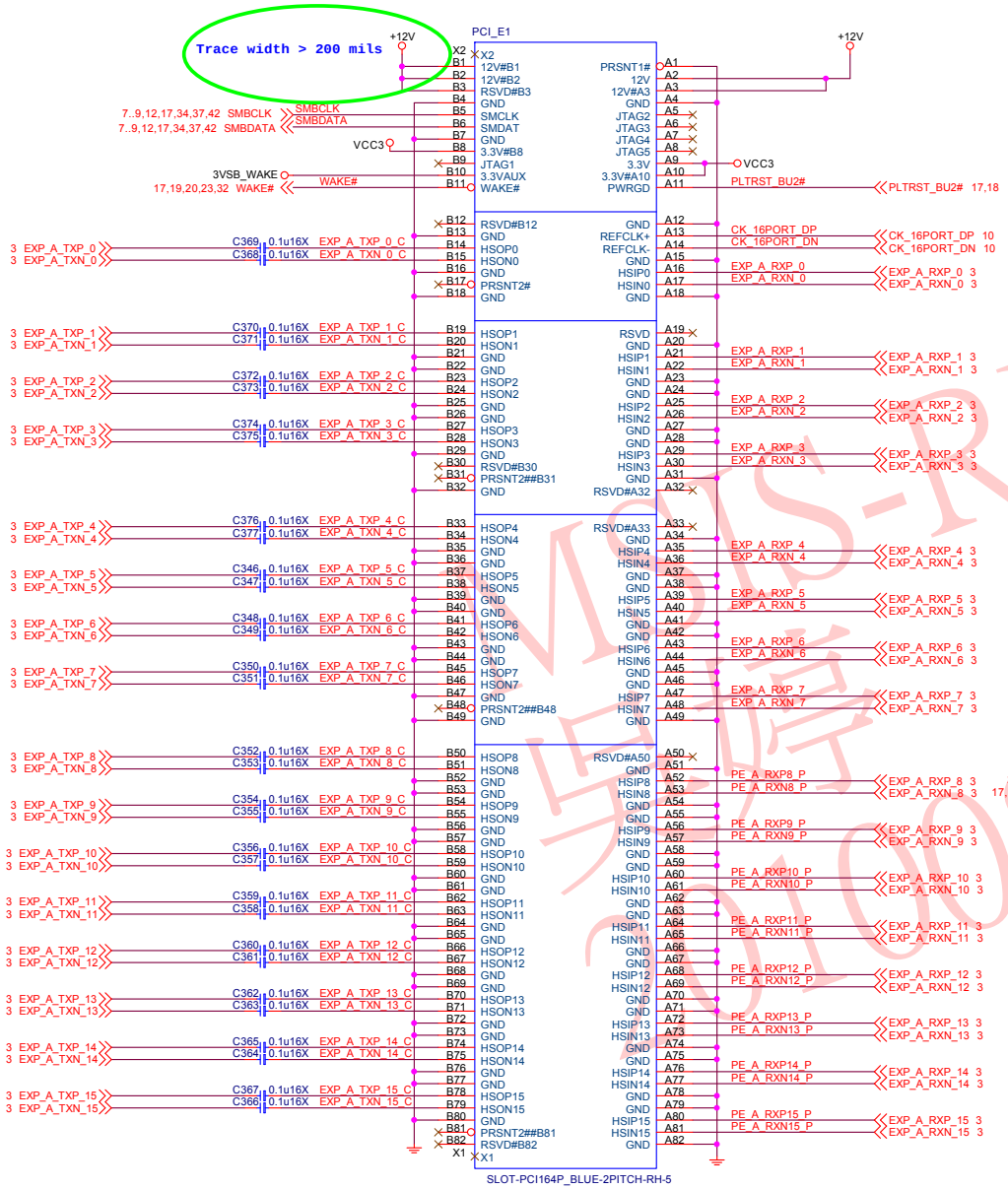
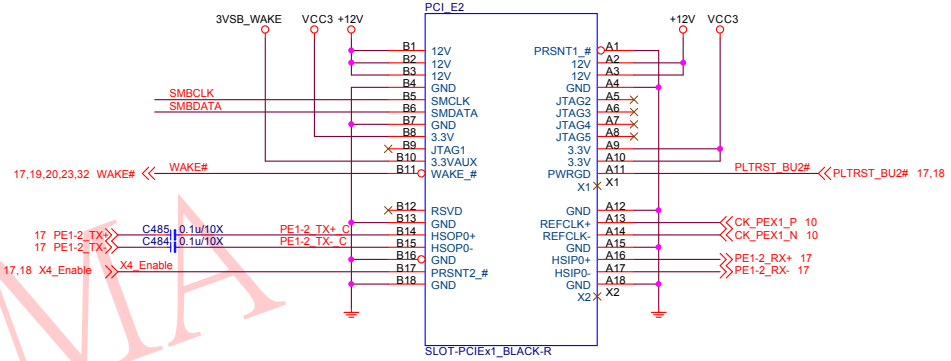
Date: Monday, July 19, 2010 | Sheet 15 of 47

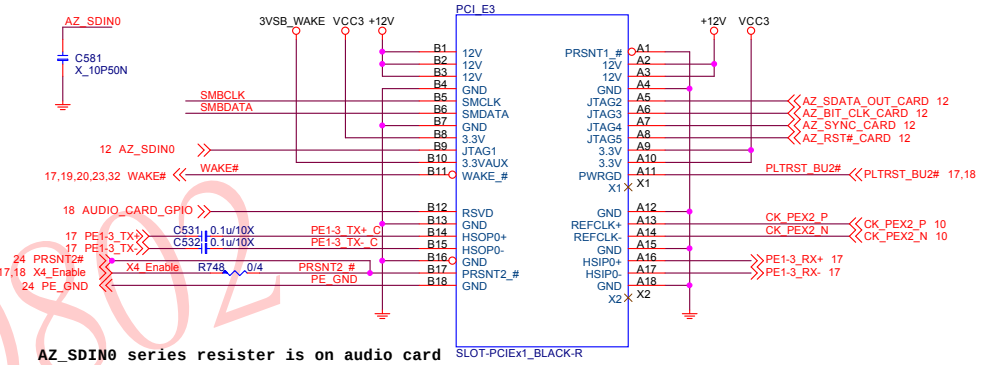
PCI_Express X16 Slot



PCI EXPRESS x1-PORT

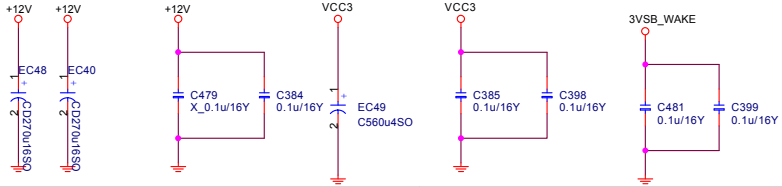


PCI EXPRESS x1-PORT



AZ_SDIN0 series resister is on audio card

AUDIO_CARD_GPIO
HI:LED OFF
LOW:LED ON



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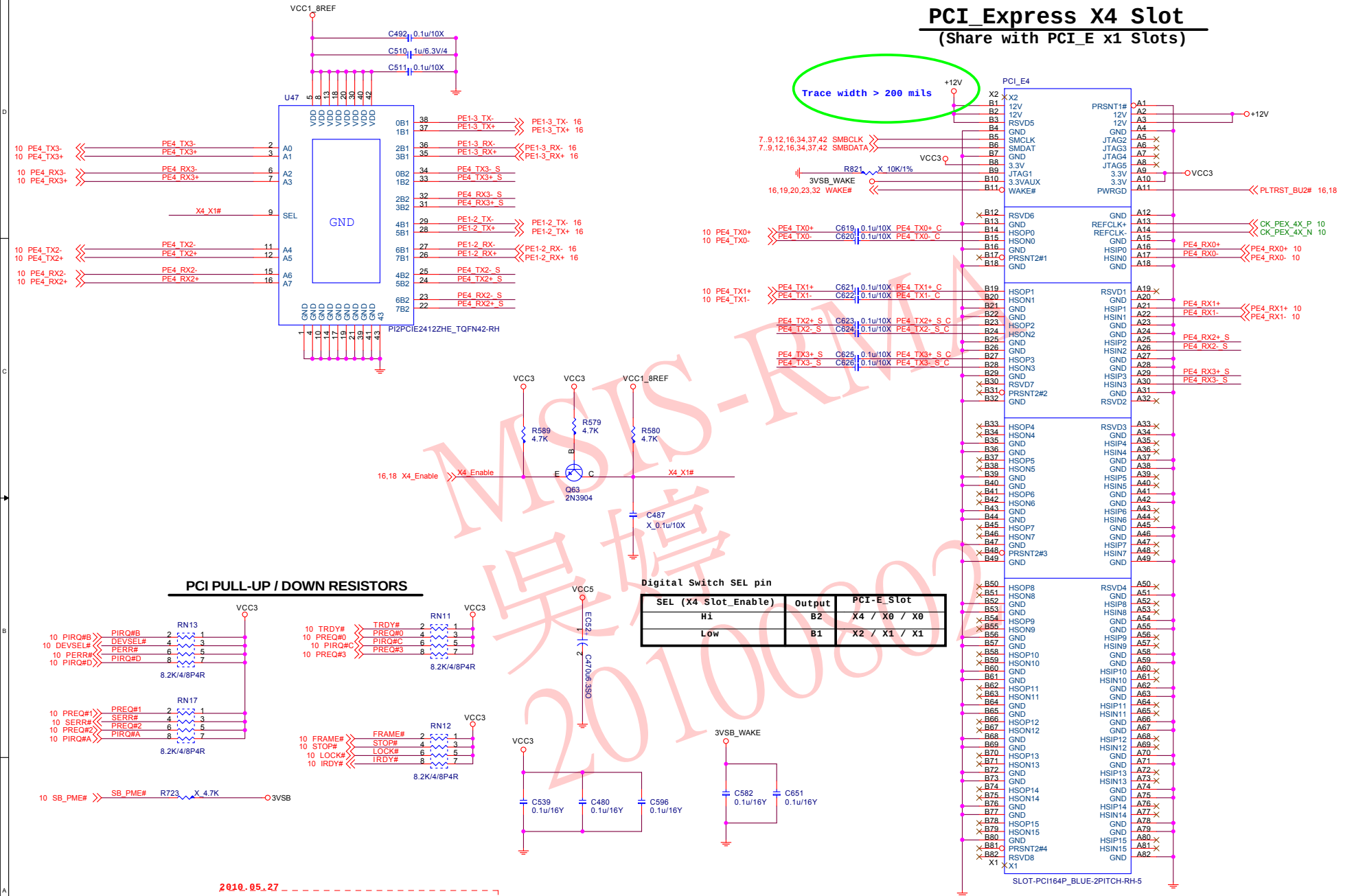
Size: Custom	Document Description: PCIE x16 /x1 /x1HDA CO-LAY	Rev: 0C
Date: Monday, July 19, 2010	Sheet 16 of 47	

PCI_Express X4 Slot
(Share with PCI_E x1 Slots)

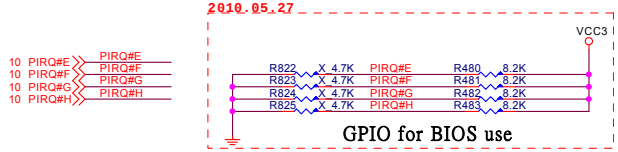


PCI PULL-UP / DOWN RESISTORS

Digital Switch SEL pin

SEL (X4 Slot_Enable)	Output	PCI-E_Slot
Hi	B2	X4 / X0 / X0
Low	B1	X2 / X1 / X1

2010.05.27



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Size: Custom | Document Description: PCIEx4 Slots | Rev: 0C

Date: Monday, July 19, 2010 | Sheet 17 of 47

SERIAL PORT 1

NO USE UART PORT2

Dual PS2 Connector

D1 always reserve

For EMI solution 2008-12-03

PS2 POWER

NEAR CONNECTOR

F71889AD

F71889AD-LAA-RH

87,86,85 :0.9V

Close pin out

LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
LDRQ#	PIN51~56=VID_OUT	PIN51~56=GPIO
DRRB#	SPI_Backup	SPI_Primary
RTSB#	PWM FAN	LINEAR FAN
RTSA#	80 Port DISABLE	80Port ENABLE

H : disable power
L : enable power

Pull down 47K:Pin 100-103 and pin 105-116 as GPIO pins

HW Monitor - Thermal

HW Monitor - Voltage

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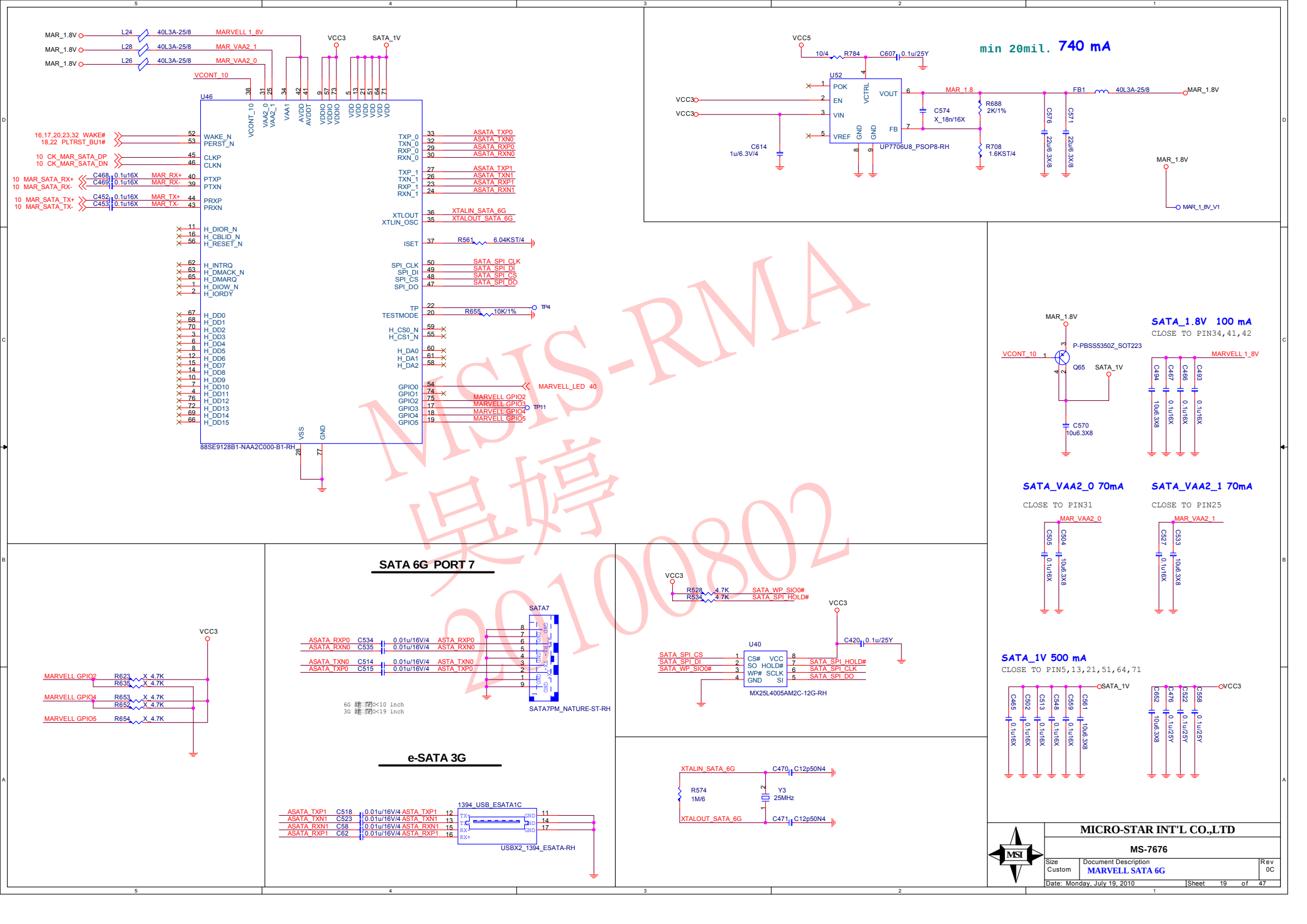
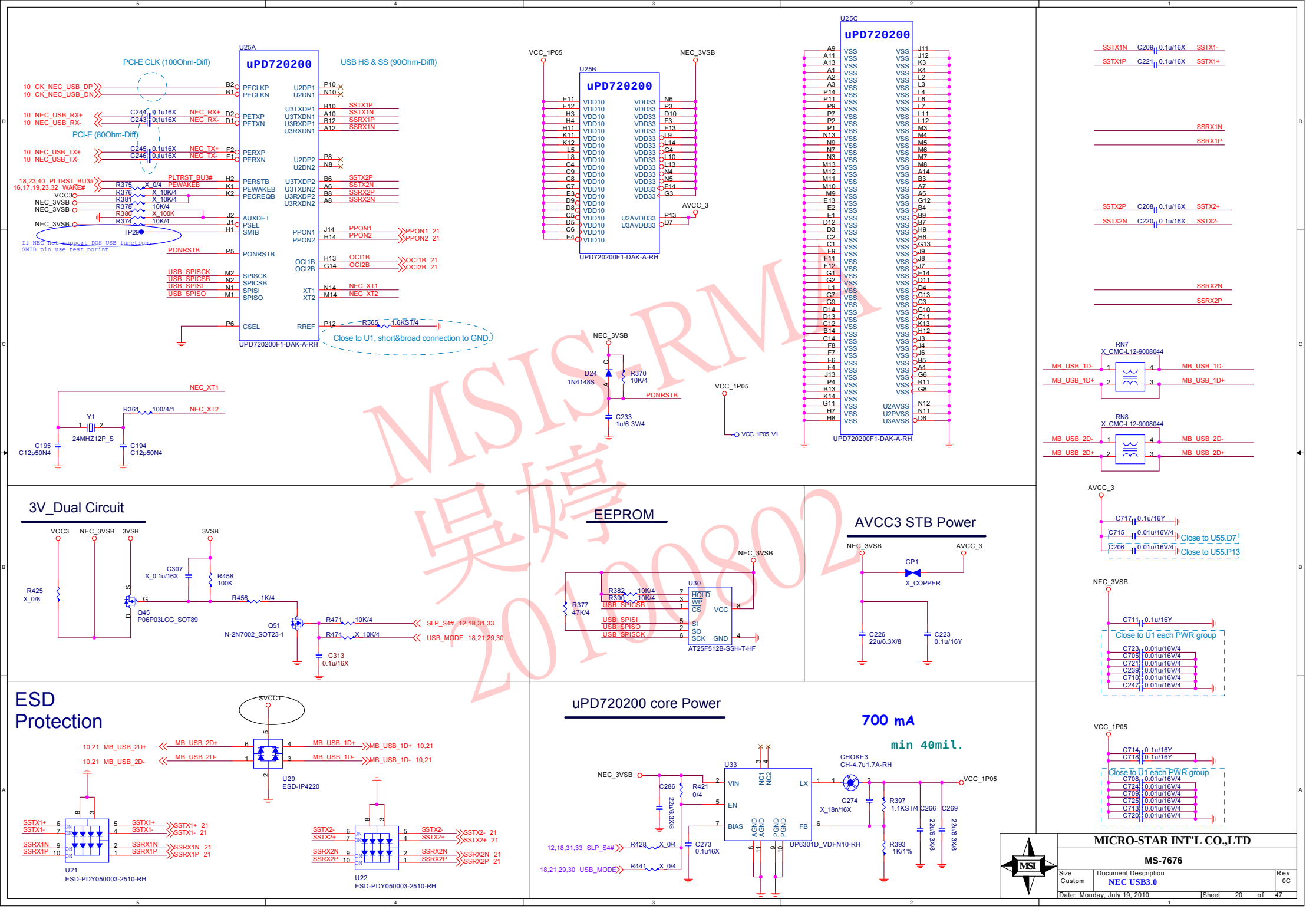
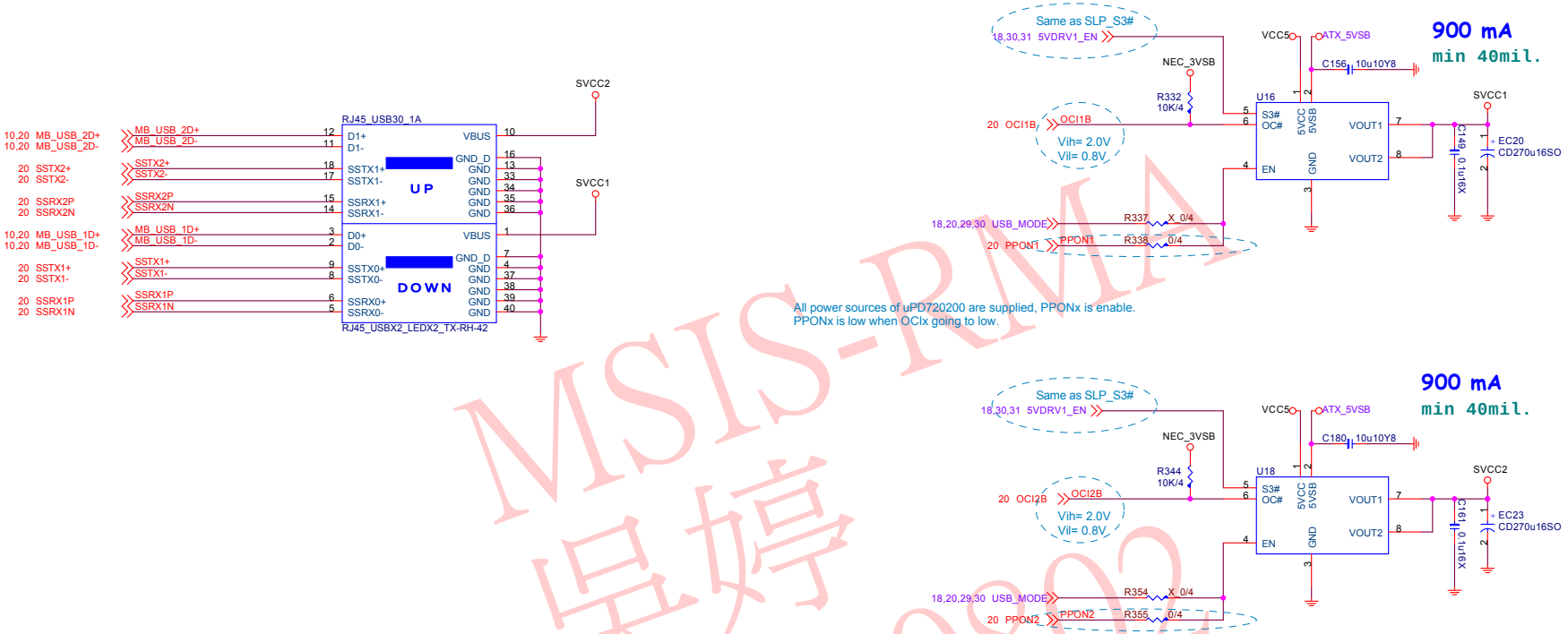
MS-7676	
Size: Custom	Document Description: SIO-Fintek F71889ED(EUP)
Date: Monday, July 19, 2010	Sheet 18 of 47







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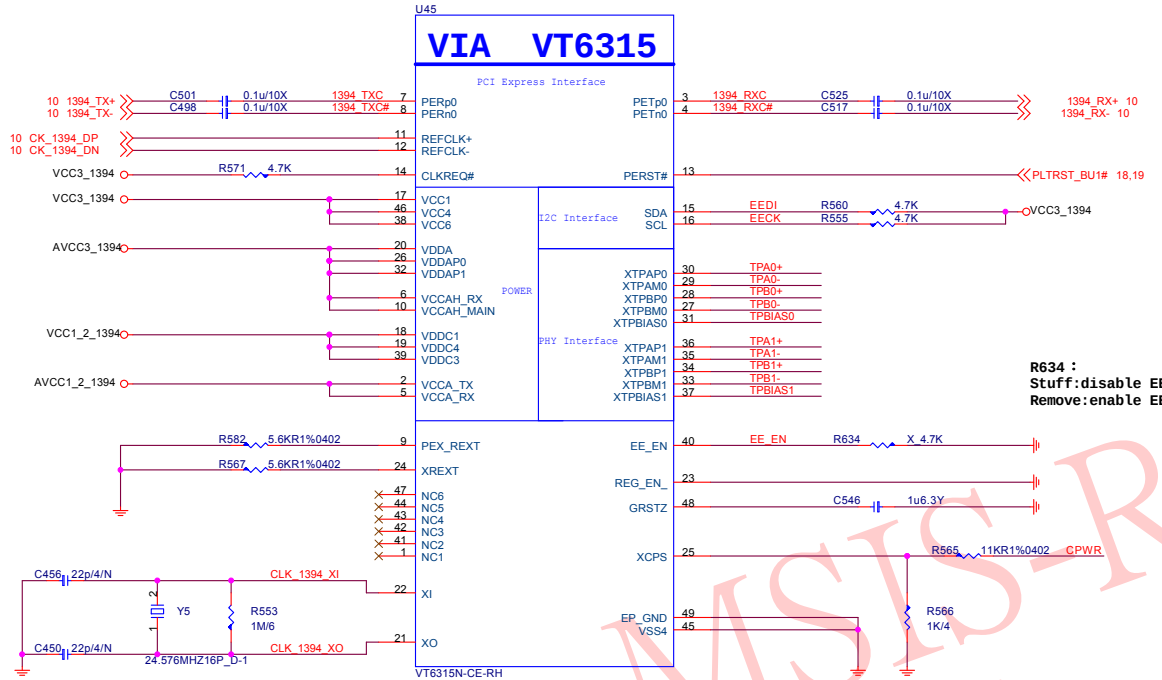
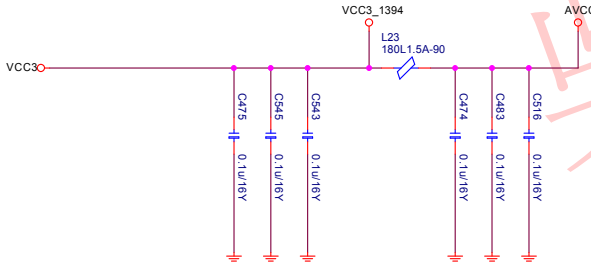
MS-7676		
Size: Custom	Document Description: NEC USB3.0 POWER & CONNECT	Rev: 0C
Date: Monday, July 19, 2010	Sheet 21 of 47	

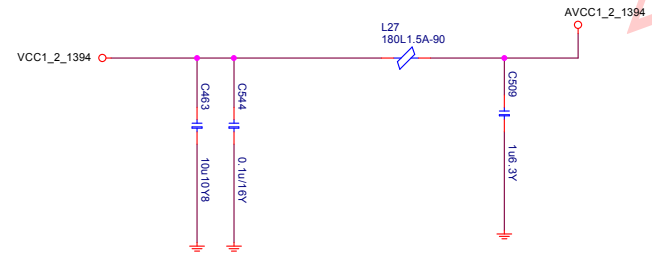
1394 CONTROLLER



R634 :
Stuff:disable EE PROM
Remove:enable EE PROM

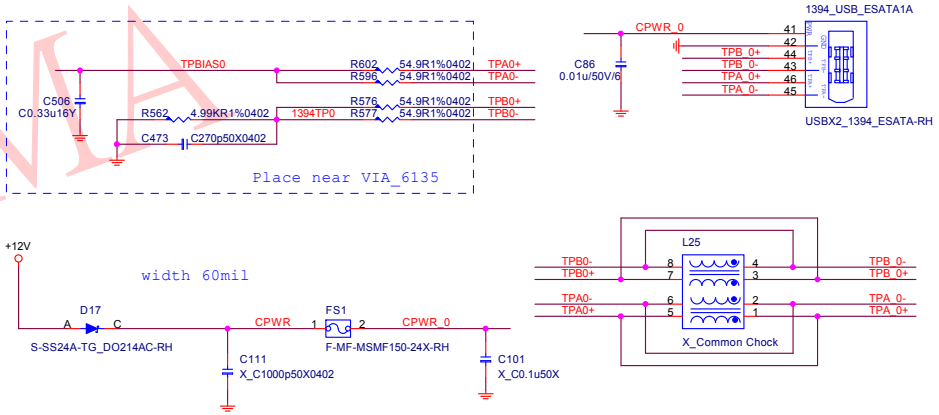


close to chip of all Cap.

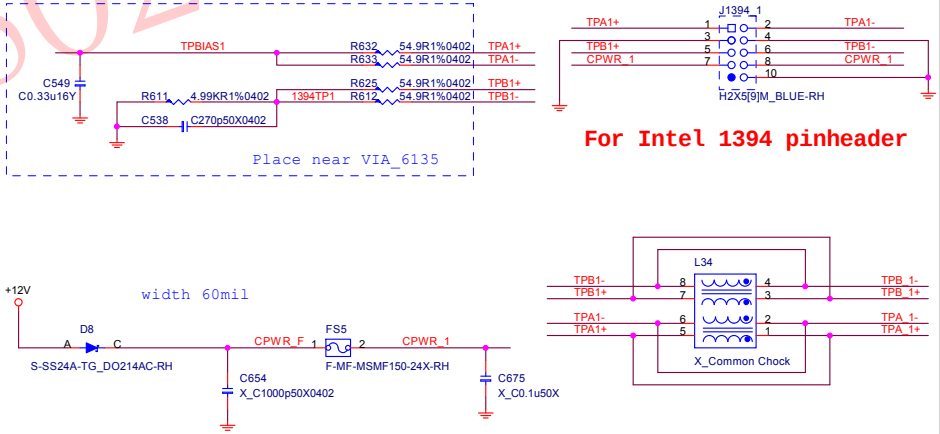


EE PROM

Rear 1394 port



Front 1394 pin header



For Intel 1394 pinheader

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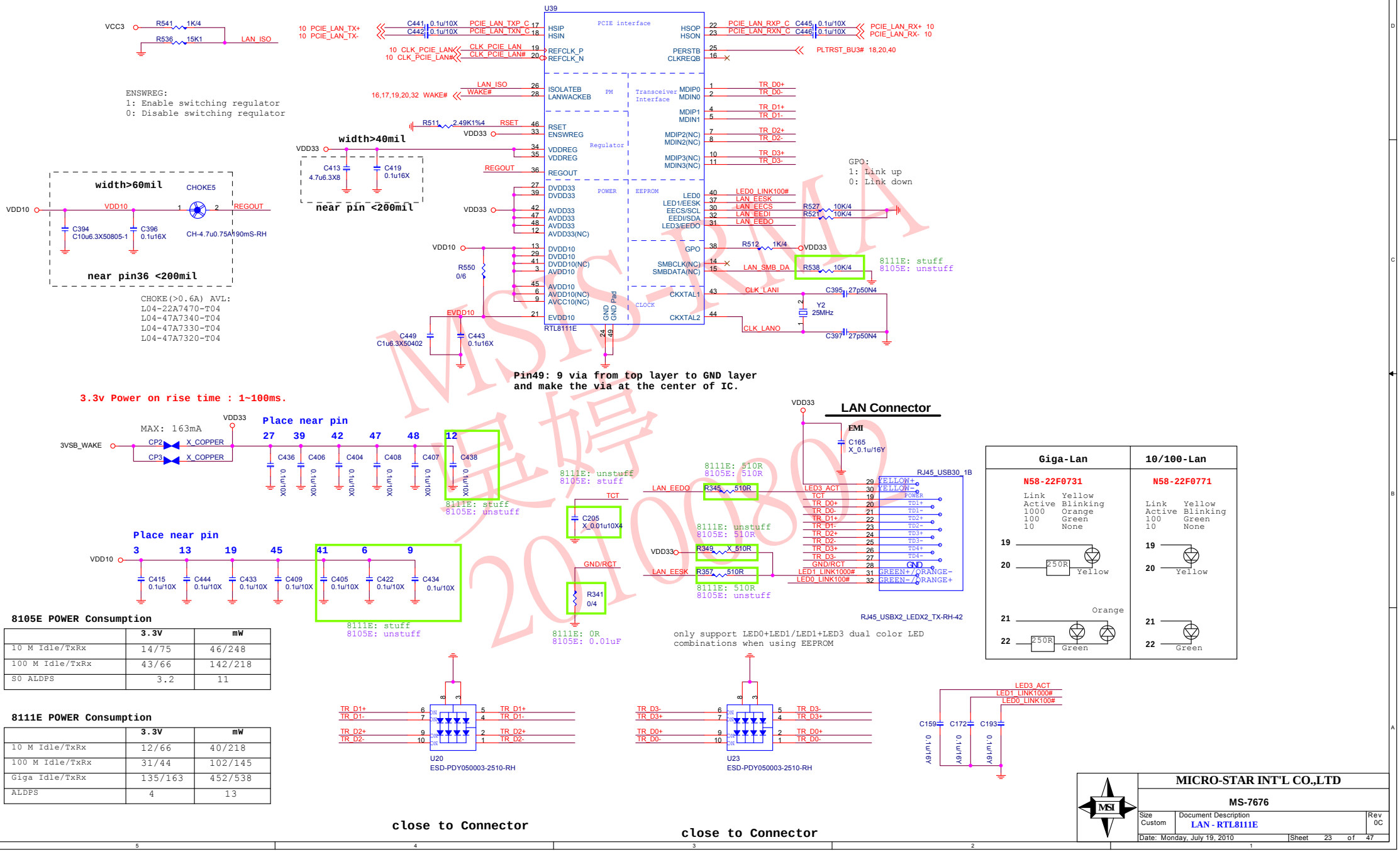
Size	Document Description	Rev
Custom	1394 Controller - VT6315N-CE	0C

Date: Monday, July 19, 2010 Sheet 22 of 47

RTL8111E Giga LAN

RTL8105E 10/100M LAN



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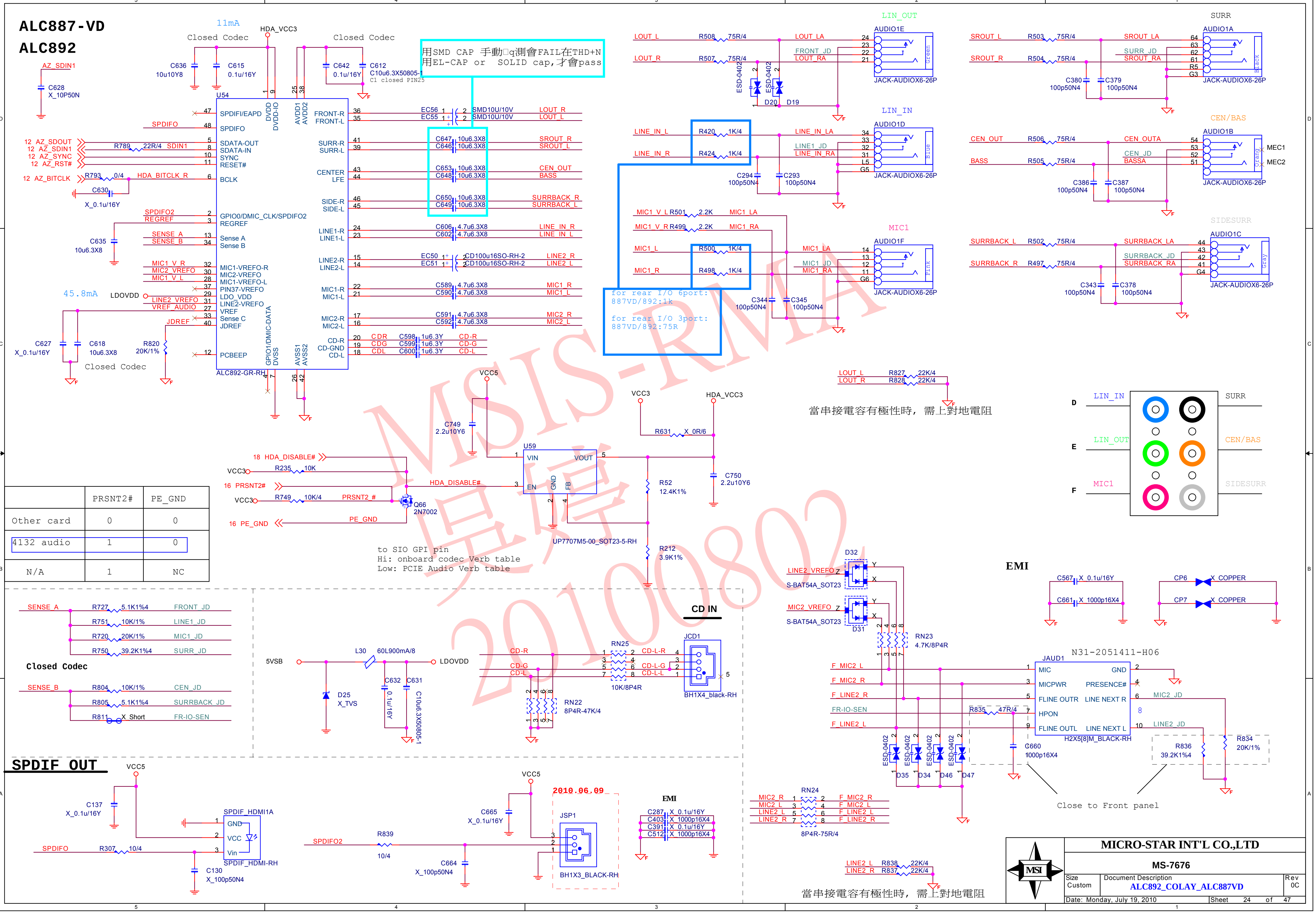
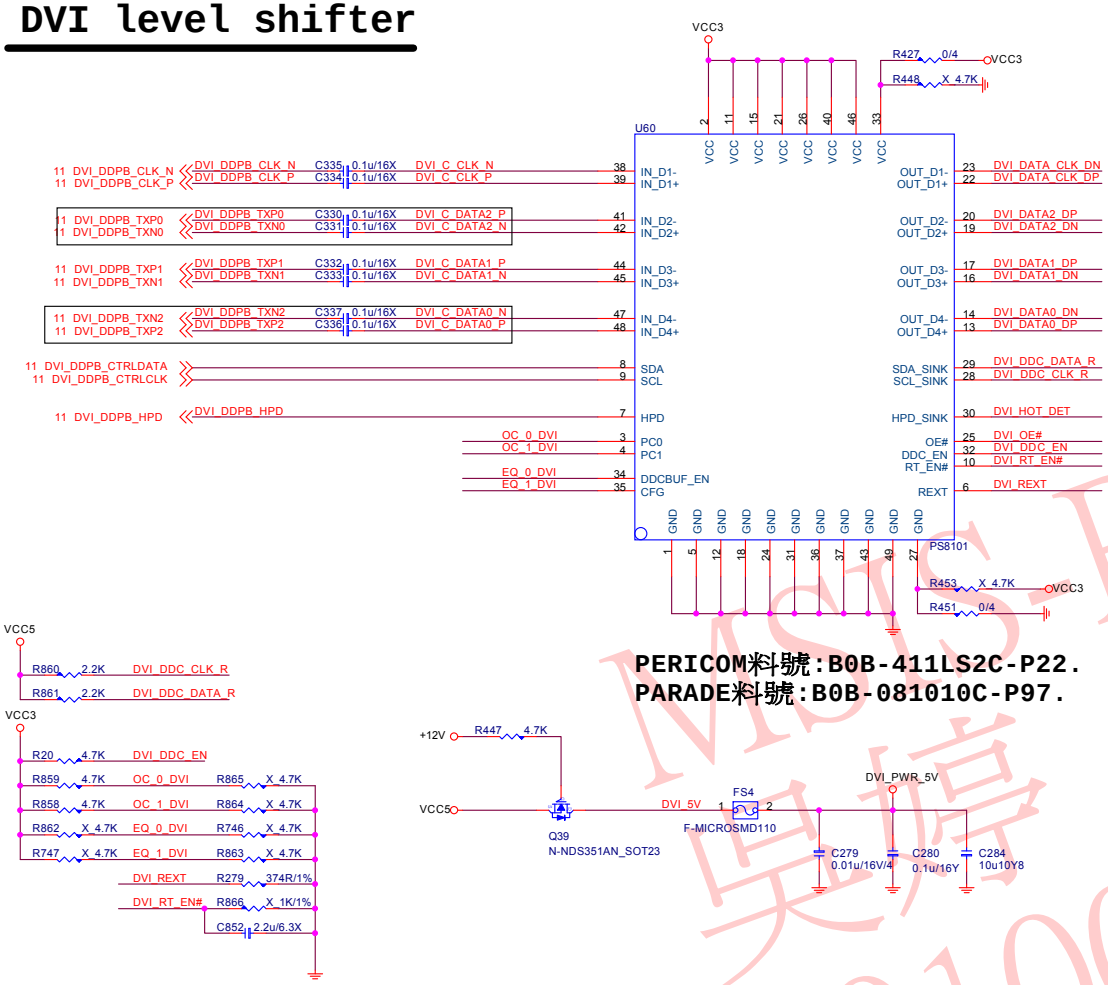
MS-7676		
Size: Custom	Document Description: LAN - RTL8111E	Rev: 0C
Date: Monday, July 19, 2010	Sheet 23 of 47	



ALC887-VD
ALC892
Closed Codec
11mA
HDA_VCC3
U54
ALC892-GR-RH
用SMD CAP 手動□q測會FAIL在THD+N
用EL-CAP or SOLID cap,才會pass
45.8mA
LDOVDD
LIN_OUT
AUDIO1E
JACK-AUDIOX6-26P
LIN_IN
AUDIO1D
MIC1
AUDIO1F
SURR
AUDIO1A
CEN/BAS
AUDIO1B
SIDESURR
AUDIO1C
for rear I/O 6port: 887VD/892:1k
for rear I/O 3port: 887VD/892:75R
當串接電容有極性時, 需上對地電阻
U59
UP7707M5-00_SOT23-5-RH
to SIO GPI pin
Hi: onboard codec Verb table
Low: PCIE Audio Verb table
EMI
CD IN
JCD1
BH1X4_black-RH
N31-2051411-H06
JAUD1
H2X5[8]M_BLACK-RH
Close to Front panel
SPDIF OUT
SPDIF_HDMI1A
SPDIF_HDMI-RH
JSP1
BH1X3_BLACK-RH
2010.06.09
MICRO-STAR INT'L CO.,LTD
MS-7676
Size Custom
Document Description ALC892_COLAY_ALC887VD
Rev 0C
Date: Monday, July 19, 2010
Sheet 24 of 47

	PRSNT2#	PE_GND
Other card	0	0
4132 audio	1	0
N/A	1	NC

DVI level shifter

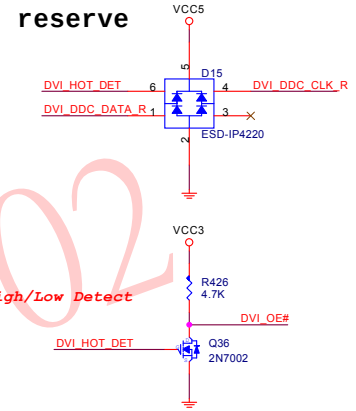


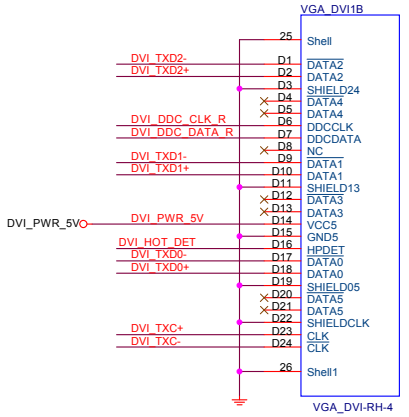
PERICOM料號:B0B-411LS2C-P22.
PARADE料號:B0B-081010C-P97.

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	

reserve



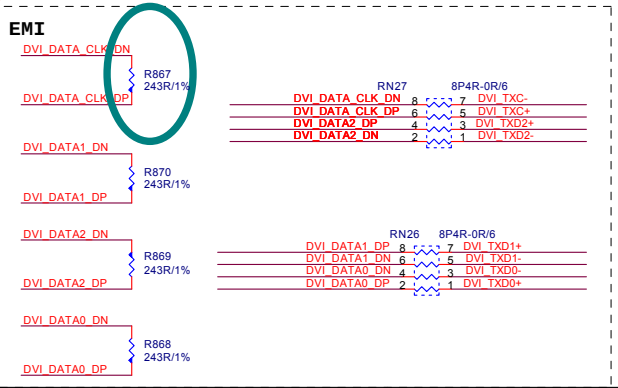


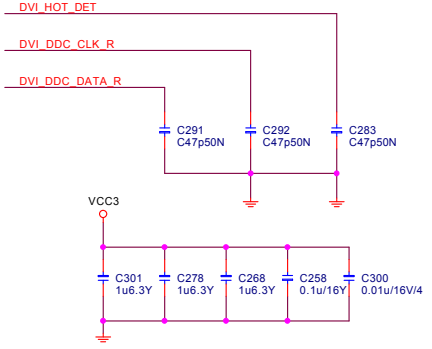
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

EMI





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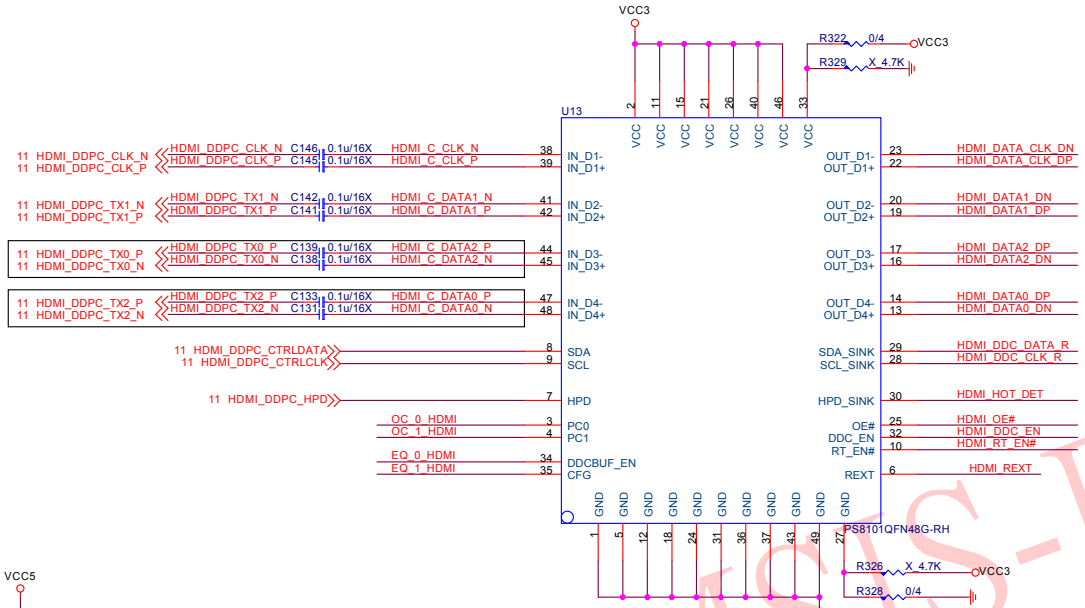
MS-7676

Size	Document Description	Rev
Custom	DVI transfer	0C

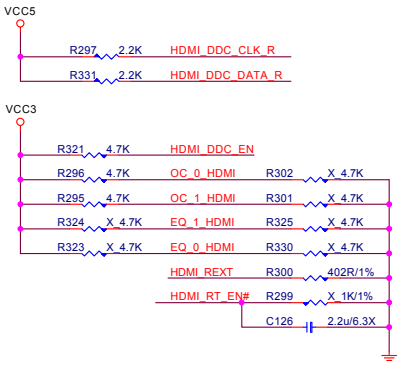
Date: Monday, July 19, 2010 Sheet 25 of 47

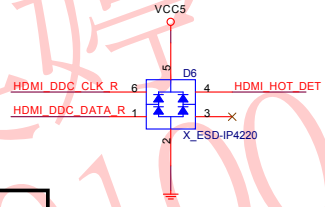
HDMI level shifter



PERICOM料號:B0B-411LS2C-P22.
PARADE料號:B0B-081010C-P97.

reserve



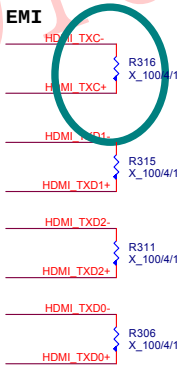


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

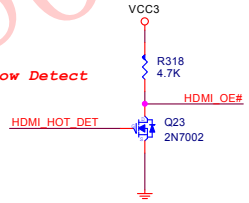
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

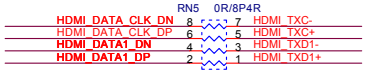
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

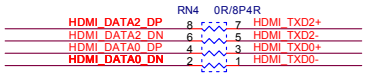
EMI

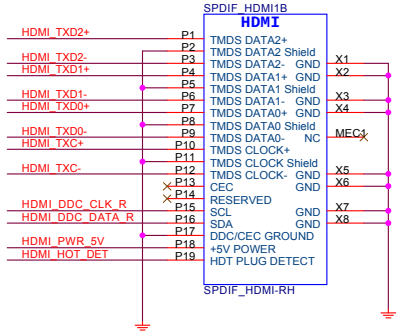


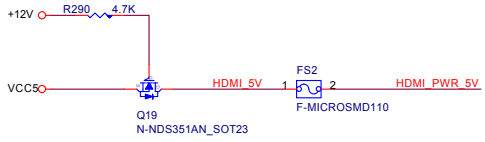
注 NHigh/Low Detect

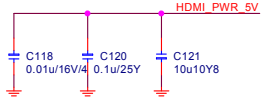












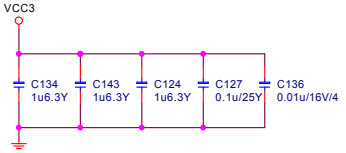


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	

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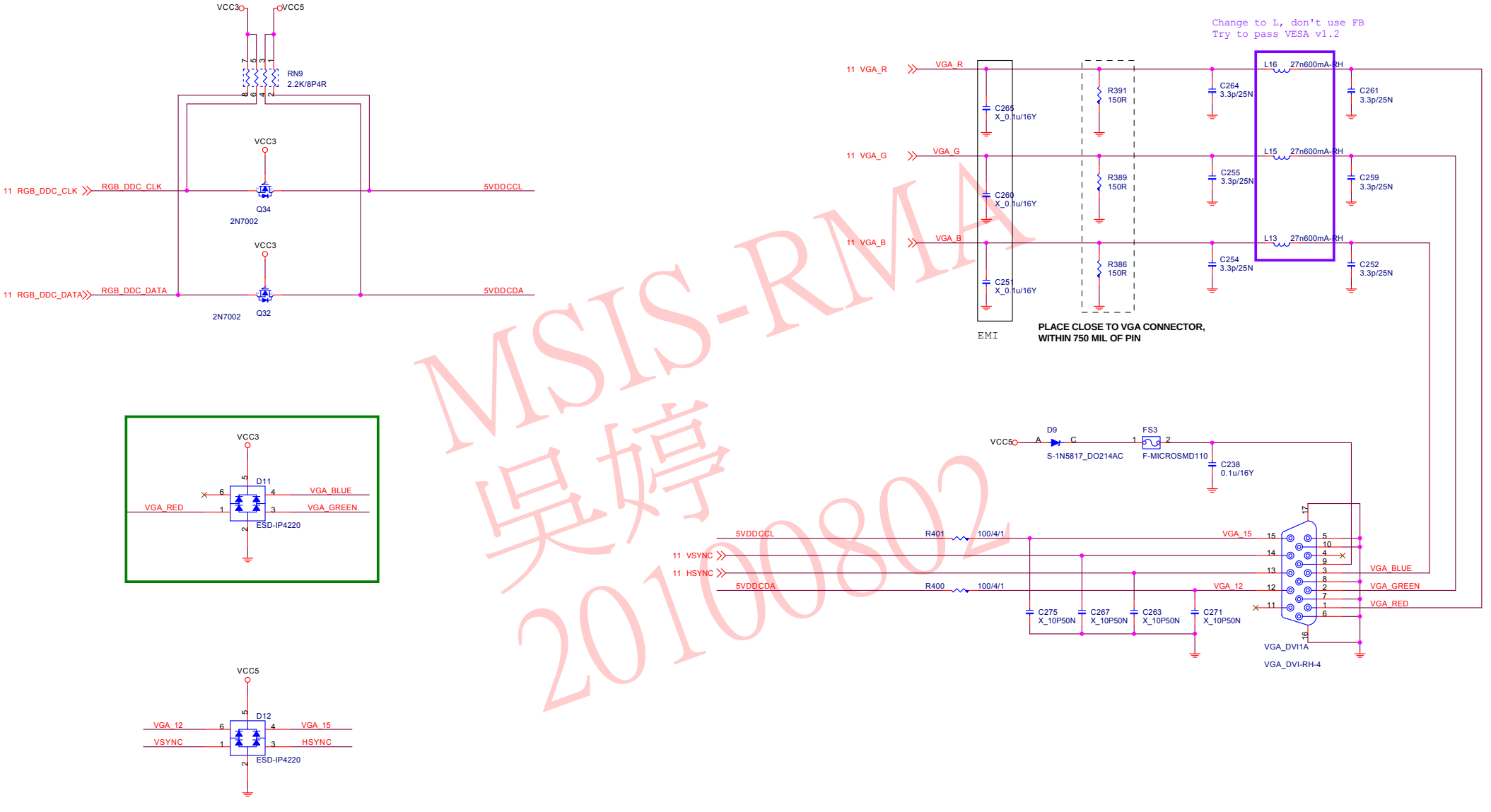
Size: Custom | Document Description: HDMI | Rev: 0C

Date: Monday, July 19, 2010 | Sheet 26 of 47

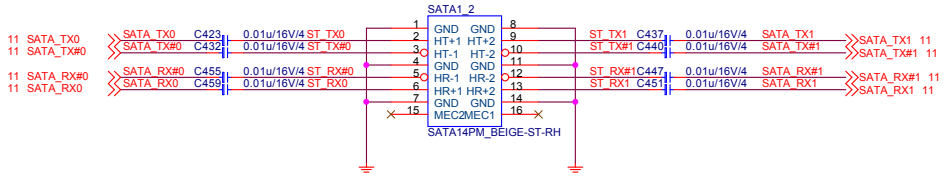
D-Sub

Level shift

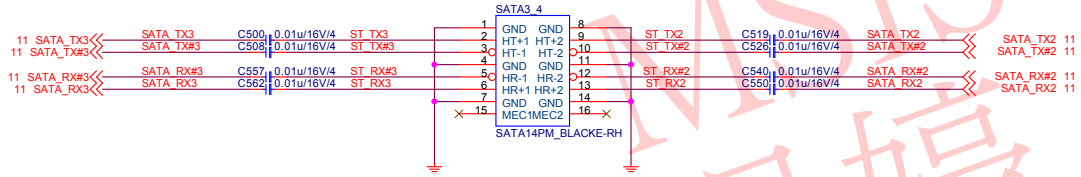


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7676	
Size: Custom	Document Description: VGA	Rev: 0C
Date: Monday, July 19, 2010	Sheet 27 of 47	

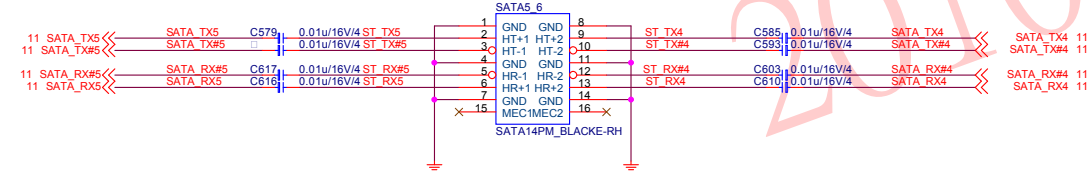
SATA 6G PORT 0,1



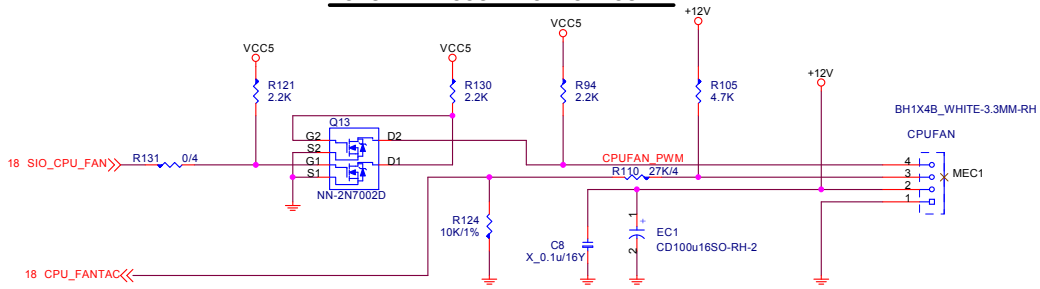
SATA 3G PORT 2,3



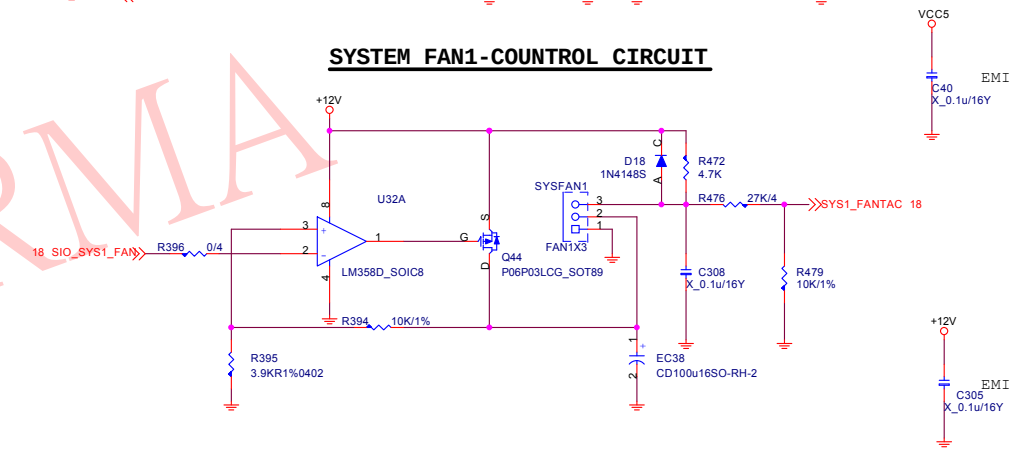
SATA 3G PORT 4,5



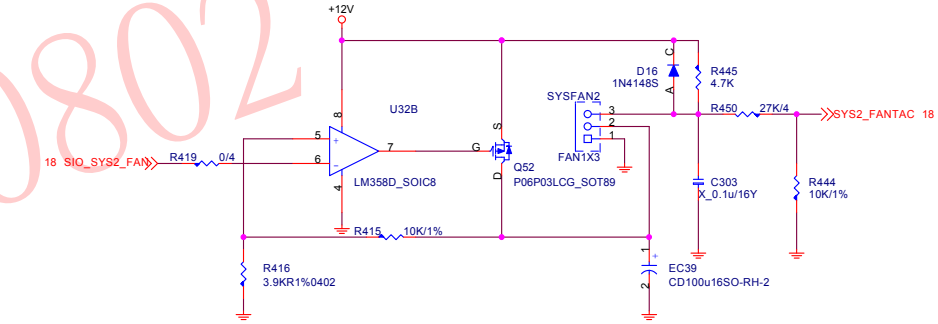
CPU FAN-COUNTROL CIRCUIT



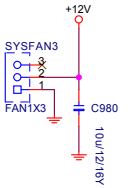
SYSTEM FAN1-COUNTROL CIRCUIT



SYSTEM FAN2-COUNTROL CIRCUIT



SYSTEM FAN3-12V



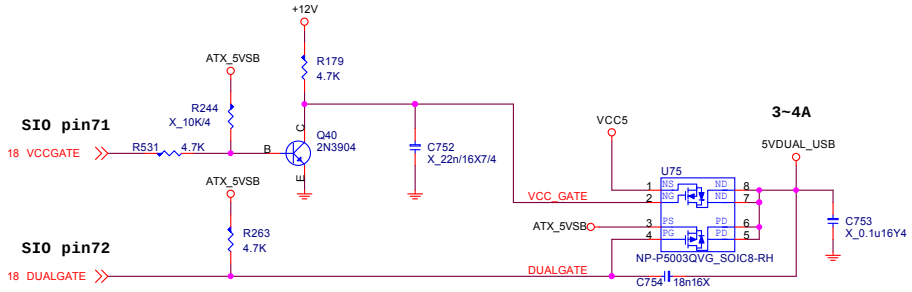
MICRO-STAR INT'L CO.,LTD

MS-7676

Size	Document Description	Rev
Custom	SATA / FAN Control	0C

Date: Monday, July 19, 2010 Sheet 28 of 47

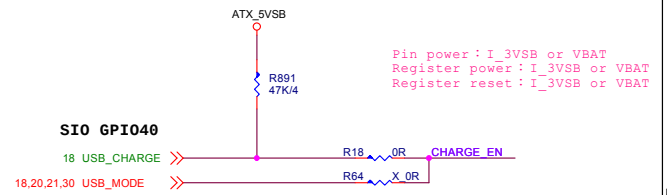
5VDUAL_USB



SIO GPIO040 Pin7 (VBAT for New F71889AD)

USB_CHARGE: (OD)
0: Don't support USB charge and resume.
1: Support USB charge and resume.

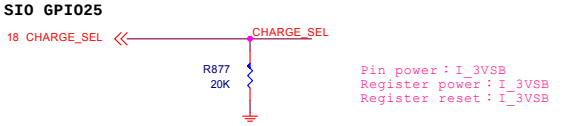
1st boot , H/W default support USB charge.



SIO GPIO025 (I_VSB3V)

CHARGE_SEL: (PUSH PULL)
0: Support i charge but don't support usb link and resume.
1: Don't support i charge but support usb link and resume.

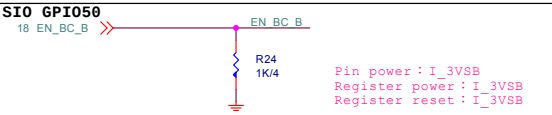
1st boot , H/W default support i charge.



SIO GPIO050 (I_VSB3V)

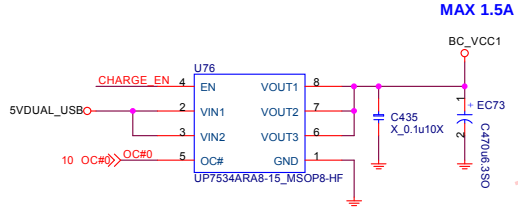
BC_SEL: (PUSH PULL)
0: Support DCP device(don't support usb link and resume)
1: Support CDP (Support usb link and resume)

1st boot , H/W default support DCP.



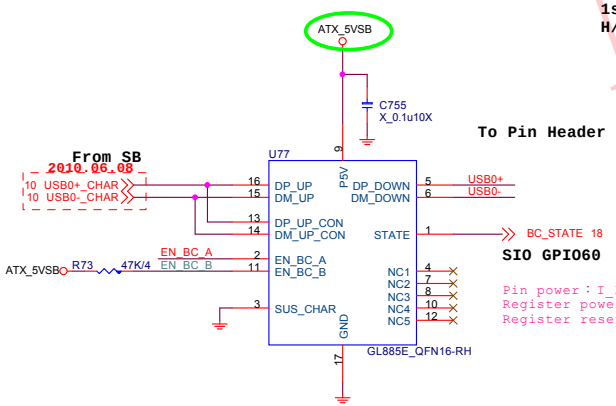
USB POWER FOR PORT 0 for Battery Charging

MAX 1.5A



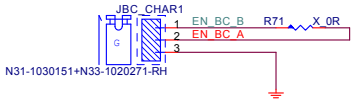
SIO GPIO pin51
Default Hi
HI= support USB charge

1st boot,
H/W default support USB charge

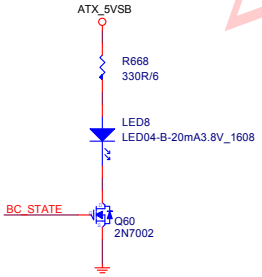


To Pin Header

Pin power : I_3VSB or VCC3
Register power : I_3VSB or VCC3
Register reset : I_3VSB or LRESET#



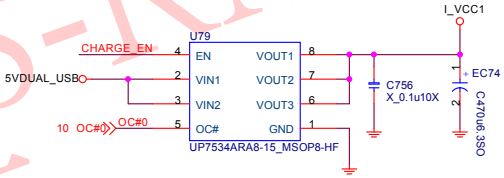
I CHARGE SELECT JUMPER JBC_CHAR1	
1 - 2	By Bios
2 - 3	NORMAL

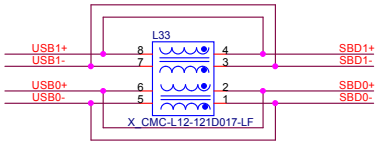


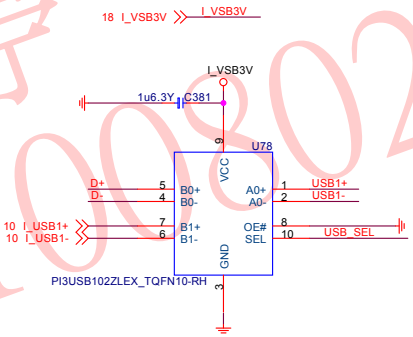
LED on when
battery charging

USB POWER FOR PORT 1 for I charge

MAX 1.7A

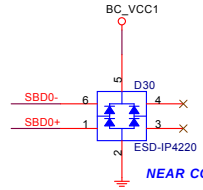






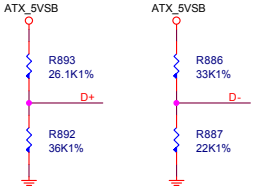
SIO GPIO pin 15
Default low
LOW= support I charge

1st boot H/W default support i charge

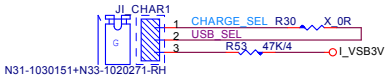


NEAR CONNECTOR

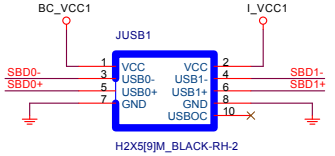
PI3USB102 has internal EDS diode.



D+ pull High 2.75 V，
D- pull High 2.05V。
皆可對 i-Pad / i-Phone / i-Pod進行充電。



I CHARGE SELECT JUMPER JI_CHAR1	
1 - 2	By Bios
2 - 3	I Charge



MICRO-STAR INT'L CO.,LTD

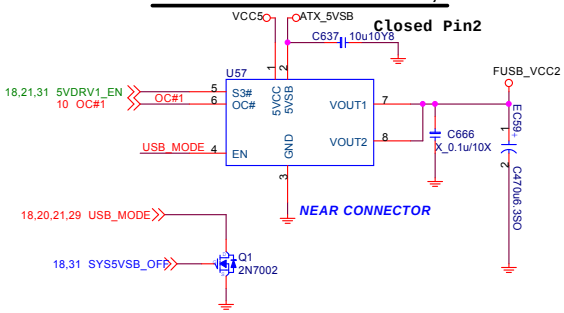
MS-7676

Size	Document Description	Rev
Custom	USB Charger	0C

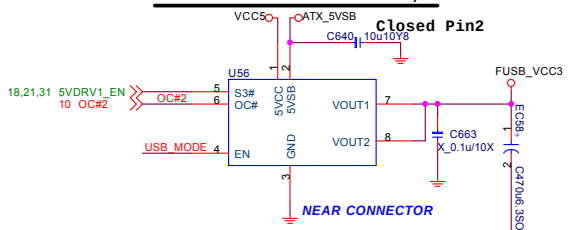
Date: Monday, July 19, 2010 | Sheet 29 of 47

Front USB Connector

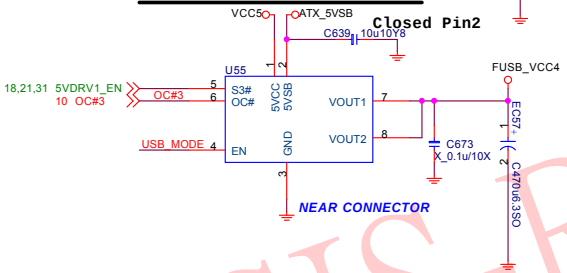
USB POWER REAL PORT 2,3



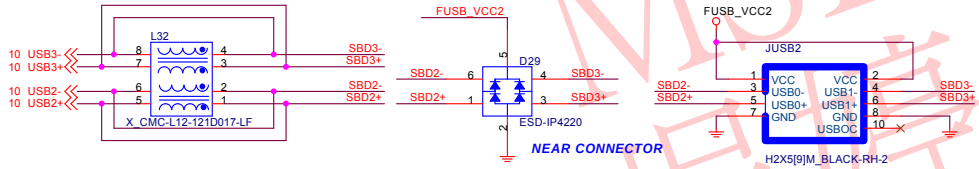
USB POWER FOR PORT 4,5



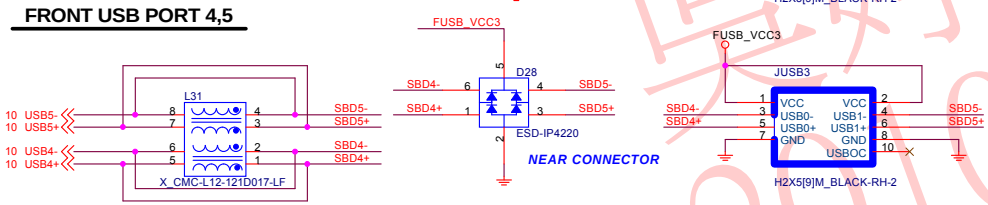
USB POWER FOR PORT 6,7



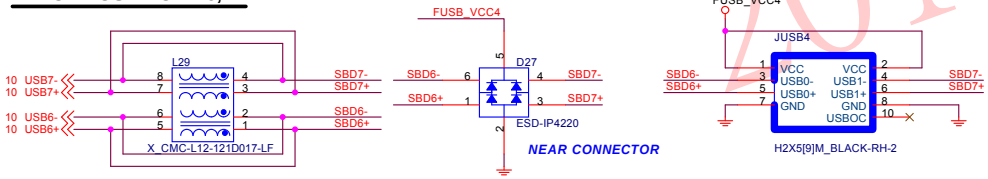
FRONT USB PORT 2,3



FRONT USB PORT 4,5

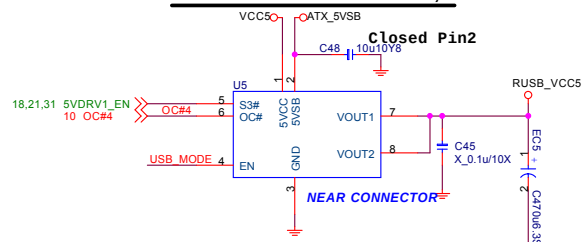


FRONT USB PORT 6,7

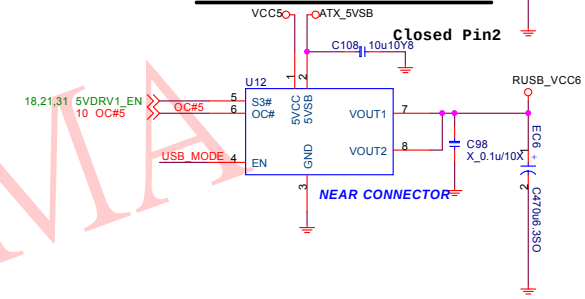


Rear USB Connector

USB POWER FOR PORT 6,7

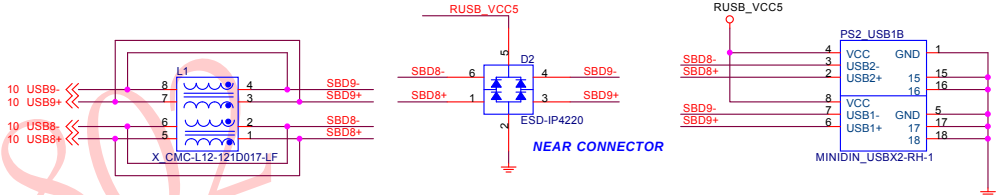


USB POWER FOR PORT 8,9

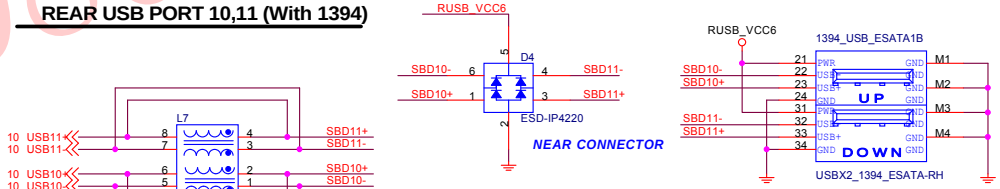


USB_MODE for USB voltage
H:Follow 5VSB
L:Always off

REAR USB PORT 8,9 (With PS2)



REAR USB PORT 10,11 (With 1394)



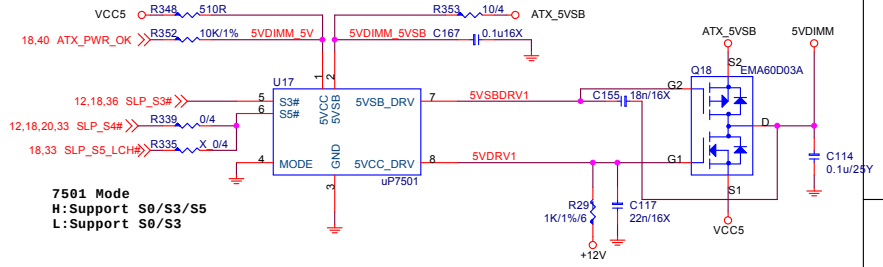
MICRO-STAR INT'L CO.,LTD

MS-7676

Size	Document Description	Rev
Custom	USB Connector	0C

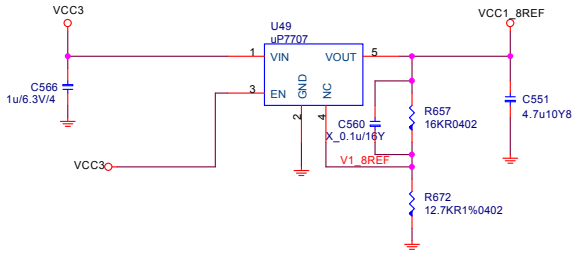
Date: Monday, July 19, 2010 Sheet 30 of 47

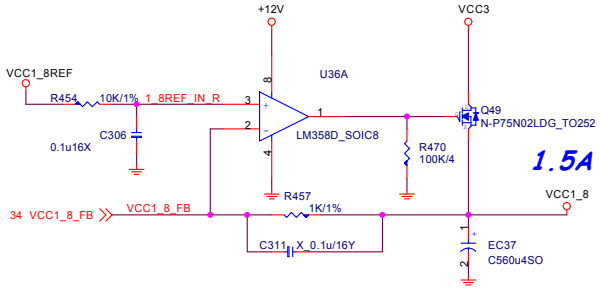
5VDIMM FOR DDR



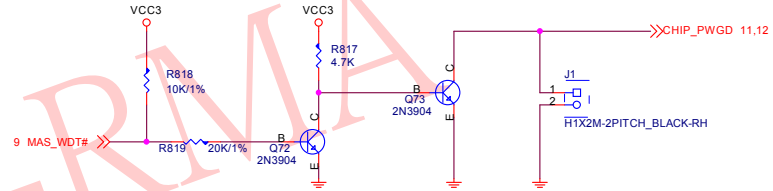
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

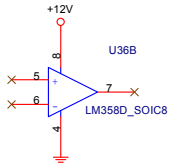
VCC1_8REF



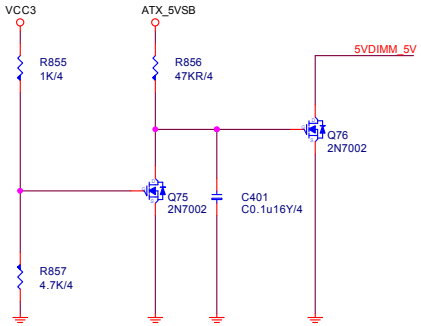


WATCH DOG

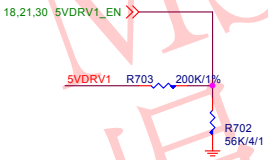




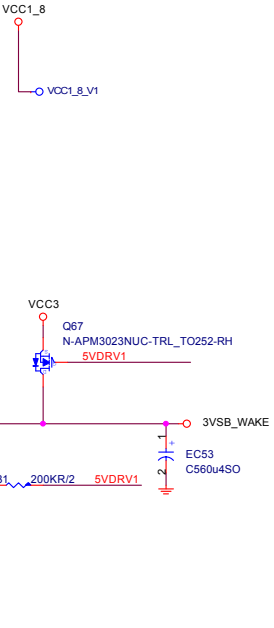
Patch COOLERMASTER 700W POWER Sequence



USB MODE

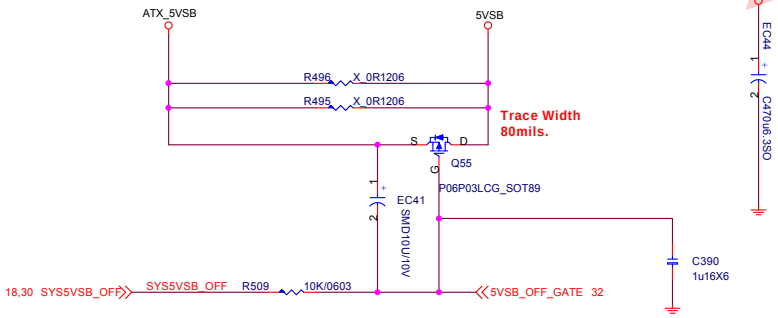


3VSB_WAKE



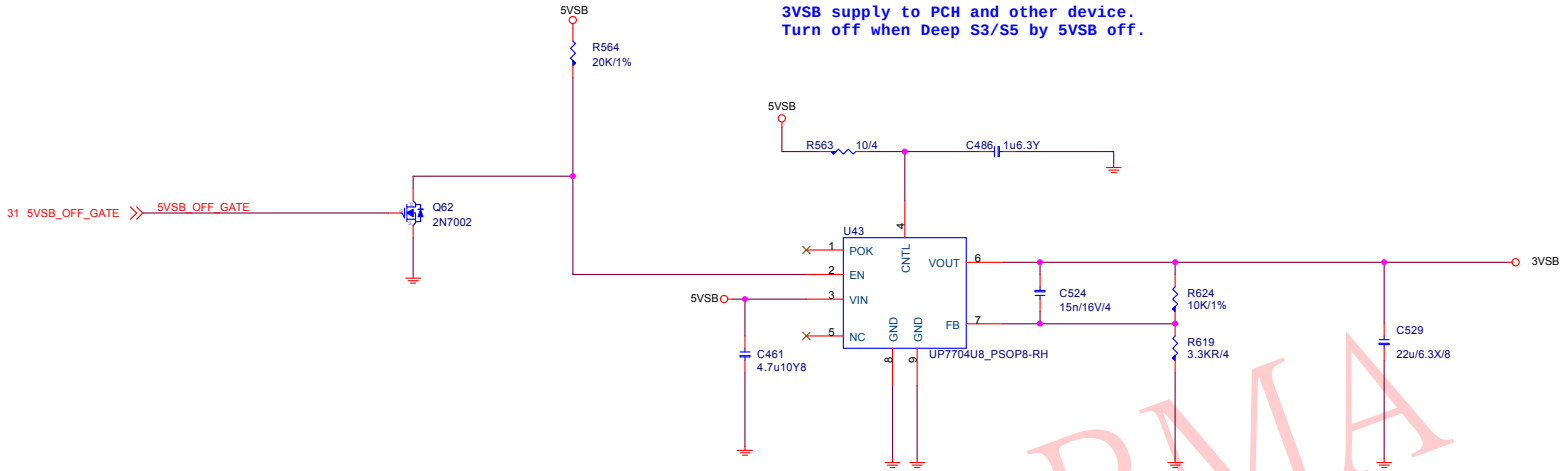
3VSB supply to PCH and other device. Turn off when Deep S3/S5.
+3VSB_WAKE supply to PCI Slot and LAN power.Turn off when Deep S3/S5 w/o WOL.

5VSB Power Switch

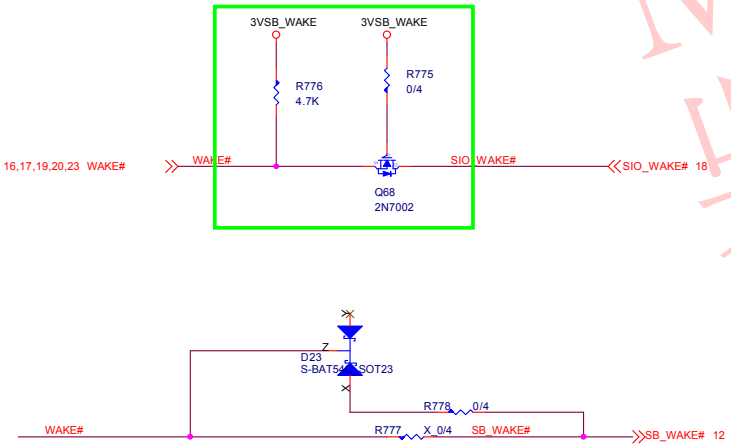


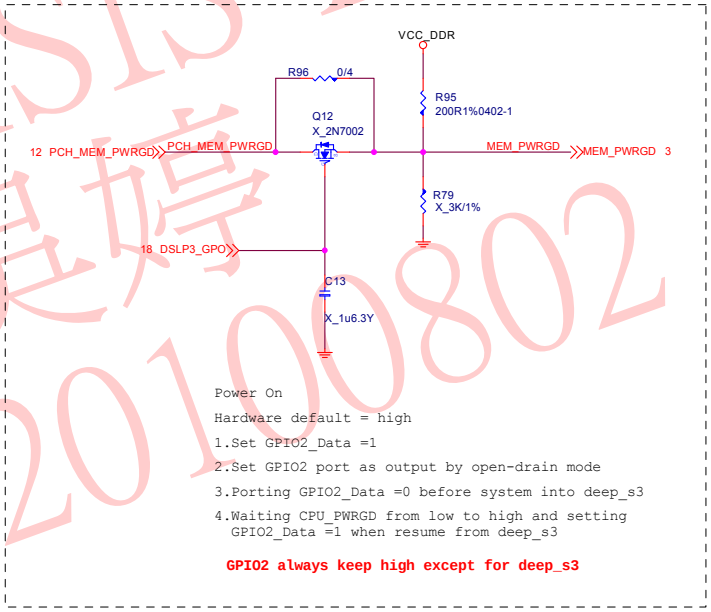
MICRO-STAR INT'L CO.,LTD	
MS-7676	
Size: Custom	Document Description: ACPI controller UPI
Rev: 0C	
Date: Monday, July 19, 2010	Sheet 31 of 47

Deep Mode WOL LAN Power CTRL Circuit

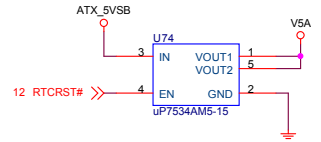


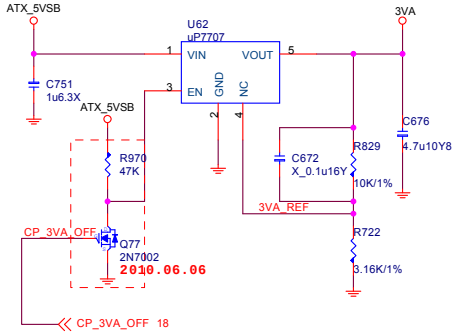
LAN/PCIE/PCI Wake Up CTRL Circuit





RTCRST patch circuit for clr-CMOS PCH will wake up issue





MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size: Custom	Document Description: Power Saving circuit	Rev: 0C
Date: Monday, July 19, 2010	Sheet 32 of 47	

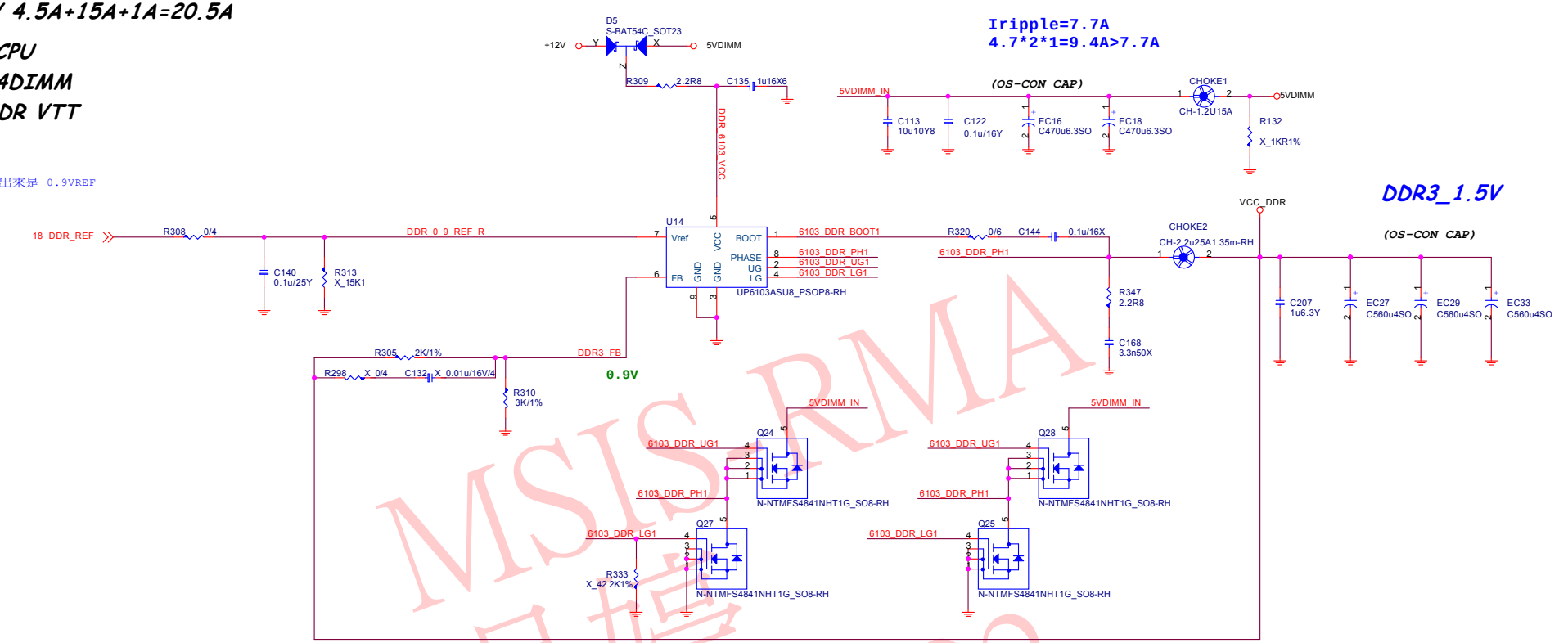
DDR Power:1.5V

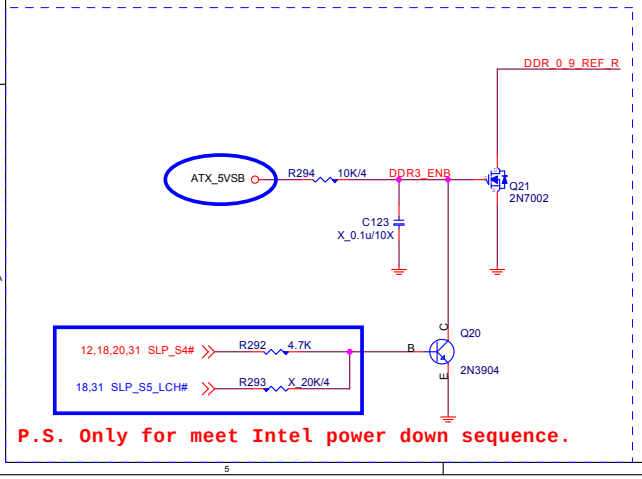
DDR3_1.5V 4.5A+15A+1A=20.5A

4.5A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

SIO 出來是 0.9VREF

Iripple=7.7A
4.7*2*1=9.4A>7.7A

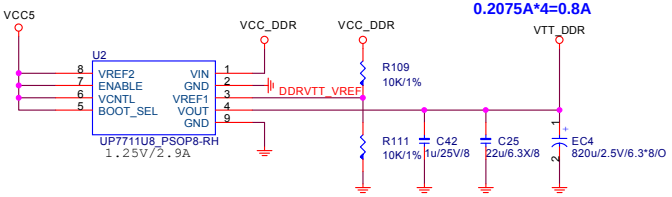


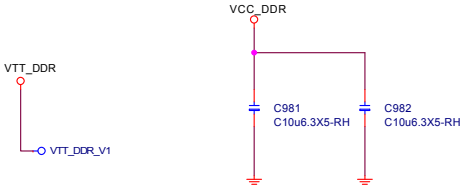


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*4=0.8A





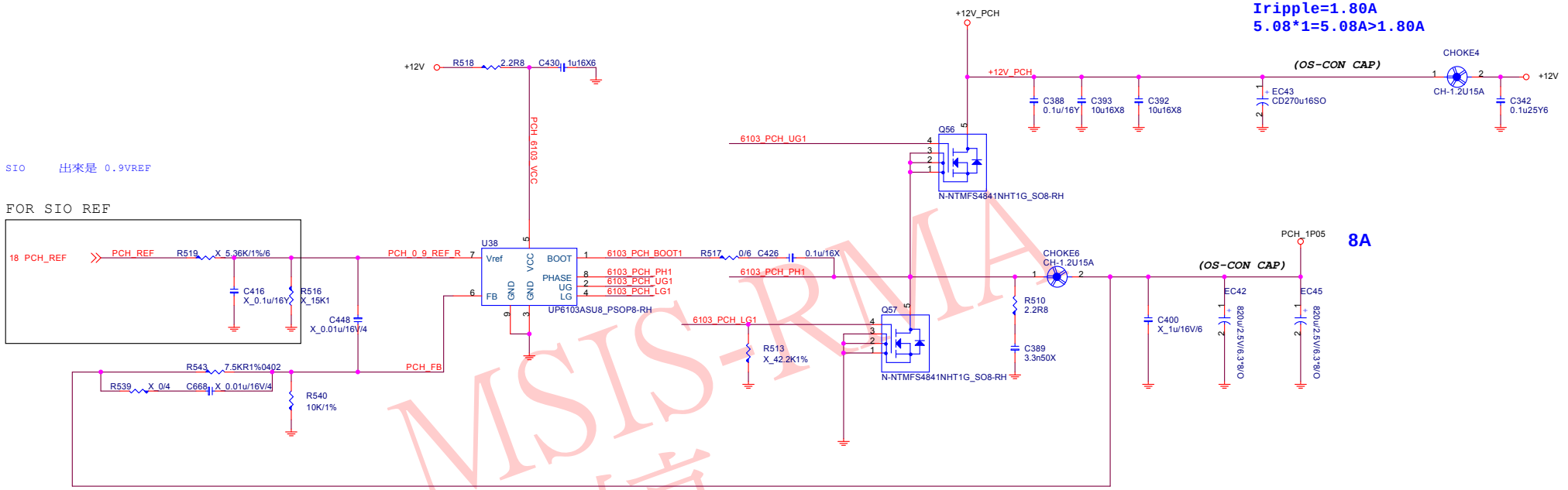
MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size: Custom	Document Description: DDR Power - uP6103 1-Phase	Rev: 0C
Date: Monday, July 19, 2010	Sheet 33 of 47	

PCH Power:1.05V

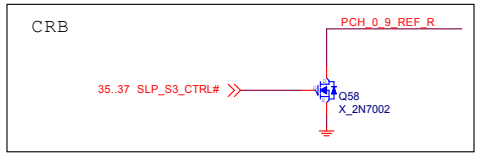
PCH Core 6.2A+1.8A=8A

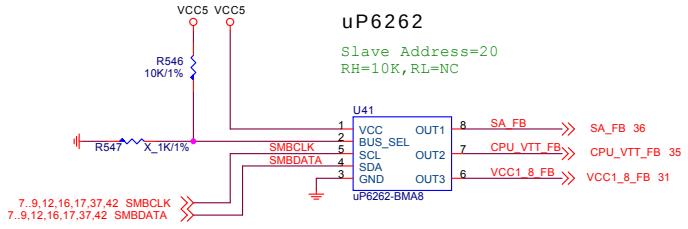
6.2A FOR PCH

1.8A FOR ME CORE



UPI VOLTAGE CONSOLE





MICRO-STAR INT'L CO.,LTD

MS-7676

Size	Document Description	Rev
Custom	PCH Power - uP6103 1-Phase	0C

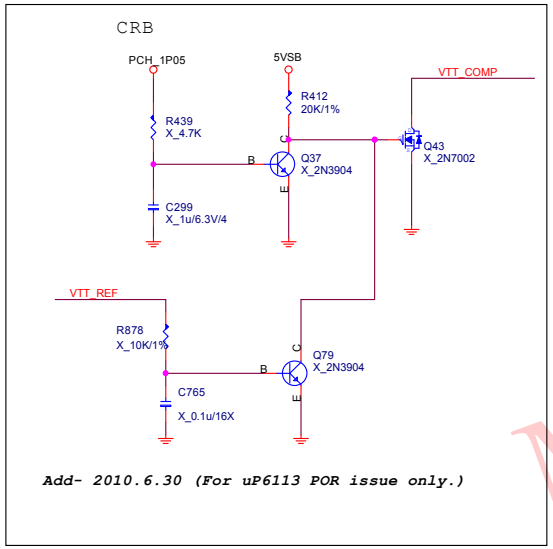
Date: Monday, July 19, 2010 Sheet 34 of 47

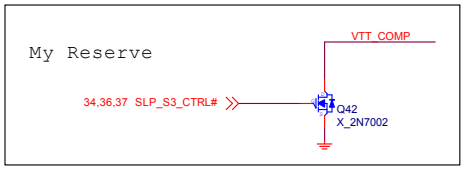
CPU_VTT:1.05/1.00

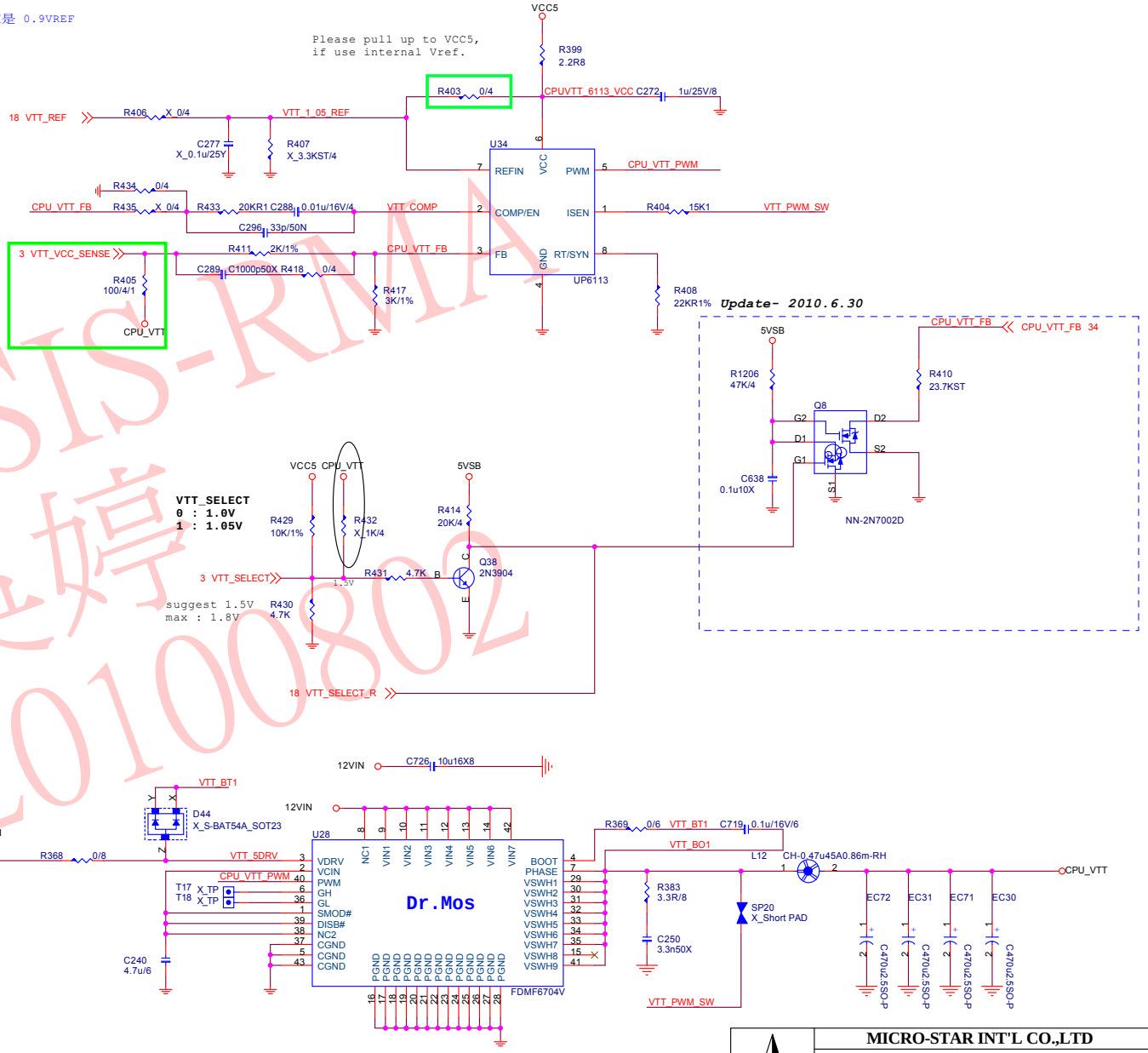
CPU VTT 8.5A

8.5A FOR CPU

SIO 出來是 0.9VREF





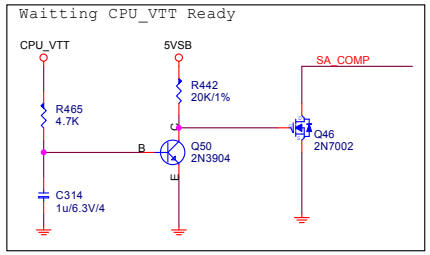


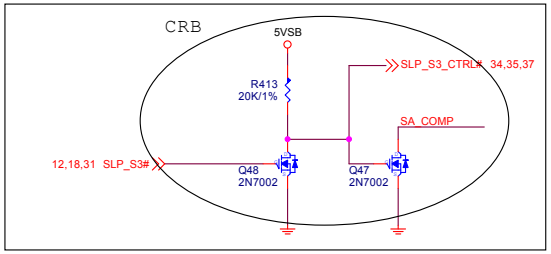
MICRO-STAR INT'L CO.,LTD	
MS-7676	
Size: Custom	Document Description: CPU_VTT - uP6113- 1-Phase
Rev: 0C	
Date: Monday, July 19, 2010	Sheet 35 of 47

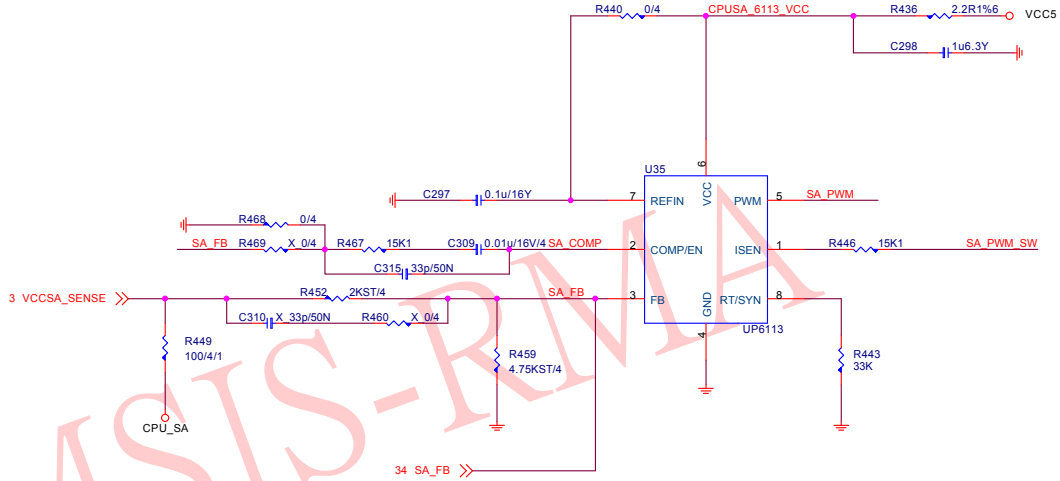
CPU_SA:0.925/0.85

SA Core =8.8A

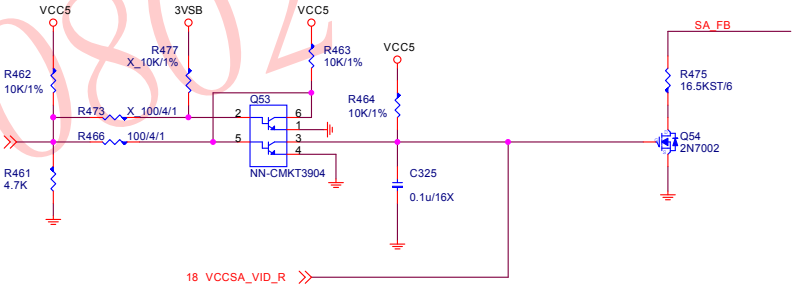
Please pull up to VCC5,
if use internal Vref.

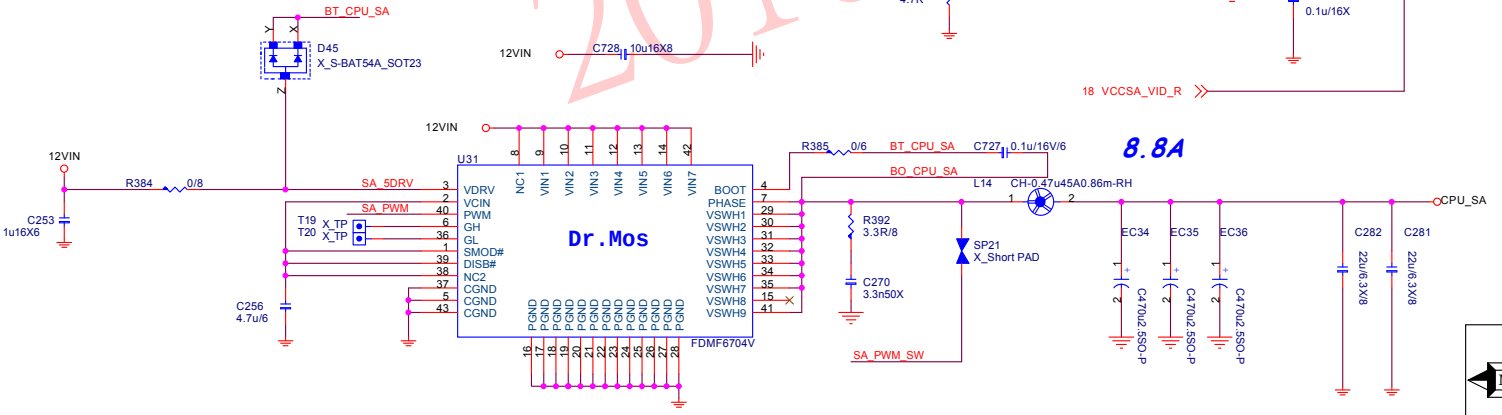




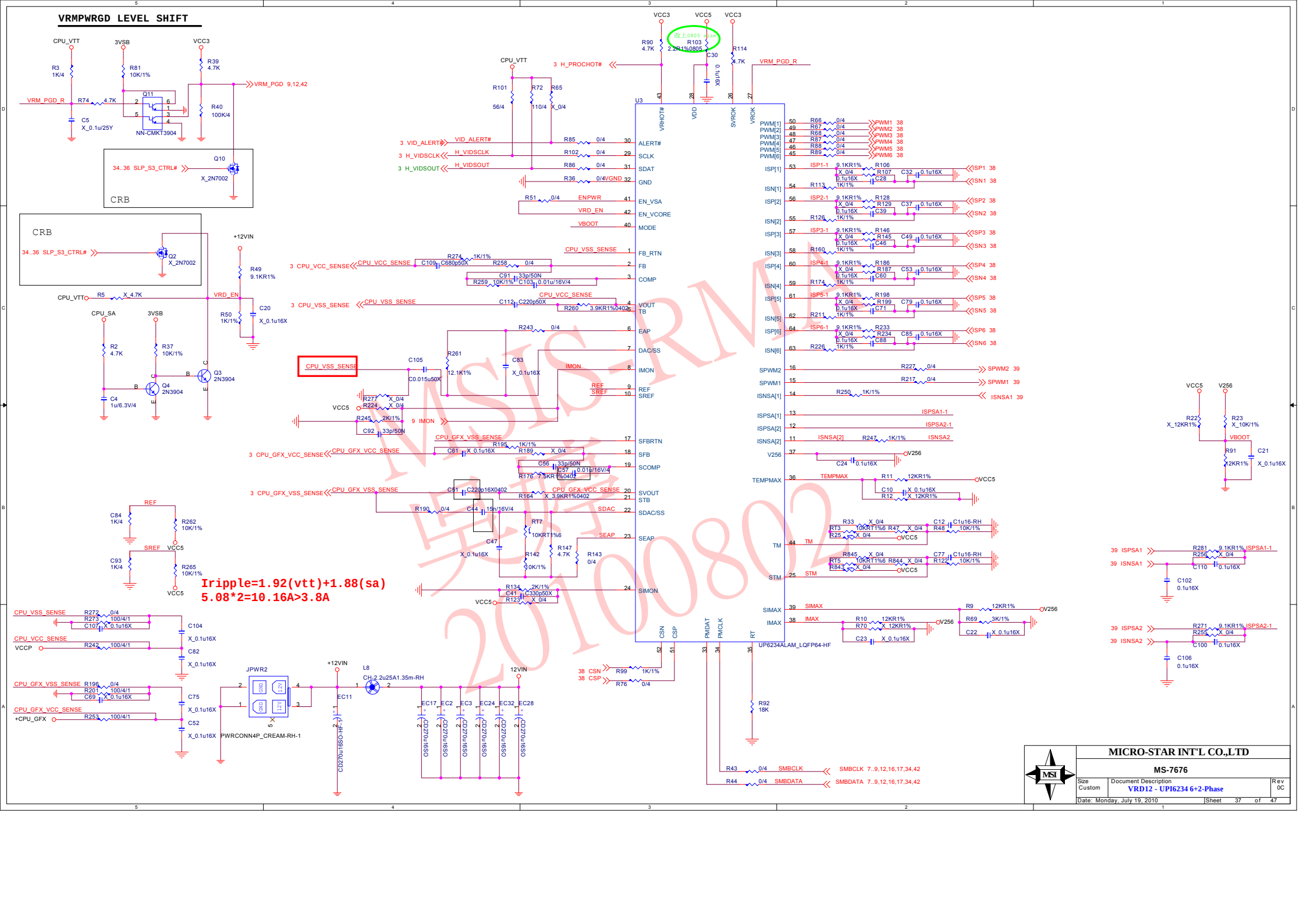


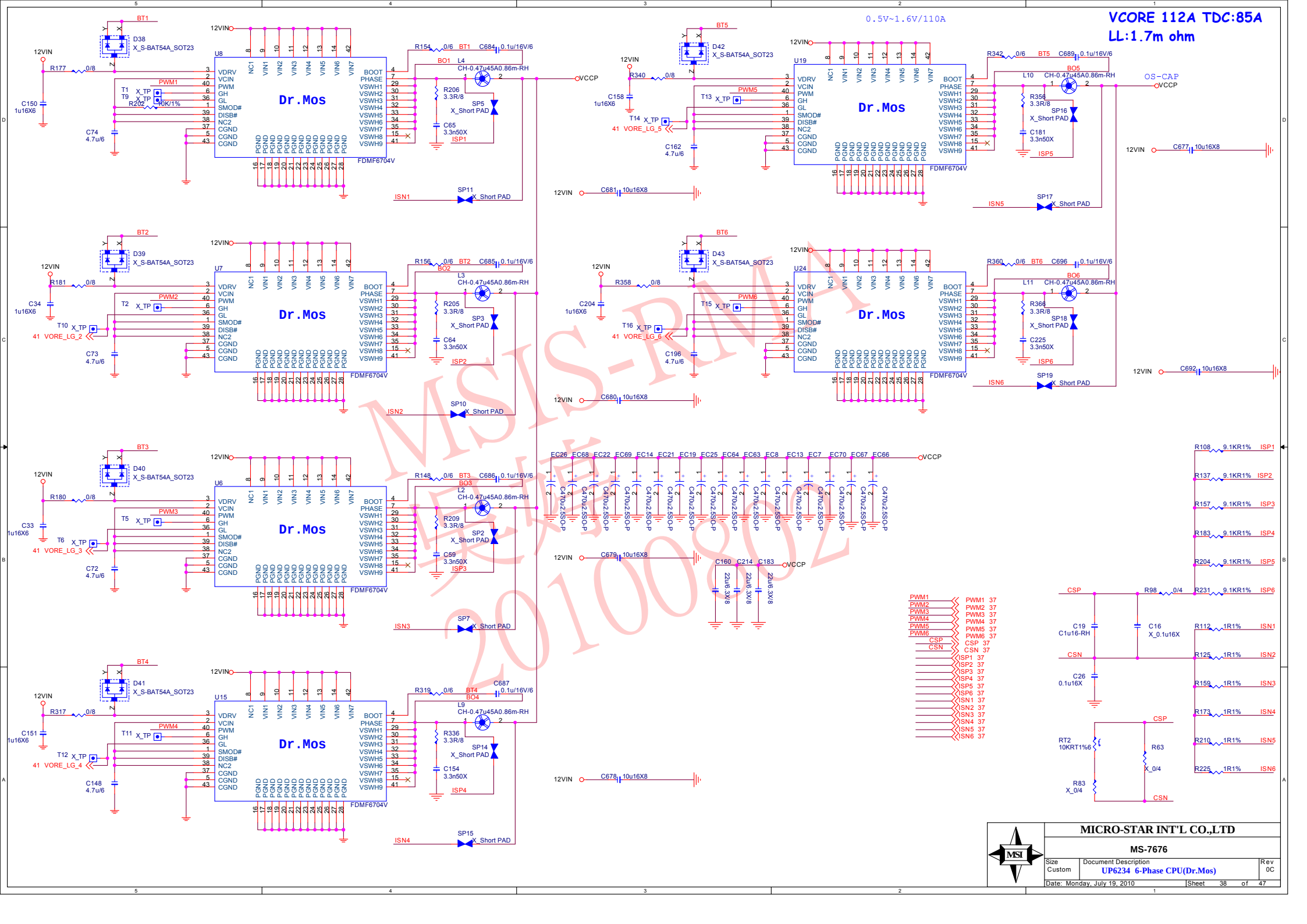
VCCSA_VID
0 : 0.925V
1 : 0.85V



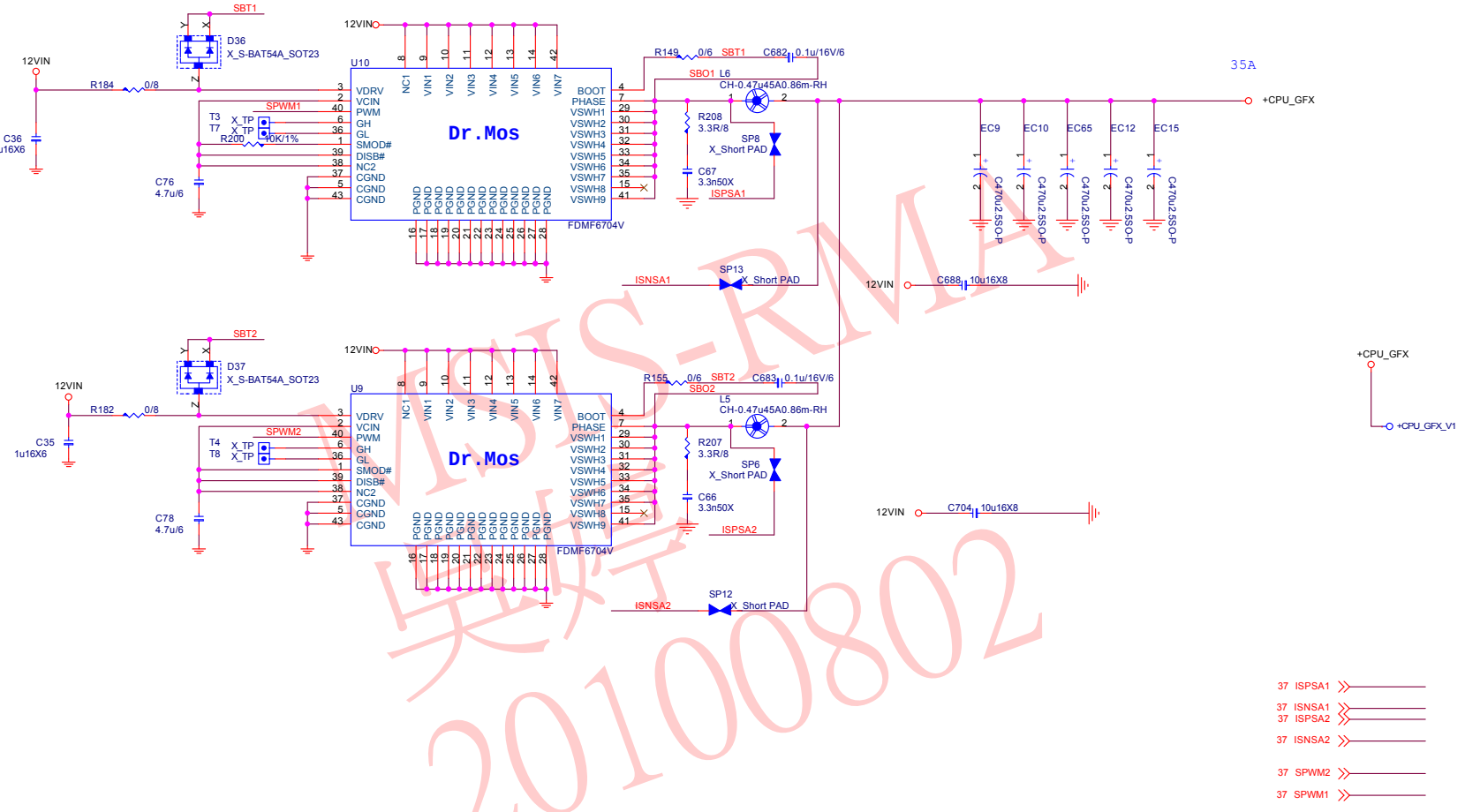


MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size: Custom	Document Description: CPU_SA - uP6113 1-Phase	Rev: 0C
Date: Monday, July 19, 2010	Sheet 36 of 47	


VRMPWRGD LEVEL SHIFT
CRB
CRB
Iripple=1.92(vtt)+1.88(sa)
5.08*2=10.16A>3.8A
UP6234ALAM_LQFP64-HF
MICRO-STAR INT'L CO.,LTD
MS-7676
VRD12 - UPI6234 6+2-Phase
Date: Monday, July 19, 2010
Sheet 37 of 47

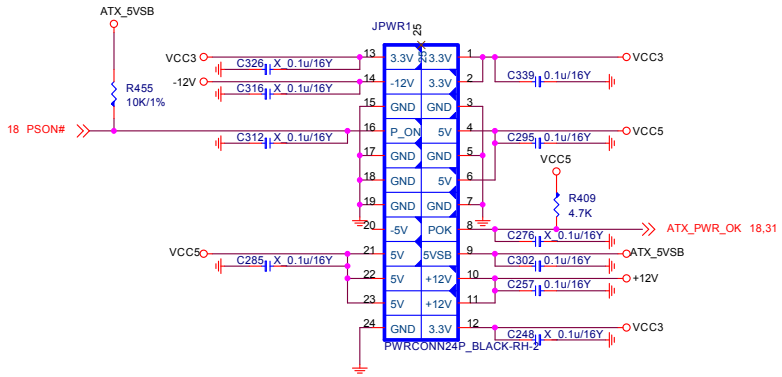


MICRO-STAR INT'L CO.,LTD	
MS-7676	
Size: Custom	Document Description: UP6234 6-Phase CPU(Dr.Mos)
Rev: 0C	
Date: Monday, July 19, 2010	Sheet 38 of 47

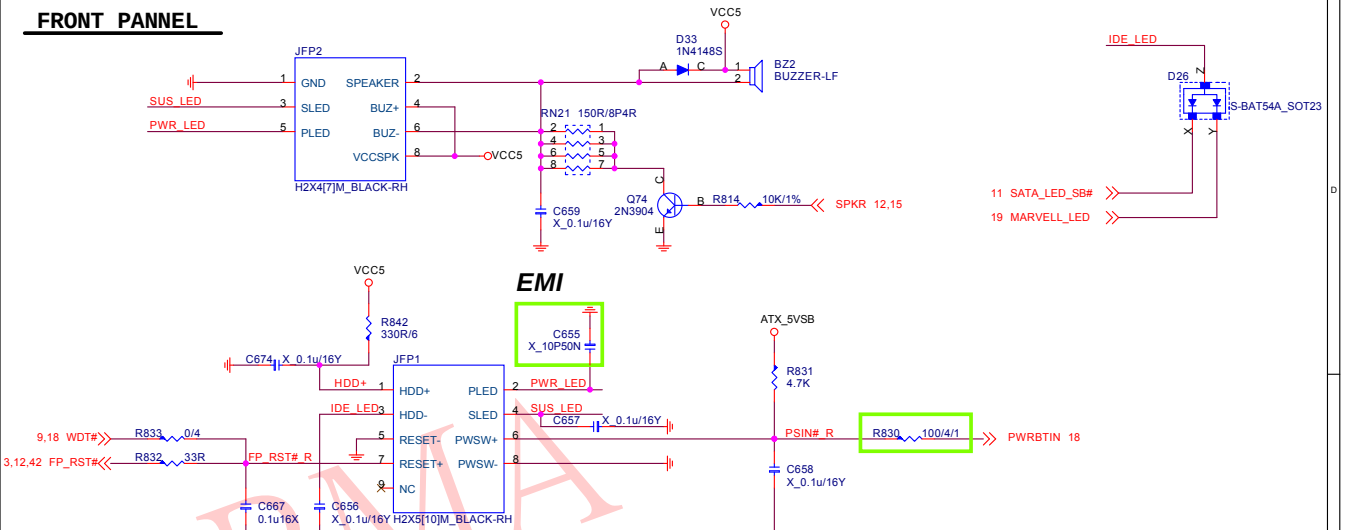


MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size: Custom	Document Description: UP6234 2-Phase GPU(Dr.Mos)	Rev: 0C
Date: Monday, July 19, 2010	Sheet 39 of 47	

ATX POWER CONNECTOR

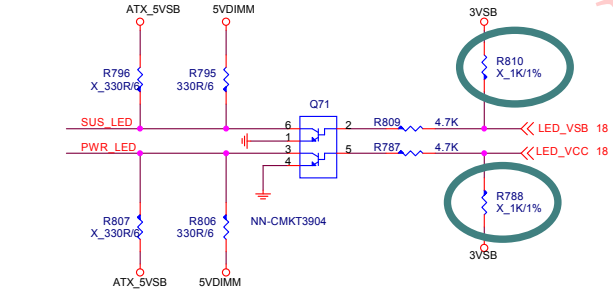


FRONT PANNEL

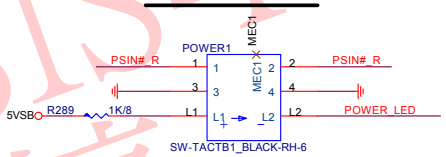


EMI

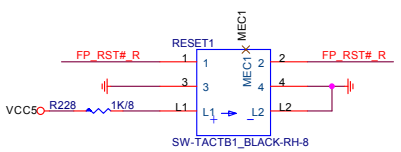
LED (for Fintek 71889)



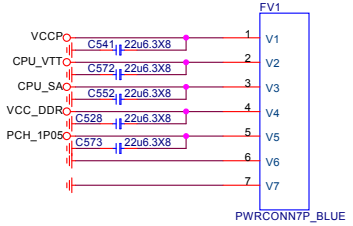
POWER ON BUTTON



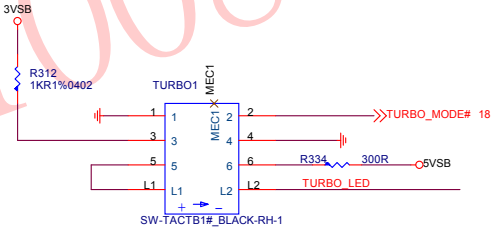
RESET BUTTON



電壓測點

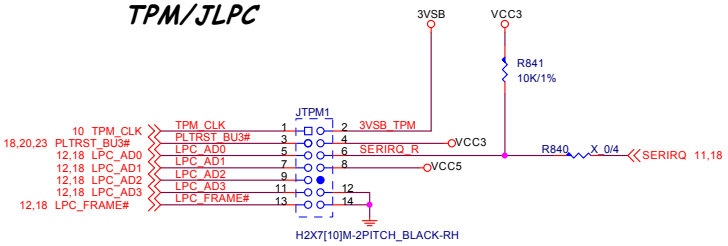


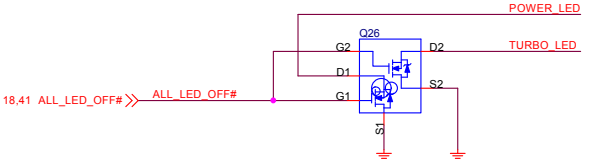
DPS Turbo Button



TURBO_MODE#

TPM/JLPC





NN-2N7002D

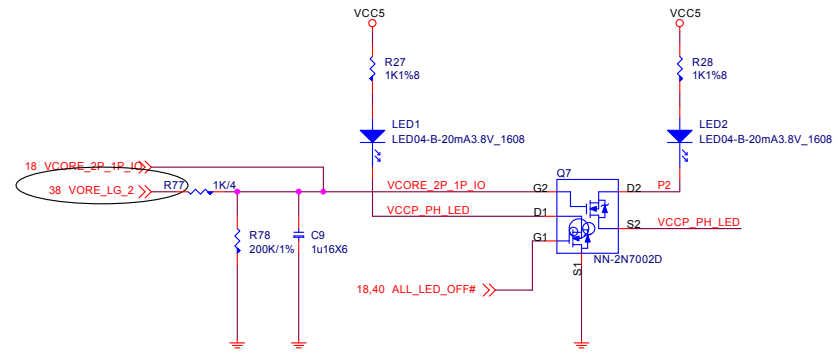
MICRO-STAR INT'L CO.,LTD

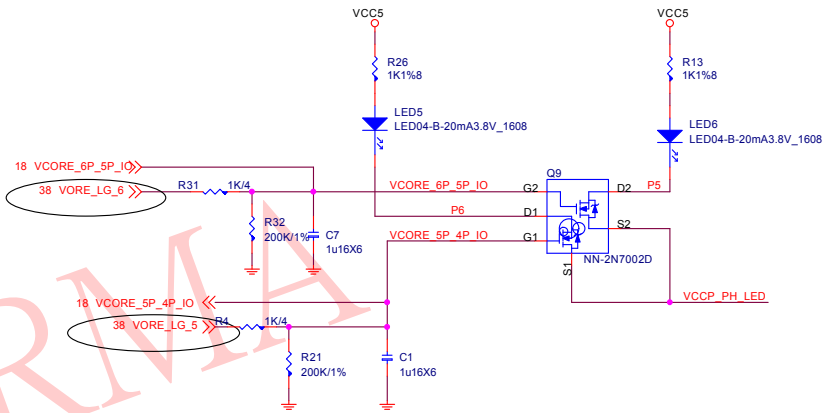
MS-7676

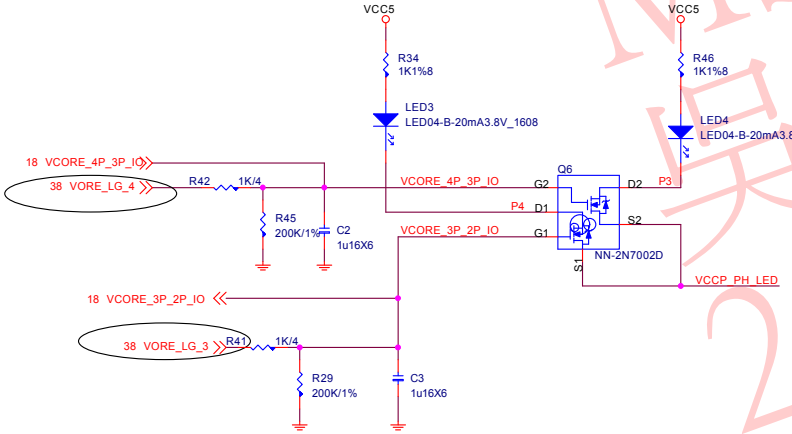
Size	Document Description	Rev
Custom	ATX PWR-Connector & Front Panel & EMI	0C

Date: Monday, July 19, 2010 Sheet 40 of 47

all on board LED switch

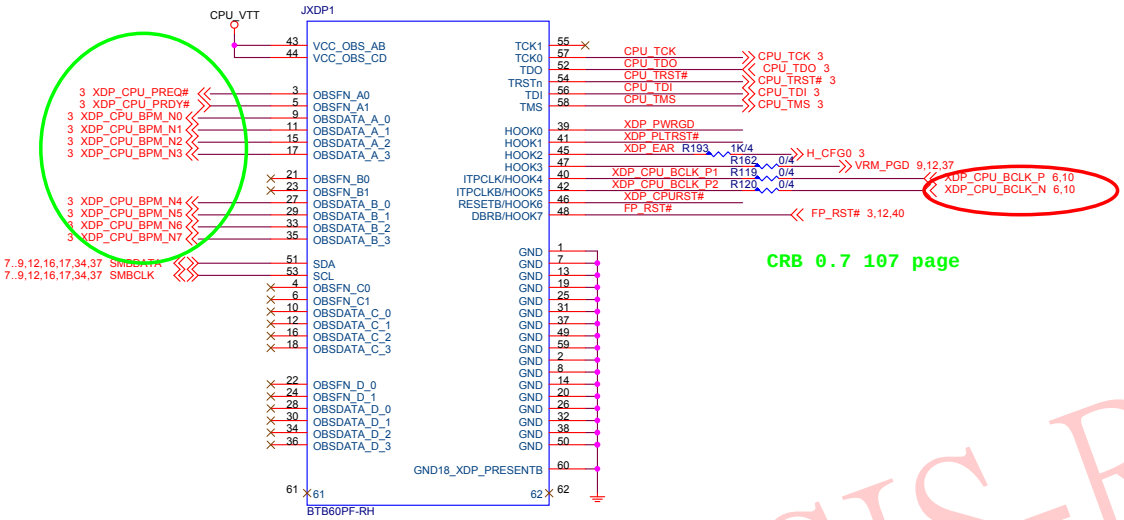






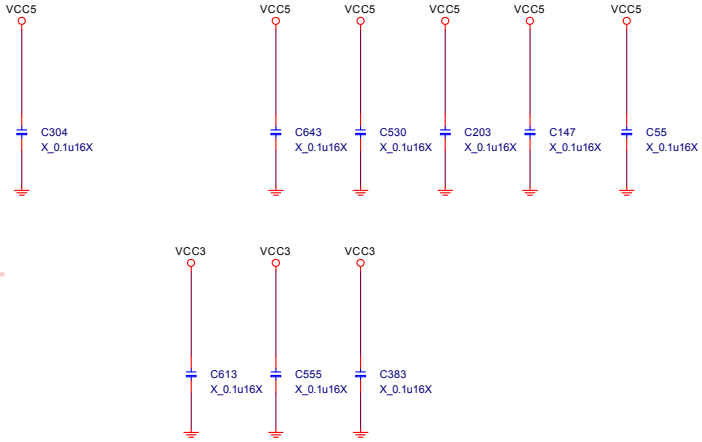
MICRO-STAR INT'L CO.,LTD	
MS-7676	
Size: Custom	Document Description: PHASE Dropping & PSI & LED
Rev: 0C	
Date: Monday, July 19, 2010	Sheet 41 of 47

Reserve debug port 5020

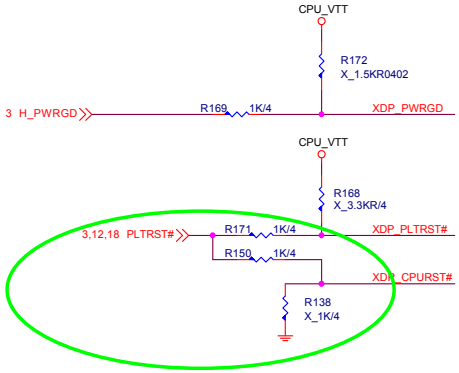


CRB 0.7 107 page

PCH XDP

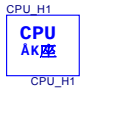


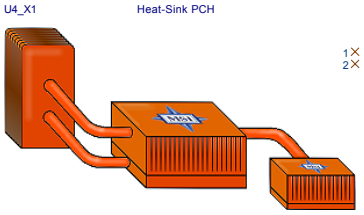
PCH XDP PWRGD/RESET



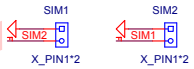
PK0-076760A-E48競華,27,寶安恩斯邁廠(MSIS)
PK0-076760A-G37,精成,27,寶安恩斯邁廠(MSIS)

CPU Heat-pipe

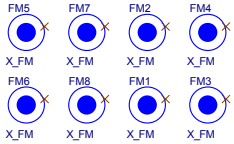




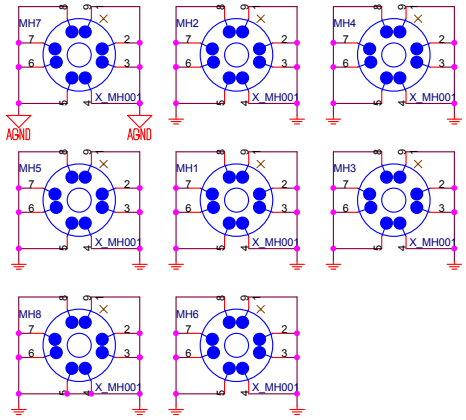
Simulation



Optical Fiducial Marks-120



Mounting Holes



MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size: Custom	Document Description: XDP / Manual Parts	Rev: 0C
Date: Monday, July 19, 2010	Sheet 42 of 47	