“Polaris 12” XL Databook

Technical Reference Manual - AMD Confidential

Part Number: 55950_1.02

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Revision History

Note: The release states are defined as:

Preliminary Releases:

Revision numbers 0.xx are rough works.

Revision numbers 1.xx are documents with substantial info

Revision numbers 2.xx are documents with complete information.

Full Release

Revision numbers 3.xx are for production.

Revision History

Rev 1.02 (June 5, 2017)

- Updated Branding diagram in Part Identification (p. 1).
- Updated DisplayPort link data rate information in DisplayPort (DP) and Embedded DisplayPort (eDP) Features (p. 10).
- Updated Driver and Test Platform in Thermal Design Power (TDP) (p. 68).

Rev 1.01 (March 2, 2017)

- Updated HD Audio Controller ID in Part Identification (p. 1).
- Updated DisplayPort version across the document.
- Removed non-applicable information from DVI/HDMI™ Features (p. 9).
- Updated Transmitter Electrical Specification in SMBus Electrical Characteristics (p. 64).

Rev 1.00 (January 17, 2016)

- Preliminary release.

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1 Introduction

TBD.

The features and functionalities identified in this databook are preliminary information and do not constitute specifications until they have been qualified by AMD.
The databook is updated as necessary following qualification to convert this document to a formal specification.

Please review any errata and advisories as they identify amendments to the specifications in this databook.

Contact your local AMD support person for the software support schedules of GPU features.

1.1 Part Identification

1.1.1 Packaging Types, Device IDs, and Part Numbers

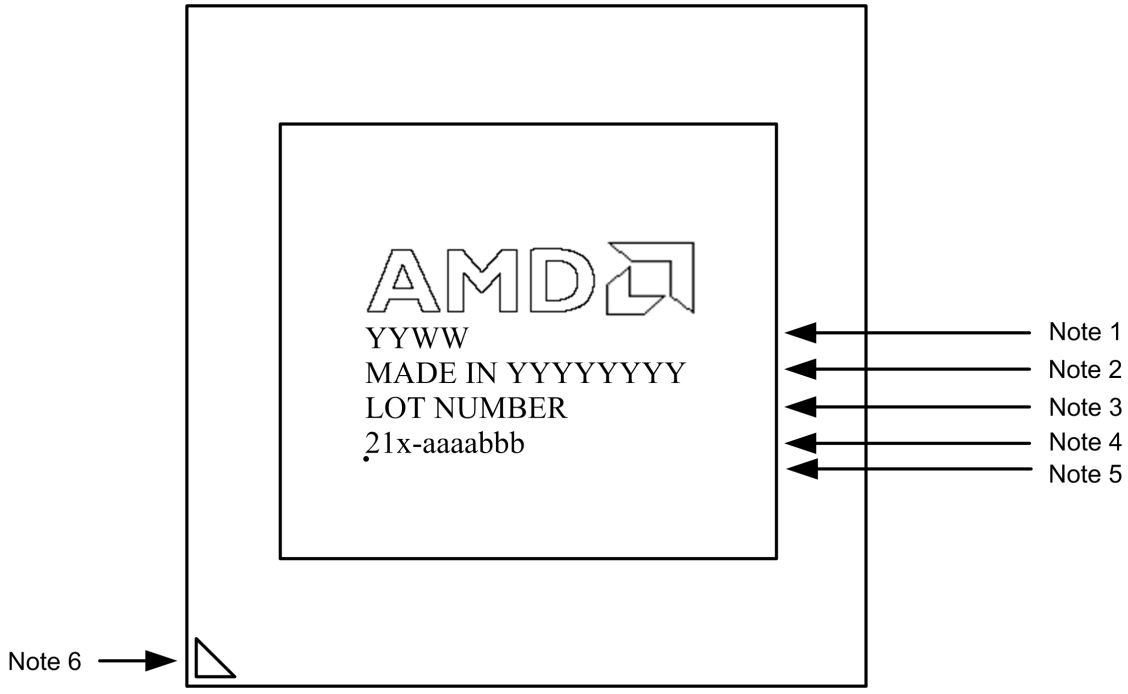
The vendor ID is 0×1002.

Table 1–1 Package Information

Part	Device ID / Revision ID	Part Number	HD Audio Controller ID	HD Audio Codec ID	Package
“Polaris 12” XL	699F/C7	215-0904018	AB10	AA01	769 FCBGA

1.1.2 Branding Format

Figure 1–1 “Polaris 12” XL Branding



Note:

1. The date code where YY is the assembly start year and WW is the assembly start week. Special markings that help differentiate the GPU from others may also appear on this line. For example, ES is found after the date code for engineering samples.
2. Country of origin YYYYYYYY (The assembly site; such as USA, SINGAPORE, TAIWAN, and CHINA).
3. The wafer foundry's lot number.
4. The part number. Refer to Table 1–1 (p. 1) for the appropriate part number.
5. Pin 1 dot.
6. GPU pin A1.

The branding format can be in laser, ink, or mixed laser and ink marking.

2

Functional Overview

This section describes the major subsystems and interfaces of “Polaris 12” XL. To go to a topic of interest, use the following list of linked cross-references:

2.1 Memory Interface

2.1.1 Memory Configurations Support

“Polaris 12” XL have four (128-bit) DRAM sequencers. Each DRAM channel is 32-bit wide. All DRAM devices must be of the same type, have the same size on each channel and must run at the same voltage.

“Polaris 12” XL supports only GDDR5 DRAM.

Supported DRAM Component Organizations:

- 8 or 16 banks (3 or 4 bank bits). Single rank.
- Rows: 1024, 2048, 4096, 8192, 16384, 32768, or 65536 (10, 11, 12, 13, 14, 15, or 16 bits).
- Columns: 256, 512, 1024, 2048 (8, 9, 10 bits).
- CS (chip select): 1.

2.1.2 Memory Aperture Size

The memory-aperture size can be set up through either pin straps for designs that do not have dedicated ROM for the video BIOS, or ROM straps for designs that have dedicated ROM. Refer to the descriptions of the ROM_CONFIG[2:0] and MEM_AP_SIZE [2:0] straps in Configuration Straps (p. 39) for more information.

The memory aperture defines the address range that the CPU can access. The memory-aperture size assigned to the GPU by the system BIOS is different from the physical-memory size that the AMD display driver reports to the operating system and control panel. It does not limit the GPU's ability to use the entire frame-buffer memory at any time. Modern graphics and multimedia applications use drivers to alter the frame-buffer contents—direct manipulation of the frame buffer by the CPU is limited. Therefore, having a memory-aperture size that is smaller than the physical frame-buffer size does not limit performance. The AMD display driver reports the memory size based on the amount of physical VRAM installed on the card rather than the memory-aperture size.

Due to memory-management constraints, the memory-aperture size should be the same as the frame-buffer size for 64 MB, 128 MB, and 256 MB. For frame-buffer sizes larger than 256 MB, the memory-aperture size should be 256 MB. For designs requiring larger than 256 MB aperture size, consult with AMD.

2.1.3 Examples of Possible Memory Configurations

The following are examples of possible single-rank memory configurations using different memory types.

Note: Not all memories are qualified. Check with your local AMD support person for the latest qualified memory list.

2.1.3.1 GDDR5 SGRAM (Graphics Double Data Rate Synchronous Graphics RAM)

Table 2–1 GDDR5 SGRAM

Size per Part	Configuration	Row × Col × Bank Bits	Total Memory Size (128-bit Interface)
512 Mbit	2 M × 32 × 8	12 × 6 × 3	256 MB
1024 Mbit	2 M × 32 × 16	12 × 6 × 4	512 MB
2048 Mbit	4 M × 32 × 16	13 × 6 × 4	1024 MB
4096 Mbit	8 M × 32 × 16	14 × 6 × 4	2048 MB
8192 Mbit	16 M × 32 × 16	14 × 7 × 4	4096 MB

2.2 Acceleration Features

- Support for DirectX® 12 (Feature Level 12_0) features, including the full-speed 32-bit floating point per component operation:
  - Shader Model 5.0 geometry and pixel support in a unified shader architecture:
    - Vertex, pixel, geometry, compute, domain, and hull shaders.
    - 32- and 64-bit floating-point processing per component.
    - New advanced shader instructions, including flexible flow control with CPU-level flexibility on branching.
    - A nearly unlimited shader-instruction store, using an advanced caching system.
    - An advanced shader design, with an ultra-threading sequencer for high-efficiency operations.
    - Graphics Core Next supporting native scalar instructions.
    - Advanced, high-performance branching support, including static and dynamic branching.
    - High dynamic-range rendering with floating-point blending, texture filtering, and anti-aliasing support.
    - 16- and 32-bit floating-point components for high dynamic-range computations.
    - Full anti-aliasing on renderable surfaces up to and including 128-bit floating-point formats.
    - A new read/write caching system, replacing texture cache with a unified read-write two-level cache.
- Support for OpenGL 4.5.
- Support for OpenCL™ 2.0.
- Support for Mantle
- Support for AMD LiquidVR™
- Anti-aliasing filtering:
  - 2×/4×/8× MSAA (multi-sample anti-aliasing) modes are supported.
  - A multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
  - Custom filter anti-aliasing with up to 12-samples per pixel.
  - An adaptive anti-aliasing mode.
  - Lossless color compression (up to 16:1).

- Anisotropic filtering:
  - Continuous anisotropic with 1× through 16× taps.
  - Up to 128-tap texture filtering.
  - Anisotropic biasing to allow trading quality for performance.
  - Improved anisotropic filtering with unified non-power of two-tap distribution and higher precision filter computations.
  - Advanced texture compression (3Dc+™).
  - High quality 4:1 compression for normal and luminance maps.
  - Angle-invariant algorithm for improved quality.
  - Single- or two-channel data format compatibility.
- 3D resources virtualized to a 40-bit virtual addressing space, for support of large numbers of render targets and textures.
- Up to 16k × 16k textures, including 128-bit/pixel texture are supported.
- Programmable arbitration logic maximizes memory efficiency and is software upgradeable.
- Fully associative texture, color, and z-cache design.
- Hierarchical z- and stencil-buffers with early z-test.
- Lossless z-buffer compression for both z and stencil.
- Fast z-buffer clear.
- Fast color-buffer clear.
- Z-cache optimized for real-time shadow rendering.
- Z- and color-compression resources virtualized to a 32-bit addressing space, for support of multiple render targets and textures simultaneously.

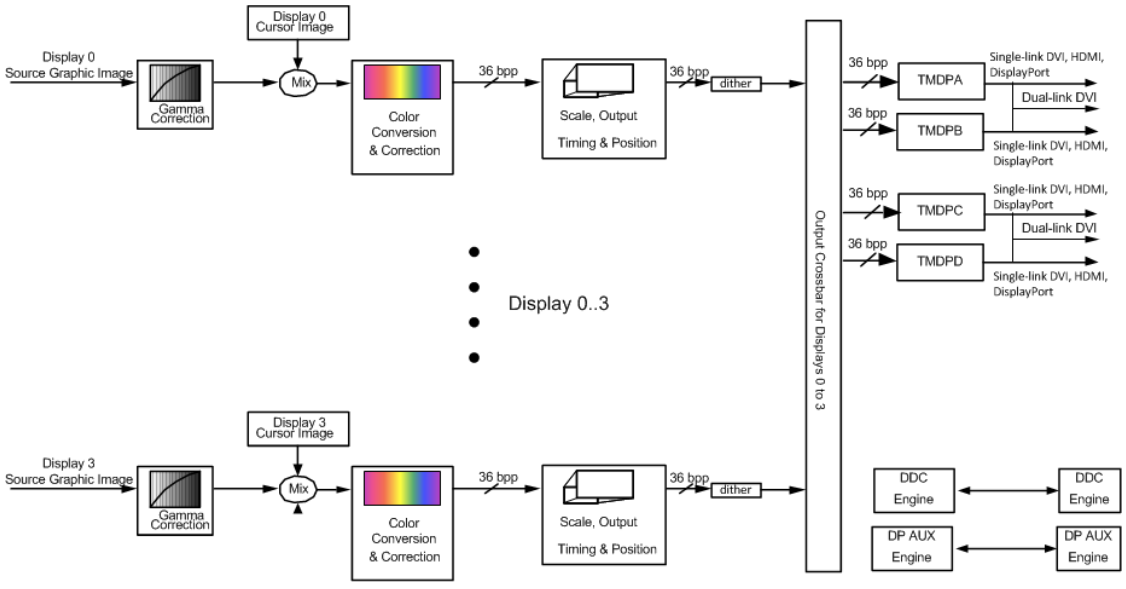
2.3 Display System

The display system supports accelerated display modes on multiple independent display controllers.

The full features of the display system are outlined in the following sections.

2.3.1 Display Features

Figure 2–1 "Polaris 12" XL Display Top-level Data-flow Diagram



Note: Although TMDPE is shown in Pin Assignment (p. 20) and Appendix A Pin Listings (p. 77), the port does not work on "Polaris 12" XL. Do not connect it.

- Up to four independent display controllers that support up to true 36-bpp (bits per pixel) throughout the display pipe.
- Support for each display output type up to the following display timings:
  - DisplayPort 1.4:
    - Up to two 5120 × 2880 pixel resolution displays @ 60 Hz refresh rates with dual-cable configuration, or
    - One 5120 × 2880 pixel resolution display @ 60 Hz refresh rates with single-cable configuration, or
    - Up to four 3840 × 2160 @ 60 Hz or four 4096 × 2160 @ 60 Hz displays.
  - HDMI™ 2.0b (6 Gbit/s) up to four 3840 × 2160 @ 60 Hz or 4096 × 2160 @ 60 Hz outputs
  - Dual-link DVI up to two 2560 × 1600 @ 60 Hz or 1920 × 1200 @ 60 Hz
  - Single-link DVI up to four 1920 × 1200 @ 60 Hz
- Support for up to four independent display timings on DisplayPort, HDMI, or DVI interfaces
- Advanced video capabilities, including high-fidelity gamma, color correction, and scaling for High Dynamic Range (HDR) or Standard Dynamic Range (SDR)
- A high-precision color pipe with the support of sRGB, Rec. 709 and Rec. 2020 color spaces with up to 12 bits/component
- HDR 10 with HDMI 2.0b and DP 1.4 HDR protocol support

- Each display pipe includes a high quality scaler for upscaling lower resolution desktop modes to available display resolutions (RMX) or underscanning for the HDMI output (if needed)
  - All desktop sources up to 4096 pixels/line may be upscaled (RMX)
  - Desktops up to 1920 wide may be underscanned for HDMI
- Support for Virtual Super Resolution (VSR) modes with surface size up to 5120 × 2880 downscaled to 3840 × 2160 @ 60 Hz
- HDCP supported independently and simultaneously on all HDMI, DVI, and DisplayPort outputs

  Note: HDCP is available only to licensed HDCP licensees and can only be enabled when connected to an HDCP-capable receiver
  - Supports HDCP version 1.4/2.2 protection for the HDMI interface
  - Supports HDCP version 1.1/2.2 protection for the DisplayPort interface
  - Supports HDCP version 1.4 protection for the DVI interface
- Content adaptive LCD backlight modulation (VariBright) to reduce embedded display panel power consumption
- Support for Stereo 3D displays through HDMI, DisplayPort, eDP, and DVI. Includes frame-sequential and frame-packed full Stereo 3D modes. Also 2D frame-compatible modes including side-by-side, top-and-bottom, line interleaved, and pixel interleaved
- Line or pixel interleave Stereo 3D mixing supported without the use of graphics shaders by using two display pipes for left and right and blending together immediately before the display output; this improves the Stereo 3D performance.

2.3.2 DVI/HDMI™/DisplayPort Features

- All TMDP links can be independently configured to any of single-link DVI, HDMI, or DisplayPort (DP)
- TMDPA and TMDPB (links A and B) may be combined to support dual-link DVI
- TMDPC and TMDPD (links C and D) may be combined to support dual-link DVI
- See Table 3–6 (p. 25) for more information on the supported display interface combinations
- Optional dithering or frame modulation from the 36-bpp internal display pipeline to 24-bit or 30-bit outputs on the DVI, HDMI, and DisplayPort if not using a 36-bpp output mode
  - Reduction to 18-bit is available for embedded DisplayPort outputs.

2.3.2.1 DVI/HDMI™ Features

- Supports industry-standard CEA-861 video modes including 480p, 720p, 1080i, 1080p, and 2160p. For a full list of currently supported modes, contact your local AMD support representative
- Supports AMD FreeSync™ technology on HDMI using AMD's vendor specific extension:
  - Fully HDMI compliant
  - Requires at least one display that is capable of AMD HDMI FreeSync™ technology
- Maximum pixel rates for 24-bpp outputs are:
  - DVI—165 MP/s (megapixels per second) for single-link DVI
  - DVI—330 MP/s for dual-link DVI
  - HDMI—594 MP/s

Table 2–2 HDMI™ Features

HDMI Feature	Support
Link Capabilities	
Maximum Signal Bandwidth (MHz)	594*
Maximum HDMI Data Bandwidth (Gbit/s)	3 × 5.94 = 17.82
Video Capabilities	
Maximum 2D Resolution	1920 × 1080p @ 144 Hz, 36 bpp 2560 × 1440 @ 100 Hz, 30 bpp 2560 × 1440 @ 144 Hz, 24 bpp 3840 × 2160 @ 60 Hz, 24 bpp 4096 × 2160 @ 60 Hz, 24 bpp 3840 × 2160 @ 30 Hz, 36 bpp 4096 × 2160 @ 30 Hz, 36 bpp
RGB	Yes
YCbCr 4:4:4 / YCbCr 4:2:2 / YCbCr 4:2:0	Yes
xvYCC	Yes
HDMI Deep Color	Yes
Maximum 4:4:4/4:2:2/4:2:0 Color Depth (bits per component)	12
PCM (Pulse-code Modulation) Audio Capabilities	
PCM Audio Rates Supported (kHz)	192, 96, 48, 176.4, 88.2, 44.1, 32
PCM Audio Bits per Sample	24, 20, 16
Maximum PCM Audio Channels	8
Maximum PCM Audio Bandwidth (rate × bits × channels) (Mbps)	36.864
Specific non-PCM Audio-format Support	
IEC 61937 Compressed-format support. For example, 5.1-channel Dolby DTS and 5.1-channel AC-3.	Yes
Dolby®-TrueHD Bitstream Capable	Yes

HDMI Feature	Support
DTS-HD Master-audio Bitstream Capable	Yes
DVD-A (DST) Support	No
SACD (DSD) Support	No
Stereo 3D Display Capabilities	
Packed Frame Stereo 3D Video Formats	2160p @ 30/25/24 Hz, 1080p @ 120/100/60/50/30/25/24 Hz, 720p @ 120/100/60/50/30/25/24 Hz
Note: *** Applies to direct connections where GPU and HDMI connectors are on the same PCB with maximum trace lengths of 127 mm or 5 inches, otherwise re-driver is needed.**	

2.3.2.2 DisplayPort (DP) and Embedded DisplayPort (eDP) Features

- Supports all the mandatory features of the *DisplayPort Standard Version 1.4* and the following optional features on all links:
  - HBR3 (8.1 Gbps) support
  - HDR protocol support
  - ACM packet-type support
  - ISRC packet-type support
- DisplayPort Multi-streaming Transport (MST) allowing up to four display pipelines to drive a single DisplayPort interface (provided the DisplayPort link bandwidth is not exceeded)
- Supports AMD FreeSync™ technology, which dynamically synchronizes the refresh rate of a display with the frame rate of the GPU:
  - Based on DisplayPort™ Adaptive-Sync technology
  - Requires at least one display that is capable of DisplayPort Adaptive-Sync technology
- Each DisplayPort link can support three options for the number of lanes and four options for link-data rate as follows:
  - Four, two, or one lane(s)
  - 8.1*-, 5.4-, 2.7-, or 1.62-Gbps link-data rate per lane
  - The eDP mode port also supports the 4.32-, 3.24-, 2.43-, or 2.16-Gbps link rate option

*

Note: Although GPU can support 8.1 Gbps link data rate, in eDP applications, GPU is validated up to 5.4 Gbps data rate due to unavailability of 8.1 Gpbs capable TCONs.

- Supports RGB formats 24, 30, and 36 bpp, as well as 18 bpp RGB for eDP
- Supports YCbCr formats in 4:4:4, 4:2:2, and 4:2:0 and 8, 10, and 12 bits/component using Rec. 709 and Rec. 2020
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth
  - Example of supported pixel rate/resolution support for four lanes at 8.1-Gbps link rate:
    - 5120 × 2880 @ 60 Hz, 24 bpp is supported using VESA timings @ 938.25 MP/sec
    - 3840 × 2160 @ 120 Hz, 24 bpp is supported using VESA timings @ 1075.804 MP/sec
  - Examples of supported pixel-rate/resolution for four lanes at 5.4-Gbps link rate:
    - 3840 × 2160 @ 60 Hz, 24 bpp or 30 bpp is supported using VESA timings @ 533.25 MP/sec
    - 3840 × 2160 @ 60 Hz, 24 bpp or 30 bpp is supported using CTA timings @ 594 MP/sec
    - 4096 × 2160 @ 60 Hz, 24 bpp or 30 bpp is supported using CTA timings @ 594 MP/sec
    - 2560 × 1440 @ 144 Hz, 24 bpp is supported using CTA timings @ 586.586 MP/sec
  - Examples of supported pixel-rate/resolution for two lanes at 5.4-Gbps link rate:
    - 2560 × 1600 @ 60 Hz, 24 bpp or 30 bpp is supported using VESA timings @ 268.5 MP/sec
  - The following table shows the maximum pixel rates for four, two, or one lane(s) at 8.1-GHz link rate.

Table 2–3 Maximum Pixel Rates for 4, 2, or 1 Lane(s) at 8.1-GHz Link Rate

	18 bpp	24 bpp	30 bpp	36 bpp
One Lane	360 MP/s	270 MP/s	216 MP/s	180 MP/s
Two Lanes	720 MP/s	540 MP/s	432 MP/s	360 MP/s
Four Lanes	1080 MP/s	1080 MP/s	864 MP/s	720 MP/s

- Embedded DisplayPort (eDP) specific features:
  - Supports VESA eDP spec version 1.4
  - Supports protected content on eDP via ASSR and HDCP
  - Panel Self Refresh (PSR) support as per eDP 1.4 specification for optimal power reduction when in static screen condition
  - AMD FreeSync™ is used as a power-savings feature in eDP applications

2.3.3 Integrated HD-Audio Controller (Azalia) and Codec

- Each HDMI and DisplayPort output supports HD audio stream independently, up to a maximum of six output streams
- Maximum output bandwidth of 73.728 Mbit/s
- Low power ECN support
- Hardware silent stream for power optimization during no audio periods
- Function level reset
- Compatible Microsoft® UAA driver support for basic audio
- For advanced functionality (as follows), an AMD or a third party driver is required
- LPCM:
  - Speaker formats: 2.0, 2.1, 3.0, 4.0, 5.1, 6.1, and 7.1
  - Sample rates: 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
  - Bits per sample: 16, 20, and 24
- Non-HBR compressed audio pass-through up to 6.144 Mbps:
  - Supports AC-3, MPEG1, MP3 (MPEG1 layer 3), MPEG2, AAC, DTS, ATRAC, Dolby Digital+, WMA Pro, and DTS-HD
- HBR compressed audio pass-through up to 24.576 Mbps:
  - Supports DTS-HD Master Audio and Dolby True HD
- Plug-and-Play:
  - Sink audio format capabilities declaration
  - Sink information
  - AV association
- Lip sync information
- HDCP content protection
- DisplayPort supports Global TimeCode using the regular AUX channel—GTC master mode only

2.4 Video Acceleration Features

- Video Decode Acceleration Technology:
  - Dedicated Unified Video Decoder hardware (UVD) for H.264, HEVC, VC-1, MPEG-4, MPEG-2, and MVC decode:
    - The H.264 implementation is based on the ISO/IEC 14496-10 specification. Up to HP@L5.1 decoding with a maximum bit rate of 160 Mbps. Support for constrained Baseline profile only (no FMO or ASO). Resolution support up to 4096 × 2160 (maximum 4K @ 60 fps).

      Multi View Coding (MVC) support for Blu-ray 3D content.
    - The HEVC implementation is based on the ISO/IEC 23008-2 specification. Up to Main/Main10 L5.1 decoding with a maximum bit rate of 160 Mbps. Resolution support up to 4096 × 2176 (maximum 4K @ 60 fps). Supports HDR-10 video playback.
    - The VC-1 implementation is based on the SMPTE 421M specification. Up to AP@L3 decoding with a maximum bit rate of 40 Mbit/sec. Resolution support up to 1920 × 1088 (maximum 1080p @ 60 fps).
    - MPEG-4 up to ASP@L5 decoding, supporting high-definition profiles. Sprite, GMC (global motion compensation), and RVLC (reversible variable length coding) are not supported. Resolution support up to 1920 × 1088 (maximum 1080p @ 60 fps).
    - The MPEG-2 implementation is based on the ISO 13818-2 specification. Up to MP@HL decoding. Resolution support up to 1920 × 1088 (maximum 1080p @ 60 fps).
    - MJPEG implementation is based on the ISO/IEC 10918-1 specification. Supports Baseline (DCT based, interleaved only). JFIF input format, 4:2:0 and 4:2:2 format support. Reference performance is 1080p @ 60 fps. MJPEG decoder can operate concurrently with other video decode or encode operations.
  - Microsoft DirectX Video Acceleration (DXVA) application interface (API) for Windows® operating systems.
- HEVC (H.265) Video Encoding acceleration technology:
  - HEVC encoder is frame interleaved with Video Decoder hardware (UVD) H.264, HEVC, VC-1, MPEG-4. and MPEG-2 decode:
    - HEVC encoding is based on the ISO/IEC 23008-2 specification.
    - Up to main profile @ level 5.0 High-Tier (4096 × 2160p @ 30fps) I and P frame (no B-frame) encode.
    - Multi-stream support with total throughput up to 1080p @ 120 fps.
    - Constant bit rate and variable bit rate rate controls.

- Video processing acceleration:
  - Video scaling and YCrCb to RGB color space conversion for video playback and fully adjustable color controls.
  - Motion Adaptive and Vector based deinterlacing filter eliminates video artifacts caused by displaying interlaced video on non-interlaced displays, and by analyzing image and using optimal deinterlacing function on a per-pixel basis.
  - HD HQV and SD HQV support: noise removal, detail enchantment, color enhancement, cadence detection, sharpness, and advanced deinterlacing.
  - Advanced upscaling of SD content to HD resolution.
  - Multi-planes compositing engine for Blu-ray player applications.
- Supports top-quality DVD and Blu-ray disc playback with the lowest CPU usage.

2.5 Video Codec Engine (VCE) Features

- Video encoding technology:
  - Video codec engine (VCE):
    - H.264 encoding is based on the ISO/IEC 14496-10 specification.
    - Up to Main Profile @ level 5.1 (3840 × 2160p @ 30 fps) I & P-frame (no B-frame) encode.
    - Multi-stream support with total throughput up to 1080p @ 120 fps.
    - Wi-Fi Display (WFD) compliant H.264 video encoding, and MPEG-2 transport stream generation, including audio muxing support for LPCM or non-LPCM (AC3/AAC) format audio with two channels up to 48 kHz.
    - HDCP2.0/2.1 encryption of protected content in WFD mode.
    - H.264 Scalable Video Coding (SVC) temporal video encoding.
    - Constant bit rate and variable bit rate rate controls.

2.6 PCI Express® Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 3.0, up to 8.0 GT/s.
- Supports ×1, ×2, ×4, and ×8 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s link-data rates.
- Supports ×8 lane reversal where the receivers on lanes 0 to 7 on the graphics endpoint are mapped to the transmitters on lanes 7 down to 0 on the root complex.
- Supports ×8 lane reversal where the transmitters on lanes 0 to 7 on the graphics endpoint are mapped to the receivers on lanes 7 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports full-swing and low-swing transmitter output levels.

2.7 Power Management Features

- Single-chip solution in 14 nm.
- Full ACPI 1.0b, OnNow, and IAPC (instantly available PC) power management.
- Intelligent power control through AMD PowerTune technology.
- Clocks to every major functional block are controlled by a unique dynamic clock-switching technique which is completely transparent to the software. By turning off the clock to a block that is idle or not in use, power consumption is significantly reduced during normal operation.
- Dynamic Power Management (DPM) defines multiple power levels (up to eight) to achieve best overall performance and idle power.

2.8 Spread-spectrum Support

2.8.1 Engine and Memory Spread-spectrum Support

- Internal engine and memory spread-spectrum support:
  - Internal engine spread-spectrum support programmable from 0% to 2% down spread with modulation frequencies from 30 kHz to 33 kHz.
  - Internal memory spread-spectrum support programmable from 0% to 1.25% down spread with modulation frequencies from 30 kHz to 33 kHz.
- External memory spread-spectrum support:
  - For GDDR5 memory, the external spread-spectrum clock is not supported. Only internal spread spectrum is supported for GDDR5 memory.

2.8.2 DisplayPort Internal Spread-spectrum Support

- From 0.25% to 0.5% down spread.
- Modulation frequency between 30 kHz and 33 kHz.

2.9 Internal Thermal Sensor

“Polaris 12” XL has an integrated thermal sensor that offers the following advantages:

- Provides GPU die temperature (accuracy ± 3°C) without the need for an external chip.
- High- and low-notification limits can be defined to generate interrupts and to change power states.

- Can be used to control a fan through PWM (see Table 3–18 (p. 35)).
- A critical temperature limit can be defined to allow the system to protect the GPU from damage (see GPIO_19_CTF).
- Temperature information can be provided through software (ACPI control methods) or directly through the SMBus hardware interface.

2.10 Thermal Diode

The thermal diode in “Polaris 12” XL is a grounded collector PNP BJT. The thermal diode has two pins for its interface—DPLUS and DMINUS (see Table 3–18 (p. 35)). DPLUS connects to the emitter of the BJT while DMINUS connects to its base. The collector is tied to substrate ground.

Note:

- The thermal diode can only be used when the GPU is powered; for example, it cannot be used when in D3 cold. The 3.3-V supply has to be active for temperature sensing to work because of the ESD protection diodes.
- The ideality factor of the on-die thermal diode varies significantly with temperature and sourcing current. If a design chooses to use the on die thermal diode of the GPU coupled with an external thermal sensor chip to read the GPU temperature, the external thermal sensor chip must support and enable beta compensation.

2.11 Logo Compliance

This product complies with the Windows Logo Program requirements for all target operating systems. This includes both the current logo and future (draft) requirements that will be enforced during the lifespan of the product.

2.12 Test Capability Features

“Polaris 12” XL has a variety of test modes and capabilities that provide a high-fault coverage and low-DPM (defect per million) ratio:

- Full-scan implementation on the digital core logic which provides high-fault coverage through ATPG (automatic test-pattern generation) vectors.
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules.
- JTAG (Joint Test Action Group) test mode, largely compliant with the IEEE 1149.1 standard, with internal scan chain for access to chip-level test functions and some board-level connectivity testing.
- Integrated hardware-diagnostic tests performed automatically upon initialization.
- Improved access to analog modules and PLLs to allow full evaluation and characterization of these modules.

2.13 Other Features

- Support for serial-ROM video BIOS.
- Support for 32- and 64-bit operating systems based on Intel, AMD, and PowerPC CPUs.

2.14 Export Control Classification

For information on the export control classification of this product, please contact dl.exportcontrol@amd.com.

3

Signal Descriptions

This section describes the signals of “Polaris 12” XL.

The following conventions are used:

- All active low signals are shown with the suffix "B", such as CASA0B.
- "PD" denotes a permanent internal pull down. "PD-register" denotes an internal pull down which is register controlled, and by default is turned off. "PD-reset" denotes an internal pull down which is register controlled, and by default is turned on. "PD-reset" also denotes that the internal pull down is active during reset. "PD" or "PD-reset" is not relevant when the pins are in output modes.
- To designate a group of pins that have the same pin name but are distinguished by a trailing number only, such as QSA_0, QSA_1, or QSA_2, the abbreviation "Pin name[y:x]" is used. For example, QSA_[7:0] means pins QSA_7 to QSA_0.
- In the “Polaris 12” XL pin assignment:
  - NC or NC_*: Pins marked as NC are free pins that have no electrical connection on the GPU package.
  - RSVD: These pins should float (i.e., no electrical connection) on the PCB.

To go to a topic of interest, use the following list of linked cross-references:

3.1 Pin Assignment

Table 3–1 "Polaris 12" XL Pin Assignment—Left Half

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A		VSS	DQA1_30	DQA1_28	VSS	DQA1_27	DQA1_25	WCKA1_1	VSS	DQA1_22	DQA1_20	DDBIA1_2	VSS	DQA1_17	DQA1_15	DQA1_13	VSS	EDCA1_1	DQA1_11	DQA1_9	VSS
B	VSS	TEST6	DQA1_31	DQA1_29	DDBIA1_3	EDCA1_3	DQA1_26	DQA1_24	WCKA1B_1	DQA1_23	DQA1_21	EDCA1_2	DQA1_19	DQA1_18	DQA1_16	DQA1_14	DQA1_12	DDBIA1_1	DQA1_10	DQA1_8	WCKA1B_0
C	DQB0_1	DQB0_0	FB_VMEMIO		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
D	DQB0_3	DQB0_2					CLKA1		CLKA1B		WEA1B		MAA1_3		MAA1_8		CASA1B		RASA1B		RASA0B
E	VSS	DDBIB0_0	VSS	VSS			CSA1B_0		VSS		MAA1_9		VSS		MAA1_0		VSS		CKEA1		VSS
F	DQB0_4	EDCB0_0																			
G	DQB0_6	DQB0_5	VSS	CLKB0	CSB0B_0		VSS				VSS		MAA1_2		VSS		MAA1_7		VSS		CKEA0
H	WCKB0_0	DQB0_7									MAA1_4		MAA1_5		MAA1_1		MAA1_6		ADBIA1		ADBIA0
J	VSS	WCKB0B_0	VSS	CLKB0B	VSS		TEMPINRETURN	TEMPIN0													
K	DQB0_9	DQB0_8									VMEMIO		VMEMIO		MEM_CALRA		MVREFDA		VMEMIO		VSS
L	DQB0_11	DQB0_10	VSS	WEB0B	MAB0_9		VSS	MAB0_4		VMEMIO	VSS		VDDCI		VSS		VDDCI		VSS		VDDCI
M	DDBIB0_1	EDCB0_1																			
N	VSS	DQB0_12	VSS	MAB0_3	VSS		MAB0_2	MAB0_5		VMEMIO	VDDCI		VDDC		VDDC		VSS		VSS		VDDC
P	DQB0_14	DQB0_13																			
R	DQB0_16	DQB0_15	VSS	MAB0_8	MAB0_0		VSS	MAB0_1		MEM_CALRB	VSS		VDDC		VDDC		VSS		VSS		VDDC
T	DQB0_18	DQB0_17																			
U	VSS	DQB0_19	VSS	CASB0B	VSS		MAB0_7	MAB0_6		MVREFDB	VDDCI		VDDC		VDDC		VSS		VSS		VDDC
V	EDCB0_2	DDBIB0_2																			
W	DQB0_20	DQB0_21	VSS	RASB0B	CKEB0		VSS	ADBIB0		VMEMIO	VSS		VDDC		VDDC		VSS		VSS		VDDC
Y	DQB0_22	DQB0_23																			
AA	VSS	WCKB0B_1	VSS	RASB1B	VSS		CKEB1	ADBIB1		VSS	VDDCI		VDDC		VDDC		VSS		VSS		VDDC
AB	WCKB0_1	DQB0_24																			
AC	DQB0_25	DQB0_26	VSS	CASB1B	MAB1_7		VSS	MAB1_6		VMEMIO	VSS		VDDC		VDDC		VSS		VSS		VDDC
AD	DQB0_27	EDCB0_3																			
AE	VSS	DDBIB0_3	VSS	MAB1_8	VSS		MAB1_0	MAB1_1		VSS	VDDCI		VDDC		VDDC		VSS		VSS		VDDC
AF	DQB0_28	DQB0_29																			
AG	DQB0_30	DQB0_31	VSS	MAB1_3	MAB1_2		VSS	MAB1_5		VMEMIO	VSS		VDDC		VDDC		VSS		VSS		VDDC
AH	DQB1_0	DQB1_1																			
AJ	VSS	DQB1_2	VSS	MAB1_4	VSS		WEB1B	MAB1_9		VSS	VSS		VDDC		VDDC		VDDC		VDDC		VDDC
AK	DQB1_3	DDBIB1_0																			
AL	EDCB1_0	DQB1_4	VSS	CLKB1B	CLKB1		VSS	CSB1B_0		VSS	VSS		VDDC		VDDC		VDDC		VDDC		VDDC
AM	DQB1_5	DQB1_6									DRAM_RSTB		TSVDD		VDD_18		VSS		AUX2N		DDCAUX3P
AN	VSS	DQB1_7	VSS	WCKB1_1	WCKB1B_1		VSS	DQB1_28													
AP	WCKB1_0	WCKB1B_0									DQB1_31		VSS		VDD_18		VSS		AUX2P		DDCAUX3N
AR	DQB1_8	DQB1_9	VSS	DQB1_24	DQB1_25		VSS				VSS		FB_VDDC		VDD_18		GPIO_SVT		VSS		VSS
AT	DQB1_10	DQB1_11																			
AU	VSS	EDCB1_1	VSS	DQB1_26			DQB1_27		VSS		DQB1_30		FB_VSS		PLLCHARZ_H		GPIO_SVC		DDC2DATA		GPIO_14_HPD2
AV	DDBIB1_1	DQB1_12					EDCB1_3		DDBIB1_3		DQB1_29		FB_VDDCI		PLLCHARZ_L		GPIO_SVD		DDC2CLK		HPD1
AW	DQB1_13	DQB1_14	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS
AY	VSS	VSS	DQB1_15	DQB1_17	DQB1_19	DDBIB1_2	DQB1_21	DQB1_22	VSS	DDC1CLK	AUX1P	VSS	TEST_PG	TXCEP_DPE3P	TX0P_DPE2P	TX1P_DPE1P	VSS	TX2P_DPE0P	TXCDP_DPD3P	TX0P_DPD2P	TX1P_DPD1P
BA		VSS	DQB1_16	DQB1_18	VSS	EDCB1_2	DQB1_20	DQB1_23	VSS	DDC1DATA	AUX1N	AUX_ZVSS	TEST_PG_BACO	TXCEM_DPE3N	TX0M_DPE2N	TX1M_DPE1N	VSS	TX2M_DPE0N	TXCDM_DPD3N	TX0M_DPD2N	TX1M_DPD1N
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

Table 3–2 “Polaris 12” XL Pin Assignment—Right Half

22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	
WCKA1_0	DQA1_6	DQA1_4	VSS	DQA1_3	DQA1_1	DQA0_31	VSS	DQA0_28	EDCA0_3	DQA0_26	VSS	WCKA0_1	DQA0_23	DQA0_21	VSS	DDBIA0_2	DQA0_18	VSS		A
DQA1_7	DQA1_5	EDCA1_0	DDBIA1_0	DQA1_2	DQA1_0	DQA0_30	DQA0_29	DDBIA0_3	DQA0_27	DQA0_25	DQA0_24	WCKA0B_1	DQA0_22	DQA0_20	EDCA0_2	DQA0_19	DQA0_17	VSS	VSS	B
	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	DQA0_16	DQA0_15	C
	CASA0B		MAA0_8		MAA0_3		MAA0_4		CLKA0B		WCKA0_0		DQA0_7					DQA0_14	DQA0_13	D
	MAA0_7		VSS		MAA0_2		VSS		CLKA0		WCKA0B_0		DQA0_6			DQA0_5	VSS	DQA0_12	VSS	E
																		DDBIA0_1	EDCA0_1	F
	VSS		MAA0_0		VSS		WEA0B		VSS				VSS		DQA0_4	EDCA0_0	VSS	DQA0_11	DQA0_10	G
	MAA0_6		MAA0_1		MAA0_5		MAA0_9		CSA0B_0									DQA0_9	DQA0_8	H
												VSS	DQA0_3		VSS	DDBIA0_0	VSS	VSS	VSS	J
	VMEMIO		VSS		VMEMIO		VSS		VMEMIO									VSS	RSVD	K
	VSS		VDDCI		VSS		VDDCI		VSS	DRAM_RSTA		DQA0_0	VSS		DQA0_1	DQA0_2	VSS	DBGDATA_0	DBGDATA_1	L
																		DBGDATA_2	DBGDATA_3	M
	VDDC		VSS		VSS		VDDC		VDDC	VSS		DMINUS	DPLUS		VSS	TS_A	VSS	DBGDATA_4	DBGDATA_5	N
																		DBGDATA_6	DBGDATA_7	P
	VDDC		VSS		VSS		VDDC		VDDC	VSS		RSVD	VSS		GPIO_17_THERMAL_INT	GPIO_19_CTF	VSS	DBGDATA_8	DBGDATA_9	R
																		DBGDATA_10	DBGDATA_11	T
	VDDC		VSS		VSS		VDDC		VDDC	VSS		GPIO_16_8P_DETECT	GPIO_6_TACH		VSS	GPIO_28_FDO	VSS	DBGDATA_12	DBGDATA_13	U
																		DBGDATA_14	DBGDATA_15	V
	VDDC		VSS		VSS		VDDC		VDDC	VDD_08		HSYNC	VSYNC		GPIO_29	GPIO_30	VSS	GPIO_0	GPIO_11	W
																		GPIO_12	GPIO_13	Y
	VDDC		VSS		VSS		VDDC		VDDC	VSS		GPIO_5_REG_HOT_AC_BATT	GPIO_2		BP_1	BP_0	VSS	GPIO_1	GPIO_15	AA
																		GPIO_20	GPIO_21	AB
	VDDC		VSS		VSS		VDDC		VDDC	VDD_08		SDA	SCL		BL_ENABLE	BL_PWM_DIM	VSS	DIGON	PX_EN	AC
																		JTAG_TDI	JTAG_TMS	AD
	VDDC		VSS		VSS		VDDC		VDDC	VSS		SWAPLOCKB	VSS		PCIE_TX7P	PCIE_TX7N	VSS	TESTEN	JTAG_TCK	AE
																		JTAG_TRSTB	JTAG_TDO	AF
	VDDC		VSS		VSS		VDDC		VDDC	VDD_08		SWAPLOCKA	VDD_08		PCIE_TX6P	PCIE_TX6N	VSS	VSS	VSS	AG
																		PCIE_RX7N	PCIE_RX7P	AH
	VDDC		VDDC		VDDC		VDDC		VDDC	VDD_08		VDD_08	VSS		PCIE_TX5P	PCIE_TX5N	VSS	PCIE_RX6N	PCIE_RX6P	AJ
																		PCIE_RX5N	PCIE_RX5P	AK
	VDDC		VDDC		VDDC		VDDC		VDDC	VSS		VDD_08	VSS		PCIE_TX4P	PCIE_TX4N	VSS	PCIE_RX4N	PCIE_RX4P	AL
	VSS		GPIO_9_ROMSI		GPIO_10_ROMSCK		GENERICG		VDD_33									PCIE_RX3N	PCIE_RX3P	AM
												DDCVGACLK	VSS		PCIE_TX3P	PCIE_TX3N	VSS	VSS	VSS	AN
	DDCAUX4N		GPIO_8_ROMSO		GPIO_22_ROMCSB		GENLK_VSYNC		DDCVGADATA									PCIE_RX2N	PCIE_RX2P	AP
	DDCAUX4P		VSS		VSS		GENLK_CLK		VSS				VSS		PCIE_TX2P	PCIE_TX2N	VSS	PCIE_RX1N	PCIE_RX1P	AR
																		PCIE_RX0N	PCIE_RX0P	AT
	VSS		GENERIC_HPD4		DDCAUX5P		VSS		GENERICC		PCIE_RFCLKN		PCIE_TX0N			PCIE_TX1P	PCIE_TX1N	WAKEB	PCIE_ZVSS	AU
	GENERICF_HPD5		GPIO_18_HPD3		DDCAUX5N		GENERICB		GENERICD		PCIE_RFCLKP		PCIE_TX0P					CLKREQB	PERSTB	AV
	VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS	SMBCLK	SMBDAT	AW
TX2P_DPD0P	VSS	TXCCP_DPC3P	TX3P_DPC2P	TX4P_DPC1P	TX5P_DPC0P	TXCBP_DPB3P	VSS	TX0P_DPB2P	TX1P_DPB1P	TX2P_DPB0P	TXCAP_DPA3P	TX3P_DPA2P	TX4P_DPA1P	TX5P_DPA0P	VSS	ANALOGIO	XTALOUT	VSS	VSS	AY
TX2M_DPD0N	VSS	TXCCM_DPC3N	TX3M_DPC2N	TX4M_DPC1N	TX5M_DPC0N	TXCBM_DPB3N	VSS	TX0M_DPB2N	TX1M_DPB1N	TX2M_DPB0N	TXCAM_DPA3N	TX3M_DPA2N	TX4M_DPA1N	TX5M_DPA0N	VSS	GENERICA	XTALIN	VSS		BA
22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	

3.2 PCI Express® Bus Interface

For more information on signal definitions and electrical requirements, refer to the *PCI Express® Card Electromechanical 3.0 Specification* and *PCI Express Base 3.0 Specification*.

Note:

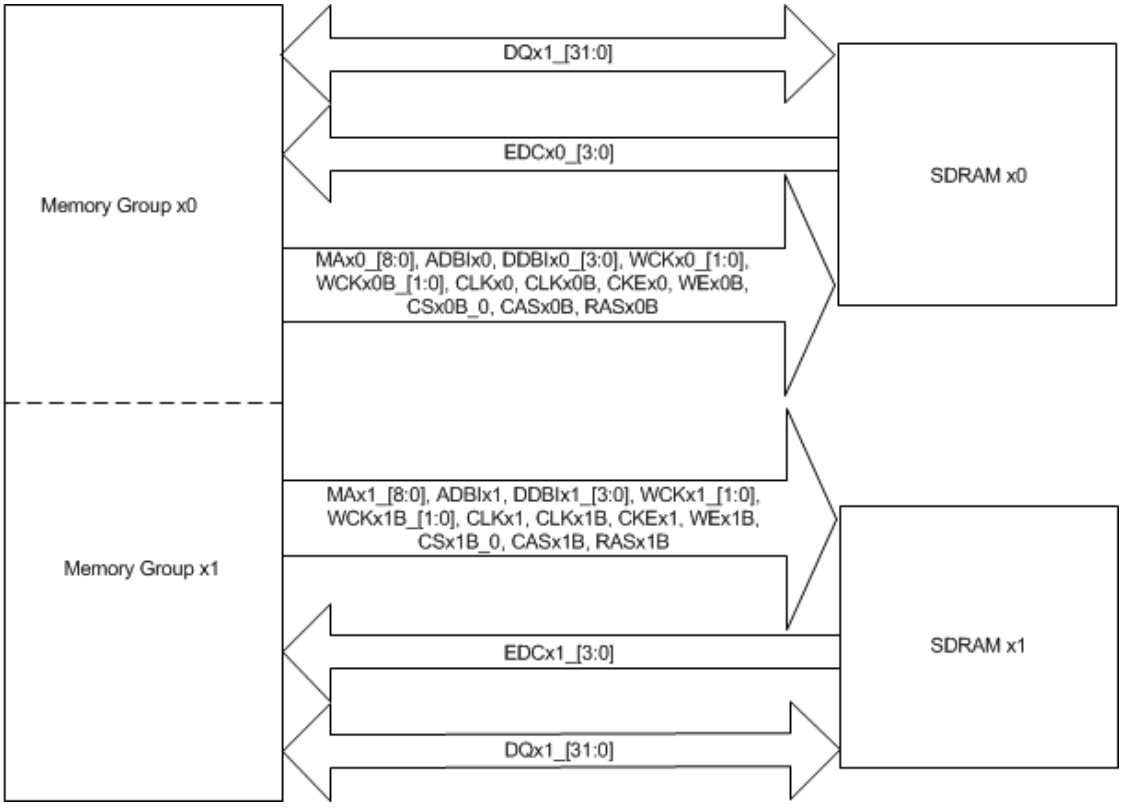
- “Polaris 12” XL supports ×8 lane reversal, where the receivers on lanes 0 to 7 of the graphics endpoint are mapped to the transmitter on lanes 7 down to 0 of the root complex. If ×8 lane reversal is employed, both the receive and transmit lanes must be reversed. In addition, polarity inversion is supported, such as when the + of the differential pair is connected to the - at the root complex.
- 220-nF AC-coupling capacitors are required.

Table 3–3 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTB	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3. A buffered reset signal dedicated to the GPU is required.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to 8.0-GT/s bit rate.
PCIE_ZVSS	I	Connect to VSS through a 200Ω (1% tolerance) resistor.
CLKREQB	I/O	CLKREQB only: CLKREQB is an open drain output on the GPU and an input on the platform which can be used to request the PCIe® reference clock to GPU on or off. L1 PM Substates: CLKREQB is a bi-directional open drain that can be asserted by either the GPU or the platform to initiate an L1 exit.
WAKEB	I	WAKEB is used as an input for the PCIe Optimized Buffer Flush/Fill (OBFF) feature. OBFF serves as a mechanism for the platform to tune power management (PM), and to align device activities. The signaling on WAKEB helps to tell the system status (CPU active or idle). The PCIe device will respond to this information to control its upstream traffic. Support from the platform is required.

3.3 Memory Interface (SGRAM, SDRAM)

Figure 3–1 Memory Interface



Note:

- A lower-case "x" is used to represent any of the available primary 64-bit-wide memory channels. “Polaris 12” XL have memory groups A and B.
- A "0" or "1" after "x" is used to separate the 64-bit-wide memory channel into two 32-bit wide sub-channels.
- “Polaris 12” XL supports GDDR5 memory with the mapping shown in Table 3–5 (p. 24).

Table 3–4 Memory Interface

Pin Name	Type	Description
MEM_CALRx	I	Connect to VSS through a 120-Ω (± 0.5%) resistor. Preferred resistor tolerance is 0.5%, but 1% is acceptable.
DQx0_[31:0]	I/O	Memory data bus for channel x0.
DQx1_[31:0]	I/O	Memory data bus for channel x1.
MAx0_[9:0]	O	Memory address bus for channel x0. Supplies bank addresses and row/column addresses for one 32-bit interface.
MAx1_[9:0]	O	Memory address bus for channel x1. Supplies bank addresses and row/column addresses for one 32-bit interface.
EDCx0_[3:0]	I	Error detection pins.
EDCx1_[3:0]	I	Error detection pins.
ADBIx0	O	Address dynamic bus inversion for channel x0.

Pin Name	Type	Description
ADBIx1	O	Address dynamic bus inversion for channel x1.
DDBIx0_[3:0]	I/O	Data dynamic bus inversion.
DDBIx1_[3:0]	I/O	Data dynamic bus inversion.
WCKx0_[1:0] **WCKx0B_[1:0]**	O	Forwarded clock.
WCKx1_[1:0] **WCKx1B_[1:0]**	O	Forwarded clock.
CLKx0 **CLKx0B**	O	Differential memory clock for channel x0.
CLKx1 **CLKx1B**	O	Differential memory clock for channel x1.
CKEx0	O	Clock enable control for channel x0.
CKEx1	O	Clock enable control for channel x1.
WEx0B	O	Write enable for channel x0.
WEx1B	O	Write enable for channel x1.
CSx0B_0	O	Chip select for channel x0.
CSx1B_0	O	Chip select for channel x1.
CASx0B	O	Column address strobe for channel x0.
CASx1B	O	Column address strobe for channel x1.
RASx0B	O	Row address strobe for channel x0.
RASx1B	O	Row address strobe for channel x1.
MVREFDx	A-I	Reference voltage per channel (memory data). 0.7 × VMEMIO.
DRAM_RSTx	O	Reset for all populated DRAMs (active low).

Table 3–5 GDDR5 Memory Mapping

GPU Signal	MAA0_9	MAA0_8	MAA0_7	MAA0_6	MAA0_5	MAA0_4	MAA0_3	MAA0_2	MAA0_1	MAA0_0
Memory Signal Mapping when **MF = 0**	RSVD	A13/A12	A7/A8	A6/A11	A5/BA1	A4/BA2	A3/BA3	A2/BA0	A1/A9	A0/A10

3.4 Display Configuration Overview

“Polaris 12” XL has up to four display links, A to D.

Table 3–6 Display Configuration Overview for Links A, B, C, and D

Pin Name	Possible Display Configurations		
TX[5:3]P/M_DPA[0:2]P/N **TXCAP/M_DPA3P/N**	Single-link DisplayPort/ TMDS	Dual-link DVI	A DisplayPort can be connected to any of links A, B, C, or D. The four links are independent and can be active simultaneously. HDMI™ can be connected to any of links A, B, C, or D. Dual-link DVI is available on links A and B, or C and D, respectively. B or D must be the master link for the respective dual-link pair.
TX[2:0]P/M_DPB[0:2]P/N **TXCBP/M_DPB3P/N**	Single-link DisplayPort/ TMDS		
TX[5:3]P/M_DPC[0:2]P/N **TXCCP/M_DPC3P/N**	Single-link DisplayPort/ TMDS	Dual-link DVI	
TX[2:0]P/M_DPD[0:2]P/N **TXCDP/M_DPD3P/N**	Single-link DisplayPort/ TMDS		

3.5 Integrated HDMI™/TMDS Interface

“Polaris 12” XL has four display links, A to D.

Note:

- The maximum pixel clock rate is 594 MHz on direct connectors. The GPU and HDMI connector are on the same PCB with a maximum trace length of 127 mm or 5 inches, and may be affected by TMDS signals layout and trace lengths.
- For unused interfaces, all signal outputs can be unconnected. AUX_ZVSS should always be connected.

Please refer to the *Digital Visual Interface (DVI) 1.0 Specification* and the *High-Definition Multimedia Interface (HDMI) Specification* for additional details.

Table 3–7 Integrated HDMI™/TMDS Interface

Pin Name	Type	Description
TX[5:3]P/M_DPA[0:2]P/N **TX[2:0]P/M_DPB[0:2]P/N** **TX[5:3]P/M_DPC[0:2]P/N** **TX[2:0]P/M_DPD[0:2]P/N**	O	TMDS data pairs (+/-). For single- and dual-link configurations. Transmitting at a bit rate of 10× pixel clock, up to 594-MHz pixel clock. A 100-nF capacitor is required on each differential signal placed near the connector. A 500-Ω resistor to ground is required on each differential-signal line. One FET is needed to disconnect the path from the 500-Ω resistors to ground when the system is off and the panel is on.
TXCAP/M_DPA3P/N **TXCBP/M_DPB3P/N** **TXCCP/M_DPC3P/N** **TXCDP/M_DPD3P/N**	O	TMDS clock channels (+/-). For single- and dual-link configurations. A 100-nF capacitor is required on each differential signal placed near the connector. A 500-Ω resistor to ground is required on each differential-signal line. One FET is needed to disconnect the path from the 500-Ω resistors to ground when the system is off and the panel is on. **Note:** TXCBP/M_DPB3P/N and TXCDP/M_DPD3P/N are used as the clock pairs for dual-link configurations.
TX[2:0]P/M_DPE[0:2]P/N **TXCEP/M_DPE3P/N**	N/A	Not supported; do not use.
DDC[2:1]CLK **DDC[2:1]DATA** **DDCAUX[5:3]N** **DDCAUX[5:3]P**	I/O	Differential signals for HDMI/TMDS DDC. For more details, see Table 3–15 (p. 33). NOT 5-V tolerant.
AUX_ZVSS	A	Analog calibration. Connect to VSS through a 150-Ω (1%) resistor.

3.6 DisplayPort Interface

Note: If this interface is not used, all signal outputs can be unconnected. AUX_ZVSS should always be connected.

“Polaris 12” XL supports up to four DisplayPort links.

The GPU and DisplayPort connector are on the same PCB with a maximum trace length of 127 mm or 5 inches.

Please refer to the *DisplayPort Standard Version 1.4* for additional details.

Table 3–8 DisplayPort Interface

Pin Name	Type	Description
TX[5:3]P/M_DPA[0:2]P/N **TXCAP/M_DPA3P/N**	O	DisplayPort (DPA) differential signals. DPA can be configured as a DisplayPort link. A 100-nF capacitor is required on each differential signal placed near the connector.
TX[2:0]P/M_DPB[0:2]P/N **TXCBP/M_DPB3P/N**	O	DisplayPort (DPB) differential signals. DPB can be configured as a DisplayPort link. A 100-nF capacitor is required on each differential signal placed near the connector.
TX[5:3]P/M_DPC[0:2]P/N **TXCCP/M_DPC3P/N**	O	DisplayPort (DPC) differential signals. DPC can be configured as a DisplayPort link. A 100-nF capacitor is required on each differential signal placed near the connector.
TX[2:0]P/M_DPD[0:2]P/N **TXCDP/M_DPD3P/N**	O	DisplayPort (DPD) differential signals. DPD can be configured as a DisplayPort link. A 100-nF capacitor is required on each differential signal placed near the connector.
TX[2:0]P/M_DPE[0:2]P/N **TXCEP/M_DPE3P/N**	N/A	Not supported; do not use.
AUX[2:1]P/N **DDCAUX[5:3]N** **DDCAUX[5:3]P**	I/O	DisplayPort auxiliary differential signals. See Table 3–15 (p. 33)
AUX_ZVSS	A	Analog calibration. Connect AUX_ZVSS to VSS through a 150-Ω (1%) resistor.

3.7 Hardware I²C Interface

Table 3–9 Hardware IC Interface

Pin Name	Type	Description
SCL	I/O 3.3 V (VDD_33)	I²C clock. **Note:** Can be left unconnected if not used.
SDA	I/O 3.3 V (VDD_33)	I²C data/address. **Note:** Can be left unconnected if not used.

3.8 Serial Flash Interface

Configuration straps must be set to identify the appropriate ROM type. See ROM Configurations (p. 42).

Table 3–10 Serial Flash Interface

Pin Name	Type	PD/PU	Description
GPIO_8_ROMSO	I 3.3 V (VDD_33)	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output.
GPIO_9_ROMSI	O 3.3 V (VDD_33)	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMSCK	O 3.3 V (VDD_33)	PD-reset	Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_22_ROMCSB	O 3.3 V (VDD_33)	PU-reset	BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations.

3.9 General Purpose I/O Interface

Table 3–11 General Purpose I/O Interface

Pin Name	Type	PD/PU	Description
3.3-V GPIOs			
The following signals, if not used for their primary purposes, may be used as GPIO pins.			
GPIO_0	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O and pin strap. See Table 3–26 (p. 40) for pin strap definition.
GPIO_1	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O.
GPIO_5_REG_HOT_AC_BATT	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O or fast power switch interrupt input. See Table 3–23 (p. 38) for the latter usage.
GPIO_6_TACH	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O or fan tachometer feedback. See Table 3–18 (p. 35) for the latter usage.
GPIO_8_ROMSO	I/O 3.3 V (VDD_33)	PD-reset	Pin strap, general purpose I/O, or serial-ROM output. See Table 3–26 (p. 40) for pin strap definition. See Table 3–10 (p. 28) for serial ROM usage.

Pin Name	Type	PD/PU	Description
GPIO_9_ROMSI	I/O 3.3 V (VDD_33)	PD-reset	Pin strap, general purpose I/O, or serial-ROM input. See Table 3–26 (p. 40) for pin strap definition. See Table 3–10 (p. 28) for serial ROM usage.
GPIO_10_ROMSCK	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O or serial-ROM clock. See Table 3–10 (p. 28) for serial ROM usage.
GPIO_12	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O and pin strap. See Table 3–26 (p. 40) for pin strap definition.
GPIO_14_HPD2	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O or hot-plug detect signal from the display device. See Table 3–15 (p. 33) for the latter usage.
GPIO_15	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O and pin strap. See Table 3–26 (p. 40) for pin strap definition.
GPIO_16_8P_DETECT	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O on mobile.
GPIO_17_THERMAL_INT	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O or thermal interrupt. See Table 3–18 (p. 35) for the latter usage.
GPIO_18_HPD3	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O or hot-plug detect signal from the display device. See Table 3–15 (p. 33) for the latter usage.
GPIO_20	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O and pin strap. See Table 3–26 (p. 40) for pin strap definition.
GPIO_21	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O.
GPIO_28_FDO	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O or fan drive. See Table 3–18 (p. 35) for the latter usage.
GPIO_29	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O and pin strap. See Table 3–26 (p. 40) for pin strap definition.

Pin Name	Type	PD/PU	Description
GPIO_30	I/O 3.3 V (VDD_33)	PD-reset	General purpose I/O.
GPIO_2	I/O 3.3 V (VDD_33)	PU-reset	General purpose I/O and pin strap. See Table 3–26 (p. 40) for pin strap definition.
GPIO_11	I/O 3.3 V (VDD_33)	PU-reset	General purpose I/O and pin strap. See Table 3–26 (p. 40) for pin strap definition.
GPIO_13	I/O 3.3 V (VDD_33)	PU-reset	General purpose I/O and pin strap. See Table 3–26 (p. 40) for pin strap definition.
GPIO_22_ROMCSB	I/O 3.3 V (VDD_33)	PU-reset	Pin strap, general purpose I/O, or ROM chip-select. See Table 3–26 (p. 40) for pin strap definition. See Table 3–10 (p. 28) for serial ROM usage.

Note:

1. During the ramp-up of the VDD_33 power rail, all GPIOs are undefined and a voltage bump may appear momentarily (up to 800 mV). GPIOs should be gated/filtered using an appropriate qualifier if they are connected to external circuits that are sensitive or responsive to the voltage bump.
2. Internal PU or PD is effective after VDDC is at ready state. Before VDDC is ready, the GPIOs are of Hi-Z state.
3. All GPIOs are configured as input by default after VDDC is at ready state. GPIOs can be programmed as output by the video BIOS. For any GPIOs that are default to PD internally, but used as output and expected to drive high level at power-up, if the external circuit is sensitive and responsive to the voltage level present on the GPIO during the period before the vBIOS is loaded, a strong pull-up of 1K Ω (5%) is recommended.
4. For GPIOs that serve as pin straps, any external circuits using them must not conflict with the logic level required by the strap after power up until PCIe reset gets de-asserted.
5. See Configuration Straps (p. 39) for more information on pin strap configurations.

3.10 AMD SVI2 Master Interface

Table 3–12 AMD SVI2 Master Interface

Pin Name	Type	Description
GPIO_SVC	O 1.8 V (VDD_18)	Serial VID clock. Push-pull clock output for the SVI2 data bus; driven by the GPU. Point-to-point connection to the SVI2 voltage regulator controller.
GPIO_SVD	I/O 1.8 V (VDD_18)	Serial VID data. Push-pull data output for the SVI2 data bus; driven by the GPU. Sets the voltage, power-state indicator, load-line slope, and voltage offsets for two voltage rails. Point-to-point connection to the SVI2 voltage regulator controller.
GPIO_SVT	I 1.8 V (VDD_18)	Serial VID telemetry. Push-pull data input driven by the SVI2 voltage regulator controller. Continuously streams the voltage and current telemetry information to the GPU. Also provides an indication when positive voltage transitions are complete (VOTFC).

3.11 Panel Control Interface

Note: All signals in this interface can be unconnected if not used. This interface may be used for eDP panels.

Table 3–13 Panel Control Interface

Pin Name	Type	PD/PU	Description
DIGON	O 3.3 V (VDD_33)	PD-reset	Controls panel digital power on/off. **Note:** External pull-down resistor is recommended.
BL_PWM_DIM	O 3.3 V (VDD_33)	PD-reset	LCD PWM (Pulse Width Modulated) output for adjustment of LCD brightness. Active high. BL_PWM_DIM can be used to control backlight on/off (backlight enable) by setting BL_PWM_CNTL.BL_PWM_EN = 0. **Note:** External pull-down resistor is recommended.
BL_ENABLE	O 3.3 V (VDD_33)	PD-reset	Controls backlight on/off. Active high. If this is not needed as the backlight enable signal, it can alternatively be used as a GPIO or an open-drain type output. **Note:** External pull-down resistor is recommended.
Note: During ramp-up of the VDD_33 power rail, these balls are undefined and a voltage bump may appear momentarily (up to 800 mV). These balls may need to be gated/filtered using an appropriate qualifier if they are connected to external circuits that are sensitive or responsive to the voltage bump.			

3.12 Global Swap Lock on Multiple GPUs

Global swap lock is used to synchronize the timing and surface flip for multiple display pipes on multiple GPUs.

If this feature is not required, the following signals can be used as 3.3-V GPIOs or left unconnected on the PCB.

Table 3–14 Global Swap Lock on Multiple GPUs

Pin Name	Type	PD/ PU	Description
GENLK_CLK	I/O 3.3 V (VDD_33)	PD-reset	Reference-clock input for the display PLLs (including the DCPLL and pixel PLLs) received from the framelock/genlock interface. **Note:** Can be unconnected if not used.
GENLK_VSYNC	I/O 3.3 V (VDD_33)	PD-reset	Frame-timing indicator. Output to the framelock/genlock interface.
SWAPLOCKA	Open drain 3.3 V	-	(Optional) Used in a multiple GPU design with multiple display outputs to allow all displays in group A to update at the same time and have synchronous left/right stereo timing. In a multiple GPU design where displays are connected to more than one GPU, connect SWAPLOCKA from all GPUs together with an external 10-kΩ pull-up resistor. GPU genlock is needed, either via a genlock system or by feeding all GPUs with the same reference clock. Connecting SWAPLOCKB is preferred but not required.
SWAPLOCKB	Open drain 3.3 V	-	(Optional) Used in a multiple GPU design with multiple display outputs to allow all displays in group B to update at the same time and have synchronous left/right stereo timing. In a multiple GPU design where displays are connected to more than one GPU, connect SWAPLOCKB from all GPUs together with an external 10-kΩ pull-up resistor. GPU genlock is needed, either via a genlock system or by feeding all GPUs with the same reference clock.

3.13 Display Identification Interface

Table 3–15 Display Identification Interface

Pin Name	Type	Description
DDC1CLK/ DDC1DATA or AUX1P/N	I/O 3.3 V (VDD_33)	DDC1CLK/DDC1DATA and AUX1P/N signal pairs are mutually exclusive. A design can use either the DDC1 or AUX1 pair on one display connector. Alternatively, DDC1DATA can be connected to AUX1N, and DDC1CLK can be connected to AUX1P on one DisplayPort connector (see reference schematics). **Note:** Can be unconnected if not used. For the DDC functionality (DDC data and clock signals (I^2C master)): • These pins can be used to support internal high-bandwidth digital content protection (HDCP). • Outputs are open drain and NOT 5-V tolerant. External pull-up resistors to 3.3 V are required. For the AUX functionality (auxiliary differential signals for DisplayPort): • A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector, and • A source detection pull-down resistor (100-kΩ 5% tolerance) is required on the AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on the AUXN signal.
DDC2CLK/ DDC2DATA or AUX2P/N	I/O 3.3 V (VDD_33)	DDC2CLK/DDC2DATA and AUX2P/N signal pairs are mutually exclusive. A design can use either the DDC2 or AUX2 pair on one display connector. Alternatively, DDC2DATA can be connected to AUX2N, and DDC2CLK can be connected to AUX2P on one DisplayPort connector (see reference schematics). **Note:** Can be unconnected if not used. For the DDC functionality (DDC data and clock signals (I^2C master)): • These pins can be used to support internal HDCP. • Outputs are open drain and NOT 5-V tolerant. External pull-up resistors to 3.3 V are required. For the AUX functionality (auxiliary differential signals for DisplayPort): • A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector, and • A source detection pull-down resistor (100-kΩ 5% tolerance) is required on the AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on the AUXN signal.
DDCAUX[5:3]N DDCAUX[5:3]P	I/O 3.3 V (VDD_33)	DDC data/clock for DVI/HDMI or auxiliary differential signals for DisplayPort. These pins can be used to support internal HDCP. **Note:** Can be unconnected if not used. For the AUX functionality: • A 100-nF AC-coupling capacitor is required on each differential signal placed near the connector, and • A source detection pull-down resistor (100-kΩ 5% tolerance) is required on each AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on each AUXN signal. For the I^2C functionality:

Pin Name	Type	Description
		Outputs are open drain and NOT 5-V tolerant. External pull-up resistors to 3.3 V are required.
HPD1 **GPIO_14_HPD2** **GPIO_18_HPD3** **GENERICE_HPD4** **GENERICF_HPD5**	I 3.3 V (VDD_33)	Hot-plug detect signal from the display device to the GPU.

3.14 JTAG Interface

In order to debug issues, AMD requires access to the JTAG interface.

Test points can be used on the JTAG signals to minimize the PCB space needed.

Table 3–16 JTAG Interface

Pin Name	Type	PD/ PU	Description
TESTEN	I 3.3 V (VDD_33)	-	Reserved signal. This pin must be tied to ground through a 1-kΩ to 10-kΩ resistor for normal GPU operation.
JTAG_TRSTB	I/O 3.3 V (VDD_33)	PU-reset	TRSTB (test reset). This pin can be left floating, or tied to 3.3 V through a 10-kΩ resistor for normal GPU operation. Must be accessible on all PCBs through a test point or resistor pad.
JTAG_TDI	I/O 3.3 V (VDD_33)	PU-reset	TDI (test data input). This pin can be left floating, or tied to 3.3 V through a 10-kΩ resistor for normal GPU operation. Must be accessible on all PCBs through a test point or resistor pad.
JTAG_TCK	I/O 3.3 V (VDD_33)	PD-reset	TCK (test clock). This pin can be left floating, or tied to ground through a 10-kΩ resistor for normal GPU operation. Must be accessible on all PCBs through a test point or resistor pad.
JTAG_TMS	I/O 3.3 V (VDD_33)	PU-reset	TMS (test mode select). This pin can be left floating, or tied to 3.3 V through a 10-kΩ resistor for normal GPU operation. Must be accessible on all PCBs through a test point or resistor pad.
JTAG_TDO	I/O 3.3 V (VDD_33)	-	TDO (test data output). This pin can be left floating, or unconnected if not used. Must be accessible on all PCBs through a test point or resistor pad.

3.15 Debug Port

Table 3–17 Debug Port

Pin Name	Functional Name
SMBDAT	Serial debug port data
SMBCLK	Serial debug port clock
DBGDATA[15:0]	Debug bus output data
TEST6	Connect to GND through a zero-Ω resistor
BP_0	Provide a pull-up resistor to 1.8 V on the PCB
BP_1	Provide a pull-up resistor to 1.8 V on the PCB
ANALOGIO	Provide access on the PCB through a test pad
PLLCHARZ_H	Provide access on the PCB through a test pad
PLLCHARZ_L	Provide access on the PCB through a test pad

3.16 Thermal Information and Management Interface

Table 3–18 Thermal Interface Signals

Pin Name	Type	PU/PD	Description
DPLUS	Anode	-	Thermal diode plus side (anode), used by the external temperature controller to obtain GPU die temperature. **Note:** Can be unconnected if not used.
DMINUS	Cathode	-	Thermal diode minus side (cathode), used by the external temperature controller to obtain the GPU die temperature. **Note:** Can be unconnected if not used.
GPIO_6_TACH	I 3.3 V (VDD_33)	PD-reset	Fan tachometer feedback.
GPIO_17_THERMAL_INT	Bi-dir 3.3 V (VDD_33)	PD-reset	Thermal monitor interrupt. An input from an external temperature sensor (ALERTb).
GPIO_19_CTF[1]	O 3.3 V (VDD_33)	PD-reset	Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the GPU from damage by removing power. If GPIO_19_CTF is expected to be latched at “high” level upon occurrence of the CTF event, 1.8 V and 3.3 V to the GPU must remain. The CTF setpoint is 99°C by default, and is programmed during GPU initialization.

Pin Name	Type	PU/PD	Description
GPIO_28_FDO	O	PD-reset	Fan drive output (output to control fan). In PWM mode, the PWM frequency is 15 kHz to 50 kHz.
TEMPIN0	I	-	A provision to connect to the anode of an external thermal diode for the GPU to read the temperature from a spot of interest on the board or platform. For experimental purposes and should be left unconnected.
TEMPINRETURN	I	-	A provision to connect to the cathode of an external thermal diode for the GPU to read the temperature from a spot of interest on the board or platform. For experimental purposes and should be left unconnected.

Note:
1. **Like other GPIOs, during the ramp-up of the VDD_33 power rail, GPIO_19_CTF is undefined and a voltage bump may appear momentarily (up to 800 mV). It should be gated/filtered using an appropriate qualifier if it is connected to a external circuit that is sensitive or responsive to the voltage bump.**

3.17 SMBus Interface

Table 3–19 SMBus Interface

Pin Name	Type	Description
SMBDAT	Bi-dir 3.3 V (VDD_33)	SMBus data. Connected to the SMBDAT line of the SMBus master with an external pull-up resistor to 3.3 V. Supports the SMBus 2.0 protocol. The SMBus slave address can be set to one of the four values from 0×40 to 0×43 through pin straps on DBGDATA_7 and DBGDATA_6. For more details, see Table 3–26 (p. 40). The GPU also supports ARP.
SMBCLK	Bi-dir 3.3 V (VDD_33)	SMBus clock. Connected to the line of the SMBus master with an external pull-up resistor to 3.3 V. Supports the SMBus 2.0 protocol. The SMBus slave address can be set to one of the four values from 0×40 to 0×43 through pin straps on DBGDATA_7 and DBGDATA_6. For more details, see Table 3–26 (p. 40). The GPU also supports ARP.

3.18 PLL Interface

Table 3–20 PLL Interface

Pin Name	Type	Description
XTALIN	A-I 1.8 V	An external 100-MHz non-spread 1.8-V oscillator is required to connect to XTALIN to provide the reference clock. Oscillator characteristics: • Frequency: 100 MHz. • Voltage swing: 1.8 V. • V_{IH} = 1.45 V (min) • V_{IL} = 0.45 V (max) • Accuracy: ± 10 ppm at room temperature, (± 30 ppm overall (including temperature drift)). • Duty cycle (worst case): 45-55 (max). • Jitter: 200 ps (max) cycle-to-cycle jitter. 300 ps (max) long-term jitter (10,000 cycles after the triggered edge).
XTALOUT	A-O 1.8 V	PLL Reference Clock Provides a provision to have a parallel-resonant crystal connected between XTALIN and XTALOUT as a reference clock to the GPU. Backup plan. Crystal characteristics: • ESR: <80Ω. • Combined frequency tolerance and stability: ±30 ppm max. A 1-MΩ resistor must be connected between XTALIN and XTALOUT when a crystal is used. Capacitive loading from the package and PCB trace should be subtracted from the C1 and C2 capacitor values. **Note:** External oscillator must connect to XTALIN only. (An oscillator cannot be connected to XTALOUT.)

Table 3–21 Recommended Clock-input Configurations

Memory Type	Description
GDDR5	100-MHz non-spread (1.8 V) oscillator connected to XTALIN.

3.19 AMD PowerXpress™ Interface

Table 3–22 AMD PowerXpress™ Interface

Pin Name	Type	PD/ PU	Description
PX_EN	O	PD	On/off regulator control signal for AMD ZeroCore Power feature (BACO mode). High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PG is asserted and PERSTb is de-asserted. Can be left unconnected if not used.

3.20 AMD PowerPlay™ Interface

Table 3–23 AMD PowerPlay™ Interface

Pin Name	Type	PD/ PU	Description
GPIO_5_REG_HOT_AC_BATT	I/O	PD-reset	(Optional) An input which allows the system to request a fast power reduction by setting GPIO_5_REG_HOT_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. This pin can be used for: • Battery protection on notebooks when AC power supply is suddenly removed. In this usage, the GPU will first be forced to the lowest DPM level of AC state then moved to battery state. Or • Other critical graphics/platform event that requires immediate power reduction on the GPU. For example, voltage regulator overheating and over power/current on the platform. In this usage, the GPU will be forced to the lowest DPM level of AC state until the event disappears after which normal DPM switching will be re-enabled. To enable the protection, the video BIOS needs to be properly configured. Also, battery protection requires different configuration of the video BIOS than other critical events. If both protection methods are required on the same platform, use GPIO_5 for battery protection and GPIO_6 for the other protection event. Power reductions that are less time-critical should use only the standard software methods in order to prevent display disturbances.
GPIO_21	I/O	PD-reset	(Optional) Voltage control signal for the memory voltage regulator. Can be configured to another free GPIO if GPIO_21 is used for other purposes.

3.21 Power and Ground Descriptions and Operating Conditions

Note:

- All power and ground pins must always be connected.

Table 3–24 Power and Ground Descriptions and Operating Conditions

Pin Name	Value	Description
Main Power and Ground Pins		
VDDC	0.700 V to 1.031 V	Dedicated core power, provides power to the internal logic. Refer to the Electrical Design Power section for the SVI2 and other requirements on VDDC. The voltage quoted is the set voltage through SVI2.
VDDCI	0.800 V to 0.875 V	Isolated (clean) core power for the l/O logic. Particular attention should be paid to minimize AC ripple on VDDCI.
FB_VDDC	—	Provides VDDC feedback path to the regulator. If unused, connect to a test point or leave not connected.

Pin Name	Value	Description
FB_VDDCI	—	Provides VDDCI feedback path to the regulator. If unused, connect to a test point or leave not connected.
FB_VMEMIO	—	Provides VMEMIO feedback path to the regulator. If unused, connect to a test point or leave not connected.
FB_VSS	—	Provides ground feedback path to the regulator. If unused, connect to a test point or leave not connected.
VDD_08	0.9 V	Digital power supply for PLL, PCIe, and display PHYs.
VDD_18	1.8 V	1.8-V I/O power for PLL, PCIe, and display PHYs.
TSVDD	1.8 V	On-die thermal sensor power.
VMEMIO (memory)	1.5 V	I/O power for the memory interface.
VDD_33	3.3 V	I/O power for 3.3-V pins, such as GPIOs.
VSS	Gnd	Ground.

Table 3–25 Other Signals

Pin Name	Type	Description
TEST_PG **TEST_PG_BACO**	I	TEST_PG and TEST_PG_BACO should be accessible for test purposes and must be pulled up to the 1.8-V power rail for normal operation.
TS_A	I	Reserved. Do not connect on the PCB.

3.22 Configuration Straps

3.22.1 GPIO Pin Straps

“Polaris 12” XL uses GPIO pin straps (i.e., one GPIO for one strap).

Some of the straps are on 3.3-V GPIOs while others are on 1.8-V GPIOs.

Each strap pin has either an internal pull-down resistor which provides a default value of 0, or an internal pull-up resistor which provides a default value of 1, at power up. For each strap that defaults to 0 by the GPU, provide a pull-up resistor option (to 3.3-V or 1.8-V depending on the GPIO type) on the PCB. For each strap that defaults to 1 by the GPU, provide a pull-down resistor option to GND on the PCB.

To change the straps from the default values, use pull-up or pull-down resistors of **5.1K Ω (5%)** on the PCB.

Any external circuit using these pins must not conflict with the logic level required by the strap after power up until PCIe reset gets de-asserted.

Table 3–26 Pin Straps

Strap Name	Pin Name	Description	GPU Default	Recommended Settings[1]
BIF_VGA_DIS	GPIO_29	Determine whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space). 0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).	0 (Internal pull-down)	Design dependent Provide a pull-up resistor option to VDD_33.
TX_DEEMPH_EN	GPIO_20	PCI Express transmitter de-emphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.	0 (Internal pull-down)	1 Through pull-up resistor to VDD_33.
TX_HALF_SWING	GPIO_0	Controls the transmitter full/half swing mode. 0: The transmitter full-swing is enabled. 1: The transmitter half-swing is enabled.	0 (Internal pull-down)	0 Provide a pull-up resistor option to VDD_33.
ROM_CONFIG[2:0]	GPIO_13 GPIO_12 GPIO_11	a) If BIOS_ROM_EN = 1, then ROM_CONFIG[2:0] defines the ROM type. See ROM Configurations (p. 42) for details. b) If BIOS_ROM_EN = 0, then ROM_CONFIG[2:0] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 42) for details.	101 (Internal pull-up/ pull-down)	Design dependent. Provide a pull-down resistor option to GND on the PCB for GPIO_13. Provide a pull-up resistor option to VDD_33 on the PCB for GPIO_12. Provide a pull-down resistor option to GND on the PCB for GPIO_11.
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device. **Note:** When an external BIOS ROM device is used, GPIO_22_ROMCSB also connects to the ROM device's chip select (active low).	1 (Internal pull-up)	Design dependent. Provide a pull-down resistor option to GND on the PCB.

Strap Name	Pin Name	Description	GPU Default	Recommended Settings[1]
Special Usage [1] Special Usage [0]	HSYNC VSYNC	Special usage	0 (Internal pull-down)	Design dependent. Refer to application note order #55739 on the special usage. Provide a pull-up resistor option to VDD_33 on the PCB for each pin.
AUD_PORT_CONN [2:0]	DBGDATA_2 DBGDATA_1 DBGDATA_0	Determine the maximum number of digital display audio endpoints that will be presented to the OS and user. This should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the GPU itself, the number and type of connectors on the board (DP/HDMI), and the number of sinks for each DP connector (the DP MST link policy of the video driver). Unused endpoints should be disabled. 111: No usable endpoints 110: One usable endpoint 101: Two usable endpoints 100: Three usable endpoints 011: Four usable endpoints 010: Five usable endpoints 001: Six usable endpoints 000: All endpoints are usable	0 (Internal pull-down)	Design dependent, see description. Provide a pull-up resistor option **to VDD_18** on the PCB for each pin.
BOARD_CONFIG [2:0]	DBGDATA_5 DBGDATA_4 DBGDATA_3	Provides an option to specify certain board-level specifics to the VBIOS or driver.	0 (Internal pull-down)	Design dependent. Provide a pull-up resistor option **to VDD_18** on the PCB for each pin.
SMBUS_ADDR [1:0]	DBGDATA_7 DBGDATA_6	Provide a strap option to change the SMBUS slave address of the GPU. 00: 0×40 01: 0×41 10: 0×42 11: 0×43	0 (Internal pull-down)	Design dependent. Provide a pull-up resistor option **to VDD_18** on the PCB for each pin. Strap on the PCB the address **to 0×41** if it does not cause address conflict on the platform.
BIF_GEN3_EN_A	GPIO_2	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.	1 (Internal pull-up)	Design dependent. Provide a pull-down resistor option to GND on the PCB.

Strap Name	Pin Name	Description	GPU Default	Recommended Settings[1]
BIF_CLK_PM_EN	GPIO_8_ROMSO	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.	0 (Internal pull-down)	1 Provide a pull-up resistor option to VDD_33 on the PCB.
Reserved	GPIO_15	Reserved	0 (Internal pull-down)	Must default to 0 for production. Provide a pull-up resistor option to VDD_33 on the PCB.
Reserved	GPIO_9_ROMSI	Reserved	0 (Internal pull-down)	Must default to 0 for production. Provide a pull-up resistor option to VDD_33 on the PCB.

Note:
1. To change the straps from the default values, use pull-up or pull-down resistors of **5.1K Ω (5%)** on the PCB.

3.22.2 ROM Configurations

For designs that have a dedicated ROM device for the GPU video BIOS:

- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
- Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).

3.22.3 Primary Memory Aperture Size

The following table shows the primary memory aperture sizes requested at PCI configuration.

Table 3–27 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110
4 GB	111

Note: The memory aperture size should be the same as the frame buffer size for 64 MB, 128 MB, and 256 MB. For a frame buffer size larger than 256 MB, memory aperture size should be set to 256 MB.
For designs requiring larger than 256 MB aperture size, consult with AMD.

3.22.4 ROM Straps for Add-in Card Design

If a dedicated ROM is used for the video BIOS (see ROM_CONFIG[2:0] and BIOS_ROM_EN in GPIO Pin Straps (p. 39)), then after PERSTB goes inactive (high), the ROM is read at the BIOS addresses and default BIOS settings in the following table.

The ROM straps are ORed with the corresponding pin straps.

Table 3–28 ROM Straps

Strap Name	Description	Default BIOS Setting
F0_64BAR_DIS_A	Enable 64-bit BAR for function 0. Affects bit 2 of BLOCK_MEM_TYPE for each BAR register in the PCI configuration space.	1
SUBSYS_VEN_ID	Subsystem vendor ID (SSVID) in the PCI configuration space. If a VBIOS ROM is not used, then the SBIOS is permitted to overwrite this register for each PCI function on the device before the enumeration cycle is initiated, otherwise the default value is used.	0x1002
F0_SUBSYS_ID	Subsystem ID (SSID) for the PCI configuration space for function 0. If enabled, SSID for the secondary display function (F1) is set to the same value as the primary display function (F0) with bit 0 inverted.	
F0_BAR_EN	0 = Disable resizable BAR feature. 1 = Enable resizable BAR feature.	1

Strap Name	Description	Default BIOS Setting
MEM_AP_SIZE[2:0]	Size of the primary memory apertures claimed in the PCI configuration space: If F0_BAR_EN = 1 (i.e., resizable BAR enabled): • 000: 256 MB to 1 GB • 001: 256 MB to 4 GB • 010: 256 MB to 8 GB • 011: 256 MB to 16 GB • 100: 128 MB to 1 GB • 101: 128 MB to 2 GB • 110: 128 MB to 8 GB • 111: 128 MB to 16 GB If F0_BAR_EN = 0 (i.e., resizable BAR disabled): • 000: 128 MB • 001: 256 MB • 010: 64 MB • 011: 8 GB • 100: 16 GB • 101: 1 GB • 110: 2 GB • 111: 4 GB When F0_BAR_EN = 0, the aperture size should be set to the same size as the frame buffer size for 64 MB, 128 MB, and 256 MB. For a frame bugger size larger than 256 MB, the aperture size should be set to 256 MB. For designs requiring larger than 256 MB aperture size, contact AMD.	Depends on the board configuration, see the description.
AUDIO_EN	Multi-function device select. Affects bit seven of the header register in the PCI configuration space. PCI configuration setting: 0 = Audio function not present. 1 = Audio function present. Boards with a ROM will require both the ROM and the specific pin straps to be set in order to enable the audio function. Boards without a ROM will only require the pin straps to be set in order to enable the audio function.	Depends on the board configuration, see the description.
VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in PCI configuration space): 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system’s VGA controller.	0
DEBUG_ACCESS	The debug access sets the debug MUX settings from the ROM in order to bring out internal signals for observation when registers are inaccessible through the host interface.	0

4

Timing Specifications

This chapter describes bus and memory timing specifications of “Polaris 12” XL.

To link to a topic of interest, use the following list of linked cross-references:

4.1 DRAM Timing

4.1.1 Programming Timing Values

The following tables show the memory-timing parameters that can be programmed through the registers MC_SEQ_RAS_TIMING, MC_SEQ_CAS_TIMING, MC_SEQ_MISC_TIMING, and MC_SEQ_MISC_TIMING2.

The MC_SEQ_RAS_TIMING register allows the programming of the row operation timing parameters.

Table 4–1 MC_SEQ_RAS_TIMING Parameters

Field	Bits	Description
TRCDW	4:0	ACTIVE to WRITE (in hclk) - 1.
TRCDWA	9:5	ACTIVE to WRITE with AUTO PRECHARGE (in hclk) - 1.
TRCDR	14:10	ACTIVE to READ (in hclk) - 1.
TRCDRA	19:15	ACTIVE to READ with AUTO PRECHARGE (in hclk) - 1.
TRRD	23:20	ACTIVE bank a to ACTIVE bank b (in hclk) - 1.
TRC	30:24	ACTIVE to ACTIVE (same bank)/AUTO REFRESH period (in hclk).
TRCDW	31	Most significant bit of TRCDW.

The MC_SEQ_CAS_TIMING register allows the programming of the column operation timing parameters.

Table 4–2 MC_SEQ_CAS_TIMING Parameters

Field	Bits	Description
TNOPW	1:0	Extra write pitch between bursts for debug purposes (in hclk).
TNOPR	3:2	Extra read pitch between bursts for debug purposes (in hclk).
TR2W	8:4	READ to WRITE turnaround time (in hclk) - 1.

Field	Bits	Description
TCCDL	11:9	Col to Col access delay – 1 (within the same bank group). GDDR5 only.
TR2R	15:12	READ to READ different rank (in hclk) - 1.
TW2R	20:16	WRITE to READ turn around time (in hclk) - 1.
TCL	28:24	CAS to read data return latency - 2 (0 to 20).

The MC_SEQ_MISC_TIMING and MC_SEQ_MISC_TIMING2 registers allow programming of miscellaneous timing parameters.

Table 4–3 MC_SEQ_MISC_TIMING Parameters

Field	Bits	Description
TRP_WRA	5:0	AUTO PRECHARGE to ACTIVE for WRITE (in hclk) - 1.
TRP_RDA	13:8	AUTO PRECHARGE to ACTIVE for READ (in hclk) - 1.
TRP	19:16	PRECHARGE command period (in hclk) - 1.
TRFC	28:20	AUTO REFRESH command period (in hclk) -1.
TRCDWA	29	Most significant bit of TRCDWA described in Table 4–1 (p. 45).
TRCDR	30	Most significant bit of TRCDR described in Table 4–1 (p. 45).
TRCDRA	31	Most significant bit of TRCDRA described in Table 4–1 (p. 45).

Table 4–4 MC_SEQ_MISC_TIMING2 Parameters

Field	Bits	Description
PA2RDATA	2:0	READ PREAMBLE (for GDDR4 only) (in hclk).
PA2WDATA	6:4	WRITE PREAMBLE (for GDDR4 only) (in hclk).
FAW	12:8	FOUR ACTIVE WINDOW (in mclk) - 5.
TREDC	15:13	READ EDC LATENCY in addition to READ DATA LATENCY (in hclk).
TWEDC	20:16	WRITE EDC LATENCY (in hclk)– 8.
T32AW	24:21	32 ACTIVE TIMING WINDOW (in mclk).
TWDATATR	24:21	DQ→WCMD timing for write training.

Table 4–5 Mapping DRAM Parameters to Programmed Values (GDDR5)

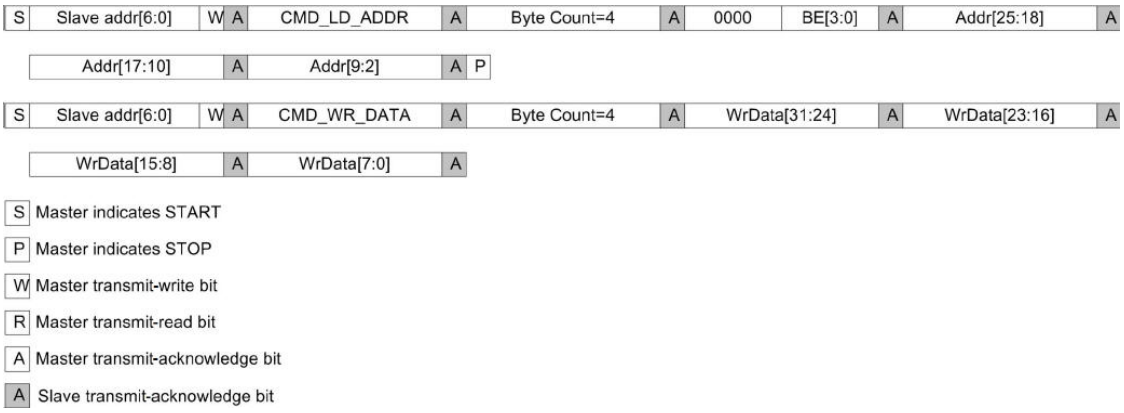
Parameter	Programmed Value	Unit
Burst Length	8	edge
YCLK	4000	MHz
HCLK (memory clock)	1000	MHz
MCLK	500	MHz
HCLK Period	1.0	ns

4.2 SMBus Timing

4.2.1 SMBus Write Cycle

The following figure shows an SRBM (system register bus manager) write cycle on the SMBus interface.

Figure 4–1 SMBus Write Cycle



A typical SMBus write cycle consists of the following steps:

1. Issuing a Load Address Command to the SMB_ADDR register:
   - **a.** The SMBus master issues a START bit to the slave.
   - **b.** The SMBus master issues 7-bit slave address to the slave.
   - **c.** The SMBus master issues a write bit to the slave.
   - **d.** The SMBus slave acknowledges the master.
   - **e.** The SMBus master issues an 8-bit CMD_LD_ADDR command to the slave.
   - **f.** The SMBus slave acknowledges the master.
   - **g.** The SMBus master sends a byte count (always 4).
   - **h.** The SMBus slave acknowledges the master.
   - **i.** The SMBus master issues a 4-bit byte enable with a 4-bit zero padding.
   - **j.** The SMBus slave acknowledges the master.
   - **k.** The SMBus master sends SMB_ADDR[25:18] to the slave.
   - **l.** The SMBus slave acknowledges the master.
   - **m.** The SMBus master sends SMB_ADDR[17:10] to the slave.
   - **n.** The SMBus slave acknowledges the master.
   - **o.** The SMBus master sends SMB_ADDR[9:2] to the slave.
   - **p.** The SMBus slave acknowledges the master.
   - **q.** The SMBus master sends a STOP bit to the slave.
2. Issuing a Write Data Command to the SMB_WR_DATA register:
   - **a.** The SMBus master issues a START bit to the slave.

b. The SMBus master issues a 7-bit slave address to the slave.

c. The SMBus master issues a write bit to the slave.

d. The SMBus slave acknowledges the master.

e. The SMBus master issues an 8-bit CMD_WR_DATA command to the slave.

f. The SMBus slave acknowledges the master.

g. The SMBus master sends a byte count (always 4).

h. The SMBus slave acknowledges the master.

i. The SMBus master sends SMB_WR_DATA[31:24] to the slave.

j. The SMBus slave acknowledges the master.

k. The SMBus master sends SMB_WR_DATA[23:16] to the slave.

l. The SMBus slave acknowledges the master.

m. The SMBus master sends SMB_WR_DATA[15:8] to the slave.

n. The SMBus slave acknowledges the master.

o. The SMBus master sends SMB_WR_DATA[7:0] to the slave.

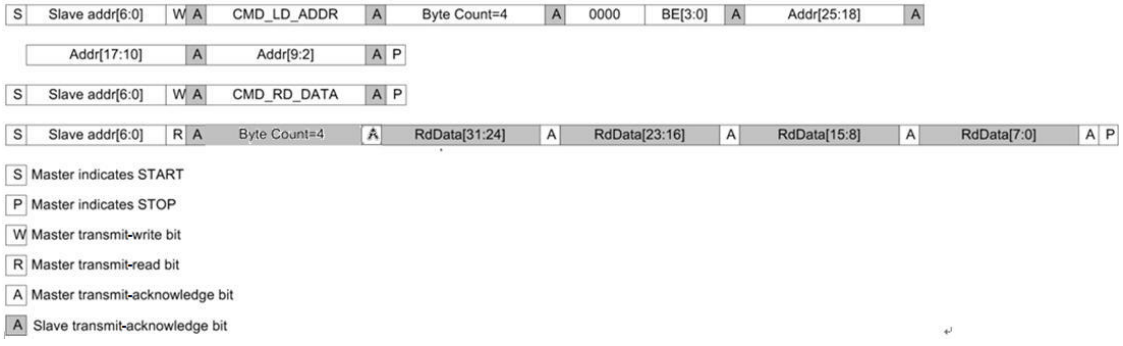
p. The SMBus slave acknowledges the master.

q. The SMBus master sends a STOP bit to the slave.

4.2.2 SMBus Read Cycle

The following figure shows an SRBM read cycle on the SMBus interface.

Figure 4–2 SMBus Read Cycle



A typical SMBus read cycle consists of the following steps:

1. Issuing a Load Address Command to the SMB_ADDR register:

a. The SMBus master issues a START bit to the slave.

b. The SMBus master issues a 7-bit slave address to the slave.

c. The SMBus master issues a write bit to the slave.

d. The SMBus slave acknowledges the master.

e. The SMBus master issues an 8-bit CMD_LD_ADDR command to the slave.

f. The SMBus slave acknowledges the master.

g. The SMBus master sends a byte count (always 4).

h. The SMBus slave acknowledges the master.

i. The SMBus master issues a 4-bit byte enable with a 4-bit zero padding. These bits should have no effect on the reads.

j. The SMBus slave acknowledges the master.

k. The SMBus master sends SMB_ADDR[25:18] to the slave.

l. The SMBus slave acknowledges the master.

m. The SMBus master sends SMB_ADDR[17:10] to the slave.

n. The SMBus slave acknowledges the master.

o. The SMBus master sends SMB_ADDR[9:2] to the slave.

p. The SMBus slave acknowledges the master.

q. The SMBus master sends a STOP bit to the slave.

2. Issuing a Read Data Command to the slave.

a. The SMBus master issues a START bit to the slave.

b. The SMBus master issues a 7-bit slave address to the slave.

c. The SMBus master issues a write bit to the slave.

d. The SMBus slave acknowledges the master.

e. The SMBus master issues an 8-bit CMD_RD_DATA command to the slave.

f. The SMBus slave acknowledges the master.

g. The SMBus master terminates the transaction with a STOP.

3. Issuing an SMBus read to the slave:

a. The SMBus master issues a START bit to the slave.

b. The SMBus master issues an 7-bit slave address to the slave.

c. The SMBus master issues a read bit to the slave.

d. The SMBus slave acknowledges the master.

e. The SMBus slave sends a byte count (always 4).

f. The SMBus master acknowledges the slave.

g. The SMBus slave sends SMB_RD_DATA[31:24] to the master.

h. The SMBus master acknowledges the slave.

i. The SMBus slave sends SMB_RD_DATA[23:16] to the master.

j. The SMBus master acknowledges the slave.

k. The SMBus slave sends SMB_RD_DATA[15:8] to the master.

l. The SMBus master acknowledges the slave.

m. The SMBus slave sends SMB_RD_DATA[7:0] to the master.

n. The SMBus master acknowledges the slave.

o. The SMBus master terminates the transaction with a STOP.

4.2.3 SMBus Read Thermal Sensor

Since SMU has moved thermal value register into indirect space, so if we want to access it, we need 2 indirect steps.

Programming sequence is shown below:

1. SMB Issue a Load Address Command(cmd1) to the SMC_IND_INDEX_7 address. (Tell SMBus slave the index address.)

   82 01 04 0f 00 00 8E

2. SMB Issue a Write Data Command(cmd2) to the thermal register real address. (Tell SMBus slave to write the real address to #1's index.)

   82 02 04 c0 30 00 14

3. SMB Issue a Load Address Command(cmd1) to the SMC_IND_DATA_7 (Tell SMBus slave the index pair's data address.)

   82 01 04 0f 00 00 8F

4. SMB Issue a Read Data Command(cmd3) (Tell SMBus slave to read out thermal value.)

   82 03 83 <value read back>

5. Repeat step 4.

4.3 Initialization Sequence and Timing

4.3.1 Initialization Sequence and Timing

1. Chip reset (PERSTB) is asserted, and PCIE_REFCLK starts running.
2. All GPIOs go to a tristate (input) mode at RESETB. Some GPIOs have internal pull-down (PD) or pull-up (PU) resistors—see descriptions of pin-based straps.
3. External pin straps are driving their values onto the GPU pins.
4. Chip reset (PERSTB) is deasserted.
5. External pin-strap values are latched internally.
6. In parallel:
   a. eFuse state machine begins to read "eFuse straps."
   b. If a ROM exists (and is programmed), a request is sent to the ROM controller to read the "ROM straps."

7. eFuse and ROM straps are "forwarded" to PHY.
8. In parallel:
    a. If GPU memory repair is required, then memory repair starts.
    b. eFuse and ROM straps are "forwarded" to other blocks in the GPU.
9. Wait for memory repair to complete. De-assert a hard reset to all the blocks including BIF. Enable PCIe® PHY impedance calibration. After polling for the PHY impedance calibration, distribute the remaining fuses and poll for BIF to complete its reset sequence.
10. The GPU begins link training according to the PCIe specification.

    After link training and the reset sequence are complete, the system is ready for the first transaction, such as a configuration space request.

The following figure and table provide an outline of the “Polaris 12” XL reset sequence.

Figure 4–3 Reset Sequence

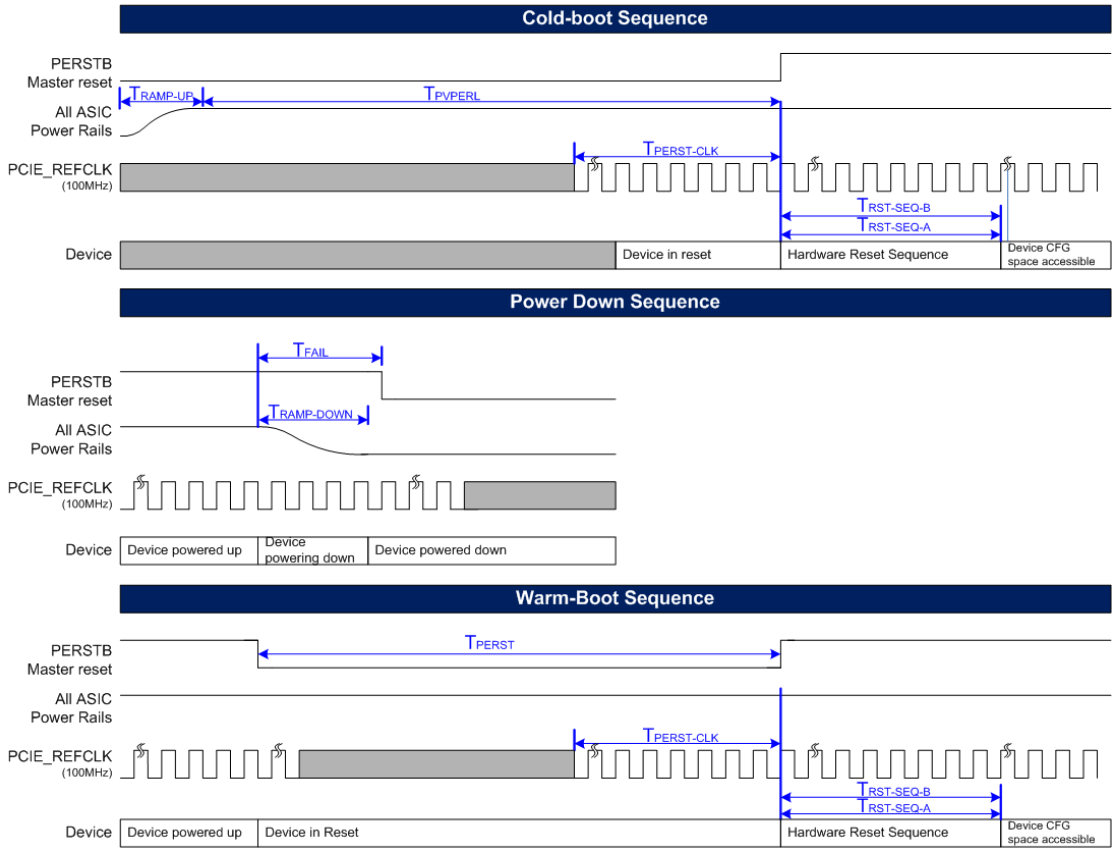


Table 4–6 Power-on Reset Sequence Timing Parameters

Parameter	Description	Minimum Time	Maximum Time
$T_{RAMP-UP}$	Power rail ramp-up time	0 ms	20 ms
T_{PVPERL}	All GPU power rails stable to PERSTB inactive	100 ms	Not limited
$T_{PERST-CLK}$	PCIE_REFCLK stable before PERSTB inactive	100 µs	Not limited

Parameter	Description	Minimum Time	Maximum Time
$T_{RST-SEQ-A}$	The time required by the GPU to complete its internal reset sequence, and become ready for PCI configuration space access	N/A	100 ms
$T_{RST-SEQ-B}$	The time the system software must wait after de-assertion of PERSTB before accessing the GPU's PCI configuration space	100 ms	Not limited
$T_{RAMP-DOWN}$	Power rail ramp-down time	0 ms	20 ms
T_{FAIL}	Power level invalid to PERSTB active	No requirements	No requirements
T_{PERST}	PERSTB active time	100 µs	Not limited

4.3.2 Standard Boot-up Sequence

1. PERSTB (fundamental reset) is asserted to the device.
2. Select internal-strap values are determined by the configuration of pin straps on a subset of GPIOs on the board.
3. PERSTB is deasserted, and pin-strap settings are latched permanently into the device (until PERSTB is asserted again, or the power is removed).
4. In parallel:
   a. The device begins to read "eFuse straps."
   b. If a ROM exists (and is programmed), the device begins to read "ROM straps" from its external ROM.

   Note: The system may not issue a configuration transaction to the device until the device internal reset sequence is complete.
5. For an add-in card implementation, the device completes reading the "ROM straps."
6. Device internal reset is complete. The system begins enumerating the devices attached to it by issuing configuration transactions.
7. The chip responds to any pending transaction requests, and the system continues PCI Express® enumeration, which sets up the configuration registers of the device.
8. The system copies the contents of the ROM into system memory, and executes the video BIOS, completing the device initialization. This occurs before POST begins in the system BIOS, based on the *PC 98 System Design Guide*.

   The device is ready for normal operation.

There are three configurations for strap/BIOS implementation:

Configuration 1. The controller is located on an add-in card, and there is access to a local video BIOS serial flash memory.

The ROM state machine of “Polaris 12” XL will read in all the "ROM-based straps" right after PERSTB reset is deasserted. There are a total of 33 DWORDs of "ROM-based straps" which are stored at byte locations 0x70 through 0xF4 in the serial flash memory. See Table 3–28 (p. 43) for details.

For “Polaris 12” XL, security features have been implemented to block access to the ROM when a fuse is set. After this, when the ROM needs to be accessed, external

software will have to message the SMU firmware which will authenticate the new ROM contents and write it out.

Configuration 2. The controller is located on the system motherboard and the video BIOS is stored in the system BIOS serial-flash memory (i.e., no dedicated ROM for the video BIOS).

The system BIOS will be responsible for loading the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID through an aliased address in the controller chip's configuration space. The reason for writing through an aliased address (16#4c) is that the configuration location 16#2c is read only. Any writes to this location (16#4c) will also change the content of the SUBSYSTEM_VENDOR_ID at 16#2c.

Configuration 3. A combination of configurations 1 and 2 (add-in card and device on the motherboard)

The system BIOS will take care of the graphics device on the motherboard as in case 2, while the chip on the add-in board will be taken care of as in case 1. This should cover the situation where the OS does not read the add-in card’s video BIOS because the ROM state machine from the graphics chip reads the "ROM-based straps" independently from the video BIOS.

Note: If neither the system BIOS nor the add-in card video BIOS supply the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID, their values default to the DEVICE_ID and VENDOR_ID respectively inside the chip.

4.4 Serial Flash Read/Write Timing

Figure 4–4 Serial Flash Write/Read Timing

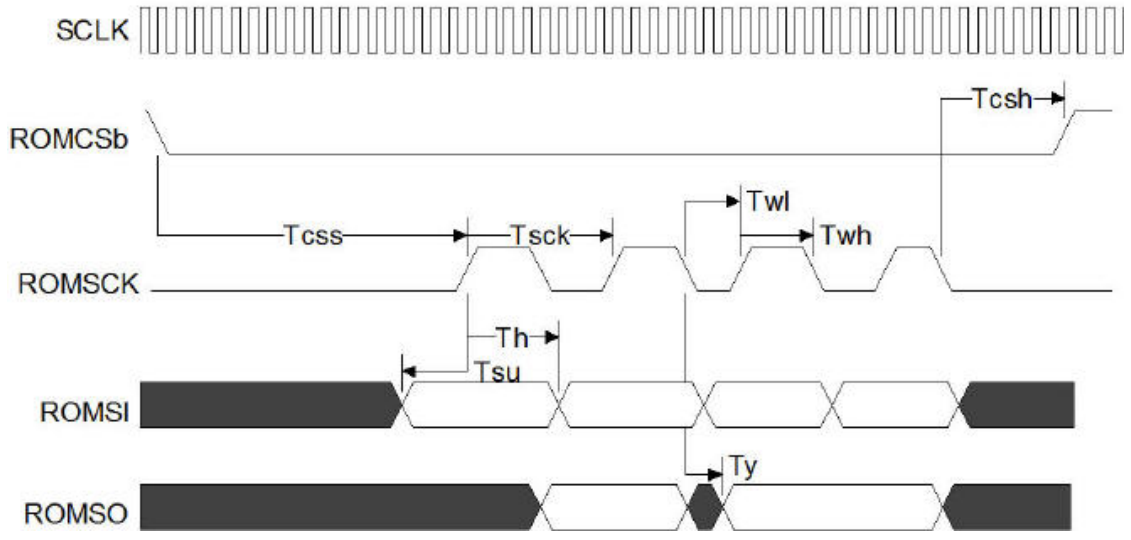


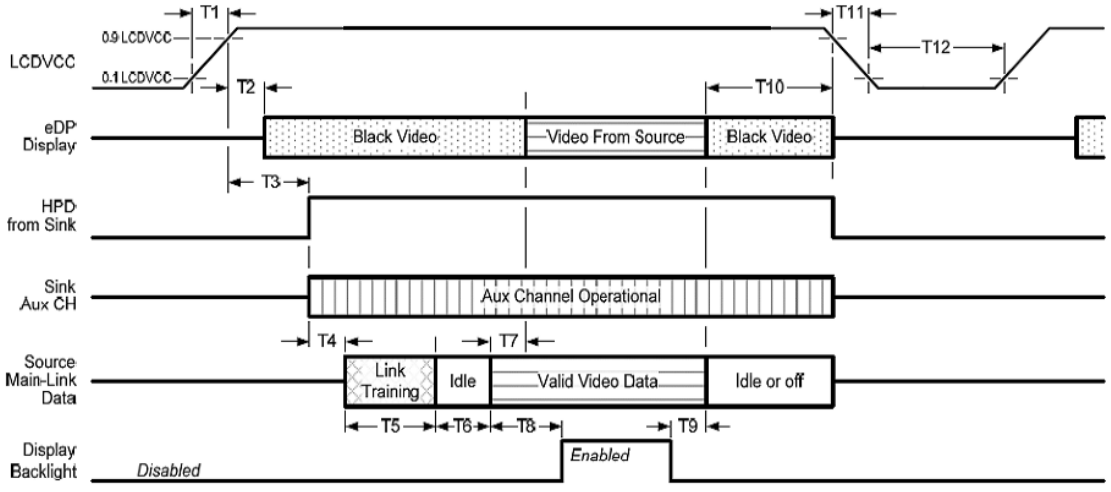
Table 4–7 Serial Flash Write/Read Timing Parameters for the Bootup Case

Symbol	Description	Min (ns)	Max (ns)
Tcss	ROMCSb falling edge to first clock sent to the device.	110	
Tsck	ROMSCK period.	70	
Twl	ROMSCK low time.	30	
Twh	ROMSCK high time.	30	

Symbol	Description	Min (ns)	Max (ns)
Tsu	ROMSI data setup.	20	
Th	ROMSI data hold.	40	
Ty	ROMSO data valid.	0	20
Tcsh	Last clock sent to the ROMCSb rising edge.	70	
SCLK = 100 MHz, XTALIN = 27 MHz, ROM_CNTL.SCK_PRESCALE_CRYSTAL_CLK=0x1			

4.5 LCD Panel Power-up/down Timing (eDP Interface)

Figure 4–5 eDP Panel Power-up/down Timing



Note: The Aux CH response from sink is dependent on the application of LCDVCC.

Table 4–8 Registers for Setting Backlight PWM Parameters

Parameter	Description	Time (ms)
T1+T2	Power rail rise time from 10% to 90% and delay from LCDVDCC to black video generation	Hardware controlled, up to 210 ms
T3	Delay from LCDVCC active to HPD high and Aux	Software controlled
T4	Delay from HPD high to link training initialization	Software controlled
T8	Delay from “Valid Video Data” to ENA_BL/VARY_BL active	Software controlled
T9	Delay from ENA_BL/VARY_BL inactive to the end of “Valid Video Data”	Software controlled
T10	Delay from “Source Main-Link Data” off to LCDVCC Off	Software controlled
T11	Power rail fall time from 90% to 10%	Hardware controlled, up to 10 ms
T12	Minimum panel off duration (off time is ≥ T12)	Software controlled

4.6 LCD Panel Backlight Control with PWM

Figure 4–6 Backlight PWM Parameters

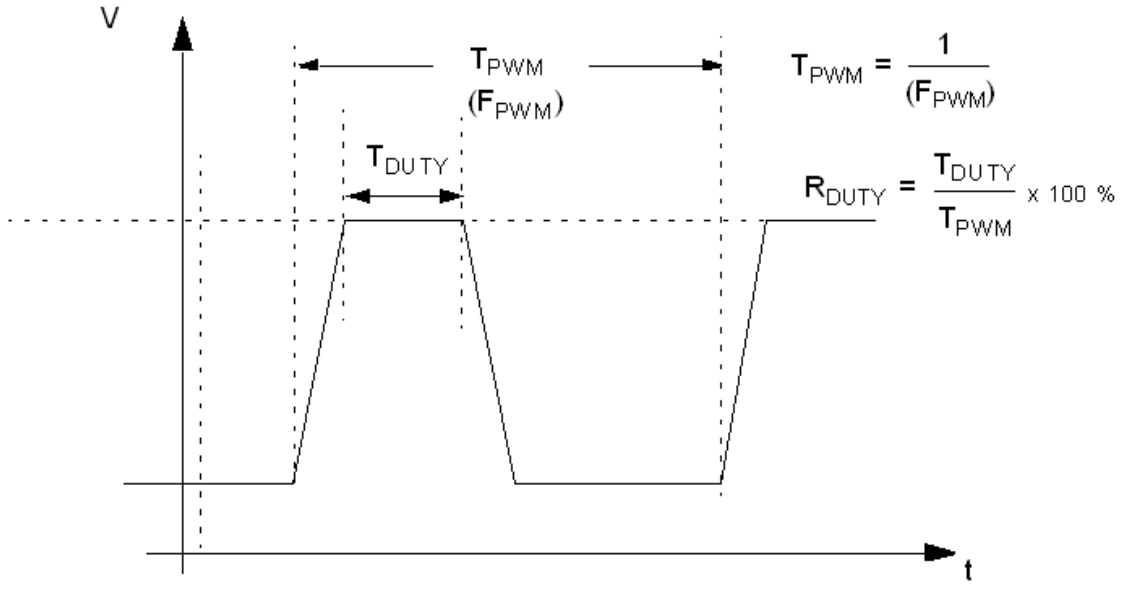


Table 4–9 Registers for Setting Backlight PWM Parameters

Register Field	Description
DISPOUT.LVTMA_PWRSEQ_REF_DIV.BL_PWM_REF_DIV	PWM frequency coarse control. This 16-bit value specifies the input reference clock divider. The frequency of the input reference clock (REF) is divided down by this amount specified. This value represents a divider of 1 to 65536. “0” is a special value that represents a divider of 65536. Other values (1 to 65535) map directly to the same divider value.
DISPOUT.BL_PWM_CNTL.BL_PWM_EN	Set to 1 to enable the PWM signal generator.
DISPOUT.BL_PWM_CNTL.BL_PWM_FRACTIONAL_EN	Set to 1 to enable fractional active duty-cycle mode. When enabled, the active duty cycle of each backlight period can vary over time to achieve the requested active duty cycle (both integer and fractional components) specified by the BL_ACTIVE_INT_FRAC_CNT value.
DISPOUT.BL_PWM_PERIOD_CNTL.BL_PWM_PERIOD_BITCNT	This 4-bit value has a dual purpose. First, it specifies the number of LSBs of the BL_PWM_PERIOD register used to represent the backlight period. The second purpose of this register is to specify how many MSBs of the BL_ACTIVE_INT_FRAC_CNT register field represent the integer component of the active duty cycle. The remaining LSBs of this register field represent the fractional component of the active duty cycle. For this register field, “0” is a special value that implies 16 bits are to be used for the period (and integer active duty cycle). Other values of 1 to 15 for this field directly map to the same number of bits to be used for the period (and MSBs of the active duty cycle as the integer component of the active duty-cycle value). When fractional active duty-cycle mode is enabled, this value should be programmed to the value that represents the smallest number of bits possible to represent the required backlight period.
DISPOUT.BL_PWM_PERIOD_CNTL.BL_PWM_PERIOD	PWM frequency fine control. Specifies the period of the backlight PWM signal. This 16-bit value represents the number of divided down input reference clock (REF /

Register Field	Description
	[BL_PWM_REF_DIV]) cycles in each backlight period. The BL_PWM_PERIOD_BITCNT register field represents how many LSBs of this register field, from 1 to 16, are actually used as the backlight period value.
DISPOUT.BL_PWM_CNTL.BL_ACTIVE_INT_FRAC_CNT	This 16-bit value specifies the backlight active duty cycle, in units of divided reference clock cycles (similar to the backlight period). This value consists of both an integer component and potentially a fractional component of the active duty cycle. The BL_PWM_PERIOD_BITCNT MSBs of this register field represent the integer component of the active duty cycle. This applies regardless of whether fractional active duty mode (BL_PWM_FRACTIONAL_EN) is enabled or disabled. The valid range for the integer component of the active duty cycle, contained in the (BL_PWM_PERIOD_BITCNT) MSBs of this register, is from 0 up to the BL_PWM_PERIOD value (contained in the (BL_PWM_PERIOD_BITCNT) LSBs of the BL_PWM_PERIOD register value). When fractional active duty cycle mode is enabled, the (16 - BL_PWM_PERIOD_CNT) LSBs of this register field represent the fractional component of the active duty cycle.

Table 4–10 Backlight PWM Parameters

Parameter	Description	Min	Typ	Max	Unit
REF	xtal_freq or xtal_freq × 2	—	27 or 54	—	MHz
F_{PWM}	Backlight PWM signal frequency. `= REF / ( [ (BL_PWM_PERIOD) × (BL_PWM_REF_DIV) ] )` where `REF` is the input reference clock frequency (typically 27 or 54 MHz), `BL_PWM_REF_DIV` is a 16-bit value specifying the division factor for this input reference clock, and `BL_PWM_PERIOD` is a 16-bit value representing the period of the backlight PWM signal in units of divided input reference clock cycles. Typical Range: 55 Hz to 50 kHz.	0.007	—	13 M	Hz
R_{DUTY}	Active duty cycle ratio. `= (BL_ACTIVE_INT_FRAC_CNT) / (BL_PWM_PERIOD)` Minimum duty cycle increment size is (1/65535) of BL_PWM_PERIOD.	0	—	100	%

The backlight pulse width modulation circuit generates a backlight PWM signal with a frequency:

```
= REFCLK / ( [ (BL_PWM_PERIOD) * (BL_PWM_REF_DIV) ] )
```

`REFCLK` is the input reference clock frequency (typically 27 or 54 MHz).

`BL_PWM_REF_DIV` is a 16-bit value specifying the division factor for this input reference clock.

`BL_PWM_PERIOD` is a 16-bit value representing the period of the backlight PWM signal in units of divided input reference clock cycles.

To set the backlight modulation,

1. Set the coarse frequency by selecting BL_PWM_REF_DIV:

   ```
   BL_PWM_REF_DIV = ceil (REF / (65535 ×
                            FTARGET))
   ```

2. Compute the fine frequency by selecting the period BL_PWM_PERIOD:

   ```
   BL_PWM_PERIOD = ceil (REF / (FTARGET ×
                            BL_PWM_REF_DIV))
   ```

   The period should be a value between 1 and 65535.

3. Compute the actual frequency:

   ```
   FINIT = REF / ((BL_PWM_PERIOD) ×
                            (BL_PWM_REF_DIV))
   ```

4. Compute the relative error:

   ```
   EINIT = (FTARGET – FINIT) / FTARGET
   ```

   Note:
   - For 50-kHz FTARGET, EINIT will equal zero (no error).
   - For 55-Hz FTARGET, EINIT will be less than 0.0006%.
   - The number of usable steps for the active duty cycle is (BL_PWM_PERIOD + 1), that is from 0% up to 100% active duty cycle.

5

Electrical Characteristics

This chapter describes the electrical characteristics of “Polaris 12” XL.

All voltages are with respect to VSS unless specified otherwise.

To link to a topic of interest, use the following list of linked cross-references:

5.1 Maximum Voltage Ranges

Note: The maximum voltage ranges are stress voltage ranges only, and the operation of the device at these conditions is not implied. Voltage ranges refer to the delta between FB_VDDC and FB_VSS, FB_VDDCI and FB_VSS, or power balls and VSS for rails that do not have voltage sensing feedback. Any stress voltage greater than the *absolute maximum range* may cause permanent damage to the device, or adversely affect the device reliability.

Table 5–1 Maximum Voltage Ranges

Supply	Maximum Voltage Range
VDDC, VDDCI	0 V to 1.075 V
VDD_33	0 V to 3.630 V
VMEMIO	0 V to 1.600 V
VDD_18, TSVDD	0 V to 1.980 V
VDD_08	0 V to 0.945 V

5.2 Electrical Design Power

The following table lists the estimated Thermal Design Current (TDC) numbers for all GPU power rails. Designers must ensure that their regulator circuits are capable of supplying continuous TDC safely. The regulator circuits must also meet AMD's

Electrical Design Current (EDC) requirement that is defined as the minimum current for which the voltage regulator must be capable of safely supplying for a minimum of 1 ms. This means that if a voltage regulator design can safely supply this amount of current for more than 1 ms, it meets AMD's EDC criterion. EDC can be estimated to be 1.5 times of TDC unless otherwise specified.

It is required that AMD's SVI2-compliant voltage controllers be used on all “Polaris 12” XL designs for VDDC. A SVI2-compliant voltage controller has two independent voltage domains built in such that one controller can deliver two power rails to the GPU, saving both cost and space compared to two-regulator solutions. Both voltage outputs are controlled through the high-speed SVI2 bus from dedicated GPU pins. The core domain of the SVI2 regulator should be used to power the VDDC rail, and the other domain can be used to power VDDCI.

All voltage regulators that are compliant with AMD's SVI2 specification use the SVT pin to serially stream real-time voltage and current telemetry to the GPU. “Polaris 12” XL uses the telemetry information to enable power management features. In order to maintain the accuracy of the current measurement, it is required that the passive current-sensing components have a tolerance less than or equal to ±5%. For example, if an inductor DCR (direct current resistance) is being used as the current-sensing element, the tolerance of the DCR must be less than or equal to ±5%. Full-scale current calibration is also required. Please refer to AMD's application note, order# 54265, for details on the calibration procedure.

For the power-up sequence requirements affected by the adoption of SVI2-compliant voltage regulators, refer to Power-up/down Sequence (p. 61).

To allow for driver optimizations, faster CPUs, and new applications, designers need to provide adequate electrical margins.

The numbers are preliminary estimates and subject to change.

Table 5–2 Regulator Guidelines

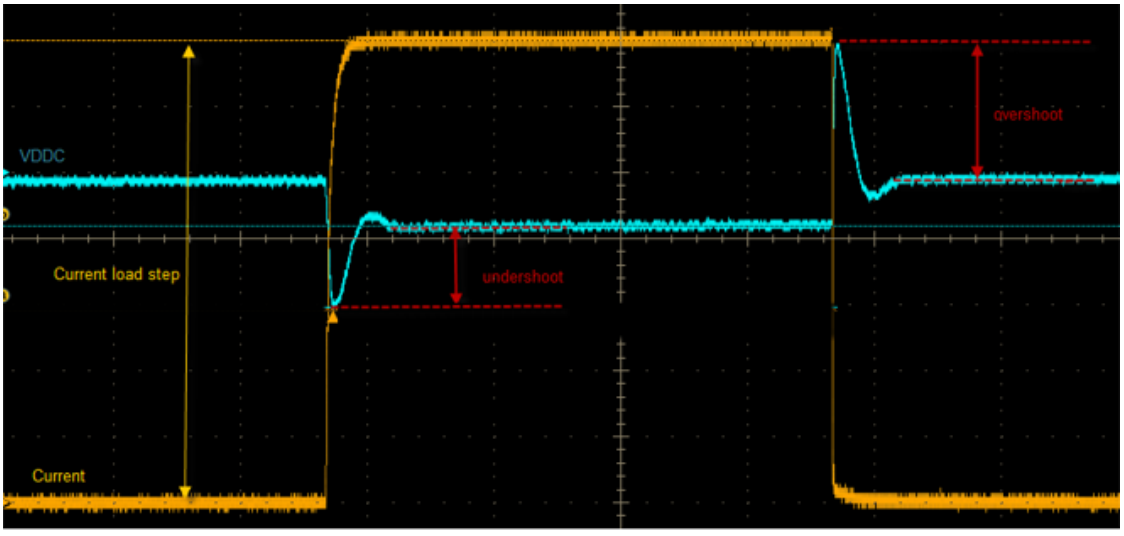
Rail Name	Nominal Voltage	DC Tolerance	AC Tolerance	Maximum Current	Notes
VDDC	0.700 V to 1.031 V	VID_VDDC - I_VDDC × 0.6 mΩ ± 20 mV	Overshoot: 175 mV Undershoot: 155 mV	36 A (TDC) 70 A (EDC)	1, 2, 4
VDDCI	0.800 V to 0.875 V	± 3%	± 3%	8 A (TDC)	
VDD_08	0.9 V	± 3%	± 3%	4 A (TDC)	
VMEMIO	1.5 V	± 3%	± 3%	2 A (TDC)	3

Rail Name	Nominal Voltage	DC Tolerance	AC Tolerance	Maximum Current	Notes
VDD_18	1.8 V	± 3%	± 3%	1 A (TDC)	5, 6
VDD_33	3.3 V	± 3%	± 3%	10 mA (TDC)	
TSVDD	1.8 V	± 3%	± 3%	13 mA	7

Note:

1. The SVI2 regulator can provide any voltage required on VDDC.
2. Undershoot and overshoot are conceptually illustrated in the following figure Electrical Design Power (p. 59). The set voltage is 1.0 V. The current load step is 35 A.
3. GPU consumption only and does not include memory parts. Consult with your memory vendor for additional current requirements to size the regulator.
4. AMD requires an effective load line of 0.6 mΩ on the VDDC rail.
5. If a switching regulator is used to power VDD_18, a filter inductor should be placed between the output of the regulator circuit and the GPU decoupling capacitors, and outside the feedback loop of the switching regulator. The filter inductor should be of 0.24 µH, and its DCR should be of 15 mΩ or less. The LDO solution does not need the filter inductor.
6. For the switching regulator, tolerance is defined at the 1.8-V regulator output before the filter inductor.
7. TSVDD can be merged with VDD_18 and powered by the same regulator.

Figure 5–1 Sample Undershoot and Overshoot



5.3 Power-up/down Sequence

“Polaris 12” XL has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/µs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 µs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.

5.4 TTL Interface Electrical Characteristics

The following table provides the electrical characteristics of the TTL Interface (GPIOs).

Table 5–3 DC Characteristics for 3.3-V GPIO Pads

Parameter	Condition	Min	Max	Unit	Notes
V_{IL}—input voltage low level.	Maximum DC voltage at the PAD pin that will produce a logic low.	—	0.7	V	—
V_{IH}—input voltage high level.	Minimum DC voltage at the PAD pin that will produce logic high.	1.7	—	V	—
V_{OL}—output voltage low level.	Maximum output low voltage @ I = 8 mA.	—	0.42	V	1, 2
V_{OH}—output voltage high level.	Minimum output high voltage @ I = 8 mA.	2.5	—	V	1, 2
I_{OL}—output current low level.	Minimum output low current @ V = 0.1 V.	1.9	—	mA	1, 2
I_{OH}—output current high level.	Minimum output high current @ V = VDDR - 0.1 V.	1.9	—	mA	1, 2

5.5 Memory Interface Electrical Characteristics

The following table provides the electrical characteristics of the memory interface.

Table 5–4 Memory Interface Electrical Characteristics

Parameters	Min	Typical	Max
GDDR5: **MVREFx, MVREFDx—input reference voltages.**	0.69 × VMEMIO	0.7 × VMEMIO	0.71 × VMEMIO
V_{IH-DC}—DC input logic high level.	MVREFDx + 100 mV	—	VMEMIO
V_{IL-DC}—DC input logic low level.	0	—	MVREFDx - 100 mV
V_{IH-AC}—AC input logic high level.	MVREFDx + 150 mV	—	—
V_{IL-AC}—AC input logic low level.	—	—	MVREFDx - 150 mV
$VOL(DC)_{VMEMIO = 1.5 V}$—output logic low-level voltage.	—	—	0.62 V
Note: • **Peak-to-peak AC noise on MVREFDx/MVREFx may not exceed ±25 mV.** • **VTT of the transmitting device must track VREF of the receiving device.** • **A 3-V/ns input-signal minimum slew rate is to be maintained for GDDR5.** • **The VI-xx voltage levels exceed the DRAM specification for GDDR5, leading to higher performance.**			

5.6 DDC I^2C Mode Electrical Characteristics

The following tables provide the electrical characteristics for the DDC pins in I^2C mode.

Table 5–5 Transmitter Electrical Specification for DDC I²C

Symbol	Description	Min	Max	Unit	Notes
I2C_Tx$_{Freq}$	Supported transmittable data rate.	—	400	kHz	-
I2C_V$_{OL}$	Maximum output low voltage @ I = 8 mA.	—	300	mV	1, 2, 3
I2C_V$_{OH}$	Minimum output high voltage.	VDD5 - 0.25	—	mV	1, 2, 3, 4

Note:
1. **For detailed current/voltage characteristics, refer to the IBIS model.**
2. **Measurement taken with NMOS strength set to default values, PVT = Noml case.**
3. **The I²C interface is an open-drain circuit and pull high is determined by external power.**
4. **VDD5 refers to a 5-V external pull up.**

Table 5–6 Receiver Electrical Specification for DDC I²C Pins

Symbol	Description	Min	Max	Unit	Notes
I2C_Y_V$_{IH-AC}$	Minimum AC voltage at the PAD pin that will produce a stable high at the I2C_Y pin of the macro.	2.3		V	3
I2C_Y_V$_{IL-AC}$	Maximum AC voltage at the PAD pin that will produce a stable low at the I2C_Y pin of the macro.		1.5	V	3
I2C_Y_V$_{IH-DC}$	Minimum DC voltage at the PAD pin that will produce a stable high at the I2C_Y pin of the macro.	2.3		V	1
I2C_Y_V$_{IL-DC}$	Maximum DC voltage at the PAD pin that will produce a stable low at the I2C_Y pin of the macro.		1.5	V	1
I2C_Y_Rx$_{Freq}$	Supported received frequency.		400	kHz	-
I2C_Y$_{dc}$	I2C_Y output duty cycle.	40	60	%	2

Note:
1. **Measured with an edge rate of 1 µs at the PAD pin.**
2. **Assuming perfect duty cycle on input.**
3. **Measured at the maximum operating frequency.**

5.7 DisplayPort AUX Electrical Specification

This table provides the electrical characteristics of the DisplayPort AUX.

Table 5–7 DisplayPort AUX Electrical Specification

Symbol	Description	Min	Max	Unit	Notes
AUX_V$_{cm}$	Input/output common-mode voltage.	550	620	mV	-
AUX_V$_{diff}$	Pad differential-output swing.	525	622	mV	-
AUX_Tx$_{Freq}$	Supported transmit-data rate.	—	5	MHz	-
AUX_Rx$_{Freq}$	Supported received frequency.	—	5	MHz	-
AUX_Pad$_{dc}$	PADP/N output duty cycle.	40	60	%	1

Note:
1. **Assuming perfect duty cycle on input.**

5.8 DisplayPort Main Link Electrical Characteristics

This table provides the electrical characteristics of the DisplayPort main link.

Table 5–8 DisplayPort Main Link Electrical Specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
UI_{HIGH_RATE}	Unit interval for the DP high bit rate (2.7 Gbps/lane).	—	370	—	ps	High limit = +300 ppm Low limit = -5300 ppm
UI_{LOW_RATE}	Unit interval for the DP reduced bit rate (1.62 Gbps/ lane).	—	617	—	ps	High limit = +300 ppm Low limit = -5300 ppm
UI_{HIGH_RATE2}	Unit interval for DP high-bit rate 2 (5.4 Gbps/lane).	—	185	—	ps	High limit = +300 ppm Low limit = -5300 ppm
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$	Ratio of output voltage level 1/ level 0.	0.8		6.0	dB	-
	Ratio of output voltage level 2/ level 1.	0.1		5.1	dB	-
$V_{TX\text{-}OUTPUT\text{-}RATIO\_HBR2}$	Ratio of output voltage level 2/ level 0.	5.2		6.9	dB	-
	Ratio of output voltage level 2/ level 1.	1.6		3.5	dB	-
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$	Delta of pre-emphasis level 1 versus level 0.	2.0			dB	-
	Delta of pre-emphasis level 2 versus level 1.	1.6			dB	-
$V_{TX\text{-}PREEMP\text{-}OFF}$	Maximum pre-emphasis when disabled.			0.25	dB	-

5.9 SMBus Electrical Characteristics

The following tables provide the electrical characteristics for the SMBus DATA, CLOCK, and CLK_REQB pads.

Table 5–9 Transmitter Electrical Specification

Symbol	Description	Min	Max	Unit
F_{TX}	Supported transmit data rate.	—	100	kHz
V_{OL}	Maximum output low voltage @ I = 4 mA.	—	400	mV
V_{OH}	Minimum output high voltage.	VDD33 - 0.4	—	mV

Table 5–10 Receiver Electrical Specification

Symbol	Description	Min	Max	Unit	Notes
VIH_{AC}	Minimum AC voltage at the PAD pin that will produce a stable high at the Y pin of the macro at FRX.	2.0	—	V	3
VIL_{AC}	Maximum AC voltage at the PAD pin that will produce a stable low at the Y pin of the macro.	—	0.8	V	3
VIH_{DC}	Minimum DC voltage at the PAD pin that will produce a stable high at the Y pin of the macro.	2.0	—	V	1

Symbol	Description	Min	Max	Unit	Notes
VIL_{DC}	Maximum DC voltage at the PAD pin that will produce a stable low at the Y pin of the macro.	—	0.8	V	1
F_{RX}	Supported received frequency.	—	100	kHz	-
Y_{dc}	Y output duty cycle.	40	60	%	2
Y_{tiPDr}	Receiver propagation delay rise.	—	400	ns	1, 2, 4
Y_{tiPDf}	Receiver propagation delay fall.	—	20	ns	1, 2, 4

1. **Measured with an edge rate of 1 µs at the PAD pin.**
2. **Assuming perfect duty cycle on input.**
3. **Measured at the maximum operating frequency.**
4. **Typical simulation corner only.**

6

Thermal Data

To link to a topic of interest, use the following list of linked cross-references:

6.1 Thermal Equations

For the thermal equations, the Delphi model is recommended.

Note: Thermal simulation models are available. Please refer to the AMD OEM Resource Center for more information.

6.2 Thermal Characteristics

For engineering design purposes, the thermal characteristics, $T_C$max and $T_J$max, found in the thermal simulation models are not practical as they are not easily determined. Instead, it is more convenient to define a new parameter, maximum recommended operating temperature ($T_{j,op}$), and re-define $T_{j,\ max}$ as shown in the following table:

Table 6–1 Thermal Characteristics

Variable	Value
$T_{j,op}$: Maximum recommended operating temperature. **This is the maximum temperature at which the functionality is qualified and tested. Operation above this temperature will negatively impact product reliability.** **This temperature is measured using an on-die temperature sensor near the integrated thermal diode (see Thermal Diode Characteristics (p. 68)).**	93°C
$T_{j,max}$: Absolute maximum rated junction temperature. **This is the maximum allowable instantaneous GPU temperature, above which damage to the GPU is likely.** **This temperature is measured using an on-die temperature sensor near the integrated thermal diode (see Thermal Diode Characteristics (p. 68)).**	99°C
Minimum ambient operating temperature.	0°C
θ_{JC}: Junction to case thermal resistance (based on the two-resistor model). **Note: Case here means the center of the top of the GPU package.**	0.07°C/W
θ_{JB}: Junction to board thermal resistance (based on the two-resistor model).	5.84°C/W

6.3 Thermal Design Power (TDP)

The thermal design power is defined as the power dissipated by the GPU while running a selected application at up to the maximum recommended operating temperature, and is measured as the maximum average power in a five-second moving window.

The TDP is intended as a recommended thermal design point; it is not an absolute maximum power under all conditions.

“Polaris 12” XL has up to eight defined Dynamic Power Management (DPM) states, from DPM_0 to DPM_7, in ascending order of performance and power. When a graphics demanding application (such as a game) is running, AMD's PowerTune constantly switches GPU among the states based on run-time analysis of GPU activities, power and thermal conditions. The effective power/performance depends on the percentage of time spent in each state.

The data are targets only, and are subject to change.

Table 6–2 TDP for Discrete Variants

Variant		**“Polaris 12” XL**
VDDC (V)		0.700 to 1.031
VDDCI (V)		0.800 to 0.875
Engine (MHz)	DPM_7	1183
	DPM_6	1124
	DPM_5	1098
	DPM_4	1046
	DPM_3	980
	DPM_2	734
	DPM_1	551
	DPM_0	214
Memory (MHz)		Up to 1750
Memory Voltage (V)		1.5
Memory Interface (bits)		128
GPU Leakage		Variable
GPU Die Temperature (°C)		93
Driver		17.30
Test Platform		Intel Core™i7-4790X Extreme Edition 3.6-GHz CPU, 16-GB RAM
PCIe® Configuration		PCIe revision 3.0, up to 8.0 GT/s
TDP Targets (W)		35

6.4 Thermal Diode Characteristics

For “Polaris 12” XL, the ideality factor of the on-die thermal diode varies significantly with temperature and sourcing current. If a design chooses to use the GPU's on-die thermal diode coupled with an external thermal sensor chip to read the GPU temperature, the external thermal sensor chip must support and enable beta compensation.

6.5 Storage Requirements

Ambient temperature < 40°C

Relative humidity < 90%

7

Mechanical Data

This chapter contains information on the mechanical data for “Polaris 12” XL. To go to a topic of interest, use the following list of linked cross-references:

7.1 Physical Dimensions

7.1.1 “Polaris 12” XL Physical Dimensions

Figure 7–1 “Polaris 12” XL Package Outline (MOD-00310 REV 01)

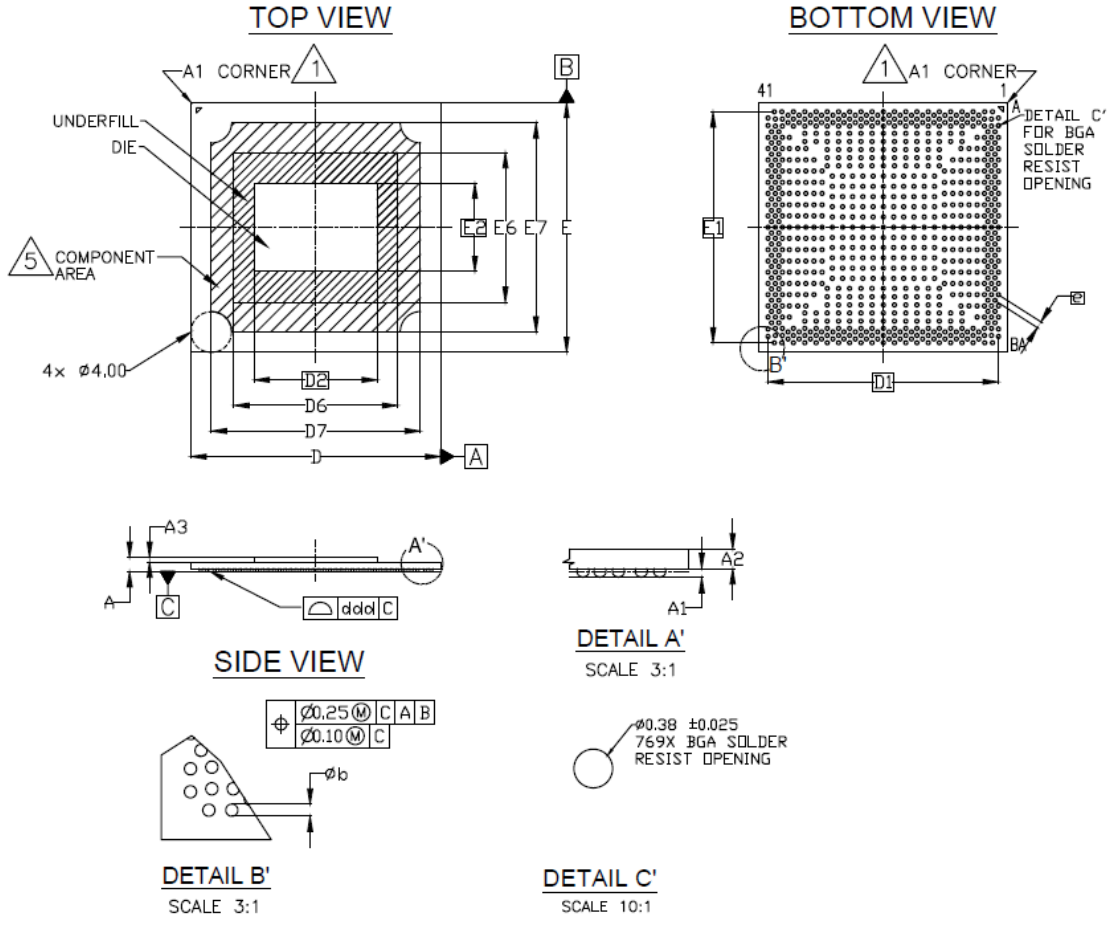


Table 7–1 Physical Dimensions (mm)

Symbol	Minimum	Normal	Maximum	Note
A	1.26	1.38	1.50	See side view.
A1	0.24	0.29	0.34	See side view.
A2	0.54	0.64	0.74	See side view.
A3	0.41	0.45	0.49	See side view.
øb	0.35	0.40	0.45	See bottom view.
D	24.40	24.50	24.60	See top view.
D1	—	22.60	—	See bottom view.
D2	—	12.07	—	See top view.
D6	16.07	—	—	See top view.
D7	—	—	20.50	See top view.
E	24.40	24.50	24.60	See top view.
E1	—	22.60	—	See top view.
E2	—	8.65	—	See top view.
E6	14.65	—	—	See top view.
E7	—	—	20.50	See top view.
e	0.65 BSC (basic)			See bottom view.
ddd	—	—	0.20	See side view.
N	769			Number of pins.

Note:
- **This is a multi-pitch (more than one pitch or distance on the substrate between the balls) package.**
- **The SMT (surface mount technology) component height from the substrate top surface is 0.31 mm maximum.**

7.2 Pressure Specification

To avoid damage to the GPU (die or solder-ball joint cracks) caused by improper mechanical assembly of the cooling device, follow the following recommendations:

- It is recommended that the maximum pressure that is evenly applied across the contact area between the thermal management device and the die does not exceed 75 PSI. A contact pressure of 30-40 PSI is adequate to secure the thermal management device and to achieve the lowest thermal contact resistance with a temperature drop across the thermal interface material of no more than 3°C. Also, the surface flatness of the metal spreader should be 0.001 inch/1 inch.
- Pre-test the assembly fixture with a strain gauge to ensure that the flexing of the final assembled board and the pressure applying around the GPU package will not exceed 600-micron strain under any circumstance.
- Ensure that any distortion (bow or twist) of the board after SMT and cooling device assembly is within industry guidelines (IPC/EIA J-STD-001). For the measurement method, refer to the industry approved technique described in the manual, *IPC-TM-650*, section 2.4.22.

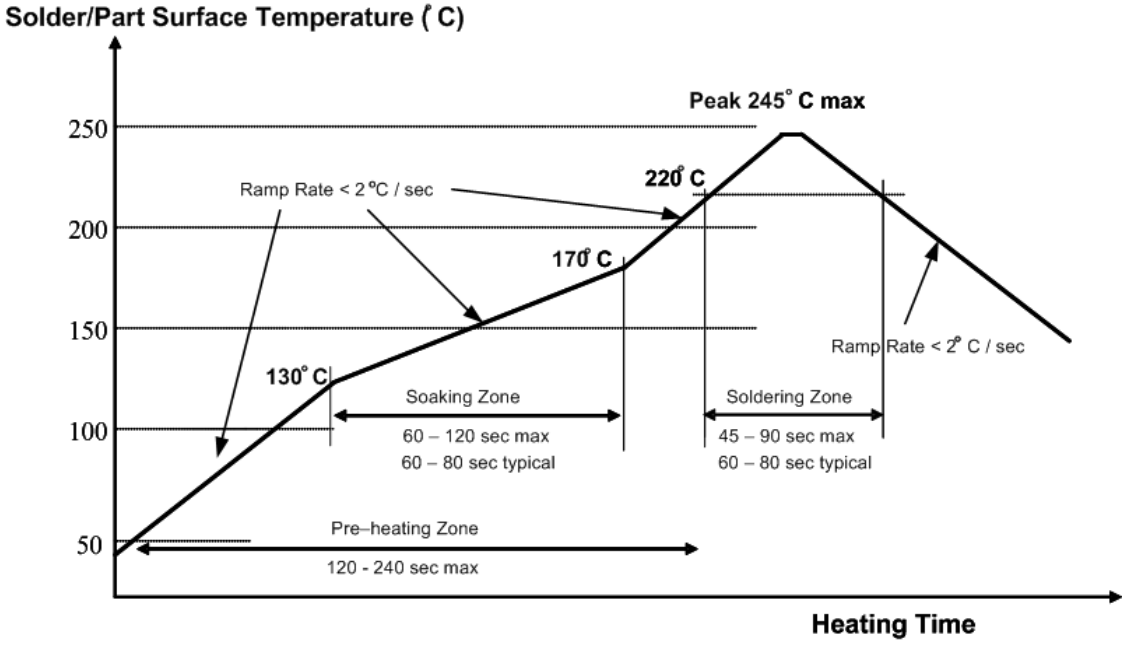
7.3 Board Solder Reflow Process Recommendations

7.3.1 Stencil Opening Size for Solderball Pads on PCB

Warpage of the PCB and the BGA package may cause solder-joint quality issues at the surface mount. Therefore, it is recommended that the stencil opening sizes be adjusted to compensate for the warpage. The recommendation is for the stencil aperture of BGA balls to be kept as the same size as the PWB BGA pad design.

7.3.2 FCBGA Reference Reflow Profile for RoHS/Lead-free Solder

Figure 7–2 FCBGA Reference Reflow Profile for RoHS/Lead-Free SMT



Notes when using RoHS/lead-free solder (SAC305 Tin-Silver-Cu):

- The final reflow temperature profile will depend on the type of solder paste and chemistry of flux used in the SMT process or BGA rework process. Modifications to this reference reflow profile may also be required in order to accommodate to other critical components.
- The use of a reflow oven with 10 heating zones or above is highly recommended.
- To ensure that the reflow profile meets the target specification on both sides of SMT components, a different reflow profile for the first and second reflow may be required.
- A mechanical stiffening carrier boat can be used to minimize PWB warpage during the reflow process.

- It is suggested to decrease the temperature cooling rate to minimize BGA component and PWB warpage.
- This recommended reflow profile applies only to the RoHS/lead-free (high temperature) soldering process, and it should not be applied to Eutectic solder packages without any reliability validation.
- Maximum three reflows are allowed on the same part.

Table 7–2 Recommended Profiling — RoHS/Lead-Free Solder

Profiling Stage	Temperature	Process Range
Overall Preheat	Room temperature to 220℃	Two to four minutes
Soaking Time	130℃ to 170℃	Typically 60 to 80 seconds
Liquidus	220℃	Typically 60 to 80 seconds
Ramp Rate	Ramp up and cooling	< 2℃ / second
Peak	Maximum 245℃	235℃ ± 5℃
Temperature at Peak Within 5℃	240℃ to 245℃	10 to 30 seconds

8

Boundary Scan Specification

This chapter contains information on boundary scan specifications as they apply to “Polaris 12” XL. To go to a topic of interest, use the following list of linked cross-references:

8.1 Introduction

“Polaris 12” XL has a JTAG 1149.1 compliant TAP controller. The boundary scan implementation is IEEE compliant. The implementation supports BYPASS, EXTEST, and PRELOAD instructions. A BSDL file for each of the modes can be obtained from the AMD OEM Resource Center.

8.2 Boundary Scan

The “Polaris 12” XL boundary scan can perform board-level capture and drive out on all pins mentioned in the BSDL file.

8.3 JTAG Interface Signals

Table 8–1 JTAG Interface

Pin-name	I/O	Description
JTAG_TCK	I	TCK: Test clock.
JTAG_TMS	I	TMS: Test mode select.
JTAG_TDI	I	TDI: Test data in.
JTAG_TDO	O	TDO: Test data out.
JTAG_TRSTB	I	TRST#: Test asynchronous reset.
TESTEN	I	Compliance pin: Pull up to 3.3 V to enable JTAG access.

8.4 JTAG Timing Characteristics

Table 8–2 JTAG Timing Characteristics

Symbol	Description	Min	Max
f_{cyc}	Frequency of operation.	0.001 MHz	10 MHz
t_{cyc}	TCK cycle period.	0.10 µs	1000 µs
t_{bsst}	Input data setup time to TCK rise.	15 ns	
t_{bsht}	Input data hold time to TCK rise.	20 ns	
t_{bsdv}	TCK low to output data valid.	0.00 µs	0.05 µs
t_{tcst}	TDI, TMS setup time to TCK rise.	2.5 ns	
t_{tcht}	TDI, TMS hold time to TCK rise.	3.0 ns	
t_{tcdv}	TCK low to TDO data valid.	0.0 µs	0.05 µs

Figure 8–1 Timing of the Boundary Scan Signals with Respect to TCK

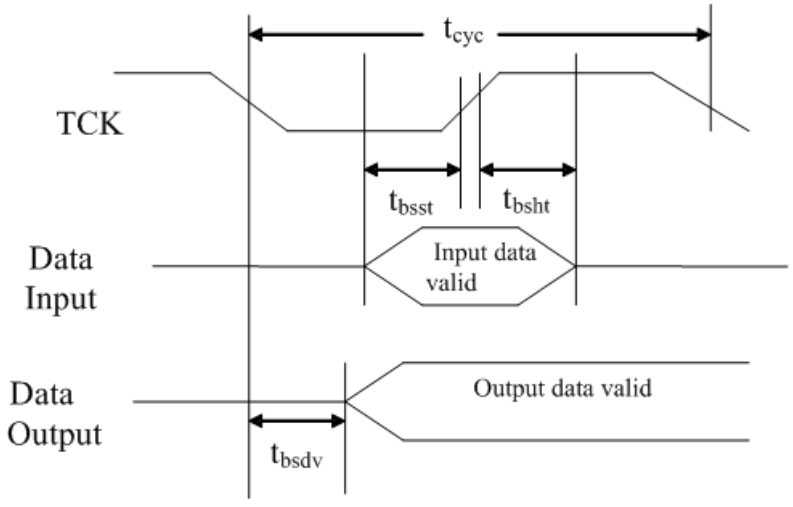
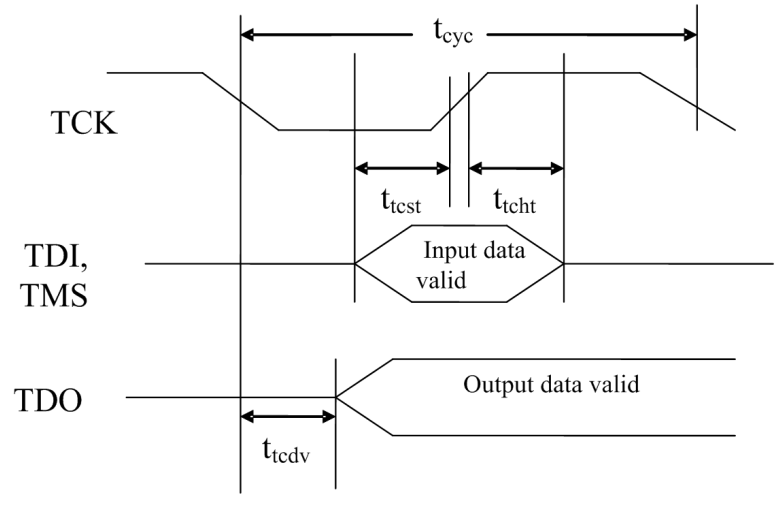


Figure 8–2 Timing of the TAP Ports (TDI, TMS, and TDO) with Respect to TCK



Appendix A

Pin Listings

This appendix contains pin listings for “Polaris 12” XL sorted in two ways. To go to the listing of interest, use the following list of linked cross-references:

- Pins Sorted by Ball Reference (p. 77)
- Pins Sorted by Signal Name (p. 95)

A.1 Pins Sorted by Ball Reference

Table A–1 “Polaris 12” XL Pins Sorted by Ball Reference

Ball Reference	Signal Name
A2	VSS
A3	DQA1_30
A4	DQA1_28
A5	VSS
A6	DQA1_27
A7	DQA1_25
A8	WCKA1_1
A9	VSS
A10	DQA1_22
A11	DQA1_20
A12	DDBIA1_2
A13	VSS
A14	DQA1_17
A15	DQA1_15
A16	DQA1_13
A17	VSS
A18	EDCA1_1
A19	DQA1_11
A20	DQA1_9
A21	VSS
A22	WCKA1_0
A23	DQA1_6
A24	DQA1_4
A25	VSS
A26	DQA1_3
A27	DQA1_1

Ball Reference	Signal Name
A28	DQA0_31
A29	VSS
A30	DQA0_28
A31	EDCA0_3
A32	DQA0_26
A33	VSS
A34	WCKA0_1
A35	DQA0_23
A36	DQA0_21
A37	VSS
A38	DDBIA0_2
A39	DQA0_18
A40	VSS
B1	VSS
B2	TEST6
B3	DQA1_31
B4	DQA1_29
B5	DDBIA1_3
B6	EDCA1_3
B7	DQA1_26
B8	DQA1_24
B9	WCKA1B_1
B10	DQA1_23
B11	DQA1_21
B12	EDCA1_2
B13	DQA1_19
B14	DQA1_18
B15	DQA1_16
B16	DQA1_14
B17	DQA1_12
B18	DDBIA1_1
B19	DQA1_10
B20	DQA1_8
B21	WCKA1B_0
B22	DQA1_7
B23	DQA1_5
B24	EDCA1_0
B25	DDBIA1_0
B26	DQA1_2
B27	DQA1_0
B28	DQA0_30
B29	DQA0_29

Ball Reference	Signal Name
B30	DDBIA0_3
B31	DQA0_27
B32	DQA0_25
B33	DQA0_24
B34	WCKA0B_1
B35	DQA0_22
B36	DQA0_20
B37	EDCA0_2
B38	DQA0_19
B39	DQA0_17
B40	VSS
B41	VSS
C1	DQB0_1
C2	DQB0_0
C3	FB_VMEMIO
C5	VSS
C7	VSS
C9	VSS
C11	VSS
C13	VSS
C15	VSS
C17	VSS
C19	VSS
C21	VSS
C23	VSS
C25	VSS
C27	VSS
C29	VSS
C31	VSS
C33	VSS
C35	VSS
C37	VSS
C39	VSS
C40	DQA0_16
C41	DQA0_15
D1	DQB0_3
D2	DQB0_2
D7	CLKA1
D9	CLKA1B
D11	WEA1B
D13	MAA1_3
D15	MAA1_8

Ball Reference	Signal Name
D17	CASA1B
D19	RASA1B
D21	RASA0B
D23	CASA0B
D25	MAA0_8
D27	MAA0_3
D29	MAA0_4
D31	CLKA0B
D33	WCKA0_0
D35	DQA0_7
D40	DQA0_14
D41	DQA0_13
E1	VSS
E2	DDBIB0_0
E3	VSS
E4	VSS
E7	CSA1B_0
E9	VSS
E11	MAA1_9
E13	VSS
E15	MAA1_0
E17	VSS
E19	CKEA1
E21	VSS
E23	MAA0_7
E25	VSS
E27	MAA0_2
E29	VSS
E31	CLKA0
E33	WCKA0B_0
E35	DQA0_6
E38	DQA0_5
E39	VSS
E40	DQA0_12
E41	VSS
F1	DQB0_4
F2	EDCB0_0
F40	DDBIA0_1
F41	EDCA0_1
G1	DQB0_6
G2	DQB0_5
G3	VSS

Ball Reference	Signal Name
G4	CLKB0
G5	CSB0B_0
G7	VSS
G11	VSS
G13	MAA1_2
G15	VSS
G17	MAA1_7
G19	VSS
G21	CKEA0
G23	VSS
G25	MAA0_0
G27	VSS
G29	WEA0B
G31	VSS
G35	VSS
G37	DQA0_4
G38	EDCA0_0
G39	VSS
G40	DQA0_11
G41	DQA0_10
H1	WCKB0_0
H2	DQB0_7
H11	MAA1_4
H13	MAA1_5
H15	MAA1_1
H17	MAA1_6
H19	ADBIA1
H21	ADBIA0
H23	MAA0_6
H25	MAA0_1
H27	MAA0_5
H29	MAA0_9
H31	CSA0B_0
H40	DQA0_9
H41	DQA0_8
J1	VSS
J2	WCKB0B_0
J3	VSS
J4	CLKB0B
J5	VSS
J7	TEMPINRETURN
J8	TEMPIN0

Ball Reference	Signal Name
J34	VSS
J35	DQA0_3
J37	VSS
J38	DDBIA0_0
J39	VSS
J40	VSS
J41	VSS
K1	DQB0_9
K2	DQB0_8
K11	VMEMIO
K13	VMEMIO
K15	MEM_CALRA
K17	MVREFDA
K19	VMEMIO
K21	VSS
K23	VMEMIO
K25	VSS
K27	VMEMIO
K29	VSS
K31	VMEMIO
K40	VSS
K41	RSVD
L1	DQB0_11
L2	DQB0_10
L3	VSS
L4	WEB0B
L5	MAB0_9
L7	VSS
L8	MAB0_4
L10	VMEMIO
L11	VSS
L13	VDDCI
L15	VSS
L17	VDDCI
L19	VSS
L21	VDDCI
L23	VSS
L25	VDDCI
L27	VSS
L29	VDDCI
L31	VSS
L32	DRAM_RSTA

Ball Reference	Signal Name
L34	DQA0_0
L35	VSS
L37	DQA0_1
L38	DQA0_2
L39	VSS
L40	DBGDATA_0
L41	DBGDATA_1
M1	DDBIB0_1
M2	EDCB0_1
M40	DBGDATA_2
M41	DBGDATA_3
N1	VSS
N2	DQB0_12
N3	VSS
N4	MAB0_3
N5	VSS
N7	MAB0_2
N8	MAB0_5
N10	VMEMIO
N11	VDDCI
N13	VDDC
N15	VDDC
N17	VSS
N19	VSS
N21	VDDC
N23	VDDC
N25	VSS
N27	VSS
N29	VDDC
N31	VDDC
N32	VSS
N34	DMINUS
N35	DPLUS
N37	VSS
N38	TS_A
N39	VSS
N40	DBGDATA_4
N41	DBGDATA_5
P1	DQB0_14
P2	DQB0_13
P40	DBGDATA_6
P41	DBGDATA_7

Ball Reference	Signal Name
R1	DQB0_16
R2	DQB0_15
R3	VSS
R4	MAB0_8
R5	MAB0_0
R7	VSS
R8	MAB0_1
R10	MEM_CALRB
R11	VSS
R13	VDDC
R15	VDDC
R17	VSS
R19	VSS
R21	VDDC
R23	VDDC
R25	VSS
R27	VSS
R29	VDDC
R31	VDDC
R32	VSS
R34	RSVD
R35	VSS
R37	GPIO_17_THERMAL_INT
R38	GPIO_19_CTF
R39	VSS
R40	DBGDATA_8
R41	DBGDATA_9
T1	DQB0_18
T2	DQB0_17
T40	DBGDATA_10
T41	DBGDATA_11
U1	VSS
U2	DQB0_19
U3	VSS
U4	CASB0B
U5	VSS
U7	MAB0_7
U8	MAB0_6
U10	MVREFDB
U11	VDDCI
U13	VDDC
U15	VDDC

Ball Reference	Signal Name
U17	VSS
U19	VSS
U21	VDDC
U23	VDDC
U25	VSS
U27	VSS
U29	VDDC
U31	VDDC
U32	VSS
U34	GPIO_16_8P_DETECT
U35	GPIO_6_TACH
U37	VSS
U38	GPIO_28_FDO
U39	VSS
U40	DBGDATA_12
U41	DBGDATA_13
V1	EDCB0_2
V2	DDBIB0_2
V40	DBGDATA_14
V41	DBGDATA_15
W1	DQB0_20
W2	DQB0_21
W3	VSS
W4	RASB0B
W5	CKEB0
W7	VSS
W8	ADBIB0
W10	VMEMIO
W11	VSS
W13	VDDC
W15	VDDC
W17	VSS
W19	VSS
W21	VDDC
W23	VDDC
W25	VSS
W27	VSS
W29	VDDC
W31	VDDC
W32	VDD_08
W34	HSYNC
W35	VSYNC

Ball Reference	Signal Name
W37	GPIO_29
W38	GPIO_30
W39	VSS
W40	GPIO_0
W41	GPIO_11
Y1	DQB0_22
Y2	DQB0_23
Y40	GPIO_12
Y41	GPIO_13
AA1	VSS
AA2	WCKB0B_1
AA3	VSS
AA4	RASB1B
AA5	VSS
AA7	CKEB1
AA8	ADBIB1
AA10	VSS
AA11	VDDCI
AA13	VDDC
AA15	VDDC
AA17	VSS
AA19	VSS
AA21	VDDC
AA23	VDDC
AA25	VSS
AA27	VSS
AA29	VDDC
AA31	VDDC
AA32	VSS
AA34	GPIO_5_REG_HOT_AC_BATT
AA35	GPIO_2
AA37	BP_1
AA38	BP_0
AA39	VSS
AA40	GPIO_1
AA41	GPIO_15
AB1	WCKB0_1
AB2	DQB0_24
AB40	GPIO_20
AB41	GPIO_21
AC1	DQB0_25
AC2	DQB0_26

Ball Reference	Signal Name
AC3	VSS
AC4	CASB1B
AC5	MAB1_7
AC7	VSS
AC8	MAB1_6
AC10	VMEMIO
AC11	VSS
AC13	VDDC
AC15	VDDC
AC17	VSS
AC19	VSS
AC21	VDDC
AC23	VDDC
AC25	VSS
AC27	VSS
AC29	VDDC
AC31	VDDC
AC32	VDD_08
AC34	SDA
AC35	SCL
AC37	BL_ENABLE
AC38	BL_PWM_DIM
AC39	VSS
AC40	DIGON
AC41	PX_EN
AD1	DQB0_27
AD2	EDCB0_3
AD40	JTAG_TDI
AD41	JTAG_TMS
AE1	VSS
AE2	DDBIB0_3
AE3	VSS
AE4	MAB1_8
AE5	VSS
AE7	MAB1_0
AE8	MAB1_1
AE10	VSS
AE11	VDDCI
AE13	VDDC
AE15	VDDC
AE17	VSS
AE19	VSS

Ball Reference	Signal Name
AE21	VDDC
AE23	VDDC
AE25	VSS
AE27	VSS
AE29	VDDC
AE31	VDDC
AE32	VSS
AE34	SWAPLOCKB
AE35	VSS
AE37	PCIE_TX7P
AE38	PCIE_TX7N
AE39	VSS
AE40	TESTEN
AE41	JTAG_TCK
AF1	DQB0_28
AF2	DQB0_29
AF40	JTAG_TRSTB
AF41	JTAG_TDO
AG1	DQB0_30
AG2	DQB0_31
AG3	VSS
AG4	MAB1_3
AG5	MAB1_2
AG7	VSS
AG8	MAB1_5
AG10	VMEMIO
AG11	VSS
AG13	VDDC
AG15	VDDC
AG17	VSS
AG19	VSS
AG21	VDDC
AG23	VDDC
AG25	VSS
AG27	VSS
AG29	VDDC
AG31	VDDC
AG32	VDD_08
AG34	SWAPLOCKA
AG35	VDD_08
AG37	PCIE_TX6P
AG38	PCIE_TX6N

Ball Reference	Signal Name
AG39	VSS
AG40	VSS
AG41	VSS
AH1	DQB1_0
AH2	DQB1_1
AH40	PCIE_RX7N
AH41	PCIE_RX7P
AJ1	VSS
AJ2	DQB1_2
AJ3	VSS
AJ4	MAB1_4
AJ5	VSS
AJ7	WEB1B
AJ8	MAB1_9
AJ10	VSS
AJ11	VSS
AJ13	VDDC
AJ15	VDDC
AJ17	VDDC
AJ19	VDDC
AJ21	VDDC
AJ23	VDDC
AJ25	VDDC
AJ27	VDDC
AJ29	VDDC
AJ31	VDDC
AJ32	VDD_08
AJ34	VDD_08
AJ35	VSS
AJ37	PCIE_TX5P
AJ38	PCIE_TX5N
AJ39	VSS
AJ40	PCIE_RX6N
AJ41	PCIE_RX6P
AK1	DQB1_3
AK2	DDBIB1_0
AK40	PCIE_RX5N
AK41	PCIE_RX5P
AL1	EDCB1_0
AL2	DQB1_4
AL3	VSS
AL4	CLKB1B

Ball Reference	Signal Name
AL5	CLKB1
AL7	VSS
AL8	CSB1B_0
AL10	VSS
AL11	VSS
AL13	VDDC
AL15	VDDC
AL17	VDDC
AL19	VDDC
AL21	VDDC
AL23	VDDC
AL25	VDDC
AL27	VDDC
AL29	VDDC
AL31	VDDC
AL32	VSS
AL34	VDD_08
AL35	VSS
AL37	PCIE_TX4P
AL38	PCIE_TX4N
AL39	VSS
AL40	PCIE_RX4N
AL41	PCIE_RX4P
AM1	DQB1_5
AM2	DQB1_6
AM11	DRAM_RSTB
AM13	TSVDD
AM15	VDD_18
AM17	VSS
AM19	AUX2N
AM21	DDCAUX3P
AM23	VSS
AM25	GPIO_9_ROMSI
AM27	GPIO_10_ROMSCK
AM29	GENERICG
AM31	VDD_33
AM40	PCIE_RX3N
AM41	PCIE_RX3P
AN1	VSS
AN2	DQB1_7
AN3	VSS
AN4	WCKB1_1

Ball Reference	Signal Name
AN5	WCKB1B_1
AN7	VSS
AN8	DQB1_28
AN34	DDCVGACLK
AN35	VSS
AN37	PCIE_TX3P
AN38	PCIE_TX3N
AN39	VSS
AN40	VSS
AN41	VSS
AP1	WCKB1_0
AP2	WCKB1B_0
AP11	DQB1_31
AP13	VSS
AP15	VDD_18
AP17	VSS
AP19	AUX2P
AP21	DDCAUX3N
AP23	DDCAUX4N
AP25	GPIO_8_ROMSO
AP27	GPIO_22_ROMCSB
AP29	GENLK_VSYNC
AP31	DDCVGADATA
AP40	PCIE_RX2N
AP41	PCIE_RX2P
AR1	DQB1_8
AR2	DQB1_9
AR3	VSS
AR4	DQB1_24
AR5	DQB1_25
AR7	VSS
AR11	VSS
AR13	FB_VDDC
AR15	VDD_18
AR17	GPIO_SVT
AR19	VSS
AR21	VSS
AR23	DDCAUX4P
AR25	VSS
AR27	VSS
AR29	GENLK_CLK
AR31	VSS

Ball Reference	Signal Name
AR35	VSS
AR37	PCIE_TX2P
AR38	PCIE_TX2N
AR39	VSS
AR40	PCIE_RX1N
AR41	PCIE_RX1P
AT1	DQB1_10
AT2	DQB1_11
AT40	PCIE_RX0N
AT41	PCIE_RX0P
AU1	VSS
AU2	EDCB1_1
AU3	VSS
AU4	DQB1_26
AU7	DQB1_27
AU9	VSS
AU11	DQB1_30
AU13	FB_VSS
AU15	PLLCHARZ_H
AU17	GPIO_SVC
AU19	DDC2DATA
AU21	GPIO_14_HPD2
AU23	VSS
AU25	GENERICE_HPD4
AU27	DDCAUX5P
AU29	VSS
AU31	GENERICC
AU33	PCIE_REFCLKN
AU35	PCIE_TX0N
AU38	PCIE_TX1P
AU39	PCIE_TX1N
AU40	WAKEB
AU41	PCIE_ZVSS
AV1	DDBIB1_1
AV2	DQB1_12
AV7	EDCB1_3
AV9	DDBIB1_3
AV11	DQB1_29
AV13	FB_VDDCI
AV15	PLLCHARZ_L
AV17	GPIO_SVD
AV19	DDC2CLK

Ball Reference	Signal Name
AV21	HPD1
AV23	GENERICF_HPD5
AV25	GPIO_18_HPD3
AV27	DDCAUX5N
AV29	GENERICB
AV31	GENERICD
AV33	PCIE_REFCLKP
AV35	PCIE_TX0P
AV40	CLKREQB
AV41	PERSTB
AW1	DQB1_13
AW2	DQB1_14
AW3	VSS
AW5	VSS
AW7	VSS
AW9	VSS
AW11	VSS
AW13	VSS
AW15	VSS
AW17	VSS
AW19	VSS
AW21	VSS
AW23	VSS
AW25	VSS
AW27	VSS
AW29	VSS
AW31	VSS
AW33	VSS
AW35	VSS
AW37	VSS
AW39	VSS
AW40	SMBCLK
AW41	SMBDAT
AY1	VSS
AY2	VSS
AY3	DQB1_15
AY4	DQB1_17
AY5	DQB1_19
AY6	DDBIB1_2
AY7	DQB1_21
AY8	DQB1_22
AY9	VSS

Ball Reference	Signal Name
AY10	DDC1CLK
AY11	AUX1P
AY12	VSS
AY13	TEST_PG
AY14	TXCEP_DPE3P
AY15	TX0P_DPE2P
AY16	TX1P_DPE1P
AY17	VSS
AY18	TX2P_DPE0P
AY19	TXCDP_DPD3P
AY20	TX0P_DPD2P
AY21	TX1P_DPD1P
AY22	TX2P_DPD0P
AY23	VSS
AY24	TXCCP_DPC3P
AY25	TX3P_DPC2P
AY26	TX4P_DPC1P
AY27	TX5P_DPC0P
AY28	TXCBP_DPB3P
AY29	VSS
AY30	TX0P_DPB2P
AY31	TX1P_DPB1P
AY32	TX2P_DPB0P
AY33	TXCAP_DPA3P
AY34	TX3P_DPA2P
AY35	TX4P_DPA1P
AY36	TX5P_DPA0P
AY37	VSS
AY38	ANALOGIO
AY39	XTALOUT
AY40	VSS
AY41	VSS
BA2	VSS
BA3	DQB1_16
BA4	DQB1_18
BA5	VSS
BA6	EDCB1_2
BA7	DQB1_20
BA8	DQB1_23
BA9	VSS
BA10	DDC1DATA
BA11	AUX1N

Ball Reference	Signal Name
BA12	AUX_ZVSS
BA13	TEST_PG_BACO
BA14	TXCEM_DPE3N
BA15	TX0M_DPE2N
BA16	TX1M_DPE1N
BA17	VSS
BA18	TX2M_DPE0N
BA19	TXCDM_DPD3N
BA20	TX0M_DPD2N
BA21	TX1M_DPD1N
BA22	TX2M_DPD0N
BA23	VSS
BA24	TXCCM_DPC3N
BA25	TX3M_DPC2N
BA26	TX4M_DPC1N
BA27	TX5M_DPC0N
BA28	TXCBM_DPB3N
BA29	VSS
BA30	TX0M_DPB2N
BA31	TX1M_DPB1N
BA32	TX2M_DPB0N
BA33	TXCAM_DPA3N
BA34	TX3M_DPA2N
BA35	TX4M_DPA1N
BA36	TX5M_DPA0N
BA37	VSS
BA38	GENERICA
BA39	XTALIN
BA40	VSS

A.2 Pins Sorted by Signal Name

Table A–2 "Polaris 12" XL Pins Sorted by Signal Name

Signal Name	Ball Reference
ADBIA0	H21
ADBIA1	H19
ADBIB0	W8
ADBIB1	AA8
ANALOGIO	AY38
AUX1N	BA11
AUX1P	AY11

Signal Name	Ball Reference
AUX2N	AM19
AUX2P	AP19
AUX_ZVSS	BA12
BL_ENABLE	AC37
BL_PWM_DIM	AC38
BP_0	AA38
BP_1	AA37
CASA0B	D23
CASA1B	D17
CASB0B	U4
CASB1B	AC4
CKEA0	G21
CKEA1	E19
CKEB0	W5
CKEB1	AA7
CLKA0	E31
CLKA0B	D31
CLKA1	D7
CLKA1B	D9
CLKB0	G4
CLKB0B	J4
CLKB1	AL5
CLKB1B	AL4
CLKREQB	AV40
CSA0B_0	H31
CSA1B_0	E7
CSB0B_0	G5
CSB1B_0	AL8
DBGDATA_0	L40
DBGDATA_1	L41
DBGDATA_2	M40
DBGDATA_3	M41
DBGDATA_4	N40
DBGDATA_5	N41
DBGDATA_6	P40
DBGDATA_7	P41
DBGDATA_8	R40
DBGDATA_9	R41
DBGDATA_10	T40
DBGDATA_11	T41
DBGDATA_12	U40
DBGDATA_13	U41

Signal Name	Ball Reference
DBGDATA_14	V40
DBGDATA_15	V41
DDBIA0_0	J38
DDBIA0_1	F40
DDBIA0_2	A38
DDBIA0_3	B30
DDBIA1_0	B25
DDBIA1_1	B18
DDBIA1_2	A12
DDBIA1_3	B5
DDBIB0_0	E2
DDBIB0_1	M1
DDBIB0_2	V2
DDBIB0_3	AE2
DDBIB1_0	AK2
DDBIB1_1	AV1
DDBIB1_2	AY6
DDBIB1_3	AV9
DDC1CLK	AY10
DDC1DATA	BA10
DDC2CLK	AV19
DDC2DATA	AU19
DDCAUX3N	AP21
DDCAUX3P	AM21
DDCAUX4N	AP23
DDCAUX4P	AR23
DDCAUX5N	AV27
DDCAUX5P	AU27
DDCVGACLK	AN34
DDCVGADATA	AP31
DIGON	AC40
DMINUS	N34
DPLUS	N35
DQA0_0	L34
DQA0_1	L37
DQA0_2	L38
DQA0_3	J35
DQA0_4	G37
DQA0_5	E38
DQA0_6	E35
DQA0_7	D35
DQA0_8	H41

Signal Name	Ball Reference
DQA0_9	H40
DQA0_10	G41
DQA0_11	G40
DQA0_12	E40
DQA0_13	D41
DQA0_14	D40
DQA0_15	C41
DQA0_16	C40
DQA0_17	B39
DQA0_18	A39
DQA0_19	B38
DQA0_20	B36
DQA0_21	A36
DQA0_22	B35
DQA0_23	A35
DQA0_24	B33
DQA0_25	B32
DQA0_26	A32
DQA0_27	B31
DQA0_28	A30
DQA0_29	B29
DQA0_30	B28
DQA0_31	A28
DQA1_0	B27
DQA1_1	A27
DQA1_2	B26
DQA1_3	A26
DQA1_4	A24
DQA1_5	B23
DQA1_6	A23
DQA1_7	B22
DQA1_8	B20
DQA1_9	A20
DQA1_10	B19
DQA1_11	A19
DQA1_12	B17
DQA1_13	A16
DQA1_14	B16
DQA1_15	A15
DQA1_16	B15
DQA1_17	A14
DQA1_18	B14

Signal Name	Ball Reference
DQA1_19	B13
DQA1_20	A11
DQA1_21	B11
DQA1_22	A10
DQA1_23	B10
DQA1_24	B8
DQA1_25	A7
DQA1_26	B7
DQA1_27	A6
DQA1_28	A4
DQA1_29	B4
DQA1_30	A3
DQA1_31	B3
DQB0_0	C2
DQB0_1	C1
DQB0_2	D2
DQB0_3	D1
DQB0_4	F1
DQB0_5	G2
DQB0_6	G1
DQB0_7	H2
DQB0_8	K2
DQB0_9	K1
DQB0_10	L2
DQB0_11	L1
DQB0_12	N2
DQB0_13	P2
DQB0_14	P1
DQB0_15	R2
DQB0_16	R1
DQB0_17	T2
DQB0_18	T1
DQB0_19	U2
DQB0_20	W1
DQB0_21	W2
DQB0_22	Y1
DQB0_23	Y2
DQB0_24	AB2
DQB0_25	AC1
DQB0_26	AC2
DQB0_27	AD1
DQB0_28	AF1

Signal Name	Ball Reference
DQB0_29	AF2
DQB0_30	AG1
DQB0_31	AG2
DQB1_0	AH1
DQB1_1	AH2
DQB1_2	AJ2
DQB1_3	AK1
DQB1_4	AL2
DQB1_5	AM1
DQB1_6	AM2
DQB1_7	AN2
DQB1_8	AR1
DQB1_9	AR2
DQB1_10	AT1
DQB1_11	AT2
DQB1_12	AV2
DQB1_13	AW1
DQB1_14	AW2
DQB1_15	AY3
DQB1_16	BA3
DQB1_17	AY4
DQB1_18	BA4
DQB1_19	AY5
DQB1_20	BA7
DQB1_21	AY7
DQB1_22	AY8
DQB1_23	BA8
DQB1_24	AR4
DQB1_25	AR5
DQB1_26	AU4
DQB1_27	AU7
DQB1_28	AN8
DQB1_29	AV11
DQB1_30	AU11
DQB1_31	AP11
DRAM_RSTA	L32
DRAM_RSTB	AM11
EDCA0_0	G38
EDCA0_1	F41
EDCA0_2	B37
EDCA0_3	A31
EDCA1_0	B24

Signal Name	Ball Reference
EDCA1_1	A18
EDCA1_2	B12
EDCA1_3	B6
EDCB0_0	F2
EDCB0_1	M2
EDCB0_2	V1
EDCB0_3	AD2
EDCB1_0	AL1
EDCB1_1	AU2
EDCB1_2	BA6
EDCB1_3	AV7
FB_VDDC	AR13
FB_VDDCI	AV13
FB_VMEMIO	C3
FB_VSS	AU13
GENERICA	BA38
GENERICB	AV29
GENERICC	AU31
GENERICD	AV31
GENERICE_HPD4	AU25
GENERICF_HPD5	AV23
GENERICG	AM29
GENLK_CLK	AR29
GENLK_VSYNC	AP29
GPIO_0	W40
GPIO_1	AA40
GPIO_2	AA35
GPIO_5_REG_HOT_AC_BATT	AA34
GPIO_6_TACH	U35
GPIO_8_ROMSO	AP25
GPIO_9_ROMSI	AM25
GPIO_10_ROMSCK	AM27
GPIO_11	W41
GPIO_12	Y40
GPIO_13	Y41
GPIO_14_HPD2	AU21
GPIO_15	AA41
GPIO_16_8P_DETECT	U34
GPIO_17_THERMAL_INT	R37
GPIO_18_HPD3	AV25
GPIO_19_CTF	R38
GPIO_20	AB40

Signal Name	Ball Reference
GPIO_21	AB41
GPIO_22_ROMCSB	AP27
GPIO_28_FDO	U38
GPIO_29	W37
GPIO_30	W38
GPIO_SVC	AU17
GPIO_SVD	AV17
GPIO_SVT	AR17
HPD1	AV21
HSYNC	W34
JTAG_TCK	AE41
JTAG_TDI	AD40
JTAG_TDO	AF41
JTAG_TMS	AD41
JTAG_TRSTB	AF40
MAA0_0	G25
MAA0_1	H25
MAA0_2	E27
MAA0_3	D27
MAA0_4	D29
MAA0_5	H27
MAA0_6	H23
MAA0_7	E23
MAA0_8	D25
MAA0_9	H29
MAA1_0	E15
MAA1_1	H15
MAA1_2	G13
MAA1_3	D13
MAA1_4	H11
MAA1_5	H13
MAA1_6	H17
MAA1_7	G17
MAA1_8	D15
MAA1_9	E11
MAB0_0	R5
MAB0_1	R8
MAB0_2	N7
MAB0_3	N4
MAB0_4	L8
MAB0_5	N8
MAB0_6	U8

Signal Name	Ball Reference
MAB0_7	U7
MAB0_8	R4
MAB0_9	L5
MAB1_0	AE7
MAB1_1	AE8
MAB1_2	AG5
MAB1_3	AG4
MAB1_4	AJ4
MAB1_5	AG8
MAB1_6	AC8
MAB1_7	AC5
MAB1_8	AE4
MAB1_9	AJ8
MEM_CALRA	K15
MEM_CALRB	R10
MVREFDA	K17
MVREFDB	U10
PCIE_REFCLKN	AU33
PCIE_REFCLKP	AV33
PCIE_RX0N	AT40
PCIE_RX0P	AT41
PCIE_RX1N	AR40
PCIE_RX1P	AR41
PCIE_RX2N	AP40
PCIE_RX2P	AP41
PCIE_RX3N	AM40
PCIE_RX3P	AM41
PCIE_RX4N	AL40
PCIE_RX4P	AL41
PCIE_RX5N	AK40
PCIE_RX5P	AK41
PCIE_RX6N	AJ40
PCIE_RX6P	AJ41
PCIE_RX7N	AH40
PCIE_RX7P	AH41
PCIE_TX0N	AU35
PCIE_TX0P	AV35
PCIE_TX1N	AU39
PCIE_TX1P	AU38
PCIE_TX2N	AR38
PCIE_TX2P	AR37
PCIE_TX3N	AN38

Signal Name	Ball Reference
PCIE_TX3P	AN37
PCIE_TX4N	AL38
PCIE_TX4P	AL37
PCIE_TX5N	AJ38
PCIE_TX5P	AJ37
PCIE_TX6N	AG38
PCIE_TX6P	AG37
PCIE_TX7N	AE38
PCIE_TX7P	AE37
PCIE_ZVSS	AU41
PERSTB	AV41
PLLCHARZ_H	AU15
PLLCHARZ_L	AV15
PX_EN	AC41
RASA0B	D21
RASA1B	D19
RASB0B	W4
RASB1B	AA4
RSVD	K41
RSVD	R34
SCL	AC35
SDA	AC34
SMBCLK	AW40
SMBDAT	AW41
SWAPLOCKA	AG34
SWAPLOCKB	AE34
TEMPIN0	J8
TEMPINRETURN	J7
TEST6	B2
TESTEN	AE40
TEST_PG	AY13
TEST_PG_BACO	BA13
TSVDD	AM13
TS_A	N38
TX0M_DPB2N	BA30
TX0M_DPD2N	BA20
TX0M_DPE2N	BA15
TX0P_DPB2P	AY30
TX0P_DPD2P	AY20
TX0P_DPE2P	AY15
TX1M_DPB1N	BA31
TX1M_DPD1N	BA21

Signal Name	Ball Reference
TX1M_DPE1N	BA16
TX1P_DPB1P	AY31
TX1P_DPD1P	AY21
TX1P_DPE1P	AY16
TX2M_DPB0N	BA32
TX2M_DPD0N	BA22
TX2M_DPE0N	BA18
TX2P_DPB0P	AY32
TX2P_DPD0P	AY22
TX2P_DPE0P	AY18
TX3M_DPA2N	BA34
TX3M_DPC2N	BA25
TX3P_DPA2P	AY34
TX3P_DPC2P	AY25
TX4M_DPA1N	BA35
TX4M_DPC1N	BA26
TX4P_DPA1P	AY35
TX4P_DPC1P	AY26
TX5M_DPA0N	BA36
TX5M_DPC0N	BA27
TX5P_DPA0P	AY36
TX5P_DPC0P	AY27
TXCAM_DPA3N	BA33
TXCAP_DPA3P	AY33
TXCBM_DPB3N	BA28
TXCBP_DPB3P	AY28
TXCCM_DPC3N	BA24
TXCCP_DPC3P	AY24
TXCDM_DPD3N	BA19
TXCDP_DPD3P	AY19
TXCEM_DPE3N	BA14
TXCEP_DPE3P	AY14
VDDC	N13
VDDC	N15
VDDC	N21
VDDC	N23
VDDC	N29
VDDC	N31
VDDC	R13
VDDC	R15
VDDC	R21
VDDC	R23

Signal Name	Ball Reference
VDDC	R29
VDDC	R31
VDDC	U13
VDDC	U15
VDDC	U21
VDDC	U23
VDDC	U29
VDDC	U31
VDDC	W13
VDDC	W15
VDDC	W21
VDDC	W23
VDDC	W29
VDDC	W31
VDDC	AA13
VDDC	AA15
VDDC	AA21
VDDC	AA23
VDDC	AA29
VDDC	AA31
VDDC	AC13
VDDC	AC15
VDDC	AC21
VDDC	AC23
VDDC	AC29
VDDC	AC31
VDDC	AE13
VDDC	AE15
VDDC	AE21
VDDC	AE23
VDDC	AE29
VDDC	AE31
VDDC	AG13
VDDC	AG15
VDDC	AG21
VDDC	AG23
VDDC	AG29
VDDC	AG31
VDDC	AJ13
VDDC	AJ15
VDDC	AJ17
VDDC	AJ19

Signal Name	Ball Reference
VDDC	AJ21
VDDC	AJ23
VDDC	AJ25
VDDC	AJ27
VDDC	AJ29
VDDC	AJ31
VDDC	AL13
VDDC	AL15
VDDC	AL17
VDDC	AL19
VDDC	AL21
VDDC	AL23
VDDC	AL25
VDDC	AL27
VDDC	AL29
VDDC	AL31
VDDCI	L13
VDDCI	L17
VDDCI	L21
VDDCI	L25
VDDCI	L29
VDDCI	N11
VDDCI	U11
VDDCI	AA11
VDDCI	AE11
VDD_08	W32
VDD_08	AC32
VDD_08	AG32
VDD_08	AG35
VDD_08	AJ32
VDD_08	AJ34
VDD_08	AL34
VDD_18	AM15
VDD_18	AP15
VDD_18	AR15
VDD_33	AM31
VMEMIO	K11
VMEMIO	K13
VMEMIO	K19
VMEMIO	K23
VMEMIO	K27
VMEMIO	K31

Signal Name	Ball Reference
VMEMIO	L10
VMEMIO	N10
VMEMIO	W10
VMEMIO	AC10
VMEMIO	AG10
VSS	A2
VSS	A5
VSS	A9
VSS	A13
VSS	A17
VSS	A21
VSS	A25
VSS	A29
VSS	A33
VSS	A37
VSS	A40
VSS	B1
VSS	B40
VSS	B41
VSS	C5
VSS	C7
VSS	C9
VSS	C11
VSS	C13
VSS	C15
VSS	C17
VSS	C19
VSS	C21
VSS	C23
VSS	C25
VSS	C27
VSS	C29
VSS	C31
VSS	C33
VSS	C35
VSS	C37
VSS	C39
VSS	E1
VSS	E3
VSS	E4
VSS	E9
VSS	E13

Signal Name	Ball Reference
VSS	E17
VSS	E21
VSS	E25
VSS	E29
VSS	E39
VSS	E41
VSS	G3
VSS	G7
VSS	G11
VSS	G15
VSS	G19
VSS	G23
VSS	G27
VSS	G31
VSS	G35
VSS	G39
VSS	J1
VSS	J3
VSS	J5
VSS	J34
VSS	J37
VSS	J39
VSS	J40
VSS	J41
VSS	K21
VSS	K25
VSS	K29
VSS	K40
VSS	L3
VSS	L7
VSS	L11
VSS	L15
VSS	L19
VSS	L23
VSS	L27
VSS	L31
VSS	L35
VSS	L39
VSS	N1
VSS	N3
VSS	N5
VSS	N17

Signal Name	Ball Reference
VSS	N19
VSS	N25
VSS	N27
VSS	N32
VSS	N37
VSS	N39
VSS	R3
VSS	R7
VSS	R11
VSS	R17
VSS	R19
VSS	R25
VSS	R27
VSS	R32
VSS	R35
VSS	R39
VSS	U1
VSS	U3
VSS	U5
VSS	U17
VSS	U19
VSS	U25
VSS	U27
VSS	U32
VSS	U37
VSS	U39
VSS	W3
VSS	W7
VSS	W11
VSS	W17
VSS	W19
VSS	W25
VSS	W27
VSS	W39
VSS	AA1
VSS	AA3
VSS	AA5
VSS	AA10
VSS	AA17
VSS	AA19
VSS	AA25
VSS	AA27

Signal Name	Ball Reference
VSS	AA32
VSS	AA39
VSS	AC3
VSS	AC7
VSS	AC11
VSS	AC17
VSS	AC19
VSS	AC25
VSS	AC27
VSS	AC39
VSS	AE1
VSS	AE3
VSS	AE5
VSS	AE10
VSS	AE17
VSS	AE19
VSS	AE25
VSS	AE27
VSS	AE32
VSS	AE35
VSS	AE39
VSS	AG3
VSS	AG7
VSS	AG11
VSS	AG17
VSS	AG19
VSS	AG25
VSS	AG27
VSS	AG39
VSS	AG40
VSS	AG41
VSS	AJ1
VSS	AJ3
VSS	AJ5
VSS	AJ10
VSS	AJ11
VSS	AJ35
VSS	AJ39
VSS	AL3
VSS	AL7
VSS	AL10
VSS	AL11

Signal Name	Ball Reference
VSS	AL32
VSS	AL35
VSS	AL39
VSS	AM17
VSS	AM23
VSS	AN1
VSS	AN3
VSS	AN7
VSS	AN35
VSS	AN39
VSS	AN40
VSS	AN41
VSS	AP13
VSS	AP17
VSS	AR3
VSS	AR7
VSS	AR11
VSS	AR19
VSS	AR21
VSS	AR25
VSS	AR27
VSS	AR31
VSS	AR35
VSS	AR39
VSS	AU1
VSS	AU3
VSS	AU9
VSS	AU23
VSS	AU29
VSS	AW3
VSS	AW5
VSS	AW7
VSS	AW9
VSS	AW11
VSS	AW13
VSS	AW15
VSS	AW17
VSS	AW19
VSS	AW21
VSS	AW23
VSS	AW25
VSS	AW27

Signal Name	Ball Reference
VSS	AW29
VSS	AW31
VSS	AW33
VSS	AW35
VSS	AW37
VSS	AW39
VSS	AY1
VSS	AY2
VSS	AY9
VSS	AY12
VSS	AY17
VSS	AY23
VSS	AY29
VSS	AY37
VSS	AY40
VSS	AY41
VSS	BA2
VSS	BA5
VSS	BA9
VSS	BA17
VSS	BA23
VSS	BA29
VSS	BA37
VSS	BA40
VSYNC	W35
WAKEB	AU40
WCKA0B_0	E33
WCKA0B_1	B34
WCKA0_0	D33
WCKA0_1	A34
WCKA1B_0	B21
WCKA1B_1	B9
WCKA1_0	A22
WCKA1_1	A8
WCKB0B_0	J2
WCKB0B_1	AA2
WCKB0_0	H1
WCKB0_1	AB1
WCKB1B_0	AP2
WCKB1B_1	AN5
WCKB1_0	AP1
WCKB1_1	AN4

Signal Name	Ball Reference
WEA0B	G29
WEA1B	D11
WEB0B	L4
WEB1B	AJ7
XTALIN	BA39
XTALOUT	AY39