Schematic Page List Hide

- 009_CPU_CFG,RSVD
- 010_CPU_POWER_CAP
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- 012_
- 013_DDR4_
- 014_DDR4 SO-DIMM_A
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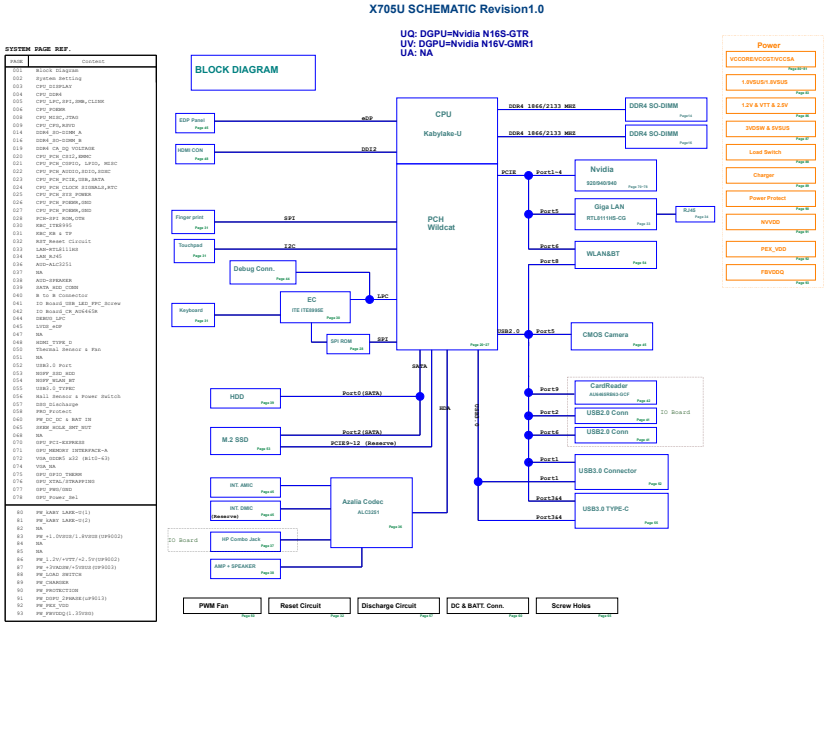
- 017_DDR4_****
- 018_DDR4_****
- 019_DDR4_CA_DQ_VOLTAGE
- 020_CPU_PCH_CSI2,EMMC
- 021_CPU_PCH_CGPIO, LPIO, MISC
- 022_CPU_PCH_AUDIO,SDIO,SDXC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNALS,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND



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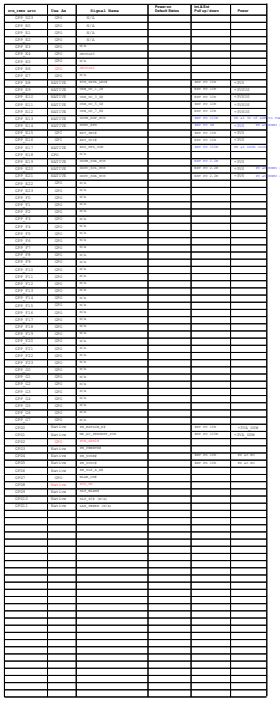
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND

X705 PCH_ GPIO



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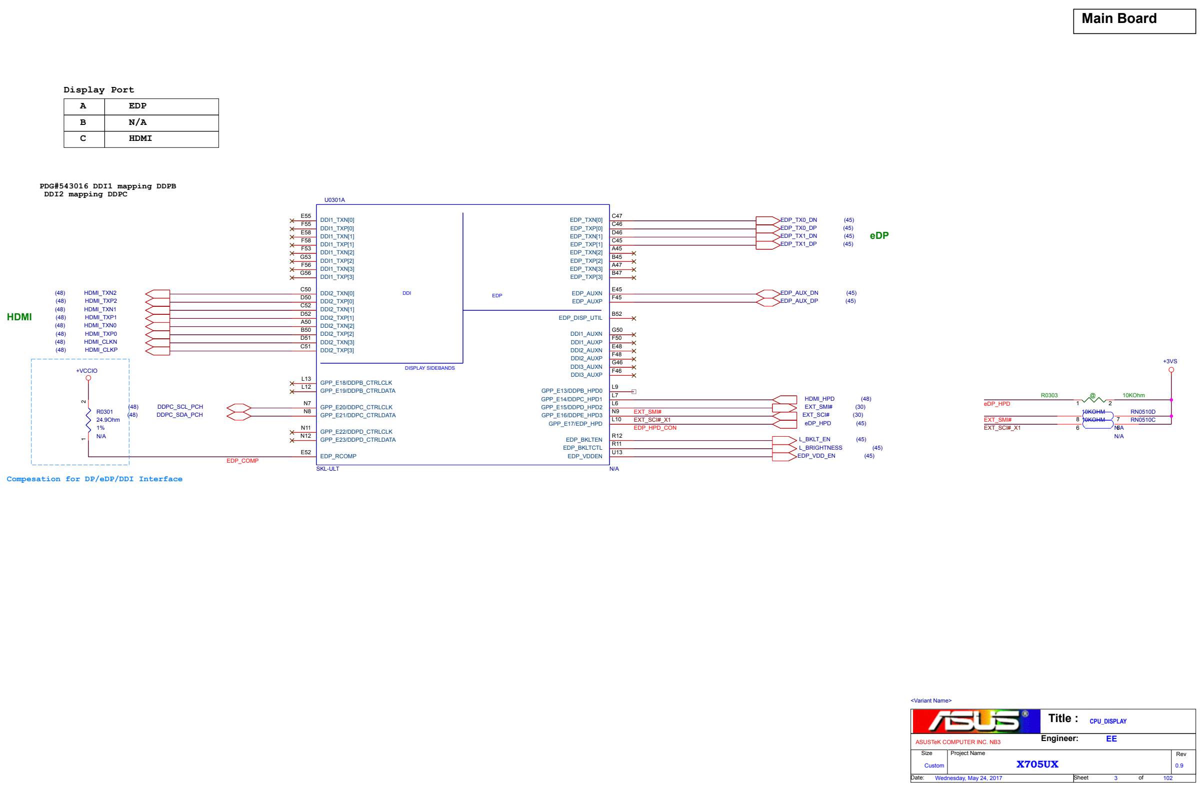

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- 009_CPU_CFG,RSVD
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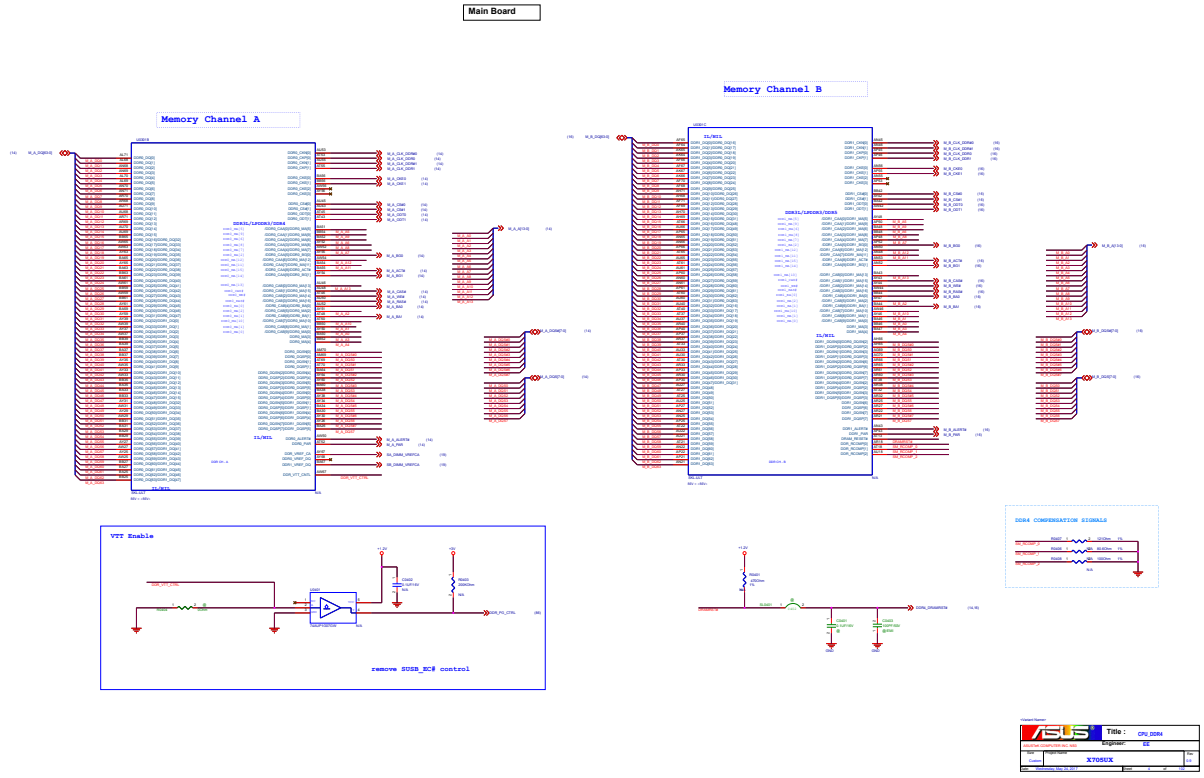

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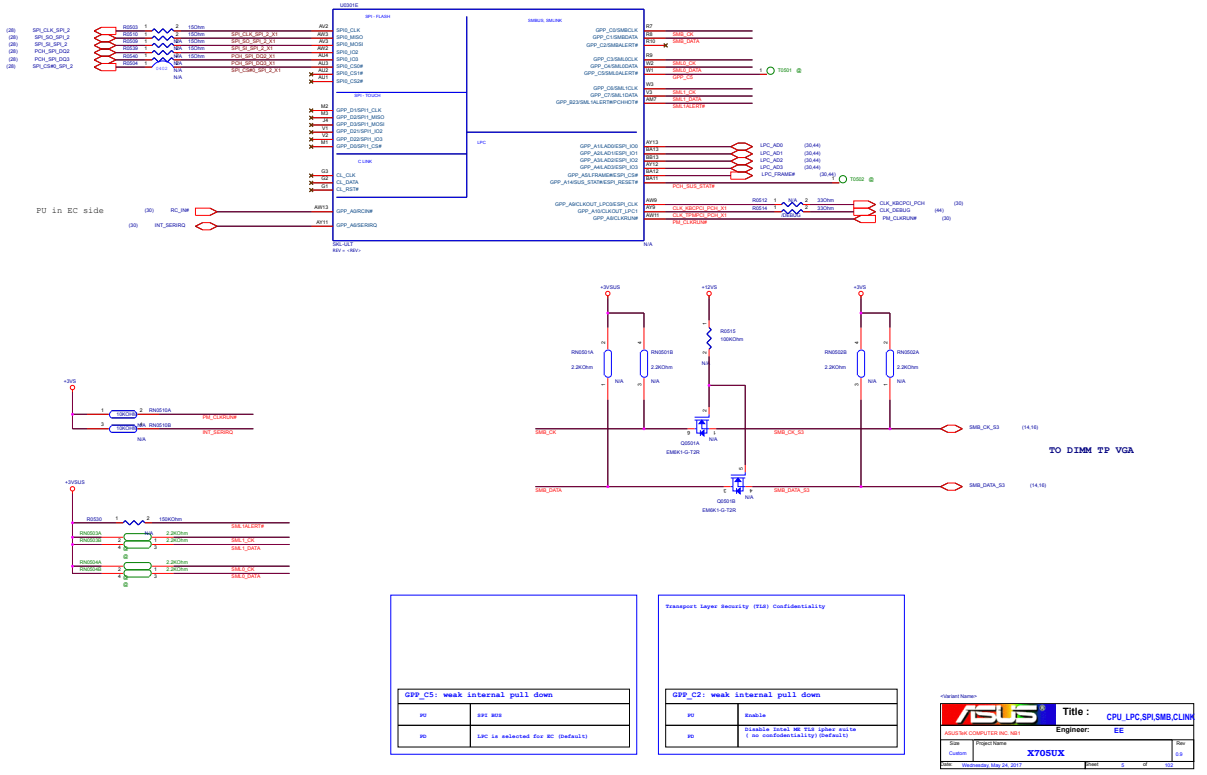
- 027_CPU_PCH_POEWR,GND

Main Board



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- 009_CPU_CFG,RSVD
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- 027_CPU_PCH_POEWR,GND

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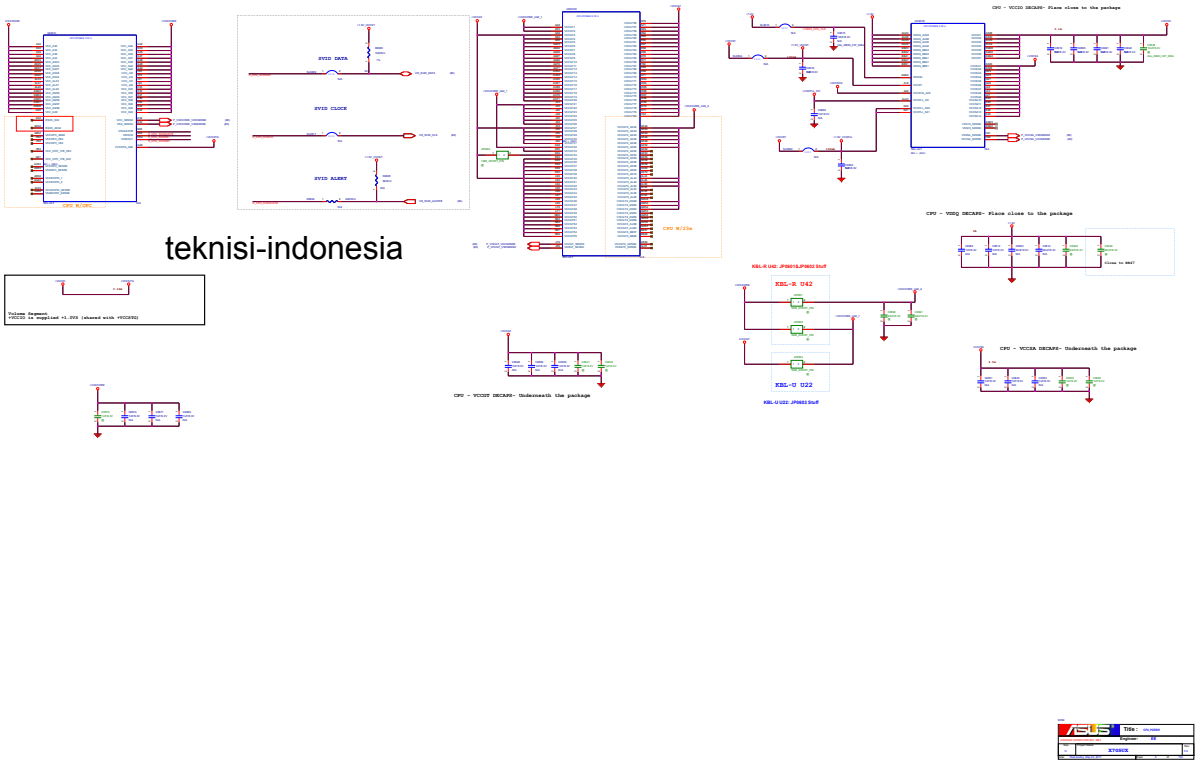
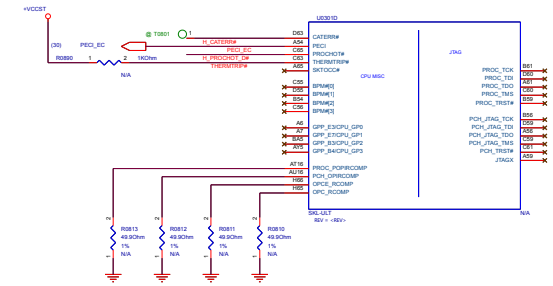
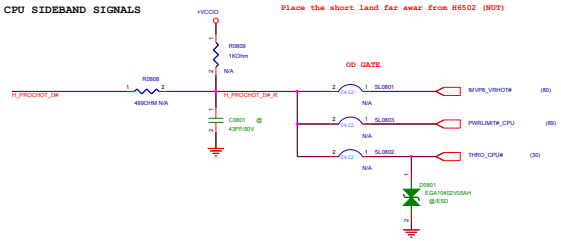


Main Board





Title :	CPU_MISC,JTAG,CLK		
Engineer:	EE		
Size: B	Project Name: X705UX		Rev: 0.9
Date: Wednesday, May 24, 2017	Sheet 8 of 102		

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- 009_CPU_CFG,RSVD
- 010_CPU_POWER_CAP
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- 026_CPU_PCH_POEWR,GND
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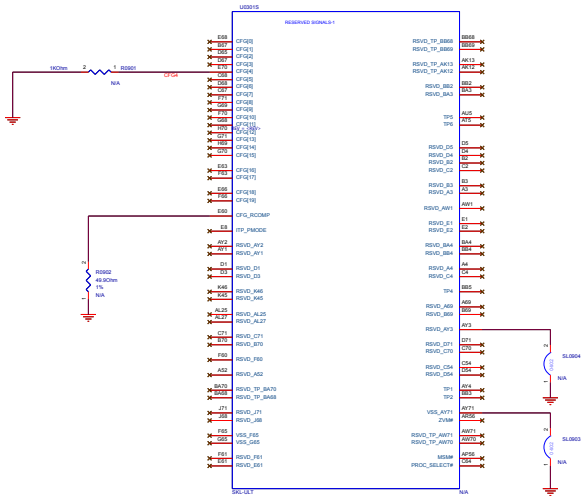
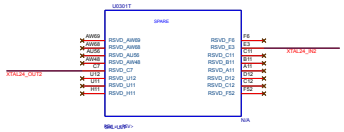
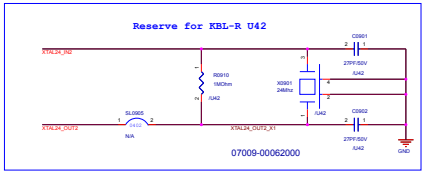
Main Board



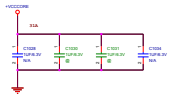




	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCU PLL LOCK UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE

Title :	CPU_CFG,RSVD
Engineer:	EE
Project Name	X756U
Date	Wednesday, May 24, 2017

CPU - VCC DECAPS- Underneath the package



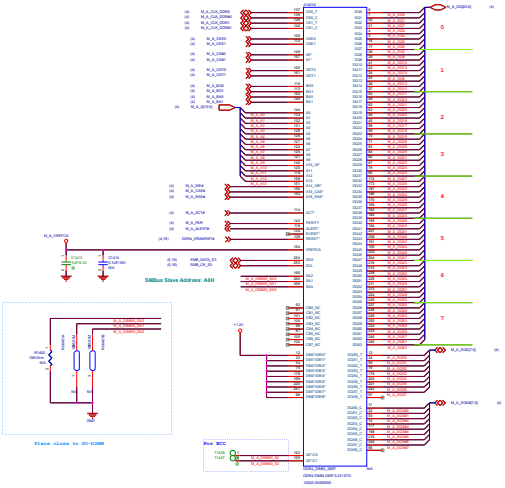
CPU - VCC DECAPS- Place close to the package

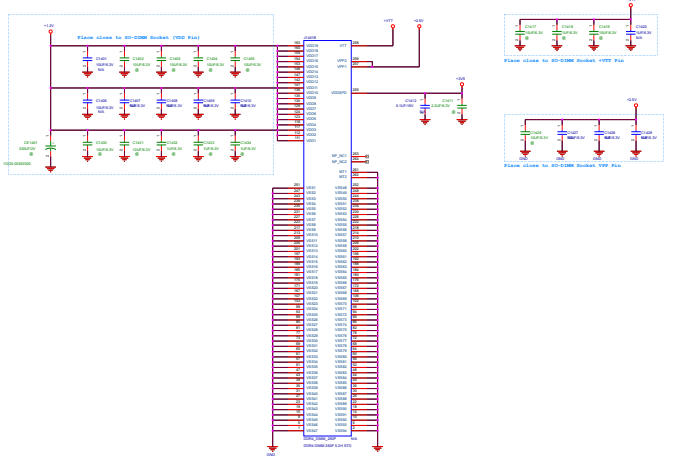
Title : CPU_POWER_CAP

Engineer: EE

X705

Schematic Page List Hide





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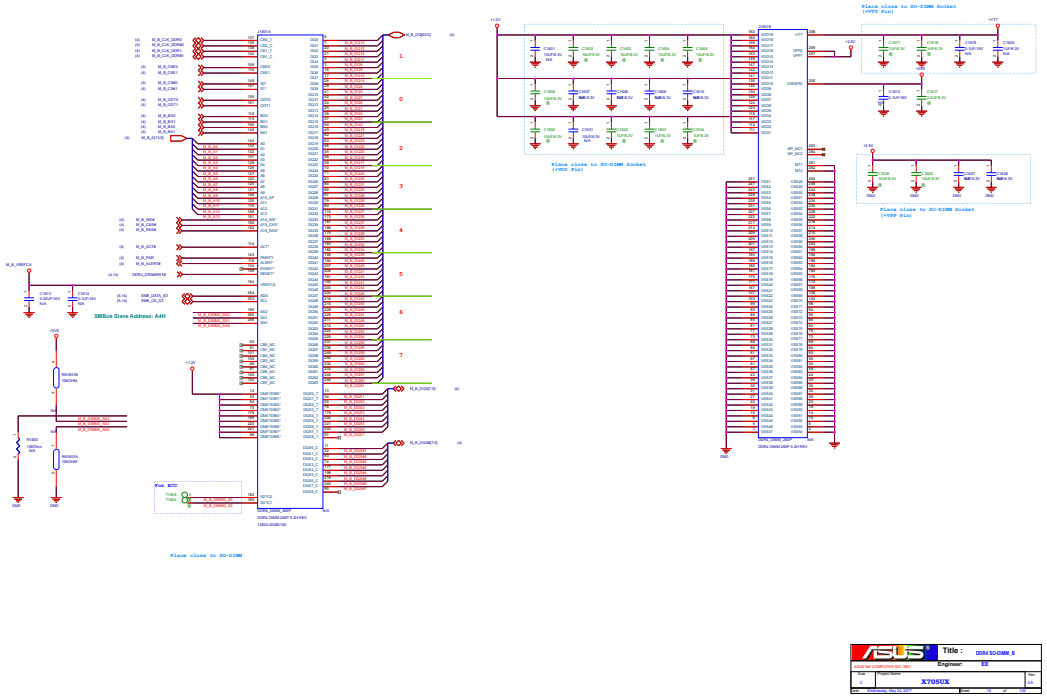
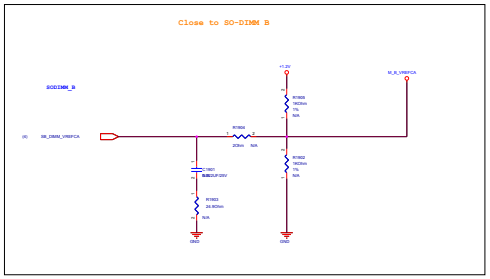
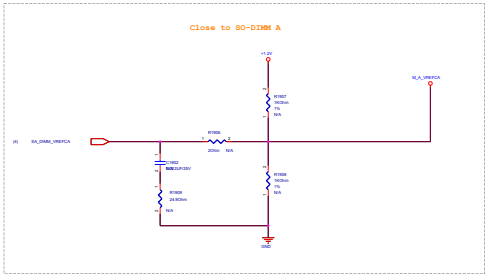
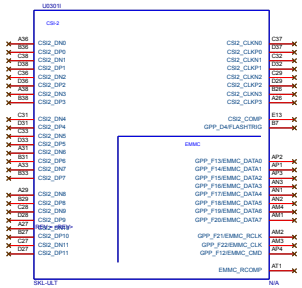
SODIMM CHB-DIMM0







Title : DDR3L_CA_DQ_VOLTAGE
Engineer: EE
X705UX



BOM

Title : CPU_PCH_CSI2,EMMC

ASUSTeK COMPUTER INC. NB3

Engineer: EE

Size	Project Name	Rev
B	X705UX	0.9

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- 009_CPU_CFG,RSVD
- 010_CPU_POWER_CAP
- 011_
- 012_
- 013_DDR4_
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- 025_CPU_PCH_SYS_POWER
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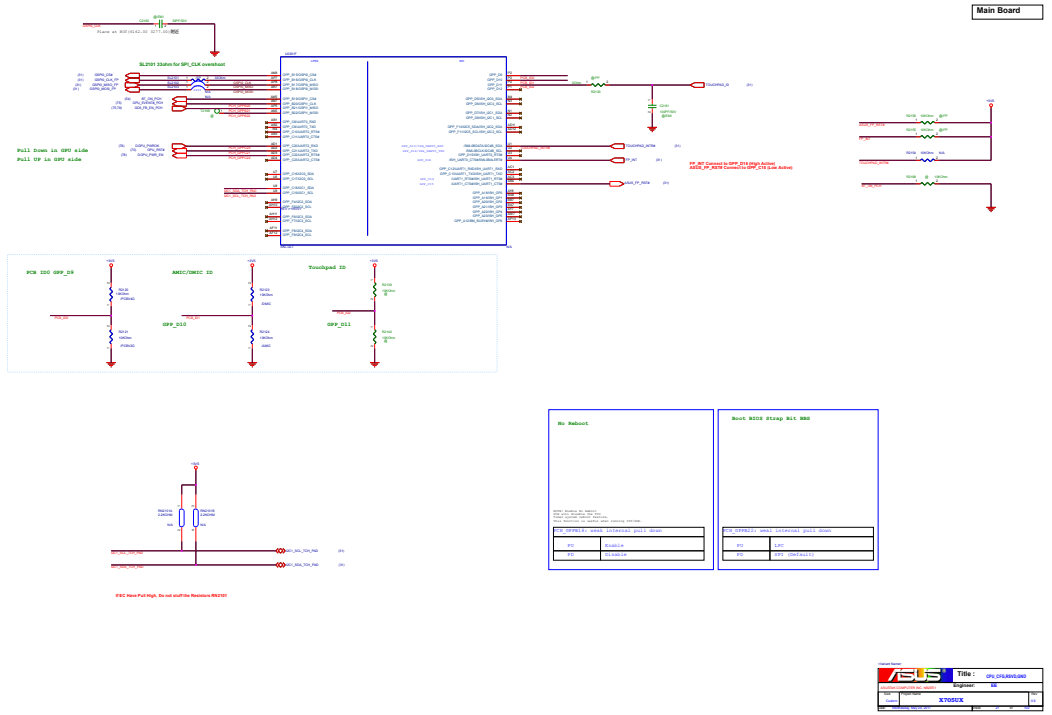
- 027_CPU_PCH_POEWR,GND



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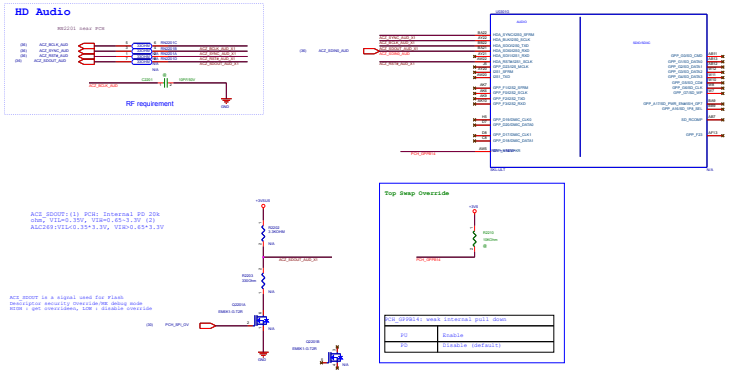

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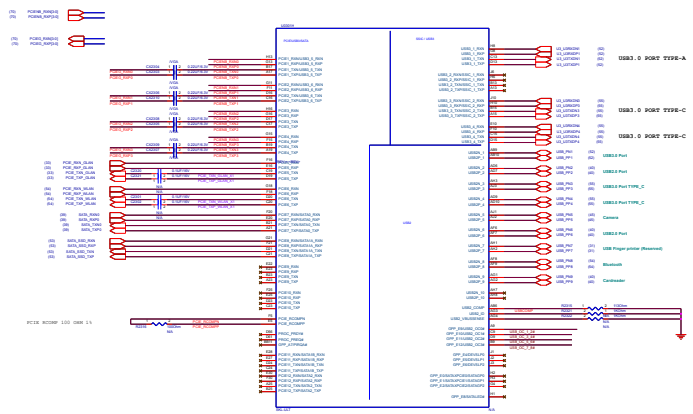

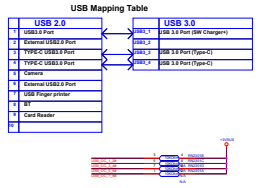

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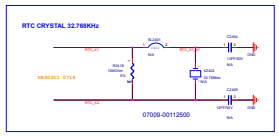
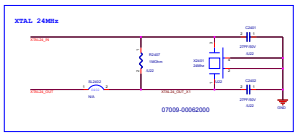
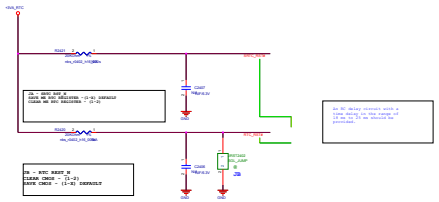
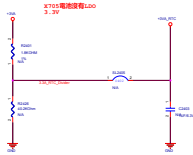
- 024_CPU_PCH_CLOCK SIGNALS,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH
- 029_PCH-XDP
- 030_KBC_ITE8995
- 031_KBC_KB & TP & FP
- 032_RST_Reset Circuit
- 033_LAN-RTL8111HS-CG
- 034_LAN_RJ45
- 035_
- 036-AUDIO_CODEC
- 037_
- 038_AUD-SPEAKER
- 039_SATA_HDD_CONN
- 040_B to B Connector
- 041_IO Board_USB_LED_FPC_Sc









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- 024_CPU_PCH_CLOCK SIGNALS,RTC
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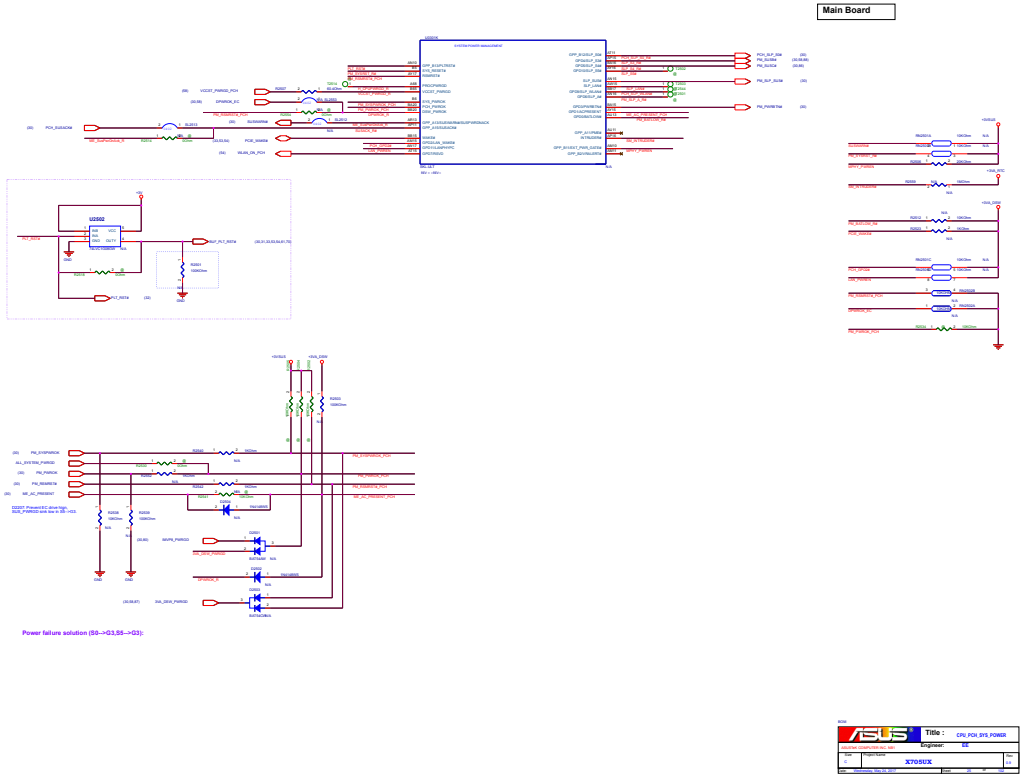

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- 022_CPU_PCH_AUDIO,SDIO,SDXC
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- 025_CPU_PCH_SYS_POWER
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- 040_B to B Connector
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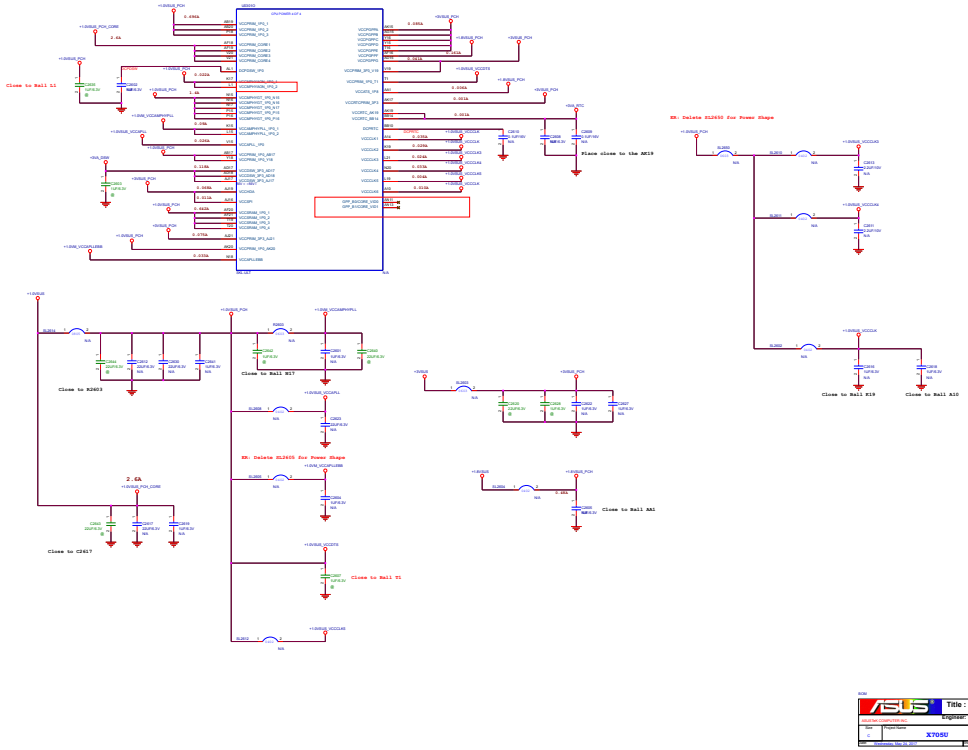

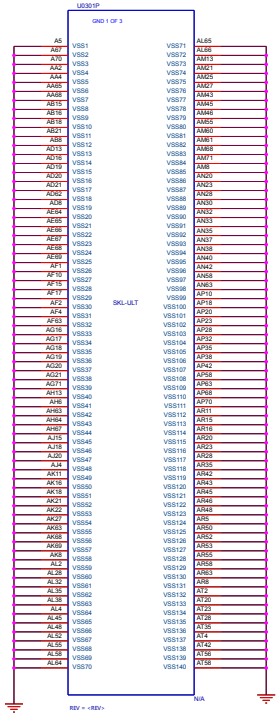

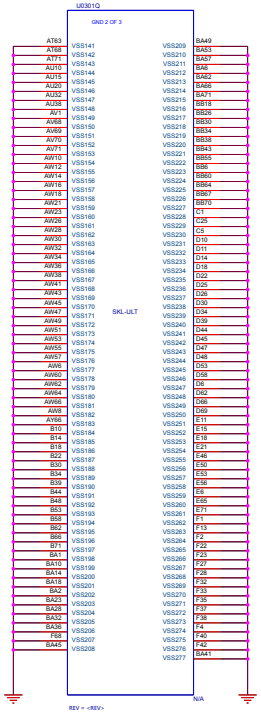

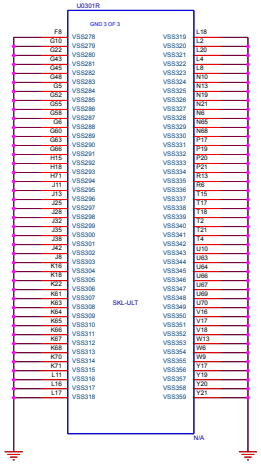

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- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH
- 029_PCH-XDP
- 030_KBC_ITE8995
- 031_KBC_KB & TP & FP
- 032_RST_Reset Circuit
- 033_LAN-RTL8111HS-CG
- 034_LAN_RJ45
- 035_
- 036-AUDIO_CODEC
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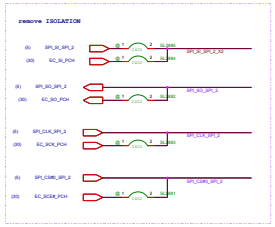
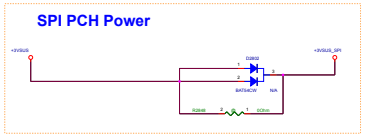
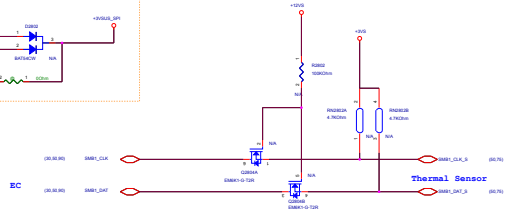
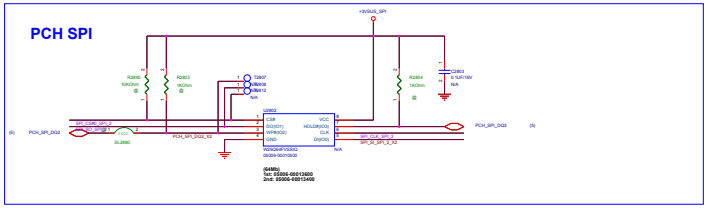
- 040_B to B Connector
- 041_IO Board_USB_LED_FPC_Sc









System Management Interface

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- 029_PCH-XDP
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- 033_LAN-RTL8111HS-CG
- 034_LAN_RJ45
- 035_
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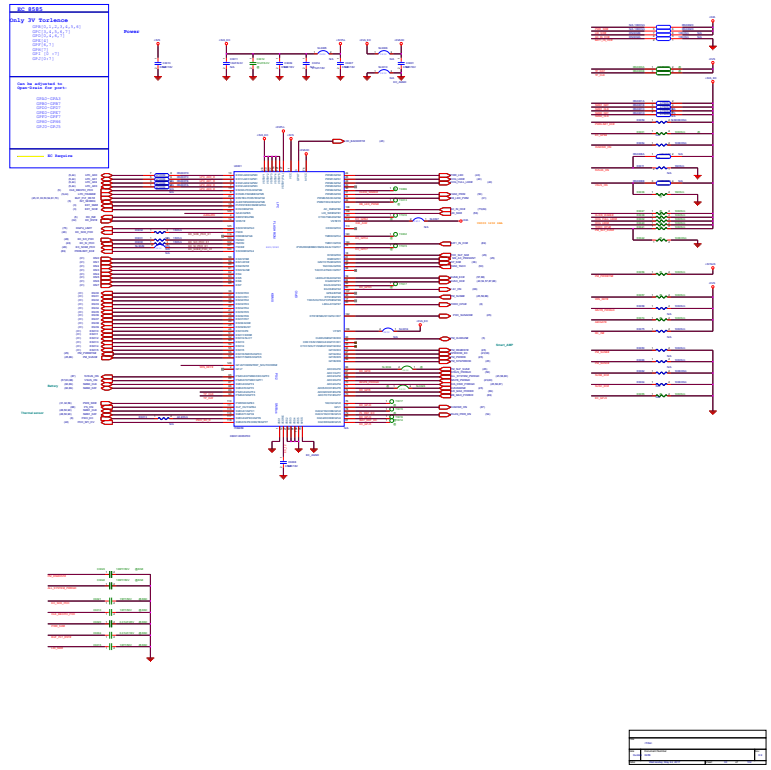

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- 036-AUDIO_CODEC
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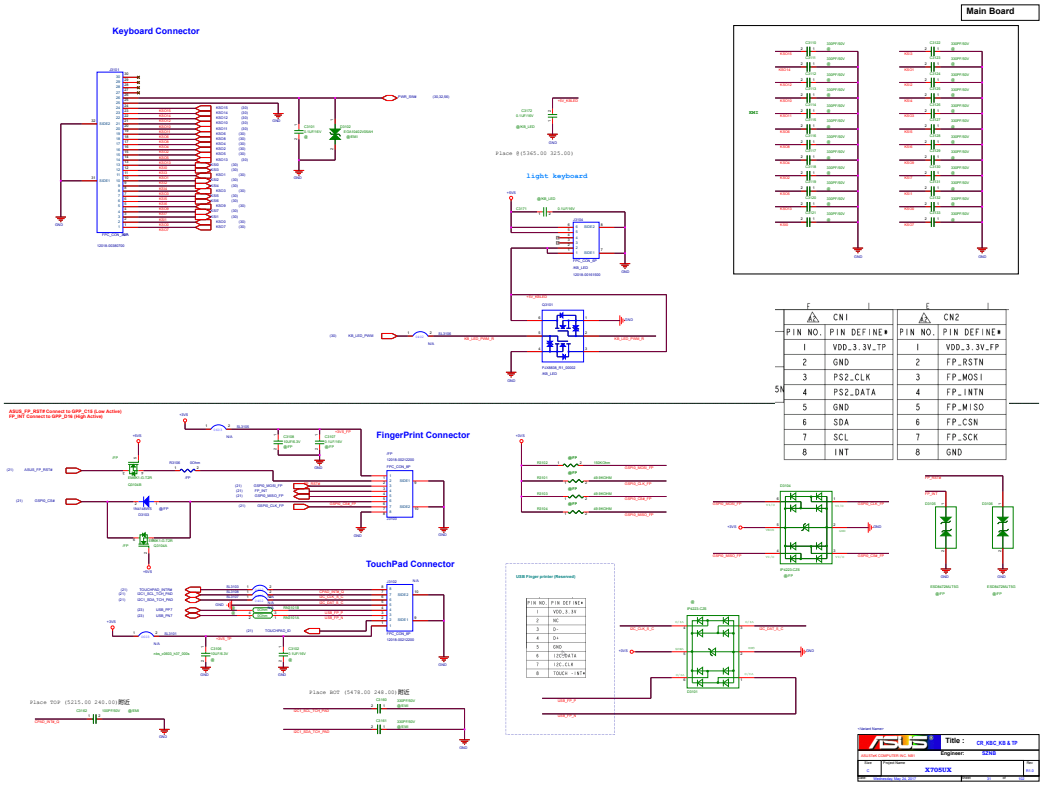

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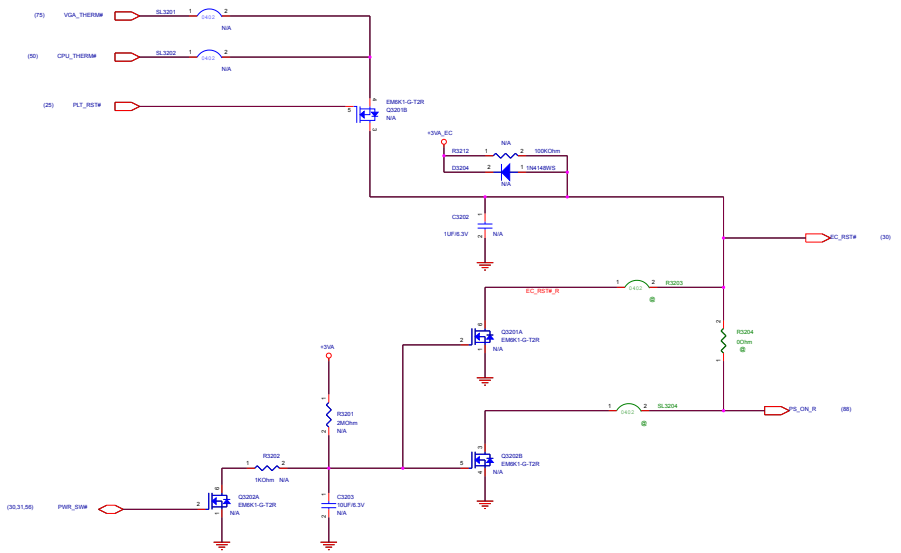

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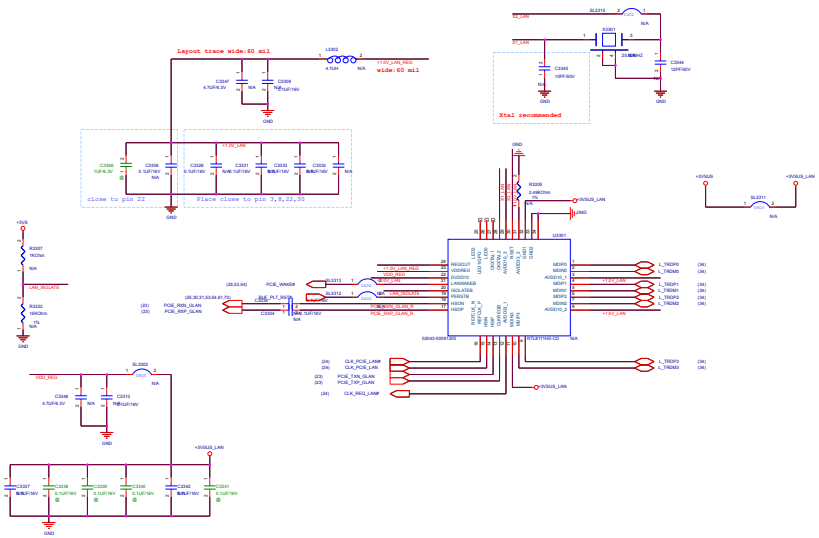
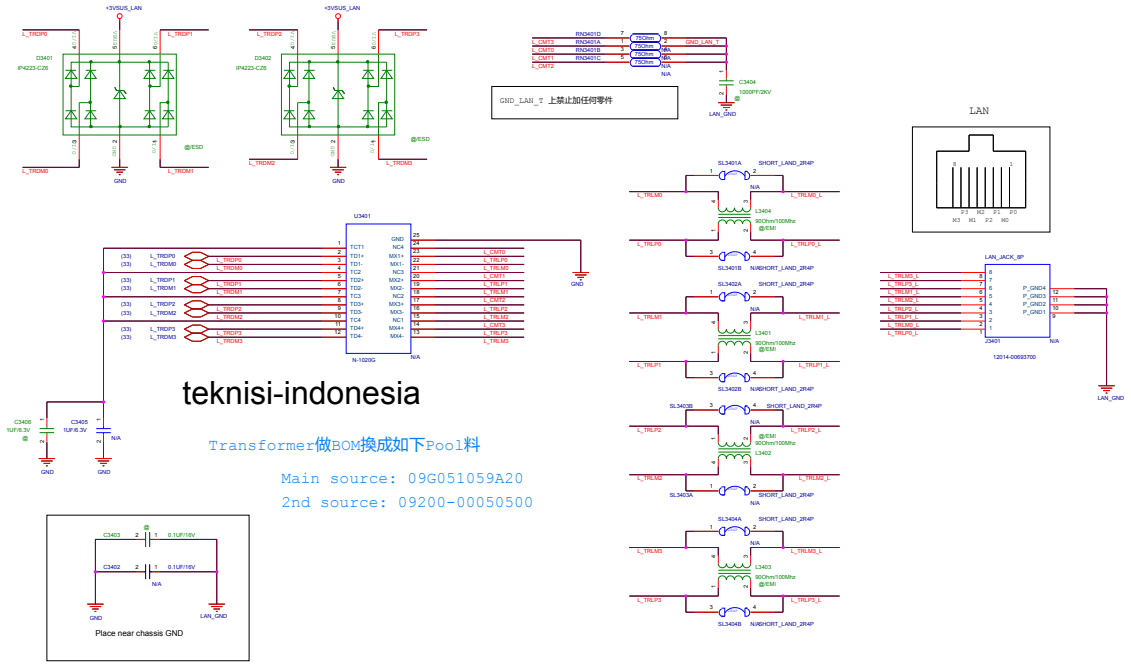


Title : LAN_RTL8111E_R1.2-1

Engineer:



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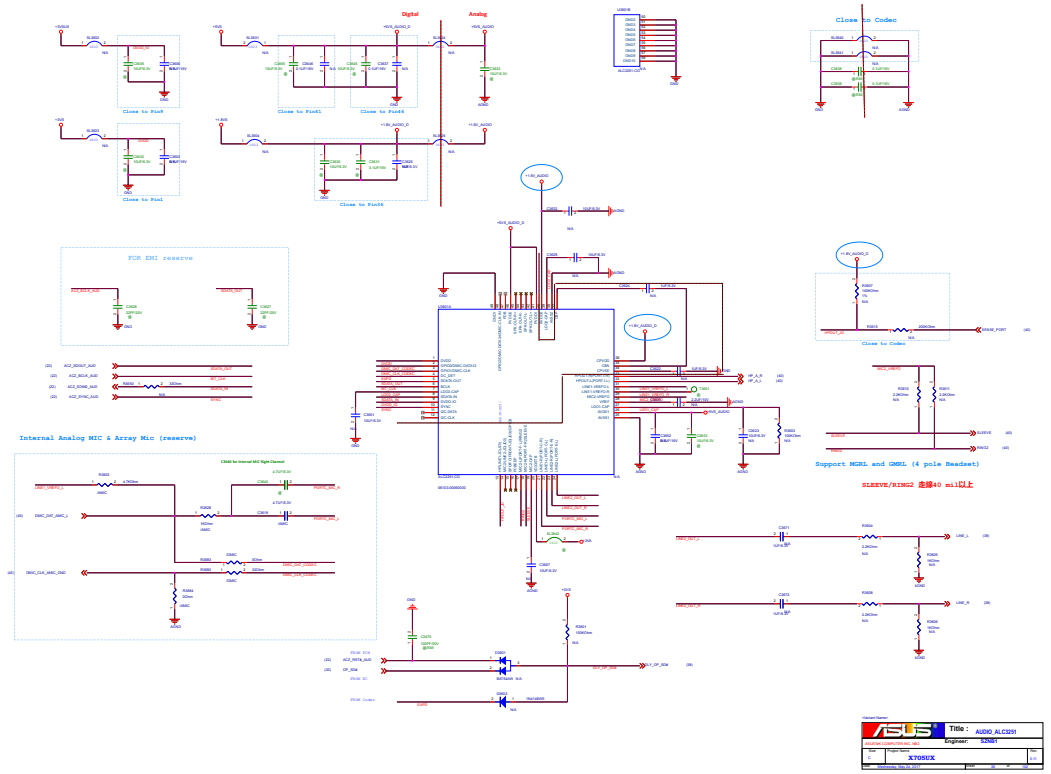

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- 042_IO Board_CR_AU6465R
- 043_
- 044_DEBUG_LPC
- 045_LCD_eDP_CMOS_DMIC
- 046_
- 047_
- 048_HDMI-Type-D
- 049_*****
- 050_Thermal Sensor & Fan
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- 053. NGFF_SSD_CONN
- 054_NGFF_WLAN_BT
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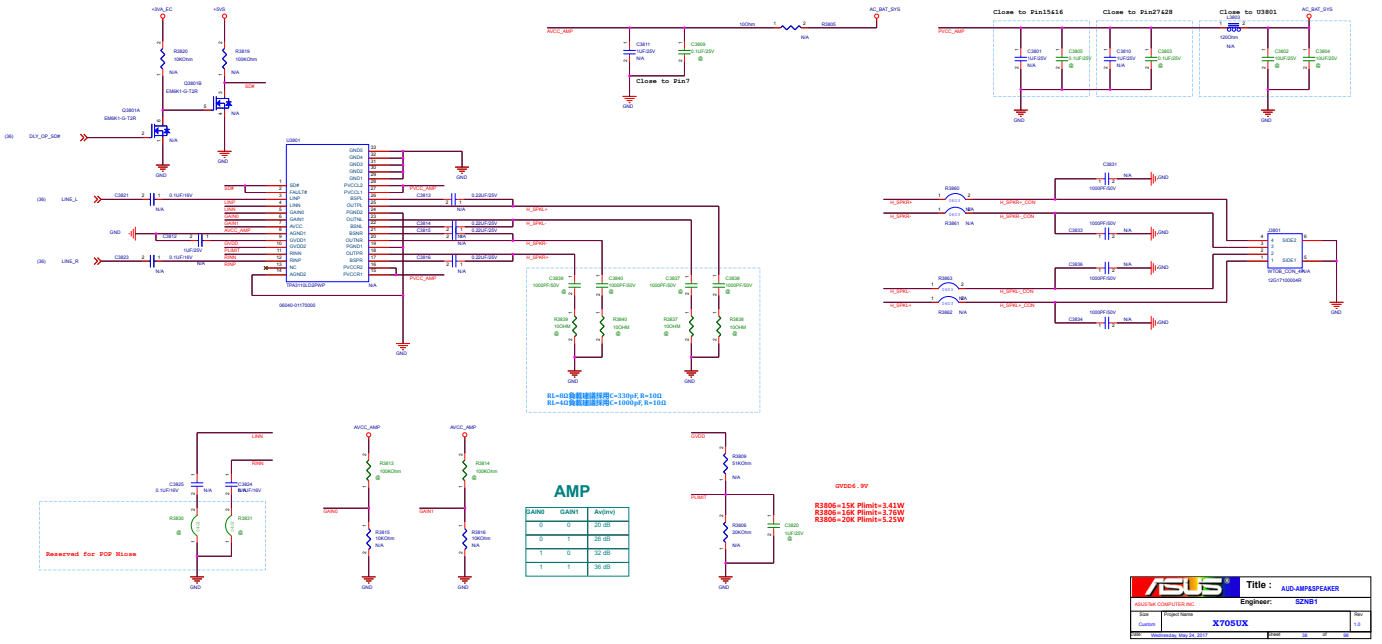

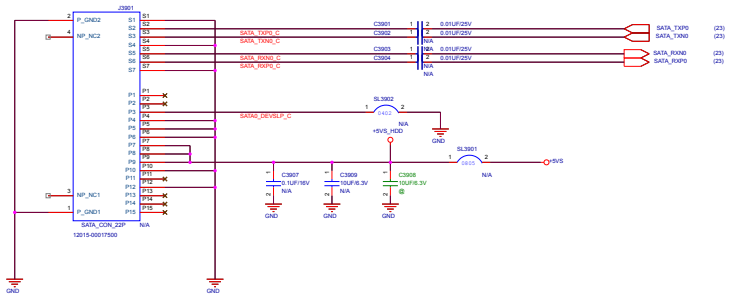

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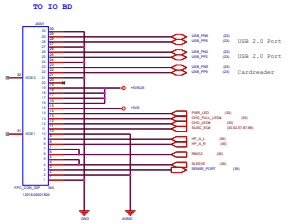
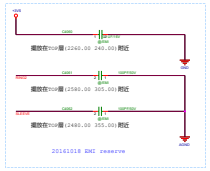
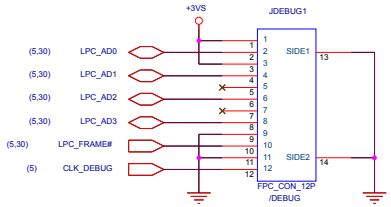




LPC Debug Port



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Title : SB_DEBUG_LPC

ASUSTeK COMPUTER INC.

Engineer: SZNB2

Size	Project Name	Rev
A	X705UX	R1.0

Date: Wednesday, May 24, 2017 Sheet 44 of 102

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- 036-AUDIO_CODEC
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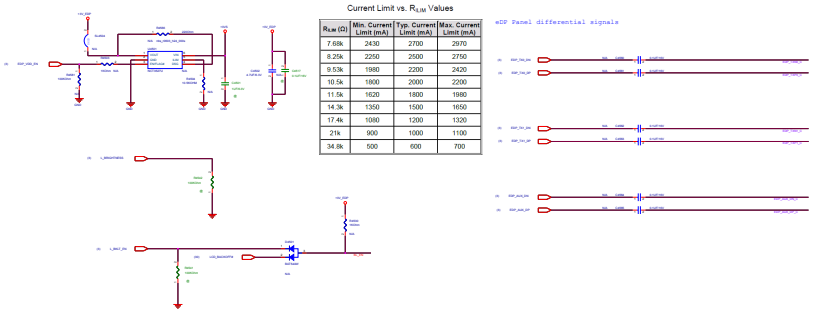

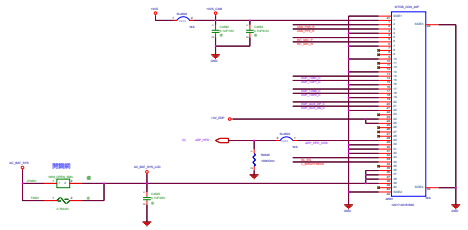

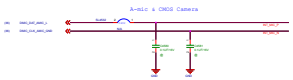

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- 045_LCD_eDP_CMOS_DMIC
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- 047_
- 048_HDMI-Type-D
- 049_*****
- 050_Thermal Sensor & Fan
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- 054_NGFF_WLAN_BT
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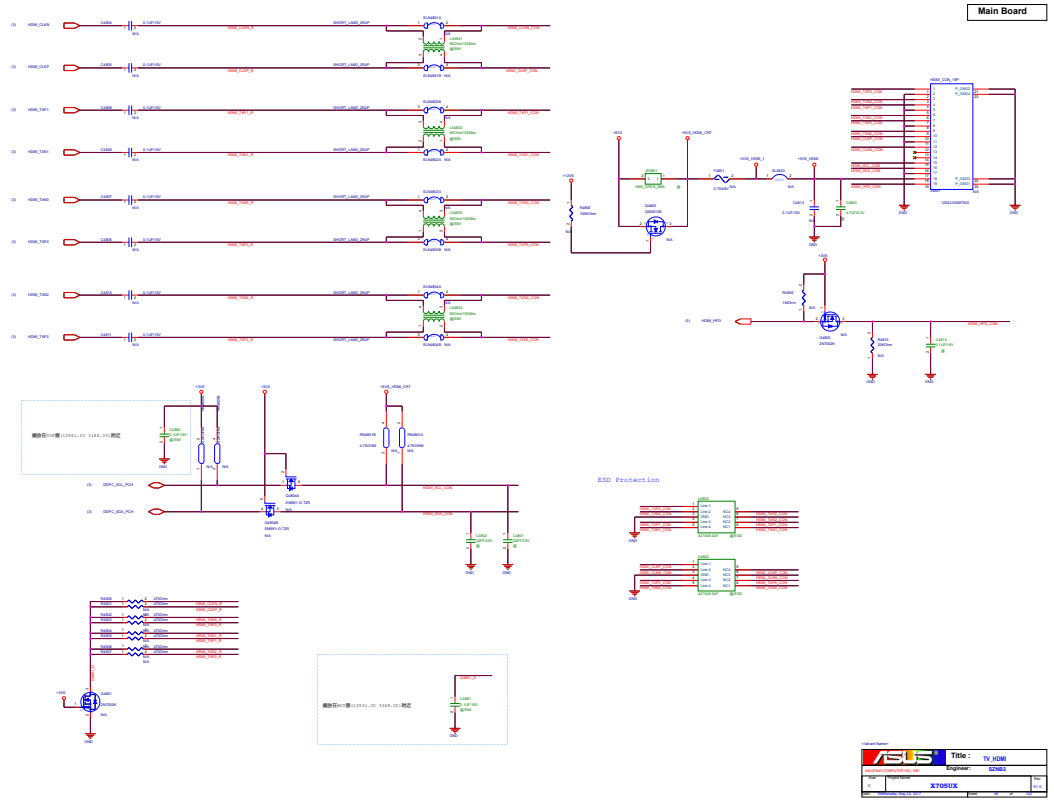

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- 044_DEBUG_LPC
- 045_LCD_eDP_CMOS_DMIC
- 046_
- 047_
- 048_HDMI-Type-D
- 049_*****
- 050_Thermal Sensor & Fan
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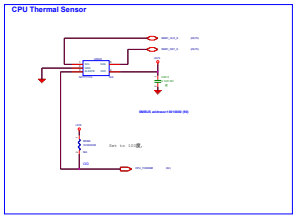
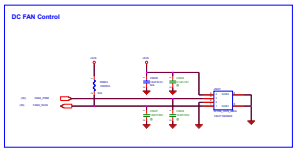
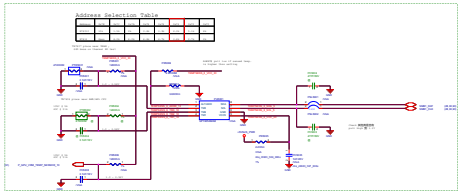


Main Board





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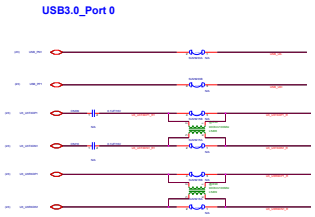

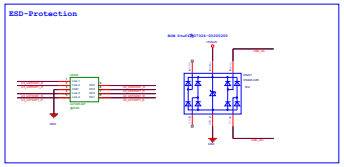

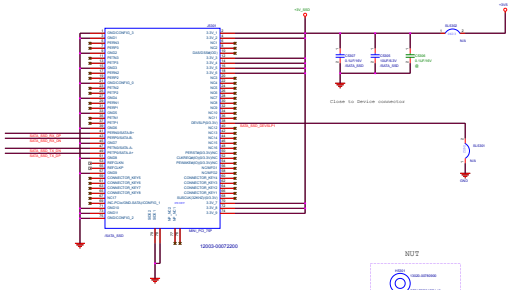

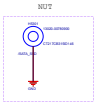

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

Table 36-7. SATA / PCI Express® Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to "Chapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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- 036-AUDIO_CODEC
- 037_
- 038_AUD-SPEAKER
- 039_SATA_HDD_CONN
- 040_B to B Connector
- 041_IO Board_USB_LED_FPC_Screw
- 042_IO Board_CR_AU6465R
- 043_
- 044_DEBUG_LPC
- 045_LCD_eDP_CMOS_DMIC
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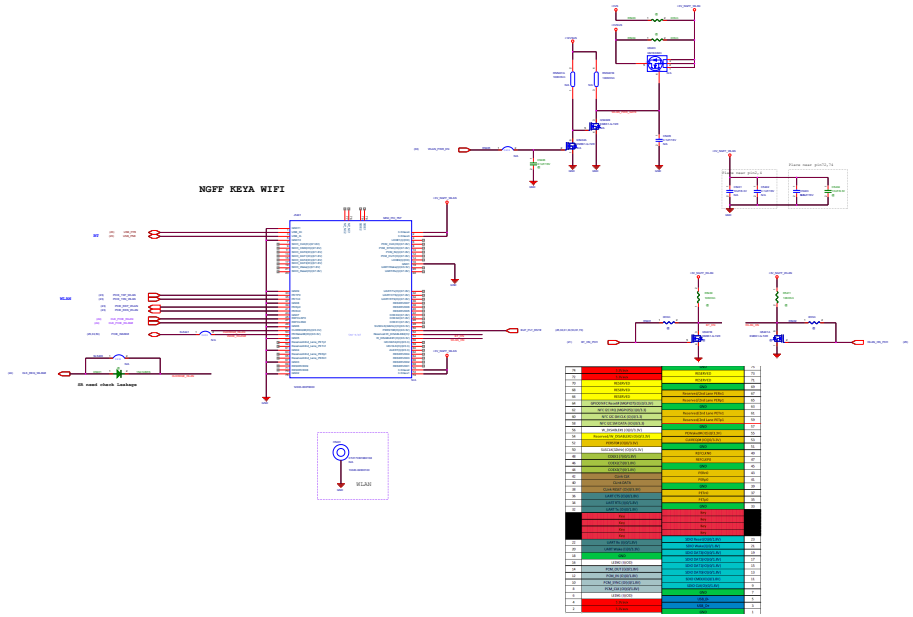

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- 044_DEBUG_LPC
- 045_LCD_eDP_CMOS_DMIC
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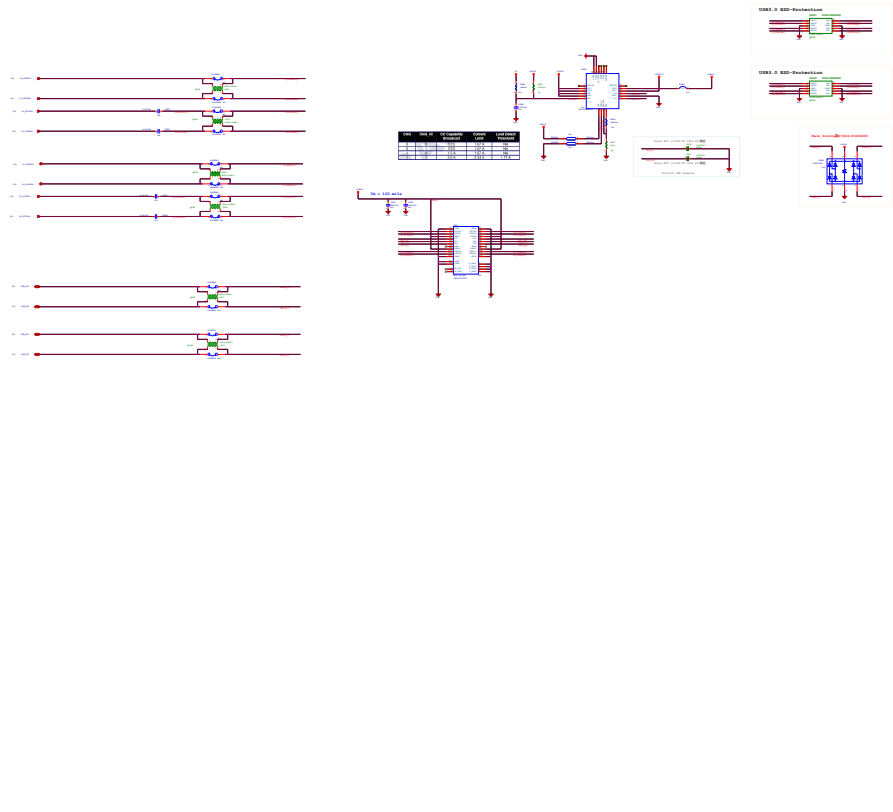

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- 054_NGFF_WLAN_BT
- 055_USB3.0_TYPEC
- 056_Hall Sensor & Power Switch
- 057_DSG_Discharge
- 058_PRO_Protect
- 059_*****
- 060_PW_DC_DC & BAT IN
- 061_EMI_RESERVE
- 062_*****
- 063_*****
- 064_*****
- 065_SKEW_HOLE_SMT_NUT
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- 067_*****
- 068_
- 069_*****
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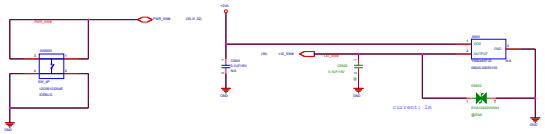
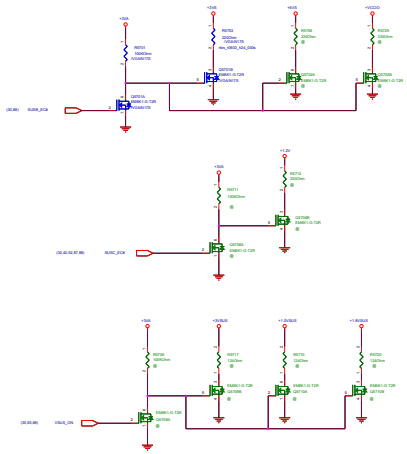
- 071_GPU_MEMORY INTERFACE





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072_VGA_GDDR5_(Bit0~63)

073_VGA_GDDR5_(NA)

074_VGA_nVIDIA_N16V/S_DISPLAY

075_GPU_GPIO_THERM

076_GPU_XTAL/STRAPPING

077_GPU_PWG/GND

078_GPU_Power_Sel

079_*****

080_PW_KABY LAKE-U(1)

081_PW_KABY LAKE-U(2)

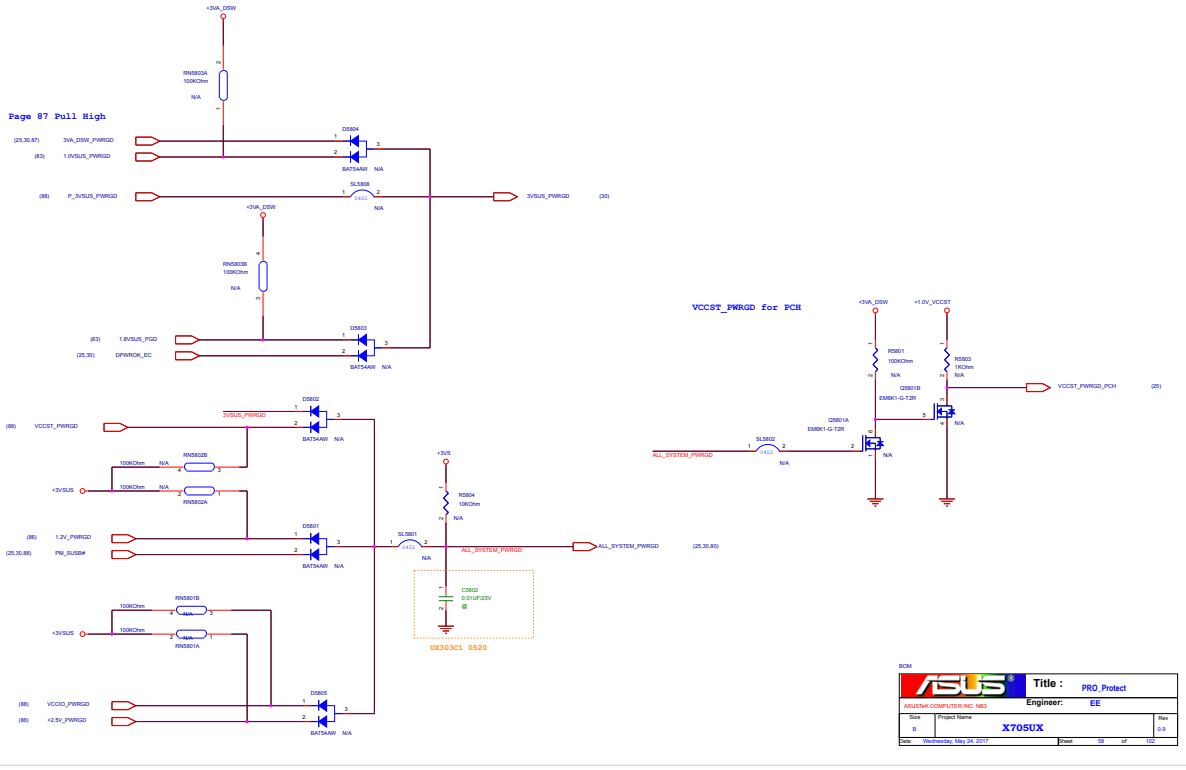
082_PW_***

083_PW_+1.0VSUS/1.8VSUS(UP9002)

084_PW_

085_PW_***

086_PW_1.2V/+VTT/+2.5V(UP9002)



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071_GPU_MEMORY INTERFACE

072_VGA_GDDR5_(Bit0~63)

073_VGA_GDDR5_(NA)

074_VGA_nVIDIA_N16V/S_DISPLAY

075_GPU_GPIO_THERM

076_GPU_XTAL/STRAPPING

077_GPU_PWG/GND

078_GPU_Power_Sel

079_*****

080_PW_KABY LAKE-U(1)

081_PW_KABY LAKE-U(2)

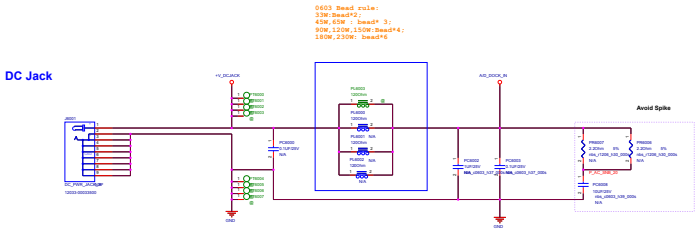
082_PW_***

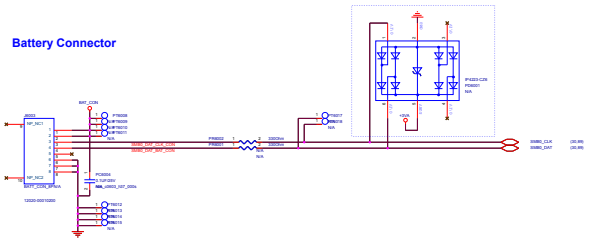
083_PW_+1.0VSUS/1.8VSUS(UP9002)

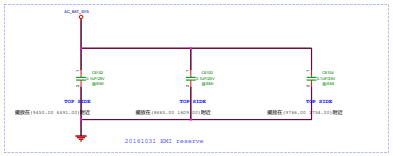
084_PW_

085_PW_***

086_PW_1.2V/+VTT/+2.5V(UP9002)





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Engineer:
X705UX

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073_VGA_GDDR5_(NA)

074_VGA_nVIDIA_N16V/S_DISPLAY

075_GPU_GPIO_THERM

076_GPU_XTAL/STRAPPING

077_GPU_PWG/GND

078_GPU_Power_Sel

079_*****

080_PW_KABY LAKE-U(1)

081_PW_KABY LAKE-U(2)

082_PW_***

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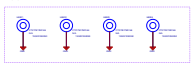
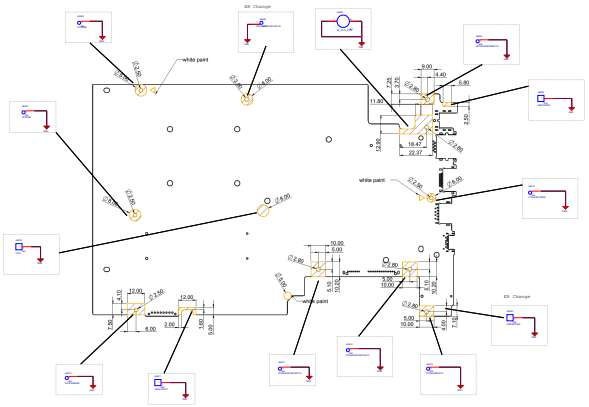
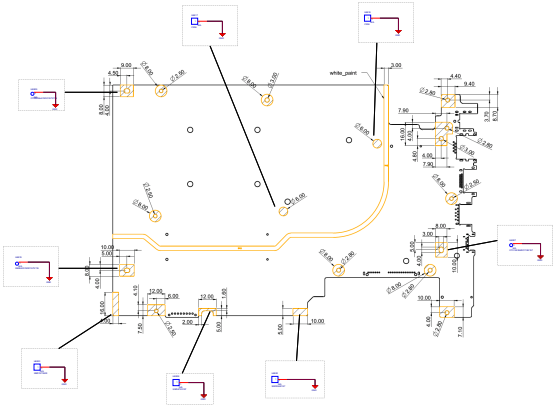
084_PW_

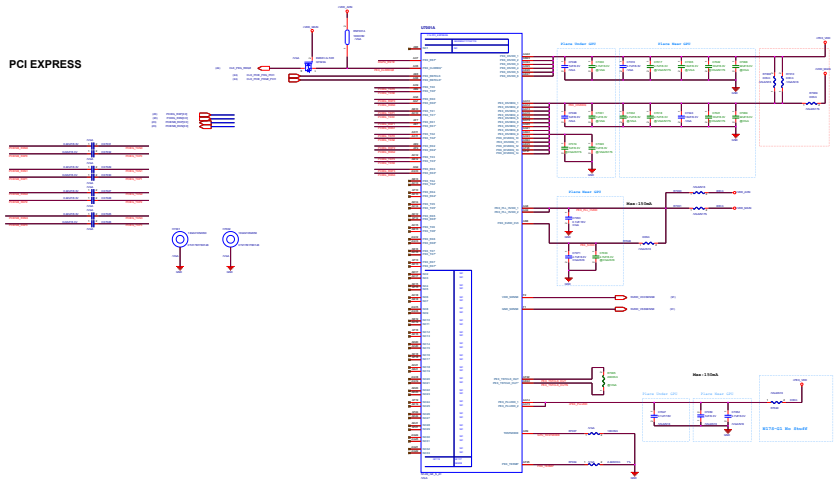
085_PW_***

086_PW_1.2V/+VTT/+2.5V(UP9002)









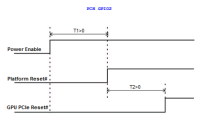


Figure 18-4. Cold Reset Sequence Requirement for Optimus

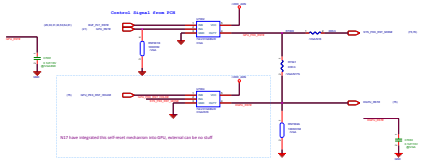


Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

Note: All GPIO, I2CA/B/C/5, DAC_H/V_SYNC, PCIE Reset, CLKREQ#, XTAL, and JTAG signals, when pulled-up, should be connected to 3V3_AON power rail. Also PEX_PLL_HVDD and PEX_3V3_SVDD must be sourced by 3V3_AON.

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
PEX_PLLVDD Supply Rail					
GB2B-64	0.1 µF	X7R	0402	1	N/A	Under GPU
	1.0 µF	X5R	0603	1	N/A	Near GPU
	4.7 µF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail					
GB2B-64	4.7 µF	X5R	0603	2	N/A	Near GPU
PEX_PLL_HVDD Supply Rail					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

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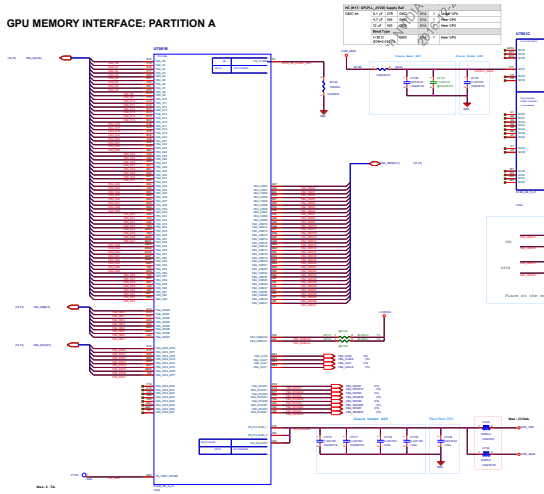
- 068_
- 069_*****
- 070_GPU_PCI-EXPRESS
- 071_GPU_MEMORY INTERFACE
- 072_VGA_GDDR5_(Bit0~63)
- 073_VGA_GDDR5_(NA)
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_GPU_GPIO_THERM
- 076_GPU_XTAL/STRAPPING
- 077_GPU_PWG/GND
- 078_GPU_Power_Sel
- 079_*****
- 080_PW_KABY LAKE-U(1)
- 081_PW_KABY LAKE-U(2)
- 082_PW_***
- 083_PW_+1.0VSUS/1.8VSUS(UP9002)
- 084_PW_
- 085_PW_***
- 086_PW_1.2V/+VTT/+2.5V(UP9002)



GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 3V3_MAIN (N17 VDD18) Supply Rail					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	2	Under GPU
	1.0 µF	X65	0603	1	1	Near GPU
	4.7 µF	X65	0603	1	1	Near GPU
N16 3V3_AON (N17 1V8_AON) Supply Rail					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Under GPU
	1.0 µF	X65	0603	1	1	Near GPU
	4.7 µF	X65	0603	1	1	Near GPU

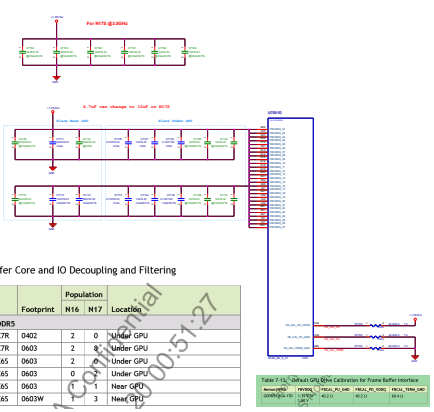


Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X65	0805	1	1	Near GPU
Bead Type					
	30 Ω (ESR=0.01Ω @)		0603	1	1	Near GPU

Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	0	Under GPU
	4.7 µF	X65	0603	2	0	Under GPU
	10 µF	X65	0603	0	2	Under GPU
	10 µF	X65	0603		1	Near GPU
	22 µF	X65	0603W		3	Near GPU

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068_

069_*****

070_GPU_PCI-EXPRESS

071_GPU_MEMORY INTERFACE

072_VGA_GDDR5_(Bit0~63)

073_VGA_GDDR5_(NA)

074_VGA_nVIDIA_N16V/S_DISPLAY

075_GPU_GPIO_THERM

076_GPU_XTAL/STRAPPING

077_GPU_PWG/GND

078_GPU_Power_Sel

079_*****

080_PW_KABY LAKE-U(1)

081_PW_KABY LAKE-U(2)

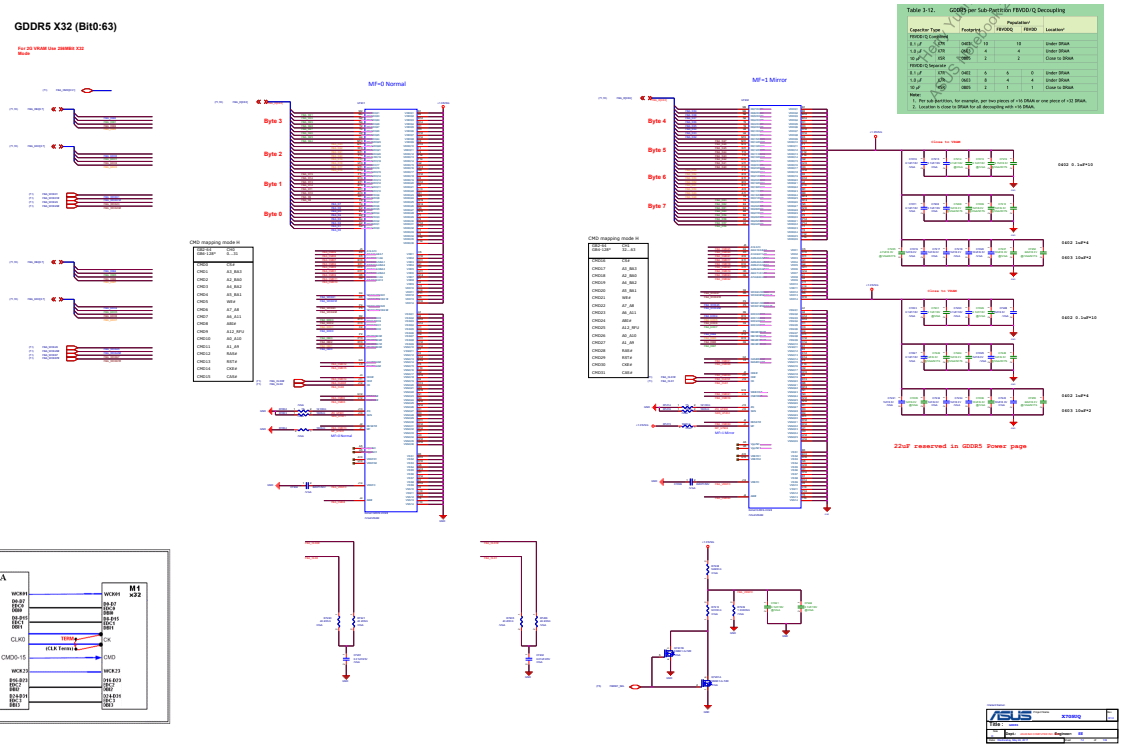
082_PW_***

083_PW_+1.0VSUS/1.8VSUS(UP9002)

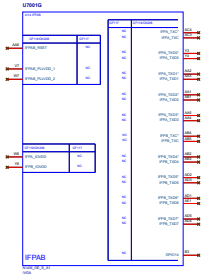
084_PW_

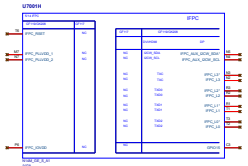
085_PW_***

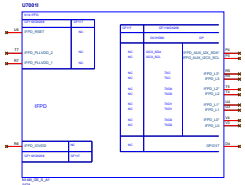
086_PW_1.2V/+VTT/+2.5V(UP9002)

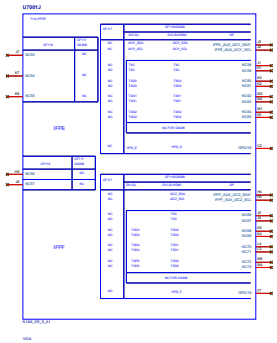


LVDS









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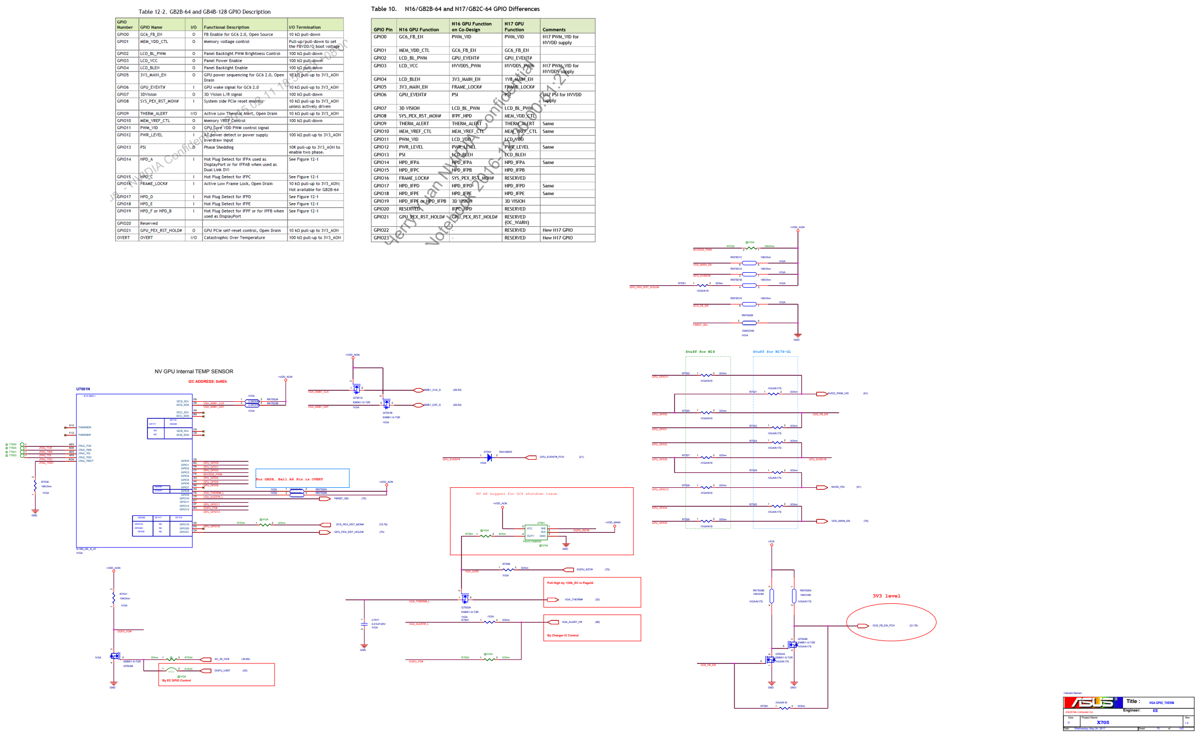

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072_VGA_GDDR5_(Bit0~63)

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074_VGA_nVIDIA_N16V/S_DISPLAY

075_GPU_GPIO_THERM

076_GPU_XTAL/STRAPPING

077_GPU_PWG/GND

078_GPU_Power_Sel

079_*****

080_PW_KABY LAKE-U(1)

081_PW_KABY LAKE-U(2)

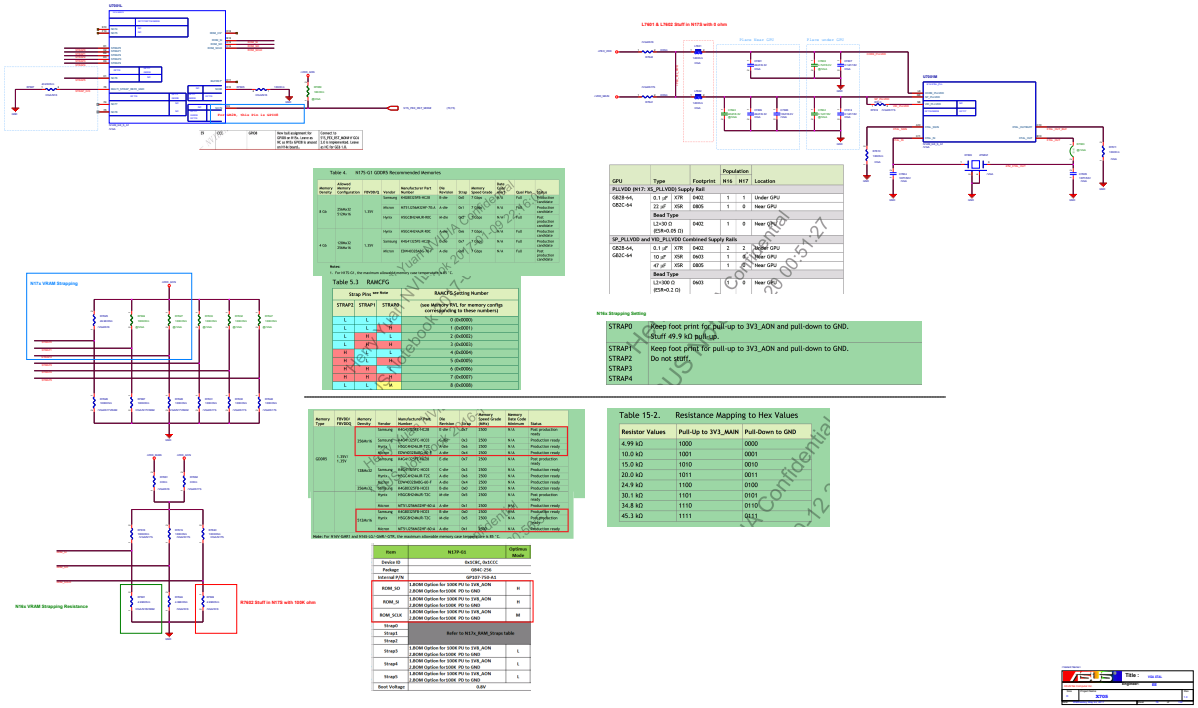
082_PW_***

083_PW_+1.0VSUS/1.8VSUS(UP9002)

084_PW_

085_PW_***

086_PW_1.2V/+VTT/+2.5V(UP9002)



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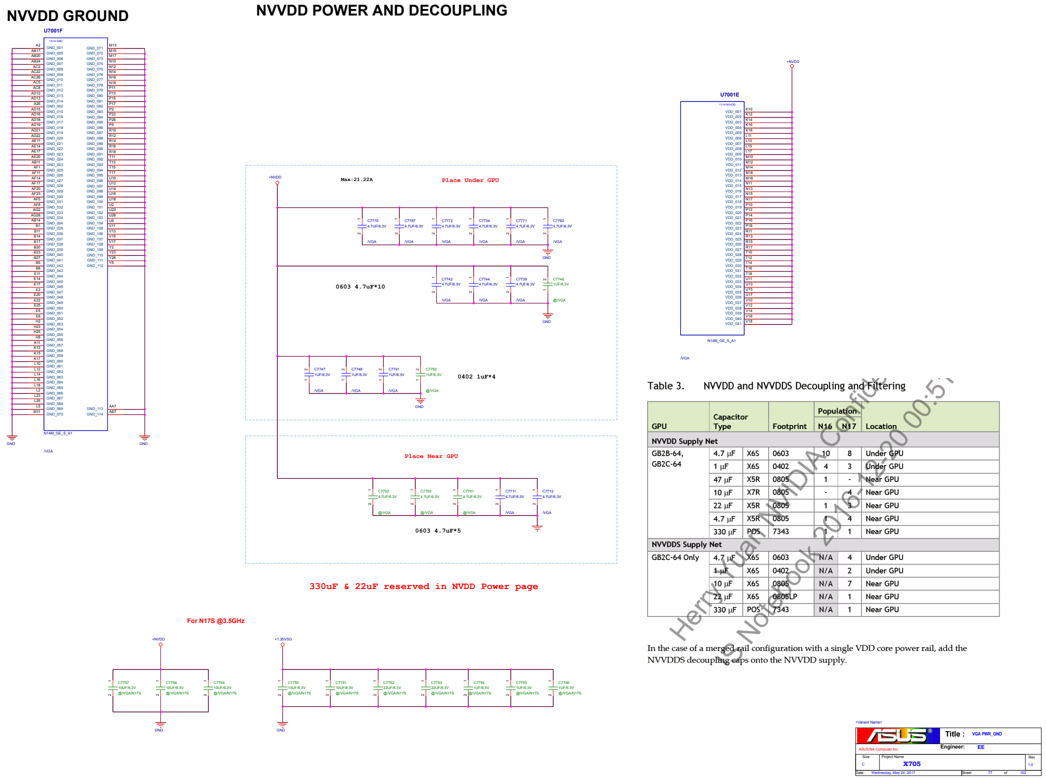

Table 3. NVVDD and NVVDDS Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
NVVDD Supply Net						
GB2B-64, GB2C-64	4.7 µF	X6S	0603	10	8	Under GPU
	1 µF	X6S	0402	4	3	Under GPU
	47 µF	X5R	0805	1	-	Near GPU
	10 µF	X7R	0805	-	4	Near GPU
	22 µF	X5R	0805	1	3	Near GPU
	4.7 µF	X5R	0805	1	4	Near GPU
	330 µF	POS	7343	1	1	Near GPU
NVVDDS Supply Net						
GB2C-64 Only	4.7 µF	X6S	0603	N/A	4	Under GPU
	1 µF	X6S	0402	N/A	2	Under GPU
	10 µF	X6S	0805	N/A	7	Near GPU
	22 µF	X6S	0805LP	N/A	1	Near GPU
	330 µF	POS	7343	N/A	1	Near GPU

In the case of a merged rail configuration with a single VDD core power rail, add the NVVDDS decoupling caps onto the NVVDD supply.

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- 076_GPU_XTAL/STRAPPING
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- 078_GPU_Power_Sel
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- 084_PW_
- 085_PW_***
- 086_PW_1.2V/+VTT/+2.5V(UP9002)
- 087_PW_+3VADSW/+5VSUS(UP9003)
- 088_PW_LOAD SWITCH
- 089.PW_CHARGER
- 090_PW_PROTECTION
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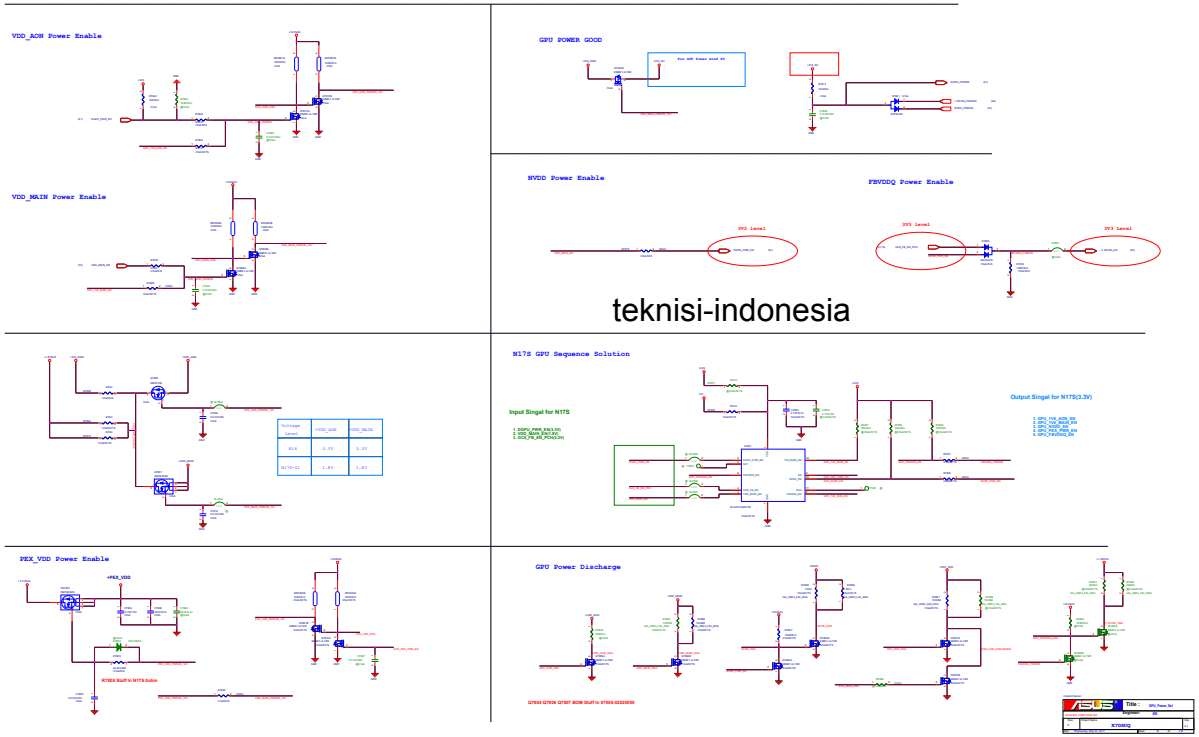

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- 085_PW_***
- 086_PW_1.2V/+VTT/+2.5V(UP9002)
- 087_PW_+3VADSW/+5VSUS(UP9003)
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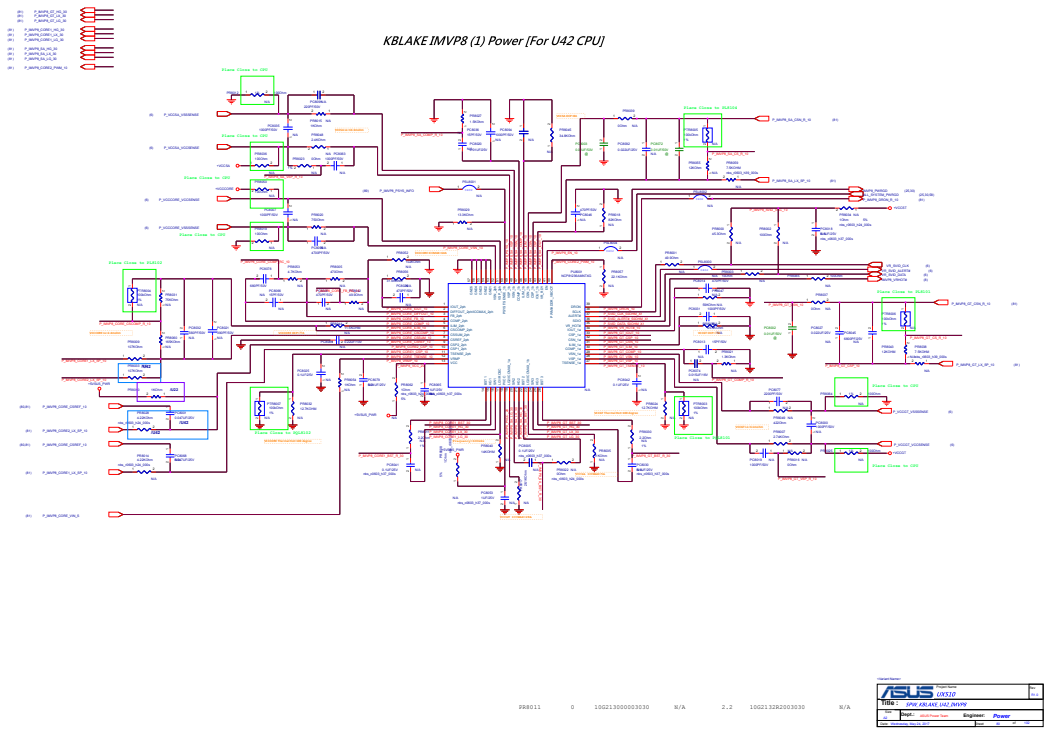

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- 081_PW_KABY LAKE-U(2)
- 082_PW_***
- 083_PW_+1.0VSUS/1.8VSUS(UP9002)
- 084_PW_
- 085_PW_***
- 086_PW_1.2V/+VTT/+2.5V(UP9002)
- 087_PW_+3VADSW/+5VSUS(UP9003)
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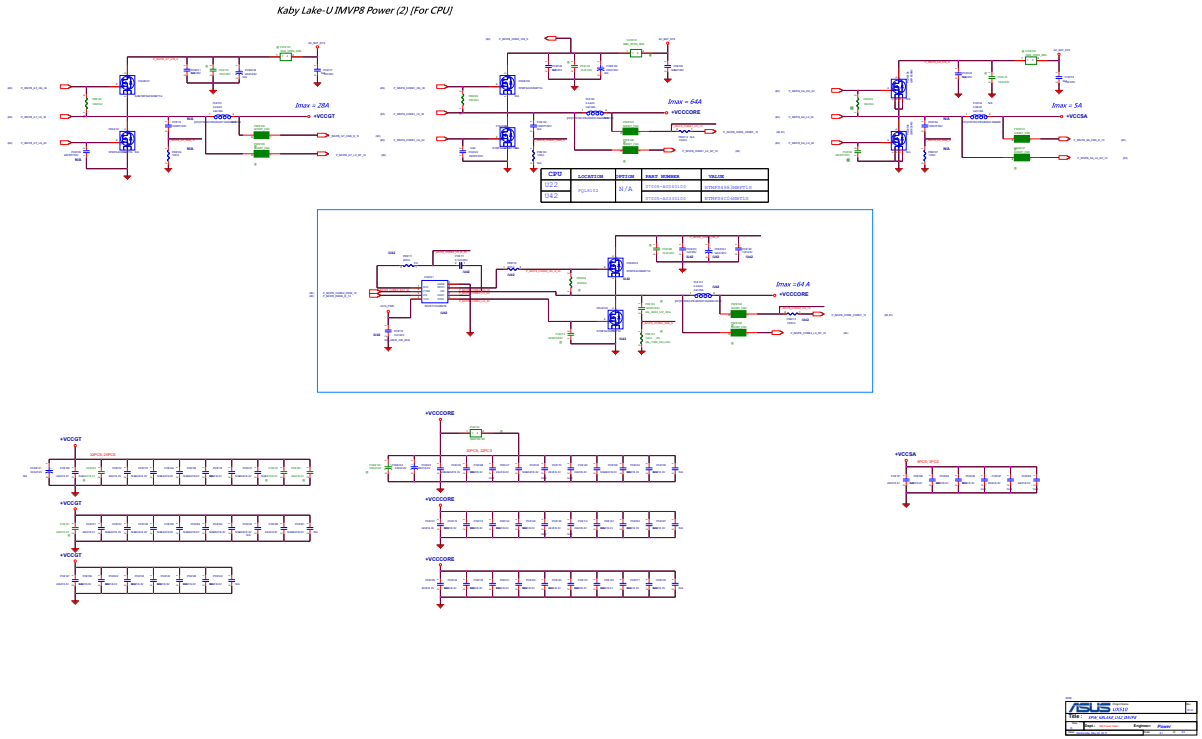
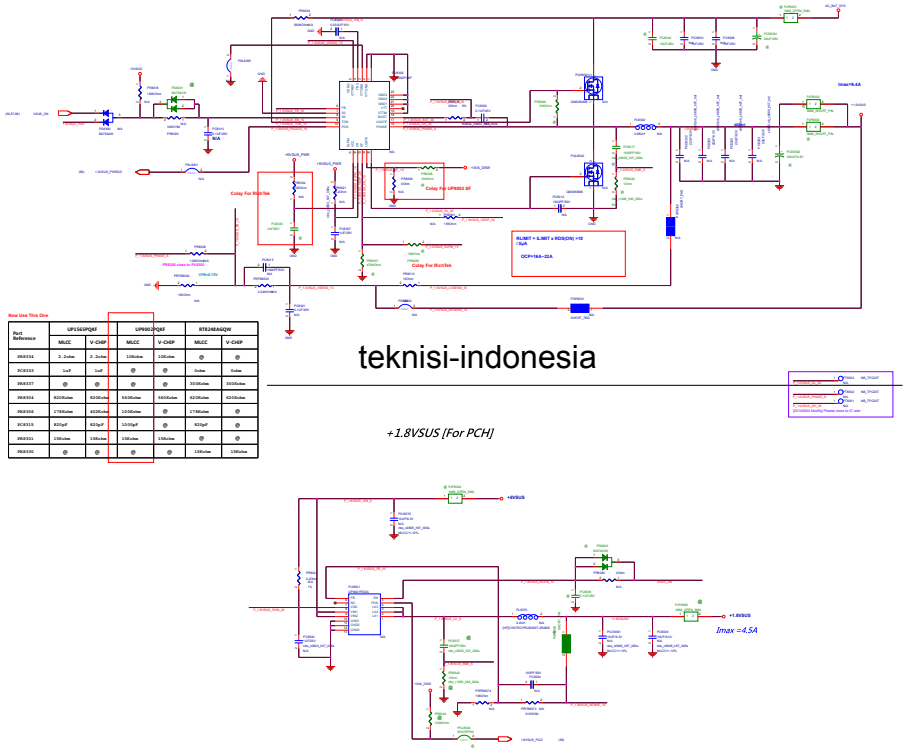
- 091_PW_DGPU_2PHASE(uP9024)

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- 081_PW_KABY LAKE-U(2)
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- 086_PW_1.2V/+VTT/+2.5V(UP9002)
- 087_PW_+3VADSW/+5VSUS(UP9003)
- 088_PW_LOAD SWITCH
- 089.PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_DGPU_2PHASE(uP9024)

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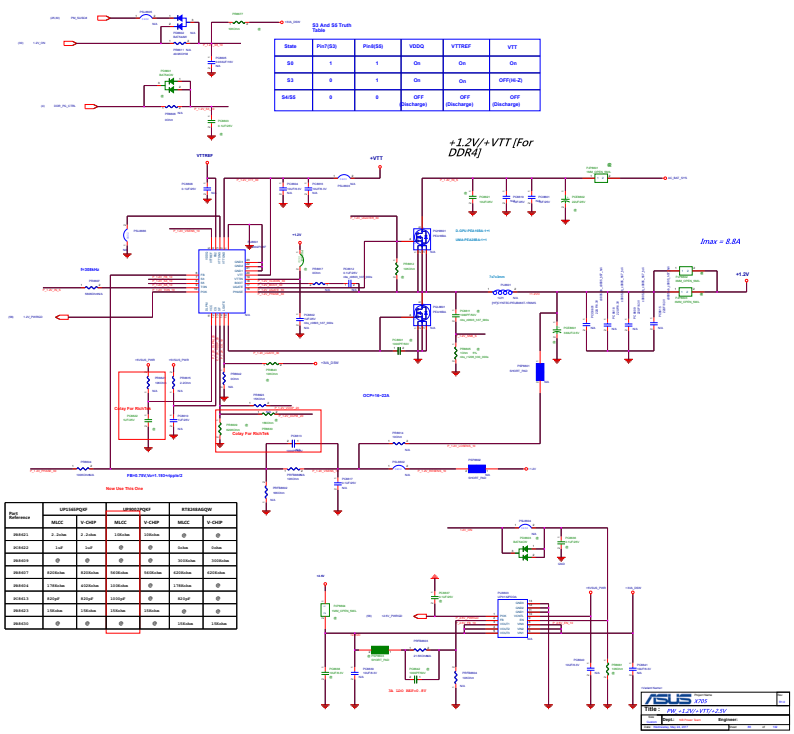

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- 077_GPU_PWG/GND
- 078_GPU_Power_Sel
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- 081_PW_KABY LAKE-U(2)
- 082_PW_***
- 083_PW_+1.0VSUS/1.8VSUS(UP9002)
- 084_PW_
- 085_PW_***
- 086_PW_1.2V/+VTT/+2.5V(UP9002)
- 087_PW_+3VADSW/+5VSUS(UP9003)
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- 089.PW_CHARGER
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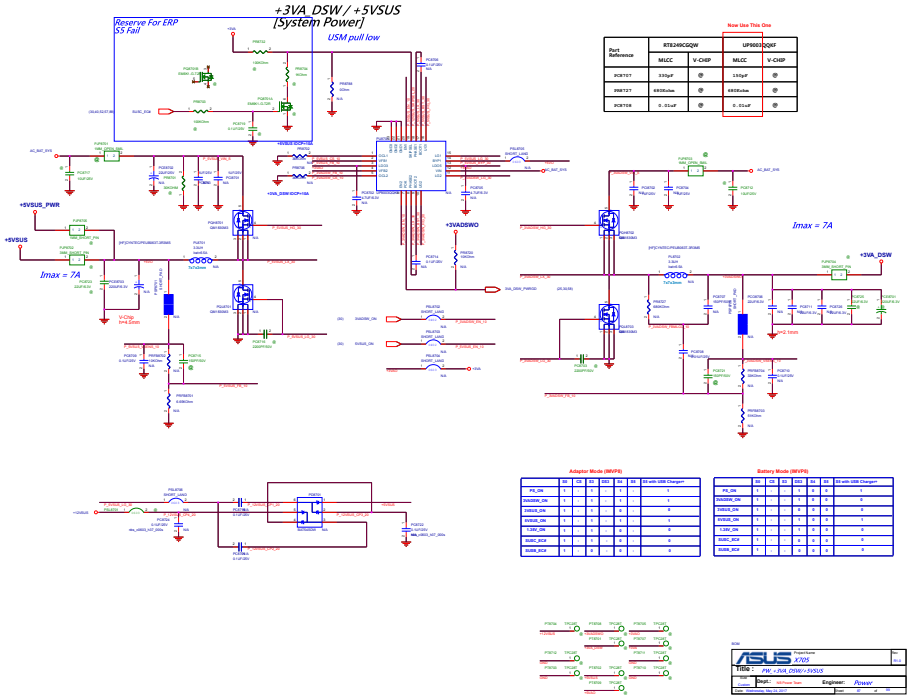

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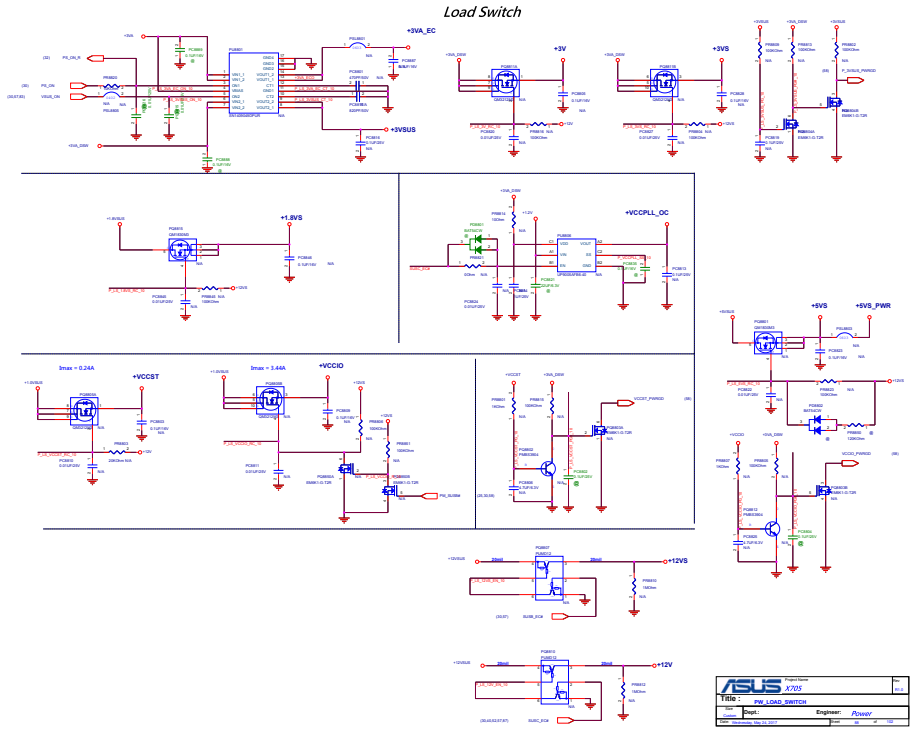
- 077_GPU_PWG/GND
- 078_GPU_Power_Sel
- 079_*****
- 080_PW_KABY LAKE-U(1)
- 081_PW_KABY LAKE-U(2)
- 082_PW_***
- 083_PW_+1.0VSUS/1.8VSUS(UP9002)
- 084_PW_
- 085_PW_***
- 086_PW_1.2V/+VTT/+2.5V(UP9002)
- 087_PW_+3VADSW/+5VSUS(UP9003)
- 088_PW_LOAD SWITCH
- 089.PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_DGPU_2PHASE(uP9024)



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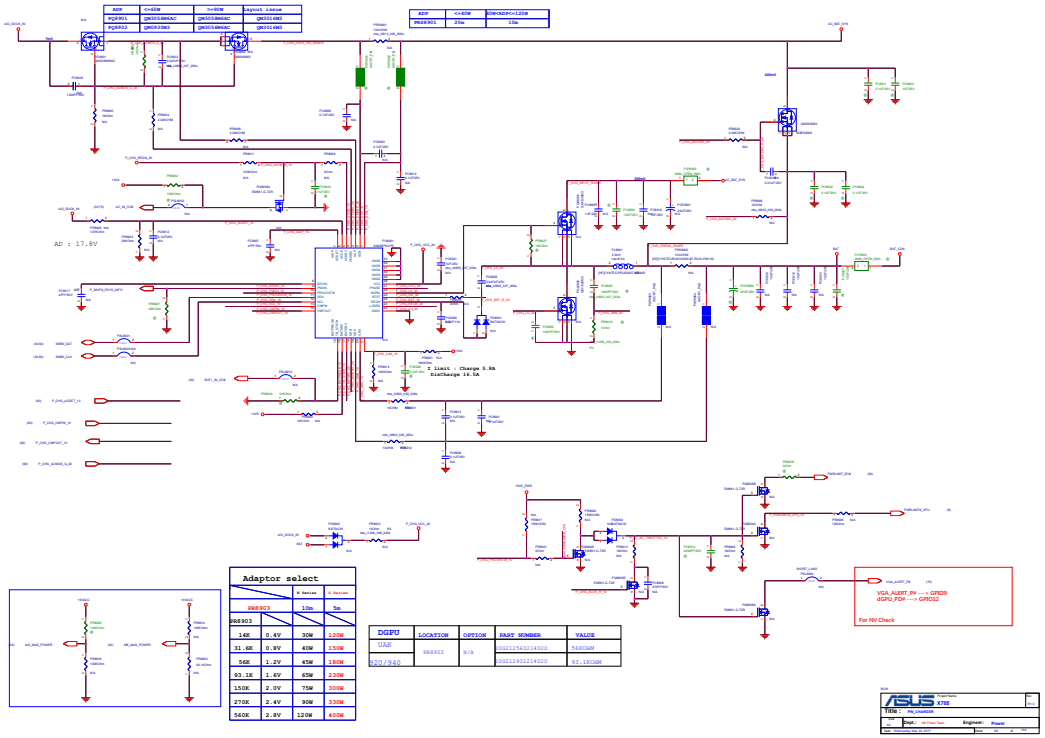
- AY
- 075_GPU_GPIO_THERM
- 076_GPU_XTAL/STRAPPING
- 077_GPU_PWG/GND
- 078_GPU_Power_Sel
- 079_*****
- 080_PW_KABY LAKE-U(1)
- 081_PW_KABY LAKE-U(2)
- 082_PW_***
- 083_PW_+1.0VSUS/1.8VSUS(UP9002)
- 084_PW_
- 085_PW_***
- 086_PW_1.2V/+VTT/+2.5V(UP9002)
- 087_PW_+3VADSW/+5VSUS(UP9003)
- 088_PW_LOAD SWITCH
- 089.PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_DGPU_2PHASE(uP9024)



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- 082_PW_***
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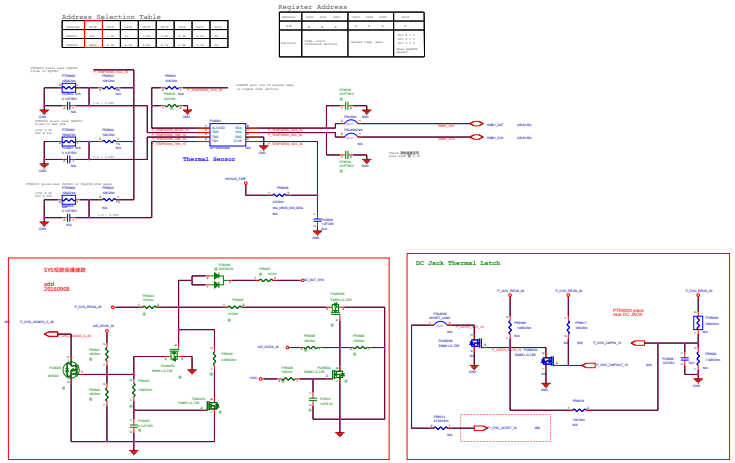
- 087_PW_+3VADSW/+5VSUS(UP9003)
- 088_PW_LOAD SWITCH
- 089.PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_DGPU_2PHASE(uP9024)



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- AY
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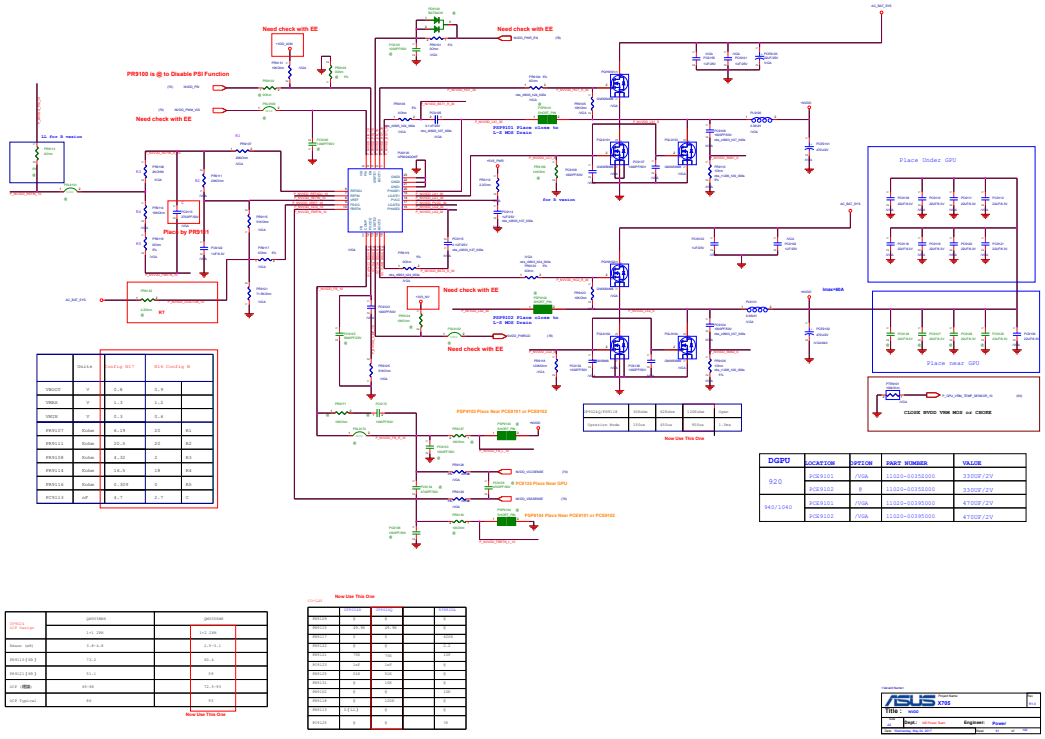
Global Search | 077 | 078 | 080 | 081 | 083 | 086 | 087 | 088 | 089 | 090 | 091

Toggle FullScreen | Pre Page | Next Page | MoveTo



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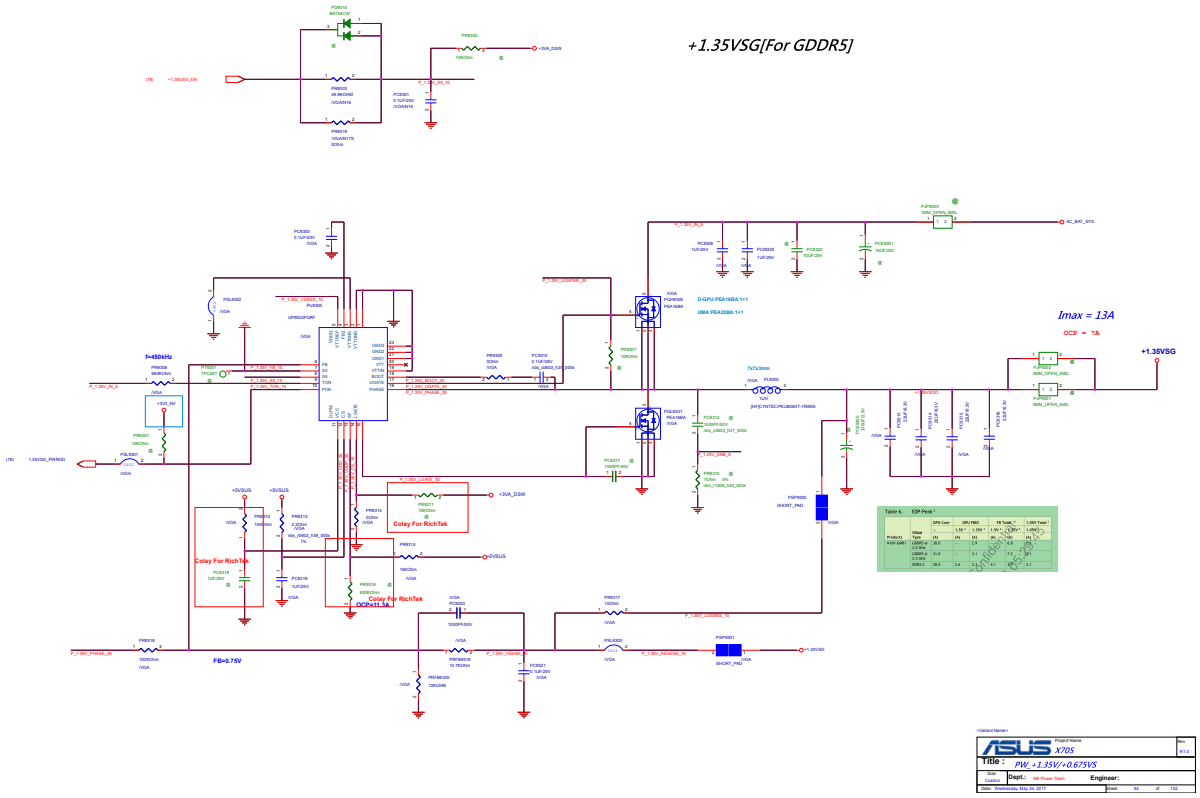

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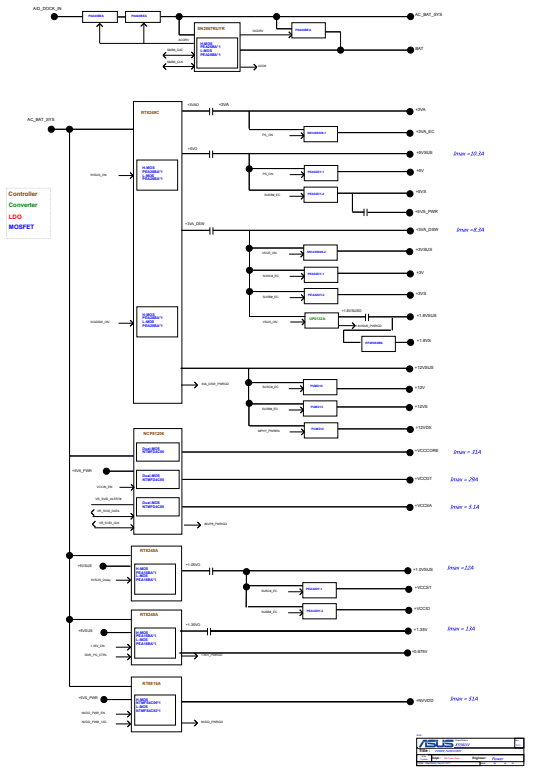
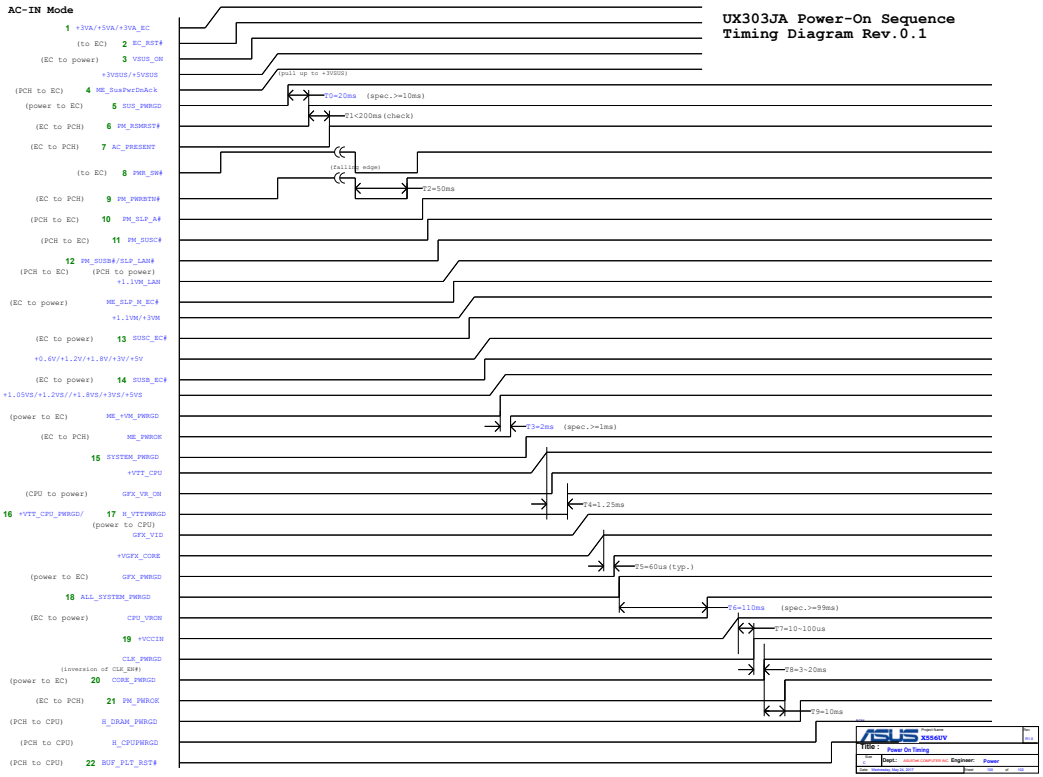
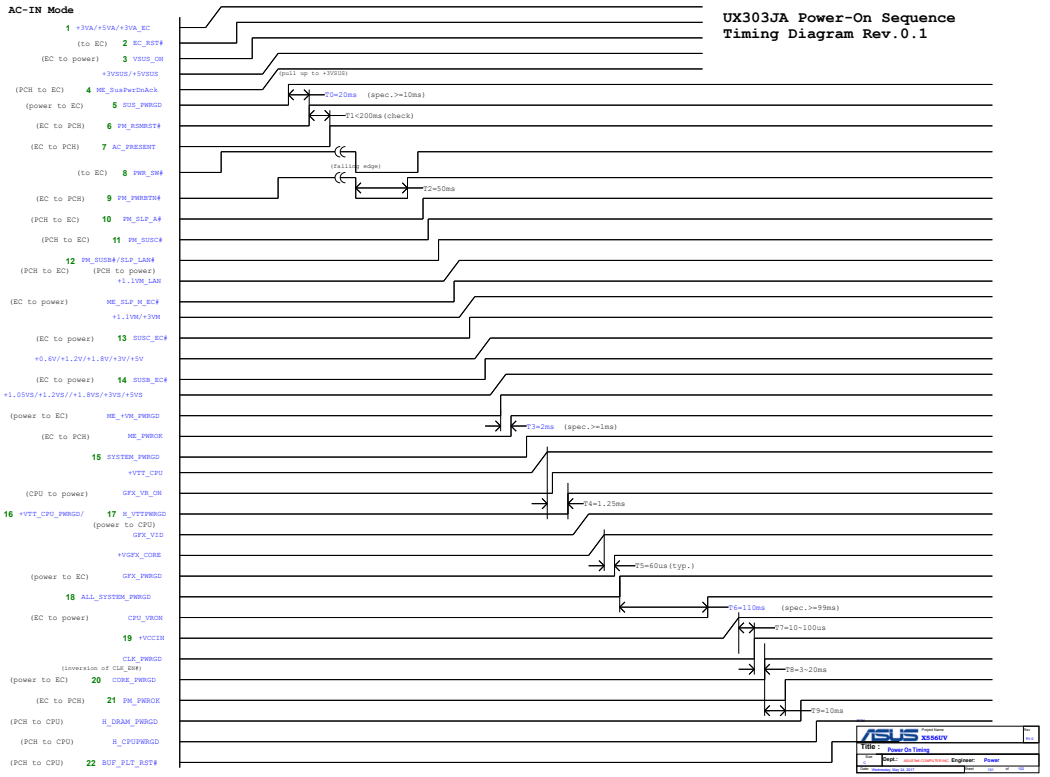
Engineer:	







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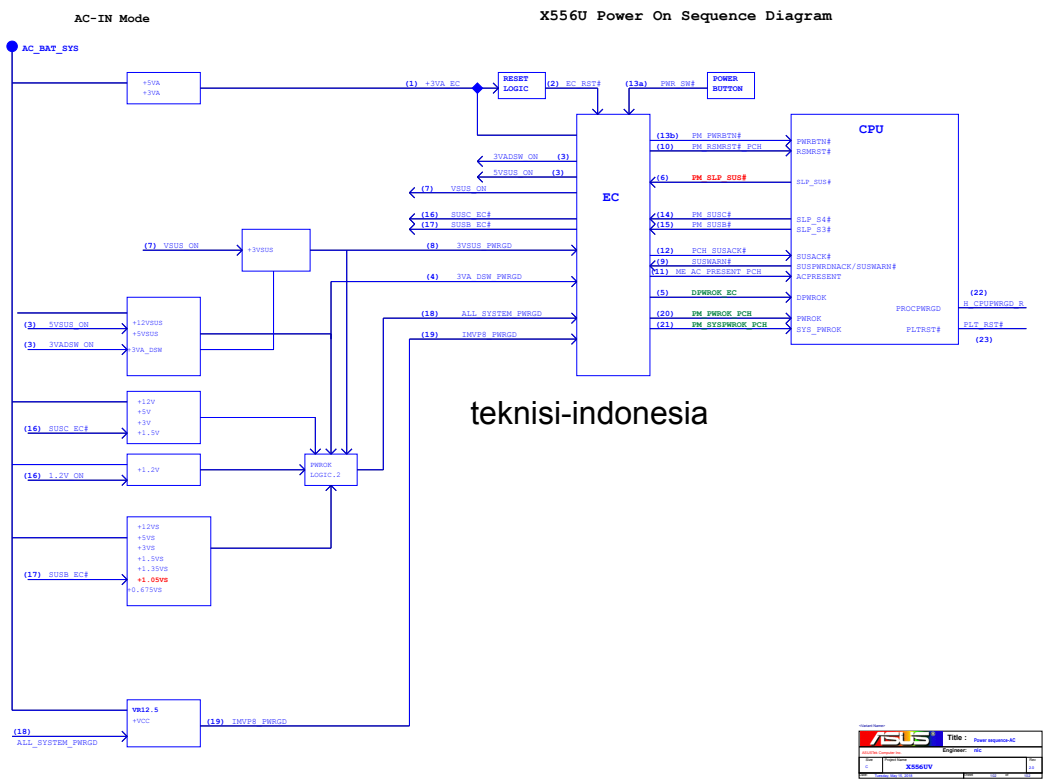

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