1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-01-12

D7 MLB

LAST_MODIFIED=Thu Jan 12 10:24:09 2012

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97	110	Platform VReg Constraints	D7_DAVE 12/12/2011
98	111	TBT/DP Constraints	D7_NICK 12/13/2011
99	112	GDDR5/GPU Constraints	D7_DAVE 12/12/2011
100	113	BLC Constraints	D7_DAVE 12/12/2011

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9509	1	SCH,MLB,D7	SCH	CRITICAL	
820-3302	1	PCBF,MLB,D7	PCB	CRITICAL	

DRAWING
TITLE=D7
ABBREV=DRAWING
LAST_MODIFIED=Thu Jan 12 10:24:09 2012

DRAWING TITLE: SCH,D7,MLB

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DRAWING NUMBER: 051-9509 SIZE: D
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System Block diagram can be found on Kismet

PATH: Kismet > K70/72 > Block Diagrams > K70 Block Diagram

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE
System Block Diagram

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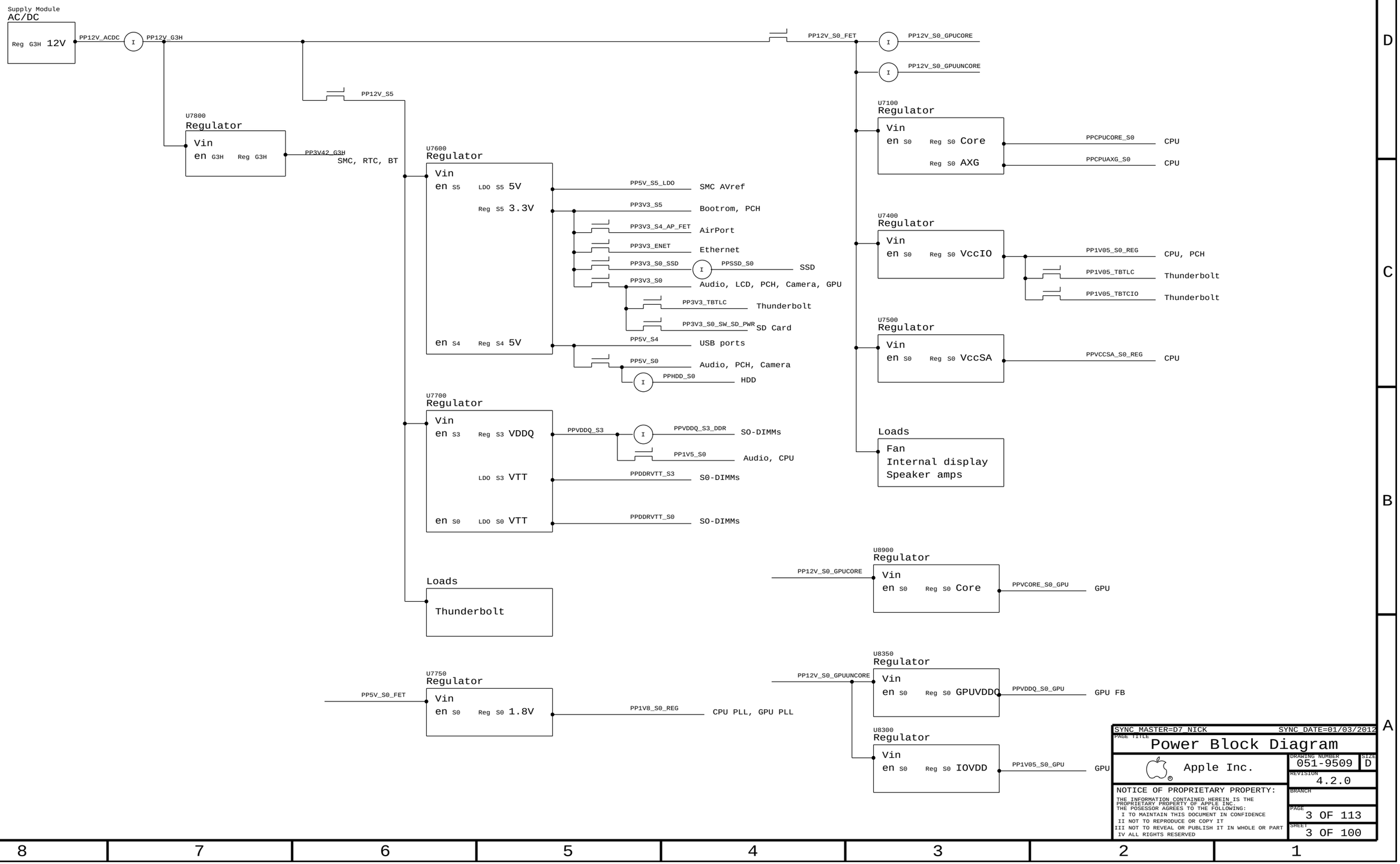

SYNC_MASTER=D7 NICK SYNC_DATE=01/03/2012

PAGE TITLE
Power Block Diagram

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Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-4441	PCBA,MLB,DEV,D7	DEVELOPMENT,D7_DEVEL
639-3566	PCBA,MLB,D7,GSA,GOOD	D7_COMMON,CPU:GOOD,GPU:GSA,GS,FBA,SSD:N,EEEE:DF98
639-3668	PCBA,MLB,D7,GSB,GOOD	D7_COMMON,CPU:GOOD,GPU:GSB,GS,FBB,SSD:N,EEEE:F117
639-3567	PCBA,MLB,D7,GTX,BETTER	D7_COMMON,CPU:BETTER,GPU:107GTX,FBA,FBB,SSD:Y,EEEE:DT42
639-3665	PCBA,MLB,D7,GTX,CTO	D7_COMMON,CPU:CTO,GPU:107GTX,FBA,FBB,SSD:Y,EEEE:F116

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7122	1	MLB LABEL,48.0X4.8	EEEE_DF98	CRITICAL	EEEE:DF98
825-7122	1	MLB LABEL,48.0X4.8	EEEE_DT42	CRITICAL	EEEE:DT42
825-7122	1	MLB LABEL,48.0X4.8	EEEE_F116	CRITICAL	EEEE:F116
825-7122	1	MLB LABEL,48.0X4.8	EEEE_F117	CRITICAL	EEEE:F117

BOM Groups

BOM GROUP	BOM OPTIONS
D7_COMMON	COMMON,ALTERNATE,D7_COMMON1,D7_COMMON2,D7_PROGPARTS
D7_COMMON1	XDP,RSMRST:SMC,SPEAKERID,TBTHV:P12V
D7_COMMON2	SNS_CPUCORE:3PHASE,CPUCOREDRV:ISL6612,IG:N,GPU_ROM:YES,SNS_GPUS0:K70,SNS_VDDQS3_DDR:Y
D7_PROGPARTS	SMC:PROTO1,BOOTROM:PROG,T29ROM:PROG,CIVROM:PROG,CAMROM:PROG
D7_DEVEL	XDP_CONN,LPCPLUS,VREFMRGN:EXT,BKLT_PWM,DEVEL_SENSORS,DEVEL_AUDIO
DEVEL_SENSORS	SNS_VDDQS0_GPU:Y,SNS_VDDQS3:Y,TEMPSNSDEV
D7_PRODUCTION	SNS_VDDQS0_GPU:N,SNS_VDDQS3:N,VREFMRGN:N

Add 'K70_PRODUCTION' at RevA release

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4240	1	IVB,QC13,QS,E0,2.8G,65W,4+1,1.10,6M,LGA	CPU	CRITICAL	CPU:GOOD
337S4258	1	IVB,QC48,QS,E1,2.9G,65W,4+2,1.10,6M,LGA	CPU	CRITICAL	CPU:BETTER
337S4246	1	IVB,SR0PN,PRQ,E1,3.1G,65W,4+2,1.15,8M,LG	CPU	CRITICAL	CPU:CTO

Replace with 65W part

Module Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4234	1	IC,PCH,PPT-DT,Z77,QS,C1	U1800	CRITICAL	
338S1047	1	IC,TBT,CR-4C,ES1,288 FCBGA,12X12MM	U3600	CRITICAL	
337S4221	1	IC,GPU,NV,GK107-GS-2/1-QS-A	U8000	CRITICAL	GPU:GSA
337S4220	1	IC,GPU,NV,GK107-GS-2/1-QS-A	U8000	CRITICAL	GPU:GSB
337S4239	1	IC,GPU,NV,GK107-GTX-QS-A2	U8000	CRITICAL	GPU:107GTX
343S0592	1	IC,BCM57766,CIV+,A0,8X8	U3900	CRITICAL	
607-9432	1	K70,GDDR5,SAMSUNG	VRAM	CRITICAL	GPU:107GTX

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S3493	1	IC,CR,V24.2,D7/D7I	U3690	CRITICAL	T29ROM:PROG
335S0865	1	IC,EEPROM,SERIAL,256KB,MLP8	U3690	CRITICAL	T29ROM:BLANK
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5110	CRITICAL	BOOTROM:BLANK
341S3480	1	IC,PROGRMD,EFI ROM,K70	U5110	CRITICAL	BOOTROM:PROG
335S0862	1	IC,SERIAL FLASH,2MBIT,2.7V,REV F	U3990	CRITICAL	CIVROM:BLANK
341S3487	1	IC,ENET 1MBITFLASH,CIV,PVT,J40	U3990	CRITICAL	CIVROM:PROG
338S1098	1	IC,SMC12-A3,BLANK,D7	U4900	CRITICAL	SMC:BLANK
341S3484	1	IC,SMC,PROGRMD,PROTO1,D7	U4900	CRITICAL	SMC:PROTO1
341S3388	1	IC,SMC,PROGRMD,EVT,D7	U4900	CRITICAL	SMC:EVT
341S3389	1	IC,SMC,PROGRMD,DVT,D7	U4900	CRITICAL	SMC:DVT
341S3390	1	IC,SMC,PROGRMD,PVT,D7	U4900	CRITICAL	SMC:PVT
341S3409	1	IC,SMC,PROGRMD,PROD,D7	U4900	CRITICAL	SMC:PROD
341S3453	1	IC,CAMERA FLASH,K70/K72	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK

Alternate: 335S0812

Alternate: 335S0854

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0107	377S0126		ALL	USB diodes
157S0055	157S0058		ALL	Enet magnetics
376S1081	376S0975		ALL	P/NCh dual FET
341S3486	341S3487		ALL	P/NCh dual FET

CPU Socket

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0073	1	SOCKET,MOLEX,LGA1155,CPU-LF	U1000	CRITICAL	

CPU Socket Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
511S0071	511S0073		ALL	TYCO SOCKET
511S0072	511S0073		ALL	FOXCONN SOCKET

VRAM BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
607-9432	K70,GDDR5,SAMSUNG	FB:BOTH_SAMSUNG
607-9435	K70,GDDR5,HYNIX	FB:BOTH_HYNIX
607-9433	K70,GDDR5,SAMSUNG_CH1	FB:CH1_SAMSUNG
607-9436	K70,GDDR5,HYNIX_CH1	FB:CH1_HYNIX
607-9434	K70,GDDR5,SAMSUNG_CH2	FB:CH2_SAMSUNG
607-9437	K70,GDDR5,HYNIX_CH2	FB:CH2_HYNIX

VRAM Module Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0619	4	IC,SGRAM,GDDR5,32MX32,1.5GHz,G-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB:BOTH_SAMSUNG
333S0620	4	IC,GDDR5,32MX32,1.5GHZ,VEGA 44NM,B-DIE	U8400,U8450,U8500,U8550	CRITICAL	FB:BOTH_HYNIX
333S0631	2	IC,SGRAM,GDDR5,64MX32,4.2GBPS,D-DIE,HF	U8400,U8450	CRITICAL	FB:CH1_SAMSUNG
333S0630	2	IC,GDDR5,2GB,M-DIE,170B FBGA	U8400,U8450	CRITICAL	FB:CH1_HYNIX
333S0631	2	IC,SGRAM,GDDR5,64MX32,4.2GBPS,D-DIE,HF	U8500,U8550	CRITICAL	FB:CH2_SAMSUNG
333S0630	2	IC,GDDR5,2GB,M-DIE,170B FBGA	U8500,U8550	CRITICAL	FB:CH2_HYNIX

VRAM Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
607-9435	607-9432		VRAM	GDDR5_BOTH
607-9436	607-9433	GPU:GSA	VRAM	GDDR5_CH1
607-9437	607-9434	GPU:GSB	VRAM	GDDR5_CH2

GPU Module Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
607-9433	1	K70,GDDR5,SAMSUNG_CH1	VRAM	CRITICAL	GPU:GSA
607-9434	1	K70,GDDR5,SAMSUNG_CH2	VRAM	CRITICAL	GPU:GSB

Programmable Parts (unused)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0724	1	IC,1 MBIT SERIAL FLASH	U8701	CRITICAL	GPUROM:BLANK

SYNC_MASTER=D7_NICK SYNC_DATE=12/13/2011

PAGE TITLE: BOM Configuration

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DRAWING NUMBER: 051-9509 SIZE: D

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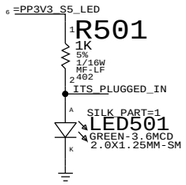
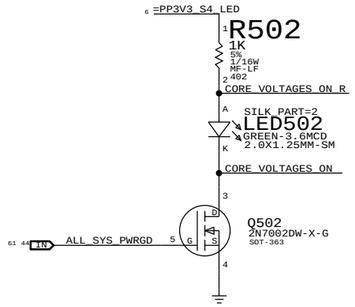
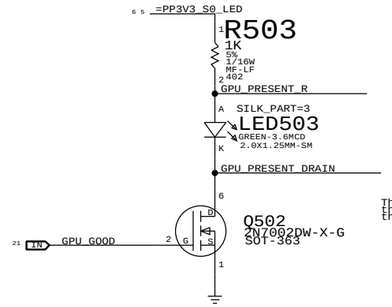
S5 Led



ALL_SYS_PWRGD Led

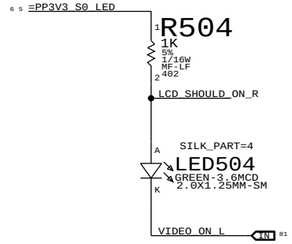


GPU GOOD Led



This LED is a GPIO driven from the southbridge that indicates that chipset has enumerated graphics

VIDEO ON Led



SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE: DEBUG LEDS

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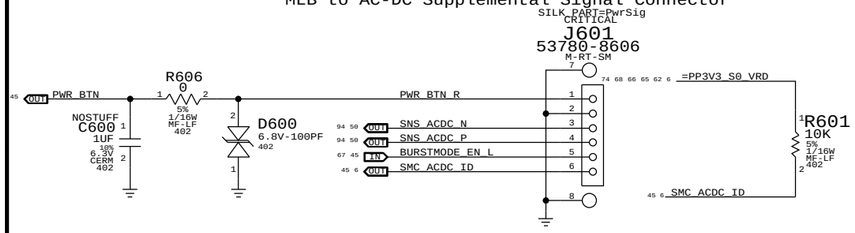
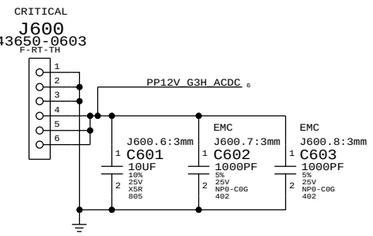
MLB to AC-DC Supplemental Signal Connector



MLB to AC-DC Connector



G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3
MAKE_BASE=TRUE
VOLTAGE=3.3V
NET_SPACING_TYPE=POWER
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=3MM
- PP3V3_G3H_RTC — 22 26
- =PP3V3_G3_PCH — 18 19

G3H Rails

PP12V_ACDC (97) MAKE_BASE=TRUE
- PP12V_G3H_ACDC — 6

PP12V_G3H (97) MAKE_BASE=TRUE
- PP12V_G3H_SNS — 48
- =PP12V_G3H_REG_3V42_G3H — 69
- =PP12V_G3H_FET_P12V_S5 — 69
- =PP12V_G3H_FET_P12V_S0 — 70

PP3V42_G3H (97) MAKE_BASE=TRUE
- PP3V42_G3H_REG — 69
- =PP3V3_G3H_BT — 33
- =PP3V3_G3H_SMC — 44 45
- =PP3V3_RTC_D — 26
- =PPVIN_G3H_SMCVREF — 45
- =PP3V3_G3H_SMC_USBMUX — 42

S5 Rails

Enabled when system has AC and is in S5

PP12V_S5 (97) MAKE_BASE=TRUE
- PP12V_S5_FET — 69
- =PP12V_S5_REG_P3V3P5V_S5 — 67
- =PP12V_S5_REG_VDDQ_S3 — 68
- =PP12V_S5_PWRCTL — 60 61 70
- =PPHV_SW_TBTAPWRSW — 84
- =PPHV_SW_TBTBPWRSW — 85
- =PP12V_S5_SNS — 48

PP5V_S5 (97) MAKE_BASE=TRUE
- PP5V_S5_LDO — 67
- =PP5V_S5_PWRCTL — 67 70
- =PP5V_S5_PCH — 24

PP3V3_S5 (97) MAKE_BASE=TRUE
- PP3V3_S5_REG — 67
- =PP3V3_S5_LDO_P1V05_S5 — 67
- =PP3V3_S5_FET_P3V3_S4 — 70
- =PP3V3_S5_FET_P3V3_S0 — 70
- =PP3V3_S5_PWRCTL — 60 61 70 78
- =PP3V3_S5_VRD — 67 68
- =PP3V3_S5_LED — 5
- =PP3V3_S5_LPCPLUS — 46
- =PP3V3_S5_PCH — 19 24 26
- =PP3V3_S5_PCH_STRAPS — 15
- =PP3V3_S5_PCH_VCC_DSW — 22 24
- =PP3V3_S5_PCH_VCC_SPI — 22 24
- =PP3V3_S5_PCH_VCCSUS_HDA — 22 24
- =PP3V3_S5_PCH_VCCSUS_USB — 22 24
- =PP3V3_S5_ROM — 46
- =PP3V3_S5_SENSE — 48
- =PP3V3_S5_SMC — 45
- =PP3V3_S5_USBMUX — 42 43
- =PP3V3_S5_XDP — 25

S4 Rails

Enabled when system has AC and is in run or sleep

PP5V_S4 (97) MAKE_BASE=TRUE
- PP5V_S4_REG — 67
- =PP5V_S4_REG_VDDQ_S3 — 68
- =PP5V_S4_FET_P5V_S0 — 70
- =PP5V_S4_MEMRESET — 28
- =PP5V_S4_PWRCTL — 70
- =PP5V_S4_USB — 42 43

PP3V3_S4 (97) MAKE_BASE=TRUE
- PP3V3_S4_FET — 70
- =PP3V3_S4_FET_ENET — 38
- =PP3V3_S4_PWRCTL — 70
- =PP3V3_S4_ALS — 40
- =PP3V3_S4_AP — 33
- =PP3V3_S4_LED — 5
- =PP3V3_S4_MEMRESET — 28
- =PP3V3_S4_PCH — 15
- =PP3V3_S4_PM — 28
- =PP3V3_S4_SDCARD — 15 39
- =PP3V3_S4_SMC — 45
- =PP3V3_S4_SMBUS_SMC_2 — 47
- =PP3V3_S4_TBT — 34 35 36 84 85
- =PP3V3_S4_TBTAPWRSW — 45 84
- =PP3V3_S4_TBTBPWRSW — 45 85
- =PP3V3_S4_USB_HUB — 27
- =PP3V3_S4_VREFMRGN — 32

S3 Rails

Enabled when system is in run or sleep

PP3V3_ENET (97) MAKE_BASE=TRUE
- PP3V3_ENET_FET — 38
- =PP3V3_ENET_PHY — 37 38
- =PP3V3_ENET_SYSCLK — 26
- =PPVDDIO_ENET_CLK — 26

PPVDDQ_S3 (95) MAKE_BASE=TRUE
- PPVDDQ_S3_REG — 68
- =PPVDDQ_S3_FET_VDDQ_S0 — 70
- =PPVDDQ_S3_LDO_DDRVTT — 68
- =PPVDDQ_S3_SNS_DDR_R — 49
- =PPVDDQ_S3_VSNS

PPVDDQ_S3_DDR (95) MAKE_BASE=TRUE
- PPVDDQ_S3_SNS_DDR — 49
- =PPVDDQ_S3_DDR_VREF — 32
- =PPVDDQ_S3_MEM_A — 29
- =PPVDDQ_S3_MEM_B — 30
- =PPVDDQ_S3_MEMRESET — 28

PPDDRVTT_S3 (95) MAKE_BASE=TRUE
- PPDDRVTT_S3_LDO — 68
- =PPDDRVTT_S3_VREFCA — 32

S0 Rails

Enabled when system is in run

PP12V_S0 (97) MAKE_BASE=TRUE
- PP12V_S0_FET — 70
- =PP12V_S0_REG_CPUCORE_S0 — 63
- =PP12V_S0_REG_VCCSA_S0 — 66
- =PP12V_S0_REG_P1V05_S0 — 65
- =PP12V_S0_SNS_GPUCORE_R — 48
- =PP12V_S0_SNS_GPUUNCORE_R — 48
- =PP12V_S0_AUDIO_SPKRAMP — 54 55
- =PP12V_S0_BKLT — 86
- =PP12V_S0_FAN — 51
- =PP12V_S0_LCD — 81

PP12V_S0_GPUCORE (97) MAKE_BASE=TRUE
- PP12V_S0_SNS_GPUCORE — 48
- =PP12V_S0_REG_GPUCORE_S0 — 80

PP12V_S0_GPUUNCORE (97) MAKE_BASE=TRUE
- PP12V_S0_SNS_GPUUNCORE — 48
- =PP12V_S0_REG_GPU_P1V05_S0 — 74
- =PP12V_S0_REG_GPU_VDDQ_S0 — 74

PPHDD_S0 (97) MAKE_BASE=TRUE
- PPHDD_S0_SNS — 48
- =PP5V_S0_SATA — 41

PP5V_S0 (97) MAKE_BASE=TRUE
- PP5V_S0_FET — 70
- =PP5V_S0_REG_CPUCORE_S0 — 62
- =PP5V_S0_REG_VCCSA_S0 — 66
- =PP5V_S0_REG_P1V05_S0 — 65
- =PP5V_S0_REG_GPU_P1V05_S0 — 74
- =PP5V_S0_REG_P1V8_S0 — 68
- =PP5V_S0_REG_GPUCORE_S0 — 80
- =PP5V_S0_REG_GPU_VDDQ_S0 — 74
- =PP5V_S0_VRD — 68
- =PP5V_S0_AUDIO — 52 59
- =PP5V_S0_CAMERA — 40
- =PP5V_S0_ISENSE — 48
- =PP5V_S0_LPCPLUS — 46
- =PP5V_S0_PCH — 24
- =PP5V_S0_BKLT — 86
- =PPHDD_S0_SNS_R — 48

PP3V3_S0 (97) MAKE_BASE=TRUE
- PP3V3_S0_FET — 70
- =PP3V3_S0_P3V3TBTFET — 36
- =PP3V3_S0_PWRCTL — 70 80
- =PP3V3_S0_VRD — 6 62 65 66 68 74
- =PP3V3_S0_AUDIO — 40 52 54 55 58
- =PP3V3_S0_AUDIO_DIG — 56
- =PP3V3_S0_BT — 33
- =PP3V3_S0_CAMERA — 40
- =PP3V3_S0_DP — 47 81 83
- =PP3V3_S0_ENET — 37
- =PP3V3_S0_FAN — 51
- =PP3V3_S0_INTDPMUX — 82
- =PP3V3_S0_LED — 5
- =PP3V3_S0_LED_SATA — 15 41
- =PP3V3_S0_PCH — 18 21 24
- =PP3V3_S0_PCH_GPIO — 15 19 20 36
- =PP3V3_S0_PCH_PM — 26
- =PP3V3_S0_PCH_STRAPS — 15
- =PP3V3_S0_PCH_VCC — 22 24
- =PP3V3_S0_PCH_VCC_ADAC — 17
- =PP3V3_S0_PCH_VCC_GPIO — 22 24
- =PP3V3_S0_PCH_VCC_HVCMOS — 22 24
- =PP3V3_S0_PCH_VCC_PCI — 22 24
- =PP3V3_S0_RSTBUF — 26
- =PP3V3_S0_SDCARD — 39
- =PP3V3_S0_SENSE — 41 48 49 50
- =PP3V3_S0_SMBUS — 47
- =PP3V3_S0_SMBUS_SMC_0 — 47
- =PP3V3_S0_SMBUS_SMC_1 — 47
- =PP3V3_S0_SMBUS_SMC_3 — 47
- =PP3V3_S0_SMC — 45
- =PP3V3_S0_TBTPWRCTL — 36
- =PP3V3_S0_BKLT_VDDIO — 86
- =PP3V3_GPU_IFPX_PLLVDD — 77
- =PP3V3_GPU_MISC — 77 80
- =PP3V3_GPU_VDD33 — 71 77 78 79
- =PPSPD_S0_MEM_A — 29
- =PPSPD_S0_MEM_B — 30

PP3V3_S0_SSD (97) MAKE_BASE=TRUE
- PP3V3_S0_SSD_FET — 70
- =PPSSD_S0_SNS_R — 49

PPSSD_S0 (97) MAKE_BASE=TRUE
- PPSSD_S0_SNS — 49
- =PP3V3_S0_SSD — 41
- =PP3V3_S0_SATAMUX — 41

PP1V8_S0 (97) MAKE_BASE=TRUE
- PP1V8_S0_REG — 68
- =PP1V8_S0_CAMERA — 40
- =PP1V8_S0_CPU_PLL — 13 16
- =PP1V8_S0_PCH — 19
- =PP1V8_S0_PCH_VCC_DFTERM — 22 24
- =PP1V8_S0_PCH_VCC_VRM — 24
- =PPVDDIO_S0_SBCLK — 26
- =PP1V8_S0_GPUVID — 80
- =PP1V8_S0_ENET — 38

PP1V5_S0 (95) MAKE_BASE=TRUE
- PP1V5_S0_FET — 70
- =PP1V5_S0_CPU_MEM — 11 13 16
- =PP1V5_S0_AUD_DIG — 52
- =PP1V5_S0_SENSE — 41

PPDDRVTT_S0 (95) MAKE_BASE=TRUE
- PPDDRVTT_S0_LDO — 68
- =PPDDRVTT_S0_CLAMP — 28
- =PPDDRVTT_S0_MEM_A — 29
- =PPDDRVTT_S0_MEM_B — 30

PPDDRVREF_DQ_MEM_A_S3 (97) MAKE_BASE=TRUE
- PPDDRVREF_DQ_MEM_A — 32
- =PPDDRVREF_DQ_MEM_A — 29

PPDDRVREF_CA_MEM_A_S3 (97) MAKE_BASE=TRUE
- PPDDRVREF_CA_MEM_A — 32
- =PPDDRVREF_CA_MEM_A — 29

PPDDRVREF_DQ_MEM_B_S3 (97) MAKE_BASE=TRUE
- PPDDRVREF_DQ_MEM_B — 32
- =PPDDRVREF_DQ_MEM_B — 30

PPDDRVREF_CA_MEM_B_S3 (97) MAKE_BASE=TRUE
- PPDDRVREF_CA_MEM_B — 32
- =PPDDRVREF_CA_MEM_B — 30

PP1V05_S0 (95) MAKE_BASE=TRUE
- PP1V05_S0_REG — 65
- =PP1V05_S0_DP
- =PP1V05_S0_P1V05TBTFET — 36
- =PP1V05_S0_PCH — 18 24
- =PP1V05_S0_PCH_VCC_ADPLL — 17
- =PP1V05_S0_PCH_VCC_ASW — 22 24
- =PP1V05_S0_PCH_VCC_CORE — 22 24
- =PP1V05_S0_PCH_VCC_DMI — 22 24
- =PP1V05_S0_PCH_VCC_DIFFCLK — 22
- =PP1V05_S0_PCH_VCC_SSC — 22
- =PP1V05_S0_PCH_VCCIO_DMI — 22
- =PP1V05_S0_PCH_VCCIO_PCIE — 18 19 22
- =PP1V05_S0_PCH_VCCIO_SATA — 18 22 24
- =PP1V05_S0_PCH_VCCIO_USB — 22
- =PP1V05_S0_PCH_V_PROC_IO — 22 24
- =PPVCCIO_S0_CPU — 10 11 13 16 62
- =PPVCCIO_S0_SMC — 45
- =PPVCCIO_S0_XDP — 25

PPVCORE_S0_CPU (96) MAKE_BASE=TRUE
- PPCPUCORE_S0_REG — 63
- =PPVCORE_S0_CPU — 13 16 48 62

PPVAXG_S0 (96) MAKE_BASE=TRUE
- PPCPUAXG_S0_REG — 64
- =PPVAXG_S0_CPU — 13 17 48 62

PPVCCSA_S0 (95) MAKE_BASE=TRUE
- PPVCCSA_S0_REG — 66
- =PPVCCSA_S0_CPU — 13 16

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

PP3V3_TBTLC (97) MAKE_BASE=TRUE
- =PP3V3_TBTLC_FET — 36
- =PP3V3_TBT_PCH_GPIO — 15
- =PP3V3_TBTLC_RTR — 34 35 36
- =PPVDDIO_TBT_CLK — 26

PP1V05_TBTLC (95) MAKE_BASE=TRUE
- =PP1V05_TBTLC_FET — 36
- =PP1V05_TBTLC_RTR — 35 36

PP1V05_TBTCIO (95) MAKE_BASE=TRUE
- =PP1V05_TBTCIO_FET — 36
- =PP1V05_TBTCIO_RTR — 35

GPU Rails (S0)

Enabled when system is in run

PPVCORE_S0_GPU (97) MAKE_BASE=TRUE
- PPGPUCORE_S0_REG — 80
- =PPVCORE_GPU — 72 79

PP1V05_S0_GPU (97) MAKE_BASE=TRUE
- PP1V05_S0_GPU_REG — 74
- =PP1V05_GPU_IFPCD_IOVDD — 77
- =PP1V05_GPU_IFPEF_IOVDD — 77
- =PP1V05_GPU_PEX_IOVDD — 73 79
- =PP1V05_GPU_PEX_PLLVDD — 77 79

PPVDDQ_S0_GPU (97) MAKE_BASE=TRUE
- PP1V5R1V35_S0_GPU_REG — 74
- =PP1V35_GPU_FBVDDQ — 72 75 76
- =PP1V35_GPU_S0_FB — 73

Ground/Common

GND
MAKE_BASE=TRUE

SYNC_MASTER=D7 NICK — SYNC_DATE=01/11/2012

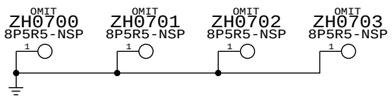
PAGE TITLE
Power Connectors/Aliases

Apple Inc.

DRAWING NUMBER 051-9509 — SIZE D
REVISION 4.2.0
BRANCH
PAGE 6 OF 113
SHEET 6 OF 100

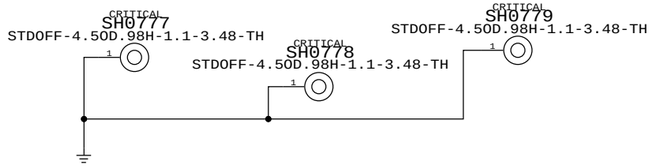
CPU Heatsink

4mm Plated Holes (998-0850)



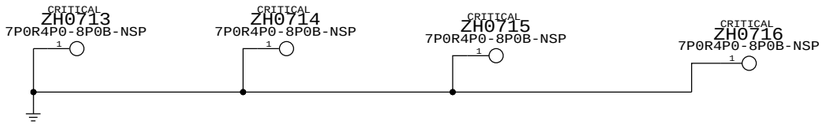
GPU HEATSINK MOUNTING FEATURES

(860-0988)



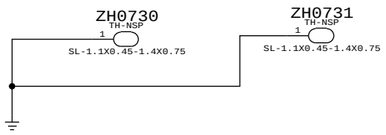
Rear Cover

998-4559 (Plated holes, 4mm inner diameter, 8mm pad)



USB Can holes

998-3975 (Plated slot holes, 1.10mm x 0.45mm)



WIRELESS CARD MTG HOLES

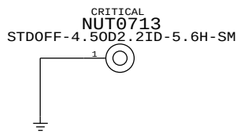
998-4560 (Plated holes, 2.3mm inner diameter, 4.3mm pad)

POGO PINS

APN: 870-1939

SSD STANDOFF

APN: 860-1461



SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE: Holes/PD parts

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

REVISION: 4.2.0

BRANCH:

PAGE: 7 OF 113

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CPU Reserved

10	TP_CPU_RSVD<16..1>	NC_CPU_RSVD<16..1>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_RSVD<46..19>	NC_CPU_RSVD<46..19>	MAKE_BASE=TRUE NO_TEST=TRUE
91 10	CPU_CFG<15..12>	TP_CPU_CFG<15..12>	MAKE_BASE=TRUE

CPU Memory

12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_A_CLK_N<2..3>	NC_MEM_A_CLKN<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_A_CLK_P<2..3>	NC_MEM_A_CLKP<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_A_CS_L<2..3>	NC_MEM_A_CS_L<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_A_CKE<2..3>	NC_MEM_A_CKE<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_B_CLK_N<2..3>	NC_MEM_B_CLKN<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_B_CLK_P<2..3>	NC_MEM_B_CLKP<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_B_CS_L<2..3>	NC_MEM_B_CS_L<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_B_CKE<2..3>	NC_MEM_B_CKE<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_A_ODT<2..3>	NC_MEM_A_ODT<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_B_ODT<2..3>	NC_MEM_B_ODT<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH USB

20	USB_PCH_4_N	NC_USB_PCH_4_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_4_P	NC_USB_PCH_4_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_N	NC_USB_PCH_5_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_P	NC_USB_PCH_5_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_N	NC_USB_PCH_6_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_P	NC_USB_PCH_6_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_N	NC_USB_PCH_11_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_P	NC_USB_PCH_11_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_N	NC_USB_PCH_12_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_P	NC_USB_PCH_12_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_N	NC_USB_PCH_13_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_P	NC_USB_PCH_13_P	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PLL

22	PP1V05_S0_PCH_VCCAPLLDMI2	NC_PP1V05_S0_PCH_VCCAPLLDMI2	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_VCCAPLL_EXP	NC_PP1V05_S0_PCH_VCCAPLL_EXP	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_VCCAPLL_SATA	NC_PP1V05_S0_PCH_VCCAPLL_SATA	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

18	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7P	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_N<3..0>	NC_PE_TXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_P<3..0>	NC_PE_TXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_N<3..0>	NC_PE_RXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_P<3..0>	NC_PE_RXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_N	NC_DMI_MIDBUS_CLK100N	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_P	NC_DMI_MIDBUS_CLK100P	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_CLKOUT_PEG_A_N	NC_CLKOUT_PEG_AN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_CLKOUT_PEG_A_P	NC_CLKOUT_PEG_AP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPP	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCH_CLK25M_XTALOUT	NC_PCH_CLK25M_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3	MAKE_BASE=TRUE NO_TEST=TRUE

PCH and CPU FDI

91 10	CPU_FDI_TX_N<7..0>	NC_CPU_FDI_TXN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
91 10	CPU_FDI_TX_P<7..0>	NC_CPU_FDI_TXP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_RX_N<7..0>	NC_PCH_FDI_RXN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_RX_P<7..0>	NC_PCH_FDI_RXP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
91 10	CPU_FDI_FSYNC<1..0>	NC_CPU_FDI_FSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
91 10	CPU_FDI_LSYNC<1..0>	NC_CPU_FDI_LSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
91 10	CPU_FDI_INT	NC_CPU_FDI_INT	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_FSYNC<1..0>	NC_PCH_FDI_FSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_LSYNC<1..0>	NC_PCH_FDI_LSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_INT	NC_PCH_FDI_INT	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Unused Display

19	TP_CRT_IG_RED	NC_CRT_IG_RED	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_AUX_N	NC_DP_IG_B_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_AUX_P	NC_DP_IG_B_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_HPD	NC_DP_IG_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_DDC_CLK	NC_DP_IG_B_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_DDC_DATA	NC_DP_IG_B_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_AUX_N	NC_DP_IG_C_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_AUX_P	NC_DP_IG_C_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_HPD	NC_DP_IG_C_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_CTRL_CLK	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_CTRL_DATA	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_AUXN	NC_DP_IG_D_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_AUXP	NC_DP_IG_D_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_HPD	NC_DP_IG_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_CTRL_CLK	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_CTRL_DATA	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLN	NC_SDVO_STALLN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLP	NC_SDVO_STALLP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTN	NC_SDVO_INTN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTP	NC_SDVO_INTP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTCTL	NC_PCH_L_BKLTCTL	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTEN	NC_PCH_L_BKLTEN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_VDD_EN	NC_PCH_L_VDD_EN	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED GRAPHICS ALIASES

	TP_DVPCNTL_M<0..1>	NC_DVPCNTL_M<0..1>	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_DVPCNTL<0..2>	NC_DVPCNTL<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_DVPCLK	NC_DVPCLK	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_DVPDATA<4..23>	NC_DVPDATA<4..23>	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_CLK_C_P	NC_HDMI_EG_CLK_C_P	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_CLK_C_N	NC_HDMI_EG_CLK_C_N	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_DDC_CLK	NC_HDMI_EG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_DDC_DATA	NC_HDMI_EG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_DATA_C_P<0..2>	NC_HDMI_EG_DATA_C_P<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_DATA_C_N<0..2>	NC_HDMI_EG_DATA_C_N<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
77	GPU_TDIODE_P	NC_GPU_TDIODE_P	MAKE_BASE=TRUE NO_TEST=TRUE
77	GPU_TDIODE_N	NC_GPU_TDIODE_N	MAKE_BASE=TRUE NO_TEST=TRUE
78	EG_LCD_PWR_EN	NC_EG_LCD_PWR_EN	MAKE_BASE=TRUE NO_TEST=TRUE

PCH SATA

18	TP_SATA_C_R2D_CN	NC_SATA_C_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_R2D_CP	NC_SATA_C_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RN	NC_SATA_C_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RP	NC_SATA_C_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RN	NC_SATA_D_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RP	NC_SATA_D_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RN	NC_SATA_E_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RP	NC_SATA_E_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RN	NC_SATA_F_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RP	NC_SATA_F_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Reserved

19	TP_PCH_RESERVE_0	NC_PCH_RESERVE_0	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_1	NC_PCH_RESERVE_1	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_2	NC_PCH_RESERVE_2	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_3	NC_PCH_RESERVE_3	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_4	NC_PCH_RESERVE_4	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_5	NC_PCH_RESERVE_5	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_6	NC_PCH_RESERVE_6	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_7	NC_PCH_RESERVE_7	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_8	NC_PCH_RESERVE_8	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_9	NC_PCH_RESERVE_9	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_10	NC_PCH_RESERVE_10	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_11	NC_PCH_RESERVE_11	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_12	NC_PCH_RESERVE_12	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_13	NC_PCH_RESERVE_13	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_14	NC_PCH_RESERVE_14	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_15	NC_PCH_RESERVE_15	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_16	NC_PCH_RESERVE_16	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_17	NC_PCH_RESERVE_17	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_18	NC_PCH_RESERVE_18	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_19	NC_PCH_RESERVE_19	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_20	NC_PCH_RESERVE_20	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_21	NC_PCH_RESERVE_21	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_22	NC_PCH_RESERVE_22	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_23	NC_PCH_RESERVE_23	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_24	NC_PCH_RESERVE_24	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_25	NC_PCH_RESERVE_25	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_26	NC_PCH_RESERVE_26	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_27	NC_PCH_RESERVE_27	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_28	NC_PCH_RESERVE_28	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Test Points

21	TP_PCH_TP1	NC_PCH_TP1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP2	NC_PCH_TP2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP3	NC_PCH_TP3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP4	NC_PCH_TP4	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP5	NC_PCH_TP5	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP6	NC_PCH_TP6	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP7	NC_PCH_TP7	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP8	NC_PCH_TP8	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP9	NC_PCH_TP9	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP10	NC_PCH_TP10	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP11	NC_PCH_TP11	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP12	NC_PCH_TP12	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP13	NC_PCH_TP13	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP14	NC_PCH_TP14	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP15	NC_PCH_TP15	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP16	NC_PCH_TP16	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP17	NC_PCH_TP17	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP18	NC_PCH_TP18	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP19	NC_PCH_TP19	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP20	NC_PCH_TP20	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_RESET_L	NC_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_INIT3V3_L	NC_PCH_INIT3V3_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

18	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM0	NC_PCH_PWM0	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM1	NC_PCH_PWM1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM2	NC_PCH_PWM2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM3	NC_PCH_PWM3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_SST	NC_PCH_SST	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_CLK1	NC_PCH_CL_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_DATA1	NC_PCH_CL_DATA1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_RST1	NC_PCH_CL_RST1	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT2	NC_PCI_CLK33M_OUT2	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT3	NC_PCI_CLK33M_OUT3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_GPIO8	NC_PCH_GPIO8	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_FDIPLL	NC_PP1V05_S0_PCH_FDIPLL	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_VCC_A_CLK	NC_PP1V05_S0_PCH_VCC_A_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
22	TP_PPVOUT_PCH_DCPSUSBYP	NC_PPVOUT_PCH_DCPSUSBYP	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE

Unused Signal Aliases

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

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BRANCH

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Whistler aliases

89 71 PEG_D2R_N<0..15> ═══ =PEG_D2R_N<15..0> 10
MAKE_BASE=TRUE

89 71 PEG_D2R_P<0..15> ═══ =PEG_D2R_P<15..0> 10
MAKE_BASE=TRUE

89 71 PEG_R2D_C_N<0..15> ═══ =PEG_R2D_C_N<15..0> 10
MAKE_BASE=TRUE

89 71 PEG_R2D_C_P<0..15> ═══ =PEG_R2D_C_P<15..0> 10
MAKE_BASE=TRUE

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE
Signal Aliases

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D
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SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R1010.1
ROUTE B5 TO R1010.1 AS A SEPERATE 10 MIL TRACE.

OMIT TABLE
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IVY-BRIDGE
BGA-SKT-K70
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DMI
DMI_RX_0* W4
DMI_RX_1* V4
DMI_RX_2* Y4
DMI_RX_3* AA5
DMI_RX_0 W5
DMI_RX_1 V3
DMI_RX_2 Y3
DMI_RX_3 AA4
DMI_TX_0* V6
DMI_TX_1* W8
DMI_TX_2* Y7
DMI_TX_3* AA8
DMI_TX_0 V7
DMI_TX_1 W7
DMI_TX_2 Y6
DMI_TX_3 AA7

DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
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DMI_S2N_P<2>
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DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>

FLEXIBLE DISPLAY INTERFACE (Unused)
FDI_TX_0* AC7
FDI_TX_1* AC3
FDI_TX_2* AD1
FDI_TX_3* AD3
FDI_TX_4* AD6
FDI_TX_5* AE8
FDI_TX_6* AF2
FDI_TX_7* AG1
FDI_TX_0 AC8
FDI_TX_1 AC2
FDI_TX_2 AD2
FDI_TX_3 AD4
FDI_TX_4 AD7
FDI_TX_5 AE7
FDI_TX_6 AF3
FDI_TX_7 AG2
FDI_FSYNC_0 AC5
FDI_FSYNC_1 AE5
FDI_INT AG3
FDI_LSYNC_0 AC4
FDI_LSYNC_1 AE4
FDI_COMPIO AE2
FDI_ICOMPO AE1

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CPU_FDI_TX_P<7>
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CPU_FDI_LSYNC<0>
CPU_FDI_LSYNC<1>
CPU_FDI_COMPIO

=PPVCCIO_S0_CPU
R1011 24.9 1% 1/10W MF-LF 402

PCI EXPRESS -- GRAPHICS (Available for Workstation only)
PCI EXPRESS
PE_RX_0* P4
PE_RX_1* R1
PE_RX_2* T3
PE_RX_3* U1
PE_RX_0 P3
PE_RX_1 R2
PE_RX_2 T4
PE_RX_3 U2
PE_TX_0* P7
PE_TX_1* T8
PE_TX_2* R5
PE_TX_3* U6
PE_TX_0 P8
PE_TX_1 T7
PE_TX_2 R6
PE_TX_3 U5

TP_PE_RX_N<0>
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TP_PE_RX_N<3>
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TP_PE_RX_P<1>
TP_PE_RX_P<2>
TP_PE_RX_P<3>
TP_PE_TX_N<0>
TP_PE_TX_N<1>
TP_PE_TX_N<2>
TP_PE_TX_N<3>
TP_PE_TX_P<0>
TP_PE_TX_P<1>
TP_PE_TX_P<2>
TP_PE_TX_P<3>

PEG_COMPI B4
PEG_ICOMPO B5
PEG_RCOMPO C4
CPU_PEG_COMP

PLACE_NEAR=U1000.B4:12.7mm
R1010 24.9 1% 1/10W MF-LF 402
=PPVCCIO_S0_CPU

PEG_RX_0* B12
PEG_RX_1* D11
PEG_RX_2* C9
PEG_RX_3* E9
PEG_RX_4* B7
PEG_RX_5* C5
PEG_RX_6* A6
PEG_RX_7* E1
PEG_RX_8* F3
PEG_RX_9* G1
PEG_RX_10* H4
PEG_RX_11* J2
PEG_RX_12* K4
PEG_RX_13* L2
PEG_RX_14* M4
PEG_RX_15* N2
PEG_RX_0 B11
PEG_RX_1 D12
PEG_RX_2 C10
PEG_RX_3 E10
PEG_RX_4 B8
PEG_RX_5 C6
PEG_RX_6 A5
PEG_RX_7 E2
PEG_RX_8 F4
PEG_RX_9 G2
PEG_RX_10 H3
PEG_RX_11 J1
PEG_RX_12 K3
PEG_RX_13 L1
PEG_RX_14 M3
PEG_RX_15 N1
PEG_TX_0* C14
PEG_TX_1* E13
PEG_TX_2* G13
PEG_TX_3* F11
PEG_TX_4* J13
PEG_TX_5* D7
PEG_TX_6* C3
PEG_TX_7* E5
PEG_TX_8* F7
PEG_TX_9* G9
PEG_TX_10* G6
PEG_TX_11* K8
PEG_TX_12* J6
PEG_TX_13* M7
PEG_TX_14* L5
PEG_TX_15* N6
PEG_TX_0 C13
PEG_TX_1 E14
PEG_TX_2 G14
PEG_TX_3 F12
PEG_TX_4 J14
PEG_TX_5 D8
PEG_TX_6 D3
PEG_TX_7 E6
PEG_TX_8 F8
PEG_TX_9 G10
PEG_TX_10 G5
PEG_TX_11 K7
PEG_TX_12 J5
PEG_TX_13 M8
PEG_TX_14 L6
PEG_TX_15 N5

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OMIT TABLE
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RESERVED
RSVD_C38 C38
RSVD_C39 C39
RSVD_D38 D38
RSVD_H7 H7
RSVD_H8 H8
RSVD_J9 J9
RSVD_J31 J31
RSVD_J33 J33
RSVD_J34 J34
RSVD_K9 K9
RSVD_K31 K31
RSVD_K34 K34
RSVD_L9 L9
RSVD_L31 L31
RSVD_L33 L33
RSVD_L34 L34
RSVD_M34 M34 ThermDC
RSVD_N33 N33 ThermDA
RSVD_N34 N34
RSVD_P35 P35
RSVD_P37 P37
RSVD_P39 P39
RSVD_R34 R34
RSVD_R36 R36
RSVD_R38 R38
RSVD_R40 R40
RSVD_AB6 AB6
RSVD_AB7 AB7
RSVD_AD34 AD34
RSVD_AD35 AD35
RSVD_AD37 AD37
RSVD_AE6 AE6
RSVD_AF4 AF4
RSVD_AG4 AG4
RSVD_AJ11 AJ11
RSVD_AJ29 AJ29
RSVD_AJ30 AJ30
RSVD_AJ31 AJ31
RSVD_AN20 AN20
RSVD_AP20 AP20
RSVD_AT11 AT11
RSVD_AT14 AT14
RSVD_AU10 AU10
RSVD_AV34 AV34
RSVD_AW34 AW34
RSVD_AY10 AY10
RSVD_NCTF_AV1 AV1
RSVD_NCTF_AW2 AW2
RSVD_NCTF_AY3 AY3
RSVD_NCTF_B39 B39
NCTF_A38 A38
NCTF_C2 C2
NCTF_D1 D1
NCTF_AU40 AU40
NCTF_AW38 AW38

TP_CPU_RSVD<1>
TP_CPU_RSVD<2>
TP_CPU_RSVD<3>
TP_CPU_RSVD<4>
TP_CPU_RSVD<5>
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TP_CPU_RSVD<10>
TP_CPU_RSVD<11>
TP_CPU_RSVD<12>
TP_CPU_RSVD<13>
TP_CPU_RSVD<14>
TP_CPU_RSVD<15>
TP_CPU_RSVD<16>
NC_SNS_CPU_THERMDN
NO_TESTPOINT
NC_SNS_CPU_THERMDP
NO_TESTPOINT
TP_CPU_RSVD<19>
TP_CPU_RSVD<20>
TP_CPU_RSVD<21>
TP_CPU_RSVD<22>
TP_CPU_RSVD<23>
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TP_CPU_RSVD<46>
TP_CPU_RSVD_NCTF<1>
TP_CPU_RSVD_NCTF<2>
TP_CPU_RSVD_NCTF<3>
TP_CPU_RSVD_NCTF<4>
TP_CPU_NCTF<1>
TP_CPU_NCTF<2>
TP_CPU_NCTF<3>
TP_CPU_NCTF<4>
TP_CPU_NCTF<5>

INTEL SUGGESTS TO KEEP THESE TPS

CPU_CFG<0> H36 CFG_0
CPU_CFG<1> J36 CFG_1
CPU_CFG<2> J37 CFG_2
CPU_CFG<3> K36 CFG_3
CPU_CFG<4> L36 CFG_4
CPU_CFG<5> N35 CFG_5
CPU_CFG<6> L37 CFG_6
CPU_CFG<7> M36 CFG_7
CPU_CFG<8> J38 CFG_8
CPU_CFG<9> L35 CFG_9
CPU_CFG<10> M38 CFG_10
CPU_CFG<11> N36 CFG_11
CPU_CFG<12> N38 CFG_12
CPU_CFG<13> N39 CFG_13
CPU_CFG<14> N37 CFG_14
CPU_CFG<15> N40 CFG_15
CPU_CFG<16> G37 CFG_16
CPU_CFG<17> G36 CFG_17

CFG[1:0] Reserved config lane
CFG[2] PCIe Static x16 lane reversal; Refer to page 15 for more info
CFG[3] PCIe Static x4 lane reversal; Refer to page 15 for more info
CFG[4] Reserved config lane
CFG[6:5] PCIe bifurcation; Refer to page 15 for more info
CFG[17:7] Reserved config lanes

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011
PAGE TITLE
CPU DMI/PEG/FDI/RSVD
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BASED ON INTEL MOBILE SOLUTION

62 16 13 11 10 6 =PPVCCIO_S0_CPU

PLACE_NEAR=U1000.F36:50mm
R1124 1
75
5%
1/16W
MF-LF
402 2

20 IN CPU_RESET_L

R1125
43
2 1
5%
1/16W
MF-LF
402

62 16 13 11 10 6 =PPVCCIO_S0_CPU

R1101 1
51
5%
1/16W
MF-LF
402 2

60 OUT CPU_SKTOCC_L
19 OUT CPU_PROC_SEL
45 OUT CPU_CATERR_L
45 44 21 IO CPU_PECI
62 45 44 IO CPU_PROCHOT_L
45 OUT CPU_THRMTRIP_L

R1102
0
2 1
1/16W
MF-LF
5% 402
CPU_PROCHOT_R_L

PLT_RESET_LS1V05_L
19 IN PM_SYNC
25 21 IN CPU_PWRGD

16 13 11 6 =PP1V5_S0_CPU_MEM

R1120 1
200
1%
1/16W
MF-LF
402 2

FROM PCH
28 19 IN PM_MEM_PWRGD

R1121
130
2 1
1%
1/16W
MF-LF
402

PM_MEM_PWRGD_R
28 OUT CPU_MEM_RESET_L
97 11 CPU_DDR_VREF
97 32 OUT CPU_DIMM_VREF_DAC_B
97 32 OUT CPU_DIMM_VREF_DAC_A

OMIT_TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 2 OF 10

AJ33	SKTOCC*		
K32	PROC_SEL		
E37	CATERR*	THERMAL	CLOCKS
J35	PECI		
H34	PROCHOT*		
G35	THERMTRIP*		
F36	RESET*	PWR MGMT	JTAG & BPM
E38	PM_SYNC		
J40	UNCOREPWRGOOD		
AJ19	SM_DRAMPWROK	DDR3 MISC	
AW18	SM_DRAMRST*		
AJ22	SM_VREF		
AH1	SB_DIMM_VREFDQ		
AH4	SA_DIMM_VREFDQ		

BCLK_ITP	C40	IN	ITPCPU_CLK100M_P
BCLK_ITP*	D40	IN	ITPCPU_CLK100M_N
BCLK_0	W2	IN	DMI_CLK100M_CPU_P
BCLK_0*	W1	IN	DMI_CLK100M_CPU_N
PRDY*	K38	OUT	XDP_CPU_PRDY_L
PREQ*	K40	IN	XDP_CPU_PREQ_L
TCK	M40	IN	XDP_CPU_TCK
TMS	L38	IN	XDP_CPU_TMS
TRST*	J39	IN	XDP_CPU_TRST_L
TDI	L40	IN	XDP_CPU_TDI
TDO	L39	OUT	XDP_CPU_TDO
DBR*	E39	OUT	XDP_DBRESET_L
BPM[0]*	H40	BI	XDP_BPM_L<0>
BPM[1]*	H38	BI	XDP_BPM_L<1>
BPM[2]*	G38	BI	XDP_BPM_L<2>
BPM[3]*	G40	BI	XDP_BPM_L<3>
BPM[4]*	G39	BI	XDP_BPM_L<4>
BPM[5]*	F38	BI	XDP_BPM_L<5>
BPM[6]*	E40	BI	XDP_BPM_L<6>
BPM[7]*	F40	BI	XDP_BPM_L<7>

R1111
1K
5%
1/16W
MF-LF
2 402

16 13 11 6 =PP1V5_S0_CPU_MEM

R1140
1K
1%
1/16W
MF-LF
2 402

CPU_DDR_VREF 11 97

R1141
1K
1%
1/16W
MF-LF
2 402

C1140
0.1UF
10%
16V
X7R-CERM
2 402

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

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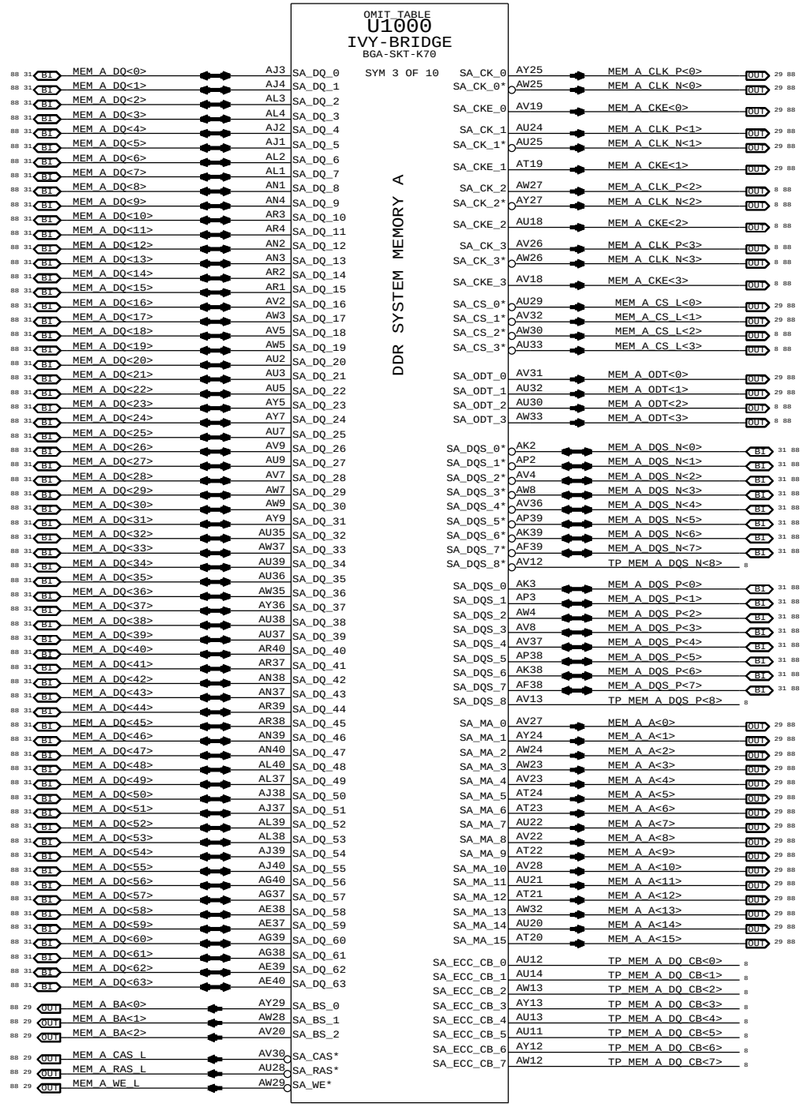

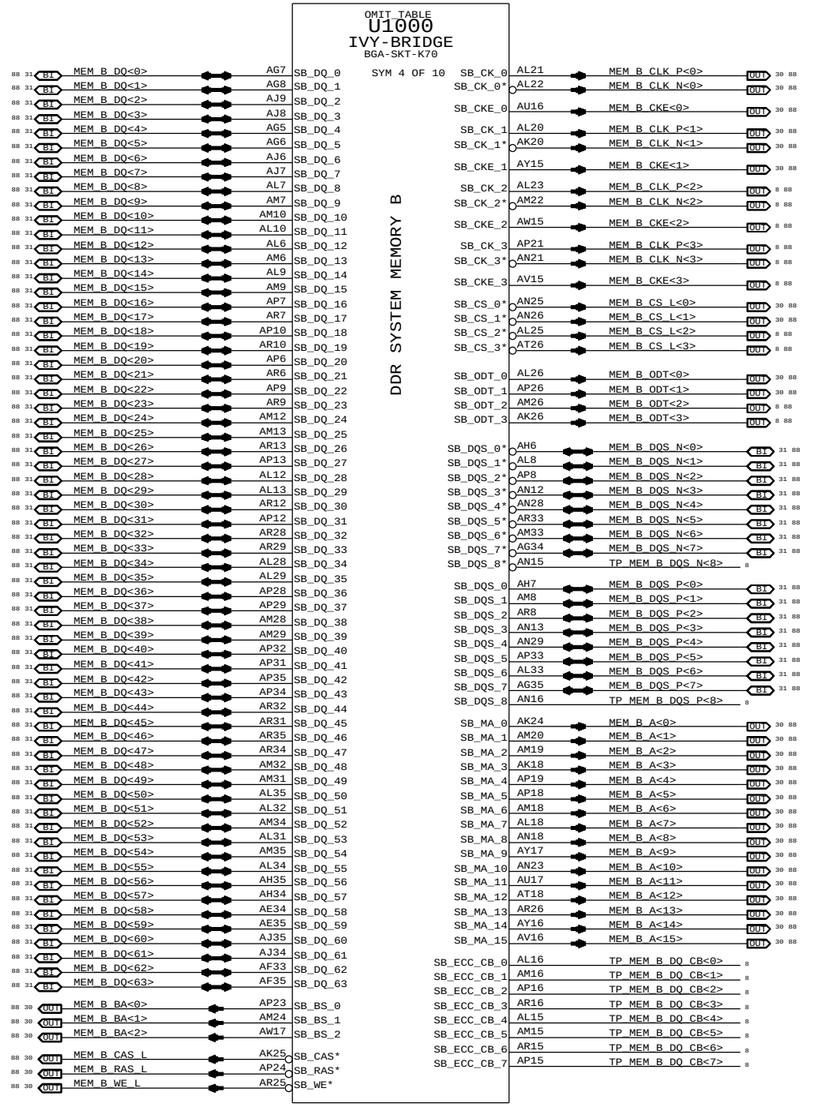

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

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BRANCH

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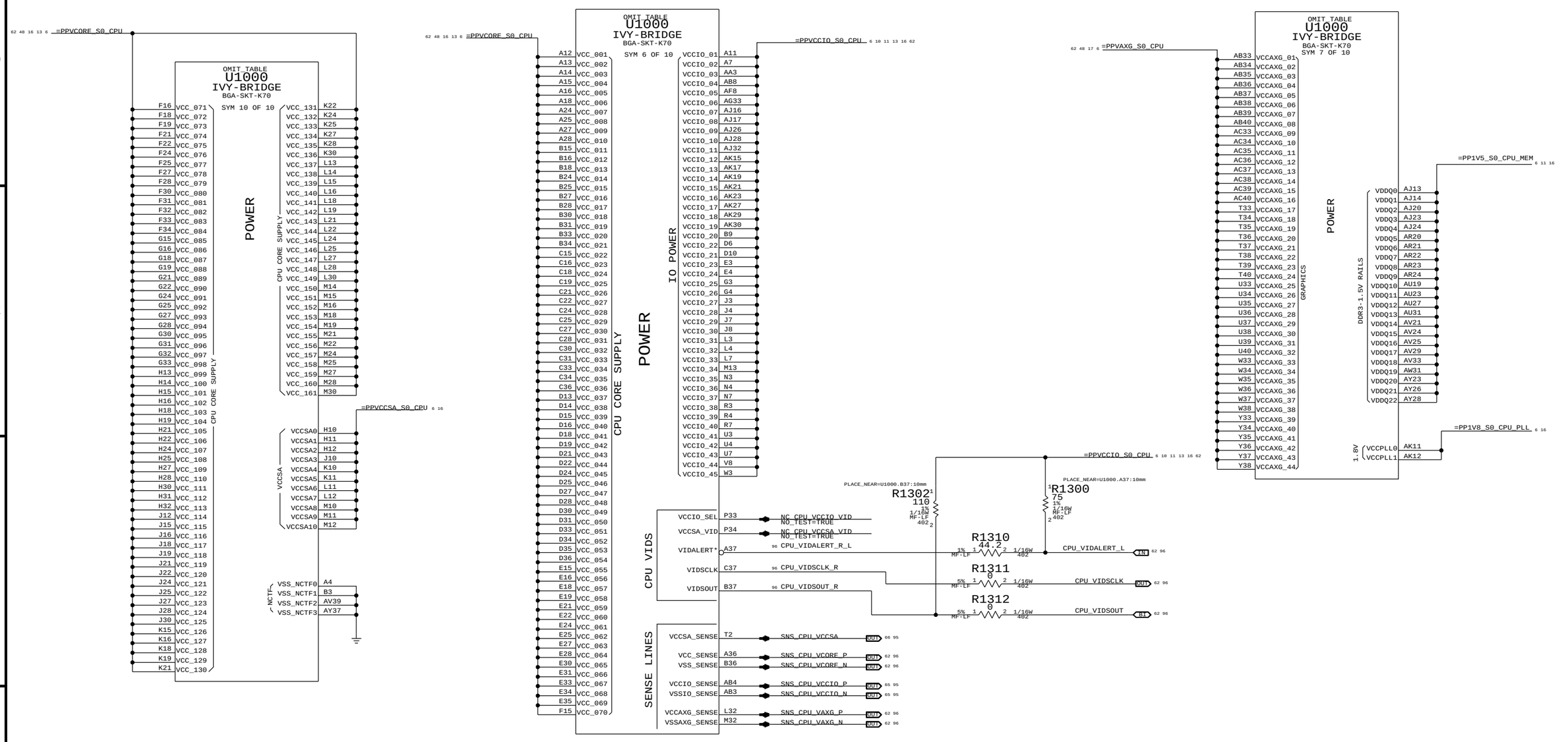

SYNC_MASTER=K70_MLB	SYNC_DATE=11/30/2011
PAGE TITLE	CPU POWER
Apple Inc.	DRAWING NUMBER 051-9509 SIZE D
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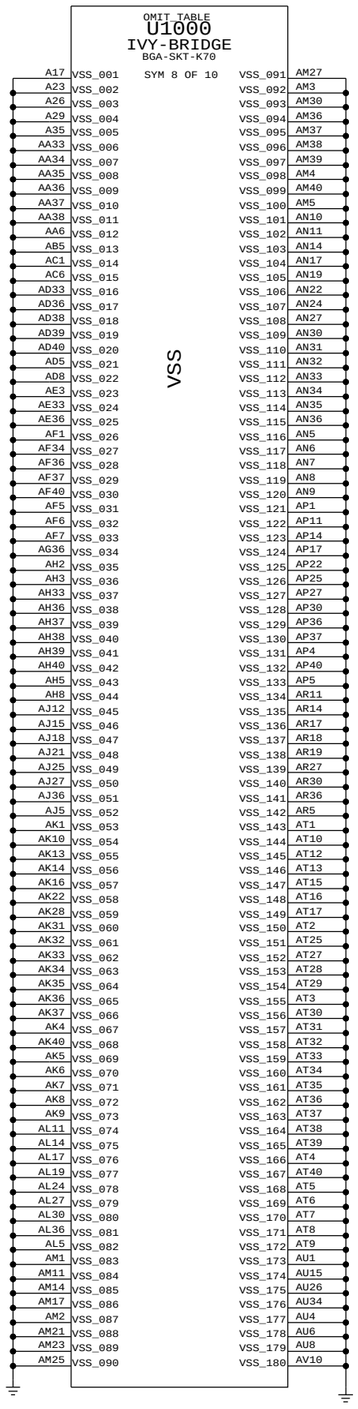

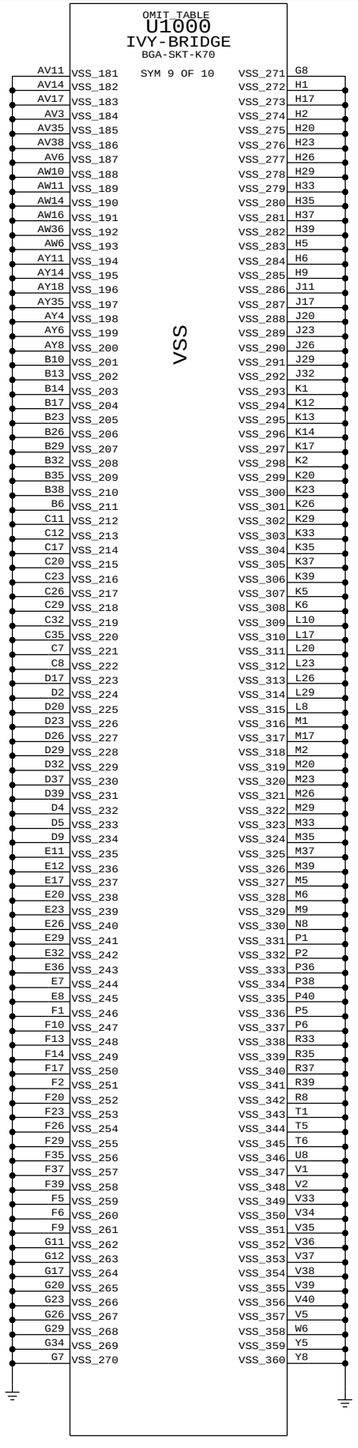

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE

CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

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=PP3V3_S5_PCH_STRAPS
10K 5% 1/16W MF-LF 402 R1501 — SMC_WAKE_SCI_L
10K 5% 1/16W MF-LF 402 R1502 — TBT_GO2SX_BIDIR
10K 5% 1/16W MF-LF 402 R1504 — PCH_SUSWARN_L
10K 5% 1/16W MF-LF 402 R1563 — PCH_GPIO72
1K 5% 1/16W MF-LF 402 R1564 — PM_PWRBTN_L
10K 5% 1/16W MF-LF 402 R1590 — PCH_SMBALERT_L

=PP3V3_S5_PCH_STRAPS
10K 5% 1/16W MF-LF 402 R1519 — USB_EXTA_OC_L
10K 5% 1/16W MF-LF 402 R1518 — USB_EXTB_OC_L
10K 5% 1/16W MF-LF 402 R1517 — USB_EXTC_OC_L
10K 5% 1/16W MF-LF 402 R1516 — USB_EXTD_OC_L
1K 5% 1/16W MF-LF 402 R1536 — USB_EXTB_OC_EHCI_L
1K 5% 1/16W MF-LF 402 R1537 — USB_EXTD_OC_EHCI_L

=PP3V3_S4_SDCARD
10K 5% 1/16W MF-LF 402 R1520 — SDCONN_STATE_CHANGE

ITPXDP_CLK100M_N — NOSTUFF R1553 0 5% 1/16W MF-LF 402 — ITPCPU_CLK100M_N
ITPXDP_CLK100M_P — NOSTUFF R1554 0 5% 1/16W MF-LF 402 — ITPCPU_CLK100M_P

=PP3V3_S0_LED_SATA
R1556 10K 5% 1/16W MF-LF 402 — PCH_SATALED_L
=PP3V3_S4_PCH
R1505 10K 5% 1/16W MF-LF 402 — AP_PWR_EN

=PP3V3_S5_PCH_STRAPS
SPI_DESCRIPTOR_OVERRIDE_L (IN) → Q1500 NTR1P02L SOT23-3-HF (S, G, D)
PLACE_NEAR=R1805.4:3mm
SPI_DESCRIPTOR_OVERRIDE_R — 330 5% 1/16W MF-LF 402 R1552 — HDA_SDOUT_R (OUT)

=PP3V3_S0_PCH_GPIO
10K 5% 1/16W MF-LF 402 R1558 — BT_PWR_RST_L
10K 5% 1/16W MF-LF 402 R1557 — TBT_PWR_REQ_L

=PP3V3_S0_PCH_STRAPS
10K 5% 1/16W MF-LF 402 R1509 — DP_AUXCH_ISOL
10K 5% 1/16W MF-LF 402 R1510 — PCH_GPIO1
10K 5% 1/16W MF-LF 402 R1511 — PCH_GPIO48

DP_AUXIO_EN Inversion

Inverts PCH GPIO DP_AUXCH_ISOL to drive DP_AUXIO_EN for external DP

=PP3V3_S0_PCH_STRAPS
R1507 10K 5% 1/16W MF-LF 402
DP_AUXIO_EN (OUT)
CRITICAL Q1509 SSM3K15AMFVAPE VESM (D, G, S)
DP_AUXCH_ISOL

=PP3V3_S0_PCH_STRAPS
NOSTUFF R1529 4.7K 5% 1/16W MF-LF 402 — PCH_SPKR
R1528 10K 5% 1/16W MF-LF 402 — SATARDRVR_EN
R1527 10K 5% 1/16W MF-LF 402 — PCH_CAM_EXT_BOOT
R1526 10K 5% 1/16W MF-LF 402 — PCH_CAM_RESET
R1525 10K 5% 1/16W MF-LF 402 — MLB_RAM_CFG1
R1524 10K 5% 1/16W MF-LF 402 — MLB_RAM_CFG0
R1542 10K 5% 1/16W MF-LF 402 — SMC_RUNTIME_SCI_L

=PP3V3_S0_PCH_STRAPS
R1540 10K 5% 1/16W MF-LF 402 — TBT_CLKREQ_L
R1539 10K 5% 1/16W MF-LF 402 — ENET_CLKREQ_L
R1538 10K 5% 1/16W MF-LF 402 — AP_CLKREQ_L
R1541 10K 5% 1/16W MF-LF 402 — SSD_CLKREQ_L
R1508 10K 5% 1/16W MF-LF 402 — PEG_CLKREQ_L

=PP3V3_TBT_PCH_GPIO
R1562 10K 5% 1/16W MF-LF 402 — JTAG_TBT_TDO
R1561 10K 5% 1/16W MF-LF 402 — JTAG_TBT_TDI
R1560 10K 5% 1/16W MF-LF 402 — JTAG_TBT_TMS
NOSTUFF R1559 10K 5% 1/16W MF-LF 402 — TBT_SW_RESET_R_L
R1567 10K 5% 1/16W MF-LF 402 — JTAG_TBT_TCK

HDA_SYNC — 1K 5% 1/16W MF-LF 402 R1514

IVB PCIe Straps configuration:

CFG[5:6] = Sel PCIe Cfg
11 = 1x16 (default)
10 = 2x8
00 = 1x8,2x4

CFG[3]=Direct/Rev for X4
1 = DIR
0 = REV

CFG[2]= Direct/Rev for x16
1 = DIR
0 = REV

CPU_CFG<5> — 1K NOSTUFF R1512 5% 1/16W MF-LF 402
CPU_CFG<6> — 1K NOSTUFF R1513 5% 1/16W MF-LF 402
CPU_CFG<3> — 1K NOSTUFF R1523 5% 1/16W MF-LF 402
U1000.18:3mm
CPU_CFG<2> — 1K R1522 5% 1/16W MF-LF 402

PM_SLP_S5_L — 100K R1570 5% 1/16W MF-LF 402
PM_SLP_S4_L — 100K R1571 5% 1/16W MF-LF 402
PM_SLP_S3_L — 100K R1572 5% 1/16W MF-LF 402
PCH_GPIO22 — 10K R1533 5% 1/16W MF-LF 402
PCH_GPIO6 — 20K R1532 5% 1/16W MF-LF 402
ENET_MEDIA_SENSE — 10K R1531 5% 1/16W MF-LF 402
WOL_EN — 10K R1530 5% 1/16W MF-LF 402
PCH_GPIO29 — 10K R1555 5% 1/16W MF-LF 402
TBT_CIO_PLUG_EVENT — 10K R1521 5% 1/16W MF-LF 402
ENET_LOW_PWR_PCH — 10K R1503 5% 1/16W MF-LF 402

UNUSED clock terminations for FCIM MODE

PCH_CLKIN_GND1 — 10K R1551 5% 1/16W MF-LF 402
PCH_CLKIN_GND0 — 10K R1550 5% 1/16W MF-LF 402
PCH_CLK14P3M_REFCLK — 10K R1549 5% 1/16W MF-LF 402
PCH_CLK100M_DMIN — PLACE_NEAR=U1800.P33:5mm — 10K R1548 5% 1/16W MF-LF 402
PCH_CLK100M_DMIP — PLACE_NEAR=U1800.R33:5mm — 10K R1547 5% 1/16W MF-LF 402
PCH_CLK100M_SATAN — PLACE_NEAR=U1800.AF55:5mm — 10K R1546 5% 1/16W MF-LF 402
PCH_CLK100M_SATAP — PLACE_NEAR=U1800.AG56:5mm — 10K R1545 5% 1/16W MF-LF 402
PCH_CLK96M_DOTN — PLACE_NEAR=U1800.BD38:5mm — 10K R1544 5% 1/16W MF-LF 402
PCH_CLK96M_DOTP — PLACE_NEAR=U1800.BF38:5mm — 10K R1543 5% 1/16W MF-LF 402

SYNC_MASTER=D7_TONY SYNC_DATE=01/11/2012
PAGE TITLE: STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D
REVISION: 4.2.0
BRANCH:
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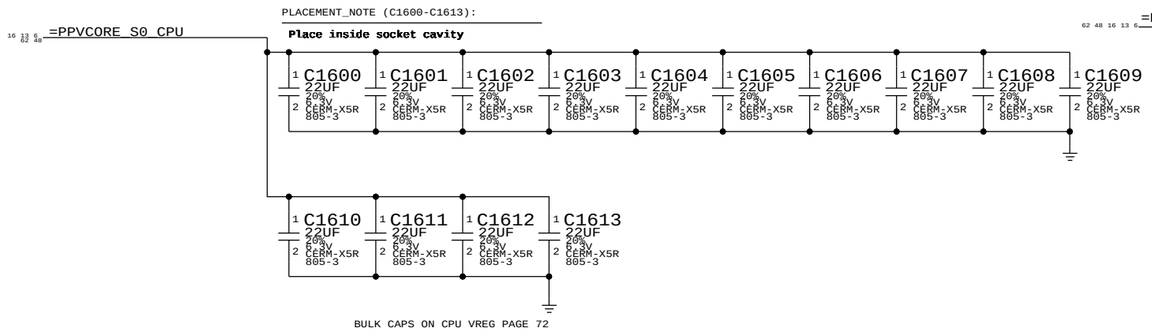
SHEET: 15 OF 100

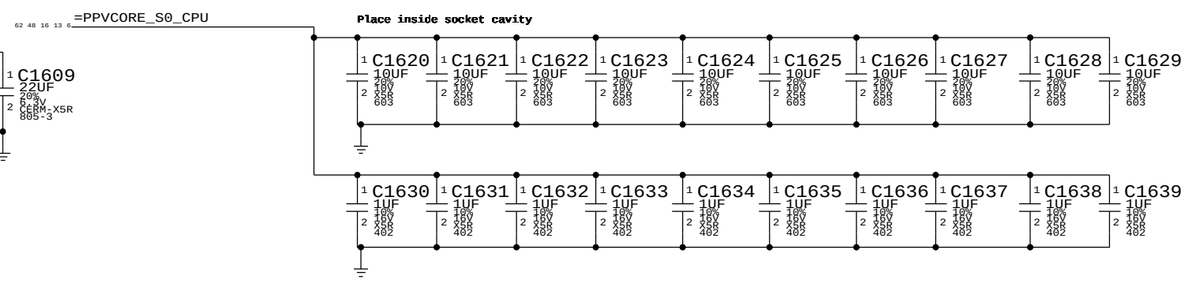
CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)



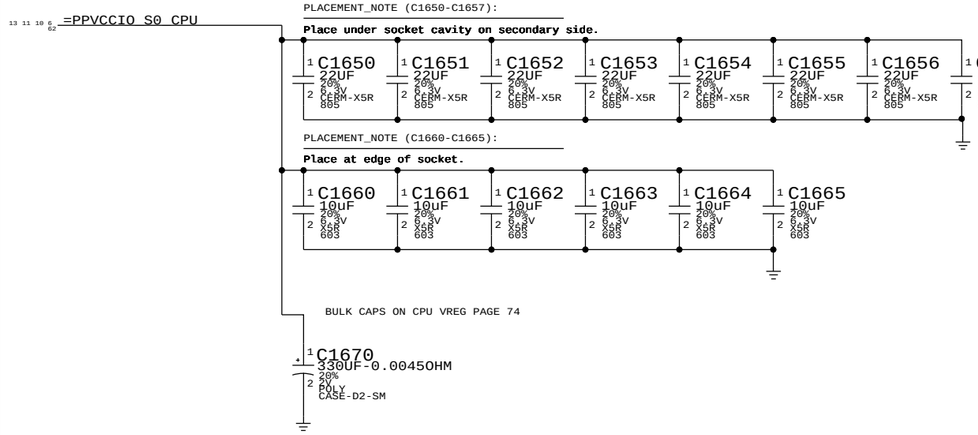
BULK CAPS ON CPU VREG PAGE 72

10x 10UF and 10x 1UF CAPACITORS



CPU VCCIO DECOUPLING

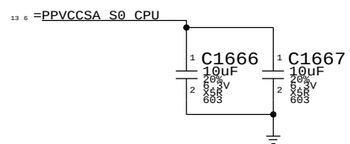
8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders



BULK CAPS ON CPU VREG PAGE 74

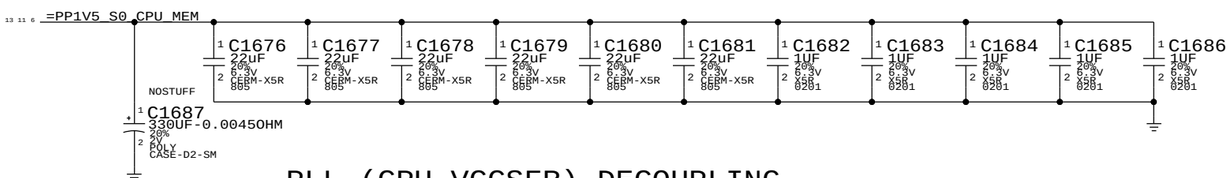
CPU VCCSA DECOUPLING

2x 10uF 0603. INTEL RECOMMENDATION 2X 10uF 0805



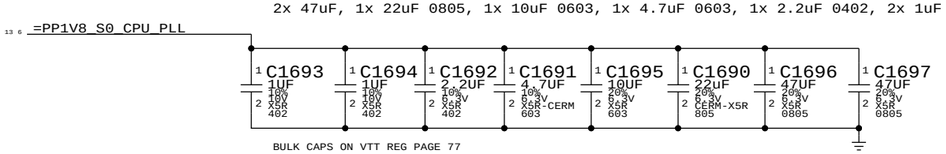
Bulk decoupling is on VCCSA reg page 75

Memory (CPU VCCDDR) DECOUPLING



PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 1x 10uF 0805



BULK CAPS ON VTT REG PAGE 77

SYNC_MASTER=K70 MLB SYNC_DATE=11/30/2011

PAGE TITLE

CPU NON-GFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

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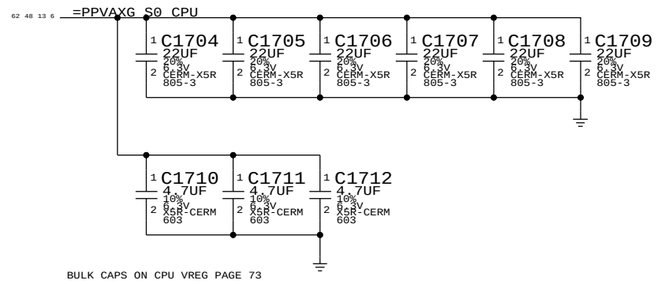
VAXG DECOUPLING

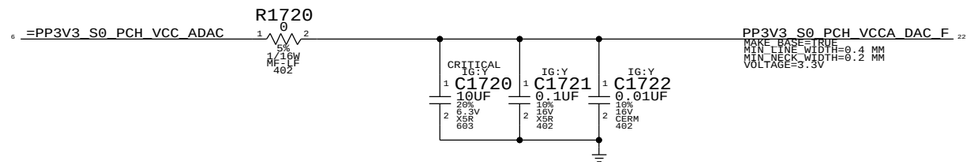
INTEL RECOMMENDATION 4X22UF 0805,3X 4.7UF

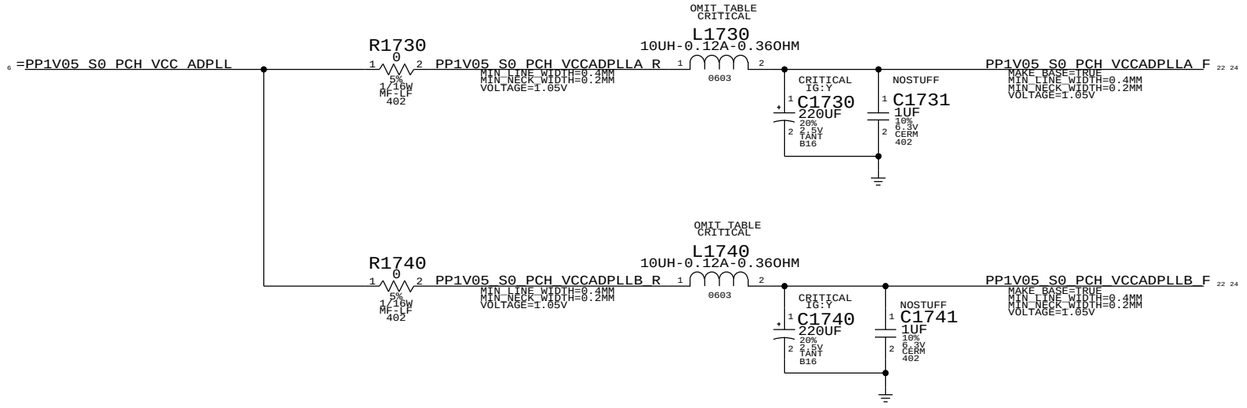
PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity



BULK CAPS ON CPU VREG PAGE 73





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1070	2	IND,WW,10UH,20%.120MA,0.36OHMS	L1730,L1740	CRITICAL	IG:Y
113S0022	2	RES,MF,1/10W,0OHM,5,0603,SMD,LF	L1730,L1740		IG:N

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE

GFX DECOUPLING & PCH PWR ALIAS

Apple Inc.

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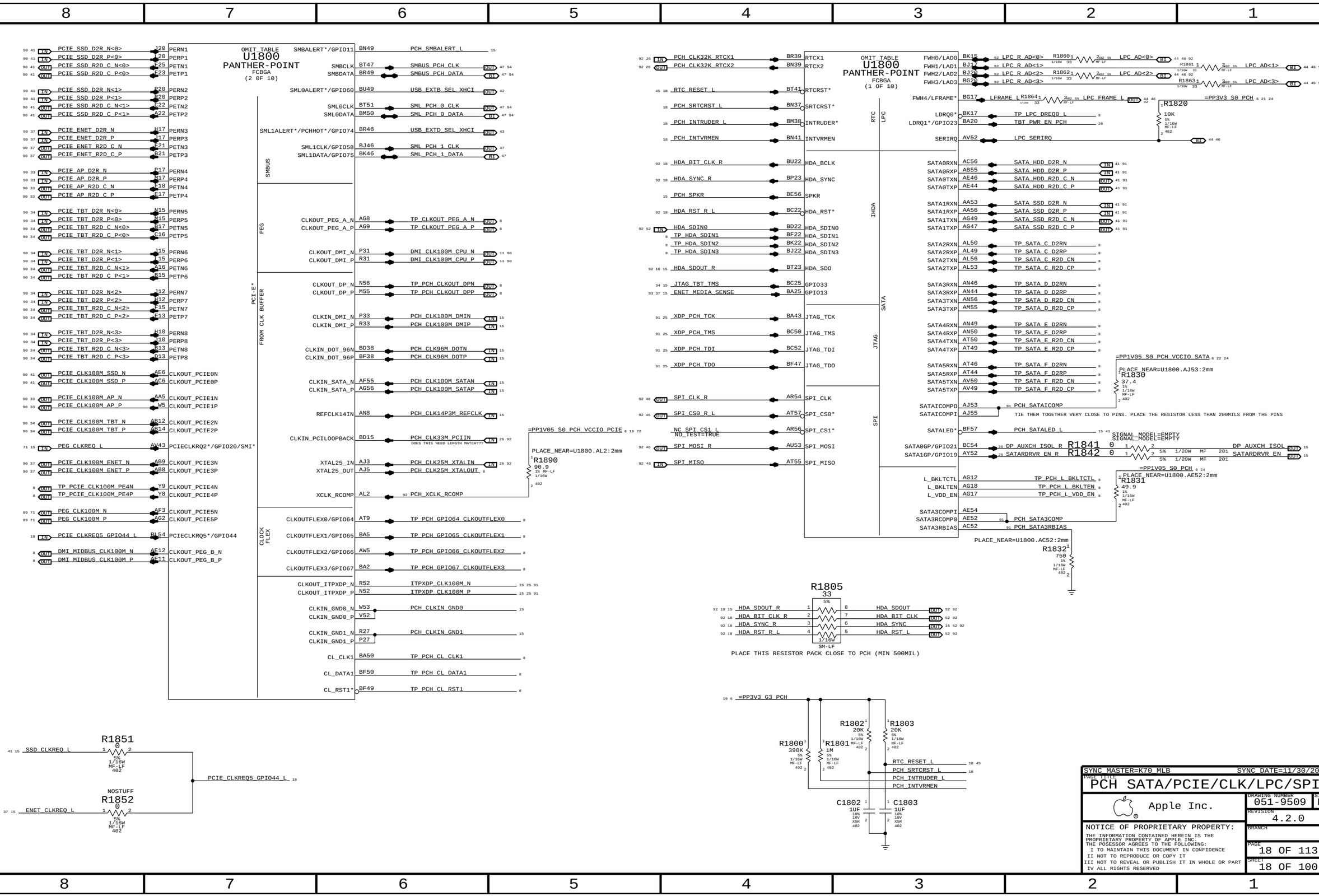
OMIT TABLE
U1800
PANTHER-POINT
FCBGA
(2 OF 10)
PCI-E*
FROM CLK BUFFER
SMBUS
PEG
CLOCK FLEX
PCIE_SSD_D2R_N<0>
PCIE_SSD_D2R_P<0>
PCIE_SSD_R2D_C_N<0>
PCIE_SSD_R2D_C_P<0>
PCIE_SSD_D2R_N<1>
PCIE_SSD_D2R_P<1>
PCIE_SSD_R2D_C_N<1>
PCIE_SSD_R2D_C_P<1>
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_D2R_N<3>
PCIE_TBT_D2R_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_C_P<3>
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
PEG_CLKREQ_L
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
PEG_CLK100M_N
PEG_CLK100M_P
PCIE_CLKREQ5_GPIO44_L
DMI_MIDBUS_CLK100M_N
DMI_MIDBUS_CLK100M_P
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20/SMI*
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKIN_GND0_N
CLKIN_GND0_P
CLKIN_GND1_N
CLKIN_GND1_P
CL_CLK1
CL_DATA1
CL_RST1*
PCH_SMBALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
USB_EXTB_SEL_XHCI
SML_PCH_0_CLK
SML_PCH_0_DATA
USB_EXTD_SEL_XHCI
SML_PCH_1_CLK
SML_PCH_1_DATA
TP_CLKOUT_PEG_A_N
TP_CLKOUT_PEG_A_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
PCH_CLK100M_DMIN
PCH_CLK100M_DMIP
PCH_CLK96M_DOTN
PCH_CLK96M_DOTP
PCH_CLK100M_SATAN
PCH_CLK100M_SATAP
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
DOES THIS NEED LENGTH MATCH???
PCH_CLK25M_XTALIN
PCH_CLK25M_XTALOUT
PCH_XCLK_RCOMP
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
PCH_CLKIN_GND0
PCH_CLKIN_GND1
TP_PCH_CL_CLK1
TP_PCH_CL_DATA1
TP_PCH_CL_RST1
=PP1V05_S0_PCH_VCCIO_PCIE
PLACE_NEAR=U1800.AL2:2mm
R1890
90.9
1% MF-LF 1/16W 402
R1851
0
SSD_CLKREQ_L
NOSTUFF
R1852
0
ENET_CLKREQ_L
PCIE_CLKREQ5_GPIO44_L
5% 1/16W MF-LF 402
OMIT TABLE
U1800
PANTHER-POINT
FCBGA
(1 OF 10)
RTC
LPC
IHDA
SATA
JTAG
SPI
PCH_CLK32K_RTCX1
PCH_CLK32K_RTCX2
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_TBT_TMS
ENET_MEDIA_SENSE
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
NC_SPI_CS1_L
NO_TEST=TRUE
SPI_MOSI_R
SPI_MISO
RTCX1
RTCX2
RTCRST*
SRTCRST*
INTRUDER*
INTVRMEN
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST*
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
GPIO33
GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
SPI_CLK
SPI_CS0*
SPI_CS1*
SPI_MOSI
SPI_MISO
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME*
LDRQ0*
LDRQ1*/GPIO23
SERIRQ
LPC_R_AD<0>
LPC_R_AD<1>
LPC_R_AD<2>
LPC_R_AD<3>
LFRAME_L
LPC_FRAME_L
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
=PP3V3_S0_PCH
R1820
10K
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA_SSD_D2R_N
SATA_SSD_D2R_P
SATA_SSD_R2D_C_N
SATA_SSD_R2D_C_P
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_C_R2D_CN
TP_SATA_C_R2D_CP
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
=PP1V05_S0_PCH_VCCIO_SATA
PLACE_NEAR=U1800.AJ53:2mm
R1830
37.4
SATAICOMPO
SATAICOMPI
PCH_SATAICOMPI
TIE THEM TOGETHER VERY CLOSE TO PINS. PLACE THE RESISTOR LESS THAN 200MILS FROM THE PINS
SATALED*
PCH_SATALED_L
SATA0GP/GPIO21
SATA1GP/GPIO19
DP_AUXCH_ISOL_R
SATARDRVR_EN_R
R1841
R1842
DP_AUXCH_ISOL
SATARDRVR_EN
SIGNAL_MODEL=EMPTY
L_BKLTCTL
L_BKLTEN
L_VDD_EN
TP_PCH_L_BKLTCTL
TP_PCH_L_BKLTEN
TP_PCH_L_VDD_EN
SATA3COMPI
SATA3RCOMP0
SATA3RBIAS
PCH_SATA3COMP
PCH_SATA3RBIAS
=PP1V05_S0_PCH
PLACE_NEAR=U1800.AE52:2mm
R1831
49.9
PLACE_NEAR=U1800.AC52:2mm
R1832
750
R1805
33
HDA_SDOUT_R
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_RST_R_L
HDA_SDOUT
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
PLACE THIS RESISTOR PACK CLOSE TO PCH (MIN 500MIL)
=PP3V3_G3_PCH
R1800
390K
R1801
1M
R1802
20K
R1803
20K
C1802
1UF
C1803
1UF
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN
SYNC_MASTER=K70_MLB
SYNC_DATE=11/30/2011
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PCH SATA/PCIE/CLK/LPC/SPI
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051-9509
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REVISION
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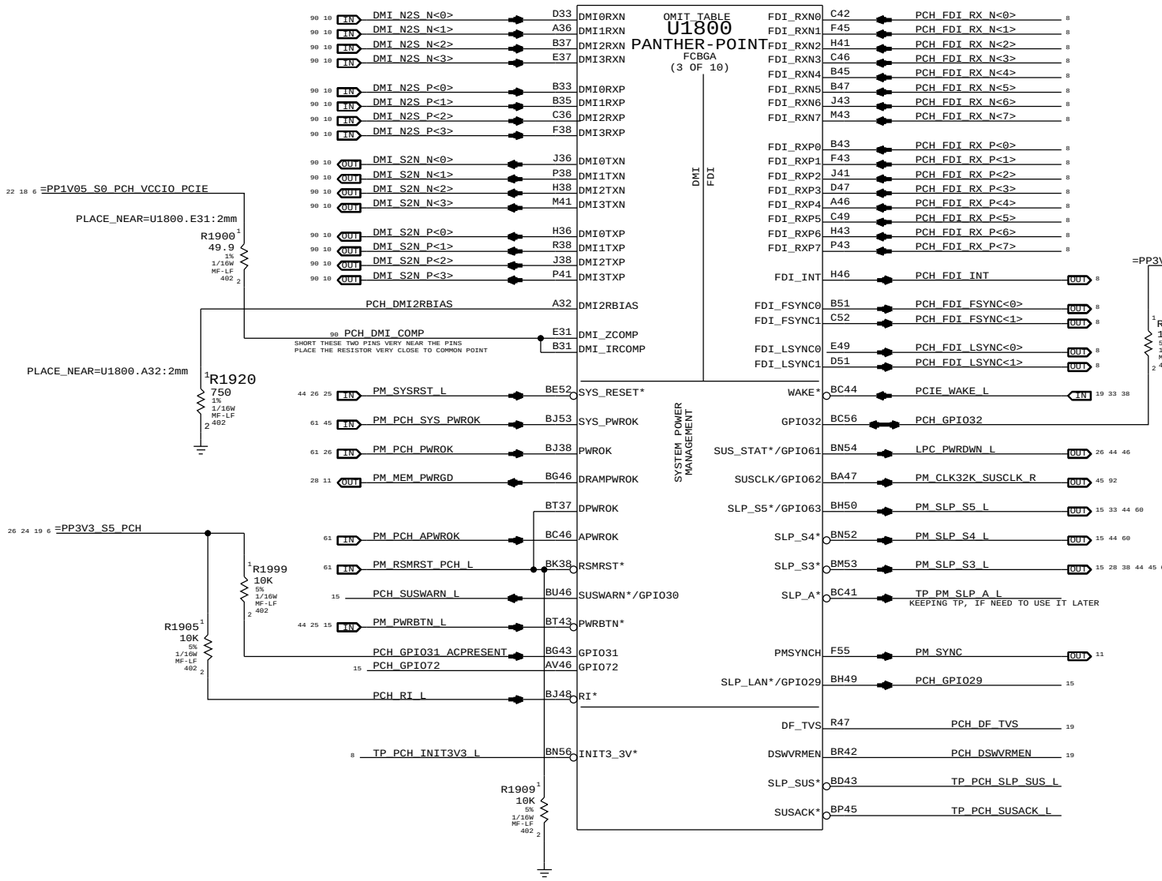

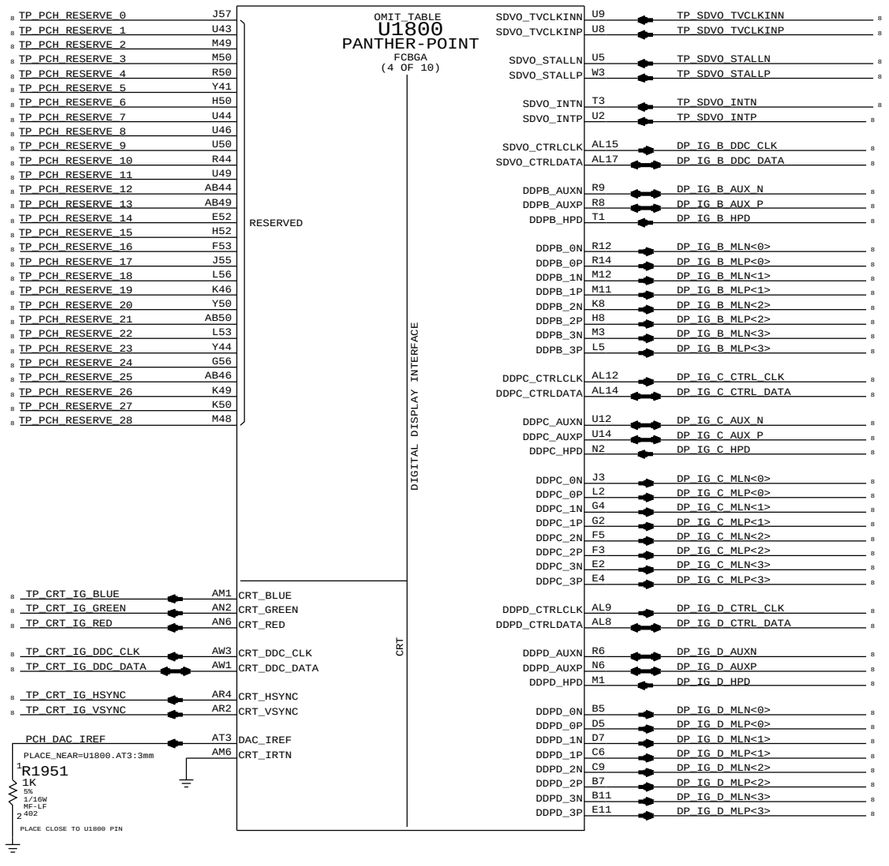

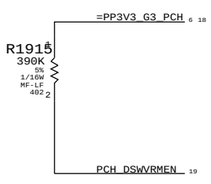

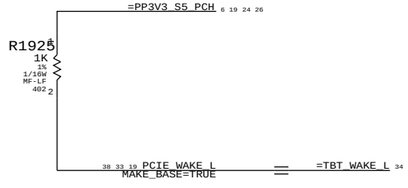

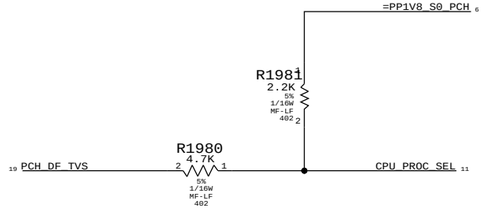

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PCH DMI/FDI/GRAPHICS

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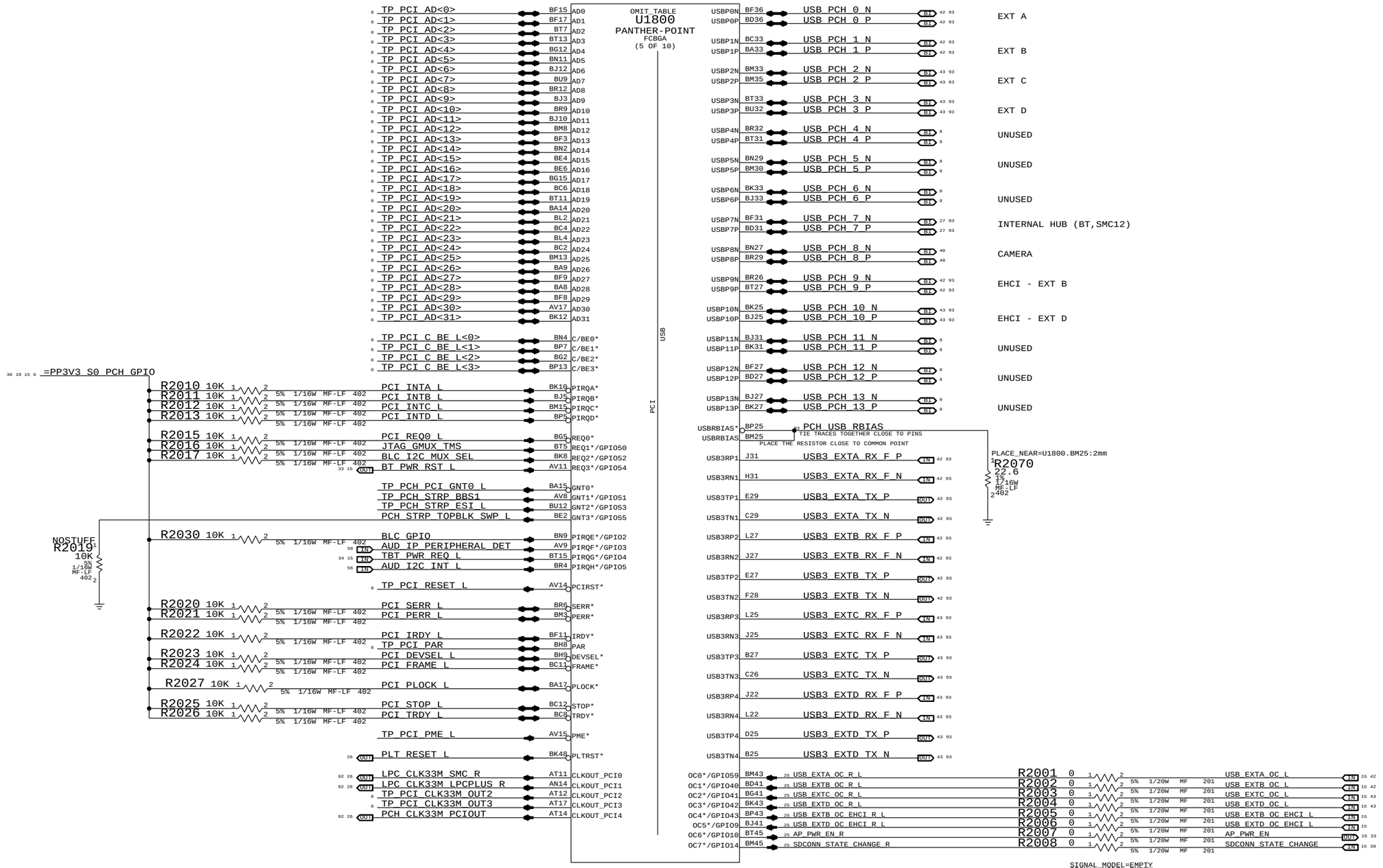

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PCH PCI/USB

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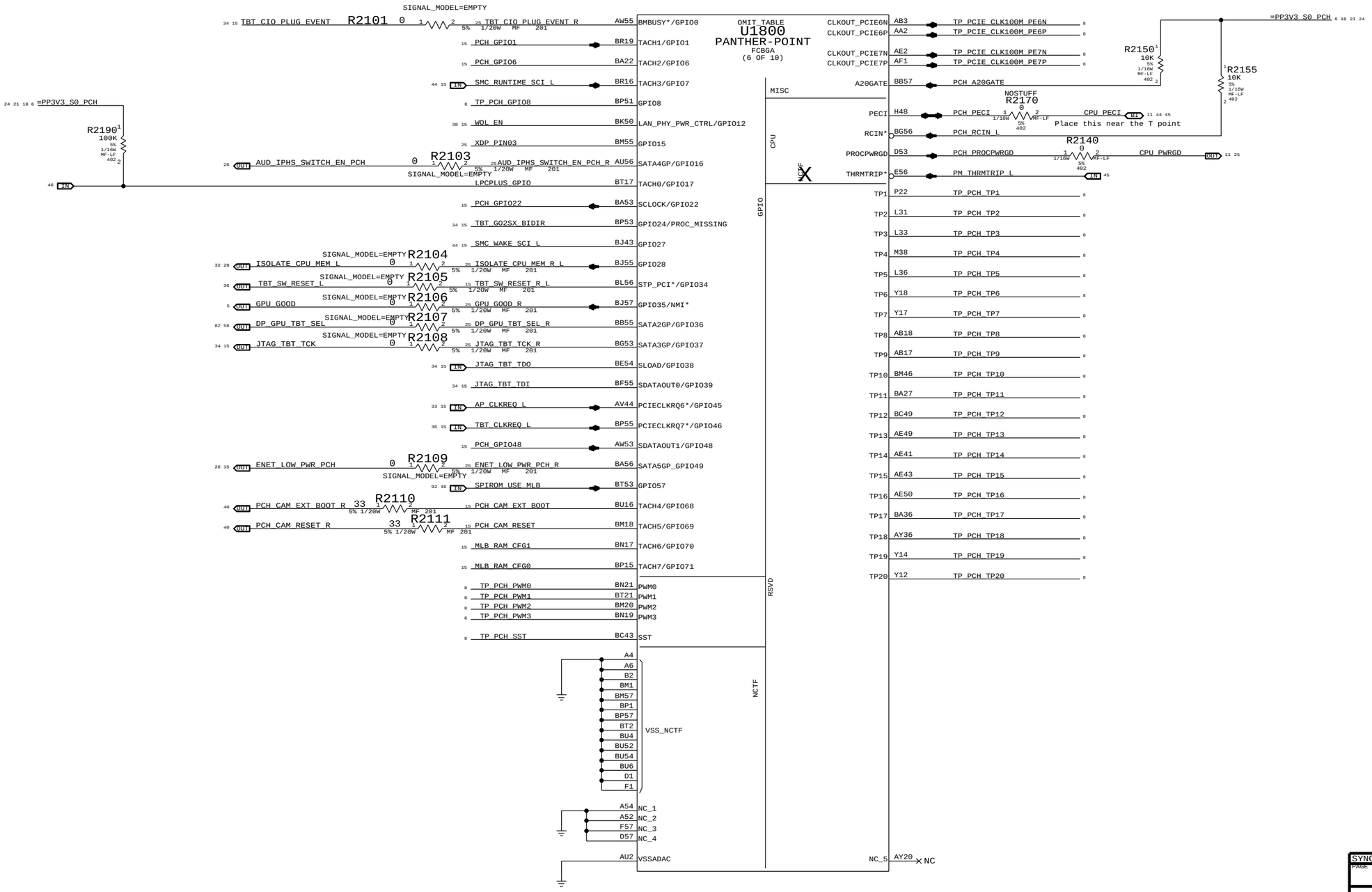

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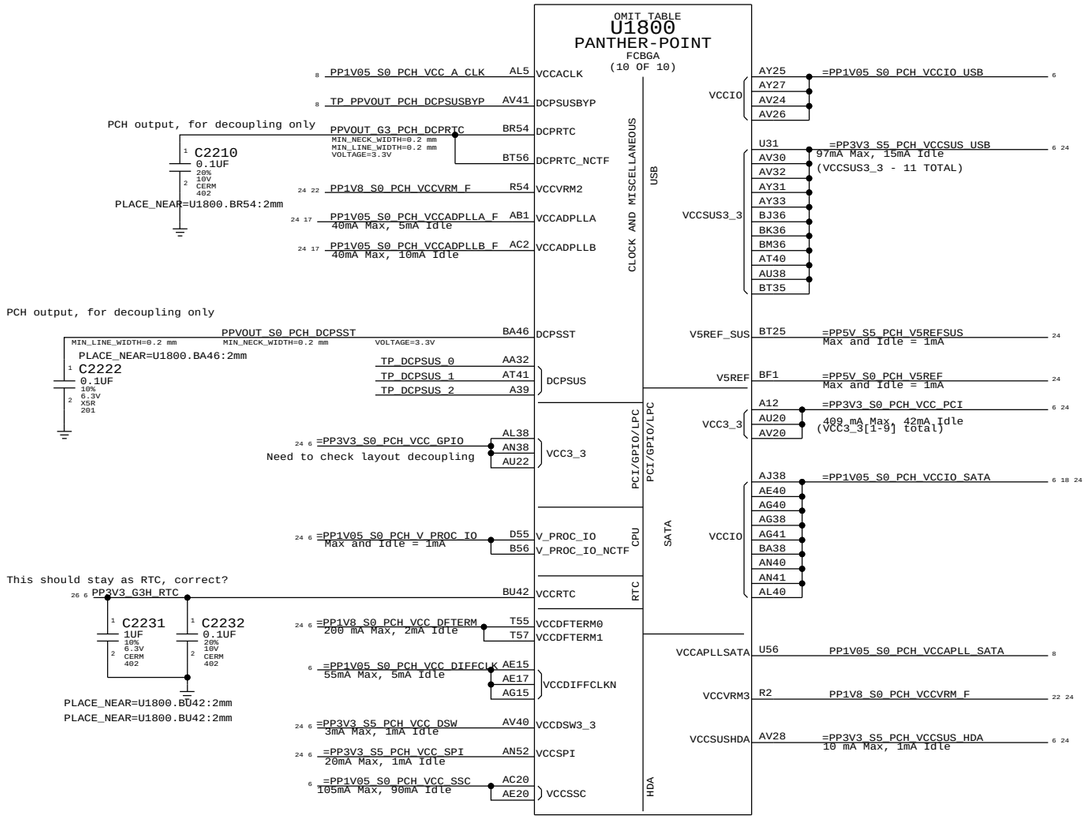

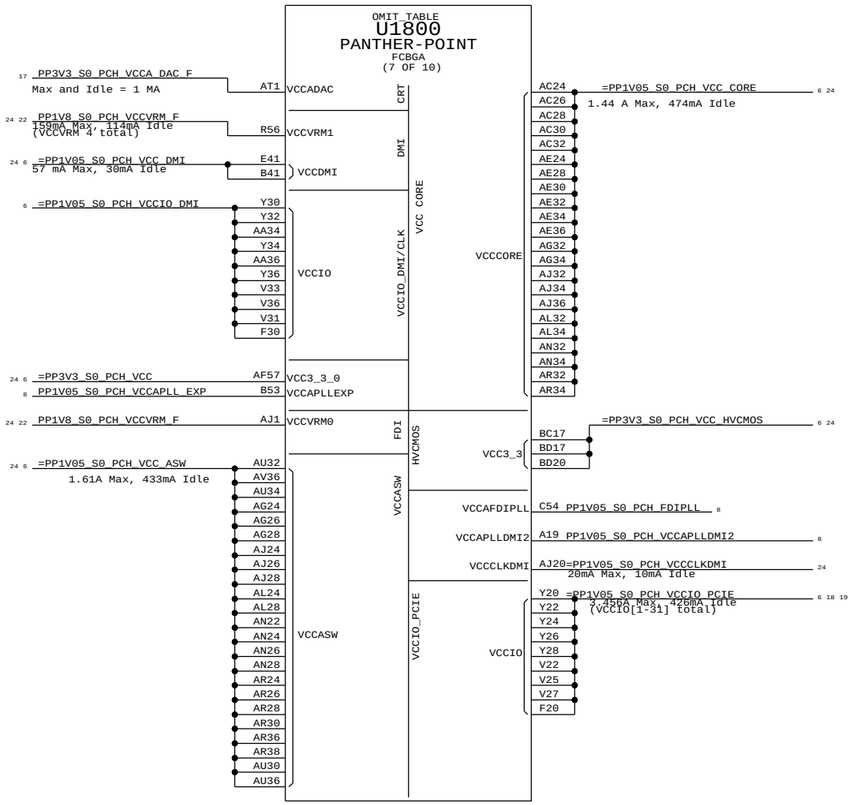

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PCH POWER

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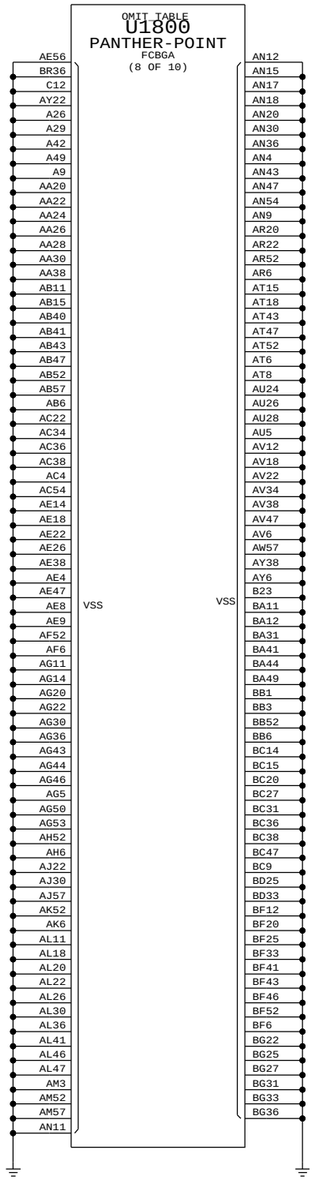

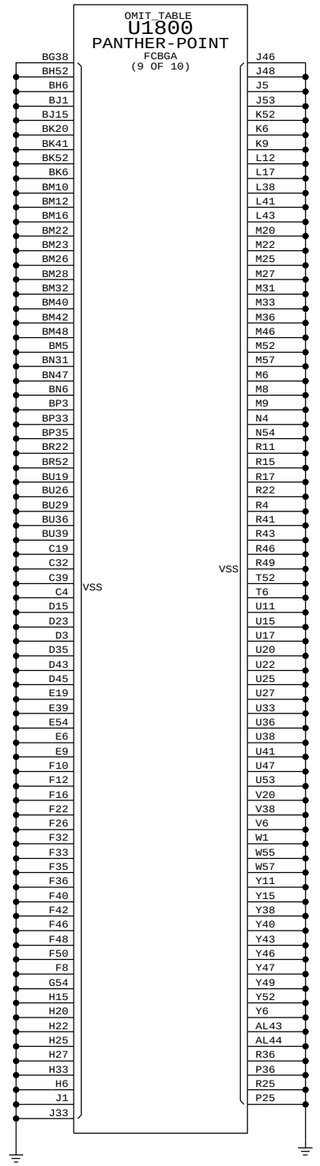

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PAGE TITLE

PCH GROUNDS

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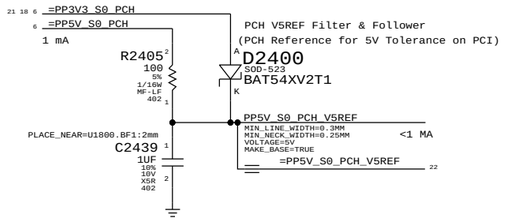
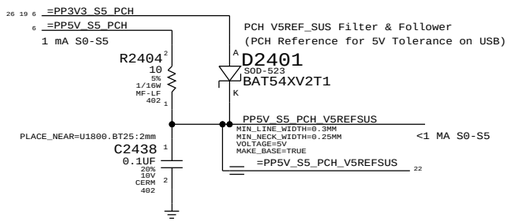
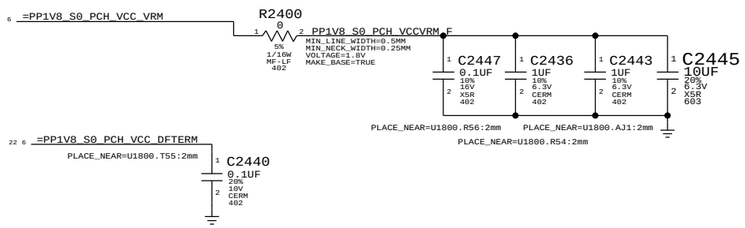
Power Sequencing

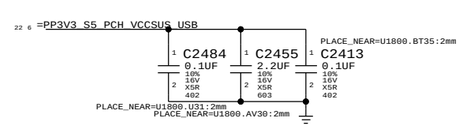


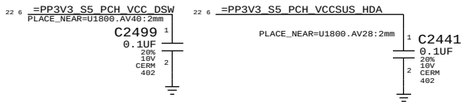


1V8 S0 Rails

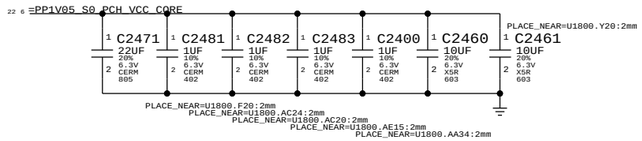


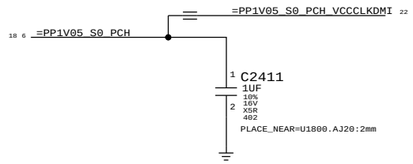
3V3 S5 Rails

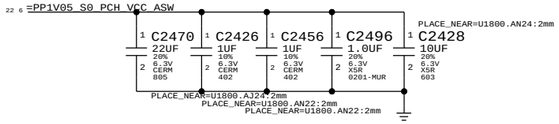


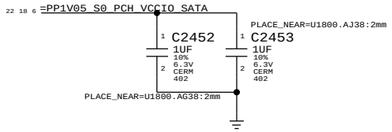


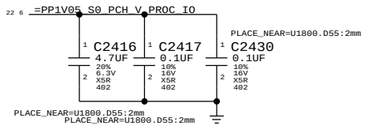
1V05 S0 Rails

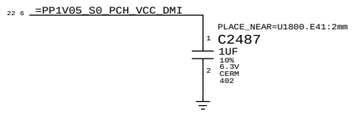


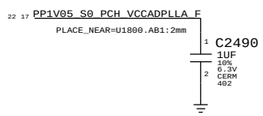


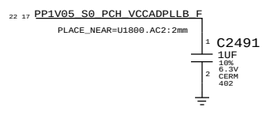




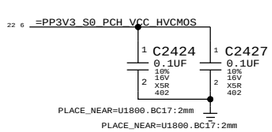


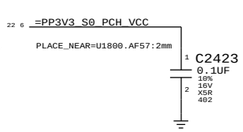


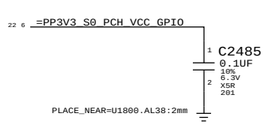


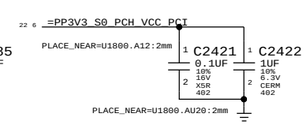


3V3 S0 Rails









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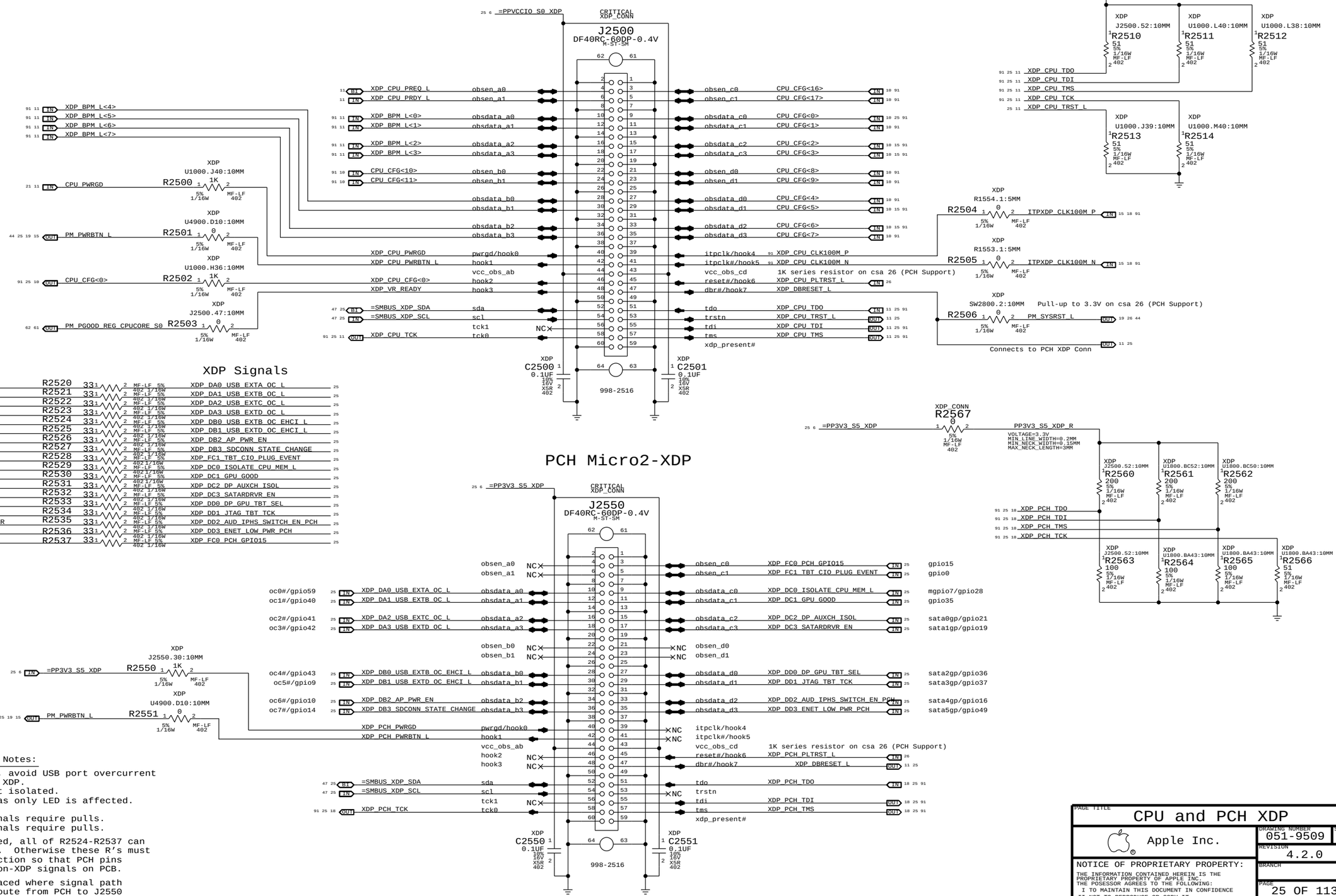
CPU Micro2-XDP



PCH Micro2-XDP

PCH Signals

USB_EXTA_OC_R_L	R2520	33	XDP_DA0_USB_EXTA_OC_L
USB_EXTB_OC_R_L	R2521	33	XDP_DA1_USB_EXTB_OC_L
USB_EXTC_OC_R_L	R2522	33	XDP_DA2_USB_EXTC_OC_L
USB_EXTD_OC_R_L	R2523	33	XDP_DA3_USB_EXTD_OC_L
USB_EXTB_OC_EHCI_R_L	R2524	33	XDP_DB0_USB_EXTB_OC_EHCI_L
USB_EXTD_OC_EHCI_R_L	R2525	33	XDP_DB1_USB_EXTD_OC_EHCI_L
AP_PWR_EN_R	R2526	33	XDP_DB2_AP_PWR_EN
SDCONN_STATE_CHANGE_R	R2527	33	XDP_DB3_SDCONN_STATE_CHANGE
TBT_CIO_PLUG_EVENT_R	R2528	33	XDP_FC1_TBT_CIO_PLUG_EVENT
ISOLATE_CPU_MEM_R_L	R2529	33	XDP_DC0_ISOLATE_CPU_MEM_L
GPU_GOOD_R	R2530	33	XDP_DC1_GPU_GOOD
DP_AUXCH_ISOL_R	R2531	33	XDP_DC2_DP_AUXCH_ISOL
SATARDRVR_EN_R	R2532	33	XDP_DC3_SATARDRVR_EN
DP_GPU_TBT_SEL_R	R2533	33	XDP_DD0_DP_GPU_TBT_SEL
JTAG_TBT_TCK_R	R2534	33	XDP_DD1_JTAG_TBT_TCK
AUD_IPHS_SWITCH_EN_PCH_R	R2535	33	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH
ENET_LOW_PWR_PCH_R	R2536	33	XDP_DD3_ENET_LOW_PWR_PCH
XDP_PIN03	R2537	33	XDP_FC0_PCH_GPIO15

XDP Signals

XDP_DA0_USB_EXTA_OC_L	R2538	33	USB_EXTA_OC_R_L
XDP_DA1_USB_EXTB_OC_L	R2539	33	USB_EXTB_OC_R_L
XDP_DA2_USB_EXTC_OC_L	R2540	33	USB_EXTC_OC_R_L
XDP_DA3_USB_EXTD_OC_L	R2541	33	USB_EXTD_OC_R_L
XDP_DB0_USB_EXTB_OC_EHCI_L	R2542	33	USB_EXTB_OC_EHCI_R_L
XDP_DB1_USB_EXTD_OC_EHCI_L	R2543	33	USB_EXTD_OC_EHCI_R_L
XDP_DB2_AP_PWR_EN	R2544	33	AP_PWR_EN_R
XDP_DB3_SDCONN_STATE_CHANGE	R2545	33	SDCONN_STATE_CHANGE_R
XDP_FC1_TBT_CIO_PLUG_EVENT	R2546	33	TBT_CIO_PLUG_EVENT_R
XDP_DC0_ISOLATE_CPU_MEM_L	R2547	33	ISOLATE_CPU_MEM_R_L
XDP_DC1_GPU_GOOD	R2548	33	GPU_GOOD_R
XDP_DC2_DP_AUXCH_ISOL	R2549	33	DP_AUXCH_ISOL_R
XDP_DC3_SATARDRVR_EN	R2550	33	SATARDRVR_EN_R
XDP_DD0_DP_GPU_TBT_SEL	R2551	33	DP_GPU_TBT_SEL_R
XDP_DD1_JTAG_TBT_TCK	R2552	33	JTAG_TBT_TCK_R
XDP_DD2_AUD_IPHS_SWITCH_EN_PCH	R2553	33	AUD_IPHS_SWITCH_EN_PCH_R
XDP_DD3_ENET_LOW_PWR_PCH	R2554	33	ENET_LOW_PWR_PCH_R
XDP_FC0_PCH_GPIO15	R2555	33	XDP_PIN03

PCH/XDP Signal Isolation Notes:

- USB OC#'s not isolated, avoid USB port overcurrent events while using PCH XDP.
- Unused GPIOs 0 & 15 not isolated.
- MXM_GOOD not isolated as only LED is affected.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

If PCH XDP not implemented, all of R2524-R2537 can be replaced with aliases. Otherwise these R's must be stuffed even in production so that PCH pins connect to appropriate non-XDP signals on PCB.

R2524-R2537 should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

PAGE TITLE	CPU and PCH XDP
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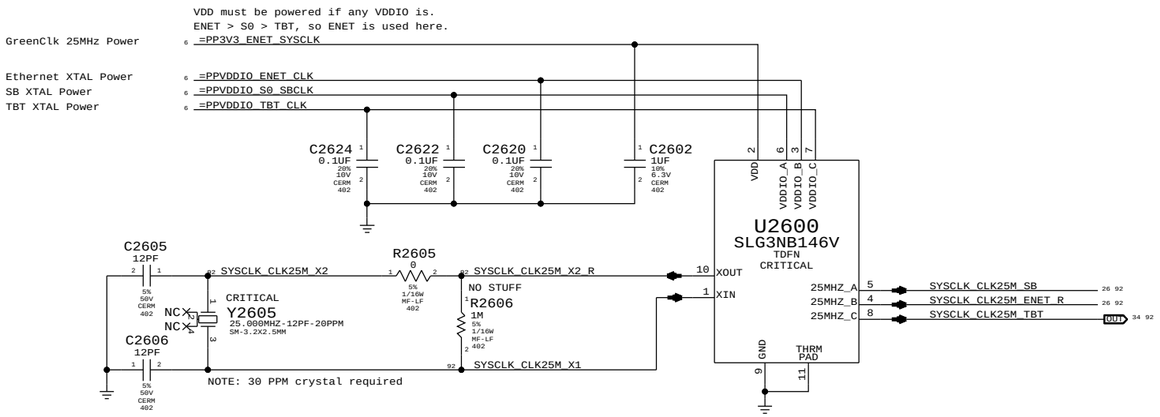
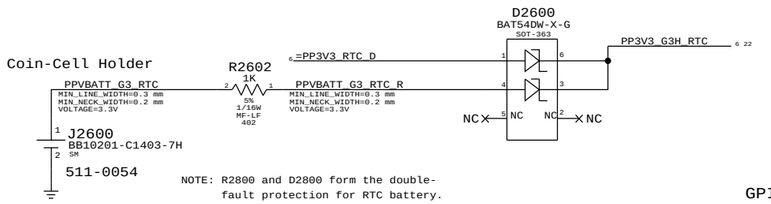
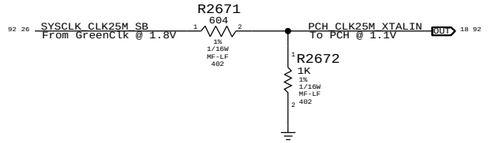
System 25MHz Clock Generator



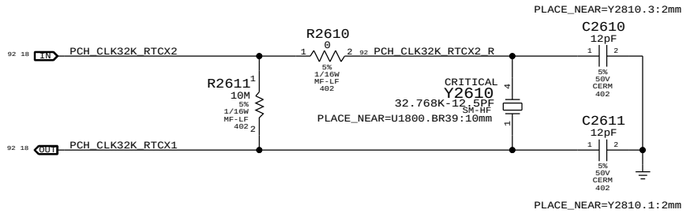
RTC Power Sources



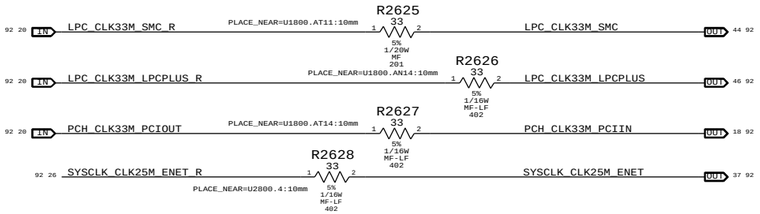
PCH 25MHZ CLOCK



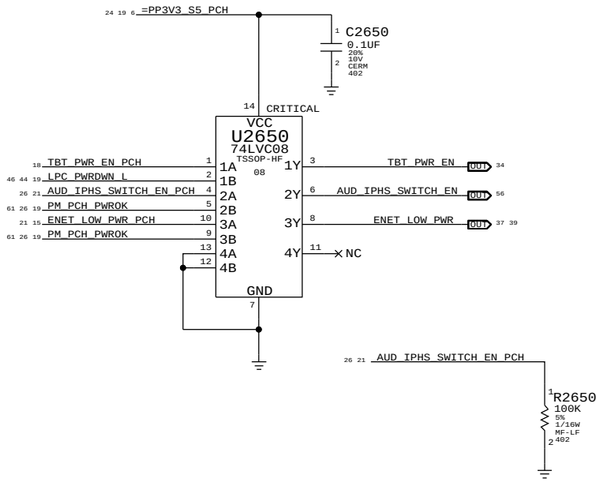
PCH RTC Crystal



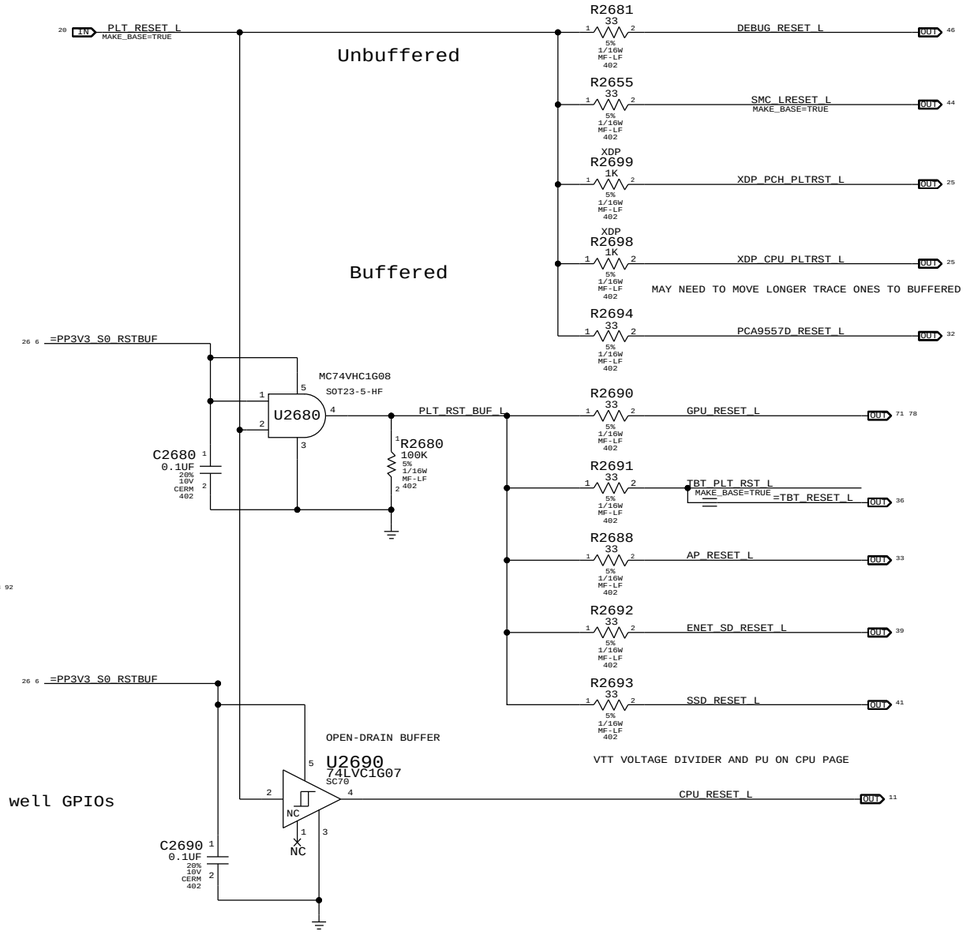
Clock series termination



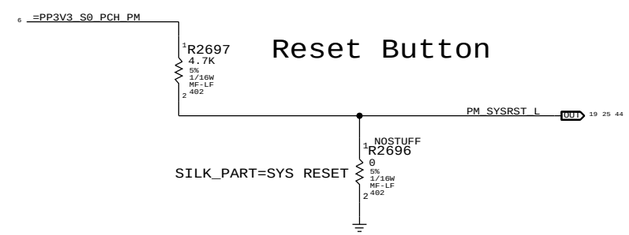
GPIO Isolation to prevent glitches on critical core well GPIOs



Platform Reset Connections



Reset Button



SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

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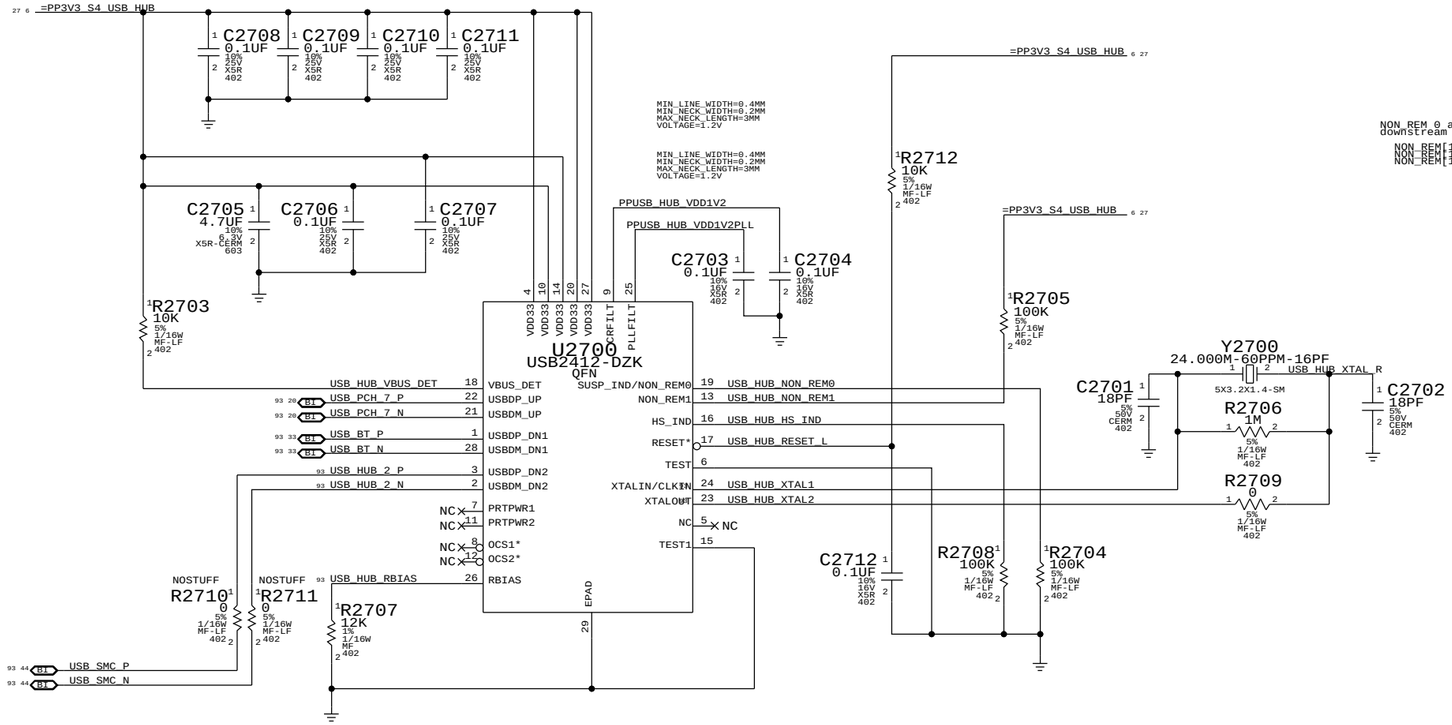

SYNC_MASTER=D7_NICK SYNC_DATE=12/13/2011

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USB HUB

Apple Inc.

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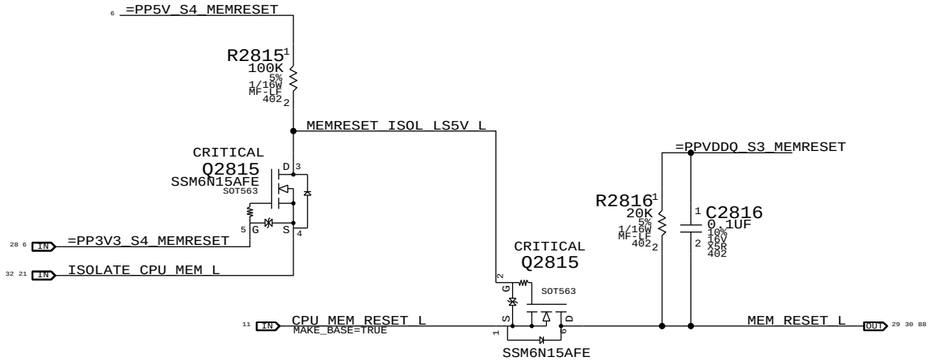
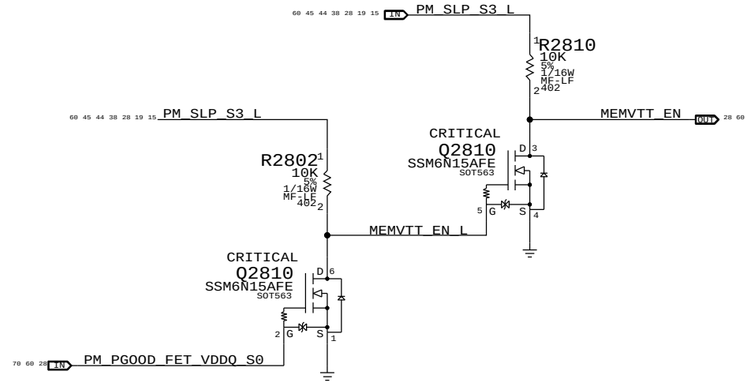
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

MEMVTT_EN = PM_PGOOD_FET_VDDQ_S0 * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L





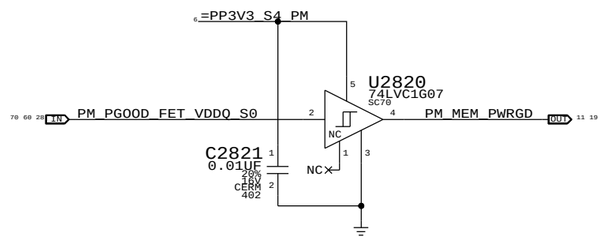
	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1
to	1	0	1	1	1	1	1
S3	2	0	0	1	1	1	0
	3	0	0	0	X	1	0
S3	4	0	0	1	X	1	0
to	5	0	1	1	0 (*)	1	1
S0	6	0	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

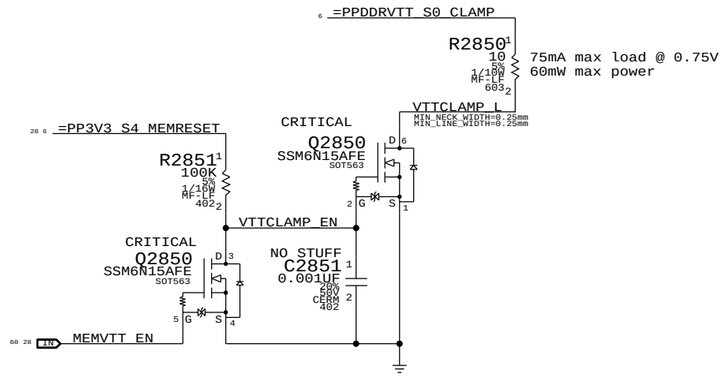
1V5 S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

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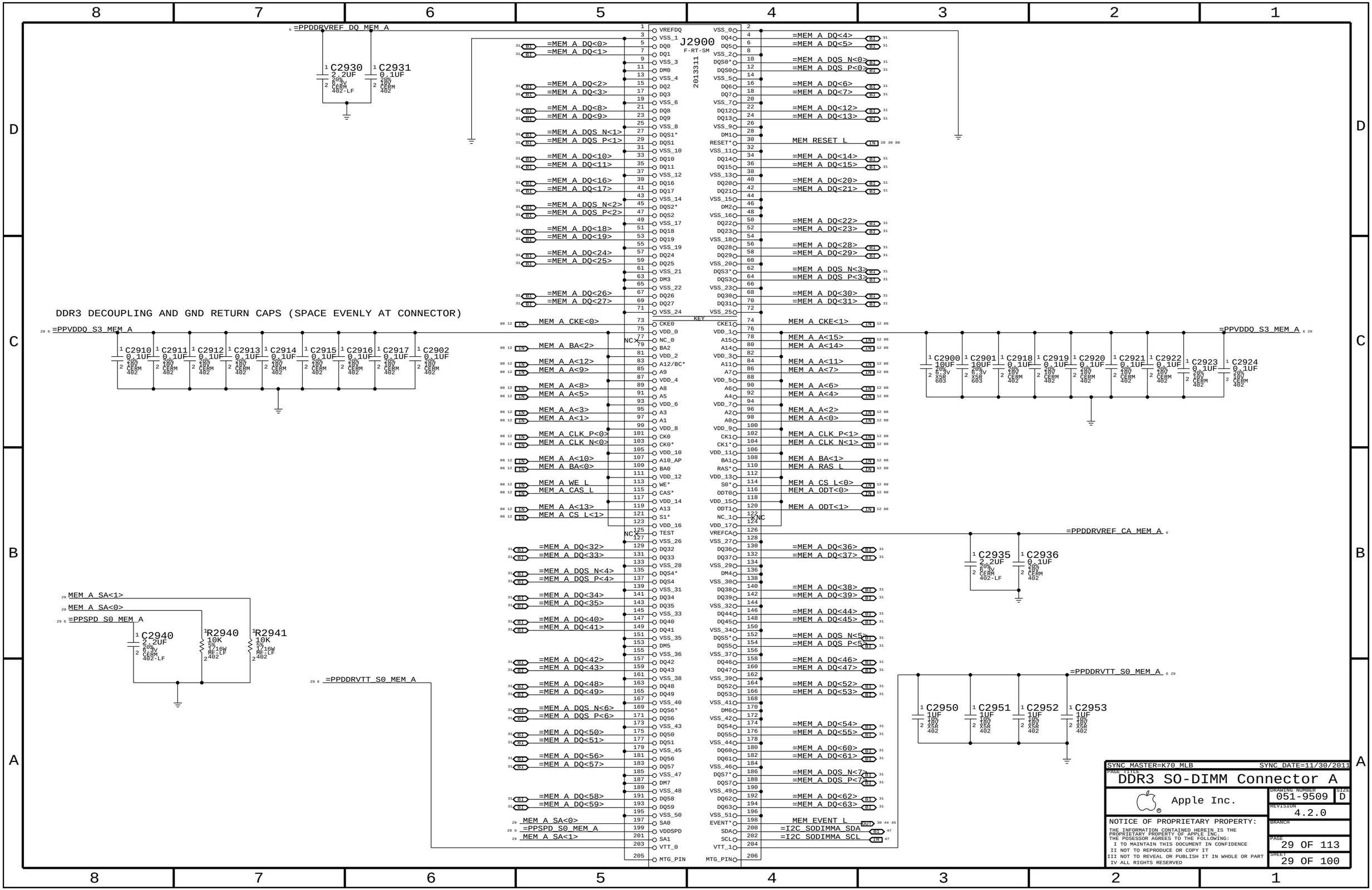
=PPDDRVREF_DQ_MEM_A
C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402
J2900 F-RT-SM
2013311
VREFDQ VSS_1 DQ0 DQ1 VSS_3 DM0 VSS_4 DQ2 DQ3 VSS_6 DQ8 DQ9 VSS_8 DQS1* DQS1 VSS_10 DQ10 DQ11 VSS_12 DQ16 DQ17 VSS_14 DQS2* DQS2 VSS_17 DQ18 DQ19 VSS_19 DQ24 DQ25 VSS_21 DM3 VSS_22 DQ26 DQ27 VSS_24
VSS_0 DQ4 DQ5 VSS_2 DQS0* DQS0 VSS_5 DQ6 DQ7 VSS_7 DQ12 DQ13 VSS_9 DM1 RESET* VSS_11 DQ14 DQ15 VSS_13 DQ20 DQ21 VSS_15 DM2 VSS_16 DQ22 DQ23 VSS_18 DQ28 DQ29 VSS_20 DQS3* DQS3 VSS_23 DQ30 DQ31 VSS_25
KEY
CKE0 VDD_0 NC_0 BA2 VDD_2 A12/BC* A9 VDD_4 A8 A5 VDD_6 A3 A1 VDD_8 CK0 CK0* VDD_10 A10_AP BA0 VDD_12 WE* CAS* VDD_14 A13 S1* VDD_16 TEST VSS_26 DQ32 DQ33 VSS_28 DQS4* DQS4 VSS_31 DQ34 DQ35 VSS_33 DQ40 DQ41 VSS_35 DM5 VSS_36 DQ42 DQ43 VSS_38 DQ48 DQ49 VSS_40 DQS6* DQS6 VSS_43 DQ50 DQ51 VSS_45 DQ56 DQ57 VSS_47 DM7 VSS_48 DQ58 DQ59 VSS_50 SA0 VDDSPD SA1 VTT_0 MTG_PIN
CKE1 VDD_1 A15 A14 VDD_3 A11 A7 VDD_5 A6 A4 VDD_7 A2 A0 VDD_9 CK1 CK1* VDD_11 BA1 RAS* VDD_13 S0* ODT0 VDD_15 ODT1 NC_1 VDD_17 VREFCA VSS_27 DQ36 DQ37 VSS_29 DM4 VSS_30 DQ38 DQ39 VSS_32 DQ44 DQ45 VSS_34 DQS5* DQS5 VSS_37 DQ46 DQ47 VSS_39 DQ52 DQ53 VSS_41 DM6 VSS_42 DQ54 DQ55 VSS_44 DQ60 DQ61 VSS_46 DQS7* DQS7 VSS_49 DQ62 DQ63 VSS_51 EVENT* SDA SCL VTT_1 MTG_PIN
=MEM_A_DQ<0> =MEM_A_DQ<1> =MEM_A_DQ<2> =MEM_A_DQ<3> =MEM_A_DQ<8> =MEM_A_DQ<9> =MEM_A_DQS_N<1> =MEM_A_DQS_P<1> =MEM_A_DQ<10> =MEM_A_DQ<11> =MEM_A_DQ<16> =MEM_A_DQ<17> =MEM_A_DQS_N<2> =MEM_A_DQS_P<2> =MEM_A_DQ<18> =MEM_A_DQ<19> =MEM_A_DQ<24> =MEM_A_DQ<25> =MEM_A_DQ<26> =MEM_A_DQ<27>
=MEM_A_DQ<4> =MEM_A_DQ<5> =MEM_A_DQS_N<0> =MEM_A_DQS_P<0> =MEM_A_DQ<6> =MEM_A_DQ<7> =MEM_A_DQ<12> =MEM_A_DQ<13> MEM_RESET_L =MEM_A_DQ<14> =MEM_A_DQ<15> =MEM_A_DQ<20> =MEM_A_DQ<21> =MEM_A_DQ<22> =MEM_A_DQ<23> =MEM_A_DQ<28> =MEM_A_DQ<29> =MEM_A_DQS_N<3> =MEM_A_DQS_P<3> =MEM_A_DQ<30> =MEM_A_DQ<31>
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NC NC
MEM_EVENT_L =I2C_SODIMMA_SDA =I2C_SODIMMA_SCL
=PPVDDQ_S3_MEM_A
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)
C2910 C2911 C2912 C2913 C2914 C2915 C2916 C2917 C2902 0.1UF 20% 10V CERM 402
C2900 C2901 10UF 20% 6.3V X5R 603
C2918 C2919 C2920 C2921 C2922 C2923 C2924 0.1UF 20% 10V CERM 402
=PPDDRVREF_CA_MEM_A
C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402
=PPSPD_S0_MEM_A
MEM_A_SA<1>
MEM_A_SA<0>
=PPSPD_S0_MEM_A
C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 R2941 10K 5% 1/16W MF-LF 402
=PPDDRVTT_S0_MEM_A
C2950 C2951 C2952 C2953 1UF 10% 10V X5R 402
SYNC_MASTER=K70_MLB
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PAGE TITLE
DDR3 SO-DIMM Connector A
Apple Inc.
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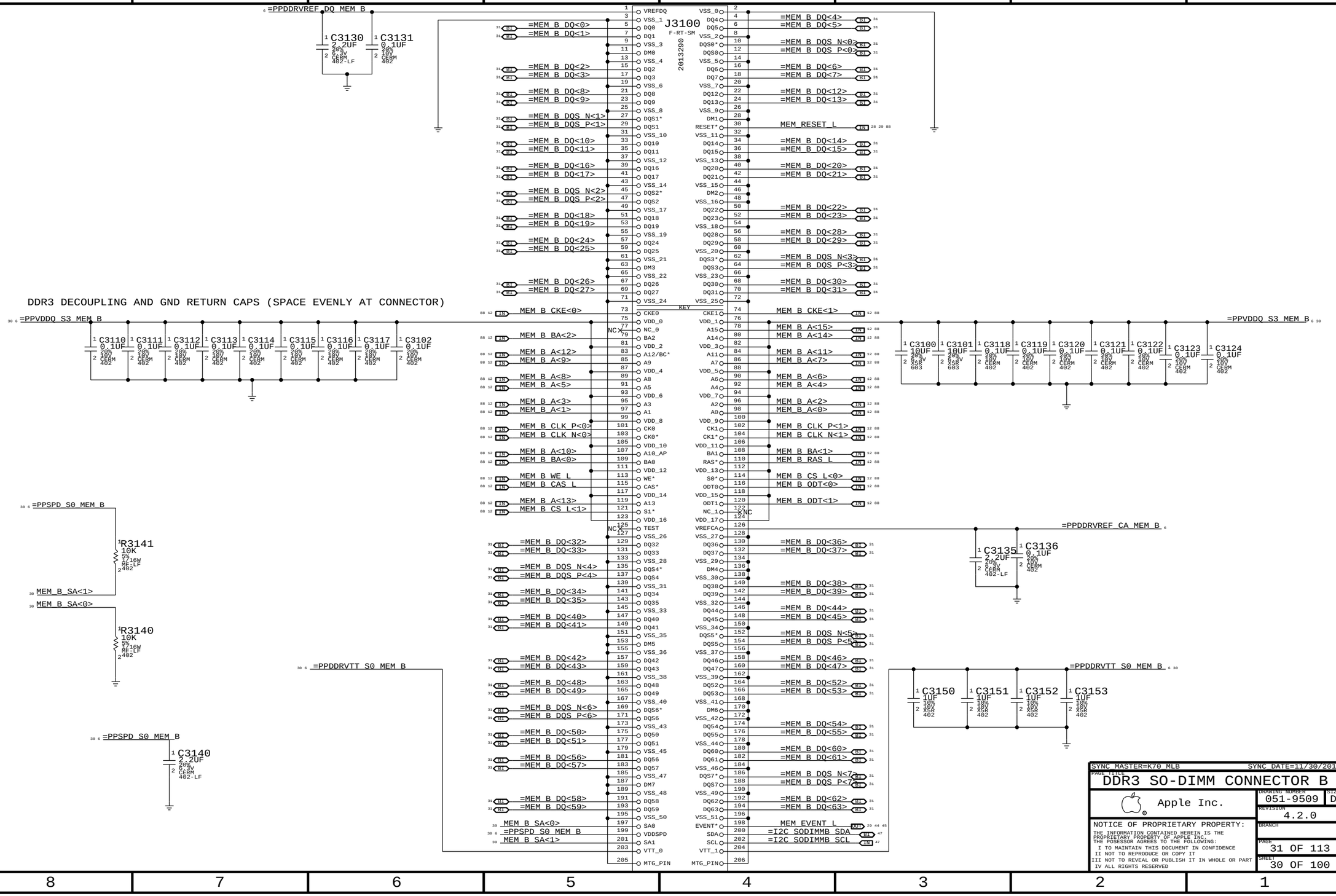
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)
J3100
F-RT-SM
20132900
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=PPVDDQ_S3_MEM_B
=PPDDRVREF_CA_MEM_B
=PPDDRVTT_S0_MEM_B
=PPSPD_S0_MEM_B
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MEM_RESET_L
MEM_EVENT_L
=I2C_SODIMMB_SDA
=I2C_SODIMMB_SCL
SYNC_MASTER=K70_MLB
SYNC_DATE=11/30/2011
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DDR3 SO-DIMM CONNECTOR B
Apple Inc.
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MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>		MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>		MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	
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MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>		MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	
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MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>		MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	
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MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>		MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>		MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>		MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	
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MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>		MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>		MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>		MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>		MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>		MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>		MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>		MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	
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MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>		MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>		MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>		MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<61>		MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<60>		MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	
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MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>		MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>		MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>		MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

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DDR3 ALIASES AND BITSWAPS

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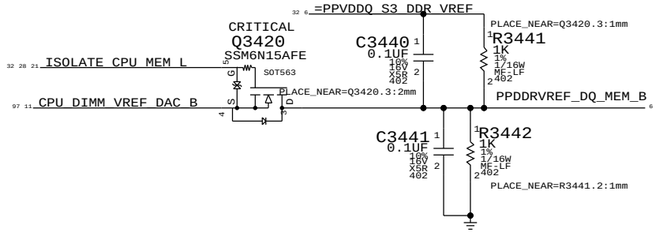
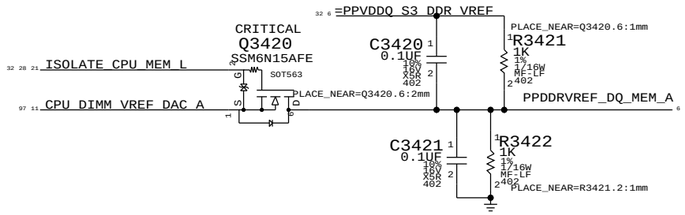
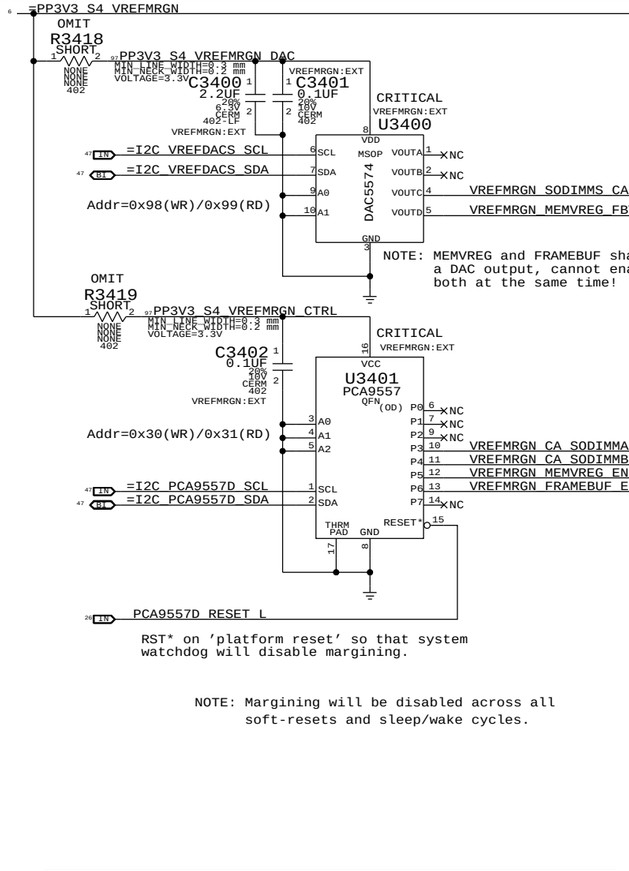
VRef DQ

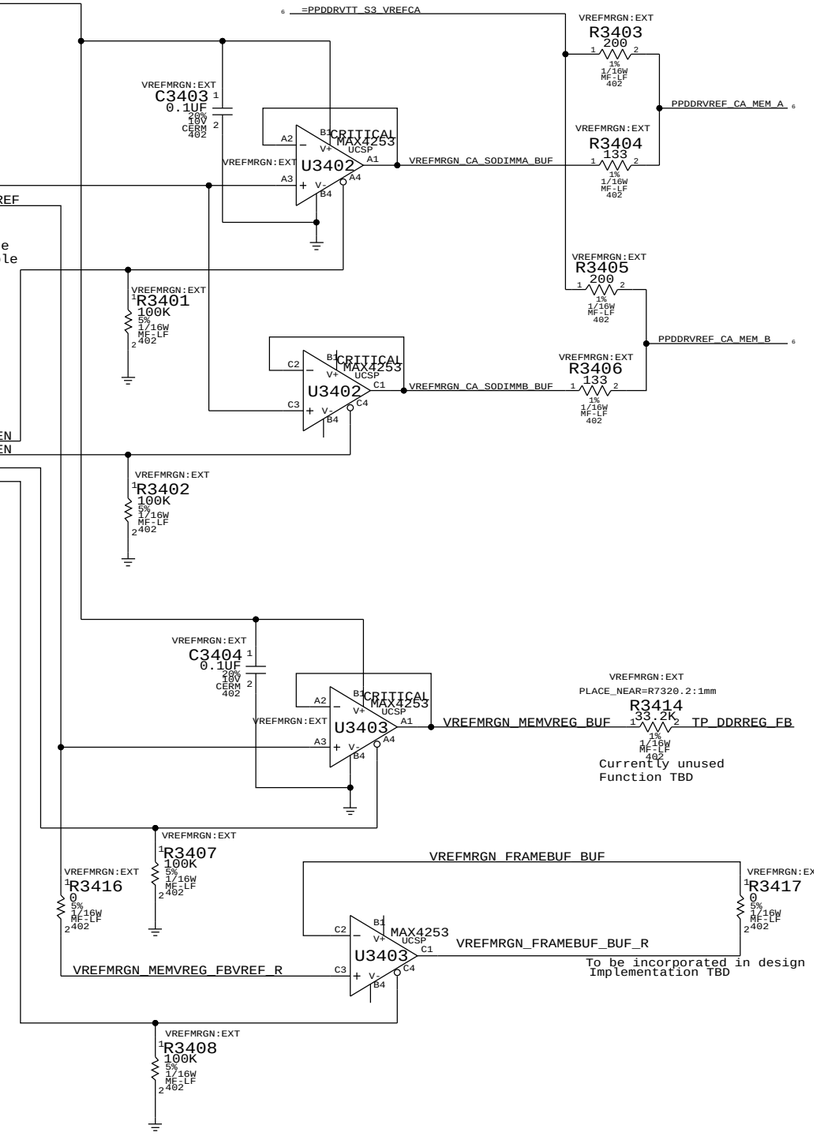
Driven by CPU

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step









PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FLM,0,5%,402,SM,LF	R3403,R3405		VREFMRGN:N

	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	C	C	D	D
PCA9557D Pin:	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)		1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)		0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)		+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

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DDR3/FRAMEBUF VREF MARGINING

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AIRPORT BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (EDP)

U3510 TPS22924B CSP
=PP3V3_S4_AP → A2 VIN, B2 VIN
AP_PWR_EN (IN) → C2 ON
VOUT A1, B1 → PP3V3_S4_AP_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
GND
C1 0.1UF 10% 16V X5R 402

L3502 CRITICAL 220-OHM-1.4A 0603
PP3V3_S4_AP_FET → PP3V3_S4_AP_FLT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3502 0.1UF 10% 16V X5R 402
C3503 0.1UF 10% 16V X5R 402
C3504 10UF 20% 6.3V X5R 603

514S0335 CRITICAL
J3500 SSD-K99 F-RT-SM1

PLACE_NEAR=J3500.4:3mm
C3505 0.1UF 10% X5R 6.3V 201
C3506 0.1UF 10% X5R 6.3V 201
PLACE_NEAR=J3500.5:3mm

PCIE_AP_R2D_C_N (IN) → C3505
PCIE_AP_R2D_C_P (IN) → C3506
AP_EVENT_L (BI)
PCIE_AP_R2D_N
PCIE_AP_R2D_P
PCIE_CLK100M_AP_N (IN)
PCIE_CLK100M_AP_P (IN)
PCIE_AP_D2R_P (OUT)
PCIE_AP_D2R_N (OUT)
AP_WAKE_L (OUT)
AP_RESET_CONN_L
AP_CLKREQ_Q_L (OUT)
USB_BT_MUX_N
USB_BT_MUX_P

U3540 TPS22924B CSP
=PP3V3_G3H_BT → A2 VIN, B2 VIN
C2 ON
VOUT A1, B1 → PP3V3_G3H_BT_FET
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
GND
C1 0.1UF 10% 16V X5R 402

L3501 CRITICAL 220-OHM-1.4A 0603
PP3V3_G3H_BT_FET → PP3V3_G3H_BT_FLT
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C3507 0.1UF 10% 16V X5R 402
C3508 10UF 20% 6.3V X5R 603

SMC_S4_WAKESRC_EN
R3542 10K 5% 1/16W MF-LF 402

CRITICAL
Q3540 SSM6L36FE SOT563 P-CH
D 3 → BT_PWR_RST
G 5 ← BT_PWR_RST_L (IN)
S 4 ← =PP3V3_S0_BT
D 6 → BT_PWR_EN
G 2 ← BT_PWR_RST
S 1
N-CH
R3543 10K 5% 1/16W MF-LF 402

Wake from BT in G3H circuit

SMC_PME_S4_WAKE_L (OUT)
Q3501 SSM3K15FV SOD-VESM-HF
R3500 15K 1% 1/20W MF 201
PP3V3_G3H_BT_FET
C3500 0.1UF 20% 16V CERM 402

U3501 USB3740 DFN
VDD
USB_BT_N (BI) → DP_2
USB_BT_P (BI) → DM_2
USB_BT_WAKEN → DP_1
USB_BT_WAKEP → DM_1
CRITICAL
DP → USB_BT_MUX_N
DM → USB_BT_MUX_P
OE* ← R3502 0 5% 1/16W MF-LF 402 ← PM_SLP_S5_L (IN)
S
GND
C3501 0.1UF 20% 16V CERM 402 NOSTUFF
R3501 15K 1% 1/20W MF 201

SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

Supervisor & CLKFREG # Isolation
Delay = 60 ms +/- 20%

PP3V3_S4_AP_FLT
=PP3V3_S4_AP
R3530 100K 1% 1/16W MF-LF 402
R3531 232K 1% 1/16W MF-LF 402
CRITICAL
C3530 0.1uF 20% 10V CERM 402
U3530 SLG4AP016V TDFN
VDD
P3V3AP_VMON → SENSE 0.7V
DLY
AP_RESET_CONN_L → RESET*
MR* → AP_RESET_L (IN)
EN ← AP_PWR_EN (IN)
AP_CLKREQ_Q_L → IN
OUT (OD) → AP_CLKREQ_L (OUT)
THRM PAD
GND
R3532 100K 1% 1/16W MF-LF 402

Q3570 SSM3K15FV SOD-VESM-HF
PP3V3_S4_AP_FLT → R3570 10K 5% 1/16W MF-LF 402
PCIE_WAKE_L → AP_WAKE_L

SYNC_MASTER=D7_NICK	SYNC_DATE=12/13/2011
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CRITICAL
OMIT_TABLE
U3600
CACTUSRIDGE4C
FCBGA
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PCIE GEN2

RECEIVE

PCIE_TBT_R2D_C_P<0>	C3600 0.1UF	PCIE_TBT_R2D_P<0>	AB9 PERP_0
PCIE_TBT_R2D_C_N<0>	C3601 0.1UF	PCIE_TBT_R2D_N<0>	AA10 PERN_0
PCIE_TBT_R2D_C_P<1>	C3602 0.1UF	PCIE_TBT_R2D_P<1>	AA12 PERP_1
PCIE_TBT_R2D_C_N<1>	C3603 0.1UF	PCIE_TBT_R2D_N<1>	AB13 PERN_1
PCIE_TBT_R2D_C_P<2>	C3604 0.1UF	PCIE_TBT_R2D_P<2>	AB15 PERP_2
PCIE_TBT_R2D_C_N<2>	C3605 0.1UF	PCIE_TBT_R2D_N<2>	AA16 PERN_2
PCIE_TBT_R2D_C_P<3>	C3606 0.1UF	PCIE_TBT_R2D_P<3>	AA18 PERP_3
PCIE_TBT_R2D_C_N<3>	C3607 0.1UF	PCIE_TBT_R2D_N<3>	AB19 PERN_3

TRANSMIT

PCIE_TBT_D2R_C_P<0>	C3640 0.1UF	PCIE_TBT_D2R_P<0>	AD5 PETP_0
PCIE_TBT_D2R_C_N<0>	C3641 0.1UF	PCIE_TBT_D2R_N<0>	AD7 PETN_0
PCIE_TBT_D2R_C_P<1>	C3642 0.1UF	PCIE_TBT_D2R_P<1>	AD9 PETP_1
PCIE_TBT_D2R_C_N<1>	C3643 0.1UF	PCIE_TBT_D2R_N<1>	AD11 PETN_1
PCIE_TBT_D2R_C_P<2>	C3644 0.1UF	PCIE_TBT_D2R_P<2>	AD13 PETP_2
PCIE_TBT_D2R_C_N<2>	C3645 0.1UF	PCIE_TBT_D2R_N<2>	AD15 PETN_2
PCIE_TBT_D2R_C_P<3>	C3646 0.1UF	PCIE_TBT_D2R_P<3>	AD17 PETP_3
PCIE_TBT_D2R_C_N<3>	C3647 0.1UF	PCIE_TBT_D2R_N<3>	AD19 PETN_3

MISC

=PP3V3_S4_TBT
R3610 47K 5% 1/16W MF-LF 402

TBT_PCIE_RESET_L	R6	PERST_N
TBT_PWR_ON_POC_RST_L	J2	PWR_ON_POC_RST_N
TP_TBT_MONDC0	AD23	MONDC0
TP_TBT_MONDC1	AC24	MONDC1
TBT_MONOBSP	W18	MONOBS_P
TBT_MONOBSN	W16	MONOBS_N
TP_TBT_THERM_DP	Y7	THERMDA
TBT_SPI_MOSI	R4	EE_DI
TBT_SPI_MISO	P5	EE_DO
TBT_SPI_CS_L	AD3	EE_CS_N
TBT_SPI_CLK	W4	EE_CLK

NO STUFF C3610 0.1UF 10% 16V X5R 402

OMIT R3615 NOSTUFF NONE NONE NONE 402

DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
Use AA8 GND ball for THERM_DN

EEPROM

R3690 3.3K 5% 1/16W MF-LF 402
R3691 3.3K 5% 1/16W MF-LF 402
C3690 1UF 10% 6.3V CERM 402
R3692 3.3K 5% 1/16W MF-LF 402
R3693 3.3K 5% 1/16W MF-LF 402

CRITICAL
OMIT_TABLE
U3690 M95256-RMC6XG MLP

(TBT_SPI_MOSI)	D	
(TBT_SPI_CLK)	C	
(TBT_SPI_CS_L)	S*	
TBTROM_WP_L	W*	
TBTROM_HOLD_L	HOLD*	
	Q	(TBT_SPI_MISO)
	VCC	
	VSS	
	THM PAD	

JTAG_TBT_TDI	V1	TDI
JTAG_TBT_TMS	AB3	TMS
JTAG_TBT_TCK	AA6	TCK
JTAG_TBT_TDO	R2	TDO
TBT_TEST_EN	N4	TEST_EN
TBT_TEST_PWR_GOOD	AB5	TEST_PWR_GOOD

JTAG/TEST PORT

R3625 0 5% 1/16W MF-LF 402
R3629 0 5% 1/16W MF-LF 402

RSENSE U20 TBT_RSENSE
RBIAS W20 TBT_RBIAS
R3655 1K 1% 1/20W MF 201
NC U4 NC

Not used in host mode.

PCIE RESET

PCIE_RST_0_N	N6	TP_TBT_PCIE_RESET0_L
PCIE_RST_1_N	T1	TP_TBT_PCIE_RESET1_L
PCIE_RST_2_N	Y5	TP_TBT_PCIE_RESET2_L
PCIE_RST_3_N	U2	TP_TBT_PCIE_RESET3_L

PCIE_CLKREQ_OD_N	W6	=TBT_CLKREQ_L
EN_LC_PWR	K5	TBT_EN_LC_PWR

CLOCKS

REFCLK_100_IN_P	AB21	PCIE_CLK100M_TBT_P
REFCLK_100_IN_N	AD21	PCIE_CLK100M_TBT_N
XTAL_25_IN	AA24	SYSCLK_CLK25M_TBT_R
XTAL_25_OUT	AB23	TP_TBT_XTAL25OUT
TMU_CLK_OUT	AA4	TBT_TMU_CLK_OUT
TMU_CLK_IN	Y3	TBT_TMU_CLK_IN

=PP3V3_TBTLC_RTR
R3698 10K 5% 1/16W MF-LF 402
R3695 806 1% 1/16W MF-LF 402
SYSCLK_CLK25M_TBT
Divides 3.3V to 1.8V

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

DISPLAYPORT

SINK PORT 0

DP_TBTSNK0_ML_P<3>	E14	DPSNK0_3_P
DP_TBTSNK0_ML_N<3>	D13	DPSNK0_3_N
DP_TBTSNK0_ML_P<2>	E16	DPSNK0_2_P
DP_TBTSNK0_ML_N<2>	D15	DPSNK0_2_N
DP_TBTSNK0_ML_P<1>	E18	DPSNK0_1_P
DP_TBTSNK0_ML_N<1>	D17	DPSNK0_1_N
DP_TBTSNK0_ML_P<0>	E20	DPSNK0_0_P
DP_TBTSNK0_ML_N<0>	D19	DPSNK0_0_N
DP_TBTSNK0_AUXCH_P	A6	DPSNK0_AUX_P
DP_TBTSNK0_AUXCH_N	B5	DPSNK0_AUX_N
DP_TBTSNK0_HPD	U6	DPSNK0_HPD

SINK PORT 1

DP_TBTSNK1_ML_P<3>	E6	DPSNK1_3_P
DP_TBTSNK1_ML_N<3>	D5	DPSNK1_3_N
DP_TBTSNK1_ML_P<2>	E8	DPSNK1_2_P
DP_TBTSNK1_ML_N<2>	D7	DPSNK1_2_N
DP_TBTSNK1_ML_P<1>	E10	DPSNK1_1_P
DP_TBTSNK1_ML_N<1>	D9	DPSNK1_1_N
DP_TBTSNK1_ML_P<0>	E12	DPSNK1_0_P
DP_TBTSNK1_ML_N<0>	D11	DPSNK1_0_N
DP_TBTSNK1_AUXCH_P	A4	DPSNK1_AUX_P
DP_TBTSNK1_AUXCH_N	B3	DPSNK1_AUX_N
DP_TBTSNK1_HPD	T5	DPSNK1_HPD

R3630 100K 5% 1/16W MF-LF 402
R3631 100K 5% 1/16W MF-LF 402

SOURCE PORT 0

DPSRC_3_P	A14	TP_DP_TBTSRC_ML_CP<3>
DPSRC_3_N	B15	TP_DP_TBTSRC_ML_CN<3>
DPSRC_2_P	A12	TP_DP_TBTSRC_ML_CP<2>
DPSRC_2_N	B13	TP_DP_TBTSRC_ML_CN<2>
DPSRC_1_P	A10	TP_DP_TBTSRC_ML_CP<1>
DPSRC_1_N	B11	TP_DP_TBTSRC_ML_CN<1>
DPSRC_0_P	A8	TP_DP_TBTSRC_ML_CP<0>
DPSRC_0_N	B9	TP_DP_TBTSRC_ML_CN<0>
DPSRC_AUX_P	C2	TP_DP_TBTSRC_AUXCH_CP
DPSRC_AUX_N	D3	TP_DP_TBTSRC_AUXCH_CN
DPSRC_HPD_OD	V3	DP_TBTSRC_HPD

R3632 100K 5% 1/16W MF-LF 402

GPIO_2/GO2SX	Y1	TBT_GO2SX_BIDIR
(FORCE_PWR) GPIO_3	W2	TBT_PWR_EN
GPIO_4/WAKE_N_OD	J4	=TBT_WAKE_L
GPIO_5/CIO_PLUG_EVENT	AA2	TBT_CIO_PLUG_EVENT
GPIO_6/CIO_SDA_OD	AB1	=I2C_TBTRTR_SDA
GPIO_7/CIO_SCL_OD	AC2	=I2C_TBTRTR_SCL
GPIO_8/EN_CIO_PWR_OD*	P3	(TBT_EN_CIO_PWR_L)
GPIO_9/OK2GO2SX_OD*	H5	TBT_GPIO_9
GPIO_14	T3	TBT_GPIO_14
GPIO_15	V5	TBT_DDC_XBAR_EN_L

TBT_PWR_REQ_L
TBT_EN_CIO_PWR_L
MAKE_BASE=TRUE

R3696 1K 5% 1/16W MF-LF 402
R3697 100K 5% 1/16W MF-LF 402
NO STUFF R3699 10K 5% 1/16W MF-LF 402
R3680 10K 5% 1/16W MF-LF 402

TBT_DDC_XBAR_EN_L
TBT_GO2SX_BIDIR
R3681 for CYA, allows separation of GPIO_2/GPIO_9 if necessary. Stuff one of R3861/2.
R3681 0 5% 1/16W MF-LF 402
TBT_GPIO_9
TBT_GPIO_14
R3683 10K 5% 1/16W MF-LF 402
NO STUFF R3682 10K 5% 1/16W MF-LF 402

=PP3V3_S4_TBT
R3685 10K 5% 1/16W MF-LF 402
R3686 10K 5% 1/16W MF-LF 402
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
R3688 10K 5% 1/16W MF-LF 402
R3687 10K 5% 1/16W MF-LF 402

PORT0

TBT_A_R2D_C_P<0>	G24	PA_CIO0_TX_P/DP_SRC_0_P
TBT_A_R2D_C_N<0>	E24	PA_CIO0_TX_N/DP_SRC_0_N
TBT_A_D2R_P<0>	G22	PA_CIO0_RX_P
TBT_A_D2R_N<0>	E22	PA_CIO0_RX_N
TBT_A_CONFIG1_BUF	K1	PA_CONFIG1/CIO_0_LSEO
TBT_A_CONFIG2_RC	G4	PA_CONFIG2/CIO_0_LSOE

PORT1

TBT_A_R2D_C_P<1>	L24	PA_CIO1_TX_P/DP_SRC_2_P
TBT_A_R2D_C_N<1>	J24	PA_CIO1_TX_N/DP_SRC_2_N
TBT_A_D2R_P<1>	L22	PA_CIO1_RX_P
TBT_A_D2R_N<1>	J22	PA_CIO1_RX_N
TBT_A_LSTX	N2	PA_LSTX/CIO_1_LSEO
TBT_A_LSRX	J6	PA_LSRX/CIO_1_LSOE

PORT2

TBT_B_R2D_C_P<0>	R24	PB_CIO2_TX_P/DP_SRC_0_P
TBT_B_R2D_C_N<0>	N24	PB_CIO2_TX_N/DP_SRC_0_N
TBT_B_D2R_P<0>	R22	PB_CIO2_RX_P
TBT_B_D2R_N<0>	N22	PB_CIO2_RX_N
TBT_B_CONFIG1_BUF	P1	PB_CONFIG1/CIO_2_LSEO
TBT_B_CONFIG2_RC	H5	PB_CONFIG2/CIO_2_LSOE

PORT3

TBT_B_R2D_C_P<1>	W24	PB_CIO3_TX_P/DP_SRC_2_P
TBT_B_R2D_C_N<1>	U24	PB_CIO3_TX_N/DP_SRC_2_N
TBT_B_D2R_P<1>	W22	PB_CIO3_RX_P
TBT_B_D2R_N<1>	U22	PB_CIO3_RX_N
TBT_B_LSTX	L6	PB_LSTX/CIO_3_LSEO
TBT_B_LSRX	G6	PB_LSRX/CIO_3_LSOE

PORTS

DP_TBTPA_ML_C_P<1>	A16	PA_DPSRC_1_P
DP_TBTPA_ML_C_N<1>	B17	PA_DPSRC_1_N
DP_TBTPA_ML_C_P<3>	A18	PA_DPSRC_3_P
DP_TBTPA_ML_C_N<3>	B19	PA_DPSRC_3_N
DP_TBTPA_AUXCH_C_P	F3	PA_AUX_P
DP_TBTPA_AUXCH_C_N	F1	PA_AUX_N
DP_TBTPA_HPD	H1	PA_DPSRC_HPD
TBT_A_HV_EN	G2	GPIO_0/PA_HV_EN/BYP0
TBT_A_CIO_SEL	M3	GPIO_10/PA_CIO_SEL/BYP1
TBT_A_DP_PWRDN	H3	GPIO_12/PA_DP_PWRDN/BYP2

DP_TBTPB_ML_C_P<1>	A20	PB_DPSRC_1_P
DP_TBTPB_ML_C_N<1>	B21	PB_DPSRC_1_N
DP_TBTPB_ML_C_P<3>	A22	PB_DPSRC_3_P
DP_TBTPB_ML_C_N<3>	B23	PB_DPSRC_3_N
DP_TBTPB_AUXCH_C_P	D1	PB_AUX_P
DP_TBTPB_AUXCH_C_N	E2	PB_AUX_N
DP_TBTPB_HPD	K3	PB_DPSRC_HPD
TBT_B_HV_EN	M1	GPIO_1/PB_HV_EN/BYP0
TBT_B_CIO_SEL	L2	GPIO_11/PB_CIO_SEL/BYP1
TBT_B_DP_PWRDN	L4	GPIO_13/PB_DP_PWRDN/BYP2

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C3620 0.1UF	DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0>	C3621 0.1UF	DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1>	C3622 0.1UF	DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1>	C3623 0.1UF	DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2>	C3624 0.1UF	DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2>	C3625 0.1UF	DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3>	C3626 0.1UF	DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3>	C3627 0.1UF	DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P	C3628 0.1UF	DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N	C3629 0.1UF	DP_TBTSNK0_AUXCH_N

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C3630 0.1UF	DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0>	C3631 0.1UF	DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1>	C3632 0.1UF	DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1>	C3633 0.1UF	DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2>	C3634 0.1UF	DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2>	C3635 0.1UF	DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3>	C3636 0.1UF	DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3>	C3637 0.1UF	DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P	C3638 0.1UF	DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N	C3639 0.1UF	DP_TBTSNK1_AUXCH_N

SYNC_MASTER=D7_DOUG SYNC_DATE=01/11/2012

PAGE TITLE: Thunderbolt Host (1 of 2)

Apple Inc.

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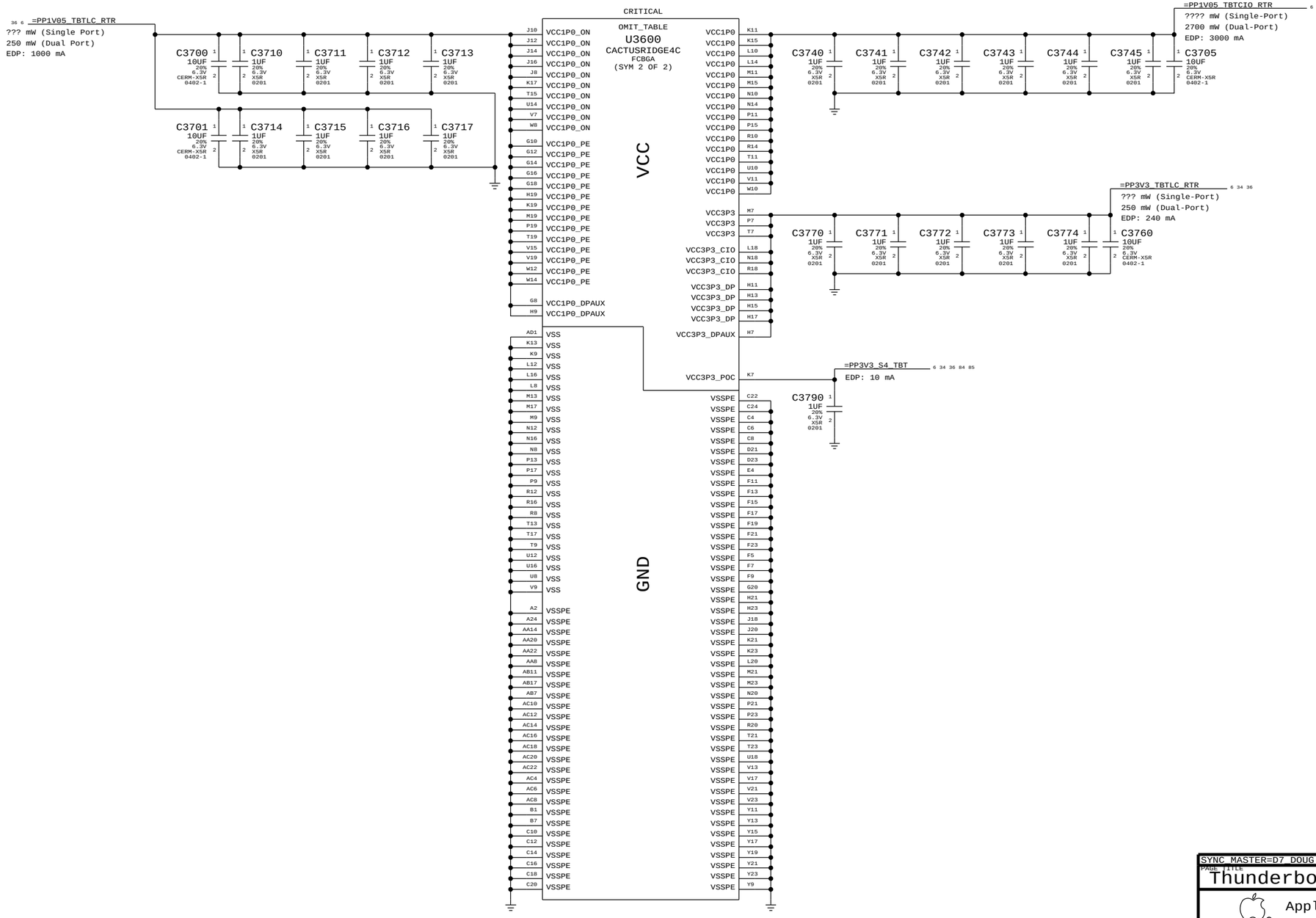

EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC_MASTER=D7_DOUG SYNC_DATE=01/11/2012

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

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REVISION: 4.2.0

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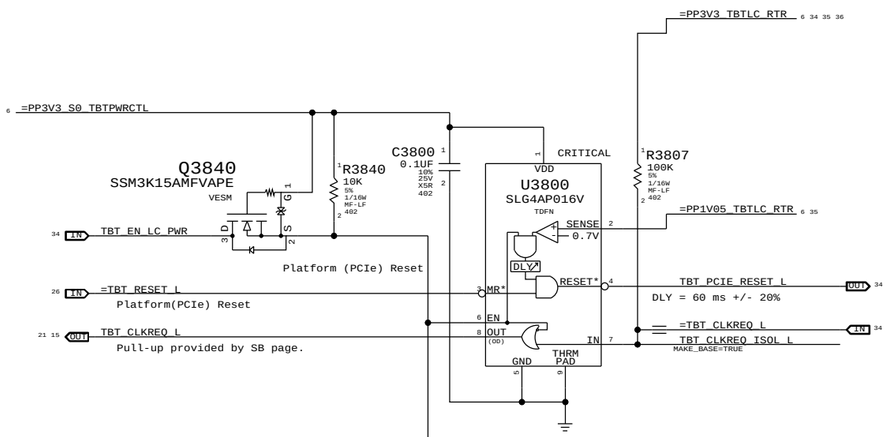
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

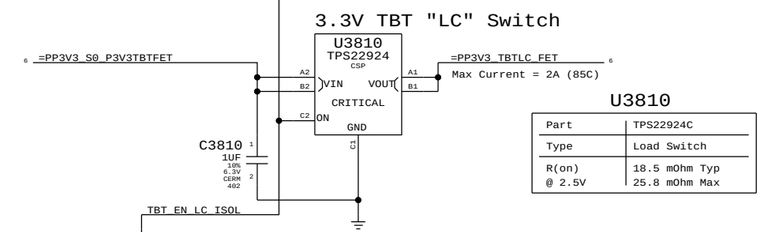
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Supervisor & CLKREQ# Isolation

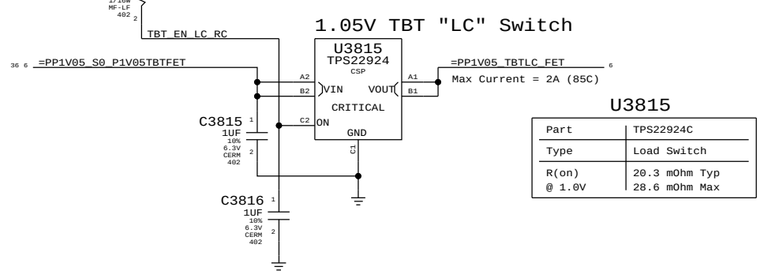


3.3V TBT "LC" Switch



U3810	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

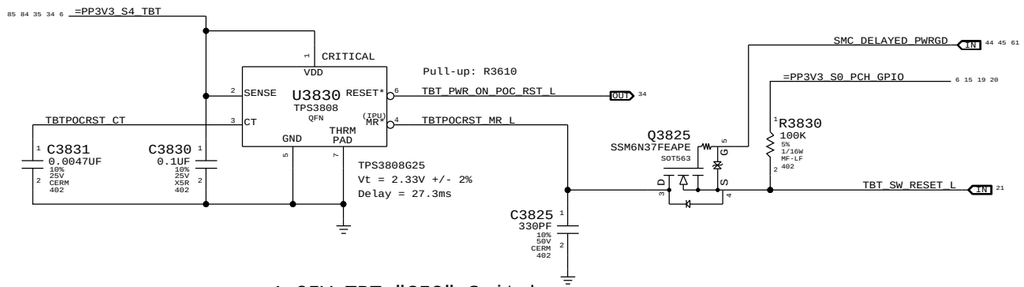
1.05V TBT "LC" Switch



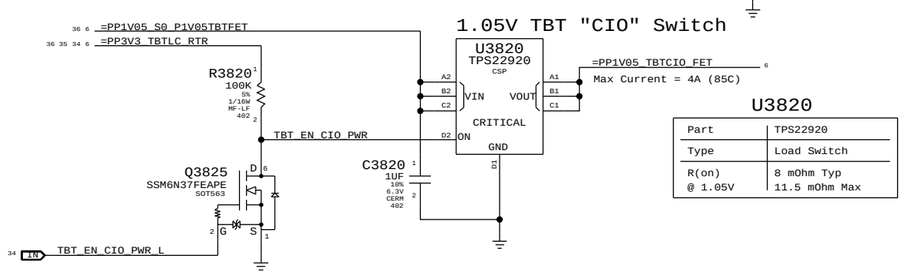
U3815	
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



U3820	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=D7_DOUG SYNC_DATE=01/11/2012

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Thunderbolt Power Support

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3900 0.1UF 10% 10V X5R-CERM 0201
ENET_XTALVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
PP3V3_ENET_PHY_BIASVDDH
C3905 0.1UF 10% 10V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
PP3V3_ENET_PHY_AVDDH
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 10V X5R-CERM 0201
C3911 0.1UF 10% 10V X5R-CERM 0201

VDD for Card Reader I/O
PP3V3R1V8_CR_VDDIO MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.15 mm VOLTAGE=3.3V

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM-1 402
C3916 0.1UF 10% 10V X5R-CERM 0201

ENET_SR_LX
ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_AVDDL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3921 0.1UF 10% 10V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3926 0.1UF 10% 10V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_GPHYPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.15 mm VOLTAGE=1.2V
C3931 0.1UF 10% 10V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 10V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

AVDDH BIASVDDH XTALVDDH VDDO SR_VDD SR_VDDP SR_LX SR_VFB AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC

OMIT_TABLE
U3900 BCM57766C0KMLG QFN-8X8

=PP3V3_S0_ENET
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1UF 10% 10V X5R-CERM 0201
C3951 0.1UF 10% 10V X5R-CERM 0201
C3955 0.1UF 10% 10V X5R-CERM 0201
C3956 0.1UF 10% 10V X5R-CERM 0201

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N

ENET_VMAIN_PRSNT → VMAIN_PRSNT (IPD-ENET)
PCIE_ENET_D2R_C_N → PCIE_TXD_N
PCIE_ENET_D2R_C_P → PCIE_TXD_P
PCIE_ENET_R2D_P → PCIE_RXD_P
PCIE_ENET_R2D_N → PCIE_RXD_N
PCIE_CLK100M_ENET_P → PCIE_REFCLK_P
PCIE_CLK100M_ENET_N → PCIE_REFCLK_N
ENET_RESET_L → PERST* (IPD)
ENET_CLKREQ_L → CLKREQ* (OD)
=ENET_WAKE_L (See note) → WAKE* (OD)
ENET_LOW_PWR → LOW_PWR (IPD)
SMB_ENET_SCL → SMB_CLK
SMB_ENET_SDA → SMB_DATA (IPD-ENETM)
ENET_SCLK → SCLK_SPD1000LED*
ENET_MISO → SI/EEDATA
ENET_MOSI → SO_LINKLED*
ENET_CS_L → CS*/EECLK (IPU)
ENET_CR_3V3_EN_L → SPD100LED*/SERIAL_DO (OD)
ENET_TRAFFICLED_L → TRAFFICLED*/SERIAL_DI (OD)
SYSCLK_CLK25M_ENET → XTALI
NC → XTALO
ENET_RDAC → RDAC
THRM_PAD

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

R3965 1.24K 1% 1/16W MF-LF 402

NOTE: "IPx" == Programmable pull-up/down (IPx-ENET)
SD_DETECT can only be used active low due to errata.

GPIO_0/CR_ACT_LED* (IPD) → ENET_CR_1V8_EN
GPIO_1/LR_OUT → PP3V3R1V8_ENET_LR_OUT MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.15 mm VOLTAGE=3.3V
GPIO_2/MEDIA_SENSE → ENET_MEDIA_SENSE
SD_DETECT* (IPU-ENET) → ENET_SD_DETECT_L

CR_CMD → ENET_SD_CMD → R3961 33 5% 1/20W MF 201 → SDCONN_CMD
CR_CLK → ENET_SD_CLK → R3979 33 5% 1/20W MF 201 → SDCONN_CLK
CR_DATA0 → ENET_CR_DATA<0> → R3971 33 5% 1/20W MF 201 → SDCONN_DATA<0>
CR_DATA1 → ENET_CR_DATA<1> → R3972 33 5% 1/20W MF 201 → SDCONN_DATA<1>
CR_DATA2 → ENET_CR_DATA<2> → R3973 33 5% 1/20W MF 201 → SDCONN_DATA<2>
CR_DATA3 → ENET_CR_DATA<3> → R3974 33 5% 1/20W MF 201 → SDCONN_DATA<3>
CR_DATA4 → ENET_CR_DATA<4> → R3975 33 5% 1/20W MF 201 → SDCONN_DATA<4>
CR_DATA5 → ENET_CR_DATA<5> → R3976 33 5% 1/20W MF 201 → SDCONN_DATA<5>
CR_DATA6 → ENET_CR_DATA<6> → R3977 33 5% 1/20W MF 201 → SDCONN_DATA<6>
CR_DATA7 → ENET_CR_DATA<7> → R3978 33 5% 1/20W MF 201 → SDCONN_DATA<7>
(IPU-ENET)

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

MS_INS* (IPU-ENET) → NC
CR_LED*/CR_BUS_PWR (IPU-ENET) → ENET_CR_PWREN
CR_WP* (IPU-ENET) → SDCONN_WP
SR_DISABLE (NO IPU OR IPD-ENET) → ENET_SR_DISABLE (See note) → R3981 1K 5% 1/16W MF-LF 402

ENET 1.2V SR IS ENABLED IF FLOATING.
ENET supports both active-levels for WP.

ENETCONN_MDI P<0> TRD0_P 40
ENETCONN_MDI N<0> TRD0_N 41
ENETCONN_MDI P<1> TRD1_P 44
ENETCONN_MDI N<1> TRD1_N 43
ENETCONN_MDI P<2> TRD2_P 46
ENETCONN_MDI N<2> TRD2_N 47
ENETCONN_MDI P<3> TRD3_P 50
ENETCONN_MDI N<3> TRD3_N 49

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_ENET_PHY
C3990 0.1UF 10% 10V X5R-CERM 0201
U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC SCK CS* WP* RESET* SI SO GND
ENET_SCLK
ENET_CS_L
ENET_MOSI
ENET_MISO
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=D7_NICK SYNC_DATE=01/12/2012
PAGE TITLE: ETHERNET PHY (CAESAR IV)
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CAESAR IV 1.2V INT.VR CMPTS

38 37 6 =PP3V3_ENET_PHY

Power decoupling

C4010 4.7UF 20% 6.3V X5R-CERM1 402

C4011 0.1UF 10% 16V X5R 402

37 ENET_SR_LX

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE

L4010 4.7UH-0.8A PCAA031B-SM

Feedback loop

C4012 10UF 20% 6.3V X5R 603

C4013 0.1UF 10% 16V X5R 402

PP1V2_ENET_INTREG 38

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V

38 PP1V2_ENET_INTREG
MAKE_BASE=TRUE

=PP1V2_ENET_PHY 37

ENET_SR_VFB 37

ENET Enable Generation

"ENET" = "S0" || ("S3/S5" && "WOL_EN")

21 15 IN WOL_EN

60 45 44 28 19 15 IN PM_SLP_S3_L

Q4021 2N7002DW-X-G SOT-363

Q4021 2N7002DW-X-G SOT-363

PM_EN_ENET_L

R4020 10K 5% 1/16W MF-LF 402

R4021 100K 5% 1/16W MF-LF 402

3.3V ENET FET

CRITICAL
Q4020 NTR4101P SOT-23-HF

6 =PP3V3_S4_FET_ENET

P3V3ENET_SS

C4020 0.033UF 10% 16V X5R 402

C4021 0.01UF 10% 50V X7R 402

PP3V3_ENET_FET 6

CAESAR IV ACTIVITY LED

38 37 6 =PP3V3_ENET_PHY

DEVELOPMENT
R4050 330 5% 1/16W MF-LF 402

ENET_ACT

DEVELOPMENT
LED3850 GREEN-3.6MCD 2.0X1.25MM-SM

SILKSCREEN:ENET ACT

37 ENET_TRAFFICLED_L

CAESAR IV WAKE# ISOLATION

=PP3V3_ENET_PHY 6 37 38

Q4070 SSM3K15AMFVAPE VESM

R4070 10K 5% 1/16W MF-LF 402

33 19 PCIE_WAKE_L

ENET_WAKE_L
MAKE_BASE=TRUE

=ENET_WAKE_L 37

38 =PP3V3_S4_ENET_FET

6 =PP1V8_S0_ENET

38 37 ENET_CR_3V3_EN_L

OMIT_TABLE
UFET-1.60X1.60 FDME1024NZT Q4030

38 37 ENET_CR_1V8_EN

UFET-1.60X1.60 FDME1024NZT Q4030

PP3V3R1V8_CR_FET
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.15MM
VOLTAGE=3.3V

R4030 0 5% 1/16W MF-LF 402

NOSTUFF
R4031 0 5% 1/16W MF-LF 402

37 PP3V3R1V8_ENET_LR_OUT

PP3V3R1V8_CR_VDDIO 37

C4030 4.7UF 20% 6.3V X5R-CERM2 402

C4031 0.1UF 10% 16V X5R-CERM 0201

C4032 0.1UF 10% 16V X5R-CERM 0201

38 =PP3V3_S4_ENET_FET

R4032 10K 5% 1/20W MF 201

R4033 10K 5% 1/20W MF 201

38 37 ENET_CR_3V3_EN_L

38 37 ENET_CR_1V8_EN

157S0058
CRITICAL
T4000 SM

93 37 B1 ENETCONN_MDI_P<1> 1
93 37 B1 ENETCONN_MDI_N<1> 2
3
TX
LFE8904CF
4
93 37 B1 ENETCONN_MDI_P<3> 5
93 37 B1 ENETCONN_MDI_N<3> 6
RX

12 ENETCONN_MDI_T_P<1> 38 93 B1
11 ENETCONN_MDI_T_N<1> 38 93 B1
10 ENETCONN_MCT1
9 ENETCONN_MCT3
8 ENETCONN_MDI_T_P<3> 38 93 B1
7 ENETCONN_MDI_T_N<3> 38 93 B1

CRITICAL
T4010 SM

93 37 B1 ENETCONN_MDI_N<2> 1
93 37 B1 ENETCONN_MDI_P<2> 2
3
TX
LFE8904CF
4
93 37 B1 ENETCONN_MDI_N<0> 5
93 37 B1 ENETCONN_MDI_P<0> 6
RX

12 ENETCONN_MDI_T_N<2> 38 93 B1
11 ENETCONN_MDI_T_P<2> 38 93 B1
10 ENETCONN_MCT2
9 ENETCONN_MCT0
8 ENETCONN_MDI_T_N<0> 38 93 B1
7 ENETCONN_MDI_T_P<0> 38 93 B1

ENETCONN_TCT

C4001 0.1UF 20% 10V CERM 402

C4002 0.1UF 20% 10V CERM 402

C4003 0.1UF 20% 10V CERM 402

C4004 0.1UF 20% 10V CERM 402

R4000 75 5% 1/16W MF-LF 402

R4001 75 5% 1/16W MF-LF 402

R4002 75 5% 1/16W MF-LF 402

R4003 75 5% 1/16W MF-LF 402

93 ENETCONN_MCT_BS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm

NOSTUFF
C4000 1000PF 10% 2KV CERM 1206

514-0822
CRITICAL
J4000 K70-K72 F-ANG-TH

93 38 B1 ENETCONN_MDI_T_N<3> 8 ENET_MDI_TRAN3-
93 38 B1 ENETCONN_MDI_T_P<3> 7 ENET_MDI_TRAN3+
93 38 B1 ENETCONN_MDI_T_N<1> 6 ENET_MDI_TRAN1-
93 38 B1 ENETCONN_MDI_T_N<2> 5 ENET_MDI_TRAN2-
93 38 B1 ENETCONN_MDI_T_P<2> 4 ENET_MDI_TRAN2+
93 38 B1 ENETCONN_MDI_T_P<1> 3 ENET_MDI_TRAN1+
93 38 B1 ENETCONN_MDI_T_N<0> 2 ENET_MDI_TRAN0-
93 38 B1 ENETCONN_MDI_T_P<0> 1 ENET_MDI_TRAN0+

ENET_MDI

9
10
11
12
13
14
SHIELD PINS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S1092	1	MOSFET,COMP N-/P-CH,20V,3.8/2.6A	Q4030	CRITICAL	

SYNC_MASTER=D7_NICK SYNC_DATE=01/12/2012

PAGE TITLE
Ethernet Support & Connector

Apple Inc.

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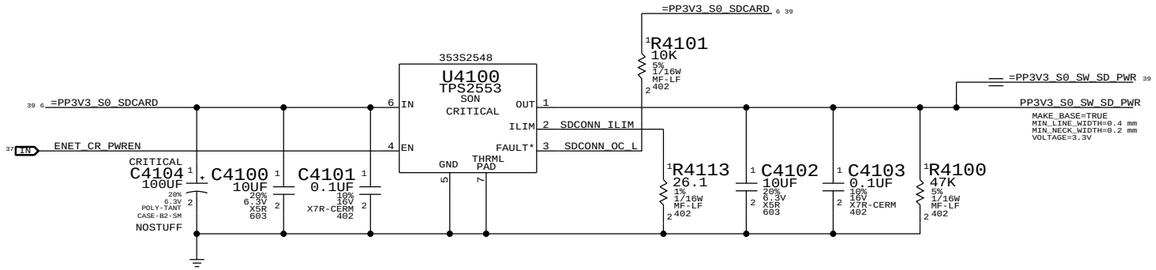
SD CARD 3.3V OVERCURRENT PROTECTION CHIP



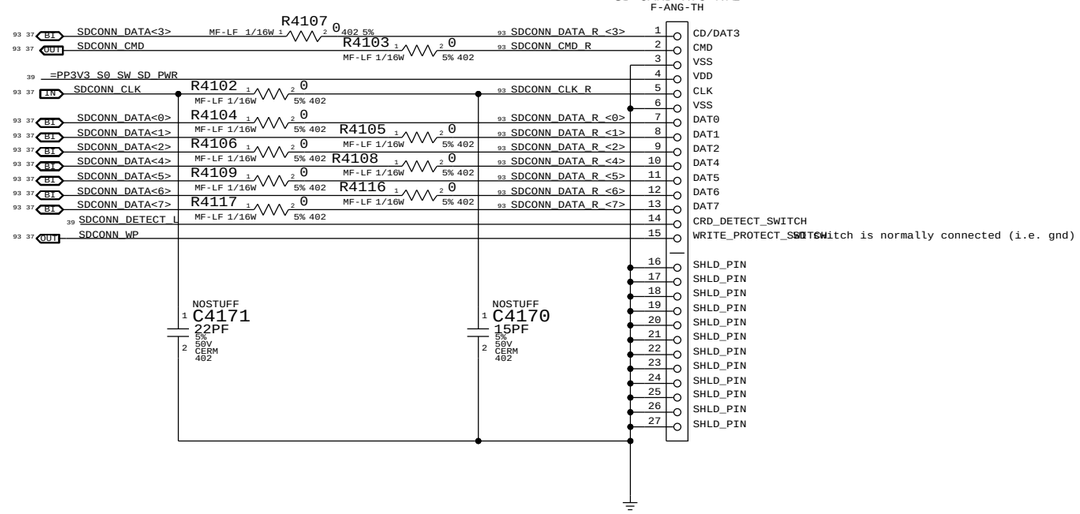
516-0249

SD CARD CONNECTOR

J4100

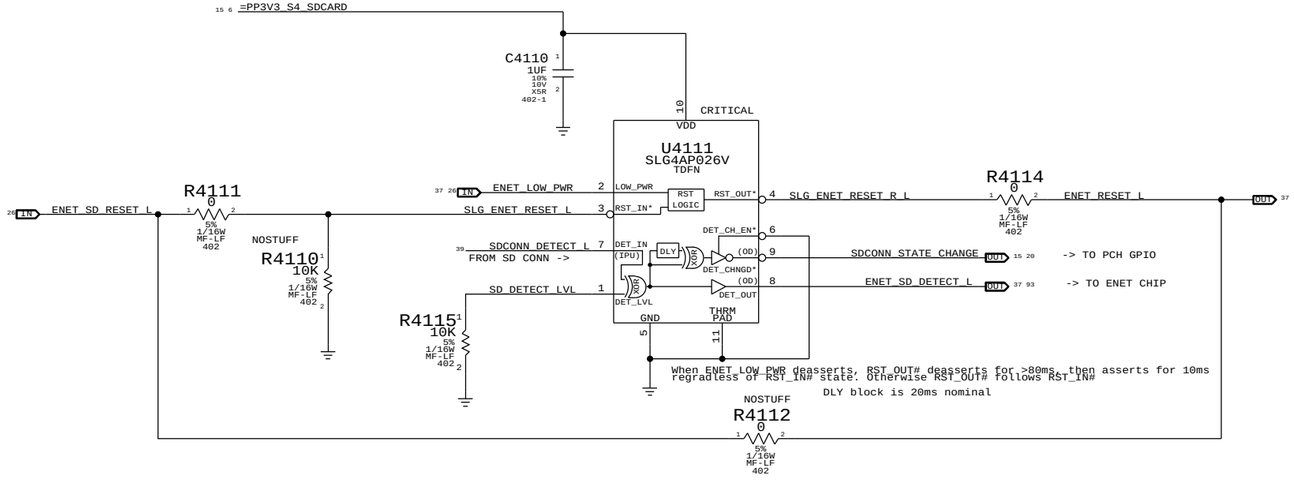
SD-CARD-K70-K72

F-ANG-TH



WRITE_PROTECT_SWITCH is normally connected (i.e. gnd)

SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=D7_NICK SYNC_DATE=01/12/2012

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

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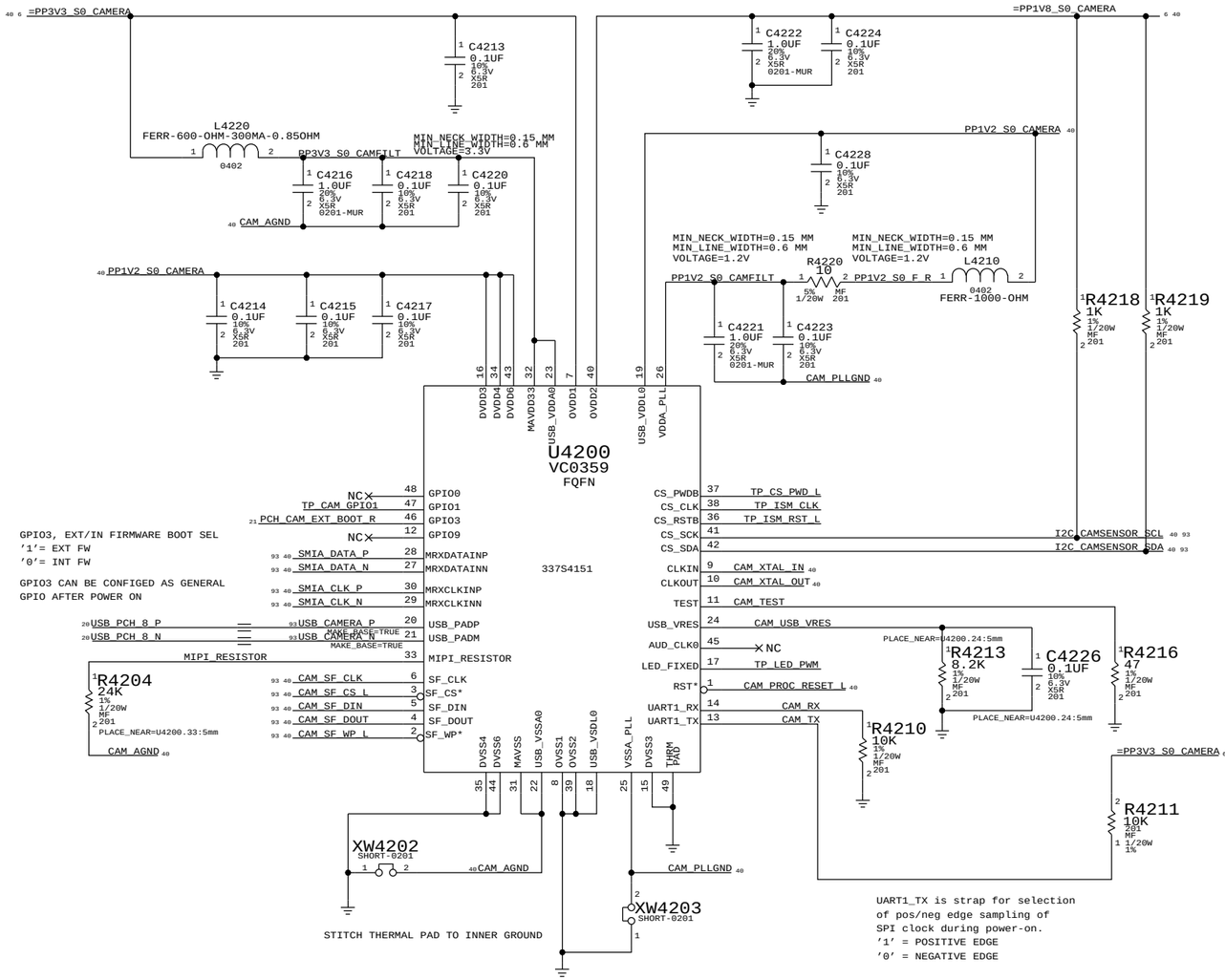
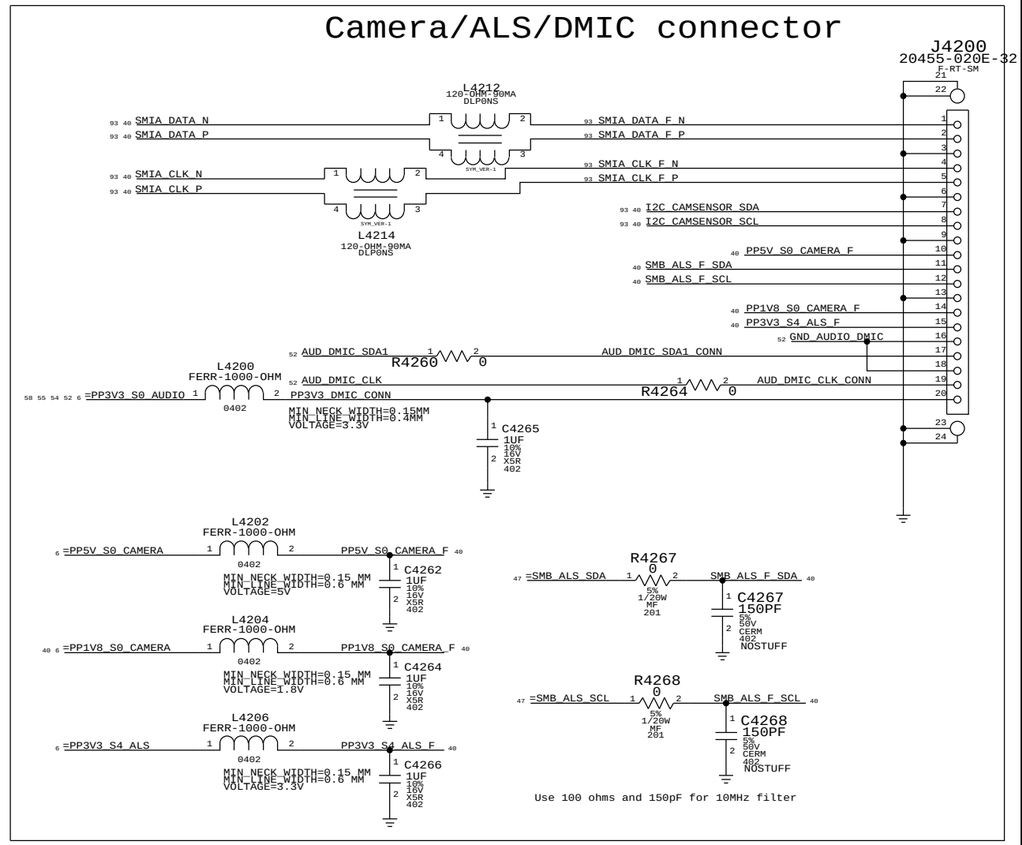
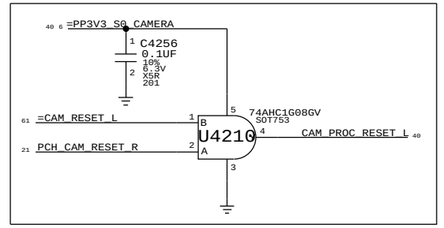
USB CAMERA CONTROLLER

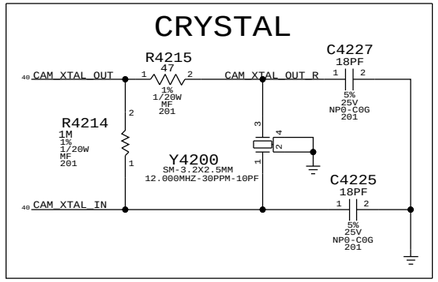


Camera/ALS/DMIC connector

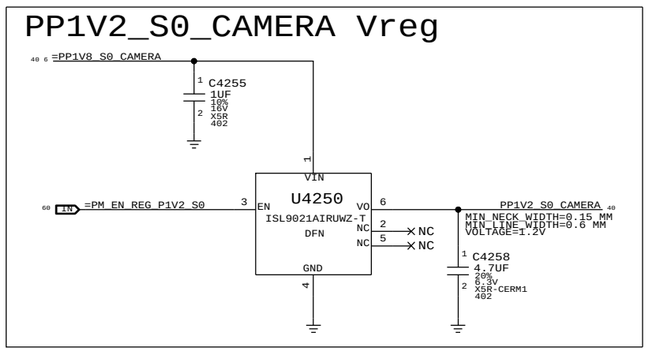




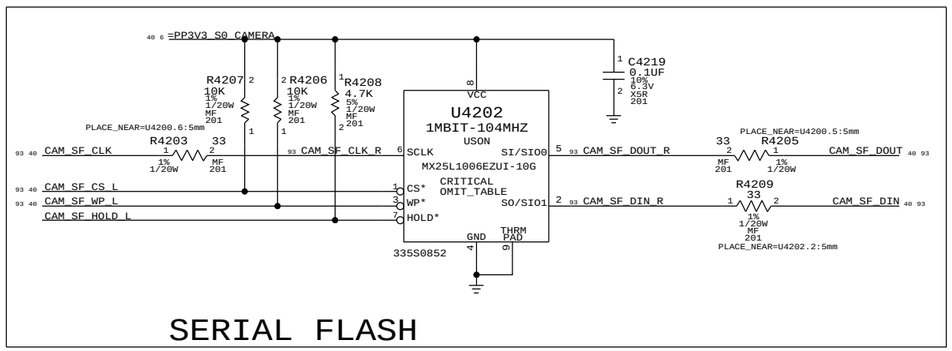
CRYSTAL



PP1V2_S0_CAMERA Vreg



SERIAL FLASH



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	Apple Inc.
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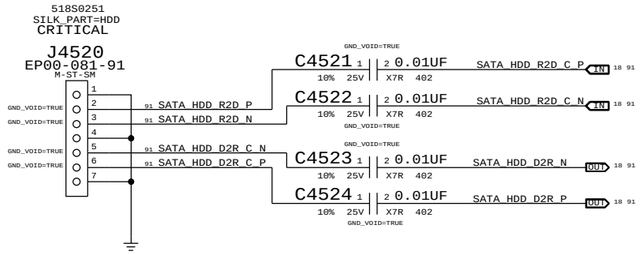
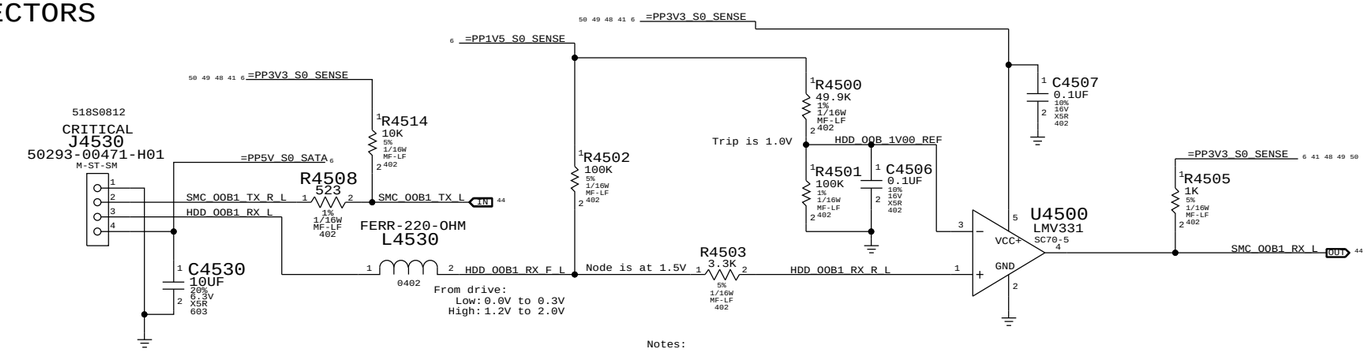
HDD CONNECTORS



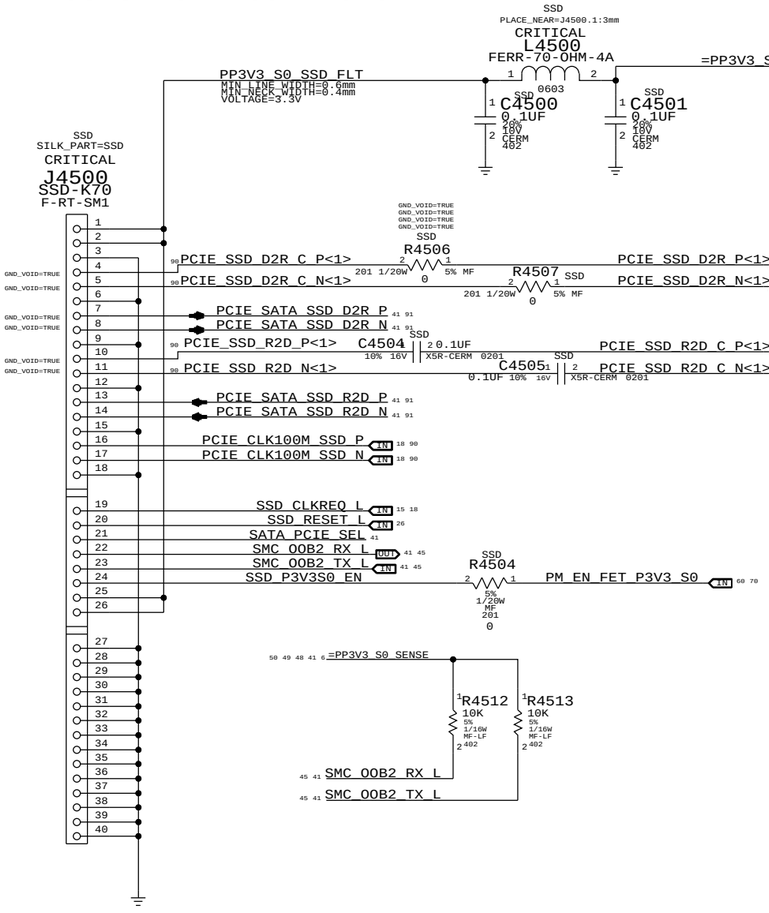
HDD Out-of-Band Temperature Sensing

Temperature read from SATA power connecter pin 11

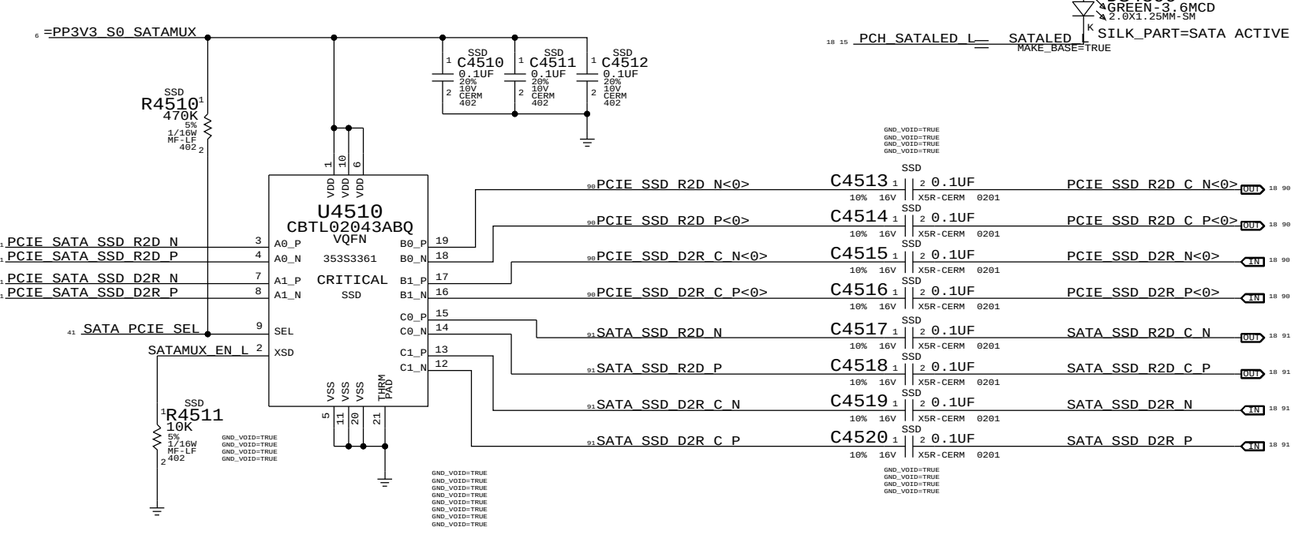


Notes:
- Drive active: Valid signal protocol
- Drive asleep: HDD drives HDD_OOB_TEMP low
- Drive disconnected: Pulled high

GUMSTICK2 CONNECTOR



SATA Activity LED



SYNC_MASTER=D7_NICK	SYNC_DATE=12/16/2011
PAGE TITLE: SATA Connectors	
Apple Inc.	DRAWING NUMBER: 051-9509 SIZE: D
	REVISION: 4.2.0
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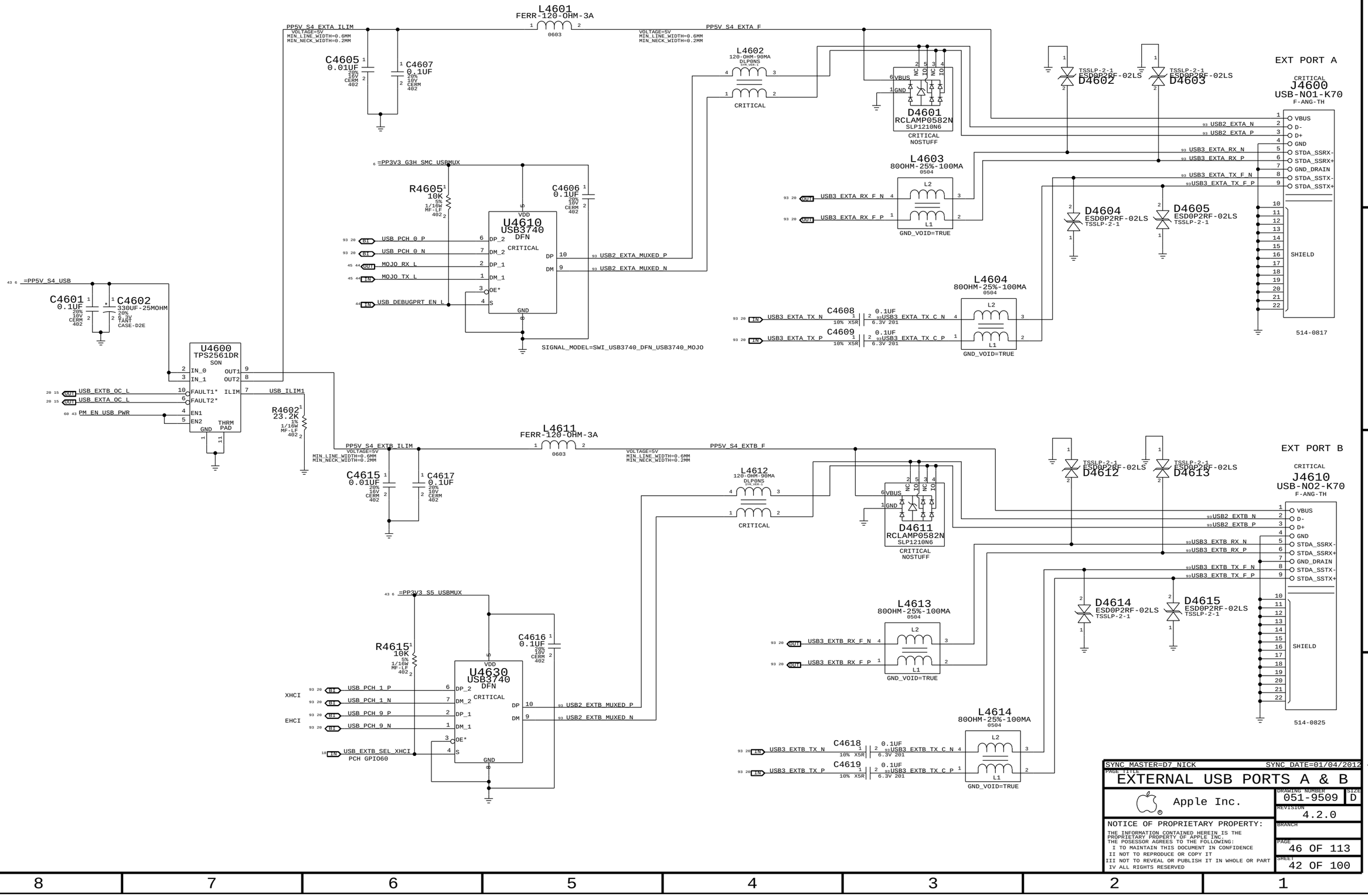
L4601
FERR-120-OHM-3A
0603
PP5V_S4_EXTA_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
C4605
0.01UF
C4607
0.1UF
PP5V_S4_EXTA_F
L4602
120-OHM-90MA
DLP0NS
CRITICAL
D4601
RCLAMP0582N
SLP1210N6
CRITICAL
NOSTUFF
D4602
D4603
EXT PORT A
J4600
USB-NO1-K70
F-ANG-TH
USB2_EXTA_N
USB2_EXTA_P
USB3_EXTA_RX_N
USB3_EXTA_RX_P
USB3_EXTA_TX_F_N
USB3_EXTA_TX_F_P
SHIELD
514-0817
L4603
80OHM-25%-100MA
0504
USB3_EXTA_RX_F_N
USB3_EXTA_RX_F_P
GND_VOID=TRUE
D4604
D4605
ESD0P2RF-02LS
TSSLP-2-1
=PP3V3_G3H_SMC_USBMUX
R4605
10K
C4606
0.1UF
U4610
USB3740
DFN
CRITICAL
USB_PCH_0_P
USB_PCH_0_N
MOJO_RX_L
MOJO_TX_L
USB_DEBUGPRT_EN_L
USB2_EXTA_MUXED_P
USB2_EXTA_MUXED_N
SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO
=PP5V_S4_USB
C4601
0.1UF
C4602
330UF-25MOHM
CASE-D2E
U4600
TPS2561DR
SON
USB_EXTB_OC_L
USB_EXTA_OC_L
PM_EN_USB_PWR
USB_ILIM1
R4602
23.2K
L4604
80OHM-25%-100MA
0504
C4608
0.1UF
C4609
0.1UF
USB3_EXTA_TX_C_N
USB3_EXTA_TX_C_P
USB3_EXTA_TX_N
USB3_EXTA_TX_P
GND_VOID=TRUE
L4611
FERR-120-OHM-3A
0603
PP5V_S4_EXTB_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
PP5V_S4_EXTB_F
C4615
0.01UF
C4617
0.1UF
L4612
120-OHM-90MA
DLP0NS
CRITICAL
D4611
RCLAMP0582N
SLP1210N6
CRITICAL
NOSTUFF
D4612
D4613
EXT PORT B
J4610
USB-NO2-K70
F-ANG-TH
USB2_EXTB_N
USB2_EXTB_P
USB3_EXTB_RX_N
USB3_EXTB_RX_P
USB3_EXTB_TX_F_N
USB3_EXTB_TX_F_P
SHIELD
514-0825
L4613
80OHM-25%-100MA
0504
USB3_EXTB_RX_F_N
USB3_EXTB_RX_F_P
GND_VOID=TRUE
D4614
D4615
ESD0P2RF-02LS
TSSLP-2-1
=PP3V3_S5_USBMUX
R4615
10K
C4616
0.1UF
U4630
USB3740
DFN
CRITICAL
XHCI
EHCI
USB_PCH_1_P
USB_PCH_1_N
USB_PCH_9_P
USB_PCH_9_N
USB_EXTB_SEL_XHCI
PCH GPIO60
USB2_EXTB_MUXED_P
USB2_EXTB_MUXED_N
L4614
80OHM-25%-100MA
0504
C4618
0.1UF
C4619
0.1UF
USB3_EXTB_TX_C_N
USB3_EXTB_TX_C_P
USB3_EXTB_TX_N
USB3_EXTB_TX_P
GND_VOID=TRUE
SYNC_MASTER=D7_NICK
SYNC_DATE=01/04/2012
PAGE TITLE
EXTERNAL USB PORTS A & B
Apple Inc.
DRAWING NUMBER
051-9509
SIZE
D
REVISION
4.2.0
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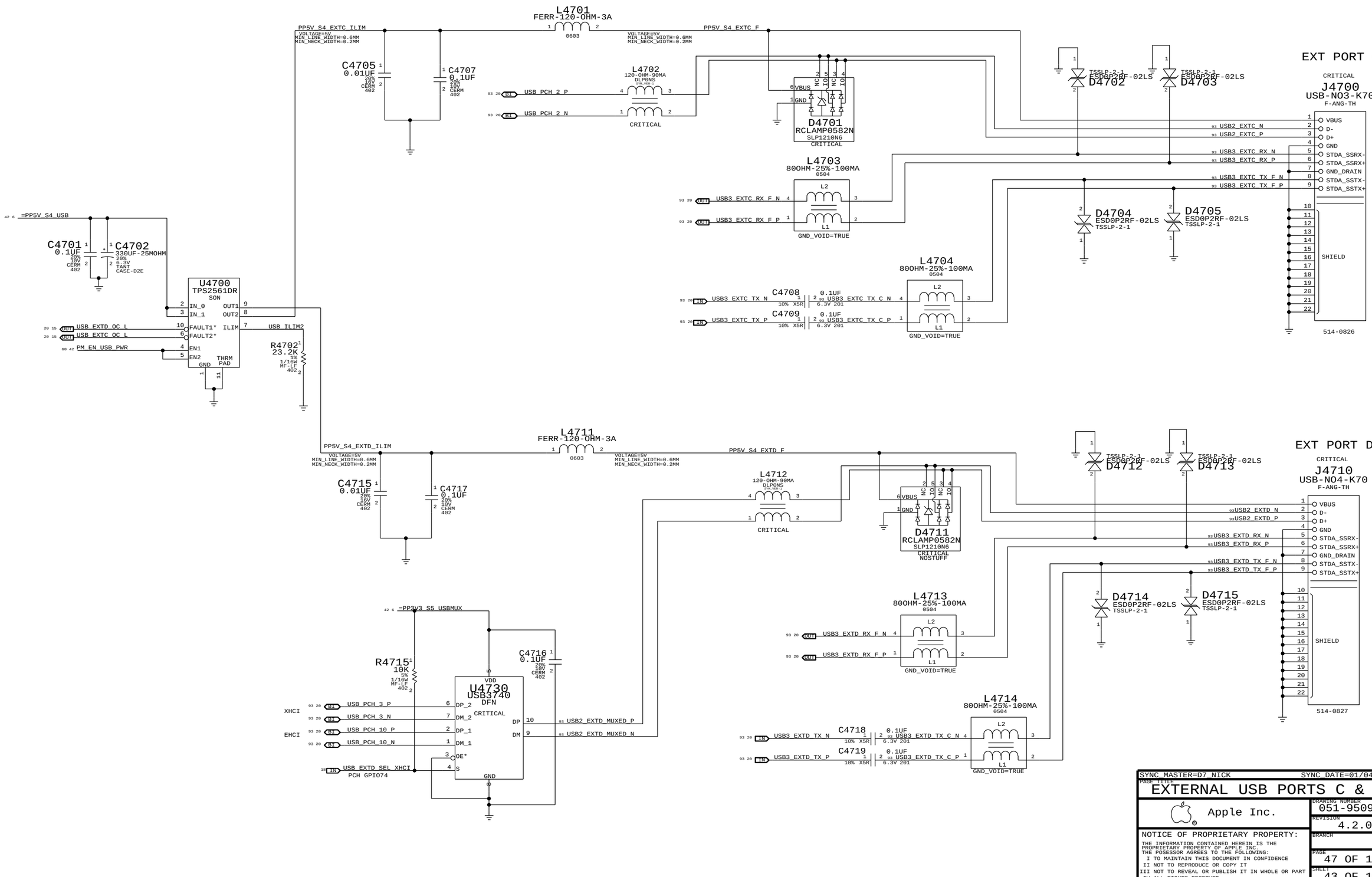

SYNC_MASTER=D7_NICK SYNC_DATE=01/04/2012

PAGE TITLE
EXTERNAL USB PORTS C & D

Apple Inc.

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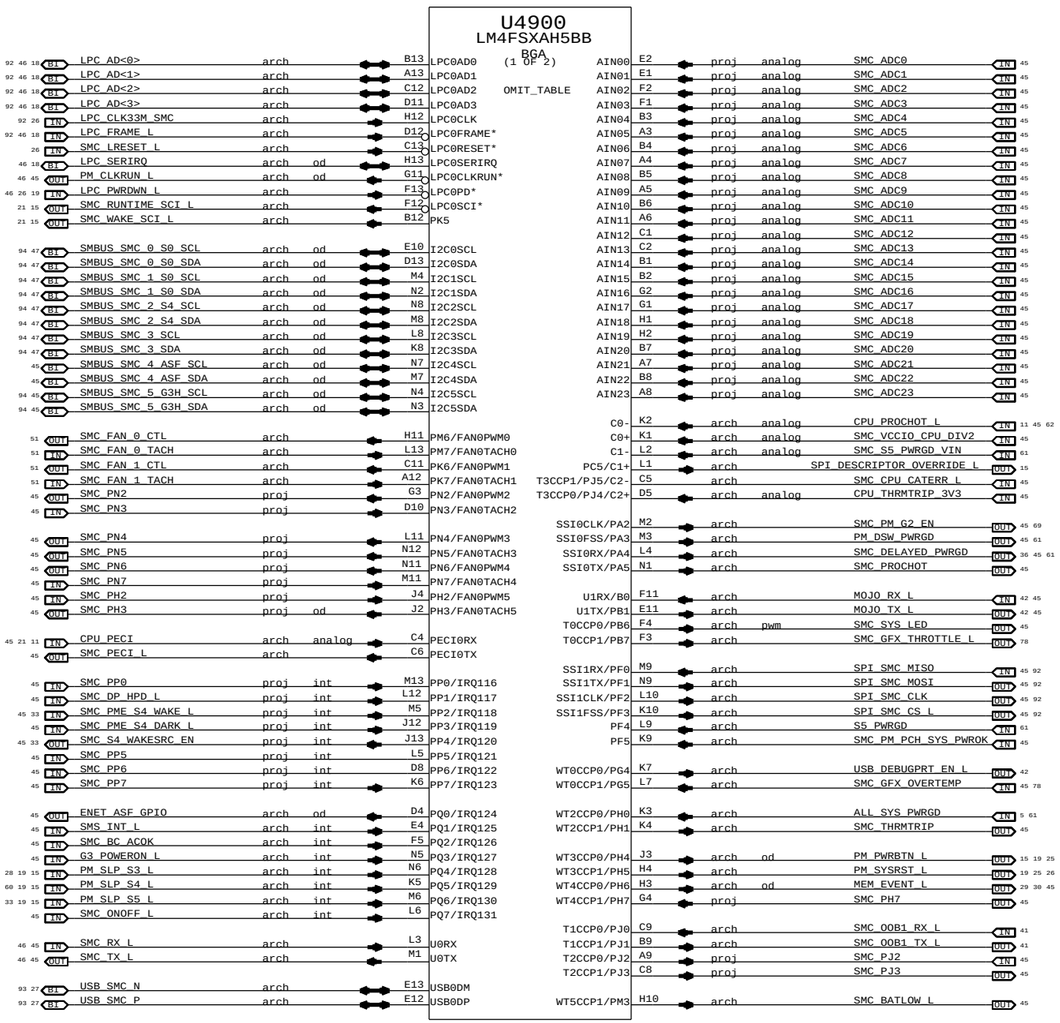
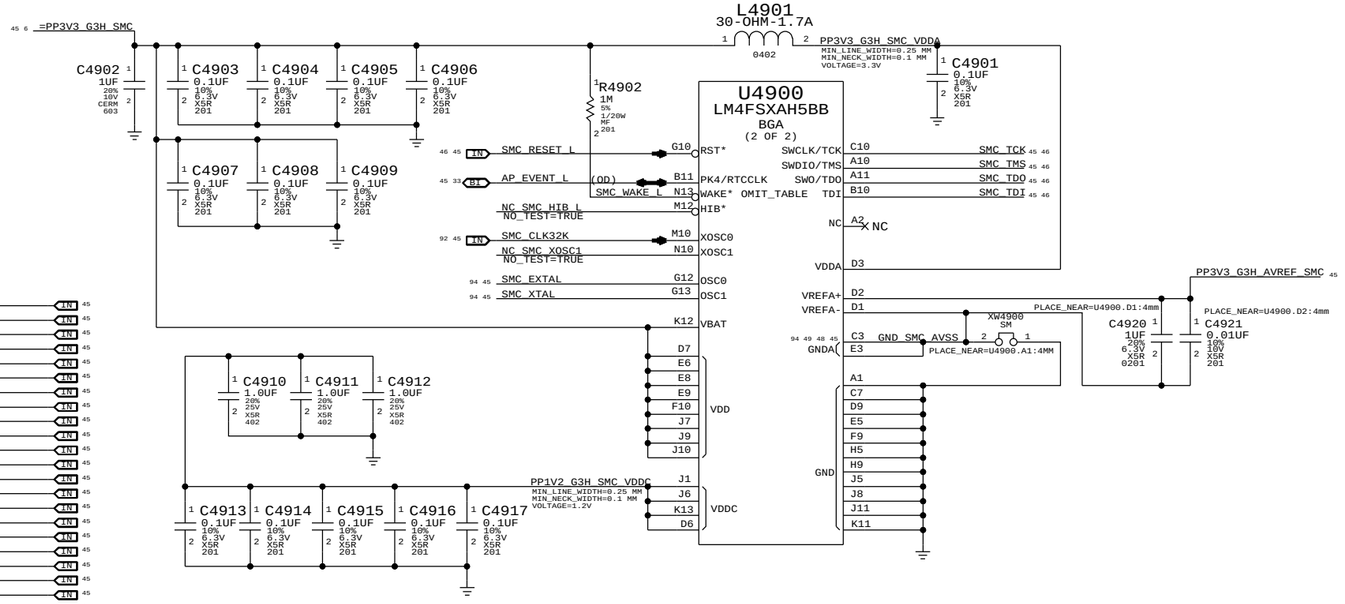
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





SYNC_MASTER=D7_DOUG	SYNC_DATE=01/11/2012
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER: 051-9509
	SIZE: D
	REVISION: 4.2.0
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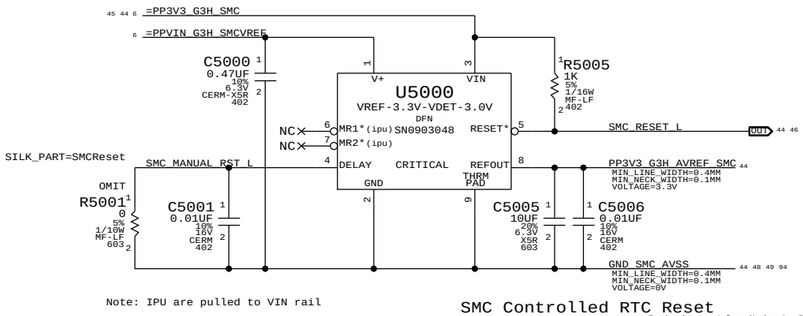
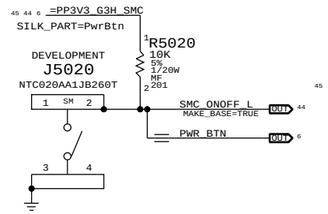
SMC Supervisor and AVREF Supply

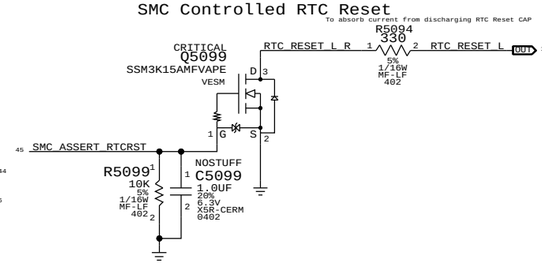


Note: IPU are pulled to VIN rail

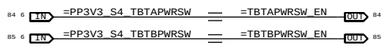
Power Button



SMC Controlled RTC Reset



Enable TBT S4 Wake Sources

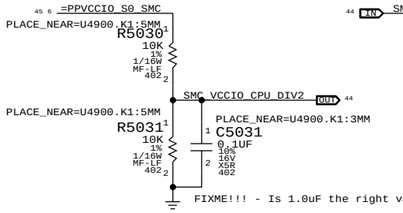


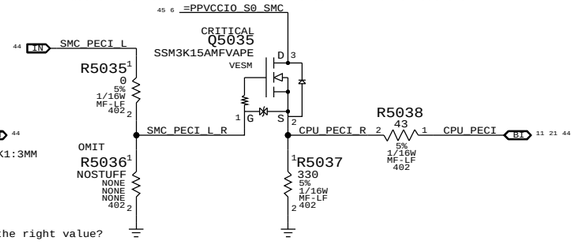
PECI Support

Level-shifter that allows SMC to drive PECI

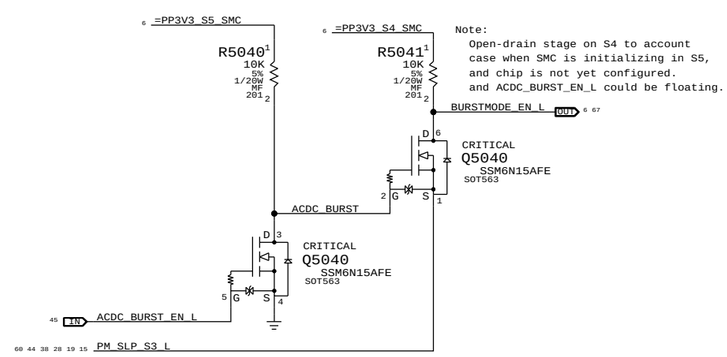
Place this circuit near the Tee point to minimize reflections

Comparator Reference





AC/DC Burst Mode Enable



ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC1	ISNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC2	VSNS_P12VS0_GPUCORE	MAKE_BASE=TRUE
SMC_ADC3	ISNS_P12VS0_GPUCORE	MAKE_BASE=TRUE
SMC_ADC6	VSNS_VDDQS3_DDR	MAKE_BASE=TRUE
SMC_ADC7	ISNS_VDDQS3_DDR	MAKE_BASE=TRUE
SMC_ADC8	VSNS_P12VS0_GPUUNCORE	MAKE_BASE=TRUE
SMC_ADC9	ISNS_P12VS0_GPUUNCORE	MAKE_BASE=TRUE
SMC_ADC10	VSNS_CPUCORE	MAKE_BASE=TRUE
SMC_ADC11	ISNS_CPUCORE	MAKE_BASE=TRUE
SMC_ADC12	VSNS_CPUAXG	MAKE_BASE=TRUE
SMC_ADC13	ISNS_CPUAXG	MAKE_BASE=TRUE
SMC_ADC14	VSNS_HDDS0	MAKE_BASE=TRUE
SMC_ADC15	ISNS_HDDS0	MAKE_BASE=TRUE
SMC_ADC16	VSNS_SSDS0	MAKE_BASE=TRUE
SMC_ADC17	ISNS_SSDS0	MAKE_BASE=TRUE

Project-specific Aliases

SMC_PH3	BDV_BKL_PWM	MAKE_BASE=TRUE
SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE
SMC_PJ3	SMC_OOB2_TX_L	MAKE_BASE=TRUE
SMC_PJ2	SMC_OOB2_RX_L	MAKE_BASE=TRUE
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE

Unused ADC Channels

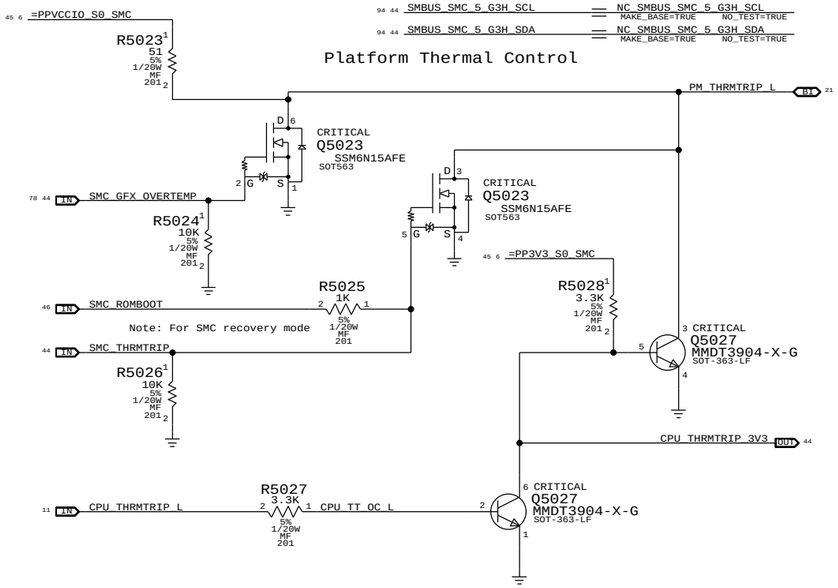
SMC_ADC4	NC_SMC_ADC4	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC5	NC_SMC_ADC5	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC18	NC_SMC_ADC18	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC19	NC_SMC_ADC19	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC20	NC_SMC_ADC20	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC21	NC_SMC_ADC21	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC23	NC_SMC_ADC23	MAKE_BASE=TRUE NO_TEST=TRUE

Unused Project-specific

SMC_PN2	NC_SMC_PN2	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN3	NC_SMC_PN3	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN4	NC_SMC_PN4	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN6	NC_SMC_PN6	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN7	NC_SMC_PN7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PH7	TP_SMC_PH7	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE NO_TEST=TRUE

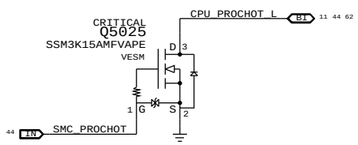
TP for access if ZPB re-intstated

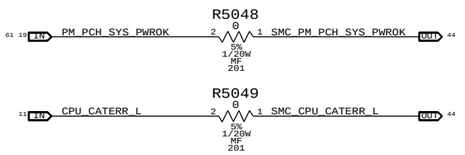
Platform Thermal Control



PROCHOT Support

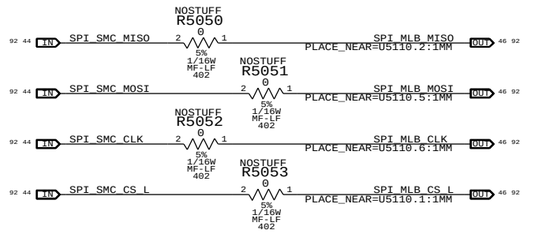
Level-shifter that allows SMC to drive PROCHOT





SMC SPI Support

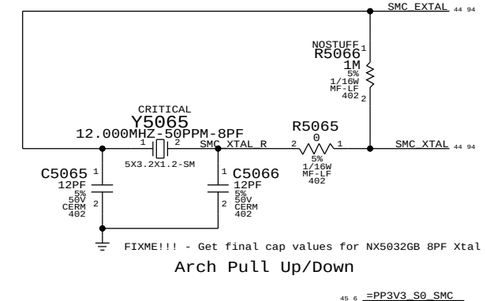
Series R are NOSTUFF until topology of 2 SPI masters is verified



SMC 32KHz Clock

SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal



FIXME!!! - Get final cap values for NX5032GB 8PF Xtal

Arch Pull Up/Down

MEM_EVENT_L	R5070	10K	=PP3V3_S0_SMC	1/20W MF 201
PM_CLKRUN_L	R5071	10K	=PP3V3_S0_SMC	1/20W MF 201
ENET_ASF_GPIO	R5075	10K	=PP3V3_G3H_SMC	1/20W MF 201
G3_POWERON_L	R5076	10K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_BATLOW_L	R5077	100K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_BC_ACOK	R5078	100K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_SYS_LED	R5079	100K	=PP3V3_G3H_SMC	1/20W MF 201
SMS_INT_L	R5080	10K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_PME_S4_WAKE_L	R5081	10K	=PP3V3_G3H_SMC	1/20W MF 201
AP_EVENT_L	R5085	10K	PP3V3_S4_AP_FET	1/20W MF 201
SMC_S4_WAKESRC_EN	R5017	100K	=PP3V3_G3H_SMC	1/20W MF 201
SMC_DELAYED_PWRGD	R5086	100K	=PP3V3_G3H_SMC	1/16W MF-LF 402
PM_DSW_PWRGD	R5084	100K	=PP3V3_G3H_SMC	1/16W MF-LF 402
SMC_PM_G2_EN	R5087	100K	=PP3V3_G3H_SMC	1/20W MF 201

Note: Pull-down needed for SMC SSI signals

Serial/JTAG Interface Pull-ups

SMC_TX_L	R5090	10K	=PP3V3_G3H_SMC
SMC_RX_L	R5091	100K	=PP3V3_G3H_SMC
MOJO_TX_L	R5092	10K	=PP3V3_G3H_SMC
MOJO_RX_L	R5093	100K	=PP3V3_G3H_SMC
SMC_TCK	R5095	10K	=PP3V3_G3H_SMC
SMC_TDI	R5096	10K	=PP3V3_G3H_SMC
SMC_TDO	R5097	10K	=PP3V3_G3H_SMC
SMC_TMS	R5098	10K	=PP3V3_G3H_SMC

SYNC_MASTER=D7_DOUG SYNC_DATE=01/11/2012

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

REVISION: 4.2.0

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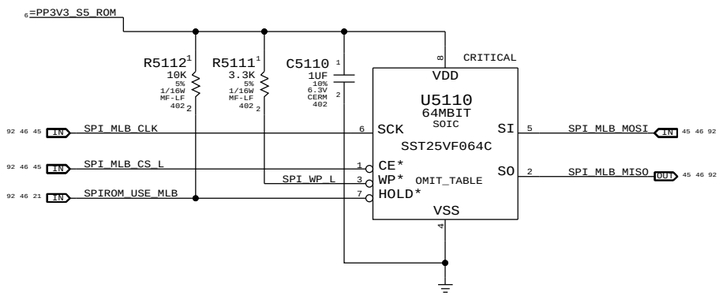
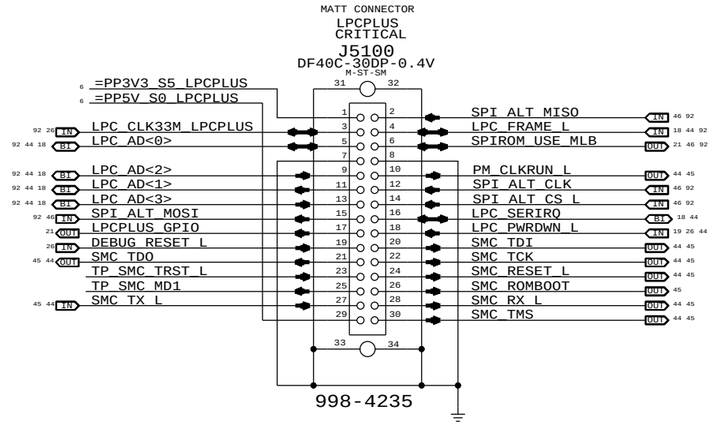
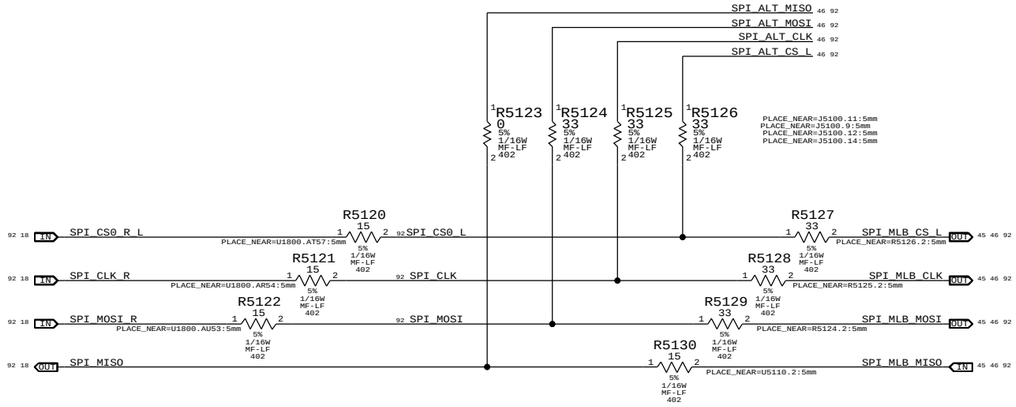
SPI BootROM



LPC+SPI Connector



SPI Series Termination



SYNC_MASTER=D7_NICK SYNC_DATE=12/13/2011

PAGE TITLE
SPI and Debug Connector

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

REVISION 4.2.0

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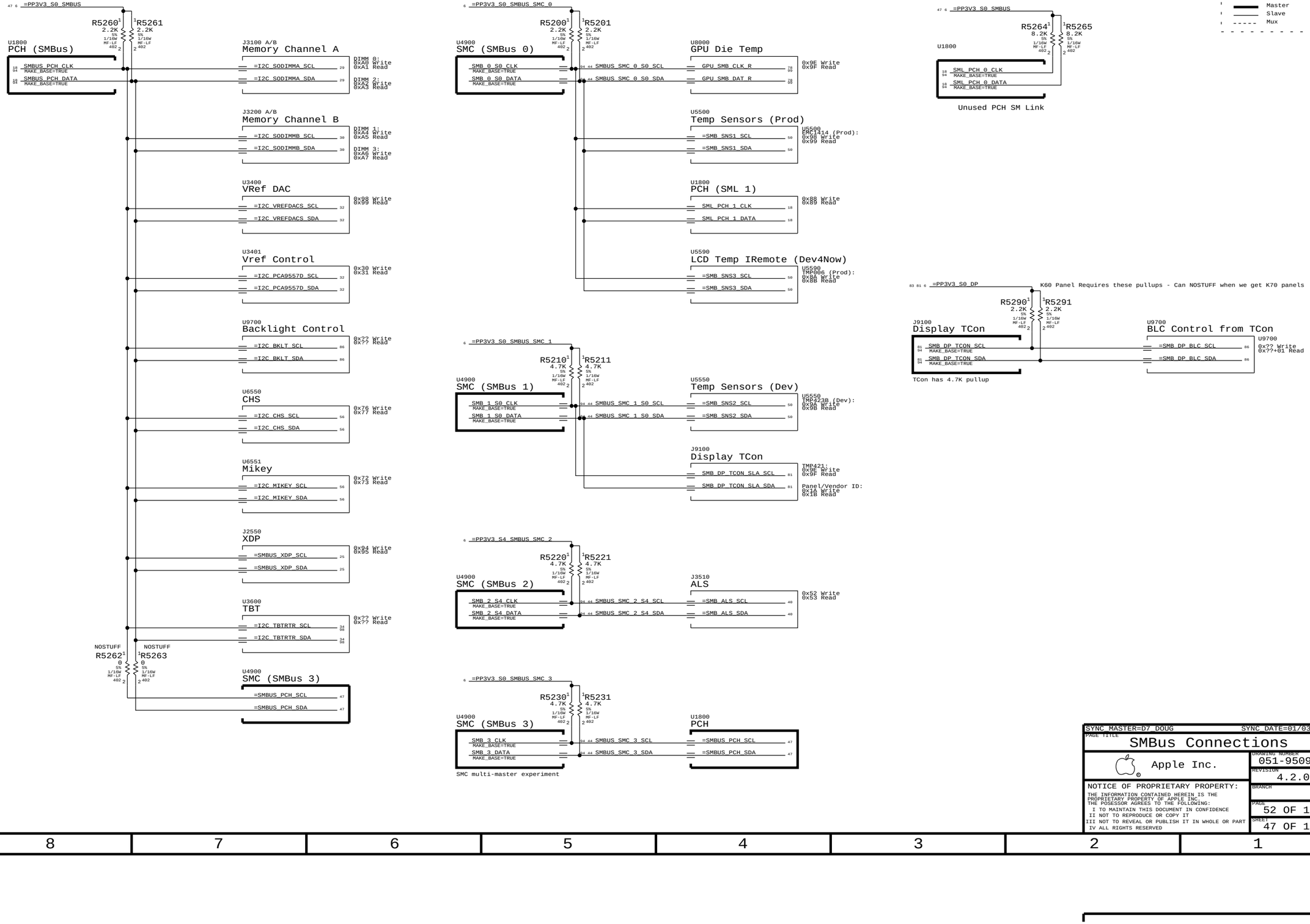
=PP3V3_S0_SMBUS
R5260 2.2K 5% 1/16W MF-LF 402
R5261 2.2K 5% 1/16W MF-LF 402
U1800
PCH (SMBus)
SMBUS_PCH_CLK
MAKE_BASE=TRUE
SMBUS_PCH_DATA
MAKE_BASE=TRUE
J3100 A/B
Memory Channel A
=I2C_SODIMMA_SCL
=I2C_SODIMMA_SDA
DIMM 0: 0xA0 Write 0xA1 Read
DIMM 2: 0xA2 Write 0xA3 Read
J3200 A/B
Memory Channel B
=I2C_SODIMMB_SCL
=I2C_SODIMMB_SDA
DIMM 1: 0xA4 Write 0xA5 Read
DIMM 3: 0xA6 Write 0xA7 Read
U3400
VRef DAC
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA
0x98 Write 0x99 Read
U3401
Vref Control
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA
0x30 Write 0x31 Read
U9700
Backlight Control
=I2C_BKLT_SCL
=I2C_BKLT_SDA
0x22 Write 0x77 Read
U6550
CHS
=I2C_CHS_SCL
=I2C_CHS_SDA
0x76 Write 0x77 Read
U6551
Mikey
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA
0x72 Write 0x73 Read
J2550
XDP
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA
0x04 Write 0x05 Read
U3600
TBT
=I2C_TBTRTR_SCL
=I2C_TBTRTR_SDA
0x?? Write 0x?? Read
NOSTUFF
R5262 0 5% 1/16W MF-LF 402
NOSTUFF
R5263 0 5% 1/16W MF-LF 402
U4900
SMC (SMBus 3)
=SMBUS_PCH_SCL
=SMBUS_PCH_SDA
=PP3V3_S0_SMBUS_SMC_0
R5200 2.2K 5% 1/16W MF-LF 402
R5201 2.2K 5% 1/16W MF-LF 402
U4900
SMC (SMBus 0)
SMB_0_S0_CLK
MAKE_BASE=TRUE
SMB_0_S0_DATA
MAKE_BASE=TRUE
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA
U8000
GPU Die Temp
GPU_SMB_CLK_R
GPU_SMB_DAT_R
0x9E Write 0x9F Read
U5500
Temp Sensors (Prod)
=SMB_SNS1_SCL
=SMB_SNS1_SDA
U5500 EMC1414 (Prod): 0x98 Write 0x99 Read
U1800
PCH (SML 1)
SML_PCH_1_CLK
SML_PCH_1_DATA
0x80 Write 0x81 Read
U5590
LCD Temp IRemote (Dev4Now)
=SMB_SNS3_SCL
=SMB_SNS3_SDA
U5590 TMP006 (Prod): 0x8A Write 0x8B Read
=PP3V3_S0_SMBUS_SMC_1
R5210 4.7K 5% 1/16W MF-LF 402
R5211 4.7K 5% 1/16W MF-LF 402
U4900
SMC (SMBus 1)
SMB_1_S0_CLK
MAKE_BASE=TRUE
SMB_1_S0_DATA
MAKE_BASE=TRUE
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA
U5550
Temp Sensors (Dev)
=SMB_SNS2_SCL
=SMB_SNS2_SDA
U5550 TMP423B (Dev): 0x4A Write 0x9B Read
J9100
Display TCon
SMB_DP_TCON_SLA_SCL
SMB_DP_TCON_SLA_SDA
TMP421: 0x9E Write 0x9F Read
Panel/Vendor ID: 0x1A Write 0x1B Read
=PP3V3_S4_SMBUS_SMC_2
R5220 4.7K 5% 1/16W MF-LF 402
R5221 4.7K 5% 1/16W MF-LF 402
U4900
SMC (SMBus 2)
SMB_2_S4_CLK
MAKE_BASE=TRUE
SMB_2_S4_DATA
MAKE_BASE=TRUE
SMBUS_SMC_2_S4_SCL
SMBUS_SMC_2_S4_SDA
J3510
ALS
=SMB_ALS_SCL
=SMB_ALS_SDA
0x52 Write 0x53 Read
=PP3V3_S0_SMBUS_SMC_3
R5230 4.7K 5% 1/16W MF-LF 402
R5231 4.7K 5% 1/16W MF-LF 402
U4900
SMC (SMBus 3)
SMB_3_CLK
MAKE_BASE=TRUE
SMB_3_DATA
MAKE_BASE=TRUE
SMBUS_SMC_3_SCL
SMBUS_SMC_3_SDA
U1800
PCH
=SMBUS_PCH_SCL
=SMBUS_PCH_SDA
SMC multi-master experiment
=PP3V3_S0_SMBUS
R5264 8.2K 5% 1/16W MF-LF 402
R5265 8.2K 5% 1/16W MF-LF 402
U1800
SML_PCH_0_CLK
MAKE_BASE=TRUE
SML_PCH_0_DATA
MAKE_BASE=TRUE
Unused PCH SM Link
Line Legend
Master
Slave
Mux
=PP3V3_S0_DP
K60 Panel Requires these pullups - Can NOSTUFF when we get K70 panels
R5290 2.2K 5% 1/16W MF-LF 402
R5291 2.2K 5% 1/16W MF-LF 402
J9100
Display TCon
SMB_DP_TCON_SCL
MAKE_BASE=TRUE
SMB_DP_TCON_SDA
MAKE_BASE=TRUE
TCon has 4.7K pullup
U9700
BLC Control from TCon
=SMB_DP_BLC_SCL
=SMB_DP_BLC_SDA
U9700
0x?? Write 0x??+01 Read
SYNC_MASTER=D7_DOUG
SYNC_DATE=01/03/2012
PAGE TITLE
SMBus Connections
Apple Inc.
DRAWING NUMBER 051-9509
SIZE D
REVISION 4.2.0
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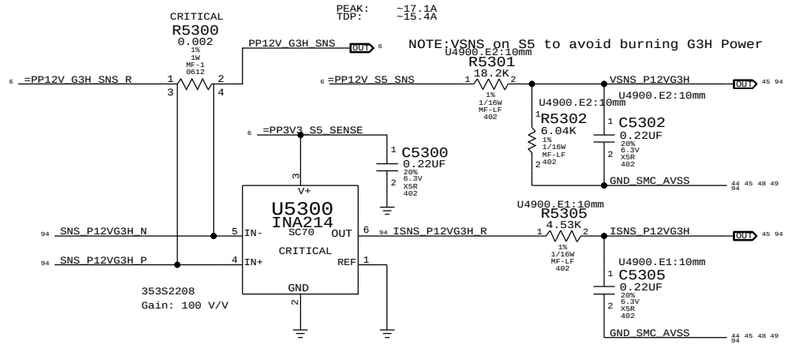
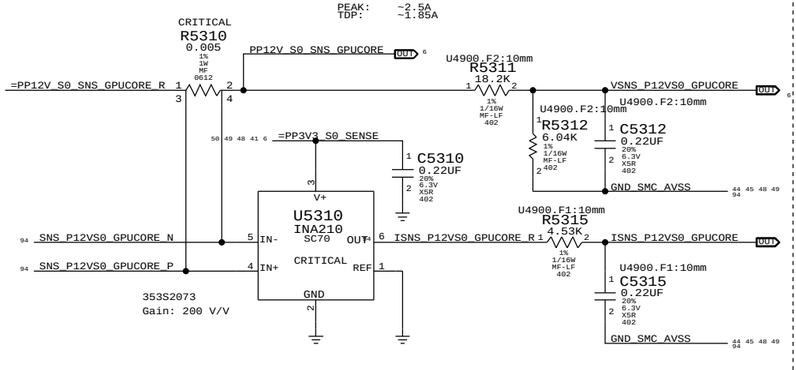
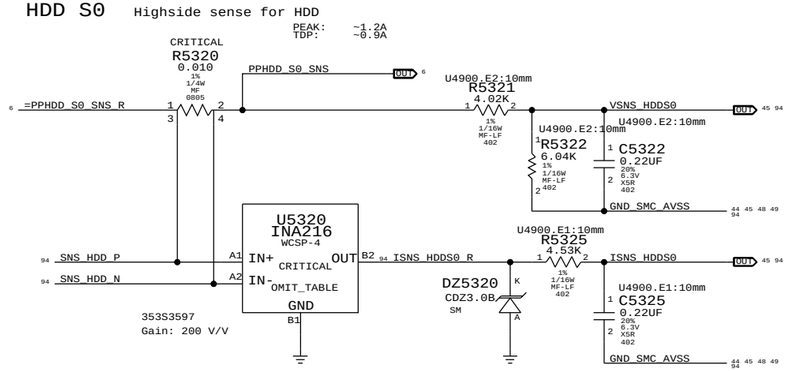
12V G3H AC/DC lowside sense (System total)



12V S0 GPU highside sense for GPU Core Regulator

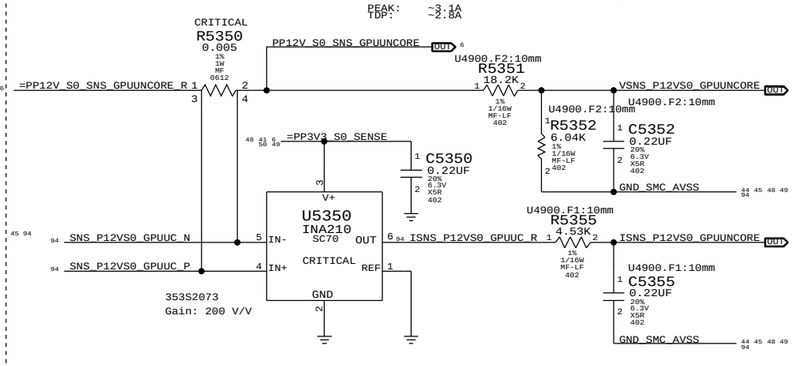


HDD S0 Highside sense for HDD

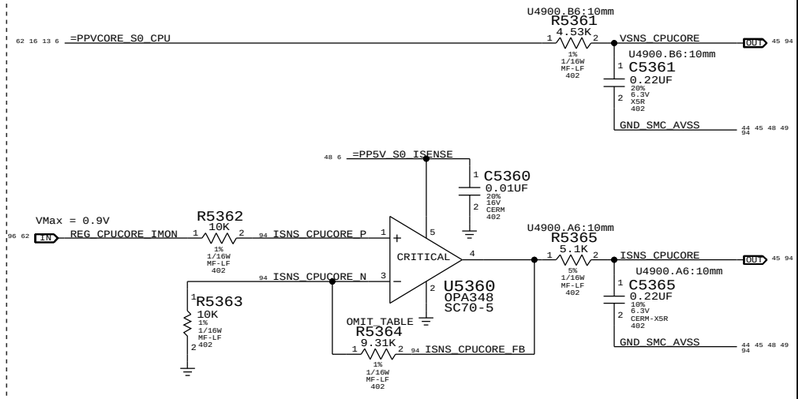


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S3597	1	INA216A4 200V/V Current Sense	U5320	

12V S0 GPU highside sense for GPU Frame Buffer 1.5V and 1.05V Regulators(Uncore)

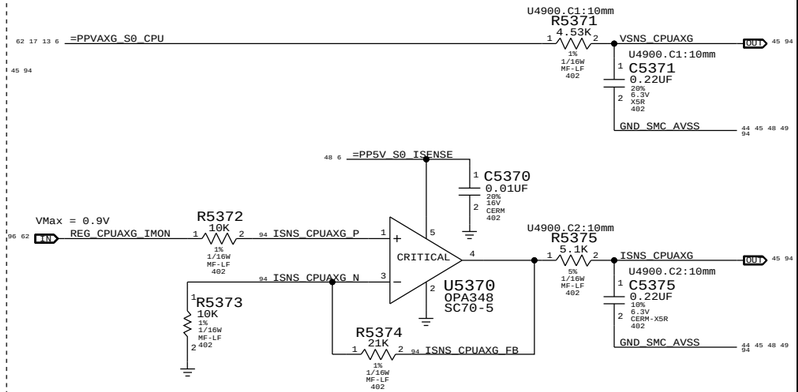


CPU Core Voltage sense and IMON amp (VC0C, IC0C)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES,MTL FILM,1/16W,9.31K,0402	R5364	SNS_CPUCORE:3PHASE
114S0345	1	RES,MTL FILM,1/16W,21K,0402	R5364	SNS_CPUCORE:4PHASE

CPU AXG Voltage sense and IMON amp (VC0G, IC0G)



SYNC_MASTER=D7_DOUG SYNC_DATE=01/06/2012

PAGE TITLE
I and V Sense(Production)

Apple Inc.

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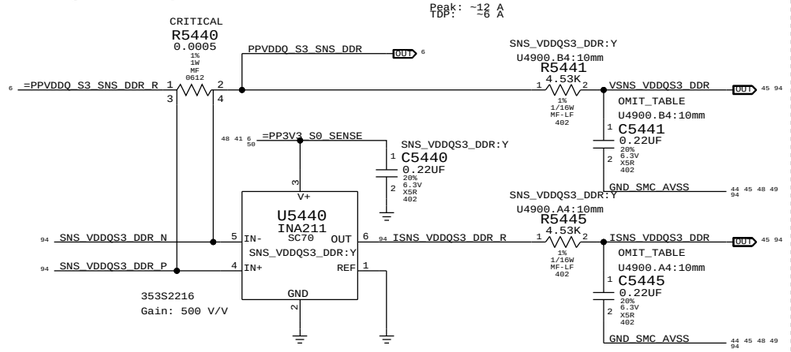
VDDQ S3

VDDQ lowside sense for SO-DIMM modules

Peak: ~12 A
TDP: ~6 A

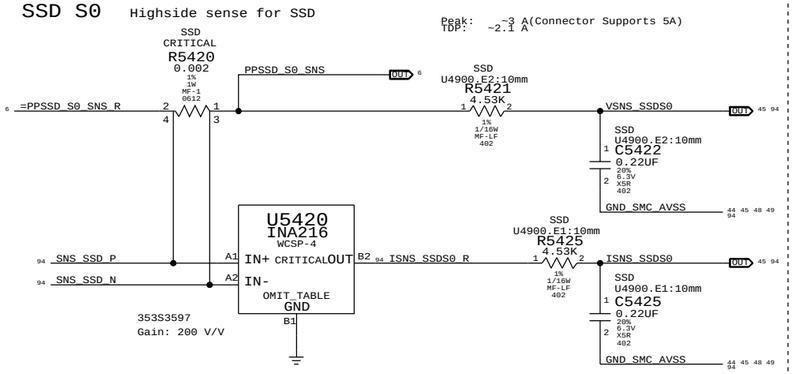


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5441,C5445	SNS_VDDQS3_DDR:Y
116S0004	2	RES,0 OHM,402	C5441,C5445	SNS_VDDQS3_DDR:N

SSD S0

Highside sense for SSD

Peak: ~3 A(Connector Supports 5A)
TDP: ~2.1 A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S3597	1	INA216A4 200V/V Current Sense	U5420	SSD

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE
I and V Sense(Development)

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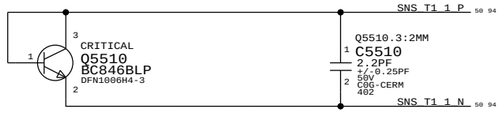
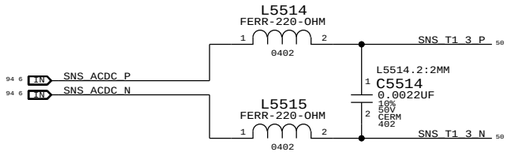
Temperature Sensor T1: Production Bound

GPU Proximity

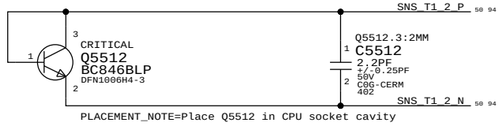


PLACEMENT_NOTE=Place Q5510 near GPU and GDDR5

AC/DC Diode on supply

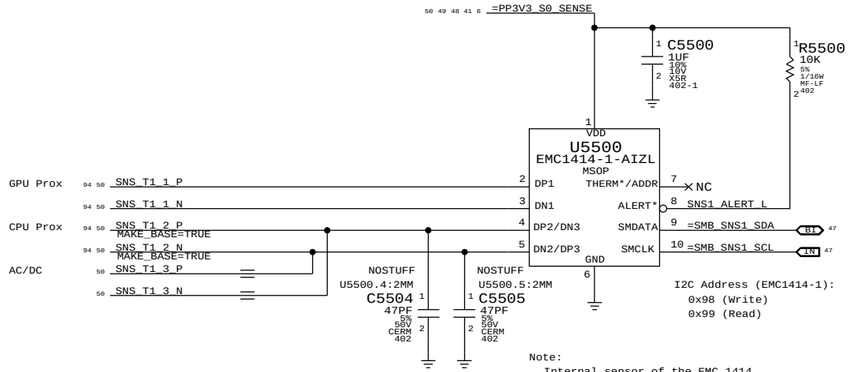


CPU Proximity



PLACEMENT_NOTE=Place Q5512 in CPU socket cavity

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

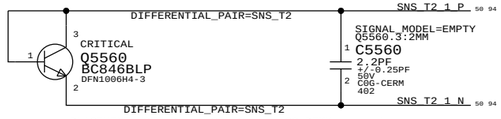


Make sure these caps are OK with U5500 Vendor!

Note:
Internal sensor of the EMC 1414
will be used as the ambient sensor.
Place U5500 at the coolest location
on the MLB.

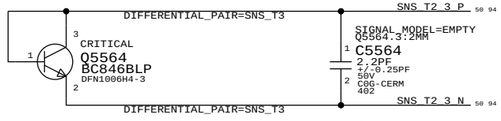
Temperature Sensor T2: Development Only

SO-DIMM Proximity



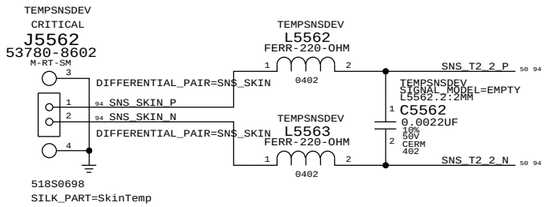
PLACEMENT_NOTE=Place Q5550 near SO-DIMM connectors

BLC Proximity

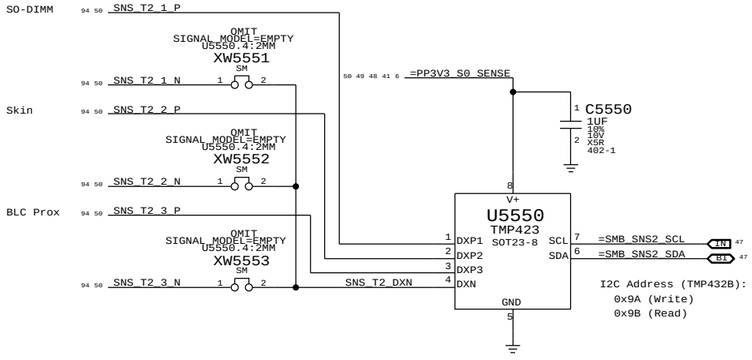


PLACEMENT_NOTE=Place Q5554 near BLC controller

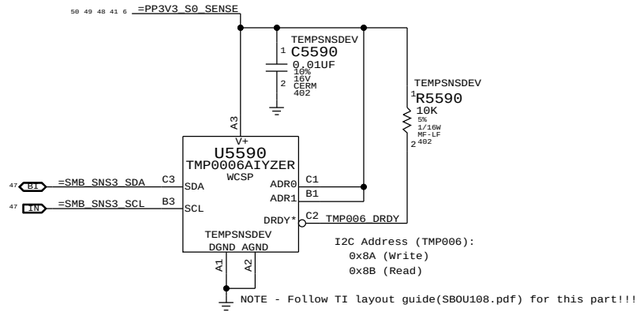
Skin



518S0698
SILK_PART=SkinTemp



Temperature Sensor T3: LCD Remote Sensor(Dev4Now)



NOTE - Follow TI layout guide(SBOU108.pdf) for this part!!!

SYNC_MASTER=D7_DOUG SYNC_DATE=12/13/2011

PAGE TITLE: Temperature Sensors

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

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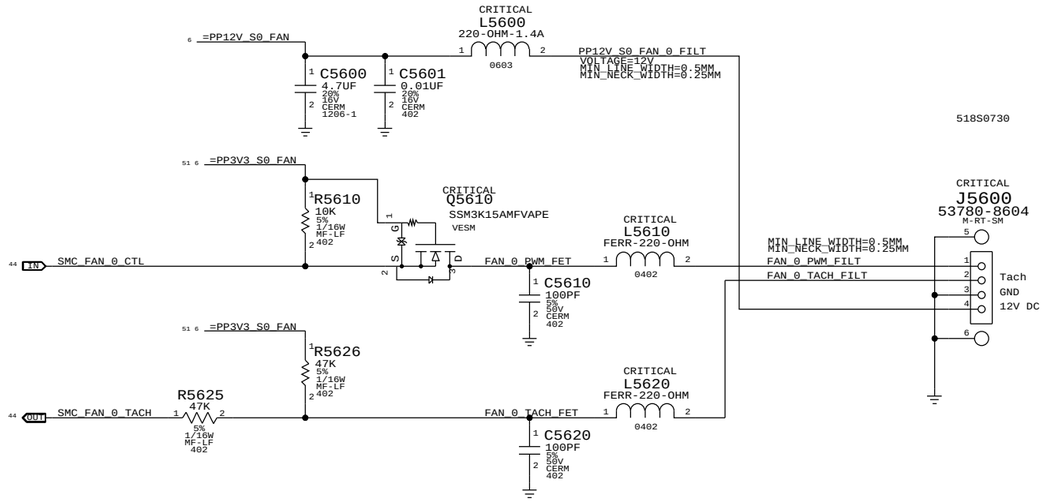
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q5610 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q5610 is at common and the SMC sinks current when Q5610 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.



SMC Fan 1 (Unused)

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE
System Fan

Apple Inc.

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AUDIO CODEC

APPLE P/N 353S2592

PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6101 4.7UF 20% 4V X5R-1 402

C6100 0.47UF 10% 10V X5R 402

C6108 10UF 20% 16V POLY-TANT CASE-B2-SM

C6109 2.2UF 20% 6.3V CERM 402-LF

C6110 2.2UF 20% 6.3V CERM 402-LF

C6102 0.47UF 10% 10V X5R 402

C6103 10UF 20% 16V POLY-TANT CASE-B2-SM

C6105 1UF 10% 10V X5R 402-1

C6104 0.47UF 10% 10V X5R 402

C6106 0.47UF 10% 10V X5R 402

C6107 CRITICAL 10UF 20% 10V X5R-CERM 0402-1

GND_AUDIO_CODEC

PP5V_AUDIO_HPAMP

=PP3V3_S0_AUDIO

PP4V5_AUDIO_ANALOG

R6100 2.67K 1% 1/16W MF-LF 402

R6105 0 5% 1/16W MF-LF 402

VBIAS_DAC

CS4206_FP

CS4206_FN

U6101 CRITICAL CS4206B QFN

VD VA_REF VA_HP VA

DMICS 1 & 2 — AUD_DMIC_SDA1 / NC TP_DMIC_SDA2

HP AMP CNTRL — AUD_GPIO_2

MAC SPKR AMP CNTRL — AUD_CODEC_MICBIAS — D6100 SOD-523 BAT54XV2T1

WIN SPKR AMP CNTRL — AUD_GPIO_3 / AUD_SENSE_A

CS4206_FLYP

CS4206_FLYC

CS4206_FLYN

C6111 2.2UF 20% 6.3V CERM 402-LF

C6112 2.2UF 20% 6.3V CERM 402-LF

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK

HDA_SYNC

HDA_SDIN0 — R6101 22 5% 1/16W MF-LF 402 — AUD_SDI_R

HDA_SDOUT

HDA_RST_L

DP_INT_SPDIF_AUDIO

AUD_SPDIF_OUT — R6102 22 5% 1/16W MF-LF 402 — AUD_SPDIF_CHIP

R6103 100K 1% 1/16W MF-LF 402

DGND THRM PAD AGND

DMICS SHOULD HAVE OWN GND ON CONNECTOR SHARED WITH CAMERA

GND_AUDIO_DMIC — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM VOLTAGE=0V — XW6100

GND_AUDIO_CODEC

CRITICAL C6113 1UF 10% 25V TANT CASE-P3-HF

CRITICAL C6114 10UF 20% 16V POLY-TANT CASE-B2-SM

C6115 0.47UF 10% 10V X5R 402

HPOUT_L — MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM — TP_AUD_HP_L NC

HPOUT_R — MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM — TP_AUD_HP_R NC

HPREF — MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM — CS4206_HPREF

LINEOUT_L1+ — AUD_LO1_L_P

LINEOUT_L1- — AUD_LO1_L_N

LINEOUT_R1+ — AUD_LO1_R_P

LINEOUT_R1- — AUD_LO1_R_N

HP AMP/LINE OUT

TWEETERS

RESERVE SPACE FOR POSSIBLE LATCH CIRCUIT

LINEOUT_L2+ — AUD_LO2_L_P

LINEOUT_L2- — AUD_LO2_L_N

LINEOUT_R2+ — AUD_LO2_R_P

LINEOUT_R2- — AUD_LO2_R_N

WOOFERS

MICBIAS — AUD_CODEC_MICBIAS

VCOM — CS4206_VCOM — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

LINEIN_L+ — NO_TEST=TRUE — NC_AUD_LI_P_L NC

LINEIN_C- — NO_TEST=TRUE — NC_AUD_LI_COM NC

LINEIN_R+ — NO_TEST=TRUE — NC_AUD_LI_P_R NC

MICIN_L+ — AUD_MIC_INL_P

MICIN_L- — AUD_MIC_INL_N

MICIN_R+ — NO_TEST=TRUE — NC_AUD_MIC_INP_R NC

MICIN_R- — NO_TEST=TRUE — NC_AUD_MIC_INN_R NC

VREF+_ADC — CS4206_VREF_ADC NC — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

DMIC_SCL — CS4206_DMIC_SCL — R6104 22 5% 1/16W MF-LF 402 — AUD_DMIC_CLK

Q6170 P_S / Q6170 P_G — DEVEL_AUDIO CRITICAL Q6170 DMC2400UV SOT563 — R6170 0 5% 1/16W MF-LF 402

Q6170 N_G / Q6170 N_S — DEVEL_AUDIO CRITICAL Q6170 DMC2400UV SOT563 — R6171 0 5% 1/16W MF-LF 402

Q6171 P_S / Q6171 P_G — DEVEL_AUDIO CRITICAL Q6171 DMC2400UV SOT563 — R6172 0 5% 1/16W MF-LF 402

Q6171 N_G / Q6171 N_S — DEVEL_AUDIO CRITICAL Q6171 DMC2400UV SOT563 — R6173 0 5% 1/16W MF-LF 402

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0134	127S0111		C6113	THAILAND ALTERNATE

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

L6111 FERR-220-OHM 0402 — MIN_LINE_WIDTH=0.18MM MIN_NECK_WIDTH=0.08MM VOLTAGE=4.5V — PP5V_AUDIO_HPAMP

L6110 FERR-220-OHM 0402 — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=4.5V — =PP5V_S0_AUDIO

VR6101 TPS71745 CRITICAL — 4V5_REG_IN — 4V5_REG_EN — 4V5_NR — PP4V5_AUDIO_ANALOG MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.15MM VOLTAGE=4.5V

R6120 0 5% 1/16W MF-LF 402 — =PP3V3_S0_AUDIO

C6122 1UF 10% 10V X5R 402-1

XW6110

C6123 0.1UF 10% 16V X7R-CERM 402

C6124 1UF 10% 10V X5R 402-1 — MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

GND_AUDIO_CODEC — MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

XW6111

GND_AUDIO_HPAMP — MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5

SYNC_MASTER=D7_BREECE SYNC_DATE=01/03/2012

PAGE TITLE: AUDIO: CODEC/REGULATORS

Apple Inc.

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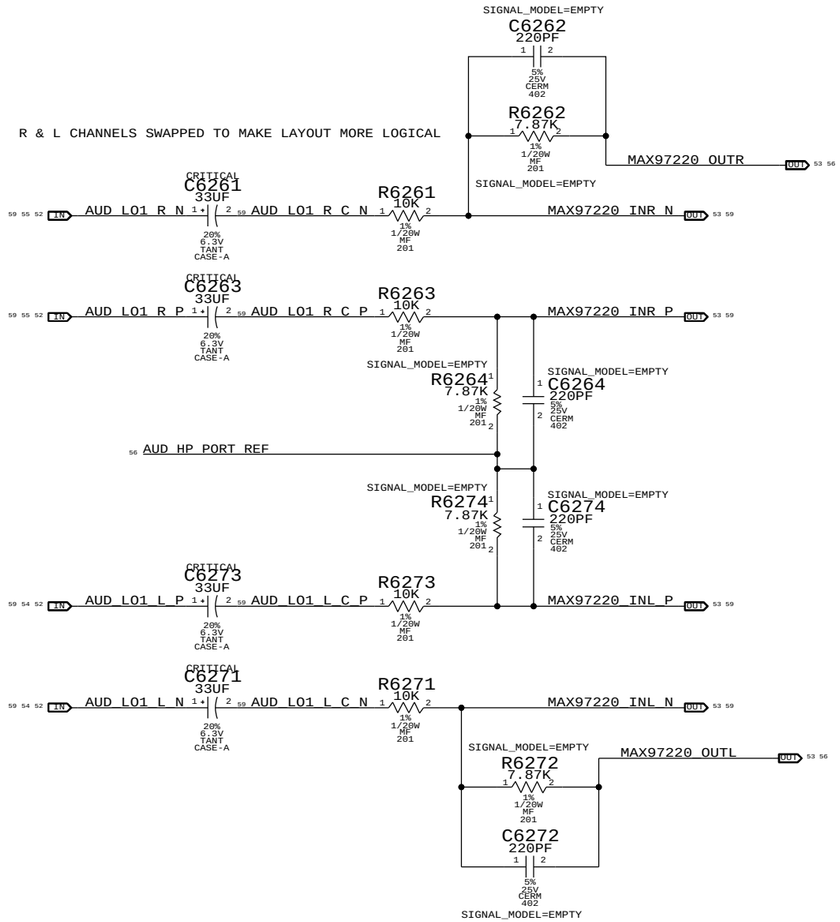
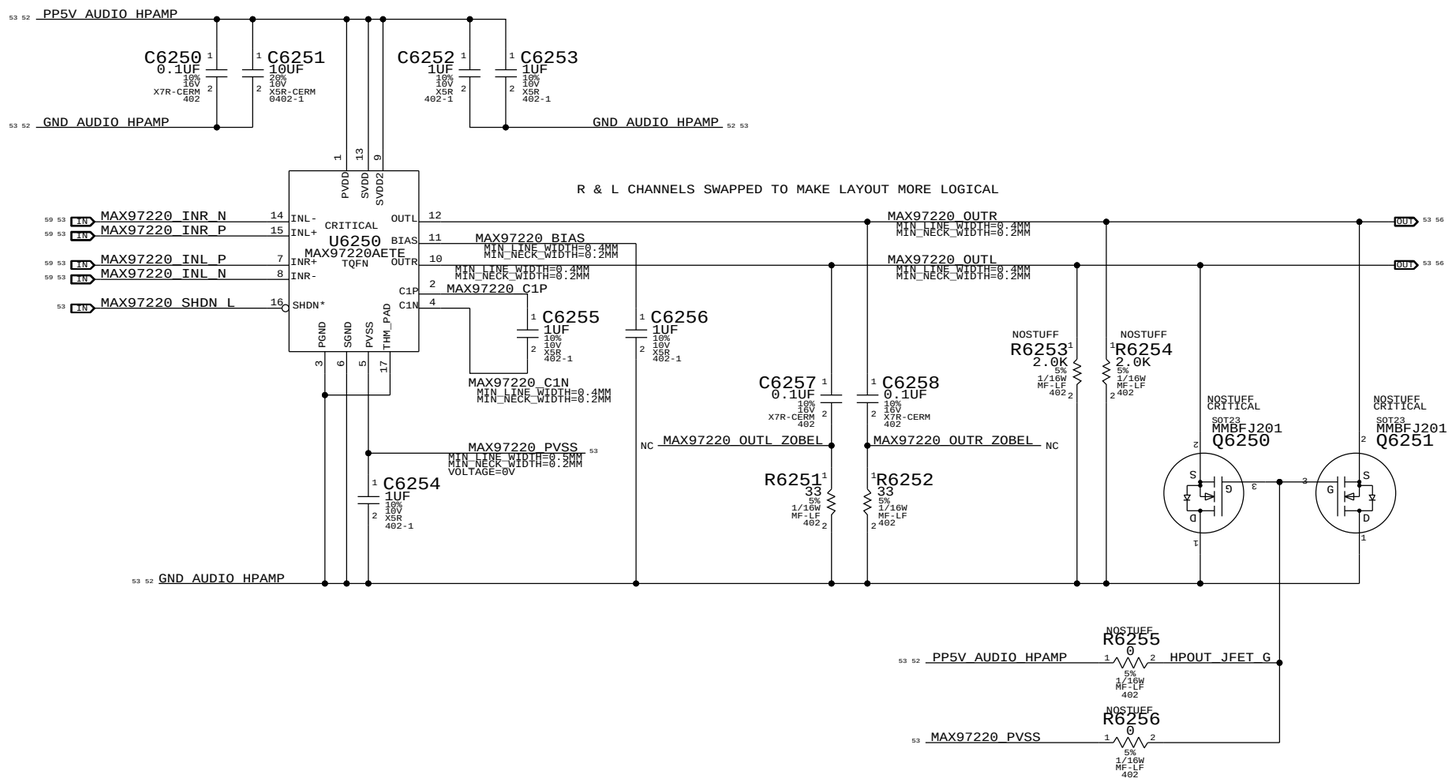
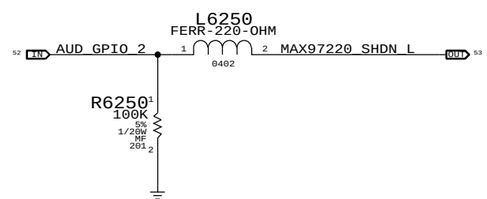


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0135	127S0120		C6261	THAILAND ALTERNATE
127S0135	127S0120		C6263	THAILAND ALTERNATE
127S0135	127S0120		C6271	THAILAND ALTERNATE
127S0135	127S0120		C6273	THAILAND ALTERNATE





SYNC_MASTER=D7 BREECE SYNC_DATE=01/03/2012

PAGE TITLE

AUDIO: HEADPHONE AMP

Apple Inc.

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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~18 HZ (0.22 UF)

55 6 IN =PP12V_S0_AUDIO_SPKRAMP

C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 10% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6303 FERR-1000-OHM 0402
C6308 4700PF 5% 50V NPO-C0G 805
59 53 52 IN AUD_LO1_L_N — AUD_LAMP_RINC_P — AUD_LAMP_RIN_P

L6302 FERR-1000-OHM 0402
C6309 4700PF 5% 50V NPO-C0G 805
59 53 52 IN AUD_LO1_L_P — AUD_LAMP_RINC_N — AUD_LAMP_RIN_N

L6300 FERR-1000-OHM 0402
C6310 0.22UF 10% 16V CERM 402
59 52 IN AUD_LO2_L_N — AUD_LAMP_LINC_P — AUD_LAMP_LIN_P

L6301 FERR-1000-OHM 0402
C6311 0.22UF 10% 16V CERM 402
59 52 IN AUD_LO2_L_P — AUD_LAMP_LINC_N — AUD_LAMP_LIN_N

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

58 55 52 40 6 =PP3V3_S0_AUDIO

34 35 36 37 PVDD

CRITICAL U6300 SSM3302 LFCSP

20	INR+	
19	INR-	
22	STDNR*	WOOFERS & TWEETERS ON UNDER MAC OS — 55 54 IN AUD_SPKRAMP_MAC_SHDN_L
16	MONO	54 IN AUD_LAMP_MONO
9	STDNL*	ONLY WOOFERS ON UNDER WINDOWS — 55 54 IN AUD_SPKRAMP_WIN_SHDN_L
11	INL+	
12	INL-	
21	GAIN	54 IN AUD_LAMP_GAIN
8	VREG/AVDD	54 AUD_LAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)
23	REGEN	
7 24	AGND	
41	THRM_PAD	
31 32 33 38 39 40	PGND	
17	THERM	TP_AUD_LAMP_THERM — NC
30	BOOTR+	C6313 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTRP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
28 29	OUTR+	
26 27	OUTR-	
25	BOOTR-	C6314 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTRN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
10	EDGE	54 IN AUD_LAMP_EDGE
1	BOOTL+	C6315 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTLP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
2 3	OUTL+	
4 5	OUTL-	
6	BOOTL-	C6316 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTLN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
18	NC	NC
13	NC	NC
14	NC	
15	NC	

C6317 2.2UF 20% 10V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

AUD_LAMP_OUTPR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) — 54 IN AUD_LAMP_OUTNR
CRITICAL L6305 110-OHM-3A DLY5ATN111SQ2 (SIGNAL_MODEL=EMPTY)
AUD_SPKR_LTWT_OUT_P — SIGNAL_MODEL=EMPTY CRITICAL C6323 1000PF 5% 25V NP0-C0G 402 — AUD_SPKR_LTWT_OUT_N
AUD_LAMP_OUTPR — 54 IN AUD_LAMP_OUTNR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)

AUD_LAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) — AUD_LAMP_OUTNL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
CRITICAL L6307 110-OHM-3A DLY5ATN111SQ2 (SIGNAL_MODEL=EMPTY)
AUD_SPKR_LWFR_OUT_N — SIGNAL_MODEL=EMPTY CRITICAL C6324 1000PF 5% 25V NP0-C0G 402 — AUD_SPKR_LWFR_OUT_P

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

SIGNAL_MODEL=EMPTY — CRITICAL C6320 1000PF 5% 25V NP0-C0G 402 — CRITICAL C6322 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY
SIGNAL_MODEL=EMPTY — CRITICAL C6319 1000PF 5% 25V NP0-C0G 402 — CRITICAL C6321 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY

L6308 FERR-1000-OHM 0402
52 IN AUD_CODEC_MICBIAS — AUD_SPKRAMP_MAC_SHDN_L OUT 54 55
R6301 100K 5% 1/16W MF-LF 402
NOSTUFF C6312 100PF 5% 50V CERM 402

R6308 0 5% 1/16W MF-LF 402
52 IN AUD_GPIO_3 — AUD_SPKRAMP_WIN_SHDN_L OUT 54 55
R6309 100K 5% 1/16W MF-LF 402
NOSTUFF C6318 100PF 5% 50V CERM 402

EDGE RATE CONTROL

	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	NOSTUFF
+15 DB	0 OHM	NOSTUFF
+18 DB	NOSTUFF	47 KOHM
+24 DB	47 KOHM	NOSTUFF

54 AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402
NOSTUFF R6305 0 5% 1/16W MF-LF 402
AUD_LAMP_EDGE OUT 54
AUD_LAMP_MONO OUT 54
R6303 0 5% 1/16W MF-LF 402
NOSTUFF R6306 0 5% 1/16W MF-LF 402
R6307 0 5% 1/16W MF-LF 402
AUD_LAMP_GAIN OUT 54

SYNC_MASTER=D7_BREECE SYNC_DATE=01/03/2012
PAGE TITLE: AUDIO: LEFT SPKR AMP

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RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~18 HZ (0.22 UF)

=PP12V_S0_AUDIO_SPKRAMP
C6400 10UF 10% 25V X5R 805
C6401 10UF 10% 25V X5R 805
C6402 0.1UF 10% 25V X5R 402
C6403 1UF 10% 25V X5R 603-1
C6404 0.1UF 10% 25V X5R 402
C6405 1UF 10% 25V X5R 603-1
CRITICAL C6406 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6400 FERR-1000-OHM 0402 — AUD_LO2_R_N — C6408 0.22UF 10% 16V CERM 402 — AUD_RAMP_RINC_P — AUD_RAMP_RIN_P
L6401 FERR-1000-OHM 0402 — AUD_LO2_R_P — C6409 0.22UF 10% 16V CERM 402 — AUD_RAMP_RINC_N — AUD_RAMP_RIN_N
L6402 FERR-1000-OHM 0402 — AUD_LO1_R_P — C6410 4700PF 5% 50V NP0-C0G 805 — AUD_RAMP_LINC_P — AUD_RAMP_LIN_P
L6403 FERR-1000-OHM 0402 — AUD_LO1_R_N — C6411 4700PF 5% 50V NP0-C0G 805 — AUD_RAMP_LINC_N — AUD_RAMP_LIN_N

=PP3V3_S0_AUDIO

CRITICAL U6400 SSM3302 LFCSP

20	INR+	
19	INR-	
22	STDNR*	AUD_SPKRAMP_WIN_SHDN_L (ONLY WOOFERS ON UNDER WINDOWS)
16	MONO	AUD_RAMP_MONO
9	STDNL*	AUD_SPKRAMP_MAC_SHDN_L (WOOFERS & TWEETERS ON UNDER MAC OS)
11	INL+	
12	INL-	
21	GAIN	AUD_RAMP_GAIN
8	VREG/AVDD	AUD_RAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)
23	REGEN	
34,35,36,37	PVDD	
7,24,41	AGND	
31,32,33,38,39,40	PGND	
17	THERM	TP_AUD_RAMP_THERM = NC
30	BOOTR+	C6413 0.22UF — AUD_RAMP_BOOTRP
28,29	OUTR+	
26,27	OUTR-	
25	BOOTR-	C6414 0.22UF — AUD_RAMP_BOOTRN
10	EDGE	AUD_RAMP_EDGE
1	BOOTL+	C6415 0.22UF — AUD_RAMP_BOOTLP
2,3	OUTL+	
4,5	OUTL-	
6	BOOTL-	C6416 0.22UF — AUD_RAMP_BOOTLN
18	NC	
13	NC	
NC	14	
15		

C6417 2.2UF 20% 10V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

AUD_RAMP_OUTPR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) — SIGNAL_MODEL=EMPTY — CRITICAL L6405 110-OHM-3A DLY5ATN111SQ2 — AUD_SPKR_RWFR_OUT_P — SIGNAL_MODEL=EMPTY CRITICAL C6423 1000PF 5% 25V NP0-C0G 402 — AUD_SPKR_RWFR_OUT_N
AUD_RAMP_OUTNR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
AUD_RAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) — SIGNAL_MODEL=EMPTY — CRITICAL L6407 110-OHM-3A DLY5ATN111SQ2 — AUD_SPKR_RTWT_OUT_P — SIGNAL_MODEL=EMPTY CRITICAL C6424 1000PF 5% 25V NP0-C0G 402 — AUD_SPKR_RTWT_OUT_N
AUD_RAMP_OUTNL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)

CRITICAL C6420 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY
CRITICAL C6422 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY
CRITICAL C6419 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY
CRITICAL C6421 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY

EDGE RATE CONTROL

	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	NOSTUFF
+15 DB	0 OHM	NOSTUFF
+18 DB	NOSTUFF	47 KOHM
+24 DB	47 KOHM	NOSTUFF

AUD_RAMP_AVDD
R6404 0 5% 1/16W MF-LF 402 — AUD_RAMP_EDGE
NOSTUFF R6405 0 5% 1/16W MF-LF 402
R6403 0 5% 1/16W MF-LF 402 — AUD_RAMP_MONO
NOSTUFF R6406 0 5% 1/16W MF-LF 402 — AUD_RAMP_GAIN
R6407 0 5% 1/16W MF-LF 402

SYNC_MASTER=D7_BREECE SYNC_DATE=01/03/2012
PAGE TITLE: AUDIO: RIGHT SPKR AMP

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MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640

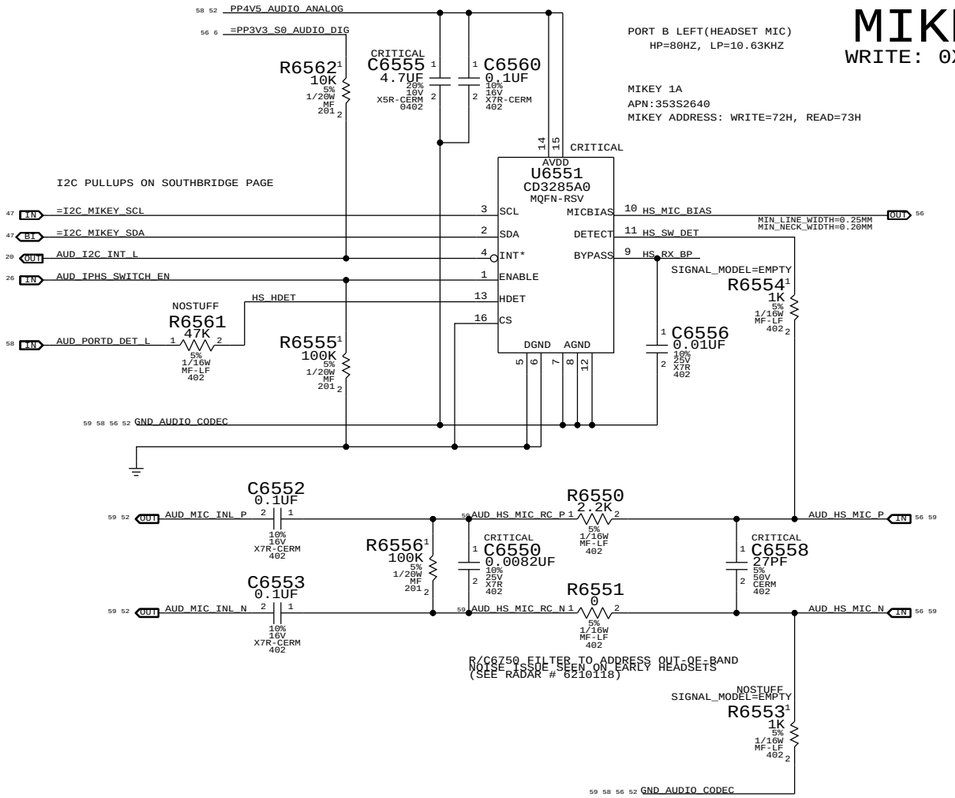
PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

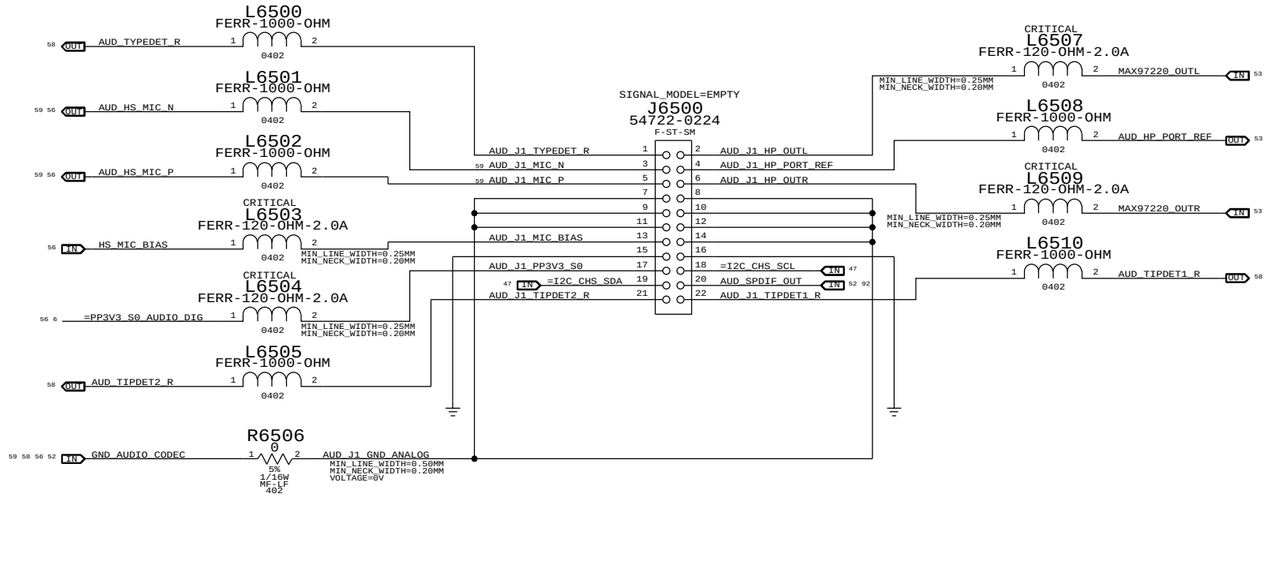
MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

AUDIO JACK: HP CONNECTOR WITH MIKEY
PLACE XWS 6500 & 6501 AT J6500 PINS





SYNC_MASTER=D7_BREECE SYNC_DATE=01/03/2013

PAGE TITLE: AUDIO: Jack, Mikey, CHS Switch

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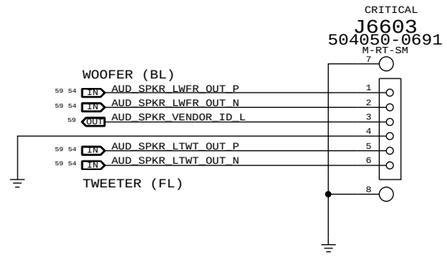
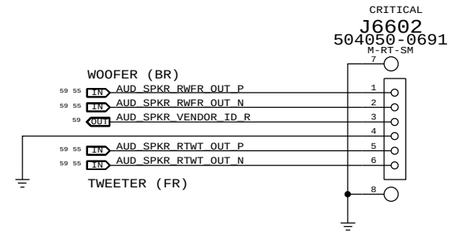
SPEAKER CABLE CONNECTORS

APPLE P/N 998-4119



APPLE P/N 998-4119



SYNC_MASTER=D7_BREECE SYNC_DATE=01/03/2012

PAGE TITLE
Audio: Spkr/Mic Conn.

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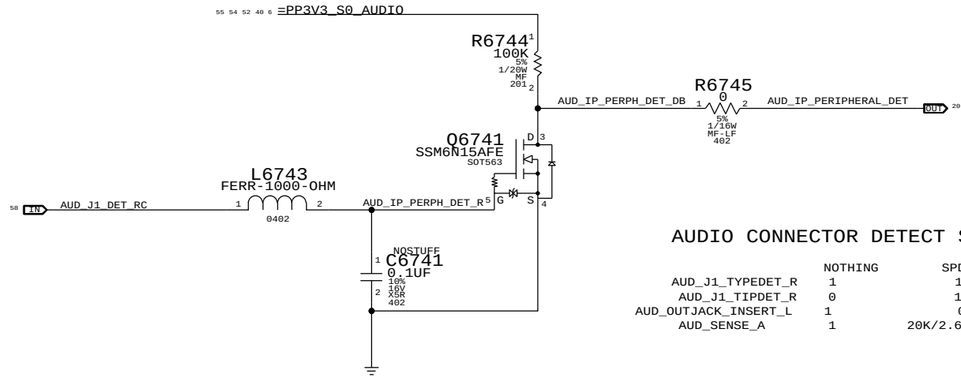
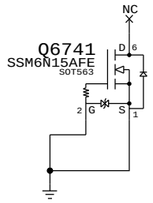
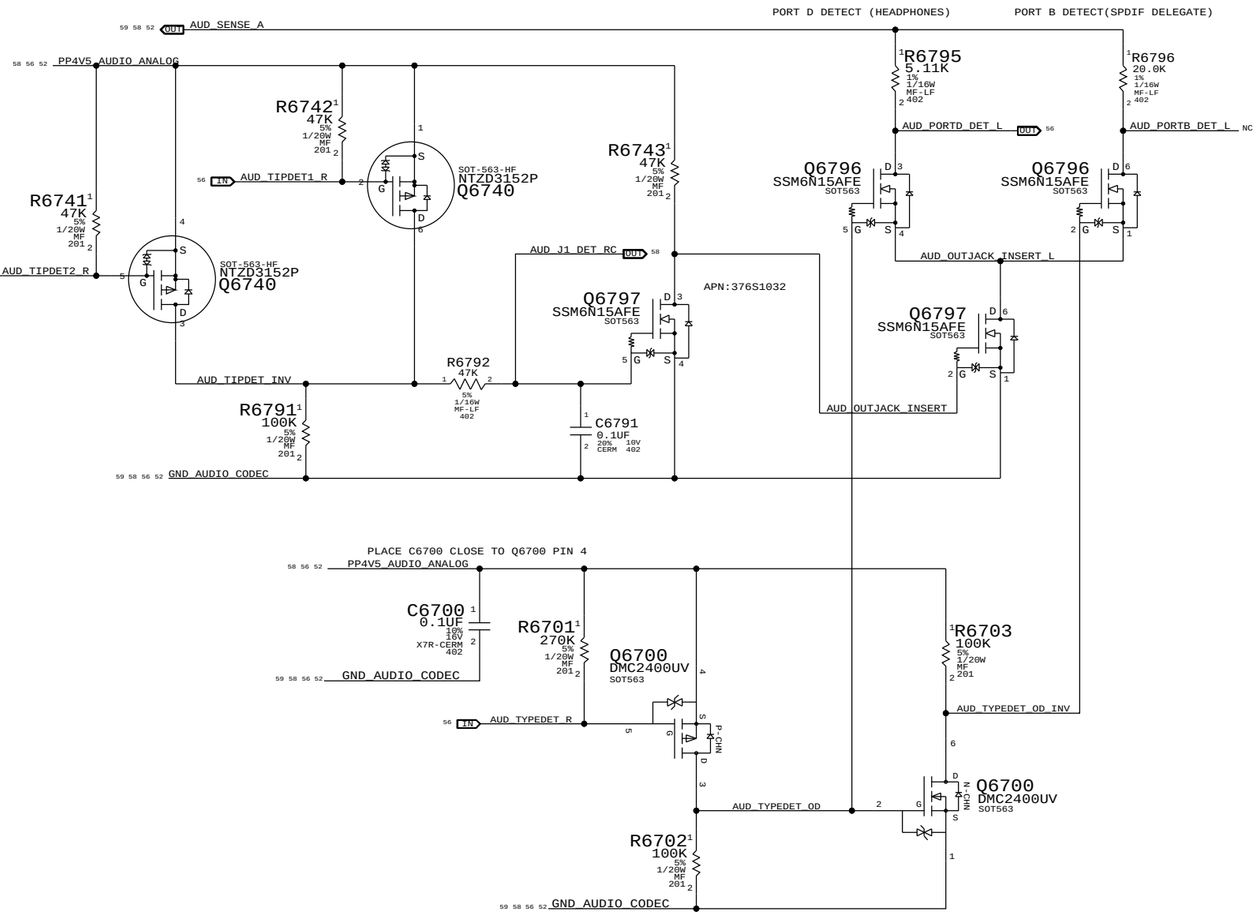
IPHS HS Detect Debounce CKT

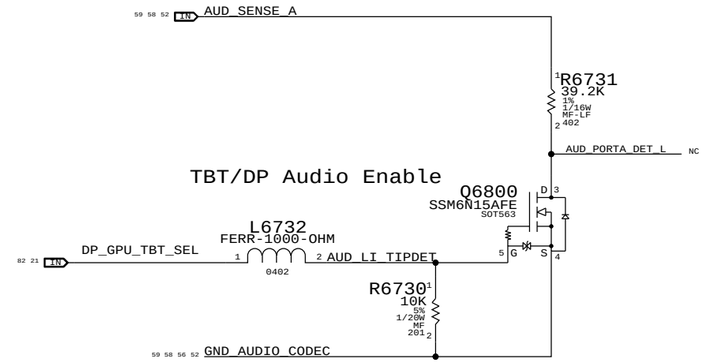


AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV







SYNC_MASTER=D7_BREECE SYNC_DATE=01/03/2012

PAGE TITLE
AUDIO: Detects/Grounding

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	PANTHER POINT GPIO 16	PANTHER POINT GPIO 5 (RCV0_INT) PANTHER POINT GPIO 3 (PERIPH DET)

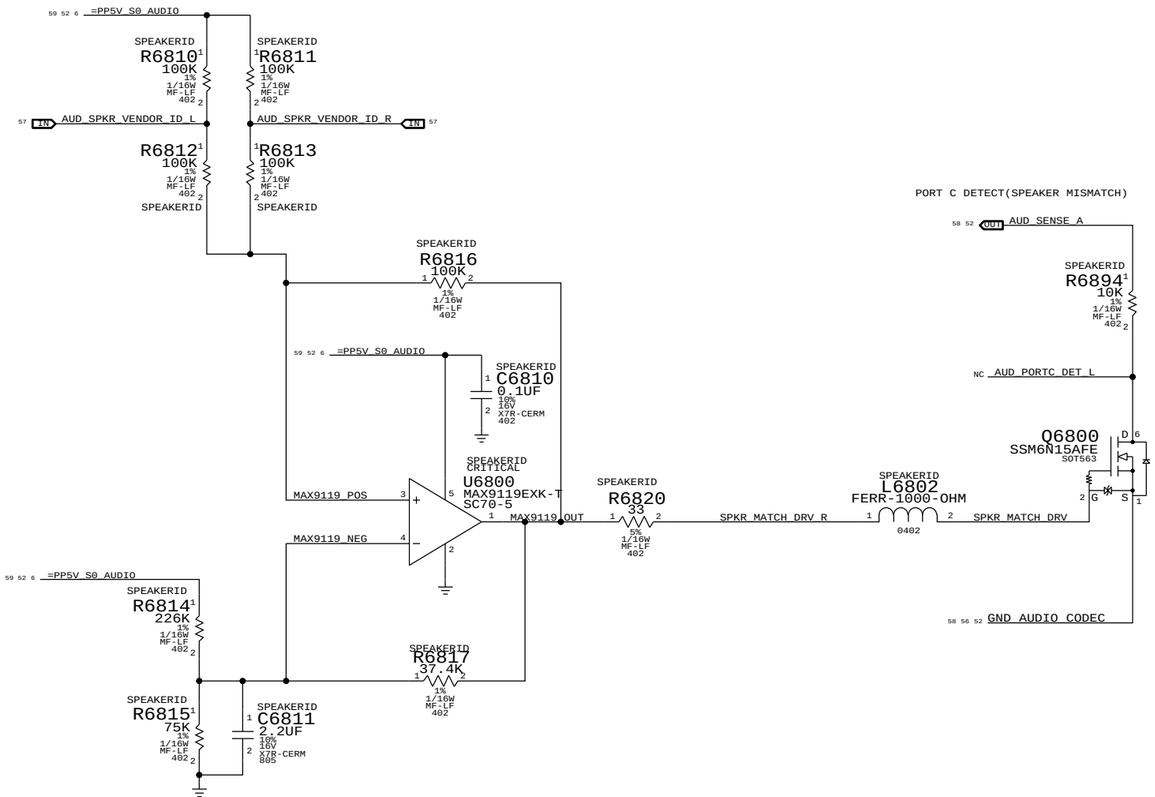
OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM



ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
1545 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	52 53 54
1546 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	52 53 54
1547 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	53
1548 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	53
1549 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	52 53 55
1550 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	52 53 55
1551 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	53
1552 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	53
1553 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	52 54
1554 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	52 54
1555 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	52 55
1556 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	52 55
1557 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	55
1558 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	55
1559 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	55
1560 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	55
1561 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	55
1562 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	55
1563 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	55
1564 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	55
1565 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	54
1566 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	54
1567 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	54
1568 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	54
1569 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	54
1570 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	54
1571 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	54
1572 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	54
1573 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INL_P	53
1574 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INL_N	53
1575 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INR_P	53
1576 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INR_N	53
1577 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	55 57
1578 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	55 57
1579 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	55 57
1580 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	55 57
1581 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	54 57
1582 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	54 57
1583 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	54 57
1584 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	54 57
1585 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	52 56
1586 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	52 56
1587 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	56
1588 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	56
1589 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	56
1590 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	56
1591 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	56
1592 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	56

SYNC_MASTER=D7_BREECE SYNC_DATE=01/03/2012

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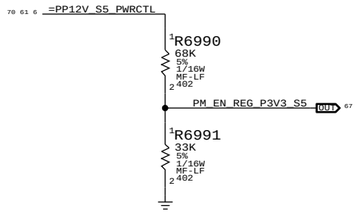
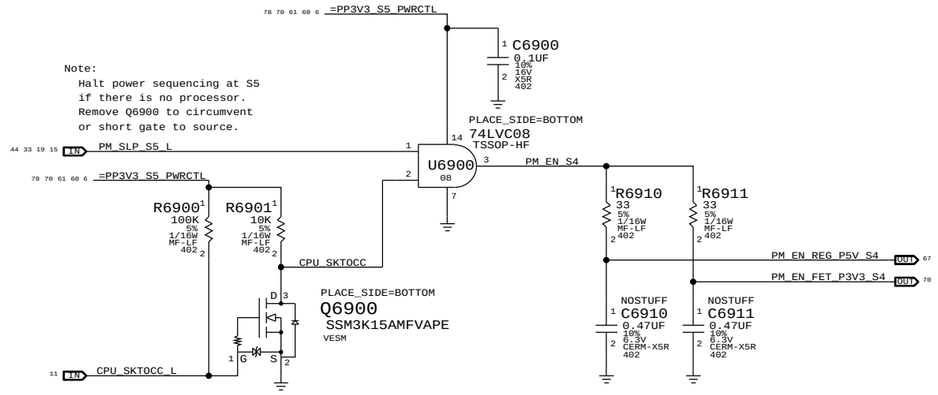
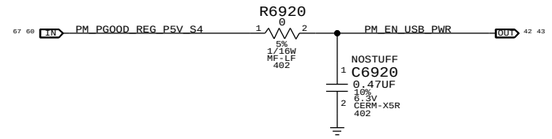
S5 Soft Enable



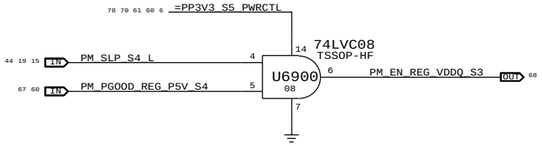
S4 Enables



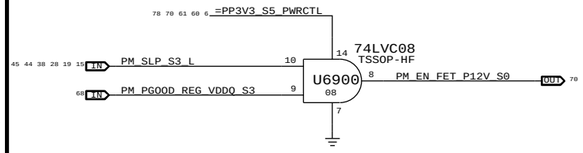
S4 USB Enable

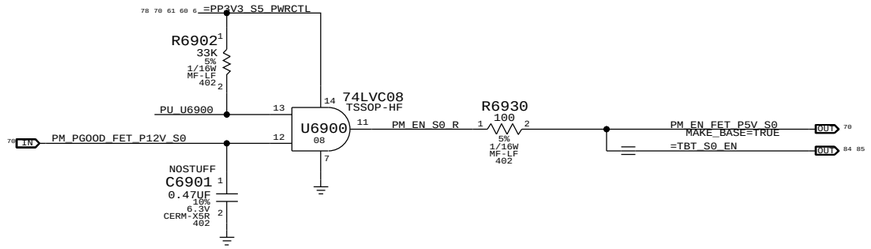


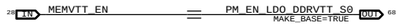
S3 VDDQ Enable

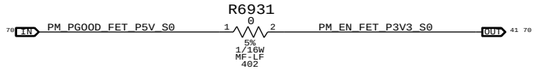


S0 Enables

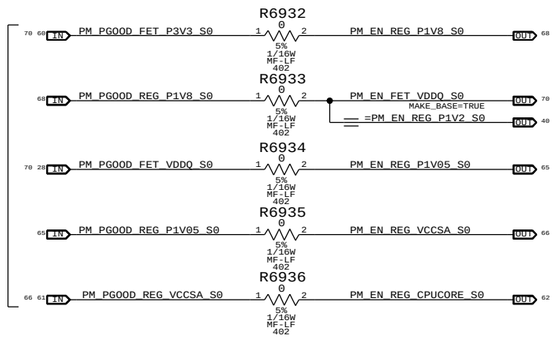




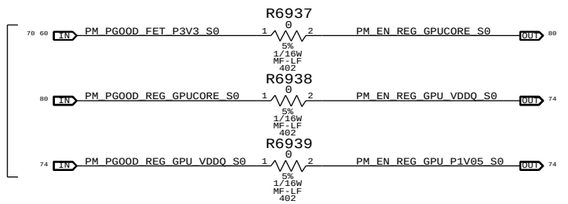




CPU/PCH Sequencing



GPU Sequencing



Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.8 V 1.5 V, PCH Core/PLL/VRM)
Uncore: VccSA, VDDQ, VccA (1.8 V), VccIO (VccSA, VccA, and VccIO must ramp within 50 ms of each other)

Notes on sequencing requirements

Intel:

1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK

NVIDIA:

1. 3V3_S0 must ramp first
2. IFPA/B_IOVDD (1.8 V) can ramp simultaneously or after 3V3_S0 (unused)
3. NVVDD (GPU_CORE) must ramp after IFPA/B_IOVDD
4. VDDQ must ramp after CPU_CORE
5. PEX_VDD with IFPC/D/E/F_IOVDD (1.05V) must ramp after VDDQ
6. All rails must reach their target voltages in more than 40 uS

SYNC_MASTER=D7_NICK SYNC_DATE=12/13/2011

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PM Regulator Enables

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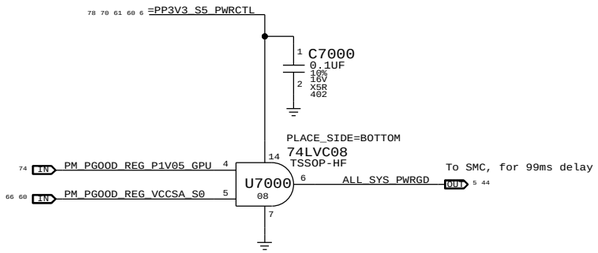
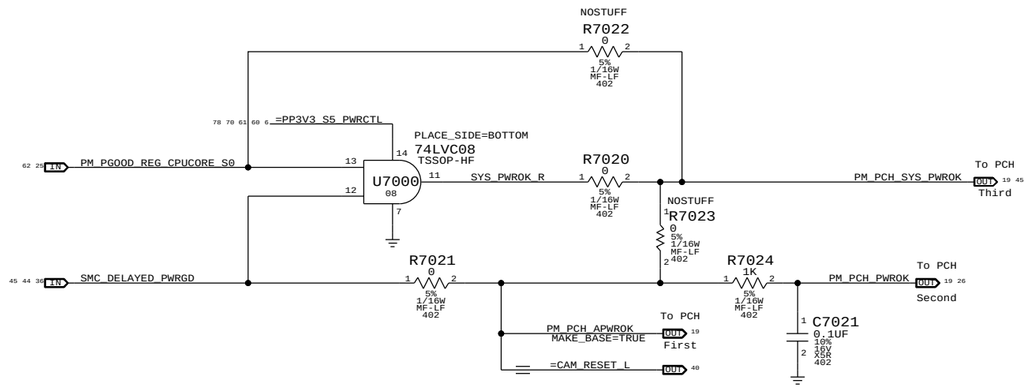
Platform and UnCore Power Good

Derive SMC ALL_SYS_PWRGD

Note: GPU power goods are implicitly included because the power goods for VDDQ, DPVDDC, and GPU Core are wired-or together



PCH Power Goods



Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

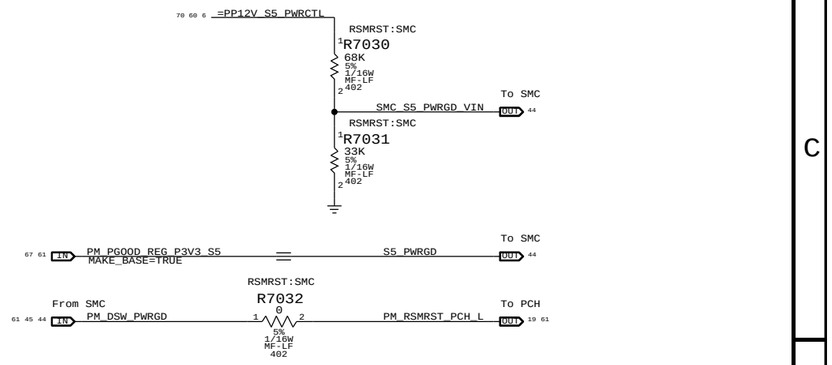
Note:
The iMac K70K72 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Primary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation.

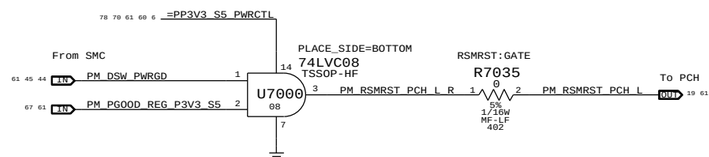
SMC de-asserts RSMRST# (PM_DSW_PWRGD) when S5_PWRGD input is asserted and SMC_S5_PWRGD_VIN input is above comparator input level of 1.5 V.

SMC asserts RSMRST# (PM_DSW_PWRGD) when SMC_S5_PWRGD_VIN input drops from 1.8 V to 1.5 V (as implemented) when 12 V S5 rail drops to 10 V.



Secondary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC_MASTER=D7_NICK SYNC_DATE=12/13/2011

PAGE TITLE: PM Power Good

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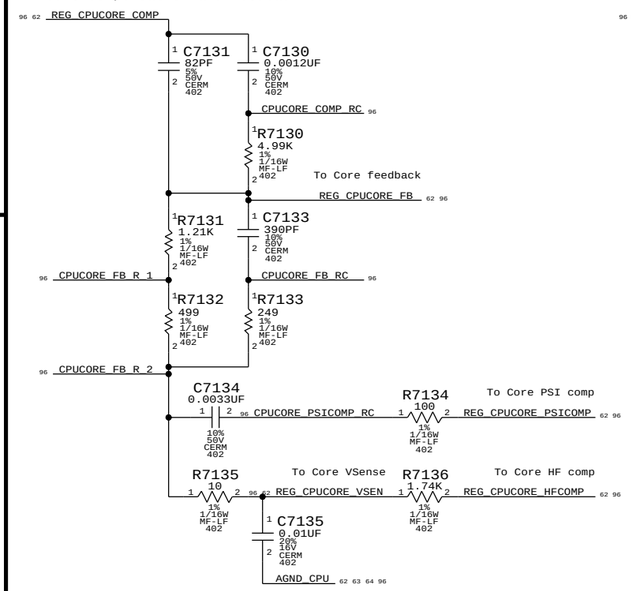
CPU Core S0 Regulator

Max avg current: ? A (design)/ 41.05 A (budget)
Max peak current: ? A (design)/75.05 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

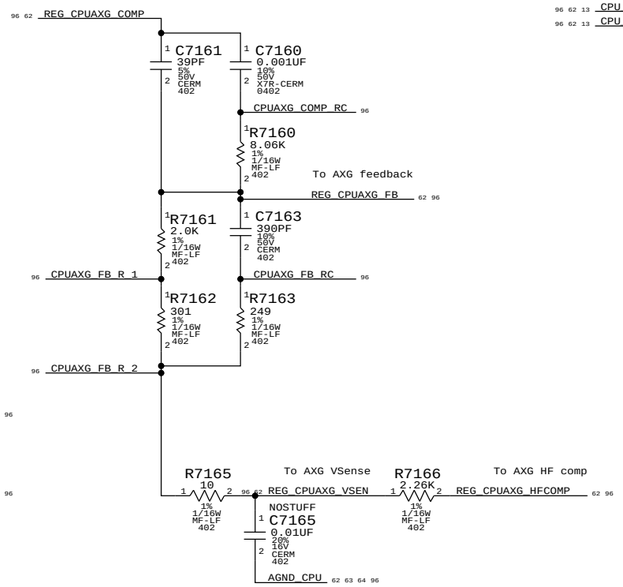
Core compensation and feedback



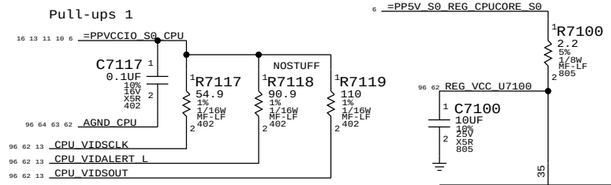
CPU AXG S0 Regulator

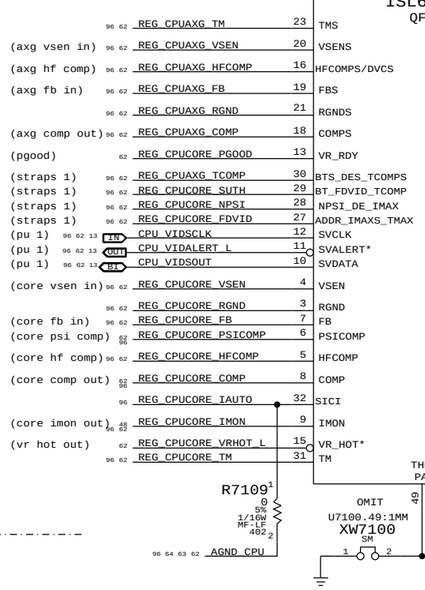
Max avg current: ? A (design)/ 10 A (budget)
Max peak current: ? A (design)/ 30 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

AXG compensation and feedback

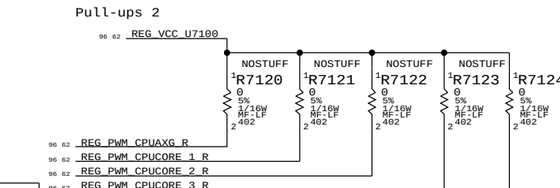


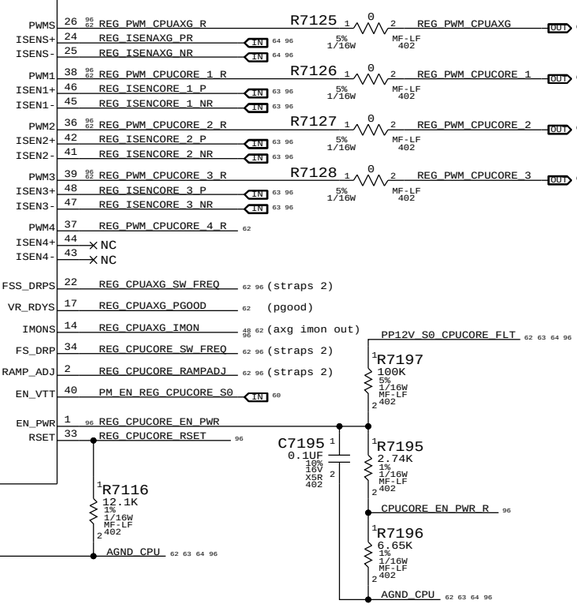
Pull-ups 1



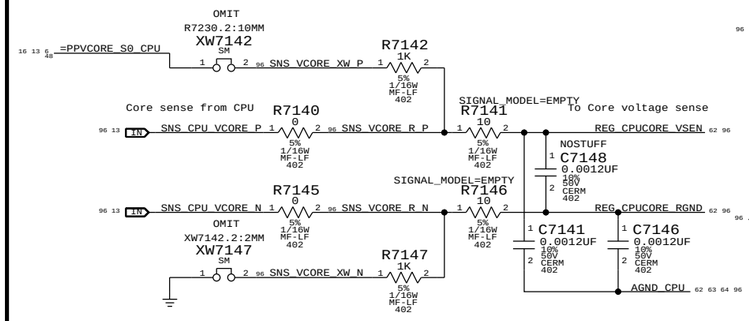


Pull-ups 2

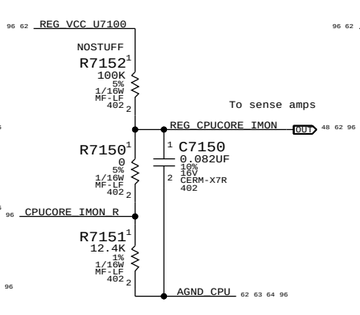




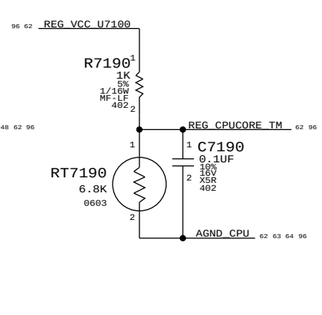
Core voltage sense input



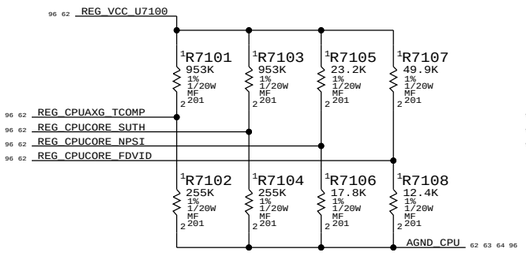
Core IMON output



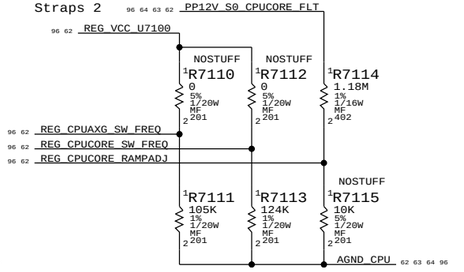
Core temp measurement



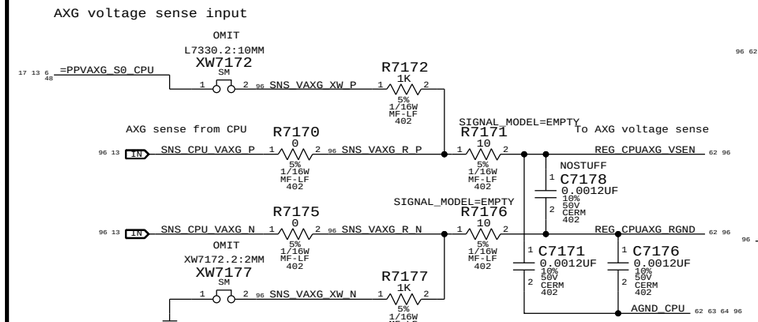
Straps 1



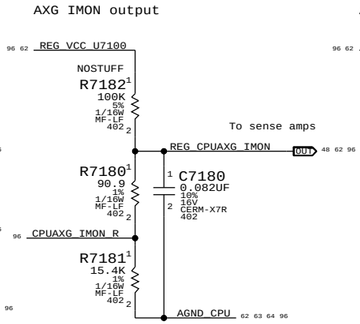
Straps 2



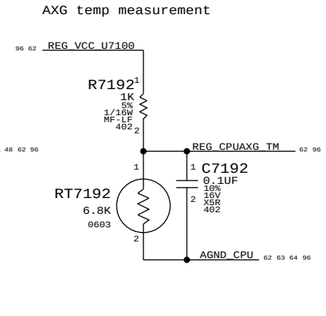
AXG voltage sense input



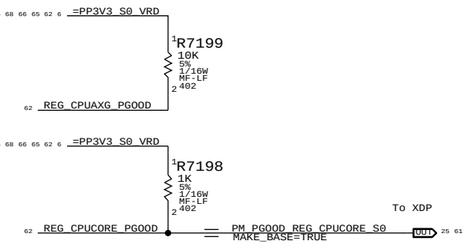
AXG IMON output



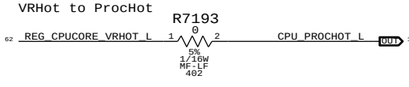
AXG temp measurement



Power goods



VRHot to ProcHot



SYNC_MASTER=D7_NICK SYNC_DATE=01/04/2012

PAGE TITLE
VReg CPU Core/AXG Cntl

Apple Inc.

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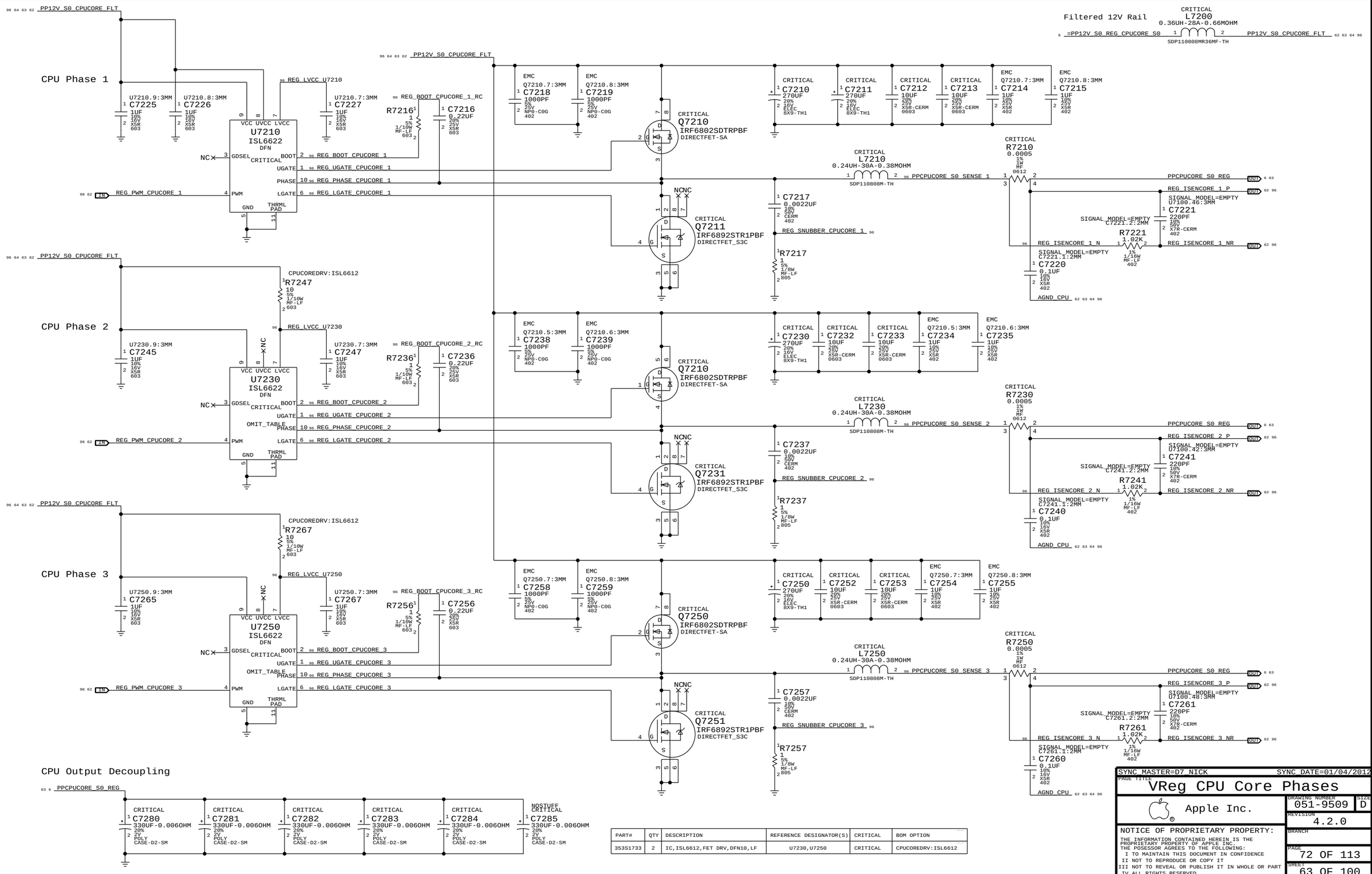

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1733	2	IC,ISL6612,FET DRV,DFN10,LF	U7230,U7250	CRITICAL	CPUCOREDRV:ISL6612

AXG Phase

96 64 63 62 PP12V_S0_CPUCORE_FLT

NOSTUFF
R7347
10
5%
1/10W
MF-LF
603

REG_LVCC_U7330

U7330.9:3MM
C7345
1UF
10%
16V
X5R
603

U7330.8:3MM
C7346
1UF
10%
16V
X5R
603

U7330.7:3MM
C7347
1UF
10%
16V
X5R
603

U7330
ISL6622
DFN

VCC UVCC LVCC

NC
GDSEL
CRITICAL

BOOT 96 REG_BOOT_CPUAXG
UGATE 96 REG_UGATE_CPUAXG
PHASE 96 REG_PHASE_CPUAXG
LGATE 96 REG_LGATE_CPUAXG

96 62 REG_PWM_CPUAXG
PWM

GND
THRML PAD

96 REG_BOOT_CPUAXG_RC
R7336
1
5%
1/10W
MF-LF
603

C7336
0.22UF
20%
25V
X5R
603

96 64 63 62 PP12V_S0_CPUCORE_FLT

EMC
Q7250.5:3MM
C7338
1000PF
5%
25V
NP0-C0G
402

EMC
Q7250.6:3MM
C7339
1000PF
5%
25V
NP0-C0G
402

CRITICAL
Q7250
IRF6802SDTRPBF
DIRECTFET-SA

CRITICAL
Q7331
IRF6892STR1PBF
DIRECTFET_S3C

NC
NC

C7337
0.0022UF
10%
50V
CERM
402

REG_SNUBBER_CPUAXG 96

R7337
1
5%
1/8W
MF-LF
805

CRITICAL
C7330
270UF
20%
16V
ELEC
8X9-TH1

CRITICAL
C7331
270UF
20%
16V
ELEC
8X9-TH1

CRITICAL
C7332
10UF
20%
25V
X5R-CERM
0603

CRITICAL
C7333
10UF
20%
25V
X5R-CERM
0603

EMC
Q7250.5:3MM
C7334
1UF
10%
25V
X5R
402

EMC
Q7250.6:3MM
C7335
1UF
10%
25V
X5R
402

CRITICAL
L7330
0.24UH-30A-0.38MOHM
SDP110808M-TH

96 PPCPUAXG_S0_SENSE

CRITICAL
R7330
0.0005
1%
1W
MF
0612

PPCPUAXG_S0_REG OUT 6 64

SIGNAL_MODEL=EMPTY
C7342.1:2MM
R7342
301
1%
1/10W
MF-LF
402

REG_ISENAXG_P 96

REG_ISENAXG_PR OUT 62 96

SIGNAL_MODEL=EMPTY
R7342.1:2MM

SIGNAL_MODEL=EMPTY
C7341.2:2MM
C7341
220PF
10%
50V
X7R-CERM
402

R7341
1.02K
1%
1/10W
MF-LF
402

REG_ISENAXG_N 96

SIGNAL_MODEL=EMPTY
R7342.1:2MM
C7340
0.1UF
10%
16V
X5R
402

AGND_CPU 62 63 64 96

REG_ISENAXG_NR OUT 62 96

SIGNAL_MODEL=EMPTY
U7100.24:3MM
C7342
120PF
5%
50V
CERM
402

AGND_CPU 62 63 64 96

AXG Phase

64 6 PPCPUAXG_S0_REG

CRITICAL
C7390
330UF-0.006OHM
20%
2V
POLY
CASE-D2-SM

CRITICAL
C7391
330UF-0.006OHM
20%
2V
POLY
CASE-D2-SM

CRITICAL
C7392
330UF-0.006OHM
20%
2V
POLY
CASE-D2-SM

CRITICAL
C7393
330UF-0.006OHM
20%
2V
POLY
CASE-D2-SM

CRITICAL
C7396
330UF-0.006OHM
20%
2V
POLY
CASE-D2-SM

CRITICAL
C7397
330UF-0.006OHM
20%
2V
POLY
CASE-D2-SM

C7394
10UF
20%
10V
X5R
603

C7395
10UF
20%
10V
X5R
603

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VReg CPU AXG Phases

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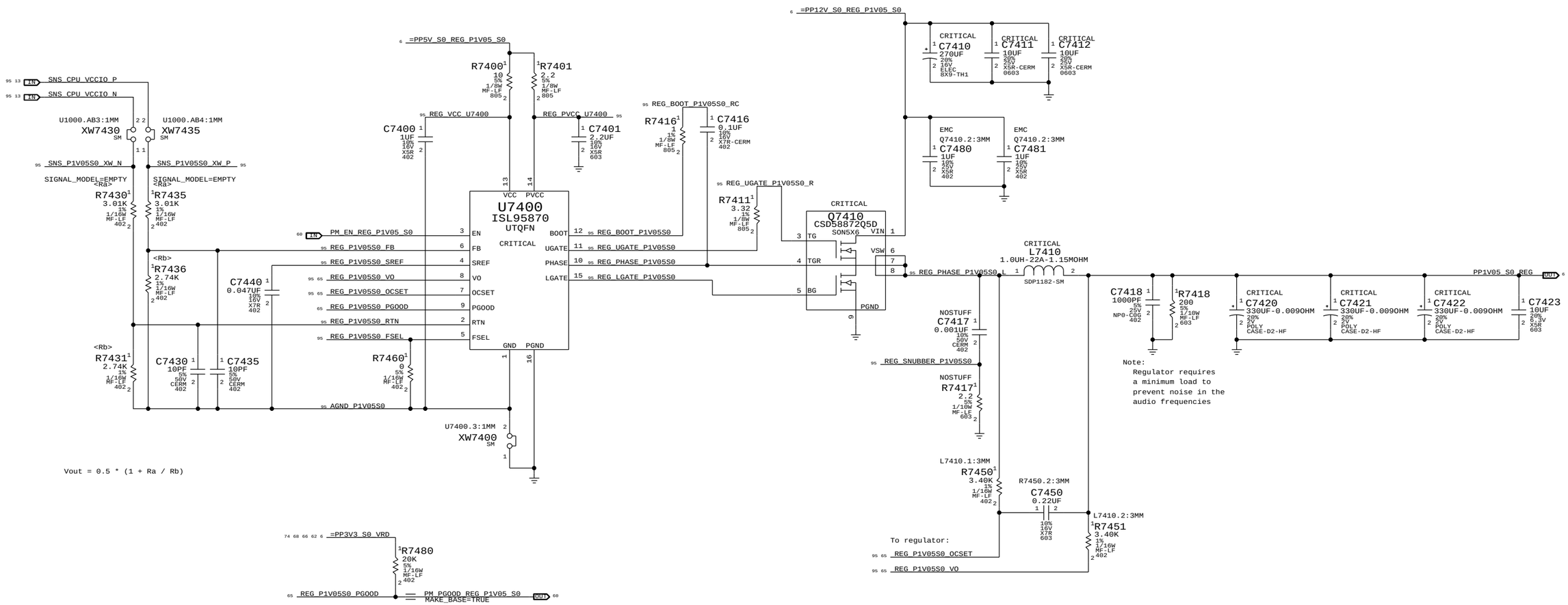
CPU VccIO/PCH (1.05V) S0 Regulator

Max avg current: ? A (design)/ 14.38 A (budget)
Max peak current: ? A (design)/ 18.38 A (budget)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



Vout = 0.5 * (1 + Ra / Rb)

SYNC_MASTER=D7_NICK SYNC_DATE=01/04/2012

PAGE TITLE: VReg CPU/PCH 1.05V S0

Apple Inc.

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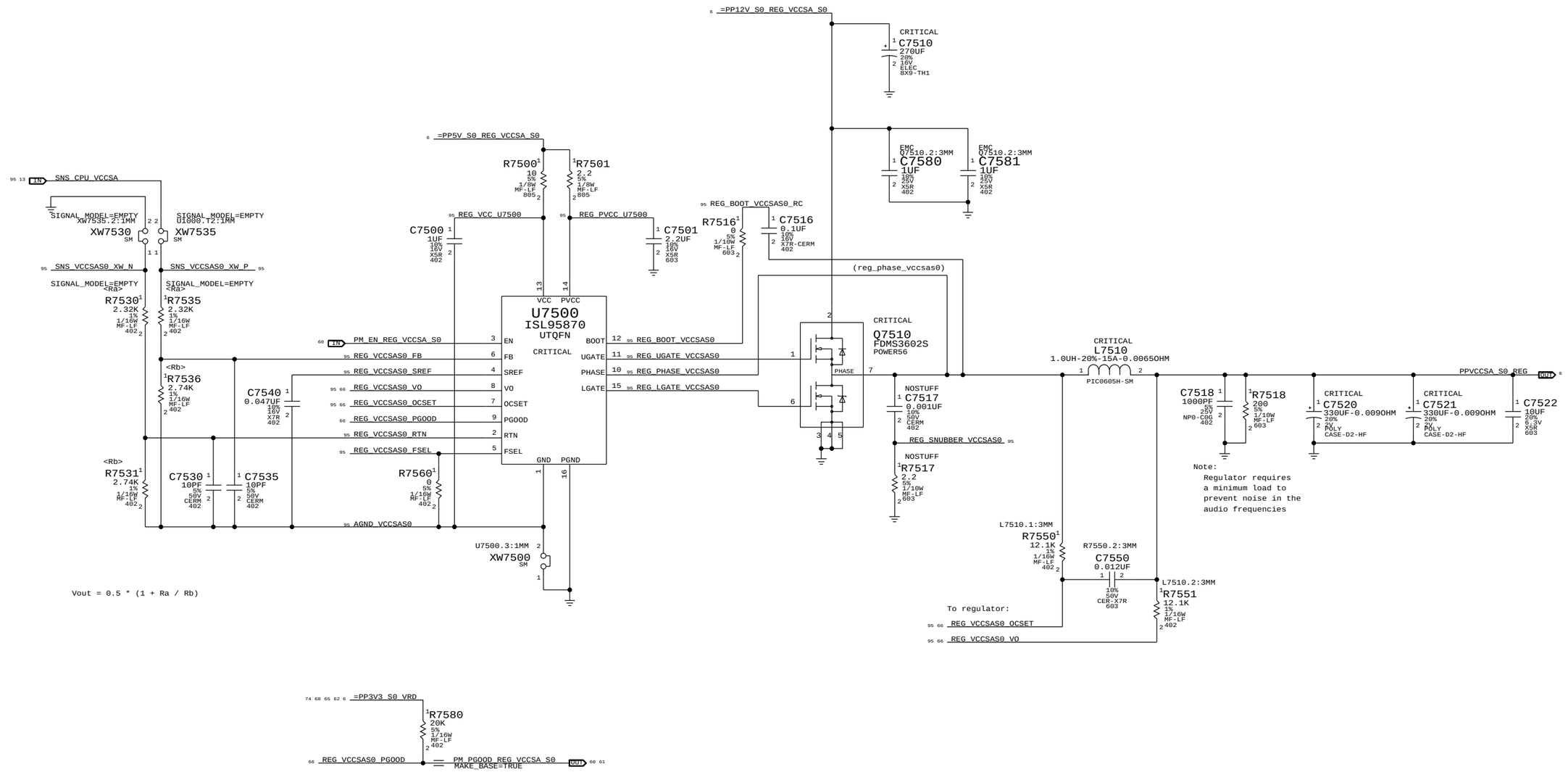
CPU VccSA (0.925V) S0 Regulator

Max avg current: ? A (design)/ 1.51 A (budget)
Max peak current: ? A (design)/ 8.76 A (budget)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



SYNC_MASTER=D7 NICK SYNC_DATE=01/04/2012

PAGE TITLE
VReg CPU VccSA S0

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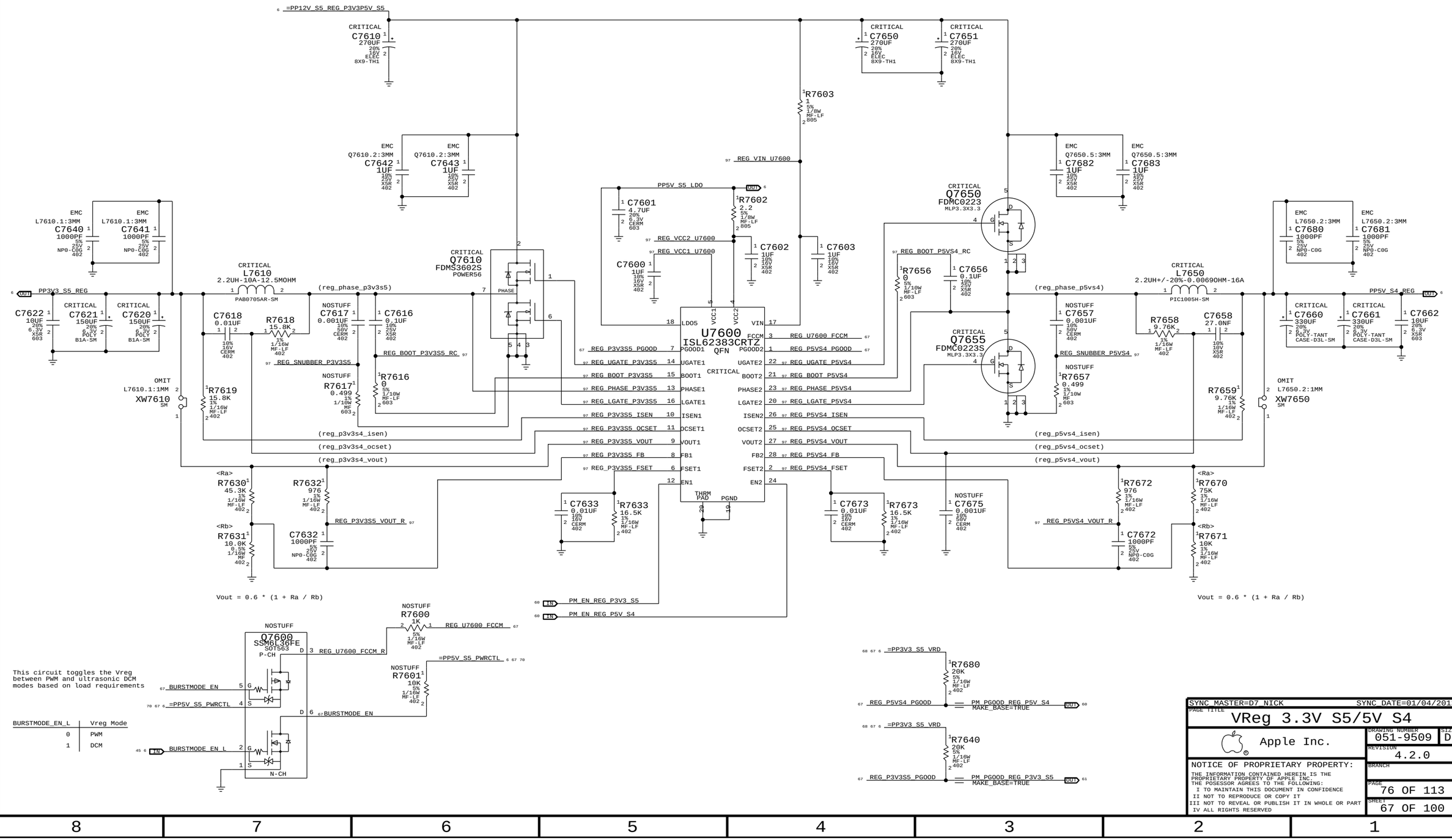
3.3V S5 Regulator

Max avg current: 6 A (design)/ 4.85 A (budget)
Max peak current: ? A (design)/ 6.6 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz

5V S4 Regulator

Max avg current: 10 A (design)/ 6.08 A (budget)
Max peak current: ? A (design)/ 6.9 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz



SYNC_MASTER=D7_NICK SYNC_DATE=01/04/2012

PAGE TITLE: VReg 3.3V S5/5V S4

Apple Inc.

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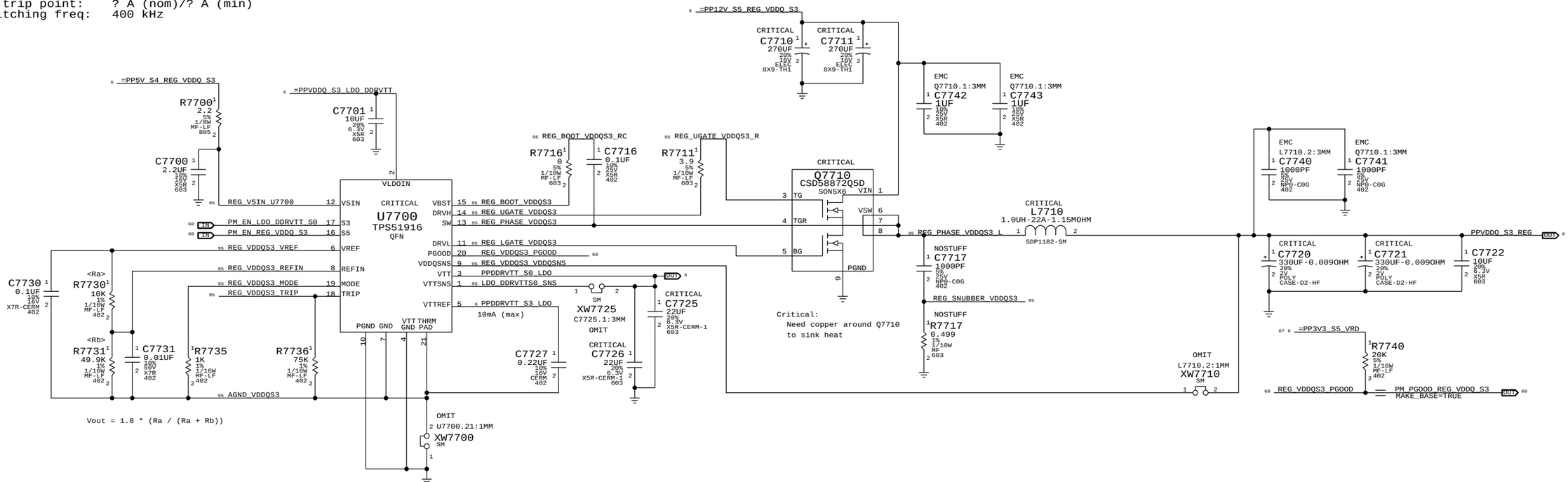
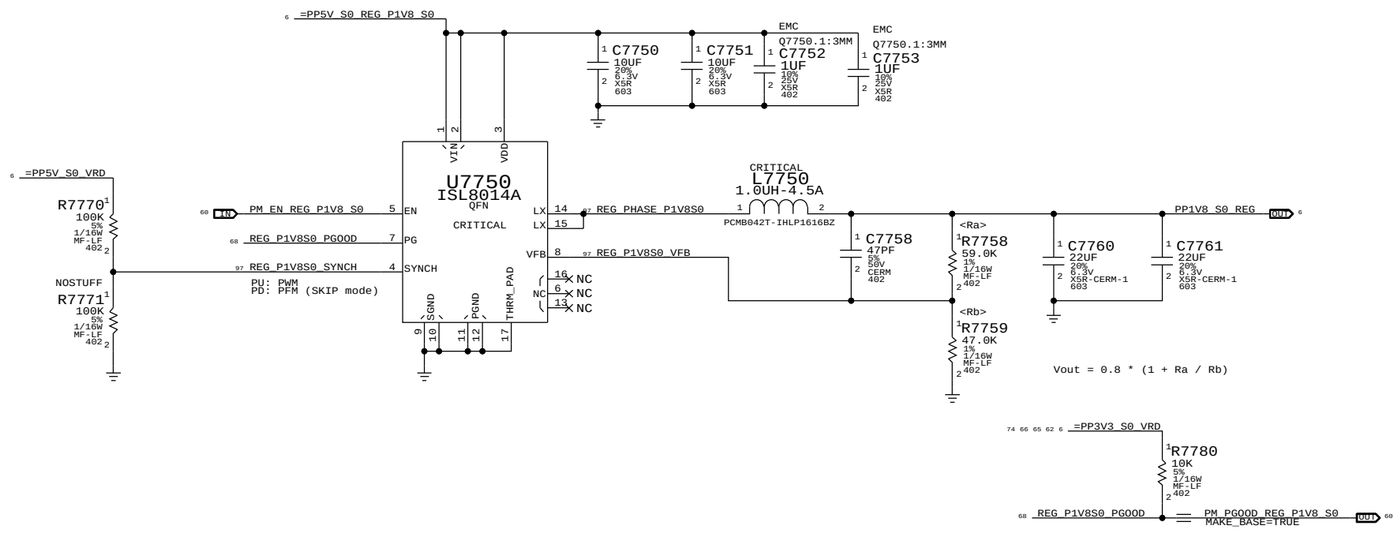
VDDQ (1.5V) S3 Regulator

Max avg current: ? A (design)/ 8 A (budget)
Max peak current: ? A (design)/ 17.8 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 400 kHz



1.8V S0 Regulator

Max avg current: 3 A (design)/ 0.61 A (budget)
Max peak current: ? A (design)/ 1.83 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



SYNC_MASTER=D7 NICK SYNC_DATE=01/04/2012

PAGE TITLE: VReg VDDQ and 1.8V S0

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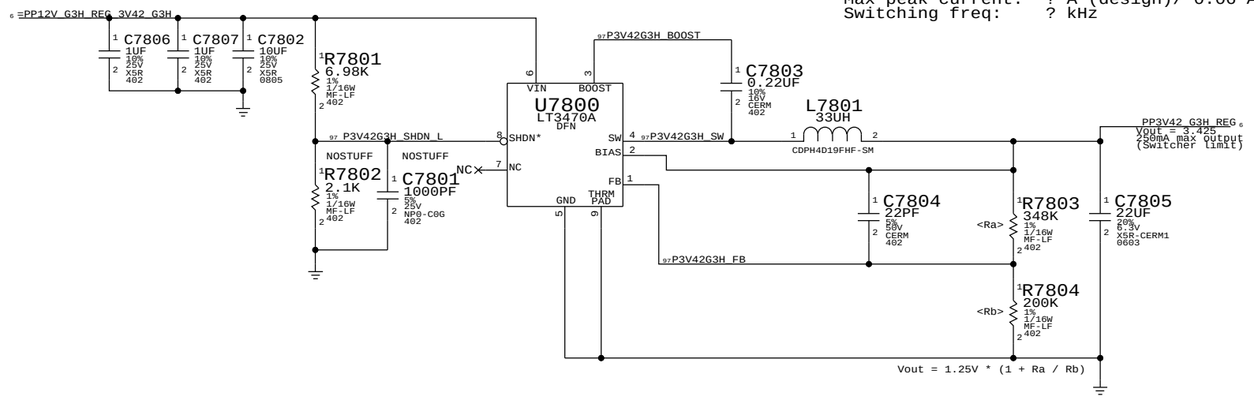
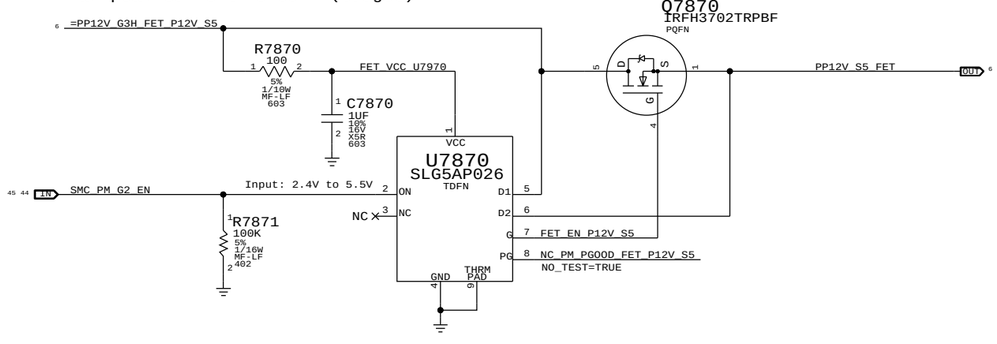
3.425V "G3Hot" Regulator

Max avg current: ? A (design)/ 0 A (budget)
Max peak current: ? A (design)/ 0.06 A (budget)
Switching freq: ? kHz



12V S5 FET

Max avg current: 7.03 A (budget)
Max peak current: 9.69 A (budget)



SYNC_MASTER=D7_NICK	SYNC_DATE=01/04/2012
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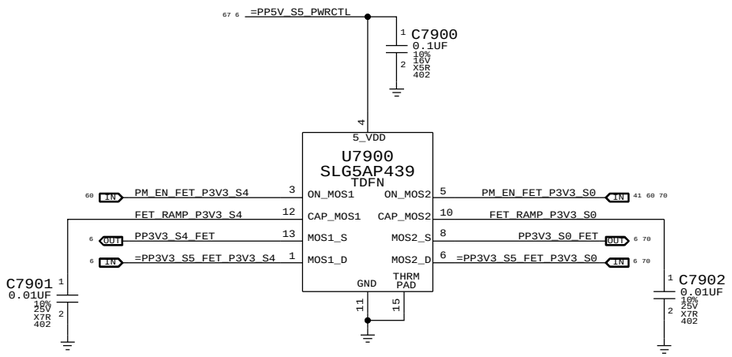
3.3V S4 FET

Max avg current: 0.85 A (budget)
Max peak current: 1.48 A (budget)

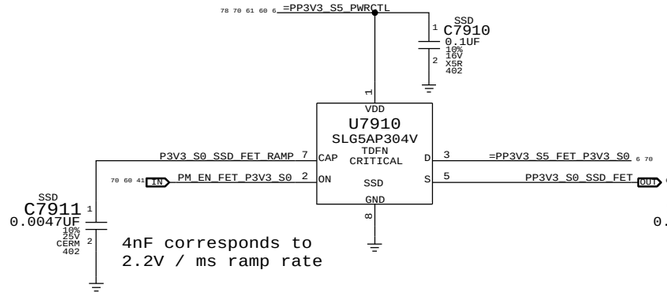


3.3V S0 FET

Max avg current: 1.7 A (budget)
Max peak current: 1.82 A (budget)

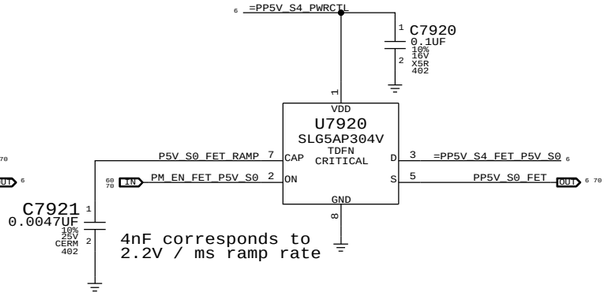
3V3 S0 SSD

Max avg current: 2.12 A (budget)
Max peak current: 3.03 A (budget)

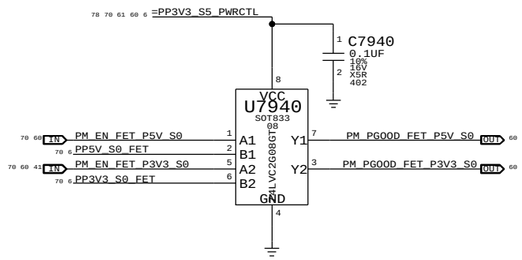


5V S0 FET

Max avg current: 1.26 A (budget)
Max peak current: 2.08 A (budget)

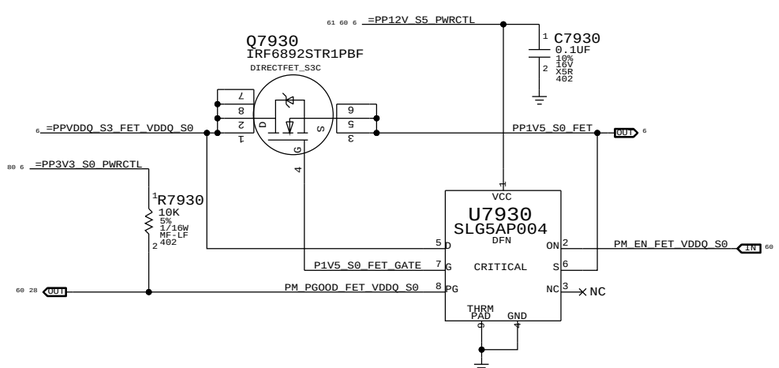


5V / 3V3 S0 PGOODs



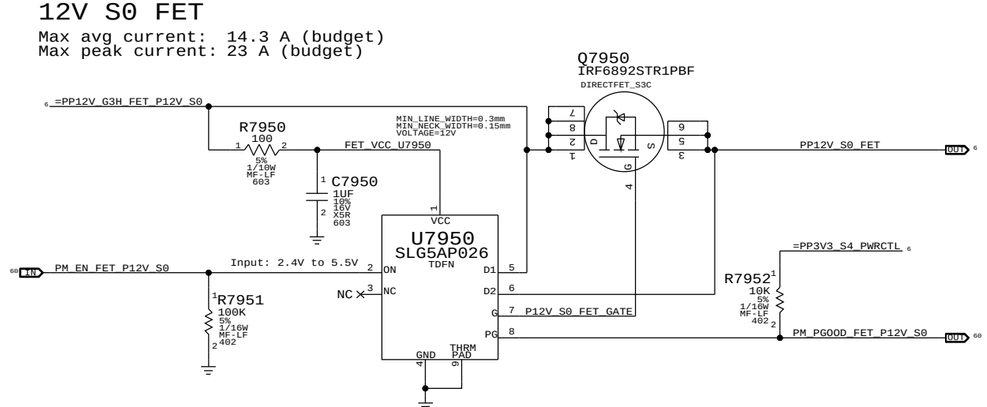
1.5V S0 FET

Max avg current: 1.27 A (budget)
Max peak current: 4.8 A (budget)



12V S0 FET

Max avg current: 14.3 A (budget)
Max peak current: 23 A (budget)



SYNC_MASTER=D7_NICK SYNC_DATE=01/04/2012

PAGE TITLE
FET-Controlled S0 and S4

Apple Inc.

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Page Notes

Power aliases required by this page:

- +PP3V3_GPU_VDD33

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

Polarity swaps intended on Lanes 0, 5, 8, 9, and 11.

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							Polarity swapped!!
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Polarity swapped!!							
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OMIT_TABLE

U8000
NV-GK107
BGA
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PEG_R2D_N<3>	AM15	PEX_RX3*		PEX_TX3*	AK16	PEG_D2R_C_N<3>	
PEG_R2D_P<4>	AN17	PEX_RX4		PEX_TX4	AK17	PEG_D2R_C_P<4>	
PEG_R2D_N<4>	AM17	PEX_RX4*		PEX_TX4*	AJ17	PEG_D2R_C_N<4>	
PEG_R2D_P<5>	AP17	PEX_RX5		PEX_TX5	AH17	PEG_D2R_C_P<5>	
PEG_R2D_N<5>	AP18	PEX_RX5*		PEX_TX5*	AG17	PEG_D2R_C_N<5>	
PEG_R2D_P<6>	AN18	PEX_RX6		PEX_TX6	AK18	PEG_D2R_C_P<6>	
PEG_R2D_N<6>	AM18	PEX_RX6*		PEX_TX6*	AJ18	PEG_D2R_C_N<6>	
PEG_R2D_P<7>	AN20	PEX_RX7		PEX_TX7	AL19	PEG_D2R_C_P<7>	
PEG_R2D_N<7>	AM20	PEX_RX7*		PEX_TX7*	AK19	PEG_D2R_C_N<7>	
PEG_R2D_P<8>	AP20	PEX_RX8		PEX_TX8	AK20	PEG_D2R_C_P<8>	
PEG_R2D_N<8>	AP21	PEX_RX8*		PEX_TX8*	AJ20	PEG_D2R_C_N<8>	
PEG_R2D_P<9>	AN21	PEX_RX9		PEX_TX9	AH20	PEG_D2R_C_P<9>	
PEG_R2D_N<9>	AM21	PEX_RX9*		PEX_TX9*	AG20	PEG_D2R_C_N<9>	
PEG_R2D_P<10>	AN23	PEX_RX10		PEX_TX10	AK21	PEG_D2R_C_P<10>	
PEG_R2D_N<10>	AM23	PEX_RX10*		PEX_TX10*	AJ21	PEG_D2R_C_N<10>	
PEG_R2D_P<11>	AP23	PEX_RX11		PEX_TX11	AL22	PEG_D2R_C_P<11>	
PEG_R2D_N<11>	AP24	PEX_RX11*		PEX_TX11*	AK22	PEG_D2R_C_N<11>	
PEG_R2D_P<12>	AN24	PEX_RX12		PEX_TX12	AK23	PEG_D2R_C_P<12>	
PEG_R2D_N<12>	AM24	PEX_RX12*		PEX_TX12*	AJ23	PEG_D2R_C_N<12>	
PEG_R2D_P<13>	AN26	PEX_RX13		PEX_TX13	AH23	PEG_D2R_C_P<13>	
PEG_R2D_N<13>	AM26	PEX_RX13*		PEX_TX13*	AG23	PEG_D2R_C_N<13>	
PEG_R2D_P<14>	AP26	PEX_RX14		PEX_TX14	AK24	PEG_D2R_C_P<14>	
PEG_R2D_N<14>	AP27	PEX_RX14*		PEX_TX14*	AJ24	PEG_D2R_C_N<14>	
PEG_R2D_P<15>	AN27	PEX_RX15		PEX_TX15	AL25	PEG_D2R_C_P<15>	
PEG_R2D_N<15>	AM27	PEX_RX15*		PEX_TX15*	AK25	PEG_D2R_C_N<15>	
PEG_CLK100M_P	AL13	PEX_REFCLK		PEX_TSTCLK_OUT	AJ26	PEX_TSTCLK_O_PL	R8002 200 5% 1/20W MF 201 NOSTUFF
PEG_CLK100M_N	AK13	PEX_REFCLK*		PEX_TSTCLK_OUT*	AK26	PEX_TSTCLK_O_NG	
GPU_RESET_L	R8000 0 5% 1/20W MF 201 GPU_RESET_R_L	AJ12	PEX_RST*				
				PEX_TERMP	AP29	GPU_PEX_TERMP	R8005 2.49K 1% 1/20W MF 201
PEG_CLKREQ_L	AK12	PEX_CLKREQ*					
NC	AJ11	PEX_WAKE*		PEX_SVDD_3V3	AG12	=PP3V3_GPU_VDD33	

SYNC_MASTER=D7_TONY SYNC_DATE=01/10/2012

PAGE TITLE: KEPLER PCI-E

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D
REVISION: 4.2.0
BRANCH:
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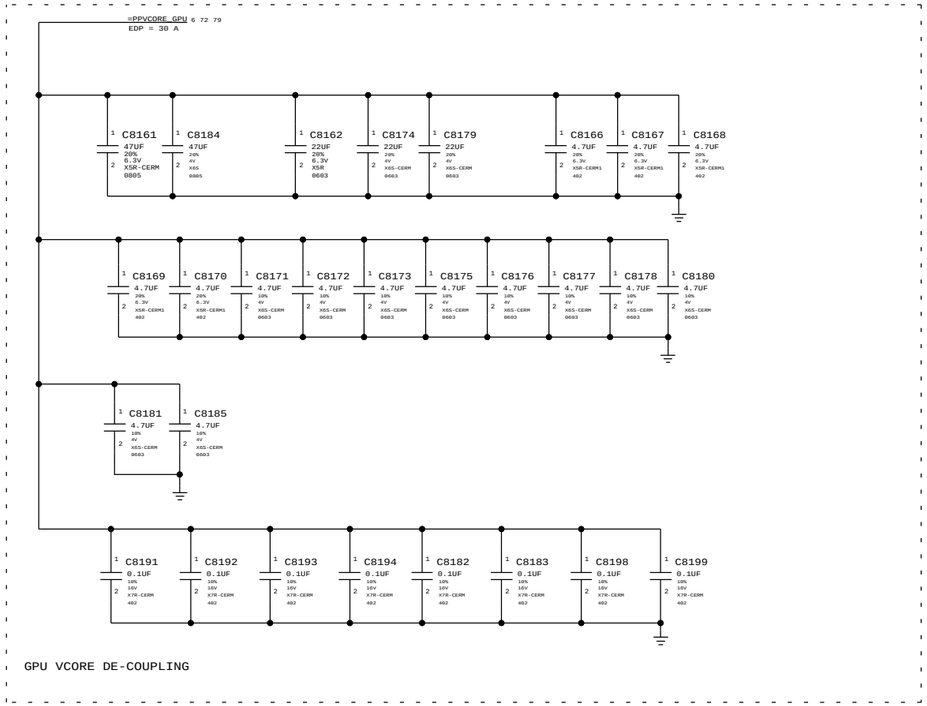

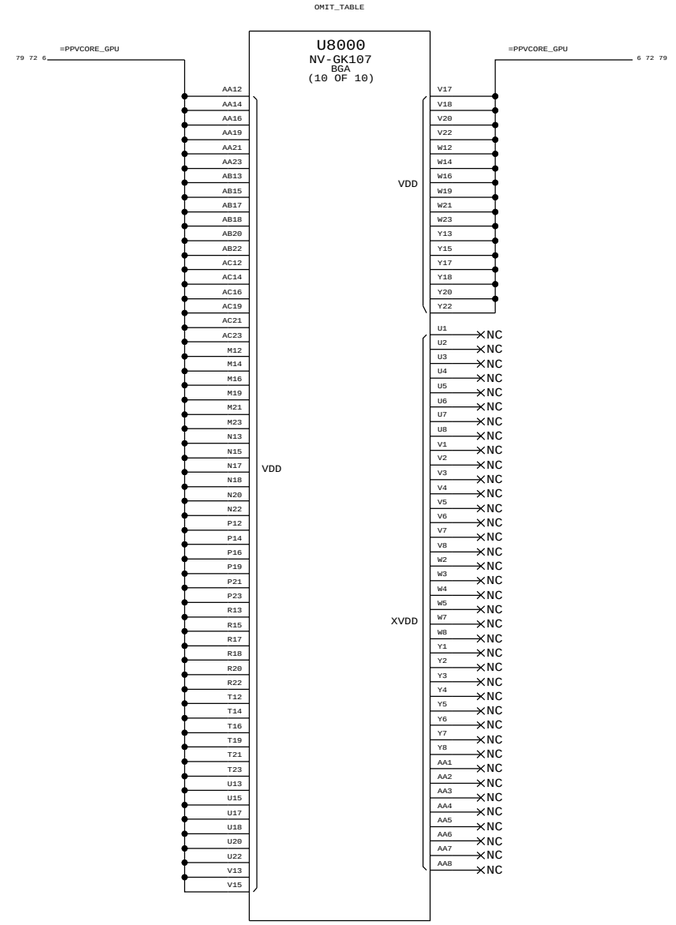

Page Notes

Power aliases required by this page:

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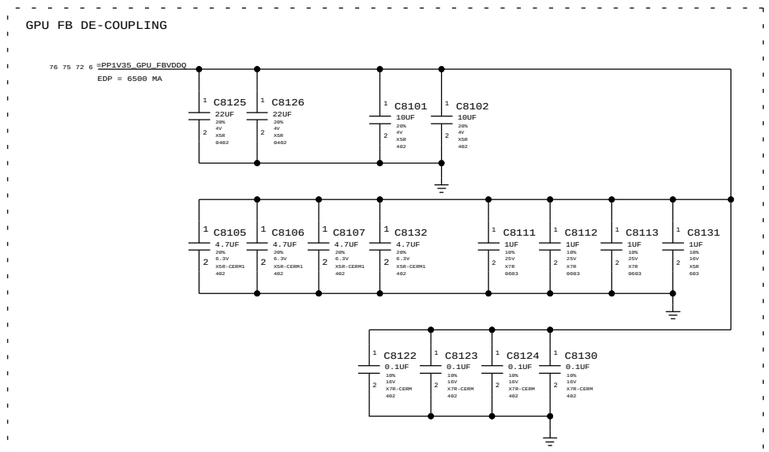
- =PPVSS_GPU_FBVDDQ

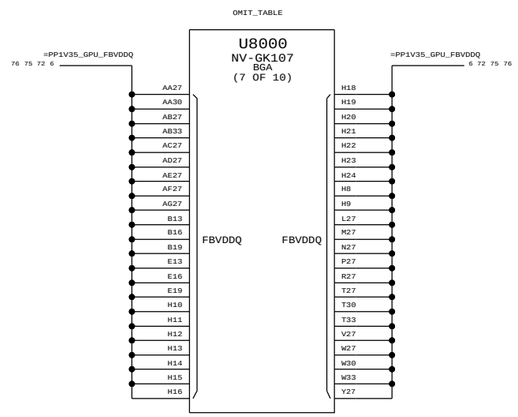
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)





SYNC_MASTER=D7_TONY	SYNC_DATE=01/10/2012
PAGE TITLE	KEPLER CORE/FB POWER
Apple Inc.	DRAWING NUMBER 051-9509 SIZE D
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NOTE:GDDR5 MODE H MAPPING

OMIT_TABLE

U8000
NV-GK107
BGA
(3 OF 10)
MEM INTERFACE A

FBA_D0	L28	FBA_CMD0	U30	FBA_DQM0	P30
FBA_D1	M29	FBA_CMD1	T31	FBA_DQM1	F31
FBA_D2	L29	FBA_CMD2	U29	FBA_DQM2	F34
FBA_D3	M28	FBA_CMD3	R34	FBA_DQM3	M32
FBA_D4	N31	FBA_CMD4	R33	FBA_DQM4	AD31
FBA_D5	P29	FBA_CMD5	U32	FBA_DQM5	AL29
FBA_D6	R29	FBA_CMD6	U33	FBA_DQM6	AM32
FBA_D7	P28	FBA_CMD7	U28	FBA_DQM7	AF34
FBA_D8	J28	FBA_CMD8	V28		
FBA_D9	H29	FBA_CMD9	V29	FBA_DQS_RN0	M30
FBA_D10	J29	FBA_CMD10	V30	FBA_DQS_RN1	H30
FBA_D11	H28	FBA_CMD11	U34	FBA_DQS_RN2	E34
FBA_D12	G29	FBA_CMD12	V31	FBA_DQS_RN3	M34
FBA_D13	E31	FBA_CMD13	V34	FBA_DQS_RN4	AF30
FBA_D14	E32	FBA_CMD14	V33	FBA_DQS_RN5	AK31
FBA_D15	F30	FBA_CMD15	Y32	FBA_DQS_RN6	AM34
FBA_D16	C34	FBA_CMD16	AA31	FBA_DQS_RN7	AF32
FBA_D17	D32	FBA_CMD17	AA29		
FBA_D18	B33	FBA_CMD18	AA28	FBA_DQS_WP0	M31
FBA_D19	C33	FBA_CMD19	AC34	FBA_DQS_WP1	G31
FBA_D20	F33	FBA_CMD20	AC33	FBA_DQS_WP2	E33
FBA_D21	F32	FBA_CMD21	AA32	FBA_DQS_WP3	M33
FBA_D22	H33	FBA_CMD22	AA33	FBA_DQS_WP4	AE31
FBA_D23	H32	FBA_CMD23	Y28	FBA_DQS_WP5	AK30
FBA_D24	P34	FBA_CMD24	Y29	FBA_DQS_WP6	AN33
FBA_D25	P32	FBA_CMD25	W31	FBA_DQS_WP7	AF33
FBA_D26	P31	FBA_CMD26	Y30		
FBA_D27	P33	FBA_CMD27	AA34	FBA_DLL_AVDD	K27
FBA_D28	L31	FBA_CMD28	Y31	FBA_PLL_AVDD	U27
FBA_D29	L34	FBA_CMD29	Y34		
FBA_D30	L32	FBA_CMD30	Y33	FBA_DEBUG	R28
FBA_D31	L33	FBA_CMD31	V31	FBA_DEBUG	AC28
FBA_D32	AG28				
FBA_D33	AF29	FBA_CLK0	R30	FBA_CAL_PD_VDDQ	J27
FBA_D34	AG29	FBA_CLK0*	R31	FBA_CAL_PU_GND	H27
FBA_D35	AF28	FBA_CLK1	AB31	FBA_CAL_TERM_GND	H25
FBA_D36	AD30	FBA_CLK1*	AC31		
FBA_D37	AD29			FBA_CLAMP	E1
FBA_D38	AC29				
FBA_D39	AD28			FBA_CMD_RFU	R32
FBA_D40	AJ29			FBA_CMD_RFU	AC32
FBA_D41	AK29				
FBA_D42	AJ30			FBA_VDDQ_SENSE	F1
FBA_D43	AK28				
FBA_D44	AM29			FBA_GND_SENSE	F2
FBA_D45	AD34				
FBA_D46	AN29				
FBA_D47	AM30				
FBA_D48	AN31				
FBA_D49	AN32				
FBA_D50	AP30				
FBA_D51	AP32				
FBA_D52	AM33				
FBA_D53	AL31				
FBA_D54	AK33				
FBA_D55	AK32				
FBA_D56	AD32				
FBA_D57	AC30				
FBA_D58	AD33				
FBA_D59	AF31				
FBA_D60	AG34				
FBA_D61	AG32				
FBA_D62	AG33				
FBA_D63	AD34				
FBA_WCK01	K31				
FBA_WCK01*	L30				
FBA_WCK23	H34				
FBA_WCK23*	J34				
FBA_WCK45	AG30				
FBA_WCK45*	AG31				
FBA_WCK67	AJ34				
FBA_WCK67*	AK34				
FBA_WCKB01	J30				
FBA_WCKB01*	J31				
FBA_WCKB23	J32				
FBA_WCKB23*	J33				
FBA_WCKB45	AH31				
FBA_WCKB45*	AJ31				
FBA_WCKB67	AJ32				
FBA_WCKB67*	AJ33				

FB_A0_RESET_L → R8250 10K 1% 1/20W MF 201 → 2

FB_A1_RESET_L → R8251 10K 1% 1/20W MF 201 → 2

=PP1V35_GPU_S0_FB → R8252 10K 1% 1/20W MF 201 → FB_A0_CKE_L

=PP1V35_GPU_S0_FB → R8253 10K 1% 1/20W MF 201 → FB_A1_CKE_L

FB VREF GEN (TEST ONLY)

=PP1V35_GPU_S0_FB → NOSTUFF R8258 1.33K 1% 1/20W MF 201 → FB_VREF

FB_VREF → NOSTUFF R8259 1.33K 1% 1/20W MF 201 → GND

FB_VREF → NOSTUFF C8260 0.1UF 10% 6.3V X5R 201 → GND

PLACE_NEAR=U8000.H26:0.4MM

PLACE_NEAR=U8000.H25:0.4MM

PLACE_NEAR=U8000.H27:0.4MM

FB_CAL_TERM_GND → R8201 60.4 1% 1/20W MF 201 → FB_CAL_PD_VDDQ

FB_CLAMP → R8261 10K 1% 1/20W MF 201 → GND

=PP1V35_GPU_S0_FB → NOSTUFF R8203 60.4 1% 1/20W MF 201 → FB_DEBUG

=PP1V35_GPU_S0_FB → NOSTUFF R8202 60.4 1% 1/20W MF 201 → FB_DEBUG

FB_VDDQ_SENSE → R8270 100 5% 1/20W MF 201 → NOSTUFF → SNS_GPUVDDQ_P

FB_GND_SENSE → R8271 100 5% 1/20W MF 201 → NOSTUFF → SNS_GPUVDDQ_N

PLACE CLOSE TO BGA

FB_CAL_PU_GND → R8204 40.2 1% 1/20W MF 201 → GND

=PP1V35_GPU_S0_FB → R8205 40.2 1% 1/20W MF 201 → FB_CAL_PD_VDDQ

OMIT_TABLE

U8000
NV-GK107
BGA
(4 OF 10)
MEM INTRERFACE B

FBB_D0	G9	FBB_CMD0	D13	FBB_DQM0	E11
FBB_D1	E9	FBB_CMD1	E14	FBB_DQM1	E3
FBB_D2	G8	FBB_CMD2	F14	FBB_DQM2	A3
FBB_D3	F9	FBB_CMD3	A12	FBB_DQM3	C9
FBB_D4	F11	FBB_CMD4	B12	FBB_DQM4	F23
FBB_D5	G11	FBB_CMD5	C14	FBB_DQM5	F27
FBB_D6	F12	FBB_CMD6	B14	FBB_DQM6	C30
FBB_D7	G12	FBB_CMD7	G15	FBB_DQM7	A24
FBB_D8	G6	FBB_CMD8	F15		
FBB_D9	F5	FBB_CMD9	E15	FBB_DQS_RN0	D9
FBB_D10	E6	FBB_CMD10	D15	FBB_DQS_RN1	E4
FBB_D11	F6	FBB_CMD11	A14	FBB_DQS_RN2	B2
FBB_D12	F4	FBB_CMD12	D14	FBB_DQS_RN3	A9
FBB_D13	G4	FBB_CMD13	A15	FBB_DQS_RN4	D22
FBB_D14	E2	FBB_CMD14	B15	FBB_DQS_RN5	D28
FBB_D15	F3	FBB_CMD15	C17	FBB_DQS_RN6	A30
FBB_D16	C2	FBB_CMD16	D18	FBB_DQS_RN7	B23
FBB_D17	D4	FBB_CMD17	E18		
FBB_D18	D3	FBB_CMD18	F18	FBB_DQS_WP0	D10
FBB_D19	C1	FBB_CMD19	A20	FBB_DQS_WP1	D5
FBB_D20	B3	FBB_CMD20	B20	FBB_DQS_WP2	C3
FBB_D21	C4	FBB_CMD21	C18	FBB_DQS_WP3	B9
FBB_D22	B5	FBB_CMD22	B18	FBB_DQS_WP4	E23
FBB_D23	C5	FBB_CMD23	G18	FBB_DQS_WP5	E28
FBB_D24	A11	FBB_CMD24	G17	FBB_DQS_WP6	B30
FBB_D25	C11	FBB_CMD25	F17	FBB_DQS_WP7	A23
FBB_D26	D11	FBB_CMD26	D16		
FBB_D27	B11	FBB_CMD27	A18	FBB_PLL_AVDD	H17
FBB_D28	D8	FBB_CMD28	D17		
FBB_D29	A8	FBB_CMD29	A17	FBB_DEBUG0	G14
FBB_D30	C8	FBB_CMD30	B17	FBB_DEBUG1	G20
FBB_D31	B8	FBB_CMD31	E17		
FBB_D32	F24			FB_VREF	H26
FBB_D33	G23	FBB_CLK0	D12		
FBB_D34	E24	FBB_CLK0*	E12	FBB_CMD_RFU0	C12
FBB_D35	G24	FBB_CLK1	E20	FBB_CMD_RFU1	C20
FBB_D36	D21	FBB_CLK1*	F20		
FBB_D37	E21				
FBB_D38	G21				
FBB_D39	F21				
FBB_D40	G27				
FBB_D41	D27				
FBB_D42	G26				
FBB_D43	E27				
FBB_D44	E29				
FBB_D45	F29				
FBB_D46	E30				
FBB_D47	D30				
FBB_D48	A32				
FBB_D49	C31				
FBB_D50	C32				
FBB_D51	B32				
FBB_D52	D29				
FBB_D53	A29				
FBB_D54	C29				
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FBB_D56	B21				
FBB_D57	C23				
FBB_D58	A21				
FBB_D59	C21				
FBB_D60	B24				
FBB_D61	C24				
FBB_D62	B26				
FBB_D63	C26				
FBB_WCK01	F8				
FBB_WCK01*	E8				
FBB_WCK23	A5				
FBB_WCK23*	A6				
FBB_WCK45	D24				
FBB_WCK45*	D25				
FBB_WCK67	B27				
FBB_WCK67*	C27				
FBB_WCKB01	D6				
FBB_WCKB01*	D7				
FBB_WCKB23	C6				
FBB_WCKB23*	B6				
FBB_WCKB45	F26				
FBB_WCKB45*	E26				
FBB_WCKB67	A26				
FBB_WCKB67*	A27				

FB_B0_RESET_L → R8254 10K 1% 1/20W MF 201 → 2

FB_B1_RESET_L → R8255 10K 1% 1/20W MF 201 → 2

=PP1V35_GPU_S0_FB → R8256 10K 1% 1/20W MF 201 → FB_B0_CKE_L

=PP1V35_GPU_S0_FB → R8257 10K 1% 1/20W MF 201 → FB_B1_CKE_L

=PP1V35_GPU_S0_FB → NOSTUFF R8206 60.4 1% 1/20W MF 201 → FB_DEBUG0

=PP1V35_GPU_S0_FB → NOSTUFF R8207 60.4 1% 1/20W MF 201 → FB_DEBUG1

=PP1V05_GPU_PEX_IOVDD → L8201 30-OHM-25%-5A-0.01-OHM 0603 CRITICAL ESR = 0.050HM → PP1V05_GPU_FB_PLL_AVDD

MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

C8201 22UF 20% 6.3V X5R 402
C8202 1UF 20% 6.3V X5R 0201
C8203 0.1UF 10% 16V X7R-CERM 402
C8204 0.1UF 10% 16V X7R-CERM 402

=PP1V05_GPU_PEX_IOVDD → L8202 30-OHM-25%-5A-0.01-OHM 0603 CRITICAL ESR = 0.050HM → PP1V05_GPU_FB_DLL_AVDD

MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

C8208 22UF 20% 6.3V X5R 402
C8209 1UF 20% 6.3V X5R 0201
C8205 0.1UF 10% 16V X7R-CERM 402

FB PLL & DLL VDD

C8206 1UF 20% 6.3V X5R 0201
C8207 0.1UF 10% 6.3V X5R 201

MEM VREFC & VREFD SWITCH

FB_SW_LEG → Q8265 SSM3K15AMFVAPE VESM (CRITICAL)

Q8265 pin 3 D, pin 2 S, pin 1 G

GPU_ALT_VREF → R8260 10K 5% 1/20W MF 201 → GND

Page Notes

Power aliases required by this page:
- =PP1V35_GPU_S0_FB
- =PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=D7 TONY SYNC_DATE=01/10/2012

PAGE TITLE
KEPLER FRAME BUFFER I/F

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GPU VDDQ SUPPLY

VOUT = 1.5V / 1.35V

10 A MAX OUTPUT

F = ??? KHZ

GPIO_16 VID 1	VID 0	GPU VDDQ
0	0	1.5 V
1	0	1.35 V

Vout = 0.5 * (1 + Ra / Rb)

GPU 1V05 SUPPLY

VOUT = 1.05V

3.43 A MAX OUTPUT

F = 500 KHZ

Vout = 0.5V * (1 + Ra / Rb)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
110S0568	1	RES,MF,3.32 OHM,1/10W,1,603,LF	R8311	CRITICAL	

SYNC_MASTER=D7_NICK SYNC_DATE=01/03/2012

PAGE TITLE: 1V05 GPU POWER SUPPLY

Apple Inc.

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Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

This memory device is in Mirrored Mode.

CK TERMINATION - A0

CK TERMINATION - A1

U8400 32MX32-1.5GHZ-MFL BGA K4G10325FG-HC03 (1 OF 2)

U8400 32MX32-1.5GHZ-MFL BGA K4G10325FG-HC03 (2 OF 2)

U8450 32MX32-1.5GHZ-MFH BGA K4G10325FG-HC03 (1 OF 2)

U8450 32MX32-1.5GHZ-MFH BGA K4G10325FG-HC03 (2 OF 2)

OMIT_TABLE

PLACE CLOSE TO U8400

PLACE CLOSE TO U8450

SYNC_MASTER=D7_TONY	SYNC_DATE=12/13/2011
PAGE TITLE	GDDR5 Frame Buffer A
Apple Inc.	DRAWING NUMBER 051-9509 SIZE D
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Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

This memory device is in Mirrored Mode.

CK TERMINATION - B0

CK TERMINATION - B1

U8500 32MX32-1.5GHZ-MFL BGA K4G10325FG-HC03 (1 OF 2)

U8500 32MX32-1.5GHZ-MFL BGA K4G10325FG-HC03 (2 OF 2)

U8550 32MX32-1.5GHZ-MFH BGA K4G10325FG-HC03 (1 OF 2)

U8550 32MX32-1.5GHZ-MFH BGA K4G10325FG-HC03 (2 OF 2)

OMIT_TABLE

PLACE CLOSE TO U8500

PLACE CLOSE TO U8550

SYNC_MASTER=D7_TONY	SYNC_DATE=12/13/2011
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-9509 SIZE D
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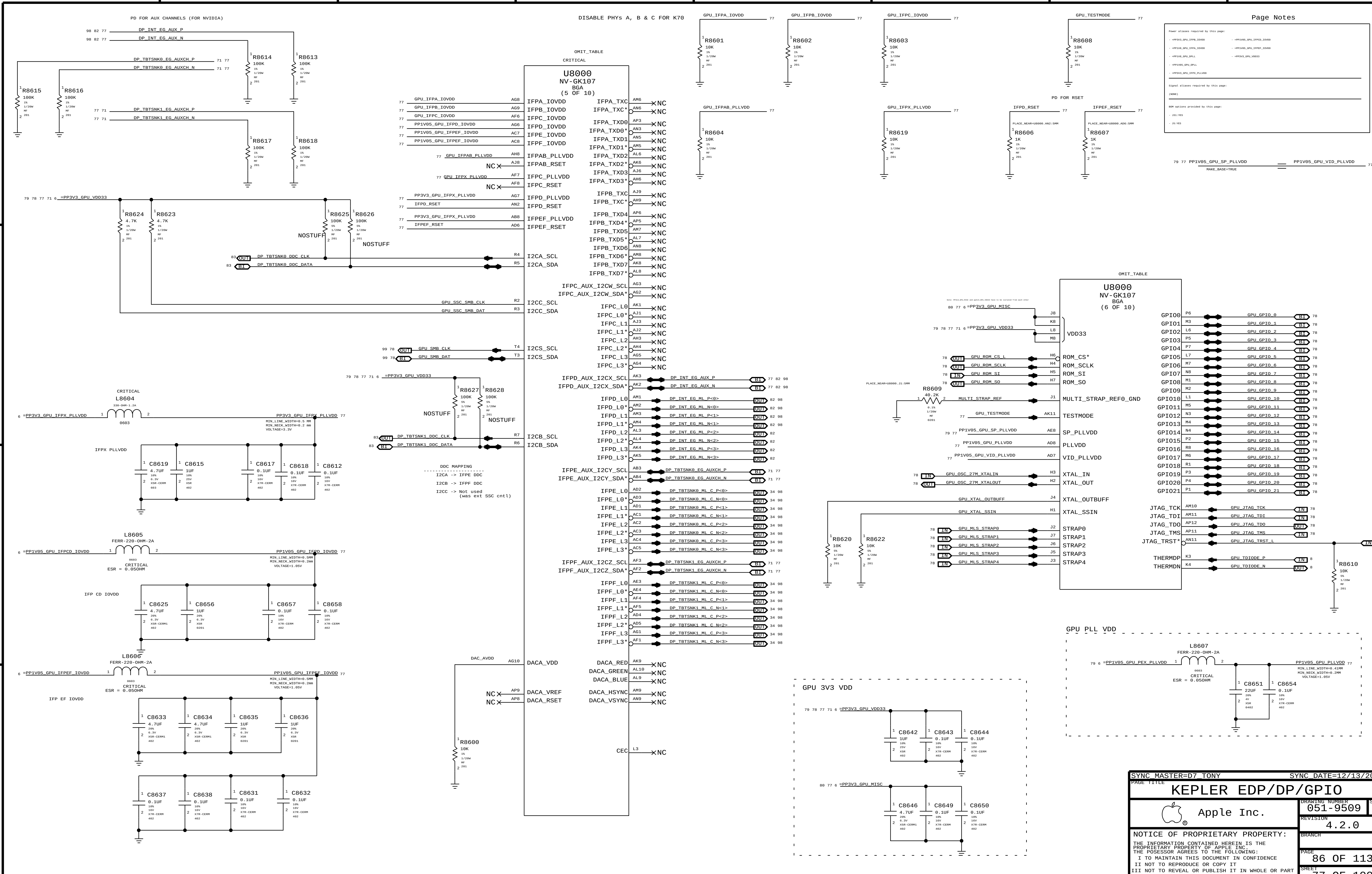


SYNC_MASTER=D7_TONY SYNC_DATE=12/13/2011

PAGE TITLE

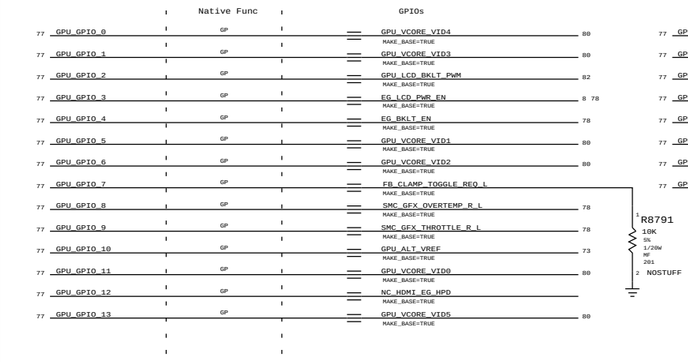
KEPLER EDP/DP/GPIO

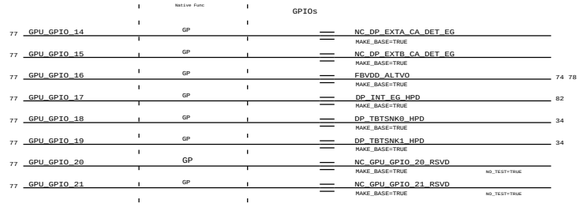
Apple Inc.

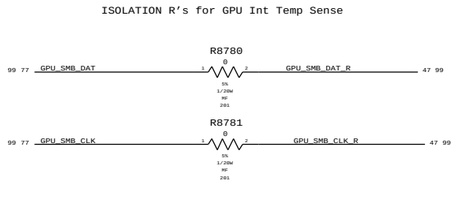
DRAWING NUMBER 051-9509 SIZE D

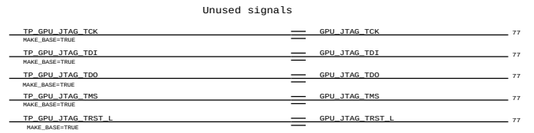
REVISION 4.2.0

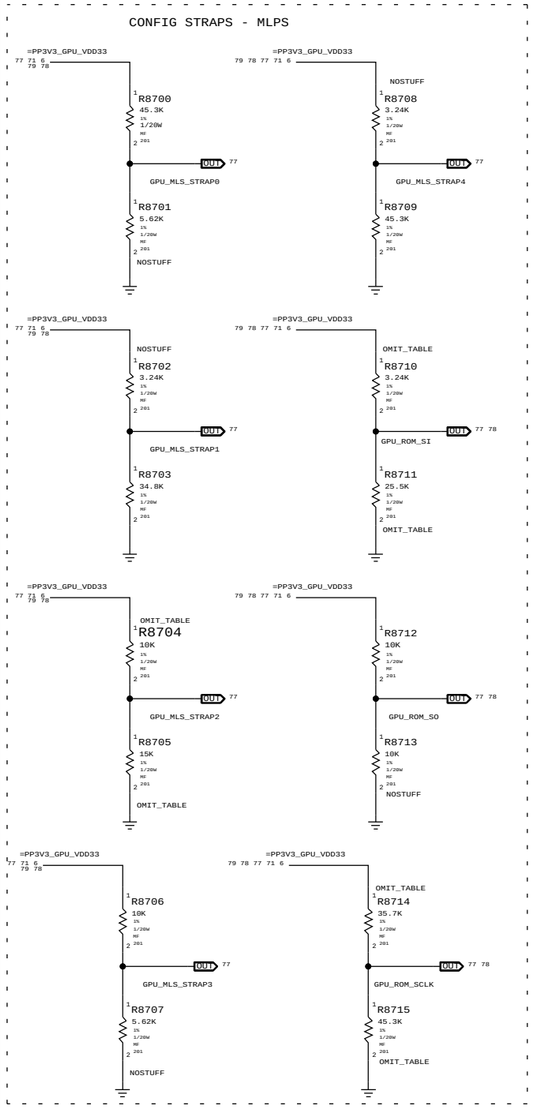
BRANCH

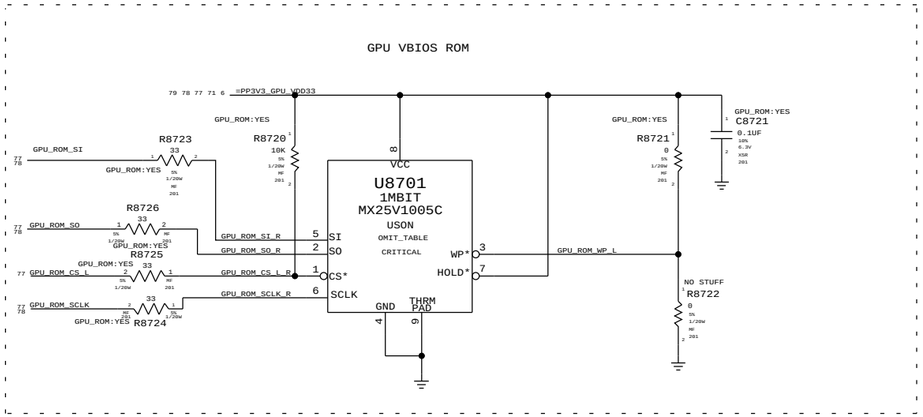


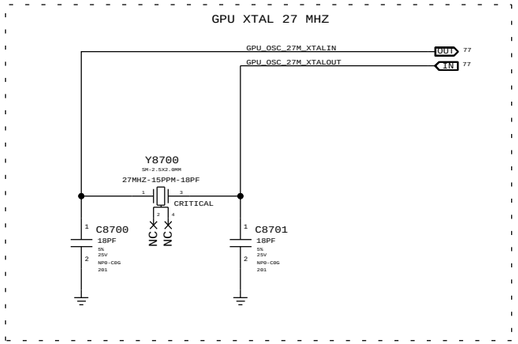


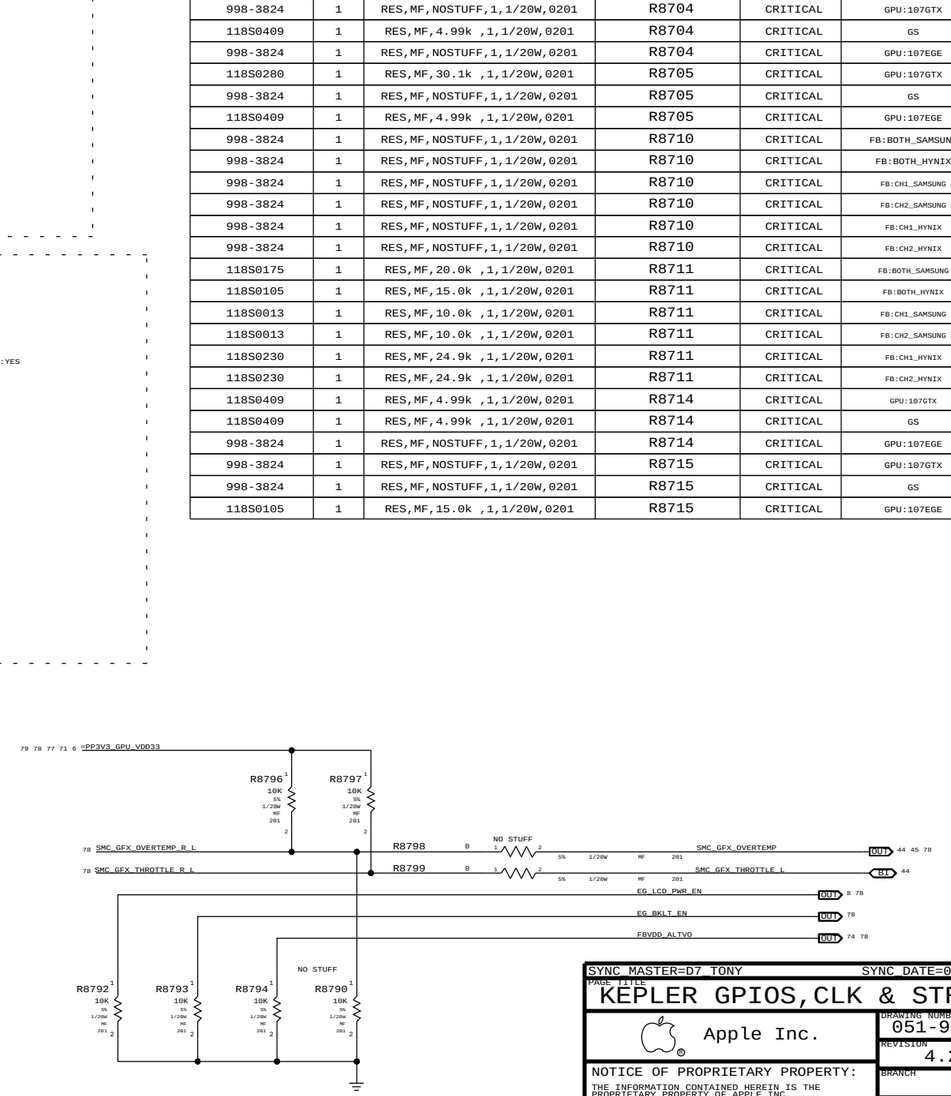












PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8704	CRITICAL	GPU:107GTX
118S0409	1	RES,MF,4.99k ,1,1/20W,0201	R8704	CRITICAL	GS
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8704	CRITICAL	GPU:107EGE
118S0280	1	RES,MF,30.1k ,1,1/20W,0201	R8705	CRITICAL	GPU:107GTX
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8705	CRITICAL	GS
118S0409	1	RES,MF,4.99k ,1,1/20W,0201	R8705	CRITICAL	GPU:107EGE
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:BOTH_SAMSUNG
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:BOTH_HYNIX
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:CH1_SAMSUNG
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:CH2_SAMSUNG
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:CH1_HYNIX
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:CH2_HYNIX
118S0175	1	RES,MF,20.0k ,1,1/20W,0201	R8711	CRITICAL	FB:BOTH_SAMSUNG
118S0105	1	RES,MF,15.0k ,1,1/20W,0201	R8711	CRITICAL	FB:BOTH_HYNIX
118S0013	1	RES,MF,10.0k ,1,1/20W,0201	R8711	CRITICAL	FB:CH1_SAMSUNG
118S0013	1	RES,MF,10.0k ,1,1/20W,0201	R8711	CRITICAL	FB:CH2_SAMSUNG
118S0230	1	RES,MF,24.9k ,1,1/20W,0201	R8711	CRITICAL	FB:CH1_HYNIX
118S0230	1	RES,MF,24.9k ,1,1/20W,0201	R8711	CRITICAL	FB:CH2_HYNIX
118S0409	1	RES,MF,4.99k ,1,1/20W,0201	R8714	CRITICAL	GPU:107GTX
118S0409	1	RES,MF,4.99k ,1,1/20W,0201	R8714	CRITICAL	GS
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8714	CRITICAL	GPU:107EGE
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8715	CRITICAL	GPU:107GTX
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8715	CRITICAL	GS
118S0105	1	RES,MF,15.0k ,1,1/20W,0201	R8715	CRITICAL	GPU:107EGE

SYNC_MASTER=D7_TONY SYNC_DATE=01/10/2012

PAGE TITLE
KEPLER GPIOS,CLK & STRAPS

Apple Inc.

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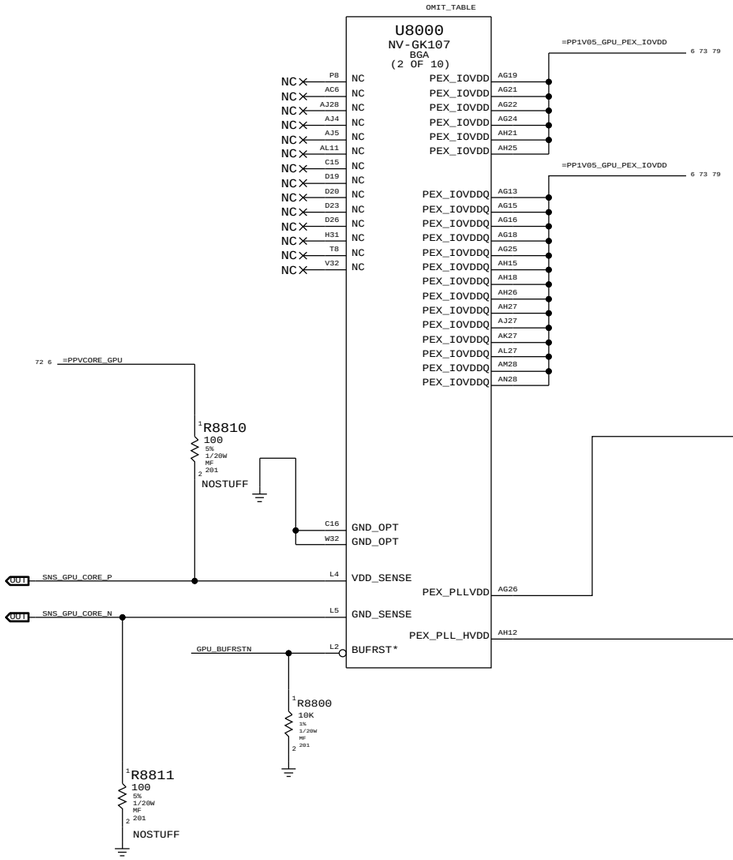

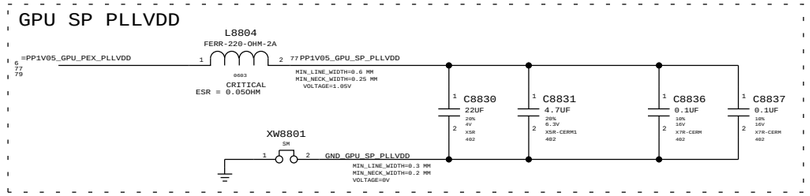

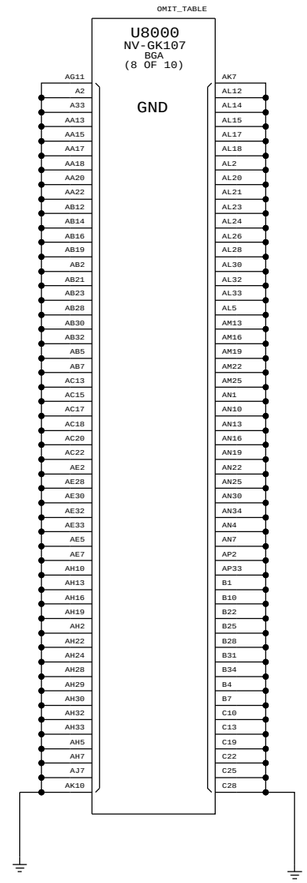

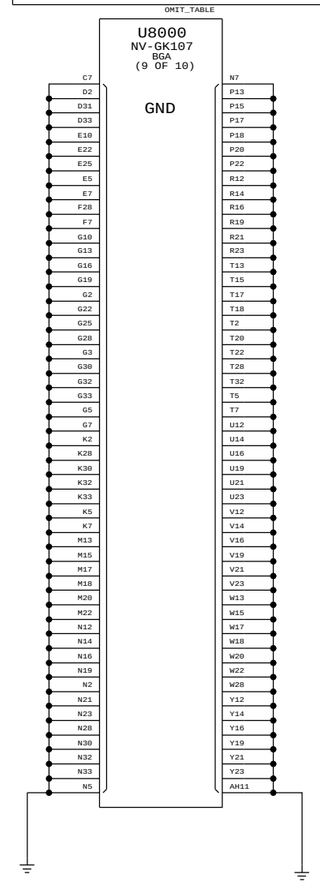

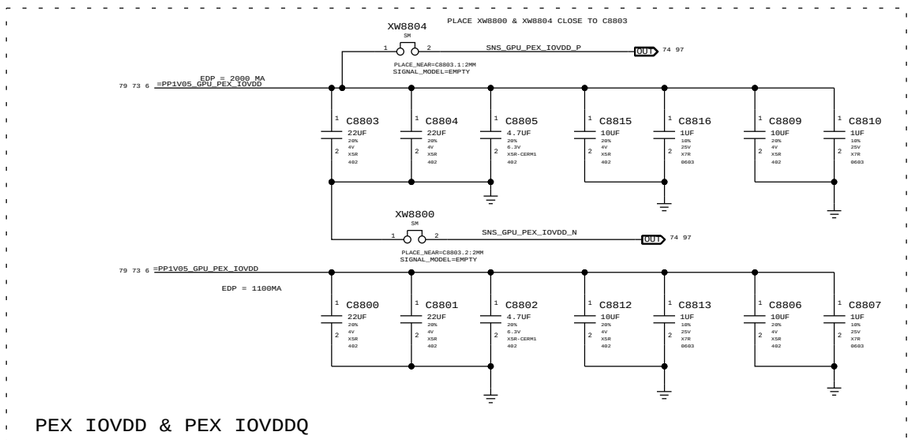

Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP1V05_GPU_PEX_IOVDD
- =PP1V05_GPU_PEX_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC_MASTER=D7_TONY SYNC_DATE=01/10/2012

PAGE TITLE

KEPLER PEX PWR/GNDS

Apple Inc.

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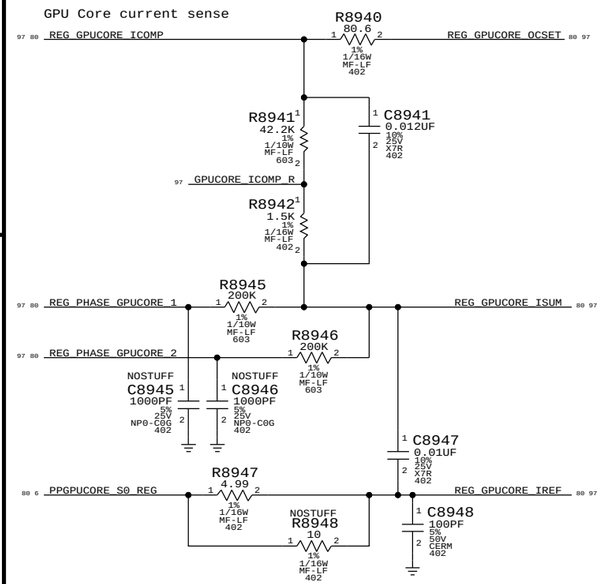
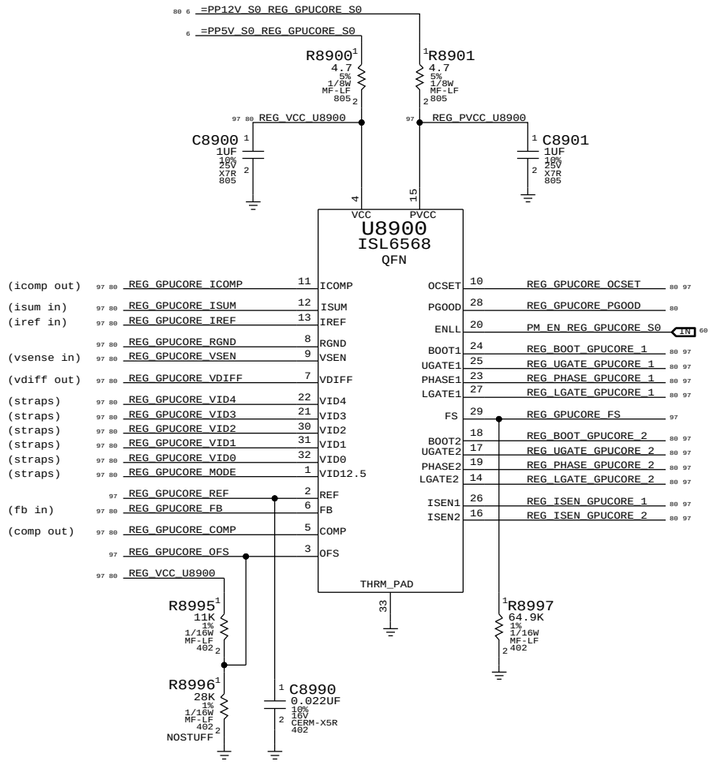
GPU Core S0 Regulator

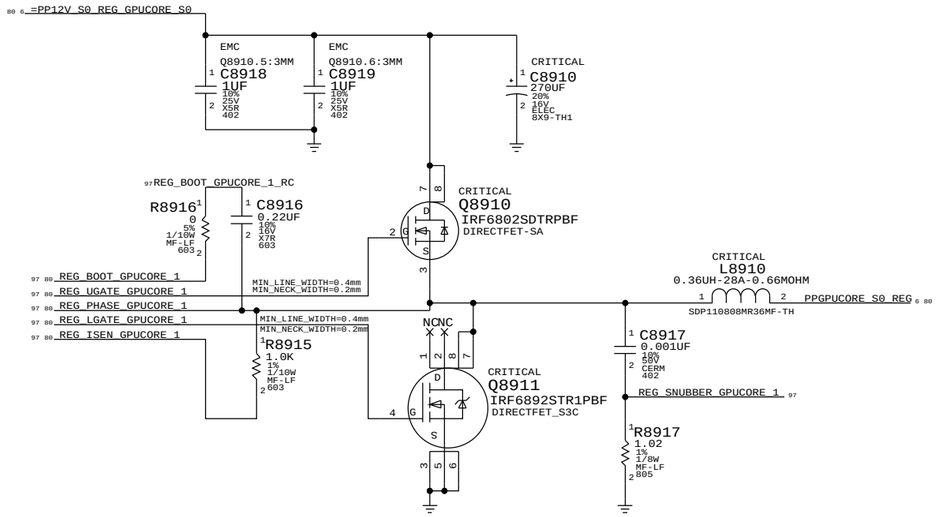
Max avg current: ? A (design)/? A (budget)
Max peak current: ? A (design)/? A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

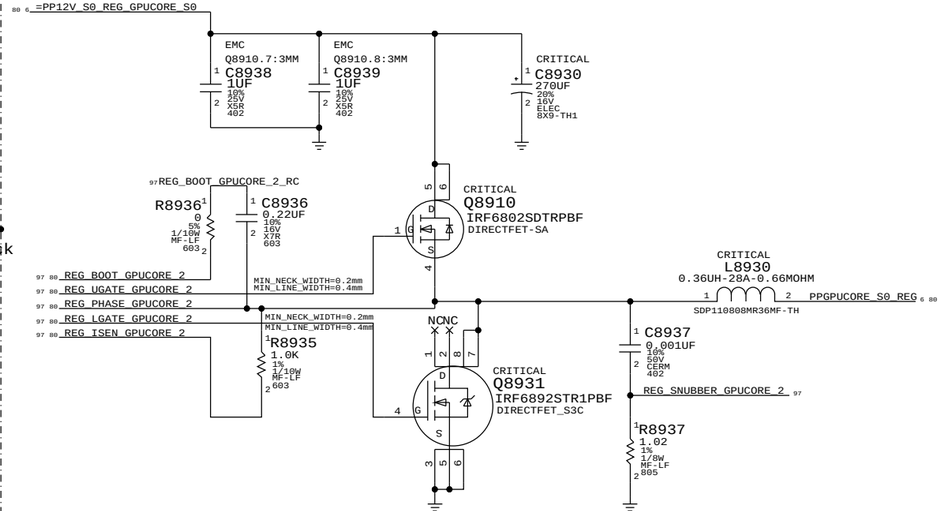
GPU Core current sense



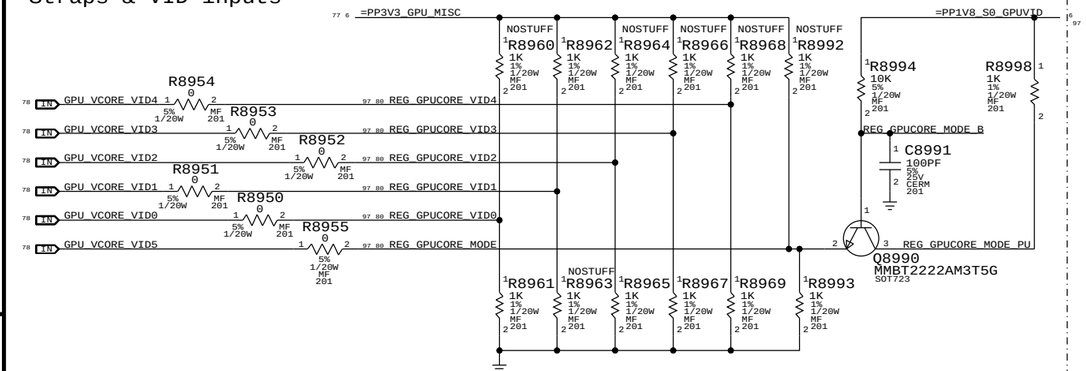


GPU Core Phases

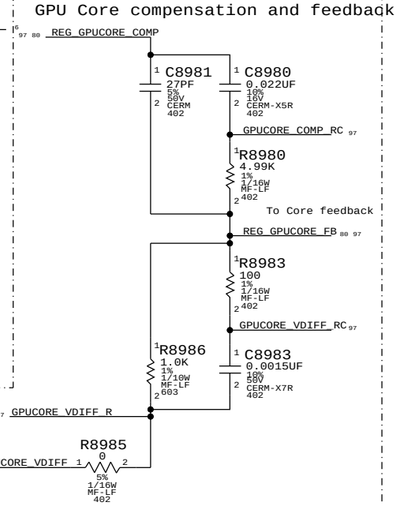




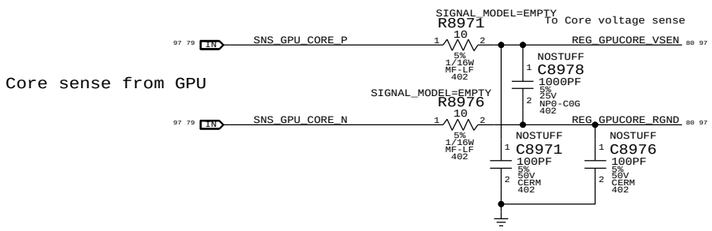
Straps & VID inputs



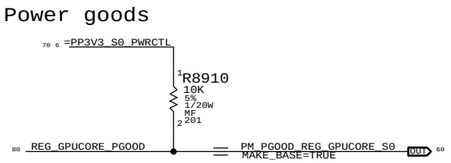
GPU Core compensation and feedback



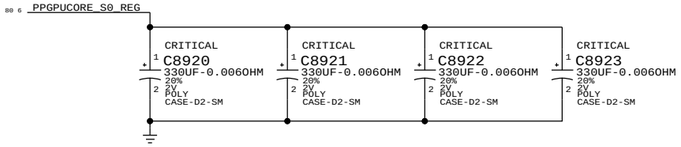
GPU Core voltage sense input



Power goods



GPU Core Output Decoupling



SYNC_MASTER=D7_NICK SYNC_DATE=01/03/2012

PAGE TITLE: VReg GPU Core

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D
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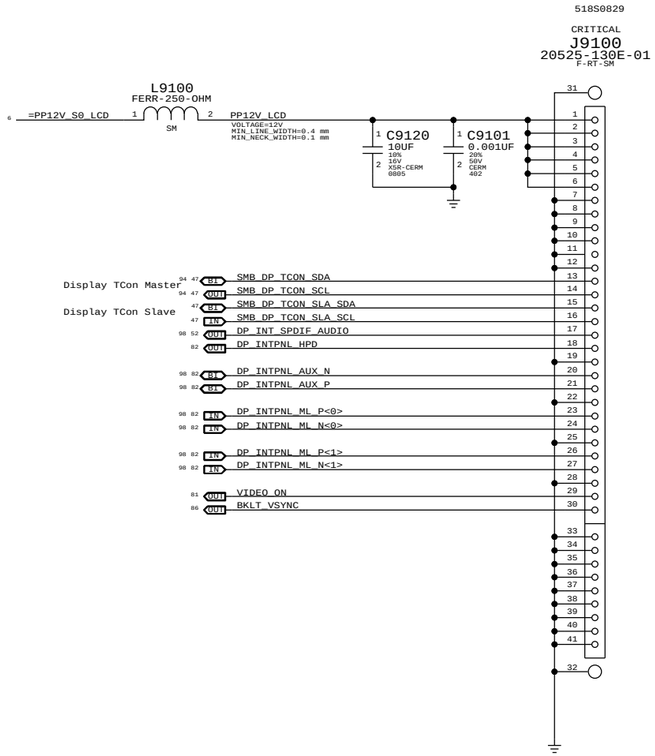
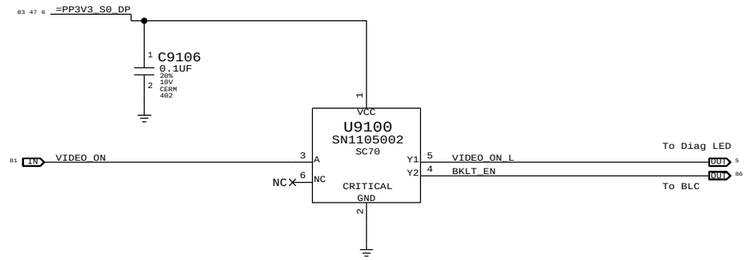
Internal DP Connector



Backlight Control

U9000 output Y2 is a non-inverted, delayed version of input A
The delay applies only on a L->H transition on A. This guarantees video is valid before the backlight is enabled.
On a H->L transition of A, Y2 follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video
Y1 is simply an inverted version of A, with no delay



SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE
Internal DP Support

Apple Inc.

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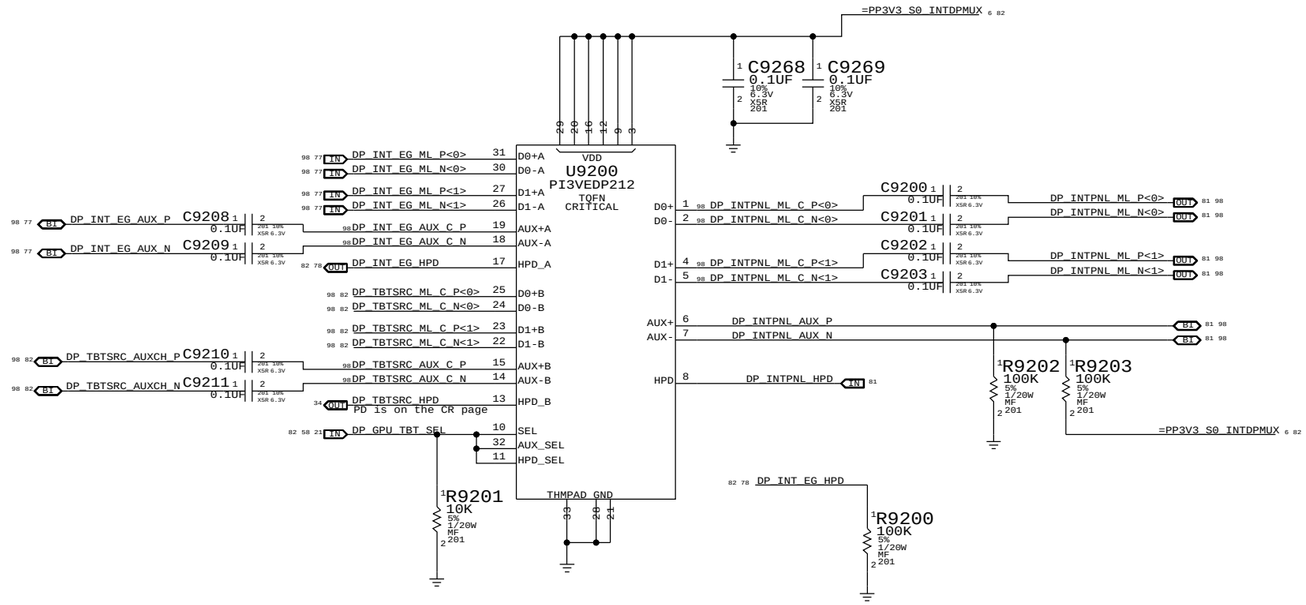
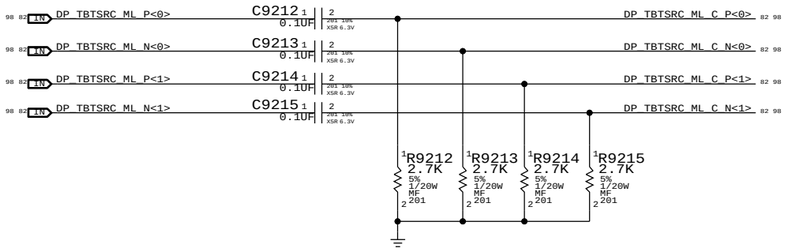
TP to DP aliases

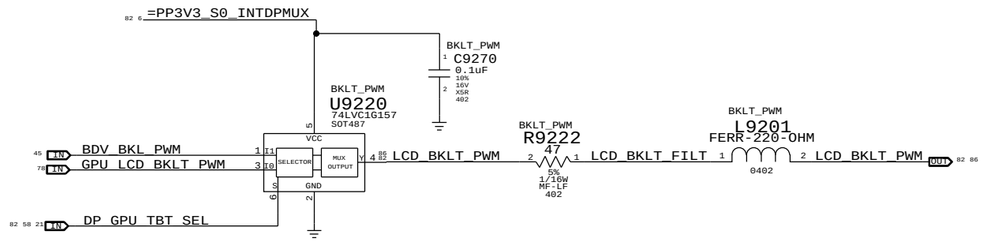
TP_DP_TBTSRC_ML_CP<0>	MAKE_BASE=TRUE	DP_TBTSRC_ML_P<0>	82 98
TP_DP_TBTSRC_ML_CN<0>	MAKE_BASE=TRUE	DP_TBTSRC_ML_N<0>	82 98
TP_DP_TBTSRC_ML_CP<1>	MAKE_BASE=TRUE	DP_TBTSRC_ML_P<1>	82 98
TP_DP_TBTSRC_ML_CN<1>	MAKE_BASE=TRUE	DP_TBTSRC_ML_N<1>	82 98
TP_DP_TBTSRC_AUXCH_CP	MAKE_BASE=TRUE	DP_TBTSRC_AUXCH_P	82 98
TP_DP_TBTSRC_AUXCH_CN	MAKE_BASE=TRUE	DP_TBTSRC_AUXCH_N	82 98

NC aliases

TP_DP_TBTSRC_ML_CP<2>	NO_TEST=TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_P<2>
TP_DP_TBTSRC_ML_CN<2>	NO_TEST=TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_N<2>
TP_DP_TBTSRC_ML_CP<3>	NO_TEST=TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_P<3>
TP_DP_TBTSRC_ML_CN<3>	NO_TEST=TRUE MAKE_BASE=TRUE	NC_DP_TBTSRC_ML_N<3>
DP_INT_EG_ML_P<2>	NO_TEST=TRUE MAKE_BASE=TRUE	NC_DP_INT_EG_ML_P<2>
DP_INT_EG_ML_N<2>	NO_TEST=TRUE MAKE_BASE=TRUE	NC_DP_INT_EG_ML_N<2>
DP_INT_EG_ML_P<3>	NO_TEST=TRUE MAKE_BASE=TRUE	NC_DP_INT_EG_ML_P<3>
DP_INT_EG_ML_N<3>	NO_TEST=TRUE MAKE_BASE=TRUE	NC_DP_INT_EG_ML_N<3>







SYNC_MASTER=D7_NICK	SYNC_DATE=12/14/2011
PAGE TITLE	Internal DP MUXing
Apple Inc.	DRAWING NUMBER 051-9509 · SIZE D
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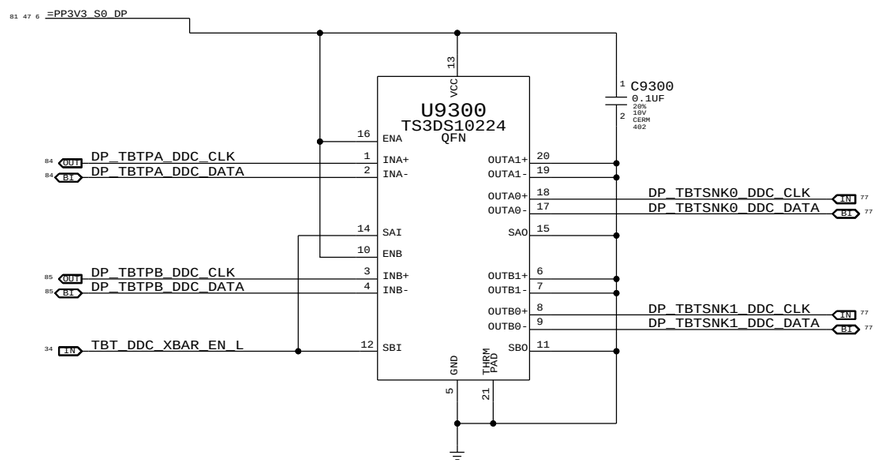
Dual-Port Host DDC Crossbar



SYNC_MASTER=D7_DOUG SYNC_DATE=12/15/2011

PAGE TITLE

TBT DDC Crossbar

Apple Inc.

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW
CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9480 22UF 20% 6.3V X5R-CERM-1 603
C9481 0.1UF 20% 10V CERM 402
=PPHV_SW_TBTAPWRSW 18.9V Max
C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 50V X7R 603-1
U9410 CRITICAL CD3210A0RGP QFN
V3P3OUT, NC, OUT, VHV, RSVD, EN, HV_EN, S0, ISET_S3, ISET_S0, ISET_V3P3, GND, THRM PAD
PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C9411 0.1UF 10% 50V X7R 603-1
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
12V: See below
TBTHV:P15V
R9410 22.6K 1% 1/16W MF-LF 402
R9411 22.6K 1% 1/16W MF-LF 402
R9412 36.5K 1% 1/16W MF-LF 402
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R9413 22.6K 1% 1/16W MF-LF 402
R9414 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9410,R9413		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

=PP3V3_S4_TBT
C9420 0.1UF 10% 6.3V X5R 201
C9421 0.1UF 10% 6.3V X5R 201
R9427 10K 5% 1/20W MF 201
R9429 100K 5% 1/20W MF 201
U9420 CRITICAL CBTL05023 HVQFN
VDD, BIASIN, AUXIO_EN, AUX-, AUX+, DDC_DAT, DDC_CLK, CA_DETOUT, DP+, DP-, LSTX, LSRX, DP_PD, HPDOUT, BIASOUT, AUXIO-, AUXIO+, CA_DET, DPMLO+, DPMLO-, HPD, GND_THMPAD
TBT_A_BIAS VOLTAGE=3.3V
C9425 0.1UF 10% 6.3V X5R 201
TBT_A_CIO_SEL
DP_AUXIO_EN
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C9430 0.1UF 10% 6.3V X5R 201
C9431 0.1UF 10% 6.3V X5R 201
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C9432 0.22UF 20% 6.3V X5R 0201
C9433 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_LSTX
TBT_A_LSRX_UNBUF
TBT_A_DP_PWRDN
DP_TBTPA_HPD
TBT_A_HPD
=PP3V3_S4_TBT
U9460 74AUP1T97 SOT891
TBT_A_LSRX
C9460 0.1UF 10% 16V X5R-CERM 0201
R9426 1M 5% 1/20W MF 201
R9428 100K 5% 1/20W MF 201

L9400 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C9400 0.01UF 10% 50V X7R 402
TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V
R9401 12 5% 1/20W MF 201
C9401 0.01UF 10% 50V X7R 402
TBT Dir
DP Dir
GND_VOID=TRUE (Both C's)
C9474 0.22UF 20% 6.3V XSR 0201
C9475 0.22UF 20% 6.3V XSR 0201
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
NOTE: Polarity Swapped for layout!
R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
C9478 0.22UF 20% 6.3V XSR 0201
C9479 0.22UF 20% 6.3V XSR 0201
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201
TBT: Terminated
TBT_A_BIAS
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201
C9476 0.22UF 20% 6.3V XSR 0201
C9477 0.22UF 20% 6.3V XSR 0201
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
NOTE: Polarity Swapped for layout!
CRITICAL D9498 BAR90-02LRH TSLP-2-7
CRITICAL D9499 BAR90-02LRH TSLP-2-7
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603
CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603
DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C9498 30PF 5% 50V CERM 402
C9499 30PF 5% 50V CERM 402
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R 201
C9495 330PF 10% 16V X7R 201
R9441 100K 5% 1/20W MF 201
C9402 0.01UF 10% 25V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL
J9400 DUAL-MDP-K70
SHLD, HPD, CONFIG1, CONFIG2, GND2, ML_LANE3P, ML_LANE3N, GND4, AUX_CHP, AUX_CHN, DP_PWR, F-ANG-TH, ML_LANE0P, ML_LANE0N, GND1, ML_LANE1P, ML_LANE1N, GND3, ML_LANE2P, ML_LANE2N, RETURN, PORT A SHLD
514-0824

C9405 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
DP Dir
TBT Dir
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
C9406 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1
GND_VOID=TRUE (Both C's)
C9470 0.22UF 20% 6.3V XSR 0201
C9471 0.22UF 20% 6.3V XSR 0201
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
NOTE: Polarity Swapped for layout!
C9472 0.22UF 20% 6.3V XSR 0201
C9473 0.22UF 20% 6.3V XSR 0201
TBT_A_R2D_C_N<1>
TBT_A_R2D_C_P<1>
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=D7_DOUG	SYNC_DATE=12/15/2011
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

=PP3V3_S4_TBTBPWRSW

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

CRITICAL C9687 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9680 22UF 20% 6.3V X5R-CERM-1 603
C9681 0.1UF 20% 10V CERM 402

=PPHV_SW_TBTBPWRSW
18.9V Max

C9615 4.7UF 10% 25V X5R-CERM 0603
C9610 0.1UF 10% 50V X7R 603-1

CRITICAL U9610 CD3210A0RGP QFN

V3P3 (19,20) V3P3OUT (18) NC
VHV (6,7) OUT (12,14) PPHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C9611 0.1UF 10% 50V X7R 603-1
RSVD (16) RSVD (15)
EN (5) =TBTBPWRSW_EN
HV_EN (11) TBT_B_HV_EN
S0 (17) =TBT_S0_EN
ISET_V3P3 (8) TBTBPWRSW_ISET_V3P3
ISET_S0 (10) TBTBPWRSW_ISET_S0
ISET_S3 (9) TBTBPWRSW_ISET_S3
GND (1,2,3,4,13,21) THRM PAD

TBTHV:P15V
R9610 22.6K 1% 1/16W MF-LF 402
R9611 22.6K 1% 1/16W MF-LF 402
R9612 36.5K 1% 1/16W MF-LF 402
12V: See below

TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V
R9613 22.6K 1% 1/16W MF-LF 402
R9614 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9610,R9613		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B

=PP3V3_S4_TBT

C9620 0.1UF 10% 6.3V X5R 201
C9621 0.1UF 10% 6.3V X5R 201
R9627 10K 5% 1/20W MF 201
R9629 100K 5% 1/20W MF 201

CRITICAL U9620 CBTL05023 HVQFN
VDD (15)

BIASIN	1	24	BIASOUT
AUXIO_EN	2	23	AUXIO-
AUX-	7	22	AUXIO+
AUX+	8	18	CA_DET
DDC_DAT	4	19	DPMLO+
DDC_CLK	5	20	DPMLO-
CA_DETOUT	16	17	HPD
DP+	11		
DP-	10		
LSTX	14		
LSRX	13		
DP_PD	6		
HPDOUT	12		
GND_THMPAD	9,21,25		

TBT_B_BIAS (85) VOLTAGE=3.3V
C9625 0.1UF 10% 6.3V X5R 201

TBT_B_CIO_SEL (34 IN) → BIASIN
DP_AUXIO_EN (84 15 IN) → AUXIO_EN
DP_TBTPB_AUXCH_C_N (98 34 IN) → C9630 0.1UF 10% 6.3V X5R 201 → AUX-
DP_TBTPB_AUXCH_C_P (98 34 IN) → C9631 0.1UF 10% 6.3V X5R 201 → AUX+
DP_TBTPB_AUXCH_N (98) → DP_TBTPB_AUXCH_P (98)
DP_TBTPB_DDC_DATA (83 IN) → DDC_DAT
DP_TBTPB_DDC_CLK (83 IN) → DDC_CLK
TBT_B_CONFIG1_BUF (34 OUT) → CA_DETOUT
DP_TBTPB_ML_C_P<1> (98 34 IN) → C9632 0.22UF 20% 6.3V X5R 0201 → DP+
DP_TBTPB_ML_C_N<1> (98 34 IN) → C9633 0.22UF 20% 6.3V X5R 0201 → DP-
DP_TBTPB_ML_P<1> (99) → DP_TBTPB_ML_N<1> (99)
TBT_B_LSTX (34 IN) → LSTX
TBT_B_LSRX_UNBUF → LSRX
TBT_B_DP_PWRDN (34 IN) → DP_PD
DP_TBTPB_HPD (34 OUT) → HPDOUT

DP_B_AUXCH_DDC_N (85 98) ← AUXIO-
DP_B_AUXCH_DDC_P (85 98) ← AUXIO+
TBT: RX_1 Bias Sink
TBT_B_CONFIG1_RC (85) ← CA_DET
DP_B_LSX_ML_P<1> (85 98) ← DPMLO+
DP_B_LSX_ML_N<1> (85 98) ← DPMLO-
TBT: LSX_A_R2P/P2R (P/N)
TBT_B_HPD (85) ← HPD

R9626 1M 5% 1/20W MF 201
R9628 100K 5% 1/20W MF 201

=PP3V3_S4_TBT
U9660 74AUP1T97 SOT891
TBT_B_LSRX (34 OUT)
C9660 0.1UF 10% 16V X5R-CERM 0201

L9600 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C9600 0.01UF 10% 50V X7R 402
C9601 0.01UF 10% 50V X7R 402
TBTBCONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V
R9601 12 5% 1/20W MF 201

C9605 0.01UF
TBTBCONN_1_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V) 10% 25V X5R-CERM 0201
DP Dir TBT Dir
TBT_B_R2D_P<0> (98)
TBT_B_R2D_N<0> (98)
TBT: TX_0
GND_VOID=TRUE (Both C's)
C9670 0.22UF 20% 6.3V X5R 0201
C9671 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<0> (IN 34 98)
TBT_B_R2D_C_N<0> (IN 34 98)
R9670 470K 5% 1/20W MF 201
R9671 470K 5% 1/20W MF 201

C9606 0.01UF
TBTBCONN_7_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V) 10% 25V X5R-CERM 0201
DP_B_LSX_ML_P<1> (85 98)
DP_B_LSX_ML_N<1> (85 98)
TBT: LSX_R2P/P2R (P/N)

CRITICAL J9400 DUAL-MDP-K70 F-ANG-TH
SHLD (58,57,56,55,54,53)
PORT B SHLD (65,64,63,62,61,60,59)

HPD	22	21	GND0
CONFIG1	24	23	ML_LANE0P
CONFIG2	26	25	ML_LANE0N
GND2	28	27	GND1
ML_LANE3P	30	29	ML_LANE1P
ML_LANE3N	32	31	ML_LANE1N
GND4	34	33	GND3
AUX_CHP	36	35	ML_LANE2P
AUX_CHN	38	37	ML_LANE2N
DP_PWR	40	39	RETURN

514-0824

TBT_B_R2D_P<1> (98)
TBT_B_R2D_N<1> (98)
TBT: TX_1
GND_VOID=TRUE (Both C's)
C9672 0.22UF 20% 6.3V X5R 0201
C9673 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_N<1> (IN 34 98)
TBT_B_R2D_C_P<1> (IN 34 98)
R9672 470K 5% 1/20W MF 201
R9673 470K 5% 1/20W MF 201

NOTE: Polarity Swapped for Layout!
470k R's for ESD protection on AC-coupled signals.

GND_VOID=TRUE (Both C's)
C9674 0.22UF 20% 6.3V X5R 0201
C9675 0.22UF 20% 6.3V X5R 0201
TBT_B_D2R_N<0> (98 34 OUT) → TBT_B_D2R_C_P<0> (98)
TBT_B_D2R_P<0> (98 34 OUT) → TBT_B_D2R_C_N<0> (98)
NOTE: Polarity Swapped for Layout!

R9694 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9695 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

C9678 0.22UF 20% 6.3V X5R 0201
C9679 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_C_P<3> (98 34 IN) → DP_TBTPB_ML_P<3> (98)
DP_TBTPB_ML_C_N<3> (98 34 IN) → DP_TBTPB_ML_N<3> (98)
R9678 470K 5% 1/20W MF 201
R9679 470K 5% 1/20W MF 201
TBT: Terminated

TBT_B_BIAS (85)
R9698 2.2K 5% 1/20W MF 201
R9699 2.2K 5% 1/20W MF 201

GND_VOID=TRUE (Both C's)
C9676 0.22UF 20% 6.3V X5R 0201
C9677 0.22UF 20% 6.3V X5R 0201
TBT_B_D2R_N<1> (98 34 OUT) → TBT_B_D2R_C_P<1> (98)
TBT_B_D2R_P<1> (98 34 OUT) → TBT_B_D2R_C_N<1> (98)
NOTE: Polarity Swapped for Layout!

CRITICAL
GND_VOID=TRUE (Both D's)
D9698 BAR90-02LRH TSLP-2-7 → TBT_B_D2R1_AUXDDC_P (98)
D9699 BAR90-02LRH TSLP-2-7 → TBT_B_D2R1_AUXDDC_N (98)

CRITICAL L9698 650NH-5%-0.430MA-0.52OHM 0603 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
CRITICAL L9699 650NH-5%-0.430MA-0.52OHM 0603 GND_VOID=TRUE SIGNAL_MODEL=EMPTY

DP_B_AUXCH_DDC_P (98 85)
DP_B_AUXCH_DDC_N (98 85)
C9698 30PF 5% 50V CERM 402
C9699 30PF 5% 50V CERM 402

TBT_B_HPD (85)
TBT_B_CONFIG1_RC (85)
TBT_B_CONFIG2_RC (34 OUT)
R9652 1M 5% 1/20W MF 201
R9651 1M 5% 1/20W MF 201
C9694 330PF 10% 16V X7R 201
C9695 330PF 10% 16V X7R 201
R9641 100K 5% 1/20W MF 201

C9602 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0745	138S0743		BLC_CAP	BLC Ouput Cap

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1592	152S1591		L9700	BLC Switch Inductor
371S0648	371S0694		D9700	BLC Switch Diode

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1054	376S1022		Q9700	BLC Switch FET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1071	376S1073		ALL	Short Protection FET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0845	376S1067		Q9702	BLC Inrush FET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S3665	1	IC,LP8561,LED BKLT CTRLR,LLP24,B0	U9700	CRITICAL	

SYNC_MASTER=D7_NICK SYNC_DATE=01/03/2012

PAGE TITLE: LCD Backlight Driver (LP8545)

Apple Inc.

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K70 Board Specific Physical and Spacing Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	*	0.076 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

Board Stack-up

Finished board thickness: 1.58 mm

Top	Signal	0.5 oz (Cu plated)	
	Prepreg	0.071 mm	
2	Plane	1 oz	
	Prepreg	0.076 mm	
3	Signal	0.5 oz	
	Prepreg	0.435 mm	
4	Plane	1 oz	
	Core	0.127 mm	
5	Plane	1 oz	
	Prepreg	0.435 mm	
6	Signal	0.5 oz	
	Prepreg	0.076 mm	
2	Plane	1 oz	
	Prepreg	0.071 mm	
Btm	Signal	0.5 oz (Cu plated)	

SYNC_MASTER=D7_DAVE SYNC_DATE=12/12/2011

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF

Minimum diff spacing is 4 mil
Table 3-5, Intel Doc# 473718

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2.5:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?

Main Segment Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Trace	Design (diff)	Iso	Design	Comments
3-2	4	9.84	15	19.69	CLK trace spacing controlled by =68_OHM_DIFF
3-3	8	9.84	12	13.78	
3-4	6	7.87	12	13.78	
3-5	8.5	7.87	12	11.81	DQ or DQS to other signals not in the same bytelane (but not ch)
					DQ to DQ in the same bytelane of the same channel
			10	11.81	DQ to DQS in the same bytelane of the same channel
			12	11.81	DQ or DQS in different bytelanes of the same channel
			25	25.59	DQ or DQS in different channels
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
T17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	12 29
T17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	12 29
T25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	8 12
T25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	8 12
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	12 29
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	12 29
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	12 29
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	8 12
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	8 12
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	8 12
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	12 29
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	12 29
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	12 29
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	12 29
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	12 29
T19 DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	12 31
T19 DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	12 31
T19 DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	12 31
T19 DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	12 31
T19 DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	12 31
T19 DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	12 31
T19 DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	12 31
T19 DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	12 31
T19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	12 31
T19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	12 31
T19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	12 31
T19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	12 31
T20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	12 31
T20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	12 31
T20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	12 31
T20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	12 31
T23 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	12 31
T23 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	12 31
T20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	12 31
T20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	12 31
T20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	12 31
T20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	12 31
T21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	12 31
T21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	12 31
Channel B				
T17 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	12 30
T17 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	12 30
T25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	8 12
T25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	8 12
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	12 30
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	12 30
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	12 30
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	8 12
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	8 12
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	8 12
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	12 30
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	12 30
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	12 30
T22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	12 30
T22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	12 30
T22 DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	12 31
T22 DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	12 31
T22 DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	12 31
T22 DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	12 31
T22 DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	12 31
T22 DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	12 31
T22 DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	12 31
T22 DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	12 31
T23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	12 31
T23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	12 31
T23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	12 31
T23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	12 31
T24 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	12 31
T24 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	12 31
T24 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	12 31
T24 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	12 31
T23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	12 31
T23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	12 31
T24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	12 31
T24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	12 31
T24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	12 31
T24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	12 31
T24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	12 31
T24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	12 31
Reset				
T24	DDR_50S		MEM_RESET_L	28 29 30

SYNC_MASTER=D7_DAVE SYNC_DATE=12/12/2011

PAGE TITLE: DDR3 Constraints

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

REVISION: 4.2.0

BRANCH:

PAGE: 101 OF 113

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PCI Express/DMI

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE3_PHY	*	PCIE_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
PEG_R2D	PEG_R2D	*	PEG_SAME_DIR
PEG_D2R	PEG_D2R	*	PEG_SAME_DIR
PEG_D2R	PEG_R2D	*	PEG_ALT_DIR
PEG_D2R	*	*	PEG_ISO
PEG_R2D	*	*	PEG_ISO

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PEG_SAME_DIR	*	=3.5X_DIELECTRIC	?
PEG_ALT_DIR	*	=7X_DIELECTRIC	?
PEG_ISO	*	=4:1_SPACING	?

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing	
x16 Graphics			
144P PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<15> 71
144J PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<15> 71
144T	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<15> 9 71
144S	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<15> 9 71
144G PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<15> 9 71
144D PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<15> 9 71
144C	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<15> 71
144F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<15> 71
144E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<14> 71
144H PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<14> 71
145C	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<14> 9 71
145B	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<14> 9 71
145E PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<14> 9 71
145C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<14> 9 71
145G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<14> 71
145F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<14> 71
145P PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<13> 71
145K PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<13> 71
145R	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<13> 9 71
146C	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<13> 9 71
145M PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<13> 9 71
146E PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<13> 9 71
146G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<13> 71
146F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<13> 71
146E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<12> 71
146H PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<12> 71
146J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<12> 9 71
146K	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<12> 9 71
146M PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<12> 9 71
147C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<12> 9 71
146G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<12> 71
147A	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<12> 71
147J PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<11> 71
147K PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<11> 71
147L	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<11> 9 71
147M	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<11> 9 71
147P PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<11> 9 71
147R PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<11> 9 71
147G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<11> 71
147F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<11> 71
148E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<10> 71
148J PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<10> 71
148K	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<10> 9 71
148L	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<10> 9 71
148R PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<10> 9 71
148P PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<10> 9 71
148J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<10> 71
148H	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<10> 71
148P PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<9> 71
148R PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<9> 71
149J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<9> 9 71
149K	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<9> 9 71
149P PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<9> 9 71
149R PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<9> 9 71
149G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<9> 71
149F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<9> 71
149E PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<8> 71
149J PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<8> 71
149K	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<8> 9 71
149L	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<8> 9 71
149R PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<8> 9 71
149P PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<8> 9 71
149J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<8> 71
149H	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<8> 71

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing	
x16 Graphics			
150P PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<7> 71
150J PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<7> 71
150T	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<7> 9 71
150S	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<7> 9 71
150G PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<7> 9 71
150D PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<7> 9 71
151C	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<7> 71
151B	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<7> 71
151E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<6> 71
151H PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<6> 71
151L	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<6> 9 71
151K	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<6> 9 71
151G PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<6> 9 71
151M PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<6> 9 71
151F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<6> 71
151E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<6> 71
152P PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<5> 71
152N PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<5> 71
152R	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<5> 9 71
152M	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<5> 9 71
152A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<5> 9 71
152B PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<5> 9 71
152G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<5> 71
152F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<5> 71
152E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<4> 71
152H PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<4> 71
153L	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<4> 9 71
153K	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<4> 9 71
153G PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<4> 9 71
153D PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<4> 9 71
153F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<4> 71
153E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<4> 71
154P PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<3> 71
154J PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<3> 71
154T	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<3> 9 71
154S	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<3> 9 71
154G PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<3> 9 71
154M PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<3> 9 71
154F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<3> 71
154E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<3> 71
155P PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<2> 71
155N PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<2> 71
155R	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<2> 9 71
155M	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<2> 9 71
155A PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<2> 9 71
155B PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<2> 9 71
155G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<2> 71
155F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<2> 71
156P PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<1> 71
156N PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<1> 71
156R	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<1> 9 71
156M	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<1> 9 71
156A PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<1> 9 71
156B PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<1> 9 71
156G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<1> 71
156F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<1> 71
156E PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<0> 71
156J PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<0> 71
156L	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<0> 9 71
156K	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<0> 9 71
156H PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<0> 9 71
156D PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<0> 9 71
156F	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<0> 71
156E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<0> 71
CPU PCIe Clocks			
166P PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P 18 71
166N PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N 18 71
CPU PCIe Compensation			
167P	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_COMP 10

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Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D
COMP_DMI_PHY	*	50_OHM_SE

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=7X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

SSD x2 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_SSD_R2D	PCIE_SSD_R2D	*	PCIE_SAME_DIR
PCIE_SSD_D2R	PCIE_SSD_D2R	*	PCIE_SAME_DIR
PCIE_SSD_D2R	PCIE_SSD_R2D	*	PCIE_ALT_DIR
PCIE_SSD_D2R	*	*	PCIE_ISO
PCIE_SSD_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

DMI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
DMI_SAME_DIR	*	=4X_DIELECTRIC	?
DMI_ALT_DIR	*	=5X_DIELECTRIC	?
DMI_ISO	*	=4X_DIELECTRIC	?

DMI x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_SAME_DIR
DMI_S2N	DMI_S2N	*	DMI_SAME_DIR
DMI_N2S	DMI_S2N	*	DMI_ALT_DIR
DMI_N2S	*	*	DMI_ISO
DMI_S2N	*	*	DMI_ISO

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<3..0>	34
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<3..0>	34
	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<3..0>	18 34
	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<3..0>	18 34
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<3..0>	18 34
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<3..0>	18 34
	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<3..0>	34
	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<3..0>	34
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	18 34
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	18 34
x2 SSD				
PCIE_GEN2_R2D_CONN_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_P<1>	41
PCIE_GEN2_R2D_CONN_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_N<1>	41
	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_P<1>	18 41
	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_N<1>	18 41
PCIE_GEN2_D2R_CONN_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_P<1>	18 41
PCIE_GEN2_D2R_CONN_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_N<1>	18 41
	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_P<1>	41
	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_N<1>	41
PCIE_GEN2_R2D_MUX_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_P<0>	41
PCIE_GEN2_R2D_MUX_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_N<0>	41
	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_P<0>	18 41
	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_N<0>	18 41
PCIE_GEN2_D2R_MUX_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_P<0>	18 41
PCIE_GEN2_D2R_MUX_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_N<0>	18 41
	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_P<0>	41
	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_N<0>	41
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_P	18 41
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_N	18 41
x1 AirPort				
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	33
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	33
	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	18 33
	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	18 33
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	18 33
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	18 33
	PCIE_PHY	PCIE	PCIE_AP_D2R_C_P	
	PCIE_PHY	PCIE	PCIE_AP_D2R_C_N	
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	18 33
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	18 33
x1 Caesar IV				
PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	37
PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	37
	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	18 37
	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	18 37
PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	18 37
PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	18 37
	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	37
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	18 37
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	18 37

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_P<3..0>	10 19
DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_N<3..0>	10 19
DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_P<3..0>	10 19
DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_N<3..0>	10 19
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
DMI Compensation				
	COMP_DMI_PHY	COMP_PCIE	PCH_DMI_COMP	19

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_90D
COMP_SATA_PHY	*	SATA_50S

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

FDI

FDI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FDI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI	*	Y	0.25 MM	0.25 MM	3 MM	=STANDARD	=STANDARD
FDI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FDI_DIFF_PHY	*	FDI_85D
FDI_SE_PHY	*	FDI_50S
COMP_FDI_PHY	*	COMP_FDI

FDI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FDI_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FDI	*	*	FDI_ISO
COMP_FDI	*	*	COMP_FDI_ISO

FDI Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Imp	Design	Iso	Design	Comments
6-1/6-2	85	85	12	11.81	FDI main length

FDI Compensation Rules (mils)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	55	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
T80 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_P	41
T82 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_N	41
T88	SATA_PHY	SATA	SATA_HDD_R2D_C_P	18 41
T89	SATA_PHY	SATA	SATA_HDD_R2D_C_N	18 41
T84 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_P	18 41
T85 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_N	18 41
T91	SATA_PHY	SATA	SATA_HDD_D2R_C_P	41
T93	SATA_PHY	SATA	SATA_HDD_D2R_C_N	41
PCH SATA Port 1 (SSD)				
T97 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_P	41
T99 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_N	41
T86	SATA_PHY	SATA	SATA_SSD_R2D_C_P	18 41
T88	SATA_PHY	SATA	SATA_SSD_R2D_C_N	18 41
T100 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_P	18 41
T102 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_N	18 41
T106	SATA_PHY	SATA	SATA_SSD_D2R_C_P	41
T104	SATA_PHY	SATA	SATA_SSD_D2R_C_N	41
SSD PCIe/SATA Mux Output				
T111 PCIE_SATA_R2D_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_R2D_P	41
T110 PCIE_SATA_R2D_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_R2D_N	41
T117 PCIE_SATA_D2R_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_D2R_P	41
T116 PCIE_SATA_D2R_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_D2R_N	41
PCH SATA Compensation				
T120	COMP_SATA_PHY	COMP_SATA	PCH_SATA1COMP	18
T126	COMP_SATA_PHY	COMP_SATA	PCH_SATA3COMP	18
T128	COMP_SATA_PHY	COMP_SATA	PCH_SATA3RBIAS	18

FDI

Electrical Contraint Set	Physical	Spacing		
FDI				
T109 FDI_TX	FDI_DIFF_PHY	FDI	CPU_FDI_TX_P<7..0>	8 10
T131 FDI_TX	FDI_DIFF_PHY	FDI	CPU_FDI_TX_N<7..0>	8 10
T113	FDI_SE_PHY	FDI	CPU_FDI_FSYNC<1..0>	8 10
T112	FDI_SE_PHY	FDI	CPU_FDI_LSYNC<1..0>	8 10
T135	FDI_SE_PHY	FDI	CPU_FDI_INT	8 10
FDI Compensation				
T136	COMP_FDI_PHY	COMP_FDI	CPU_FDI_COMPIO	10

XDP

Electrical Contraint Set	Physical	Spacing		
CPU XDP				
T37	XDP_PHY	XDP	XDP_BPM_L<7..0>	11 25
T38	XDP_PHY	XDP	CPU_CFG<17..0>	8 10 15 25
T39 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	11 15
T40 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	11 15
T41	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	15 18 25
T43	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	15 18 25
T42	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	25
T44	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	25
T45	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	11 25
T46	XDP_PHY	XDP	XDP_CPU_TMS	11 25
T47	XDP_PHY	XDP	XDP_CPU_TDI	11 25
T48	XDP_PHY	XDP	XDP_CPU_TDO	11 25
PCH XDP				
T49	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	18 25
T50	XDP_PHY	XDP	XDP_PCH_TMS	18 25
T51	XDP_PHY	XDP	XDP_PCH_TDI	18 25
T52	XDP_PHY	XDP	XDP_PCH_TDO	18 25

SYNC_MASTER=D7_DAVE SYNC_DATE=12/12/2011

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	=2:1_SPACING	?

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI	*	=2:1_SPACING	?

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5:1_SPACING	?
CLK_LPC	*	=2:1_SPACING	?

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=2:1_SPACING	?

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
H33J	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	18 26
H32J	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	20 26

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
H33D	LPC_55S	LPC	LPC_AD<3..0>	18 44 46
H33B	LPC_55S	LPC	LPC_R_AD<3..0>	18
H33C	LPC_55S	LPC	LPC_FRAME_L	18 44 46
H33F	LPC_55S	LPC	LFRAME_L	18
LPC Clocks				
H33G	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	26 46
H34G	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 26
H34J	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	26 44
H34F	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	20 26

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
H38D	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB	26
H36D	CLK_PCH_55S	CLK_PCH	PCH_CLK25M_XTALIN	18 26
PCH Ref Clock Comp				
H34D	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP	18
PCH RTC 32K				
H44J	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 26
H43J	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 26
H52J	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	26
SMC 32K				
H39D	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	19 45
H45D	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	44 45

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
H47J	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	26
H48J	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	26
H49J	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	26
25M Reference Clocks				
H48C	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET	26 37
H49C	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET_R	26
H38D	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT	26 34
H39D	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT_R	34

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
H35D	HDA_55S	HDA	HDA_BIT_CLK	18 52
H34D	HDA_55S	HDA	HDA_BIT_CLK_R	18
H36D	HDA_55S	HDA	HDA_RST_L	18 52
H40D	HDA_55S	HDA	HDA_RST_R_L	18
H46D	HDA_55S	HDA	HDA_SDOUT	18 52
H38D	HDA_55S	HDA	HDA_SDOUT_R	15 18
H37D	HDA_55S	HDA	HDA_SYNC	15 18 52
H39D	HDA_55S	HDA	HDA_SYNC_R	18
H41D	HDA_55S	HDA	HDA_SDIN0	18 52
H42D	HDA_55S	HDA	AUD_SDI_R	52
SPDIF				
H47K		HDA	AUD_SPDIF_CHIP	52
H47J		HDA	AUD_SPDIF_OUT	52 56

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
H49J	SPI_50S	SPI	SPI_CLK_R	18 46
H49K	SPI_50S	SPI	SPI_CLK	46
H49L	SPI_50S	SPI	SPI_ALT_CLK	46
H48K	SPI_50S	SPI	SPI_SMC_CLK	44 45
H48J	SPI_50S	SPI	SPI_MLB_CLK	45 46
H39K	SPI_50S	SPI	SPI_CS0_R_L	18 46
H39L	SPI_50S	SPI	SPI_CS0_L	46
H39M	SPI_50S	SPI	SPI_ALT_CS_L	46
H40K	SPI_50S	SPI	SPI_SMC_CS_L	44 45
H40J	SPI_50S	SPI	SPI_MLB_CS_L	45 46
H39K	SPI_50S	SPI	SPI_MOSI_R	18 46
H46K	SPI_50S	SPI	SPI_MOSI	46
H46L	SPI_50S	SPI	SPI_ALT_MOSI	46
H43K	SPI_50S	SPI	SPI_SMC_MOSI	44 45
H43J	SPI_50S	SPI	SPI_MLB_MOSI	45 46
H40K	SPI_50S	SPI	SPI_MISO	18 46
H40L	SPI_50S	SPI	SPI_ALT_MISO	46
H43K	SPI_50S	SPI	SPI_SMC_MISO	44 45
H43J	SPI_50S	SPI	SPI_MLB_MISO	45 46
H49K	SPI_50S	SPI	SPIROM_USE_MLB	21 46

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D

USB-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=3:1_SPACING	?
USB2_ISO	TOP,BOTTOM	=3:1_SPACING	?
USB3_ISO	*	=5.5:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB3	*	*	USB3_ISO

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S
CIV_SPI	*	SPI_55S

CIV-specific Spacing Definitions
Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

Constraints
Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

2 kV isolation

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

Camera Processor’s SMIA Interface Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D

Camera Processor’s SMIA Interface Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing	
External Port A (J4600)			
J42C USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P 42
J42D USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N 42
J43C	USB3_PHY	USB3	USB3_EXTA_RX_F_P 20 42
J43D	USB3_PHY	USB3	USB3_EXTA_RX_F_N 20 42
J41C USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P 20 42
J41D USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N 20 42
J43A	USB3_PHY	USB3	USB3_EXTA_TX_F_P 42
J43B	USB3_PHY	USB3	USB3_EXTA_TX_F_N 42
J49C	USB3_PHY	USB3	USB3_EXTA_TX_C_P 42
J49D	USB3_PHY	USB3	USB3_EXTA_TX_C_N 42
J41A USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_P 20 42
J41B USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_N 20 42
J41C	USB2_PHY	USB2	USB2_EXTA_MUXED_P 42
J42C	USB2_PHY	USB2	USB2_EXTA_MUXED_N 42
J49A	USB2_PHY	USB2	USB2_EXTA_P 42
J49B	USB2_PHY	USB2	USB2_EXTA_N 42
External Port B (J4610)			
J42A USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P 42
J42B USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N 42
J42C	USB3_PHY	USB3	USB3_EXTB_RX_F_P 20 42
J42A	USB3_PHY	USB3	USB3_EXTB_RX_F_N 20 42
J42C USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P 20 42
J42D USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N 20 42
J42A	USB3_PHY	USB3	USB3_EXTB_TX_F_P 42
J42B	USB3_PHY	USB3	USB3_EXTB_TX_F_N 42
J49C	USB3_PHY	USB3	USB3_EXTB_TX_C_P 42
J49D	USB3_PHY	USB3	USB3_EXTB_TX_C_N 42
J43C USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_P 20 42
J43D USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_N 20 42
J43A	USB2_PHY	USB2	USB_PCH_9_P 20 42
J43B	USB2_PHY	USB2	USB_PCH_9_N 20 42
J43C	USB2_PHY	USB2	USB2_EXTB_MUXED_P 42
J43D	USB2_PHY	USB2	USB2_EXTB_MUXED_N 42
J43A	USB2_PHY	USB2	USB2_EXTB_P 42
J43B	USB2_PHY	USB2	USB2_EXTB_N 42
External Port C (J4700)			
J43C USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P 43
J43D USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N 43
J43C	USB3_PHY	USB3	USB3_EXTC_RX_F_P 20 43
J44C	USB3_PHY	USB3	USB3_EXTC_RX_F_N 20 43
J44A USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P 20 43
J44B USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N 20 43
J44A	USB3_PHY	USB3	USB3_EXTC_TX_F_P 43
J44B	USB3_PHY	USB3	USB3_EXTC_TX_F_N 43
J49C	USB3_PHY	USB3	USB3_EXTC_TX_C_P 43
J49D	USB3_PHY	USB3	USB3_EXTC_TX_C_N 43
J44C USB2_CONN	USB2_PHY	USB2	USB_PCH_2_P 20 43
J44D USB2_CONN	USB2_PHY	USB2	USB_PCH_2_N 20 43
J43C	USB2_PHY	USB2	USB2_EXTC_P 43
J49C	USB2_PHY	USB2	USB2_EXTC_N 43
External Port D (J4710)			
J45C USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P 43
J45D USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N 43
J45C	USB3_PHY	USB3	USB3_EXTD_RX_F_P 20 43
J45C	USB3_PHY	USB3	USB3_EXTD_RX_F_N 20 43
J45A USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P 20 43
J45C USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N 20 43
J46C	USB3_PHY	USB3	USB3_EXTD_TX_F_P 43
J45B	USB3_PHY	USB3	USB3_EXTD_TX_F_N 43
J49B	USB3_PHY	USB3	USB3_EXTD_TX_C_P 43
J49C	USB3_PHY	USB3	USB3_EXTD_TX_C_N 43
J46A USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_P 20 43
J46B USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_N 20 43
J46C	USB2_PHY	USB2	USB_PCH_10_P 20 43
J46A	USB2_PHY	USB2	USB_PCH_10_N 20 43
J46C	USB2_PHY	USB2	USB2_EXTD_MUXED_P 43
J46D	USB2_PHY	USB2	USB2_EXTD_MUXED_N 43
J46C	USB2_PHY	USB2	USB2_EXTD_P 43
J46B	USB2_PHY	USB2	USB2_EXTD_N 43
Camera (J3510)			
J42C USB2_CONN_TNT	USB2_PHY	USB2	USB_CAMERA_P 40
J42D USB2_CONN_TNT	USB2_PHY	USB2	USB_CAMERA_N 40
PCH USB Compensation			
J48C	PCH_55S	COMP_PCH	PCH_USB_RBIAS 20

RMH Love

Electrical Contraint Set	Physical	Spacing	
USB 2.0 Hub			
J48C USB2_HUB	USB2_PHY	USB2	USB_PCH_7_P 20 27
J48D USB2_HUB	USB2_PHY	USB2	USB_PCH_7_N 20 27
J48C USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_P 27 33
J41C USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_N 27 33
J45C USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_MUX_P 33
J45C USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_MUX_N 33
J47C USB2_HUB_RES	USB2_PHY	USB2	USB_SMC_P 27 44
J47D USB2_HUB_RES	USB2_PHY	USB2	USB_SMC_N 27 44
J46C	USB2_PHY	USB2	USB_HUB_2_P 27
J47C	USB2_PHY	USB2	USB_HUB_2_N 27
USB 2.0 Hub Compensation			
J47A	PCH_55S	COMP_PCH	USB_HUB_RBIAS 27
USB 2.0 Hub Crystal			
J47B	CLK_XTAL	XTAL	USB_HUB_XTAL1 27
J47A	CLK_XTAL	XTAL	USB_HUB_XTAL2 27

Et tu Brute?

Electrical Contraint Set	Physical	Spacing	
Ethernet			
J47C ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0> 37 38
J47D ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0> 37 38
J47C	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0> 38
J47D	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0> 38
J51C		ENET_TRANS	ENETCONN_MCT0 38
J49C		ENET_TRANS	ENETCONN_MCT1 38
J49A		ENET_TRANS	ENETCONN_MCT2 38
J49B		ENET_TRANS	ENETCONN_MCT3 38
J49A		ENET_TRANS	ENETCONN_MCT_BS 38
J47C	ENET_COMP_PHY	COMP_ENET	ENET_RDAC 37
SD			
J47C SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0> 37
J48C	SD_PHY	SD	SDCONN_DATA<7..0> 37 39
J51C	SD_PHY	SD	SDCONN_DATA_R <7..0> 39
J48C SD_CMD	SD_PHY	SD	ENET_SD_CMD 37
J48D	SD_PHY	SD	SDCONN_CMD 37 39
J51C	SD_PHY	SD	SDCONN_CMD_R 39
J48C SD_CLK	SD_PHY	SD	ENET_SD_CLK 37
J48A	SD_PHY	SD	SDCONN_CLK 37 39
J48B	SD_PHY	SD	SDCONN_CLK_R 39
J48B	SD_PHY	SD	ENET_MEDIA_SENSE 15 18 37
J48B	SD_PHY	SD	ENET_SD_DETECT_L 37 39
J48F	SD_PHY	SD	SDCONN_WP 37 39
CIV SPI			
J48C	CIV_SPI	SPI	ENET_SCLK 37
J48D	CIV_SPI	SPI	ENET_MISO 37
J49C	CIV_SPI	SPI	ENET_MOSI 37
J49D	CIV_SPI	SPI	ENET_CS_L 37

Camera Processor-Camera Sensor I/F

Electrical Contraint Set	Physical	Spacing	
J50A SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P 40
J50C SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N 40
J52C SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_F_P 40
J52A SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_F_N 40
J50A SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P 40
J50B SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N 40
J52C SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_F_P 40
J52A SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_F_N 40
J50A	SPI_50S	SPI	CAM_SF_CLK 40
J50B	SPI_50S	SPI	CAM_SF_CLK_R 40
J50C	SPI_50S	SPI	CAM_SF_DIN 40
J51C	SPI_50S	SPI	CAM_SF_DIN_R 40
J51A	SPI_50S	SPI	CAM_SF_CS_L 40
J51B	SPI_50S	SPI	CAM_SF_WP_L 40
J51C	SPI_50S	SPI	CAM_SF_DOUT 40
J51D	SPI_50S	SPI	CAM_SF_DOUT_R 40
J51A	SMB_PHY	SMB	I2C_CAMSENSOR_SDA 40
J51B	SMB_PHY	SMB	I2C_CAMSENSOR_SCL 40

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SMBus

Electrical Contraint Set	Physical	Spacing		
SMC				
I10	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	44 47
I9	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	44 47
I11	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	44 47
I12	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	44 47
I13	SMB_PHY	SMB	SMBUS_SMC_2_S4_SCL	44 47
I14	SMB_PHY	SMB	SMBUS_SMC_2_S4_SDA	44 47
I15	SMB_PHY	SMB	SMBUS_SMC_3_SCL	44 47
I16	SMB_PHY	SMB	SMBUS_SMC_3_SDA	44 47
I19	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	44 45
I20	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	44 45
PCH				
I51	TBT_I2C_5SS	TBT_I2C	SMBUS_PCH_CLK	18 47
I52	TBT_I2C_5SS	TBT_I2C	SMBUS_PCH_DATA	18 47
I53	SMB_PHY	SMB	SML_PCH_0_CLK	18 47
I54	SMB_PHY	SMB	SML_PCH_0_DATA	18 47
Display TCon				
I55	SMB_PHY	SMB	SMB_DP_TCON_SCL	47 81
I66	SMB_PHY	SMB	SMB_DP_TCON_SDA	47 81

Temperature Sense

Electrical Contraint Set	Physical	Spacing		
EMC1414-1 (Production)				
I57 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_P	50
I58 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_N	50
I59 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_2_P	50
I60 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_2_N	50
I65 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_P	6 50
I66 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_N	6 50
TMP423 (Development)				
I67 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_P	50
I68 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_N	50
I69 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_P	50
I70 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_N	50
I63 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_SKIN_P	50
I62 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_SKIN_N	50
I71 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_P	50
I72 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_N	50
HDD Out-of-Band				
I73		SENSE	SMC_HDD_OOB_TEMP	
I74		SENSE	HDD_OOB_TEMP_CONN	
I75		SENSE	HDD_OOB_TEMP_FILT	
I76		SENSE	HDD_OOB_TEMP_R	
SSD Out-of-Band				
I77		SENSE	SMC_SSD_OOB_TEMP	
I78		SENSE	SMC_SSD_TEMP_CTL	
I79		SENSE	SSD_OOB_TEMP	

SMC

Electrical Contraint Set	Physical	Spacing		
SMC				
I1	CLK_XTAL	XTAL	SMC_XTAL	44 45
I2	CLK_XTAL	XTAL	SMC_EXTAL	44 45

Current/Voltage Sense

Electrical Contraint Set	Physical	Spacing		
Common				
I3		SENSE	GND_SMC_AVSS	44 45 48 49
12V S5 (System Total)				
I4 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_P	48
I5 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_N	48
I6		SENSE	ISNS_P12VG3H_R	48
I7		SENSE	ISNS_P12VG3H	45 48
I8		SENSE	VSNS_P12VG3H	45 48
12V S0 (GPU Core)				
I22 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_P	48
I23 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_N	48
I24		SENSE	ISNS_P12VS0_GPUCORE_R	48
I25		SENSE	ISNS_P12VS0_GPUCORE	45 48
I26		SENSE	VSNS_P12VS0_GPUCORE	45 48
HDD				
I80 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_P	48
I82 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_N	48
I83		SENSE	ISNS_HDDS0_R	48
I89		SENSE	ISNS_HDDS0	45 48
I84		SENSE	VSNS_HDDS0	45 48
SSD				
I85 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_P	49
I87 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_N	49
I86		SENSE	ISNS_SSDS0_R	49
I88		SENSE	ISNS_SSDS0	45 49
I89		SENSE	VSNS_SSDS0	45 49
VDDQ S3 (DDR)				
I33 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_P	49
I32 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_N	49
I35		SENSE	ISNS_VDDQS3_DDR_R	49
I34		SENSE	ISNS_VDDQS3_DDR	45 49
I36		SENSE	VSNS_VDDQS3_DDR	45 49
VDDQ S0 (GPU Uncore)				
I37 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUUC_P	48
I38 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUUC_N	48
I39		SENSE	ISNS_P12VS0_GPUUC_R	48
I40		SENSE	ISNS_P12VS0_GPUUNCORE	45 48
I41		SENSE	VSNS_P12VS0_GPUUNCORE	45 48
CPU Core				
I42 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUCORE_P	48
I43 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUCORE_N	48
I44		SENSE	ISNS_CPUCORE_FB	48
I45		SENSE	ISNS_CPUCORE	45 48
I46		SENSE	VSNS_CPUCORE	45 48
CPU AXG				
I47 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUAXG_P	48
I48 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUAXG_N	48
I49		SENSE	ISNS_CPUAXG_FB	48
I50		SENSE	ISNS_CPUAXG	45 48
I51		SENSE	VSNS_CPUAXG	45 48

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

VDDQ S3 (1.5V)/VTT S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I143	POWER	POWER	5V			REG_V5IN_U7700	68
Local Ground							
I144	GND	GND	0V			AGND_VDDQS3	68
VDDQ S3							
I145	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3	68
I147	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L	68
I146	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3	68
I148	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC	68
I149	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3	68
I150	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3_R	68
I152	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VDDQS3	68
I151	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3	68
I154	POWER	POWER	1.5V			PPVDDQ_S3_SENSE	
I153	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS	68
I155	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF	68
I156	VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN	68
I157	VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE	68
I158	VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP	68
I159	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS	68
Output Bus							
I160	POWER	POWER	1.5V			PPVDDQ_S3	6
I161	POWER_DDR	POWER_DDR	0.75V			PPDDRVTT_S3	6
I162	POWER_DDR	POWER_DDR	0.75V			PPDDRVTT_S0	6
FET Switched							
I163	POWER	POWER	1.5V			PP1V5_S0	6
Sensed							
I164	POWER	POWER	1.5V			PPVDDQ_S3_DDR	6

CPU VccIO/ PCH 1.05V S0

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus								
I1		POWER	POWER	5V			REG_VCC_U7400	65
I2		POWER	POWER	5V			REG_PVCC_U7400	65
Local Ground								
I3		GND	GND	0V			AGND_P1V05S0	65
1.05V S0								
I5		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0	65
I4		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L	65
I7		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0	65
I6		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC	65
I8		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0	65
I9		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R	65
I10		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V05S0	65
I12		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V05S0	65
I11		VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET	65
I14		VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO	65
I13	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE				SNS_CPU_VCCIO_P	13 65
I15	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE				SNS_CPU_VCCIO_N	13 65
I16		SNS_DIFF_PHY	SENSE				SNS_P1V05S0_XW_P	65
I17		SNS_DIFF_PHY	SENSE				SNS_P1V05S0_XW_N	65
I19			SENSE				REG_P1V05S0_FB	65
I18			SENSE				REG_P1V05S0_RTN	65
I21		VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF	65
I20		VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL	65
Output Bus								
I22		POWER	POWER	1.05V			PP1V05_S0	6
FET Switched								
I23		POWER	POWER	1.05V			PP1V05_TBTLC	6
I66		POWER	POWER	1.05V			PP1V05_TBTCIO	6

CPU VccSA

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus								
I24		POWER	POWER	5V			REG_VCC_U7500	66
I25		POWER	POWER	5V			REG_PVCC_U7500	66
Local Ground								
I26		GND	GND	0V			AGND_VCCSAS0	66
VCCIO								
I27		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VCCSAS0	66
I28		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VCCSAS0	66
I29		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VCCSAS0_RC	66
I31		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VCCSAS0	66
I30		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VCCSAS0	66
I33		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VCCSAS0	66
I32		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_OCSET	66
I35		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_VO	66
I34			SENSE				SNS_CPU_VCCSA	13 66
I37	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE				SNS_VCCSAS0_XW_P	66
I36	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE				SNS_VCCSAS0_XW_N	66
I38			SENSE				REG_VCCSAS0_FB	66
I39			SENSE				REG_VCCSAS0_RTN	66
I40		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_SREF	66
I41		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_FSEL	66
Output Bus								
I42		POWER	POWER	0.925V			PPVCCSA_S0	6

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CPU Core Phases

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
	Input Bus						
H109		POWER	POWER	12V			PP12V_S0_CPUCORE_FLT 62 63 64
H110		POWER	POWER	5V			REG_VCC_U7100 62
	Local Ground						
H120		GND	GND	0V			AGND_CPU 62 63 64
	Phase 1						
H103		POWER	POWER	12V			REG_LVCC_U7210 63
H106		VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1 62 63
H108		VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1_R 62
H107		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_1 63
H104		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_1 63
H105		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_1_RC 63
H098		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_1 63
H099		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUCORE_1 63
H092		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUCORE_1 63
H097		POWER	POWER	1.1V			PPCPUCORE_S0_SENSE_1 63
H095	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_P 62 63
H094	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_N 63
H096			SENSE				REG_ISENCORE_1_NR 62 63
	Phase 2						
H113		POWER	POWER	12V			REG_LVCC_U7230 63
H116		VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2 62 63
H114		VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2_R 62
H117		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_2 63
H118		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_2 63
H119		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_2_RC 63
H148		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_2 63
H149		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUCORE_2 63
H146		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUCORE_2 63
H115		POWER	POWER	1.1V			PPCPUCORE_S0_SENSE_2 63
H112	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_P 62 63
H111	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_N 63
H145			SENSE				REG_ISENCORE_2_NR 62 63
	Phase 3						
H133		POWER	POWER	12V			REG_LVCC_U7250 63
H136		VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3 62 63
H134		VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3_R 62
H137		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_3 63
H138		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_3 63
H139		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_3_RC 63
H140		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_3 63
H141		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUCORE_3 63
H142		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUCORE_3 63
H135		POWER	POWER	1.1V			PPCPUCORE_S0_SENSE_3 63
H131	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_P 62 63
H132	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_N 63
H143			SENSE				REG_ISENCORE_3_NR 62 63

CPU AXG Phase and Core Controller

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
	AXG						
H119		POWER	POWER	12V			REG_LVCC_U7330 64
H149		VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG 62 64
H151		VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG_R 62
H150		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUAXG 64
H148		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUAXG 64
H147		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUAXG_RC 64
H146		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUAXG 64
H145		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUAXG 64
H144		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUAXG 64
H143		POWER	POWER	1.1V			PPCPUAXG_S0_SENSE 64
H140	ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_P 64
H139	ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_N 64
H138			SENSE				REG_ISENAXG_PR 62 64
H137			SENSE				REG_ISENAXG_NR 62 64
	ISL6364						
H102		VR_CTL_PHY	VR_CTL				REG_CPUCORE_COMP 62
H097		VR_CTL_PHY	VR_CTL				CPUCORE_COMP_RC 62
H101		VR_CTL_PHY	VR_CTL				REG_CPUCORE_FB 62
H102		VR_CTL_PHY	VR_CTL				CPUCORE_FB_RC 62
H103		VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_1 62
H104		VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_2 62
H105		VR_CTL_PHY	VR_CTL				CPUCORE_PSICOMP_RC 62
H100		VR_CTL_PHY	VR_CTL				REG_CPUCORE_PSICOMP 62
H106		VR_CTL_PHY	VR_CTL				REG_CPUCORE_HFCOMP 62
H163	VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_P 13 62
H164	VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_N 13 62
H161		SNS_DIFF_PHY	SENSE				SNS_VCORE_R_P 62
H160		SNS_DIFF_PHY	SENSE				SNS_VCORE_R_N 62
H162		SNS_DIFF_PHY	SENSE	1.1V			SNS_VCORE_XW_P 62
H159		SNS_DIFF_PHY	SENSE	0V			SNS_VCORE_XW_N 62
H165			SENSE				REG_CPUCORE_VSEN 62
H166			SENSE				REG_CPUCORE_RGND 62
H155		VR_CTL_PHY	VR_CTL				REG_CPUCORE_IMON 48 62
H154		VR_CTL_PHY	VR_CTL				CPUCORE_IMON_R 62
H156		VR_CTL_PHY	VR_CTL				REG_CPUCORE_TM 62
H098		VR_CTL_PHY	VR_CTL				REG_CPUCORE_SUTH 62
H099		VR_CTL_PHY	VR_CTL				REG_CPUCORE_NPSI 62
H096		VR_CTL_PHY	VR_CTL				REG_CPUCORE_FDVID 62
H095		VR_CTL_PHY	VR_CTL				REG_CPUCORE_IAUTO 62
H093		VR_CTL_PHY	VR_CTL				REG_CPUCORE_SW_FREQ 62
H157		VR_CTL_PHY	VR_CTL				REG_CPUCORE_RAMPADJ 62
H158		VR_CTL_PHY	VR_CTL				REG_CPUCORE_EN_PWR 62
H094		VR_CTL_PHY	VR_CTL				CPUCORE_EN_PWR_R 62
H153		VR_CTL_PHY	VR_CTL				REG_CPUCORE_RSET 62
H191		VR_CTL_PHY	VR_CTL				REG_CPUAXG_COMP 62
H197		VR_CTL_PHY	VR_CTL				CPUAXG_COMP_RC 62
H193		VR_CTL_PHY	VR_CTL				REG_CPUAXG_FB 62
H194		VR_CTL_PHY	VR_CTL				CPUAXG_FB_RC 62
H195		VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_1 62
H196		VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_2 62
H192		VR_CTL_PHY	VR_CTL				REG_CPUAXG_HFCOMP 62
H202	VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_P 13 62
H203	VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_N 13 62
H201		SNS_DIFF_PHY	SENSE				SNS_VAXG_R_P 62
H200		SNS_DIFF_PHY	SENSE				SNS_VAXG_R_N 62
H199		SNS_DIFF_PHY	SENSE	1.1V			SNS_VAXG_XW_P 62
H198		SNS_DIFF_PHY	SENSE	0V			SNS_VAXG_XW_N 62
H167			SENSE				REG_CPUAXG_VSEN 62
H168			SENSE				REG_CPUAXG_RGND 62
H169		VR_CTL_PHY	VR_CTL				REG_CPUAXG_IMON 48 62
H170		VR_CTL_PHY	VR_CTL				CPUAXG_IMON_R 62
H174		VR_CTL_PHY	VR_CTL				REG_CPUAXG_TM 62
H173		VR_CTL_PHY	VR_CTL				REG_CPUAXG_TCOMP 62
H172		VR_CTL_PHY	VR_CTL				REG_CPUAXG_SW_FREQ 62
H180		VR_VID_PHY	VR_VID				CPU_VIDSCLK 13 62
H181		VR_VID_PHY	VR_VID				CPU_VIDSCLK_R 13
H182		VR_VID_PHY	VR_VID				CPU_VIDALERT_L 13 62
H183		VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L 13
H184		VR_VID_PHY	VR_VID				CPU_VIDSOUT 13 62
H185		VR_VID_PHY	VR_VID				CPU_VIDSOUT_R 13
	Output Bus						
H186		POWER	POWER	1.1V			PPVCORE_S0_CPU 6
H187		POWER	POWER	1.1V			PPVAXG_S0 6

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GPU Core Phases and Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
U120	POWER	POWER	12V			REG_PVCC_U8900 80
U120	POWER	POWER	5V			REG_VCC_U8900 80
Phase 1						
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1 80
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1 80
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC 80
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1 80
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_1 80
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_ISEN_GPUCORE_1 80
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_GPUCORE_1 80
Phase 2						
U120	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2 80
U120	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_2 80
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC 80
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2 80
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_2 80
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_ISEN_GPUCORE_2 80
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_GPUCORE_2 80
ISL6568						
U127	VR_CTL_PHY	VR_CTL				REG_GPUCORE_ICOMP 80
U127	VR_CTL_PHY	VR_CTL				REG_GPUCORE_OCSET 80
U120	VR_CTL_PHY	VR_CTL				GPUCORE_ICOMP_R 80
U120	VR_CTL_PHY	VR_CTL				REG_GPUCORE_IREF 80
U120	VR_CTL_PHY	VR_CTL				REG_GPUCORE_ISUM 80
U120	VR_CTL_PHY	VR_CTL				REG_GPUCORE_COMP 80
U120	VR_CTL_PHY	VR_CTL				GPUCORE_COMP_RC 80
U120	VR_CTL_PHY	VR_CTL				REG_GPUCORE_VDIFF 80
U131	VR_CTL_PHY	VR_CTL				GPUCORE_VDIFF_R 80
U131	VR_CTL_PHY	VR_CTL				GPUCORE_VDIFF_RC 80
U131	VR_CTL_PHY	VR_CTL				REG_GPUCORE_FB 80
U130	VSNS_GPU_CORE	SNS_DIFF_PHY	SENSE			SNS_GPU_CORE_P 79 80
U130	VSNS_GPU_CORE	SNS_DIFF_PHY	SENSE			SNS_GPU_CORE_N 79 80
U131			SENSE			REG_GPUCORE_VSEN 80
U131			SENSE			REG_GPUCORE_RGND 80
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID4 80
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID3 80
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID2 80
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID1 80
U132	VR_VID_PHY	VR_VID				REG_GPUCORE_VID0 80
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_MODE 80
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_REF 80
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_OFS 80
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_FS 80
Output Bus						
U120	POWER	POWER	1.0V			PPVCORE_S0_GPU 6

GPU 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
U139	POWER	POWER	5V			REG_VCC_U8300 74
Local Ground						
U139	GND	GND	0V			P1V05_GPU_AGND 74
1.05V S0						
U138	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPU_P1V05S0 74
U138	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPU_P1V05S0_L 74
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPU_P1V05S0 74
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPU_P1V05S0_RC 74
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPU_P1V05S0 74
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPU_P1V05S0_R 74
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPU_P1V05S0 74
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_OCSET_R 74
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_VO_R 74
U140	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_OCSET 74
U140	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_VO 74
U140	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE			SNS_GPU_PEX_IOVDD_P 74 79
U140	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE			SNS_GPU_PEX_IOVDD_N 74 79
U141			SENSE			REG_GPU_P1V05S0_FB 74
U141			SENSE			REG_GPU_P1V05S0_RTN 74
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_SREF 74
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_FSEL 74
Output Bus						
U141	POWER	POWER	1.05V			PP1V05_S0_GPU 6

GPU VDDQ

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
U143	POWER	POWER	5V			REG_VCC_U8350 74
U143	POWER	POWER	5V			REG_PVCC_U8350 74
Local Ground						
U143	GND	GND	0V			AGND_GPUVDDQ 74
GPU VDDQ						
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUVDDQ 74
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUVDDQ 74
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUVDDQ_RC 74
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUVDDQ 74
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUVDDQ 74
U142	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_OCSET 74
U142	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_VO 74
U144	VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE			SNS_GPUVDDQ_P 73 74
U144	VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE			SNS_GPUVDDQ_N 73 74
U143			SENSE			REG_GPUVDDQ_FB 74
U143			SENSE			REG_GPUVDDQ_RTN 74
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SREF 74
U143	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_FSEL 74
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET0 74
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET1 74
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET1_R 74
Output Bus						
U142	POWER	POWER	1.5V			PPVDDQ_S0_GPU 6

3.3V S5/5V S4

Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus					
U144 POWER	POWER	12V			REG_VIN_U7600 67
U120 POWER	POWER	5V			REG_VCC1_U7600 67
U120 POWER	POWER	5V			REG_VCC2_U7600 67
3.3V S5					
U144 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5 67
U144 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5 67
U144 VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC 67
U140 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5 67
U060 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P3V3S5 67
U062 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5 67
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN 67
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET 67
U141 VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET 67
U106 VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT 67
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R 67
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB 67
5V S3					
U113 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4 67
U113 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4 67
U113 VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC 67
U114 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4 67
U114 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P5VS4 67
U114 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4 67
U114 VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN 67
U114 VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET 67
U114 VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET 67
U116 VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT 67
U116 VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R 67
U116 VR_CTL_PHY	VR_CTL				REG_P5VS4_FB 67
Output Bus					
U116 POWER	POWER	5V			PP5V_S5 6
U116 POWER	POWER	5V			PP5V_S4 6
U114 POWER	POWER	3.3V			PP3V3_S5 6
FET Switched					
U42 POWER	POWER	5V			PP5V_S0 6
U42 POWER	POWER	3.3V			PP3V3_S4 6
U42 POWER	POWER	3.3V			PP3V3_S0 6
U44 POWER	POWER	3.3V			PP3V3_S0_SSD 6
U42 POWER	POWER	3.3V			PP3V3_ENET 6
U30 POWER	POWER	3.3V			PP3V3_TBTLC 6
Sensed					
U45 POWER	POWER	3.3V			PPSSD_S0 6

DDR3 Vref

Physical	Spacing	Voltage	DIDT	NO_TEST	
Memory Vref					
U130 POWER	POWER	3.3V			PP3V3_S4_VREFMRGN_DAC 32
U130 POWER	POWER	3.3V			PP3V3_S4_VREFMRGN_CTRL 32
U130 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_A_S3 6
U130 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_B_S3 6
U130 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_A_S3 6
U130 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_B_S3 6
U144 POWER_DDR	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_A 11 32
U144 POWER_DDR	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_B 11 32
U130 POWER_DDR	POWER_DDR	0.75V			CPU_DDR_VREF 11

3.42V G3H

Physical	Spacing	Voltage	DIDT	NO_TEST	
3.42V G3H					
U144 POWER	VR_SWITCH	12V			P3V42G3H_BOOST 69
U144 POWER	VR_SWITCH	12V			P3V42G3H_SW 69
U144 VR_CTL_PHY	VR_CTL				P3V42G3H_FB 69
U144 VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L 69
Output Bus					
U144 POWER	POWER	3.425V			PP3V42_G3H 6

1.8V S0

Physical	Spacing	Voltage	DIDT	NO_TEST	
1.8V S0					
U110 POWER	VR_SWITCH	5V			REG_PHASE_P1V8S0 68
U110 VR_CTL_PHY	VR_CTL				REG_P1V8S0_VFB 68
U110 VR_CTL_PHY	VR_CTL				REG_P1V8S0_SYNCH 68
Output Bus					
U110 POWER	POWER	1.8V			PP1V8_S0 6

HDD S0

Physical	Spacing	Voltage	DIDT	NO_TEST	
HDD S0					
U130 POWER	POWER	5V			PPHDD_S0 6

12V

Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus					
U144 POWER	POWER	12V			PP12V_ACDC 6
FET Switched					
U144 POWER	POWER	12V			PP12V_S5 6
U142 POWER	POWER	12V			PP12V_S0 6
Sensed					
U145 POWER	POWER	12V			PP12V_G3H 6
U145 POWER	POWER	12V			PP12V_S0_GPUCORE 6
U145 POWER	POWER	12V			PP12V_S0_GPUUNCORE 6

Ground/Common

Physical	Spacing	Voltage	DIDT	NO_TEST	
Common					
U130 GND	GND	0V			GND

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?
TBT_SPI	*	=2x_DIELECTRIC	?
TBTDP	*	=5x_DIELECTRIC	?
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

Electrical Contraint Set	Physical	Spacing		
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	34 77
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	34 77
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	34
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	34
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	34 71
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	34 71
DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	34
DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	34
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	34 77
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	34 77
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	34
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	34
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	34 71
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	34 71
DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	34
DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	34
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	82
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	82
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	82
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	82
DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	82
DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	82
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	82
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	82
	TBT_I2C_55S	TBT_I2C	=I2C_TBTRTR_SCL	34 47
	TBT_I2C_55S	TBT_I2C	=I2C_TBTRTR_SDA	34 47
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	34
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	34
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	34
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	34

*: Only used on hosts supporting T29 video-in

DisplayPort

Electrical Contraint Set	Physical	Spacing		
Graphics Source				
DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<1..0>	77 82
DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<1..0>	77 82
DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	77 82
DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	77 82
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_P	82
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_N	82
Internal Panel				
	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	82
	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	82
DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	81 82
DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	81 82
DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	81 82
DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	81 82
Internal DP SPDIF				
		HDA	DP_INT_SPDIF_AUDIO	52 81

TBT/DP Net Properties

Electrical Contraint Set	Physical	Spacing		
Port A				
TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1..0>	34 84
TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1..0>	34 84
	TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	84
	TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	84
DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	34 84
DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	34 84
DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	34 84
DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	34 84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	84
DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	84
DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	84
	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	84
	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	84
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	34 84
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	34 84
TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	34 84
TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	34 84
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	34 84
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	34 84
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	84
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	84
DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	84
DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	84
	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	84
	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	84
Port B				
TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1..0>	34 85
TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1..0>	34 85
	TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	85
	TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	85
DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	34 85
DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	34 85
DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	34 85
DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	34 85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	85
DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	85
DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	85
	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	85
	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	85
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	34 85
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	34 85
TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	34 85
TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	34 85
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	34 85
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	34 85
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	85
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	85
DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	85
DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	85
	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	85
	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	85

SYNC_MASTER=D7_NICK SYNC_DATE=12/13/2011

PAGE TITLE
TBT/DP Constraints

Apple Inc.

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GDDR5

GDDR5-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12 MM	=STANDARD	=STANDARD
GDDR_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	*	GDDR_45S
GDDR_ADBI_PHY	*	GDDR_45S
GDDR_CTRL_PHY	*	GDDR_45S
GDDR_CLK_PHY	*	GDDR_80D
GDDR_DQ_PHY	*	GDDR_45S
GDDR_EDC_PHY	*	GDDR_45S
GDDR_DBI_PHY	*	GDDR_45S
GDDR_WCK_PHY	*	GDDR_80D

Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

	Trace-to-Trace				Isolation				
Table	Micro	Design	Strip	Design	Micro	Design	Strip	Design	Comments
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Memory address (MA). Implented 4.5 Gbps or less rules for K70.
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Address dynamic bus inversion (ADBI)
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Control (CTRL)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Clock (CLK)
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data (DQ)
5-6/5-7	7:1	7:1	7:1	7:1	7:1	7:1	7:1	7:1	Error detection pins (EDC). Using larger isolation rules,
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data dynamic bus inversion (DBI)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Forwarded clock (WCK)

GDDR5-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=5x_DIELECTRIC	?
GDDR_ISO	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR_MA2MA	*	=2x_DIELECTRIC	?
GDDR_MA2MA	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_ADBI2ADBI	*	=2x_DIELECTRIC	?
GDDR_ADBI2ADBI	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	*	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CLK2CLK	*	=5x_DIELECTRIC	?
GDDR_CLK2CLK	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_DQ2DQ	*	=3x_DIELECTRIC	?
GDDR_DQ2DQ	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_EDC_ISO	*	=7x_DIELECTRIC	?
GDDR_EDC_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?
GDDR_EDC2EDC	*	=7x_DIELECTRIC	?
GDDR_EDC2EDC	TOP,BOTTOM	=7x_DIELECTRIC	?
GDDR_DBI2DBI	*	=3x_DIELECTRIC	?
GDDR_DBI2DBI	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_WCK2WCK	*	=5x_DIELECTRIC	?
GDDR_WCK2WCK	TOP,BOTTOM	=5x_DIELECTRIC	?

Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_MA	*	*	GDDR_ISO
GDDR_*_*_MA	=SAME	*	GDDR_MA2MA

Data: DQxy[31:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DQ	*	*	GDDR_ISO
GDDR_*_*_DQ	=SAME	*	GDDR_DQ2DQ

Address Dynamic Bus Inversion: ADBIxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_ADBI	*	*	GDDR_ISO
GDDR_*_*_ADBI	=SAME	*	GDDR_ADBI2ADBI

Error Detection: EDCxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_EDC	*	*	GDDR_EDC_ISO
GDDR_*_*_EDC	=SAME	*	GDDR_EDC2EDC

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	=SAME	*	GDDR_CTRL2CTRL

Data Dynamic Bus Inversion: DDBIxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DBI	*	*	GDDR_ISO
GDDR_*_*_DBI	=SAME	*	GDDR_DBI2DBI

Clock: CKxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_CLK	*	*	GDDR_ISO
GDDR_*_*_CLK	=SAME	*	GDDR_CLK2CLK

Forwarded Clock: WCKxy[1:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_WCK	*	*	GDDR_ISO
GDDR_*_*_WCK	=SAME	*	GDDR_WCK2WCK

GDDR5 Frame Buffer A

Electrical Contraint Set	Physical	Spacing		
Memory Address				
164C GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<8..0>	73 75
164E GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<8..0>	73 75
Address Dynamic Bus Inv				
164A GDDR_A0_ADBI	GDDR_ADBI_PHY	GDDR_A_0_ADBI	FB_A0_ABI_L	73 75
164B GDDR_A1_ADBI	GDDR_ADBI_PHY	GDDR_A_1_ADBI	FB_A1_ABI_L	73 75
Control				
164F GDDR_A0_CKE	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CKE_L	73 75
1648 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CS_L	73 75
1649 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_WE_L	73 75
1650 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CAS_L	73 75
1651 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_RAS_L	73 75
1652 GDDR_A1_CKE	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CKE_L	73 75
1654 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CS_L	73 75
1653 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_WE_L	73 75
1655 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CAS_L	73 75
1656 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_RAS_L	73 75
Clock				
165F GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_P	73 75
1658 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_N	73 75
1660 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_P	73 75
1659 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_N	73 75
Data				
1665 GDDR_A0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<7..0>	73 75
1666 GDDR_A0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<15..8>	73 75
1662 GDDR_A0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<23..16>	73 75
1663 GDDR_A0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<31..24>	73 75
1664 GDDR_A1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<7..0>	73 75
1668 GDDR_A1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<15..8>	73 75
1667 GDDR_A1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<23..16>	73 75
1661 GDDR_A1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<31..24>	73 75
Error Detection				
167C GDDR_A0_EDC0	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<0>	73 75
166C GDDR_A0_EDC1	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<1>	73 75
167A GDDR_A0_EDC2	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<2>	73 75
167E GDDR_A0_EDC3	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<3>	73 75
167D GDDR_A1_EDC0	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<0>	73 75
167F GDDR_A1_EDC1	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<1>	73 75
167B GDDR_A1_EDC2	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<2>	73 75
1679 GDDR_A1_EDC3	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<3>	73 75
Data Dynamic Bus Inv				
167A GDDR_A0_DBI0	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<0>	73 75
167C GDDR_A0_DBI1	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<1>	73 75
168D GDDR_A0_DBI2	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<2>	73 75
167E GDDR_A0_DBI3	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<3>	73 75
168A GDDR_A1_DBI0	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<0>	73 75
168C GDDR_A1_DBI1	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<1>	73 75
168B GDDR_A1_DBI2	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<2>	73 75
168E GDDR_A1_DBI3	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<3>	73 75
Forwarded Clock				
168B GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<0>	73 75
168F GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<0>	73 75
168D GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<1>	73 75
168E GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<1>	73 75
168A GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<0>	73 75
1694 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<0>	73 75
1692 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<1>	73 75
1691 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<1>	73 75

GDDR5 Frame Buffer B

Electrical Contraint Set	Physical	Spacing		
Memory Address				
169D GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<8..0>	73 76
169E GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<8..0>	73 76
Address Dynamic Bus Inv				
169B GDDR_B0_ADBI	GDDR_ADBI_PHY	GDDR_B_0_ADBI	FB_B0_ABI_L	73 76
169F GDDR_B1_ADBI	GDDR_ADBI_PHY	GDDR_B_1_ADBI	FB_B1_ABI_L	73 76
Control				
16B0 GDDR_B0_CKE	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CKE_L	73 76
16A9 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CS_L	73 76
16AB GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_WE_L	73 76
16AC GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CAS_L	73 76
16AD GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_RAS_L	73 76
16AE GDDR_B1_CKE	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CKE_L	73 76
16B6 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CS_L	73 76
16B5 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_WE_L	73 76
16B4 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CAS_L	73 76
16B7 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_RAS_L	73 76
Clock				
16B9 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_P	73 76
16A8 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_N	73 76
16A6 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_P	73 76
16A7 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_N	73 76
Data				
16A1 GDDR_B0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<7..0>	73 76
16A2 GDDR_B0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<15..8>	73 76
16A3 GDDR_B0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<23..16>	73 76
16A5 GDDR_B0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<31..24>	73 76
16AA GDDR_B1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<7..0>	73 76
16AF GDDR_B1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<15..8>	73 76
16B3 GDDR_B1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<23..16>	73 76
16B1 GDDR_B1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<31..24>	73 76
Error Detection				
16C0 GDDR_B0_EDC0	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<0>	73 76
16C3 GDDR_B0_EDC1	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<1>	73 76
16C2 GDDR_B0_EDC2	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<2>	73 76
16C1 GDDR_B0_EDC3	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<3>	73 76
16C8 GDDR_B1_EDC0	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<0>	73 76
16C4 GDDR_B1_EDC1	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<1>	73 76
16C6 GDDR_B1_EDC2	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<2>	73 76
16C7 GDDR_B1_EDC3	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<3>	73 76
Data Dynamic Bus Inv				
16C9 GDDR_B0_DBI0	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<0>	73 76
16CB GDDR_B0_DBI1	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<1>	73 76
16CD GDDR_B0_DBI2	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<2>	73 76
16CF GDDR_B0_DBI3	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<3>	73 76
16D3 GDDR_B1_DBI0	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<0>	73 76
16D5 GDDR_B1_DBI1	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<1>	73 76
16D7 GDDR_B1_DBI2	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<2>	73 76
16D9 GDDR_B1_DBI3	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<3>	73 76
Forwarded Clock				
16D0 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<0>	73 76
16D2 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<0>	73 76
16D3 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<1>	73 76
16D4 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<1>	73 76
16D6 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<0>	73 76
16F3 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<0>	73 76
16F4 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<1>	73 76
16F2 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<1>	73 76

GPU Misc.

Electrical Contraint Set	Physical	Spacing		
SMB				
15EE	SMB_PHY	SMB	GPU_SMB_CLK	77 78
15E9	SMB_PHY	SMB	GPU_SMB_DAT	77 78
15E7	SMB_PHY	SMB	GPU_SMB_CLK_R	47 78
15E5	SMB_PHY	SMB	GPU_SMB_DAT_R	47 78

Frame Buffer Reset

Electrical Contraint Set	Physical	Spacing		
Reset				
1F44 GDDR_A0_RESET	GDDR_50S	GDDR_CTRL	FB_A0_RESET_L	73 75
1F45 GDDR_A1_RESET	GDDR_50S	GDDR_CTRL	FB_A1_RESET_L	73 75
1F46 GDDR_B0_RESET	GDDR_50S	GDDR_CTRL	FB_B0_RESET_L	73 76
1F65 GDDR_B1_RESET	GDDR_50S	GDDR_CTRL	FB_B1_RESET_L	73 76

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions
BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	0.45mm	1000

Constraints
BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_CTL	*	BLC_CTL_ISO
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

Is it chel'oh or sel'oh?

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H745	POWER	POWER	12V			PP12V_S0_BKLT_FUSED 86
H746	POWER	POWER	12V			PP12V_S0_BKLT_FILT 86
H747	POWER	POWER	12V			PP12V_S0_BKLT_PWR 86
H748	POWER	POWER	12V			PP12V_S0_BKLT_PWR_R 86
H749	POWER	POWER	5V			PP5V_S0_BKLT_R 86
H750	POWER	POWER	3.3V			PP3V3_S0_BKLT_VDDIO_R 86
Local Ground						
H751	BLC_CTL_PHY	BLC_PHASE	0V			PGND_BKLT 86
H752	BLC_CTL_PHY	BLC_PHASE	0V			DGND_BKLT 86
H886	BLC_CTL_PHY	BLC_PHASE	0V			LGND_BKLT 86
Backlight						
H753	POWER_BLC	BLC_PHASE	80V	TRUE		BKLT_PHASE 86
H754	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE 86
H755	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE_R 86
H756	BLC_CTL_PHY	BLC_PHASE	80V	TRUE	TRUE	BKLT_SNUBBER 86
H757	BLC_CTL_PHY	BLC_PHASE	12V	TRUE		BKLT_SW_R 86
H758	BLC_CTL_PHY	BLC_CTL				BKLT_ISET 86
H759	BLC_CTL_PHY	BLC_CTL				BKLT_FLT 86
H760	BLC_CTL_PHY	BLC_CTL				BKLT_FLT_RC 86
H761	SNS_DTEF_PHY	SENSE				BKLT_SW_P 86
H762	SNS_DTEF_PHY	SENSE				BKLT_SW_N 86
H763		SENSE				BKLT_FB 86
H884		BLC_HV	67V			BKLT_FB_XW 86
H764		BLC_HV	67V			BKLT_FB_R 86
H770	POWER_BLC_RET	BLC_CTL				BKLT_ISEN1 86
H771	POWER_BLC_RET	BLC_CTL				BKLT_ISEN2 86
H772	POWER_BLC_RET	BLC_CTL				BKLT_ISEN3 86
H773	POWER_BLC_RET	BLC_CTL				BKLT_ISEN4 86
H774	POWER_BLC_RET	BLC_CTL				BKLT_ISEN5 86
H775	POWER_BLC_RET	BLC_CTL				BKLT_ISEN6 86
H765	POWER_BLC_RET	BLC_HV				BKLT_ISEN1_R 86
H766	POWER_BLC_RET	BLC_HV				BKLT_ISEN2_R 86
H767	POWER_BLC_RET	BLC_HV				BKLT_ISEN3_R 86
H768	POWER_BLC_RET	BLC_HV				BKLT_ISEN4_R 86
H769	POWER_BLC_RET	BLC_HV				BKLT_ISEN5_R 86
H776	POWER_BLC_RET	BLC_HV				BKLT_ISEN6_R 86
H780	POWER_BLC_RET	BLC_HV				LED_RETURN_1 86
H781	POWER_BLC_RET	BLC_HV				LED_RETURN_2 86
H782	POWER_BLC_RET	BLC_HV				LED_RETURN_3 86
H783	POWER_BLC_RET	BLC_HV				LED_RETURN_4 86
H784	POWER_BLC_RET	BLC_HV				LED_RETURN_5 86
H785	POWER_BLC_RET	BLC_HV				LED_RETURN_6 86
Output Bus						
H779	POWER_BLC	BLC_HV	67V			BKLT_BOOST 86
H777	POWER_BLC	BLC_HV	67V			BKLT_BOOST_1 86
H778	POWER_BLC	BLC_HV	67V			BKLT_BOOST_2 86

Cello Miscellaneous

Electrical Contraint Set	Physical	Spacing	
SPI			
H666	SMB_PHY	SMB	BKLT_SCL 86
H665	SMB_PHY	SMB	BKLT_SDA 86

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