F6Ve SCHEMATIC Revision 1.0

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92	92_POWER_PROTECT
93	93_POWER_SIGNAL
94	94_POWER_FLOWCHART

<Variant Name>

ASUSTeK COMPUTER INC

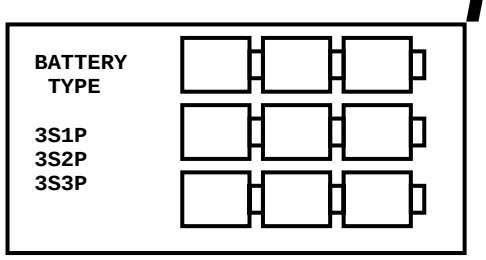
Title : PAGE REF.

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 1 of 64

F6Ve BLOCK DIAGRAM



Internal IO CON with Cable for MB

TP&F/P CON | MDC CON | BT CON | LVDS , inverter and CCD CON

Internal IO CON with Cable for IO Board

SPEAKER | INT. MIC CON

THERMAL SENSOR(G781-1)/ FOR VGA. page41

DDR2 32Mx16 x4
DDR2 32M*16-2 1.8V
Qimonda/Hynix page43

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FSB 1066MHz

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DDR2 SDRAM 667/800MHz

DDR2 667/800 SODIMM X2 +1.8V +0.9VS page14,15 — DDR2 CAP/RES

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MINI CARD WLAN page20

Azalia ALC662

AUDIO AMP TPA6017A2PWP

HP

MIC_IN

USB x1

MINI CARD 3G/UWB Co-lay

SIM CON

RJ11,RJ45 CON

IO Board

<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 2 of 64

ICH9-M GPIO

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PMSYNC#(programmed as GPO)	+3VS
GPIO 01	-	DOCKING_DET# EXT PU @	+3VS
GPIO [2:5]	GPI/OD	PCI_INT[E:H]# EXT PU	+3VS
GPIO 06	-	UNDOCKING_BTN# EXT PU @	+3VS
GPIO 07	-	IDE_BAY_IN# EXT PU @	+3VS
GPIO 08	-	EXT_SMI# EXT PU	+3VSUS
GPIO 09	-	WOL_EN EXT PU/PD @	+3VSUS
GPIO 10	GPI	RTLAN_DSM# EXT PU	+3VSUS
GPIO 11	Native	EXT_SCI#(Programmed as GPI	+3VSUS
GPIO 12	-	HDTV_DET# EXT PU @	+3VSUS
GPIO 13	-	CB_SD# (TP)	+3VSUS
GPIO 14	-	AC_PRESENT EXT PU	+3VSUS
GPIO 15(DT)	Native	STP_PCI#(PU to +3VS)	+3VSUS
GPIO 16	Native	PM_DPRSLPVR INT PD	+3VS
GPIO 17	GPO	WLAN_LED EXT PD	+3VS
GPIO 18	-	-	+3VS
GPIO 19	GPI	- EXT PU	+3VS
GPIO 20	GPO	UWB_ON INT PD	+3VS
GPIO 21	GPI	- EXT PU	+3VS
GPIO 22	-	BT_DET# EXT PU @	+3VS
GPIO 23	Native	ICH_LDRQ1# INT PU	+3VS
GPIO 24	-	-	+3VSUS
GPIO 25(DT)	Native	STP_CPU#(PU to +3VS)	+3VSUS
GPIO 26	-	-	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	BT_LED	+3VSUS
GPIO 29	Native	USB_OC#5	+3VSUS
GPIO 30	Native	USB_OC#6	+3VSUS
GPIO 31	Native	USB_OC#7	+3VSUS
GPIO 32(DT)	Native	PM_CLKRUN#	+3VS
GPIO 33	-	- INT PU	+3VS
GPIO 34	-	-	+3VS
GPIO 35	-	SATACLKREQ# EXT PU @	+3VS
GPIO 36	GPI	- EXT PU	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC1#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	+3VSUS
GPIO 45	Native	USB_OC9#	+3VSUS
GPIO 46	GPO	USB_OC10#/WLAN_ON	+3VSUS
GPIO 47	Native	USB_OC11#	+3VSUS
GPIO 48	GPI	EMAIL_LED EXT PD @	+3VS
GPIO 49	-	- INT PU	+3VS
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU	+3VS
GPIO 56	-	- EXT PU	+3VSUS
GPIO 57	GPI	MEM_ID1 EXT PU @	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	GPO	RTLAN_DSM_EN/LINKALERT# EXT PU	+3VSUS

GPIO33 Internal Pull High, Go Low= Flash Descriptor Security will be overriden

EC IT8512

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED#	
GPA1	GPO	CHG_LED#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	-	-	
GPA7	-	-	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	-	-	
GPB3	ALT	SMB0_CLK Battery	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	-	-	
GPC1	ALT	SMB1_CLK ThermalSensor	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	GPI	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	GPI	BAT1_IN_OC#	
GPC7	GPI	RFON_SW#	
GPD0	GPI	PWRLIMIT#	
GPD1	GPI	PM_SUSC#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	GPI	FAN0_TACH	
GPD7	GPO	SD_CD#_EC	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	GPI	PWR_SW#	
GPE5	-	-	
GPE6	GPI	LID_SW#	
GPE7	-	-	
GPF0	-	-	
GPF1	-	-	
GPF2	GPI	MARATHON#	
GPF3	-	-	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	-	-	
GPG0	GPO	PM_THERM#_EC	
GPG1	GPI	PM_SUSB#	
GPG2	-	-	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	-	-	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	GPO	3G_ON#	
GPH2	-	-	
GPH3	GPO	BAT_LEARN	
GPH4	-	-	
GPH5	-	-	
GPH6	GPO/OD	CAP_LED#	
-	-	-	
GPI0	GPI	VGA_ALERT#	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	PWR_MON	
GPI5	-	-	
GPI6	GPI	KB_ID0(NC)	
GPI7	GPI	KB_ID1(NC)	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	-	
GPJ3	GPO	BATSEL_2P#	
GPJ4	-	-	
GPJ5	-	-	
GPK0	-	-	
GPK1	-	-	
GPK2	-	-	
GPK3	-	-	
GPK4	-	-	
GPK5	-	-	
GPL0	-	-	
GPL1	-	-	
GPL2	-	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	-	-	
GPL6	-	-	
GPL7	-	-	
GPK6	-	-	
GPK7	-	-	

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(G780)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

PCIE 1	
PCIE 2	WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	UWB(TBD)
PCIE 6	LAN

SATA 0	SATA HDD
SATA1	SATA ODD
SATA4	
SATA5	ESATA

USB 0	USB Conn
USB 1	
USB 2	USB Conn
USB 3	USB Conn
USB 4	CMOS Camera
USB 5	CardReader
USB 6	UWB(TBD)
USB 7	WiMax
USB 8	NewCard
USB 9	3G Card
USB 10	Bluetooth
USB 11	FINGER PRINT

<Variant Name>

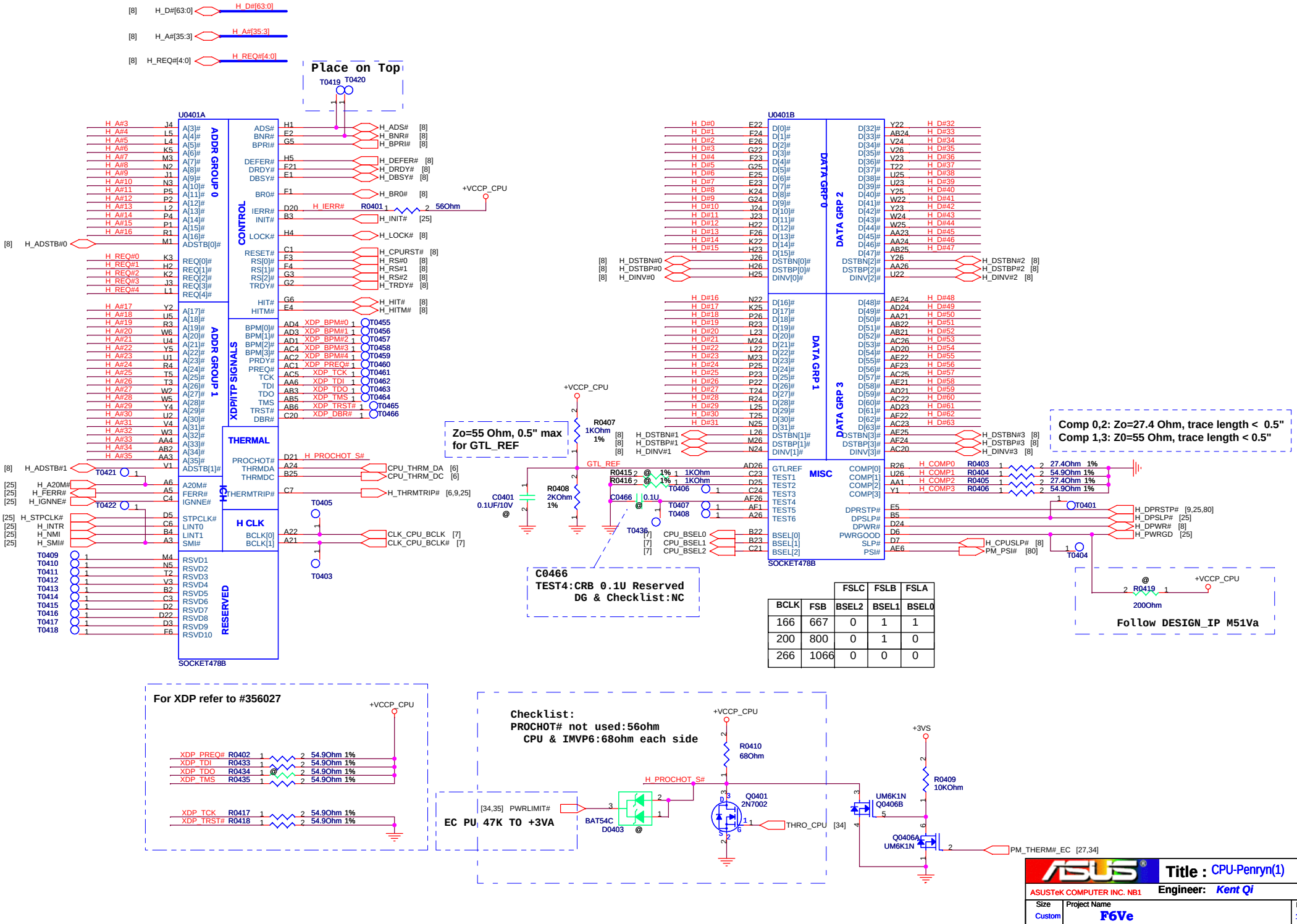
ASUSTeK COMPUTER INC

Title : Schematic Info.

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 3 of 64


[8] H_D#[63:0]
H_D#[63:0]
[8] H_A#[35:3]
H_A#[35:3]
[8] H_REQ#[4:0]
H_REQ#[4:0]
Place on Top
T0419 T0420
U0401A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
SOCKET478B
ADS# BNR# BPRI#
DEFER# DRDY# DBSY#
BR0#
IERR# INIT#
LOCK#
RESET# RS[0]# RS[1]# RS[2]# TRDY#
HIT# HITM#
BPM[0]# BPM[1]# BPM[2]# BPM[3]# PRDY# PREQ# TCK TDI TDO TMS TRST# DBR#
PROCHOT# THRMDA THRMDC
THERMTRIP#
BCLK[0] BCLK[1]
A20M# FERR# IGNNE#
STPCLK# LINT0 LINT1 SMI#
H_ADS# H_BNR# H_BPRI#
H_DEFER# H_DRDY# H_DBSY#
H_BR0#
H_IERR# R0401 56Ohm
H_INIT# [25]
H_LOCK#
H_CPURST#
H_RS#0 H_RS#1 H_RS#2 H_TRDY#
H_HIT# H_HITM#
XDP_BPM#0 XDP_BPM#1 XDP_BPM#2 XDP_BPM#3 XDP_BPM#4 XDP_PREQ# XDP_TCK XDP_TDI XDP_TDO XDP_TMS XDP_TRST# XDP_DBR#
T0455 T0456 T0457 T0458 T0459 T0460 T0461 T0462 T0463 T0464 T0465 T0466
H_PROCHOT_S#
CPU_THRM_DA [6]
CPU_THRM_DC [6]
H_THRMTRIP# [6,9,25]
CLK_CPU_BCLK [7]
CLK_CPU_BCLK# [7]
T0405 T0403
+VCCP_CPU
H_ADSTB#0 H_ADSTB#1
T0421 T0422
H_A20M# H_FERR# H_IGNNE#
H_STPCLK# H_INTR H_NMI H_SMI#
T0409 T0410 T0411 T0412 T0413 T0414 T0415 T0416 T0417 T0418
U0401B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
SOCKET478B
H_DSTBN#0 H_DSTBP#0 H_DINV#0
H_DSTBN#2 H_DSTBP#2 H_DINV#2
H_DSTBN#1 H_DSTBP#1 H_DINV#1
H_DSTBN#3 H_DSTBP#3 H_DINV#3
GTLREF TEST1 TEST2 TEST3 TEST4 TEST5 TEST6
BSEL[0] BSEL[1] BSEL[2]
CPU_BSEL0 CPU_BSEL1 CPU_BSEL2
COMP[0] COMP[1] COMP[2] COMP[3]
DPRSTP# DPSLP# DPWR# PWRGOOD SLP# PSI#
H_CPUSLP# [8]
PM_PSI# [80]
H_COMP0 H_COMP1 H_COMP2 H_COMP3
R0403 R0404 R0405 R0406 27.4Ohm 1%
H_DPRSTP# [9,25,80]
H_DPSLP# [25]
H_DPWR# [8]
H_PWRGD [25]
T0401 T0404
R0407 1KOhm 1%
R0408 2KOhm 1%
C0401 0.1UF/10V
R0415 R0416 1KOhm
C0466 0.1U
T0406 T0407 T0408 T0436
GTL_REF
Zo=55 Ohm, 0.5" max for GTL_REF
Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"
C0466
TEST4:CRB 0.1U Reserved
DG & Checklist:NC
R0419 200Ohm
Follow DESIGN_IP M51Va
FSLC FSLB FSLA
BCLK FSB BSEL2 BSEL1 BSEL0
166 667 0 1 1
200 800 0 1 0
266 1066 0 0 0
For XDP refer to #356027
XDP_PREQ# R0402
XDP_TDI R0433
XDP_TDO R0434
XDP_TMS R0435
XDP_TCK R0417
XDP_TRST# R0418
54.9Ohm 1%
Checklist:
PROCHOT# not used:56ohm
CPU & IMVP6:68ohm each side
R0410 68Ohm
H_PROCHOT_S#
[34,35] PWRLIMIT#
EC PU 47K TO +3VA
BAT54C D0403
Q0401 2N7002
THRO_CPU [34]
+3VS
R0409 10KOhm
UM6K1N Q0406B
Q0406A UM6K1N
PM_THERM#_EC [27,34]
Title : CPU-Penryn(1)
ASUSTeK COMPUTER INC. NB1
Engineer: Kent Qi
Size Custom
Project Name F6Ve
Rev 1.0
Date: Friday, September 26, 2008
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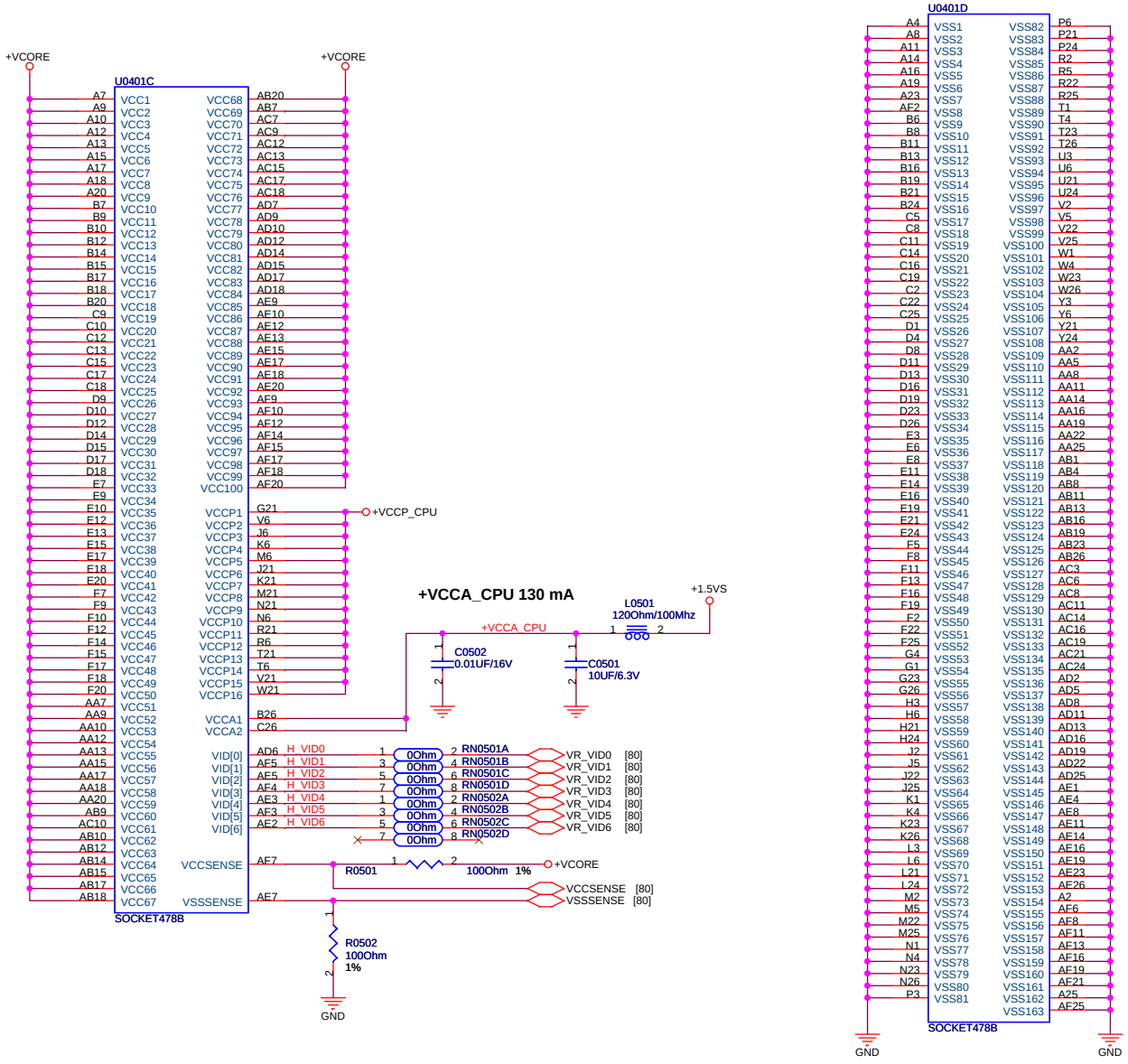


ASUSTeK COMPUTER INC. NB1	Title : CPU-Penryn(2)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 5 of 64	

Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

Cap Follow DesignIP
22U/6.3V 0805_55:11G235222625320

47A for PENRYN

+VCORE

C0614 10UF/6.3V, C0632 10UF/6.3V, C0621 10UF/6.3V, C0603 10UF/6.3V @, C0625 10UF/6.3V, C0609 10UF/6.3V @, C0631 10UF/6.3V, C0604 10UF/6.3V @, C0622 10UF/6.3V, C0629 10UF/6.3V

C0627 10UF/6.3V @, C0620 10UF/6.3V @, C0626 10UF/6.3V @, C0607 10UF/6.3V, C0624 10UF/6.3V @, C0605 10UF/6.3V, C0623 10UF/6.3V, C0601 10UF/6.3V, C0615 10UF/6.3V, C0602 10UF/6.3V

C0616 10UF/6.3V @, C0639 10UF/6.3V, C0619 10UF/6.3V @, C0610 10UF/6.3V, C0613 10UF/6.3V, C0608 10UF/6.3V @, C0612 10UF/6.3V @, C0617 10UF/6.3V, C0628 10UF/6.3V, C0630 10UF/6.3V

C0611 10UF/6.3V, C0633 10UF/6.3V @

GND

Decoupling guide from INTEL

VCORE	22uF/	* 36pcs
	330uF	* 4pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

+VCCP Decoupling Capacitor (Place near CPU)

+VCCP — JP0601 2MM_OPEN_5MIL @ — +VCCP_CPU

CE0601 100UF/2.5V, C0618 0.1UF/10V X7R, C0606 0.1UF/10V X7R, C0636 0.1UF/10V X7R X7R, C0635 0.1UF/10V X7R, C0638 0.1UF/10V, C0637 0.1UF/10V X7R

GND

Thermal Sensor

Close to Pin A24
& A25 of CPU

+3VS, +3VS_THM

THRM_ALERT# CPU — R0650 10KOhm — +3VS

CPU_THRM_DA — C0651 1000P

CPU_THRM_DC — C0652 0.1U

33Ohm R0602 — +3VS

U0650 G780P11U

[4] CPU_THRM_DA	1 VCC	8 SMBCLK	SMB1_CLK → SMB1_CLK [34,41]
[4] CPU_THRM_DC	2 DXP	7 SMBDATA	SMB1_DAT → SMB1_DAT [34,41]
	3 DXN	6 ALERT#	THRM_ALERT# CPU → T0601
[34] OS#_OC	4 THERM#	5 GND	GND

Slave address: 98h

Enable: Turn OFF system To EC(Internal Pull Hi)

+VCCP — R0606 56Ohm

+VCCP — R0652 330 — C0650 0.1U @ — GND

[4,9,25] H_THRMTRIP# — Q0650 PMBS3904 — Q0651 2N7002 — THRMTRIP# [34] — To EC

[22,26,29,33,34,38] BUF_PLT_RST#

+5VS_FAN — R0605 0Ohm — +5VSFAN

C0671 0.1U — GND

C0672 10uF/10V — GND

D0601 1SS355 @ — GND

+3VS — R0603 10KOhm @ — +5VS_FAN

2N7002 Q0611 @

[34] FAN0_PWM

0Ohm R0653

C0654 100PF/50V @ — GND

+3VS — R0659 10KOhm

[34] FAN0_TACH

C0653 100PF/50V @ — GND

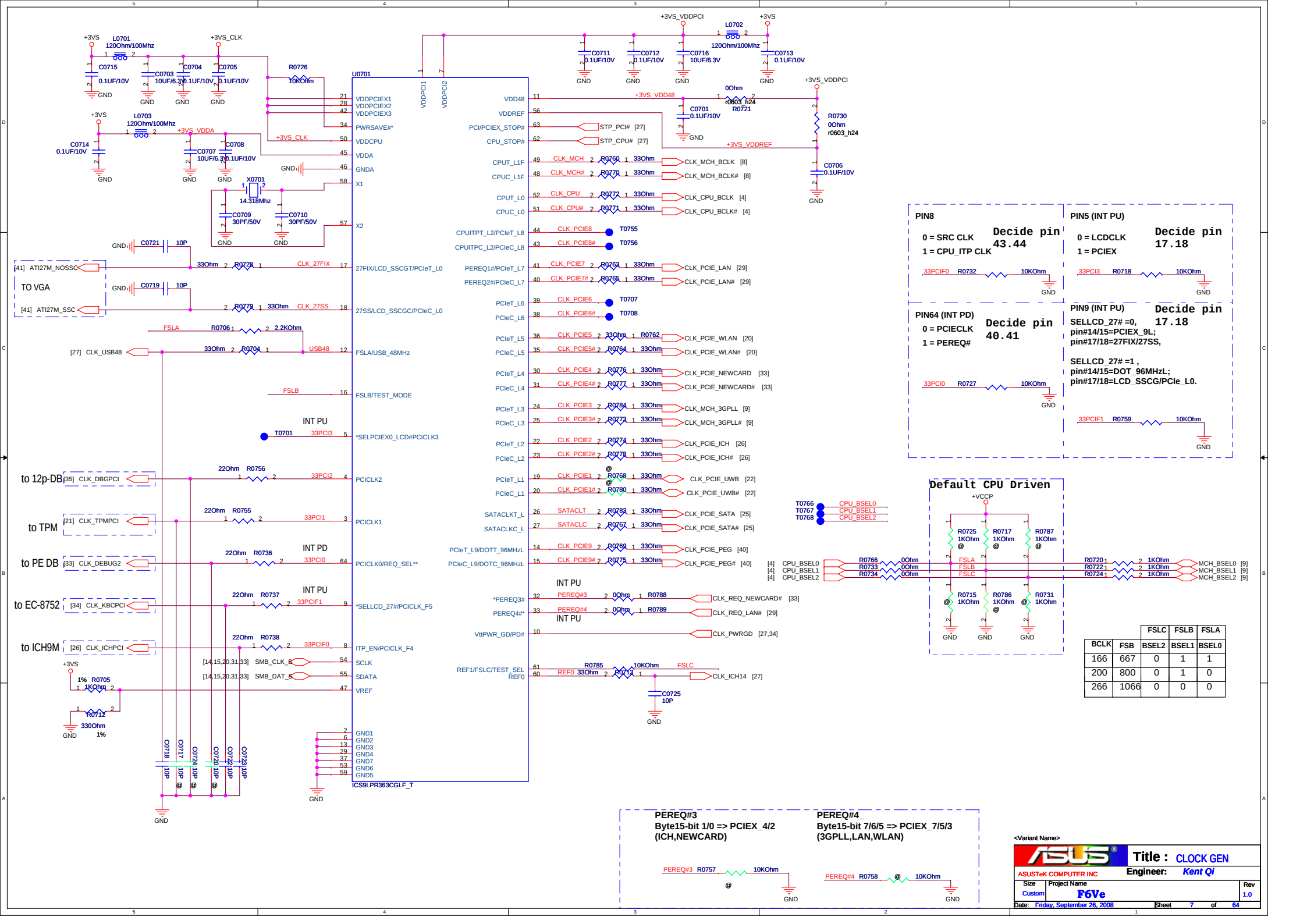
+5VS_FAN — D0603 BAT54C @

+5VSFAN — CON601 P/N:12G17100004B — WtoB_CON_4P_1

Open-collect

GND

ASUSTeK COMPUTER INC. NB1	Title : CAP,Thermal FAN	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 6 of 64	



BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

<Variant Name>

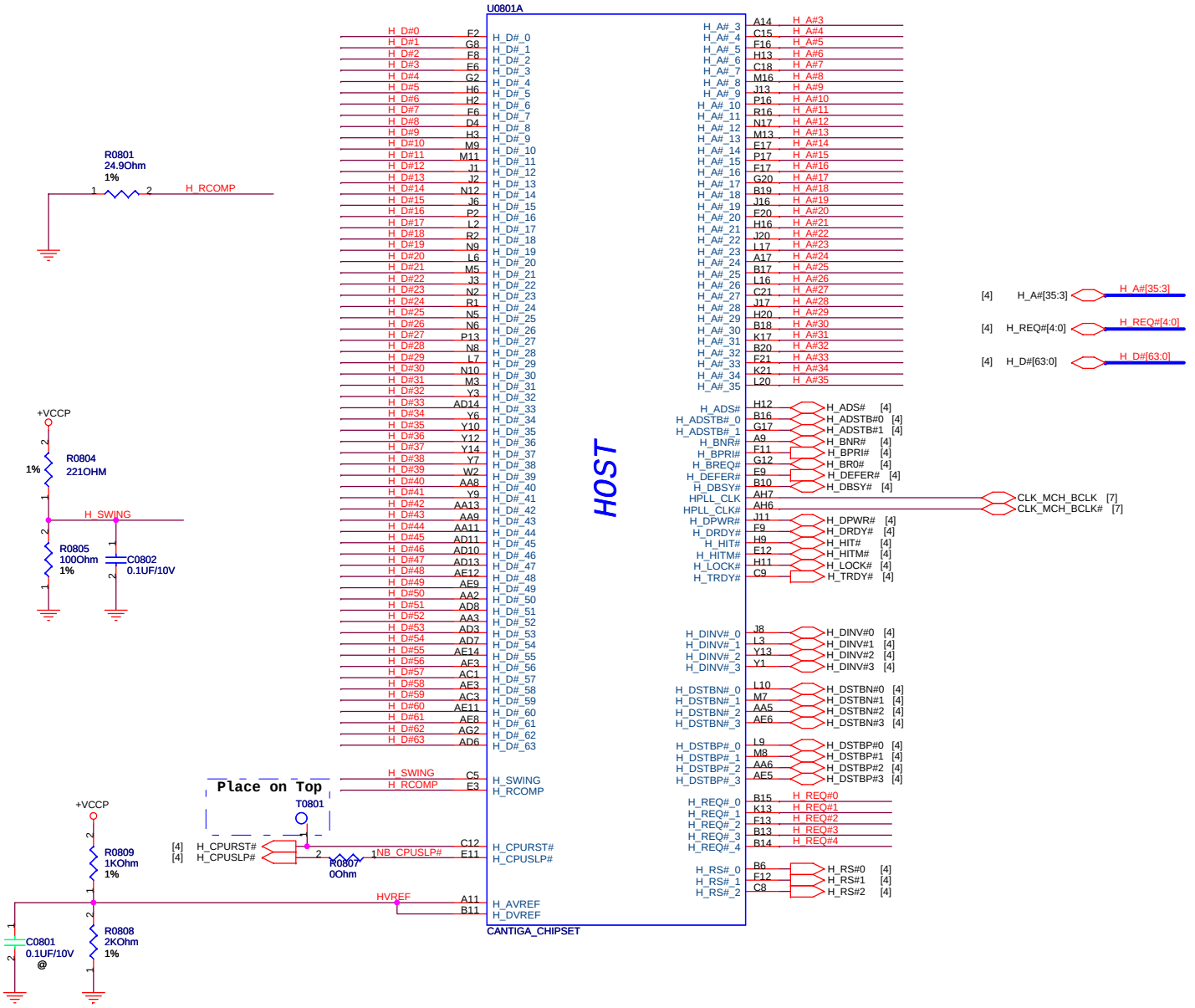
Title : CLOCK GEN

ASUSTeK COMPUTER INC

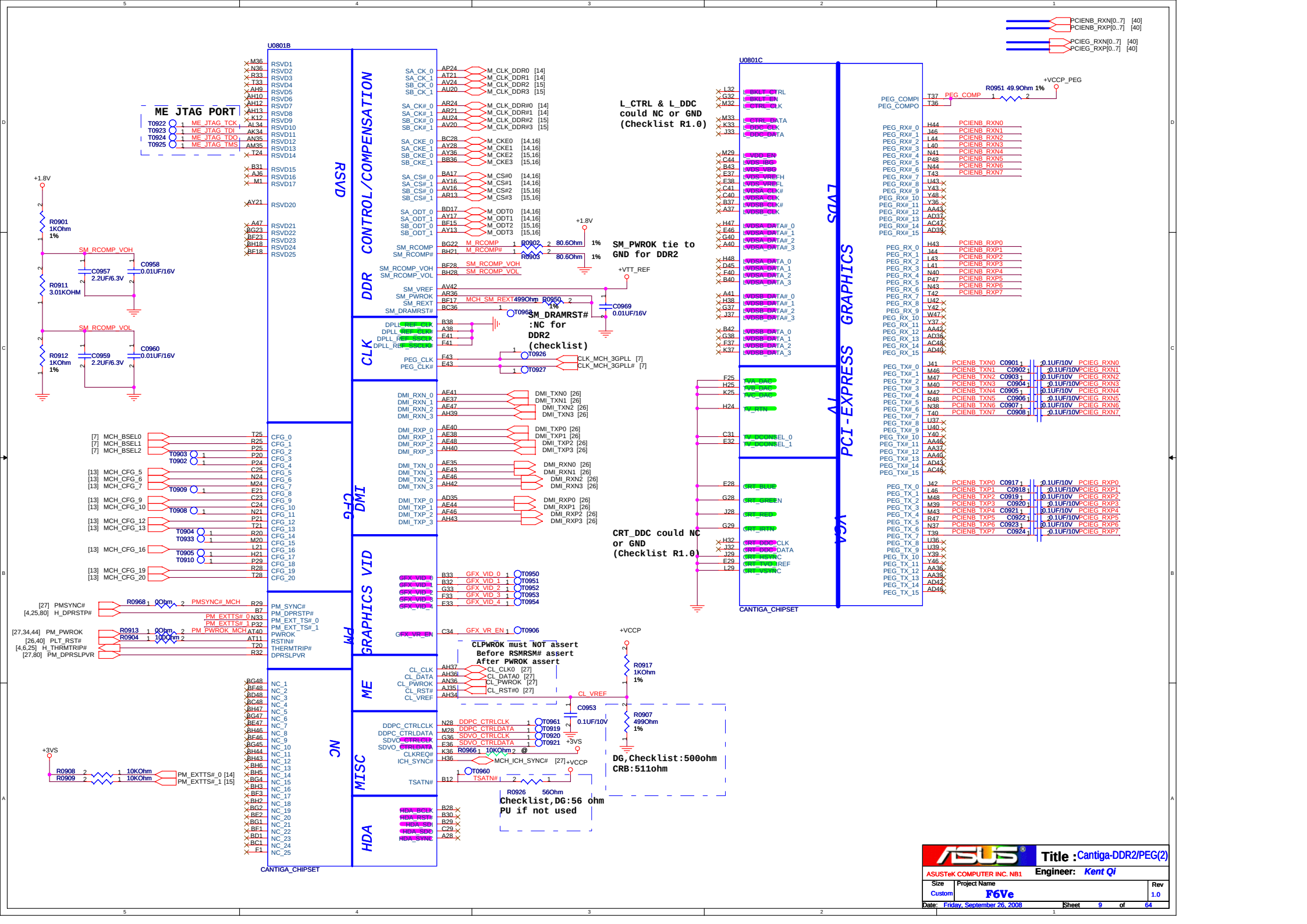
Engineer: Kent Qi

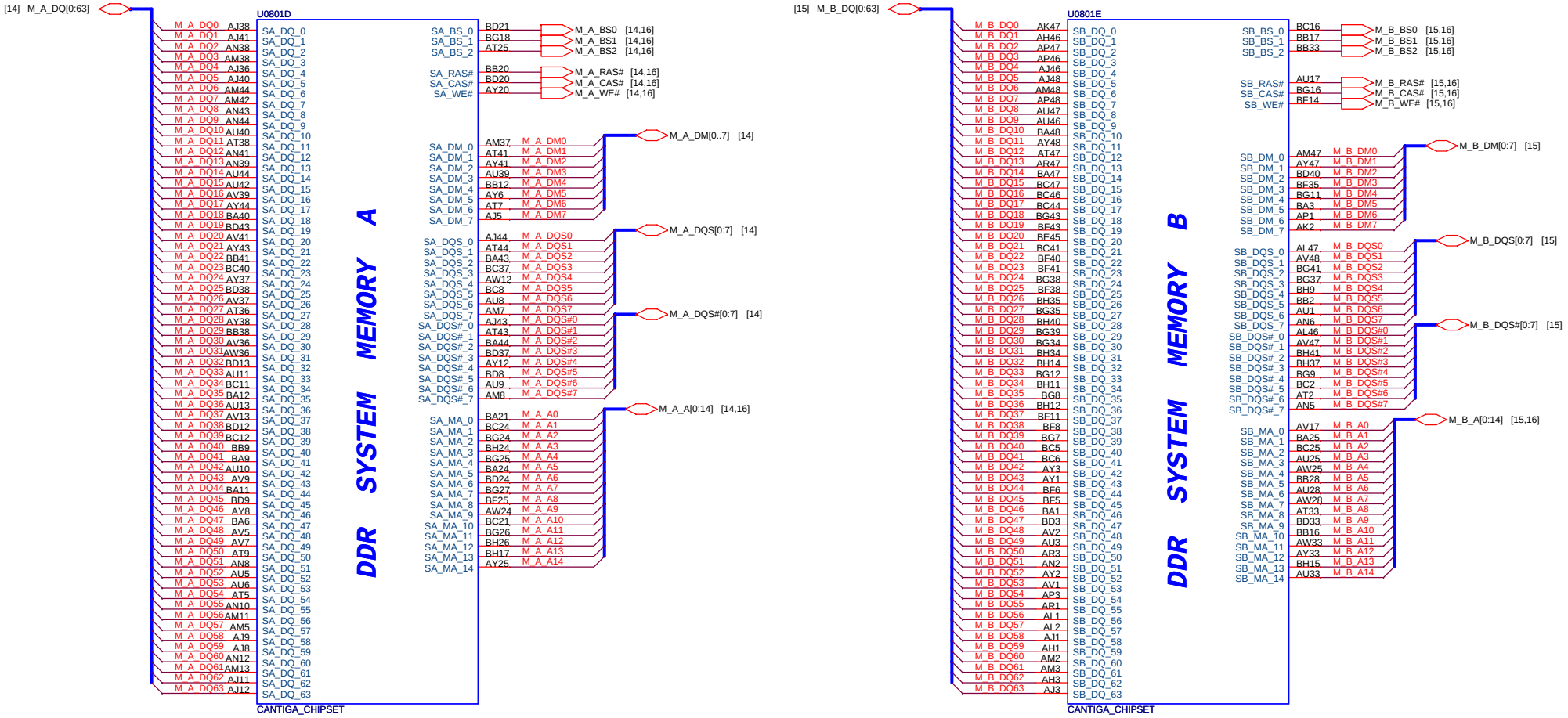
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 7 of 64



ASUSTeK COMPUTER INC. NB1	Title : Cantiga -- CPU (1)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 8 of 64	


U0801B
U0801C
CANTIGA_CHIPSET
ME JTAG PORT
T0922 ME_JTAG_TCK
T0923 ME_JTAG_TDI
T0924 ME_JTAG_TDO
T0925 ME_JTAG_TMS
RSVD
DDR CONTROL/COMPENSATION
CLK
DMI
GRAPHICS VID
PWR
ME
MISC
HDA
NC
LVDS
PCI-EXPRESS GRAPHICS
VGA
L_CTRL & L_DDC could NC or GND (Checklist R1.0)
SM_PWROK tie to GND for DDR2
SM_DRAMRST# :NC for DDR2 (checklist)
CRT_DDC could NC or GND (Checklist R1.0)
CLPWROK must NOT assert Before RSMRSM# assert After PWROK assert
DG,Checklist:500ohm CRB:511ohm
Checklist,DG:56 ohm PU if not used
PCIENB_RXN[0..7] [40]
PCIENB_RXP[0..7] [40]
PCIEG_RXN[0..7] [40]
PCIEG_RXP[0..7] [40]
+VCCP_PEG
R0951 49.9Ohm 1%
PEG_COMP
PEG_COMPI
PEG_COMPO
+1.8V
+VTT_REF
+VCCP
+3VS
R0901 1KOhm 1%
R0911 3.01KOHM
R0912 1KOhm 1%
SM_RCOMP_VOH
SM_RCOMP_VOL
C0957 2.2UF/6.3V
C0958 0.01UF/16V
C0959 2.2UF/6.3V
C0960 0.01UF/16V
R0902 80.6Ohm 1%
R0903 80.6Ohm 1%
R0950 499Ohm 1%
C0969 0.01UF/16V
R0917 1KOhm 1%
R0907 499Ohm 1%
C0953 0.1UF/10V
R0926 56Ohm
R0908 10KOhm
R0909 10KOhm
R0966 10KOhm @
PM_EXTTS#_0 [14]
PM_EXTTS#_1 [15]
CANTIGA_CHIPSET
Title : Cantiga-DDR2/PEG(2)
ASUSTeK COMPUTER INC. NB1
Engineer: Kent Qi
Size Custom
Project Name F6Ve
Rev 1.0
Date: Friday, September 26, 2008
Sheet 9 of 64



ASUSTeK COMPUTER INC. NB1

Title : Cantiga--DDR2 (3)

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

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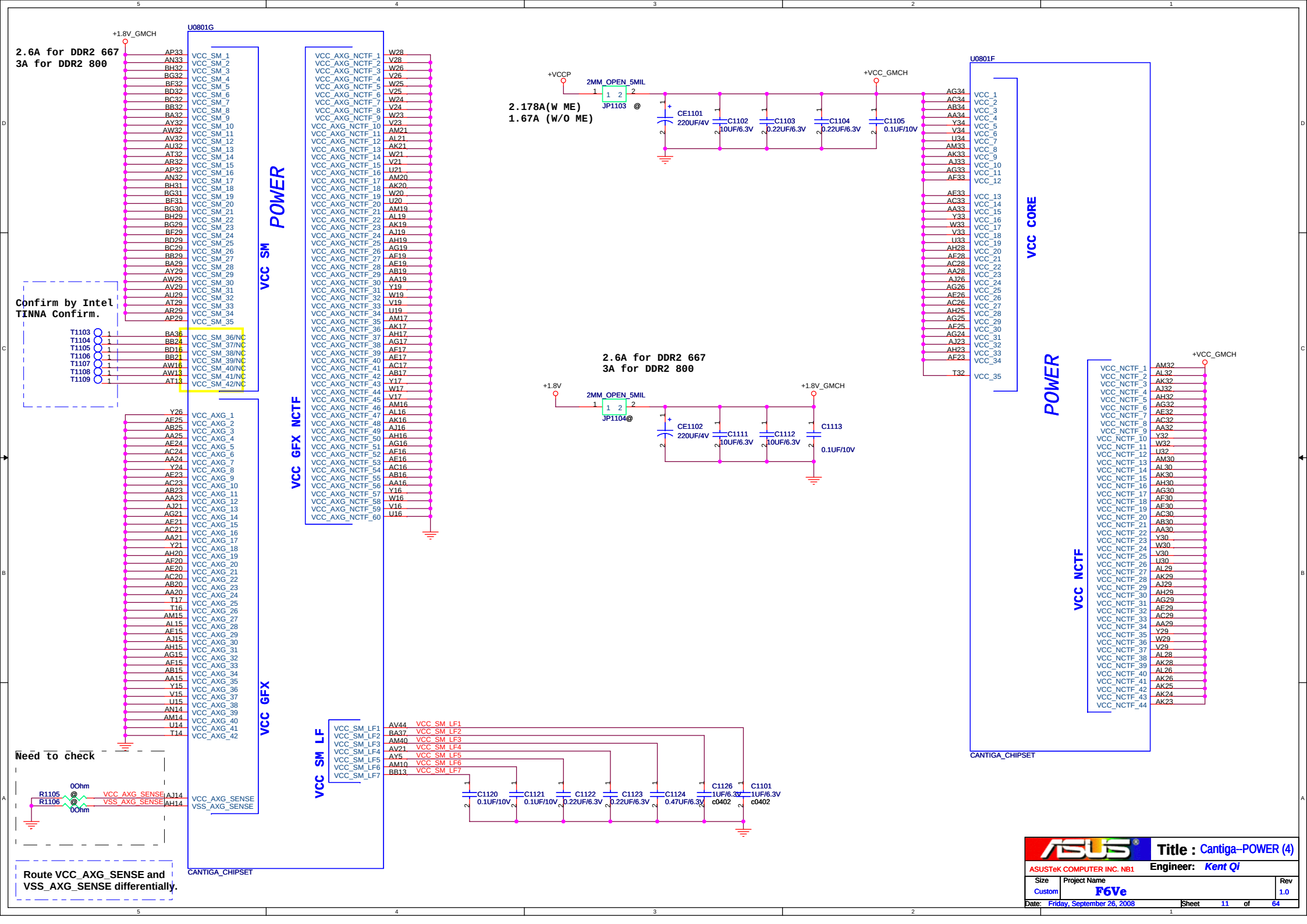
U0801G
+1.8V_GMCH
2.6A for DDR2 667
3A for DDR2 800
VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33 VCC_SM_34 VCC_SM_35
VCC SM
POWER
Confirm by Intel
TINNA Confirm.
T1103 T1104 T1105 T1106 T1107 T1108 T1109
VCC_SM_36/NC VCC_SM_37/NC VCC_SM_38/NC VCC_SM_39/NC VCC_SM_40/NC VCC_SM_41/NC VCC_SM_42/NC
VCC_AXG_1 VCC_AXG_2 VCC_AXG_3 VCC_AXG_4 VCC_AXG_5 VCC_AXG_6 VCC_AXG_7 VCC_AXG_8 VCC_AXG_9 VCC_AXG_10 VCC_AXG_11 VCC_AXG_12 VCC_AXG_13 VCC_AXG_14 VCC_AXG_15 VCC_AXG_16 VCC_AXG_17 VCC_AXG_18 VCC_AXG_19 VCC_AXG_20 VCC_AXG_21 VCC_AXG_22 VCC_AXG_23 VCC_AXG_24 VCC_AXG_25 VCC_AXG_26 VCC_AXG_27 VCC_AXG_28 VCC_AXG_29 VCC_AXG_30 VCC_AXG_31 VCC_AXG_32 VCC_AXG_33 VCC_AXG_34 VCC_AXG_35 VCC_AXG_36 VCC_AXG_37 VCC_AXG_38 VCC_AXG_39 VCC_AXG_40 VCC_AXG_41 VCC_AXG_42
VCC GFX
VCC_AXG_NCTF_1 VCC_AXG_NCTF_2 VCC_AXG_NCTF_3 VCC_AXG_NCTF_4 VCC_AXG_NCTF_5 VCC_AXG_NCTF_6 VCC_AXG_NCTF_7 VCC_AXG_NCTF_8 VCC_AXG_NCTF_9 VCC_AXG_NCTF_10 VCC_AXG_NCTF_11 VCC_AXG_NCTF_12 VCC_AXG_NCTF_13 VCC_AXG_NCTF_14 VCC_AXG_NCTF_15 VCC_AXG_NCTF_16 VCC_AXG_NCTF_17 VCC_AXG_NCTF_18 VCC_AXG_NCTF_19 VCC_AXG_NCTF_20 VCC_AXG_NCTF_21 VCC_AXG_NCTF_22 VCC_AXG_NCTF_23 VCC_AXG_NCTF_24 VCC_AXG_NCTF_25 VCC_AXG_NCTF_26 VCC_AXG_NCTF_27 VCC_AXG_NCTF_28 VCC_AXG_NCTF_29 VCC_AXG_NCTF_30 VCC_AXG_NCTF_31 VCC_AXG_NCTF_32 VCC_AXG_NCTF_33 VCC_AXG_NCTF_34 VCC_AXG_NCTF_35 VCC_AXG_NCTF_36 VCC_AXG_NCTF_37 VCC_AXG_NCTF_38 VCC_AXG_NCTF_39 VCC_AXG_NCTF_40 VCC_AXG_NCTF_41 VCC_AXG_NCTF_42 VCC_AXG_NCTF_43 VCC_AXG_NCTF_44 VCC_AXG_NCTF_45 VCC_AXG_NCTF_46 VCC_AXG_NCTF_47 VCC_AXG_NCTF_48 VCC_AXG_NCTF_49 VCC_AXG_NCTF_50 VCC_AXG_NCTF_51 VCC_AXG_NCTF_52 VCC_AXG_NCTF_53 VCC_AXG_NCTF_54 VCC_AXG_NCTF_55 VCC_AXG_NCTF_56 VCC_AXG_NCTF_57 VCC_AXG_NCTF_58 VCC_AXG_NCTF_59 VCC_AXG_NCTF_60
VCC GFX NCTF
VCC_SM_LF1 VCC_SM_LF2 VCC_SM_LF3 VCC_SM_LF4 VCC_SM_LF5 VCC_SM_LF6 VCC_SM_LF7
VCC SM LF
Need to check
R1105 0Ohm VCC_AXG_SENSE
R1106 0Ohm VSS_AXG_SENSE
VCC_AXG_SENSE VSS_AXG_SENSE
Route VCC_AXG_SENSE and
VSS_AXG_SENSE differentially.
CANTIGA_CHIPSET
+VCCP
2MM_OPEN_5MIL
JP1103 @
2.178A(W ME)
1.67A (W/O ME)
CE1101 220UF/4V
C1102 10UF/6.3V
C1103 0.22UF/6.3V
C1104 0.22UF/6.3V
C1105 0.1UF/10V
+VCC_GMCH
U0801F
VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35
VCC CORE
2.6A for DDR2 667
3A for DDR2 800
+1.8V
2MM_OPEN_5MIL
JP1104@
+1.8V_GMCH
CE1102 220UF/4V
C1111 10UF/6.3V
C1112 10UF/6.3V
C1113 0.1UF/10V
POWER
VCC_NCTF_1 VCC_NCTF_2 VCC_NCTF_3 VCC_NCTF_4 VCC_NCTF_5 VCC_NCTF_6 VCC_NCTF_7 VCC_NCTF_8 VCC_NCTF_9 VCC_NCTF_10 VCC_NCTF_11 VCC_NCTF_12 VCC_NCTF_13 VCC_NCTF_14 VCC_NCTF_15 VCC_NCTF_16 VCC_NCTF_17 VCC_NCTF_18 VCC_NCTF_19 VCC_NCTF_20 VCC_NCTF_21 VCC_NCTF_22 VCC_NCTF_23 VCC_NCTF_24 VCC_NCTF_25 VCC_NCTF_26 VCC_NCTF_27 VCC_NCTF_28 VCC_NCTF_29 VCC_NCTF_30 VCC_NCTF_31 VCC_NCTF_32 VCC_NCTF_33 VCC_NCTF_34 VCC_NCTF_35 VCC_NCTF_36 VCC_NCTF_37 VCC_NCTF_38 VCC_NCTF_39 VCC_NCTF_40 VCC_NCTF_41 VCC_NCTF_42 VCC_NCTF_43 VCC_NCTF_44
VCC NCTF
+VCC_GMCH
CANTIGA_CHIPSET
C1120 0.1UF/10V
C1121 0.1UF/10V
C1122 0.22UF/6.3V
C1123 0.22UF/6.3V
C1124 0.47UF/6.3V
C1126 1UF/6.3V c0402
C1101 1UF/6.3V c0402
Title : Cantiga--POWER (4)
ASUSTeK COMPUTER INC. NB1
Engineer: Kent Qi
Size Custom
Project Name F6Ve
Rev 1.0
Date: Friday, September 26, 2008
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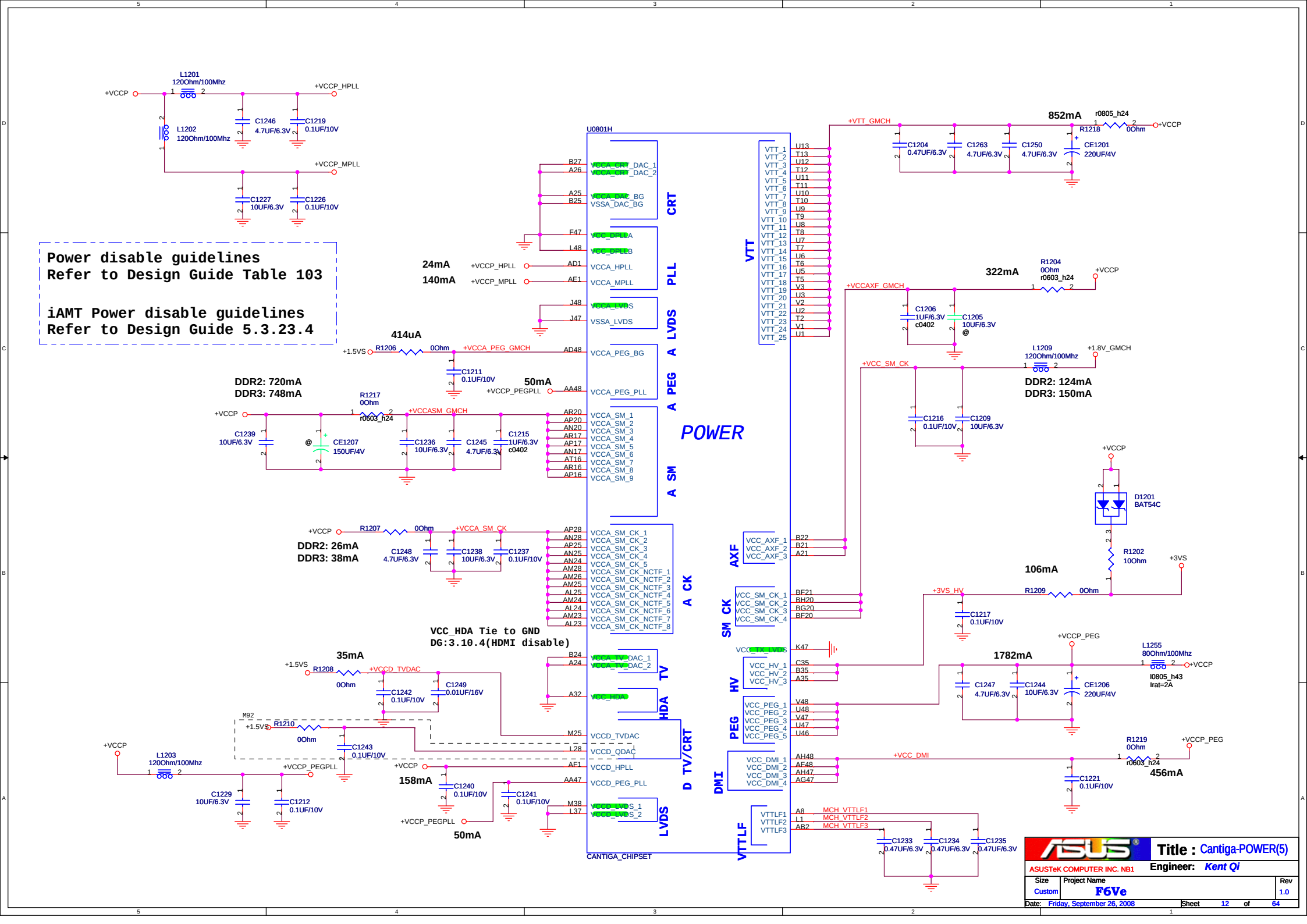
Power disable guidelines
Refer to Design Guide Table 103
iAMT Power disable guidelines
Refer to Design Guide 5.3.23.4
POWER
U0801H
CANTIGA_CHIPSET
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
DDR2: 720mA
DDR3: 748mA
DDR2: 26mA
DDR3: 38mA
VCC_HDA Tie to GND
DG:3.10.4(HDMI disable)
852mA
322mA
106mA
1782mA
456mA
158mA
50mA
414uA
24mA
140mA
35mA
DDR2: 124mA
DDR3: 150mA
Title : Cantiga-POWER(5)
ASUSTeK COMPUTER INC. NB1
Engineer: Kent Qi
Size: Custom
Project Name: F6Ve
Rev: 1.0
Date: Friday, September 26, 2008
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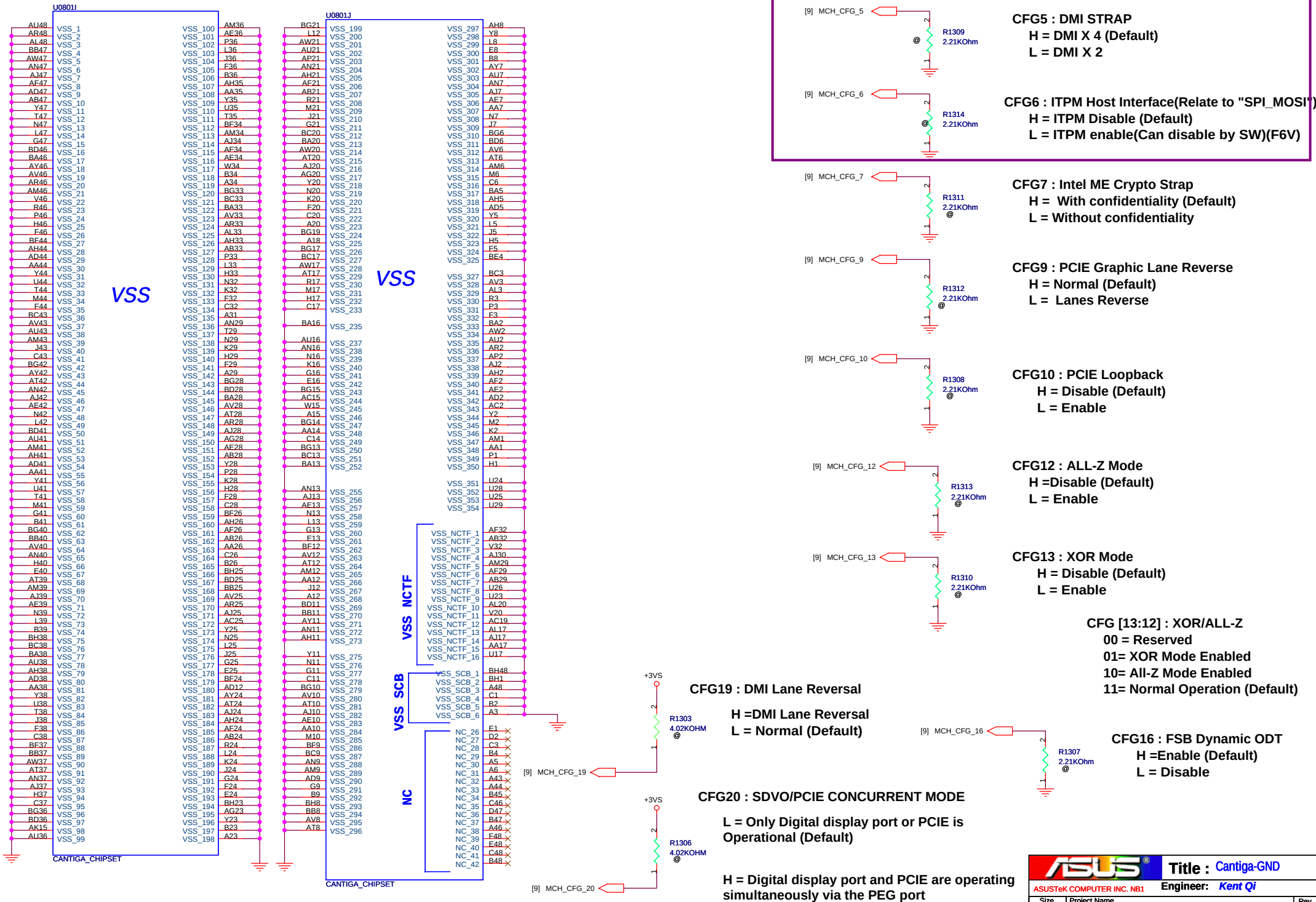

CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface(Relate to "SPI_MOSI")
H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)(F6V)

CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse

CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable

CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

CFG19 : DMI Lane Reversal
H =DMI Lane Reversal
L = Normal (Default)

CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

CFG20 : SDVO/PCIE CONCURRENT MODE
L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

ASUSTeK COMPUTER INC. NB1	Title : Cantiga-GND	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
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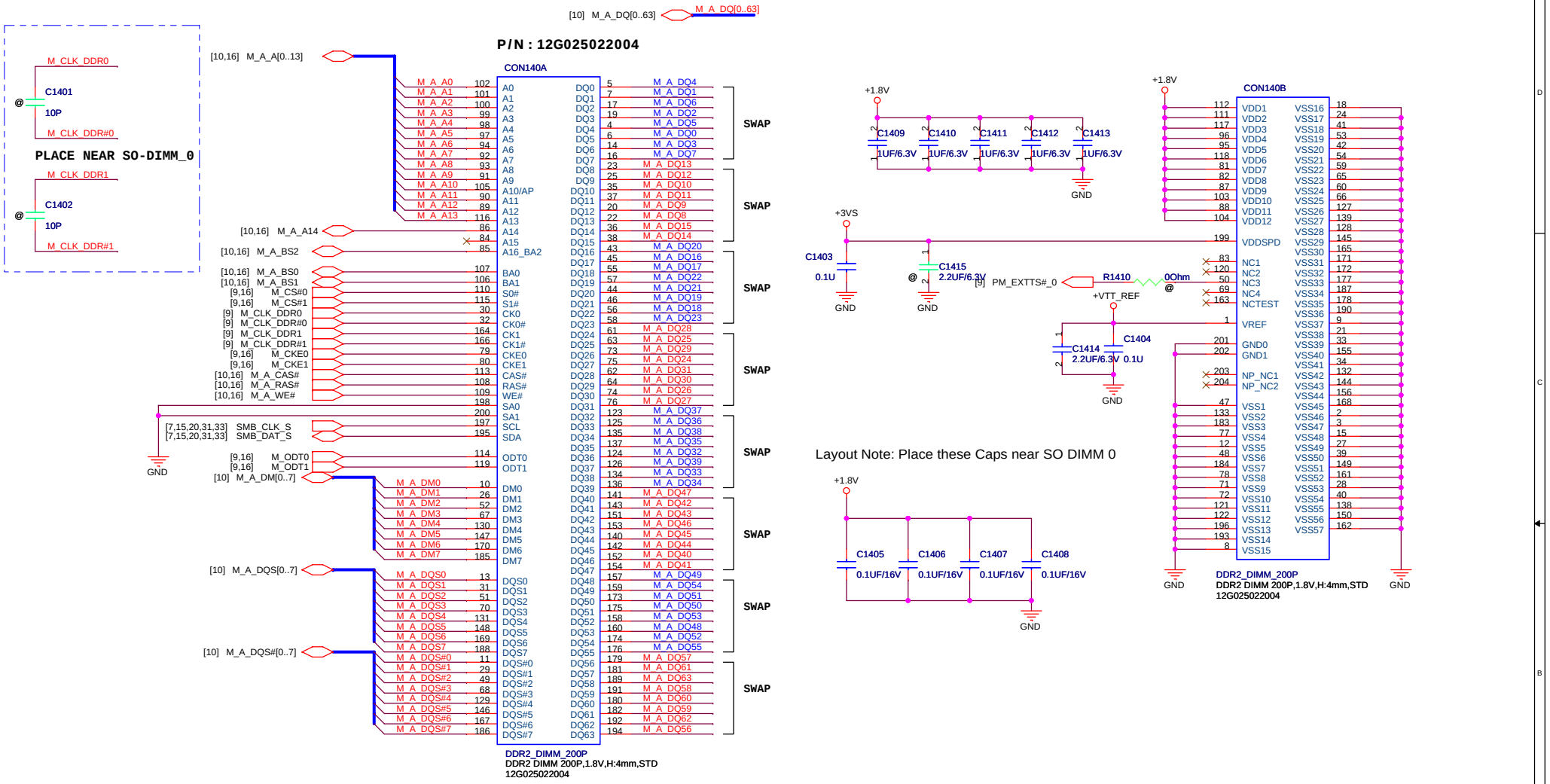

<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM 0

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

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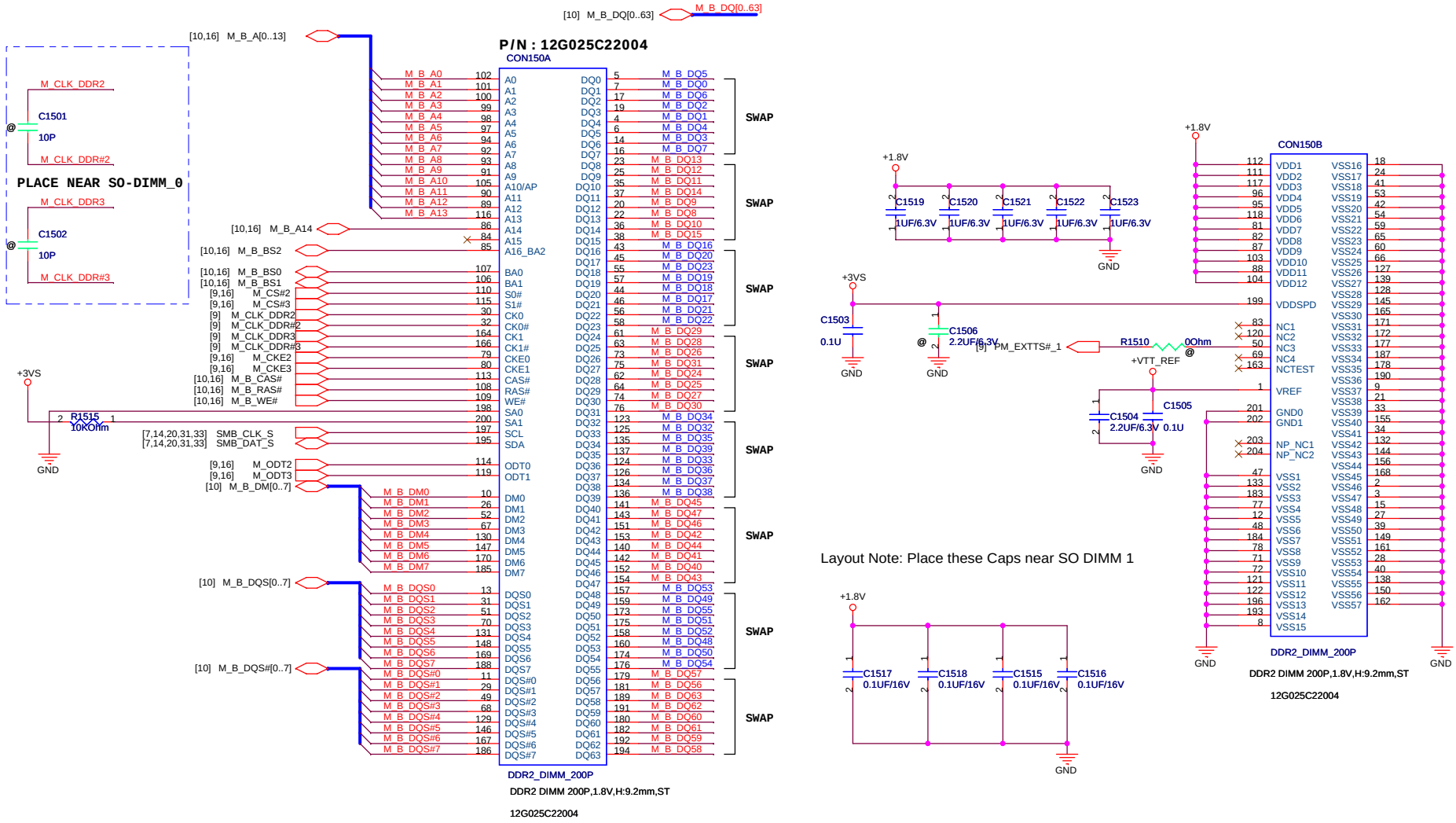
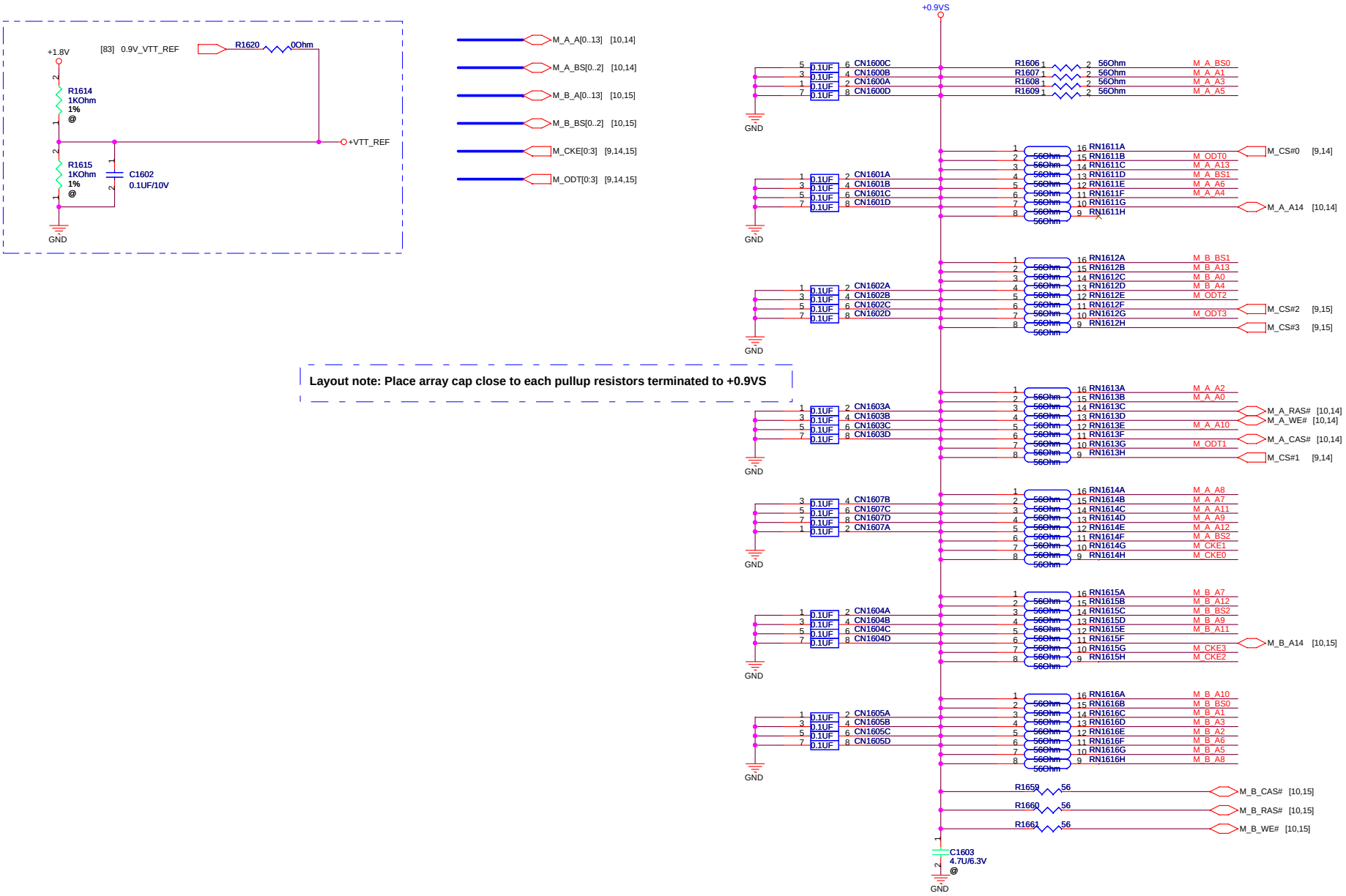


<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM_1	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 15 of 64	



<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 ADDR TERM

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

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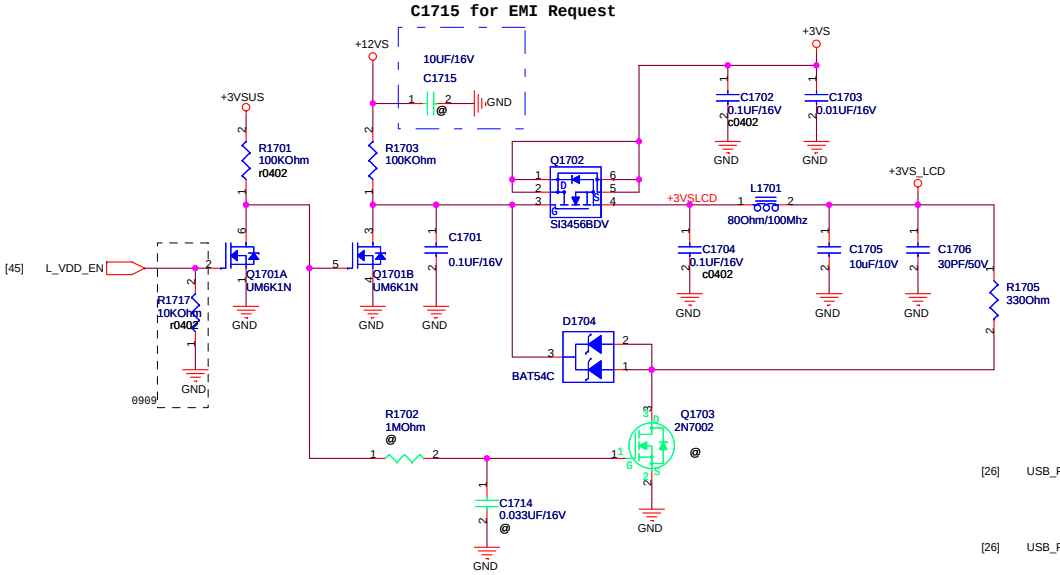
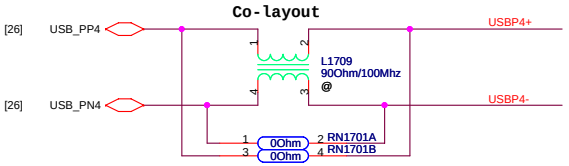
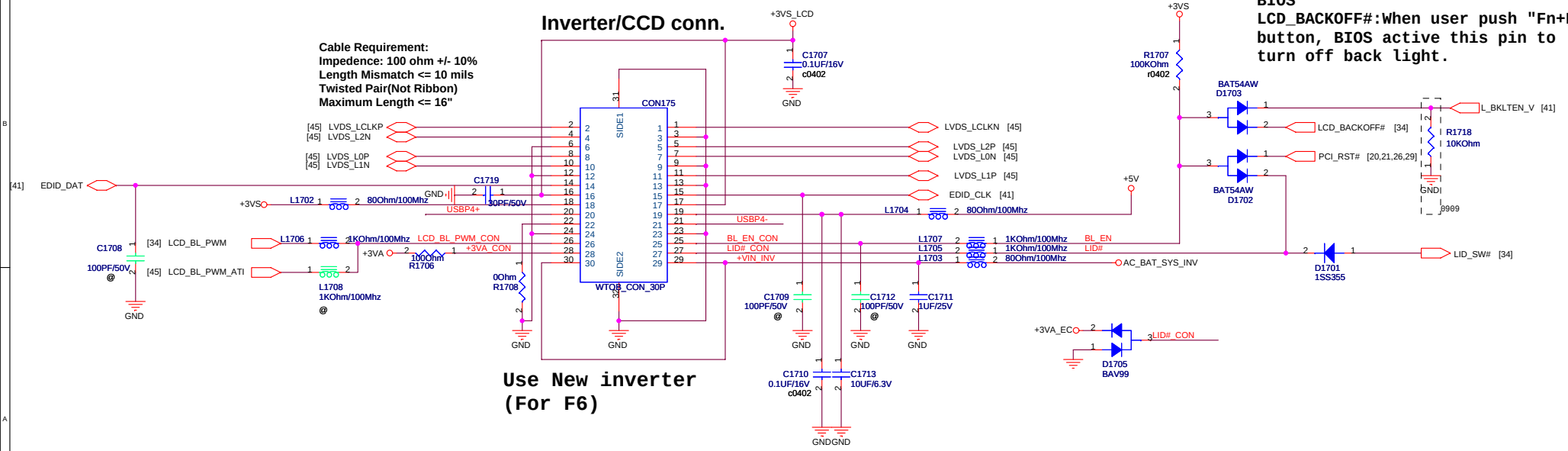
LCD Power





Inverter/CCD conn.

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

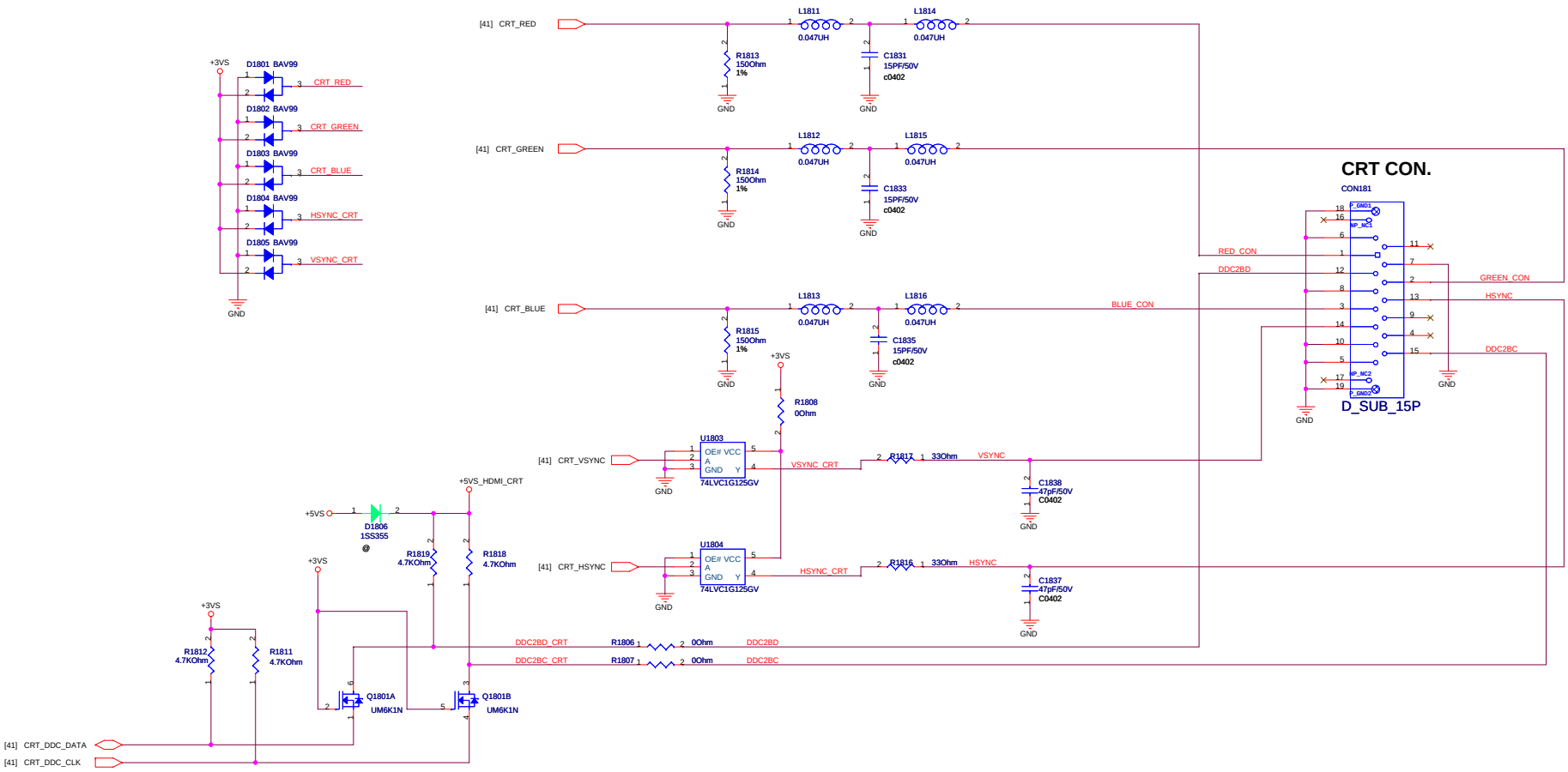


Use New inverter (For F6)

BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 17 of 64	



<Variant Name>

ASUSTeK COMPUTER INC.

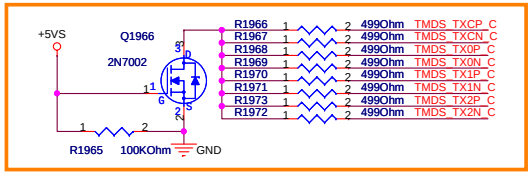
Title : CRT

Engineer: Kent Qi

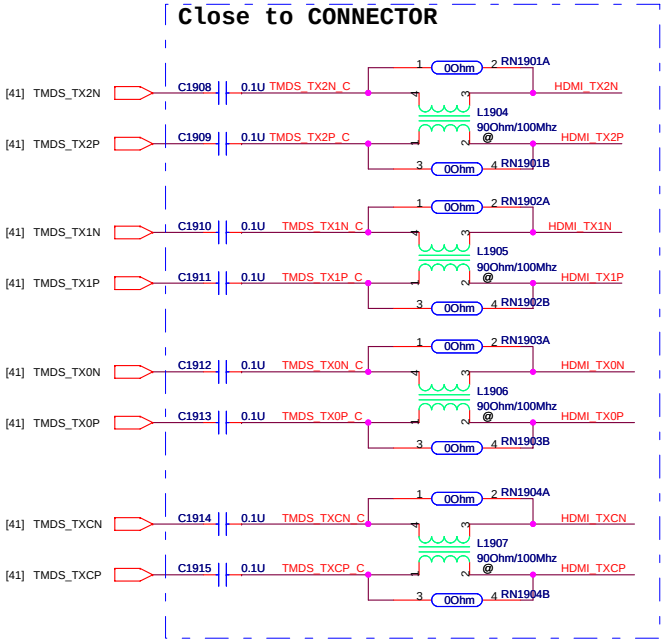
Size	Project Name	Rev
C	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 18 of 64

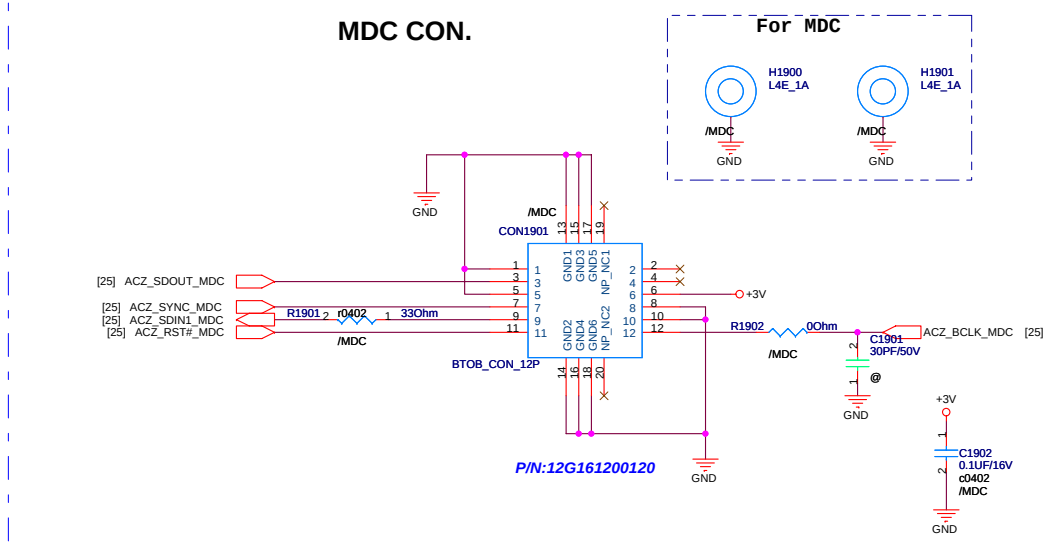
Close to CONNECTOR

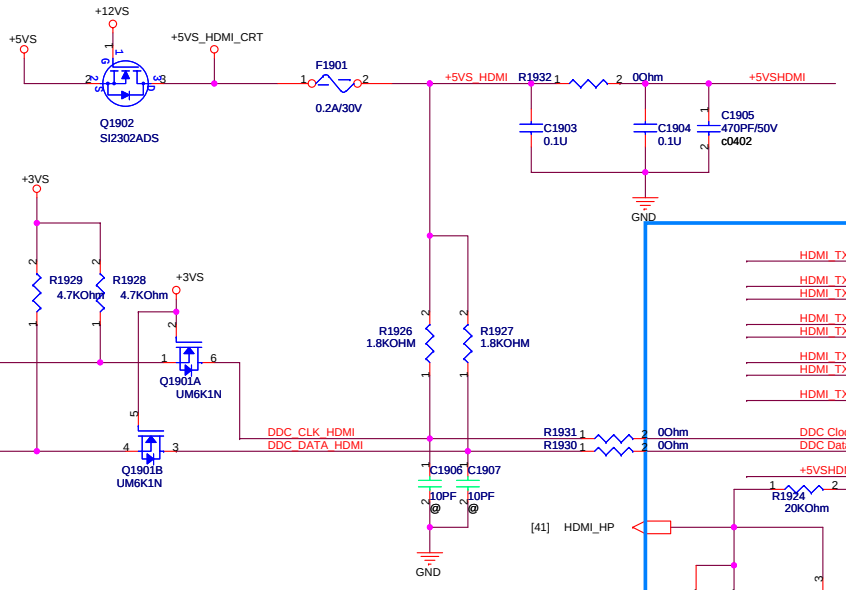


Close to CONNECTOR

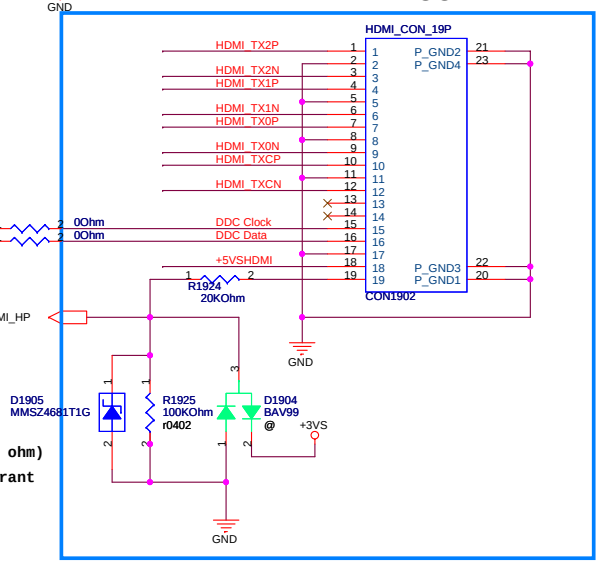


MDC CON.





HDMI CON.



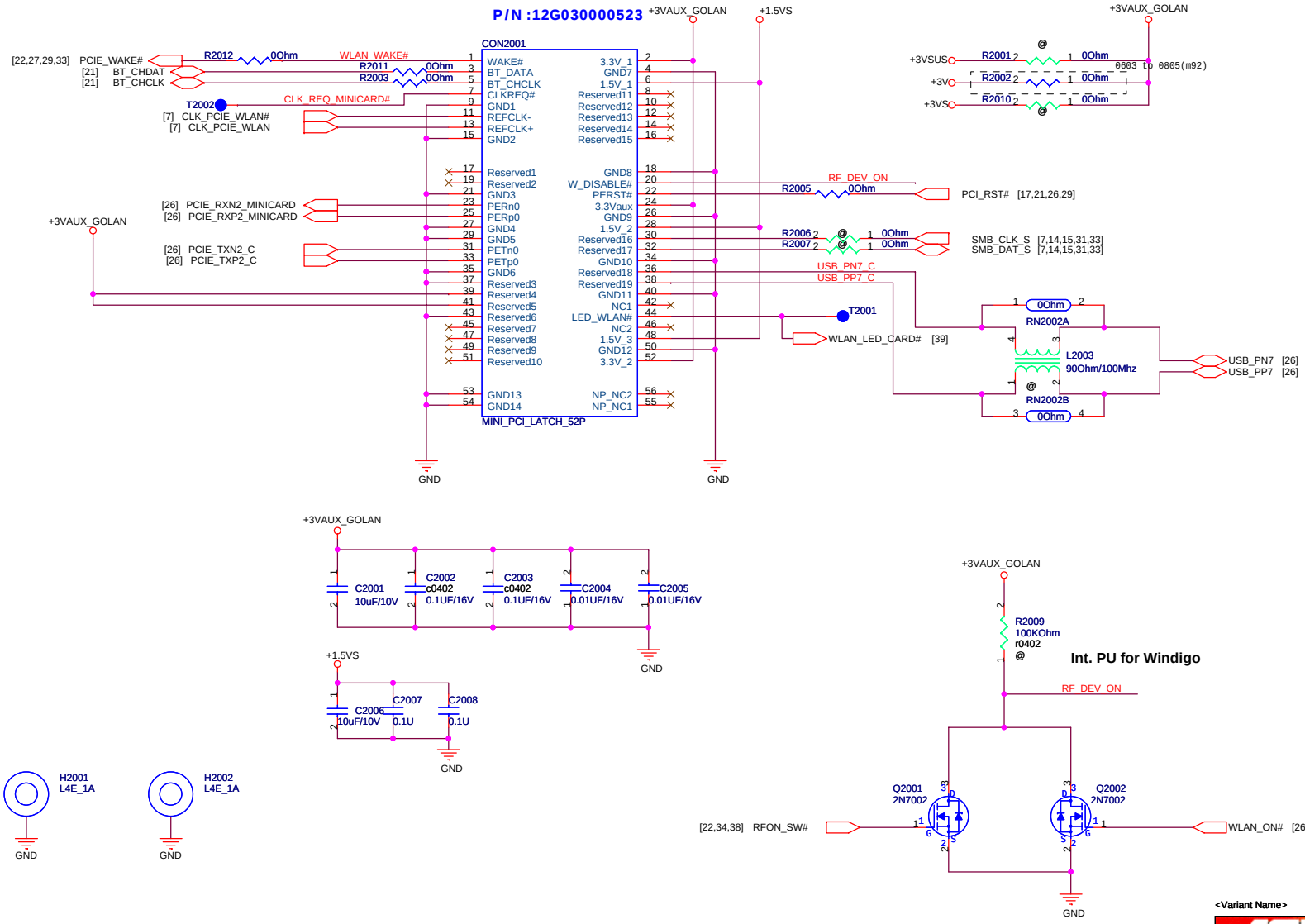
Note: 1. R1930,R1931,R1932: For EMI.(defult=0 ohm)
2. HDMI_DDC_CLK,HDMI_DDC_DATA: +3V tolerant

<Variant Name>

ASUSTeK COMPUTER INC	Title : MDC,HDMI CON	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 19 of 64	

WLAN/WIMAX

P/N :12G030000523



<Variant Name>

ASUSTeK COMPUTER INC

Title : MINI CARD--(1)

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

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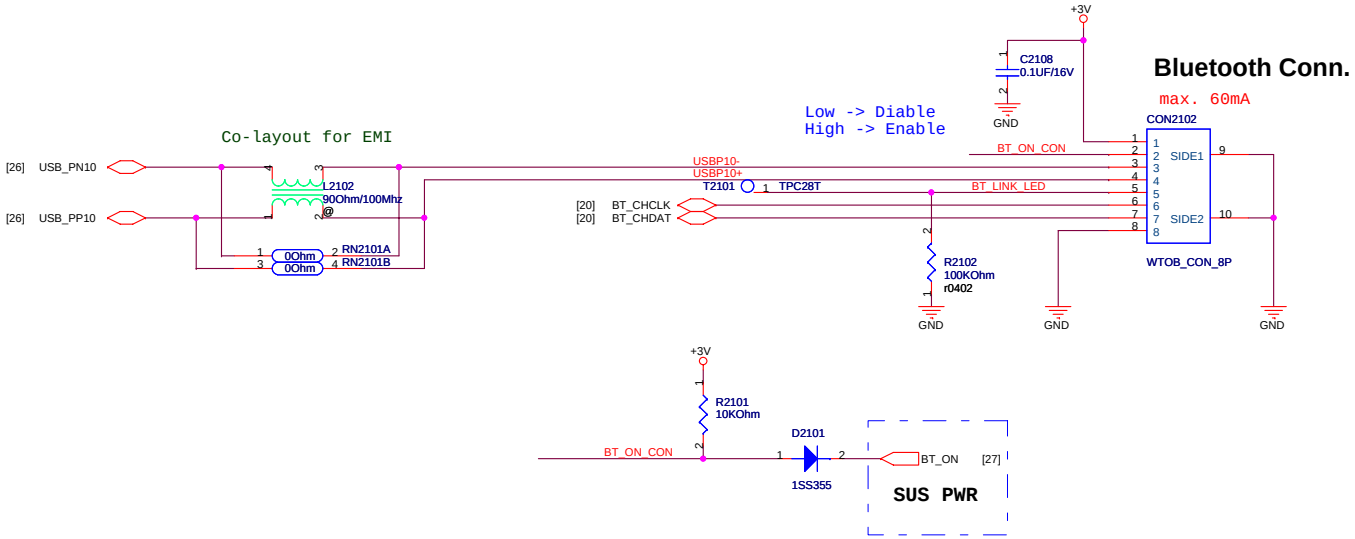

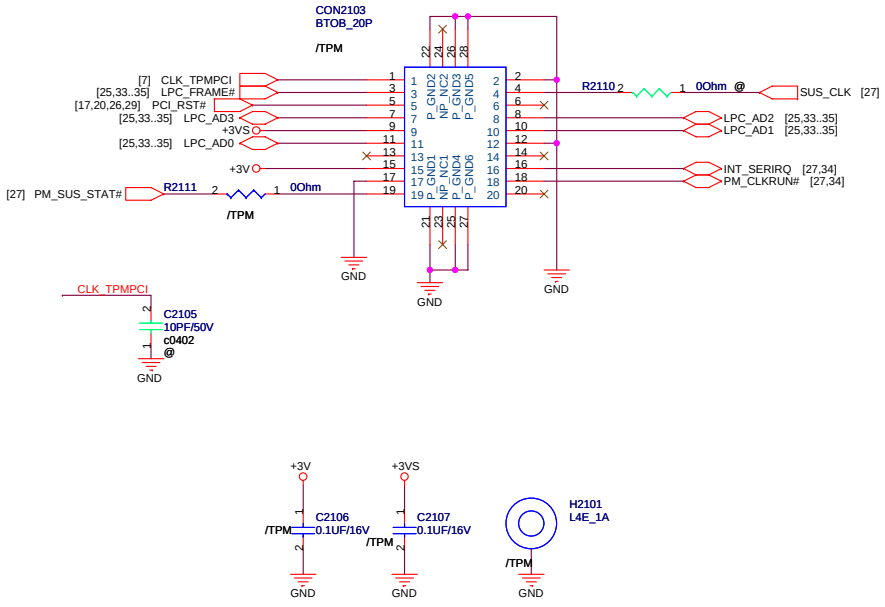

<Variant Name>

ASUSTeK COMPUTER INC

Title : B/T& TPM

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

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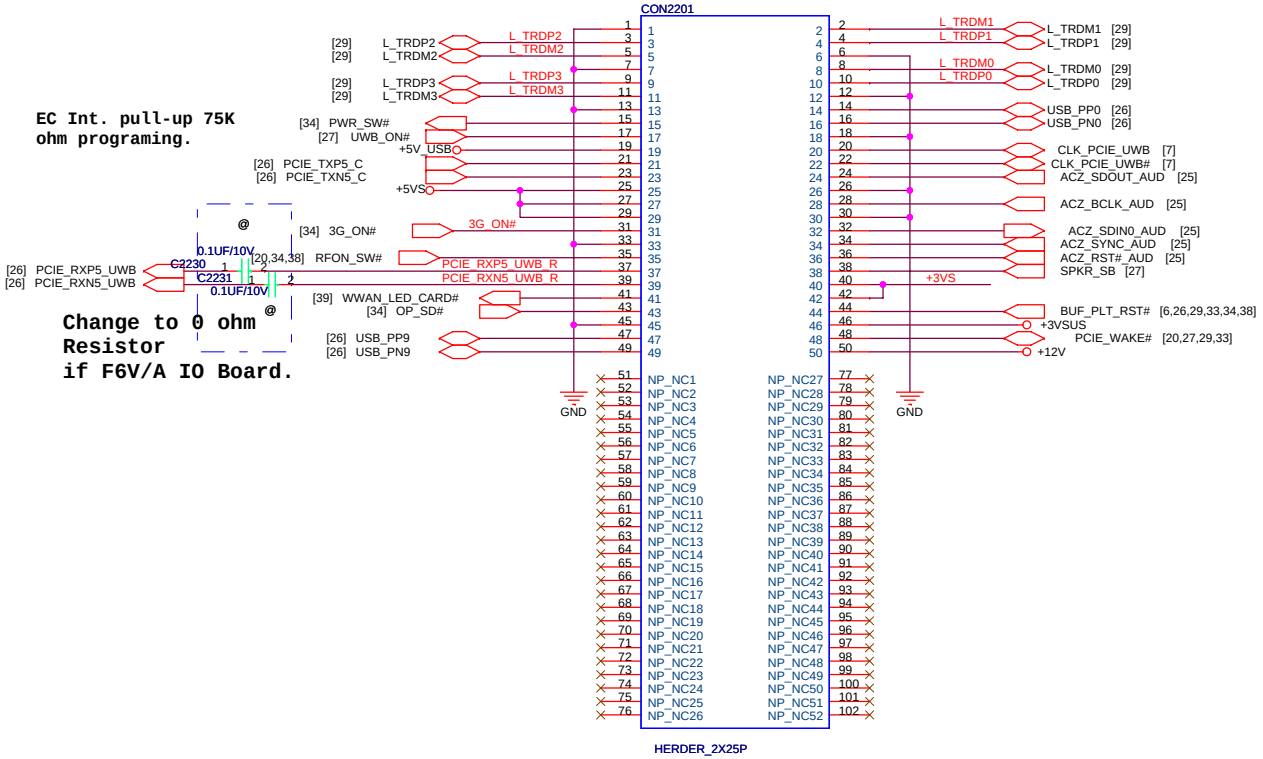
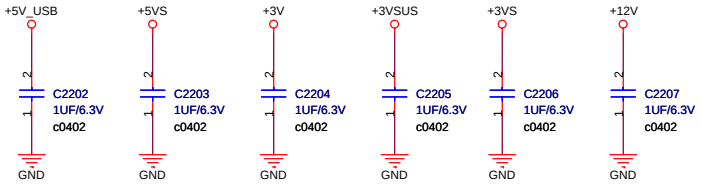




<Variant Name>

ASUSTeK COMPUTER INC

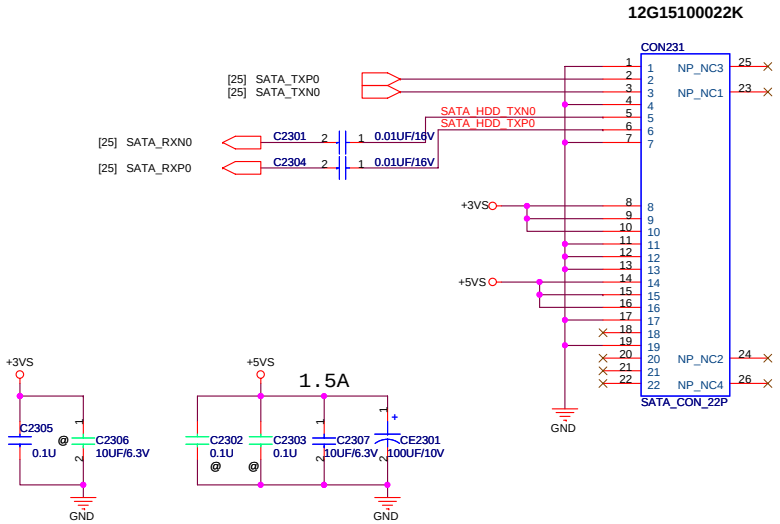
Title : B TO B CONN(M)

Engineer: Kent Qi

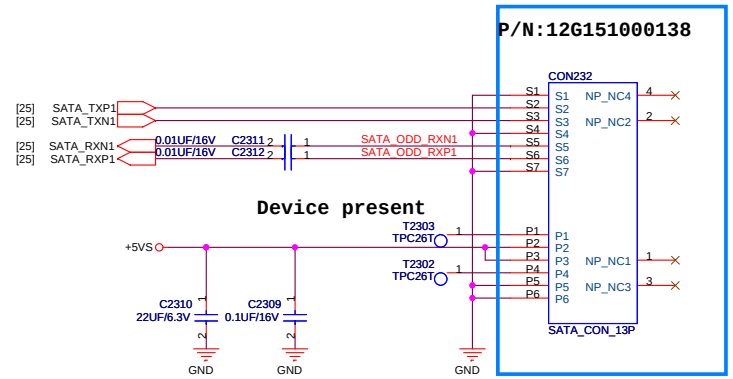
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 22 of 64

SATA HDD CON



SATA ODD CON



<Variant Name>

Title : HDD & CDROM

ASUSTeK COMPUTER INC

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

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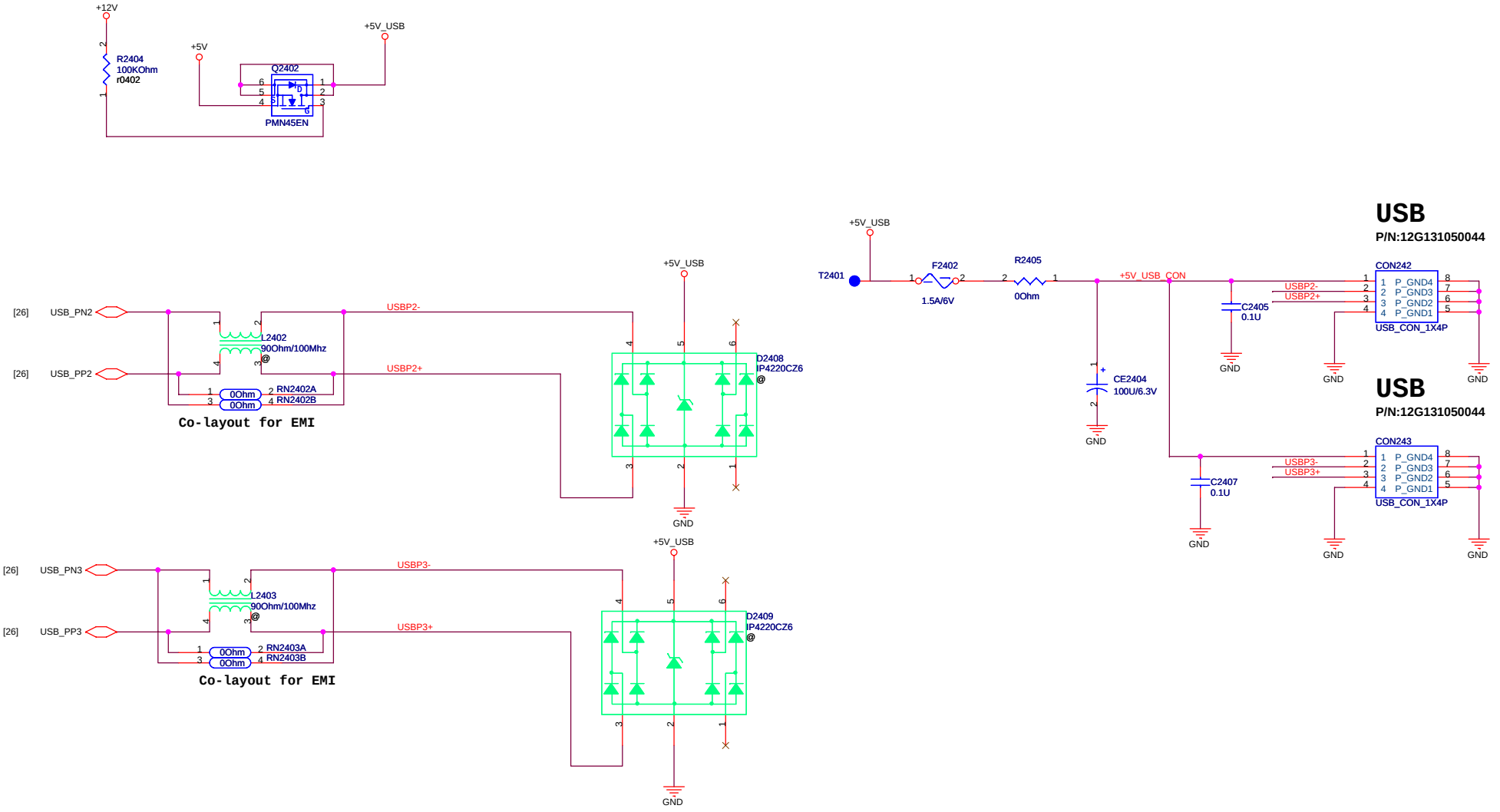
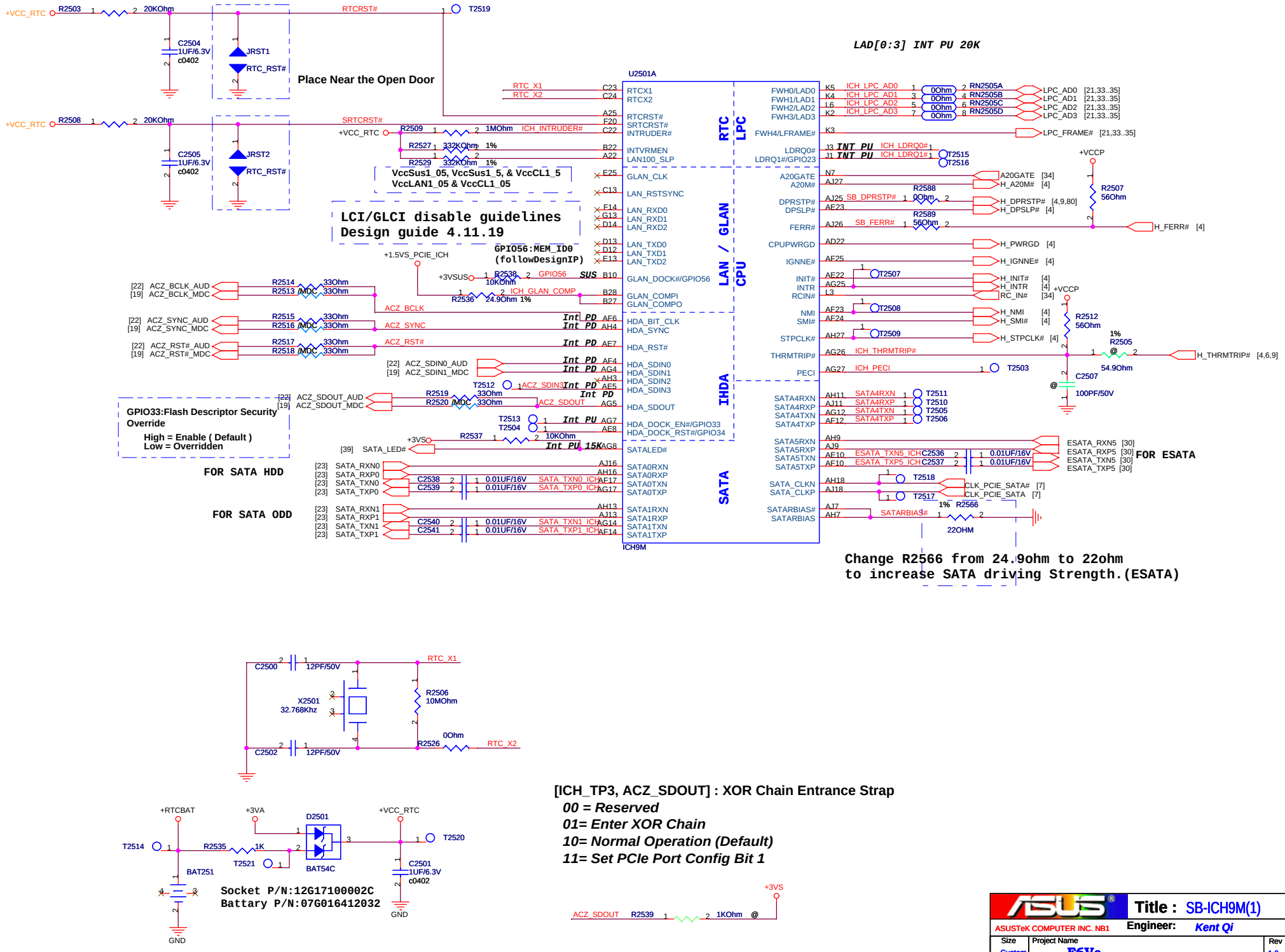


<Variant Name>

ASUSTeK COMPUTER INC	Title : USB PORTS	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 24 of 64	


LAD[0:3] INT PU 20K
Place Near the Open Door
VccSus1_05, VccSus1_5, & VccCL1_5
VccLAN1_05 & VccCL1_05
LCI/GLCI disable guidelines
Design guide 4.11.19
GPIO56:MEM_ID0
(followDesignIP)
GPIO33:Flash Descriptor Security
Override
High = Enable (Default)
Low = Overridden
FOR SATA HDD
FOR SATA ODD
FOR ESATA
U2501A
ICH9M
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
Change R2566 from 24.9ohm to 22ohm
to increase SATA driving Strength.(ESATA)
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
Socket P/N:12G17100002C
Battary P/N:07G016412032
Title : SB-ICH9M(1)
ASUSTeK COMPUTER INC. NB1
Engineer: Kent Qi
Size Custom
Project Name F6Ve
Rev 1.0
Date: Friday, September 26, 2008
Sheet 25 of 64

ICH9 Boot BIOS select

		GNT#0	SPICS#1
LPC	11	1	1 (default)
PCI	10	1	0
SPI	01	0	1

PCIE 1	
PCIE 2	WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	UWB
PCIE 6	LAN

PCI_GNT#0 R2601 1 @ 2 1KOhm

SB_SPICS1# R2602 1 @ 2 1KOhm

GNT#[0:3]:INT PU

U2501B

PCI

REQ0# F1 PCI_REQ#0 [27]
GNT0# G4 PCI_GNT#0 1 T2604
REQ1#/GPIO50 B6 PCI_REQ#1 [27] T2601
GNT1#/GPIO51 A7 1
REQ2#/GPIO52 F13 PCI_REQ#2 [27] T2602
GNT2#/GPIO53 F12 1
REQ3#/GPIO54 E6 PCI_REQ#3 [27] T2603
GNT3#/GPIO55 F6 1

C/BE0# D8
C/BE1# B4
C/BE2# D6
C/BE3# A5

IRDY# D3 PCI_IRDY# [27]
PAR E3 1 T2605
PCIRST# R1 PCI_RST# [17,20,21,29]
DEVSEL# C6 PCI_DEVSEL# [27]
PERR# E4 PCI_PERR# [27]
PLOCK# C2 PCI_LOCK# [27]
SERR# J4 PCI_SERR# [27]
STOP# A4 PCI_STOP# [27]
TRDY# F5 PCI_TRDY# [27]
FRAME# D7 PCI_FRAME# [27]

PLTRST# C14 PLT_RST# PLT_RST# [9,40]
PCICLK D4 CLK_ICHPCI [7]
PME# R2 PCI_PME# T2610
INT PU
R2609 1 2 @ 10KOhm
+3VSUS

AD0 D11
AD1 C8
AD2 D9
AD3 E12
AD4 E9
AD5 C9
AD6 E10
AD7 B7
AD8 C7
AD9 C5
AD10 G11
AD11 F8
AD12 F11
AD13 E7
AD14 A3
AD15 D2
AD16 F10
AD17 D5
AD18 D10
AD19 B3
AD20 F7
AD21 C3
AD22 F3
AD23 F4
AD24 C1
AD25 G7
AD26 H7
AD27 D1
AD28 G5
AD29 H6
AD30 G1
AD31 H3

Interrupt I/F

PIRQA# J5 [27] PCI_INTA#
PIRQB# E1 [27] PCI_INTB#
PIRQC# J6 [27] PCI_INTC#
PIRQD# C4 [27] PCI_INTD#
PIRQE#/GPIO2 H4 PCI_INTE# [27]
PIRQF#/GPIO3 K6 PCI_INTF# [27]
PIRQG#/GPIO4 F2 PCI_INTG# [27]
PIRQH#/GPIO5 G2 PCI_INTH# [27]

ICH9M

+3V
C2605 0.1UF/16V
@ c0402
GND

U2603 @
1 INB
2 INA
3 GND
5 VCC
4 OUTY
74LVC1G08GW

PLT_RST# BUF_PLT_RST# [6,22,29,33,34,38]
GND
R2608 0Ohm

U2501D

PCI-Express

PERn1 N29 [20] PCIE_RXN2_MINICARD
PERp1 N28 [20] PCIE_RXP2_MINICARD
PETn1 P27 [20] PCIE_TXN2_C
PETp1 P26 [20] PCIE_TXP2_C
C2643 1 2 0.1UF/10V PCIE_TXN2_MINICARD
C2644 1 2 0.1UF/10V PCIE_TXP2_MINICARD

PERn2 L29 [33] PCIE_RXN3_NEWCARD
PERp2 L28 [33] PCIE_RXP3_NEWCARD
PETn2 M27 [33] PCIE_TXN3_C
PETp2 M26 [33] PCIE_TXP3_C
C2645 1 2 0.1UF/10V PCIE_TXN3_NEWCARD
C2646 1 2 0.1UF/10V PCIE_TXP3_NEWCARD

PERn3 J29
PERp3 J28
PETn3 K27
PETp3 K26

PERn4 G29 [22] PCIE_RXN5_UWB
PERp4 G28 [22] PCIE_RXP5_UWB
PETn4 H27 [22] PCIE_TXN5_C
PETp4 H26 [22] PCIE_TXP5_C
C2650 1 2 0.1UF/10V PCIE_TXN5_UWB
C2649 1 2 0.1UF/10V PCIE_TXP5_UWB

PERn5 E29 [29] PCIE_RXN6_GLAN
PERp5 E28 [29] PCIE_RXP6_GLAN
PETn5 F27 [29] PCIE_TXN6_C
PETp5 F26 [29] PCIE_TXP6_C
C2648 1 2 0.1UF/10V PCIE_TXN6_GLAN
C2647 1 2 0.1UF/10V PCIE_TXP6_GLAN

PERn6/GLAN_RXN C29
PERp6/GLAN_RXP C28
PETn6/GLAN_TXN D27
PETp6/GLAN_TXP D26

Direct Media Interface

DMI0RXN V27 DMI_RXN0 [9]
DMI0RXP V26 DMI_RXP0 [9]
DMI0TXN U29 DMI_TXN0 [9]
DMI0TXP U28 DMI_TXP0 [9]

DMI1RXN Y27 DMI_RXN1 [9]
DMI1RXP Y26 DMI_RXP1 [9]
DMI1TXN W29 DMI_TXN1 [9]
DMI1TXP W28 DMI_TXP1 [9]

DMI2RXN AB27 DMI_RXN2 [9]
DMI2RXP AB26 DMI_RXP2 [9]
DMI2TXN AA29 DMI_TXN2 [9]
DMI2TXP AA28 DMI_TXP2 [9]

DMI3RXN AD27 DMI_RXN3 [9]
DMI3RXP AD26 DMI_RXP3 [9]
DMI3TXN AC29 DMI_TXN3 [9]
DMI3TXP AC28 DMI_TXP3 [9]

DMI_CLKN T26 T2608 CLK_PCIE_ICH# [7]
DMI_CLKP T25 T2609 CLK_PCIE_ICH [7]
DMI_ZCOMP AF29 DMI_COMP R2603 1 2 24.9Ohm 1% +1.5VS_PCIE_ICH
DMI_IRCOMP AF28 L<500mils

SPI

SPI_CLK [31] SPI_CLK R2612 1 15Ohm 2 @ SB_SPICLK D23 SPI_CLK
SPI_CS0# [31] SPI_CS#0 R2613 1 15Ohm 2 @ SB_SPICS0# D24 SPI_CS0
SB_SPICS1# INT PU F23 SPI_CS1#/GPIO58/CLGPIO6
T2607
SPI_SI [31] R2615 1 15Ohm 2 SB_SPISI INT PD 20K D25 SPI_MOSI
INT PU
[31] @ SPI_SO E23 SPI_MISO

+3VS R2606 1 @ 2 1KOhm 1%

SPI_MOSI (relate to MCH_CFG_6)
iTPM Enable

H: Enable (F6V)

L: Disable(Default)

USB

USBP0N AC5 USB_PN0 [22]
USBP0P AC4 USB_PP0 [22]
USBP1N AD3 USB_PN1 1 T2613
USBP1P AD2 USB_PP1 1 T2614
USBP2N AC1 USB_PN2 [24]
USBP2P AC2 USB_PP2 [24]
USBP3N AA5 USB_PN3 [24]
USBP3P AA4 USB_PP3 [24]
USBP4N AB2 USB_PN4 [17]
USBP4P AB3 USB_PP4 [17]
USBP5N AA1 USB_PN5 [36]
USBP5P AA2 USB_PP5 [36]
USBP6N W5 USB_PN6 1 T2611
USBP6P W4 USB_PP6 1 T2612
USBP7N Y3 USB_PN7 [20]
USBP7P Y2 USB_PP7 [20]
USBP8N W1 USB_PN8 [33]
USBP8P W2 USB_PP8 [33]
USBP9N V2 USB_PN9 [22]
USBP9P V3 USB_PP9 [22]
USBP10N U5 USB_PN10 [21]
USBP10P U4 USB_PP10 [21]
USBP11N U1 USB_PN11 [38]
USBP11P U2 USB_PP11 [38]

USB INT PD 15K

USB_OC#0 N4
USB_OC#1 N5
USB_OC#2 N6
USB_OC#3 P6
USB_OC#4 M1
USB_OC#5 N2
USB_OC#6 M4
USB_OC#7 M3
USB_OC#8 N3
USB_OC#9 N1
USB_OC#10 P5
USB_OC#11 P3

OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#/GPIO44
OC9#/GPIO45
OC10#/GPIO46
OC11#/GPIO47

WLAN_ON R2626 0Ohm

USBRBIAS AG2
USBRBIAS# AG1
R2605 2 1 22.6Ohm 1% USBRBIAS_PN

ICH9M

Place within 500 mils of ICH

+3V
R2611 100KOhm
WLAN_ON# [20]
Q2602 2N7002
WLAN_ON

+3VSUS

RN2606A 1 2 10KOhm USB_OC#1
RN2606B 3 4 10KOhm USB_OC#6
RN2606C 5 6 10KOhm USB_OC#2
RN2606D 7 8 10KOhm USB_OC#3
RN2607A 1 2 10KOhm USB_OC#4
RN2607B 3 4 10KOhm USB_OC#8
RN2607C 5 6 10KOhm USB_OC#7
RN2607D 7 8 10KOhm USB_OC#0
RN2609A 1 2 10KOhm USB_OC#11
RN2609B 3 4 10KOhm USB_OC#9
RN2609C 5 6 10KOhm USB_OC#10
RN2609D 7 8 10KOhm USB_OC#5

USB 0	USB Conn
USB 1	
USB 2	USB Conn
USB 3	USB Conn
USB 4	CMOS Camera
USB 5	CardReader
USB 6	UWB
USB 7	WiMax
USB 8	NewCard
USB 9	3G Card
USB 10	Bluetooth
USB 11	FINGER PRINT

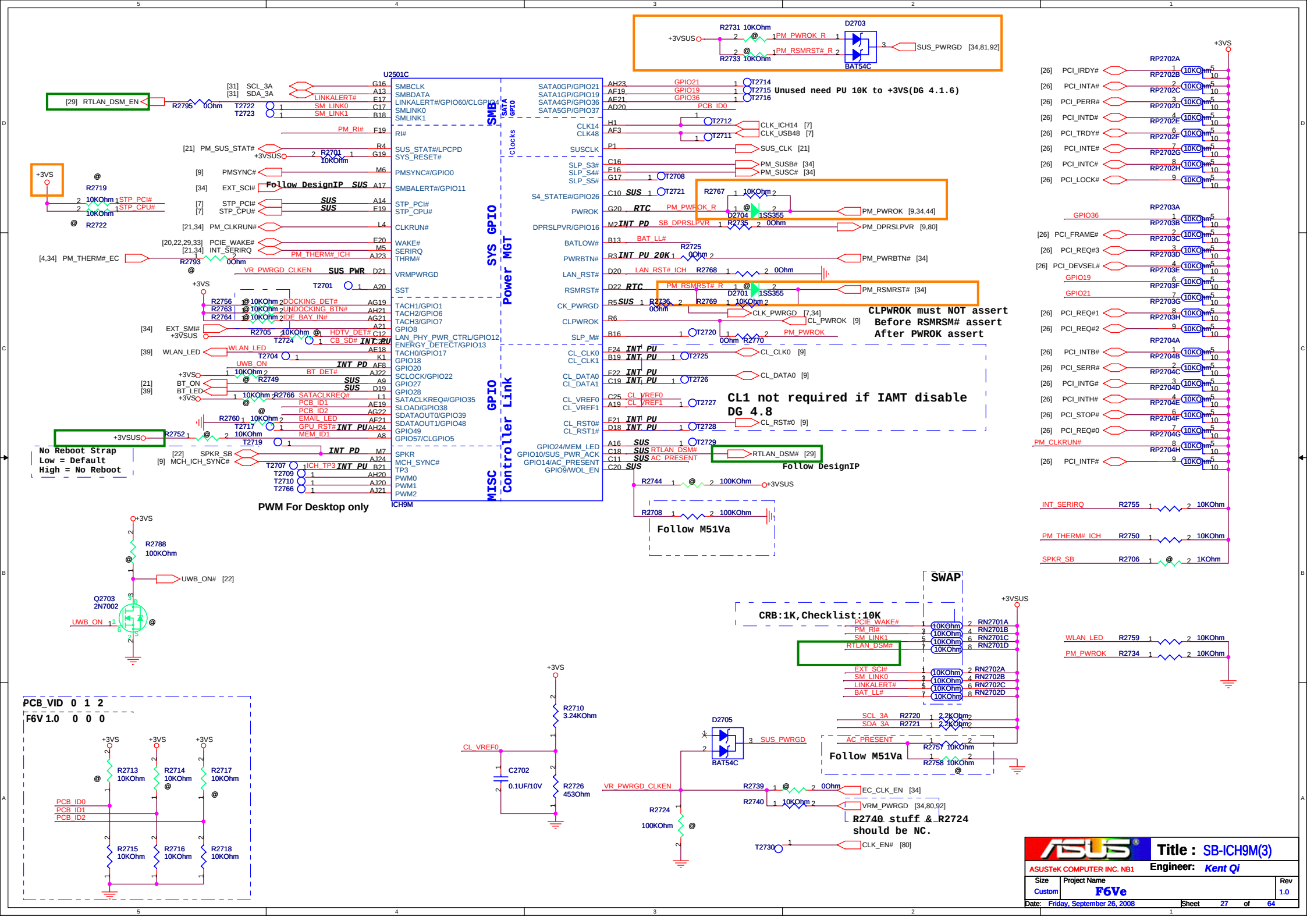
ASUSTeK COMPUTER INC. NB1

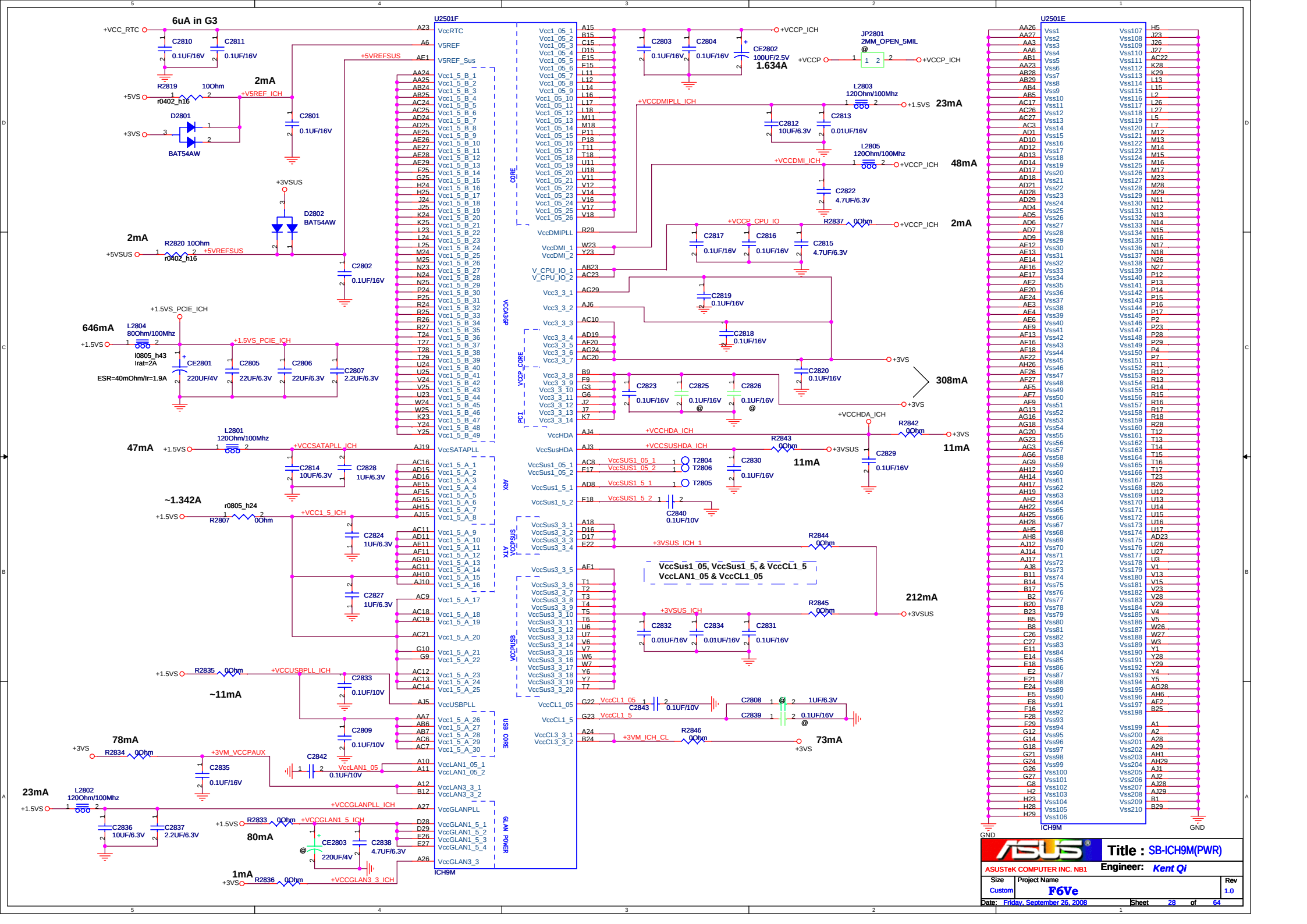
Title : SB-ICH9M(2)

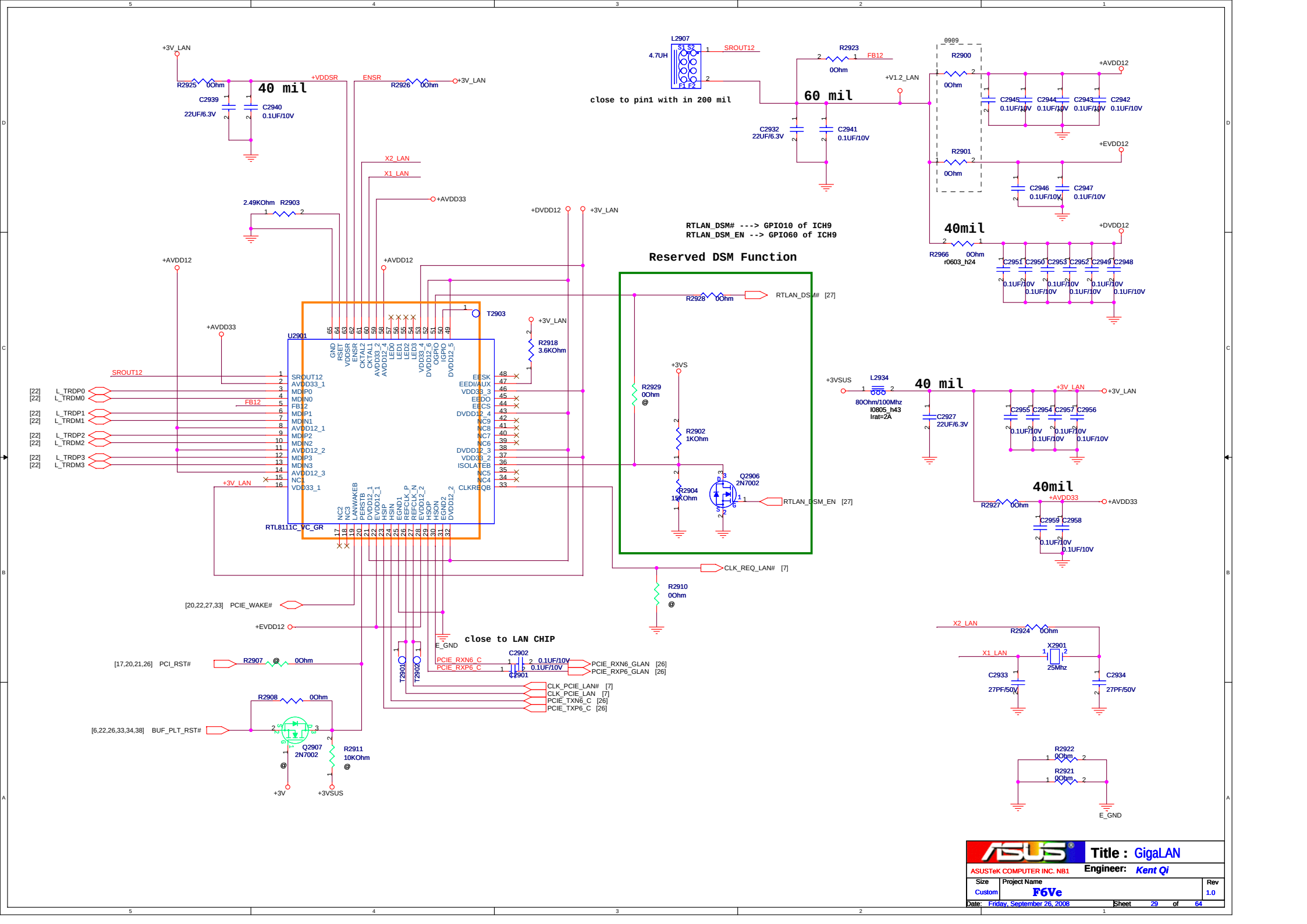
Engineer: Kent Qi

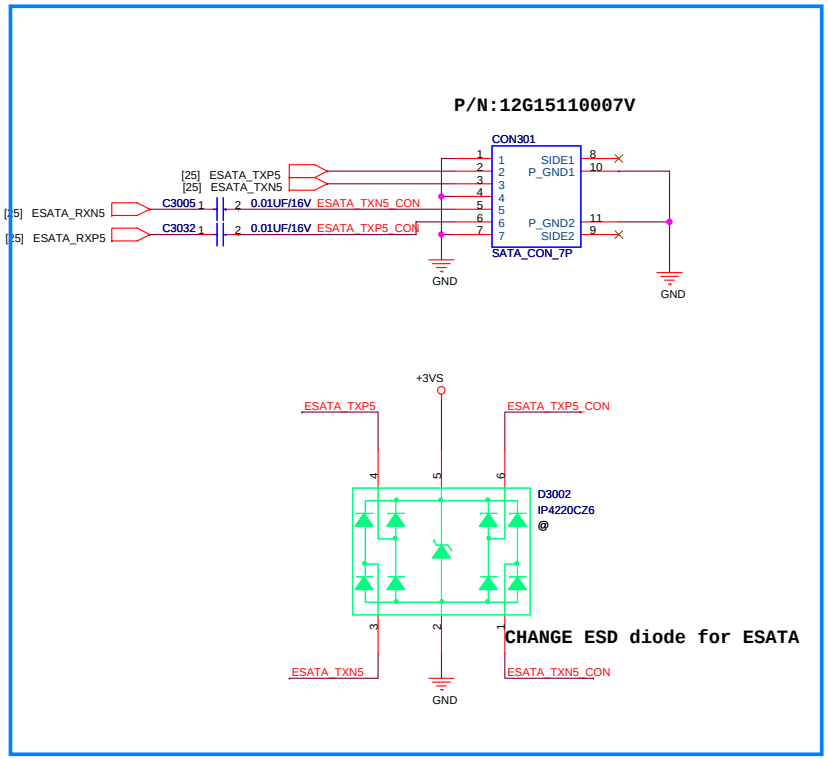
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 26 of 64


U2501C
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M
Unused need PU 10K to +3VS(DG 4.1.6)
CLPWROK must NOT assert
Before RSMRSM# assert
After PWROK assert
CL1 not required if IAMT disable
DG 4.8
Follow DesignIP
Follow M51Va
Follow DesignIP SUS
PWM For Desktop only
No Reboot Strap
Low = Default
High = No Reboot
SWAP
CRB:1K,Checklist:10K
R2720 2.2KOhm
R2721 2.2KOhm
R2710 3.24KOhm
R2726 453Ohm
C2702 0.1UF/10V
R2724 100KOhm
R2739 0Ohm
R2740 10KOhm
R2757 10KOhm
R2758 10KOhm
R2744 100KOhm
R2708 100KOhm
R2788 100KOhm
R2755 10KOhm
R2750 10KOhm
R2706 1KOhm
R2759 10KOhm
R2734 10KOhm
PCB_VID 0 1 2
F6V 1.0 0 0 0
R2713 10KOhm
R2714 10KOhm
R2717 10KOhm
R2715 10KOhm
R2716 10KOhm
R2718 10KOhm
Title : SB-ICH9M(3)
ASUSTeK COMPUTER INC. NB1
Engineer: Kent Qi
Size Custom
Project Name F6Ve
Rev 1.0
Date: Friday, September 26, 2008
Sheet 27 of 64


6uA in G3
U2501F
U2501E
2mA
47mA
~1.342A
~11mA
78mA
23mA
80mA
1mA
646mA
48mA
308mA
11mA
212mA
73mA
VccSus1_05, VccSus1_5, & VccCL1_5
VccLAN1_05 & VccCL1_05
Title : SB-ICH9M(PWR)
ASUSTeK COMPUTER INC. NB1
Engineer: Kent Qi
Project Name F6Ve
Size Custom
Rev 1.0
Date: Friday, September 26, 2008
Sheet 28 of 64


+3V_LAN
R2925 0Ohm
40 mil
+VDDSR
ENSR
R2926 0Ohm
+3V_LAN
C2939 22UF/6.3V
C2940 0.1UF/10V
L2907 4.7UH
SROUT12
R2923 0Ohm
FB12
close to pin1 with in 200 mil
60 mil
+V1.2_LAN
C2932 22UF/6.3V
C2941 0.1UF/10V
0909
R2900 0Ohm
+AVDD12
C2945 C2944 C2943 C2942 0.1UF/10V
R2901 0Ohm
+EVDD12
C2946 C2947 0.1UF/10V
40mil
R2966 0Ohm r0603_h24
+DVDD12
C2951 C2950 C2953 C2952 C2949 C2948 0.1UF/10V
X2_LAN
X1_LAN
+AVDD33
2.49KOhm R2903
+DVDD12
+3V_LAN
RTLAN_DSM# ---> GPIO10 of ICH9
RTLAN_DSM_EN --> GPIO60 of ICH9
Reserved DSM Function
+AVDD12
+AVDD12
+AVDD33
T2903
+3V_LAN
R2918 3.6KOhm
U2901
SROUT12
FB12
[22] L_TRDP0
[22] L_TRDM0
[22] L_TRDP1
[22] L_TRDM1
[22] L_TRDP2
[22] L_TRDM2
[22] L_TRDP3
[22] L_TRDM3
+3V_LAN
RTL8111C_VC_GR
R2928 0Ohm
RTLAN_DSM# [27]
+3VS
R2929 0Ohm @
R2902 1KOhm
R2904 15KOhm
Q2906 2N7002
RTLAN_DSM_EN [27]
CLK_REQ_LAN# [7]
R2910 0Ohm @
+3VSUS
L2934 80Ohm/100Mhz I0805_h43 Irat=2A
40 mil
C2927 22UF/6.3V
+3V_LAN
C2955 C2954 C2957 C2956 0.1UF/10V
40mil
R2927 0Ohm
+AVDD33
C2959 C2958 0.1UF/10V
[20,22,27,33] PCIE_WAKE#
+EVDD12
close to LAN CHIP
E_GND
[17,20,21,26] PCI_RST#
R2907 @ 0Ohm
T2901
T2902
PCIE_RXN6_C
PCIE_RXP6_C
C2902 0.1UF/10V
C2901 0.1UF/10V
PCIE_RXN6_GLAN [26]
PCIE_RXP6_GLAN [26]
CLK_PCIE_LAN# [7]
CLK_PCIE_LAN [7]
PCIE_TXN6_C [26]
PCIE_TXP6_C [26]
R2908 0Ohm
[6,22,26,33,34,38] BUF_PLT_RST#
Q2907 2N7002
R2911 10KOhm @
+3V
+3VSUS
X2_LAN
R2924 0Ohm
X1_LAN
X2901 25Mhz
C2933 27PF/50V
C2934 27PF/50V
R2922 0Ohm
R2921 0Ohm
E_GND
Title : GigaLAN
ASUSTeK COMPUTER INC. NB1
Engineer: Kent Qi
Size Custom
Project Name F6Ve
Rev 1.0
Date: Friday, September 26, 2008
Sheet 29 of 64



<Variant Name>

Title : ESATA

ASUSTeK COMPUTER INC

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

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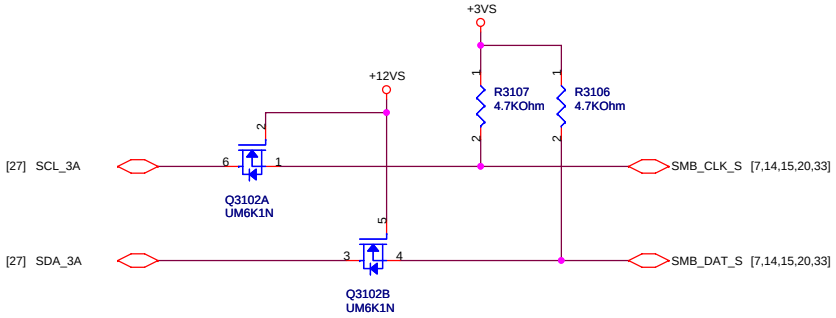
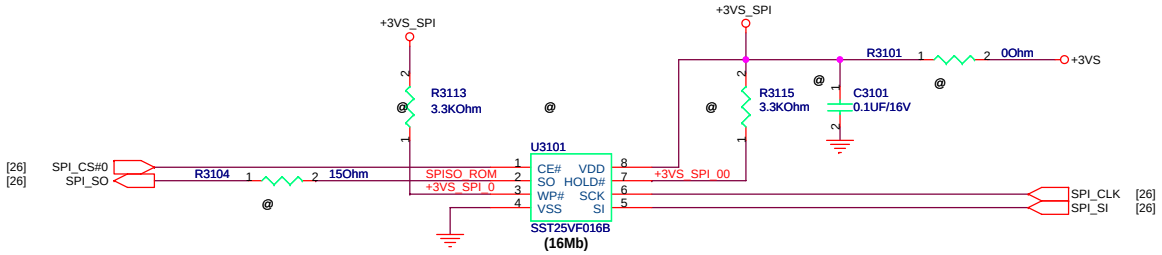




FOR iTPM

ASUSTeK COMPUTER INC. NB1	Title : ICH9M-Other	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 31 of 64	

<Variant Name>

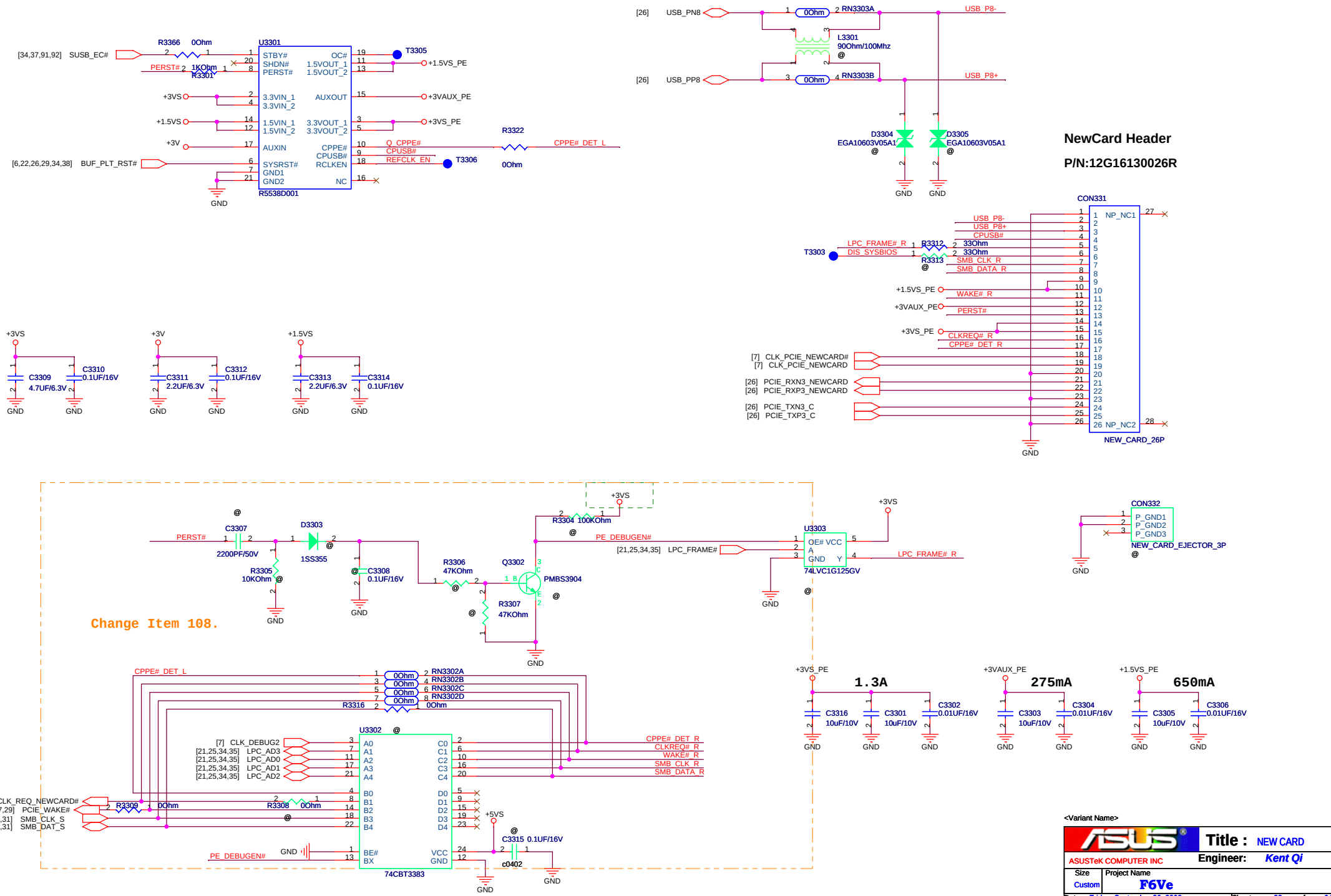
Title : EMPTY

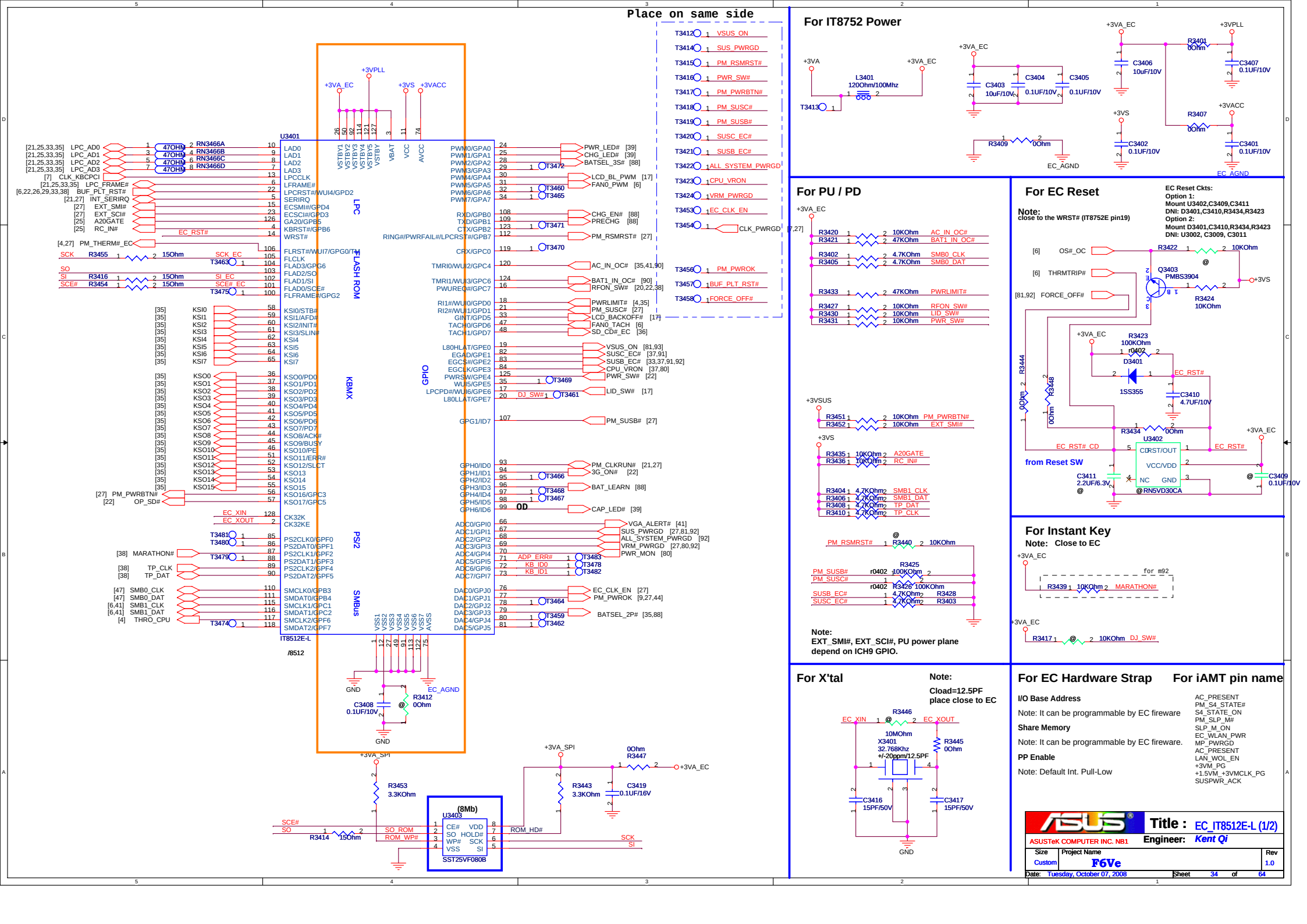
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 32 of 64


U3301
R5538D001
R3366 0Ohm
PERST# 1KOhm R3301
[34,37,91,92] SUSB_EC#
[6,22,26,29,34,38] BUF_PLT_RST#
STBY#
SHDN#
PERST#
SYSRST#
GND1
GND2
OC#
1.5VOUT_1
1.5VOUT_2
AUXOUT
3.3VOUT_1
3.3VOUT_2
CPPE#
CPUSB#
RCLKEN
NC
3.3VIN_1
3.3VIN_2
1.5VIN_1
1.5VIN_2
AUXIN
Q_CPPE#
CPUSB#
REFCLK_EN
T3305
T3306
+1.5VS_PE
+3VAUX_PE
+3VS_PE
+3VS
+1.5VS
+3V
R3322
0Ohm
CPPE# DET L
[26] USB_PN8
[26] USB_PP8
RN3303A
RN3303B
L3301
90Ohm/100Mhz
USB_P8-
USB_P8+
D3304
EGA10603V05A1
D3305
EGA10603V05A1
NewCard Header
P/N:12G16130026R
CON331
NEW_CARD_26P
NP_NC1
NP_NC2
T3303
LPC_FRAME# R
DIS_SYSBIOS
R3312 33Ohm
R3313 33Ohm
SMB_CLK_R
SMB_DATA_R
WAKE# R
PERST#
CLKREQ# R
CPPE# DET R
[7] CLK_PCIE_NEWCARD#
[7] CLK_PCIE_NEWCARD
[26] PCIE_RXN3_NEWCARD
[26] PCIE_RXP3_NEWCARD
[26] PCIE_TXN3_C
[26] PCIE_TXP3_C
C3309 4.7UF/6.3V
C3310 0.1UF/16V
C3311 2.2UF/6.3V
C3312 0.1UF/16V
C3313 2.2UF/6.3V
C3314 0.1UF/16V
GND
Change Item 108.
C3307 2200PF/50V
D3303 1SS355
R3305 10KOhm
C3308 0.1UF/16V
R3306 47KOhm
Q3302 PMBS3904
R3307 47KOhm
R3304 100KOhm
PE_DEBUGEN#
[21,25,34,35] LPC_FRAME#
U3303
74LVC1G125GV
OE# VCC
A
GND Y
LPC_FRAME# R
CON332
NEW_CARD_EJECTOR_3P
P_GND1
P_GND2
P_GND3
CPPE# DET L
RN3302A
RN3302B
RN3302C
RN3302D
R3316 0Ohm
U3302
74CBT3383
[7] CLK_DEBUG2
[21,25,34,35] LPC_AD3
[21,25,34,35] LPC_AD0
[21,25,34,35] LPC_AD1
[21,25,34,35] LPC_AD2
CPPE# DET R
CLKREQ# R
WAKE# R
SMB_CLK_R
SMB_DATA_R
[7] CLK_REQ_NEWCARD#
[20,22,27,29] PCIE_WAKE#
7,14,15,20,31] SMB_CLK_S
7,14,15,20,31] SMB_DAT_S
R3309 0Ohm
R3308 0Ohm
PE_DEBUGEN#
+5VS
C3315 0.1UF/16V
c0402
+3VS_PE
1.3A
C3316 10uF/10V
C3301 10uF/10V
C3302 0.01UF/16V
+3VAUX_PE
275mA
C3303 10uF/10V
C3304 0.01UF/16V
+1.5VS_PE
650mA
C3305 10uF/10V
C3306 0.01UF/16V
<Variant Name>
Title : NEW CARD
ASUSTeK COMPUTER INC
Engineer: Kent Qi
Size Custom
Project Name F6Ve
Rev 1.0
Date: Friday, September 26, 2008
Sheet 33 of 64



For IT8752 Power

For PU / PD

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.

For EC Reset

Note:
close to the WRST# (IT8752E pin19)

EC Reset Ckts:
Option 1:
Mount U3402,C3409,C3411
DNI: D3401,C3410,R3434,R3423
Option 2:
Mount D3401,C3410,R3434,R3423
DNI: U3002, C3009, C3011

For Instant Key

Note: Close to EC

For X'tal

Note:

Cload=12.5PF
place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM, +3VMCLK_PG
SUSPWR_ACK

ASUSTeK COMPUTER INC. NB1

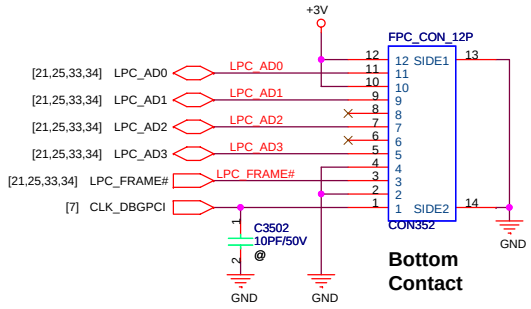
Title : EC_IT8512E-L (1/2)

Engineer: *Kent Qi*

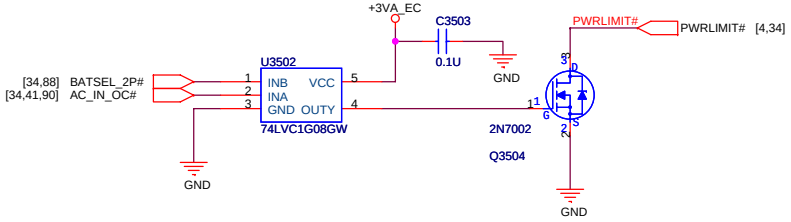
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Tuesday, October 07, 2008 Sheet 34 of 64

For Debug

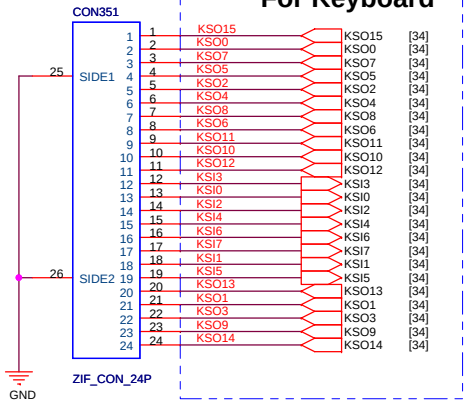


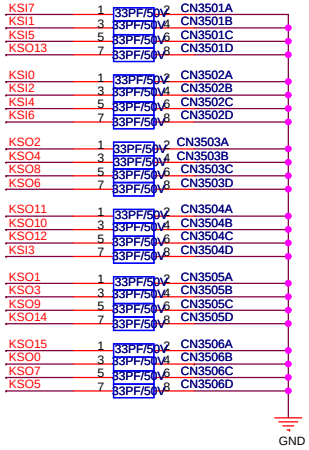
PWRLMT Circuit: For Battery 1P



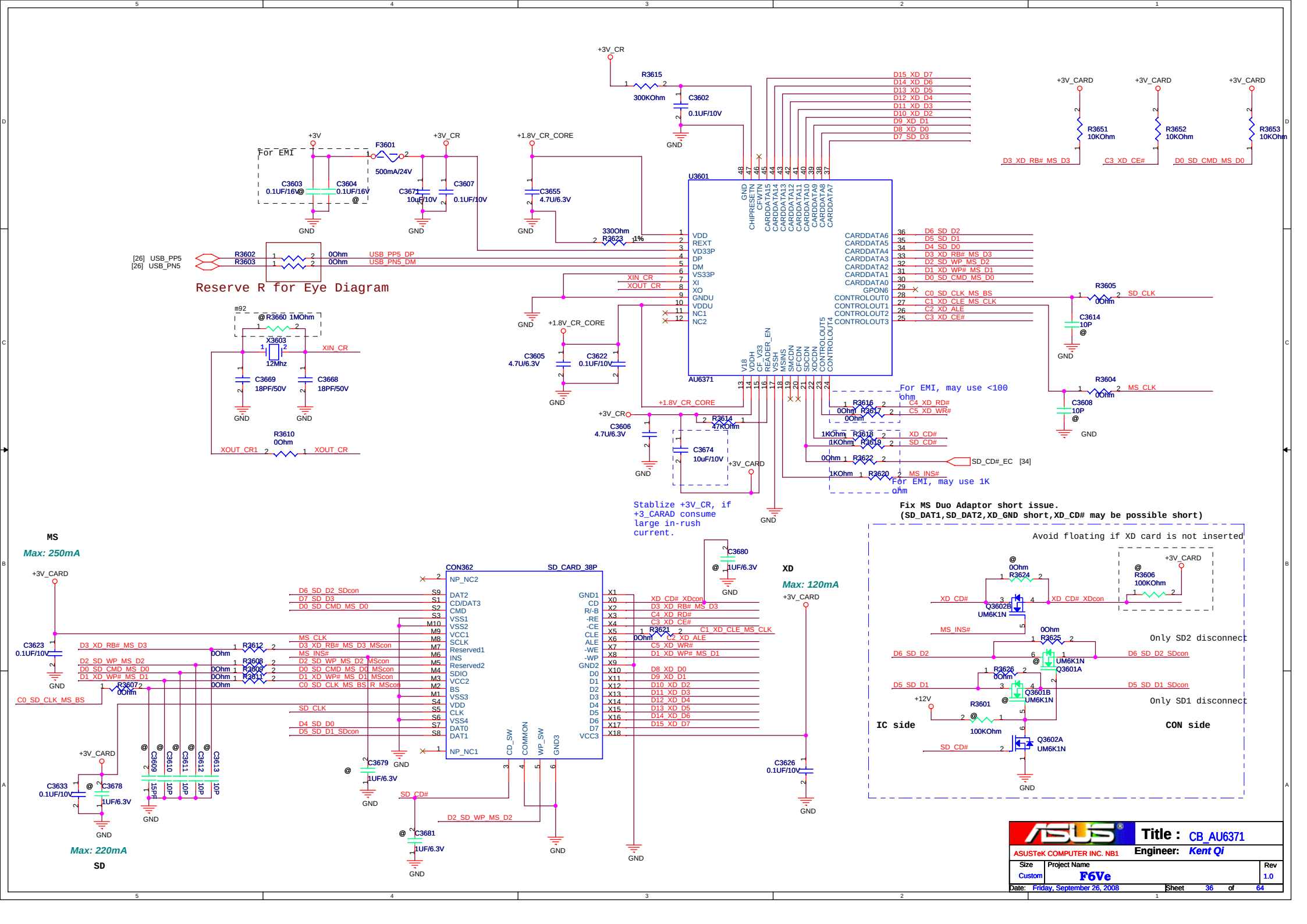
P/N:12G182402404

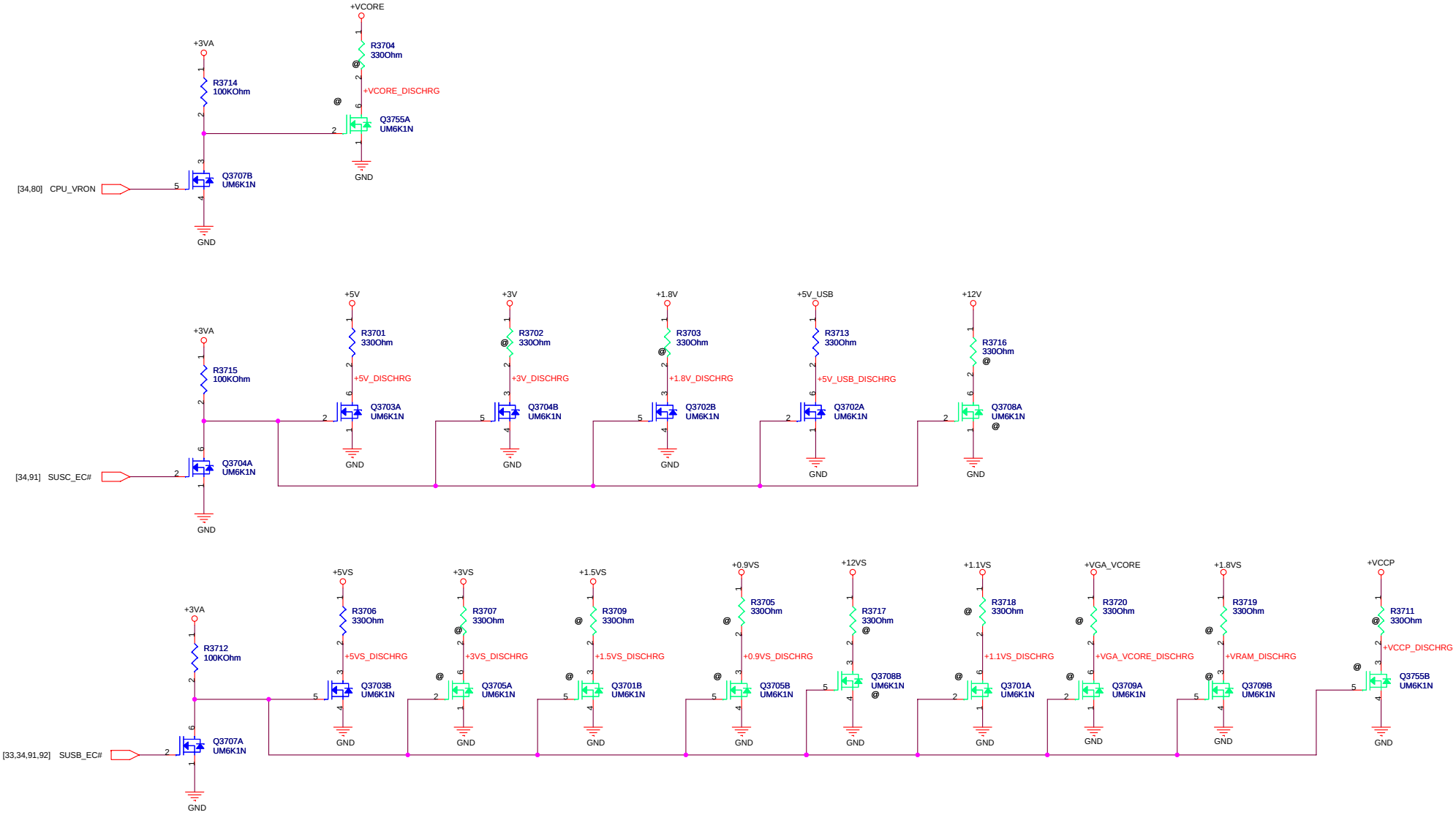
For Keyboard





ASUSTeK COMPUTER INC. NB1	Title : EC_IT8752 (2/2)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 35 of 64	

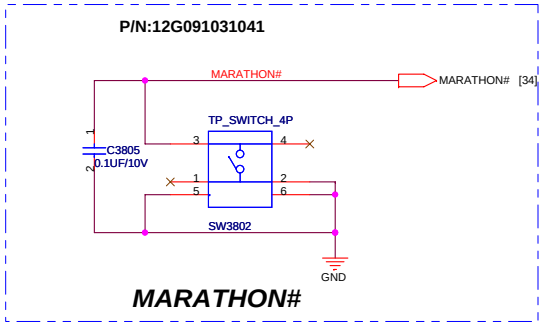

+3V_CR
R3615
300KOhm
C3602
0.1UF/10V
GND
U3601
AU6371
D15_XD_D7
D14_XD_D6
D13_XD_D5
D12_XD_D4
D11_XD_D3
D10_XD_D2
D9_XD_D1
D8_XD_D0
D7_SD_D3
+3V_CARD
R3651
10KOhm
R3652
10KOhm
R3653
10KOhm
D3_XD_RB#_MS_D3
C3_XD_CE#
D0_SD_CMD_MS_D0
+3V
For EMI
F3601
500mA/24V
C3603
0.1UF/16V
C3604
0.1UF/16V
C3671
10uF/10V
C3607
0.1UF/10V
+1.8V_CR_CORE
C3655
4.7U/6.3V
330Ohm
R3623
1%
[26] USB_PP5
[26] USB_PN5
R3602
R3603
0Ohm
USB_PP5_DP
USB_PN5_DM
Reserve R for Eye Diagram
XIN_CR
XOUT_CR
m92
@R3660 1MOhm
X3603
12Mhz
C3669
18PF/50V
C3668
18PF/50V
R3610
0Ohm
XOUT_CR1
C3605
4.7U/6.3V
C3622
0.1UF/10V
C3606
4.7U/6.3V
R3614
47KOhm
C3674
10uF/10V
R3605
0Ohm
SD_CLK
C3614
10P
R3604
0Ohm
MS_CLK
C3608
10P
For EMI, may use <100 ohm
R3616
R3617
0Ohm
C4_XD_RD#
C5_XD_WR#
1KOhm
R3618
R3619
XD_CD#
SD_CD#
0Ohm
R3622
SD_CD#_EC [34]
1KOhm
R3620
MS_INS#
For EMI, may use 1K ohm
Stablize +3V_CR, if +3_CARAD consume large in-rush current.
Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)
Avoid floating if XD card is not inserted
MS
Max: 250mA
XD
Max: 120mA
SD
Max: 220mA
CON362
SD_CARD_38P
NP_NC2
NP_NC1
DAT2
CD/DAT3
CMD
VSS1
VCC1
SCLK
Reserved1
INS
Reserved2
SDIO
VCC2
BS
VSS3
VDD
CLK
VSS4
DAT0
DAT1
CD_SW
COMMON
WP_SW
GND3
GND1
CD
R/-B
-RE
CE
CLE
ALE
-WE
-WP
GND2
VCC3
C3623
0.1UF/10V
C3680
1UF/6.3V
C3679
1UF/6.3V
C3681
1UF/6.3V
C3633
0.1UF/10V
C3678
1UF/6.3V
C3626
0.1UF/10V
C3609
C3610
C3611
C3612
C3613
15PF
10P
R3607
R3612
R3608
R3609
R3611
0Ohm
R3621
C1_XD_CLE_MS_CLK
C2_XD_ALE
R3624
R3606
100KOhm
R3625
R3626
R3601
100KOhm
Q3602B
UM6K1N
Q3601A
UM6K1N
Q3601B
UM6K1N
Q3602A
UM6K1N
Only SD2 disconnect
Only SD1 disconnect
IC side
CON side
+12V
Title : CB_AU6371
ASUSTeK COMPUTER INC. NB1
Engineer: Kent Qi
Size: Custom
Project Name: F6Ve
Rev: 1.0
Date: Friday, September 26, 2008
Sheet 36 of 64

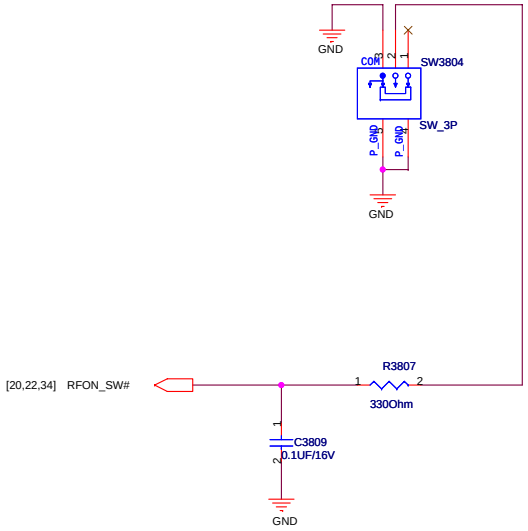


<Variant Name>

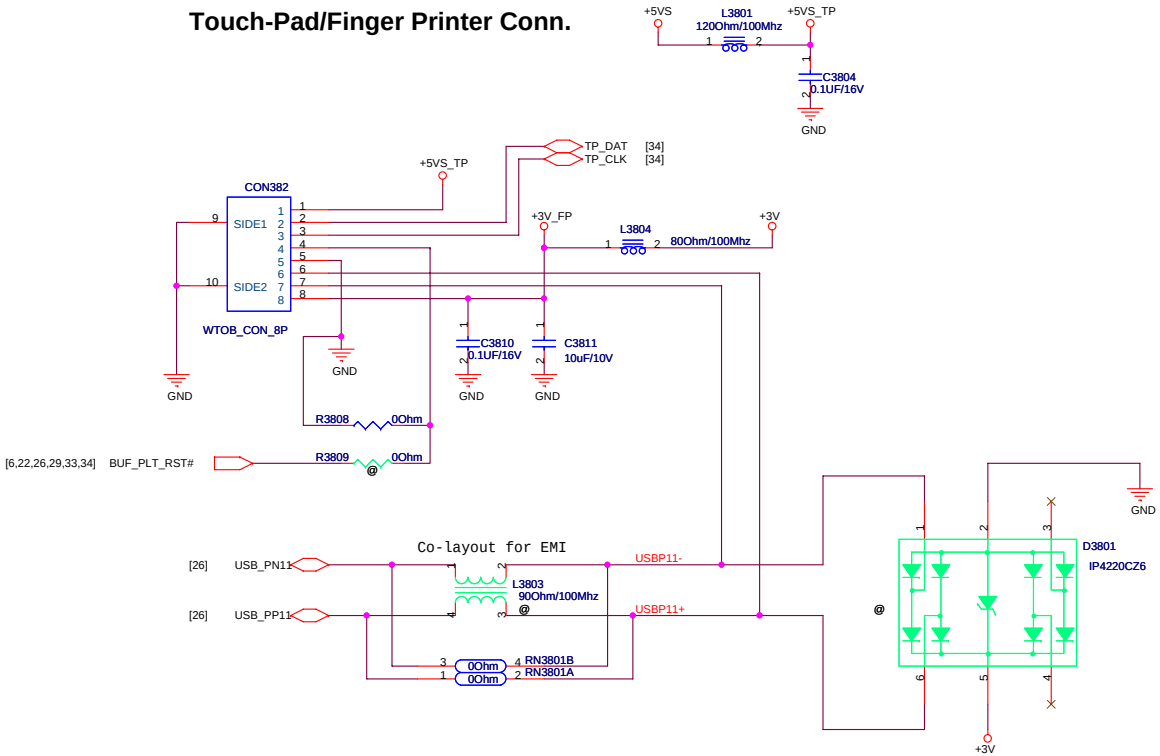
ASUSTeK COMPUTER INC	Title : DISCHARGE	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 37 of 64	

BT/WLAN SW





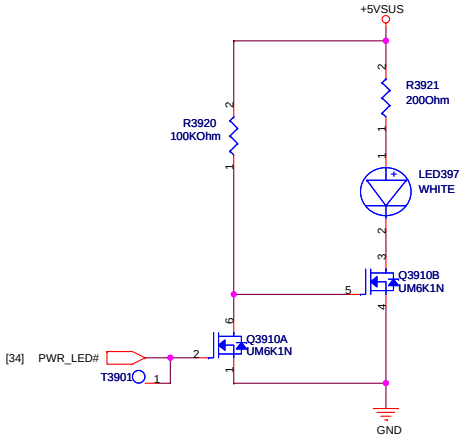
Touch-Pad/Finger Printer Conn.



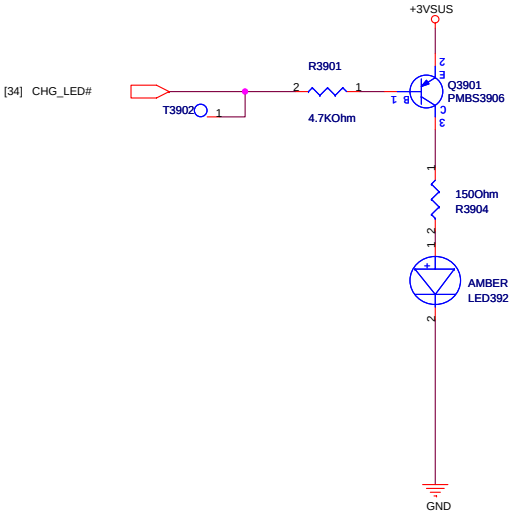
<Variant Name>

ASUSTeK COMPUTER INC	Title : KEY & LED	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 38 of 64	

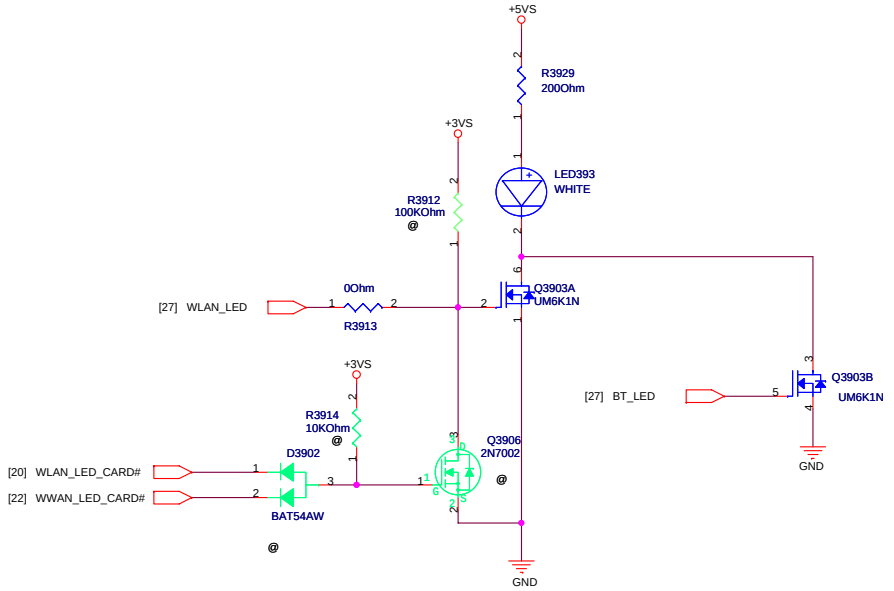
PWR LED



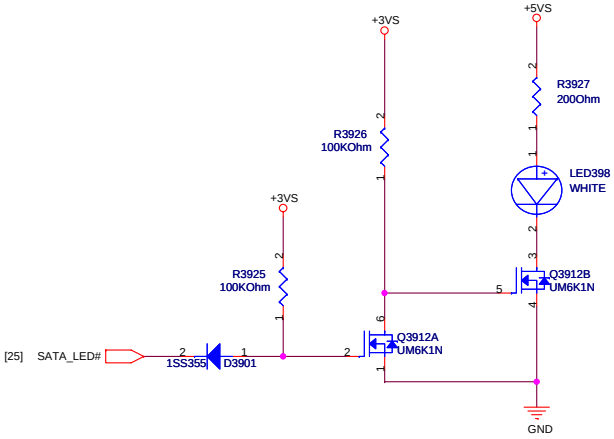
BATTERY LED



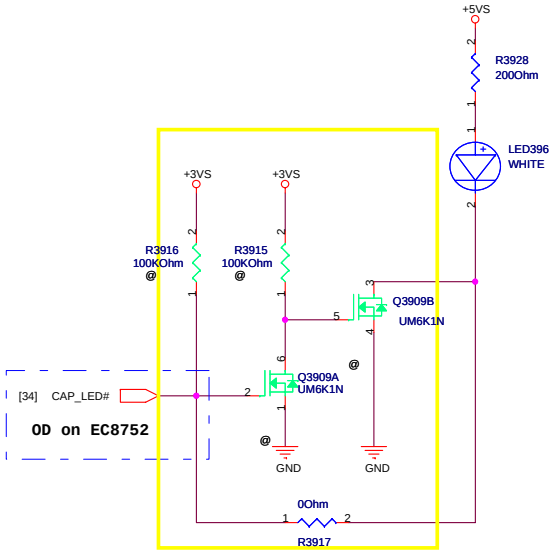
WireLess/BT LED



SATA LED

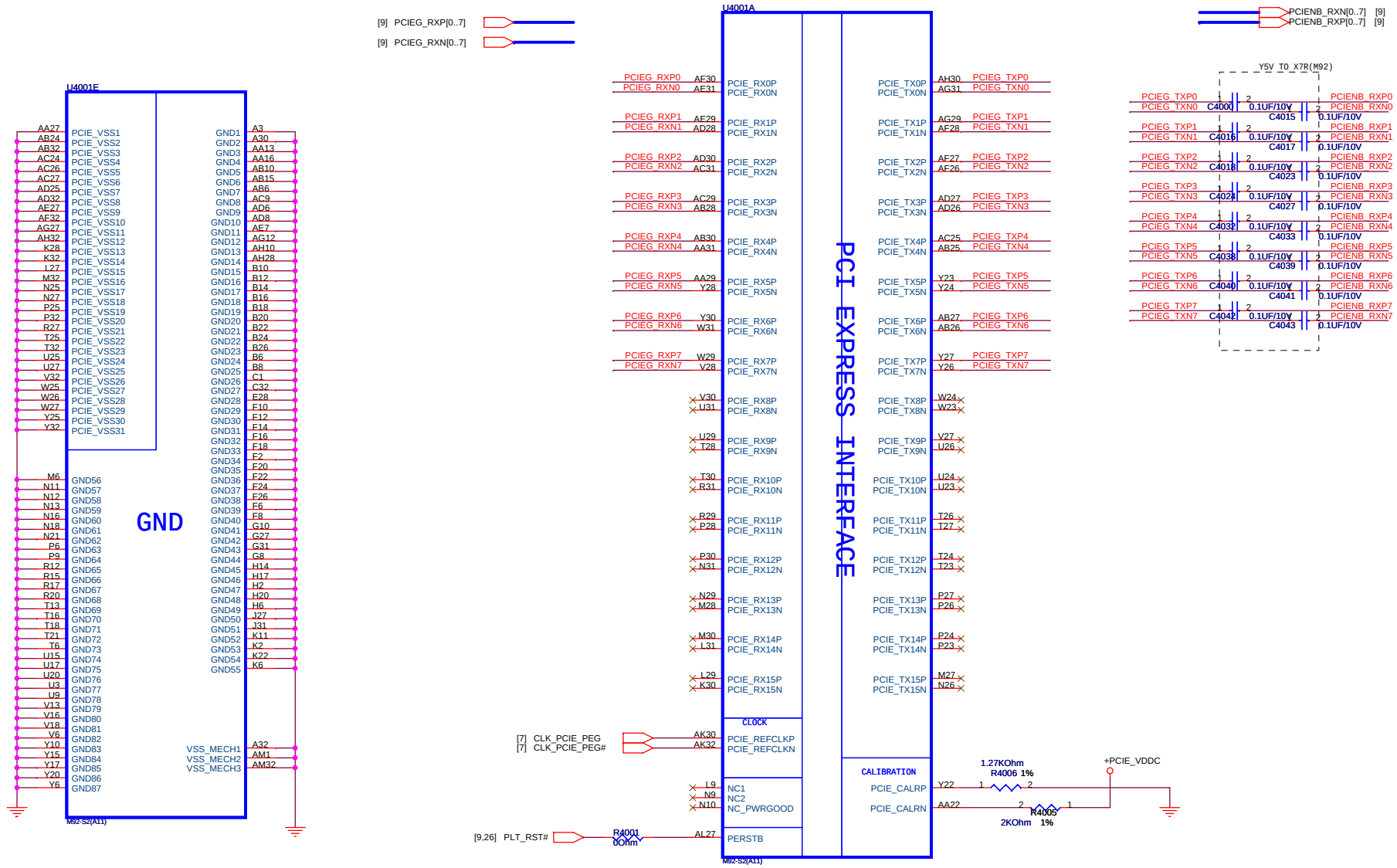


Cap. Lock



<Variant Name>

ASUSTeK COMPUTER INC	Title : LEDs	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 39 of 64	



<Variant Name>

ASUSTeK COMPUTER INC	Title : M92S2-PCIE(1)	
	Engineer: Kent Qi	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 40 of 64	

Close to U4001

37.5 ohm

55 ohm

@ JP4101 SHORT_PIN
CRT_M92_RED_S
150Ohm R4170 1%
CRT_RED [18]

@ JP4102 SHORT_PIN
CRT_M92_GREEN_S
150Ohm R4171 1%
CRT_GREEN [18]

@ JP4103 SHORT_PIN
CRT_M92_BLUE_S
150Ohm R4172 1%
CRT_BLUE [18]

GND

VRAM SIZE

+3VSG_DELAY

R4125 10KOhm r0402
R4133 10KOhm r0402 @
R4131 10KOhm r0402
VGA_GPIO13
VGA_GPIO12
VGA_GPIO11
R4132 10KOhm r0402
R4126 10KOhm r0402
R4169 10KOhm r0402

GND

GPIO[13:11] = 001, 256M memory aperture(default)
GPIO[13:11] = 100, 512M memory aperture

Memory ID

+1.8VS
R4188 0Ohm

R4127 10KOhm r0402 @
R4128 10KOhm r0402 @
R4129 10KOhm r0402 @
R4130 10KOhm r0402 @
VGAMEM_ID0
VGAMEM_ID1
VGAMEM_ID2
VGAMEM_ID3
R4134 10KOhm r0402
R4135 10KOhm r0402
R4136 10KOhm r0402
R4137 10KOhm r0402

GND

ID 0: Qimonda 64Mx16 A Channel(512M)
ID 8: SAMSUNG 64Mx16 A Channel(512M)

GPIO[0]: Tx Power Savings Enable
0: 50% Tx output swing (INT PD)
1: full Tx output swing

GPIO[1]: Tx De-emphasis Enable
0: Tx de-emphasis disbale(INT PD)
1: Tx de-emphasis enable.

GPIO2 for PCIE 2.5G/5G select.(L:2.5G default)

GPIO6 for Power control signals
GPIO8&GPIO9 for Serial ROM

GPIO19 VGA Thermtrip out(110 degree active)

+3VSG_DELAY
R4140 10KOhm VGA_GPIO
R4142 10KOhm VGA_GPIO
PCIE_GPIO2
R4145 @ 10KOhm VGA_GPIO6
R4156 @ 10KOhm VGA_GPIO8
R4146 @ 10KOhm VGA_GPIO9
R4147 @ 10KOhm PWRCNTL_0
R4148 @ 10KOhm PWRCNTL_1
R4149 @ 10KOhm VGA_GPIO19
R4158 @ 10KOhm GPIO_TRSTB
R4161 @ 10KOhm GPIO_23_CLKREQB
0918
R4150 1 10KOhm 2 VGA_BBEN
R4159 1 10KOhm 2 GPIO_TRSTB
R4160 1 10KOhm 2 PCIE_GPIO2
0916
GND

PWRCNTL_0	PWRCNTL_1	+VGA_VCORE_O
L	L	1.20V
H	L	1.10V
L	H	1.00V
H	H	0.90V

HSYNC	VSYNC	Function
L	L	No audio Function
L	H	Displayport and HDMI if adapter is detected
H	L	Displayport only
H	H	Both Displayport and HDMI

Shunt R 180ohm for M7X

U4001B

MUTI GFX

DPA
TXCAP_DPA3P AF2
TXCAM_DPA3N AF4
TMDS_TXCP [19]
TMDS_TXCN [19]
TX0P_DPA2P AG3
TX0M_DPA2N AG5
TMDS_TX0P [19]
TMDS_TX0N [19]
TX1P_DPA1P AH3
TX1M_DPA1N AH1
TMDS_TX1P [19]
TMDS_TX1N [19]
TX2P_DPA0P AK3
TX2M_DPA0N AK1
TMDS_TX2P [19]
TMDS_TX2N [19]

DPB
TXCBP_DPB3P AK5
TXCBM_DPB3N AM3
TX3P_DPB2P AK6
TX3M_DPB2N AM5
TX4P_DPB1P AJ7
TX4M_DPB1N AH6
TX5P_DPB0P AK8
TX5M_DPB0N AL7

T4105 T4106 T4103 T4107 T4104 T4108
DVPCNTL_MVP_0 AA1
DVPCNTL_MVP_1 Y4
DVPCNTL_0 AC7
DVPCNTL_1 Y2
DVPCNTL_2 U5
DVPCLK U1
DVPDATA_0 Y1
DVPDATA_1 V2
DVPDATA_2 Y3
DVPDATA_3 V4
DVPDATA_4 AB7
DVPDATA_5 W1
DVPDATA_6 AB8
DVPDATA_7 W3
DVPDATA_8 AB9
DVPDATA_9 W5
DVPDATA_10 AC6
DVPDATA_11 W6
DVPDATA_12 AD7
DVPDATA_13 AA3
DVPDATA_14 AC8
DVPDATA_15 AA5
DVPDATA_16 AE8
DVPDATA_17 AA6
DVPDATA_18 AE9
DVPDATA_19 AB4
DVPDATA_20 AD9
DVPDATA_21 AB2
DVPDATA_22 AC10
DVPDATA_23 AC5

T4110 PANEL_ID0
T4111 PANEL_ID1

0998
VGAMEM_ID0
VGAMEM_ID1
VGAMEM_ID2
VGAMEM_ID3

I2C
SCL
SDA

[17] EDID_CLK
[17] EDID_DAT
+3VSG 4.7KOhm R4115 R1
+3VSG 4.7KOhm R4116 R3

GENERAL PURPOSE I/O

GPIO_0 U6
GPIO_1 U10
GPIO_2 T10
GPIO_3_SMBDATA U8
GPIO_4_SMBCLK U7
GPIO_5_AC_BATT T9
GPIO_6 T8
GPIO_7_BLON T7
GPIO_8_ROMSO P10
GPIO_9_ROMSI P4
GPIO_10_ROMSCK P2
GPIO_11 N6
GPIO_12 N5
GPIO_13 N3
GPIO_14_HPD2 Y9
GPIO_15_PWRCNTL_0 N1
GPIO_16_SSIN M4
GPIO_17_THERMAL_INT R6
GPIO_18_HPD3 W10
GPIO_19_CTF M2
GPIO_20_PWRCNTL_1 P8
GPIO_21_BB_EN P7
GPIO_22_ROMCSB N8
GPIO_23_CLKREQB N7
GPIO_29_DRM_0 T11
GPIO_30_DRM_1 R11

AC_BATT_Detect
VGA_GPIO0 INT_PD
VGA_GPIO1 INT_PD
PCIE_GPIO2
[17] L_BKLTEN_V
VGA_GPIO8 INT_PD
VGA_GPIO9 INT_PD
VGA_GPIO11 INT_PD
VGA_GPIO12 INT_PD
VGA_GPIO13 INT_PD
[85,92] VGA_PWRGD
[85] PWRCNTL_0
[7] ATI27M_SSC
R4193 @0Ohm
INT_PD
VGA_ALERT# @0Ohm R4120
VGA_THERM R4119 @0Ohm VGA_TEMP_FAIL#
[85] PWRCNTL_1
[44] VGA_BBEN
VGA_BBEN T4131
VGA_GPIO22 INT_PD
GPIO_23_CLKREQB INT_PD
GPIO_TRSTB
T4136 GPIO_TDI
T4137 GPIO_TCK
T4138 GPIO_TMS
T4139 GPIO_TDO
1KOhm R4151
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TESTEN
T4141 GEN_B INT_PD
T4143 GEN_D HPD4
[19] HDMI_HP
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
HPD1

DAC1
R AM26 CRT_M92_RED_S
RB AK26
R4103 0Ohm GND
G AL25 CRT_M92_GREEN_S
GB AJ25
R4104 0Ohm GND
B AH24 CRT_M92_BLUE_S
BB AG25
R4105 0Ohm GND
HSYNC AH26 CRT_HSYNC [18]
VSYNC AJ27 CRT_VSYNC [18]
10KOhm @ R4110 1
10KOhm R4108 1
+3VSG_DELAY
RSET AD22 DAC_RSET 1 R4109 1% 499Ohm GND
AVDD AG24 +1.8VS_AVDD
AVSSQ AE22 GND
VDD1DI AE23 +1.8VS_VDD1DI
VSS1DI AD23 GND

DAC2
R AM12
R2B AK13
G AL11
G2B AJ11
B AK10
B2B AL9
C AH12
Y AM10
COMP AJ9
H2SYNC AL13
V2SYNC AJ13
10KOhm @ R4112 1
+3VSG_DELAY
VDD2DI AD19 +1.8VS_VDD2DI
VSS2DI AC19 GND
A2VDD AE20 +3VSG_A2VDD
A2VDDQ AE17 +1.8VS_A2VDDQ
A2VSSQ AE19 GND
R2SET AG13 2 R4111 1% 715Ohm GND

PLL/CLOCK
DPLL_PVDD AE14
DPLL_PVSS AE14
DPLL_VDDC AD14
XTALIN AM28
XTALOUT AK28
[7] ATI27M_NOSSC
+DPLL_VDDC 150Ohm R4155 1%
R4196 121Ohm 1%
T4146
VREFG AC16
R4152 499Ohm 1% r0402
VGA_VREFG
R4154 249Ohm 1% r0402
C4103 0.1UF/16V c0402
GND

DDC/AUX
DDC1CLK AE6
DDC1DATA AE5
CRT_DDC_CLK [18]
CRT_DDC_DATA [18]
AUX1P AD2
AUX1N AD4
DDC2CLK AC11
DDC2DATA AC13
HDMI_DDC_CLK [19]
HDMI_DDC_DATA [19]
AUX2P AD13
AUX2N AD11
RSVD2 AB22
RSVD3 AC22
DDCCLK_AUX5P AE16
DDCDATA_AUX5N AD16
DDC5CLK AC1
DDC5DATA AC3
DDCCLK_AUX7P AD20
NC_DDCDATA_AUX7N AC20

THERMAL
DPLUS T4
DMINUS T2
TS_FDO R5
TSVDD AD17
TSVSS AC17
VGA_THERM_DA
VGA_THERM_DC
+TSVDD
GND

M92-S0(A11)

+1.8VS_AVDD
L4101 120Ohm/100Mhz +1.8VS 70mA
C4145 0.1UF/10V
C4144 1UF/6.3V
C4141 10uF/10V
+1.8VS_VDD2DI
R4106 0Ohm
L4102 120Ohm/100Mhz +1.8VS 40mA
C4147 0.1UF/10V
C4146 1UF/6.3V
C4142 10uF/10V
GND

+3VSG_A2VDD
L4103 120Ohm/100Mhz +3VSG 65mA
C4149 0.1UF/10V
C4148 1UF/6.3V
C4143 10uF/10V
+1.8VS_A2VDDQ
L4104 120Ohm/100Mhz +1.8VS 1mA
C4152 0.1UF/10V
C4150 1UF/6.3V
C4151 10uF/10V
GND

+1.8VS
L4105 120Ohm/100Mhz 40mA/120mA
C4160 10uF/10V
C4154 1UF/6.3V
C4155 0.1UF/10V
+DPLL_PVDD
GND

+3VSG_DELAY
R4157 10KOhm
AC_BATT_Detect
Q4103 2N7002
[34,35,90] AC_IN_OC#
GND

+1.8VS
L4107 120Ohm/100Mhz 20mA
C4156 10uF/10V
C4175 1UF/6.3V
C4161 0.1UF/10V
+TSVDD
GND

+1.1VS
L4108 120Ohm/100Mhz 100mA/300mA
C4153 10uF/10V
C4176 1UF/6.3V
C4164 0.1UF/10V
+DPLL_VDDC
GND

Spread Spectrum

+3VSG
L4133 120Ohm/100Mhz
+3VS_SS
C4101 2.2UF/6.3V
C4102 0.01UF/16V
GND
R4101 0Ohm r0402
+3VS_SS
VGA_SRS
R4107 0Ohm r0402
GND
R4114 0Ohm r0402
U4102 P1819B_08SR
ATI27M_NOSSC
VGA_SRS
ATI27M_SSC
XIN XOUT
VSS VDD
SRS PDI#
ModOUT REF
ATI_27M
R4117 220HM r0603_h24
R4119 121Ohm r0603_h24

VGA_THERM_DA
C4118 1000P
VGA_THERM_DC
not enable
[34] VGA_ALERT#
R4198 4.7KOhm
+3VSG

+3VSG_VGTM
R4166 200 +3VSG
C4162 0.1UF/10V
GND

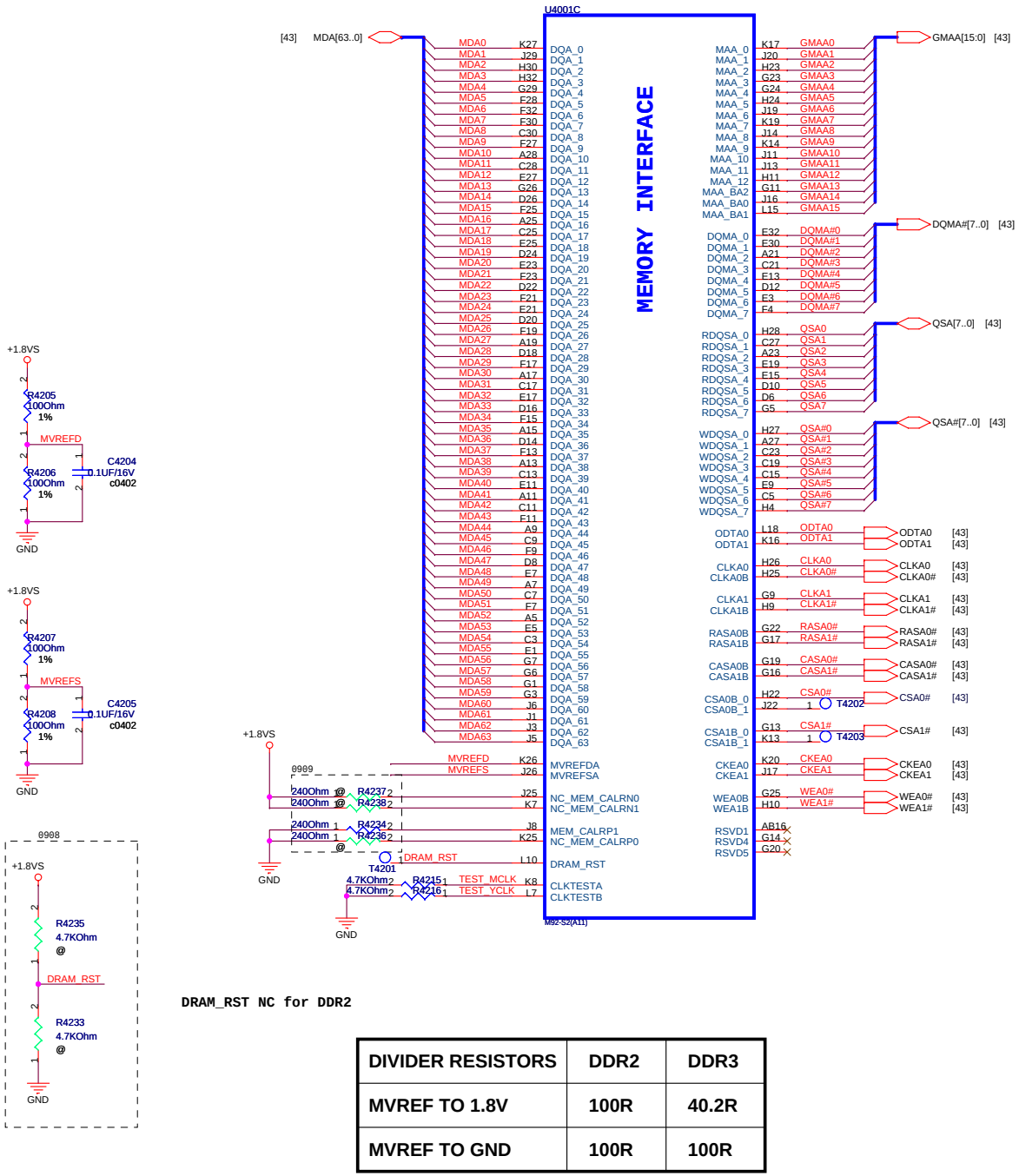
Slave Address:9A

U4105 G781-1
VCC SCLK
DXP SDA
DXN ALERT#
OVERT# GND
OD
VGA_THERM_DA
VGA_THERM_DC
SMB1_CLK [6,34]
SMB1_DAT [6,34]
VGA_THERM#
R4189 4.7KOhm
+3VSG
GND

<Variant Name>

ASUSTeK COMPUTER INC

Title : M92S2-Main(2)
Engineer: Kent Qi
Size: Custom
Project Name: F6Ve
Rev: 1.0
Date: Friday, September 26, 2008
Sheet 41 of 64



DRAM_RST NC for DDR2

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

<Variant Name>

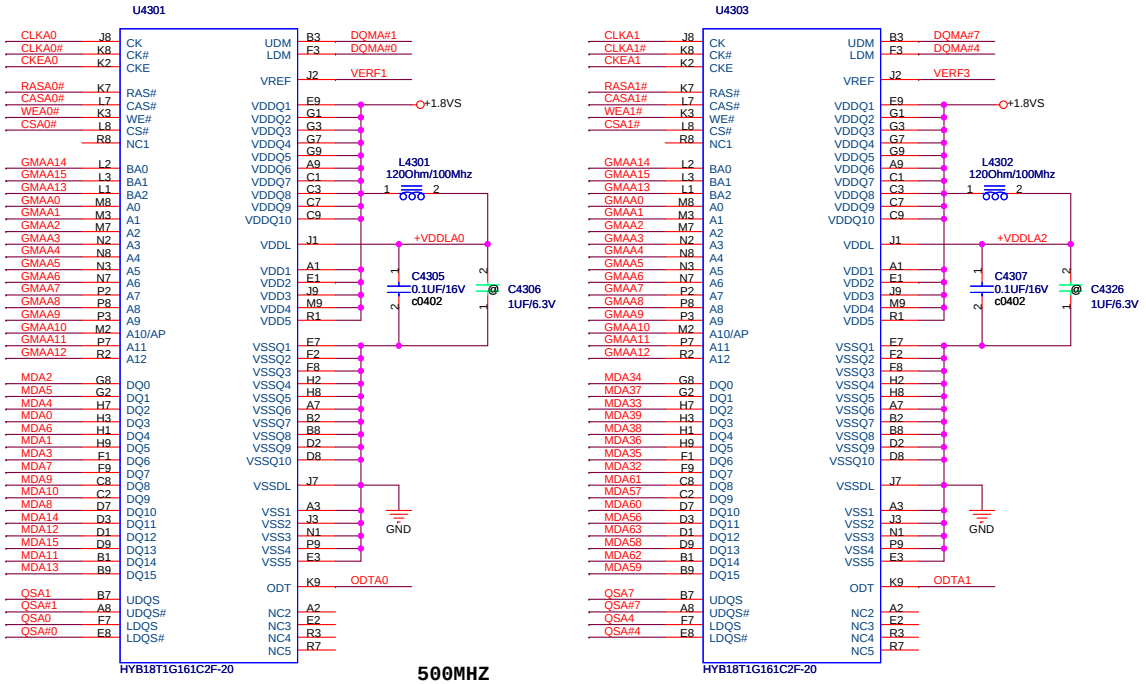
Title : M92S2-MEM CTRL(3)

ASUSTeK COMPUTER INC

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

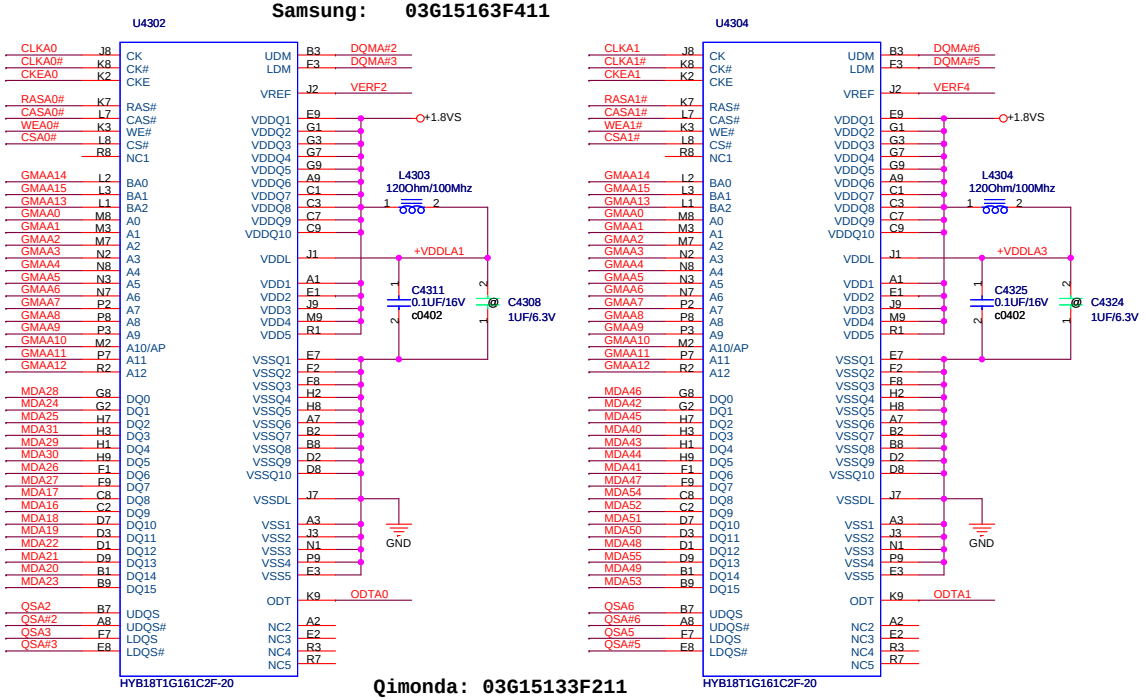
Date: Friday, September 26, 2008 Sheet 42 of 64



500MHZ

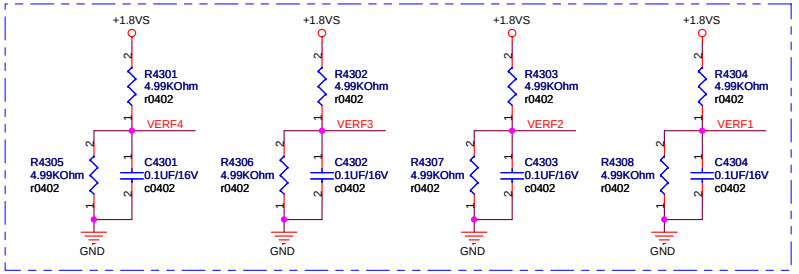
Qimonda: 03G15163F510

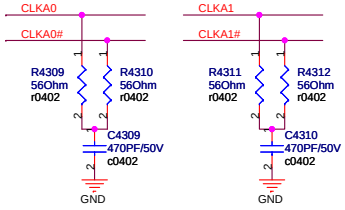
Samsung: 03G15163F411

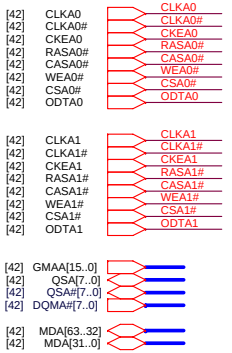


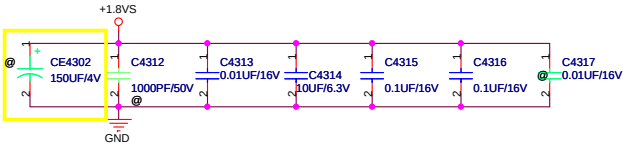
Qimonda: 03G15133F211

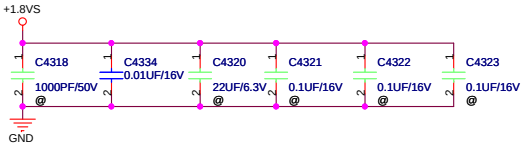
Hynix: 03G15133F114

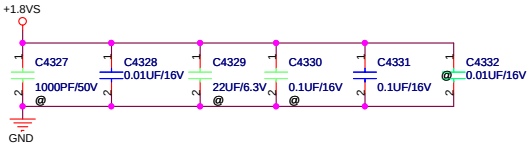


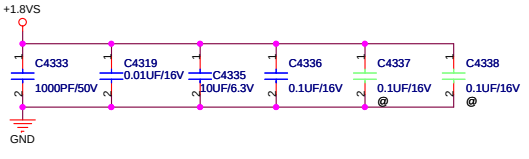












<Variant Name>

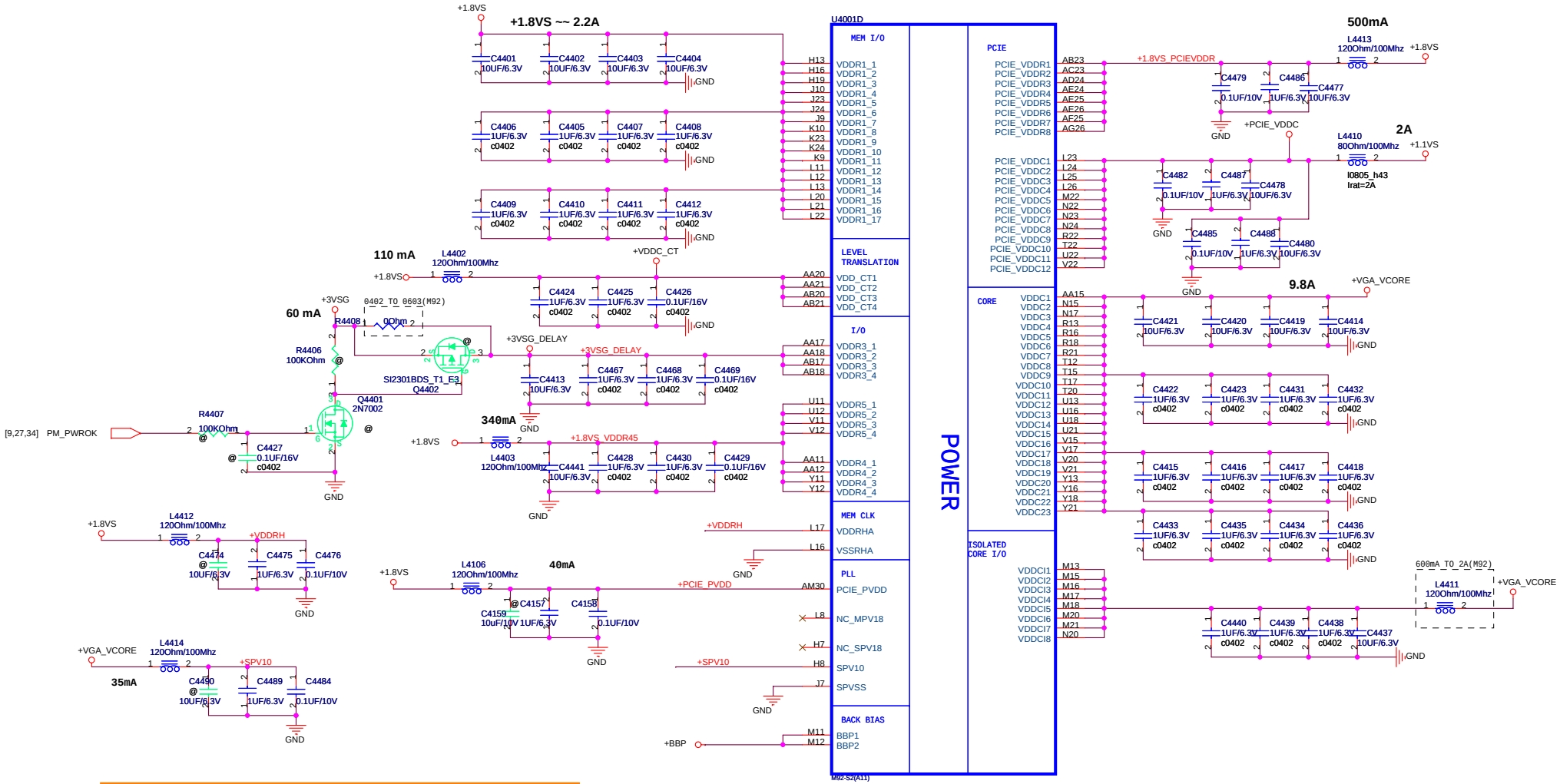
ASUSTeK COMPUTER INC

Title : M92S2-MEM VRAM(4)

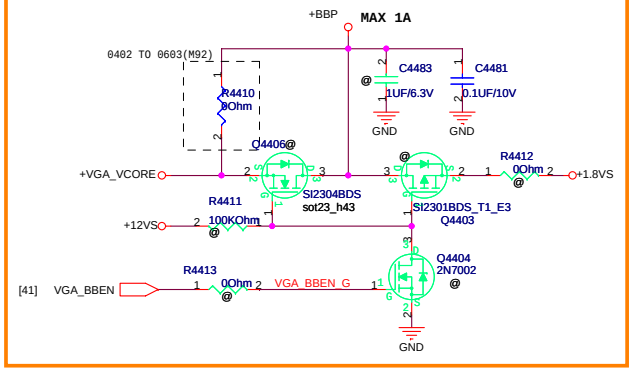
Engineer: Kent Qi

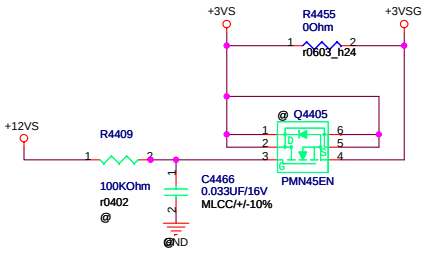
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 43 of 64



BBN could tie to GND directly for ATI suggestion.
Thus, MAX1673ESA could be save.





<Variant Name>

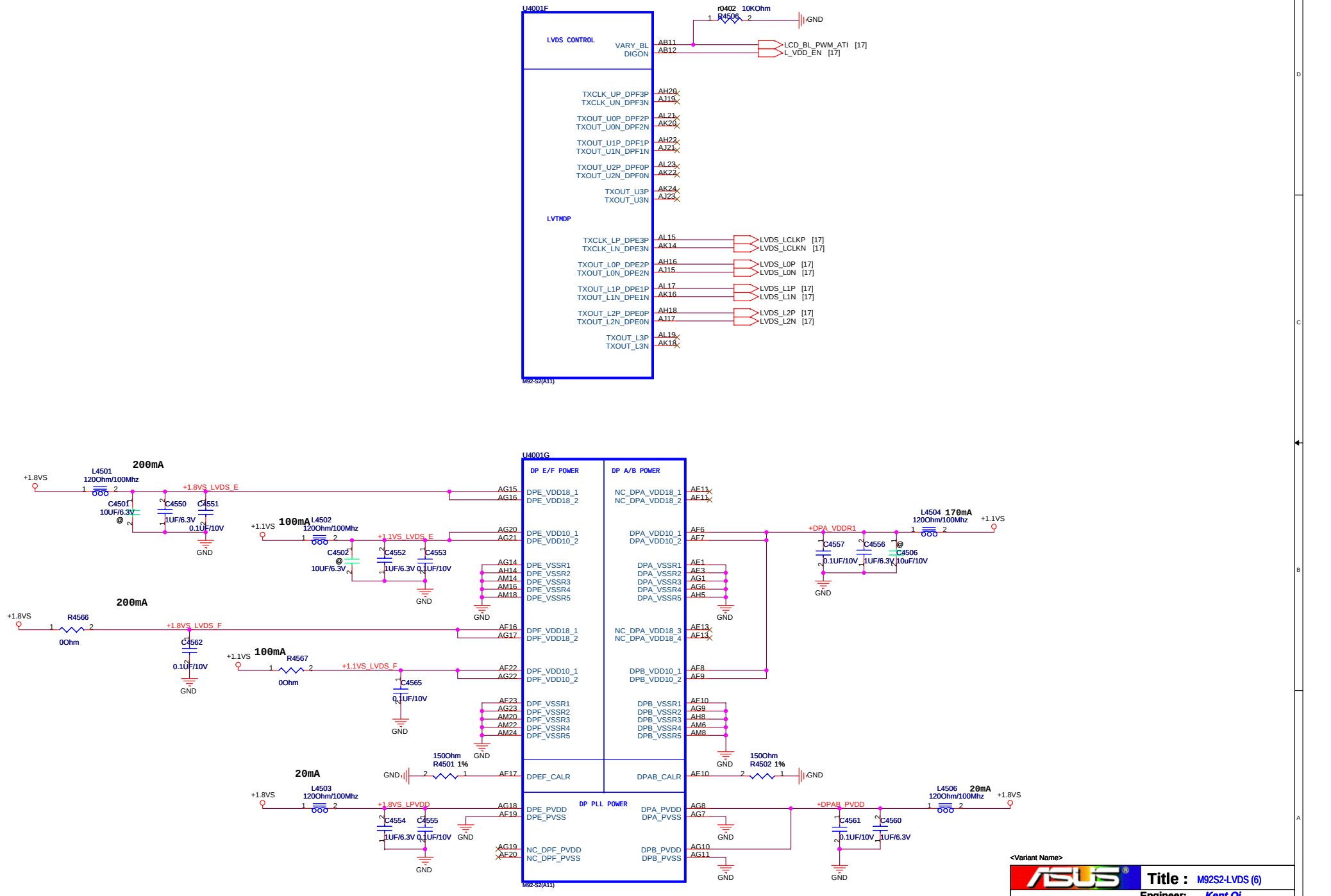
ASUSTeK COMPUTER INC

Title : M92S2-PWR (5)

Engineer: Kent Qi

Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 44 of 64



<Variant Name>

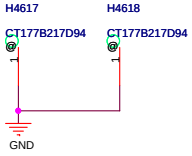
ASUSTeK COMPUTER INC

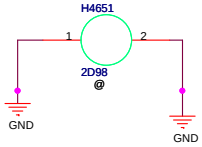
Title : M92S2-LVDS (6)

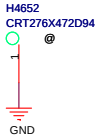
Engineer: Kent Qi

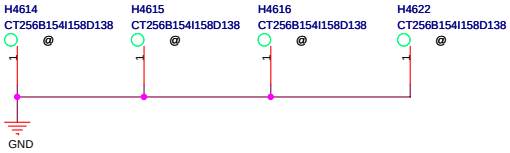
Size	Project Name	Rev
Custom	F6Ve	1.0

Date: Friday, September 26, 2008 Sheet 45 of 64



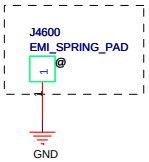


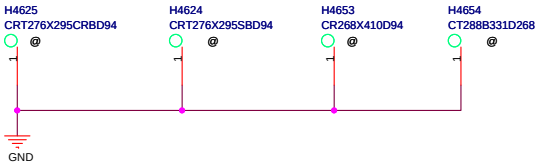


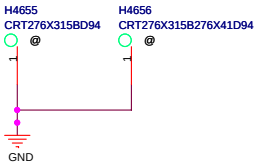


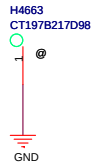
EMI SPRING

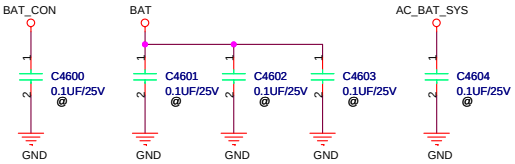
F2J SPRING(H:4.7mm)

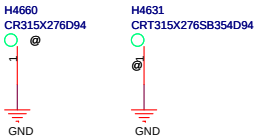


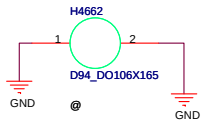


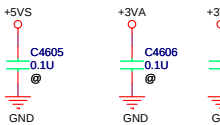


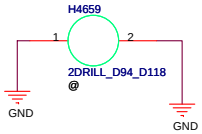


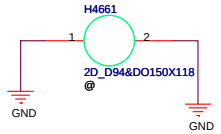


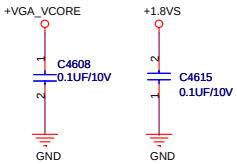


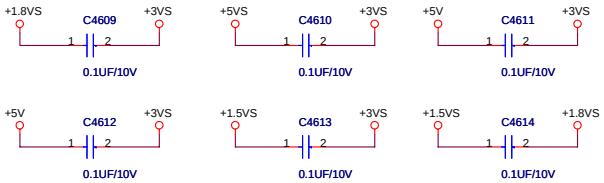












<variant_name>

ASUSTeK COMPUTER INC

Title : SCREW HOLE

Engineer:

Size	Project Name	Rev
Custom	F6Ve	1.0

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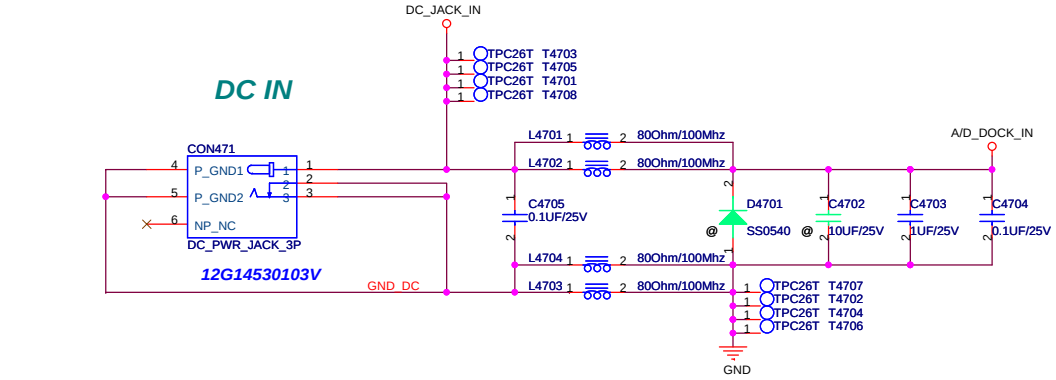

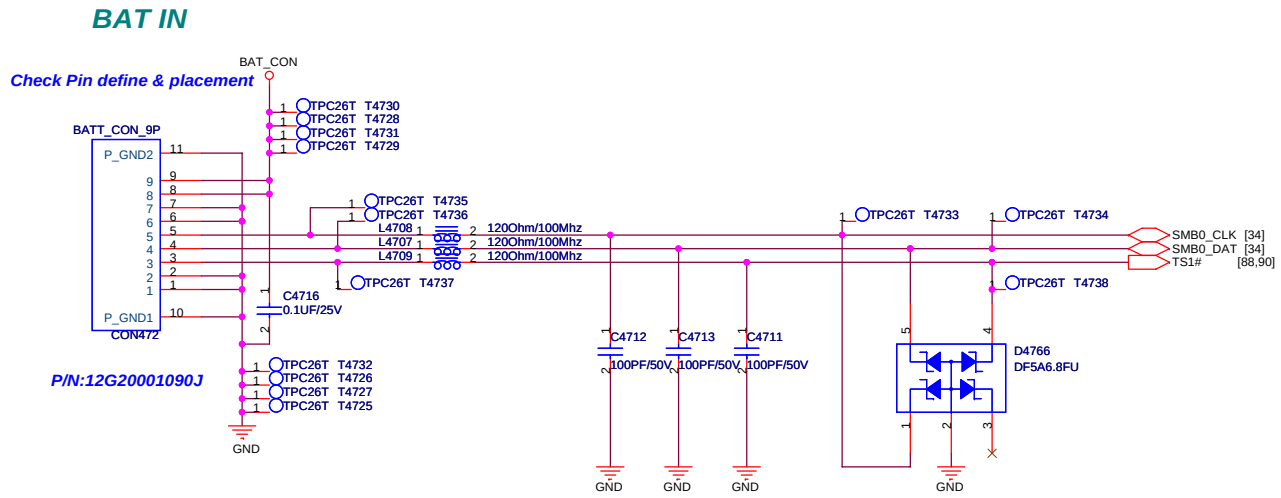

<Variant Name>

ASUSTeK COMPUTER INC

Title : DC & BAT IN

Engineer:

Size	Project Name	Rev
Custom	F6Ve	1.0

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F6V-->F6Ve modify

9.1.1,Page40~45:Change GPU M82_SE to M92-S2

9.1.2,Page40:change PCIE series capacitance from Y5V to X7Y

9.1.3,Page44:change R4408 R4410 from 0402 to 0603 and change L4411 from 600mA to 2A for current

9.1.4,Page22:change R2002 from 0603 to 0805 for current

9.1.5,Page22:remove R2201 for current

9.2.1,Page36:reserved R3660 for crystal X3603

9.2.2,Page34:place R3439 for MARATHON# pull up +3VA_EC

9.2.3,Page17:remove F1702(INVERTER Pin19) for cost down

9.2.4,Page12:add R1210 and C1243 for VCCD_QDAC to 1.5VS

9.2.5,Page33:add R3309 for PCIE_WAKE

9.4.1,Page43:change same net name to divided different name, +1.8Vs_LVDS-->+1.8Vs_LVDS_E
and +1.8Vs_LVDS_F, +1.1Vs_LVDS-->+1.1Vs_LVDS_E and +1.1Vs_LVDS_F

9.4.2,Page41:change R4188 to 0603 for current

9.5.1,Page40:remove PCIE_[8..15] for layout

9.5.2,Page41:Place R4140 R4142 prevent can not link

9.5.3,Page41:reserved Q4103 R4157 for AC_BATT_Detect

9.8.1,Page41:move memory ID from DPVDATA[0..3] to DPVDATA[20..23]

9.8.2,Page41:reserved R4235 for DRAM_RST pull up

9.8.3,Page41:reserved R4120,connect GPIO_17_thermal to EC for thermal protect.

9.9.1,Page29:change L2904 L2903 to R2900 R2901

9.9.2,Page17:change R1717 from 100K to 10K,change R1718 from 1M to 10K

9.9.3,Page42:reserved R4237 R4238 for pull up NC_MEM_CALRN0 and NC_MEM_CALRN1 to +1.8VS,
reserved R4236 for pull down NC_MEM_CALRP0 to ground

9.9.4,Page17:reserved R4159 R4160 for GPIO_TRSTB and PCIE_GPIO2 pull down

9.18.1,Page41:reserved R4161 for GPIO_23_CLKREQB pull up.

ASUSTeK COMPUTER INC	Title : History(1)	
	Engineer:	
Size: Custom	Project Name: F6Ve	Rev: 1.0
Date: Friday, September 26, 2008	Sheet 48 of 64	

<Variant Name>

Title : History(2)

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F6Ve	1.0

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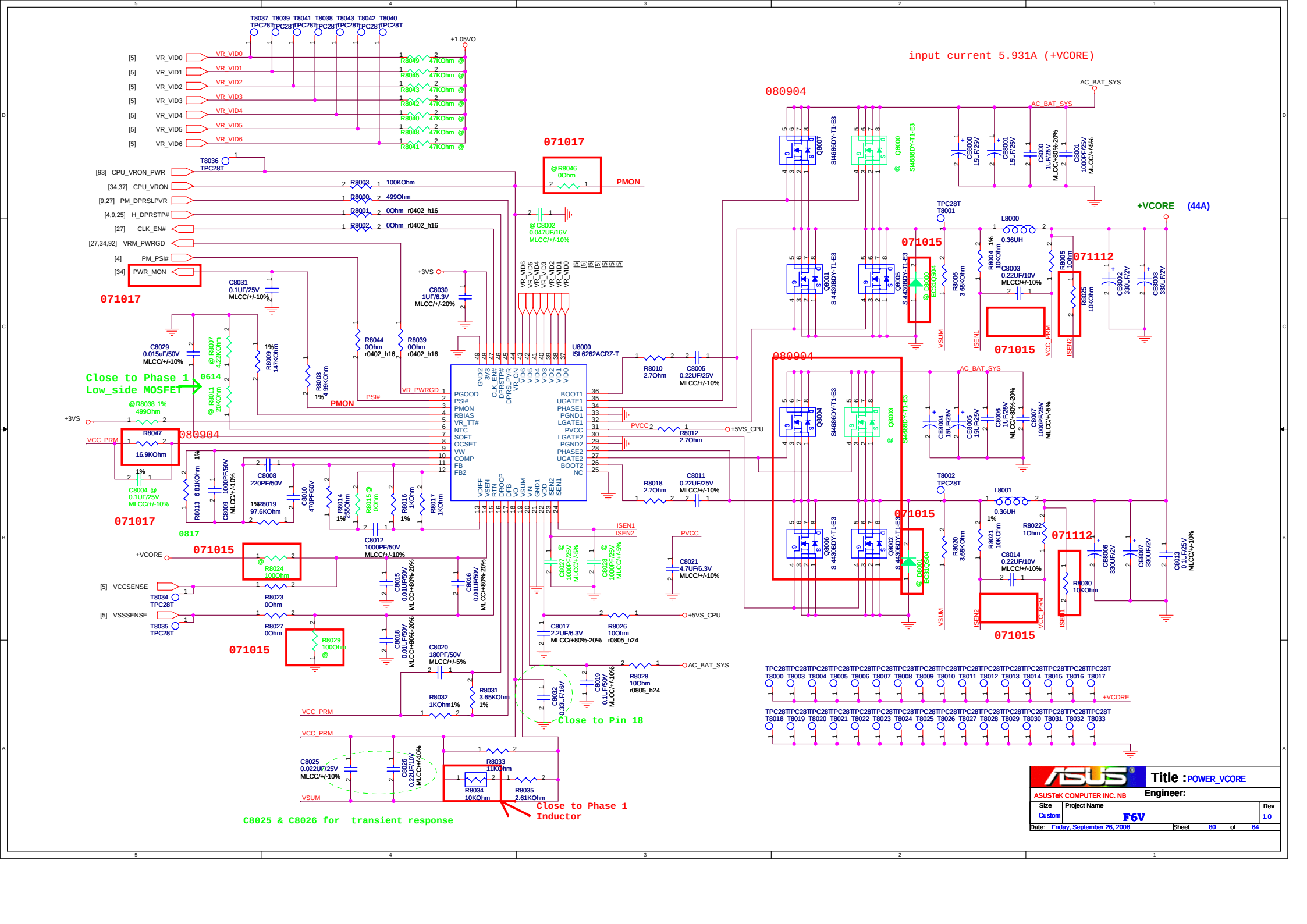
input current 5.931A (+VCORE)
+VCORE (44A)
Close to Phase 1 Low_side MOSFET
Close to Pin 18
C8025 & C8026 for transient response
Close to Phase 1 Inductor
PMON
U8000 ISL6262ACRZ-T
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer:
Project Name F6V
Size Custom
Rev 1.0
Date: Friday, September 26, 2008
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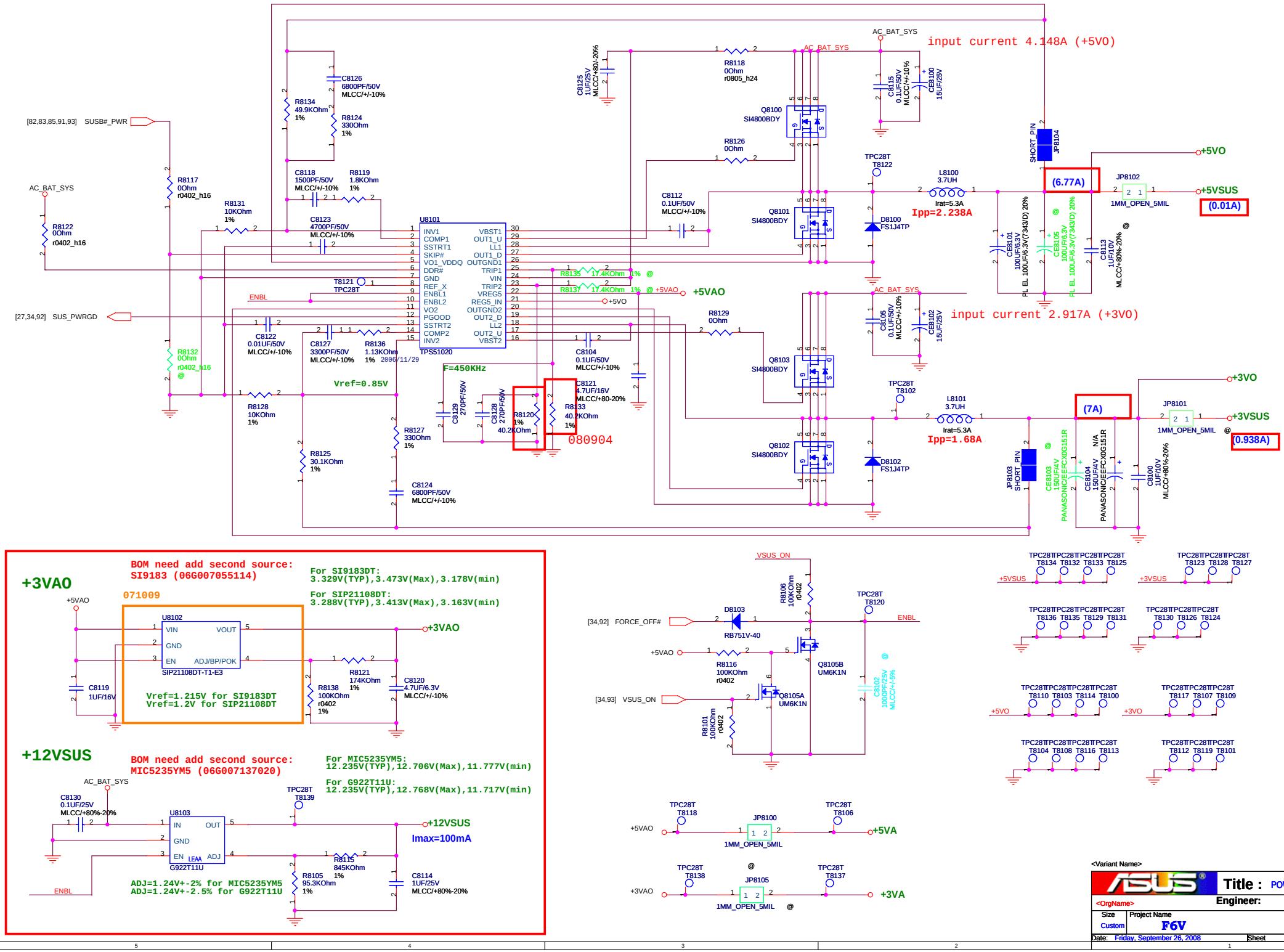
input current 4.148A (+5VO)
input current 2.917A (+3VO)
[82,83,85,91,93] SUSB#_PWR
[27,34,92] SUS_PWRGD
AC_BAT_SYS
ENBL
U8101
TPS51020
INV1
COMP1
SSTRT1
SKIP#
VO1_VDDQ
DDR#
GND
REF_X
ENBL1
ENBL2
VO2
PGOOD
SSTRT2
COMP2
INV2
VBST1
OUT1_U
LL1
OUT1_D
OUTGND1
TRIP1
VIN
TRIP2
VREG5
REG5_IN
OUTGND2
OUT2_D
LL2
OUT2_U
VBST2
F=450KHz
Vref=0.85V
080904
Q8100 SI4800BDY
Q8101 SI4800BDY
Q8103 SI4800BDY
Q8102 SI4800BDY
D8100 FS1J4TP
D8102 FS1J4TP
L8100 3.7UH
L8101 3.7UH
Irat=5.3A
Ipp=2.238A
Ipp=1.68A
(6.77A)
(7A)
(0.01A)
(0.938A)
+5VO
+5VSUS
+3VO
+3VSUS
JP8104
JP8102
JP8101
JP8103
SHORT_PIN
1MM_OPEN_5MIL
+5VAO
+3VAO
+3VA
+12VSUS
Imax=100mA
VSUS_ON
FORCE_OFF#
ENBL
RB751V-40
Q8105B UM6K1N
Q8105A UM6K1N
TPC28T T8122
TPC28T T8102
TPC28T T8120
TPC28T T8139
TPC28T T8118
TPC28T T8106
TPC28T T8138
TPC28T T8137
JP8100
JP8105
BOM need add second source:
SI9183 (06G007055114)
071009
For SI9183DT:
3.329V(TYP),3.473V(Max),3.178V(min)
For SIP21108DT:
3.288V(TYP),3.413V(Max),3.163V(min)
SIP21108DT-T1-E3
Vref=1.215V for SI9183DT
Vref=1.2V for SIP21108DT
BOM need add second source:
MIC5235YM5 (06G007137020)
For MIC5235YM5:
12.235V(TYP),12.706V(Max),11.777V(min)
For G922T11U:
12.235V(TYP),12.768V(Max),11.717V(min)
G922T11U
ADJ=1.24V+-2% for MIC5235YM5
ADJ=1.24V+-2.5% for G922T11U

Variant Name
Title : POWER_SYSTEM
Engineer:
OrgName
Size Custom
Project Name F6V
Rev 1.0
Date: Friday, September 26, 2008
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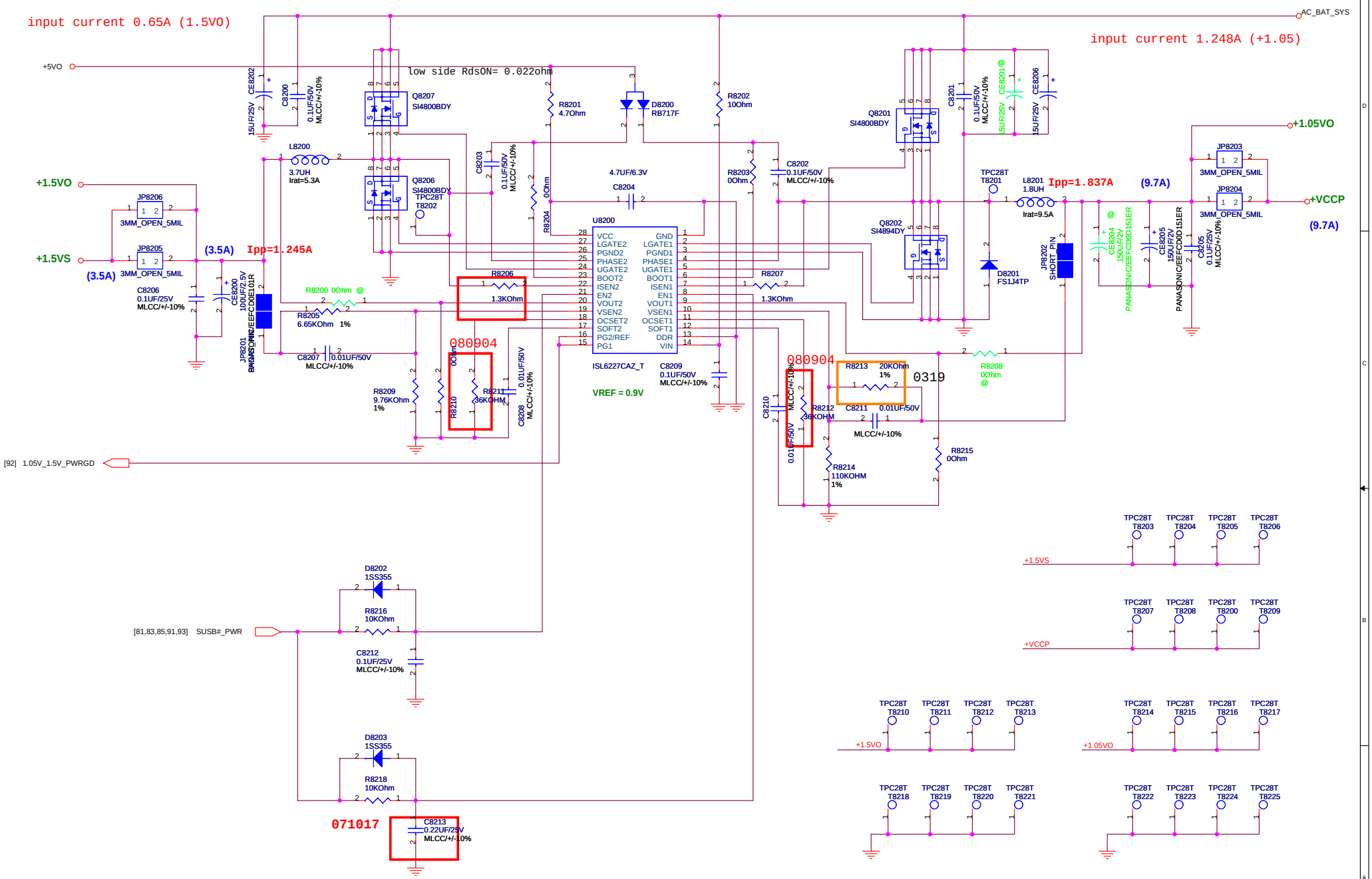

<Variant Name>

Title : POWER_I/O_1.5VS & 1.05VS

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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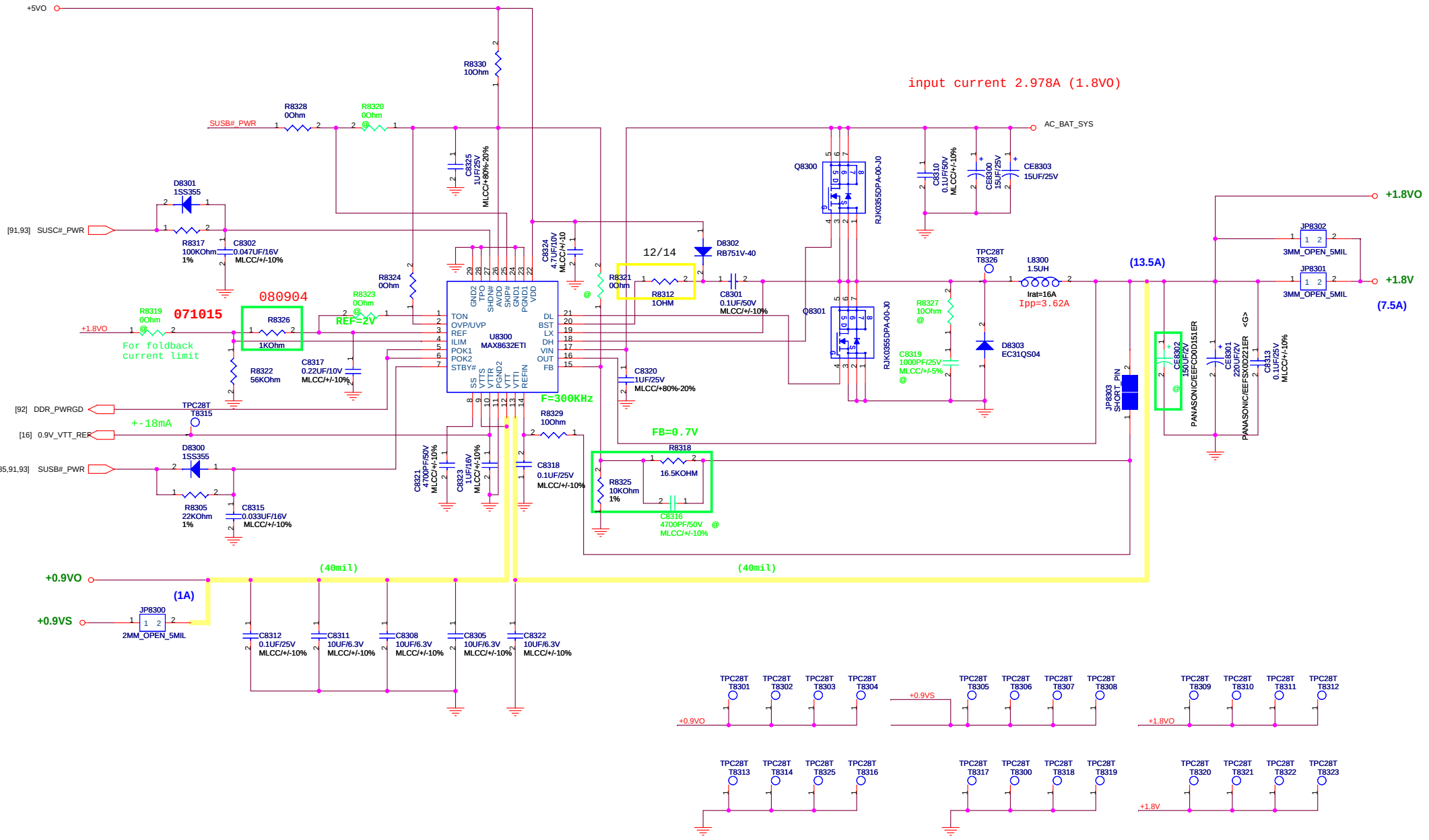
input current 2.978A (1.8VO)
+5VO
SUSB#_PWR
AC_BAT_SYS
+1.8VO
+1.8V
(7.5A)
(13.5A)
U8300
MAX8632ETI
TON
OVP/UVP
REF
ILIM
POK1
POK2
STBY#
DL
BST
LX
DH
VIN
OUT
FB
GND2
DPO
SHDN#
AVDD
SKIP#
GND1
PGND1
VDD
SS
VTTS
VTTR
PGND2
VTTI
REFIN
080904
071015
REF=2V
F=300KHz
FB=0.7V
For foldback current limit
+-18mA
Ipp=3.62A
Irat=16A
12/14
RJK0355DPA-00-J0
[91,93] SUSC#_PWR
[92] DDR_PWRGD
[16] 0.9V_VTT_REF
[81,82,85,91,93] SUSB#_PWR
+0.9VO
+0.9VS
(1A)
(40mil)
2MM_OPEN_5MIL
3MM_OPEN_5MIL
SHORT_PIN
PANASONIC/EEFCD0D151ER
PANASONIC/EEFSXD0221ER
<Variant Name>
Title : POWER_I/O_DDR & VTT
ASUSTeK COMPUTER INC. NB
Engineer:
Size: Custom
Project Name: F6V
Rev: 1.0
Date: Friday, September 26, 2008
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<Variant Name>

Title : POWER_I/O_+3VAO

ASUSTeK COMPUTER INC. NB

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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071017

20080304

1107

Add:JP8507
delete:R8503,C8516
C8514,R8514,R8527

1112, chang the working Frequency to 450Khz

1106,delete JP8502

1112

12/14

080904

12/14

1.98V set OCP as 16.69A

11/01

SKIP# = VDD , forced PWM mode
SKIP# = OPEN ,ultrasonic mode
SKIP# = GND , pulse skipping mode

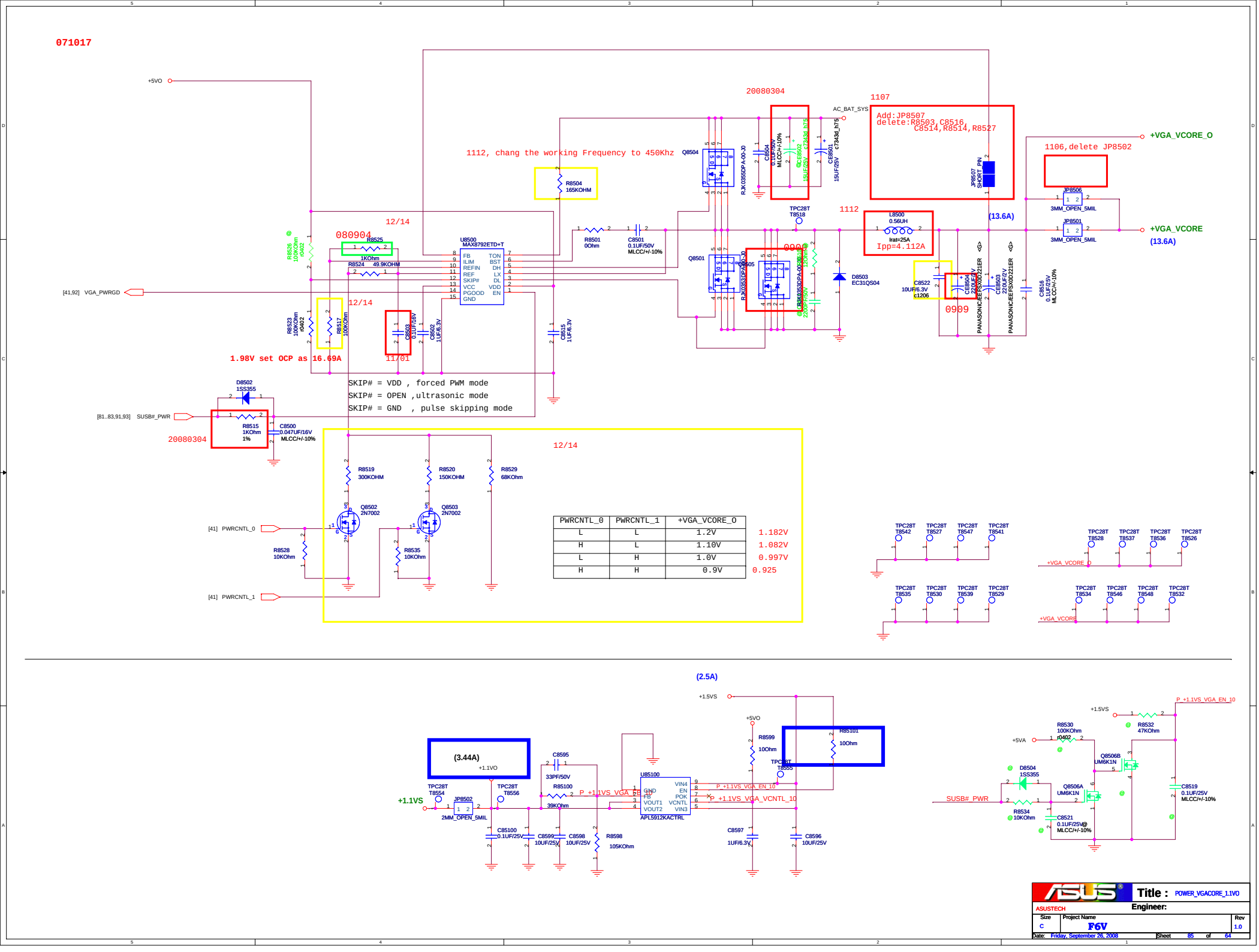
20080304

12/14

PWRCNTL_0	PWRCNTL_1	+VGA_VCORE_O	
L	L	1.2V	1.182V
H	L	1.10V	1.082V
L	H	1.0V	0.997V
H	H	0.9V	0.925

(2.5A)

(3.44A)



ASUSTEK

Title : POWER_VGACORE_1.1VO

Engineer:

Size	Project Name	Rev
C	F6V	1.0

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<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Ray

Size	Project Name	Rev
B	F6V	1.0

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<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_SHUTDOWN#

Engineer: Ray

Size	Project Name	Rev
Custom	F6V	1.0

Date: Friday, September 26, 2008 Sheet 87 of 64

POWER PATH & BAT_LEARN

90 WATT

071015

070115

0614

0319

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.010ohm
VCLS=2.5341V
=> Iin(max)=4.5A
=> Constant Power = 19 * 4.5 = 85.5W
=> R5710=20K,R5715=30K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.588V
=> Vbatt = 4.2V

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

Precgarge current=150mA

AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800

90W->10m Ohm
65W->20m Ohm

90W->30K Ohm
65W->137K Ohm

4S: Mount R8808 only
3S: Unmount all components
3S/4S: Unmount R8808, and mount others

Title : POWER_CHARGER			
ASUSTeK COMPUTER INC. NB	Engineer:		
Size: Custom	Project Name: F6V		Rev: 1.0
Date: Friday, September 26, 2008	Sheet 88 of 64		

<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F6V	1.0

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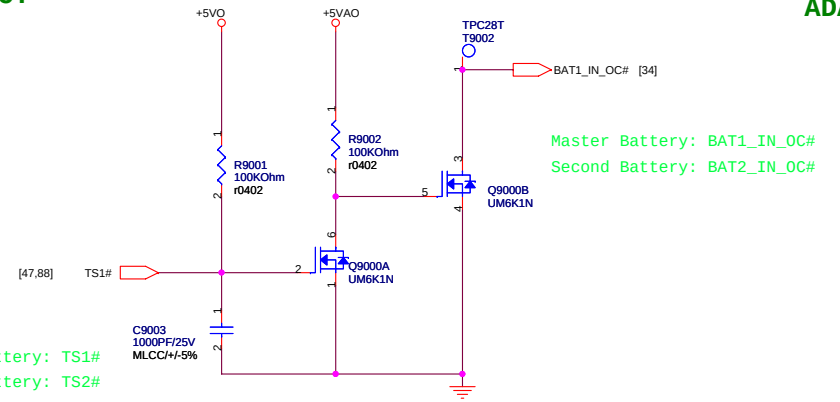
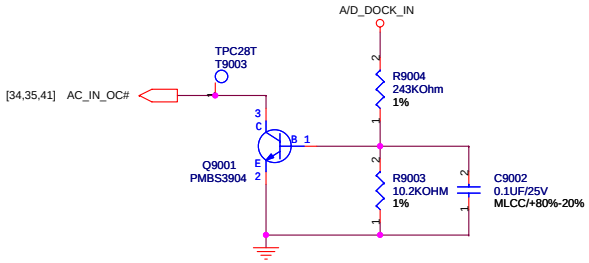
BATTERY IN DETECT



Master Battery: BAT1_IN_OC#
Second Battery: BAT2_IN_OC#

Master Battery: TS1#
Second Battery: TS2#

ADAPTER IN DETECT



+2.5VREF

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_DETECT

Engineer: Ray

Size	Project Name	Rev
Custom	F6V	1.0

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SUSB#_PWR POWER

20080304

TPC28T T9125, TPC28T T9110
+1.8VO
Q9100 FDW2501NZ_NL
DRAIN_1, DRAIN_2, SOURCE_1, SOURCE_3, SOURCE_2, SOURCE_4, GATE_1, GATE_2
TPC28T T9100, TPC28T T9122
+1.8VS (5.1A)
R9111 1KOhm 1%
C9111 0.1UF/25V MLCC/+/-10%

20080326

C9100 0.22UF/16V MLCC/+/-10%

071015

TPC28T T9104, TPC28T T9118
+3VO
Q9108 SI4800BDY
TPC28T T9109, TPC28T T9114
+3VS (4.2A)
R9108 47KOhm r0402_h16
C9102 0.1UF/25V MLCC/+/-10%
C9104 0.1UF/25V MLCC/+/-10%

TPC28T T9105, TPC28T T9115
+5VO
Q9106 FDW2501NZ_NL
DRAIN_1, DRAIN_2, SOURCE_1, SOURCE_3, SOURCE_2, SOURCE_4, GATE_1, GATE_2
TPC28T T9101, TPC28T T9127
+5VS (4.65A)
R9107 47KOhm r0402_h16
C9107 0.1UF/25V MLCC/+/-10%
C9109 0.033UF/16V MLCC/+/-10%
JP9100 SHORT_PIN
+5VS_FAN
JP9101 SHORT_PIN
+5VS_CPU
R9112 47KOhm 1%
0607
0607

TPC28T T9128, TPC28T T9129
+12VSUS
SUSB#_PWR
Q9105 UMC4N
TPC28T T9102
+12VS
R9102 100KOhm 1%

SUSC#_PWR POWER

071015

TPC28T T9111, TPC28T T9133
+3VO
Q9103 SI4800BDY
TPC28T T9126, TPC28T T9108
+3V (2A)
R9109 22KOhm 1%
C9106 0.1UF/25V MLCC/+/-10%
C9110 0.1UF/25V MLCC/+/-10%

TPC28T T9117, TPC28T T9132
+5VO
Q9101 FDW2501NZ_NL
DRAIN_1, DRAIN_2, SOURCE_1, SOURCE_3, SOURCE_2, SOURCE_4, GATE_1, GATE_2
TPC28T T9124, TPC28T T9113
+5V (2.1A)
R9110 22KOhm 1%
C9113 0.1UF/25V MLCC/+/-10%
C9105 0.033UF/16V MLCC/+/-10%
R9106 22KOhm 1%

TPC28T T9120
+12VSUS
Q9107 UMC4N
TPC28T T9112
+12V
TPC28T T9119
SUSC#_PWR
1% R9103 100KOhm

071015

[33,34,37,92] SUSB_EC#
TPC28T T9131
R9105 1KOhm
TPC28T T9135
[81..83,85,93] SUSB#_PWR

TPC28T T9121
R9104 1KOhm
[34,37] SUSC_EC#
TPC28T T9134
[83,93] SUSC#_PWR

ASUSTeK COMPUTER INC. NB

Title : POWER_LOAD SWITCH

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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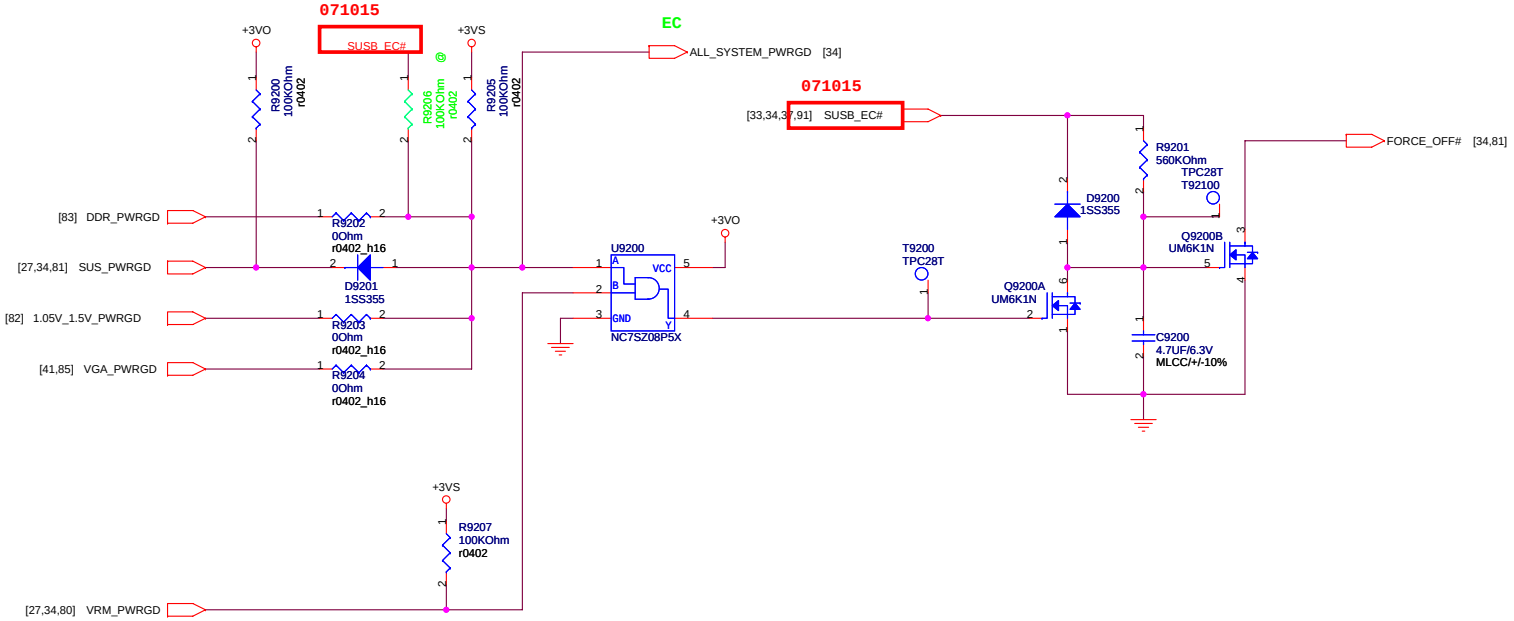
POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_PROTECT

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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AC_BAT_SYS — AC_BAT_SYS [46,80..83,85,88]

BAT — BAT [46,88]

BAT_CON — BAT_CON [46,47,88]

+3VA — +3VA [17,25,34,37,46,81]

+5VAO — +5VAO [81,90]

+5VO — +5VO [81..83,85,90,91]

+5VSUS — +5VSUS [28,39,81]

+5V — +5V [17,24,37,91]

+5VS — +5VS [18,19,22,23,28,33,37..39,46,91]

+3VO — +3VO [81,91,92]

+3VSUS — +3VSUS [17,20,22,25..29,34,39,46,81]

+3V — +3V [19..22,26,29,33,35..38,91]

+3VS — +3VS [4,6,7,9,12..15,17..23,25..31,33,34,37,39,44,80,91,92]

+12VSUS — +12VSUS [81,91]

+12V — +12V [22,24,36,37,91]

+12VS — +12VS [17,19,31,37,44,91]

+1.8VO — +1.8VO [83,91]

+1.8V — +1.8V [9,11,14..16,37,83]

+0.9VS — +0.9VS [16,37,83]

+0.9VO — +0.9VO [83]

+1.05VO — +1.05VO [80,82]

+VCCP — +VCCP [6..9,11,12,25,28,37,82]

+1.5VO — +1.5VO [82]

+1.5VS — +1.5VS [5,12,20,28,33,37,82,85]

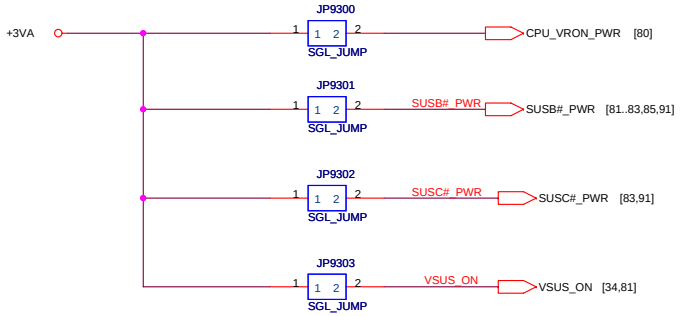
+VCORE — +VCORE [5,6,37,80]

+VGA_VCORE — +VGA_VCORE [37,44,85]

+1.8VS — +1.8VS [37,41..45,91]

+1.1VS — +1.1VS [37,41,44,45,85]

FOR POWER TEST



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_SIGNAL

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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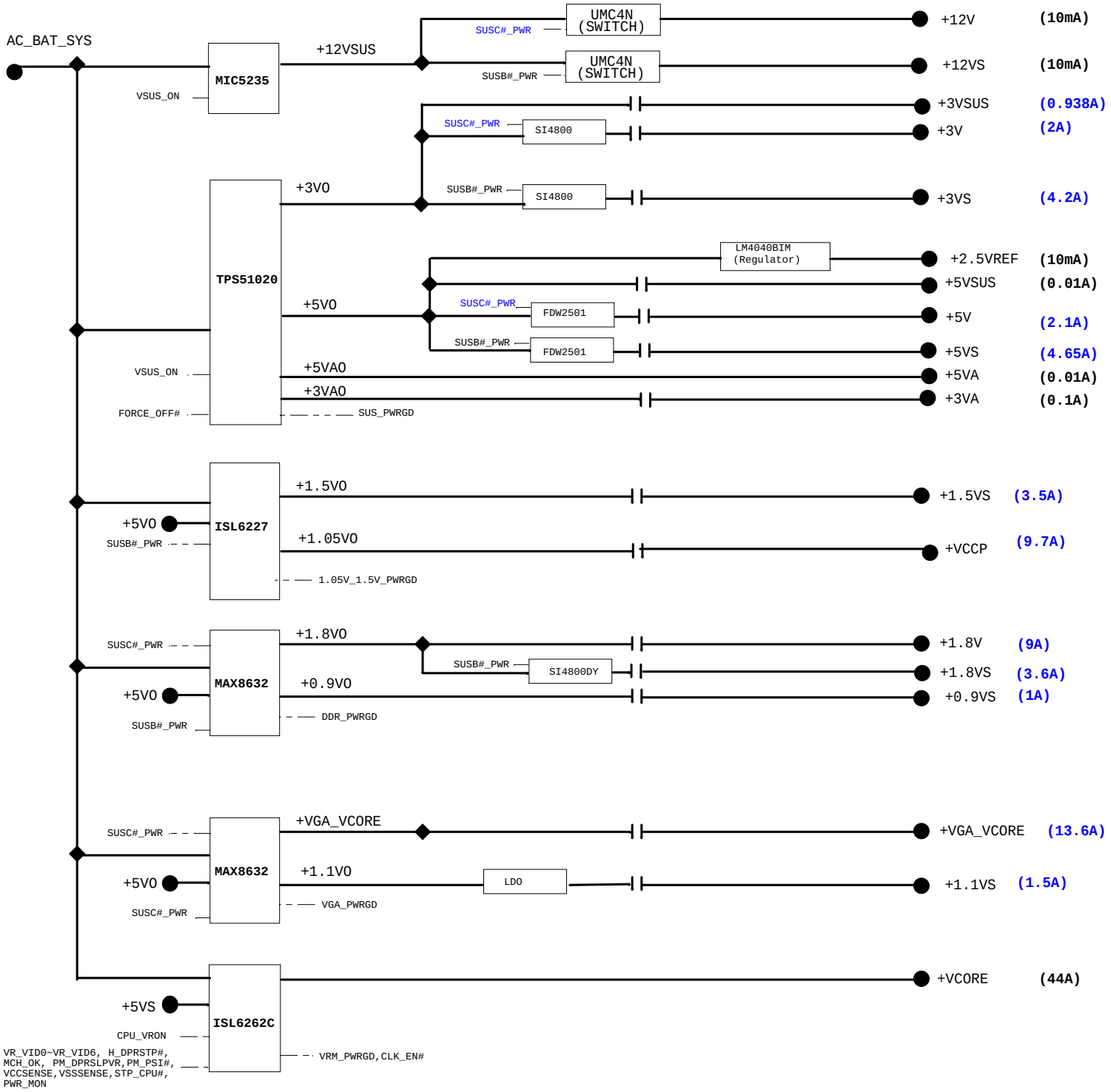

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer:

Size	Project Name	Rev
Custom	F6V	1.0

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