Project Name :GI5CPXX

Platform : CFL-H+N18P-GX(N17P)

PAGE CONTENT

M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

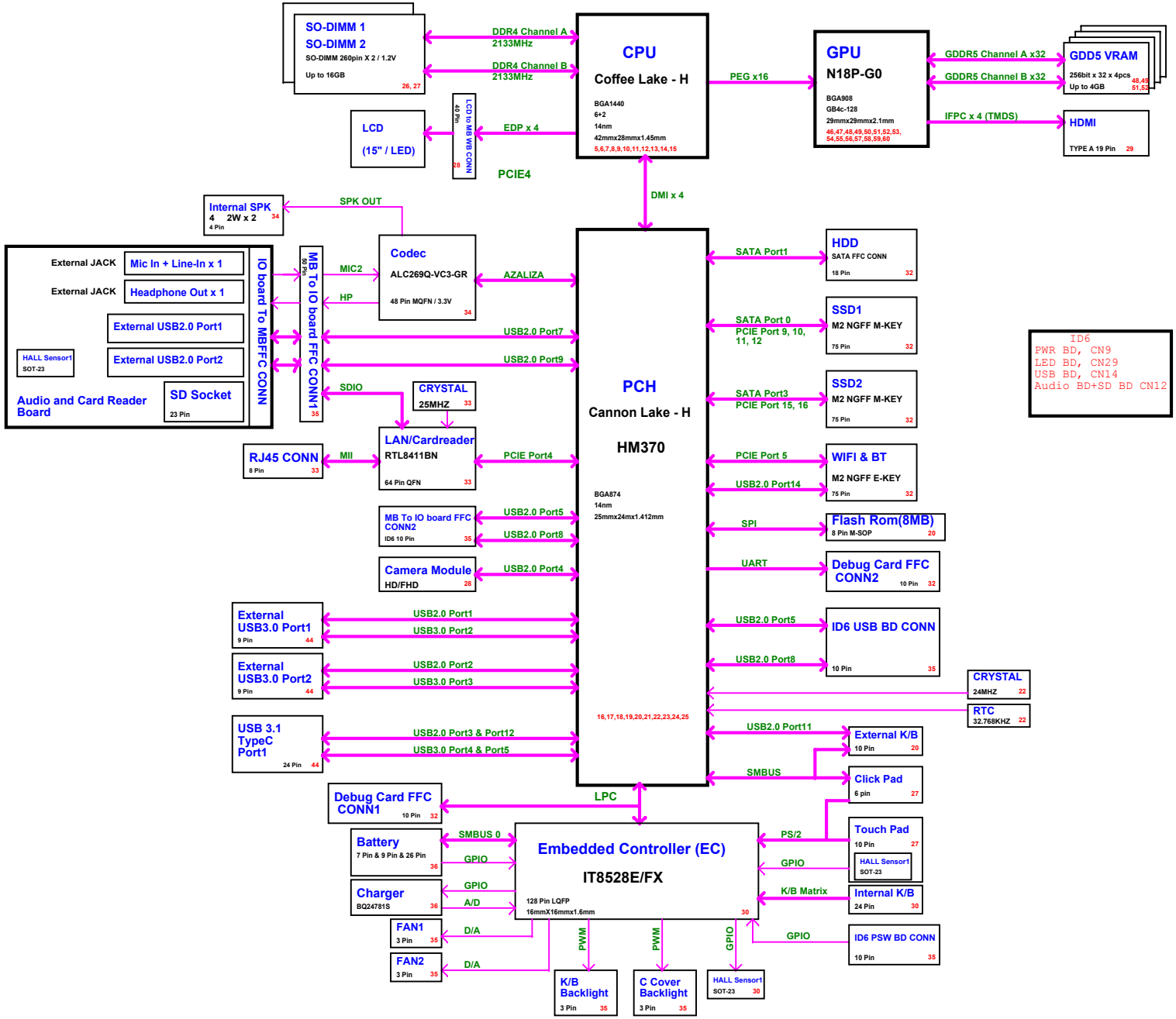
<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 01 INDEX

Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 1 of 65

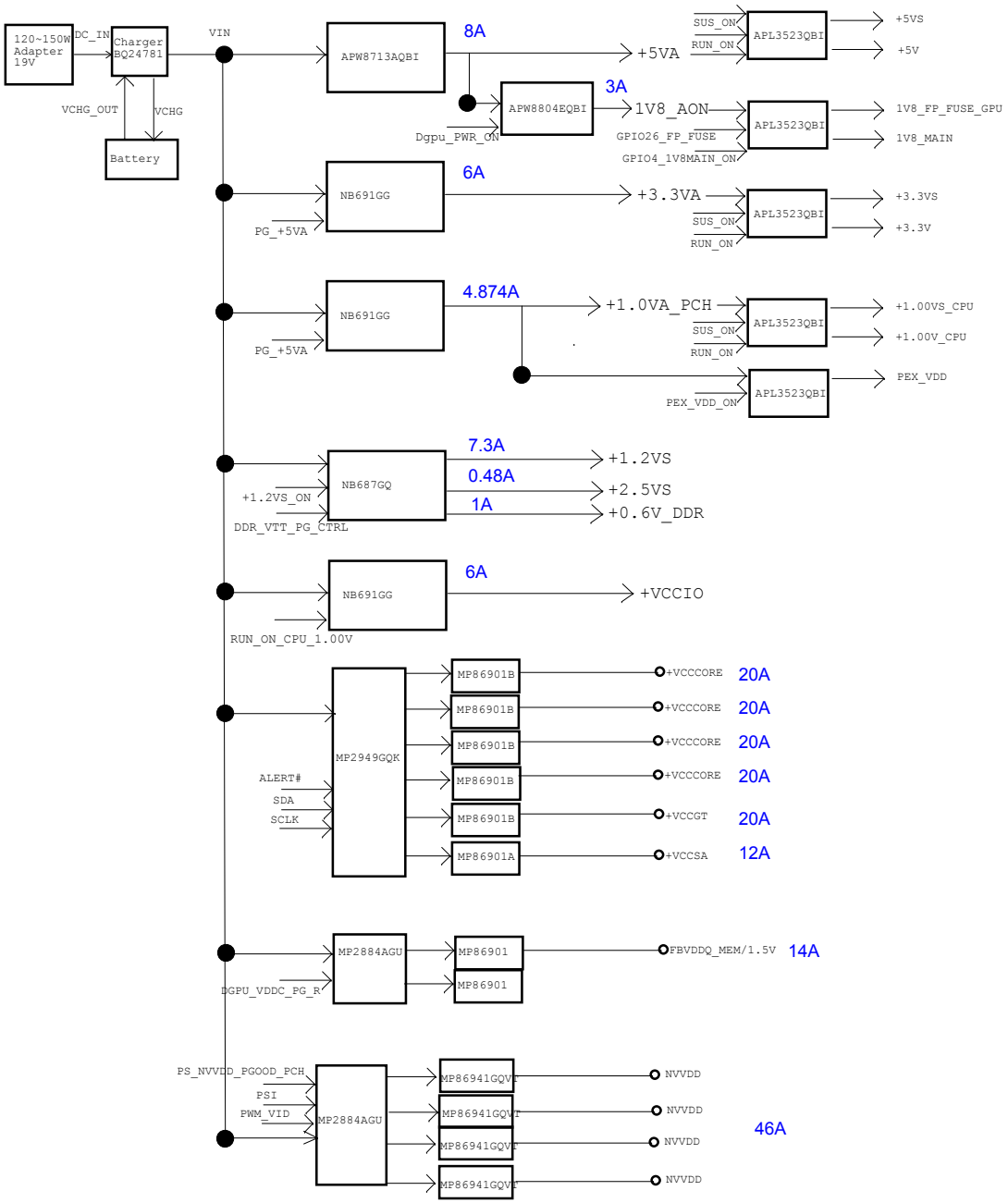
SYSTEM BLOCK DIAGRAM



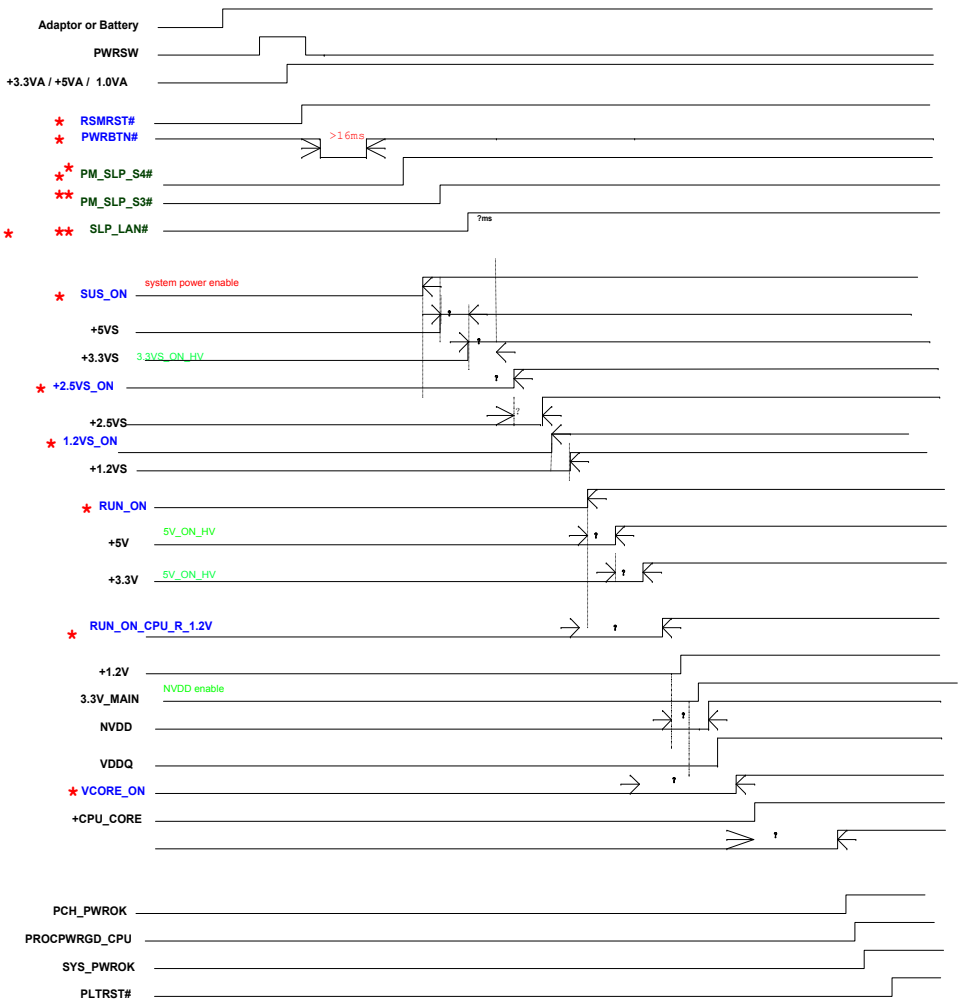
<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title	02 SYSTEM BLOCK	
Size: Custom	Document Number: GI6CPXX	Rev: S
Date: Monday, December 24, 2018	Sheet 2 of 65	

POWER BLOCK DIAGRAM



System Poewr On Sequence



* EC Control Pin (O/P)

** EC Control Pin(I/P)

<OrgName>

同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 03 POWER DIAGRAM & SEQUENCE		
Size: Custom	Document Number: GI5CPXX	Rev: B
Date: Monday, December 24, 2018	Sheet 3 of 65	

GI5CP

GPP_F21	PCH_BL_PWM	DEL
GPP_F20	T/P LED_PWM	
GPP_F19	PWM_KB BLUE	
GPA3	PWM_KB RED	
GPA4	PID_1 CHG_R LED	
GPA5	PID_2 PWR_LED	
GPA6	ME_KB_LED	
GPA7	Board ID	

ITE8528 GPIO		Default Pull/Mode
GPA0	PWM_KB GREEN	UP / GPO
GPA1	T/P LED_PWM	UP / GPO
GPA2	PWM_KB BLUE	UP / GPO
GPA3	PWM_KB RED	UP / GPO
GPA4	PID_1 CHG_R LED	UP / GPO
GPA5	PID_2 PWR_LED	UP / GPO
GPA6	C_COVER_BLM_LED_PWM	UP / GPO
GPA7	Board ID	UP / GPO
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	GPU_Adaptor In	Dn / GPI
GPB3	BAT_SMBCLK	Z / Native
GPB4	BAT_SMBDAT	Z / Native
GPB5	H_A20GATE	Z / Native
GPB6	H_RCIN#	UP / Native
GPB7	SAFTY_PROTECT	Dn / GPO
GPC0	LAN_PWR	Dn / GPO
GPC1	SMBCLK_EC	Z / Native
GPC2	SMBDAT_EC	Z / Native
GPC3	SENBAT_V	Dn / GPO
GPC4	FAN_enable0	Dn / GPO
GPC5	SYS_PWROK	Dn / GPO
GPC6	WEBCAM_ON(Reserved)	Dn / GPO
GPC7	BOOST_FAN(Reserved)	UP / GPO
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPO
GPD2	PLT_RST#	UP / GPI
GPD3	HDMI_HPD	UP / GPI
GPD4	EC_EXTSMI#	UP / GPO
GPD5	ME_WE	UP / GPO
GPD6	FAN0_detect	Dn / Native
GPD7	FAN1_detect	Dn / Native
GPE0	LID#	Dn / GPI
GPE1	+1.2VS_ON	Dn / GPO
GPE2	PWR_USB#	Dn / GPO
GPE3	EXT_WIFI_ON	Dn / GPO
GPE4	PWRSW#	UP / GPI
GPE5	LVDS_VIN	Dn / GPO
GPE6	WLAN_ON	Dn / GPO
GPE7	AMP_MUTE#	UP / GPO
GPF0	VRA_PE	UP / GPO
GPF1	PCH_PWROK	UP / GPO
GPF2	BT_ON	UP / GPO
GPF3	Q_key1	UP / GPI
GPF4	TP_CLK	UP/ Native
GPF5	TP_DATA	UP/ Native
GPF6	EC_PECI	UP/ Native
GPF7	RUN_ON	UP / GPO
GPG0	PANEL_3.3V_ON	Z/ GPO
GPG1	Reserved for AC removal	Dn/GPO
GPG2	CPUCORE_ON	Z/ GPO
GPG6	SUS_ON	Z/ GPO
GPH0	PM_CLKRUN#	Dn/ Native
GPH1	PCH_BL_EN	Dn/GPO
GPH2	ID_DET	Dn/GPI
GPH3	PANEL_VCC	Dn/GPI
GPH4	DGPU_RST_EC#	Dn/GPO
GPH5	HYB_ON#	Dn/GPI
GPH6	Clear CMOS	Dn/GPIO
GPI0	PM_RSMRST#	/GPO/Z
GPI1	EC_OVERT_GPU#	/GPI/Z
GPI2	Reserved	/GPI/Z
GPI3	ME_KB_ID	/GPI/Z
GPI4	BAT_I	/GPI/Z
GPI5	BATT_TEMP	/GPI/Z
GPI6	Iadapter_I bat	/GPI/Z
GPI7	BAT_V	/GPI/Z
GPJ0	EC_BL_ON	/GPO/Z
GPJ1	EC_PROCHOT#	/GPO/Z
GPJ2	FAN_CTRL0	/GPO/Z
GPJ3	BATT_VA_OFF#	/GPO/Z
GPJ4	FAN_CTRL1	/GPO/Z
GPJ5	CHG_REF	/GPO/Z
GPM0	LPC_AD0	Native/Z
GPM1	LPC_AD1	Native/Z
GPM2	LPC_AD2	Native/Z
GPM3	LPC_AD3	Native/Z
GPM4	CLK_EC_LPC	Native/Z
GPM5	LPC_FRAME#	Native/Z
GPM6	INT_SERIRQ	Native/Z

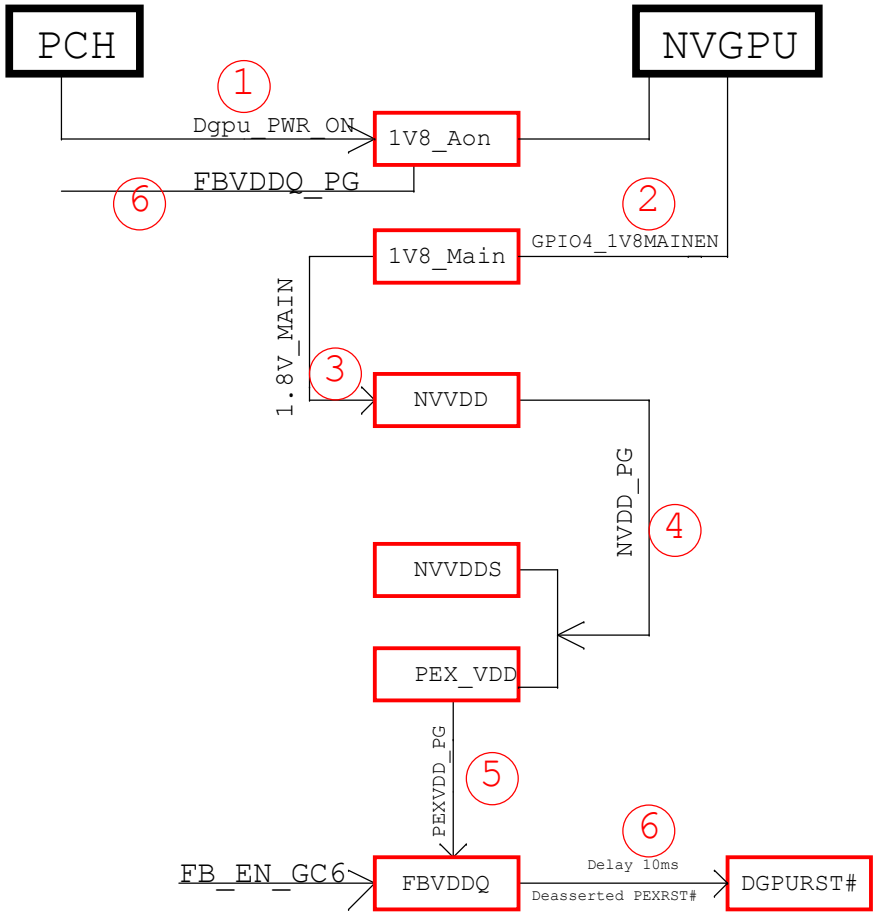
<OrgName>
同方国际信息技术有限公司 <OrgAdd1> <OrgAdd2> <OrgAdd3> <OrgAdd4>

Title: 04 GPIO & SMBUS BLOCK

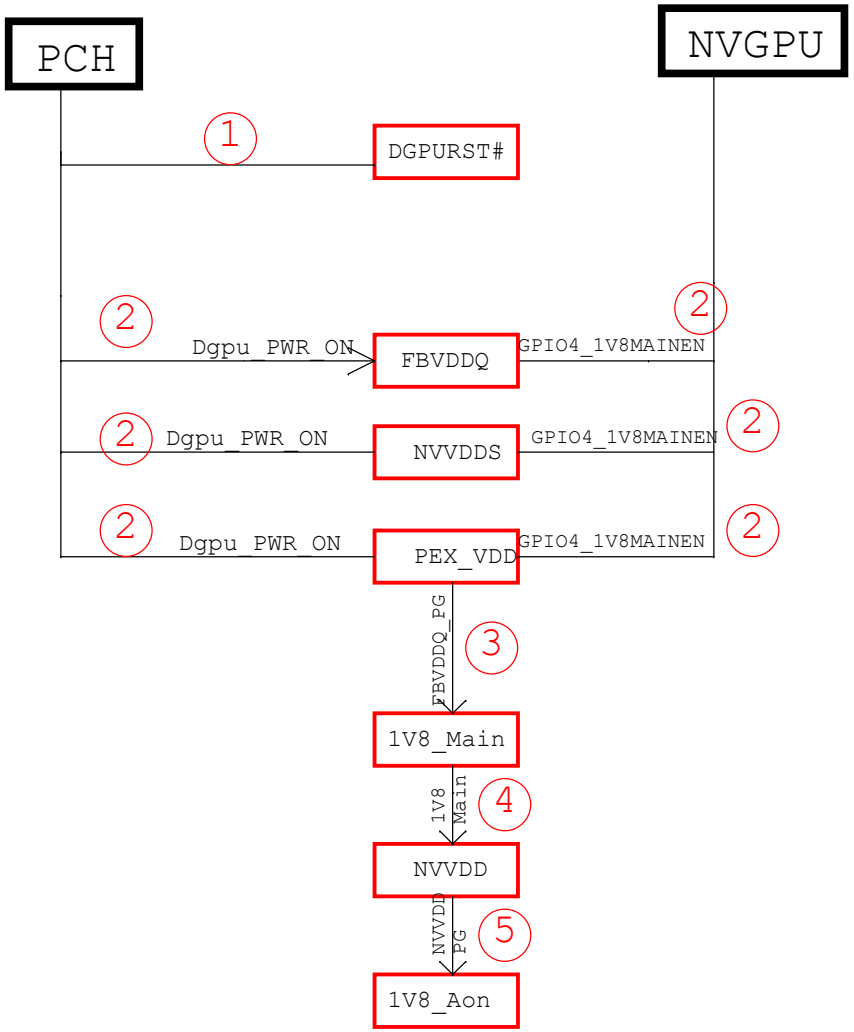
Size: Custom | Document Number: G85CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 4 of 63

DPU Power On Timing

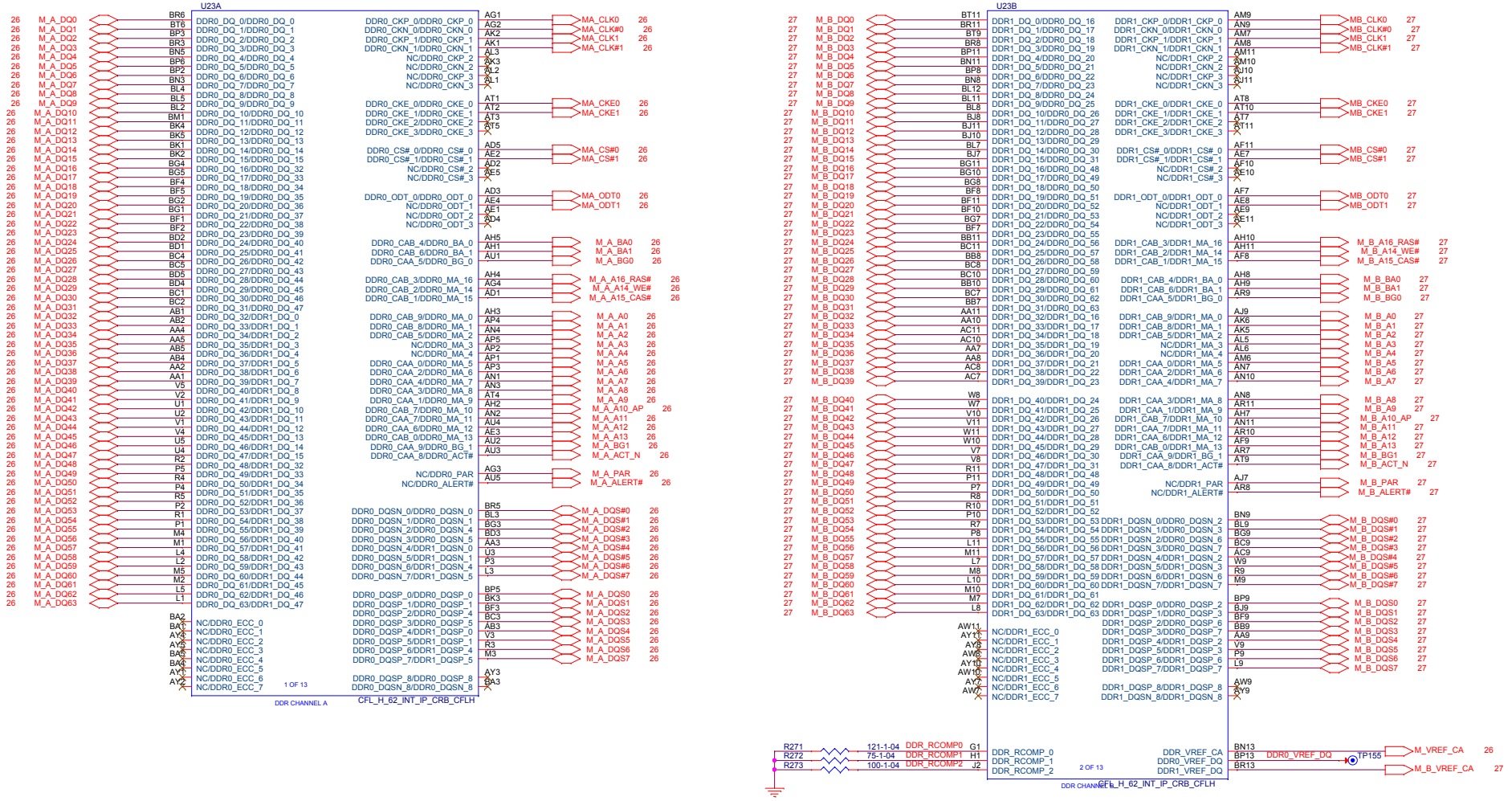


DPU Power Off Timing



<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title	03 POWER DIAGRAM & SEQUENCE	
Size: Custom	Document Number: GI5CPXX	Rev: B
Date: Monday, December 24, 2018	Sheet 5 of 65	



<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 06 CPU CFL-H : DDR4 CH-A/CH-B

Size	Document Number	Rev
Custom	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 6 of 65

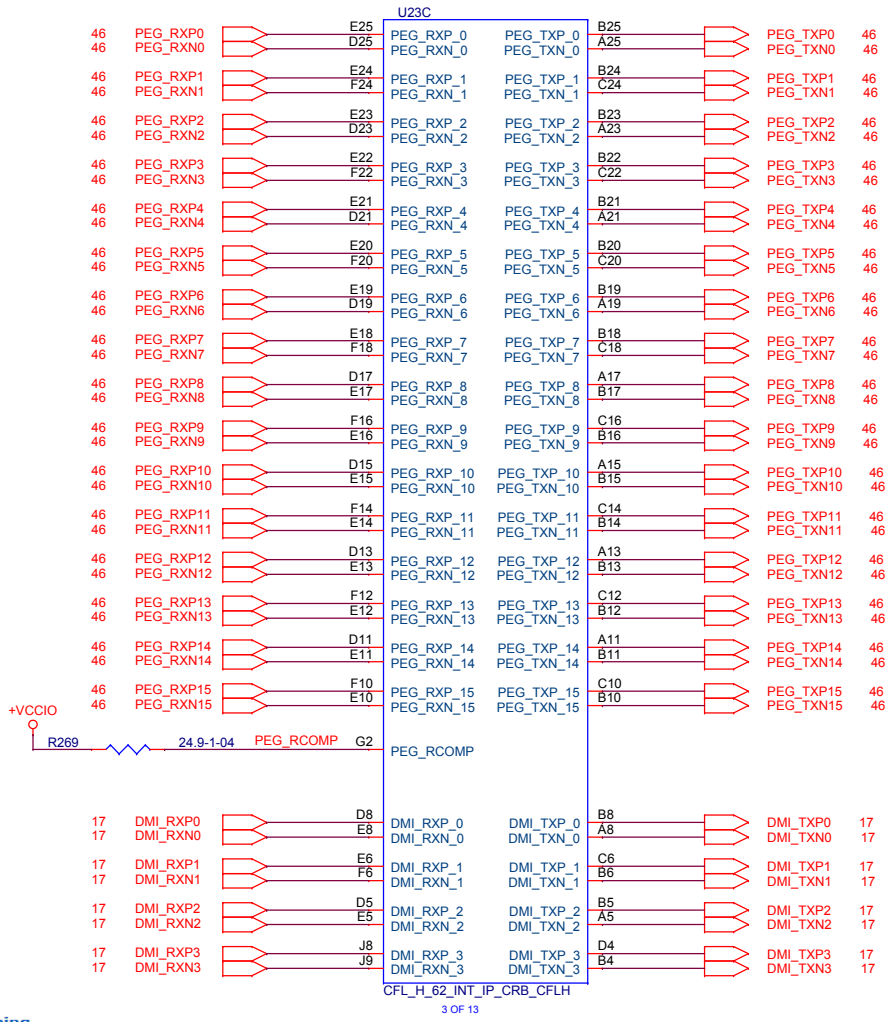


Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

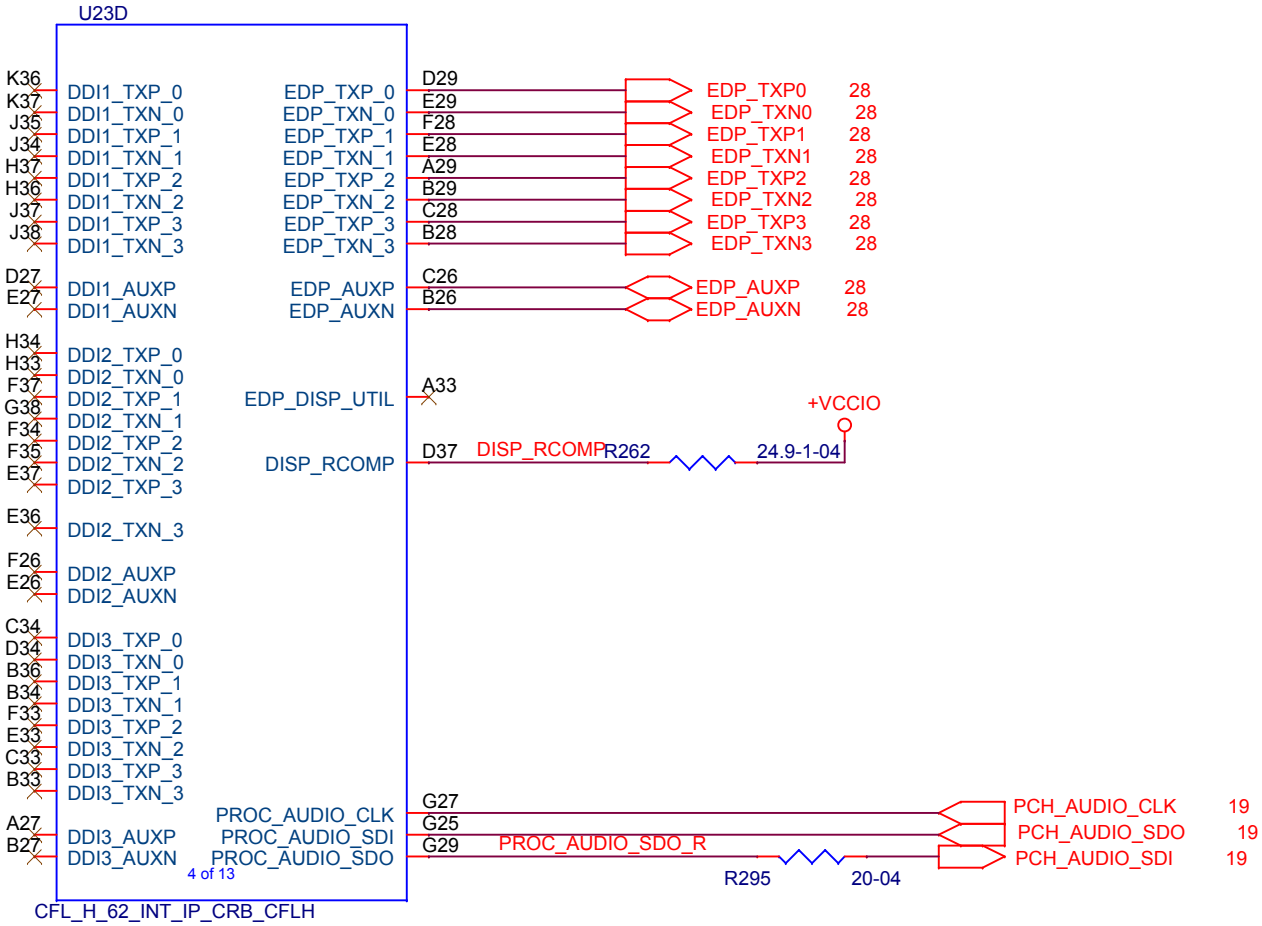
Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

<OrgName>
同方国际信息技术有限公司 <OrgAddr1>
<OrgAddr2>
<OrgAddr3> <OrgAddr4>

Title: 07 CPU CFL-H : PEG/DMI

Size: B | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 7 of 65



<OrgName>

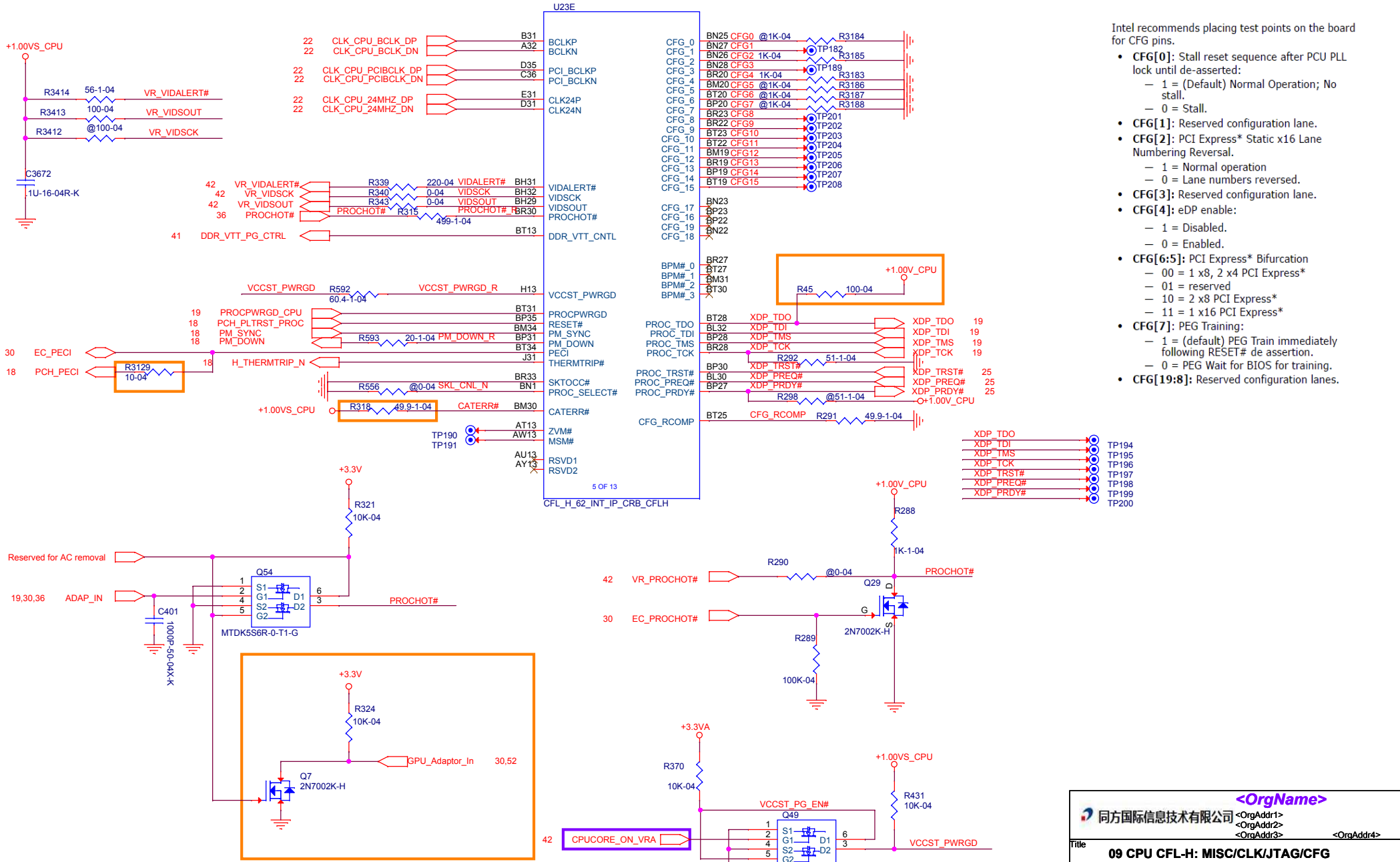
同方国际信息技术有限公司

<OrgAddr2>
<OrgAddr3> <OrgAddr4>

Title: 08 CPU CFL-H : DDI/EDP

Size	Document Number	Rev
A	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 8 of 65

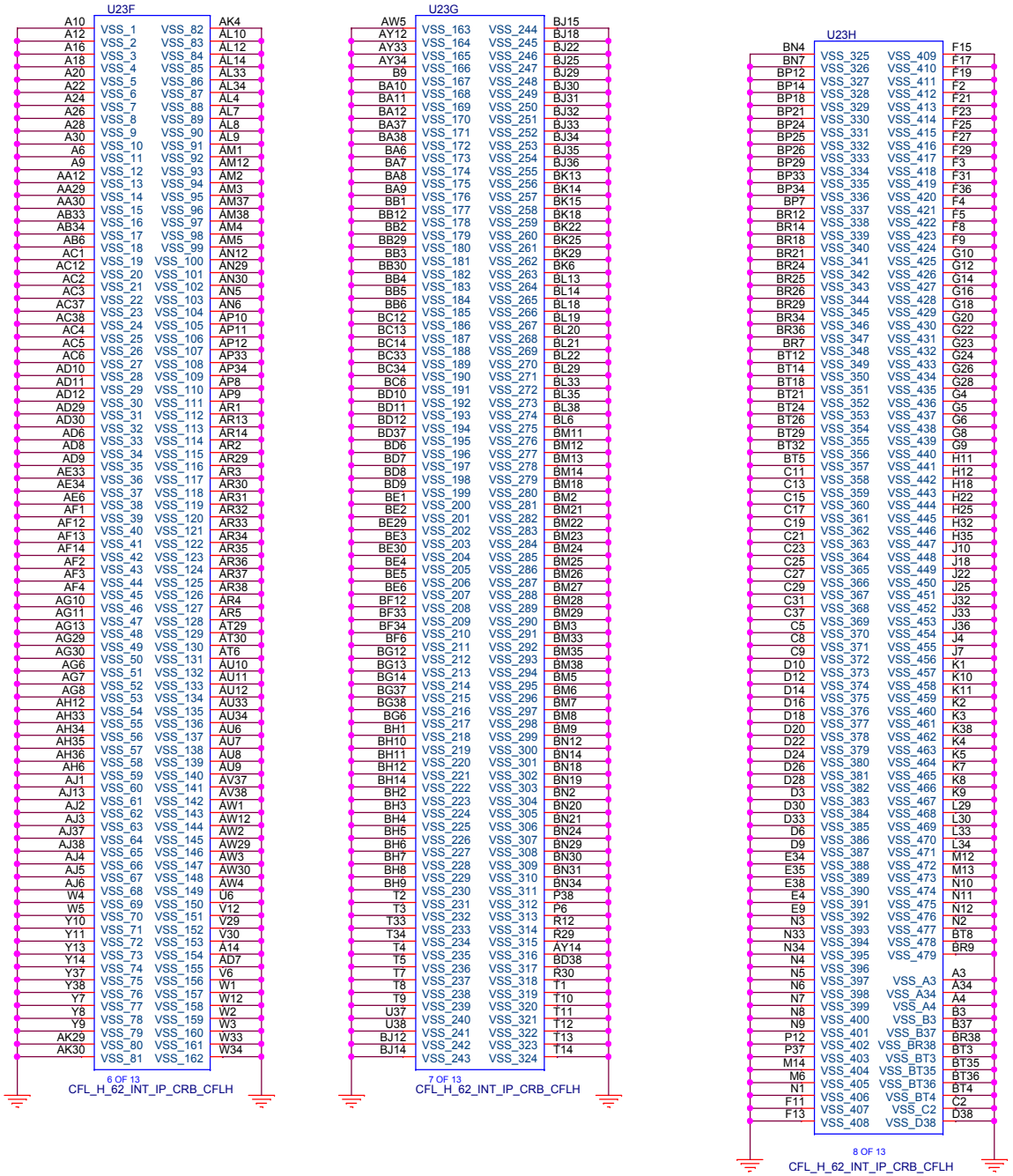


Intel recommends placing test points on the board for CFG pins.

- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.

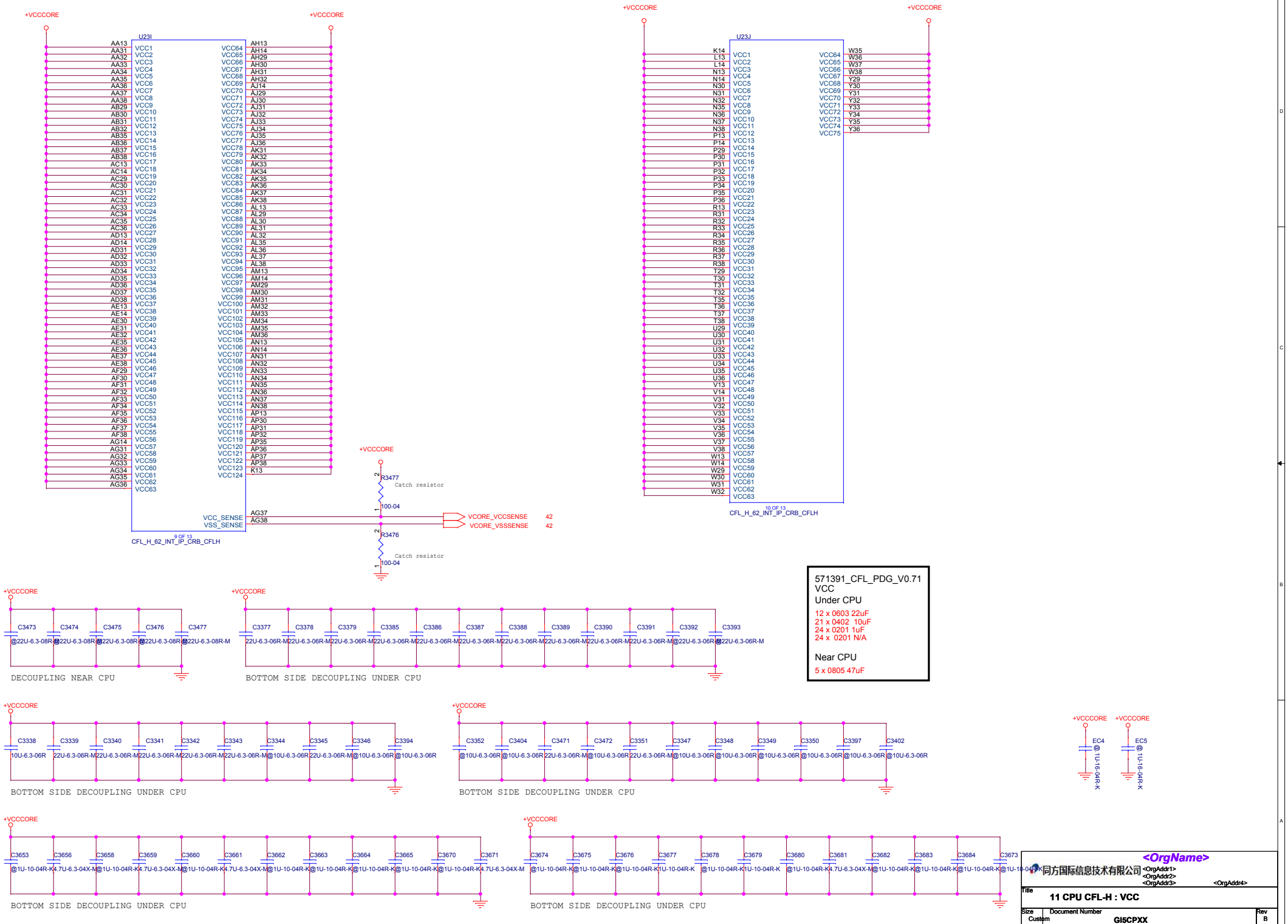
<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

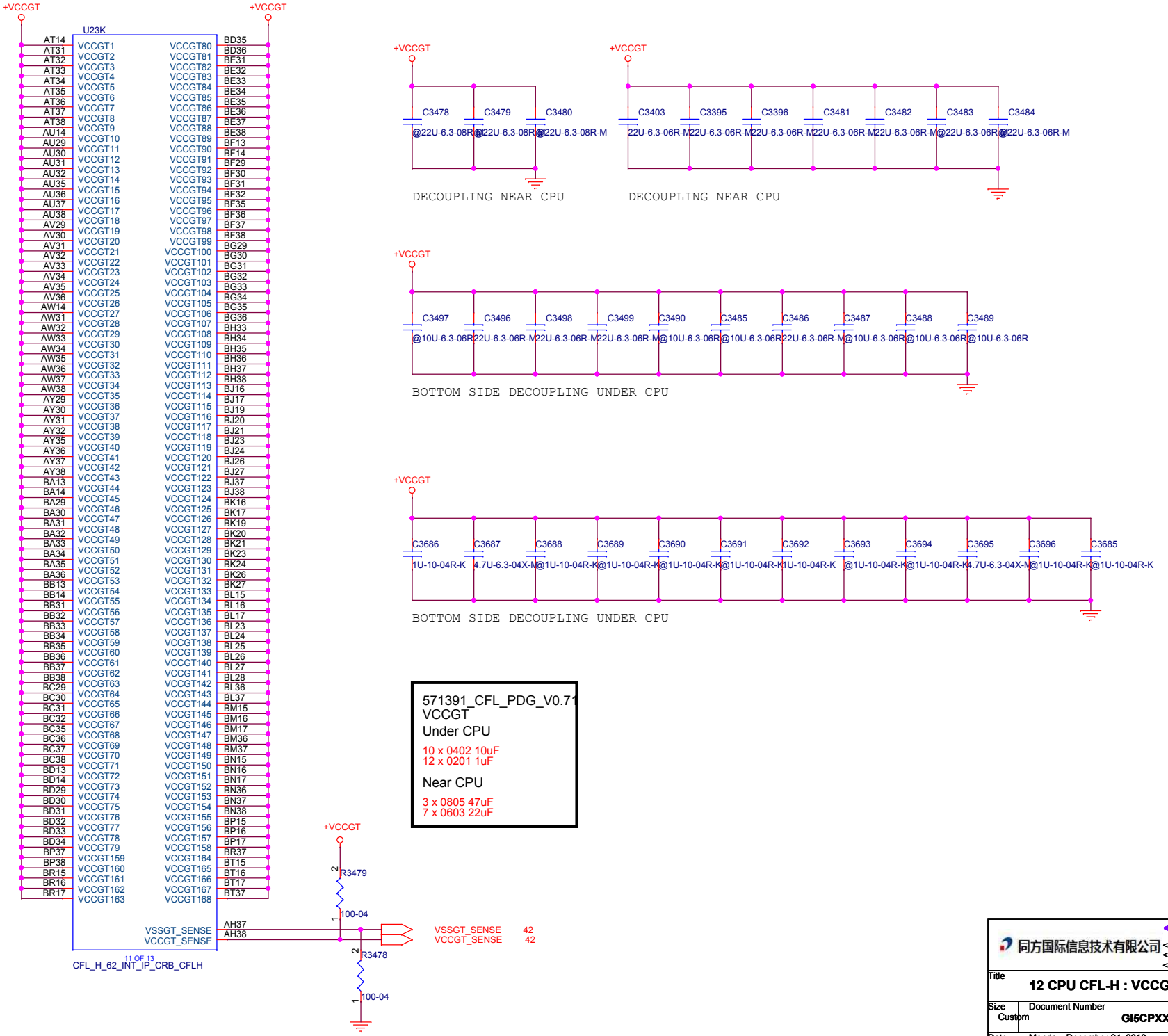
Title	09 CPU CFL-H: MISC/CLK/JTAG/CFG	
Size B	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 9 of 65	



<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

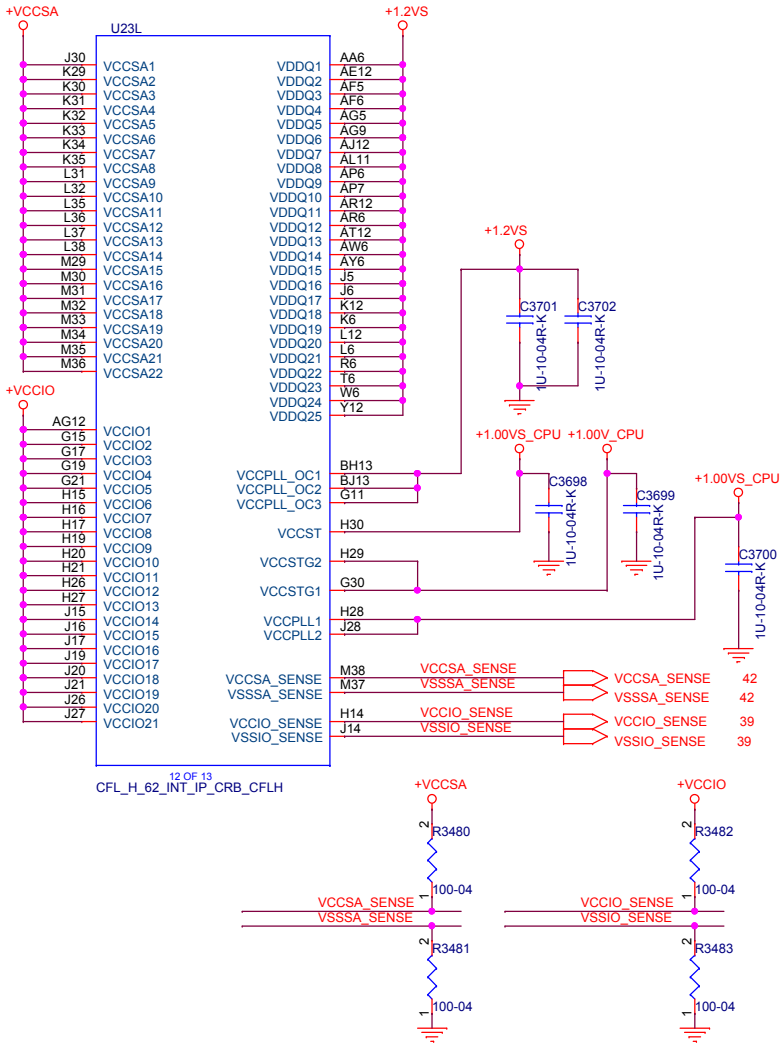
Title	10 CPU CFL-H : GND	
Size B	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 10 of 65	

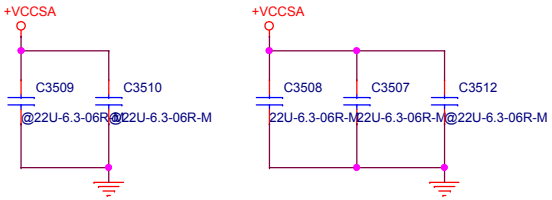

+VCCCORE
U23I
CFL_H_62_INT_IP_CRB_CFLH
9 OF 13
VCC_SENSE
VSS_SENSE
AG37
AG38
VCORE_VCCSENSE
VCORE_VSSSENSE
42
R3477
R3476
Catch resistor
100-04
U23J
CFL_H_62_INT_IP_CRB_CFLH
10 OF 13
571391_CFL_PDG_V0.71
VCC
Under CPU
12 x 0603 22uF
21 x 0402 10uF
24 x 0201 1uF
24 x 0201 N/A
Near CPU
5 x 0805 47uF
DECOUPLING NEAR CPU
BOTTOM SIDE DECOUPLING UNDER CPU
EC4
EC5
@1U-16-04R-K
<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>
Title
11 CPU CFL-H : VCC
Size
Custom
Document Number
GI5CPXX
Rev
B
Date:
Monday, December 24, 2018
Sheet
11
of
65

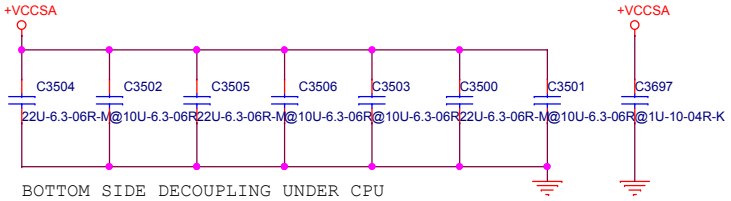


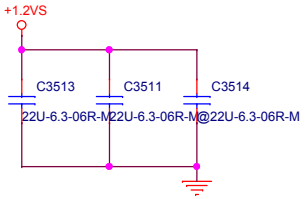
<OrgName>
同方国际信息技术有限公司 <OrgAddr1>
<OrgAddr2>
<OrgAddr3> <OrgAddr4>

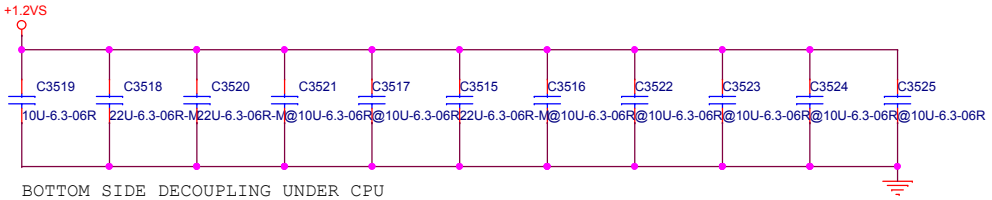
Title	12 CPU CFL-H : VCCGT	
Size: Custom	Document Number: GI5CPXX	Rev: B
Date: Monday, December 24, 2018	Sheet 12 of 65	

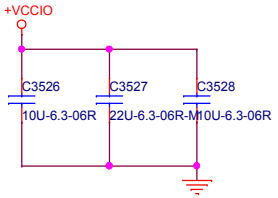












571391_CFL_PDG_V0.71

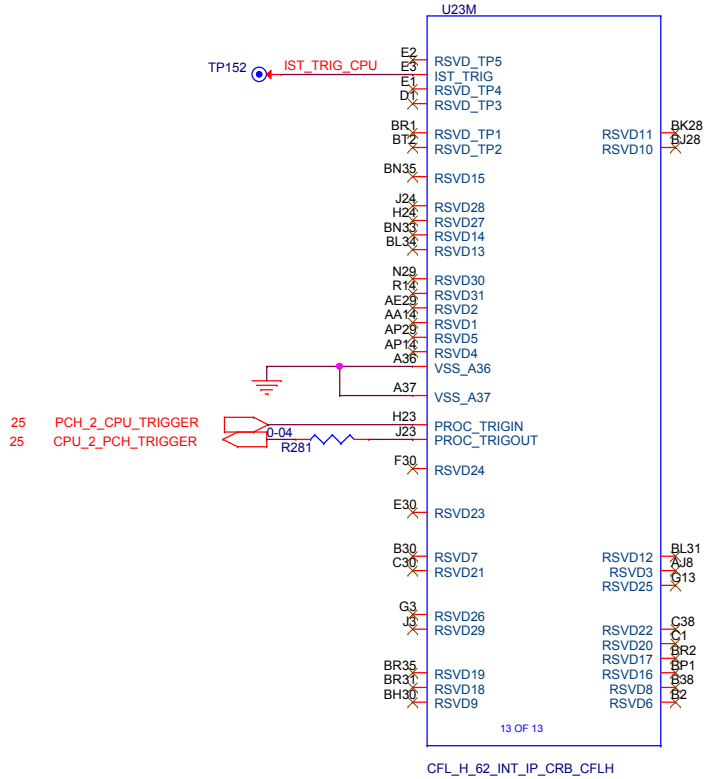
VCCSA	VCCST
Under CPU	Under CPU
7 x 0402 10uF 1 x 0201 1uF	1 x 0201 1uF
Near CPU	VCCSTG
2 x 0805 47uF 2 x 0603 22uF	Under CPU
	1 x 0201 1uF
VDDQ	
Under CPU	VCCPLL
4 x 0603 22uF 11 x 0402 10uF	Under CPU
	1 x 0201 1uF
VCCIO	
Under CPU	VCCPLL_OC
3 x 0402 10uF 3 x 0402 N/A	Under CPU
	2 x 0201 1uF

<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 13 CPU CFL-H : VCCSA/VCCIO/VDDQ

Size: B | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 13 of 65



<OrgName>
同方国际信息技术有限公司 <OrgAddr1>
<OrgAddr2>
<OrgAddr3> <OrgAddr4>

Title
14 CPU CFL-H : TRIG/RSVD

Size	Document Number	Rev
B	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 14 of 65

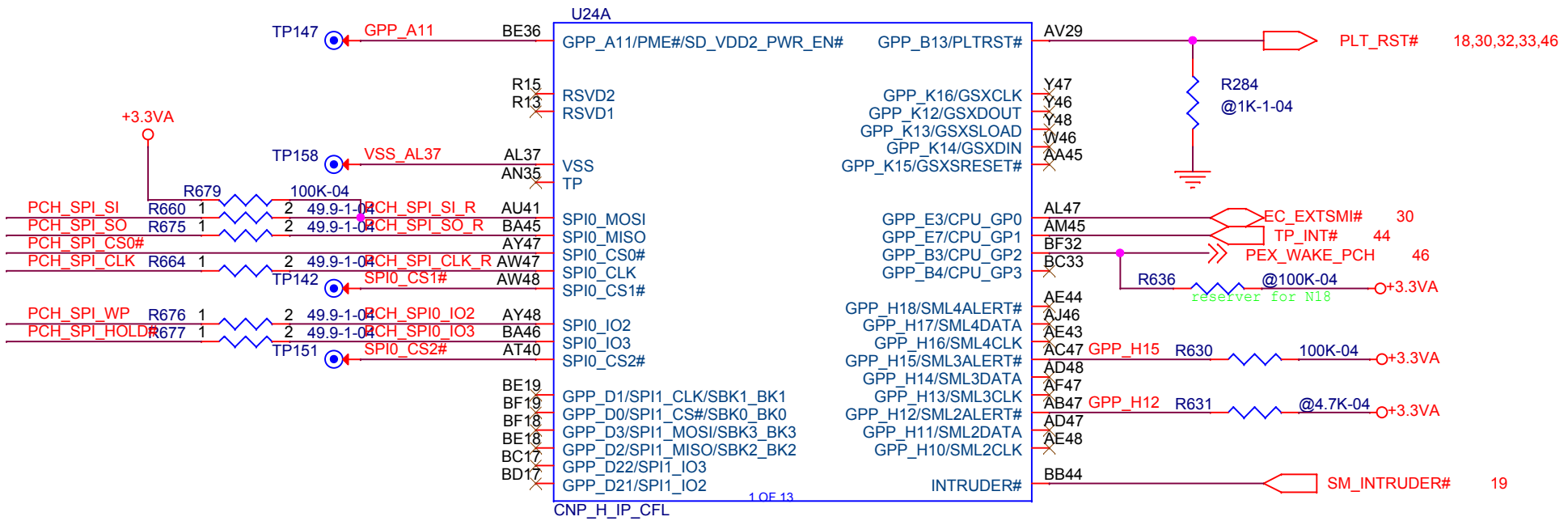
同方国际信息技术有限公司
<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title
15 RSVD1

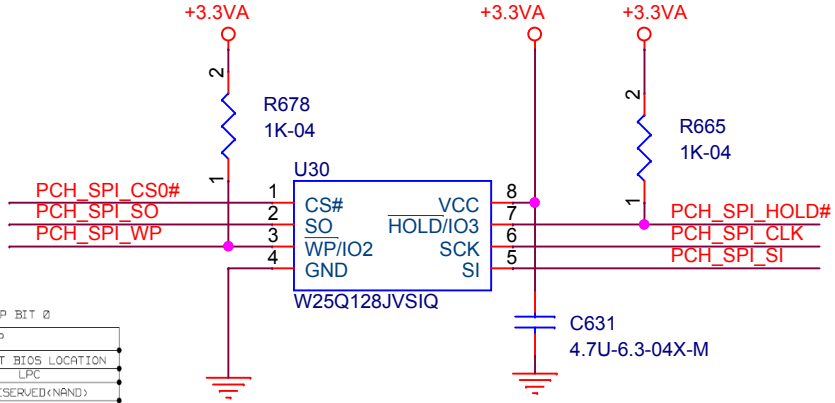
Size	Document Number	Rev
A	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 15 of 65

GPP_H15 External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.



GPP_H12 eSPI Flash Sharing Mode
0:Master Attached Flash Sharing (MAFS) enabled (internal pull down)
1:Slave Attached Flash Sharing (SAFS) enabled



BBS_BIT0 - BIOS BOOT STRAP BIT 0

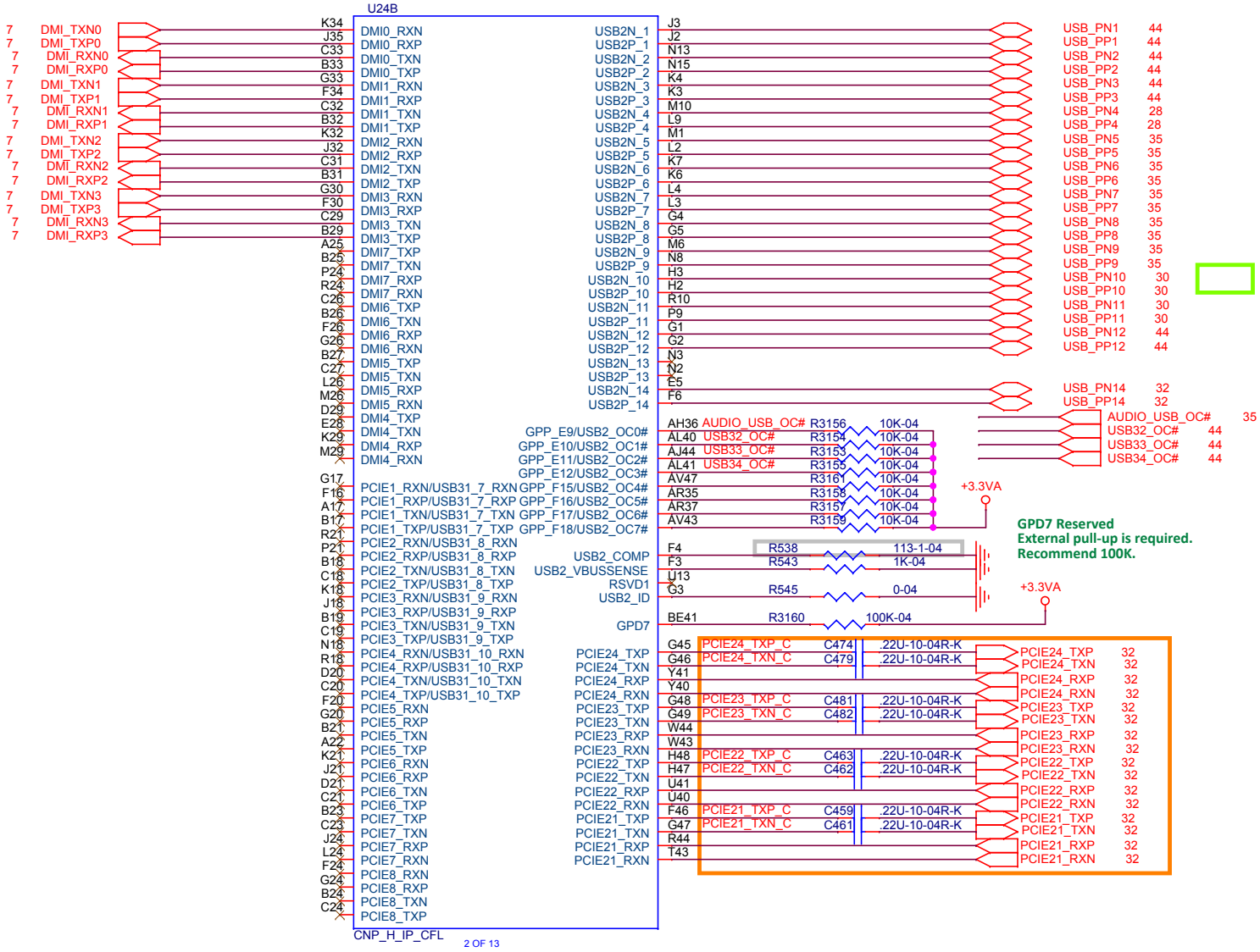
BOOT BIOS STRAP		
BBS_BIT1	BBS_BIT0	BOOT BIOS LOCATION
0	0	LPC
0	1	RESERVED(NAND)
1	0	----
1	1	SPI

<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title: 16 PCH CFL-H : SPI

Size	Document Number	Rev
A	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 16 of 65



USB2.0 Configuration Table	
USB1	USB3.0 Port1
USB2	USB3.0 Port2
USB3	TYPE-C Port1
USB4	Web Camera
USB5	ID6 USB DB Port1
USB6	USB to SD (Reserved)
USB7	Audio DB Port1
USB8	ID6 USB DB Port2
USB9	Audio DB Port2
USB10	ME Keyboard used
USB11	ME Keyboard LED used
USB12	TYPE-C Port1
USB13	N/A
USB14	Bluetooth

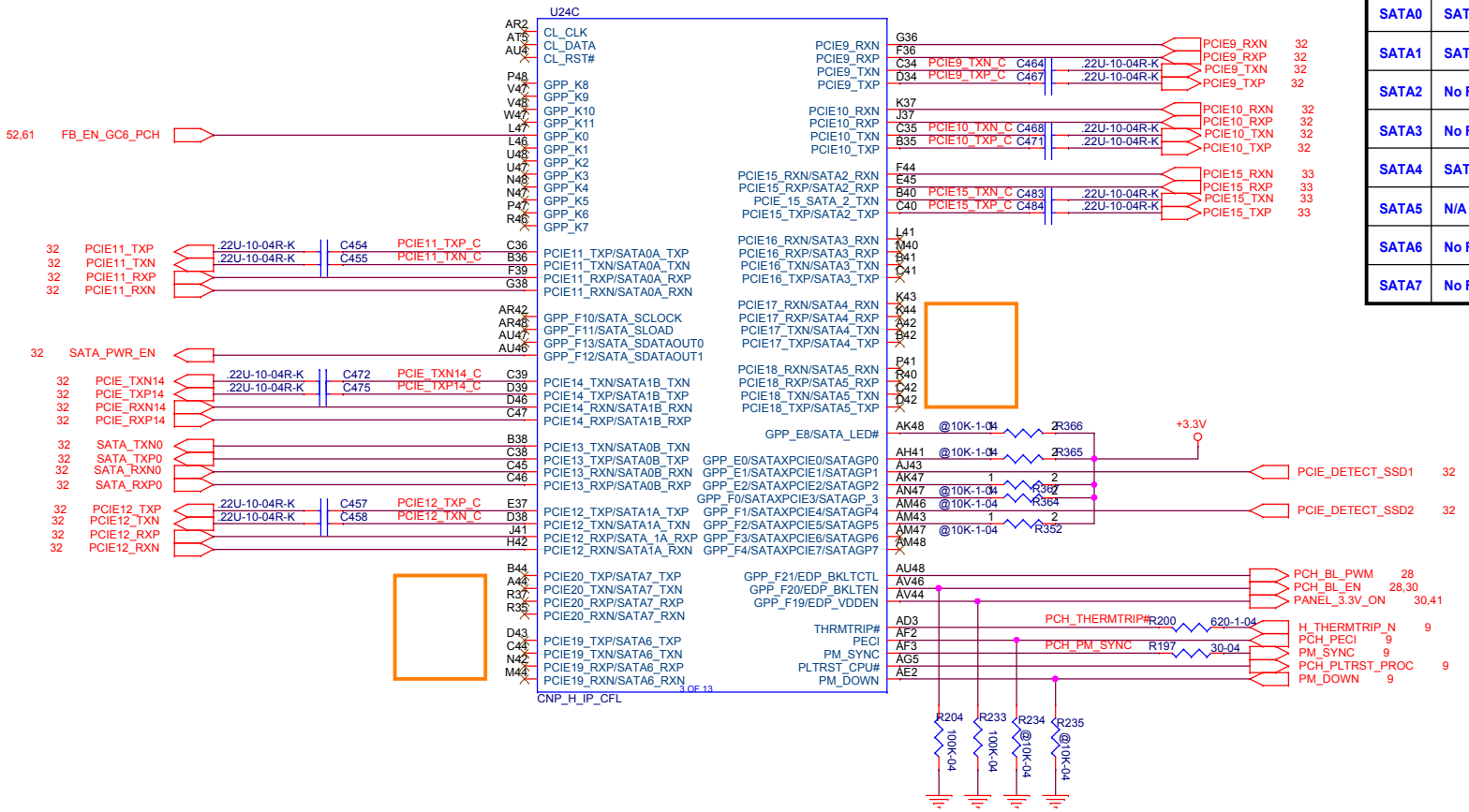
USB OC Configuration Table	
OC0	Audio DB Port1&2
OC1	USB3.0 Port1
OC2	USB3.0 Port2
OC3	TYPE-C Port1
OC4	N/A
OC5	N/A
OC6	N/A
OC7	N/A

<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 17 PCH CFL-H : DMI/USB2.0/PCIE

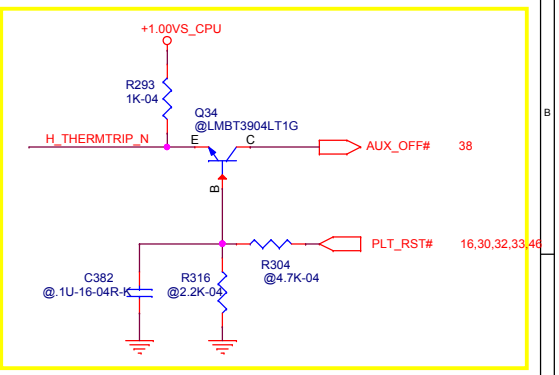
Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 17 of 65



SATA Configuration Table	
SATA0	SATA HDD
SATA1	SATA SSD1
SATA2	No Function
SATA3	No Function
SATA4	SATA SSD2
SATA5	N/A
SATA6	No Function
SATA7	No Function

PCIE Configuration Table			
PCIE1	No function	PCIE13	N/A
PCIE2	No function	PCIE14	WLAN
PCIE3	No function	PCIE15	LAN
PCIE4	No function	PCIE16	N/A
PCIE5	No function	PCIE17	PCIE SSD2
PCIE6	No function	PCIE18	PCIE SSD2
PCIE7	No function	PCIE19	PCIE SSD2
PCIE8	No function	PCIE20	PCIE SSD2
PCIE9	PCIE SSD1	PCIE21	N/A
PCIE10	PCIE SSD1	PCIE22	N/A
PCIE11	PCIE SSD1	PCIE23	N/A
PCIE12	PCIE SSD1	PCIE24	N/A

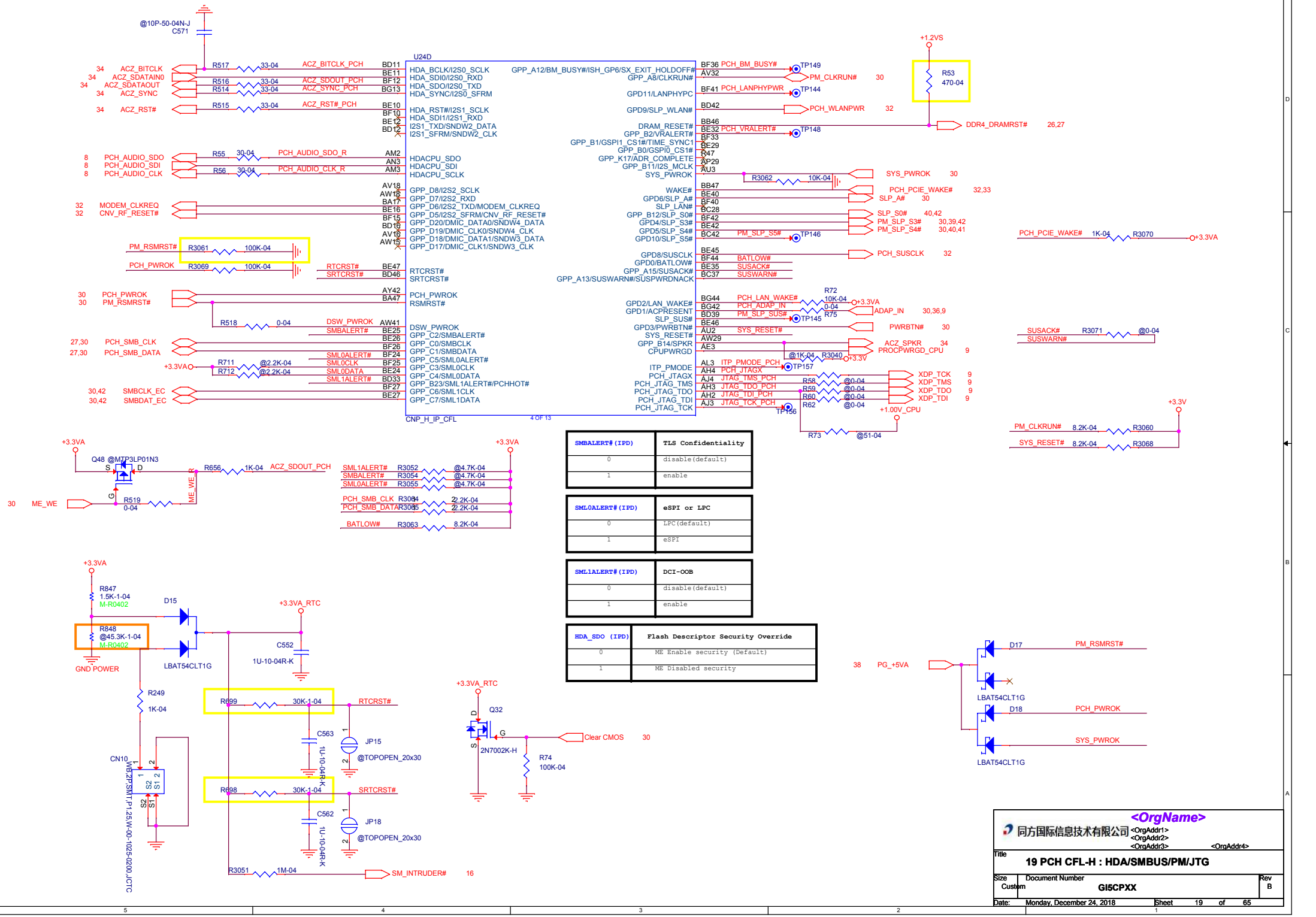


<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 18 PCH CFL-H : SATA/PCIE

Size	Document Number	Rev
Custom	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 18 of 65



SMBALERT#(IPD)	TLS Confidentiality
0	disable(default)
1	enable

SML0ALERT#(IPD)	eSPI or LPC
0	LPC(default)
1	eSPI

SML1ALERT#(IPD)	DCI-OOB
0	disable(default)
1	enable

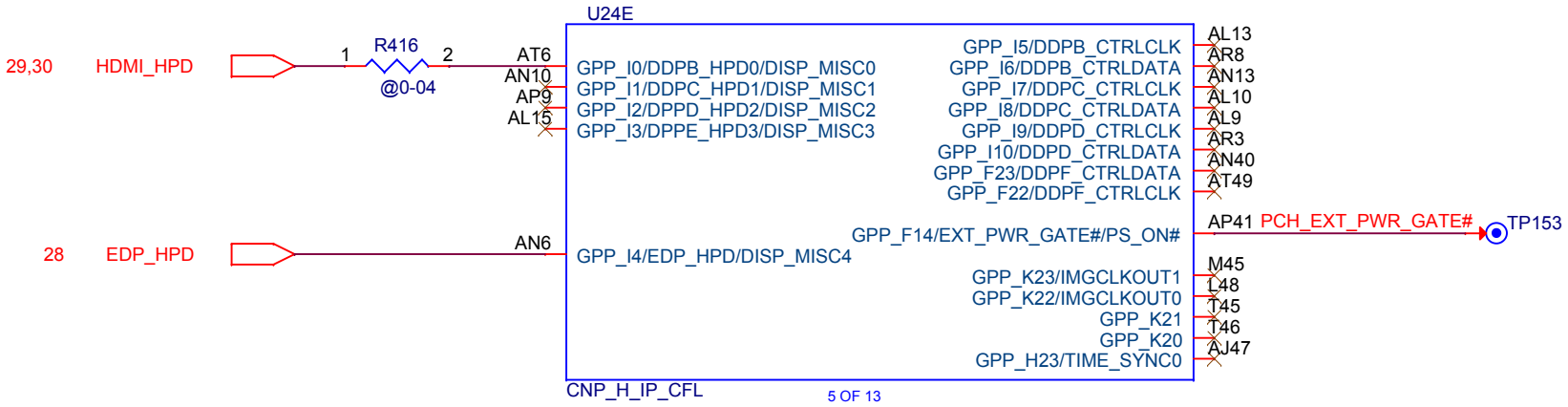
HDA_SDO (IPD)	Flash Descriptor Security Override
0	ME Enable security (Default)
1	ME Disabled security

<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title: 19 PCH CFL-H : HDA/SMBUS/PM/JTG

Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 19 of 65



<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title
20 PCH CFL-H : DDI CONTROL

Size	Document Number	Rev
A	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 20 of 65

Change +3.3V to 3VS in order to prevent leakage to +3.3V under S3
RC_IN : VSTBY power plane in EC

INT_SERIRQ R334 10K-04 +3.3V
H_RCIN# R354 @10K-04 +3.3VS
SMI# R355 4.7K-04 +3.3V
PIRQA# R356 10K-04 +3.3V

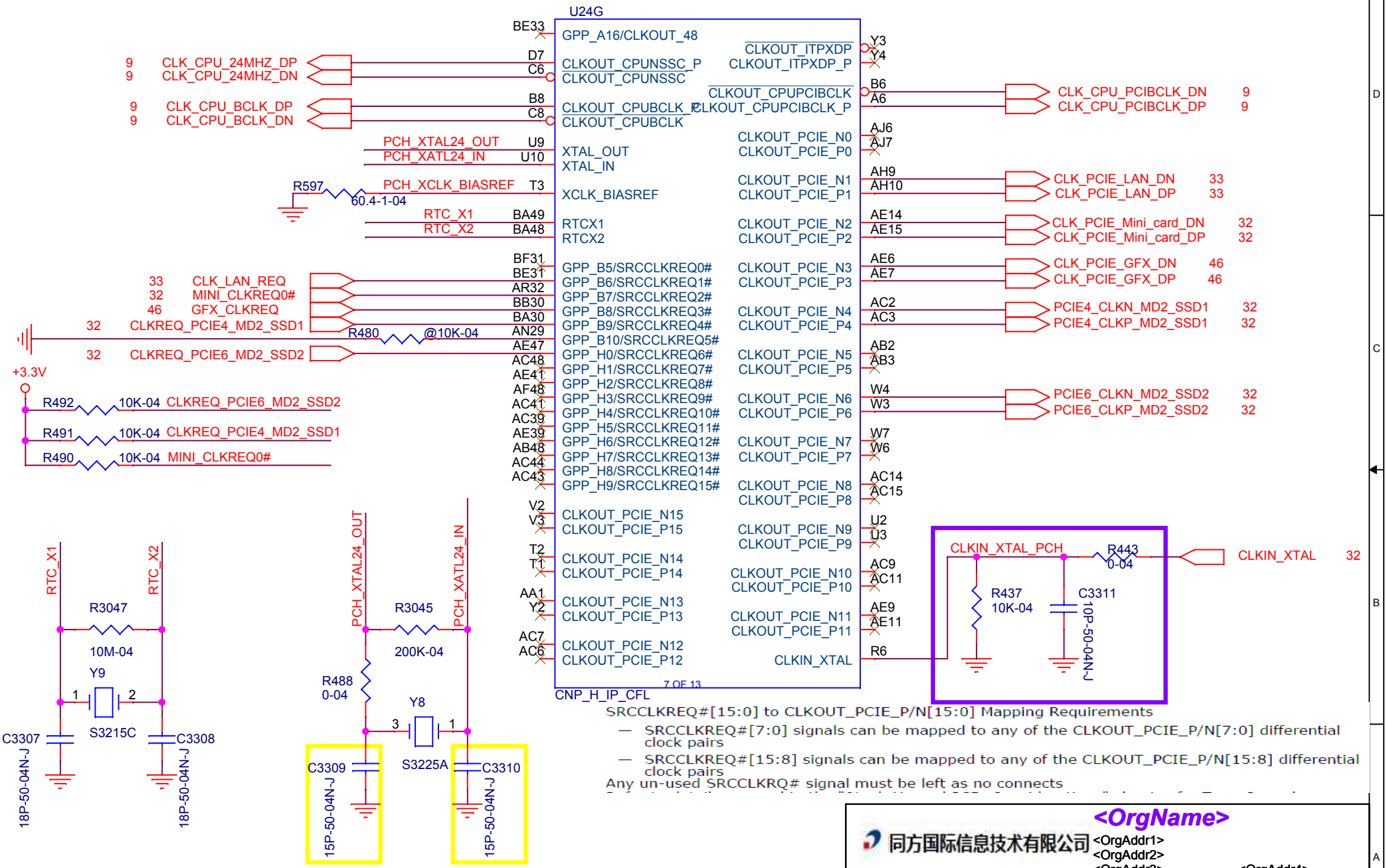
USB3.0 Configuration Table	
USB3_1	USB3.0 Port1
USB3_2	USB3.0 Port2
USB3_3	TYPE-C Port1
USB3_4	TYPE-C Port1
USB3_5	N/A
USB3_6	N/A
USB3_7	N/A
USB3_8	N/A
USB3_9	No Function
USB3_10	No Function

<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 21 PCH CFL-H : USB3.0/LPC

Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 21 of 65



<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

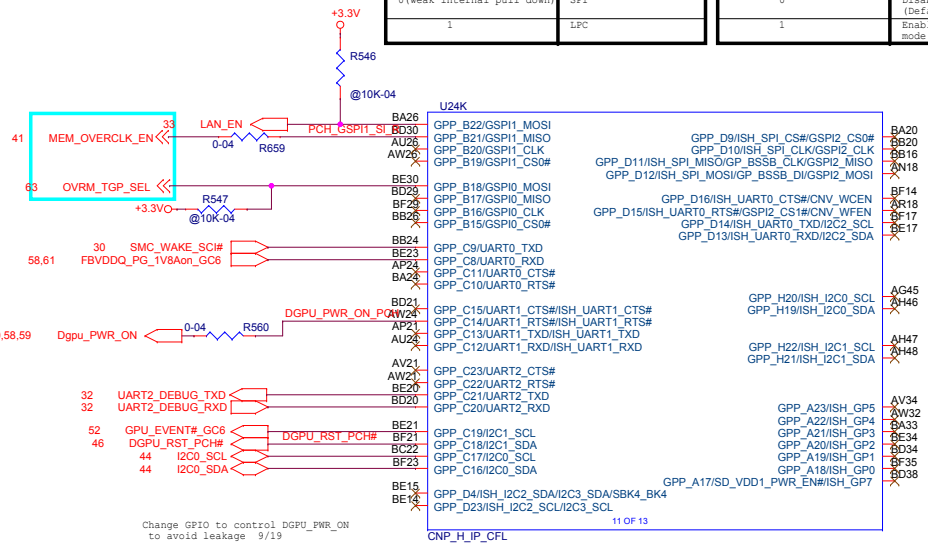
Title: **22 PCH CFL-H : CLK**

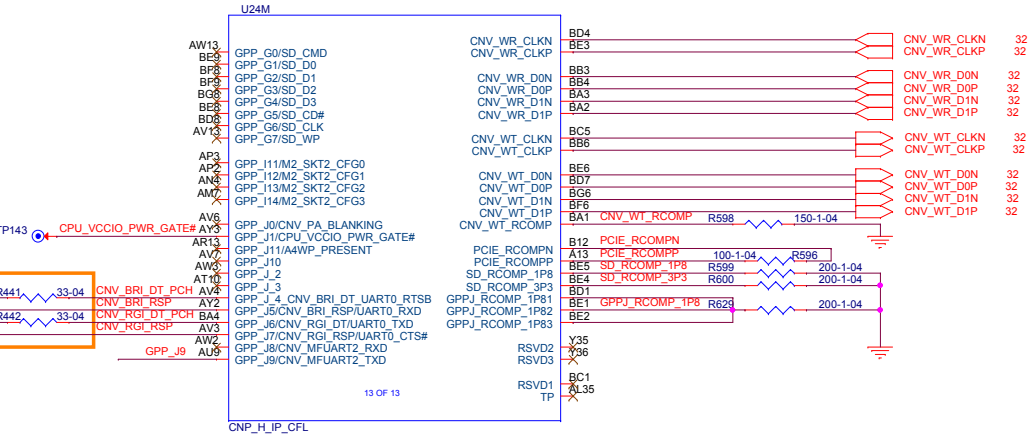
Size	Document Number	Rev
A	GI5CPXX	B

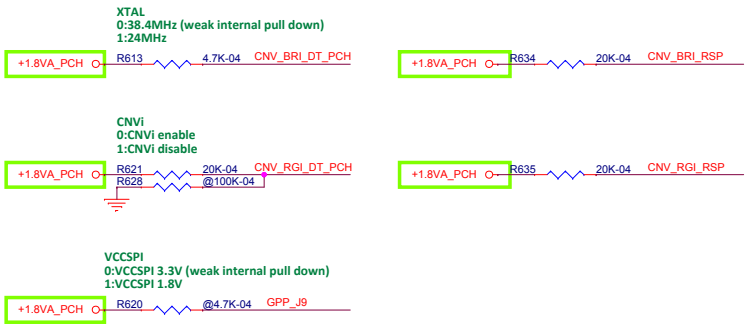
Date: Monday, December 24, 2018 Sheet 22 of 65

GPP_B22/GSPI1_MOSI(IPD)	Boot BIOS Strap Bit
0(weak internal pull down)	SPI
1	LPC

GPP_B18/GSPI0_MOSI(IPD)	No Reboot
0	Disable "No Reboot" mode. (Default)
1	Enable "No Reboot" mode





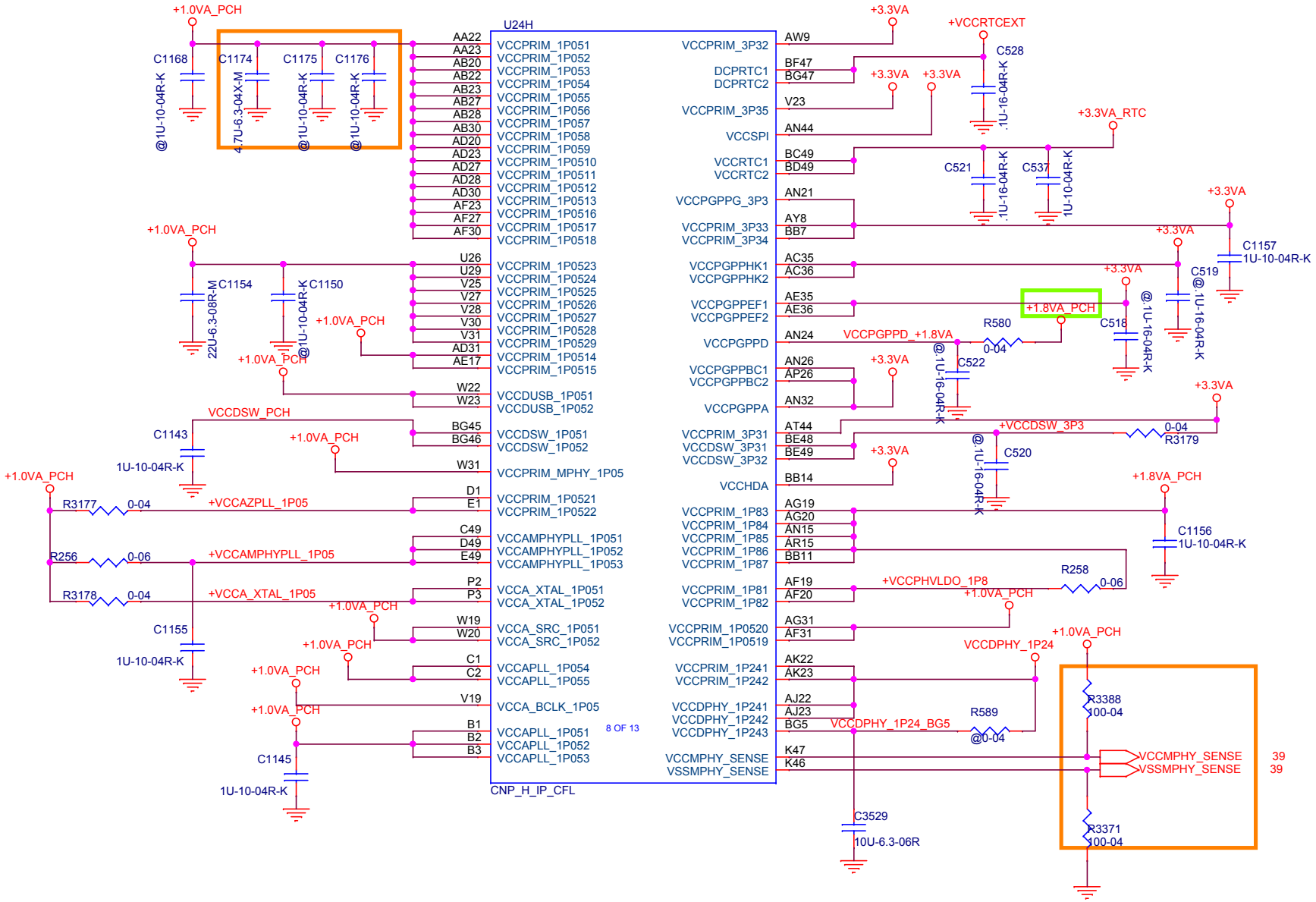


<OrgName>
同方国际信息技术有限公司 <OrgAddr1>
<OrgAddr2>
<OrgAddr3> <OrgAddr4>

Title: 23 PCH CFL-H:GSPI/UART/I2C/CNVi

Size	Document Number	Rev
Custom	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 23 of 65



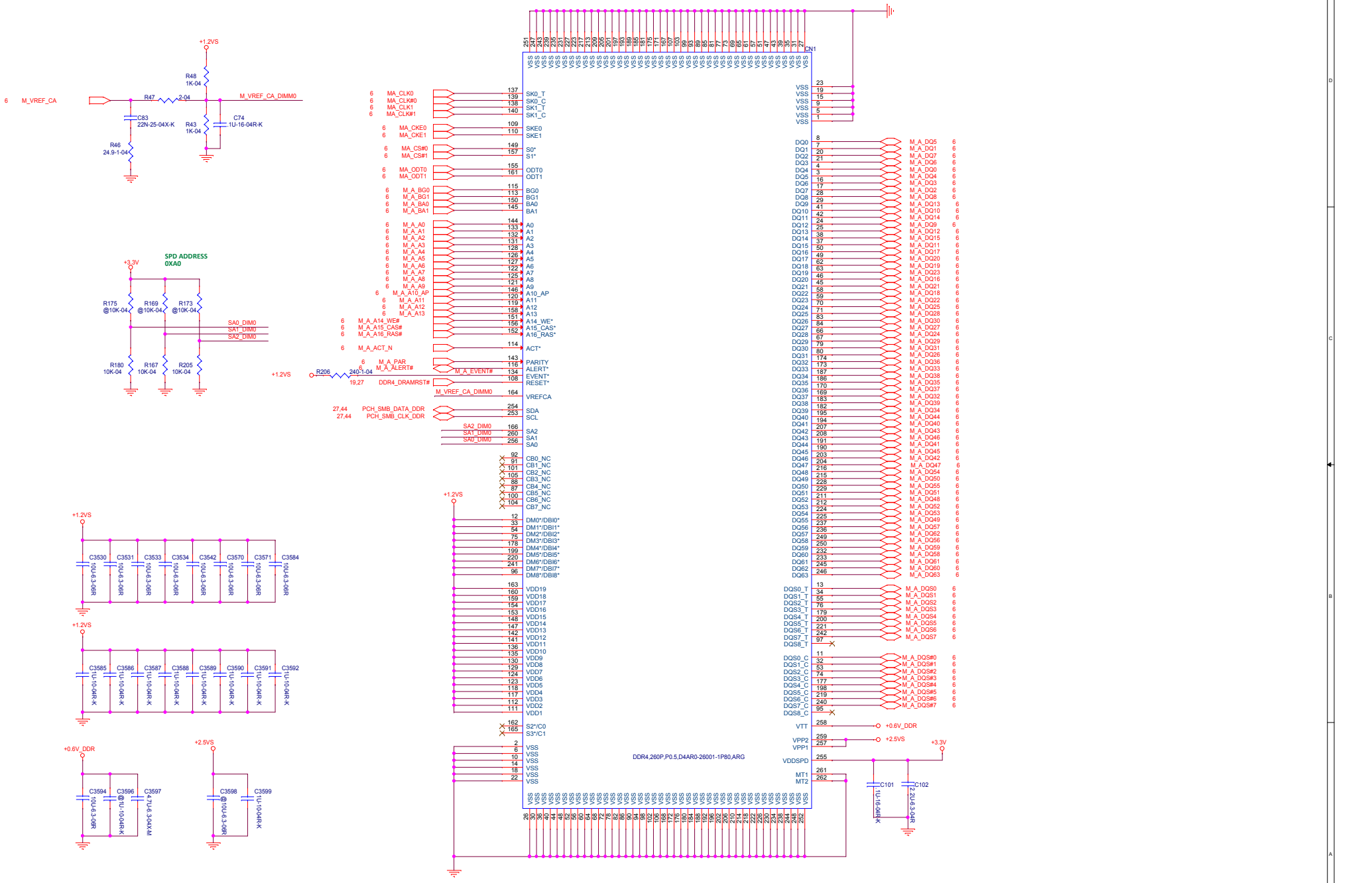
<OrgName>			
同方国际信息技术有限公司	<OrgAddr1> <OrgAddr2> <OrgAddr3>		<OrgAddr4>
Title	24 PCH CFL-H : POWER		
Size: Custom	Document Number: GI5CPXX		Rev: B
Date: Monday, December 24, 2018	Sheet 24 of 65		

<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title
25 PCH CFL-H : GND/RSVD

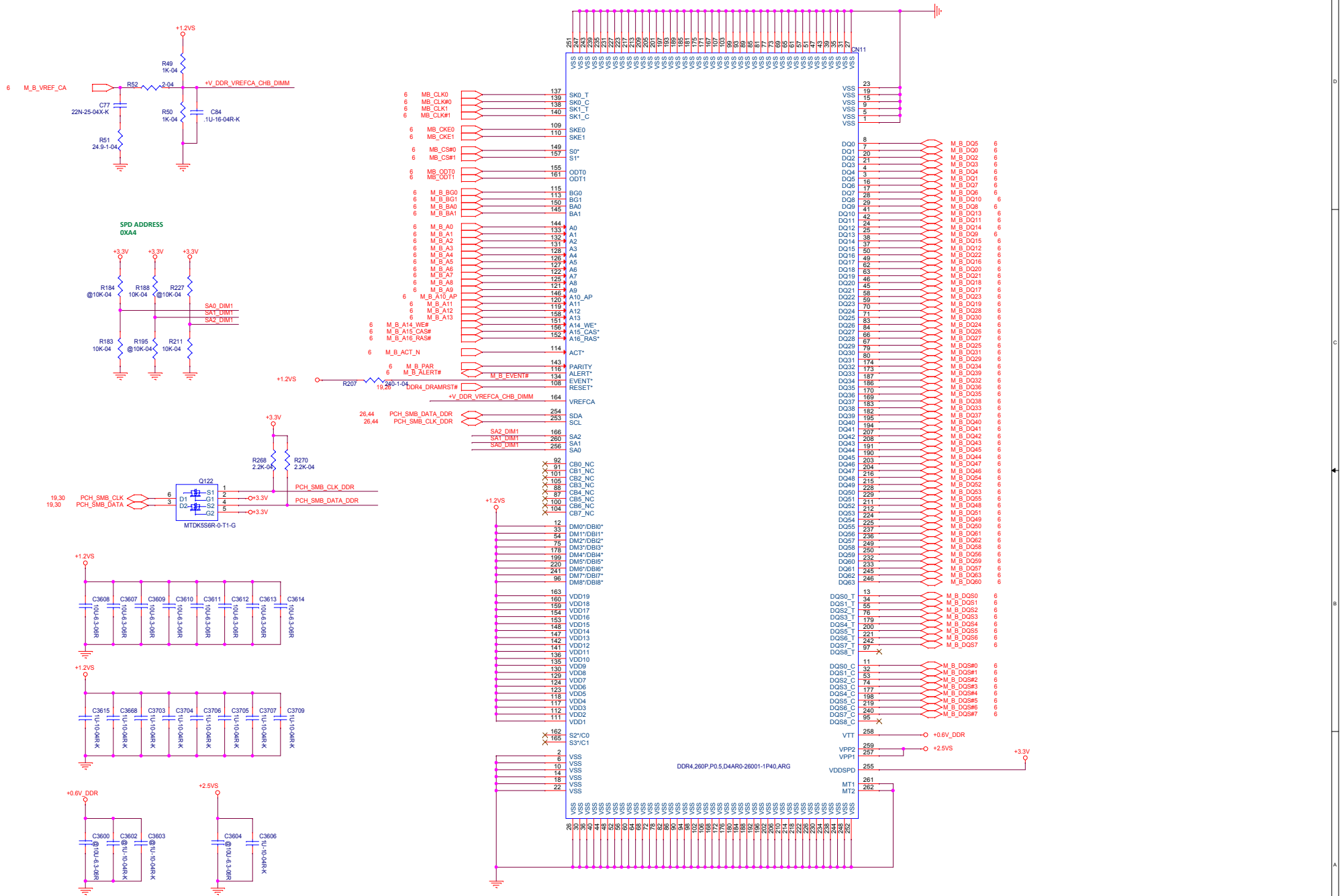
Size	Document Number	Rev
Custom	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 25 of 65



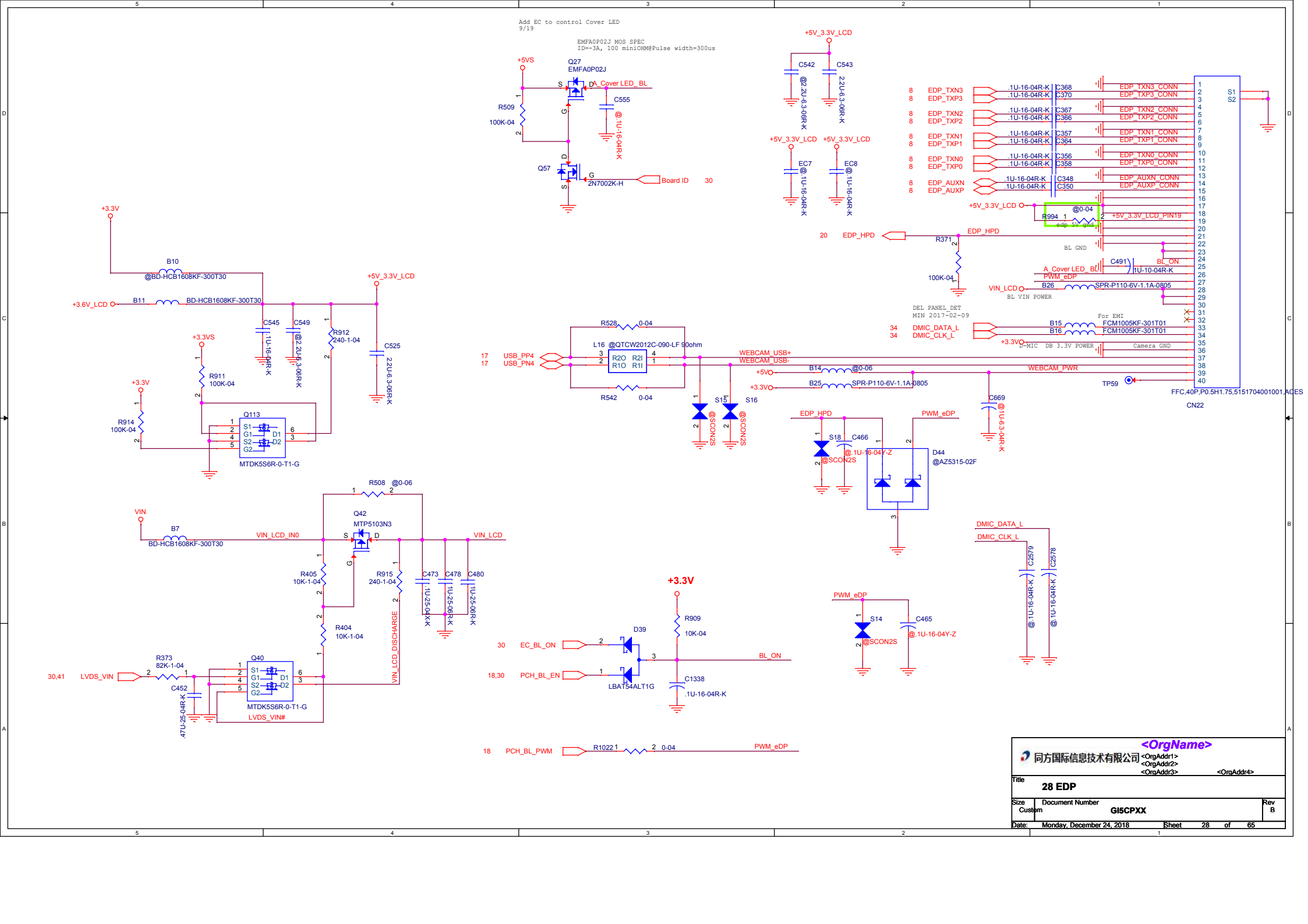
<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title	26 DDR4 SODIMM-A	
Size C	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 26 of 65	



<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

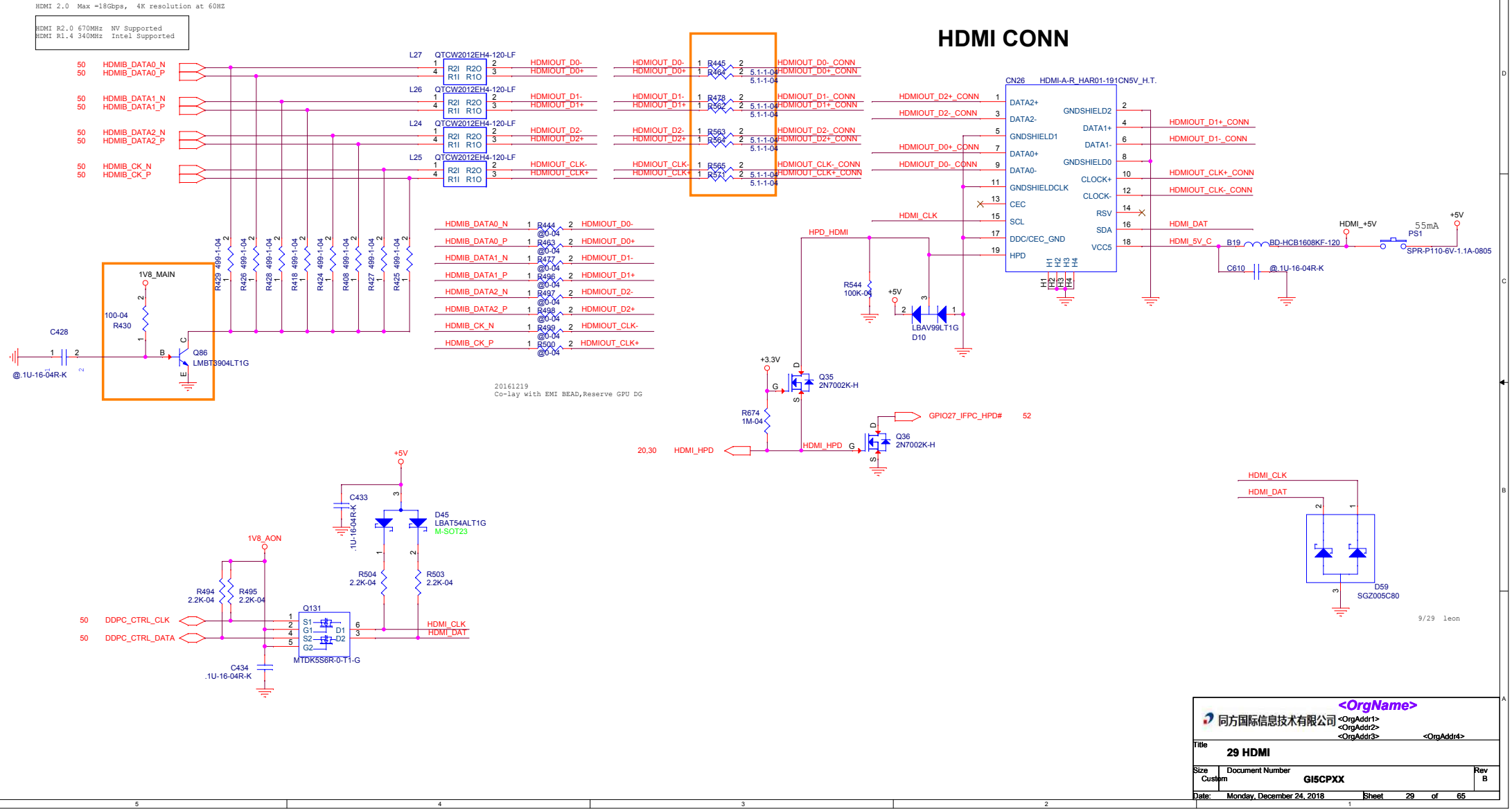
Title	27 DDR4 SODIMM-B	
Size C	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 27 of 65	


Add EC to control Cover LED
9/19
EMFA0P02J MOS SPEC
ID=-3A, 100 miniOHM@Pulse width=300us
Q27
EMFA0P02J
A_Cover LED_ BL
Board ID
30
Q57
2N7002K-H
+5V_3.3V_LCD
EDP_HPD
20
EDP_TXN3
EDP_TXP3
EDP_TXN2
EDP_TXP2
EDP_TXN1
EDP_TXP1
EDP_TXN0
EDP_TXP0
EDP_AUXN
EDP_AUXP
EDP_TXN3_CONN
EDP_TXP3_CONN
EDP_TXN2_CONN
EDP_TXP2_CONN
EDP_TXN1_CONN
EDP_TXP1_CONN
EDP_TXN0_CONN
EDP_TXP0_CONN
EDP_AUXN_CONN
EDP_AUXP_CONN
+5V_3.3V_LCD_PIN19
BL GND
BL_ON
PWM_eDP
VIN_LCD
BL VIN POWER
DEL PANEL_DET
MIN 2017-02-09
For EMI
DMIC_DATA_L
DMIC_CLK_L
B-MIC
DB 3.3V POWER
Camera GND
WEBCAM_USB+
WEBCAM_USB-
WEBCAM_PWR
TP59
FFC,40P,P0.5H1.75,5151704001001,ACES
CN22
+3.3V
+3.6V_LCD
+3.3VS
B10
@BD-HCB1608KF-300T30
B11
BD-HCB1608KF-300T30
C545
C549
R912
240-1-04
C525
2.2U-6.3-06R-K
R911
100K-04
R914
100K-04
Q113
MTDK5S6R-0-T1-G
R528
0-04
L16 @QTCW2012C-090-LF 90ohm
R542
0-04
USB_PP4
USB_PN4
S15
S16
@SCON2S
B14
@0-06
B25
SPR-P110-6V-1.1A-0805
C669
@1U-6.3-04R-K
S18
C466
@1U-16-04Y-Z
D44
@AZ5315-02F
R508
@0-06
Q42
MTP5103N3
VIN
B7
BD-HCB1608KF-300T30
VIN_LCD_IN0
R405
10K-1-04
R915
240-1-04
C473
C478
C480
1U-25-04R-K
1U-25-06R-K
R404
10K-1-04
VIN_LCD_DISCHARGE
R373
82K-1-04
Q40
MTDK5S6R-0-T1-G
LVDS_VIN#
30,41
LVDS_VIN
C452
.47U-25-04R-K
+3.3V
R909
10K-04
D39
LBAT54ALT1G
C1338
.1U-16-04R-K
30
EC_BL_ON
18,30
PCH_BL_EN
BL_ON
S14
C465
@SCON2S
@.1U-16-04Y-Z
DMIC_DATA_L
DMIC_CLK_L
C2579
C2578
@.1U-16-04R-K
18
PCH_BL_PWM
R1022
0-04
PWM_eDP
<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>
Title
28 EDP
Size
Custom
Document Number
GI5CPXX
Rev
B
Date:
Monday, December 24, 2018
Sheet
28
of
65

HDMI CONN

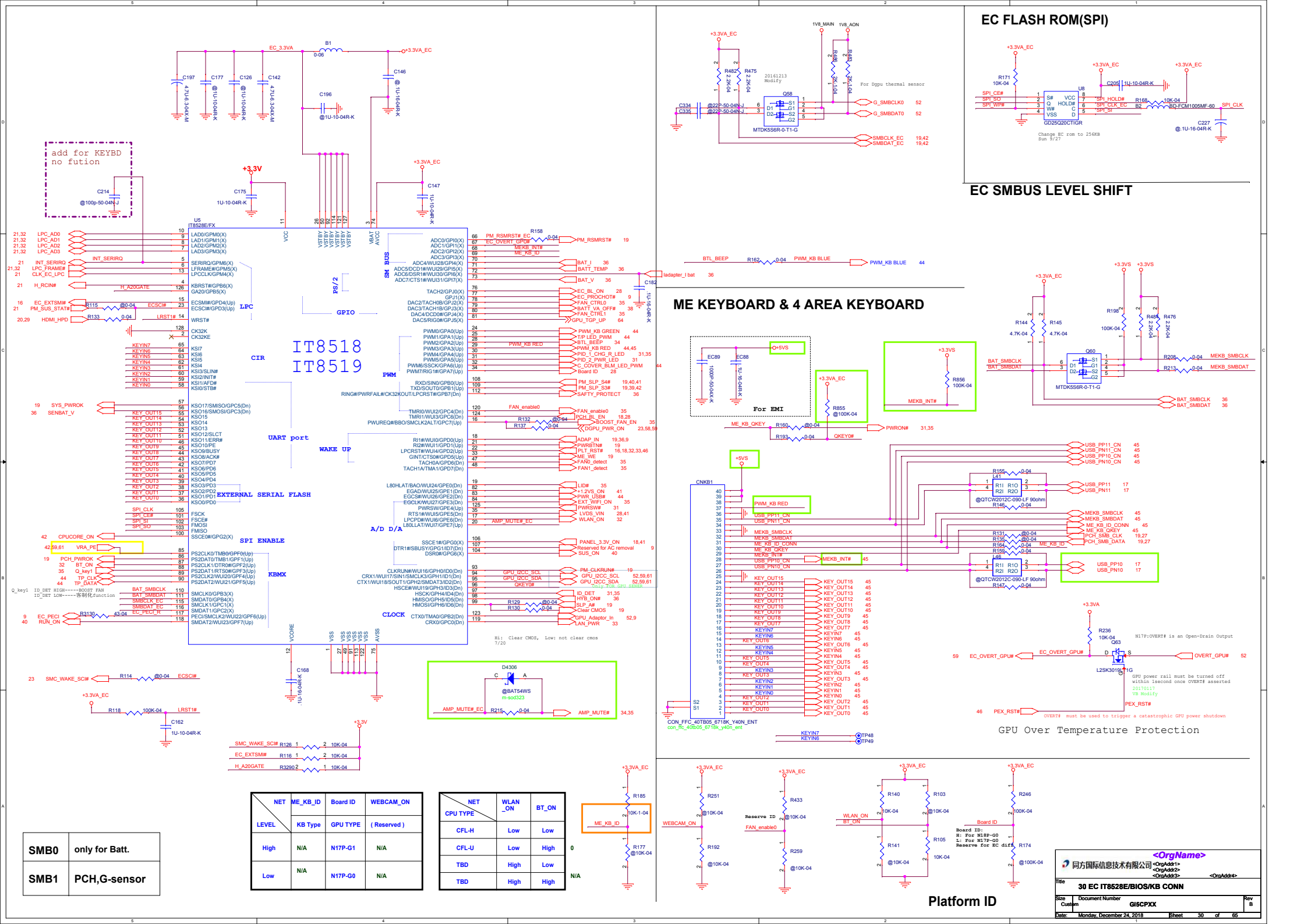
HDMI 2.0 Max =18Gbps, 4K resolution at 60HZ

HDMI R2.0 670MHz NV Supported
HDMI R1.4 340MHz Intel Supported

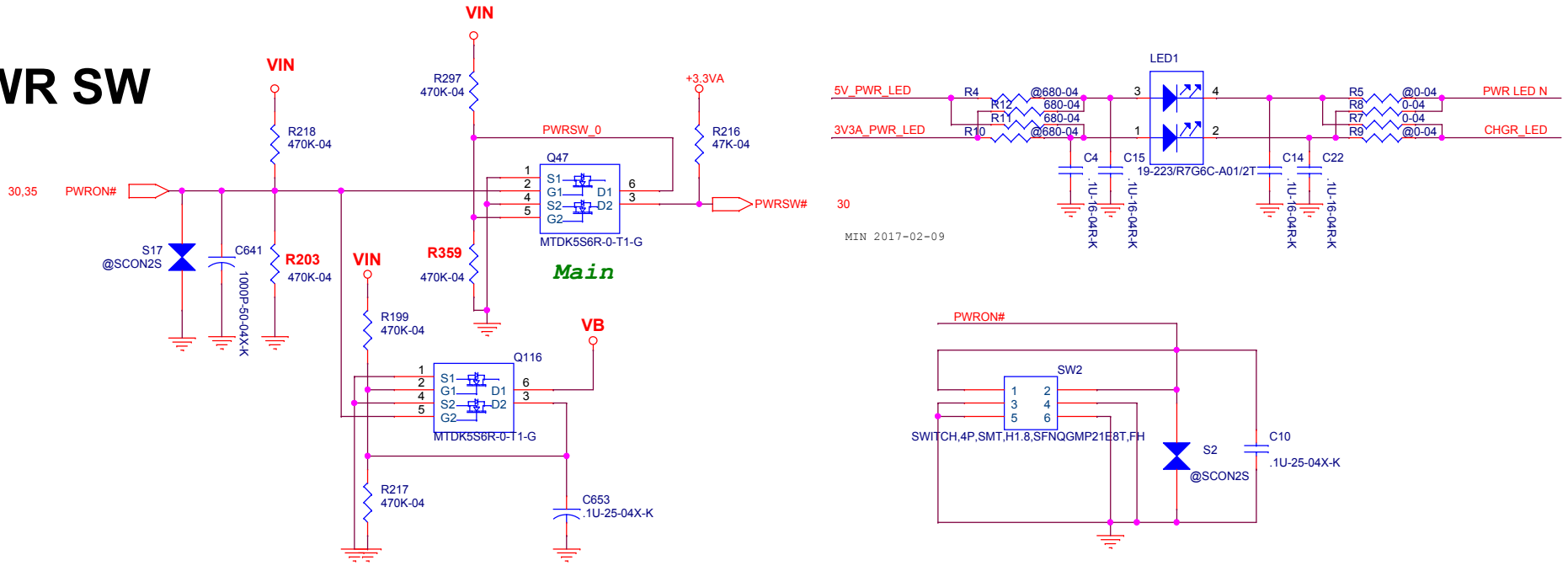


<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

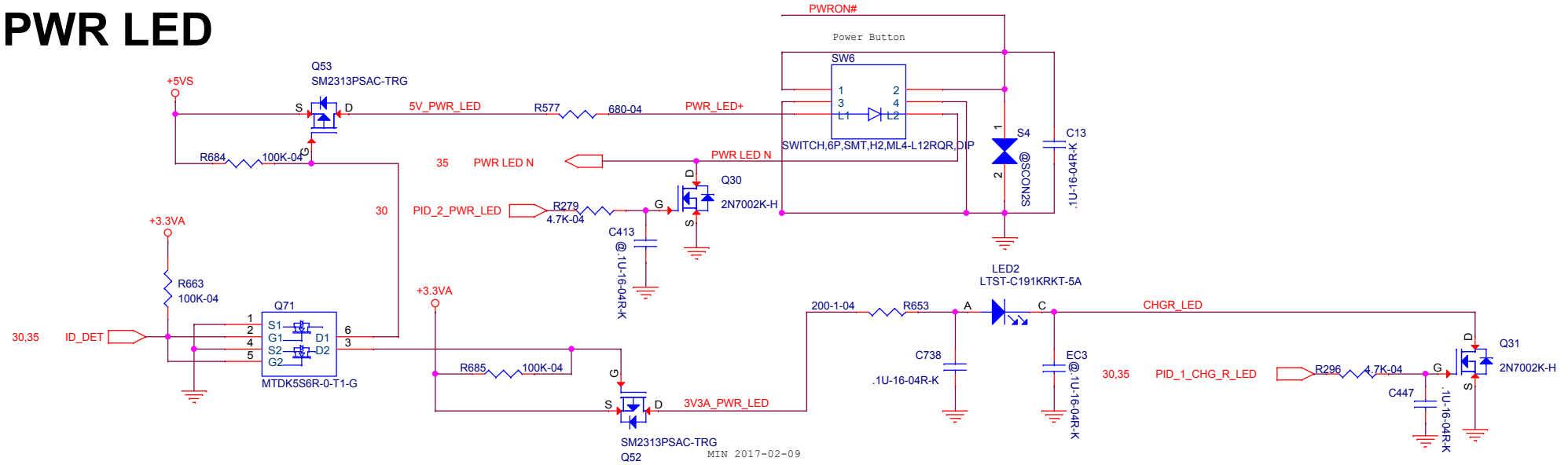
Title	29 HDMI	
Size: Custom	Document Number: GI5CPXX	Rev: B
Date: Monday, December 24, 2018	Sheet 29 of 65	


EC FLASH ROM(SPI)
EC SMBUS LEVEL SHIFT
ME KEYBOARD & 4 AREA KEYBOARD
IT8518
IT8519
add for KEYBD
no futions
U5
IT8528E/FX
LPC
PS/2
GPIO
SM BUS
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
A/D D/A
SPI ENABLE
KBMX
CLOCK
For EMI
GPU Over Temperature Protection
Platform ID
Reserve ID
Board ID:
H: For N18P-G0
L: For N17P-G0
Reserve for EC diff
SMB0 only for Batt.
SMB1 PCH,G-sensor
<OrgName>
同方国际信息技术有限公司
30 EC IT8528E/BIOS/KB CONN
GI5CPXX
Monday, December 24, 2018
Sheet 30 of 65

PWR SW



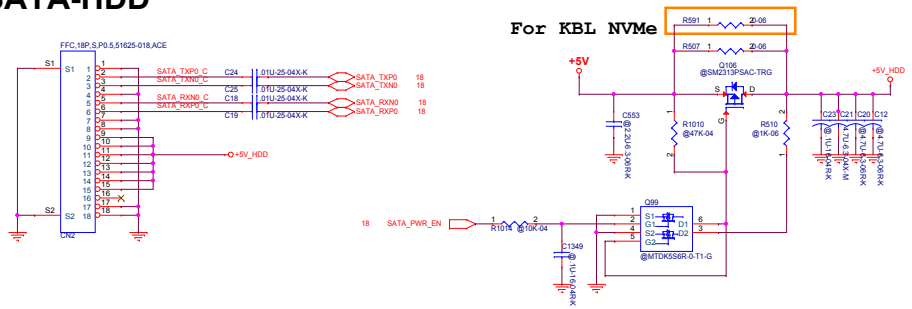
PWR LED



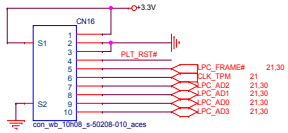
<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title	31 PSW/PWR BUTTON/LED	
Size: Custom	Document Number: GI5CPXX	Rev: B
Date: Monday, December 24, 2018	Sheet 31 of 65	

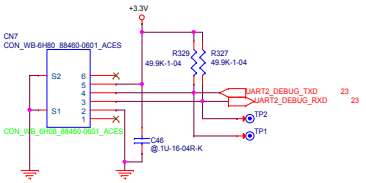
SATA-HDD



LPC debug port

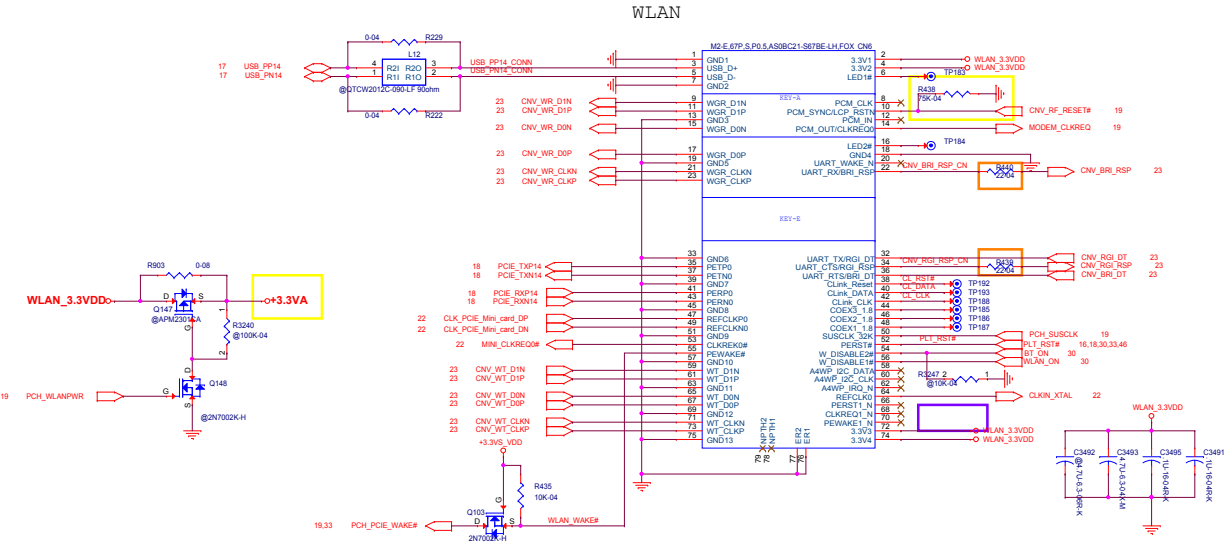


UART debug port

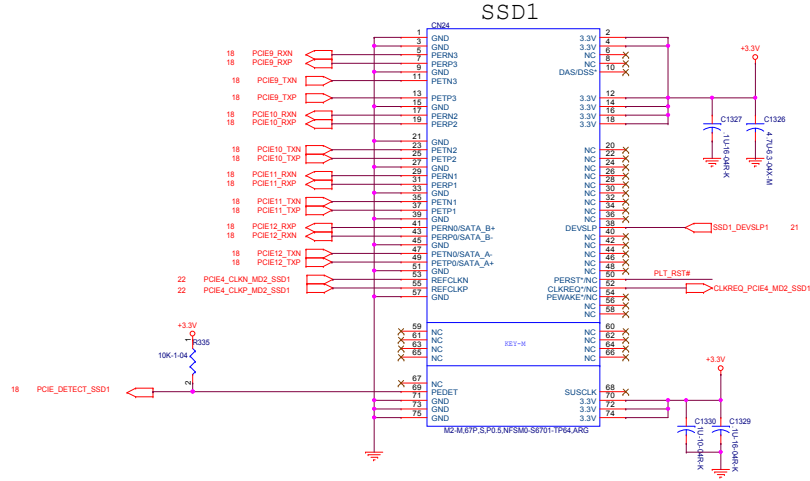


MINI CARD CONN

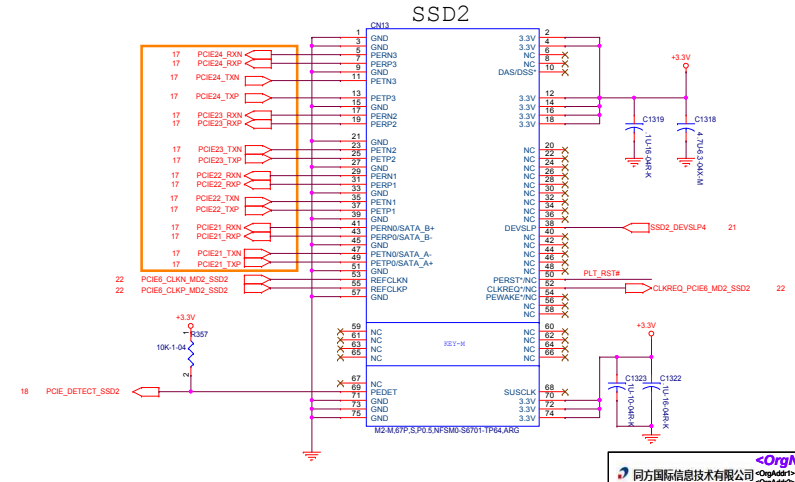
WLAN



SSD1



SSD2

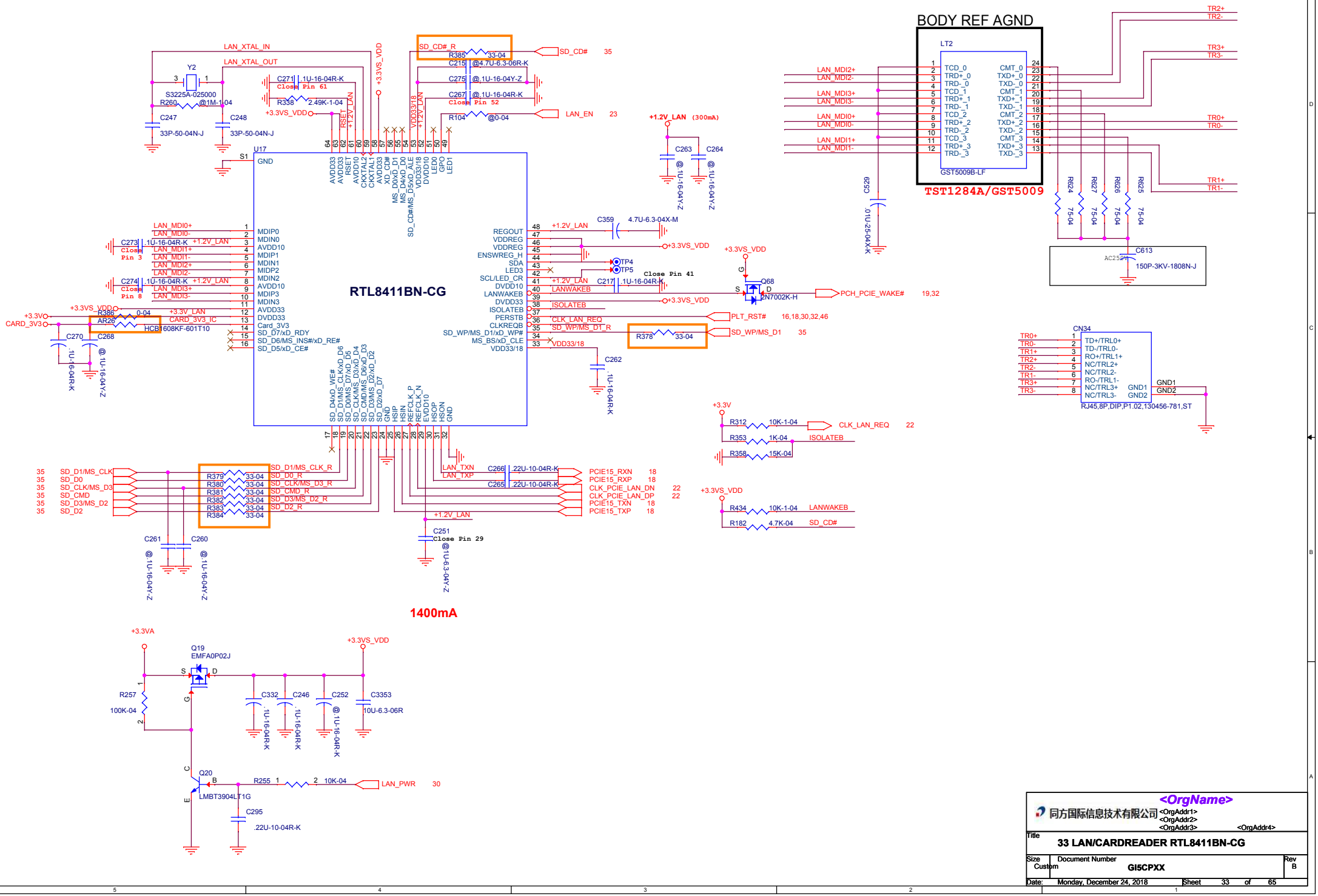


<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

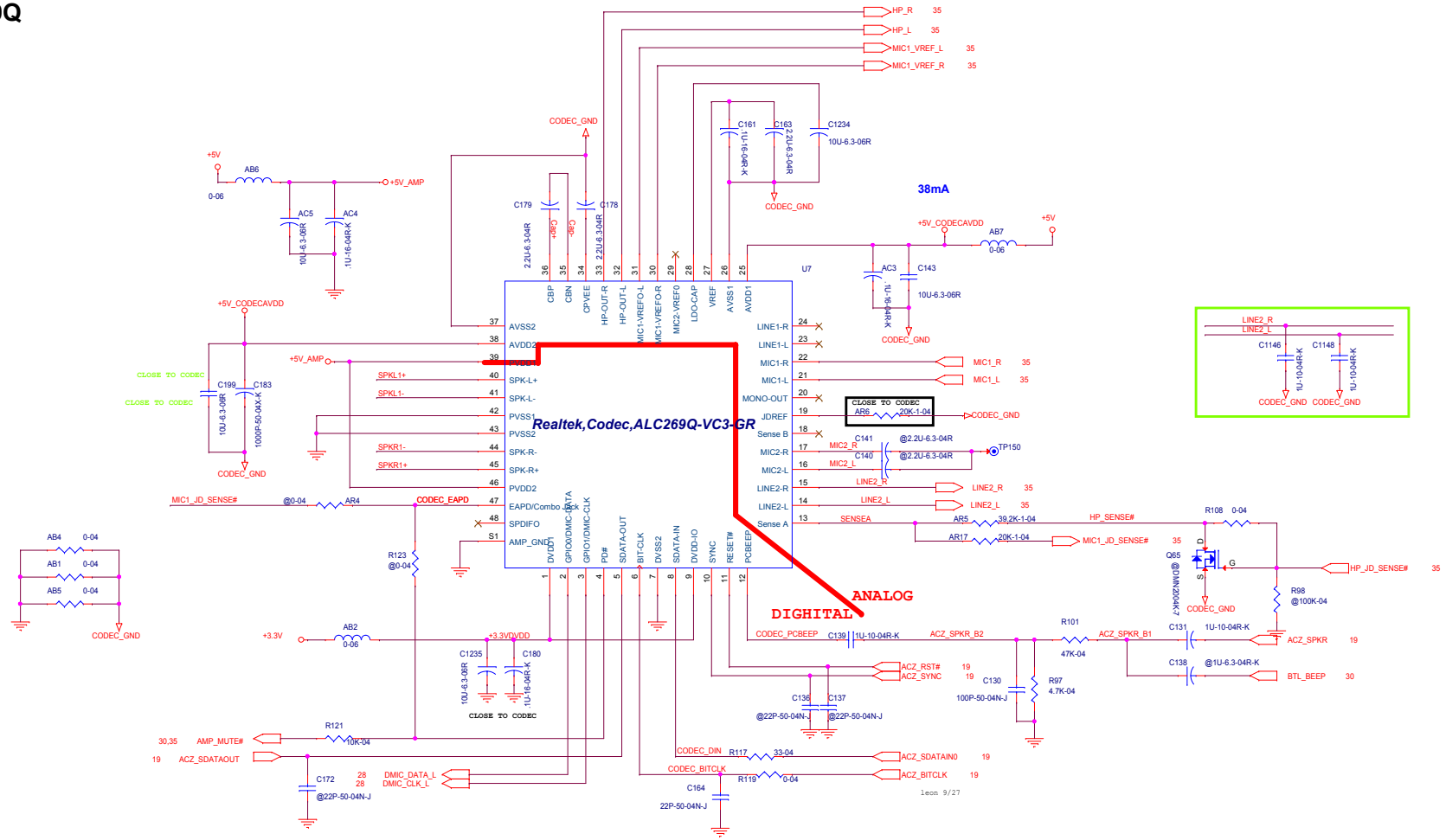
Title: 32 HDD/M.2 CONN/DEBUG

Size: Custom | Document Number: GISCPXX | Rev: B

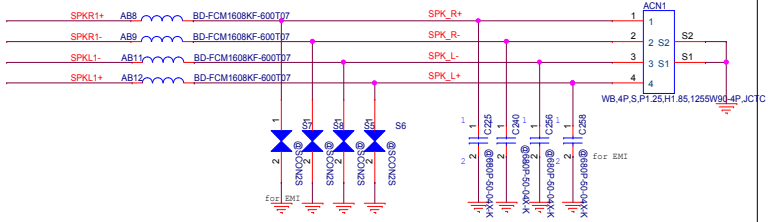
Date: Monday, December 24, 2018 | Sheet 32 of 65


RTL8411BN-CG
U17
BODY REF AGND
LT2
GST5009B-LF
TST1284A/GST5009
CN34
RJ45,8P,DIP,P1.02,130456-781,ST
Q19
EMFA0P02J
Q20
LMBT3904LT1G
Q68
2N7002K-H
1400mA
<OrgName>
同方国际信息技术有限公司
33 LAN/CARDREADER RTL8411BN-CG
GI5CPXX
Monday, December 24, 2018

CODEC ALC269Q



INT_SPEAKER

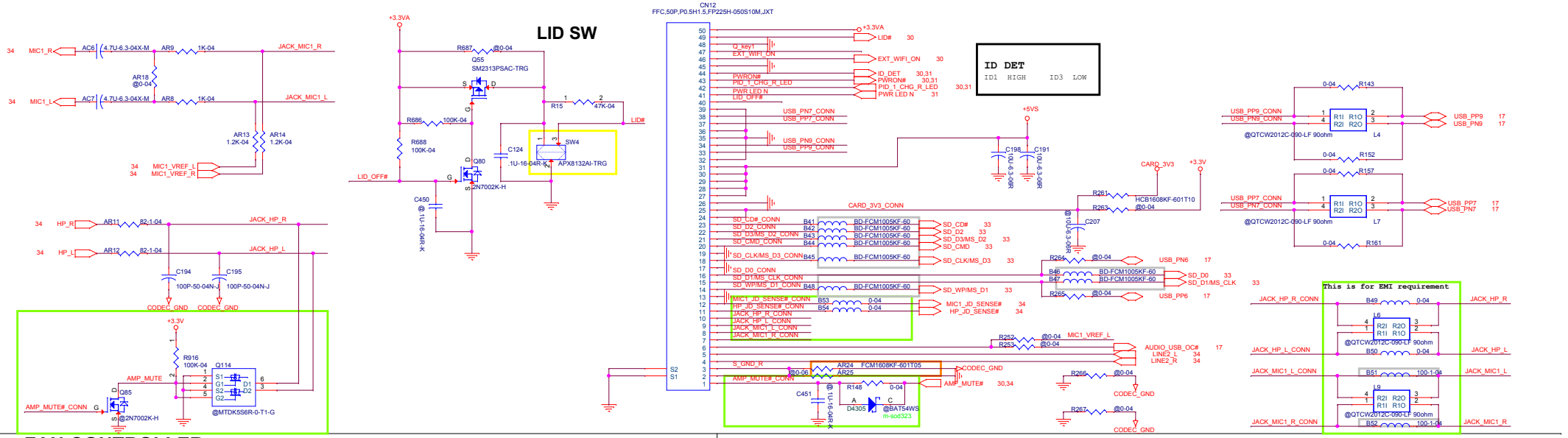


INT_MIC

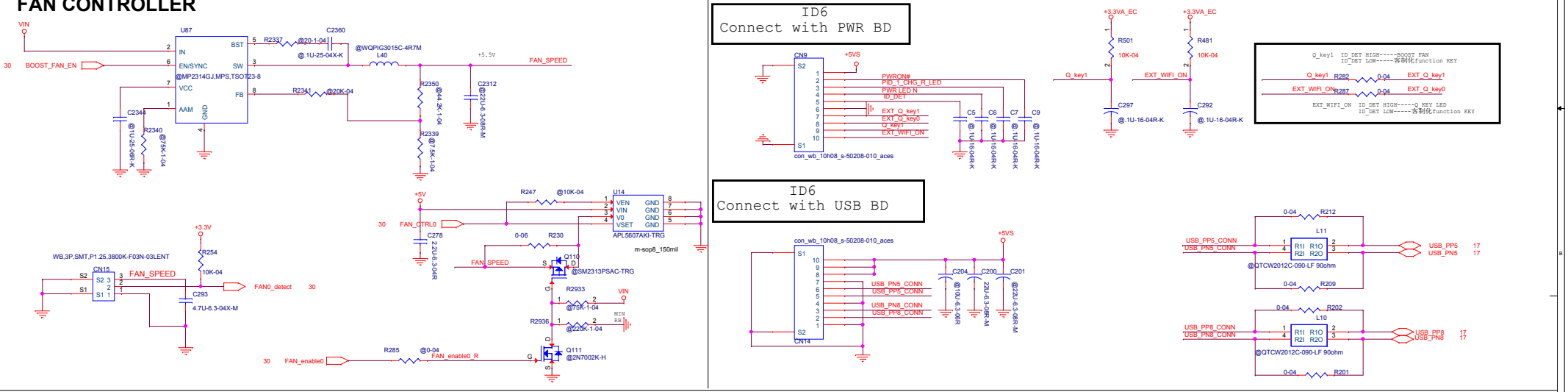
Digital Mic

<OrgName> 同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>			
Title: 34 CODEC(ALC269Q)/INT MIC/SPKR			
Size: C	Document Number: GI5CPXX		Rev: B
Date: Monday, December 24, 2018	Sheet 34 of 65		

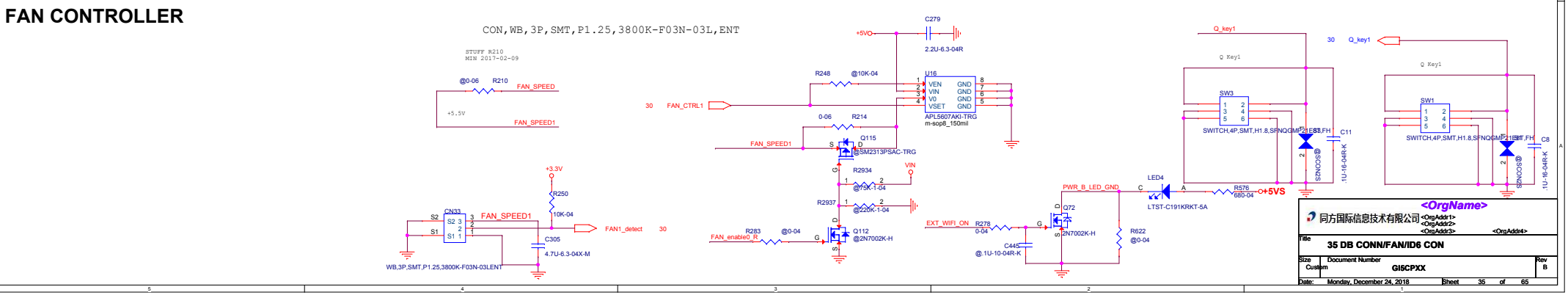
EXT MIC / EXT LINE IN / EXT USB JACK

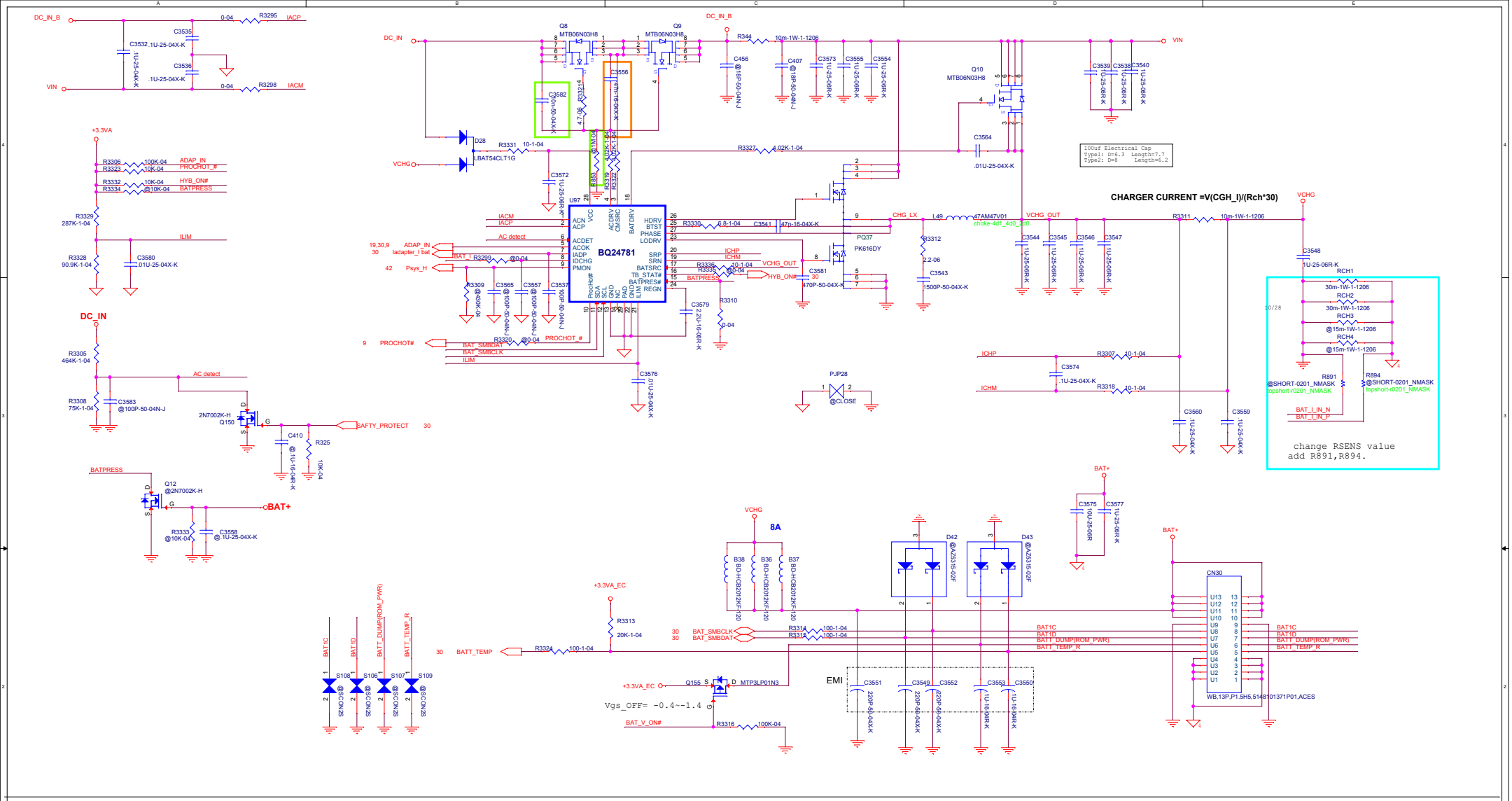


FAN CONTROLLER

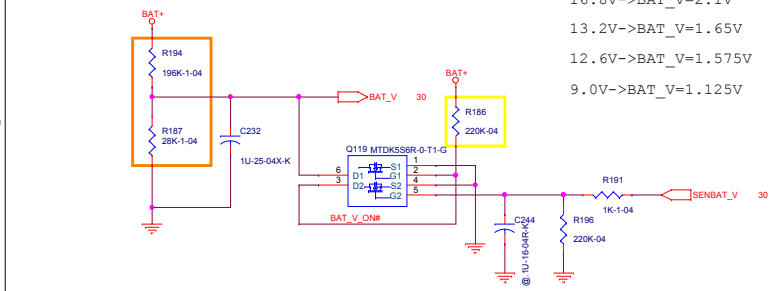


FAN CONTROLLER





Battery Voltage Detect



17.6V->BAT_V=2.2V

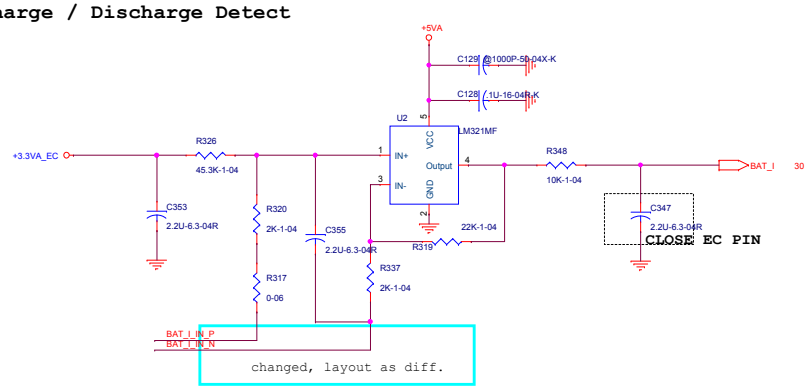
16.8V->BAT_V=2.1V

13.2V->BAT_V=1.65V

12.6V->BAT_V=1.575V

9.0V->BAT_V=1.125V

Charge / Discharge Detect



RCH1 //RCH2 =15mohm

BAT_I	ICHG (0.1724V/1A)
2.3640V	4A
2.0192V	2A
1.8468V	1A
1.6744V	0A
1.5020V	-1A
1.3296V	-2A
0.9848V	-4A
0.6400V	-6A
0.2952V	-8A
0.1228V	-9A

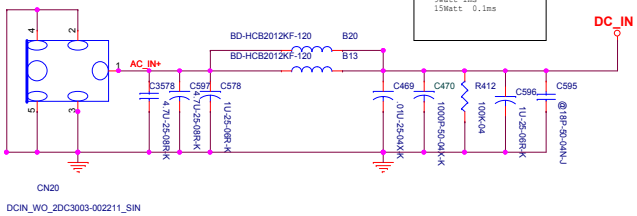
<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 36 BATT IN/CHARGER(BQ24781)

Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 36 of 65

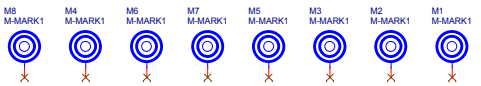
DC IN

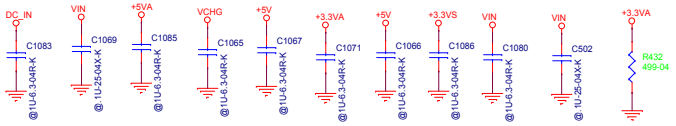


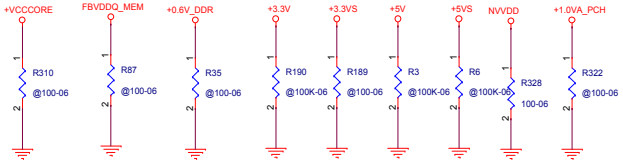
Modify safety protect circuit

Delete parts as below
C426
Q41
Q43
Q120
R347
R393
R403
R420

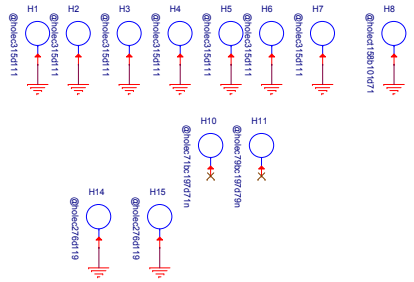
Discharge Resistor



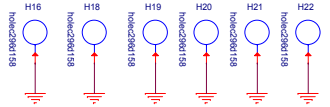




PCB HOLE



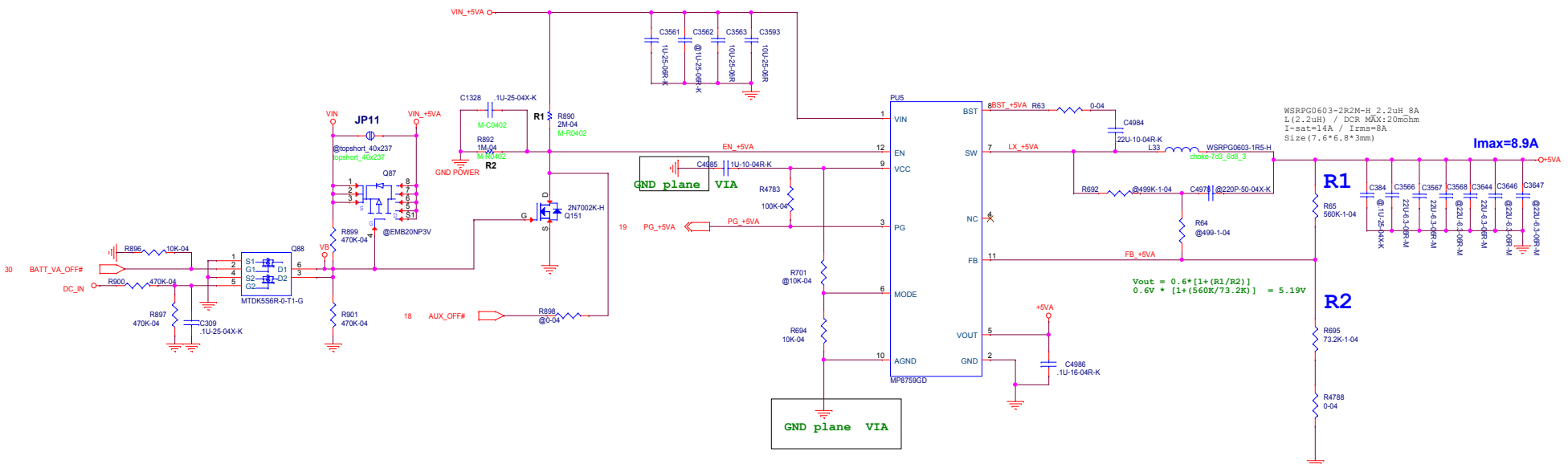
THERMAL HOLE



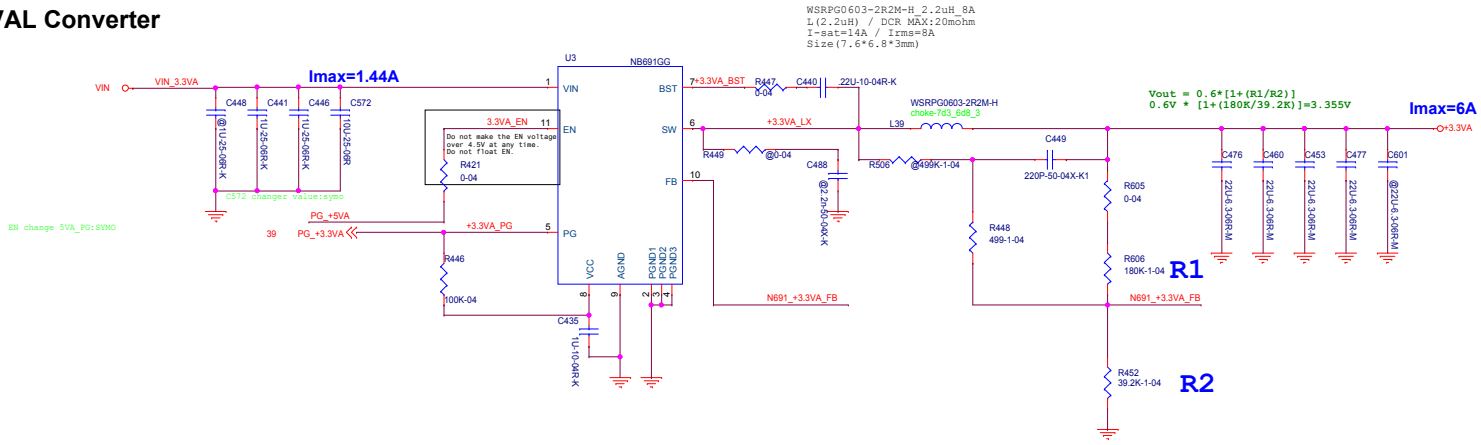
<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title	37 DC IN/TPM/DIS-R/SCREW HOLE	
Size: Custom	Document Number: GI5CPXX	Rev: B
Date: Monday, December 24, 2018	Sheet 37 of 65	

5VAL Converter



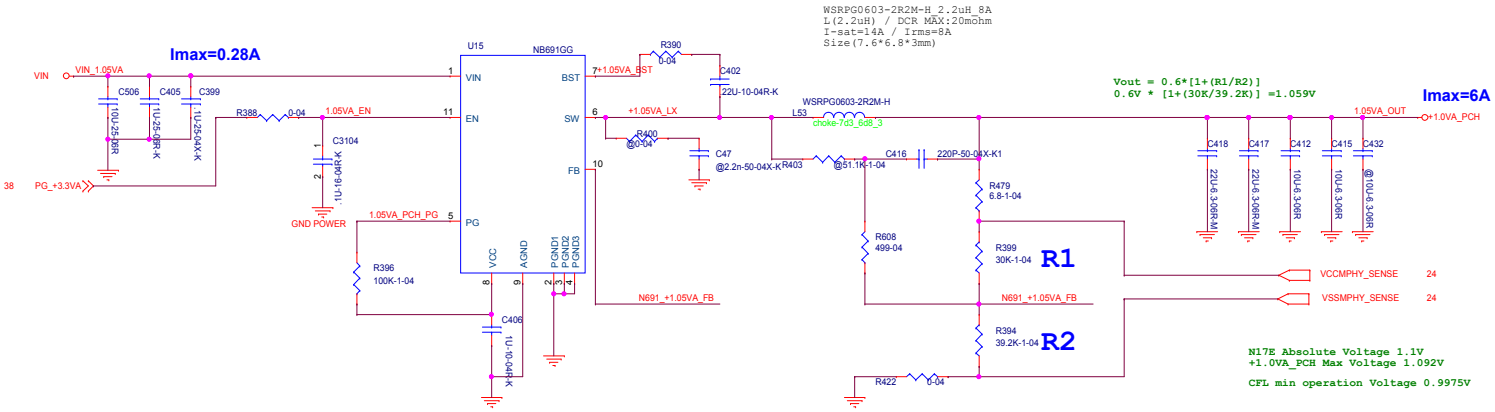
3.3VAL Converter



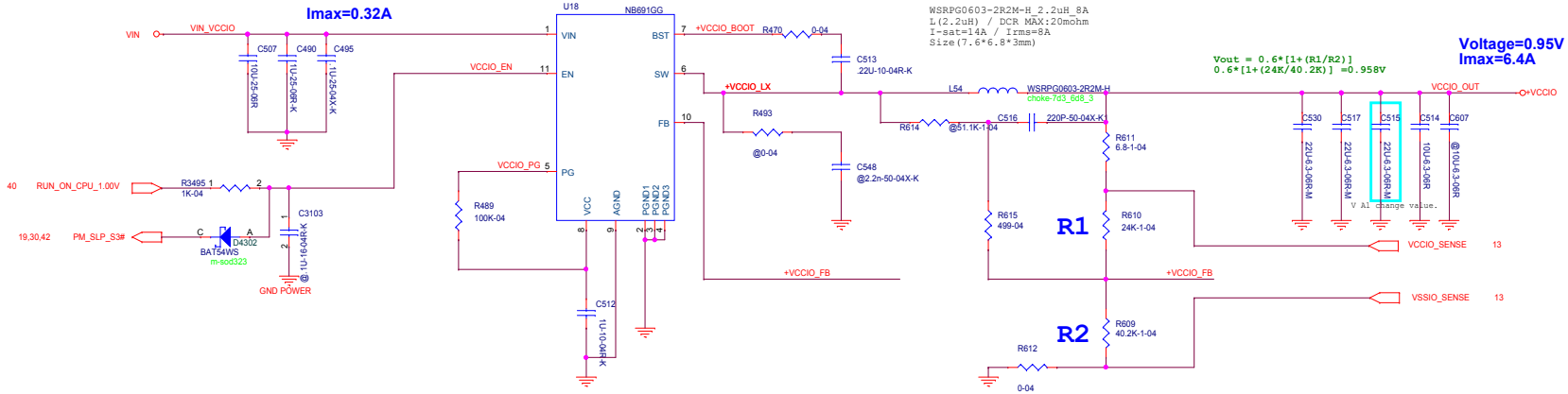
<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title	38 +5VA/+3.3VA	
Size C	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 38 of 65	

1.0VA Converter

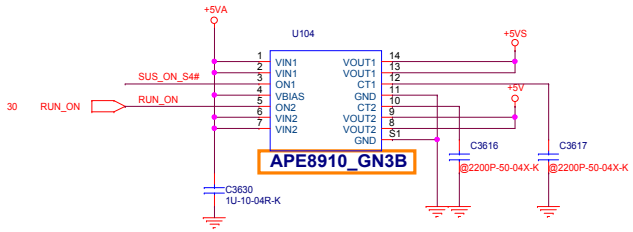


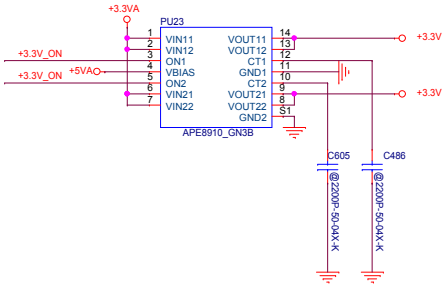
VCCIO Converter

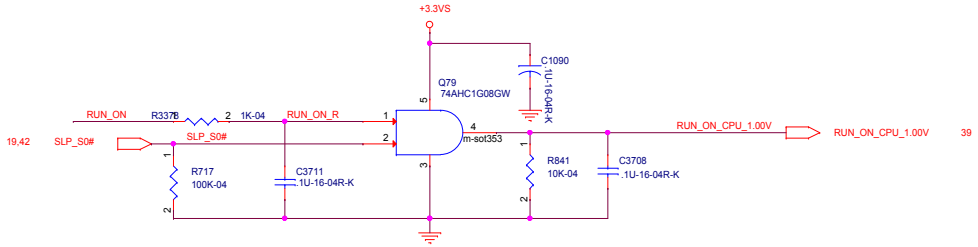


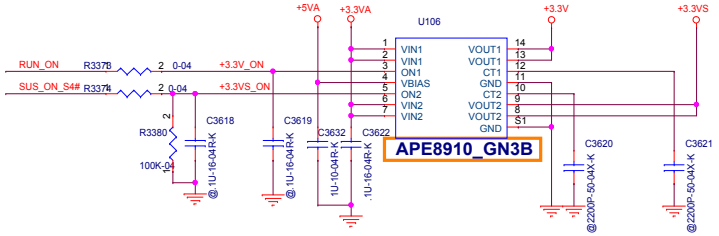
<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

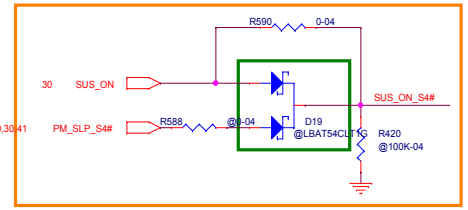
Title	39 +1.0VA_PCH/VCCIO	
Size C	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 39 of 65	

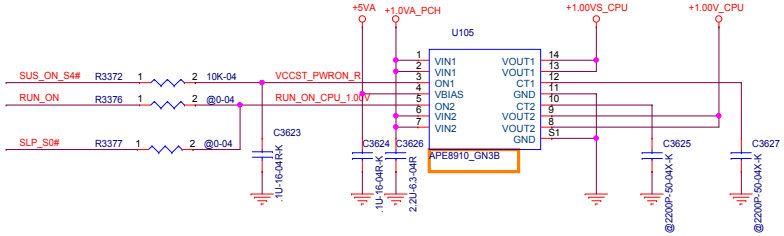












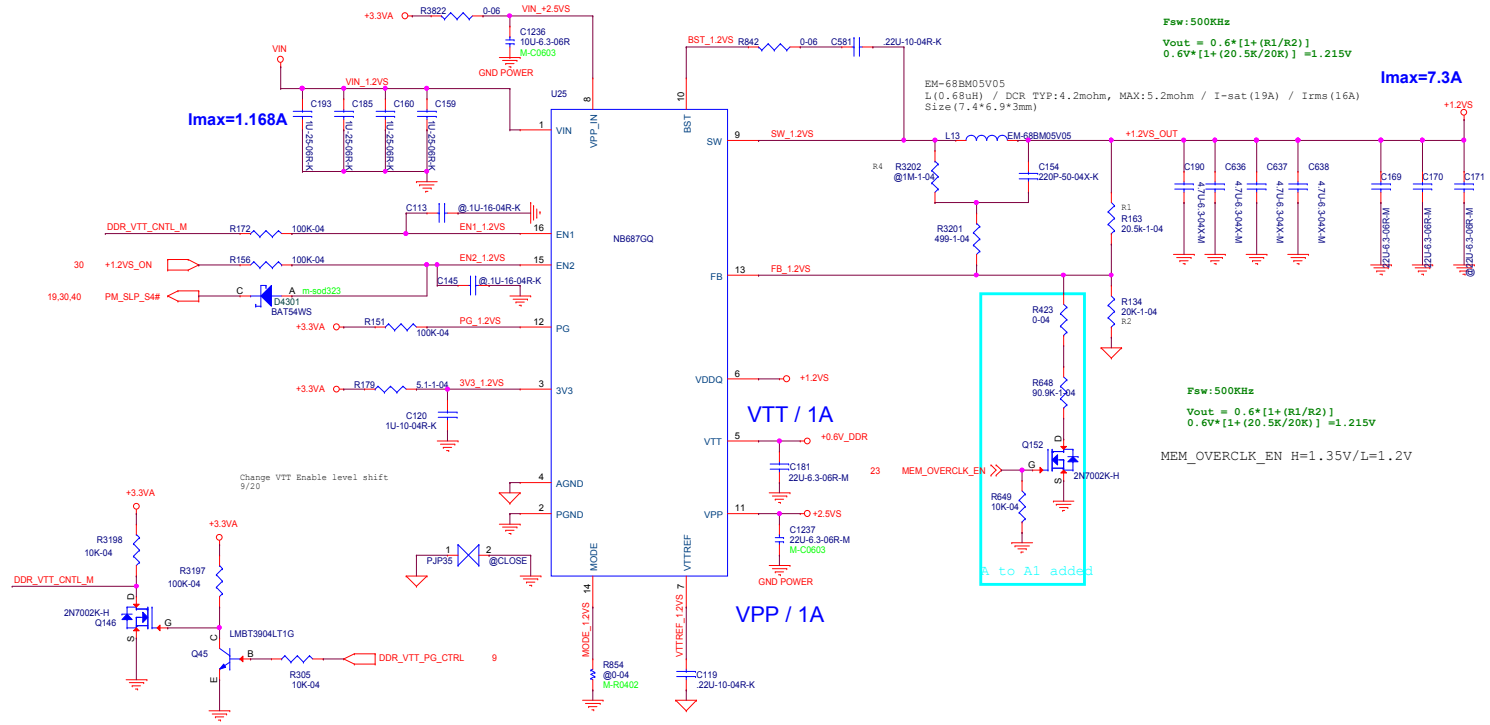
<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 40 +1.8VA/PWR SWITCH

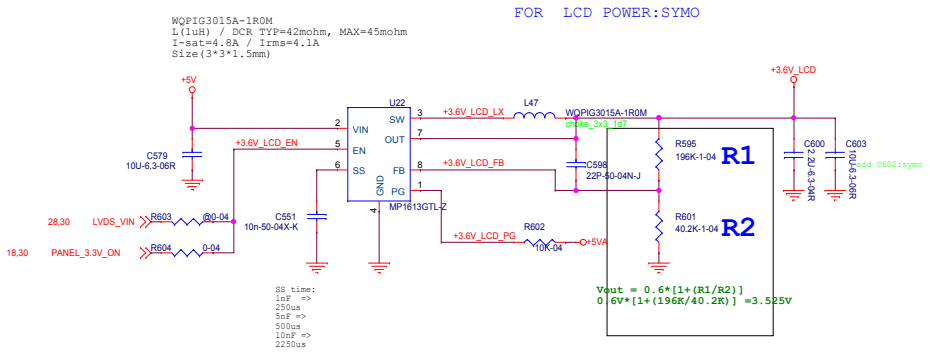
Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 40 of 65

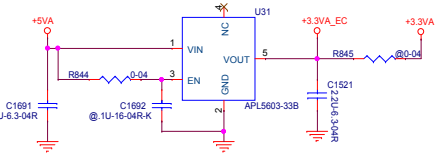
1.2VS/VTT



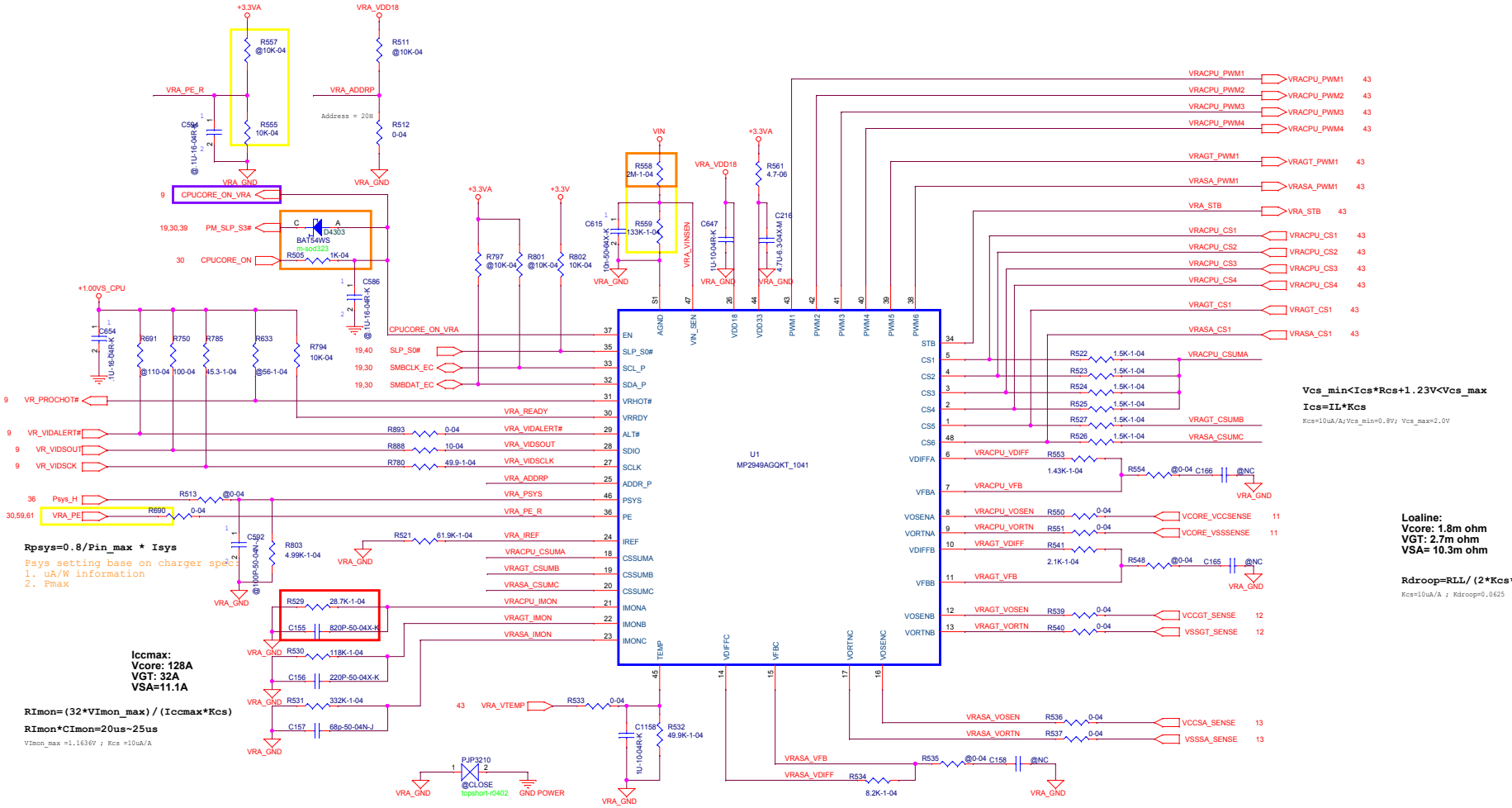
+3.6V_LCD



+3.3VA_EC



<OrgName> 同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>		
Title: 41 +1.2VS/+2.5VS/VTT		
Size: C	Document Number: GI5CPXX	Rev: B
Date: Monday, December 24, 2018	Sheet 41 of 65	



PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM POWER SENSE AMPLIFIER						
$V_{(PMON)}$	PMON output voltage		0		3.3	V
$I_{(PMON)}$	PMON output current		0		160	µA
$A_{(PMON)}$	PMON system gain	$V_{(PMON)}/(P_{IN} + P_{BAT}$, REG0x3B[9] = 1		1		µA/W

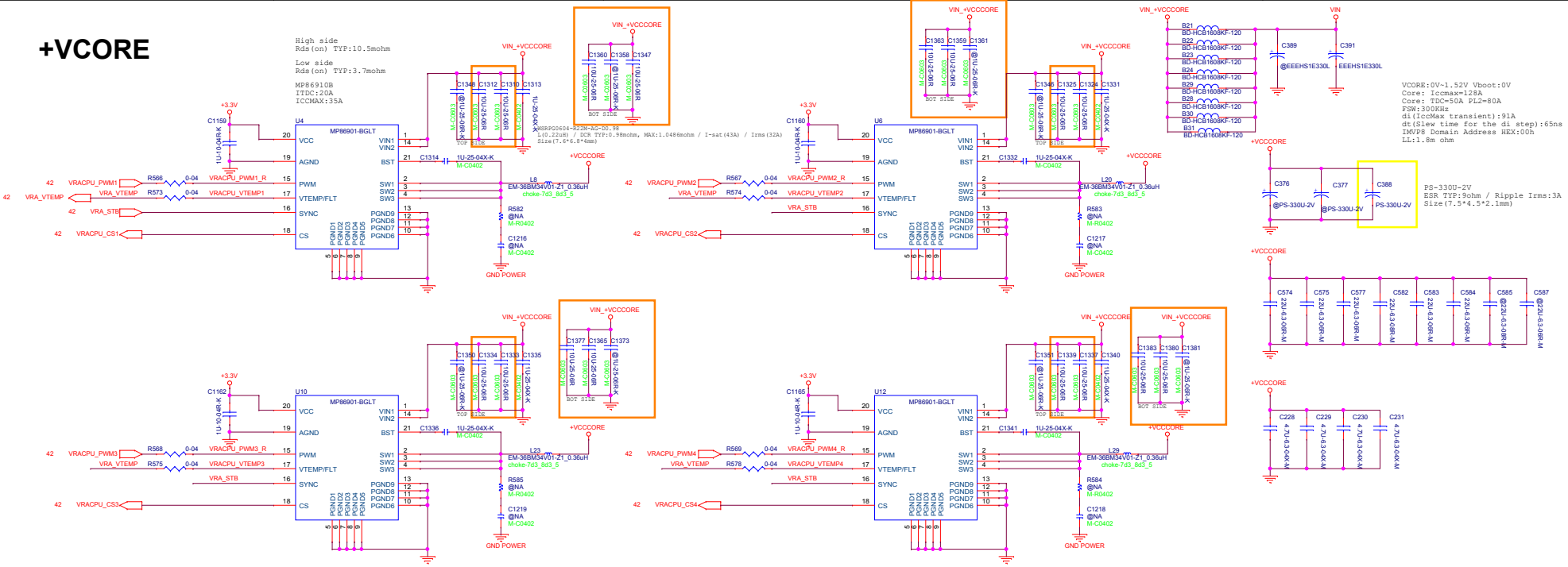
<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 42 VCORE/VCCGT/VCCSA CTRL

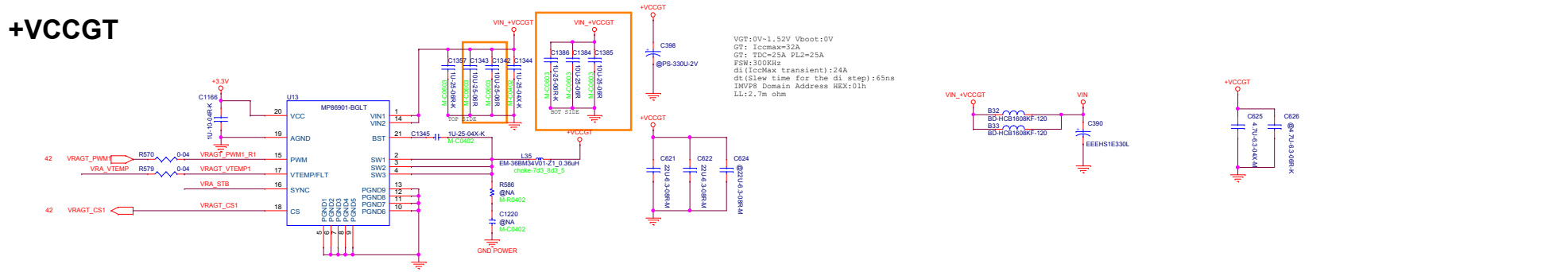
Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 42 of 65

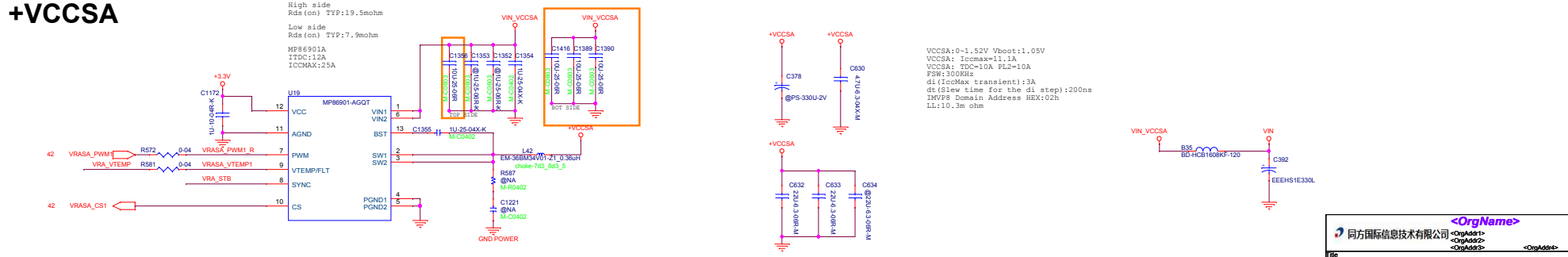
+VCORE



+VCCGT



+VCCSA



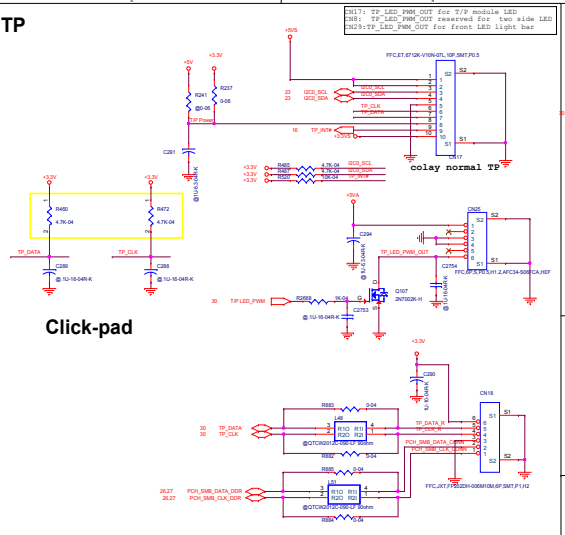
<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 43 VCORE/VCCGT/VCCSA OUTPUT

Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 43 of 65

TP



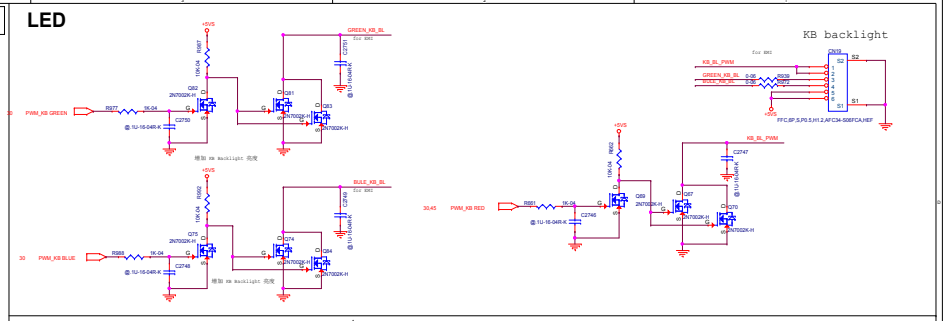
Click-pad

	Power Icon LED	KB	Pulse (TP) LED	Charging LED
Power on	on	on	on	
Fan 全轉 (Q-Key)	on	on	快呼吸	
Power off	off	off	off	
Suspend	呼吸(Follow KB)	呼吸	呼吸(Follow KB)	
Charging				on
Stop Charging (Full Battery)				off
Power on+Battery Low (<6%)				閃爍 1.5s

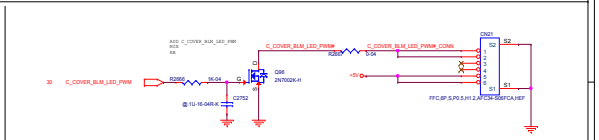
ID6
Connect with LED BD

LED CONN

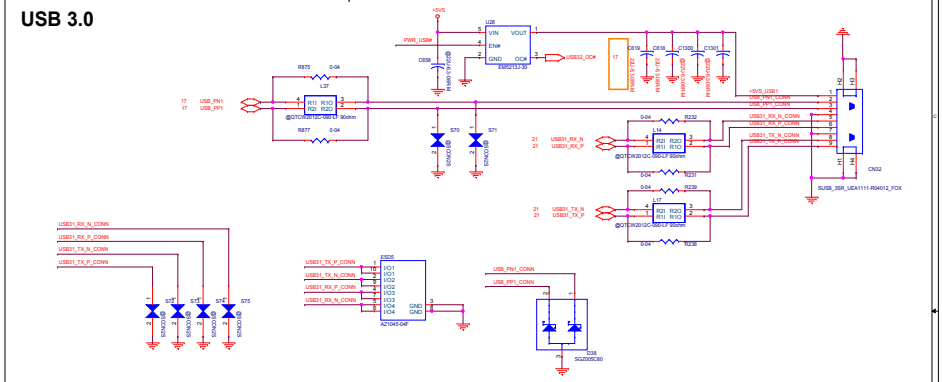
LED



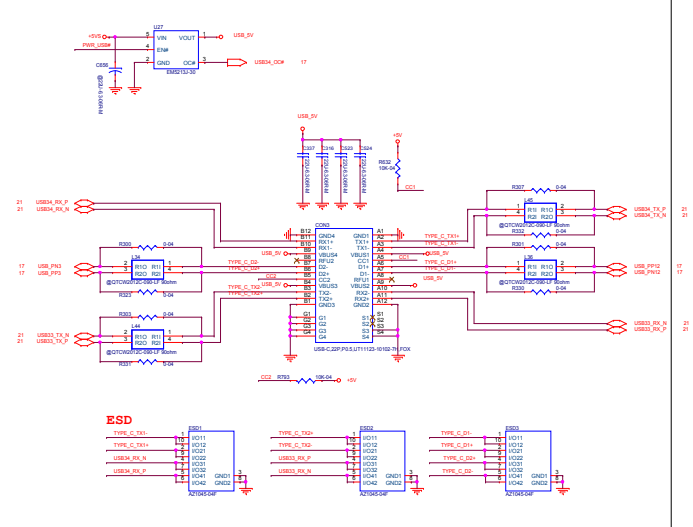
4 area KB RGB BL



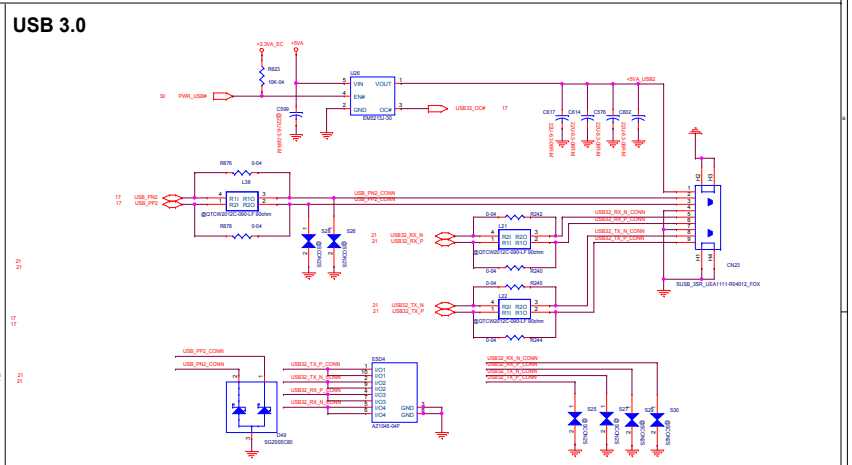
USB 3.0



USB3.0 with Type-C Port



USB 3.0

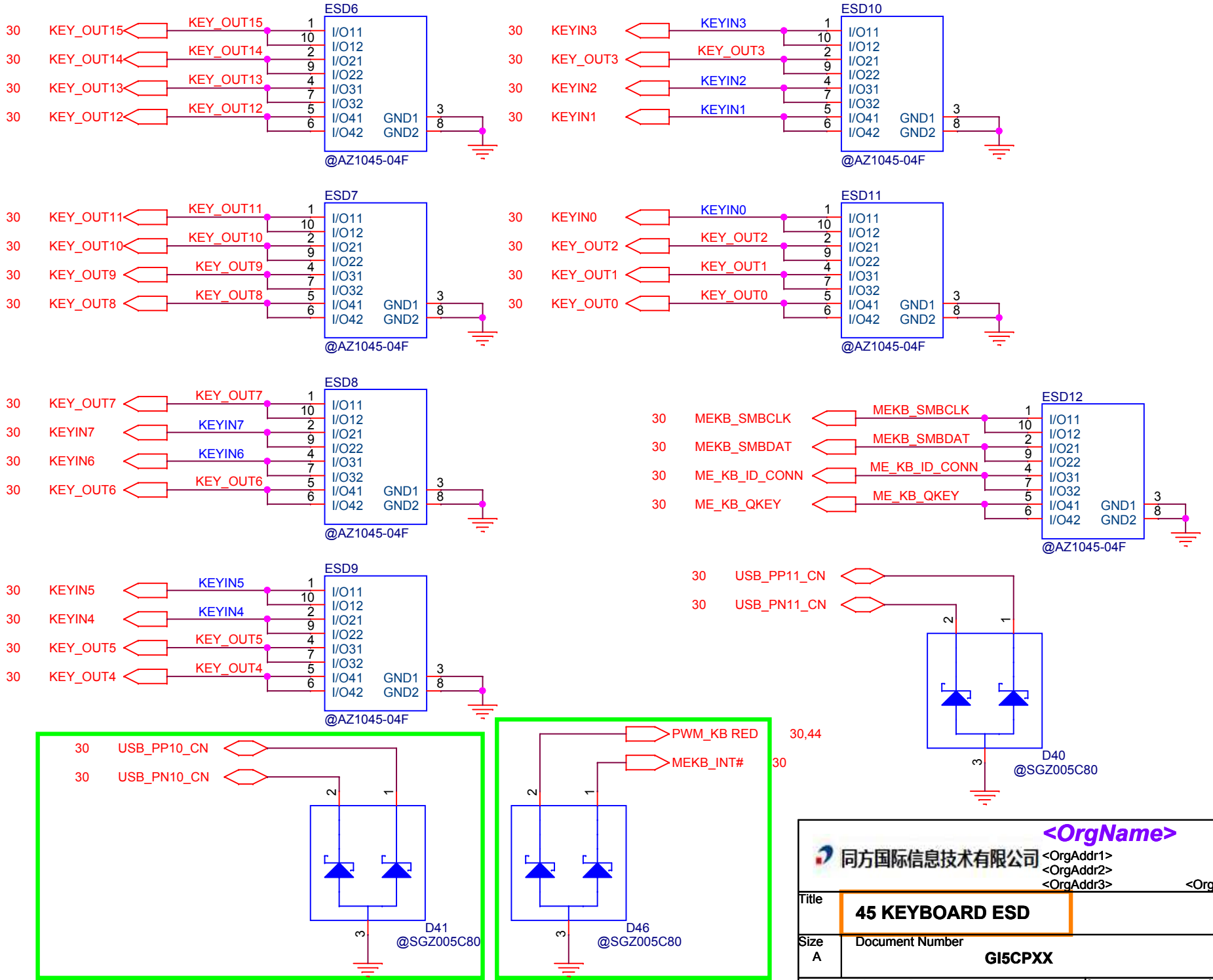


<OrgName>
同方国际信息技术有限公司 <DigAddr>

File: 44 TP/KB BACKLIGHT/USB3.0

Custom Document Number: GI5CPXX Rev: B

Date: Monday, December 28, 2015 Sheet 43 of 50


ESD6
30 KEY_OUT15 KEY_OUT15 1 I/O11
30 KEY_OUT14 KEY_OUT14 10 I/O12
30 KEY_OUT13 KEY_OUT13 2 I/O21
30 KEY_OUT12 KEY_OUT12 9 I/O22
4 I/O31
7 I/O32
5 I/O41 GND1 3
6 I/O42 GND2 8
@AZ1045-04F
ESD10
30 KEYIN3 KEYIN3
30 KEY_OUT3 KEY_OUT3
30 KEYIN2 KEYIN2
30 KEYIN1 KEYIN1
@AZ1045-04F
ESD7
30 KEY_OUT11 KEY_OUT11
30 KEY_OUT10 KEY_OUT10
30 KEY_OUT9 KEY_OUT9
30 KEY_OUT8 KEY_OUT8
@AZ1045-04F
ESD11
30 KEYIN0 KEYIN0
30 KEY_OUT2 KEY_OUT2
30 KEY_OUT1 KEY_OUT1
30 KEY_OUT0 KEY_OUT0
@AZ1045-04F
ESD8
30 KEY_OUT7 KEY_OUT7
30 KEYIN7 KEYIN7
30 KEYIN6 KEYIN6
30 KEY_OUT6 KEY_OUT6
@AZ1045-04F
ESD12
30 MEKB_SMBCLK MEKB_SMBCLK
30 MEKB_SMBDAT MEKB_SMBDAT
30 ME_KB_ID_CONN ME_KB_ID_CONN
30 ME_KB_QKEY ME_KB_QKEY
@AZ1045-04F
ESD9
30 KEYIN5 KEYIN5
30 KEYIN4 KEYIN4
30 KEY_OUT5 KEY_OUT5
30 KEY_OUT4 KEY_OUT4
@AZ1045-04F
30 USB_PP11_CN
30 USB_PN11_CN
D40
@SGZ005C80
30 USB_PP10_CN
30 USB_PN10_CN
D41
@SGZ005C80
PWM_KB RED 30,44
MEKB_INT# 30
D46
@SGZ005C80
<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>
Title
45 KEYBOARD ESD
Size A
Document Number
GI5CPXX
Rev B
Date: Monday, December 24, 2018
Sheet 45 of 65

N17P Pascal 20nm
N17P Pascal 20nm GB4C-128b 3.5GHz
Ball Pitch: 0.8mm, 1.0mm

N18P
N18P GB4D-128b 4.0GHz
Ball Pitch: 0.8mm, 1.0mm

G1A
N18P
BGA980
COMMON

1/17 PCI_EXPRESS

reserver for N18 (NC)

16 PEX_WAKE_PCH — R2730 @0-04 — PEX_WAKE#
PEX_RST#
PEX_CLKREQ#

22 CLK_PCIE_GFX_DP
22 CLK_PCIE_GFX_DN

7 PEG_RXP15	C846 22U-10-04R-K	C848 22U-10-04R-K	PEG_RXP15_GPU AK14	PEX_TX0
7 PEG_RXN15			PEG_RXN15_GPU AJ14	PEX_TX0
7 PEG_TXP15	C842 22U-10-04R-K	C845 22U-10-04R-K	PEG_TXP15_GPU AN12	PEX_RX0
7 PEG_TXN15			PEG_TXN15_GPU AM12	PEX_RX0
7 PEG_RXP14	C844 22U-10-04R-K	C847 22U-10-04R-K	PEG_RXP14_GPU AH14	PEX_TX1
7 PEG_RXN14			PEG_RXN14_GPU AG14	PEX_TX1
7 PEG_TXP14	C802 22U-10-04R-K	C843 22U-10-04R-K	PEG_TXP14_GPU AN14	PEX_RX1
7 PEG_TXN14			PEG_TXN14_GPU AM14	PEX_RX1
7 PEG_RXP13	C859 22U-10-04R-K	C867 22U-10-04R-K	PEG_RXP13_GPU AK15	PEX_TX2
7 PEG_RXN13			PEG_RXN13_GPU AJ15	PEX_TX2
7 PEG_TXP13	C854 22U-10-04R-K	C852 22U-10-04R-K	PEG_TXP13_GPU AP14	PEX_RX2
7 PEG_TXN13			PEG_TXN13_GPU AP15	PEX_RX2
7 PEG_RXP12	C855 22U-10-04R-K	C853 22U-10-04R-K	PEG_RXP12_GPU AL16	PEX_TX3
7 PEG_RXN12			PEG_RXN12_GPU AK16	PEX_TX3
7 PEG_TXP12	C805 22U-10-04R-K	C851 22U-10-04R-K	PEG_TXP12_GPU AN15	PEX_RX3
7 PEG_TXN12			PEG_TXN12_GPU AM15	PEX_RX3
7 PEG_RXP11	C1017 22U-10-04R-K	C1018 22U-10-04R-K	PEG_RXP11_GPU AK17	PEX_TX4
7 PEG_RXN11			PEG_RXN11_GPU AJ17	PEX_TX4
7 PEG_TXP11	C979 22U-10-04R-K	C977 22U-10-04R-K	PEG_TXP11_GPU AN17	PEX_RX4
7 PEG_TXN11			PEG_TXN11_GPU AM17	PEX_RX4
7 PEG_RXP10	C980 22U-10-04R-K	C978 22U-10-04R-K	PEG_RXP10_GPU AH17	PEX_TX5
7 PEG_RXN10			PEG_RXN10_GPU AG17	PEX_TX5
7 PEG_TXP10	C807 22U-10-04R-K	C975 22U-10-04R-K	PEG_TXP10_GPU AP17	PEX_RX5
7 PEG_TXN10			PEG_TXN10_GPU AP18	PEX_RX5
7 PEG_RXP9	C883 22U-10-04R-K	C974 22U-10-04R-K	PEG_RXP9_GPU AK18	PEX_TX6
7 PEG_RXN9			PEG_RXN9_GPU AJ18	PEX_TX6
7 PEG_TXP9	C879 22U-10-04R-K	C873 22U-10-04R-K	PEG_TXP9_GPU AN18	PEX_RX6
7 PEG_TXN9			PEG_TXN9_GPU AM18	PEX_RX6
7 PEG_RXP8	C882 22U-10-04R-K	C869 22U-10-04R-K	PEG_RXP8_GPU AL19	PEX_TX7
7 PEG_RXN8			PEG_RXN8_GPU AK19	PEX_TX7
7 PEG_TXP8	C806 22U-10-04R-K	C868 22U-10-04R-K	PEG_TXP8_GPU AN20	PEX_RX7
7 PEG_TXN8			PEG_TXN8_GPU AM20	PEX_RX7
7 PEG_RXP7	C1031 22U-10-04R-K	C1032 22U-10-04R-K	PEG_RXP7_GPU AK20	PEX_TX8
7 PEG_RXN7			PEG_RXN7_GPU AJ20	PEX_TX8
7 PEG_TXP7	C1029 22U-10-04R-K	C1027 22U-10-04R-K	PEG_TXP7_GPU AP20	PEX_RX8
7 PEG_TXN7			PEG_TXN7_GPU AP21	PEX_RX8
7 PEG_RXP6	C1030 22U-10-04R-K	C1028 22U-10-04R-K	PEG_RXP6_GPU AH20	PEX_TX9
7 PEG_RXN6			PEG_RXN6_GPU AG20	PEX_TX9
7 PEG_TXP6	C809 22U-10-04R-K	C1026 22U-10-04R-K	PEG_TXP6_GPU AN21	PEX_RX9
7 PEG_TXN6			PEG_TXN6_GPU AM21	PEX_RX9
7 PEG_RXP5	C1024 22U-10-04R-K	C1025 22U-10-04R-K	PEG_RXP5_GPU AK21	PEX_TX10
7 PEG_RXN5			PEG_RXN5_GPU AJ21	PEX_TX10
7 PEG_TXP5	C1022 22U-10-04R-K	C1021 22U-10-04R-K	PEG_TXP5_GPU AN23	PEX_RX10
7 PEG_TXN5			PEG_TXN5_GPU AM23	PEX_RX10
7 PEG_RXP4	C1023 22U-10-04R-K	C1020 22U-10-04R-K	PEG_RXP4_GPU AL22	PEX_TX11
7 PEG_RXN4			PEG_RXN4_GPU AK22	PEX_TX11
7 PEG_TXP4	C808 22U-10-04R-K	C1019 22U-10-04R-K	PEG_TXP4_GPU AP23	PEX_RX11
7 PEG_TXN4			PEG_TXN4_GPU AP24	PEX_RX11
7 PEG_RXP3	C1047 22U-10-04R-K	C1048 22U-10-04R-K	PEG_RXP3_GPU AK23	PEX_TX12
7 PEG_RXN3			PEG_RXN3_GPU AJ23	PEX_TX12
7 PEG_TXP3	C1045 22U-10-04R-K	C1044 22U-10-04R-K	PEG_TXP3_GPU AN24	PEX_RX12
7 PEG_TXN3			PEG_TXN3_GPU AM24	PEX_RX12
7 PEG_RXP2	C1046 22U-10-04R-K	C1042 22U-10-04R-K	PEG_RXP2_GPU AH23	PEX_TX13
7 PEG_RXN2			PEG_RXN2_GPU AG23	PEX_TX13
7 PEG_TXP2	C811 22U-10-04R-K	C1040 22U-10-04R-K	PEG_TXP2_GPU AN26	PEX_RX13
7 PEG_TXN2			PEG_TXN2_GPU AM26	PEX_RX13
7 PEG_RXP1	C1038 22U-10-04R-K	C1039 22U-10-04R-K	PEG_RXP1_GPU AK24	PEX_TX14
7 PEG_RXN1			PEG_RXN1_GPU AJ24	PEX_TX14
7 PEG_TXP1	C1036 22U-10-04R-K	C1035 22U-10-04R-K	PEG_TXP1_GPU AP26	PEX_RX14
7 PEG_TXN1			PEG_TXN1_GPU AP27	PEX_RX14
7 PEG_RXP0	C1037 22U-10-04R-K	C1034 22U-10-04R-K	PEG_RXP0_GPU AL25	PEX_TX15
7 PEG_RXN0			PEG_RXN0_GPU AK25	PEX_TX15
7 PEG_TXP0	C810 22U-10-04R-K	C1033 22U-10-04R-K	PEG_TXP0_GPU AN27	PEX_RX15
7 PEG_TXN0			PEG_TXN0_GPU AM27	PEX_RX15

N17P(G4BC-128) UNDER GPU
4X 0402 1uF

PEX_VDD NEAR GPU
2x 0603 4.7uF
1x 0805 10uF
1x 0805 22uF

PEX_VDD
PEX_DVDD AG21
PEX_DVDD AG22
PEX_DVDD AG24
PEX_DVDD AH25
PEX_CVDD AG19
PEX_CVDD AH21

C782 C783 C784 C785 C866 C787 C1450 C1051 C1049 C1050 C1471 C1043 C973 C976 C812
4.7U-6.3-04R-K 4.7U-6.3-04R-K 4.7U-6.3-04R-K 4.7U-6.3-04R-K 4.7U-6.3-04R-K 4.7U-6.3-04R-K 4.7U-6.3-04R-K 4.7U-6.3-04R-K 4.7U-6.3-04R-K 4.7U-6.3-04R-K 4.7U-6.3-04X-M 4.7U-6.3-04X-M 4.7U-6.3-04X-M

PEX_VDD
C1053 C1052 C860 C856 C728
10U-6.3-08R 10U-6.3-08R 10U-6.3-08R 22U-6.3-08R-M 22U-6.3-08R-M

PEX_HVDD AG13
PEX_HVDD AG15
PEX_HVDD AG16
PEX_HVDD AG18
PEX_HVDD AG25
PEX_HVDD AH15
PEX_HVDD AH18
PEX_HVDD AH26
PEX_HVDD AH27
PEX_HVDD AJ27
PEX_HVDD AK27
PEX_HVDD AL27
PEX_HVDD AM28
PEX_HVDD AN28

1V8_MAIN
UNDER GPU

C786 C788 C790 C789 C794 C791 C792 C793 C795 C816 C798 C796 C815 C864 C814 C813
0.47U-6.3-02R-K 4.7U-6.3-04R-K 0.47U-6.3-02R-K 0.47U-6.3-02R-K 4.7U-6.3-04R-K 0.47U-6.3-02R-K 0.47U-6.3-02R-K 0.47U-6.3-02R-K 4.7U-6.3-04R-K 0.47U-6.3-02R-K 0.47U-6.3-02R-K 0.47U-6.3-02R-K 4.7U-6.3-04X-M 4.7U-6.3-04X-M 4.7U-6.3-04X-M 4.7U-6.3-04X-M

1V8_MAIN
NEAR GPU
C865 C861 C862 C725 C727
10U-6.3-08R 10U-6.3-08R 10U-6.3-08R 22U-6.3-08R-M 22U-6.3-08R-M

PEX_PLL_HVDD AH12
1V8_MAIN
C870 .47U-6.3-04R-K
N17P 0.1UF
N18P0.47UF

1V8_AON
Q94 SN74LVC1G08
16,18,30,32,33 PLT_RST# — 1 — 4 — PEX_RST# — PEX_RST# 30
23 DGPU_RST_PCH# — 2
3
m-sot353
R852 100K-04
R851 100K-04

+3.3V
R764 10K-04
22 GFX_CLKREQ
Q78 L2SK3019LT1G
1V8_MAIN
C872 @.1U-16-04R-K
1V8_AON
R766 10K-04
PEX_CLKREQ#
R765 @10K-04

PEX_TERMP AP29 PEX_TERMP — R2729 2.49K-1-04

<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title	46 DGPU NV : PCIE	
Size C	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 46 of 65	

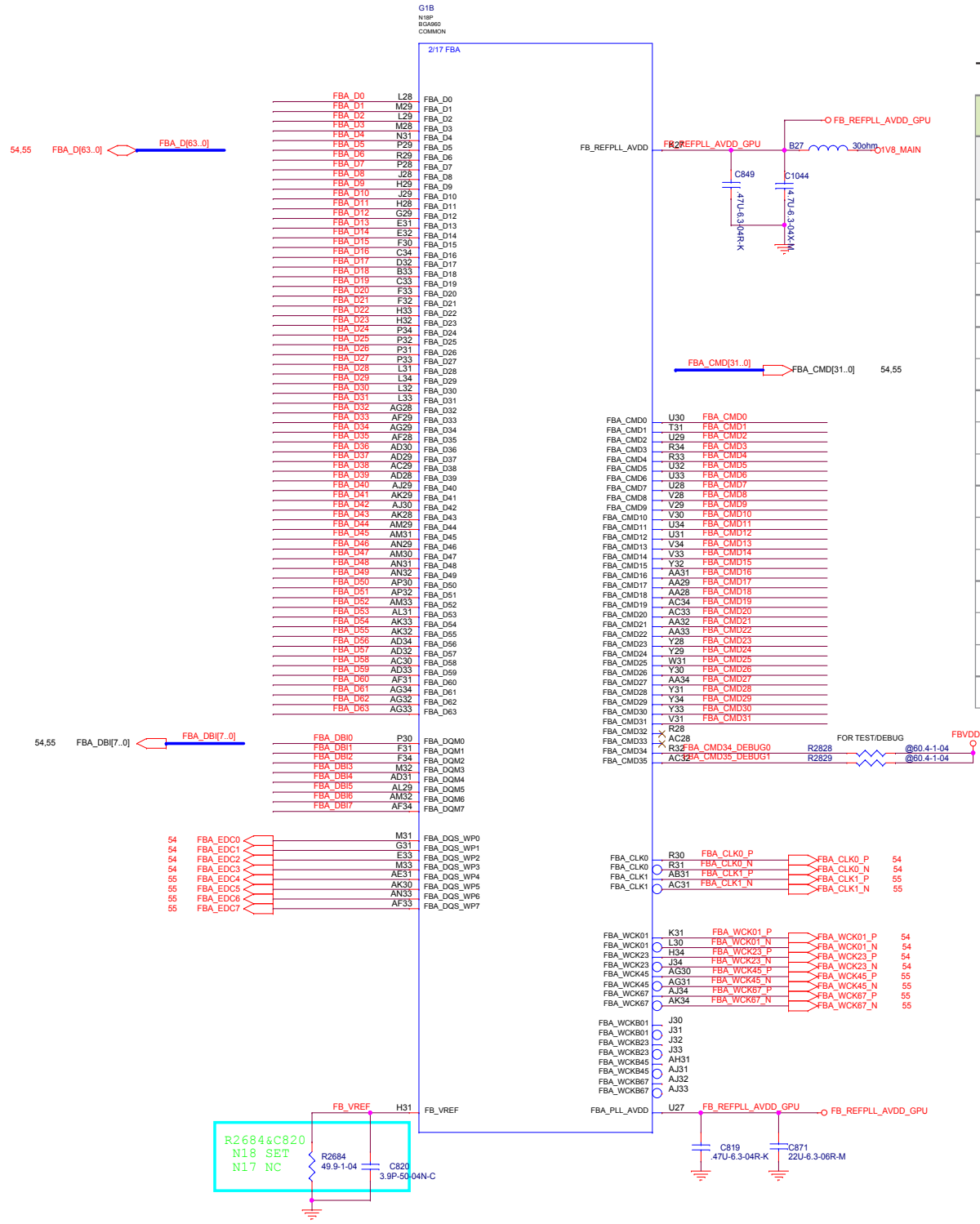


Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

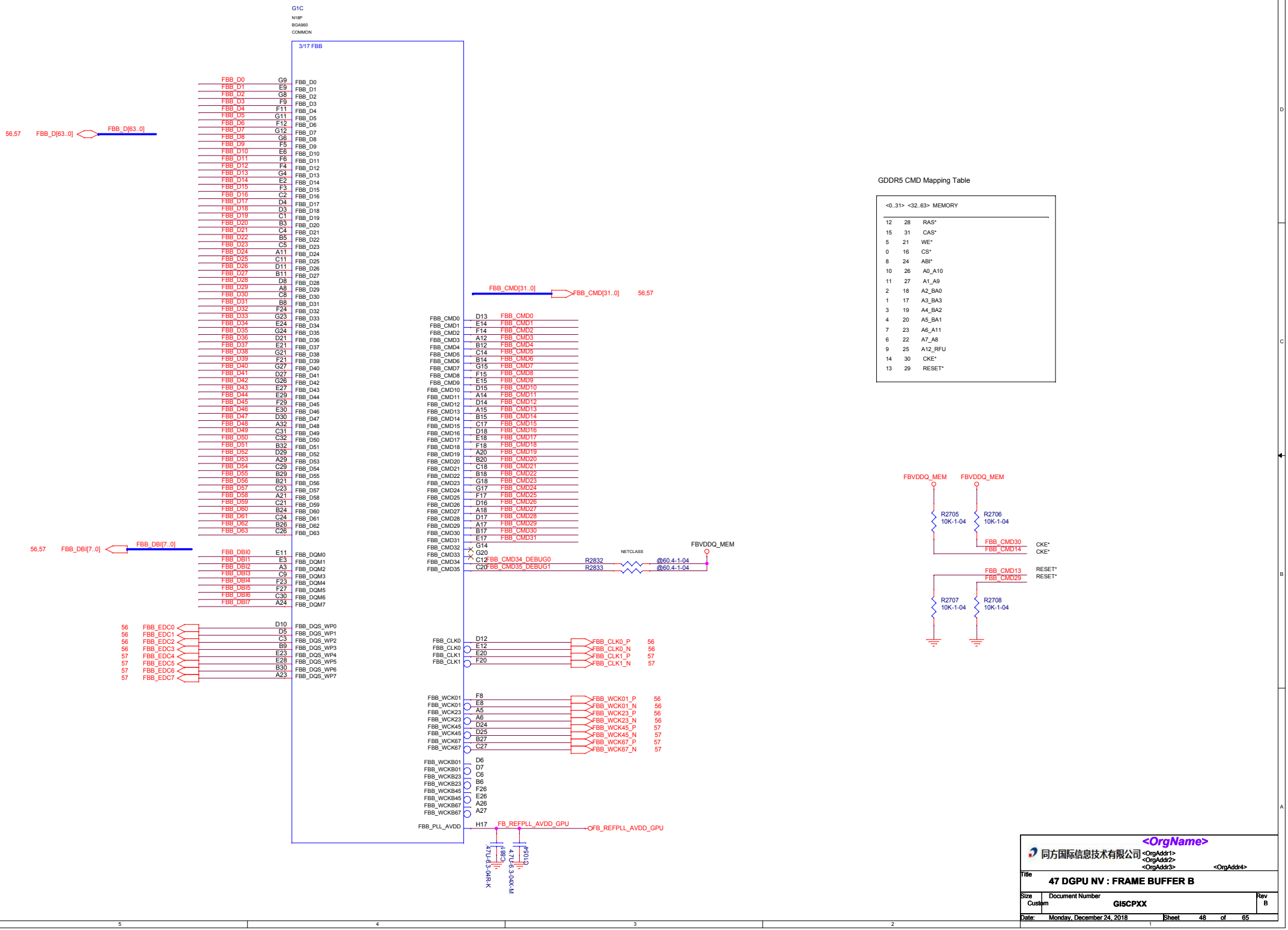
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 47 DGPU NV : FRAME BUFFER A

Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 47 of 65



GDDR5 CMD Mapping Table

<0..31>	<32..63>	MEMORY
12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	ABI*
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
14	30	CKE*
13	29	RESET*

<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 47 DGPU NV : FRAME BUFFER B

Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 48 of 65

N18&N17 co-lay floating this pin.

PLACE UNDER GPU

UNDER GPU
8X 0402 1uF
16X 0603 4.7uF
8X 0603 10uF(reducing)

NEAR GPU
9x 0603 10uF
7x 0603 22uF

UNDER GPU
12X 0402 1uF
4X 0603 10uF

NEAR GPU
2x 0603 10uF
5x 0603 22uF

UNDER GPU
10 X 0402 .47uF

NEAR GPU
3 X 0604 4.7uF

R616/C1055/R594
BUFF FOR N18P/
N17 NC:SYMO

R2771
N18=40.2 ohm
N17=60.4 ohm

<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title: 49 DGPU NV : DECOUPLING CAP

Size: Custom | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 49 of 65

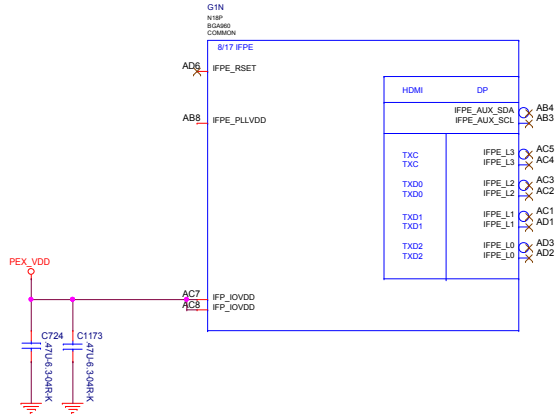
10.3 UNUSED PINS

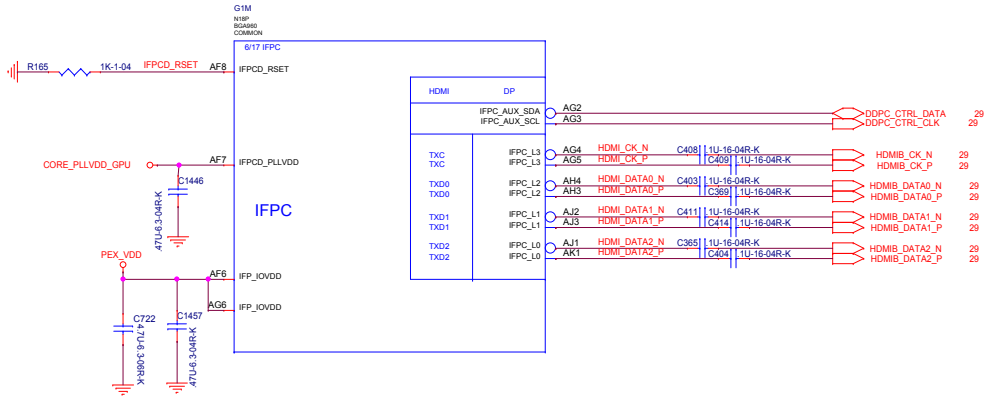
If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF) can be left unconnected if neither of IFPx /IFPy is in use. For example, If neither link of the IFPA/IFPB macro is to be used, then IFPAB_PLLVDD and IFPAB_RSET should be left disconnected, and all signals and references associated with Link A and Link B should also be left unconnected.

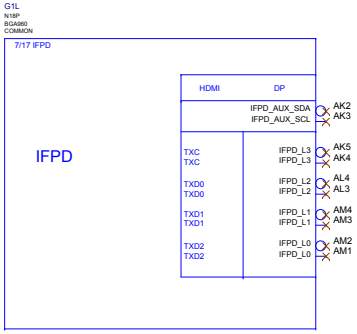
IFP_IOVDD rail can be unconnected if no IFP link is used.If any IFP is used, all IFP_IOVDD balls must be connected to power rail.

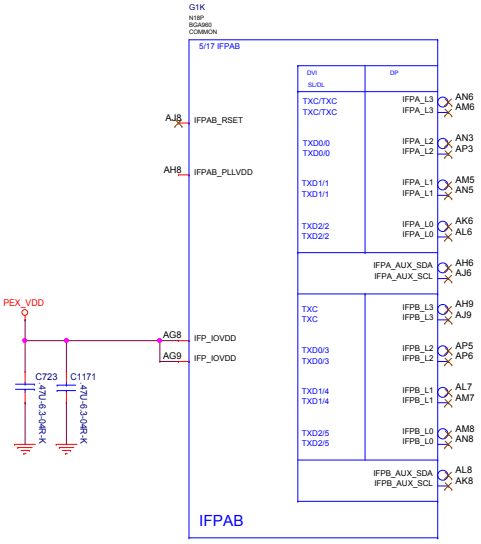
Table 10.5 Display Link Power Rail Applicability

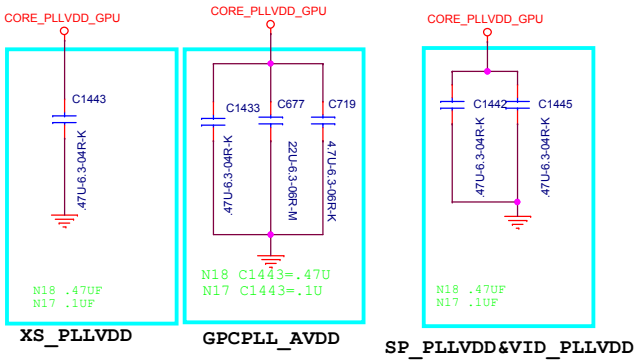
Display Link Rail	Display Links that Receive Power from This Rail					
	Link A	Link B	Link C	Link D	Link E	Link F
IFP_IOVDD	✓	✓	✓	✓	✓	✓
IFPAB_PLLVDD	✓	✓				
IFPCD_PLLVDD			✓	✓		
IFPEF_PLLVDD					✓	✓

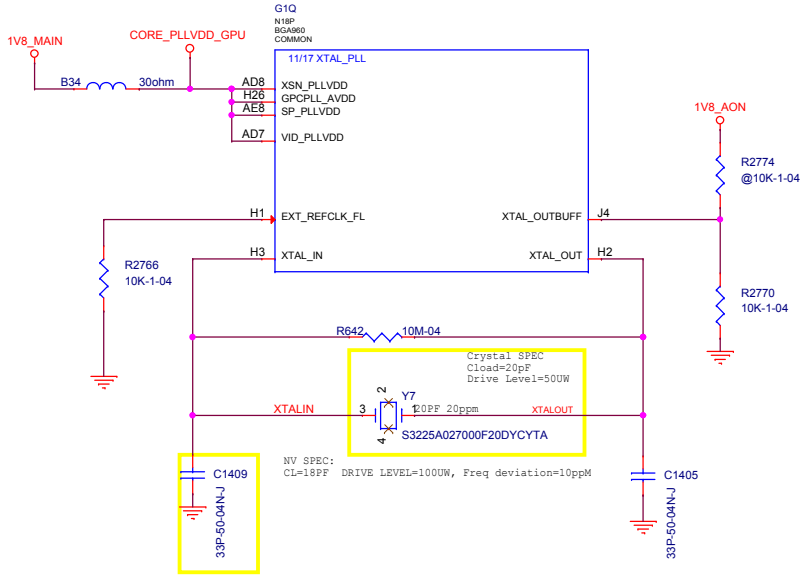


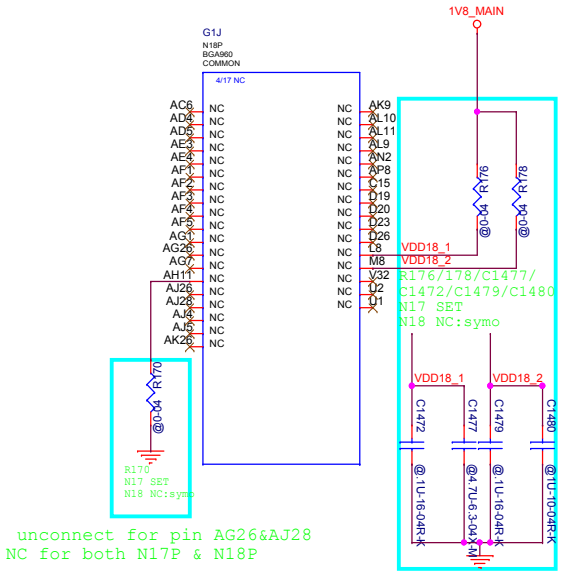










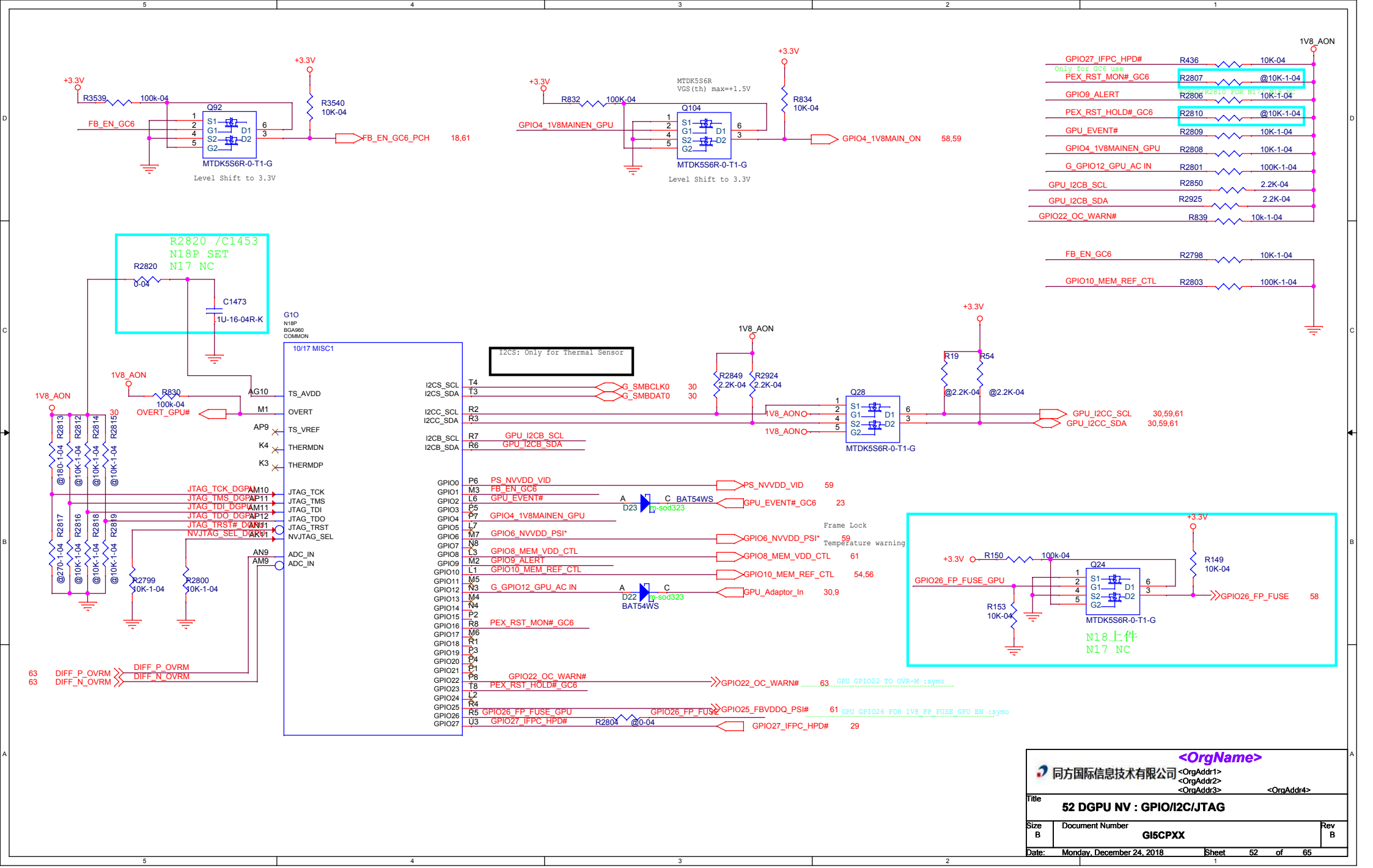


<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title: **51 DGPU NV : XTAL**

Size	Document Number	Rev
Custom	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 51 of 65

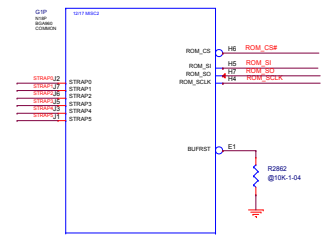


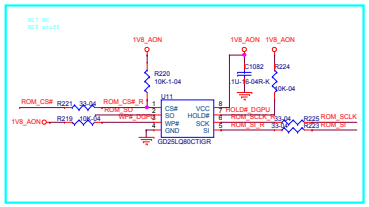
<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

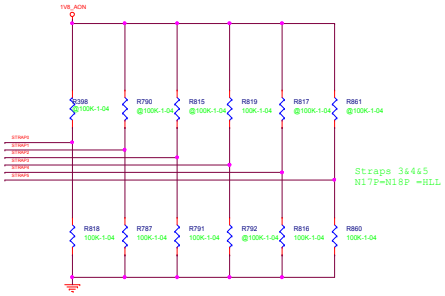
Title: 52 DGPU NV : GPIO/I2C/JTAG

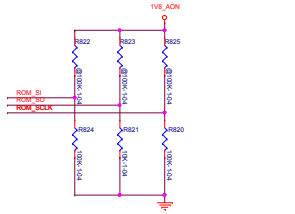
Size	Document Number	Rev
B	GI5CPXX	B

Date: Monday, December 24, 2018 Sheet 52 of 65









N18P pull low Stuff R824=R820=100K R821=10K
N17P pull High Stuff R822= R823= R825=100K

GDDR5 CFG Setting						
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
4GB	Samsung	K4G80325FB-HC28 B-die	0X0	L	L	L
4GB	Micron	MT51J256M32HF-70:A A-die	0X1	L	L	H
4GB	Hynix	H5GC8H24MJR-ROC M-die	0X2	L	H	L
2GB	Samsung	K4G41325FE-HC28 E-die	0X7	H	H	H
2GB	Micron	H5GC4H24AJR-ROC A-die	0X6	H	H	L
2GB	Hynix	EDW4032BABG-70-F A-die	0X8	L	L	M

Table 14. N17/GB4C-128 and N18/GB4D-128 Ternary Straps

Strap Pin	N17/GB4C-128	N18/GB4D-128
ROM_SI	SOR_EXPOSED[3:0]	Pull low to enable FS_OVERT*
ROM_SO[1]		
ROM_CLK		
STRAP5	• SMB_ALT_ADDR • DEVID_SEL • PCIE_CFG • VGA_DEVICE	• SMB_ALT_ADDR • DEVID_SEL • PCIE_CFG • VGA_DEVICE
STRAP4		
STRAP3		
STRAP2	RAMCFG[4:0]	RAMCFG[4:0]
STRAP1		
STRAP0		

Note:
1. The ROM_SO pin should be pulled low using a 10k-ohm resistor for N18/GB4D-128 GPUs and using a 100k-ohm resistor for N17/GB4C-128 GPUs.

N18P STRAPS

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

```
Strap5,4,3 LLH for N17&N18

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE(Select)

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL(Select)

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER(Select)

1:VGA_DEVICE ENABLE(Select)
0:VGA_DEVICE DISABLE
```

Table 12.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Note: The ternary strap pins listed in the STRAP columns must be pulled to one of three voltage levels. "L" means Low level (GND). "M" means Middle level (0.9V). "H" means High level (1.8V).

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.

	Voltage(V)		
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35 V and 1.5V[2]	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Samsung	K4G80325FC-HC25	C-die	0x0	8 Gbps	N/A	Full	Production candidate

N17P STRAPS

SOR_EXPOSED Audio Configuration Straps

Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is IFPD used? (Only supports eDP.)	See This Row of Table 5.5
4	4	NO	15
4	3	YES	13
3	3	NO	14
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8
1	0	YES	0
No other configurations are supported.			

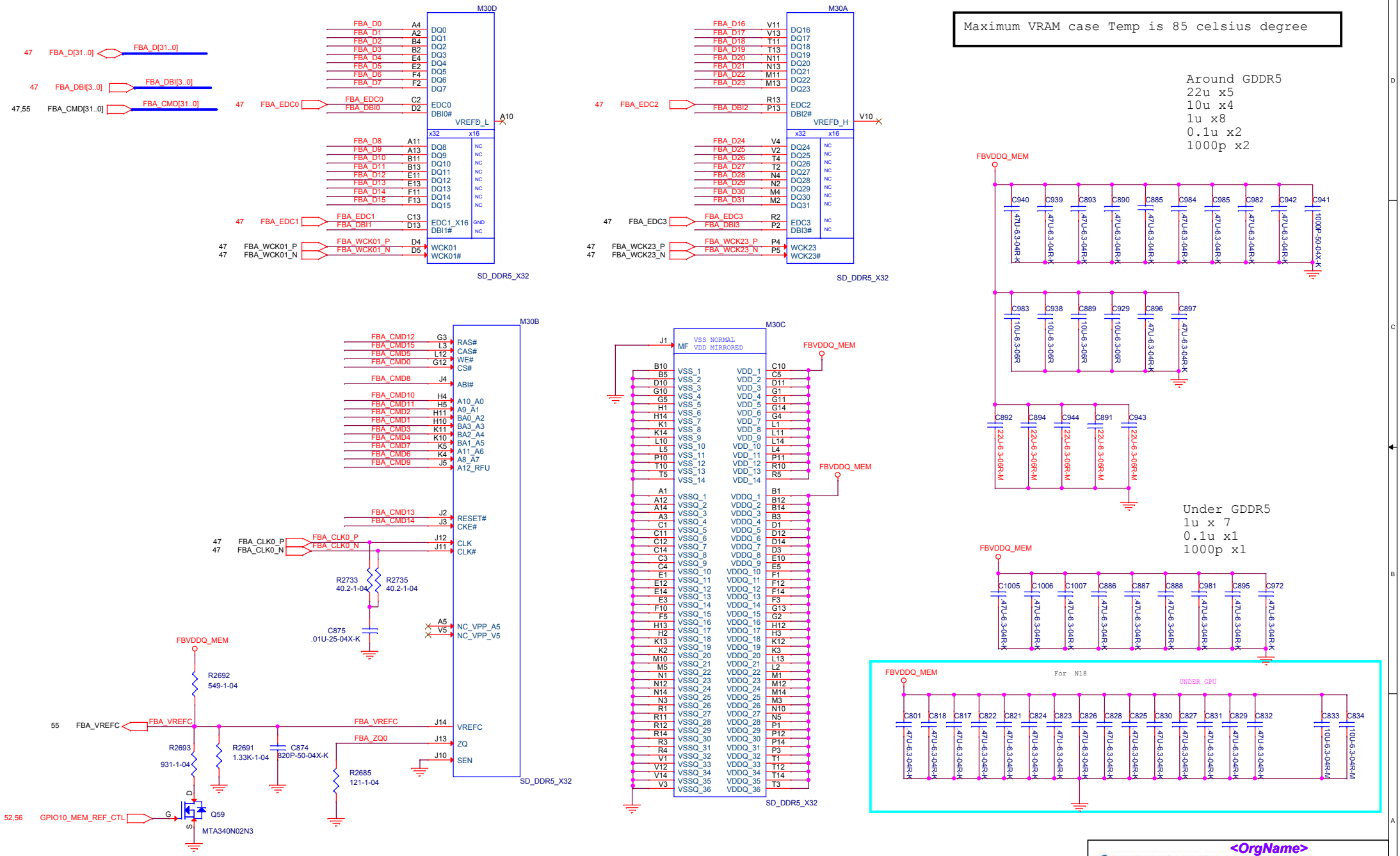
Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

N17X HW DG(DG-07875-001_v09) Page. 76

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1



<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title: 54 VRAM1 : FRAME BUFFER A

Size: Custom | Document Number: GI5CPXX | Rev: B

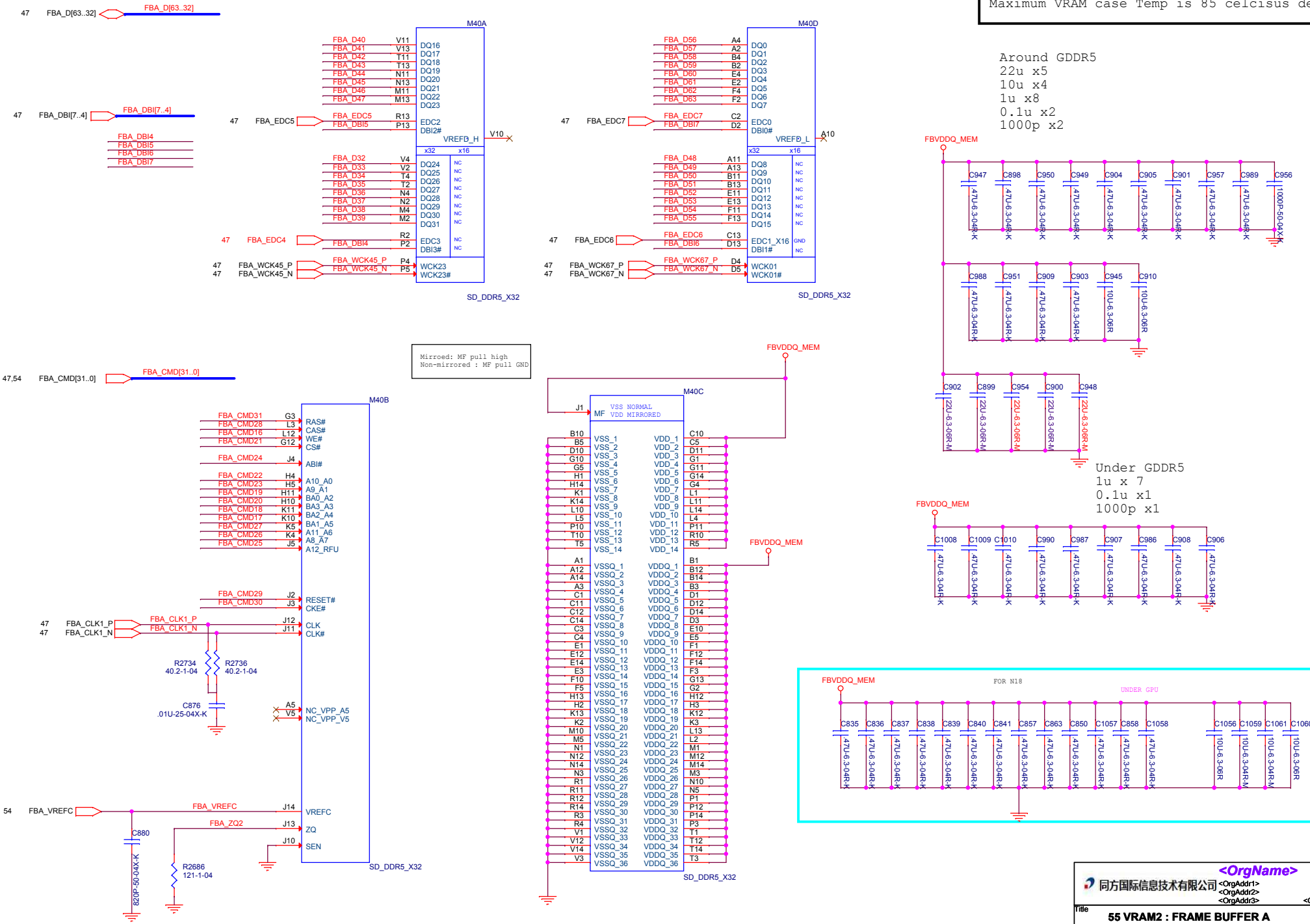
Date: Monday, December 24, 2018 | Sheet 54 of 65

Maximum VRAM case Temp is 85 celcisus degree

Around GDDR5
22u x5
10u x4
1u x8
0.1u x2
1000p x2

Under GDDR5
1u x 7
0.1u x1
1000p x1

Mirroed: MF pull high
Non-mirrored : MF pull GND



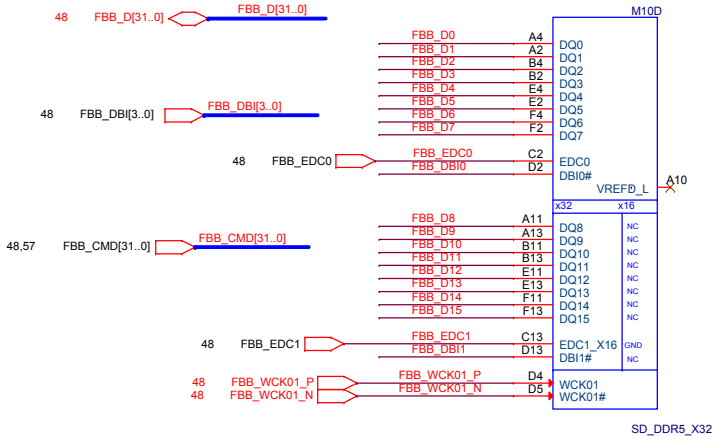
<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

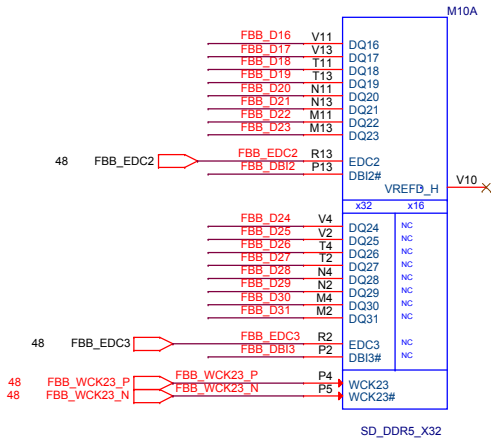
Title: 55 VRAM2 : FRAME BUFFER A

Size: Custom | Document Number: GI5CPXX | Rev: B

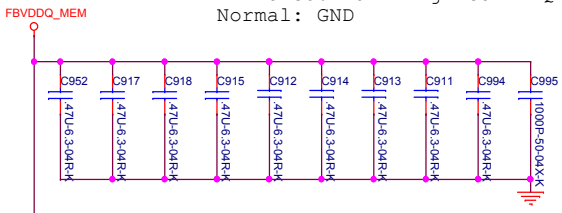
Date: Monday, December 24, 2018 | Sheet 55 of 65

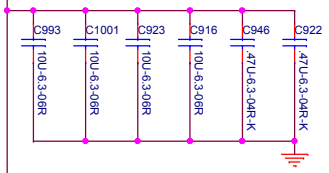
Maximum VRAM case Temp is 85 celcisus degree



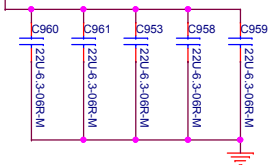


Mirrored: Pull high to VDDQ
Normal: GND

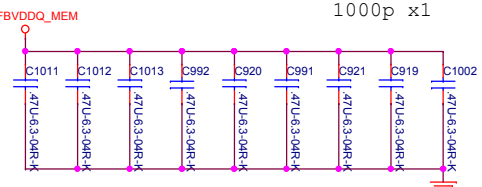


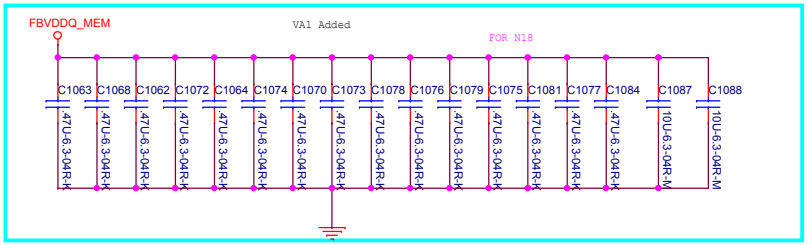


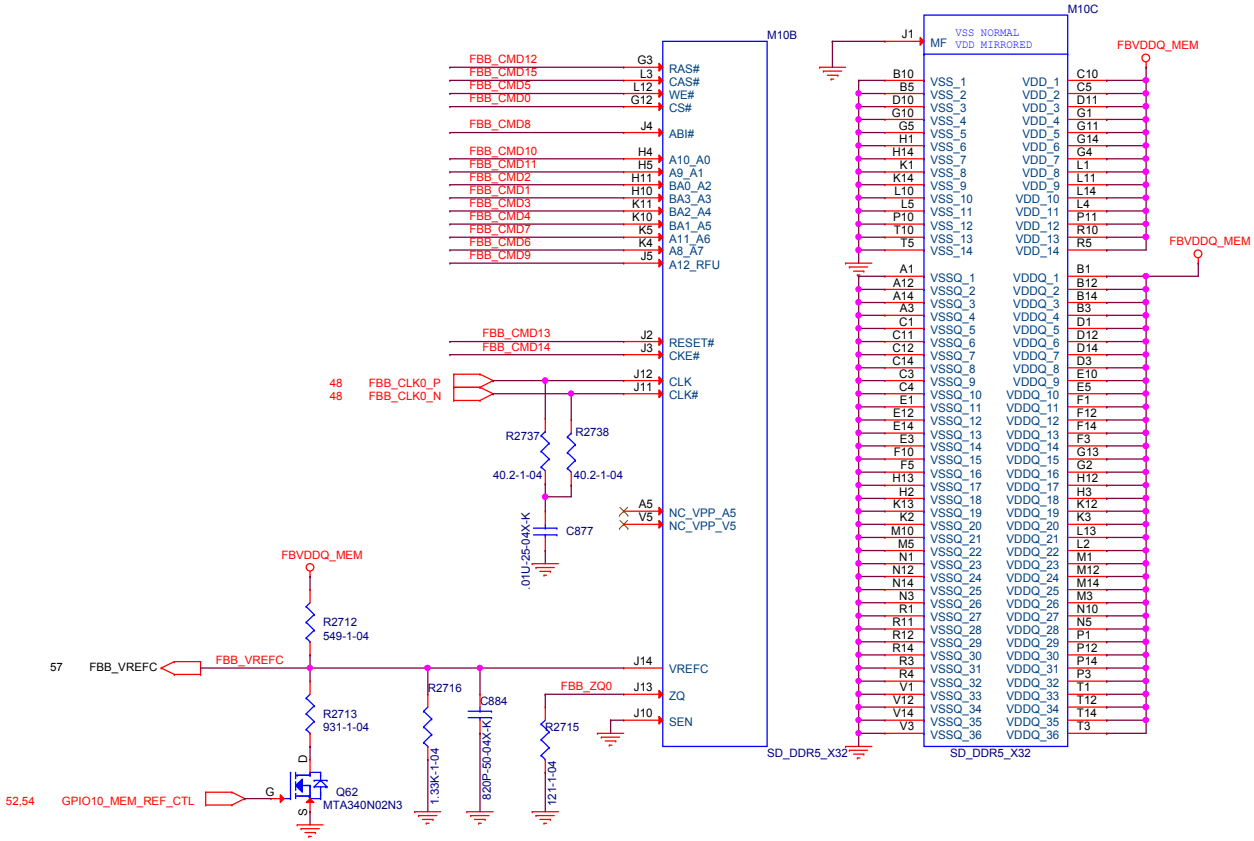
Around GDDR5
22u x5
10u x4
1u x8
0.1u x2
1000p x2



Under GDDR5
1u x 7
0.1u x1
1000p x1

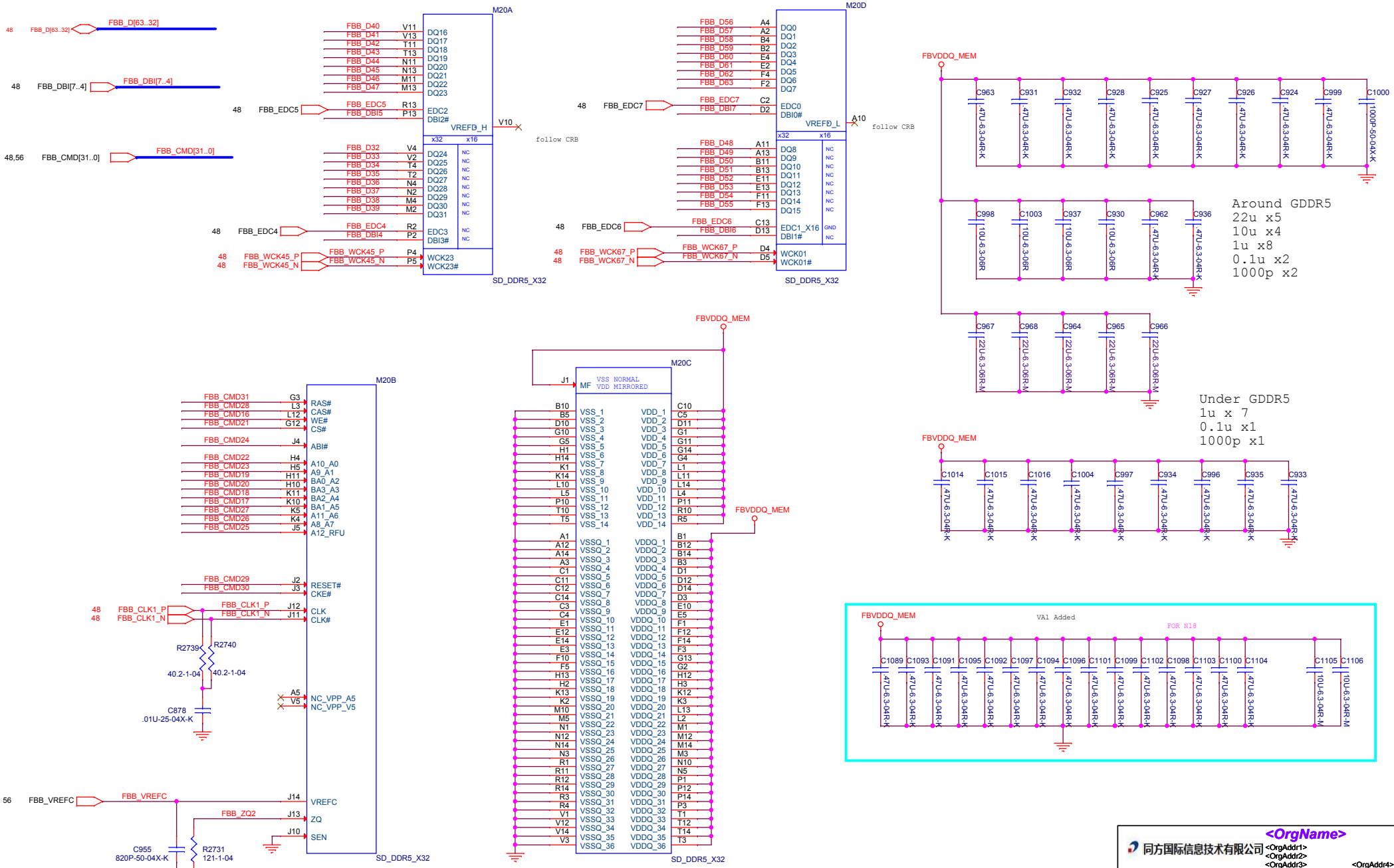




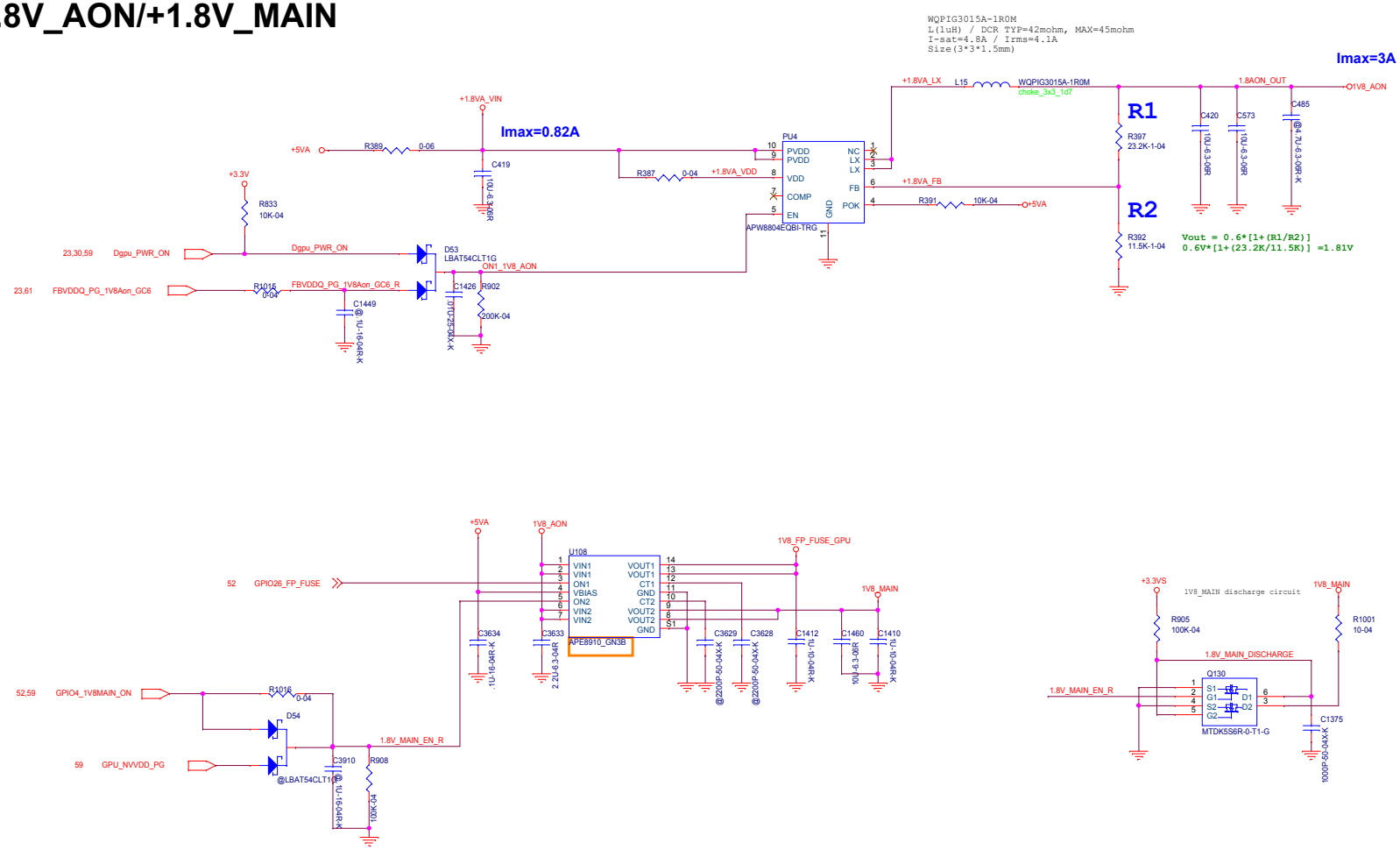


Company	<OrgName> 同方国际信息技术有限公司
Addr	<OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>
Title	56 VRAM3 : FRAME BUFFER B
Size	Custom
Document Number	GI5CPXX
Rev	B
Date	Monday, December 24, 2018
Sheet	56 of 65

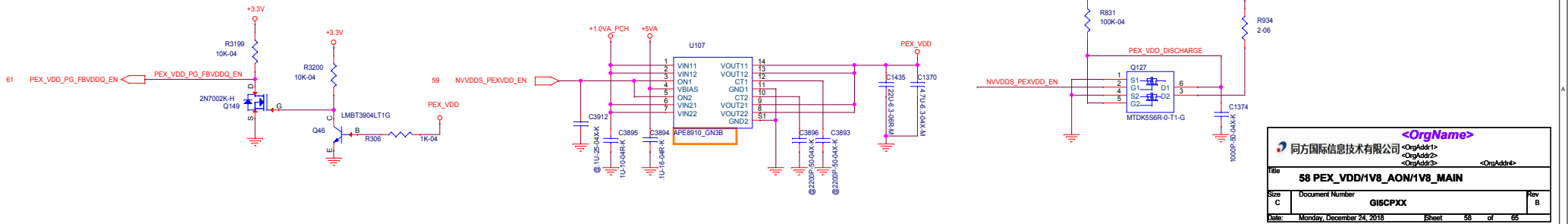
Maximum VRAM case Temp is 85 celcisus degree



+1.8V_AON/+1.8V_MAIN

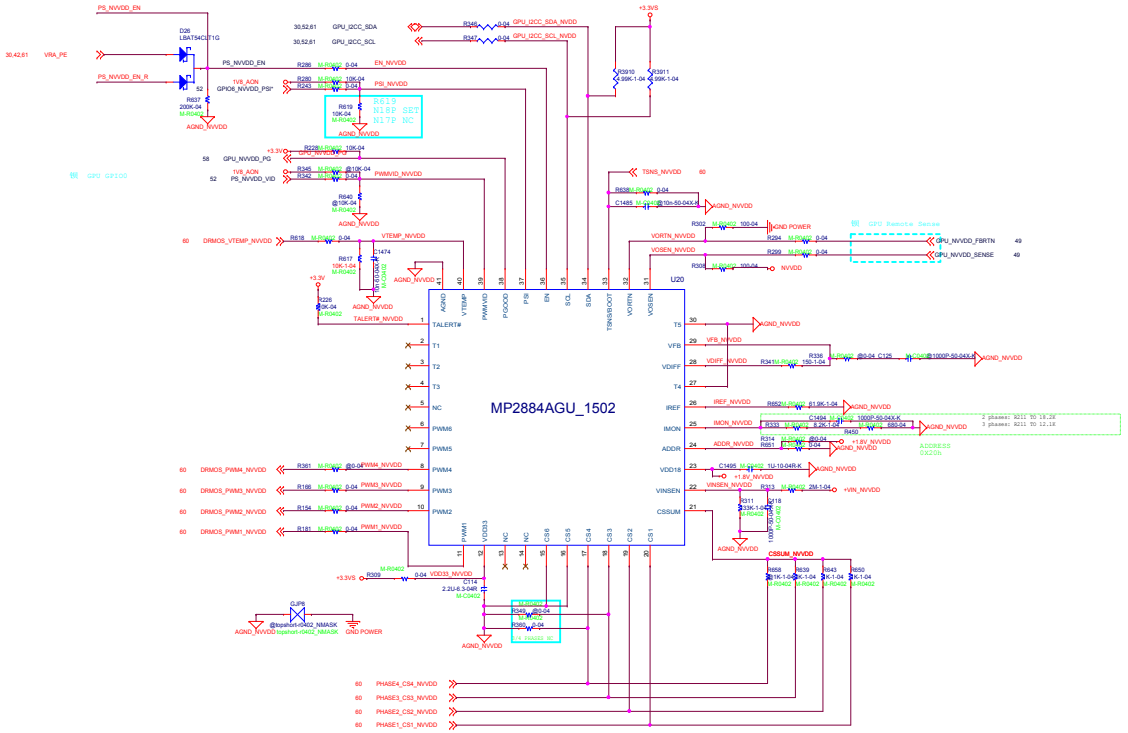


PEX_VDD Converter



<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

Title	58 PEX_VDD/1V8_AON/1V8_MAIN	
Size C	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 58 of 65	



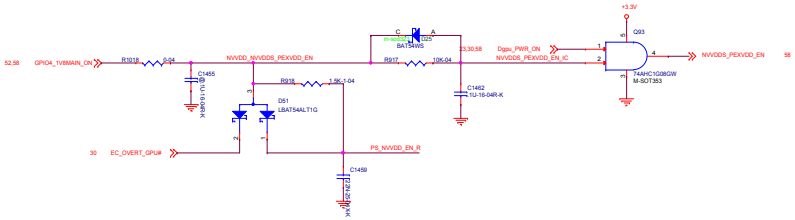
GPU	TGP (W)	GPU TDP[1,3,4] (W)	Memory TDP[2] (W)
H18P-G0	50	40	6
H18P-G0 Max-Q[5]	35	25	6

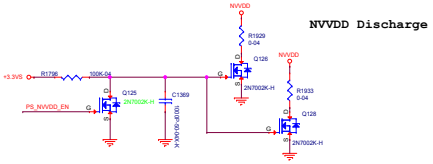
Table 10. Output EDP-Continuous (Estimated)

Product	NVVDD (A)	FB Total[5] 1.5V[4] (A)	1.0V Total[1] 1.0V[3] (A)	1.8V Total[2] 1.8V[3] (A)
H18P-G0	45	14	1.6	2.3
H18P-G0 Max-Q[6]	35	14	1.6	2.3

Table 12. Output EDP-Peak (Estimated)

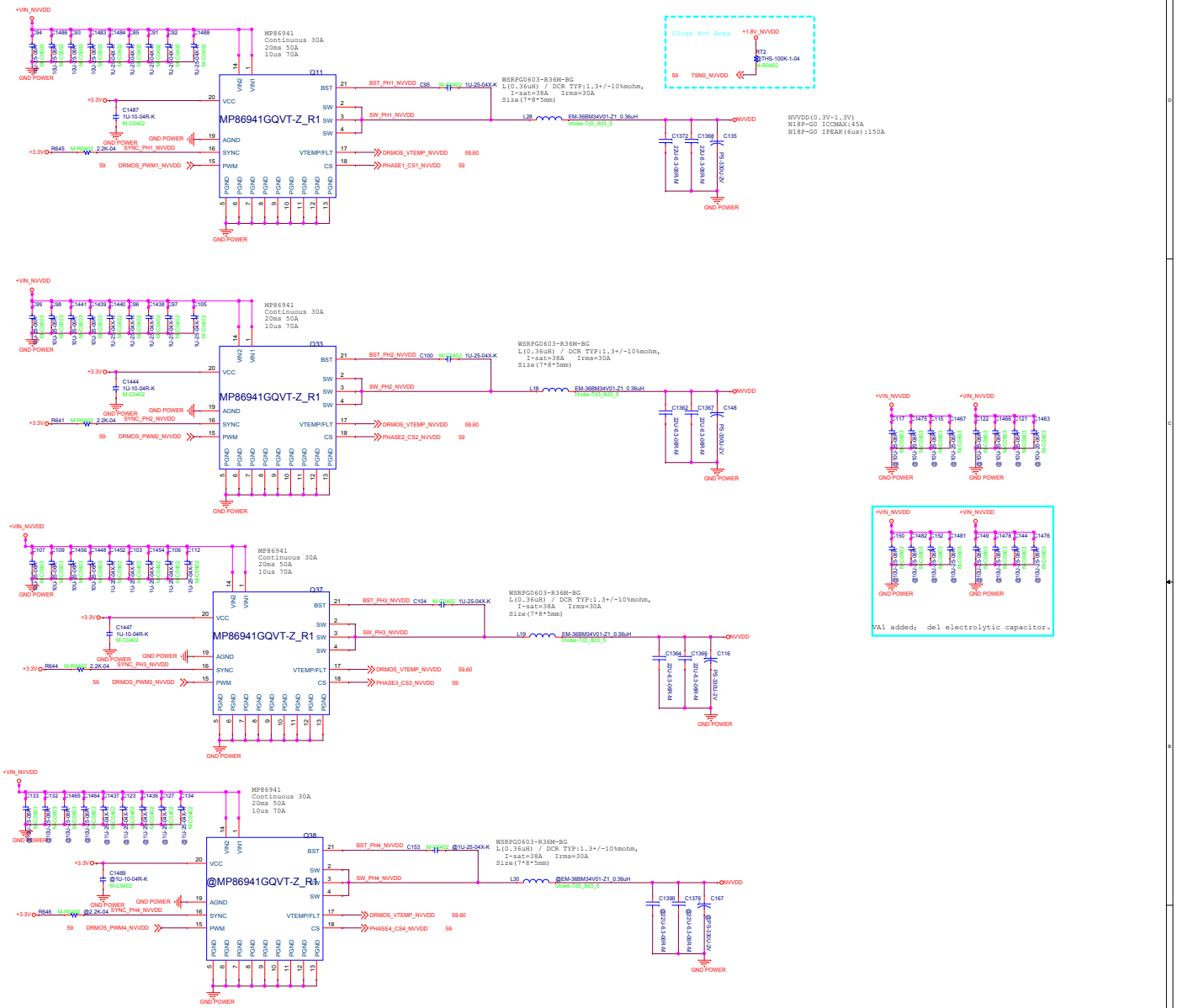
Product	NVVDD (A)	FB TOTAL[4] 1.5V[2, 3] (A)	1.0V Total[1] 1.0V[2] (A)
H18P-G0	150	20	TBD
H18P-G0 Max-Q[5]	150	20	TBD





同方国际信息技术有限公司

Title	60 NVVDD		
Size D	Document Number G16CPXX		Rev B
Date: Monday, December 24, 2018	Sheet 59 of 62		



<OrgName>
同方国际信息技术有限公司 <OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>

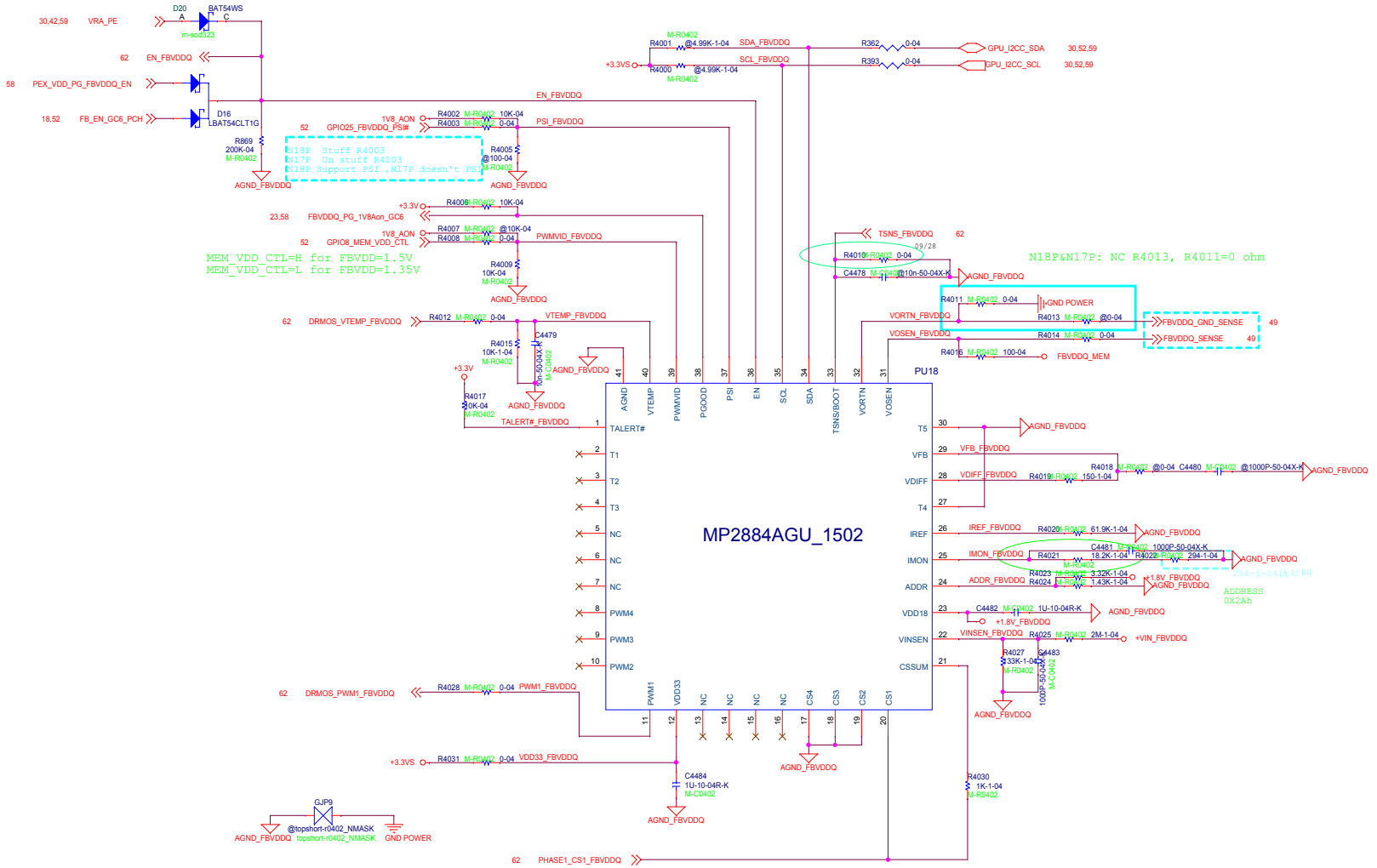
Title: 59 NVVDDS

Size	Document Number	Rev
Custom	G8CPXX	B

Date: Monday, December 24, 2018 Sheet 60 of 65

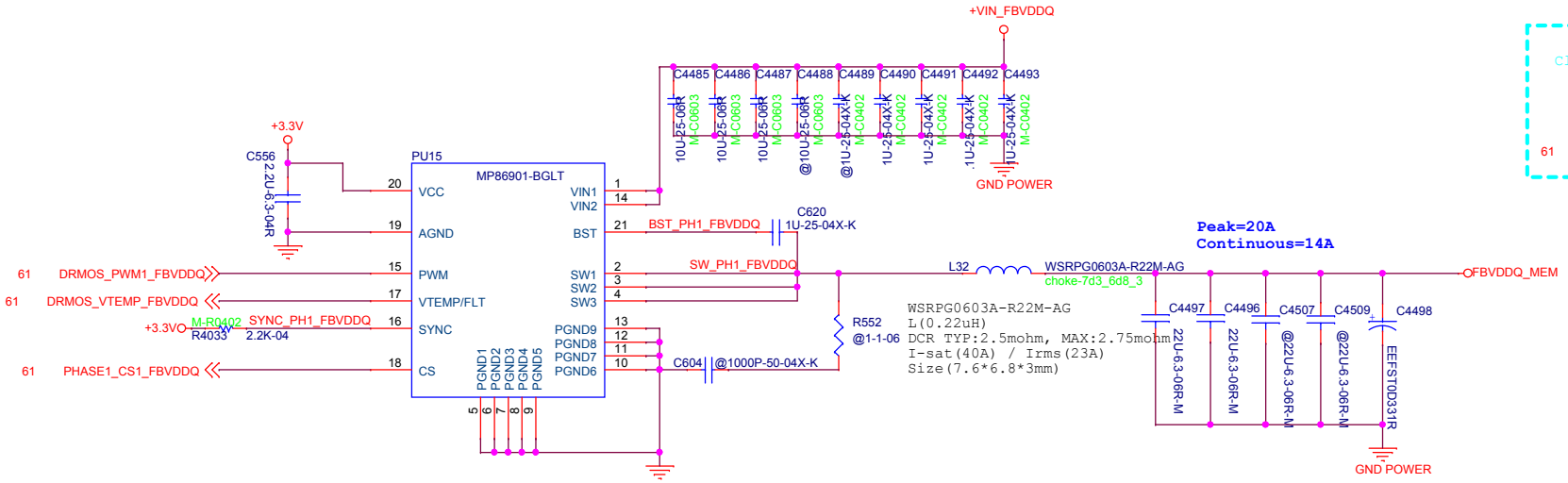
FBVDDQ_MEM

N18P-G1/G0 FBVDDQ:GDDR5
Peak: 20A
Continuous: 14A

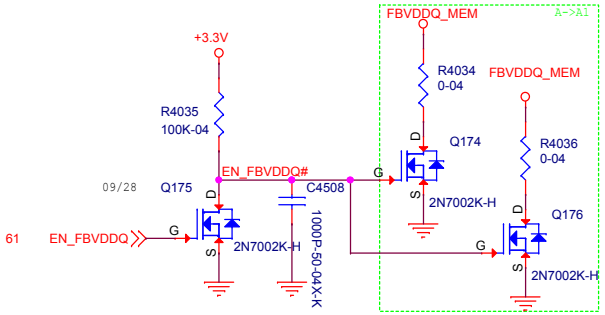


<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title	61 FBVDDQ_MEM	
Size C	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 61 of 65	

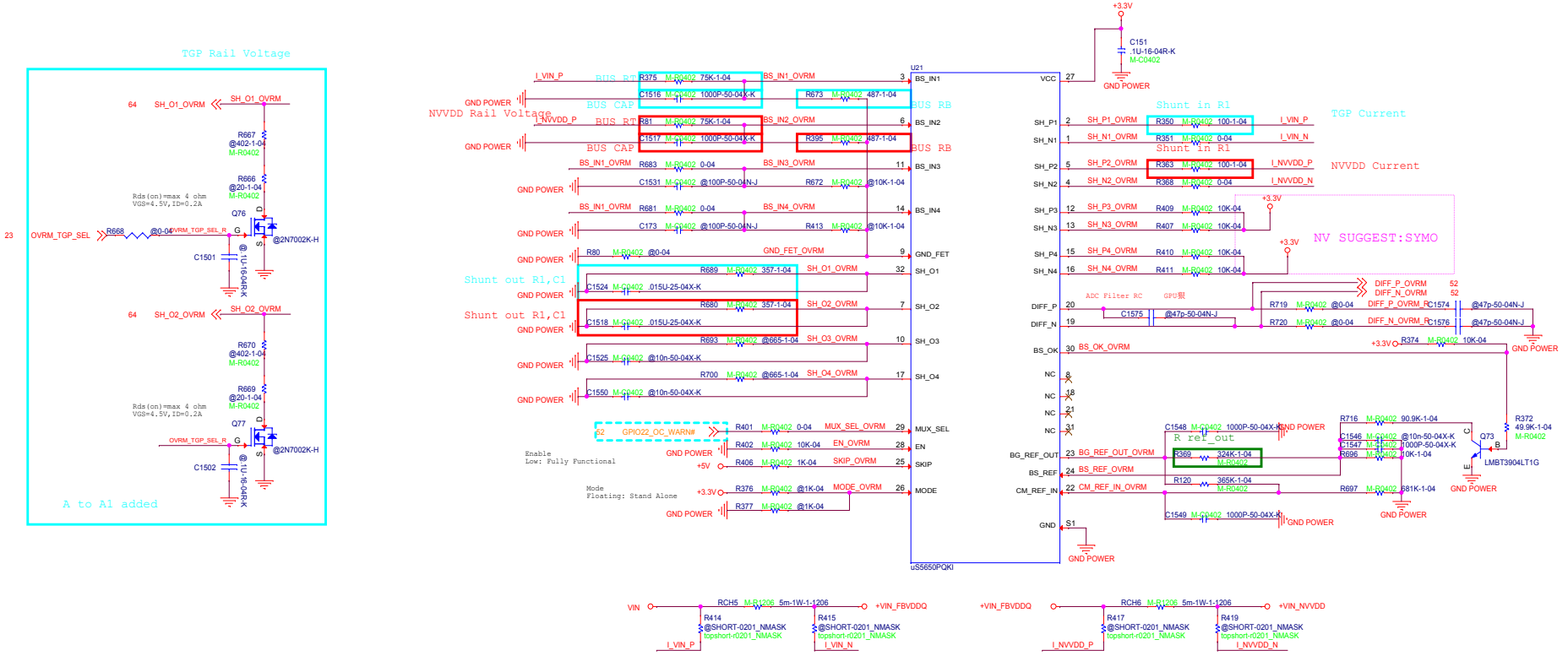


FBVDDQ_MEM_Discharge



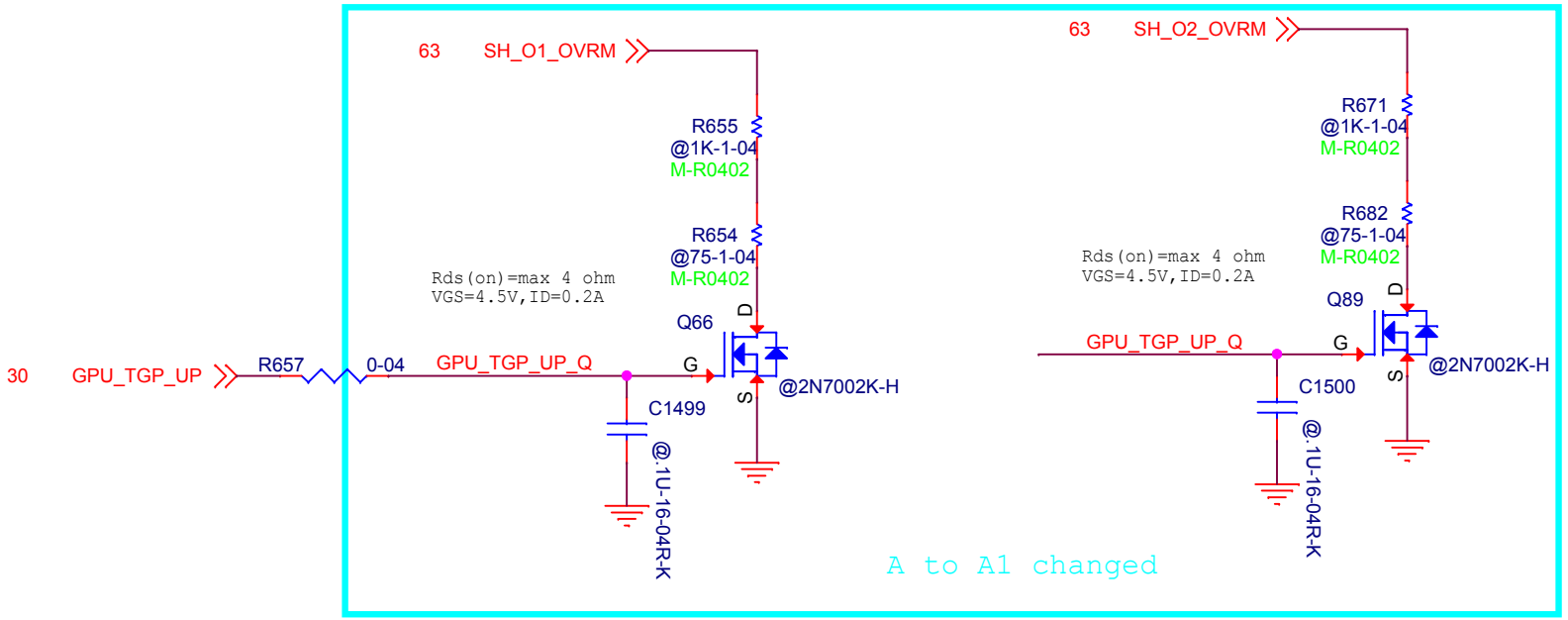
Title	62 N18P-G0_FBVDDQ_2PHASE	
Size B	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 62 of 65	

NC ALL FOR N17P



GPU	Component Values					
	R673, R395	R689, R680	R369	R375, R81	C1516, C1517	
N18P-G0	487Ω	357Ω	324KΩ	75KΩ	1.0nf	N18P-G0 TGP=50W
N18P-G0 MAX-Q						
150W+	487Ω	127Ω	324KΩ	75KΩ	1.0nf	
115W to 130W	487Ω	143Ω	324KΩ	75KΩ	1.0nf	
100W to 110W	487Ω	165Ω	324KΩ	75KΩ	1.0nf	
75W to 90W	487Ω	215Ω	324KΩ	75KΩ	1.0nf	
70W or lower	487Ω	357Ω	324KΩ	75KΩ	1.0nf	

Title	63 POWER N18P OVR-M		
Size C	Document Number GI5CPXX		Rev B
Date: Monday, December 24, 2018	Sheet 63 of 65		



TGP Control / TGP Watt	GPU_TGP_UP	OVRM_TGP_SEL
OVER 130W	HIGH	HIGH
100W TO 110W	HIGH	LOW
115W TO 130W (7S)	LOW	HIGH
75W TO 90W (7Z)	LOW	LOW

N18P-G0 TGP=50W

Title	64 OWER N18P TGP SENSE	
Size A	Document Number GI5CPXX	Rev B
Date: Monday, December 24, 2018	Sheet 64 of 65	

Version A

1. 11/9 NC R354 as EC internal PU.
2. 11/12stuff R543.
2. 11/12stuff R3069

<OrgName>
同方国际信息技术有限公司
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

Title: 65 History

Size: C | Document Number: GI5CPXX | Rev: B

Date: Monday, December 24, 2018 | Sheet 65 of 65