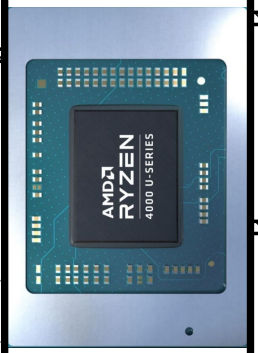
400s 15" AMD Renoir UMA

01



AMD APU

Renoir (FP6)

Power : 15W

Package : FP5 BGA

PAGE 2~14

DDR4 16GB — RVS — PAGE 28 — DDR4 2400 MT/s

DDR4 16GB — STD — PAGE 29 — DDR4 2400 MT/s

DDI0 x2 — *HD and FHD* — eDP PAGE 34

DDI1 x4 — HDMI 1.4 + Re-driver Parade PS8203 PAGE 35

USB2.0 — DP1.3 / USB 3.1 Combo port [Type C] PAGE 63

DP1.2/USB 3.1 gen1 *2 — PI3DPX1207B — MUX — PAGE 58 — DP1.2/USB 3.1 gen1 *2

DP AUX — SBU

I2C — USB Type-C Controller Cypress CCG5C PAGE 61 — CC — I2C — To KBC PAGE 47~48

USB2.0 — USB 2.0 power port (left side) PAGE 34 — on Daughter Board

USB3.0/2.0*2 — USB 3.0 Standar port*2 PAGE 57

USB2.0 Interface

primary HDD 2.5" / 7, 9.5mm PAGE 44 — SATA0 6GB/s

Camera Port 7 PAGE 34

Fingerprint VFS7552 FP Module PN: FM-3439 for 15: PAGE 52

PCIE *1 — NGFF PAGE 43 WLAN Combo — on Daughter Board

PCIE *1 — Card Reader controller RTS5237S-GR PAGE 1 — SD Socket PAGE 2

PCIE *1 — 10/100/1000 NIC Realtek RTL8111HSH PAGE 40 — RJ45 PAGE 40

SATA0 6GB/s PCIE *4 — NGFF SSD Package : 22*80 (mm) Power : PAGE 43

48MHz

32.768KHz

EC Private SPI ROM 16MB PAGE 56

LPC Interface

Keyboard PAGE 50

Battery PAGE 82

FAN PAGE 54

KBC Nuvoton NPCX797HA0BX BGA type Embedded Controller PAGE 47~48

SPI Interface

Level shifter TI SN74AVC2T45YZP PAGE 56

Level shifter NXP NTB0104GU12 PAGE 56

TPM Infineon SLB 9670VQ2.0 PAGE 51

System BIOS SPI ROM 16MB PAGE 56

HD Audio — Audio Codec Realtek ALC3247 PAGE 36 — Digital MIC PAGE 36 — Speaker PAGE 36 — Combo Jack PAGE 37

PCB 8L STACK UP (1.1mm)

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

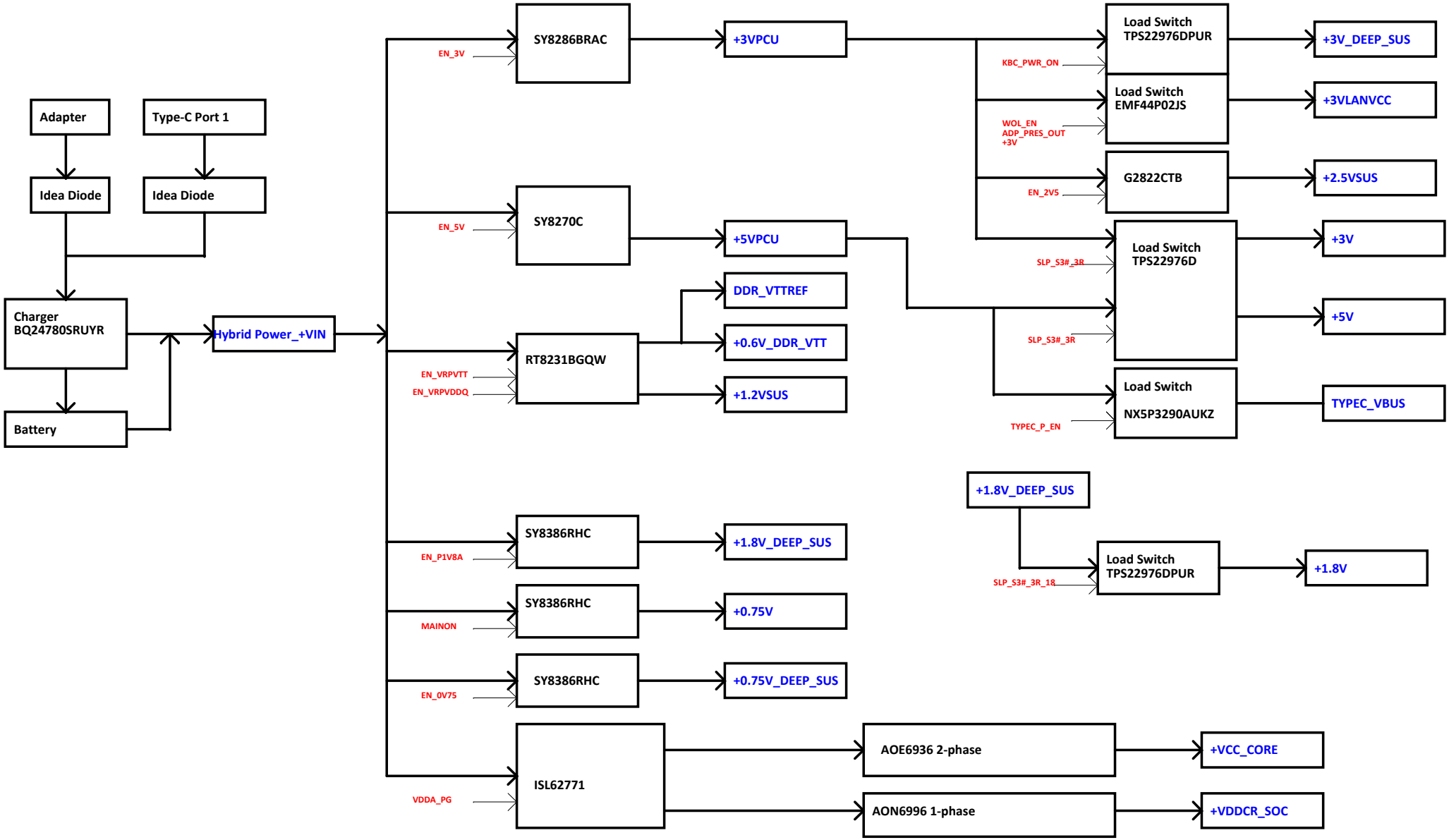
Quanta Computer Inc.
PROJECT: X9M

NB5 Custom

Size	Document Number	Rev
	AMD Block Diagram	1A
Date: Thursday, February 06, 2020	Sheet 1 of 68	

POWER BLOCK DIAGRAM

02



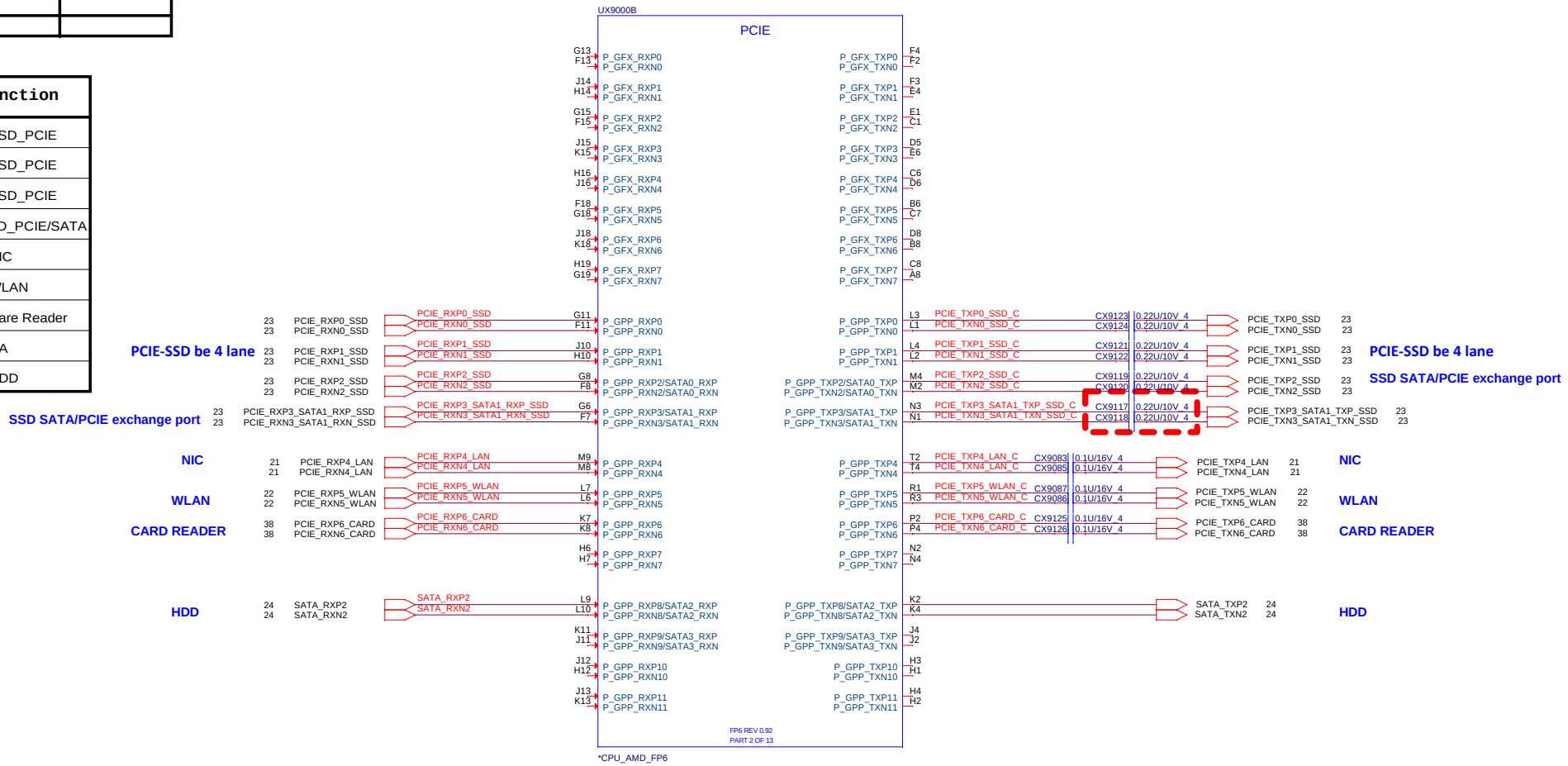
Quanta Computer Inc.		
PROJECT: X9M		
Size: NB5 Custom	Document Number: Power Block Diagram	Rev: 1A
Date: Thursday, February 06, 2020	Sheet 2 of 68	

APU PCIE

04

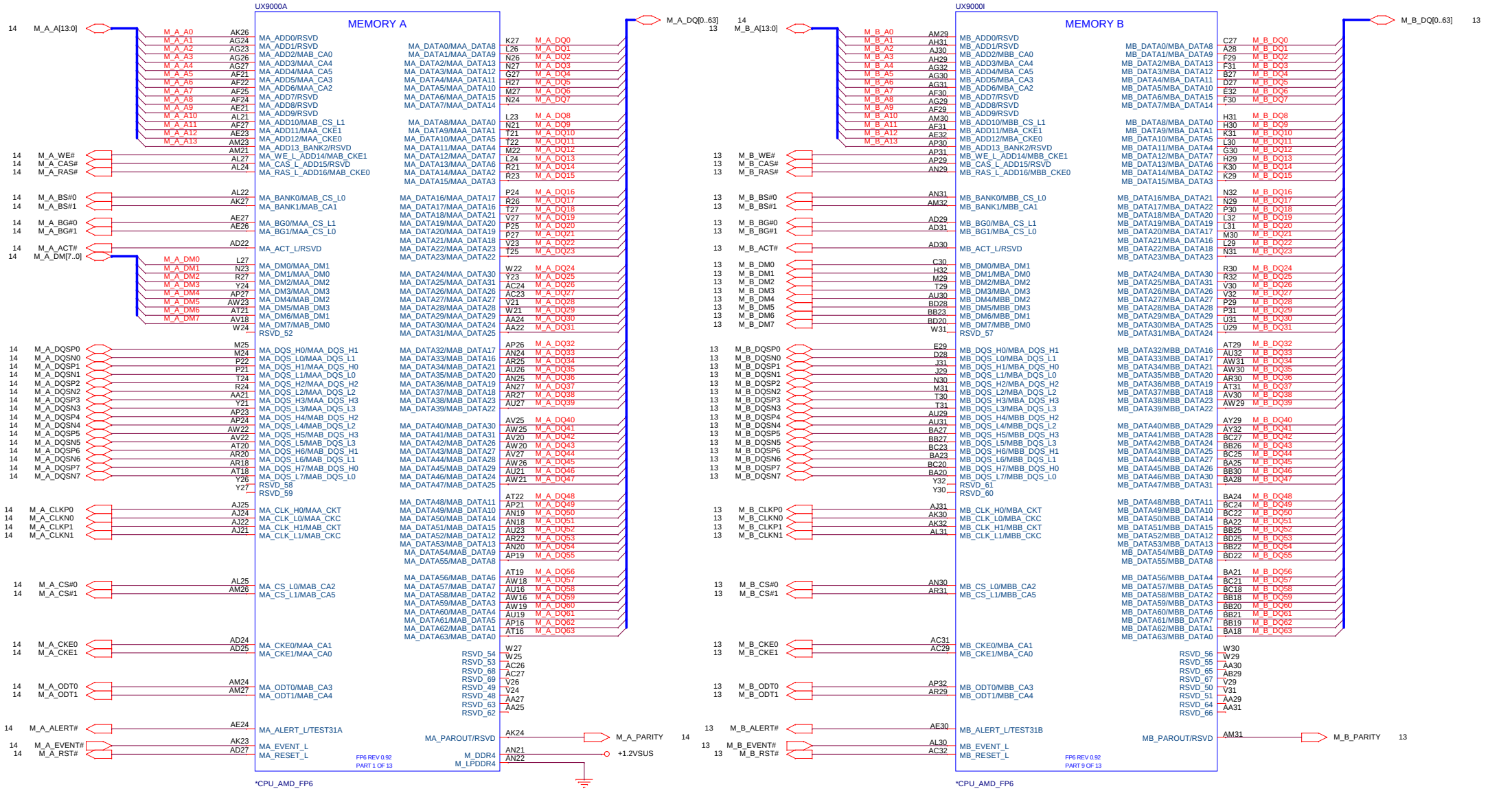
AMD APU	TOP BSQ	QBCON

PCIE Port	Function
PCIE_0	SSD_PCIE
PCIE_1	SSD_PCIE
PCIE_2	SSD_PCIE
PCIE_3	SSD_PCIE/SATA
PCIE_4	NIC
PCIE_5	WLAN
PCIE_6	Care Reader
PCIE_7	NA
PCIE_8	HDD



APU MEMORY

05



Quanta Computer Inc.	
PROJECT: X9M	
Size: NB5 Custom	Document Number: RR 2/7(MEM)
Rev: 1A	
Date: Thursday, February 06, 2020	Sheet 4 of 68

APU DISPLAY and MISC

06

UX9000C

DISPLAY/SVI2/JTAG/TEST

eDP Panel

HDMI

eDP

HDMI

TypeC
PU For internal
PD For customer

10/08: SI , change to 1K for LG Panel PWM

ESD mount

2018/12/12 PV STAGE
stuff CX9066/CX9067 to solve ESD issue

APU Serial VID

2018/08/27 :
SVC and SVD change to 22ohm

400 G7

Boot-VID code

SVC	SVD	VOLTAGE
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Close to HDT & No remove.

Can remove on MP

HDT+ Connector for Debug only

APU_PROCHOT# Signal Level :

*CPU_AMD_FP6

FP6 REV 0.92
PART 3 OF 13

HDT9000
None-CIS
HDT CONN
88511-2001-20p-I

Quanta Computer Inc.
PROJECT: X9M

Size	Document Number	Rev
NB5 Custom	RR 3/7(DIS/MISC)	1A
Date: Thursday, February 06, 2020	Sheet 5 of 68	

APU GPIO/AZ/UART

07

ACPI/AUDIO/I2C/GPIO/MISC

UX9000D

CLK/LPC/EMMC/SD/SPI/eSPI/UART

UX9000E

HDA INTERFACE

2019/07/10
AMD modern standby

8/21 : Pull-High RUNSCI_EC#

2019/09/16 SI STAGE
CX9096/CX9097 change to 3.3P to accurate

2019/09/17 SI STAGE
CX9094/CX9095 change to 15P to accurate

2019/02/26 MV:
TPX9029 add Pull high 10K(RX9772) to +3.3V

Close to CPU

400 G7

*CPU_AMD_FP6

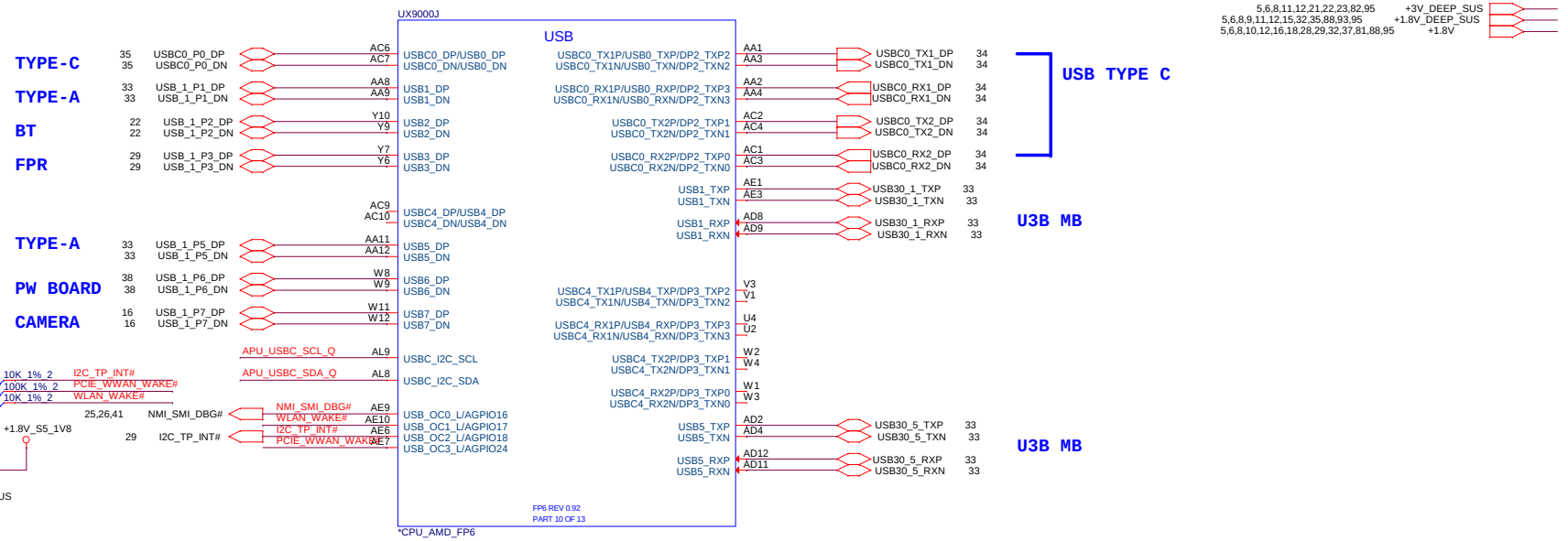
FP6 REV 0.92
PART 4 OF 13

FP6 REV 0.92
PART 5 OF 13

Quanta Computer Inc.			
PROJECT: X9M			
NB5 Custom	Size	Document Number: RR 4/7(GPIO/HDA/SPI/I2C)	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 6 of 68	

USB2 Port	Function
USB0	TYPE-C
USB1	TYPE-A
USB2	BT
USB3	FP
USB5	TYPE-A
USB6	TYPE-A (USB/B)
USB7	Camera

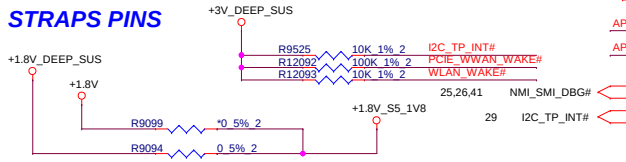
USB3 and USB2 Port Mapping

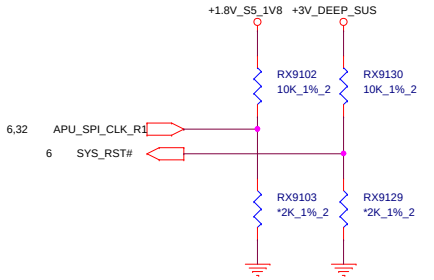


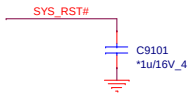
5,6,8,11,12,21,22,23,82,95 +3V_DEEP_SUS
5,6,8,9,11,12,15,32,35,88,93,95 +1.8V_DEEP_SUS
5,6,8,10,12,16,18,28,29,32,37,81,88,95 +1.8V

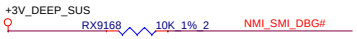
08

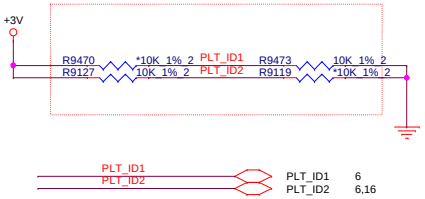
STRAPS PINS











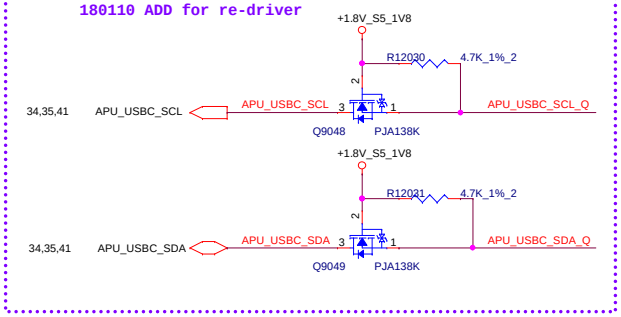
REQUIRED STRAPS

	APU_SPI_CLK	SYS_RST# (Int Pull-Up)
PULL HIGH	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	normal reset mode (DEFAULT)
PULL LOW	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

	PLT_ID1	PLT_ID2
	EGPIO142	AGPIO86
14"	0	1
15"	0	0
Reserved	1	0
Reserved	0	0

2019/06/04 : PLT_ID2 distinguish 14" or 15"

180110 ADD for re-driver



Quanta Computer Inc.
PROJECT: X9M

Size	Document Number	Rev
NB5 Custom	RR 5/7(USB/STRAP)	1A
Date: Thursday, February 06, 2020	Sheet 7 of 68	

APU POWER

09

4,11,13,14,37,87,97 +1.2VSUS
12,92 +0.75V_DEEP_SUS
5,6,7,10,12,16,18,28,29,32,37,81,88,95 +1.8V
5,6,7,10,11,12,13,14,15,16,17,18,21,22,23,25,26,27,29,30,31,32,35,37,38,81,88,95 +3V
5,6,7,11,12,21,22,23,82,95 +3V_DEEP_SUS
37,88,89 +VCC_CORE
5,6,7,9,11,12,15,32,35,88,93,95 +1.8V_DEEP_SUS
5,12,37,92,95 +0.75V
6,10,11,12,15,16,18,22,25,26,27,28,31,32,34,35,37,39,41,80,82,85,86,87,92,93,95,97 +3VPCU

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 7*22UF+1*1UF+1*180PF

+VDDCR_SOC

CX9025 180p/50V_4 | CX9020 1u/6.3V_4 | CX9027 22U/6.3VS_6 | CX9021 22U/6.3VS_6 | CX9022 22U/6.3VS_6 | CX9005 22U/6.3VS_6 | CX9004 22U/6.3VS_6 | CX9003 22U/6.3VS_6 | CX9002 22U/6.3VS_6

RR DG: 9*22UF+2*1UF+4*0.22uf+3*180PF

BOTTOM SIDE DECOUPLING UNDER APU

VDDIO_MEM-DDR4:6A

+1.2VSUS

CX9007 22u/6.3V_6 | CX9034 22u/6.3V_6 | CX9032 22u/6.3V_6 | CX9026 22u/6.3V_6 | CX9040 22u/6.3V_6 | CX9010 22u/6.3V_6 | CX9008 22u/6.3V_6 | CX9009 22u/6.3V_6 | CX9006 22u/6.3V_6 | CX9017 1u/6.3V_4 | CX9016 1u/6.3V_4 | CX9041 180p/50V_4

CX9011 0.22U/10V_4 | CX9014 0.22U/10V_4 | CX9013 0.22U/10V_4 | CX9012 0.22U/10V_4 | CX9001 180p/50V_4 | CX9015 180p/50V_4

2018/12/12 PV STAGE
RX9059 change to short_pad

RR DG: 1*22UF+3*1UF

If the VSS plane is cut to create a VDDIO_MEM_S3 plane, ceramic capacitors with NP0 or C0G dielectric are connected across the VDDIO_MEM_S3 and VSS plane split.

+0.75V_DEEP_SUS | +VDDP_S5 | 2A

RX9059 *0_5%_4/S
RX9060 *0_5%_4/S

CX9062 22u/6.3V_6 | CX9053 1u/6.3V_4 | CX9051 1u/6.3V_4 | CX9070 1u/6.3V_4

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 1*22UF+1*1UF

+1.8V_DEEP_SUS | +APU_VDDIO_AZ | 0.2A

RX9058 0_5%_6

400 G7

CX9055 1u/6.3V_4 | CX9061 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 1*22UF+2*1UF

+3V | +APU_VDD_33 | 0.25A

RX9055 0_5%_6

400 G7

CX9068 1u/6.3V_4 | CX9052 1u/6.3V_4 | CX9059 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 1*22UF+2*1UF

+3V_DEEP_SUS | +APU_VDD_33_S5 | 0.25A

RX9057 0_5%_6

400 G7

CX9069 1u/6.3V_4 | CX9072 1u/6.3V_4 | CX9060 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

+1.8V | +VDD_18 | 2.5A

RR DG: 1*22UF+2*1UF

RX9046 0_5%_6
RX9048 0_5%_6

400 G7

CX9047 1u/6.3V_4 | CX9050 1u/6.3V_4 | CX9057 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

VDDBT_RTC | 4.5uA

RX9031 *0_5%_4 | CX9064 0.22U/10V_4 | CX9063 1u/6.3V_4

RX9045 1K_1%_4 +3V_RTC

+1.8V_DEEP_SUS | +VDD_18_S5 | 1A

RR DG: 1*22UF+2*1UF

RX9049 0_5%_6

400 G7

CX9071 1u/6.3V_4 | CX9054 1u/6.3V_4 | CX9058 22u/6.3V_6

BOTTOM SIDE DECOUPLING UNDER APU

+VDDCR_SOC

UX9000F

POWER

N16	VDDCR_SOC_1	13A	70A
N18	VDDCR_SOC_2		
N20	VDDCR_SOC_3		
P17	VDDCR_SOC_4		
P19	VDDCR_SOC_5		
R18	VDDCR_SOC_6		
R20	VDDCR_SOC_7		
T19	VDDCR_SOC_8		
U18	VDDCR_SOC_9		
U20	VDDCR_SOC_10		
V19	VDDCR_SOC_11		
W18	VDDCR_SOC_12		
W20	VDDCR_SOC_13		
Y19	VDDCR_SOC_14		

AC20	VDDIO_MEM_S3_1	
AC28	VDDIO_MEM_S3_2	
AD23	VDDIO_MEM_S3_3	
AD26	VDDIO_MEM_S3_4	
AD28	VDDIO_MEM_S3_5	
AD32	VDDIO_MEM_S3_6	
AE20	VDDIO_MEM_S3_7	
AE22	VDDIO_MEM_S3_8	
AE25	VDDIO_MEM_S3_9	
AE28	VDDIO_MEM_S3_10	
AF23	VDDIO_MEM_S3_11	
AF26	VDDIO_MEM_S3_12	
AF28	VDDIO_MEM_S3_13	
AF32	VDDIO_MEM_S3_14	
AG20	VDDIO_MEM_S3_15	
AG22	VDDIO_MEM_S3_16	
AG25	VDDIO_MEM_S3_17	
AG28	VDDIO_MEM_S3_18	
AJ20	VDDIO_MEM_S3_19	
AJ23	VDDIO_MEM_S3_20	
AJ26	VDDIO_MEM_S3_21	
AJ28	VDDIO_MEM_S3_22	
AJ32	VDDIO_MEM_S3_23	
AK22	VDDIO_MEM_S3_24	
AK25	VDDIO_MEM_S3_25	
AK28	VDDIO_MEM_S3_26	
AL23	VDDIO_MEM_S3_27	
AL26	VDDIO_MEM_S3_28	
AL28	VDDIO_MEM_S3_29	
AL32	VDDIO_MEM_S3_30	
AM22	VDDIO_MEM_S3_31	
AM25	VDDIO_MEM_S3_32	
AM28	VDDIO_MEM_S3_33	
AN28	VDDIO_MEM_S3_34	
AN32	VDDIO_MEM_S3_35	
AP28	VDDIO_MEM_S3_36	
AR32	VDDIO_MEM_S3_37	

AC21	VDDIO_VPH_1	
AD21	VDDIO_VPH_2	
AP9	VDDIO_AUDIO	0.2A
AL18	VDD_33_1	0.25A
AM17	VDD_33_2	
AL20	VDD_18_1	2.5A
AM19	VDD_18_2	
AL19	VDD_18_S5_1	1A
AM18	VDD_18_S5_2	
AL17	VDD_33_S5_1	0.25A
AM16	VDD_33_S5_2	
AL11	VDDP_S5_1	2A
AL12	VDDP_S5_2	
AM12	VDDP_S5_3	
M15	VDDP_1	2A
M16	VDDP_2	
M18	VDDP_3	
AJ11	VDDBT_RTC_G	

FP6 REV 0.92
PART 6 OF 13

*CPU_AMD_FP6

RX9775 0_5%_6
CX9131 22u/6.3V_6

+APU_VDDIO_AZ
+APU_VDD_33
+VDD_18
+VDD_18_S5
+APU_VDD_33_S5
+VDDP_S5
+VDDP_S0
VDDBT_RTC

+VCC_CORE

CX9031 22U/6.3VS_6 | CX9023 22U/6.3VS_6 | CX9033 22U/6.3VS_6 | CX9029 22U/6.3VS_6 | CX9024 22U/6.3VS_6

RR DG: 16*22UF+1*180PF

CX9028 22U/6.3VS_6 | CX9018 22U/6.3VS_6 | CX9019 22U/6.3VS_6 | CX9036 22U/6.3VS_6

CX9045 22U/6.3VS_6 | CX9042 22U/6.3VS_6 | CX9035 22U/6.3VS_6 | CX9037 22U/6.3VS_6 | CX9038 22U/6.3VS_6 | CX9030 22U/6.3VS_6 | CX9039 22U/6.3VS_6 | CX9043 180p/50V_4

BOTTOM SIDE DECOUPLING UNDER APU

RR DG: 2*22UF+8*1UF+1*180PF

+0.75V | 2A | +VDDP_S0

RX9134 *0_5%_6_S
RX9133 *0_5%_6_S

BOTTOM SIDE DECOUPLING UNDER APU

CX9105 1u/6.3V_4 | CX9044 180p/50V_4 | CX9049 1u/6.3V_4 | CX9046 1u/6.3V_4 | CX9048 1u/6.3V_4

CX9113 22u/6.3V_6 | CX9112 22u/6.3V_6 | CX9111 1u/6.3V_4

CX9106 1u/6.3V_4 | CX9104 1u/6.3V_4 | CX9110 1u/6.3V_4

+BAT

RX9132 470_1%_4 +VCCRTC_2

+3VPCU

DX9005 BAT54CW

+3V_RTC | 20MIL

0.1U/16V/X7R_4 CX9116

CX9114 1u/6.3V_4

+3V_RTC

CX9115 10u/6.3V_4

Quanta Computer Inc.
PROJECT: X9M

NB5 Custom

Size	Document Number	Rev
	RR 6/7(POWER)	1A

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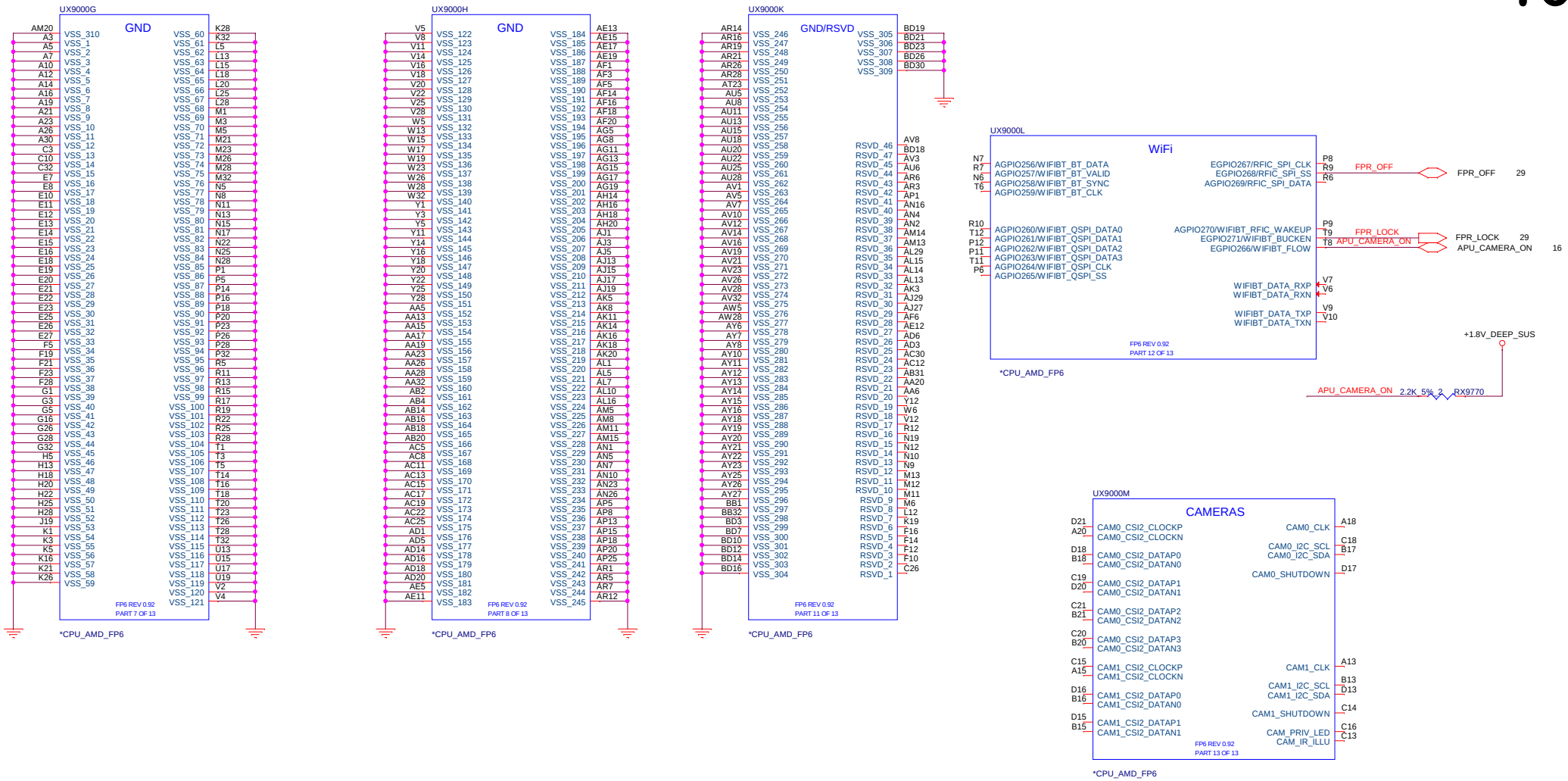
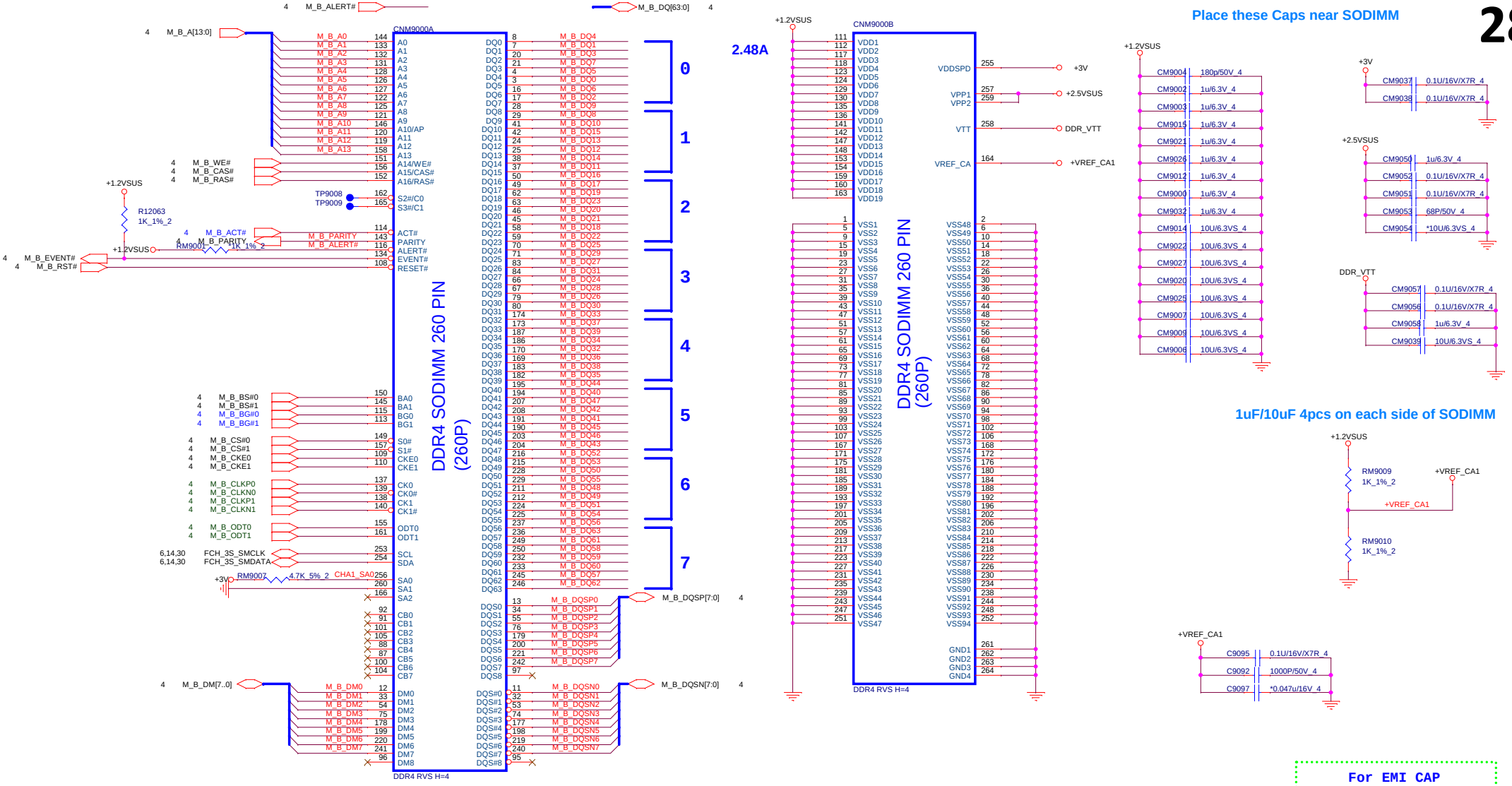
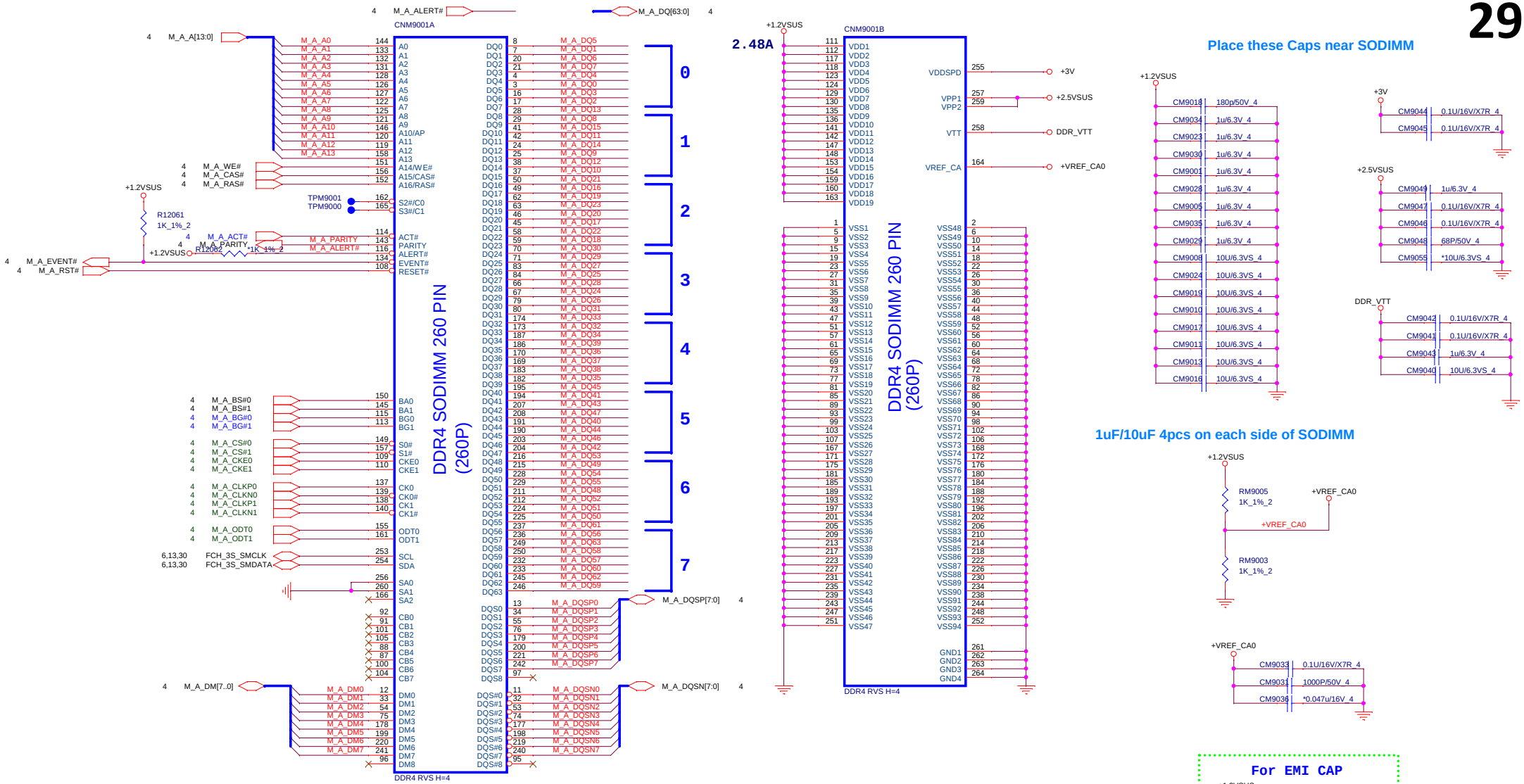
APU GND



NB5 Custom	Quanta Computer Inc. PROJECT: X9M	
	Size / Document Number: RR 7/7(GND/RSVD)	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 9 of 68



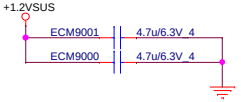
Quanta Computer Inc.	
PROJECT: X9M	
Size	Document Number: CHA0 DDR4 DIMM0 — Rev: 1A
Custom	Date: Thursday, February 06, 2020 — Sheet 13 of 68



Place these Caps near SODIMM

1uF/10uF 4pcs on each side of SODIMM

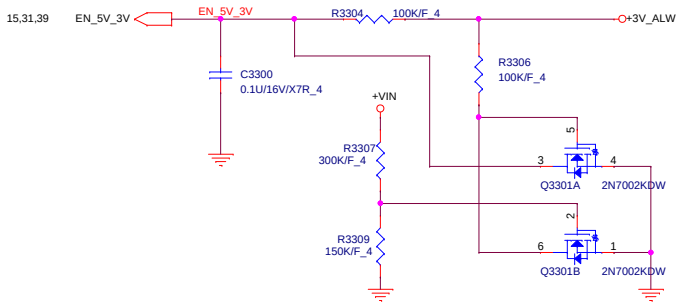
For EMI CAP

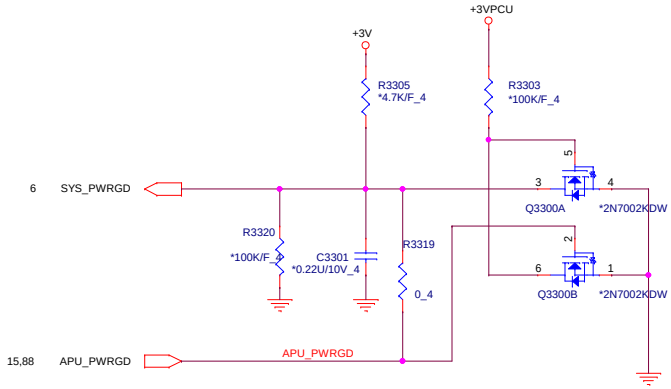


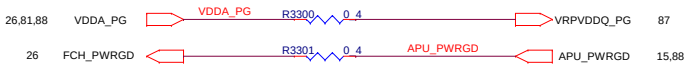
2018/12/17 PV STAGE
ECM9000/ECM9001 stuff 4.7u for RF

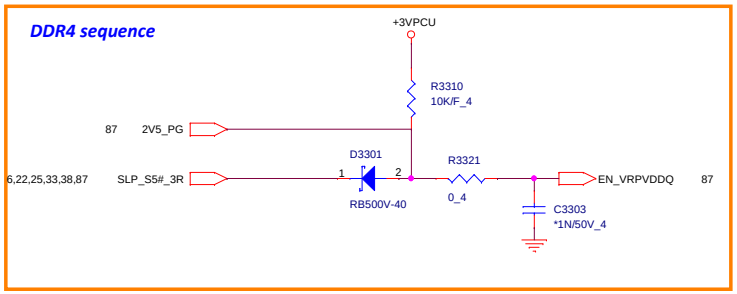
Quanta Computer Inc.		
PROJECT: X9M		
NB5 Custom	Size / Document Number: CHA1 DDR4 DIMM1	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 14 of 68

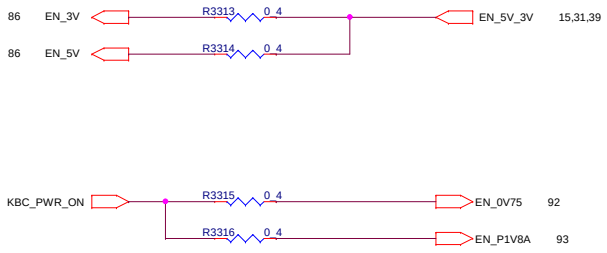
POWER TO EE NET NAME CONNECTION For AMD

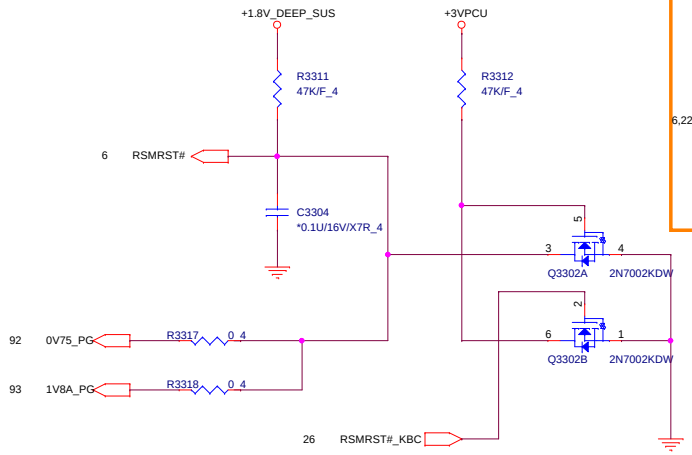












Quanta Computer Inc.			
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NB5 Custom	Size	Document Number: POWER ENABLE	Rev: 1A
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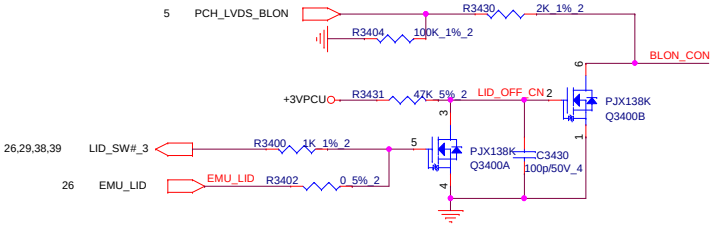
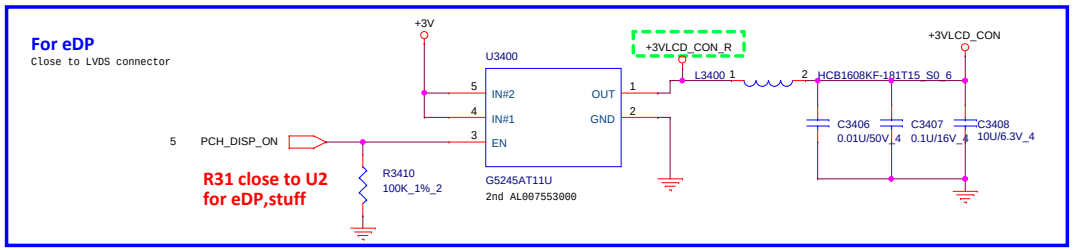
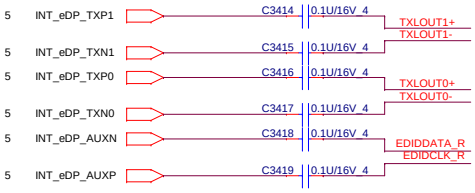
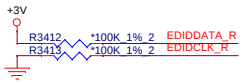
LID Switch

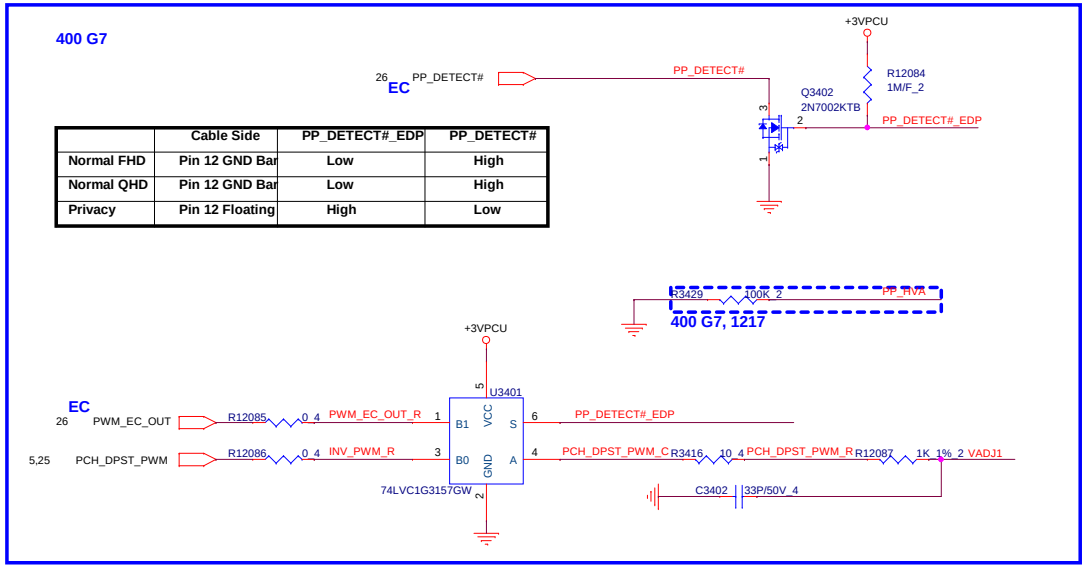
EMU_LID need confirm with GPIO by EC



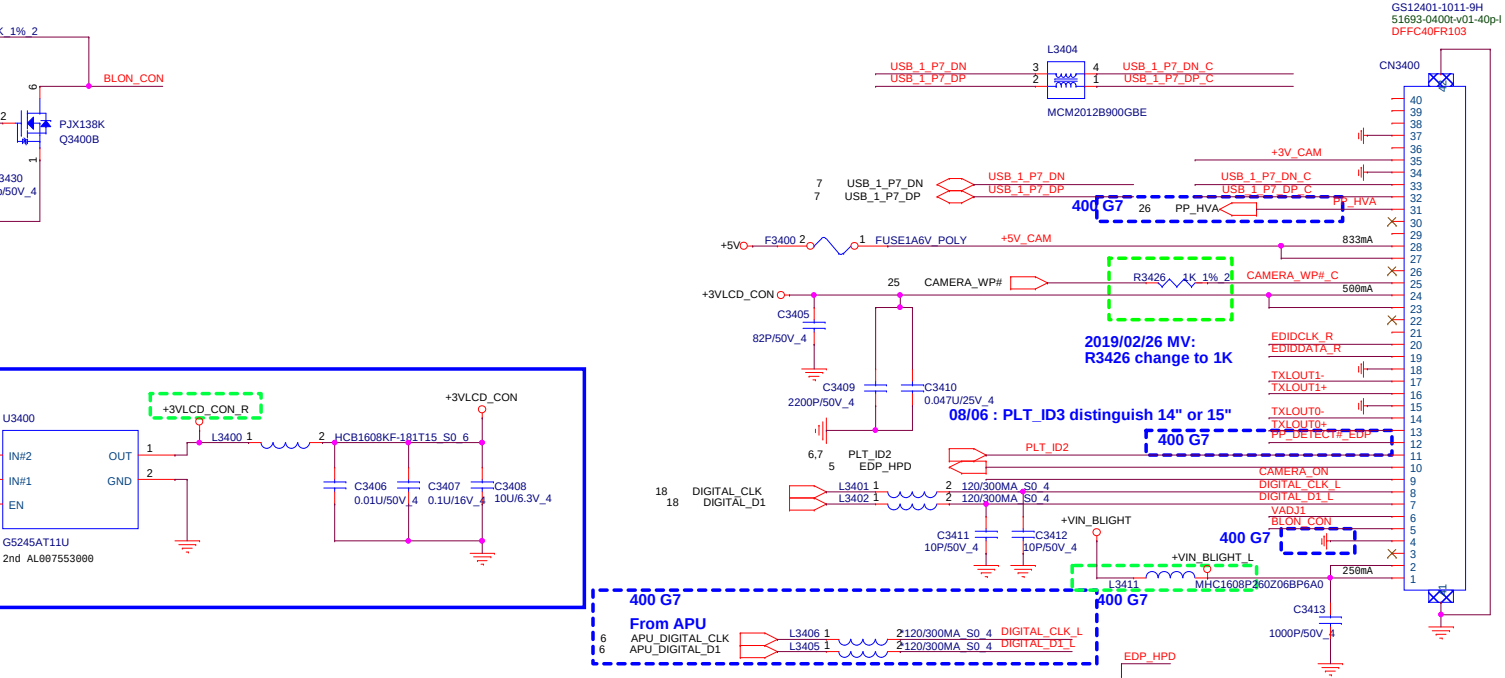


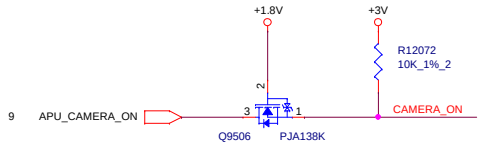


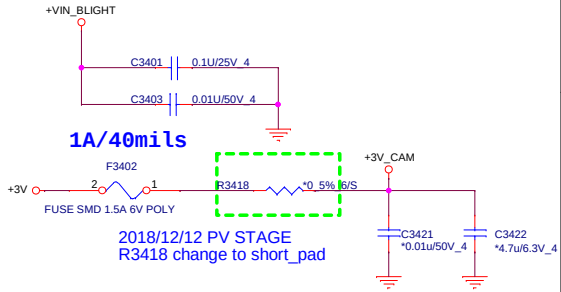




	Cable Side	PP_DETECT#_EDP	PP_DETECT#
Normal FHD	Pin 12 GND Bar	Low	High
Normal QHD	Pin 12 GND Bar	Low	High
Privacy	Pin 12 Floating	High	Low







5,6,7,8,10,11,12,13,14,15,17,18,21,22,23,25,26,27,29,30,31,32,35,37,38,81,88,95 +3V
10,12,17,18,24,27,31,37,95 +5V
11,12,15,37,41,82,86,87,89,90,92,93,97 +VIN

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EMI Solution

TX2_HDMI+	R3500	*150_5%_4	TX2_HDMI-
TX1_HDMI+	R3501	*150_5%_4	TX1_HDMI-
TX0_HDMI+	R3502	*150_5%_4	TX0_HDMI-
TXC_HDMI+	R3503	*150_5%_4	TXC_HDMI-

Output pre-emphasis setting; Internal pull down at ~150k次, 3.3V I/O.
L: no pre-emphasis
H: 2.5dB pre-emphasis

PRE R3504 *4.7K_5%_2 +3V
R3505 *4.7K_5%_2

Receiver equalization setting; Internal pull down at ~150k次, 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
M: programmable EQ for channel loss up to 8.6dB @ 3Gbps

DCIN_EN R3506 *4.7K_5%_2 +3V

DC cou;ing enable; Internal pull down at ~150k次, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input

EQ R3507 *4.7K_5%_2 +3V
R3508 *4.7K_5%_2

0905 : Update U3500 Footprint

+5V → C3500 0.1U/16V_4
U3500 G5250Q1T73U: IN (3), GND (2), OUT (1) → +5V_HDMIC
C3501 *0.01U/50V_4
C3502 0.1U/16V_4
C3503 *10U/6.3V_4

U3501 PS8203

Pin	Name	Pin	Name
38	EPAD3	35	EPAD7
39	EPAD4	34	EPAD8
40	EPAD5	36	EPAD1
41	EPAD6	37	EPAD2
1	IN_D2p	27	OUT_D2p
2	IN_D2n	26	OUT_D2n
3	HPD_SRC	25	HPD_SNK
4	IN_D1p	24	OUT_D1p
5	IN_D1n	23	OUT_D1n
6	IN_D0p	22	OUT_D0p
7	IN_D0n	21	OUT_D0n
8	DCIN_EN	20	CFG
9	IN_CKp	19	OUT_CKp
10	IN_CKn	18	OUT_CKn
11	VDD	17	CEXT
33	EPAD9	32	SDA_SRC
31	SCL_SRC	30	VDDIO
29	SDA_SNK	28	SCL_SNK
12	PD#	13	EQ
14	GND	15	PRE
16	REXT		

DPB_DDCDATA, DPB_DDCCLK, HDMI_UP_DATA, HDMI_UP_CLK

5 IN_D2 / IN_D2# / HDMI_HPD_CON / IN_D1 / IN_D1# / IN_D0 / IN_D0# / IN_CLK / IN_CLK#
C3509 0.1U/16V_4 C_TX2_HDMI+
C3510 0.1U/16V_4 C_TX2_HDMI-
HDMI_HPD_CON
C3511 0.1U/16V_4 C_TX1_HDMI+
C3512 0.1U/16V_4 C_TX1_HDMI-
C3513 0.1U/16V_4 C_TX0_HDMI+
C3514 0.1U/16V_4 C_TX0_HDMI-
DCIN_EN
C3515 0.1U/16V_4 C_TXC_HDMI+
C3516 0.1U/16V_4 C_TXC_HDMI-
+3V

HDMI_HPD

C3504 0.1U/16V_4

EQ R3509 5.9K_1%_4
PRE

CN3500 DP/HDMI CONN hdmi-hmrf2-ak520c-20p-smt

Pin	Name
1	TX2_HDMI+
2	D2+
3	TX2_HDMI-
4	GND_1
5	TX1_HDMI+
6	D2-
7	TX1_HDMI-
8	D1+
9	TX0_HDMI+
10	GND_2
11	TX0_HDMI-
12	D1-
13	TXC_HDMI+
14	D0+
15	TXC_HDMI-
16	GND_3
17	D0-
18	CK+
19	GND_4
20	CK-
21	CE Remote
22	NC
23	DDC CLK
24	DDC DATA
25	GND_DPAUX
26	+5V
27	HP DET
28	HD_DP_Option
29	X_DP(PWR)
30	SHELL1
31	SHELL2

+5V_HDMIC
R3510 2.2K_5%_2 HDMI_UP_CLK
R3511 2.2K_5%_2 HDMI_UP_DATA
C3517 *10P/50V_4
C3518 *10P/50V_4
+5V_HDMIC
HDMI_HPD
VC3500 *TVM0G5R5M220R
C3520 *220P/50V_4

+5V_HDMIC
C3519 *0.01U/50V_4
for EMI request

+3V
C3505 0.1U/16V_4
C3506 0.1U/16V_4

VDD for PS8203:
Power supply at 3.3V

+3V
C3507 0.1U/16V_4
C3508 0.1U/16V_4

VDDIO:
Supply voltage for DDC passive gate and used to set HPD_SRC output level
Its range can be 1.2V~3.6V

HDMI SMBus Isolation

+3V R3512 2.2K_5%_2
5 DPB_DDCCLK DPB_DDCCLK
5 DPB_DDCDATA DPB_DDCDATA
+3V R3513 2.2K_5%_2

NB5 Custom

Quanta Computer Inc.
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	HDMI CONNECTOR	1A

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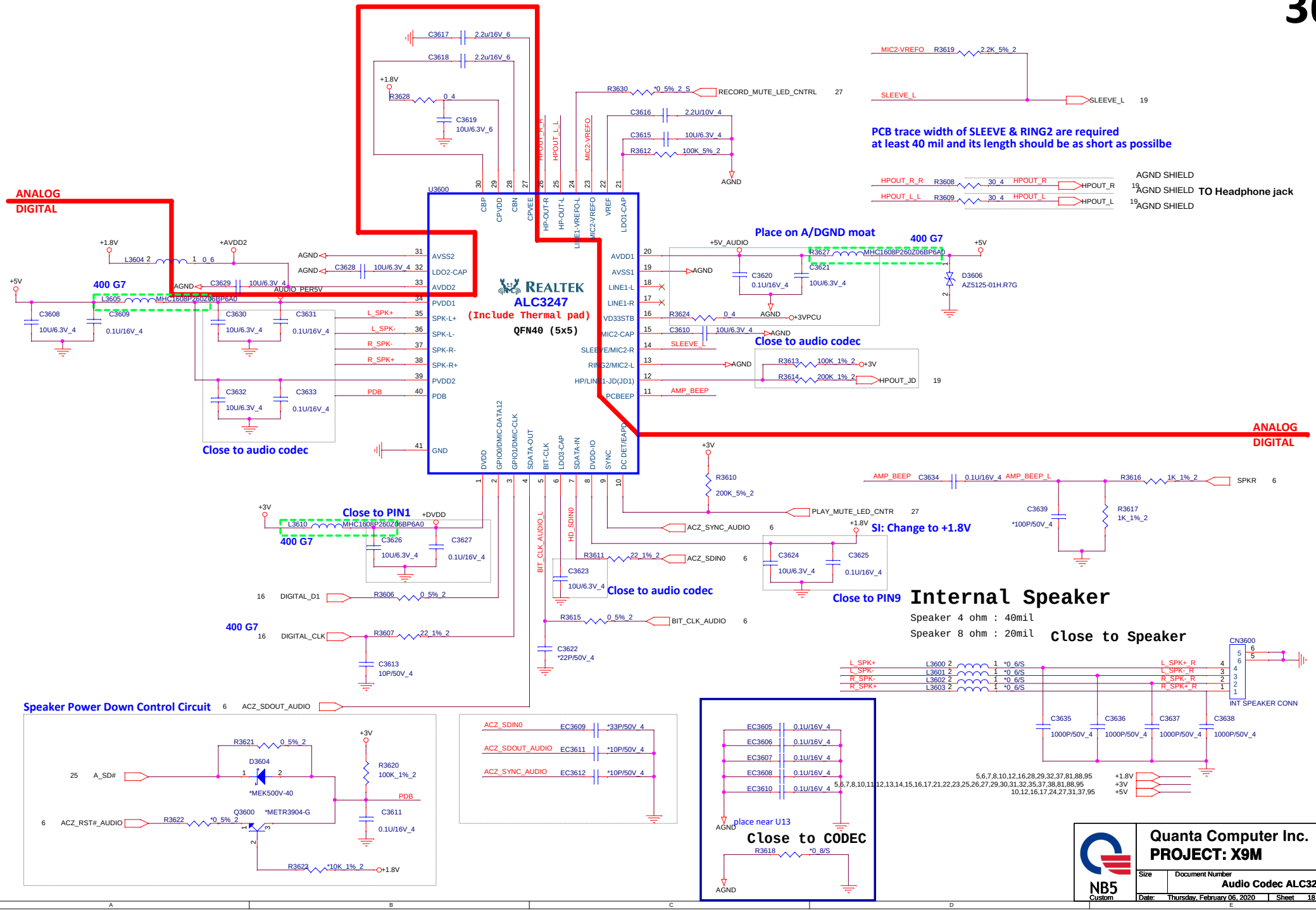
Audio Codec



Quanta Computer Inc.		
PROJECT: X9M		
Size	Document Number	Rev
	Audio Codec ALC3247	1A
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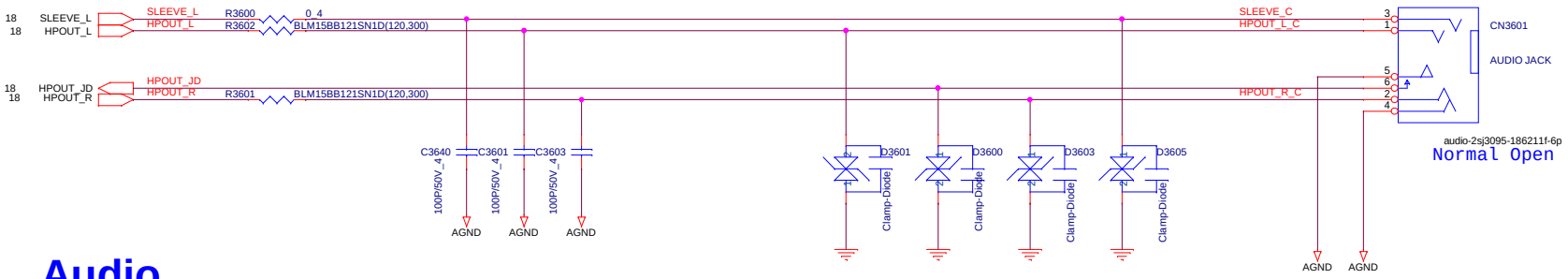
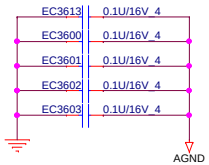
NB5 Custom		



Audio

All Clamp-Diode need close to ADO Jack.



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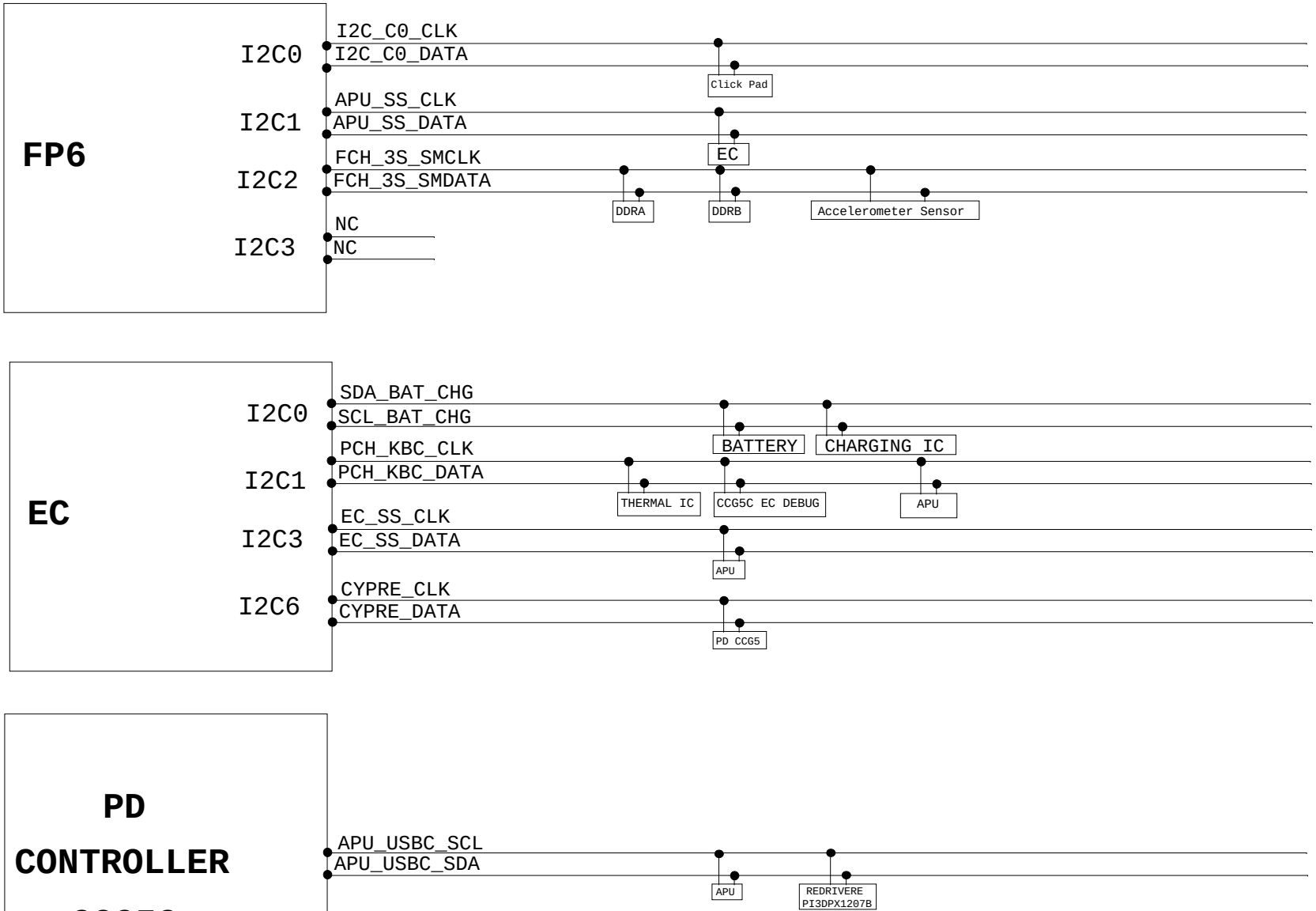

NB5 Custom	Quanta Computer Inc. PROJECT: X9M	
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400 series 0930 whole page

LAN & RJ45

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

C4000 15p/50V_4 — XTAL1 — Y4000 25MHZ/30ppm — R4002 1M_1%_2 — XTAL2 — R4018 680_5%_2 — XTAL2_C — C4001 15p/50V_4 — GND

6 LANLINK# — LANLINK# — Q4000B 2N7002KDW — Q4000A 2N7002KDW — LAN_WLED# — +3V_DEEP_SUS — +3VLANVCC

* Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3, 22, 8 , 30
* Place Cg,Ch close to each VDD10 pin-- 22(reserved)

Power trace Layout 寬度> 60mil

>60mil — >60mil

+1.05V_LAN_REGOUT — L4000 4.7uH_3.2x2.5x2 — La

Trace<30 mil
Width > 60 mil

C4004 *0.1U/16V_4 — Ca C4005 0.1U/16V_4 — Cb — C4006 4.7U/6.3V_4

PIN3 Cc C4007 0.1U/16V_4 — PIN8 Cd C4008 0.1U/16V_4 — PIN30 Ce C4009 0.1U/16V_4 — PIN22 Cf C4010 0.1U/16V_4 — PIN22 Cg C4011 *1U/6.3V_4 — PIN22 Ch C4012 0.1U/16V_4 — +1.05V_LAN_R

For SWR mode
Stuff La, Ca ,Cb
NA : Ra, Ci

U4000 RTL8111HSH-CG

Please add 9 GND VIAs connection with thermal PAD

GND — AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 LED1(GPIO) LED2(LED1)

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- — MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10_2 — REGOUT(NC) VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP

MDIP3(NC) MDIN3(NC) AVDD33(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N

+1.05V_LAN_REGOUT — +3V_LAN — +1.05V_LAN_R — PCIE_WAKE#_R — ISOLATEB — PCIE_RST# — PCIE_RXN4_LAN_L — PCIE_RXP4_LAN_L

C4038 0.1U/16V_4 — PCIE_RST# 6,22,23,38

C4002 0.1U/16V_4 PCIE_RXN4_LAN — C4003 0.1U/16V_4 PCIE_RXP4_LAN

+1.05V_LAN_R — MDI3+ MDI3- — +3V_LAN — PCIE_CLKREQ_LAN# — CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN4_LAN PCIE_TXP4_LAN

+3V — R4001 1K_1%_2 — ISOLATEB — R4004 15K_1%_2

+3VLANVCC — R4003 4.3K_5%_2 — R4005 2K_1%_2 — PCH_WAKE# — Q4001 METR3904-G — R4006 *0_5%_2 — PCH_WAKE# 6,22

PCIE_WAKE#_R

+3V_LAN — LAN_AMBLED# — LAN_WLED# — P4002 P4001 P4000

+3VLANVCC — R4007 330/F_4 — LAN_WLED — C4013 1000P/50V_4

+3VLANVCC — R4008 330/F_4 — C4014 1000P/50V_4 — LAN_AMBLED

LAN_WLED# C4036 *10P/50V_4

LAN_AMBLED# C4037 *10P/50V_4

C4035 *0.1U/16V_4

+3VLANVCC — Close U4000 — C4015 22U/6.3V_6 — C4016 *4.7U/6.3V_4

Shared with +1.05V_PCH SVR	Used internal SVR
No stuff L15	Stuff L15
Stuff R151	No stuff R151

3 PCIE_RXN4_LAN — PCIE_RXN4_LAN
3 PCIE_RXP4_LAN — PCIE_RXP4_LAN
3 PCIE_TXN4_LAN — PCIE_TXN4_LAN
3 PCIE_TXP4_LAN — PCIE_TXP4_LAN

6 CLK_PCIE_LANP — CLK_PCIE_LANP
6 CLK_PCIE_LANN — CLK_PCIE_LANN

U4001 NS892407

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3- — TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4- — MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4- — MDI0+_1 MDI0-_1 MDI1+_1 MDI1-_1 MDI2+_1 MDI2-_1 MDI3+_1 MDI3-_1

TRA_V_DAC TRA_V_DAC TRA_V_DAC TRA_V_DAC — TCT1 TCT2 TCT3 TCT4 — MCT1 MCT2 MCT3 MCT4 — LAN_MCTG3 LAN_MCTG2 LAN_MCTG1 LAN_MCTG0

C4023 0.01U/50V_4

R4014 75/F_4 — R4015 75/F_4 — R4016 75/F_4 — R4017 75/F_4

D4000 *AZ4024-01F.R7GR — C4024 10P/3KV_1808

For GiGABOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

09/19 : SI stage reserve U4002/U4003 close U4001

U4002 *AZ1045-04F

MDI0+ MDI0- MDI1+ MDI1- — IN1 IN2 GND_1 IN3 IN4 — NC_1 NC_2 GND_2 NC_3 NC_4 — MDI0+ MDI0- MDI1+ MDI1-

U4003 *AZ1045-04F

MDI2+ MDI2- MDI3+ MDI3- — IN1 IN2 GND_1 IN3 IN4 — NC_1 NC_2 GND_2 NC_3 NC_4 — MDI2+ MDI2- MDI3+ MDI3-

* Place Cj and Ck, close to each VDD33 pin-- 11, 32
* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

+3V_LAN — +3VLANVCC

PIN11 C4018 0.1U/16V_4 Cj — PIN32 C4017 0.1U/16V_4 Ck — PIN11 C4019 *4.7U/6.3V_4 Cm — PIN32 C4020 *4.7U/6.3V_4 Cn

C4021 4.7U/6.3V_4 PIN23 — C4022 0.1U/16V_4 PIN23

Co — Cp

For SWR mode
Stuff Co, Cp

Remove For Not Using SWR mode

RJ45 CN4000

(Green) LAN_WLED LAN_WLED# — LED_White_N LED_White_P — A1 A2

MDI3-_1 MDI3+_1 MDI1-_1 MDI2-_1 MDI2+_1 MDI1+_1 MDI0-_1 MDI0+_1 — RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+

GND1 GND GND2 GND3

LAN_AMBLED LAN_AMBLED# — LED_AMB_N LED_AMB_P — B1 B2

(Amber)

RJ45_CONN — rj45-2rj3y35-108211f-12p

R4013 *0_6/S — R4012 *0_6/S

09/19 : SI stage reserve D4000 close U4001

5,6,7,8,10,11,12,13,14,15,16,17,18,22,23,25,26,27,29,30,31,32,35,37,38,81,88,95 12,37,95 — +3V +3VLANVCC

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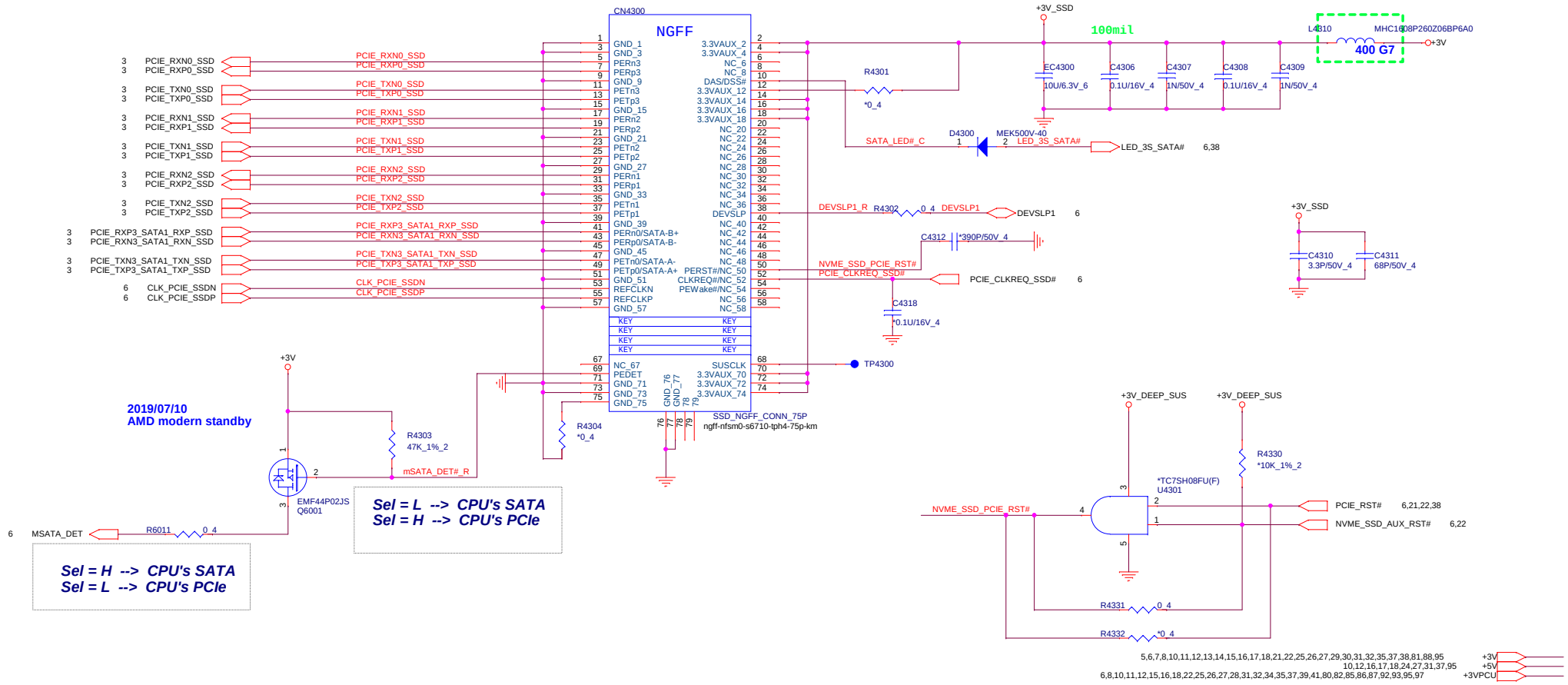
NGFF WLAN/BT

Mini Card
WLAN/BT(Option)
2.5A for WLAN

NGFF Wifi/BT connector

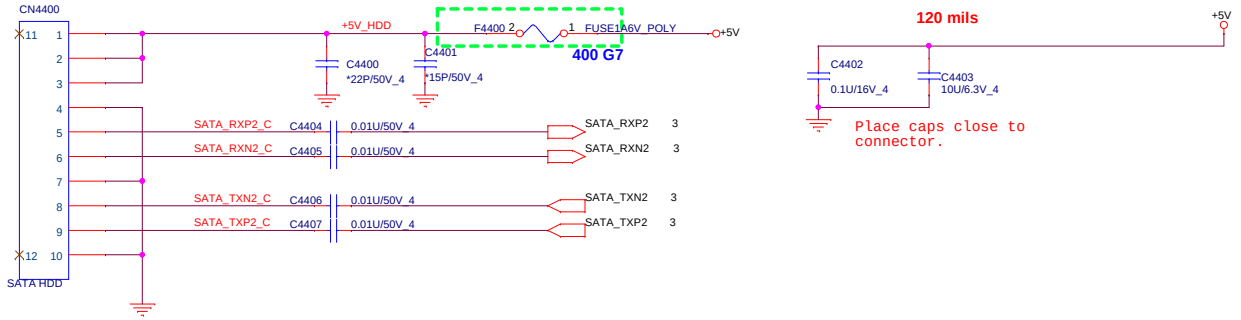
+3VPCU
U4100 AO3415
100mil
R4141 10K_1%_2
C4109 0.22u/10V_4
26 WLAN_OFF_EC
R4145 200K_1%_2
+3V_WLAN_EN
+3V_WLAN_P
C4100 0.1U/16V_4
C4101 0.1U/16V_4
C4102 4.7U/6.3V_4
R4146 200_5%_2
+3V
R4101 100K_1%_4
Q4106 2N7002K
2 WLAN_OFF_EC
6 PCIE_CLKREQ_WLAN#
Q4101 2N7002K
R4103 *0_4
REQ_WLAN#
C4107 *0.1U/16V_4
+3V_WLAN_C
400 G7
L4103 MHC1608P260Z06BP6A0
C4104 4.7u/6.3V_4
C4105 0.1U/16V_4
CN4100
NGFF
Module Key
7 USB_1_P2_DP
7 USB_1_P2_DN
USB_1_P2_DP
USB_1_P2_DN
R4109 0_4
R4110 0_4
USB_1_P2_DP_C
USB_1_P2_DN_C
GND_3 USB_D+ USB_D- GND_4 SDIO CLK(O) SDIO CMDIO) SDIO DAT0(IO) SDIO DAT1(IO) SDIO DAT2(IO) SDIO DAT3(IO) SDIO Wake(I) SDIO Reset
3.3Vaux_1 3.3Vaux_2 LED#1 PCM_CLK PCM_SYNC PCM_IN PCM_OUT LED#2 GND_13 UART Wake UART Rx
WIRELESS_ON
WIRELESS_ON 27
CNVi RBI_RSP, RGI_RSP 22 Ohm, to be placed close to the connector.
CNVi RBI_DT, RGI_DT 33 Ohm, to be placed close to the PCH.
3 PCIE_TXP5_WLAN
3 PCIE_TXN5_WLAN
3 PCIE_RXP5_WLAN
3 PCIE_RXN5_WLAN
6 CLK_PCIE_WLANP
6 CLK_PCIE_WLANN
REQ_WLAN#
WAKE#
GND_5 PETp0 PETn0 GND_6 PERp0 PERn0 GND_7 REFCLKP0 REFCLKN0 GND_8 CLKREQ0# PEWake0# GND_9 PETp1 PETn1 GND_10 PERp1 PERn1 GND_11 Reserved1 Reserved2 GND_12
UART Tx UART CTS UART RTS Clink RESET CLink DATA CLink CLK COEX3 COEX2 COEX1 SUSCLK(32KHz) PERST0# W_DISABLE2# W_DISABLE1# NFC I2C SM DATA NFC I2C SM CLK ALERT# RESERVED UIM_SWP/PERST1# UIM_POWER_SNK UIM_POWER_SRC 3.3Vaux_3 3.3Vaux_4
GND_1 GND_2 NC_1 NC_2
+3V
R4120 10K_1%_2
C4106 *390P/50V_4
WLAN_PLT_RST#
INT_BT_OFF#
INT_RF_OFF#
LAD0 LAD1 LAD2 LAD3
LAD0 6,25,41
LAD1 6,25,41
LAD2 6,25,41
LAD3 6,25,41
+3V_WLAN_C
6,41 CLK_R3S_DEBUG
6,25,41 LPC_3S_FRAME#
6,21 PCH_WAKE#
PCH_WAKE#
R4105 *0_4/S
Q4104 *2N7002K
R4117 *10K_1%_4
+3V_WLAN_P
LOTES_APCI0019-P00*A
ngff-nfse0-s6710-tph4-ke-smt
ngff-nfse0-s6710-tph4-ke-smt
DFHS75FR430
5,6,7,8,10,11,12,13,14,15,16,17,18,21,23,25,26,27,29,30,31,32,35,37,38,81,88,95 +3V
10,12,16,17,18,24,27,31,37,95 +5V
+3V_WLAN_P
400 G7
Q4102A 2N7002KDW
BT_OFF 6
R4104 10K_1%_2
R4148 *0_5%_4
SLP_S3_5R 81,95
R4147 200K_1%_2
+3V_ALW
Q4110 2N7002K
Q4102B 2N7002KDW
SLP_S5#_3R 6,15,25,33,38,87
+3V_WLAN_P
+3V_DEEP_SUS
R4107 100K_1%_2
R4108 100K_1%_2
+3V_DEEP_SUS
R4116 100K_1%_2
Q4103 METR3904-G
R4111 100K_1%_2
Q4105 METR3904-G
R4106 10K_1%_2
WLAN_TRANSMIT_OFF# 6
Add Q4105 to WLAN_TRANSMIT_OFF# 02/08
R4143 *0_4
WLAN_PLT_RST#
R4121 0_4
PCIE_RST# 6,21,23,38
NVME_SSD_AUX_RST# 6,23
D4100 BAT54AW-L

Quanta Computer Inc.		
PROJECT: X9M		
NB5 Custom	Size	Document Number: NGFF WLAN/BT — Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 22 of 68



NB5 Custom	Quanta Computer Inc. PROJECT: X9M		
	Size	Document Number: NGFF M KEY FOR SSD	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 23 of 68	

SATA-HDD



NB5 Custom	Quanta Computer Inc. PROJECT: X9M	
	Size / Document Number: HDD	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 24 of 68

for Battery charge/charge

Del to PM_SLP_A# 12/07

for Thermal IC/ G-Sensor/GPU

U4701A

NPCX797HA1BX

NOTE: Place a 1 uF capacitor as close to the CAP pin as possible.

NOTE: Connect GND and AGND planes via an 0R resistor or a one-point layout connection.

Del PVT_SCN_LED# 12/07

Replace with 2.2R resistors. 02/06

400 G7 Close to EC

11/19 PV STAGE : IM_5S_DAT and IM_5S_CLK pull-up to +3V

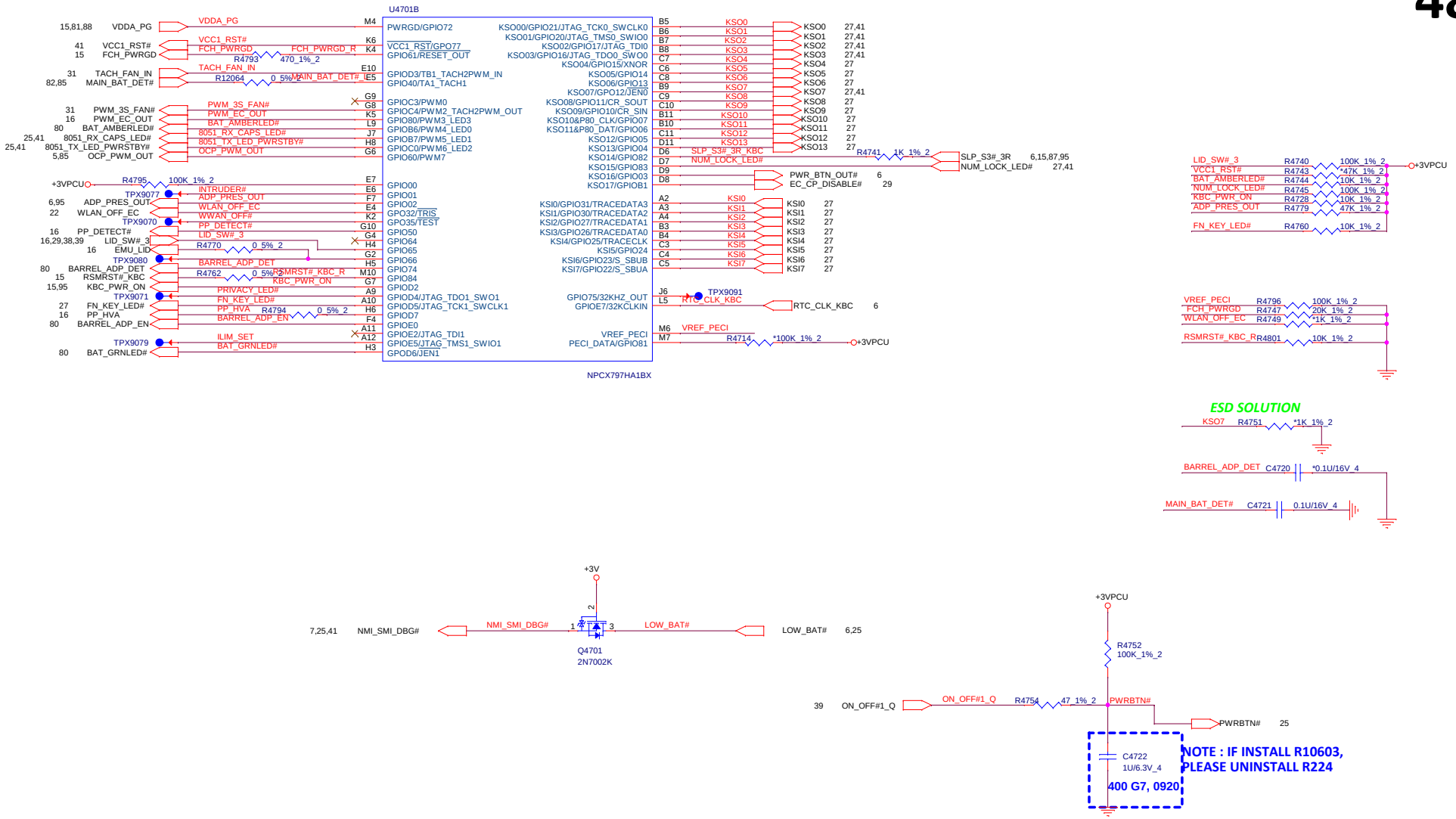
CLOSE TO EC

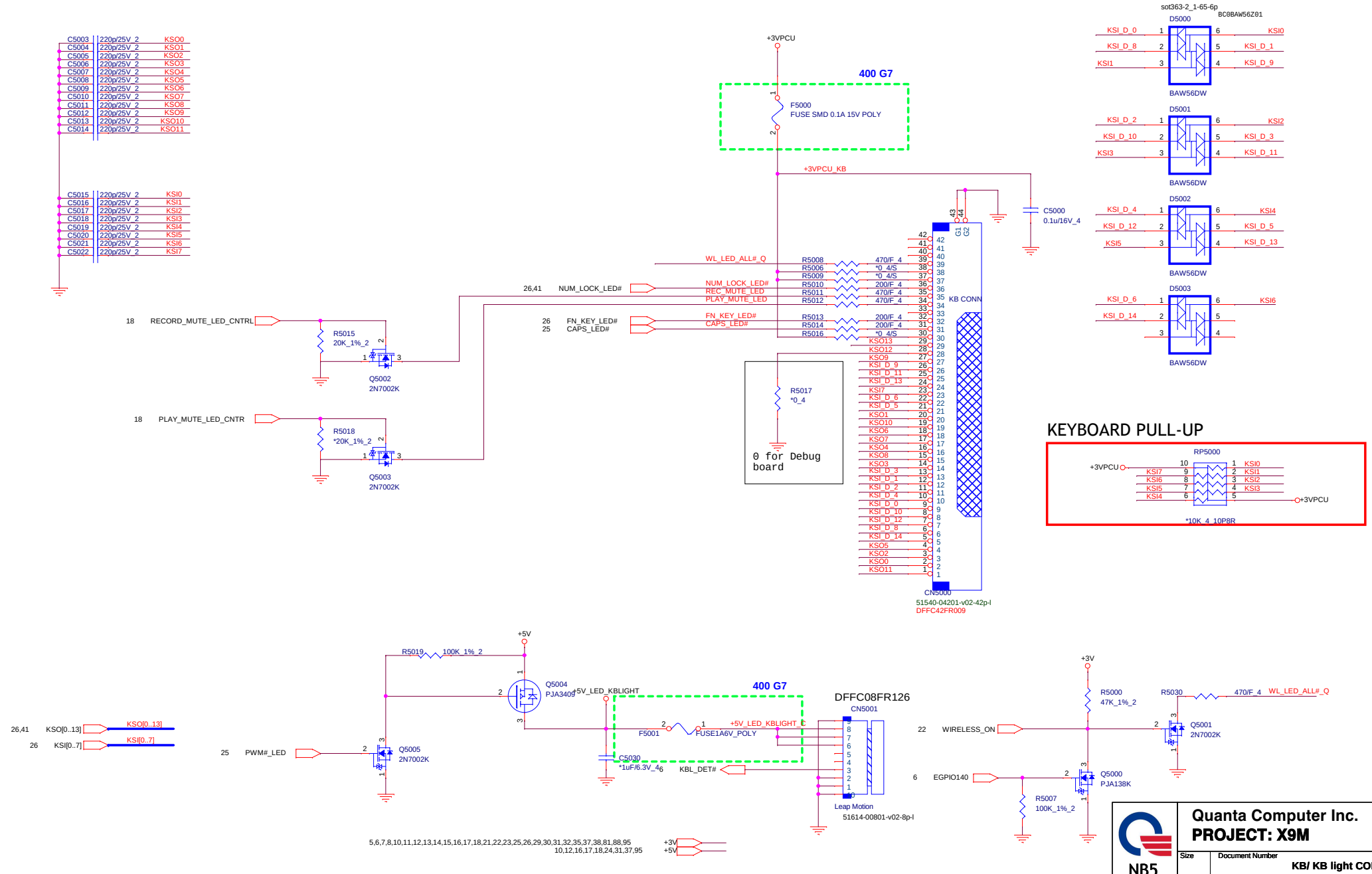
400 G7

SN74LVC2G07DCKR

Quanta Computer Inc.		
PROJECT: X9M		
Size	Document Number	Rev
	EC Nuvoton NPCX797HA0BX_1	1A
Date: Thursday, February 06, 2020	Sheet 25 of 68	

All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power



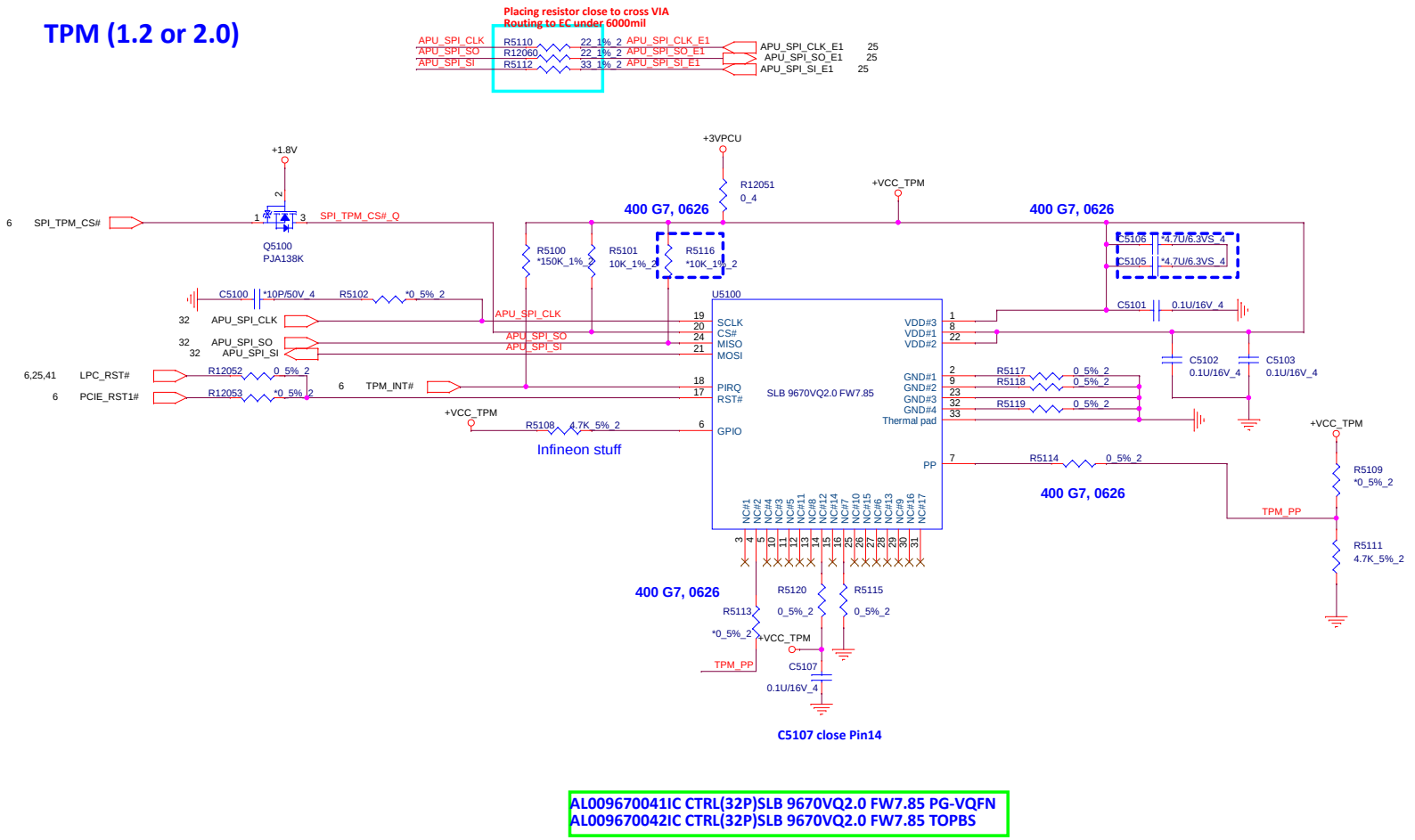


Quanta Computer Inc. PROJECT: X9M			
NB5 Custom	Size	Document Number: KB/ KB light CONN	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 27 of 68	

TPM (1.2 or 2.0)

AL000750004 AL009670042

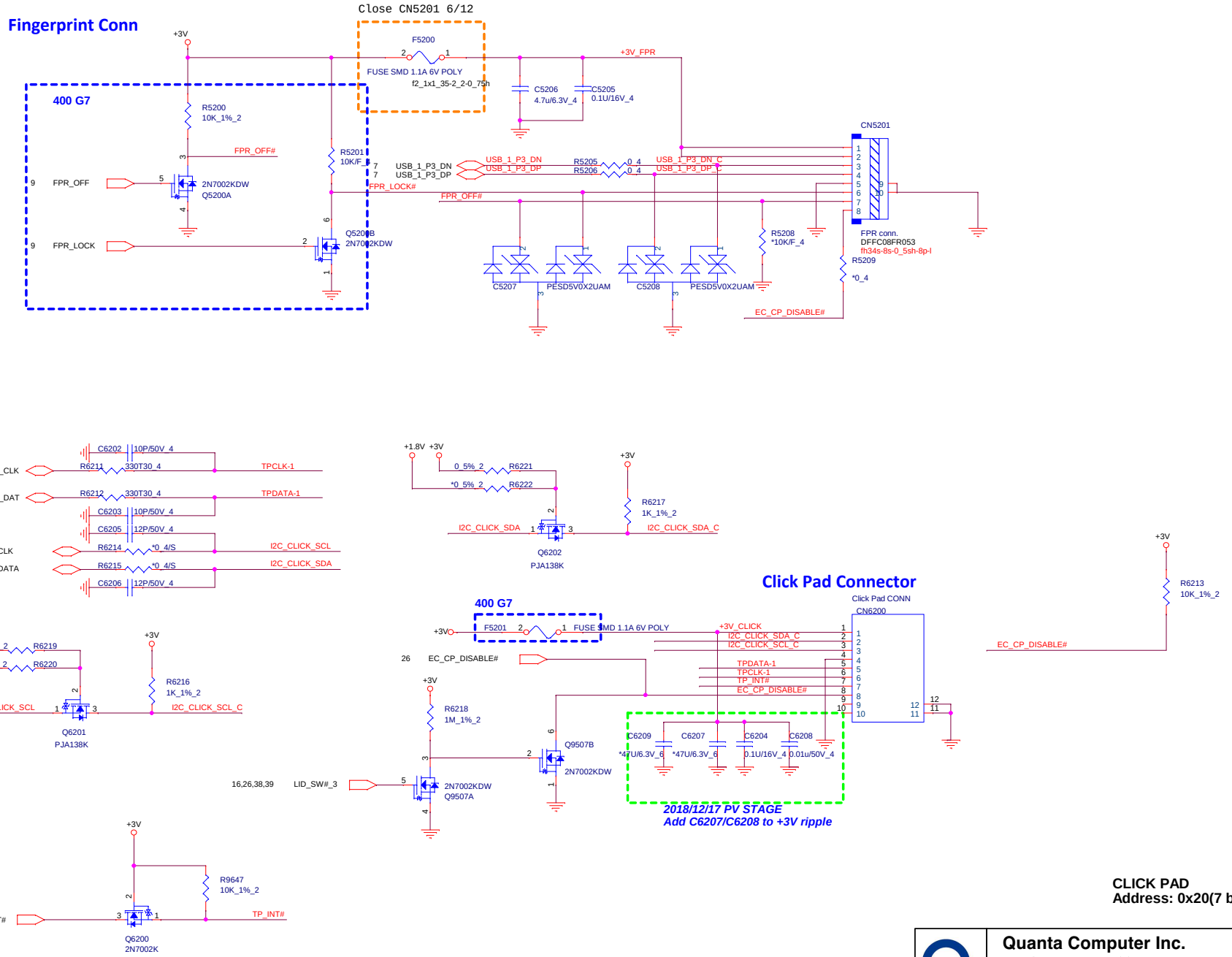
	Nuvoton	Infineon
C5106	V	
C5105	V	
R5116	V	
R5113	V	
R5115	V	V
R5117		V
R5118		V
R5119		V
R5114		V
R5108		V
R5120		V
C5107		V
R5100	150K	10K



AL009670041IC CTRL(32P)SLB 9670VQ2.0 FW7.85 PG-VQFN
AL009670042IC CTRL(32P)SLB 9670VQ2.0 FW7.85 TOPBS

Quanta Computer Inc.
PROJECT: X9M

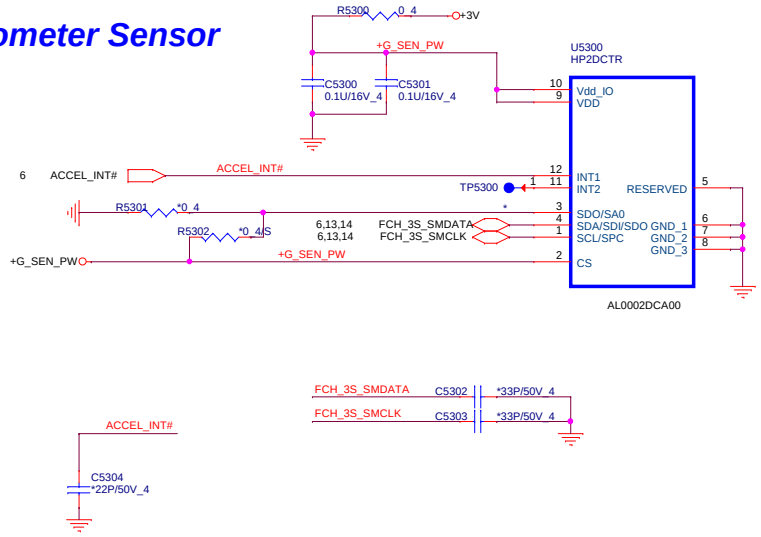
Size	Document Number	Rev
NB5 Custom	TPM SLB9670_QFN	1A
Date: Thursday, February 06, 2020	Sheet 28 of 68	



CLICK PAD
Address: 0x20(7 bit)

NB5 Custom	Quanta Computer Inc. PROJECT: X9M	
	Size / Document Number: FPR / CLICK PAD	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 29 of 68

Accelerometer Sensor



5,6,7,8,10,11,12,13,14,15,16,17,18,21,22,23,25,26,27,29,31,32,35,37,38,81,88,95 +3V

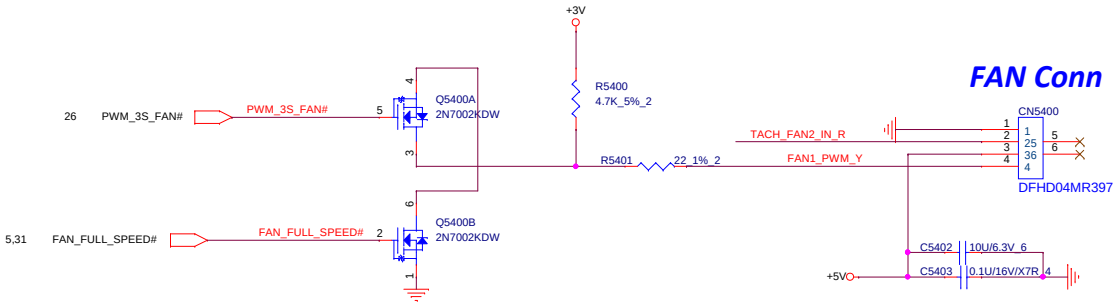
6,8,10,11,12,15,16,18,22,25,26,27,28,31,32,34,35,37,39,41,80,82,85,86,87,92,93,95,97 +3VPCU

NB5
Custom

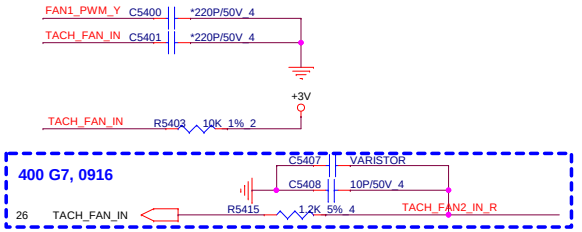
Quanta Computer Inc.
PROJECT: X9M

Size	Document Number	Rev
	Accelerometer	1A
Date: Thursday, February 06, 2020	Sheet 30 of 68	

FAN

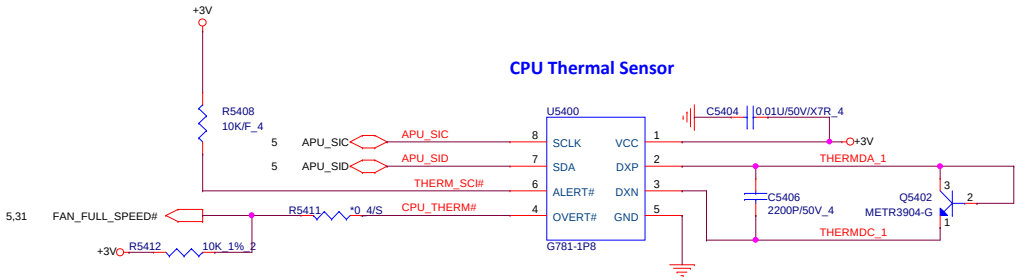


FAN Conn

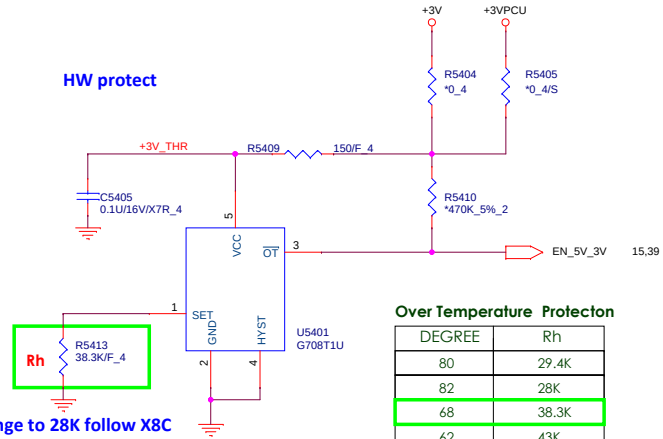


Thermal sensor

CPU Thermal Sensor



HW protect



Over Temperature Protecton

DEGREE	Rh
80	29.4K
82	28K
68	38.3K
62	43K

08/22 : change to 28K follow X8C

11/21 : PV stage, change to 38.3K for thermal request

RSET (K OHM) = 0.0012T^2 - 0.9308T + 96.147

12/12 : PV stage, change to 43K for thermal request

X9M 11/19 : PV stage, change to 38.3K for thermal request

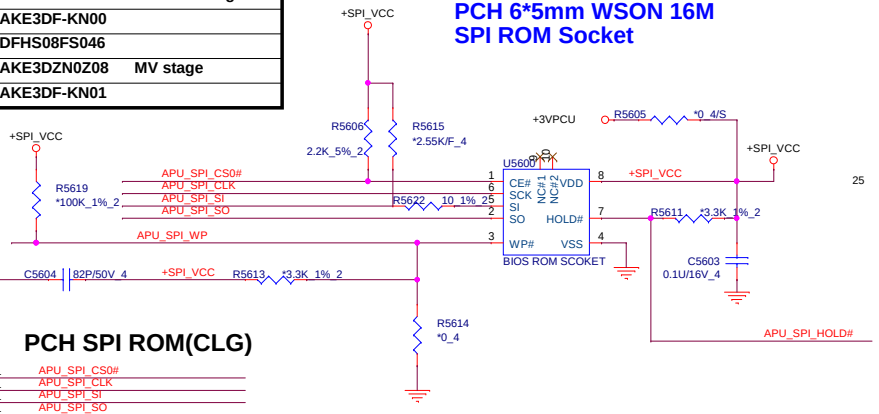
5,6,7,8,10,11,12,13,14,15,16,17,18,21,22,23,25,26,27,29,30,32,35,37,38,81,88,95 +3V
15,22,38,39,85,86,87 +3V_ALW

Quanta Computer Inc. PROJECT: X9M		
NB5 Custom	Size / Document Number: FAN and Thermal IC	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 31 of 68

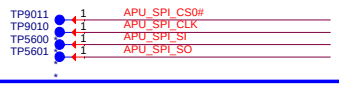
SPI ROM

Vender	Size	P/N	
MXIC	128MB	AKE3DZNKZ00	Pilot run stage
Winbond	128MB	AKE3DF-KN00	
Socket		DFHS08FS046	
MXIC	128MB	AKE3DZN0Z08	MV stage
Winbond	128MB	AKE3DF-KN01	

PCH 6*5mm WSON 16M SPI ROM Socket



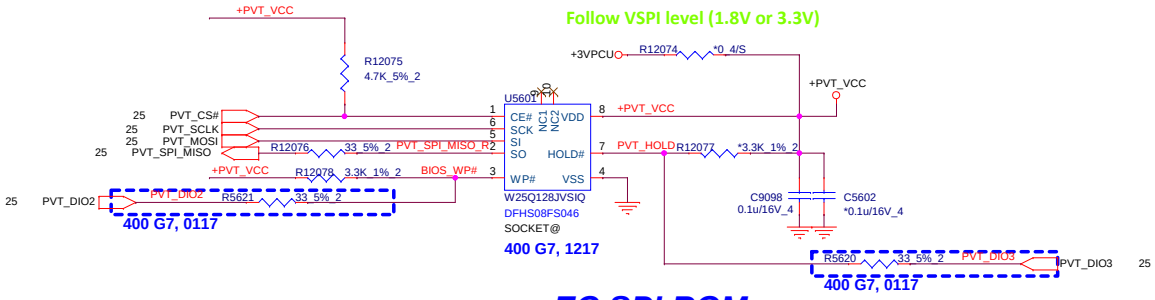
PCH SPI ROM(CLG)



EC SPI ROM 400 G7

EC SPI ROM Socket WSON 16M 6x5

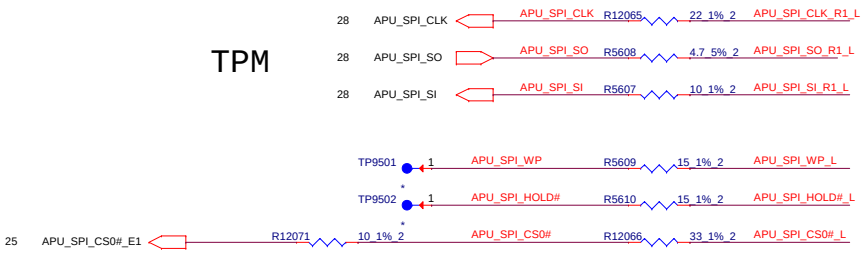
Follow VSPI level (1.8V or 3.3V)



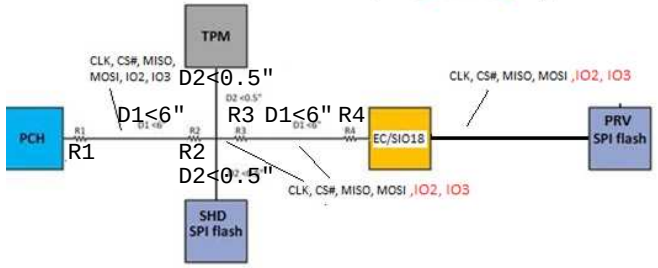
EC SPI ROM

Vender	Size	P/N	
GD	128MB	AKE2DF00Q00	Pilot run stage
GD	128MB	AKE3DZN0Q02	MV stage

TPM



Placing resistor close to cross VIA
Routing to CPU under 6000mil



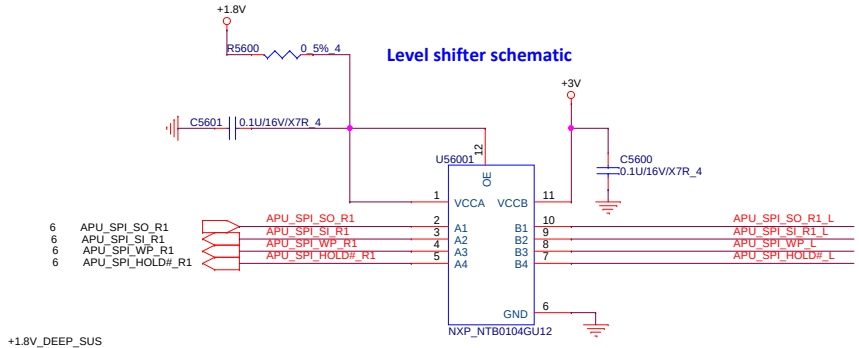
Nuvoton Confidential - Provided under NDA

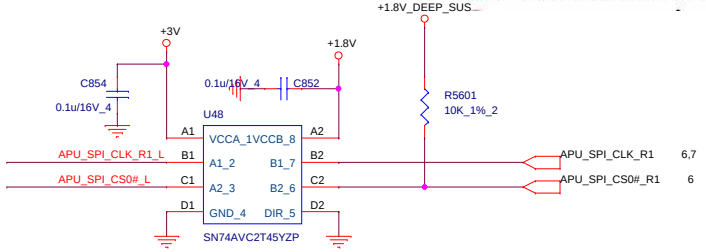
Based on EC18 testing: PCH to TPM/SPI flash = Quad I/O, SIO18 to SPI Flash = ~~Dual I/O~~ Quad I/O,
R1 = 4.7 ohm for CLK, CS#, MISO, MOSI; R1 = 0 ohm for IO2, IO3
R2 = 22 ohm for CLK, CS#, MISO, MOSI; R2 = 15 ohm for IO2, IO3
R3 = 22 ohm for CLK, CS#, MISO, MOSI; R3 = for IO2, IO3 22 ohm
R4 = 4.7 ohm for CLK, CS#, MISO, MOSI; R4 = for IO2, IO3 4.7 ohm

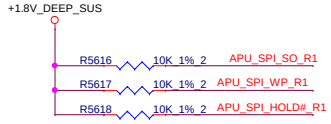
Use same values to start on IO2 and IO3

Note: The value of the resistors should be tuned according to the signal integrity simulations or actual PCB measurements.

Level shifter schematic





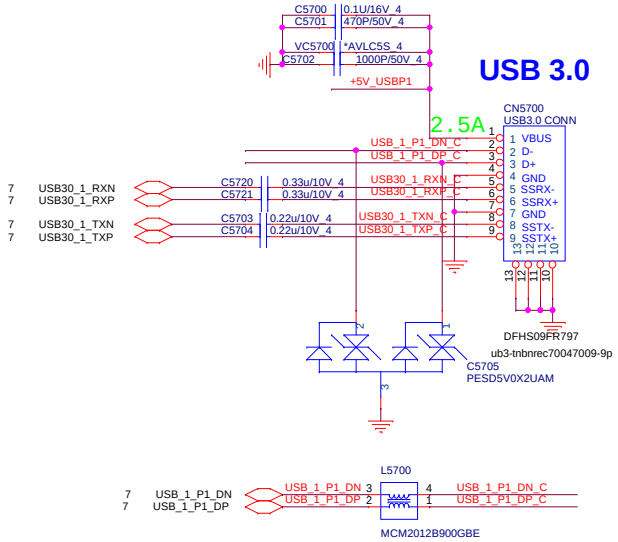


Quanta Computer Inc.
PROJECT: X9M

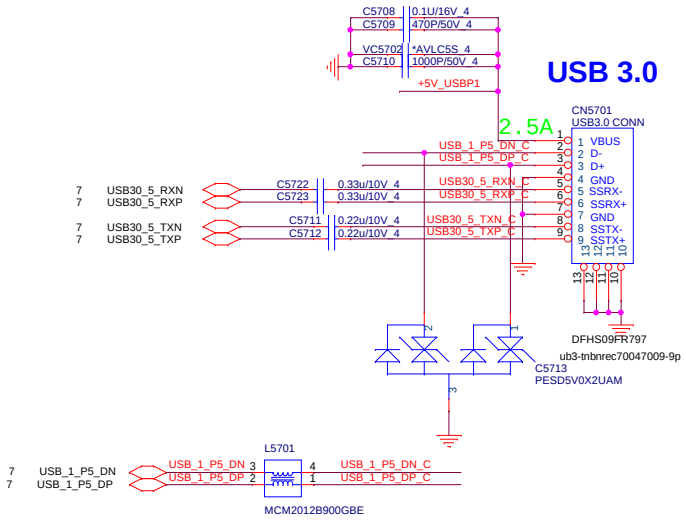
NB5 Custom

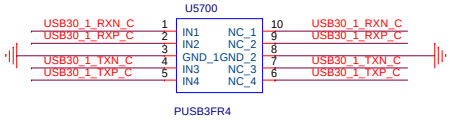
Size	Document Number	Rev
	Flash(KBC+PCH)	1A
Date: Thursday, February 06, 2020	Sheet 32 of 68	

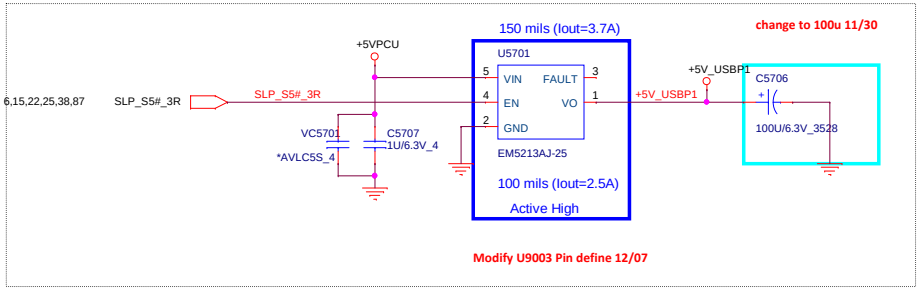
USB 2.0/3.0 Combo 15" Used

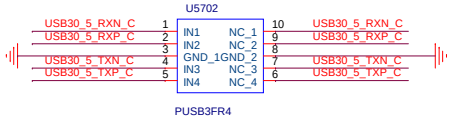


USB 2.0/3.0 Combo

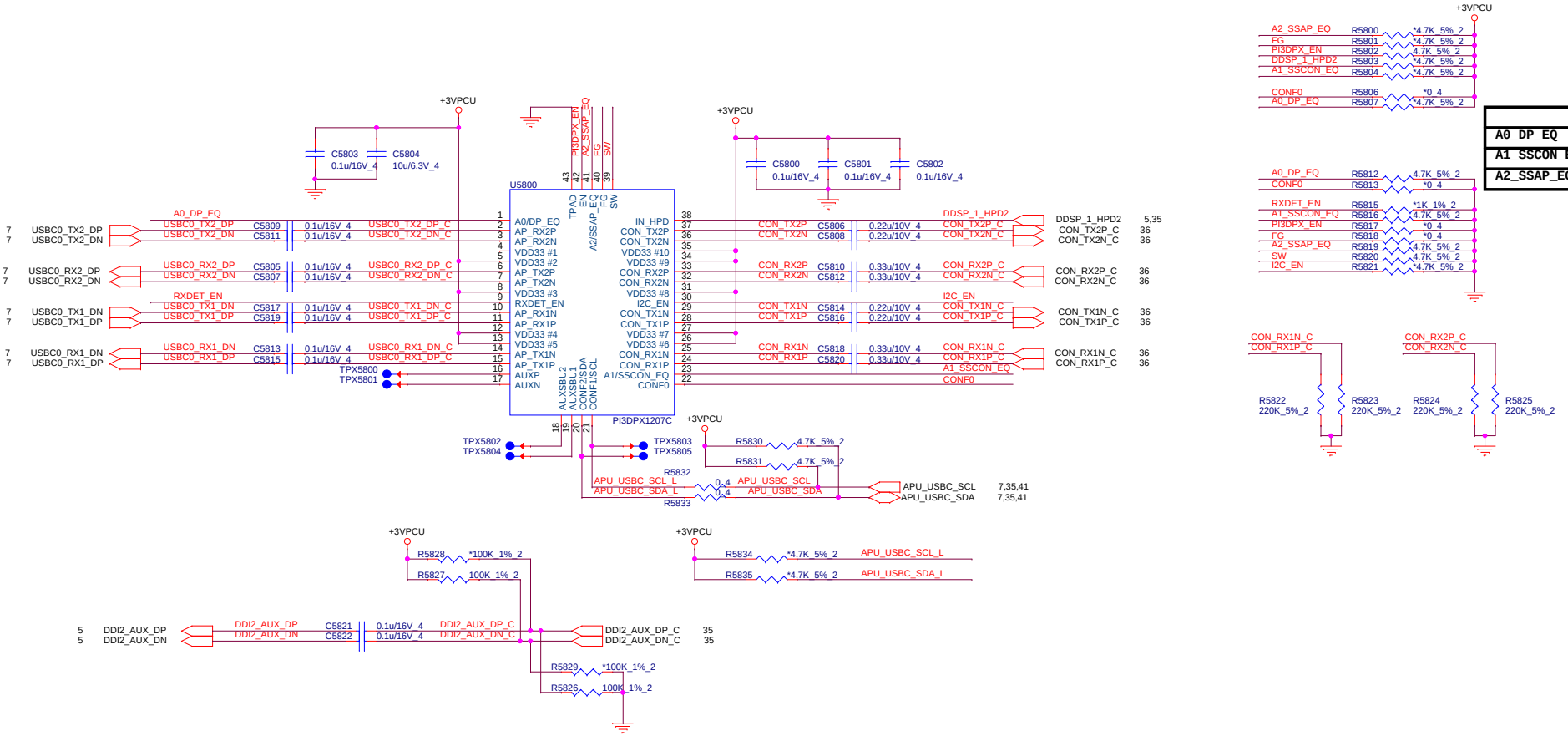








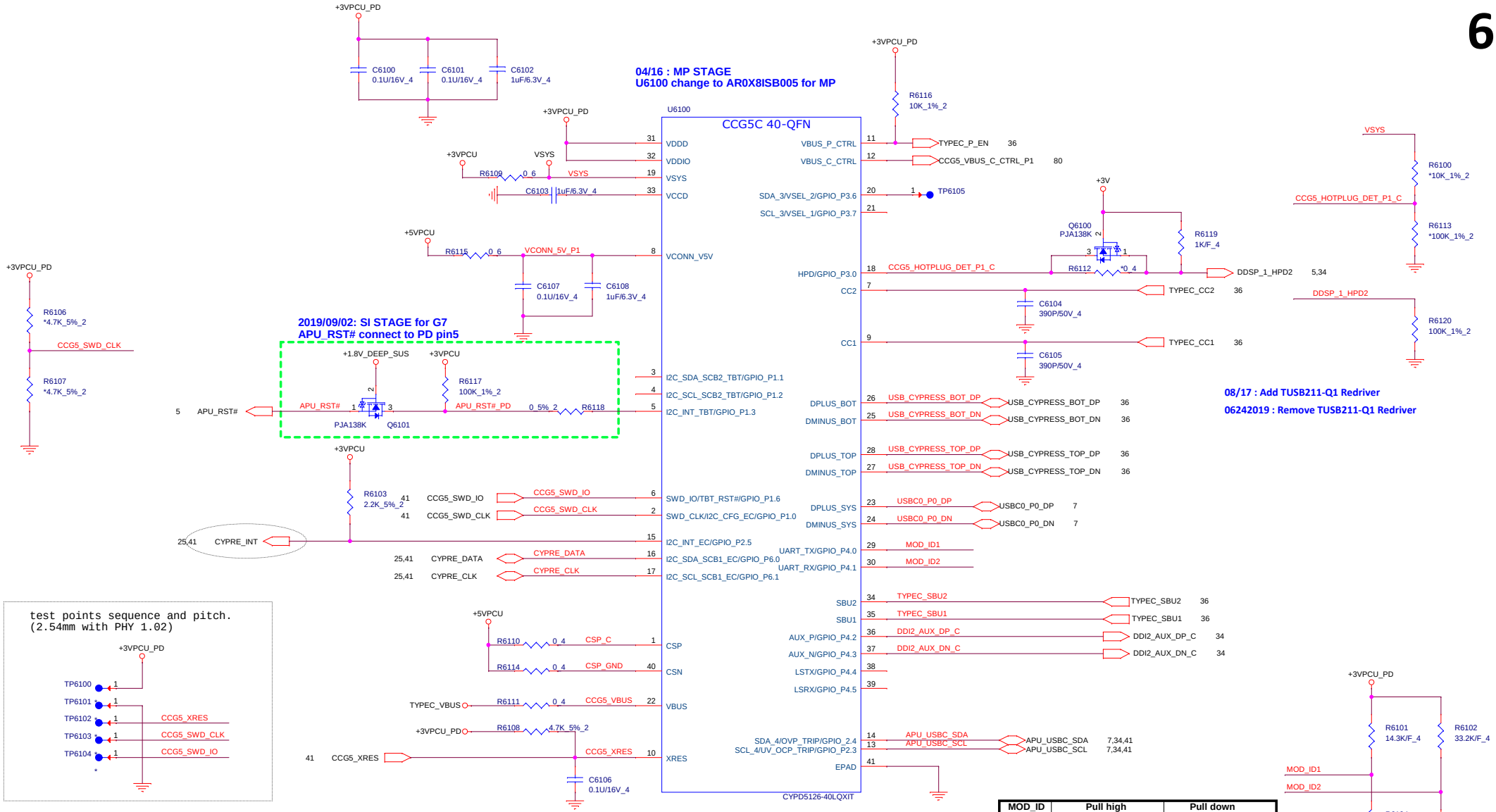
NB5 Custom	Quanta Computer Inc. PROJECT: X9M	
	Size / Document Number: USB3.0 x2	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 33 of 68



	PULL UP	PULL DOWN
A0_DP_EQ	X	4.7K
A1_SSCON_EQ	X	4.7K
A2_SSAP_EQ	X	4.7K

Quanta Computer Inc.
PROJECT: X9M

Size	Document Number	Rev
NB5 Custom	PI3DPX1207B I2C Control	1A
Date: Thursday, February 06, 2020	Sheet 34 of 68	



	Platform ID		CCG5 Dual Port	CCG5/CCG5C Single Port	L0 = 0V
	MOD_ID1	MOD_ID2	Description (Dual port)	Description (Single Port)	L1 = VDDD/8
Notebooks	L8	L7	Reserved	DRP+USB on 1-port with No MUX	L2 = 2* VDDD/8
	L7	L7	DRP+DP+ AR TBT on 2-ports	DRP+DP on 1-port with ANX MUX	L3 = 3* VDDD/8
	L6	L7	DRP+DP on 2-ports	DRP+DP+ TR TBT on 1-port	L4 = 4* VDDD/8
	L5	L7	DRP+DP on 2-ports with ANX MUX	DRP+DP+ AR TBT on 1-port (700, 800 Series)	L5 = 5* VDDD/8
	L4	L7	Malta	DRP+DP on 1-port with Parade MUX	L6 = 6* VDDD/8
	L3	L7	DRP+DP+ TR TBT on 2-ports	DRP+DP on 1-port (600/700 Series) - AMD SKU1	L7 = 7* VDDD/8
	L2	L7	Reserved	DRP+DP on 1-port (600/700 Series) - AMD SKU2	L8 = VDDD
	L1	L7	Reserved	DRP+DP on 1-port (600/700 Series) - AMD SKU3	
	L0	L7	Reserved	DRP+DP on 1-port with Parade MUX - 2019 S400 G6	
	L7	L6	Reserved	DRP+DP on 1-port (400 Series) - AMD	

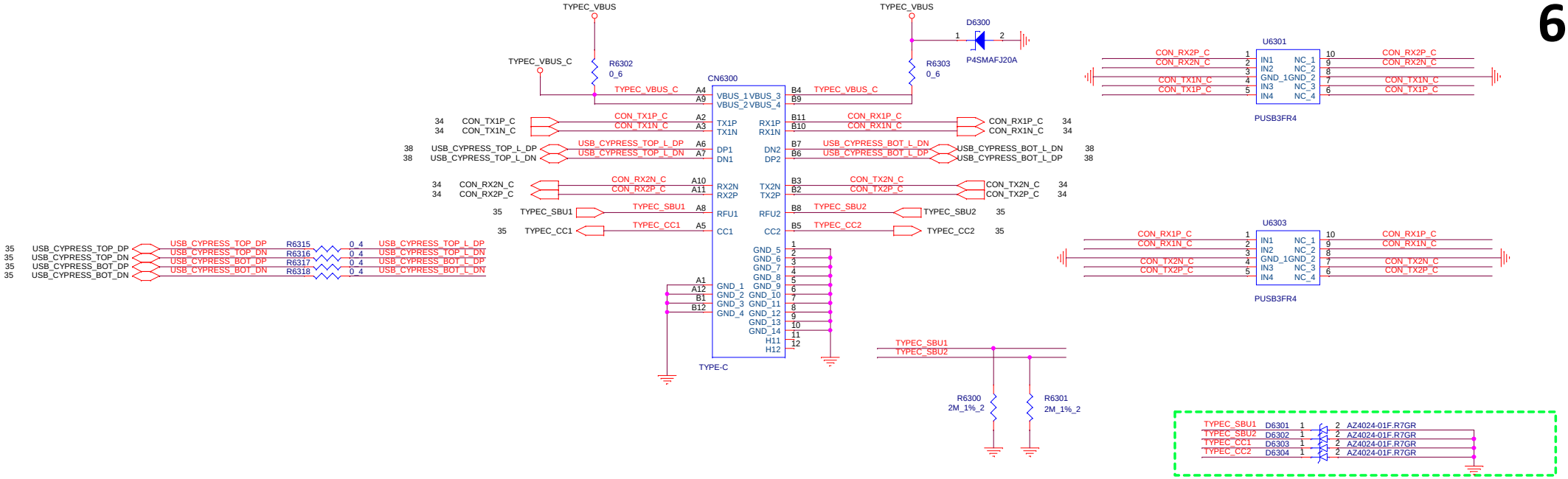
MOD_ID	Pull high	Pull down
L0	None	1K
L1	7.1K	1K
L2	5.9K	2.2K
L5	3.09K	5.1K
L6	33.2K	100K
L7	14.3K	100K

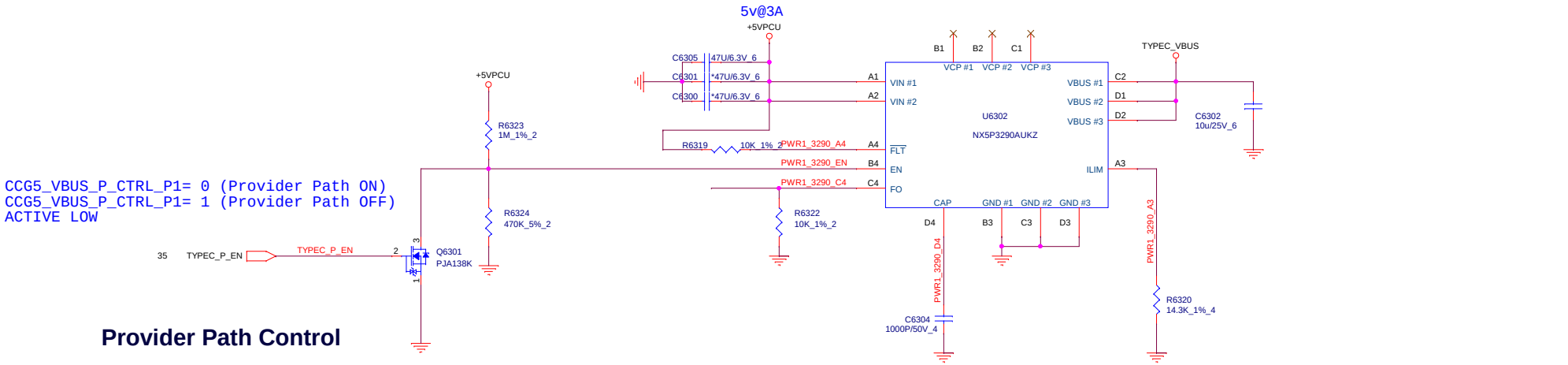
10/18 : SI STAGE
R6101 change to 14.3K CS31432FB08
R6102 change to 33.2K CS33322FB13
R6104/R6105 change to 100K CS41002FB28

NB5 Custom

Quanta Computer Inc.
PROJECT: X9M

Size	Document Number	Rev
	Cypress CCG5C	1A
Date: Thursday, February 06, 2020	Sheet 35 of 68	



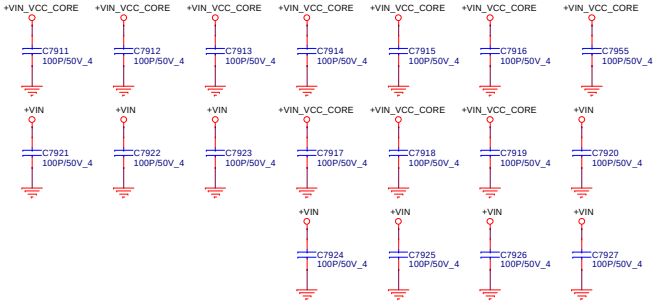


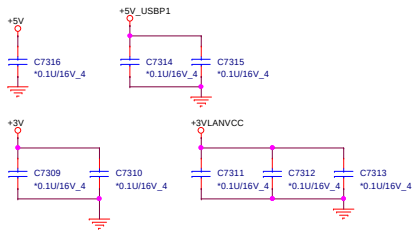

```
CCG5_VBUS_P_CTRL_P1= 0 (Provider Path ON)
CCG5_VBUS_P_CTRL_P1= 1 (Provider Path OFF)
ACTIVE LOW
```

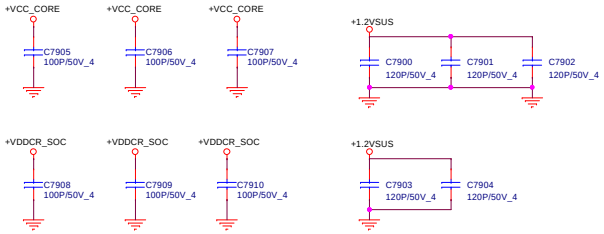
Provider Path Control

Quanta Computer Inc.		
PROJECT: X9M		
NB5 Custom	Size:	Document Number: USB TYPE — Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 36 of 68

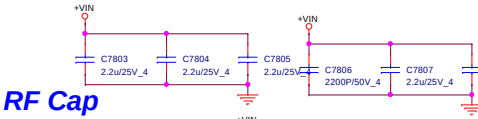
2018/10/12 ADD RF for SI

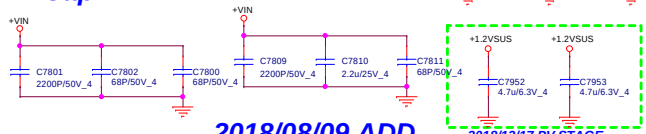




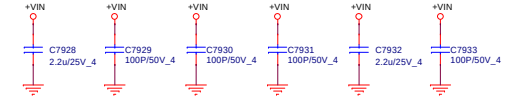


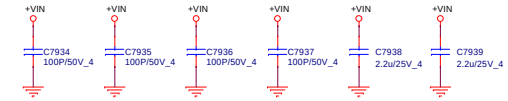
RF Cap

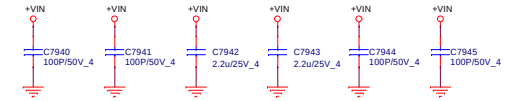


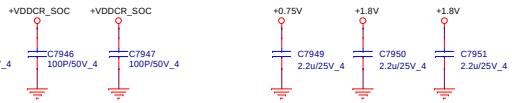


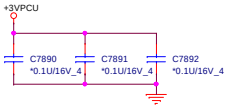
2018/12/17 PV STAGE
change C7957/C7958 to 4.7u for RF



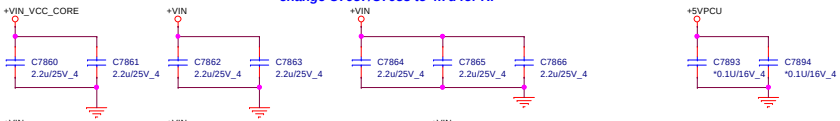


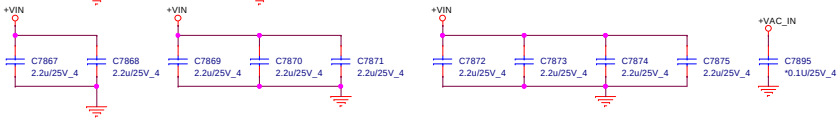


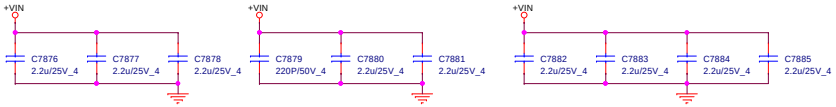




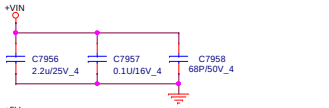
2018/08/09 ADD

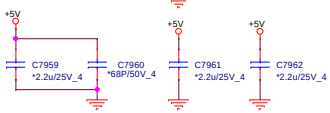


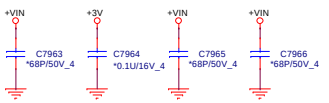


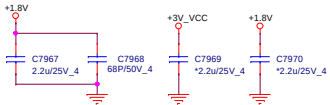


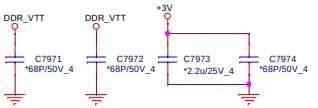
2019/07/12 ADD RF for X9M DB

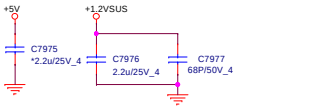


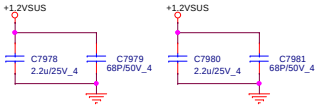


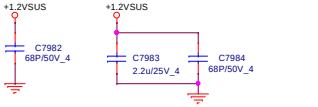




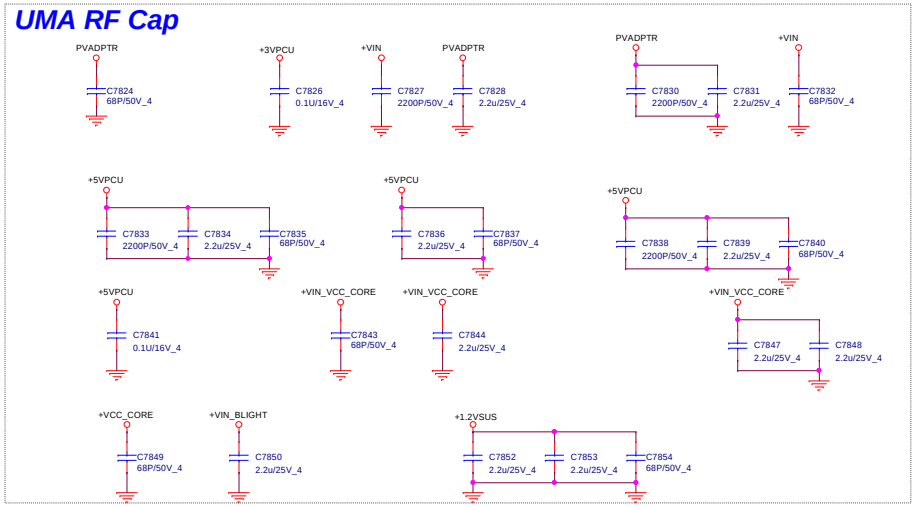








UMA RF Cap



Quanta Computer Inc.
PROJECT: X9M

Size	Document Number	Rev
NB5 Custom	EMI/RF CAP (15AMD)	1A
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TYPEC_VBUS_C

C7300
10u/25V_8

2A / 80mils

F7300
+VIN_VCC_CORE → +VIN_BLIGHT
FUSE SMD 1.5A 24V POLY

U7300
PUSB3FR4

USB_CYPRESS_BOT_L_DN	1	IN1	NC_1	10	USB_CYPRESS_BOT_L_DN
USB_CYPRESS_BOT_L_DP	2	IN2	NC_2	9	USB_CYPRESS_BOT_L_DP
	3	GND_1	GND_2	8	
USB_CYPRESS_TOP_L_DN	4	IN3	NC_3	7	USB_CYPRESS_TOP_L_DN
USB_CYPRESS_TOP_L_DP	5	IN4	NC_4	6	USB_CYPRESS_TOP_L_DP

USB_CYPRESS_BOT_L_DN → 36
USB_CYPRESS_BOT_L_DP → 36
USB_CYPRESS_TOP_L_DN → 36
USB_CYPRESS_TOP_L_DP → 36

USB LID Daugther Board Connector

38 LED#
39 ON_OFF#
16,26,29,39 LID_SW#_3
6,15,22,25,33,87 SLP_S5#_3R

LED#
ON_OFF#
LID_SW#_3
SLP_S5#_3R

14"15" Used

+3V_ALW

C7301 0.1U/16V_4

400 G7

F7600 FUSE SMD 0.1A 15V POLY

+3V_ALW_C

CN7300
HDT CONN
fpc-cf5020fd0rt-05-nh-20p-l

LED#
ON_OFF#
LID_SW#_3
SLP_S5#_3R
LID_SW#_R

R7300 100/F_4

L7300
MCM2012B900GBE

USB_1_P6_DP
USB_1_P6_DN
USB_1_P6_DP_C
USB_1_P6_DN_C

7 USB_1_P6_DN
7 USB_1_P6_DP

C7322
PESD5V0X2UAM

2018/12/17 PV STAGE
Add C7322 for ESD

400 G7
Follow INTEL

+5VPCU
R7601 0_8
+5VPCU_USB

C7305 0.1U/16V_4
C7304 1000P/50V_4
C7302 220P/50V_4
C7303 220P/50V_4

Card Reader Daugther Board Connector

+3V
R7308 10K_1%_2

CN7301
SMD FPC 22P
fpc-51519-02201-v01-22p-l

6 HDD_HALTLED
6,23 LED_3S_SATA#
HDD_HALTLED
LED_3S_SATA#

6 CLK_PCIE_CARDN
6 CLK_PCIE_CARDP
3 PCIE_TXP6_CARD
3 PCIE_TXN6_CARD
3 PCIE_RXN6_CARD
3 PCIE_RXP6_CARD

6,21,22,23 PCIE_RST#
6 PCIE_CLKREQ_CARD#
PCIE_RST#
CR_PWREN#_R

R7305 *0_4/S
+BAT

2018/12/13 PV STAGE
R7305 change to short_pad to sovle ESD issue

+3V
F7601 FUSE SMD 1.1A 6V POLY
+3V_HDDLED

400 G7
f2_1x1_35-2_2-0_75h

C7307 0.1U/16V_4
C7308 0.1U/16V_4

2018/12/13 PV STAGE
Add C7897/C7898 prevent ESD

HDD_HALTLED
LED_3S_SATA#
C7897 100P/50V_4
C7898 100P/50V_4

PCIE_RST#
C7323 100P/50V_4

+5VPCU
R7301 1M_1%_2
R7302 2M_5%_2
C7306 *0.1u/16V_4

LED# → LED# 38

Q7300B 2N7002KDW
Q7300A 2N7002KDW

25 LED_PWRSTBY#
LED_PWRSTBY#

R7303 *0_4

H7944 *O-X9M-2P2
H7945 *H-415WD-1
H7946 *h-c217d98p2
H7940 *h-o374x276id189x91p2
H7941 *H-C276D98P2

CPU

H7935 *H-TIC150BC197D150PB
H7936 *H-TIC150BC197D150PB
H7937 *H-TIC150BC197D150PB
H7938 *H-TIC150BC197D150PB

H7947 *SPAD-C335NP
H7948 *SPAD-C315NP
H7939 *SPAD-C197NP
H7942 *H-C276I91D91P2
H7943 *O-X9M-1P2
H7950 *S2D-BARCODE-8X8-S
H7951 *2D-BARCODE-8X8-S
H7928 *H-BIO177X138D122X83PB
H7949 *SPAD-RE713X213NP
H7919 *H-C276D91P2

H7900 *H-TC83BIC138D83PB
H7901 H-C315D252P2
H7910 *o-x9m-4p2
H7911 *H-O122X83D122X83N
H7912 *H-X9KA-1
H7934 *H-X9KA-2
H7929 *H-TIC276BC315D91P2

WLAN nut

H7923
h-tc197bic122d122pt

SSD nut

H7909
h-tc197bic122d122pt

Quanta Computer Inc.
PROJECT: X9M

Size	Document Number	Rev
	EMI/RF CAP (15AMD)	1A
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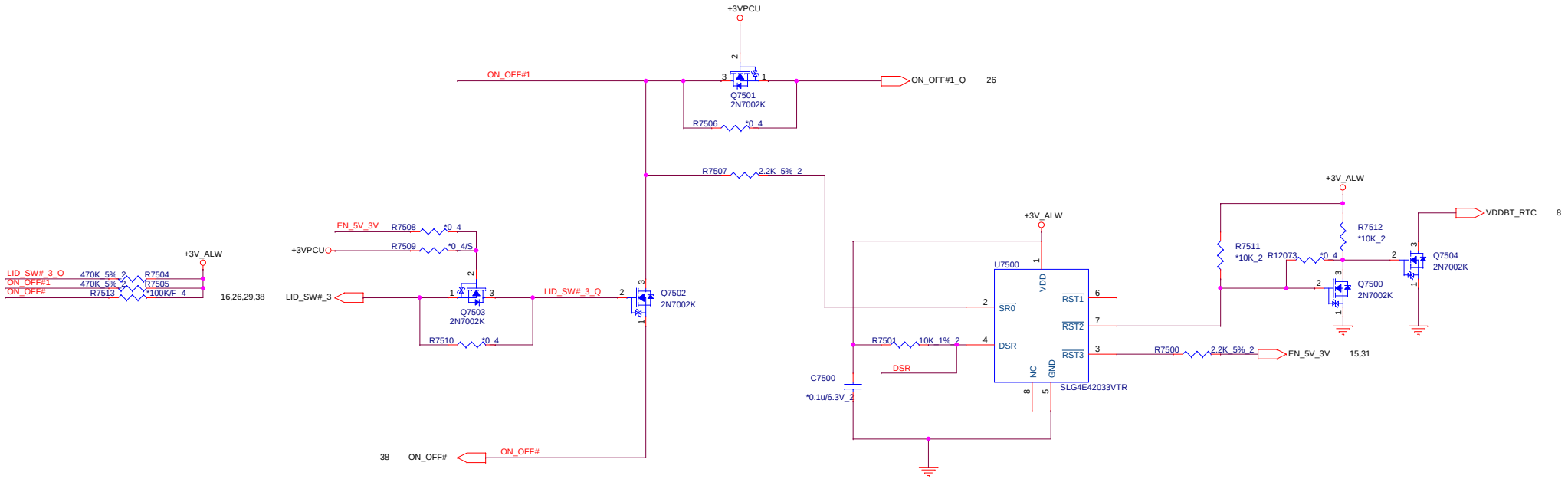
NB5
Custom

Power Botton Connector



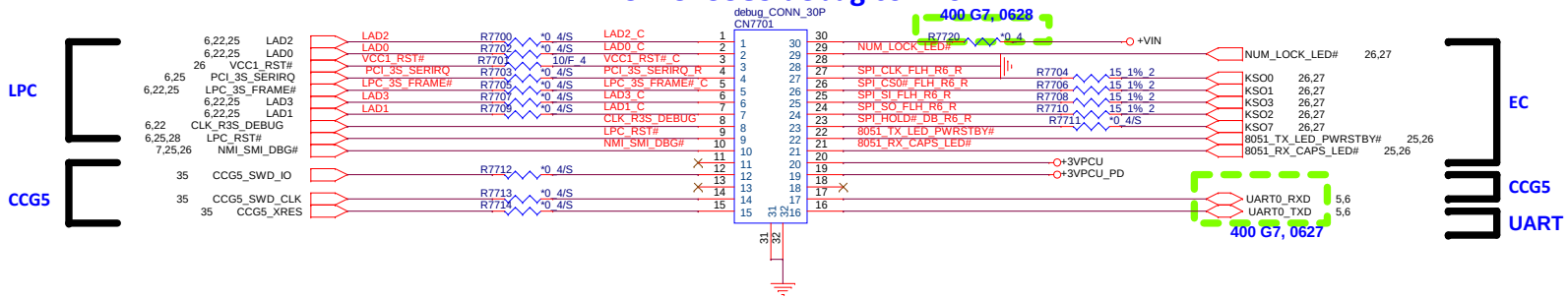
12S RESET MODE INSTAL FOR DB0	
INSTAL	R10702 R10703 R10704 R581 R10701 R595 U9068
UNINSTAL	R10754 R10755 Q7080 Q7081

5,6,7,8,10,11,12,13,14,15,16,17,18,21,22,23,25,26,27,29,30,31,32,35,37,38,81,88,95 +3V
10,12,16,17,18,24,27,31,37,95 +5V
15,22,38,85,86,87 +3V_ALW

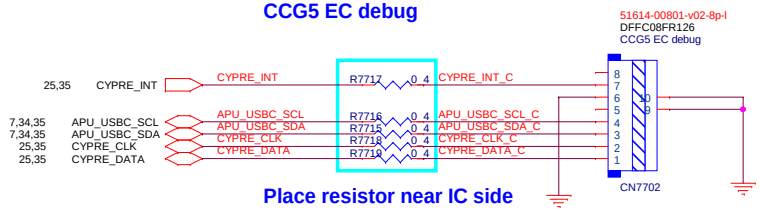
NB5 Custom	Quanta Computer Inc. PROJECT: X9M	
Size	Document Number Power Button/ HW Reset	Rev 1A
Date: Thursday, February 06, 2020	Sheet 39 of 68	

NA

LPC+EC+CCG5 debug conn on MB



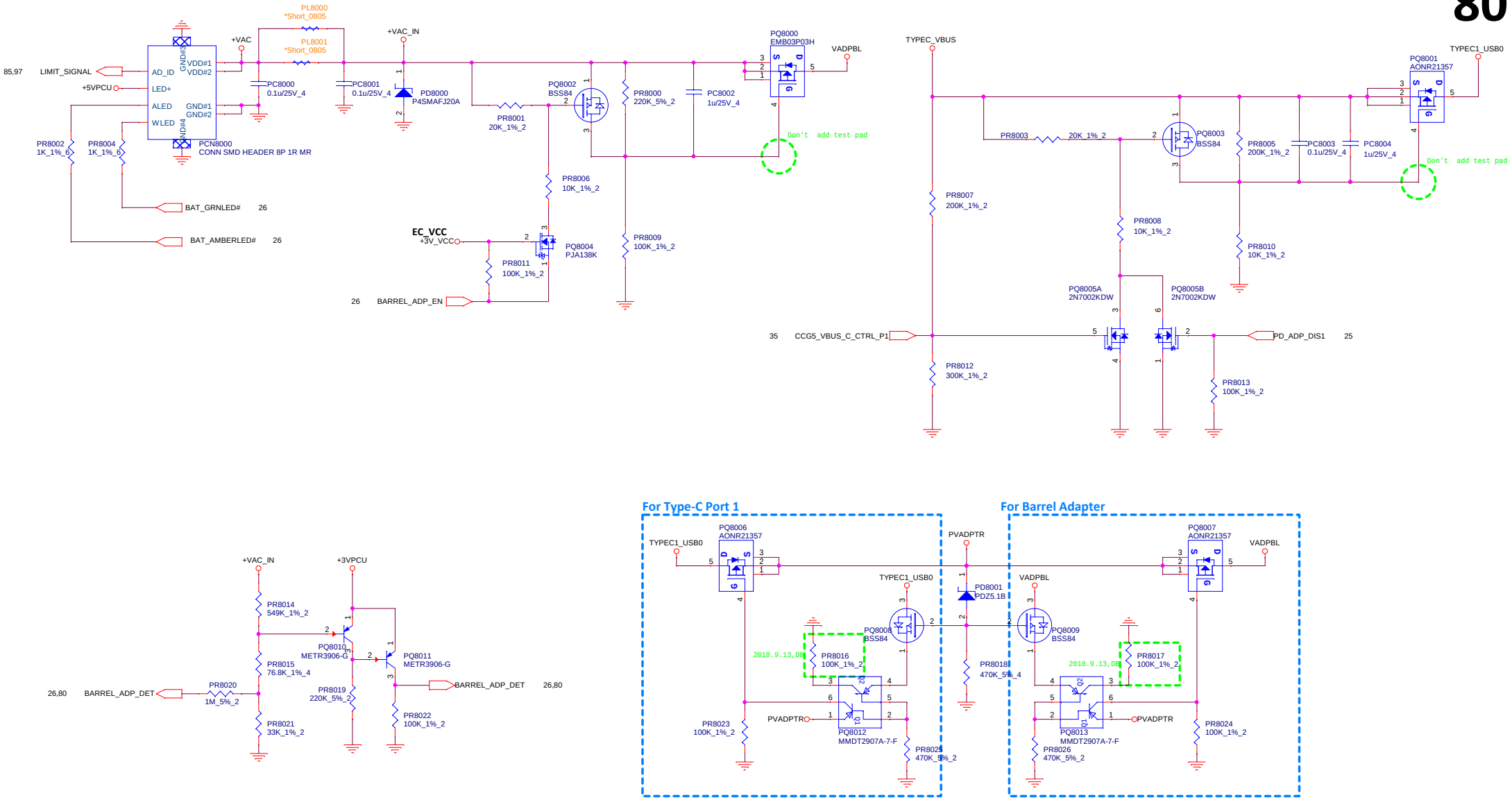
CCG5 EC debug



Place resistor near IC side

CCG5 EC debug

Quanta Computer Inc.			
PROJECT: X9M			
NB5 Custom	Size	Document Number: eSPI/UART debug conn/XDP	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 41 of 68	



Quanta Computer Inc.
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Size	Document Number	Rev
NB5 Custom	Typec-C/ Barrel switch	1A
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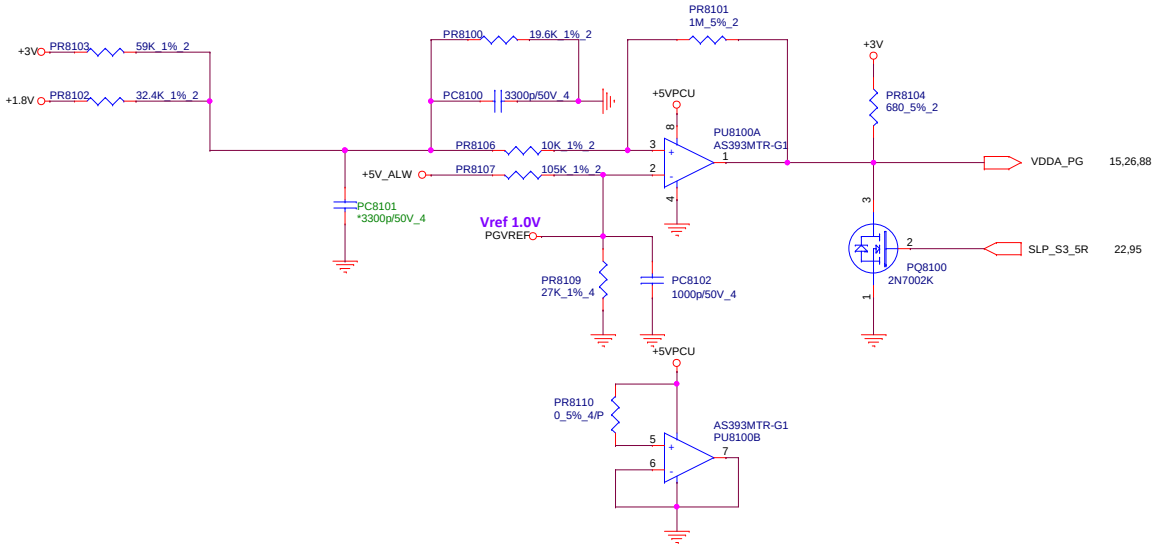

5,6,7,8,10,11,12,13,14,15,16,17,18,21,22,23,25,26,27,29,30,31,32,35,37,38,88,95 +3V
10,12,16,17,18,24,27,31,37,95 +5V

Quanta Computer Inc.		
PROJECT: X9M		
Size: NB5 Custom	Document Number: PWROK	Rev: 1A
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Charger (BQ24780S)

Place sense resistor close to to ADP connector side

Place this TVS as close as possible to the furthest +VIN shape

When ACDET pin is above 0.6 V and VCC is above UVLO, REGN LDO is present, ACOK comparator, input current buffer (IADP), discharge current buffer (IDCHG), independent comparator, and power monitor buffer (PMON) can be enabled with SMBus. When ACDET is above 2.4V, and VCC is above SRN but below ACOV, ACOK goes HIGH.

DCR= 20 mohm (max.)

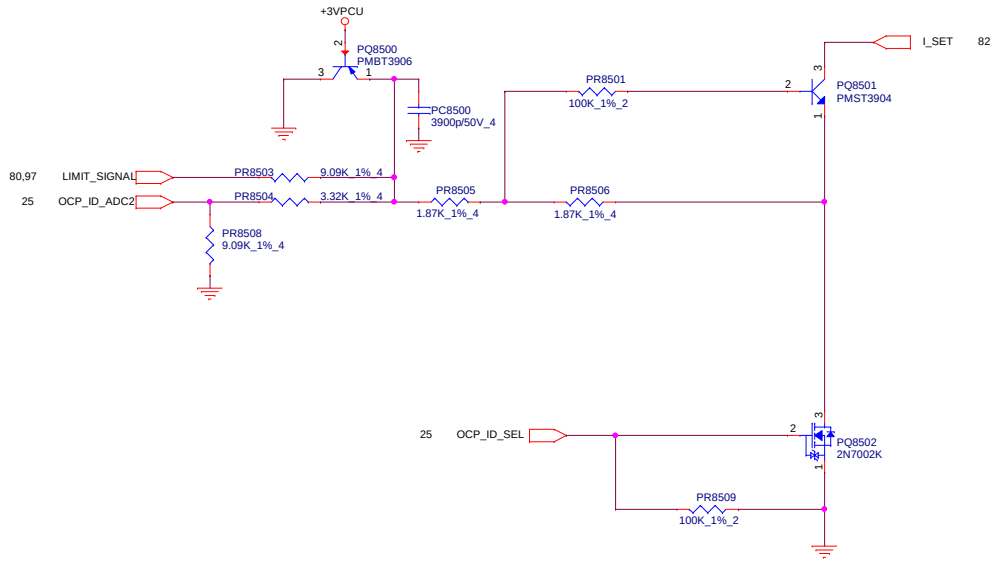
symmetrically on the top- and bottom-sides

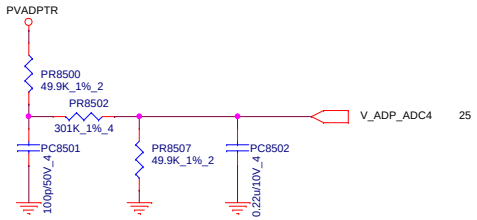
Don't add test pad

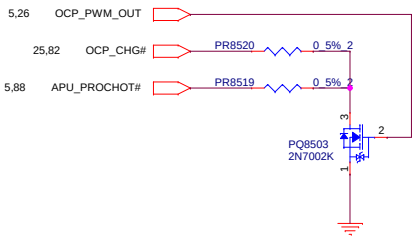
Thermal Sensor for Fast Charging

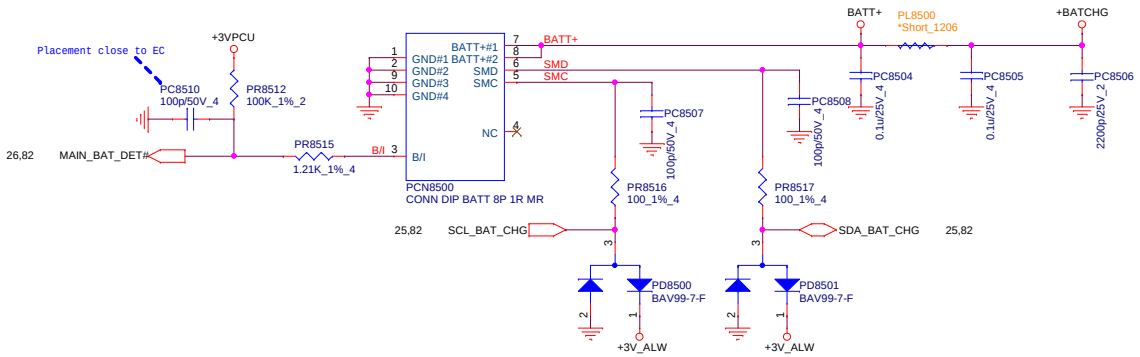
***Place close to charger inductor

Barrel Adapter OCP









Quanta Computer Inc.			
PROJECT: X9M			
Size	Document Number		Rev
NB5 Custom	CHarge III		1A
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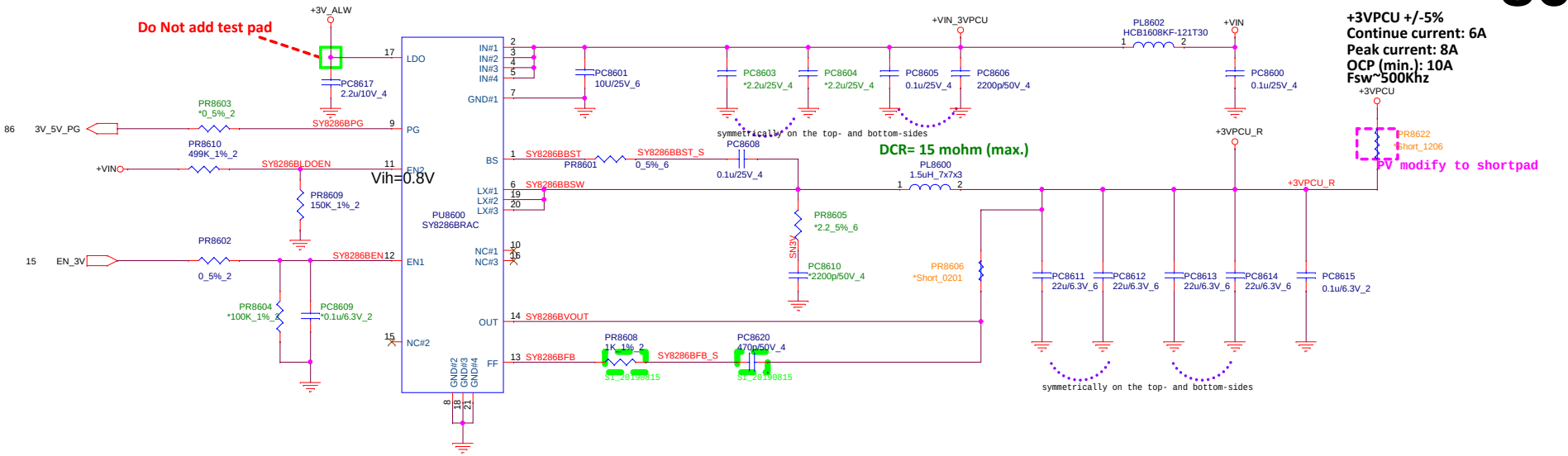

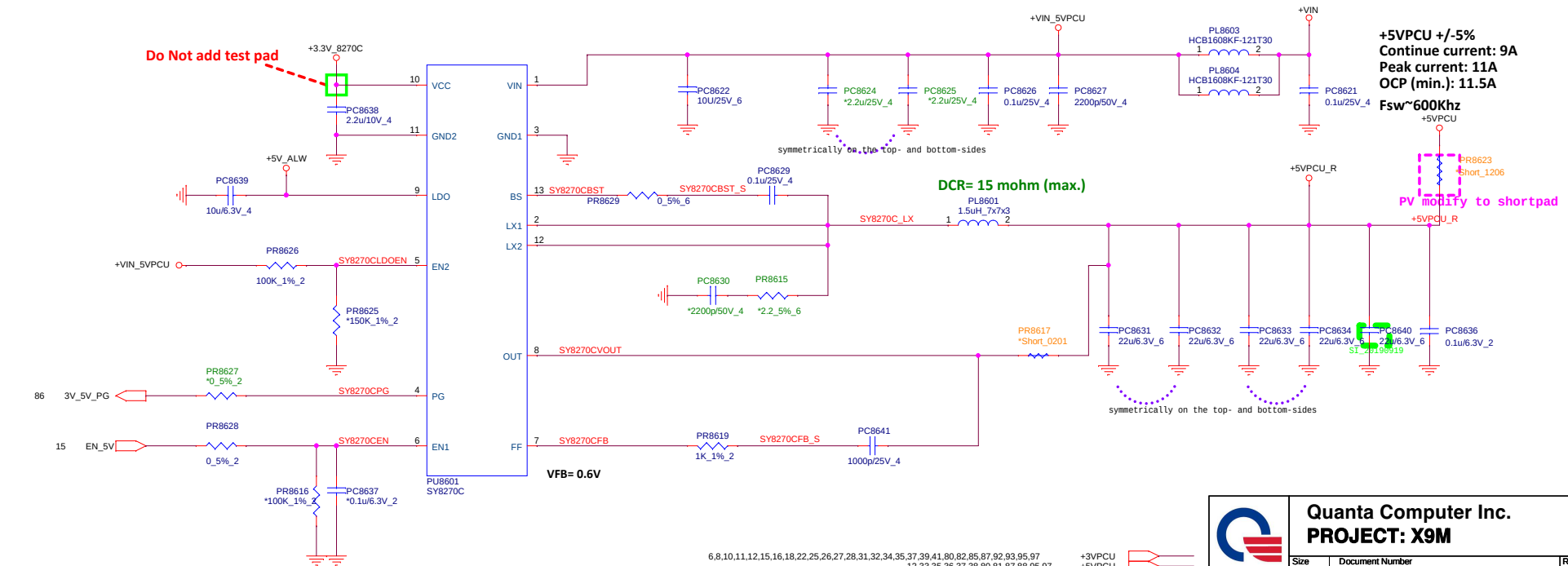

6,8,10,11,12,15,16,18,22,25,26,27,28,31,32,34,35,37,39,41,80,82,85,87,92,93,95,97 +3VPCU
12,33,35,36,37,38,80,81,87,88,95,97 +5VPCU
11,12,15,37,41,82,87,89,90,92,93,97 +VIN

NB5
Custom

Quanta Computer Inc.
PROJECT: X9M

Size	Document Number	Rev
	3V/5V	1A
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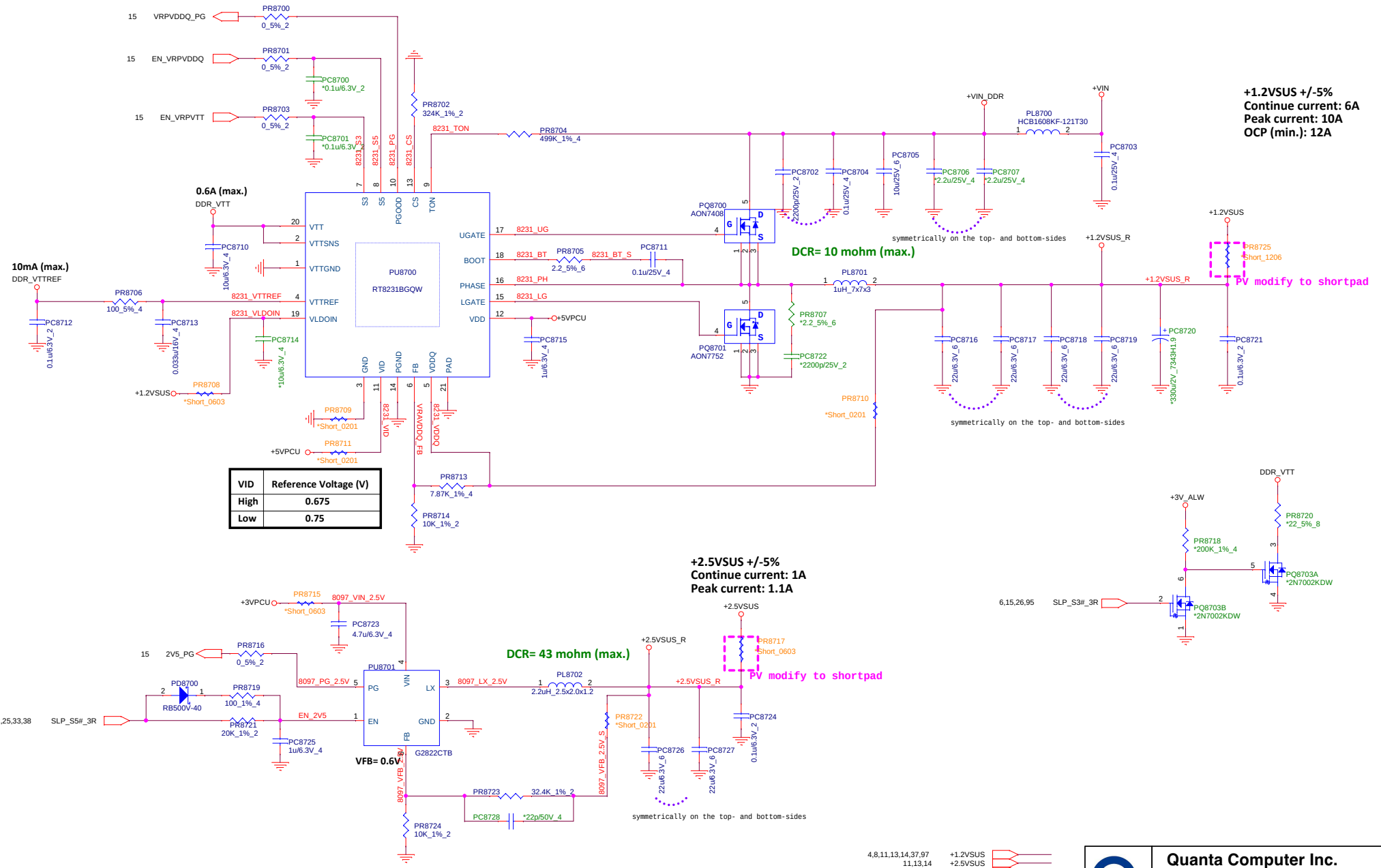
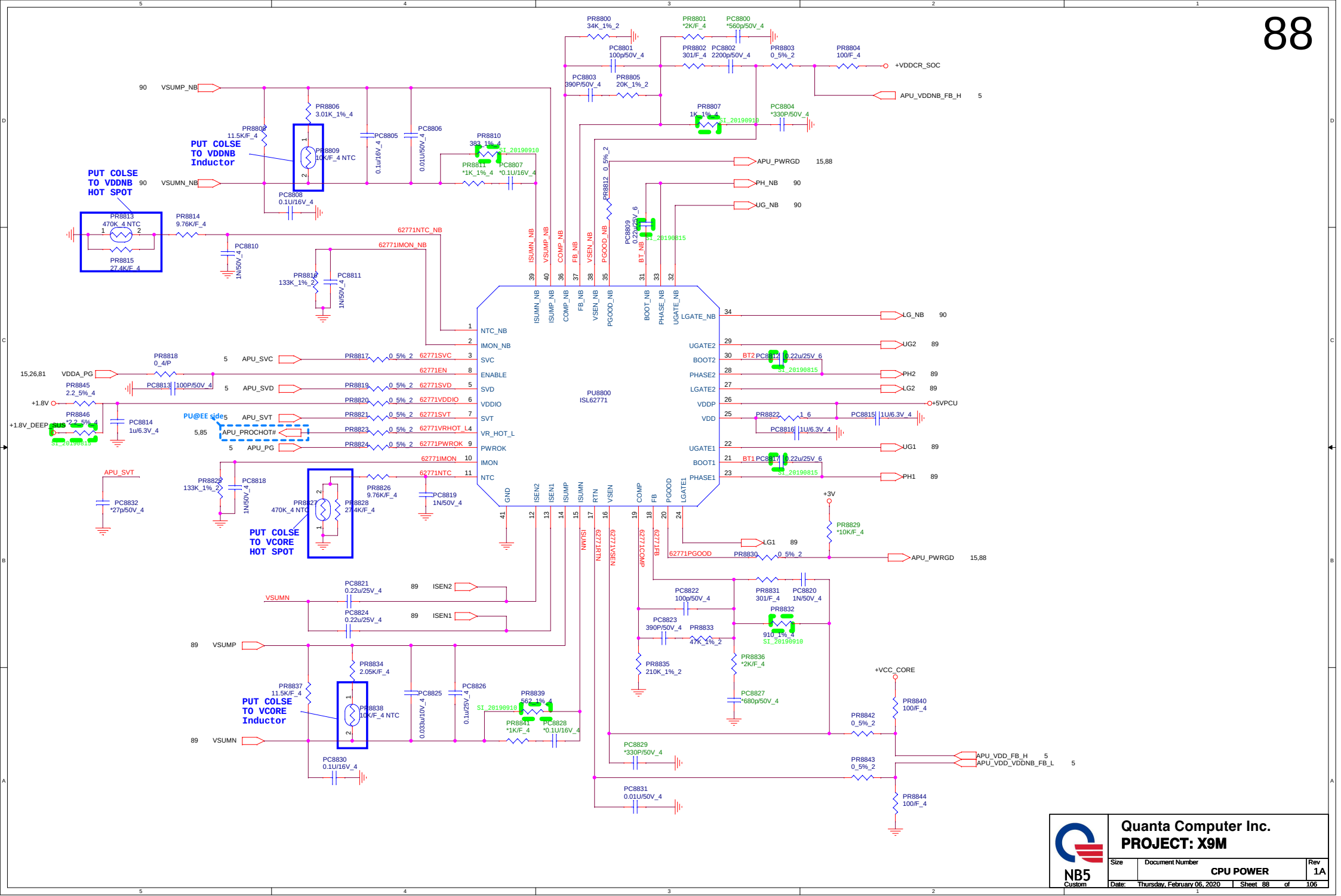


Quanta Computer Inc.		
PROJECT: X9M		
Size	Document Number	Rev
NB5 Custom	DDR	1A
Date: Thursday, February 06, 2020	Sheet 87 of 106	



Quanta Computer Inc.			
PROJECT: X9M			
NB5 Custom	Size	Document Number: CPU POWER	Rev: 1A
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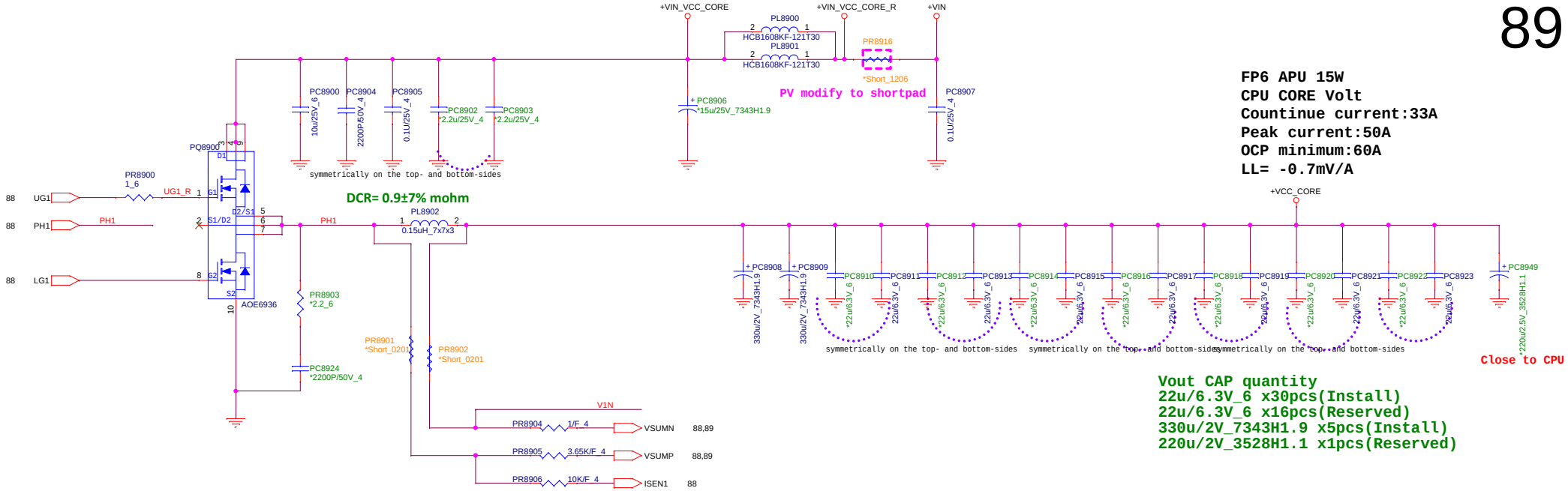
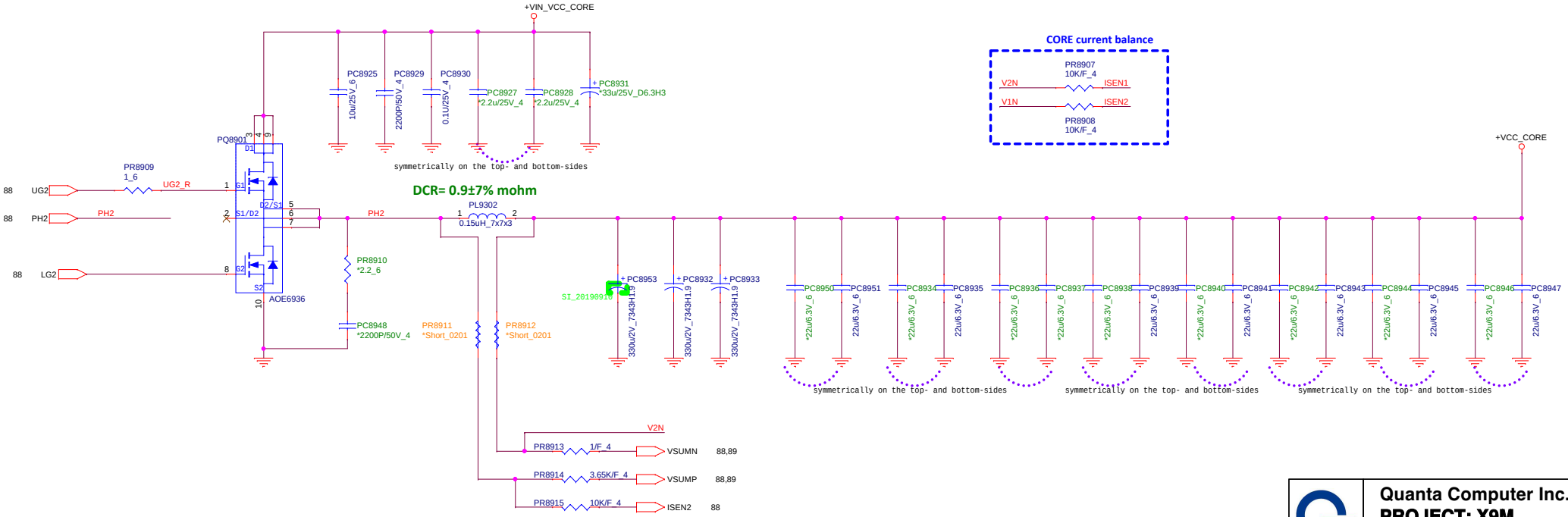
FP6 APU 15W
CPU CORE Volt
Countinue current:33A
Peak current:50A
OCP minimum:60A
LL= -0.7mV/A



Vout CAP quantity
22u/6.3V_6 x30pcs(Install)
22u/6.3V_6 x16pcs(Reserved)
330u/2V_7343H1.9 x5pcs(Install)
220u/2V_3528H1.1 x1pcs(Reserved)



NB5 Custom	Quanta Computer Inc. PROJECT: X9M	
	Size / Document Number: CPU POWER	Rev: 1A
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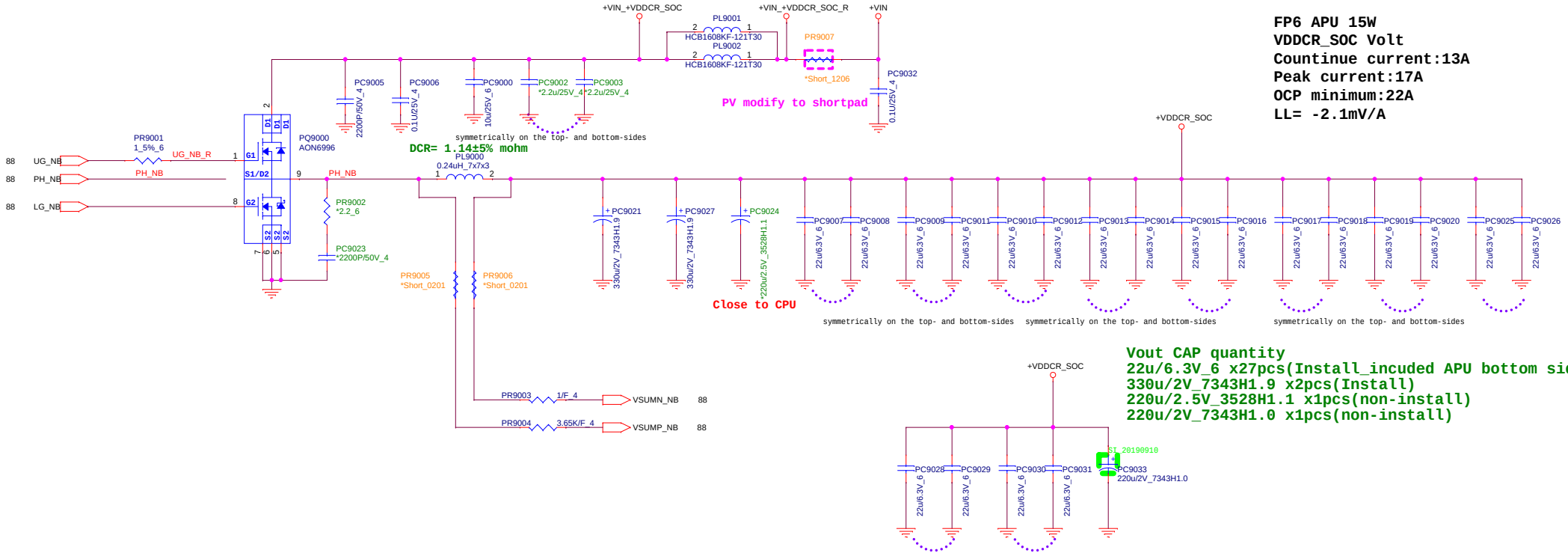


FP6 APU 15W
VDDCR_SOC Volt
Countinue current:13A
Peak current:17A
OCP minimum:22A
LL= -2.1mV/A

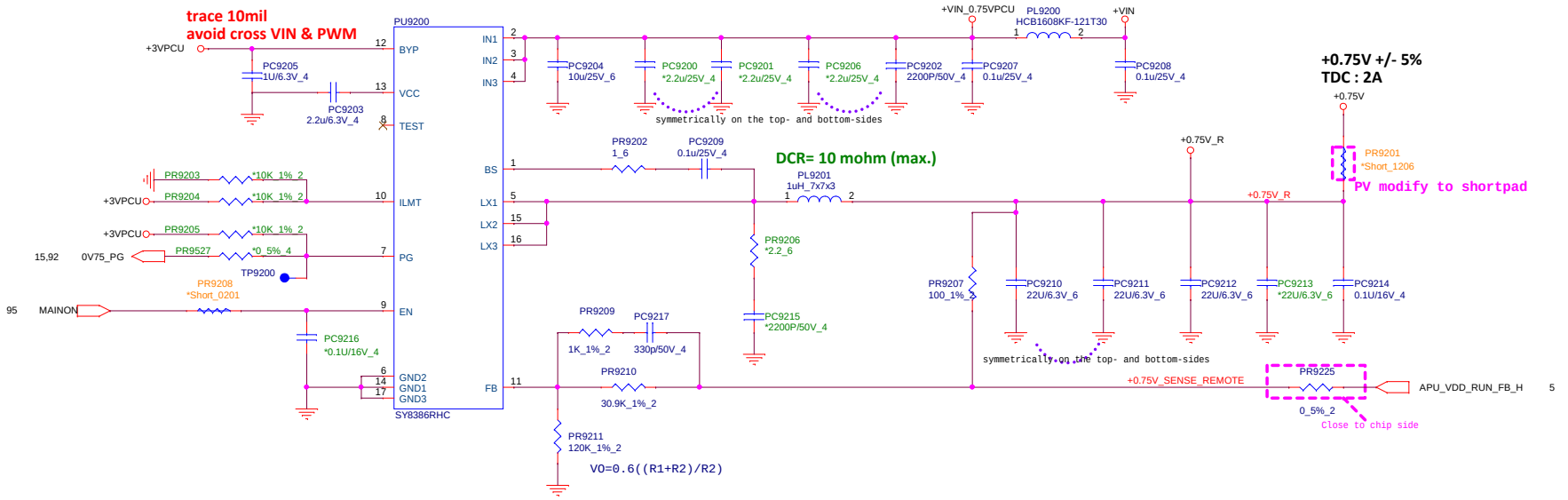
Vout CAP quantity
22u/6.3V_6 x27pcs(Install_incuded APU bottom side)
330u/2V_7343H1.9 x2pcs(Install)
220u/2.5V_3528H1.1 x1pcs(non-install)
220u/2V_7343H1.0 x1pcs(non-install)

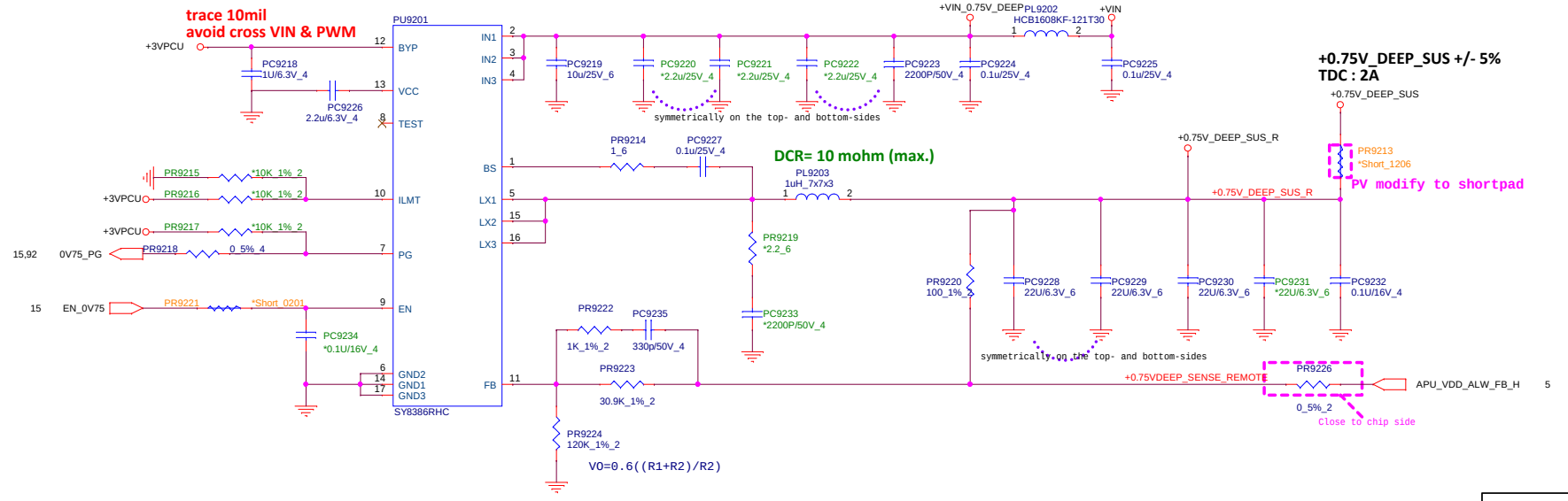
Quanta Computer Inc.		
PROJECT: X9M		
NB5 Custom	Size / Document Number: CPU POWER	Rev: 1A
	Date: Thursday, February 06, 2020	Sheet 90 of 106

NB5
Custom

Quanta Computer Inc.
PROJECT: X9M

Size	Document Number	Rev
	CPU POWER	1A
Date: Thursday, February 06, 2020	Sheet 91 of 106	





8,12 +0.75V_DEEP_SUS
5,8,12,37,95 +0.75V

Quanta Computer Inc.
PROJECT: X9M

Size	Document Number	Rev
NB5 Custom	CPU other power rail	1A
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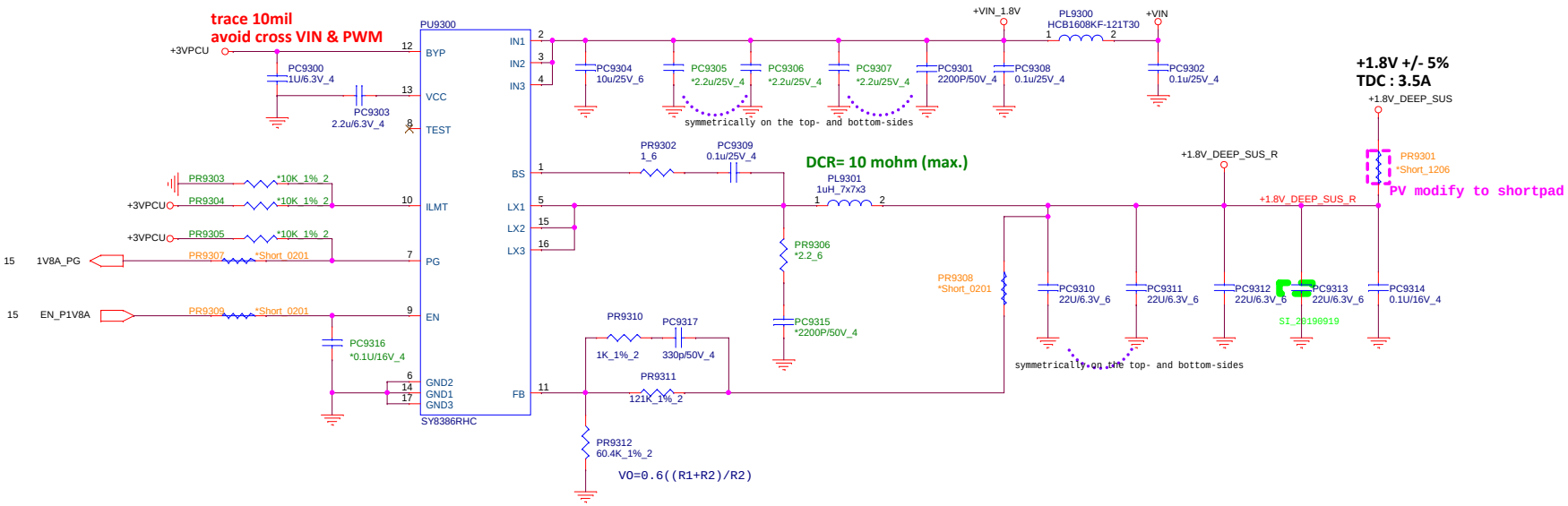

Quanta Computer Inc.		
PROJECT: X9M		
NB5 Custom	Size / Document Number: CPU other power rail	Rev: 1A
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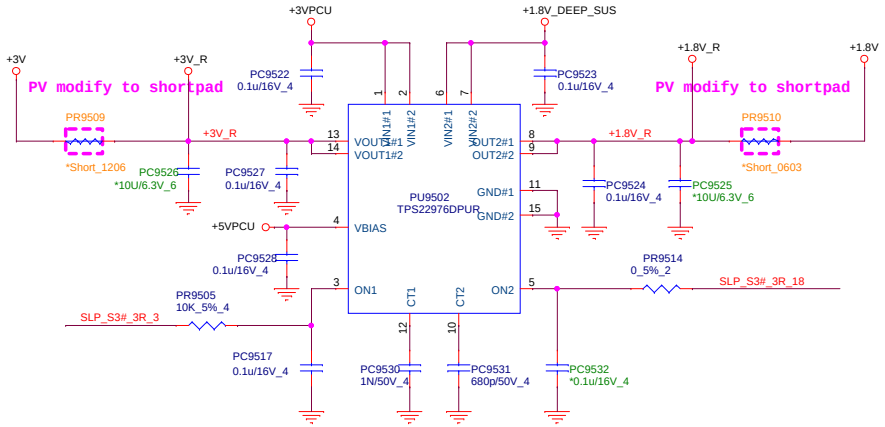
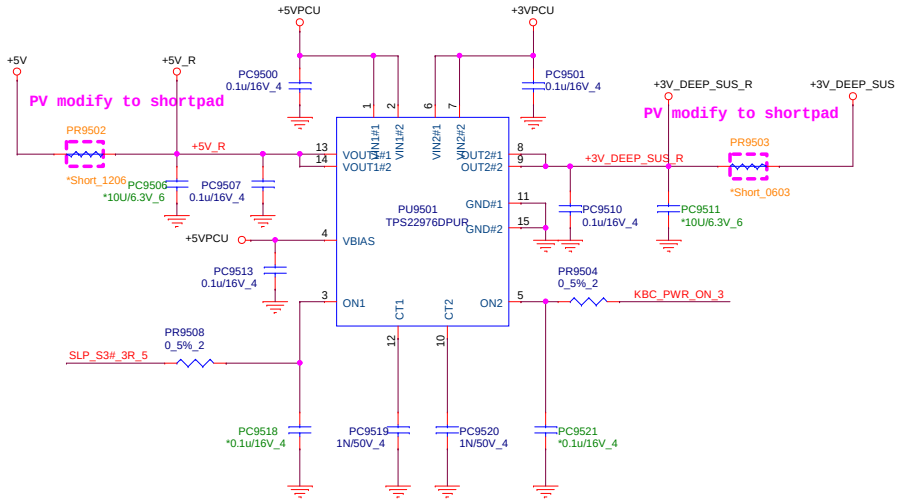
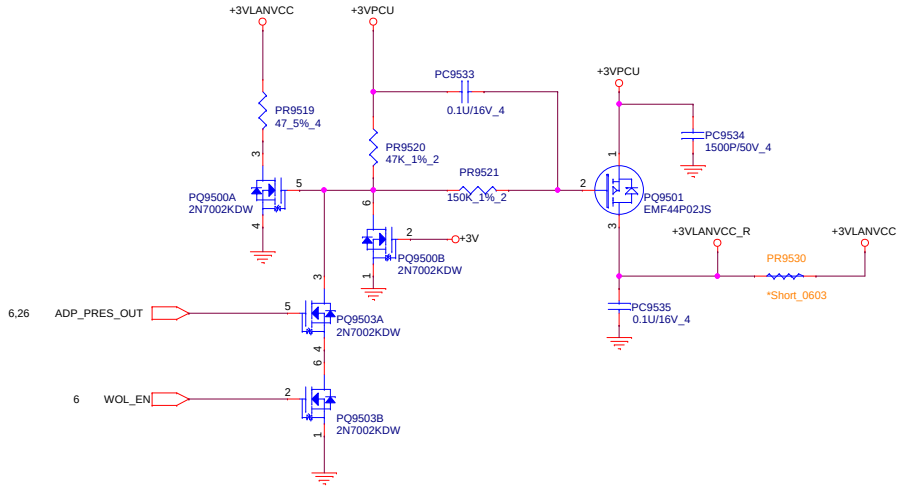
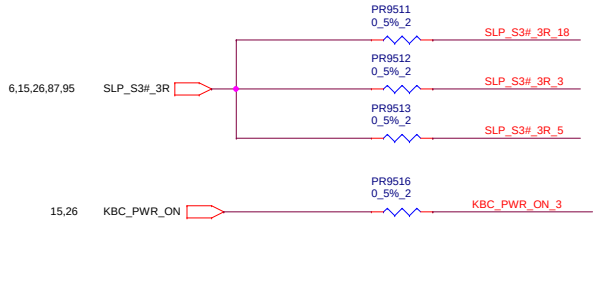
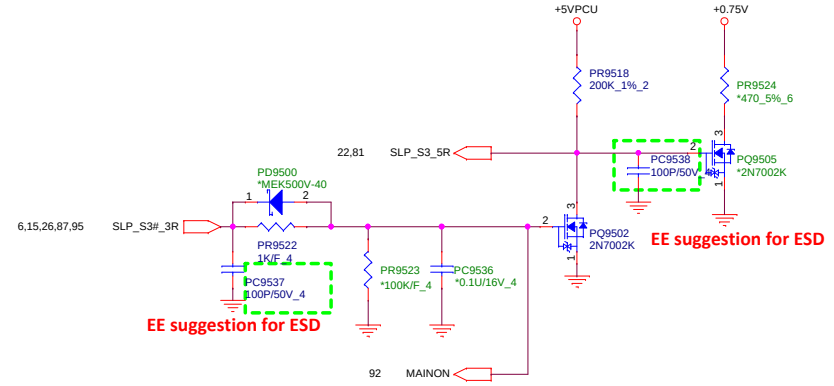
VDDCR_FCH only for Bristol ridge and Stoney Ridge











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12,21,37 +3VLANVCC

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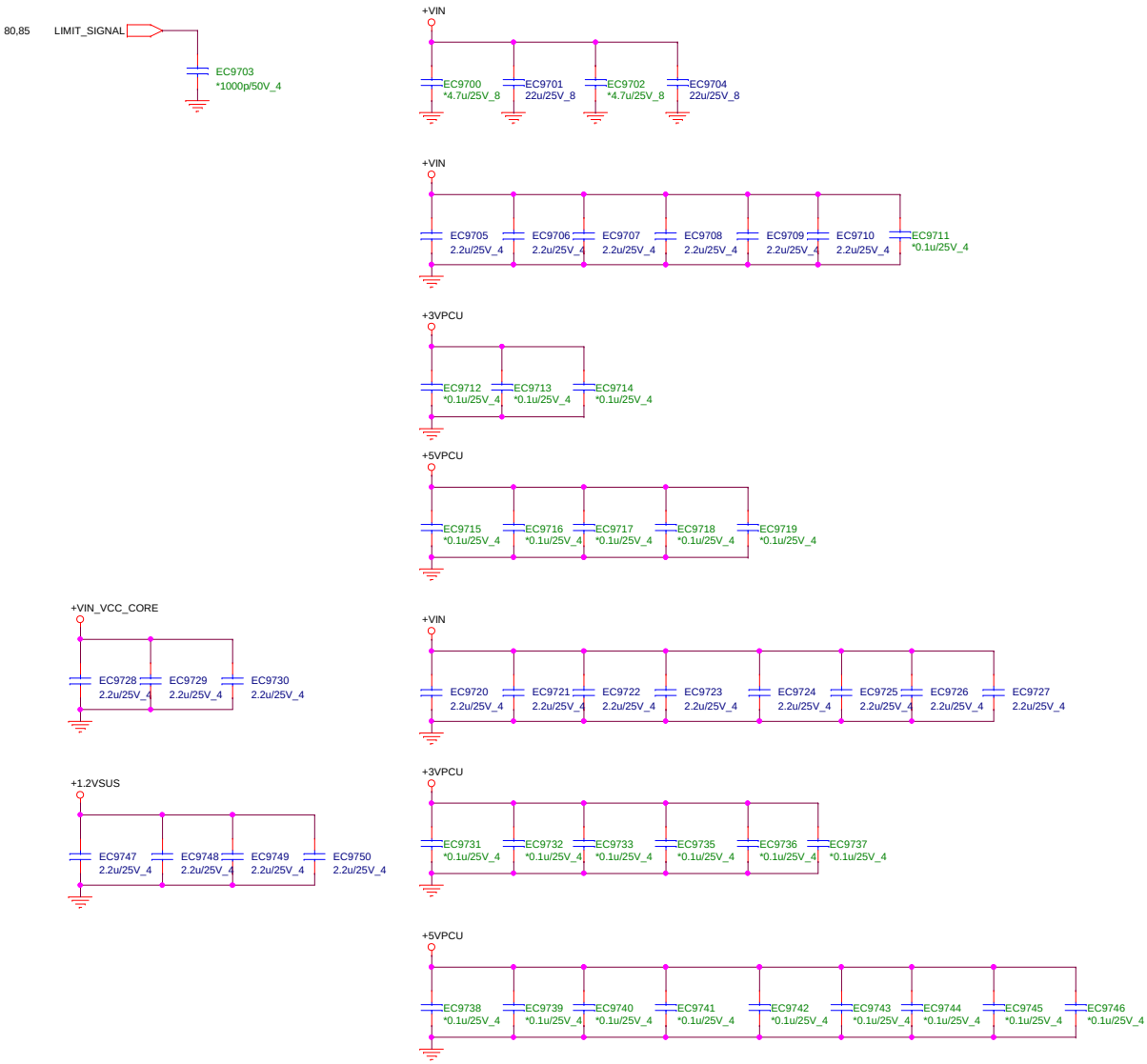

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