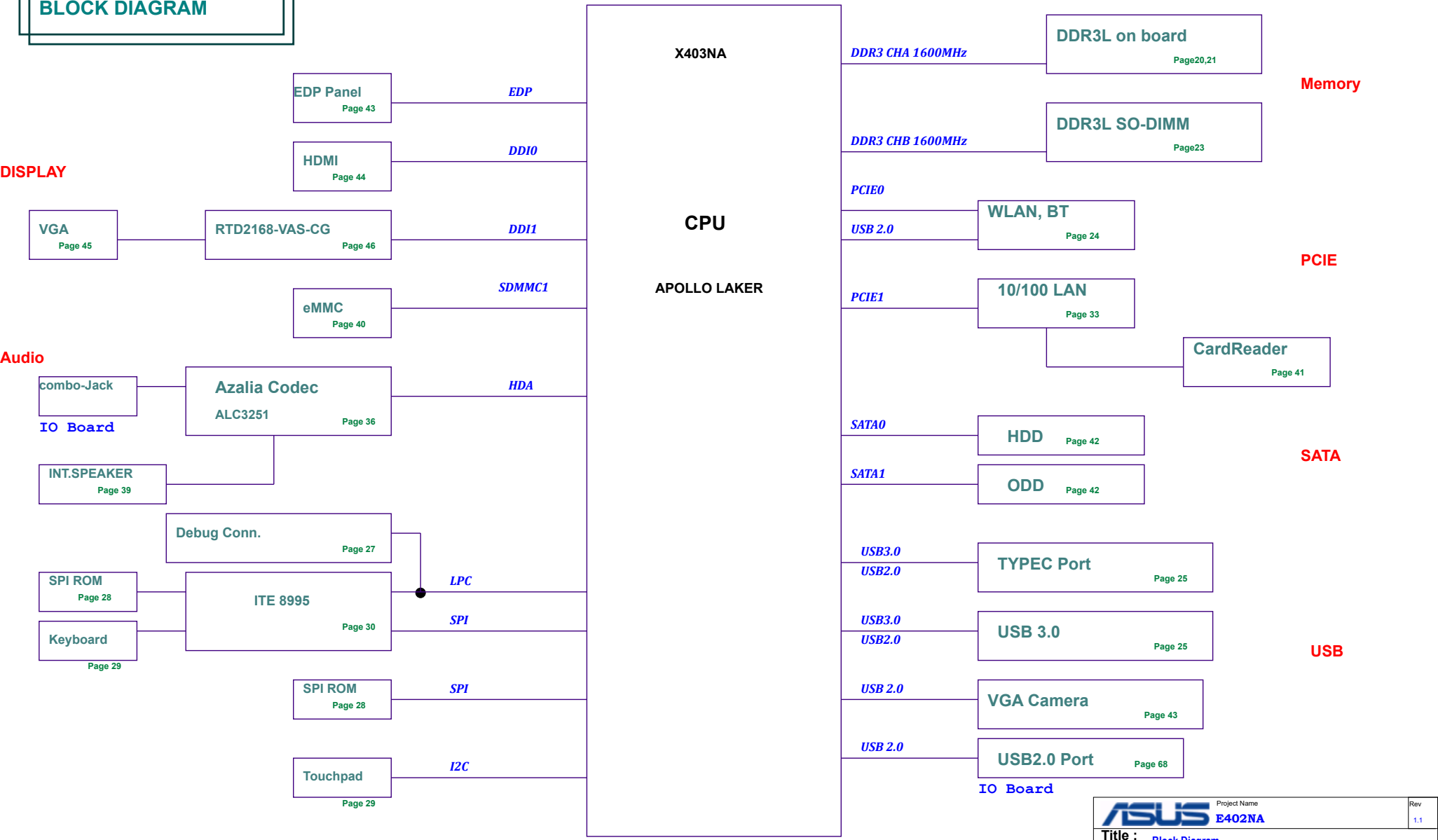
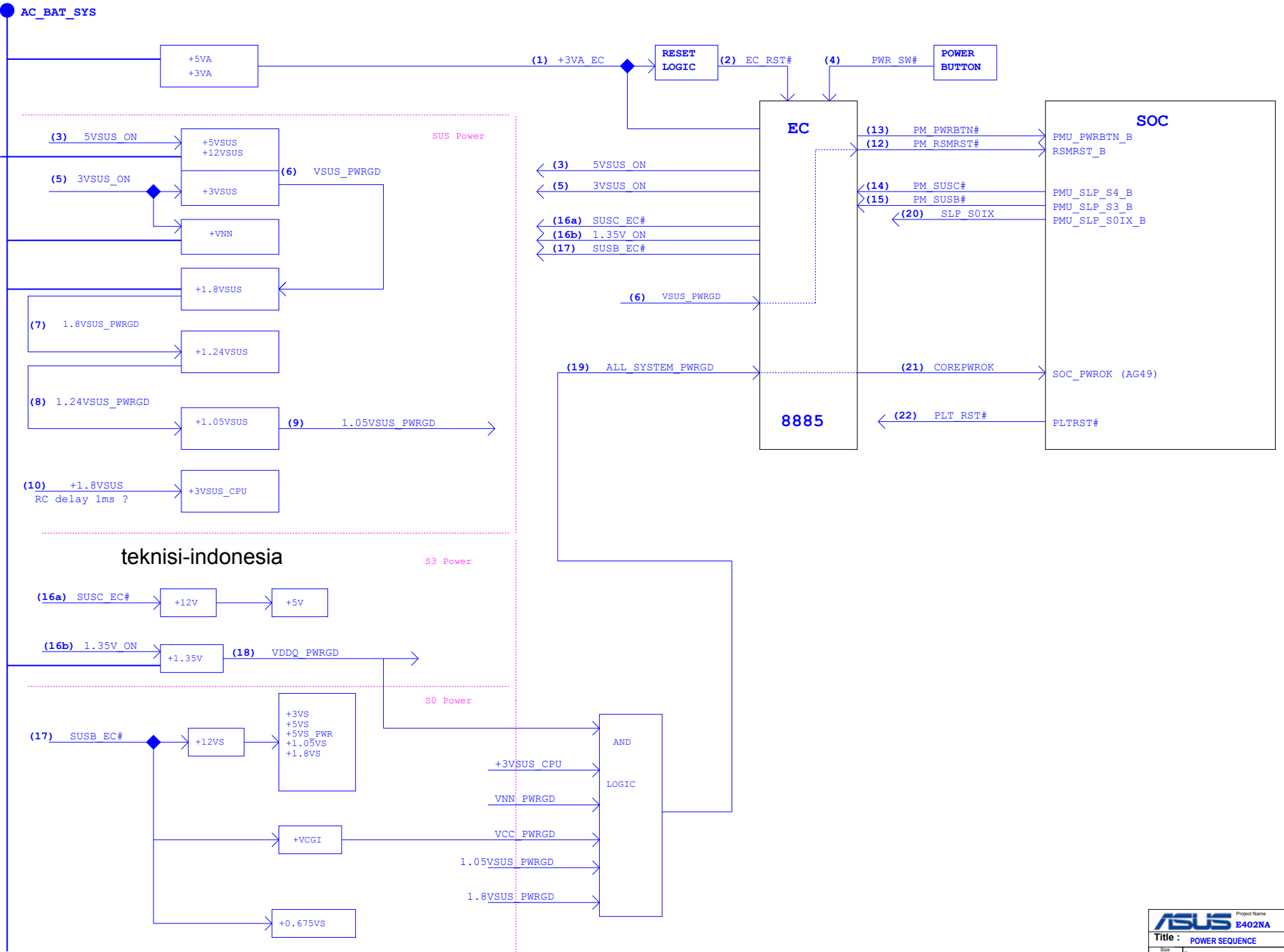
BLOCK DIAGRAM



ASUS	Project Name: E402NA		Rev: 1.1
Title :	Block Diagram		
Size: B	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016		Sheet 1 of 99	

AC-IN Mode

E402NA Power On Sequence Diagram Rev.0.1



Project Name: E402NA			Rev: 1.1
Title: POWER SEQUENCE			
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 4 of 99		

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPIO_0		GPO	DBG_PTI_CLK0			+1.8V
GPIO_1		GPO	DBG_PTI_DATA0			
GPIO_2		GPO	DBG_PTI_DATA1			
GPIO_3		GPO	DBG_PTI_DATA2			
GPIO_4		GPO	DBG_PTI_DATA3			
GPIO_5		GPO	DBG_PTI_DATA4			
GPIO_6		GPO	DBG_PTI_DATA5			
GPIO_7		GPO	DBG_PTI_DATA6			
GPIO_8		GPO	DBG_PTI_DATA7			
GPIO_9		GPI	(N.C)			
GPIO_10		GPI	(N.C)			
GPIO_11		GPI	EXT_SCI#		PU 4.7K	+1.8VSUS
GPIO_12		GPI	EC_WAKE_SCI_SOC		PU 4.7K	+1.8VSUS
GPIO_13		GPO	BT_ON_SOC#			
GPIO_14		GPO	WLAN_ON_SOC#			
GPIO_15		GPO	WLAN_LED_SOC#			
GPIO_16		GPO	BT_LED_SOC#			
GPIO_17		GPO	(N.C)			
GPIO_18		GPI	TP_INT#_SOC		PU 10K	+1.8VSUS
GPIO_19		GPO	(N.C)			
GPIO_20		GPO	(N.C)			
GPIO_21		GPO	(N.C)			
GPIO_22		GPO	(N.C)			
GPIO_23		GPO	SATA_ODD_PWRGT		PU 10K	+3VS
GPIO_24		Native	(N.C)			
GPIO_25		GPI	SATA_ODD_DA#		PU 10K	+1.8VS
GPIO_26		Native	(N.C)			
GPIO_27		GPO	(N.C)			
GPIO_28		Native	(N.C)			
GPIO_29		Native	(N.C)			
GPIO_30		GPI	PCBID0		PU/PD 1K	+1.8VSUS
GPIO_31		GPI	PCBID1		PU/PD 1K	+1.8VSUS
GPIO_32		GPI	PCBID2		PU/PD 1K	+1.8VSUS
GPIO_33		Native	(N.C)			
GPIO_34		Strap	GPIO_34			
GPIO_35		Strap	GPIO_35			
GPIO_36		Strap	GPIO_36			
GPIO_37		Strap	GPIO_37		PU 4.7K	+1.8VSUS
GPIO_38		GPO	(N.C)			
GPIO_39		Strap	LPSS_UART0_TXD			
GPIO_40		Strap	LPSS_UART1_RTS_N			
GPIO_41		Native	(N.C)			
GPIO_42		GPI	LPSS_UART1_RXD			
GPIO_43		GPI	LPSS_UART1_R_TXD			
GPIO_44		GPI	LPSS_UART1_RTS_N			
GPIO_45		Native	(N.C)			
GPIO_46		GPI	EXT_SMI#			
GPIO_47		Strap	LPSS_UART2_TXD			
GPIO_48		Strap	GPIO_48			
GPIO_49			(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPIO_62		GPO	(N.C)			+1.8V
GPIO_63		GPO	(N.C)			
GPIO_64		GPO	(N.C)			
GPIO_65		GPO	(N.C)			
GPIO_66		GPO	(N.C)			
GPIO_67		GPO	(N.C)			
GPIO_68		GPO	(N.C)			
GPIO_69		GPO	(N.C)			
GPIO_70		GPO	(N.C)			
GPIO_71		GPO	(N.C)			
GPIO_72		GPO	(N.C)			
GPIO_73		GPO	(N.C)			
		Native	DBG_H_TCK			
		Native	DBG_H_TRST_N		PD 51	+1.8VSUS
		Native	DBG_H_TMS		PD 51	+1.8VSUS
		Native	DBG_H_TDI		PD 51	+1.8VSUS
		Native	(N.C)			
		Native	DBG_H_PREQ_N		PU 100	+1.8VSUS
		Native	(N.C)			
		Native	DBG_H_PRDY_N		PU 100	+1.8VSUS
		Native	DBG_H_TDO		PU 100	+1.8VSUS
		GPI	(N.C)			
		GPI	(N.C)			
		GPI	(N.C)			
		GPI	(N.C)			
		GPI	SVID_ALERT#			+1.05VSUS
		Native	SVID_DATA			+1.05VSUS
		GPO	SVID_CLK			+1.05VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPIO_187		Native	HDMI_SDAT		PU 2.2K	+1.8VSUS
GPIO_188		GPO	HDMI_SCLK		PU 2.2K	+1.8VSUS
GPIO_189		Native	(N.C)			
GPIO_190		Native	(N.C)			
GPIO_191		GPO	(N.C)			
GPIO_192		GPO	(N.C)			
GPIO_193		GPO	EDP_VDDEN			
GPIO_194		GPO	EDP_BLEN			
GPIO_195		GPO	EDP_BLCTL		PD 100K	+1.8VSUS
GPIO_196		GPI	(N.C)			
GPIO_197		GPI	(N.C)			
GPIO_198		Native	(N.C)			
GPIO_199		GPI	DP_HPD#		PU 10K	+1.8VSUS
GPIO_200		GPI	HDMI_HPD#		PU 10K	+1.8VSUS
GPIO_201		Native	(N.C)			
GPIO_202		Native	(N.C)			
GPIO_203		GPI	USB_OC_0#		PU 10K	+1.8VSUS
GPIO_204		GPI	USB_OC_1#		PU 10K	+1.8VSUS
GPIO_213		GPO	(N.C)			
GPIO_214		GPO	(N.C)			
GPIO_215		GPO	(N.C)			
GPIO_74		GPO	(N.C)			
GPIO_75		GPI	(N.C)			
GPIO_76		GPO	(N.C)			
GPIO_77		GPO	(N.C)			
GPIO_78		Strap	GPIO_78		PU 4.7K	+1.8VSUS
GPIO_79		Native	(N.C)			
GPIO_80		Native	(N.C)			
GPIO_81		Native	(N.C)			
GPIO_82		Strap	SOC_DMIC_CLKAB2		PD 4.7K	+1.8VSUS
GPIO_83		Native	(N.C)			
GPIO_84		GPO	ACZ_RST#_AUD		PU 100K	+1.8VS
GPIO_85		Native	(N.C)			
GPIO_86		Native	(N.C)			
GPIO_87		Native	(N.C)			
GPIO_88		Strap	AVS_I2S2_SDO		PD 10K	+1.8VSUS
GPIO_89		Native	(N.C)			
GPIO_90		Native	(N.C)			
GPIO_91		Native	(N.C)		PD 10K	+1.8VSUS
GPIO_92						
GPIO_97		GPO	HSCE#_PCH			
GPIO_98		Native	(N.C)			
GPIO_99		Native	HMOSI_PCH			
GPIO_100		Native	HMISO_PCH			
GPIO_101		Native	HMIO2_PCH			
GPIO_102		Native	HMIO3_PCH			
GPIO_103		GPO	HSCK_PCH			
GPIO_104		Strap	GP_SSP0_CLK		PD 10K	+1.8VSUS
GPIO_105		Strap	GP_SSP0_FS0		PD 10K	+1.8VSUS
GPIO_106		Strap	GP_SSP0_FS1		PU 4.7K	+1.8VSUS
GPIO_109		Native	(N.C)			
GPIO_110		Strap	GP_SSP0_TXD		PD 10K	+1.8VSUS
GPIO_111		Strap	GP_SSP1_CLK		PD 4.7K	+1.8VSUS
GPIO_112		Strap	GPIO_112		PD 10K	+1.8VSUS
GPIO_113		Strap	GPIO_113		PD 10K	+1.8VSUS
GPIO_116		Native	(N.C)			
GPIO_117		Strap	GPIO_117		PD 10K	+1.8VSUS
GPIO_118		Strap	GP_SSP2_CLK		PD 10K	+1.8VSUS
GPIO_119		Strap	GP_SSP2_FS0			
GPIO_120		Strap	GP_SSP2_FS1		PD 10K	+1.8VSUS
GPIO_121		Strap	GP_SSP2_FS2		PD 10K	+1.8VSUS
GPIO_122		Native	(N.C)			
GPIO_123		Strap	GP_SSP2_TXD		PU 4.7K	+1.8VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPIO_132		Native	TP_SDA_SOC		PU 2.2K	+1.8VSUS
GPIO_133		Native	TP_SDA_SOC		PU 2.2K	+1.8VSUS
GPIO_146		GPO	ACZ_BCLK_AUD			
GPIO_147		GPO	ACZ_SYNC_AUD			
GPIO_148		GPI	ACZ_SDIN0_AUD			
GPIO_149		GPO	ACZ_SDOUT_AUD			
GPIO_209		GPI	(N.C)		PU 10K	+1.8VSUS
GPIO_210		GPI	(N.C)		PU 10K	+1.8VSUS
		GPI	ME_AC_PRESENT_SOC			
		GPI	BATLOW#		PU 10K	+3VSUS
		GPO	PLT_RST#			
		GPI	PM_PWRBTN#			
		GPI	PM_RSTBTN#			
		GPO	PM_SUSB#		PD 10K	+3VSUS
		GPO	PM_SUSC#		PD 10K	+3VSUS
		GPO	PM_SUSCLK			
		GPI	PM_WAKE#			
		Native	(N.C)			
		GPO	NC(SUSPWRDNACK)			
			(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPIO_205		GPO	PCIE_WAKE0_N			
GPIO_206		GPO	PCIE_WAKE1_N			
GPIO_207		Native	(N.C)			
GPIO_208		Native	(N.C)			
GPIO_156		GPO	EMMC_CLK			
GPIO_157		Native	EMMC_DATA0			
GPIO_158		Native	EMMC_DATA1			
GPIO_159		Native	EMMC_DATA2			
GPIO_160		Native	EMMC_DATA3			
GPIO_161		Native	EMMC_DATA4			
GPIO_162		Native	EMMC_DATA5			
GPIO_163		Native	EMMC_DATA6			
GPIO_164		Native	EMMC_DATA7			
GPIO_165		GPO	EMMC_CMD			
GPIO_172		GPO	SDCARD_CLK			
GPIO_173			SDCARD_D0			
GPIO_174		GPO	SDCARD_D1			
GPIO_175		GPO	SDCARD_D2			
GPIO_176		GPO	SDCARD_D3			
GPIO_177		GPI	SDCARD_CD_N		PU 10K	+1.8VSUS
GPIO_178		Native	SDCARD_CMD			
GPIO_182		GPI	NC(EMMC_RCLK)			
GPIO_183		GPI	SD_PWR_EN#			
GPIO_186		GPO	SDCARD_WP		PU 10K	+1.8VSUS

PCIE/USB3/SATA Mapping

HSIO Capabilities	Design IP
PCIE_P0	LAN & CardReader
PCIE_P1	WLAN
PCIE_P2	
PCIE_P3 / USB3_P4	
PCIE_P4 / USB3_P3	
PCIE_P5 / USB3_P2	USB 3.0
USB3_P1	TYPEC_B channel
USB3_P0	TYPEC_A channel
SATA_P0	HDD
SATA_P1 / USB3_P5	ODD

USB 2.0	Design IP
USB2_P7	
USB2_P6	
USB2_P5	
USB2_P4	camera
USB2_P3	BT
USB2_P2	USB 3.0
USB2_P1	USB 2.0
USB2_P0	TYPEC

I2C Settinging

I2C	Design IP
I2C_P0	
I2C_P1	
I2C_P2	
I2C_P3	
I2C_P4	touchpad
I2C_P5	
I2C_P6	
I2C_P7	

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#	PU 10K (@)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (@)	+3VA_EC
GPA3	Alt	GPO	NUM_LED#		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN0_PWM		
GPA6	Alt	PWM	NC		
GPA7	O	GPO	NC		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	EC_GPB2_NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON		
GPB5	O	GPO	A20GATE	PU 10K (@)	+3VS
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPI	PM_EXTTS#0	PU 10K (@)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K (@)	+3VSUS
GPC4	I	GPI	EC_GPC4	PU 10K	+3VSUS
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	+3VA_EC
GPC7	O	GPO	EC_GPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VSUS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN0_TACH	PU 10K	+3VS
GPD7	Alt	GPI	EC_GPD7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	LAN_WAKE#	PU 10K (@)	+3VA_EC
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUSB#	PD 100K	
GPE6	OD	GPO	EC_GPE6/CAP_LED#	PU 100K (@)	+3VA_EC
GPE7	OD	GPO	THRO_CPU#	PU 10K	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PWRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCE#/EC_SCE#_PCH	PD 10K (@)	
GPG4	GPI		EC_SI/EC_SI_PCH	PD 10K (@)	
GPG5	GPI		EC_SO/EC_SO_PCH	PD 10K (@)	
GPG6	O	GPO	USB30_5VBUS		
GPG7	GPI		EC_SCK/EC_SCK_PCH	PD 10K (@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

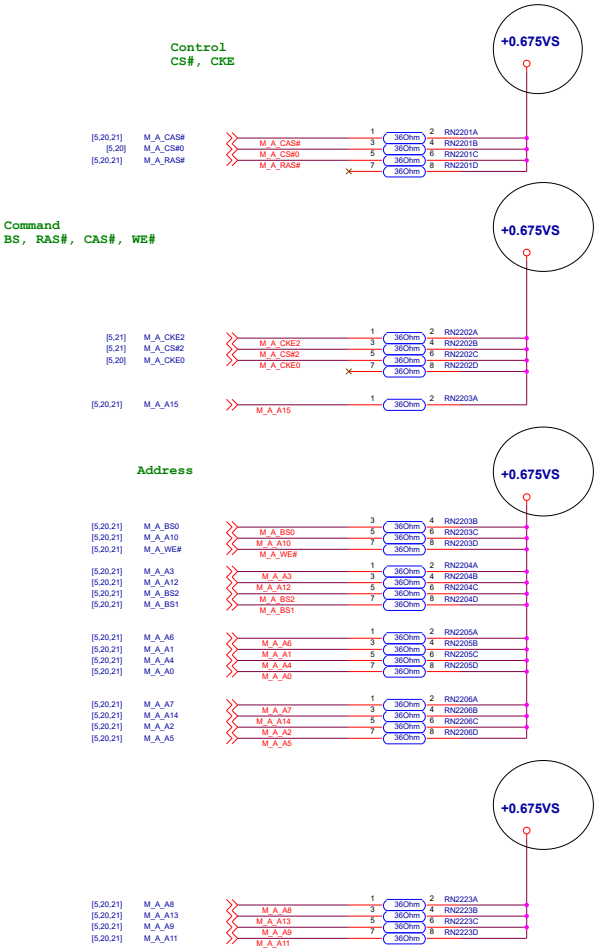
	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#		
GPI1	I	GPI	3VSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PU 100K(@)&PD 0	+3VACC
GPI7	Alt	AD	MB_MAX_POWER	PU 100K&PD 560K	+3VACC

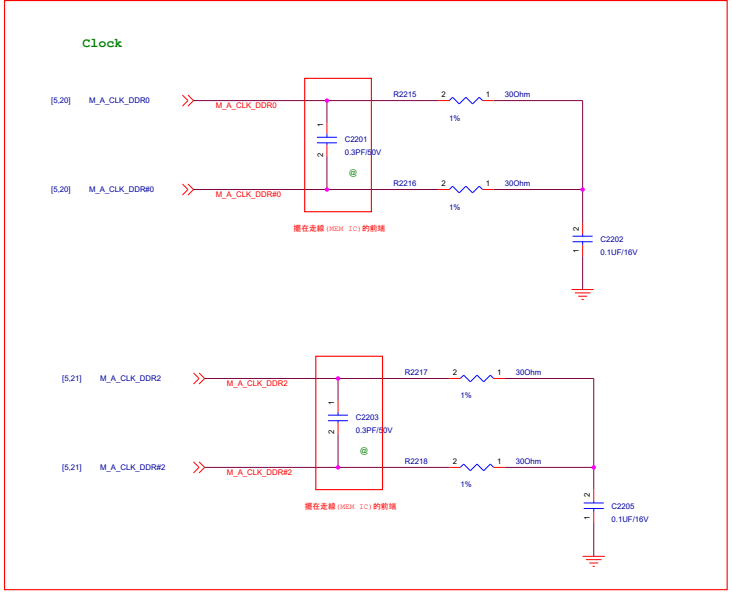
	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB31_5VBUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	EC_GPJ6/ID#	PU 10K	+3VSUS
GPJ7	O	GPO	USB_CHARGE_ON#		

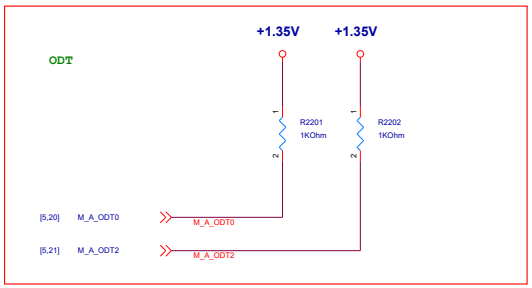
	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

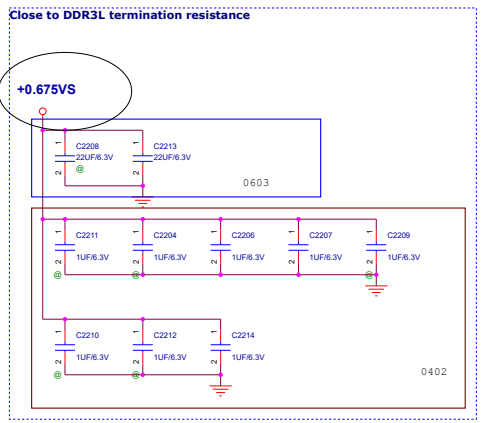
E402NA

Title : System Setting









X450UMA

MEM_On-Board CH.B

Evelyn and Kobe

PC2-RD1-Sys2-EE1

C

E402NA

1.1

Tuesday, July 19, 2016

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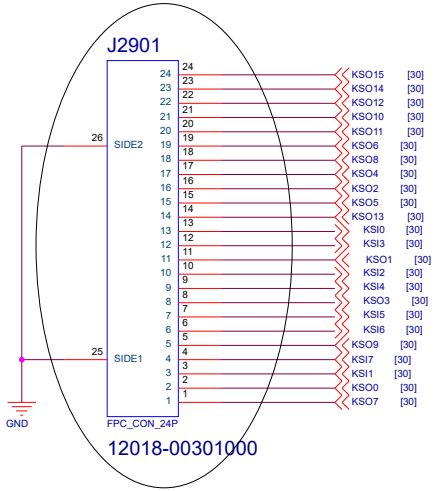
Keyboard Connector



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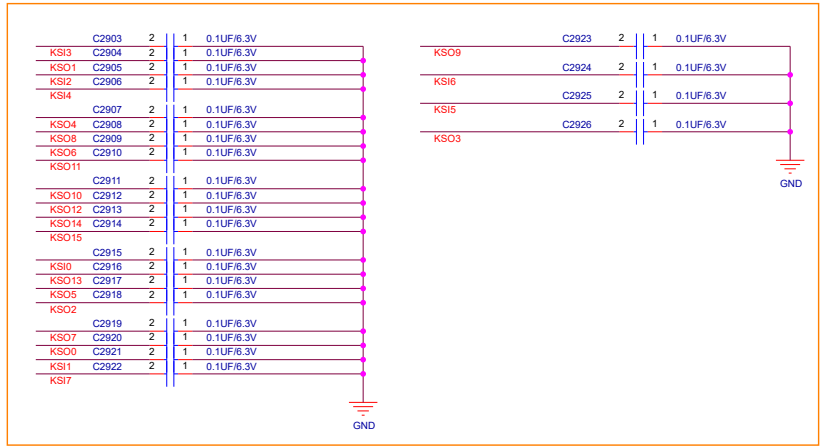
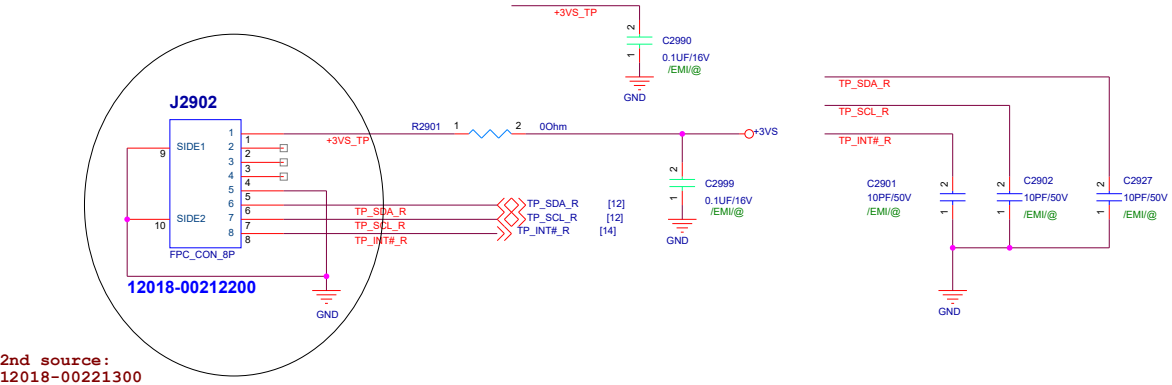


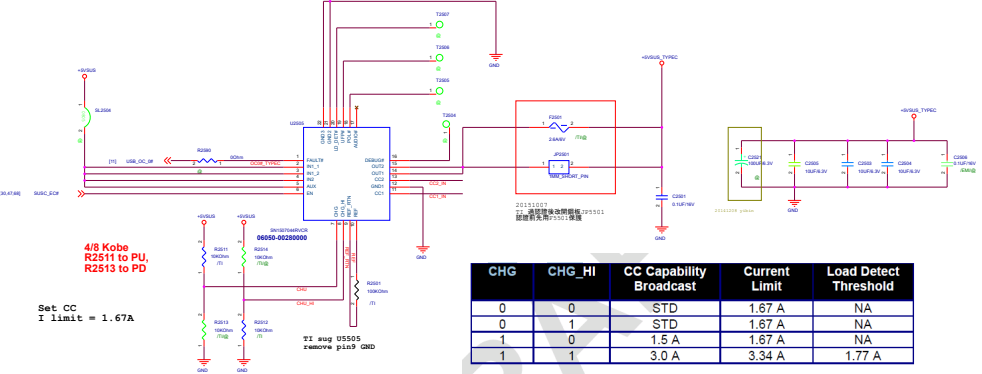
TouchPad Connector

20160303 Evelyn Modify

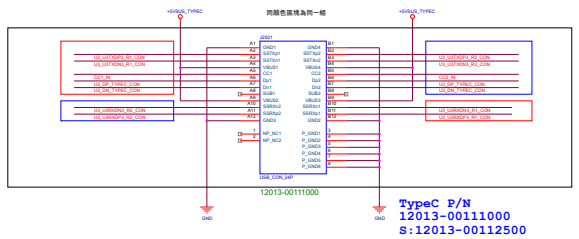


2nd source:
12018-00221300

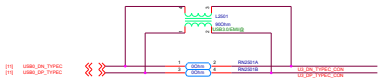
ASUS	Project Name: E402NA		Rev: 1.1
Title : KB_TP			
Size: B	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 29 of 99		



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

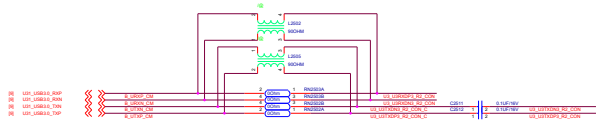


TypeC P/N
12013-00111000
S:12013-00112500

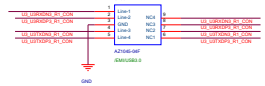


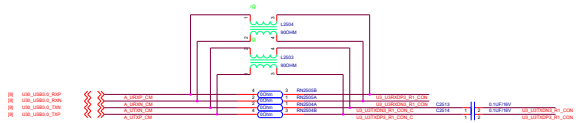
USB3.0 ESD-Protection

2nd source:
07G028076030

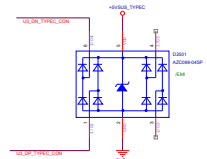


USB3.0 ESD-Protection

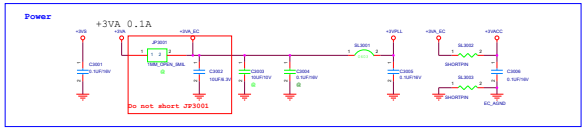


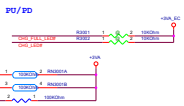


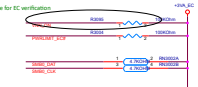
USB2.0 ESD-Protection

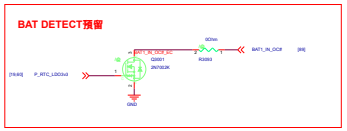


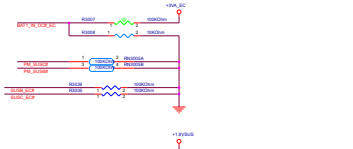
ASUS	Project Name: E402NA		Rev: 1.1
Title: Block Diagram			
Size: D	Dept.: PCH-KOT-SysLD-EX1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 25 of 59		

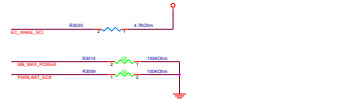

Power
+3VA 0.1A
Do not short JP3001


PU/PD

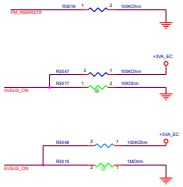

20160322 Reserve for EC verification

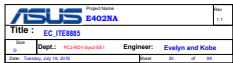

BAT DETECT預留






Thermal Verification 2016/3/16




Project Name
E402NA
Title : EC_ITE8885
Engineer: Evelyn and Kobe

E402NA R1.1 Changelist

4/8 Kobe REF SR3 schemetic
1. remove VGA
2. remove ODD
3. remove SD_PCH
4. change MEM REF SR2 (P5,P20,P21,P22)
5. P.49 add EMI solution REF SR2
6. P.13 省略 U1302 , REF SR2 因 PLT_RST# = 3V
7. P.17 change R1735 to PU,R1734 RD, EC OD pin
8. P.25 R2511 to PU,R2513 to PD (1.5A)

E502NA R1.0 Changelist

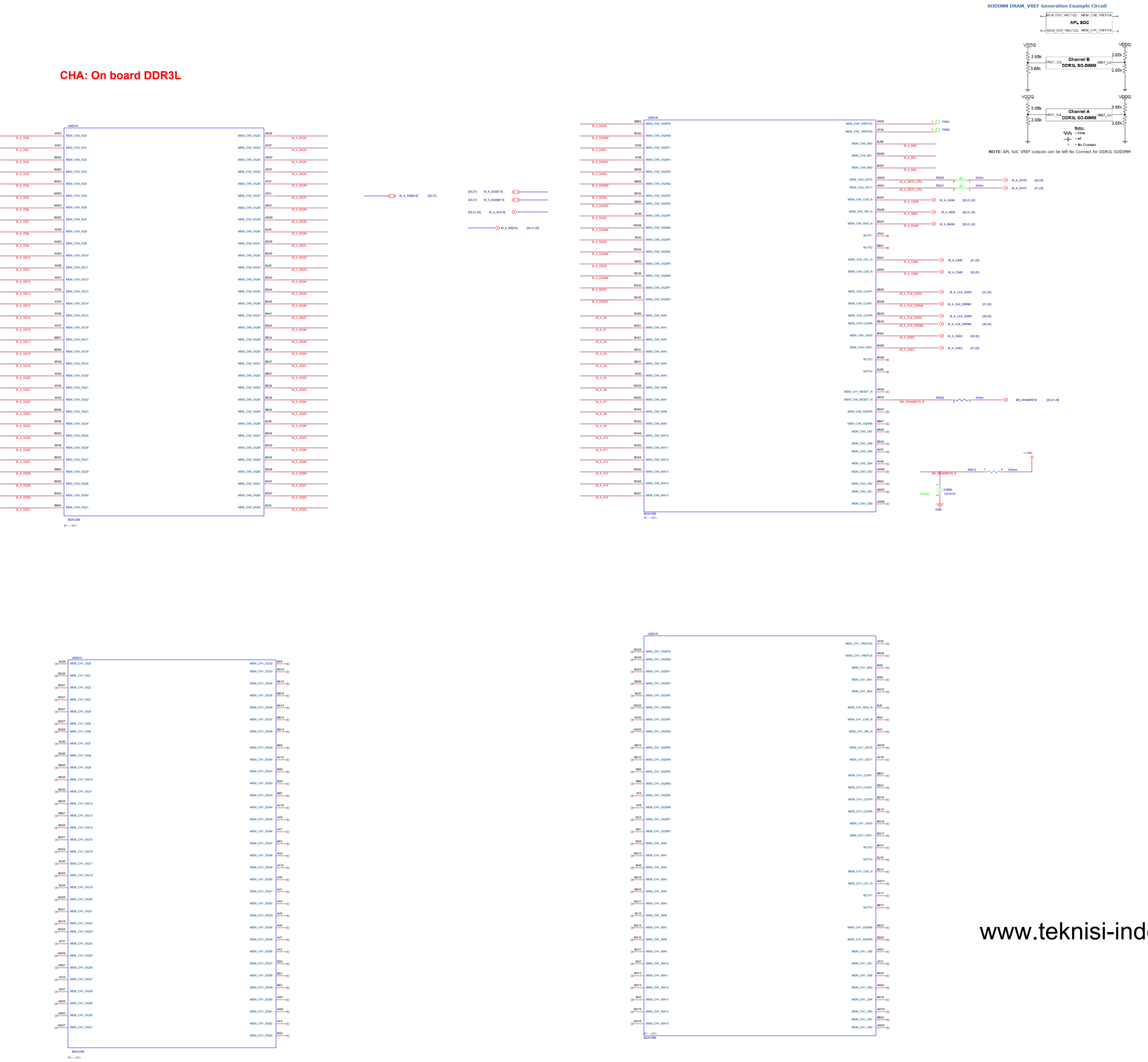
1. SVID PU +1.05VS page.11
2. CC logic +5VSUS and SUSC_EC# page.25
3. Use 1.24VSUS_PWRGD, VDDQ_PWRGD, VNN_PWRGD, VCC_PWRGD page.32
4. ITE.11 use +3VSUS ITE.67 change to 1.24VSUS_PWRGD page.30
5. Add +1.05VS and remove +3VSUS_CPU, +1.05VSUS page.26
6. Remove PCIE_WAKE page.08
7. SMBUS chamge to 3.3V page.11 17 27
8. TP INT change to +1.8VSUS page.14
9. I2C and HPD change to 1.8VSUS page.44
10. EDP HPD change to 1.8VSUS page.43
11. remove SATA_DEVSLP
12. page.32
13. C2511~C2514 change from SAMSUNG to 11G232210411070 page.25
14. change U6801 to 06016-01290000 (3.2A) page.68
15. Change 1.05VSUS to 1.05VS
16. remove +5V and +12V

E502NA R1.1 Changelist

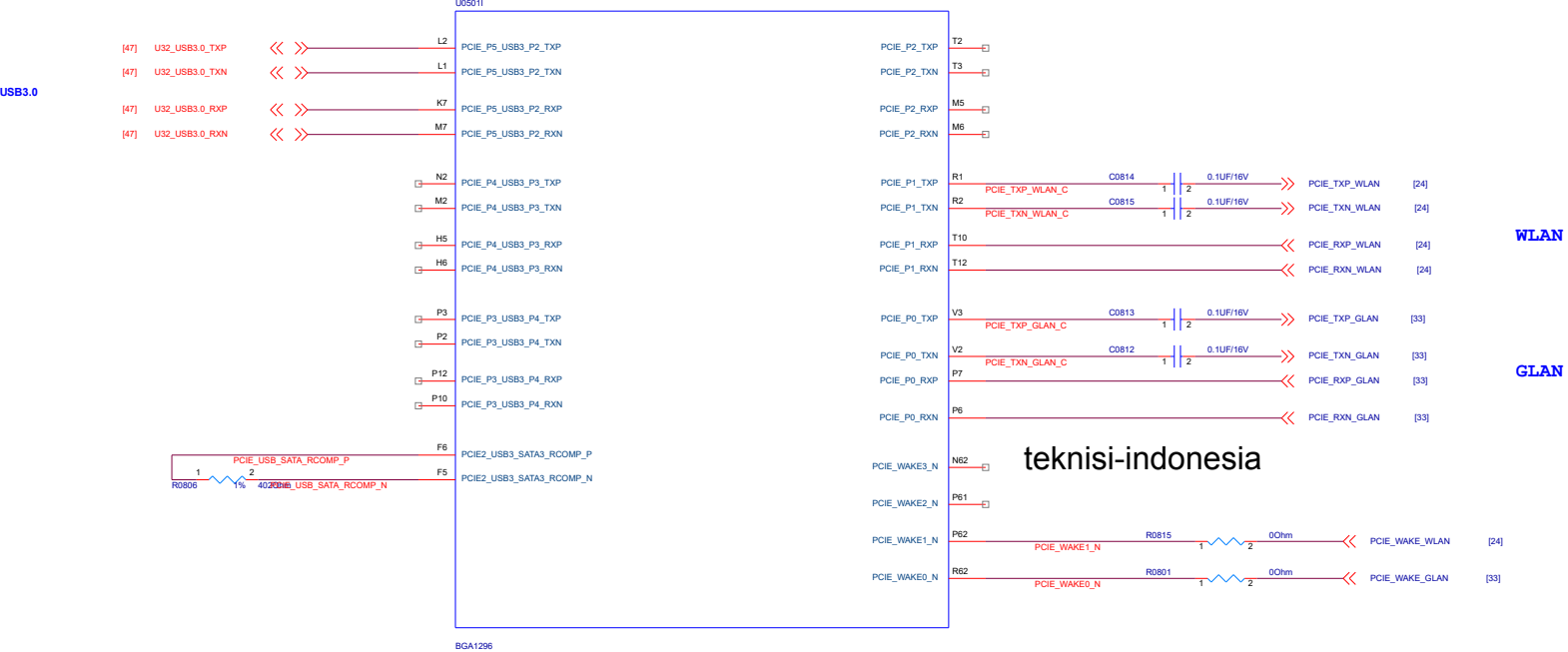
17. uP1902 (2nd) rename from Power team to EE
18. SMB1 PU to +3VA_EC
19. Change EC.11 Power to +3VA_EC page.30
20. Add C4402 and Change R4311 for EA test
21. Add R3003 for AC detect
22. R1499 change size (from 0201 to 0402) and value (from 10K to 100K)
23. Add R3108 for damping
24. R1120 @, R1121 N/A
25. R1747, R1761 @
26. Change SD card RC
27. Remove eDP LANE2, 3
28. HDMI EDID Modify for EA
29. Modify EMMC_RST_N from EDS (EDS 2.0)
30. Page 84 PRFB8401 -> 20Kohm
31. Page 88 PQ8805,PC8803,PC8809,PC8817 @
32. Page 89 PRS8901 -> 20mhom PC8909 -> 0.1uF/25V
33. RN4406 -> 10K for EDID
34. Modify EMI ESD

Project Name E402NA		Rev 1.1
Title : Change Note		
Size E	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 3 of 99	

CHA: On board DDR3L



ASUS	Project Name: E402NA	Rev 1.1
Title : CPU_DDR		
Size: E	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 5 of 99	

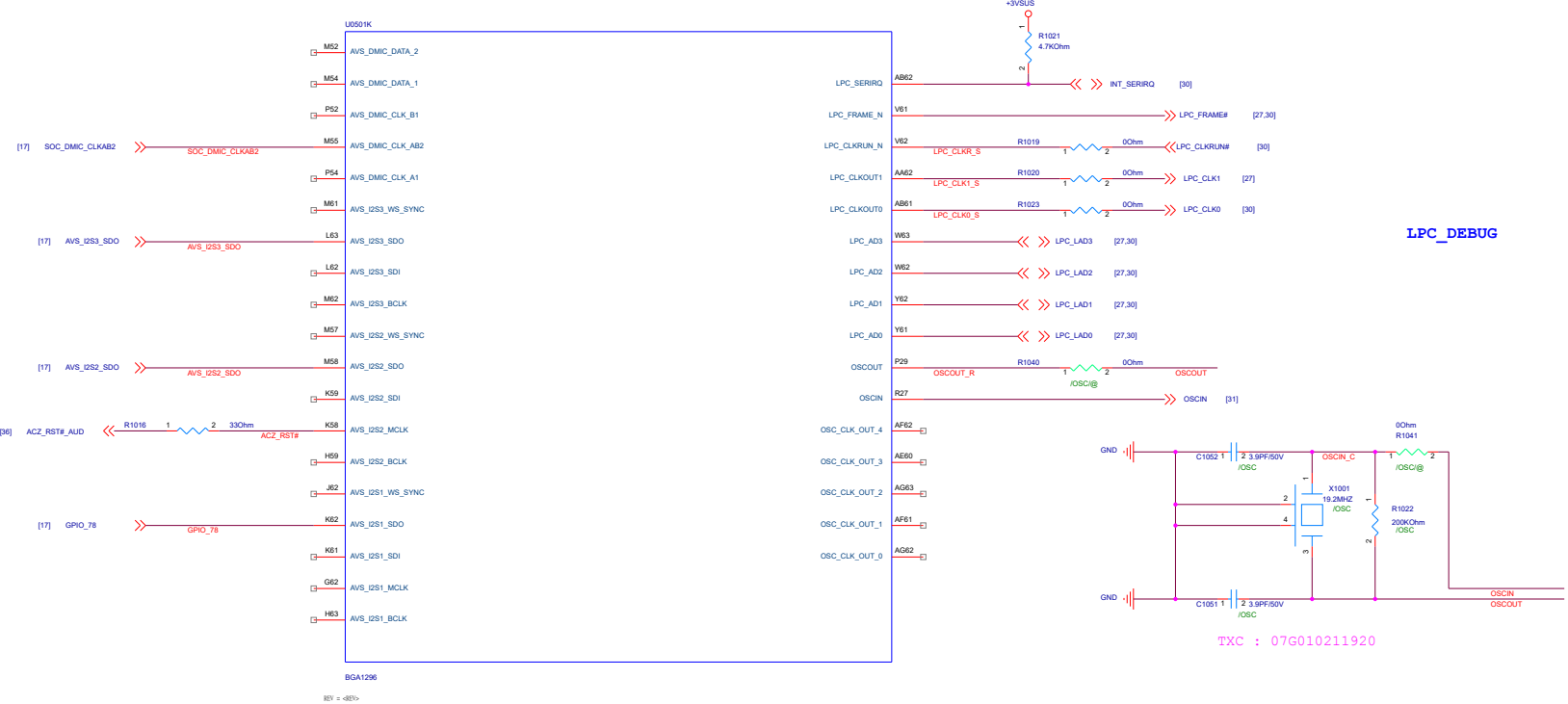


REV = <REV>

Project Name: E402NA			Rev: 1.1
Title : CPU_I2C&CLK&GPIO			
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016		Sheet 8 of 99	

REV = <REV>

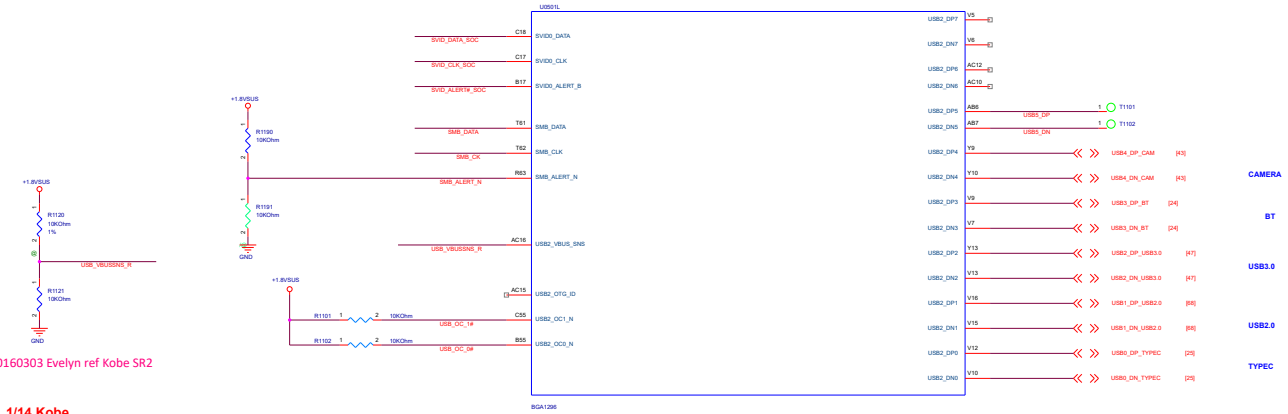
ASUS	Project Name: E402NA	Rev: 1.1
Title : Block Diagram		
Size: B	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 9 of 99	



ASUS	Project Name: E402NA		Rev: 1.1
Title : CPU_USB&UART			
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 10 of 99		

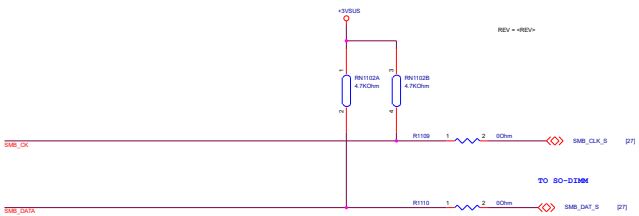
	USB 2.0
0	Type C
1	USB2.0
2	USB3.0
3	BT
4	Camera

	USB 3.0
USB3_0	Type C -->USB 3.0 Port A
USB3_1	Type C -->USB 3.0 Port B
USB3_2	USB 3.0 Port
USB3_3	

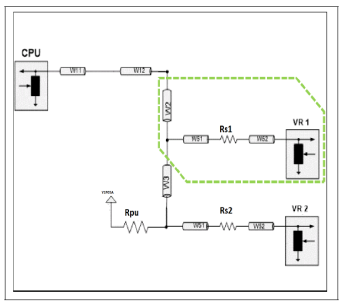


20160303 Evelyn ref Kobe SR2

1/14 Kobe
USB2 PORT0 --> OC0
USB2 PORT1~7 --> OC1



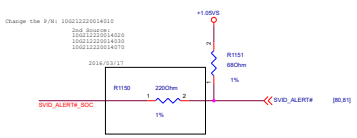
20160303 Evelyn ref Kobe SR2

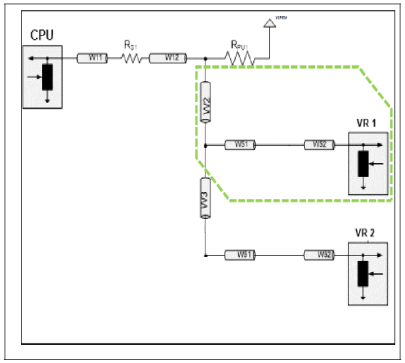


NOTE: If less than 2 VR is used, remove the first device from the topology.Example:If 1 VR is used, remove from W2 to VR1 from the topology (as illustrated by dotted line).

SVID0_CLK Design Specification

VR Options	Specifications
Total Trace Length (max)	15.6"
Series Resistor, R_{s1}/R_{s2}	95 Ω ±5%
Pull up Resistor, R_{pu}	85 Ω ±5%
Number of Vias	No restriction

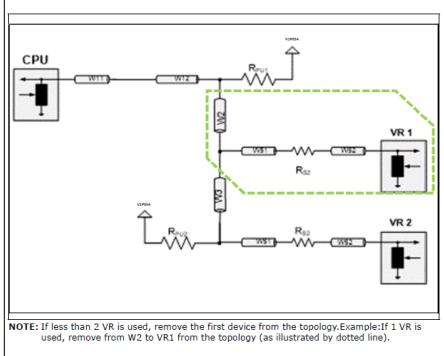




NOTE: If less than 2 VR is used, remove the first device from the topology.Example:If 1 VR is used, remove from W2 to VR1 from the topology (as illustrated by dotted line).

SVID0_ALERT_N Design Specifications

VR Options	Specifications
Total Trace Length (max)	15.6"
Series Resistor, R_{s1}	220 Ω ±5%
Pullup Resistor, R_{pu1}	68 Ω ±5%
Number of Vias	No restriction

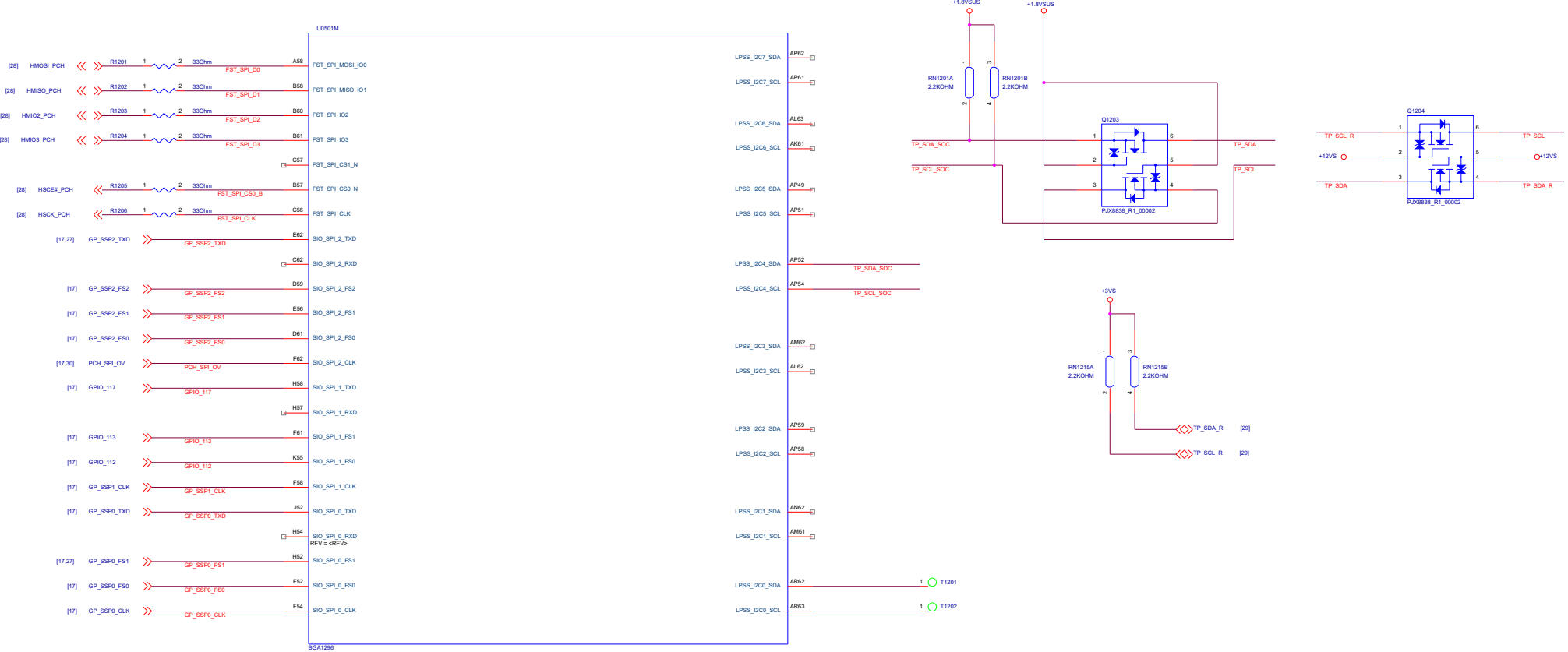


NOTE: If less than 2 VR is used, remove the first device from the topology.Example:If 1 VR is used, remove from W2 to VR1 from the topology (as illustrated by dotted line).

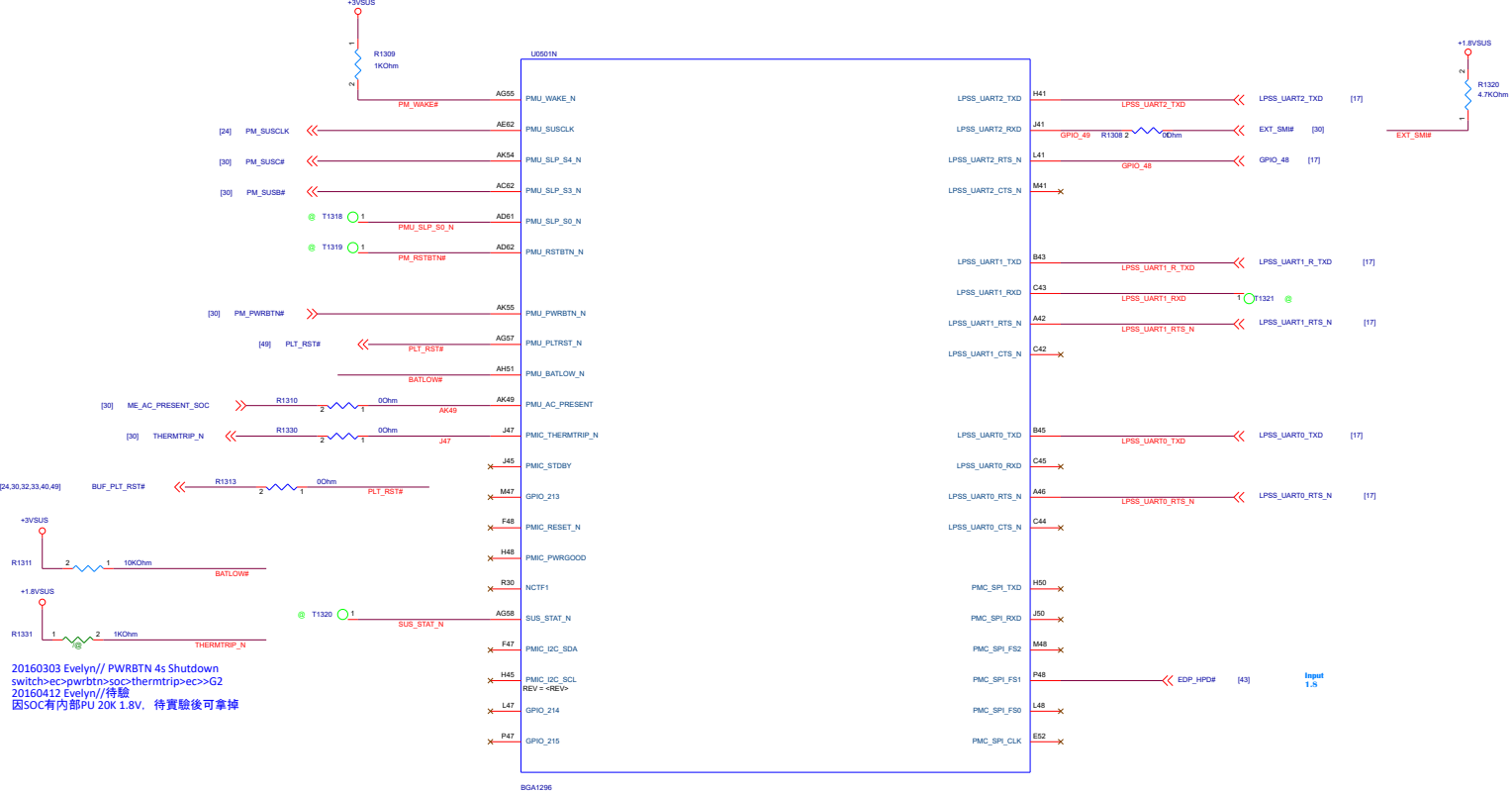
SVID_DATA Design Specifications

VR Options	Specifications
Total Trace Length (max)	15.6"
Series Resistor: R_{s1} ; R_{s2}	20 Ω ±5%
Pullup Resistor, R_{pu1} ; R_{pu2}	170 Ω ±5%
Number of Vias	No restriction

ASUS	Project Name: E402NA		Rev: 1.1
Title : CPU_POWER			
Size: Custom	Dept.: PC2-RD1-Sjs2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 11 of 99		



ASUS	Project Name: E402NA		Rev: 1.1
Title : CPU_GND			
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 12 of 99		



20160303 Evelyn// PWRBTN 4s Shutdown
switch>ec>pwrbtn>soc>thermtrip>ec>>G2
20160412 Evelyn//待驗
因SOC有內部PU 20K 1.8V，待實驗後可拿掉

Project Name: E402NA			Rev: 1.1
Title : CPU_STRAP			
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 13 of 99		

Intel HDA #560733 remove after QS
E402NA remove at PR

HD Audio

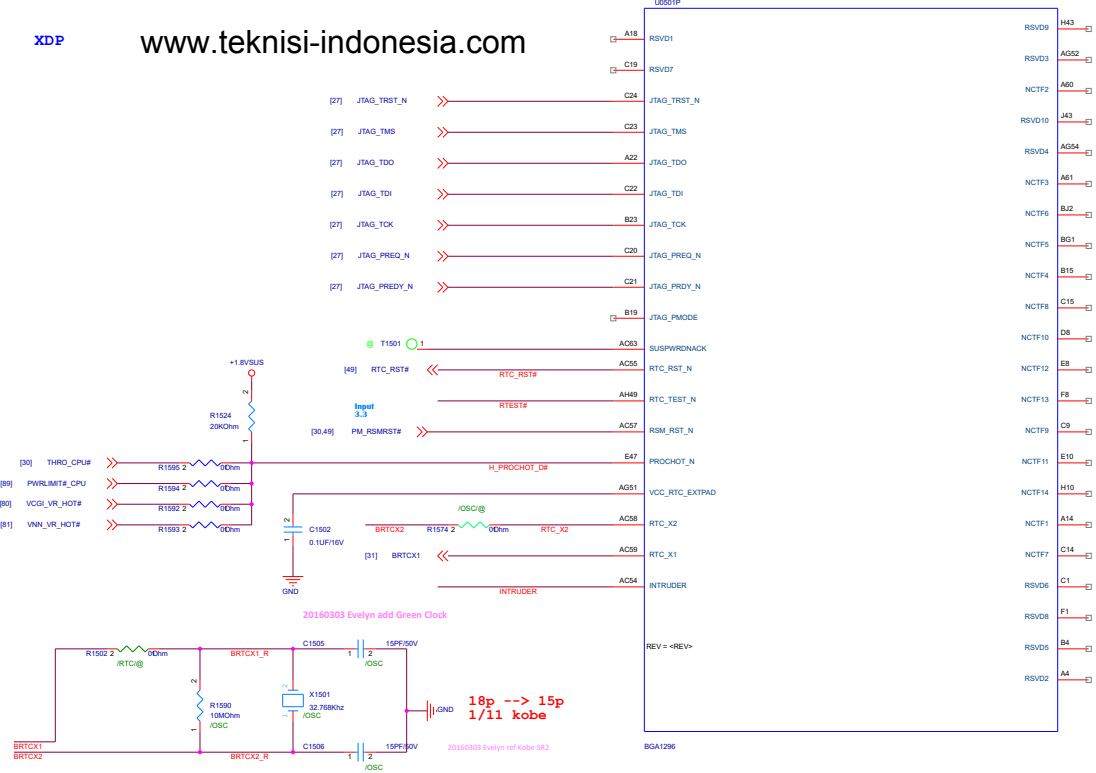
BT&WLAN與BIOS確認

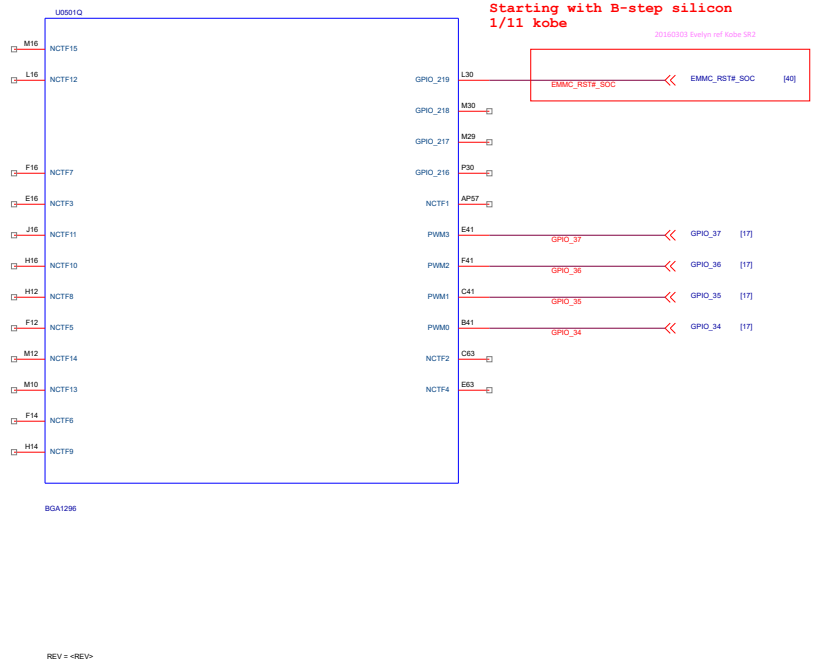
MIPI-60 reserved test point
20160418 Evelyn

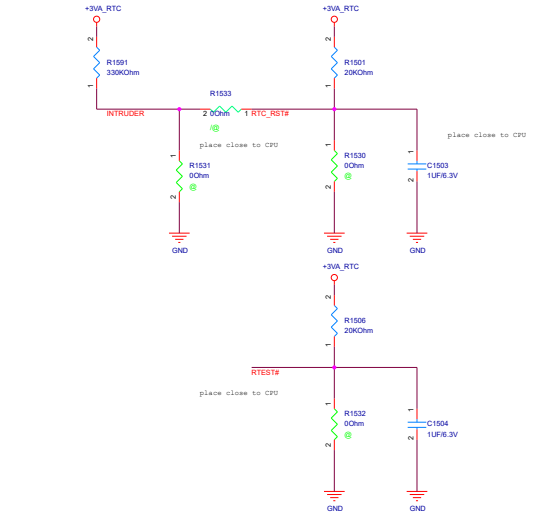
DRAM Strap

PCBID0	PCBID1	PCBID2	
0	0	0	HYNIX 4GB 03000-00053600
0	0	1	MICRON 4GB 03000-00053700
0	1	0	HYNIX 2GB
0	1	1	MICRON 2GB
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Project Name	E402NA		Rev.
Title :	CPU_Display&Camera		
Size:	Dept.:	PCJ RD1 &Jul KE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016		Sheet	of



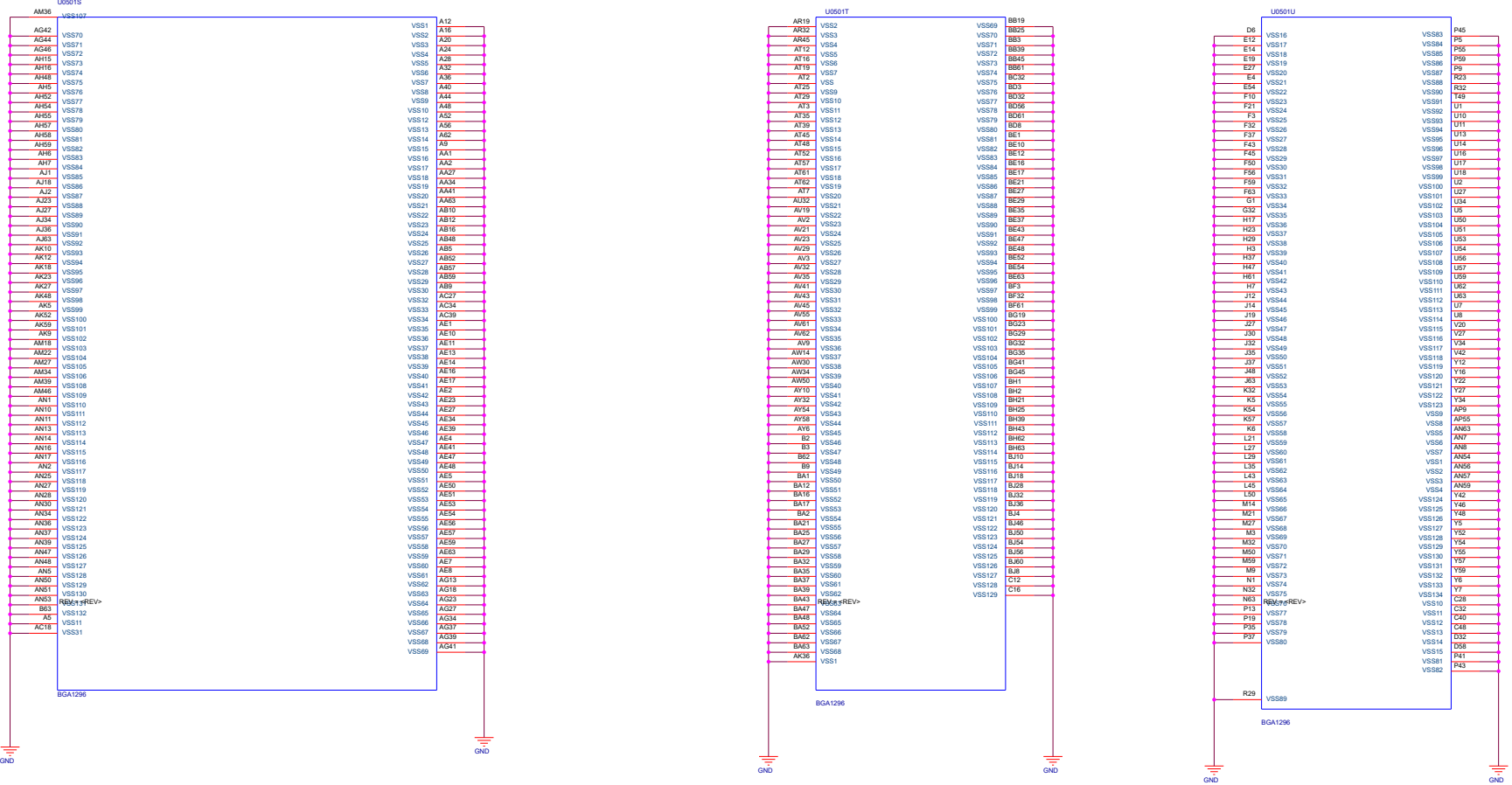




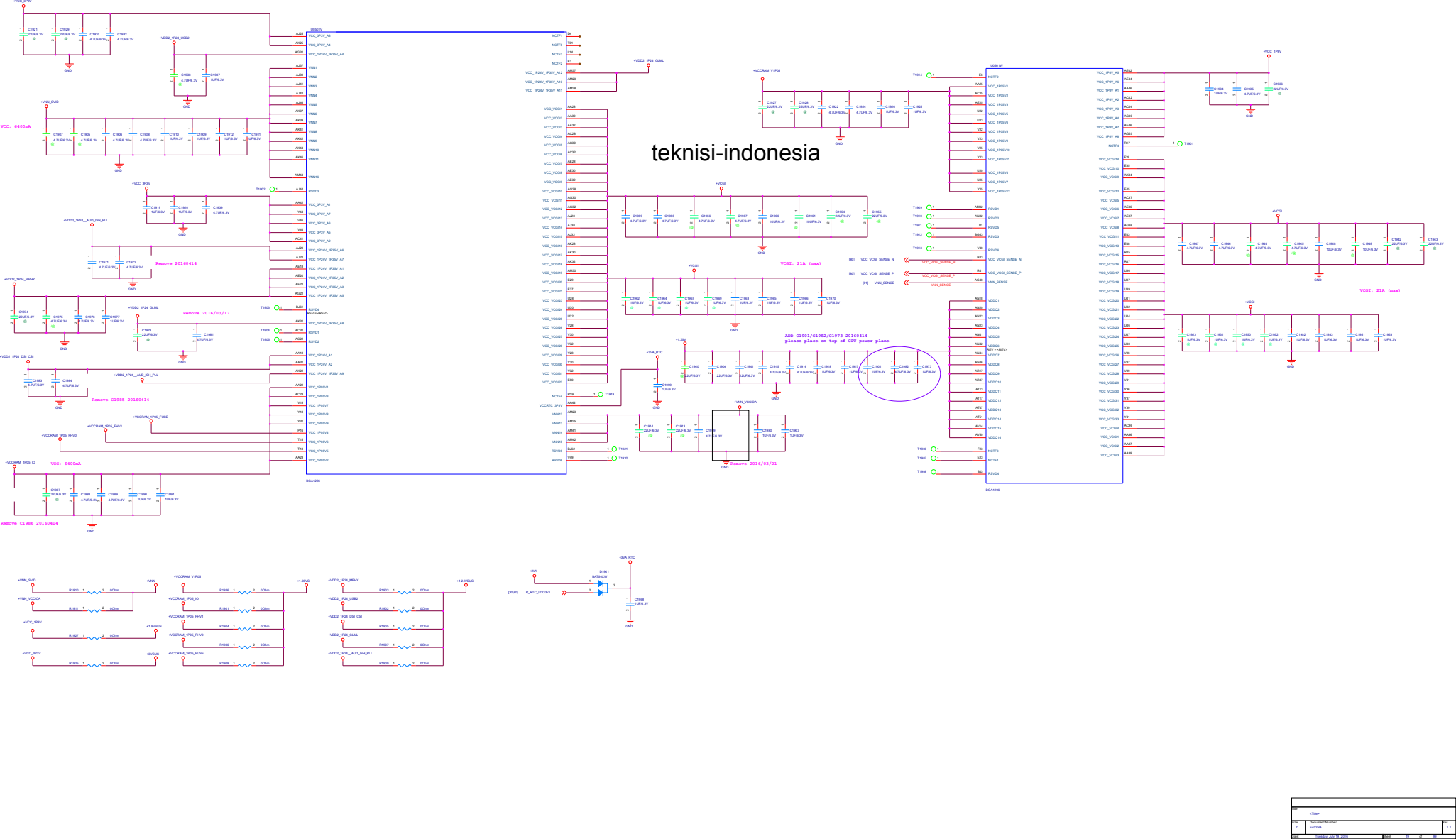
ASUS	Project Name: E402NA		Rev: 1.1
Title : CPU_Display&Camera			
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 15 of 99		

Change the P/N: 10G212113014070
2nd Source:10G212113014010
10G212113014020
10G212113014030
2016/03/17

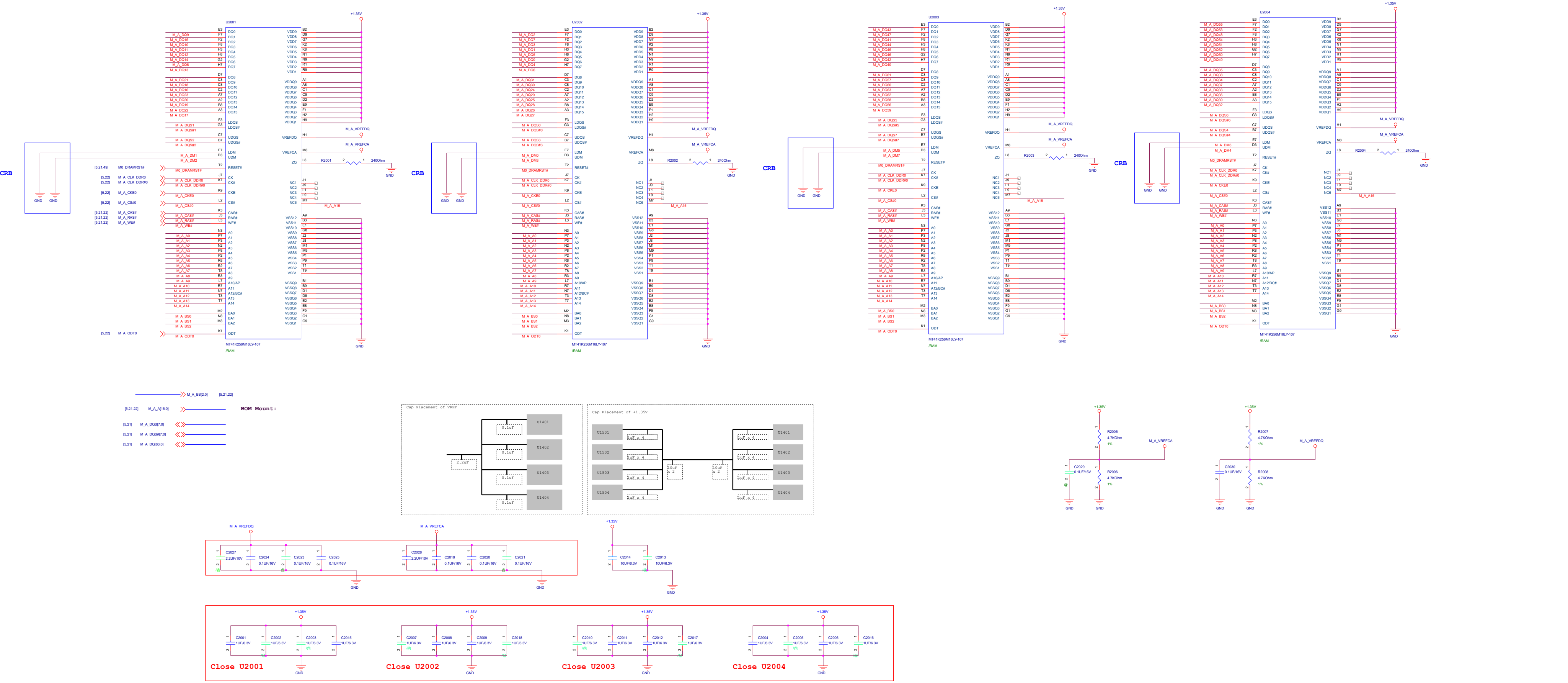
Project Name: E402NA		Rev: 1.1
Title : CPU_Display&Camera		
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 16 of 99	



Title	<Title>	
Size: C	Document Number: E402NA	Rev: 1.1
Date: Tuesday, July 19, 2016	Sheet 18 of 99	


teknisi-indonesia
VCC: 6400mA
Remove 20160414
Remove 2016/03/17
Remove C1985 20160414
Remove C1986 20160414
VCCGI: 21A (max)
ADD C1901/C1982/C1973 20160414
please place on top of CPU power plane
Remove 2016/03/21
BGA1296

Main Board



X450UMA

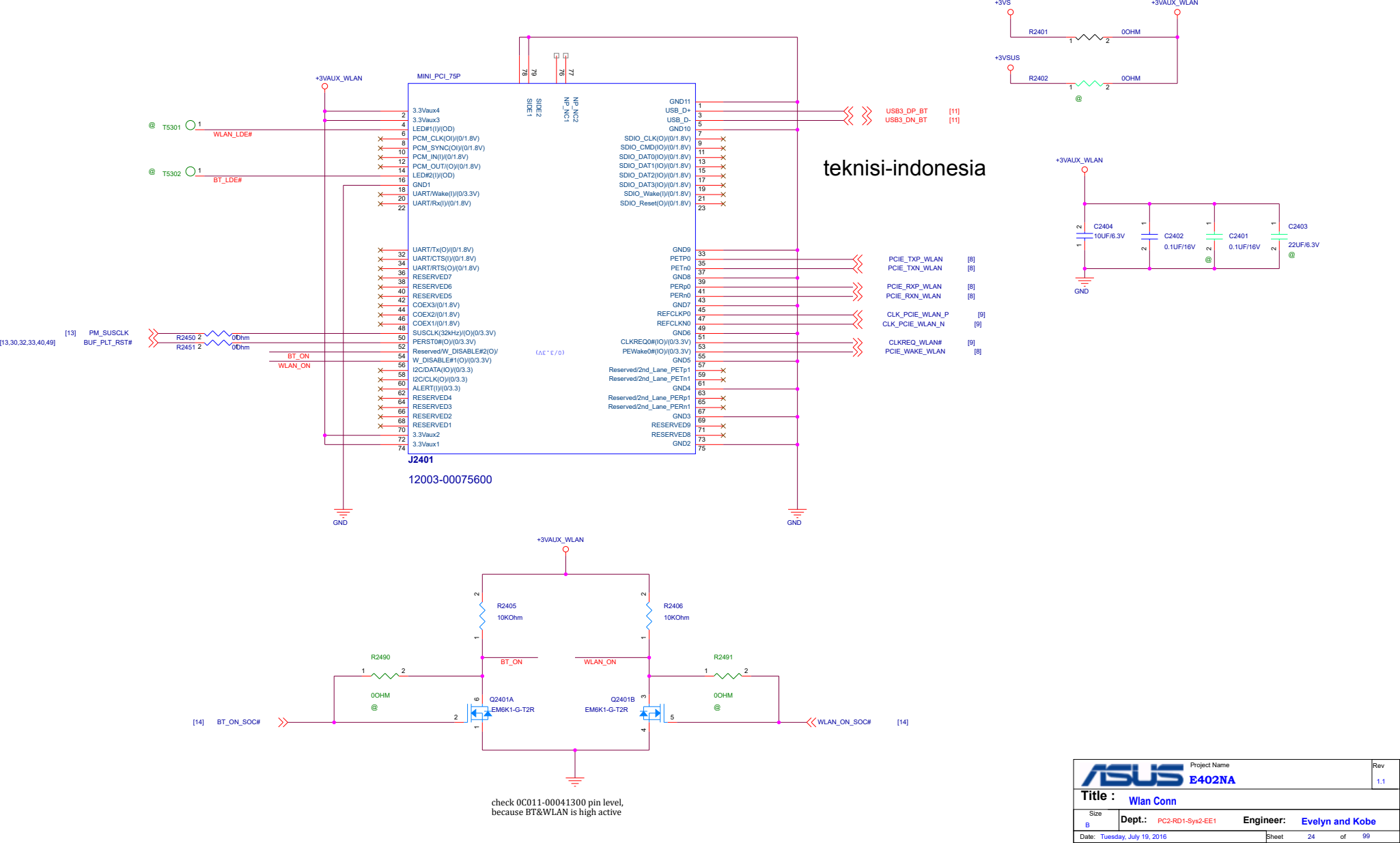
MEM_On-Board CH.B

Evelyn and Kobe

PC2-RD1-Sys2-EE1

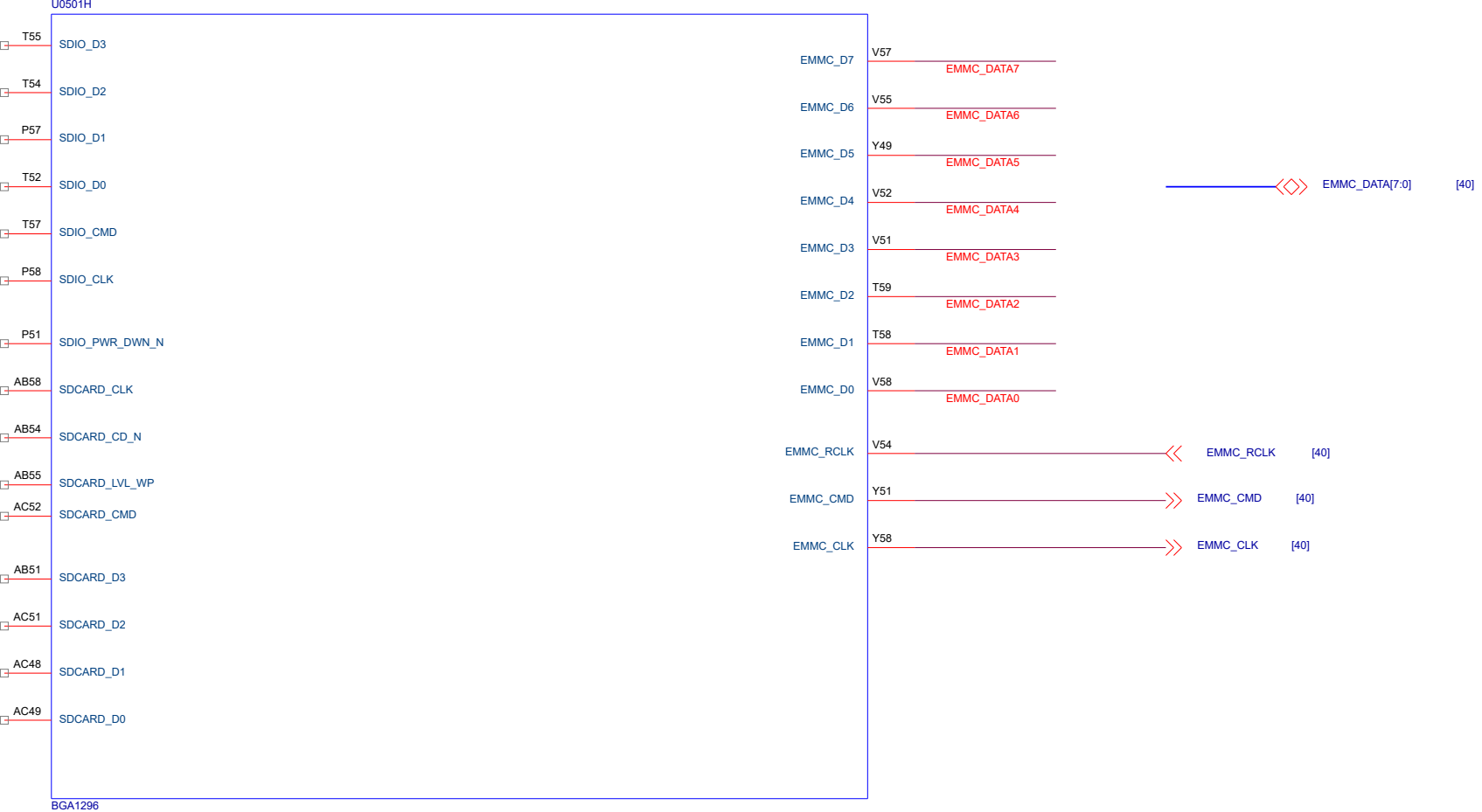
E402NA

Tuesday, July 19, 2016



check 0C011-00041300 pin level,
because BT&WLAN is high active

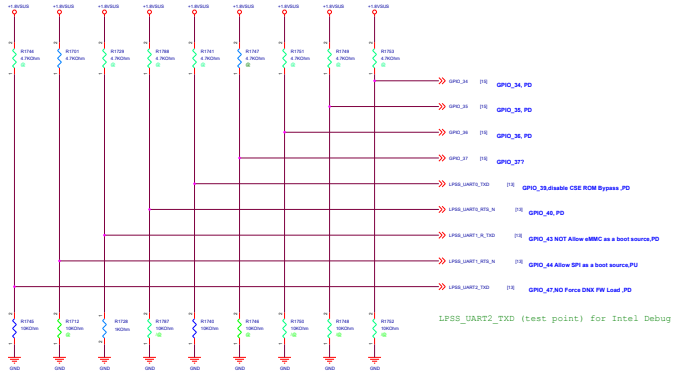
ASUS	Project Name: E402NA		Rev: 1.1
Title : Wlan Conn			
Size: B	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 24 of 99		

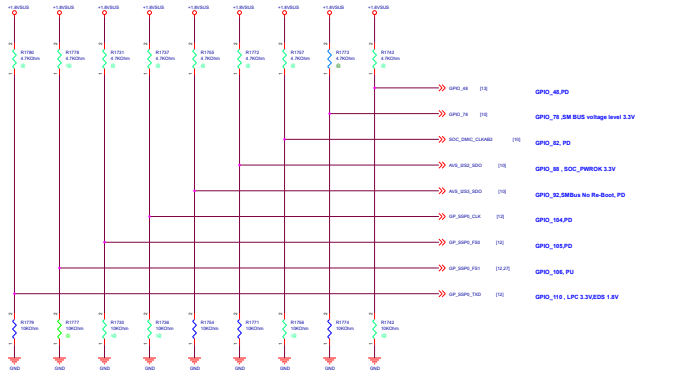


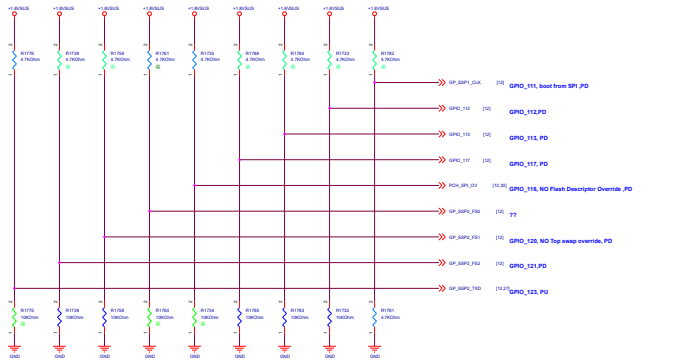
REV = <REV>

ASUS	Project Name: E402NA	Rev: 1.1
Title : CPU_SATA&PCIE&SPI&HDA		
Size: B	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 7 of 99	

CPU Strap





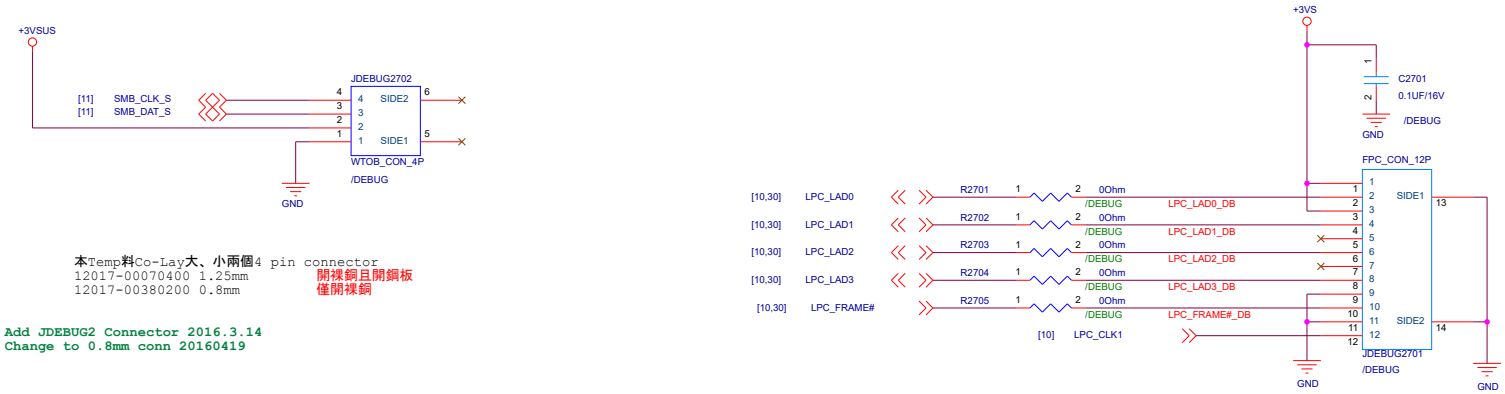


4/8 Kobe
change to PU,EC OD pin

Table 2-36. Hardware Straps

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_34	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_35	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_36	VCC_1P24V_1P35V_A voltage selection	20K PD	1 = 1.35V 0 = 1.24V (default) ***Note:*** This strap will only be used for B-step. For A-step this rails should only be set at 1.24V
GPIO_39	Enable CSE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) ***Note:*** Apollo Lake supports TXE3.0 (this is also called CSE) ***Note:*** This strap tells CSE (TXE3.0) to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of CSE (TXE3.0) before the first patch point this strap enabled the platform tell CSE (TXE3.0) to bypass the ROM causing the issue and go to the patch space instead.
GPIO_40	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_43	Allow eMMC as a boot source	20K PU	1=enable (default) 0=disable
GPIO_44	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable
GPIO_47	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) ***Note:*** DnX: Download and Execute ***Note:*** This strap is a recovery strap for corrupted FW image. This strap will force CSE (TXE3.0) to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB. CSE (TXE3.0) can do it for BIOS part of FW, but if CSE FW itself is corrupted we need this strap.
GPIO_48	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_82	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_88	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_92	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Platforms should strap this LOW. Functionality is handled by the PMC.
GPIO_104	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_105	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_106	RSVD	20K PU	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_111	Boot BIOS Strap (BBS)	20K PU	1 = Do not boot from SPI (default) 0 = Boot from SPI
GPIO_118	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override ***Note:*** This strap enables the platform to override security features in the SPI.
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_117	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_123	RSVD	20K PD	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_112	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_113	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_120	Top swap override	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_121	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

LPC DEBUG PORT

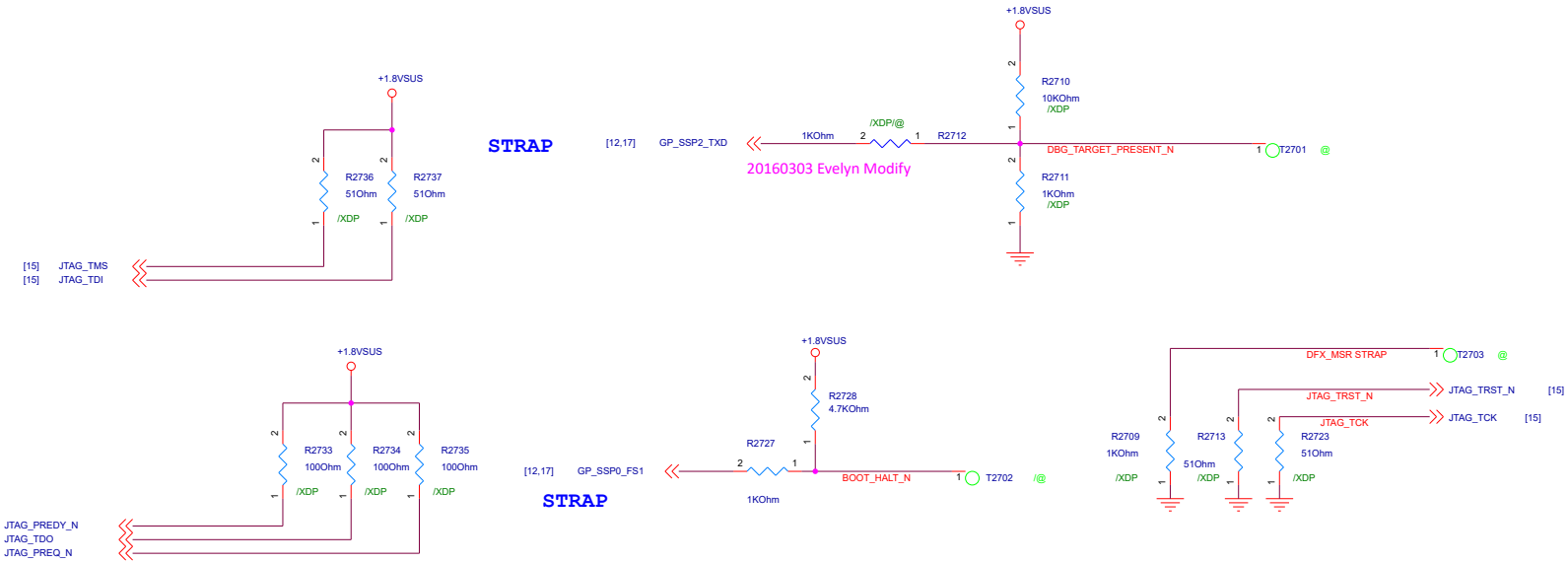


本Temp料Co-Lay大、小兩個4 pin connector
12017-00070400 1.25mm 開裸銅且開銅板
12017-00380200 0.8mm 僅開裸銅

Add JDEBUG2 Connector 2016.3.14
Change to 0.8mm conn 20160419

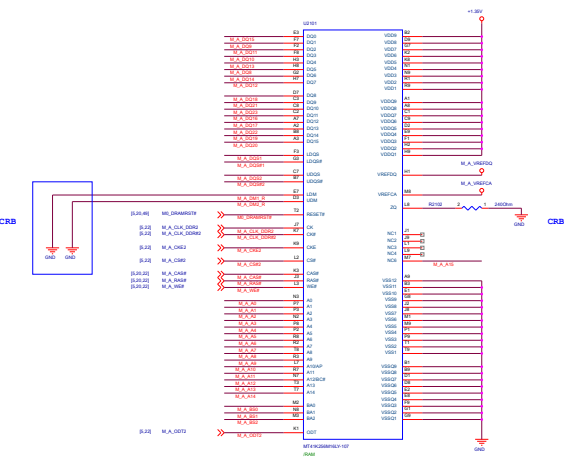
20160418 reserved by Evelyn
XDP Reserved circuit

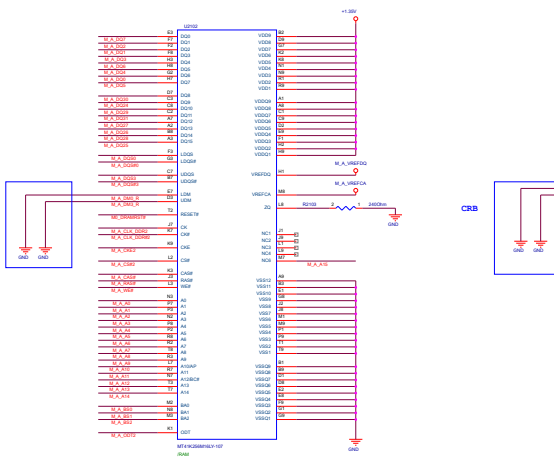
MIPI-60

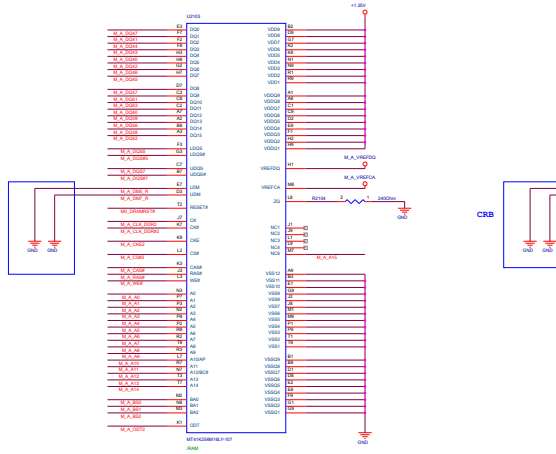


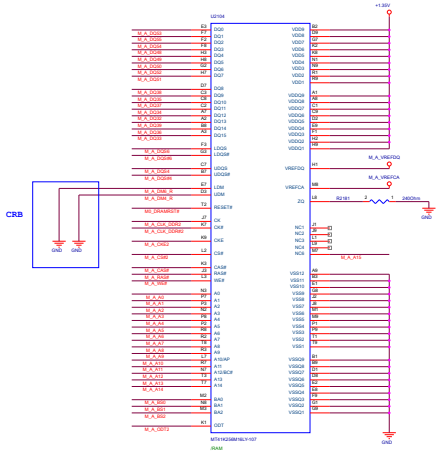
Project Name: E402NA		Rev: 1.1
Title : Debug		
Size: B	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 27 of 99	

Main Board

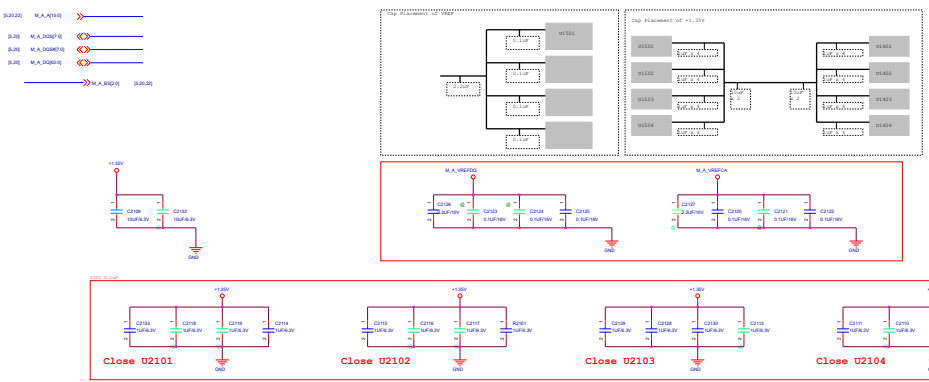


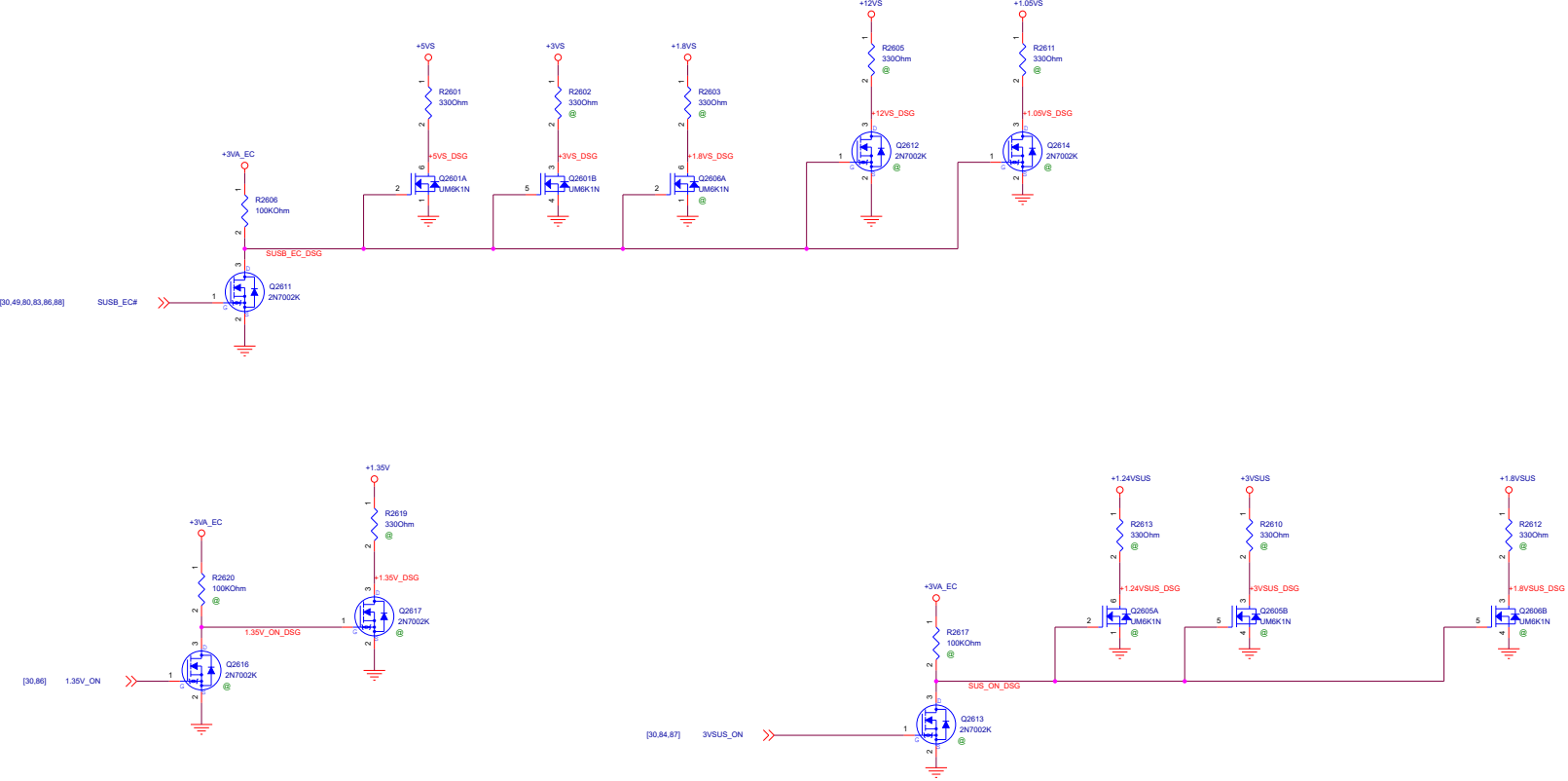






BOM Mount:

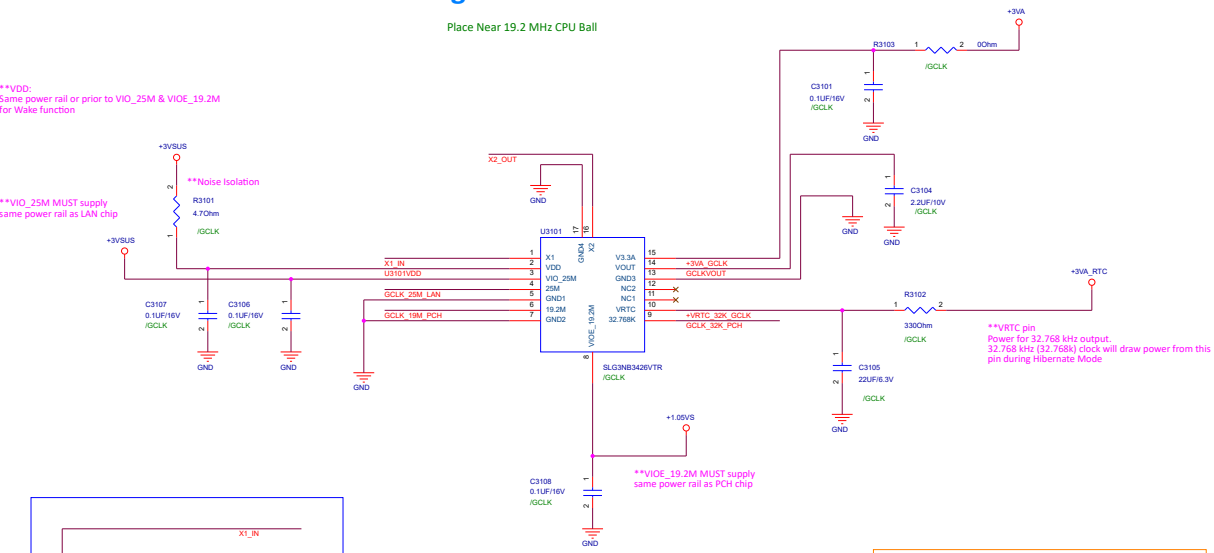


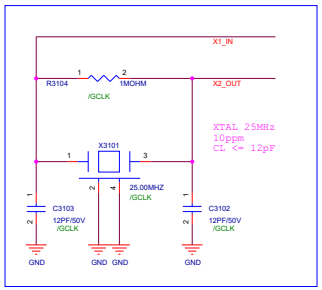


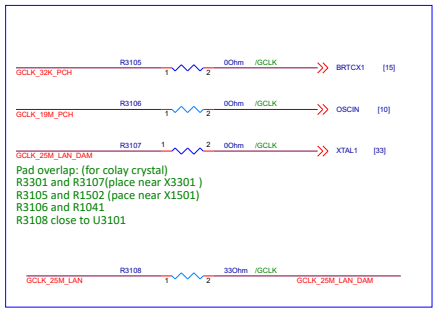
ASUS	Project Name: E402NA		Rev: 1.1
Title : Discharge			
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 26 of 99		

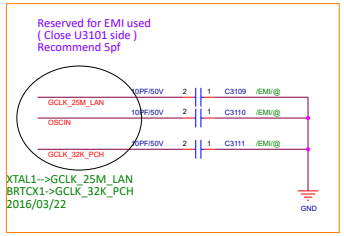
Silego Green CLK

Place Near 19.2 MHz CPU Ball



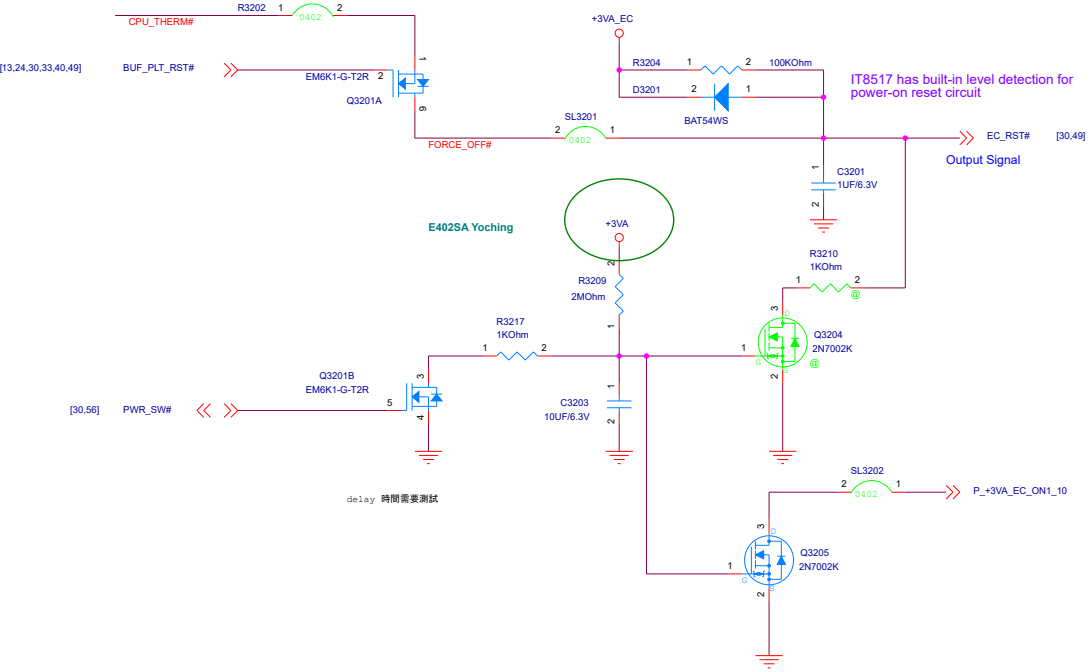


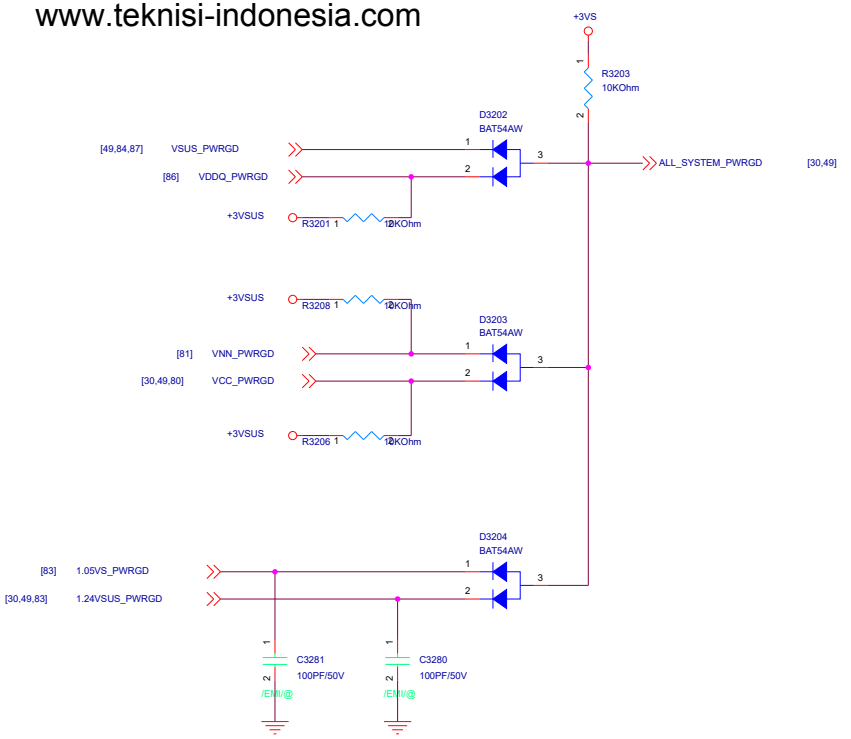




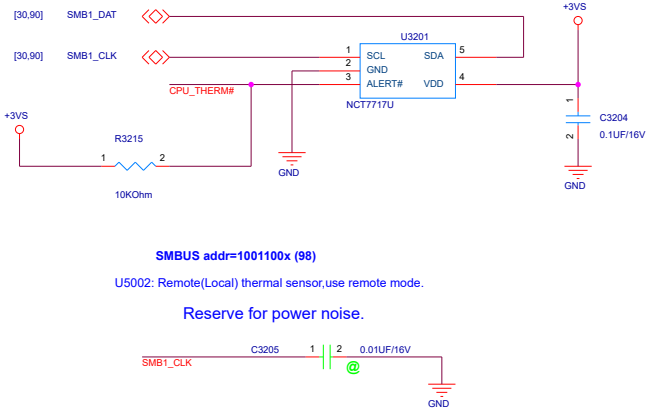
Project Name: E402NA		Rev: 1.1
Title : NA		
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 31 of 99	

Thermal Policy





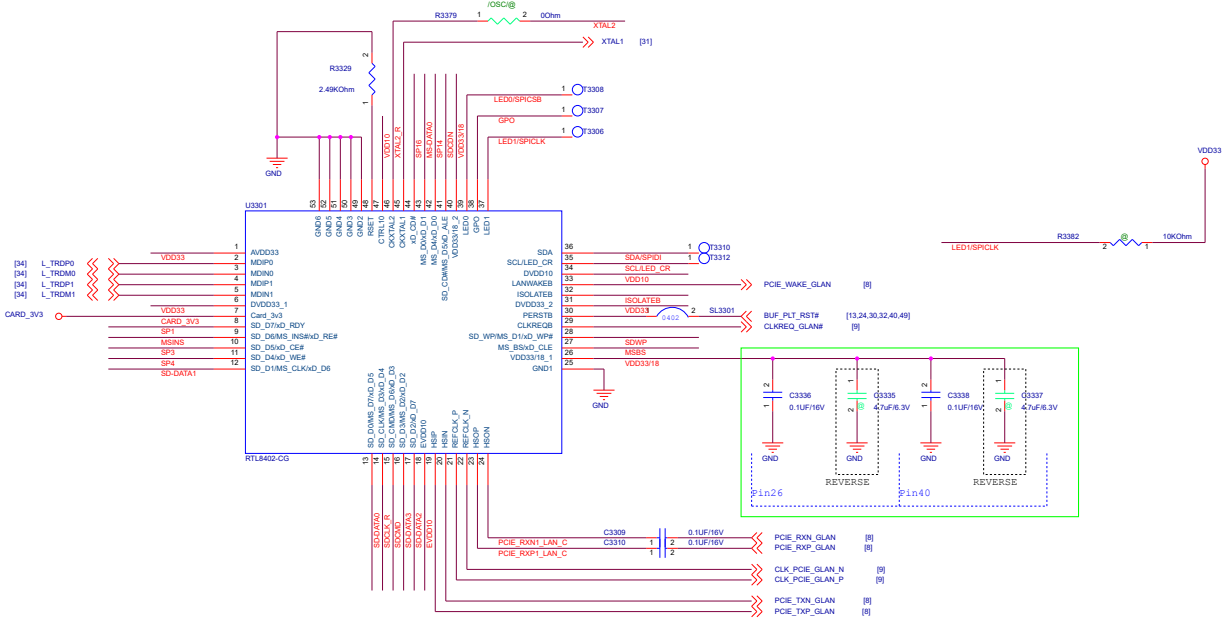
CPU Thermal Sensor



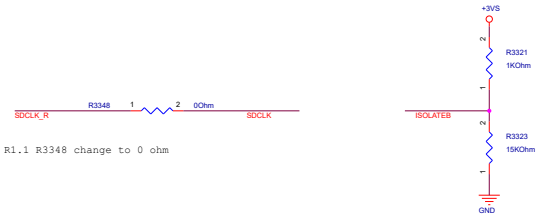
Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
10 mils
----------OTHER SIGNALS
Avoid FSB,Power

ASUS	Project Name: E402NA		Rev: 1.1
Title : PW_GD			
Size: B	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 32 of 99		



LAN



8.8.4. Auxiliary Signal Timing Parameters

Table 28. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power Stable to PERSTB Inactive	100	-	ms
$T_{PERST-CLK}$	REFCLK Stable before PERSTB Inactive	100	-	µs
T_{PERST}	PERSTB Active Time	100	-	µs
$T_{PERSTB-RTD}$	PERSTB Rising Time Duration	10	-	ms
T_{FAIL}*	Power Level Invalid to PWRGD Inactive	-	500	ns
T_{PWRON}	3.3Vaux Power On Time	1	-	ms

Note 1: T_{FAIL} means 500 ns (maximum) from the power rail going out of specification (exceeding the specified tolerances by more than 500 mV). Refer to PCI Local Bus Specification rev. 3.0 for further information. T_{FAIL} can be disregarded when implementation and timing of T_{FAIL} will not affect any LAN functions.

Note 2: The ISOLATEB pin should follow the behavior of the 3.3V main power waveform.

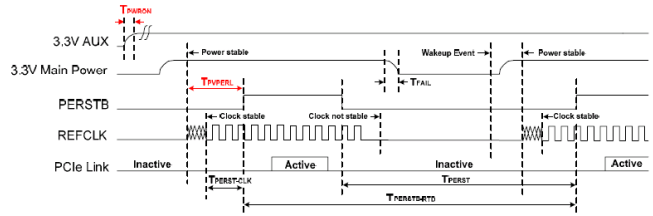


Figure 17. Auxiliary Signal Timing

6. Power Sequence

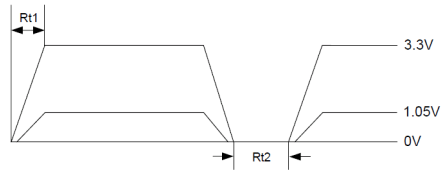


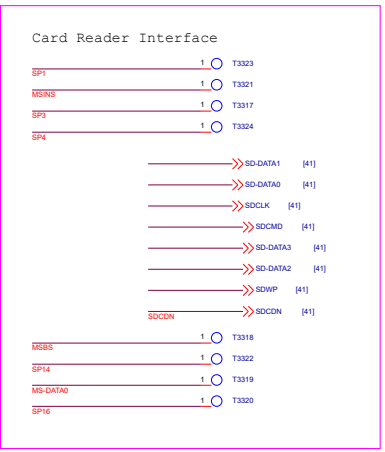
Figure 21. Power Sequence

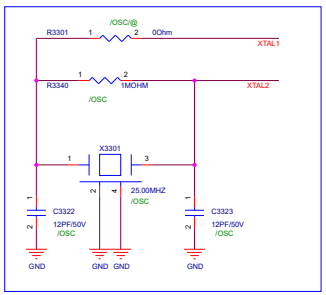
Table 1. Power Sequence Parameter

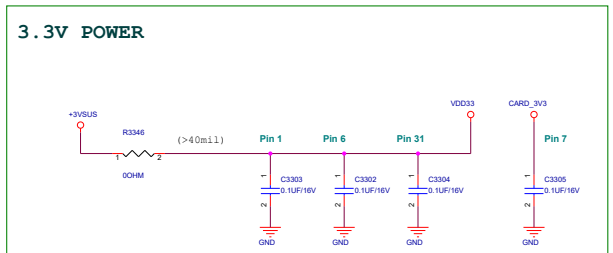
Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time	1	-	100	ms
Rt2	3.3V Off Time	50	-	-	ms

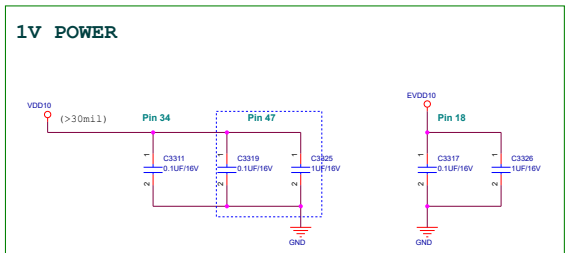
Note 1: The RTL8402 does not support fast 3.3V rising. The 3.3V rise time must be controlled over 1ms.

Note 2: If there is any action that involves consecutive ON/OFF toggling of the LDO regulator source (3.3V), the designer must make sure the OFF state of both the LDO regulator source (3.3V) and output (1.05V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 50ms.

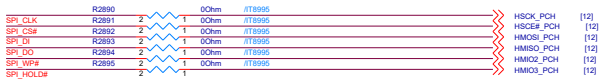




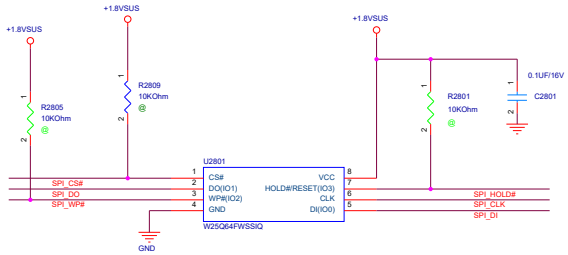




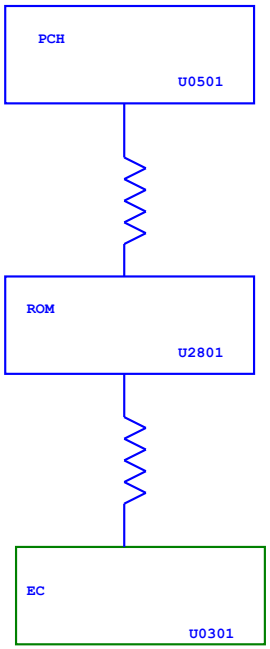
IT 8995



Close to CPU



Q Mode料號:
05006-00012500 FLASH WINBOND W25Q64FWSSIQ 64Mb



<Variant Name>

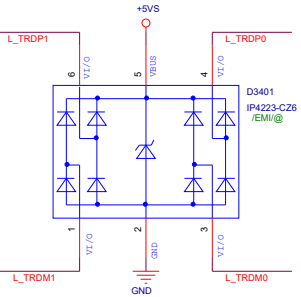
PCH_SPI ROM,OTH

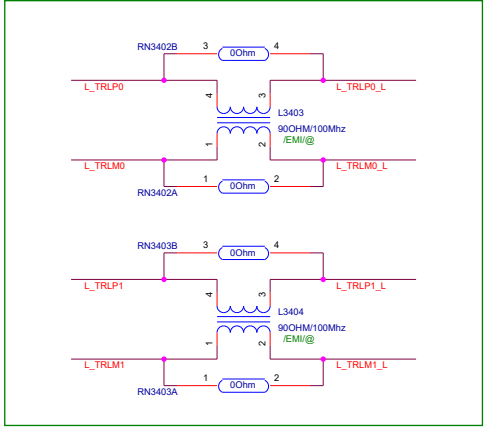
PC2-RD1-Sys2-EE1

Evelyn and Kobe

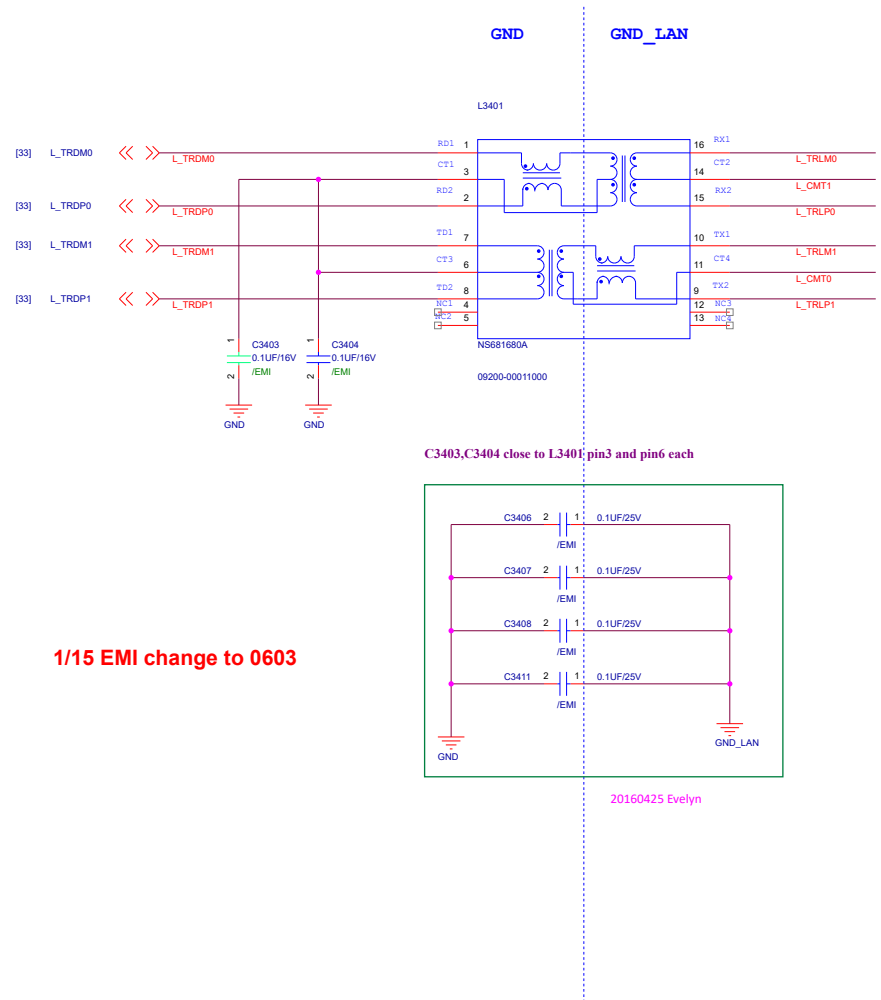
C E402NA 1.1

Tuesday, July 19, 2016 28 99





X405MA Change L3403, L3404 size



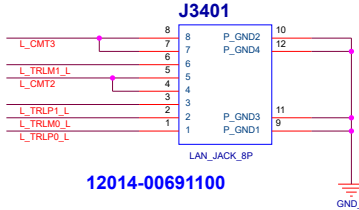
C3403,C3404 close to L3401 pin3 and pin6 each

20160425 Evelyn

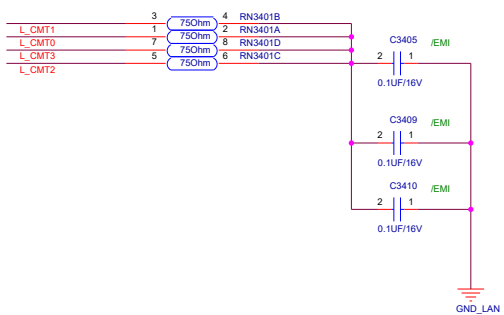
1/15 EMI change to 0603

Transformer RJ-45端
LAN GND

For RJ-45



12014-00691100



<Variant Name>

LAN-RJ45

Evelyn and Kobe

PC2-RD1-Sys2-EE1

C E402NA 1.1

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Project Name

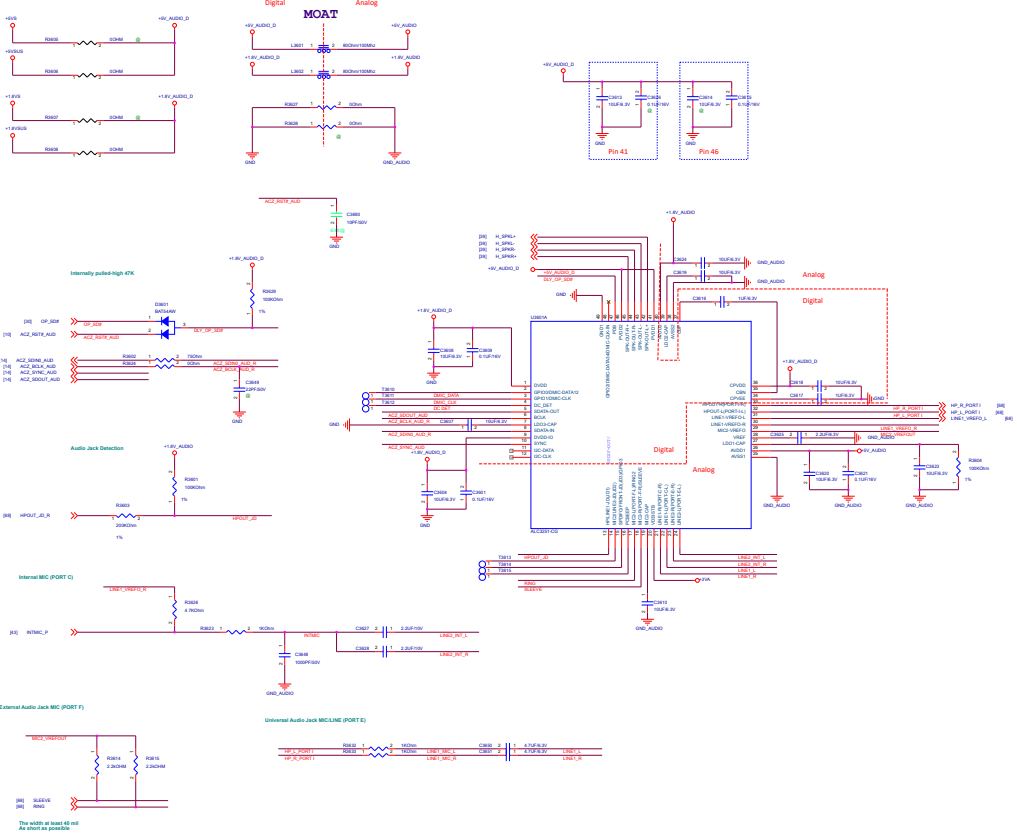
E402NA

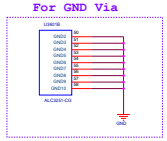
Rev 1.1

Title : MIC_SPEAKER

Size	Dept.:	Engineer:
C	PC2-RD1-Sys2-EE1	Evelyn and Kobe

Date: Tuesday, July 19, 2016





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	Project Name **E402NA**	Rev 1.1

Title :

Size B	**Dept.:** PC2-RD1-Sys2-EE1	**Engineer:** Evelyn and Kobe

Date: Tuesday, July 19, 2016	Sheet	37	of 99

<Variant Name>

NGFF KEY-B

Evelyn and Kobe

PC2-RD1-Sys2-EE1

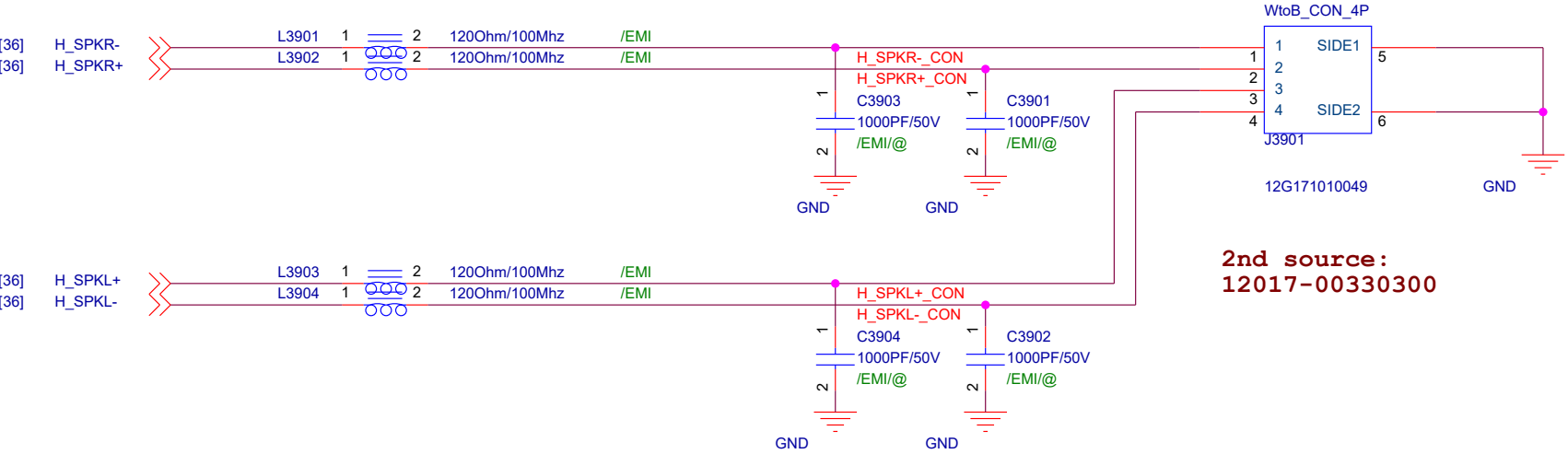
C

E402NA

1.1

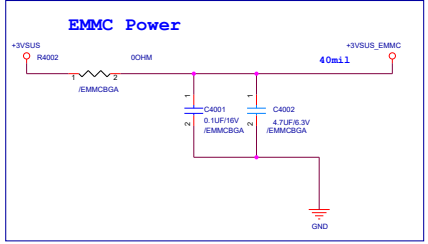
Audio Speaker

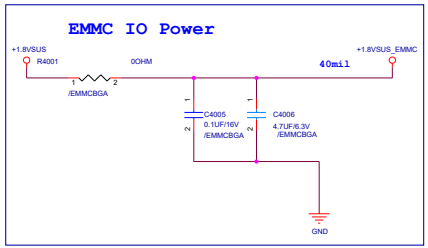
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-RSpeaker
4 ohm : 40mil
Speaker 8 ohm : 20mil

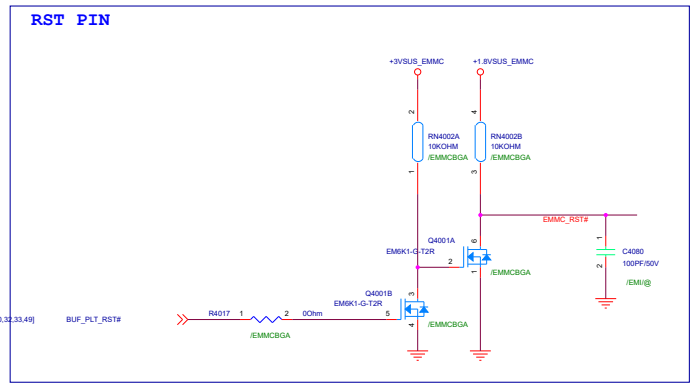


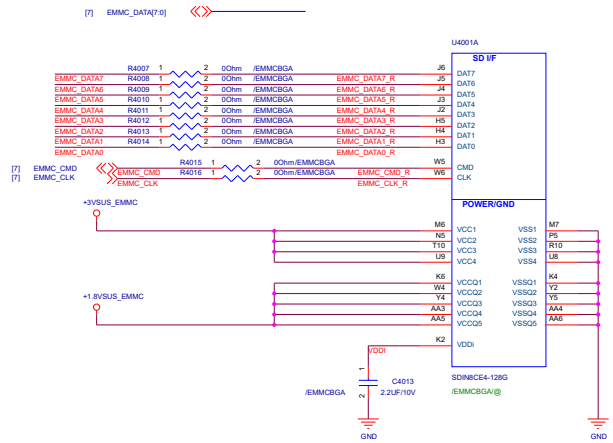
2nd source:
12017-00330300

ASUS	Project Name: E402NA	Rev: 1.1
Title : NA		
Size: A	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 39 of 99	

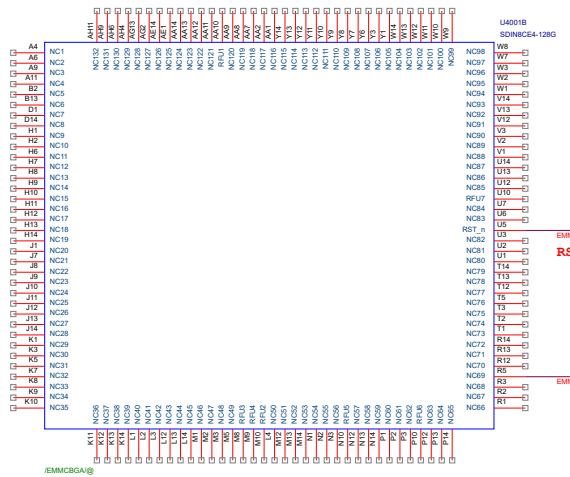




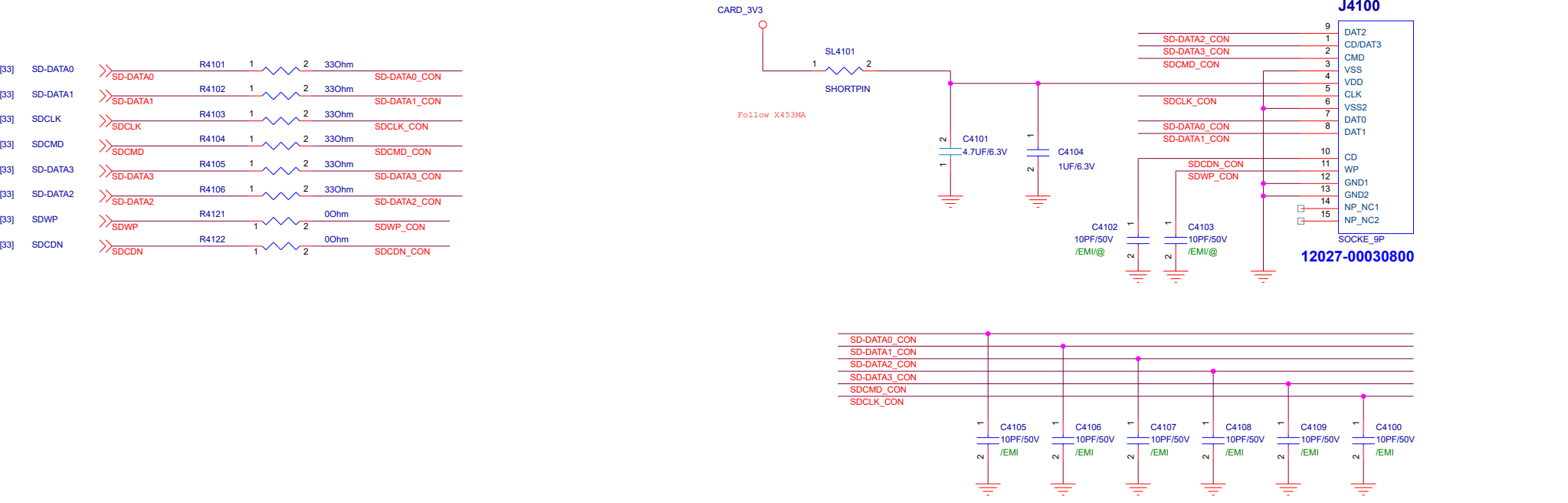




Coupling cap should be connected with VDDi and Vsm as closely possible.



FBGA-169 Colay FBGA-153



<Variant Name>

CB_****

Evelyn and Kobe

PC2-RD1-Sys2-EE1

B

E402NA

1.1

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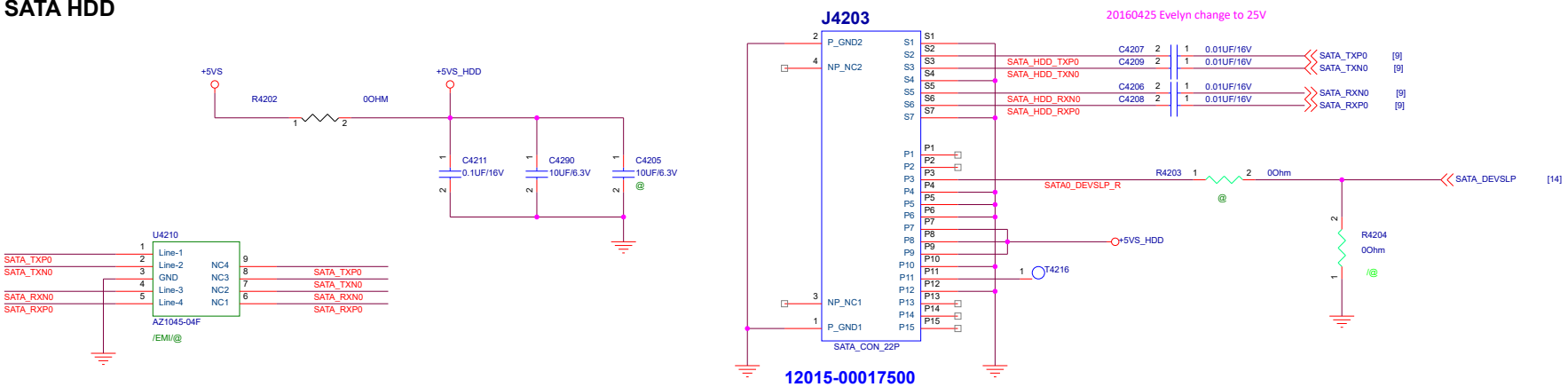
99

SATA HDD



SATA ODD

4/8 Kobe Remove ODD PART

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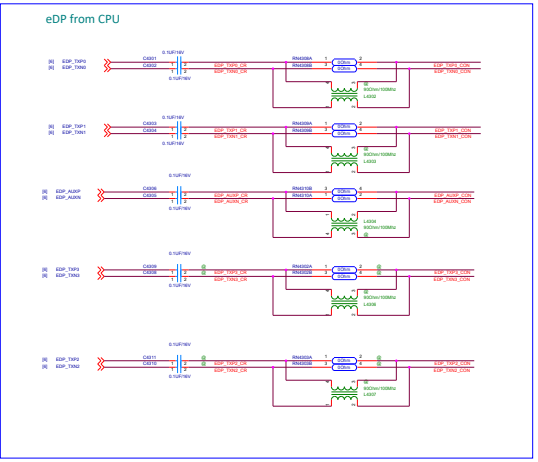
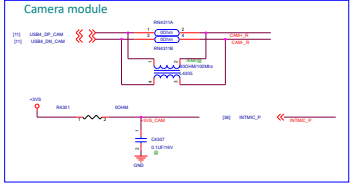
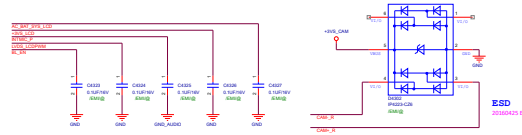
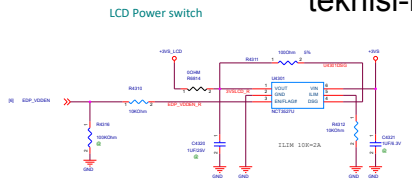
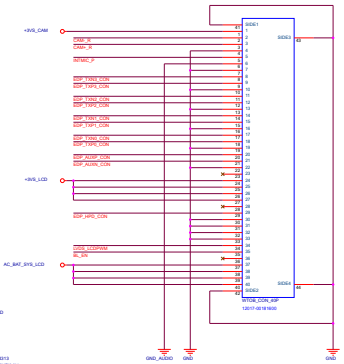
Size: B	Document Number: E402NA		Rev: 1.1
Date: Tuesday, July 19, 2016	Sheet 42 of 99		

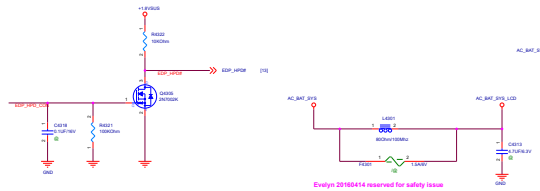


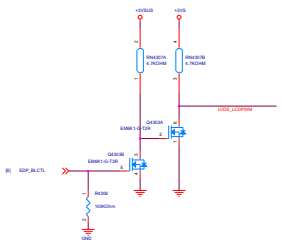


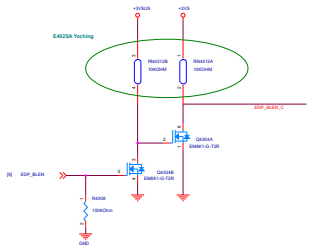


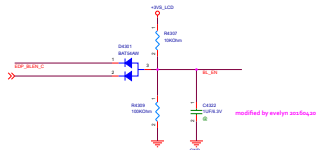




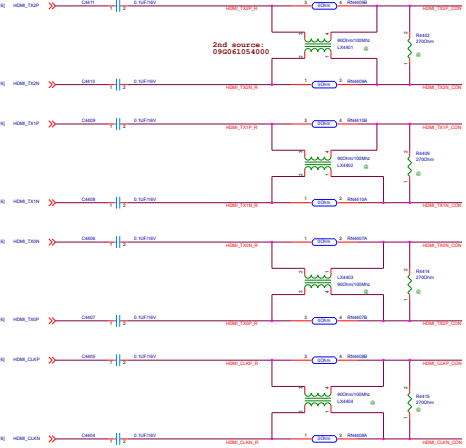


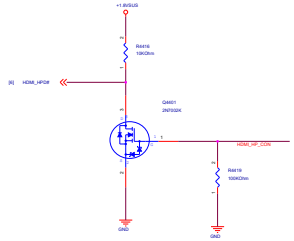


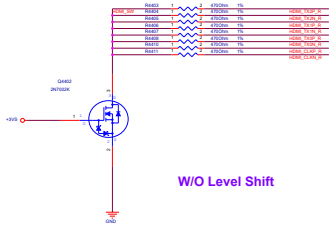


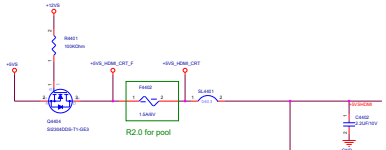


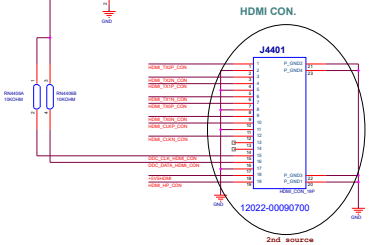
ASUS	Project Name: E402NA		Rev: 1.1
Title :	EDP cc, LVDS Conn		
Size: D	Dept.: PCI-ROI-Sys1-KE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016		Sheet 43 of 69	

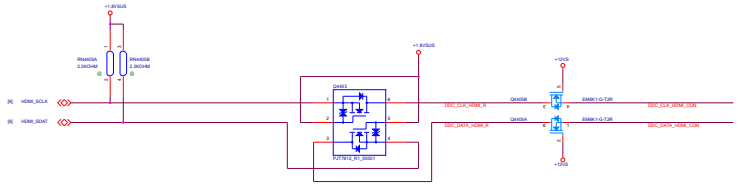


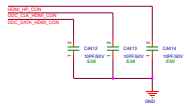






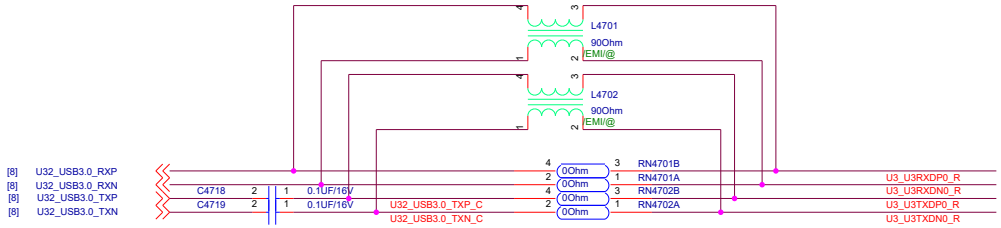




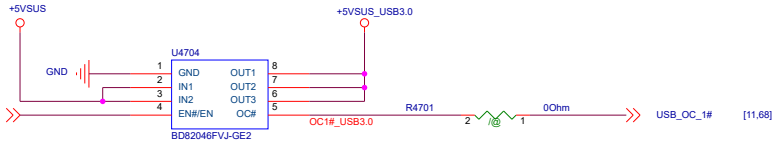


ASUS	Project Name: E402NA		Rev: 11
Title : HDMI			
Size: B	Dept.: PCI-RD1-Sy2-SE1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 09, 2019	Sheet 44 of 66		

USB3.0 port0

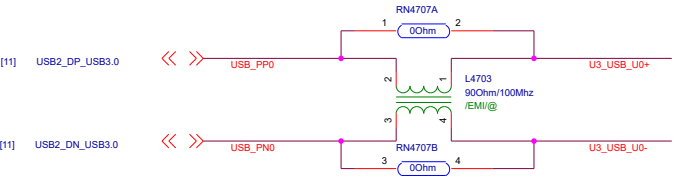


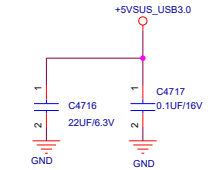
POWER



20160414 Evelyn Modify

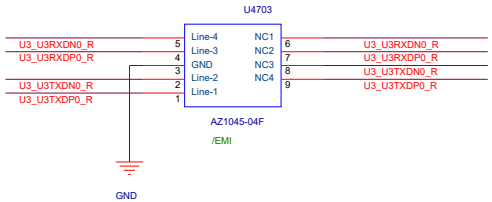
USB2.0 port0

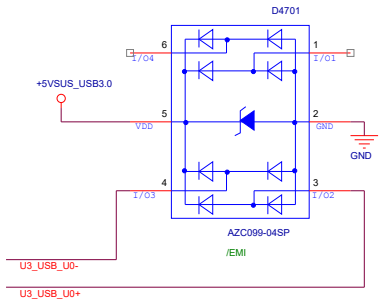




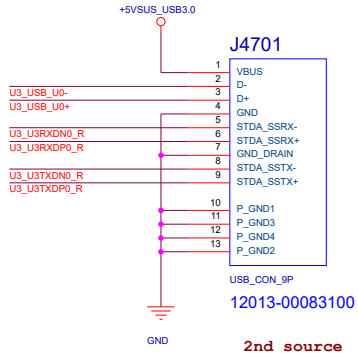
near J2301

ESD





ESD



12013-00083100

2nd source

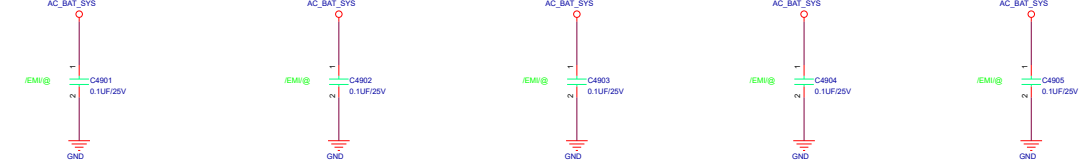
ASUS	Project Name: E402NA	Rev: 1.1
Title : USB Conn		
Size: B	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 47 of 99	

	Project Name **E402NA**	Rev 1.1

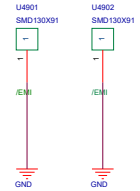
Title : NA

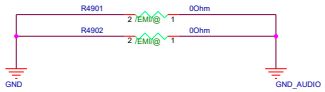
Size		
A	**Dept.:** PC2-RD1-Sys2-EE1	**Engineer:** Evelyn and Kobe

Date: Tuesday, July 19, 2016	Sheet	48	of 99

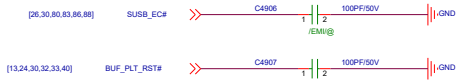


(2447.22 4541.71) (1498.10 4732.12) 1167.07 2277.28 2209.94 882.88 3545.75 660.24

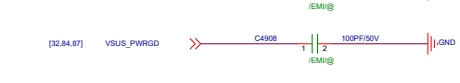




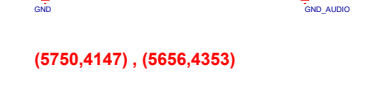
(5750,4147) , (5656,4353)



(3743, 5236) (844, 3248) (4456, 2355) (4643, 2316)



(4472, 2585) (3606,4946) (4484,2631) top layer (2838,1478) top layer (4079,1434)



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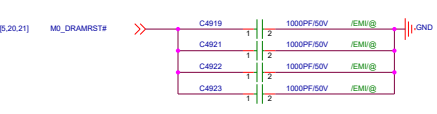
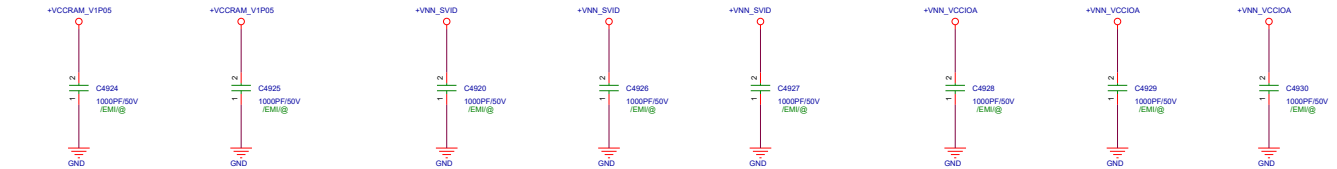


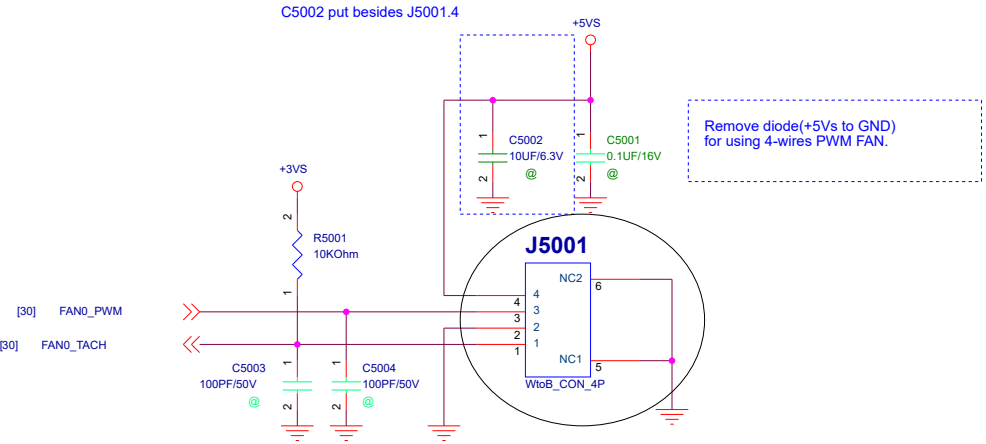


(3630 1985) (3640 1960) (2790 3215) (3005 3215) (2880 2855) (2575 3260) (2570 2915) (2540 2710)

ASUS	Project Name: E402NA	Rev: 1.1
Title : EMI		
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer: Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 49 of 99	

PWM Fan

2015/04/27 Evelyn



12G171000047

2nd: 12017-00080400

<Variant Name>

FAN_Fan & Sensor

Evelyn and Kobe

PC2-RD1-Sys2-EE1

B E402NA 1.1

Tuesday, July 19, 2016 50 99

<Variant Name>

XDD_eMMC

Evelyn and Kobe

PC2-RD1-Sys2-EE1

C

E402NA

1.1

Tuesday, July 19, 2016

51

99

	Project Name **E402NA**	Rev 1.1

Title : NA

Size		
A	**Dept.:** PC2-RD1-Sys2-EE1	**Engineer:** Evelyn and Kobe

Date: Tuesday, July 19, 2016	Sheet	52	of 99

Project Name

E402NA

Rev 1.1

Title : NA

Size	Dept.:	Engineer:
A	PC2-RD1-Sys2-EE1	Evelyn and Kobe

Date: Tuesday, July 19, 2016

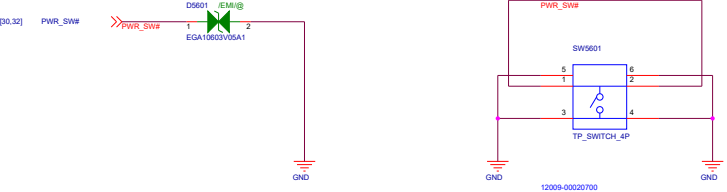
	Project Name **E402NA**	Rev 1.1
Title : NA		teknisi-indonesia
Size A	**Dept.:** PC2-RD1-Sys2-EE1	**Engineer:** Evelyn and Kobe
Date: Tuesday, July 19, 2016	Sheet 54 of 99	

	Project Name **E402NA**	Rev 1.1

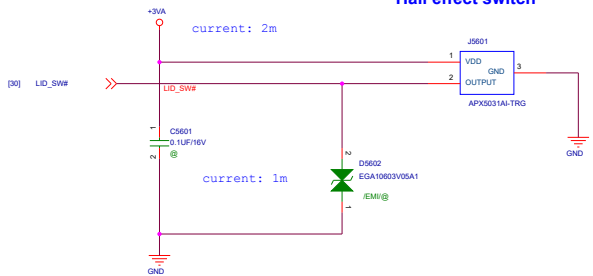
Title : NA

Size		
A	**Dept.:** PC2-RD1-Sys2-EE1	**Engineer:** Evelyn and Kobe

Date: Tuesday, July 19, 2016	Sheet	55	of 99



Hall effect switch



B-to-B Connector

Evelyn and Kobe

PC2-RD1-Sys2-EE1

A

E402NA

1.1

Tuesday, July 19, 2016

58

99

Project Name

E402NA

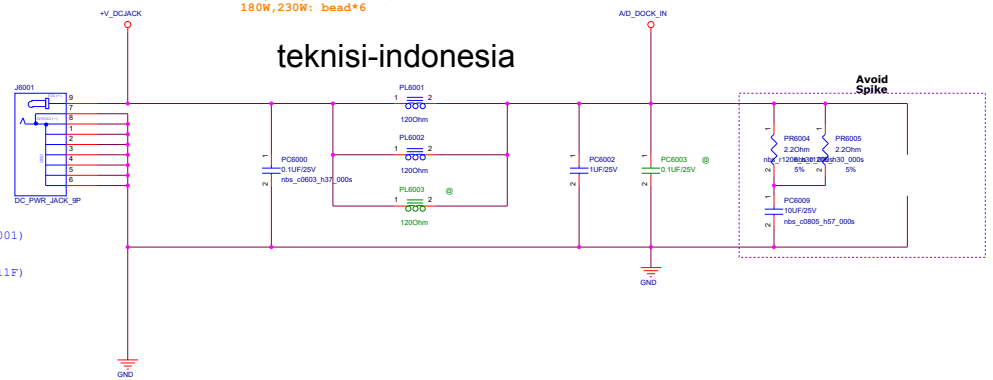
Rev 1.1

Title : IO_SWITCH

Size	Dept.:	Engineer:
B	PC2-RD1-Sys2-EE1	Evelyn and Kobe

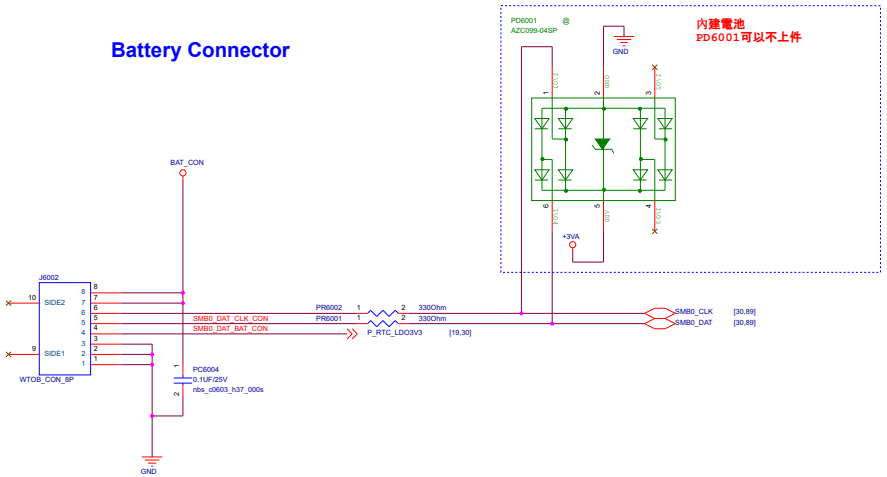
Date: Tuesday, July 19, 2016

0603 Bead rule:
33W:Bead*2;
45W,65W : bead* 3;
90W,120W,150W:Bead*4;
180W,230W: bead*6



12033-00031100 (58915-00202-001)
CH +0.8mm
2nd Source
12014-00109600 (2DC3137-005111F)

Battery Connector

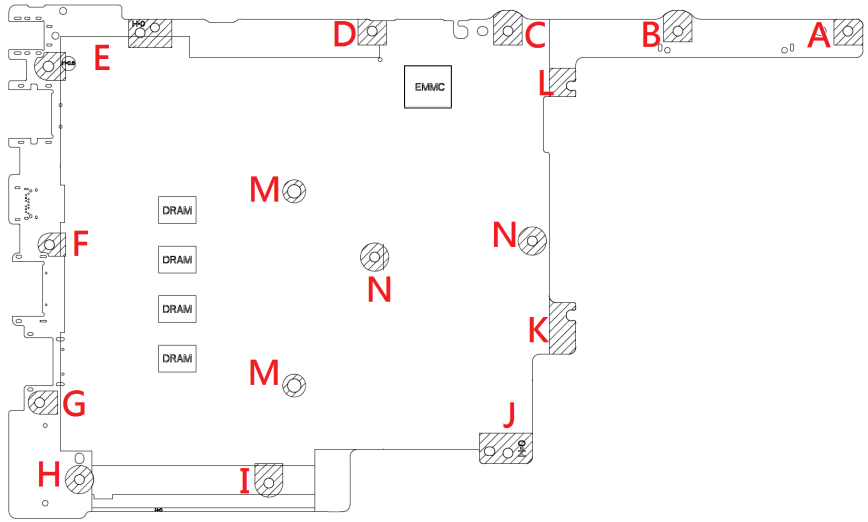


Pin define should be checked after battery team confirm

<Variant Name>

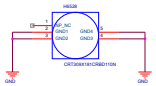
ASUS	Project Name: E402NA	Rev: 1.1
Title : DC_DC & BAT IN		
Size: C	Dept.: PC2-RD1-Sys2-EE1	Engineer:
Date: Tuesday, July 19, 2016	Sheet 60 of 99	

Screw Hole & SMT Nut



A

F



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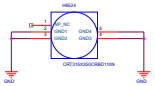


G

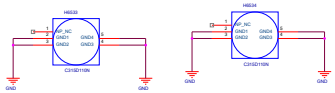
C

H

K

LAYOUT

N



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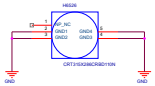

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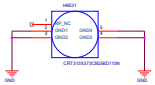
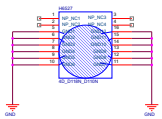


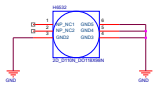
L

LAYOUT

E



J



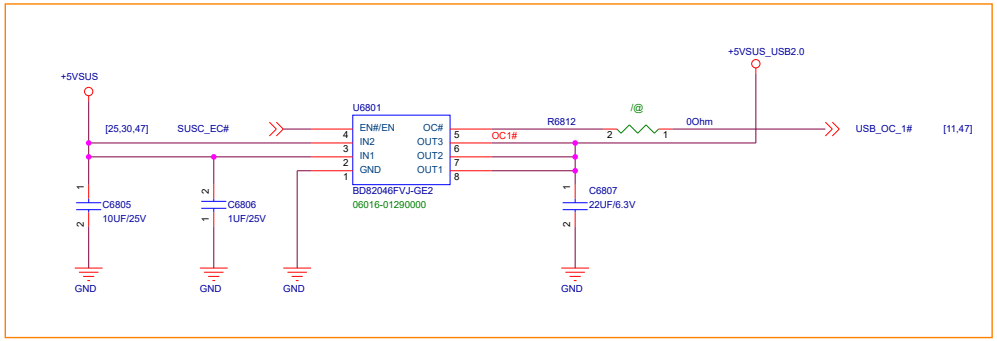
M

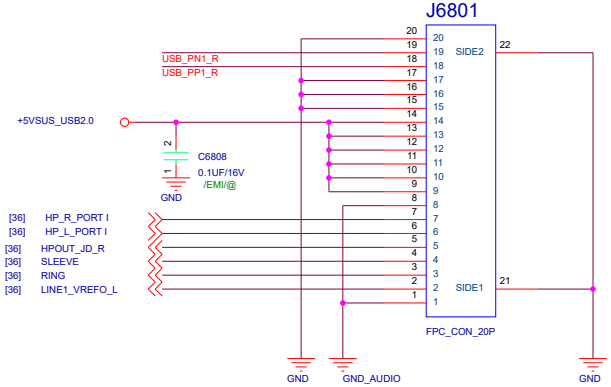
CPU NUT
13G0A2010M050-10

WLAN NUT
13020-01390000

IO B to B connector

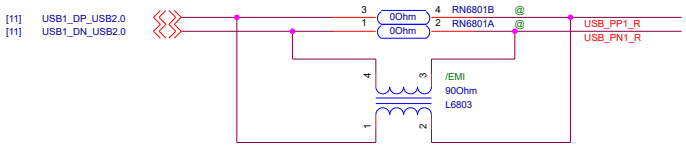
POWER



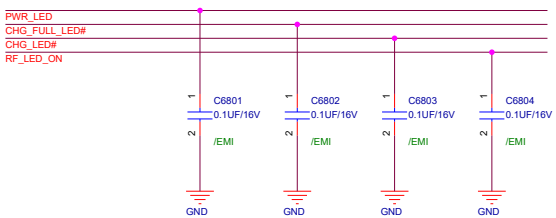


12018-00220600

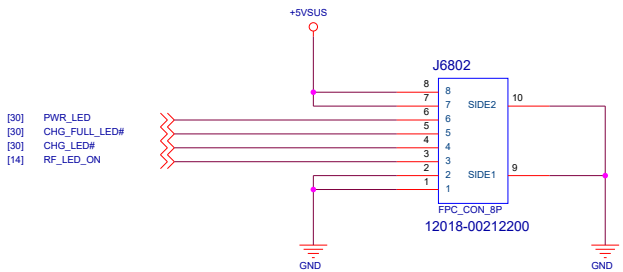
USB2.0 port0



LED B to B connector



E502SA R1.1 EMI



12018-00212200

<Core Design>

B TO B CONNECTOR

Evelyn and Kobe

PC2-RD1-Sys2-EE1

B **E402NA** 1.1

Tuesday, July 19, 2016 68 99

Project Name

E402NA

Rev

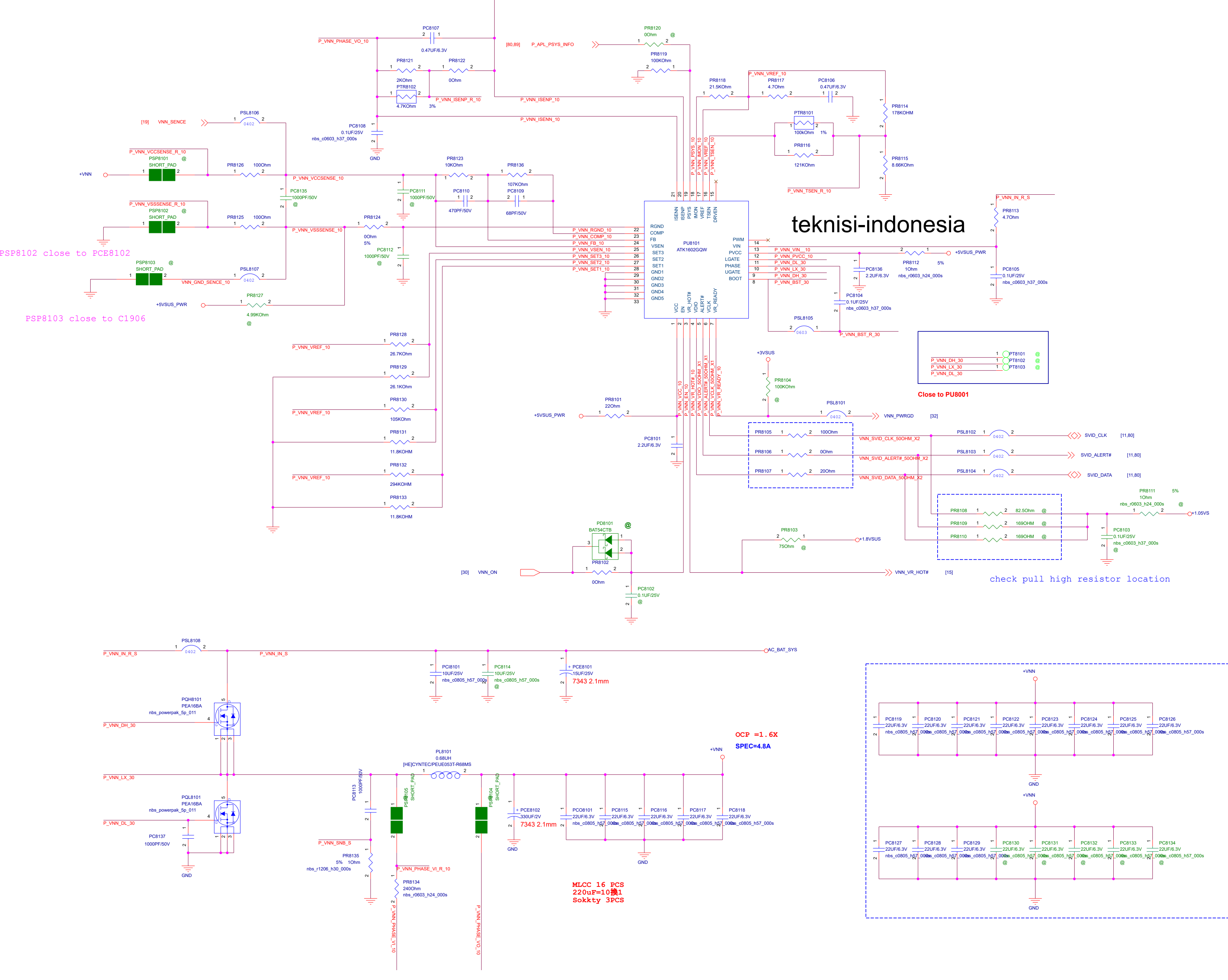
1.1

Title : CC logic

Size	Dept.:	Engineer:
C	PC2-RD1-Sys2-EE1	Evelyn and Kobe

Date: Tuesday, July 19, 2016

APL_+VNN(ATK1602GQW)



<Variant Name>

ASUS	Project Name: E402NA	Rev: 1.1
Title : PW_VNN		
Size: A2	Dept.: PC2-RD1-Sys2-EE1	Engineer:
Date: Tuesday, July 19, 2016	Sheet 81 of 99	

<Variant Name>

/SUS	Project Name **E402NA**	Rev 1.1

Title : ***

Size A3	**Dept.:** PC2-RD1-Sys2-EE1	**Engineer:**

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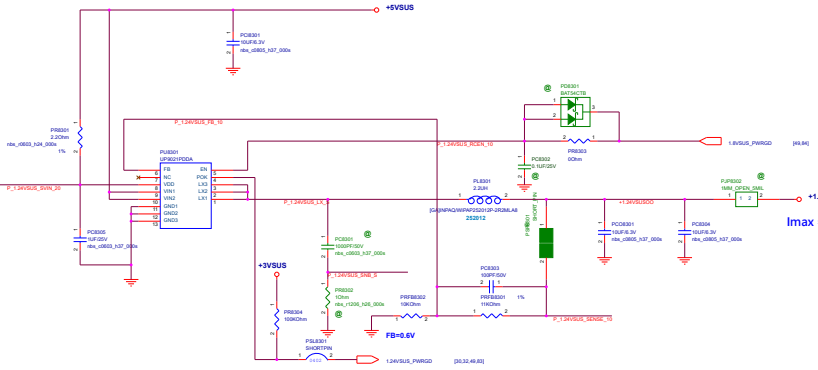
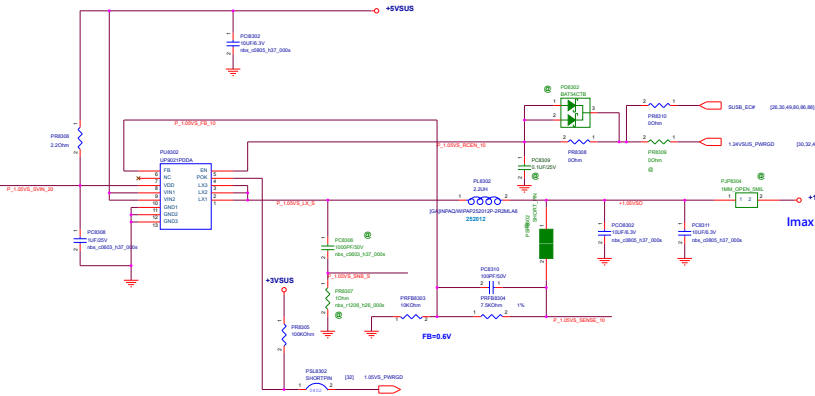
+1.24VSUS



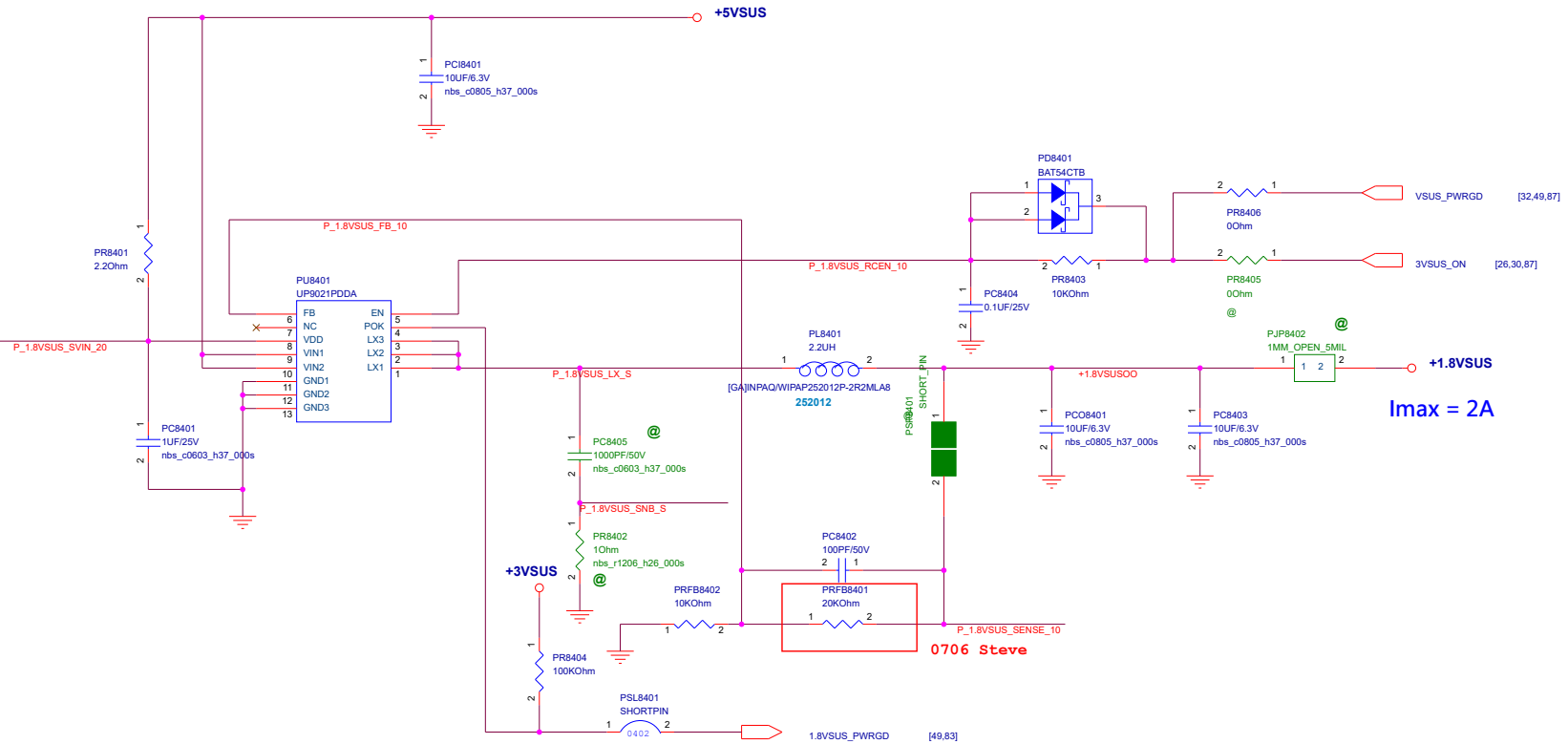
+1.05VS



<Variant Name>

ASUS	Project Name: E402NA	Rev: X.1
Title : +1.8VSUS / +1.05VS		
Size: Custom	Dept.: PCI-RD1-Sy42-EE1	Engineer: Eddie2_Lin
Date: Tuesday, July 19, 2016	Sheet 83 of 99	

+1.8VSUS



<Variant Name>

ASUS	Project Name: E402NA	Rev: 1.1
Title : PW_+1.8VSUS		
Size: A3	Dept.: PC2-RD1-Sys2-EE1	Engineer:
Date: Tuesday, July 19, 2016	Sheet 84 of 99	

<Variant Name>

	Project Name E402NA	Rev 1.1

Title : PW_***

Size A	**Dept.:** PC2-RD1-Sys2-EE1	**Engineer:**

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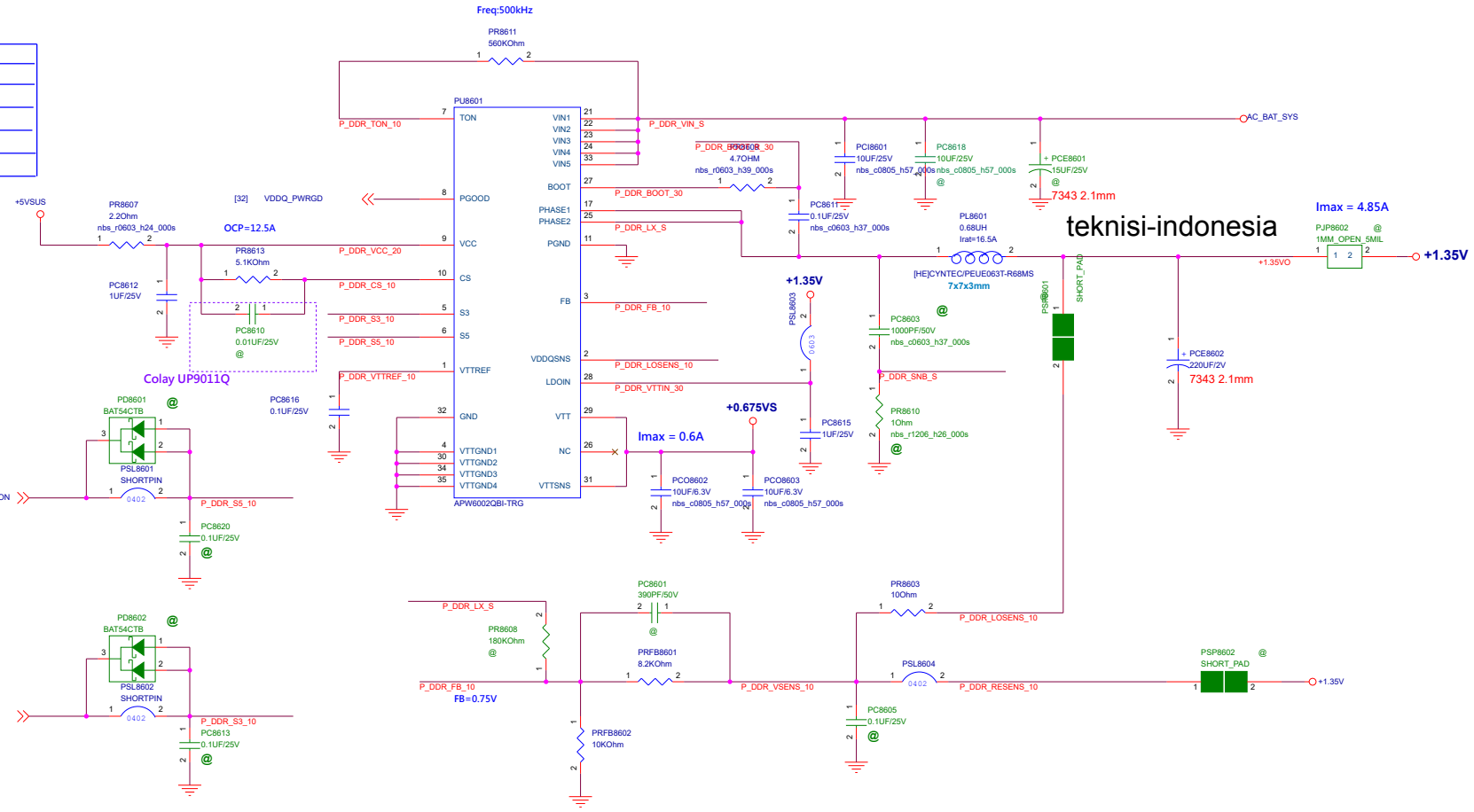
+1.35V / +VTT

PRFB8601	Vout
3.6kohm	1.0V
4.02kohm	1.05V
6.2kohm	1.2V
8.2kohm	1.35V
10.5kohm	1.5V

Colay table

	APW6002	UP9001Q
PC8610	@	N/A
PR8609	4.7Ohm	2.2Ohm
PC8608	@	N/A
PC8601	@	N/A
PR8608	@	N/A
PR8613	5.1Kohm	9.1Kohm



<Variant Name>

ASUS	Project Name: E402NA	Rev: 1.1
Title : +1.35V / +0.6VS		
Size: A3	Dept.: ASUS Power Team	Engineer: Kevin
Date: Tuesday, July 19, 2016	Sheet 86 of 99	

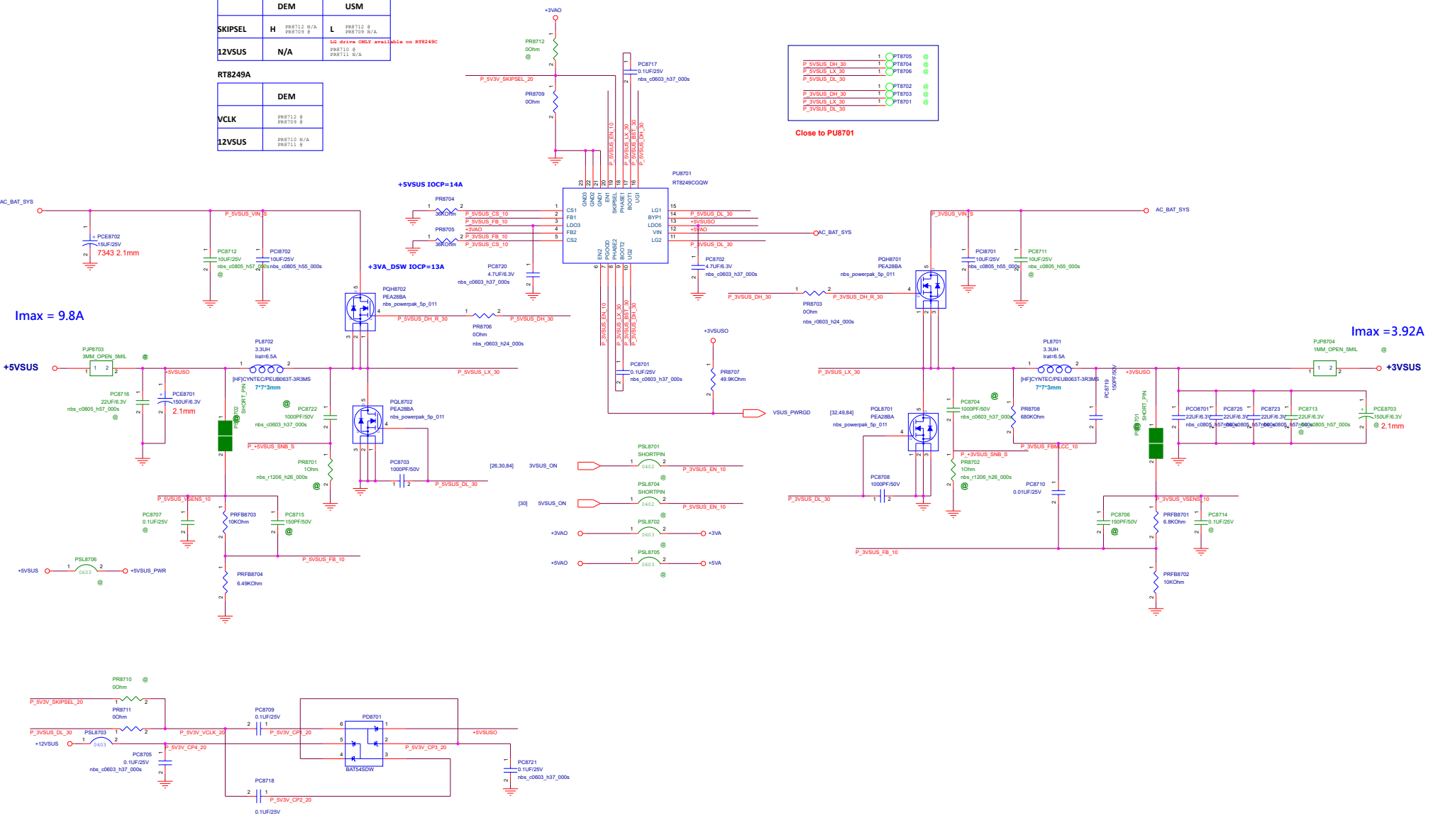
+3VSUS / +5VSUS [System Power]

RT8249C

	DEM	USM
SKIPSEL	H PR8712 N/A PR8709 0	L PR8712 0 PR8709 N/A
12VSUS	N/A	LG drive ONLY available on RT8249C PR8710 0 PR8711 N/A

RT8249A

	DEM
VCLK	PR8712 0 PR8709 0
12VSUS	PR8710 N/A PR8711 0

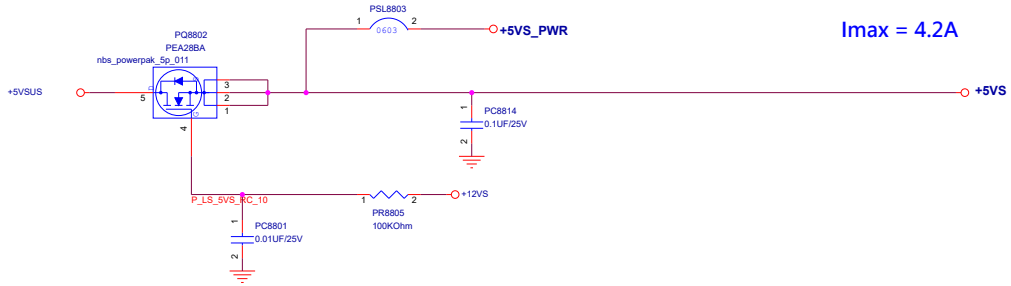


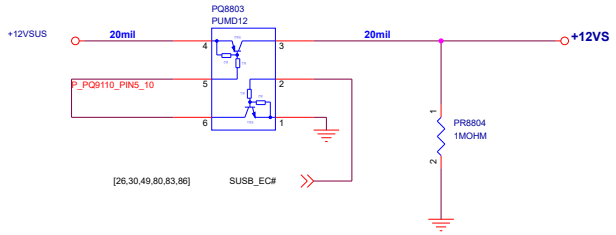
請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

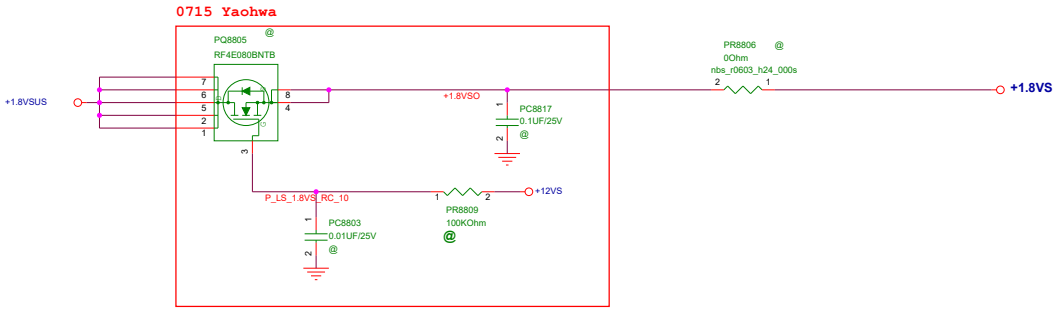
<Variant Name>

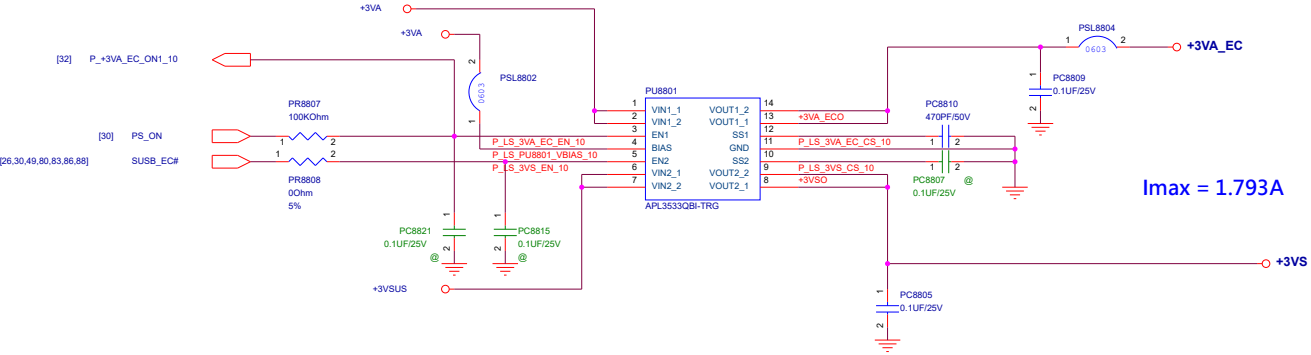
ASUS	Project Name: E402NA	Rev: 1.1
Title :	PW_+3VSUS/+5VSUS	
Size: Custom	Dept.:	Engineer:
Date: Tuesday, July 19, 2016	Sheet 87 of 99	

Load Switch



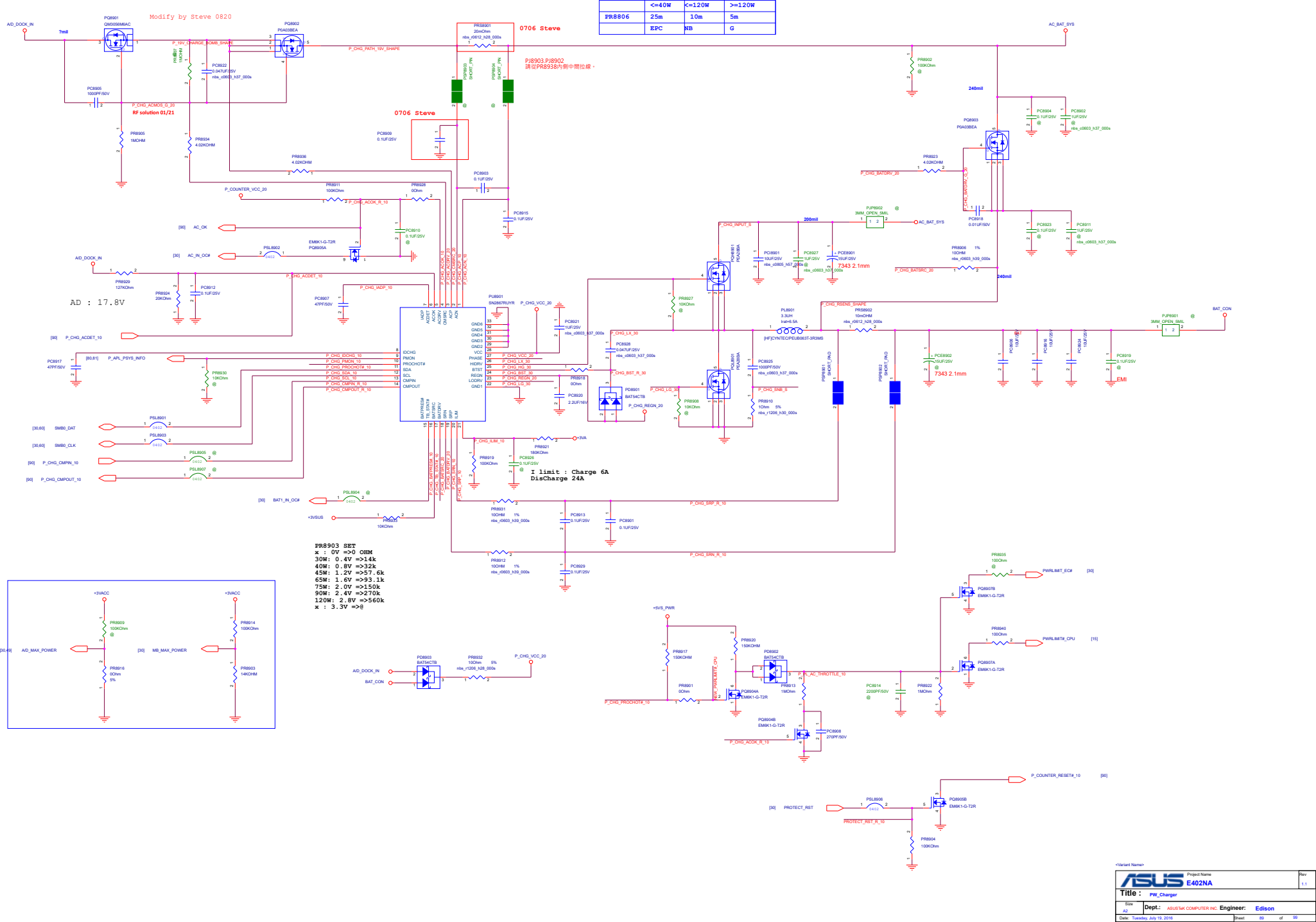






<Variant Name>

Project Name: E402NA		Rev: 1.1
Title : PW_LS		
Size: A3	Dept.: NB3/EE1	Engineer:
Date: Tuesday, July 19, 2016	Sheet 88 of 99	



	<=40W	<=120W	>=120W
PR8806	25m	10m	5m
	EPC	NB	G

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
R7901	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
R7902	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

2nd UP1905
EE線路for Thermal Team

TR7901 place near DGPU VRAM ,
SSD base on thermal RD test

TR7902 place near AMD/APL CPU

TR7903 place near DGPU VRM Lwo-Side MOS

ALERT# pull low if sensed temp. is higher than setting

Check 其他頁是否有 pull high 到 3.3V

PTR9000 place near PQ8901

PTR9001 place near J6002(BAT_CONN)

PTR9002 place near PL8901

UMA delete VGA_ALERT_P# 0409

Change SMB net name 0409

Close to EC

I2C VIH=0.942V
I2C VIL=0.810V

ALERT# pull low if sensed temp. is higher than setting

Check 其他頁是否有 pull high 到 3.3V

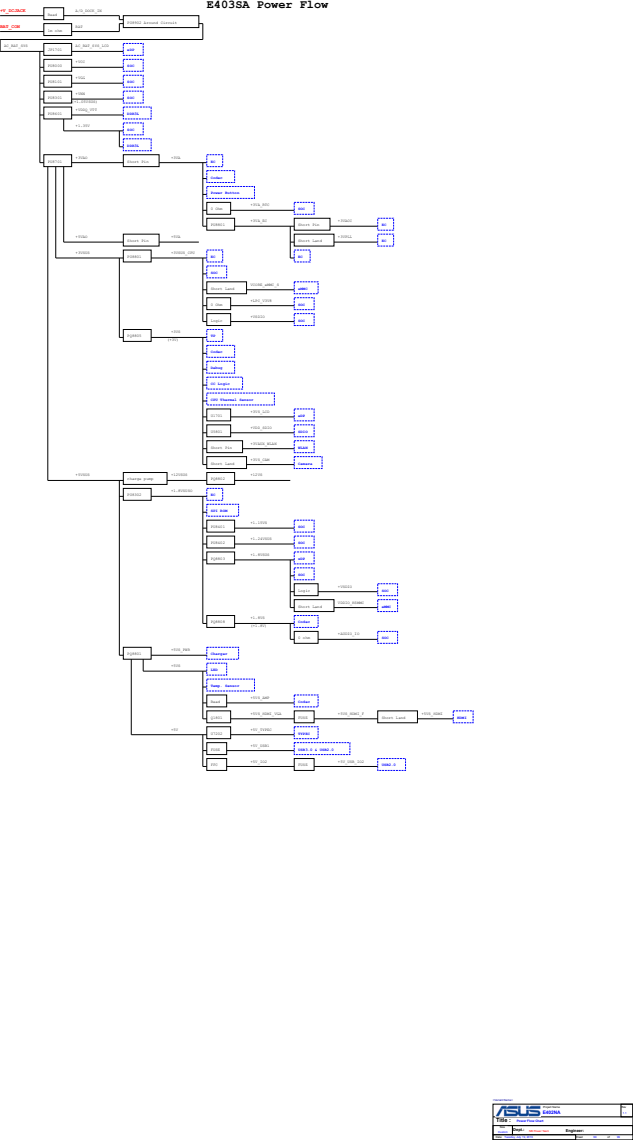
teknisi-indonesia

counter

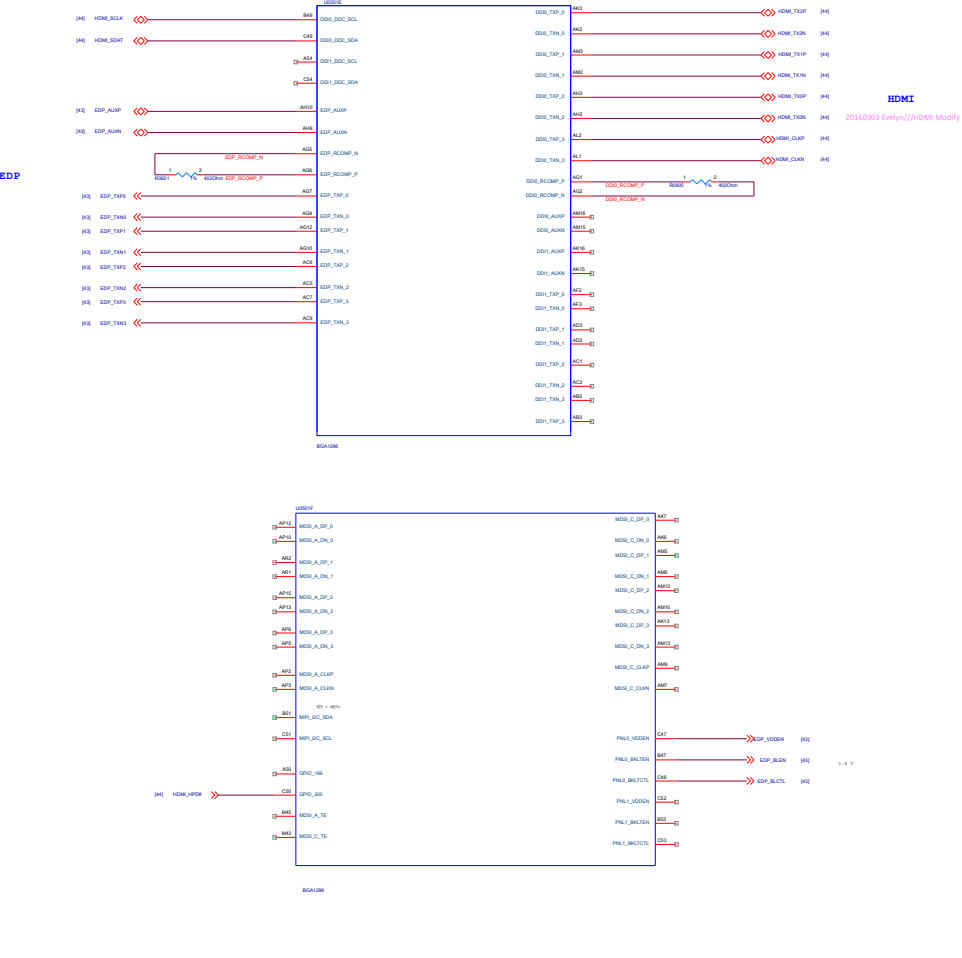
thermal latch

PTR9006 place near J6001 (DC_JAck)

E403SA Power Flow



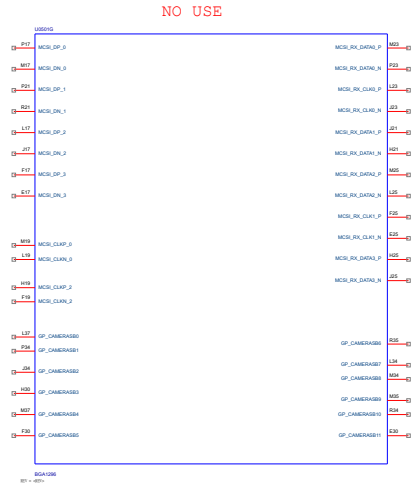
ASUSTeK Computer Inc.			
ASUS	E403SA		
Title : Power Flow Chart			
Size:	Project Code:	Version:	
Date: Thursday, July 18, 2013	Sheet	of	



HDMI

20160303 Evelyn///HDMI Modify

EDP



Project Name: E402NA			Rev: 1.1
Title: CPU_Display&Camera			
Size: D	Dept.: PCS-RD1-SysS-SS1	Engineer: Evelyn and Kobe	
Date: Tuesday, July 19, 2016	Sheet 6 of 99		

APL_+VCGI(ATK1602GQW)