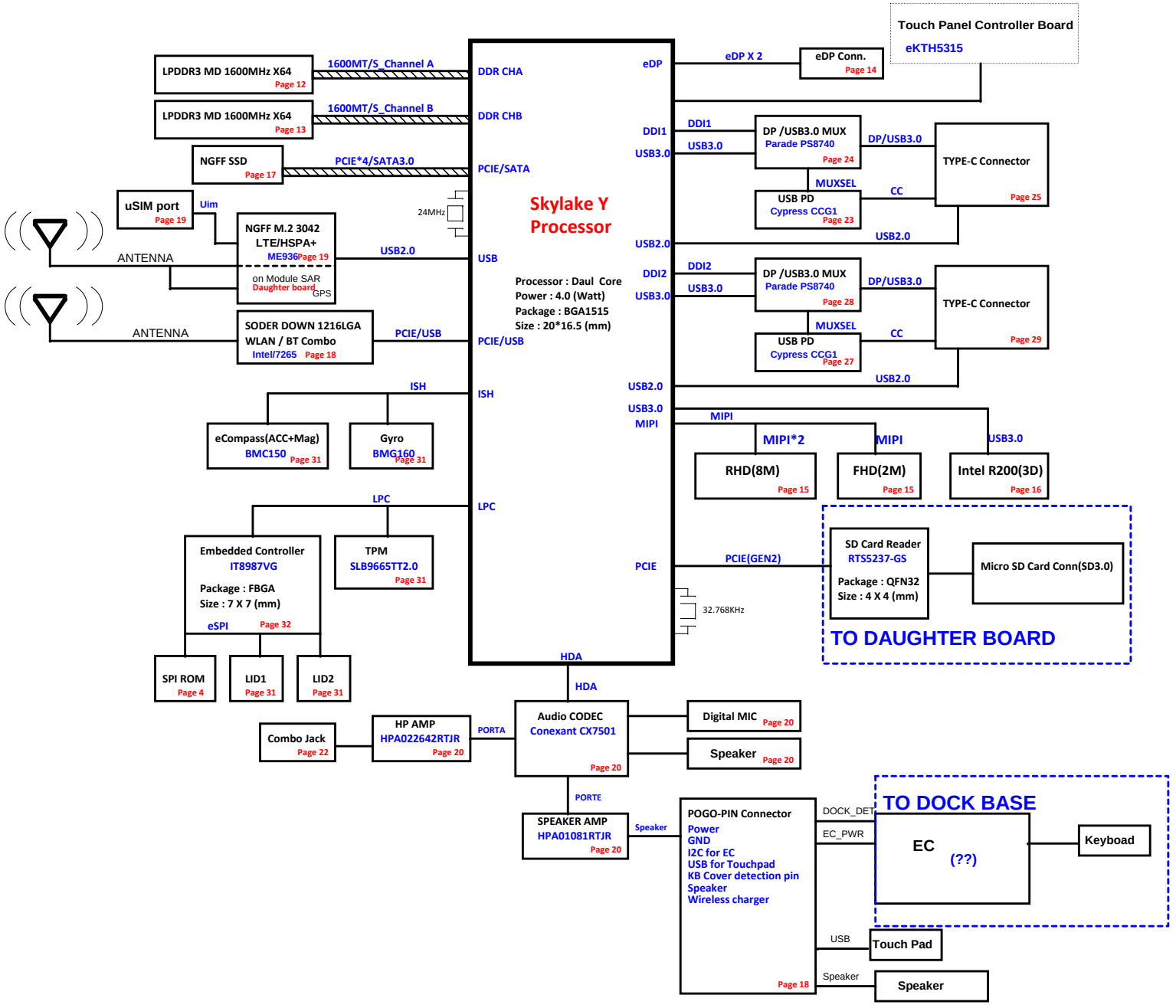
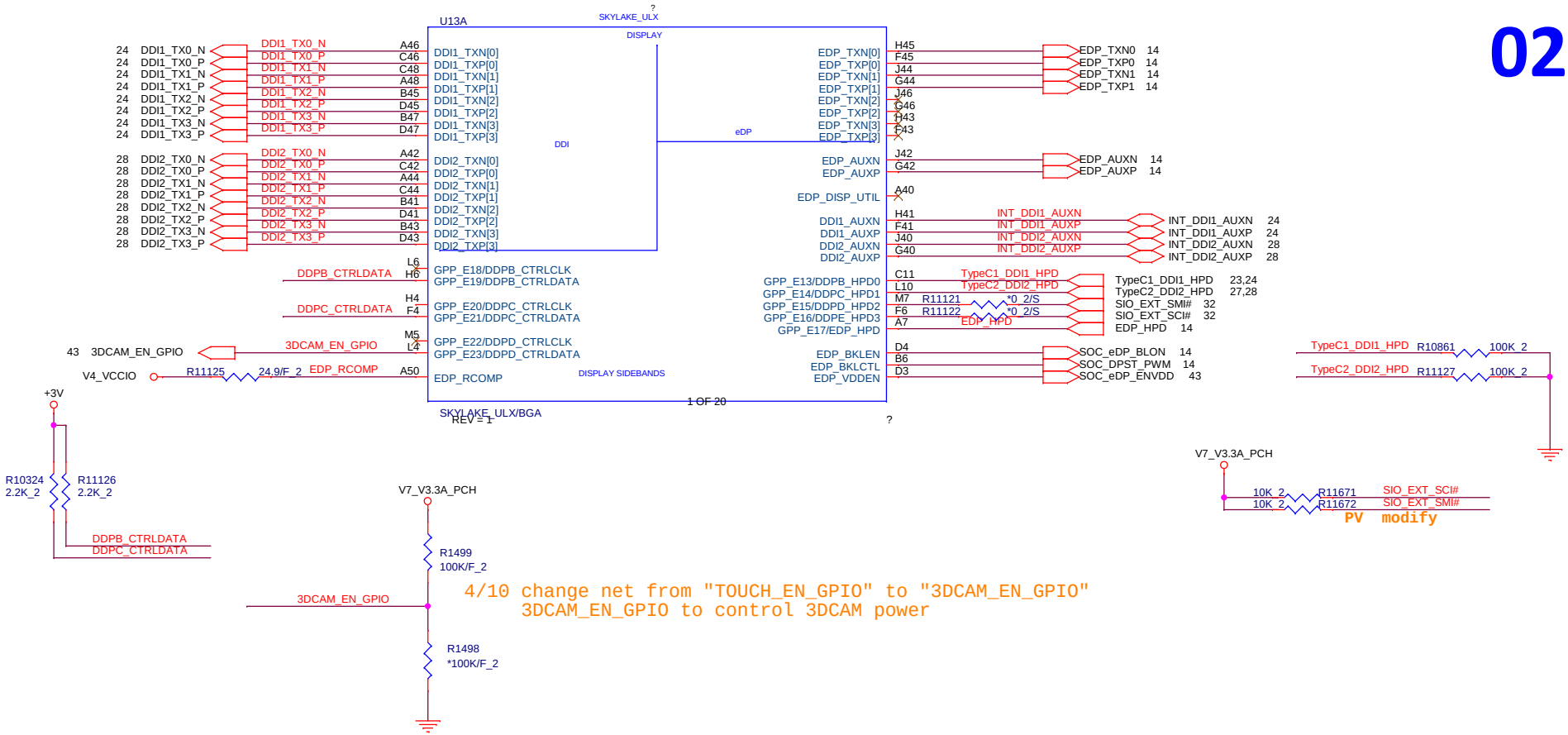
Millhone Block Diagram

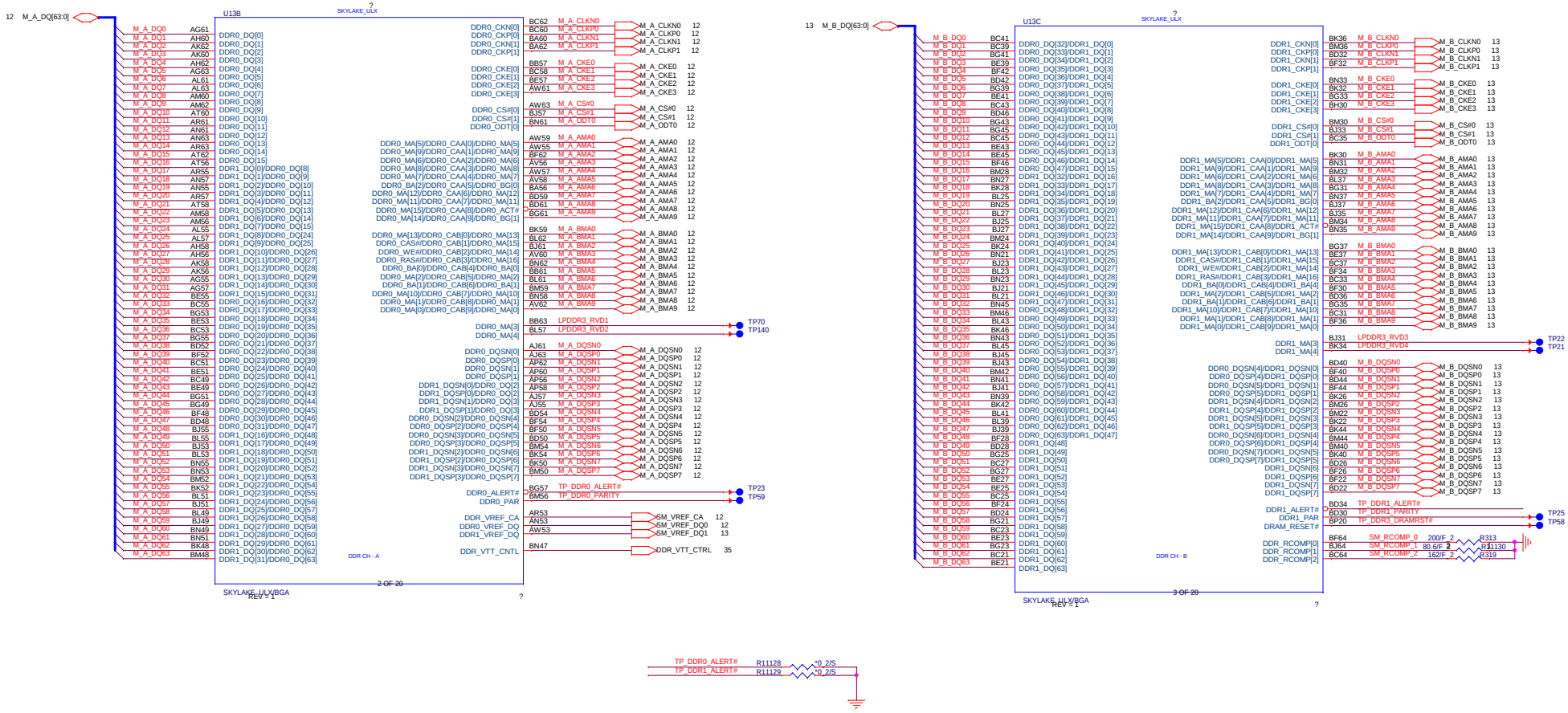
01



Millhone Custom NB5 HW	PROJECT : Millhone Quanta Computer Inc.	
Size	Document Number Block diagram	Rev A
Date: Friday, August 28, 2015	Sheet 1 of 48	

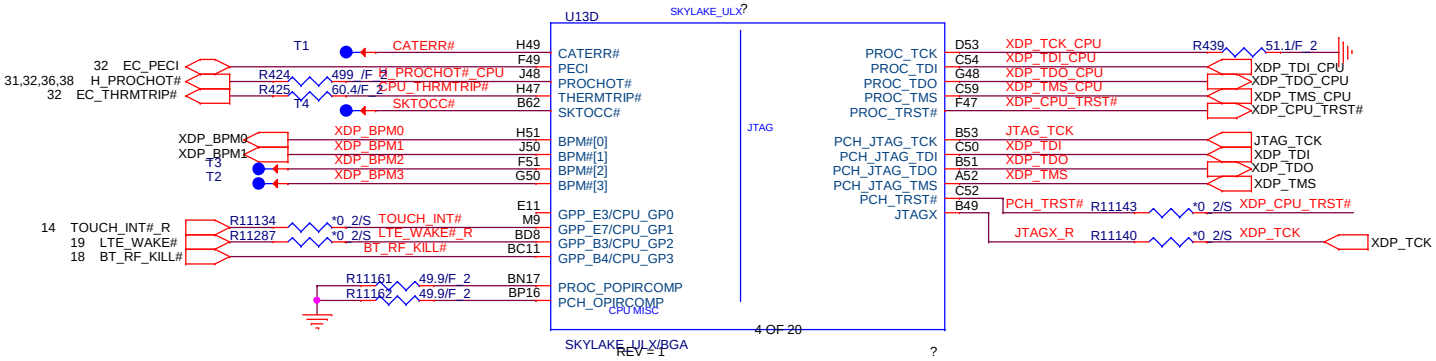


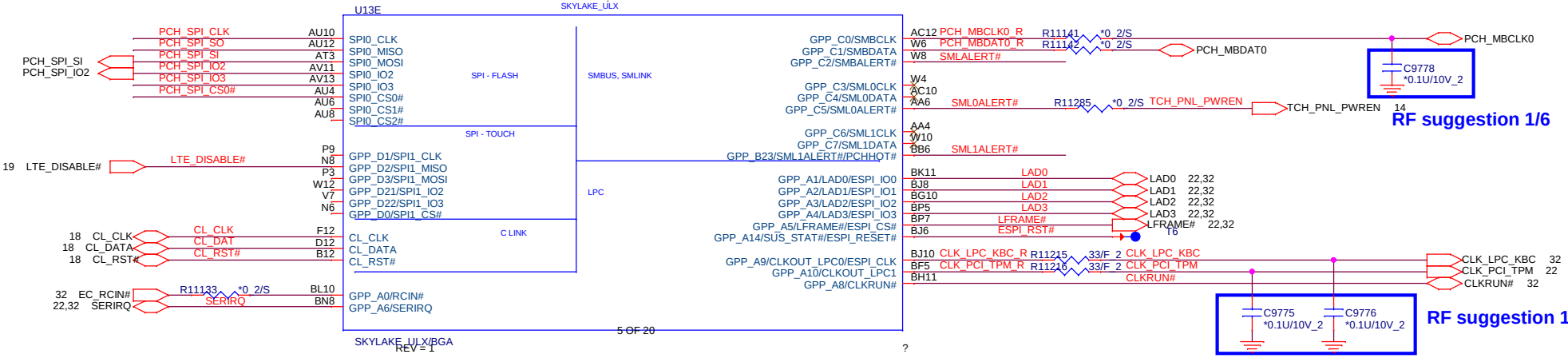
NB5 HW	PROJECT : Millhone Quanta Computer Inc.		
	Size	Document Number SKL-Y CPU (DDI/EDP)	Rev A
	Date: Friday, August 28, 2015	Sheet 2 of 48	



NB5 HW	PROJECT : Millhone Quanta Computer Inc.	
	Size	Document Number: SKL-Y CPU (Memory) — Rev: A
	Date: Friday, August 28, 2015	Sheet 3 of 48

04



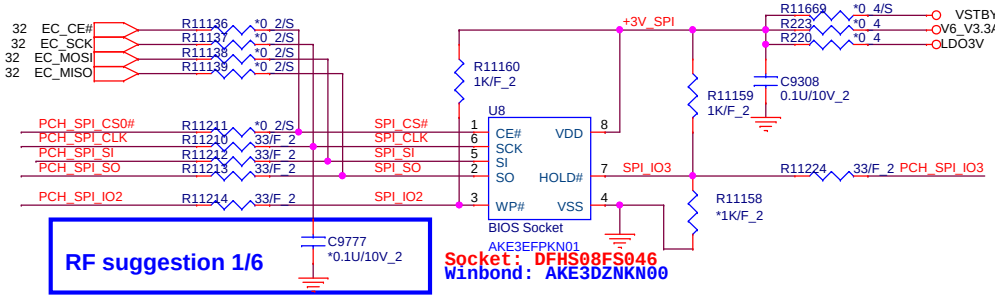


RF suggestion 1/6

RF suggestion 1/6

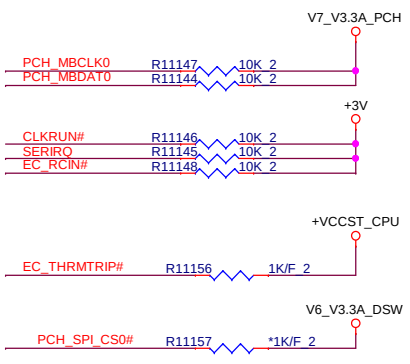
RF suggestion 1/6

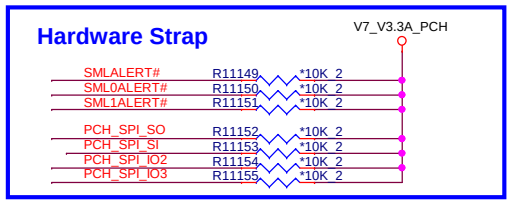
SPI ROM for EC & BIOS



RF suggestion 1/6

Socket: DFHS08FS046
Winbond: AKE3DZNKN00

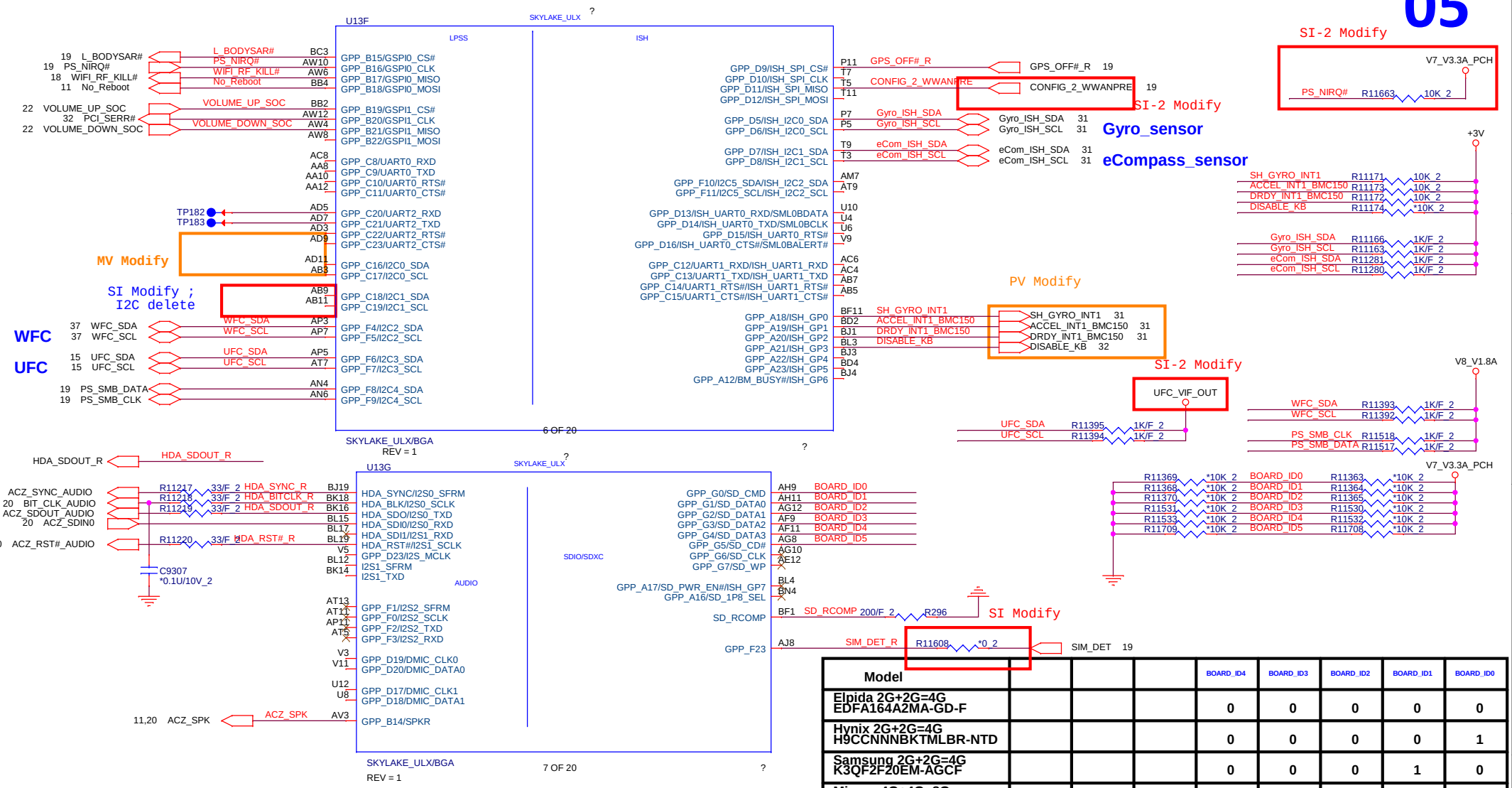




NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	SKL-Y CPU (MISC/JTAG/SMB)	A
Date: Friday, August 28, 2015	Sheet 4 of 48	

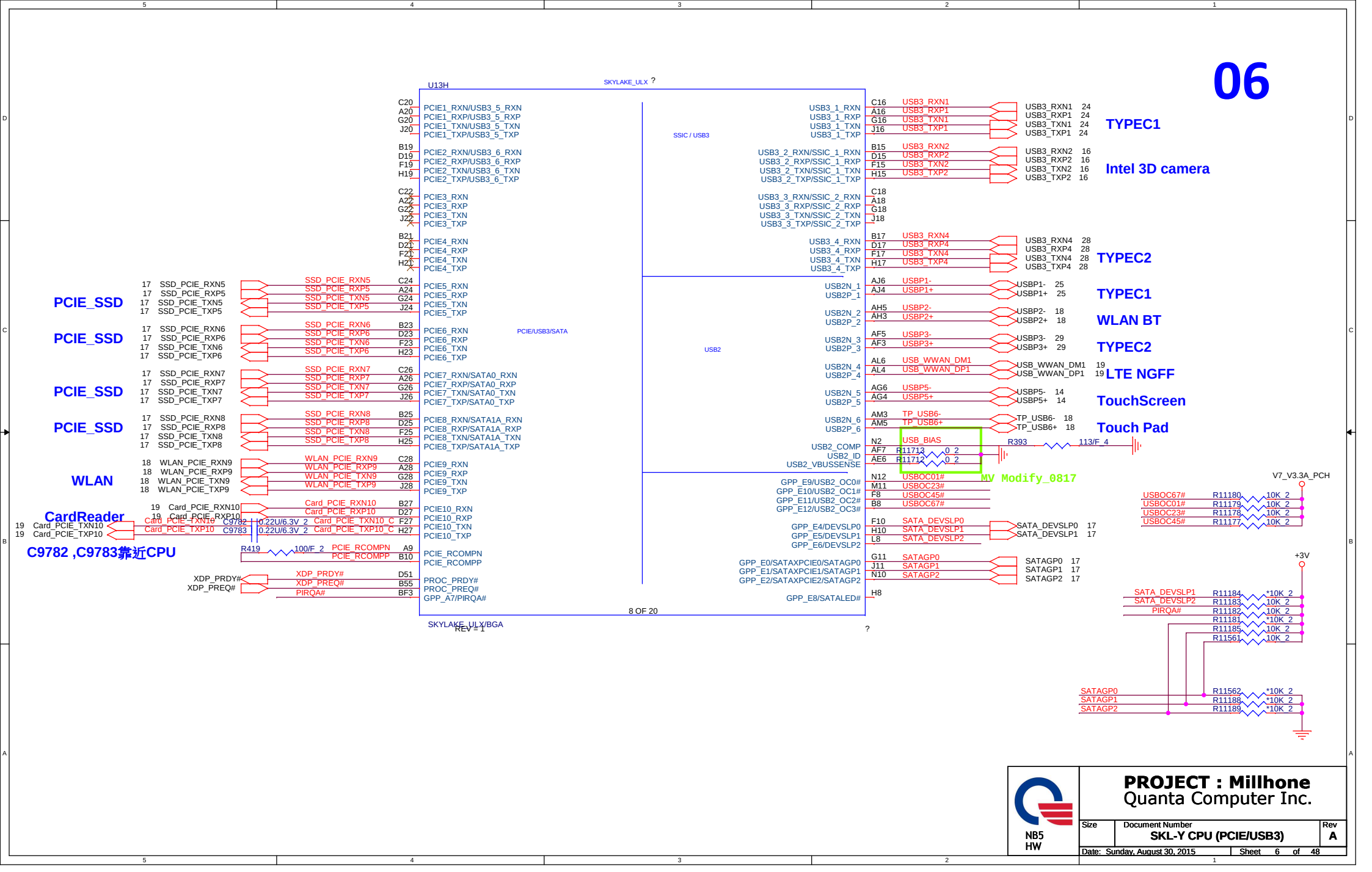


Model				BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Elpida 2G+2G=4G EDFA164A2MA-GD-F				0	0	0	0	0
Hynix 2G+2G=4G H9CCNNNBKTMLBR-NTD				0	0	0	0	1
Samsung 2G+2G=4G K3QF2F20EM-AGCF				0	0	0	1	0
Micron 4G+4G=8G EDFB164A1MA-GD-F				0	0	0	1	1
Hynix 4G+4G=8G H9CCNNNCPTMLBR-NTD				0	0	1	0	0

NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	SKL-Y CPU (LPSS/ISH/HDA)	A
Date: Sunday, August 30, 2015	Sheet 5 of 48	



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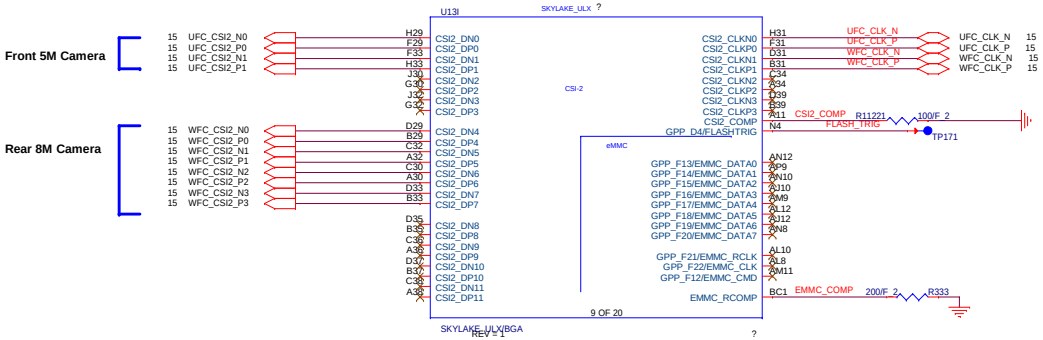
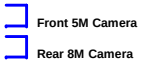
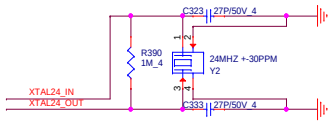
07

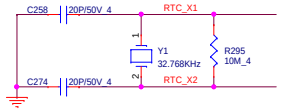


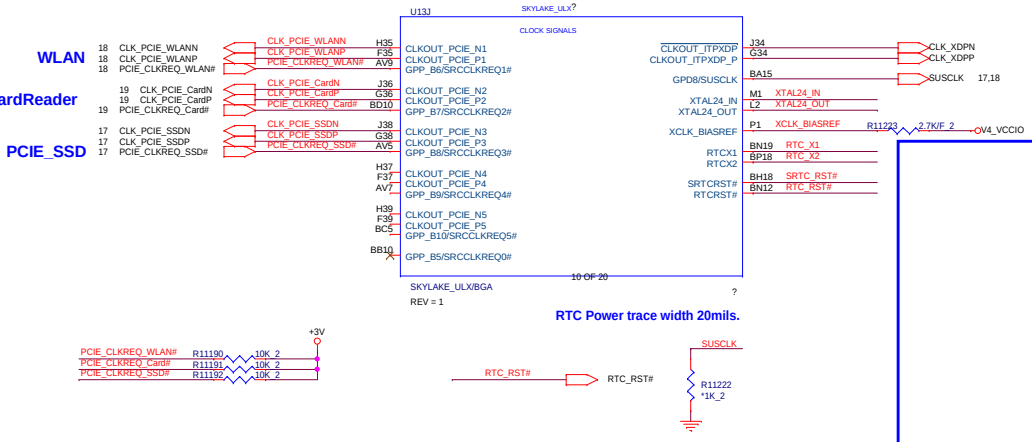


PCH Crystal (CLG)

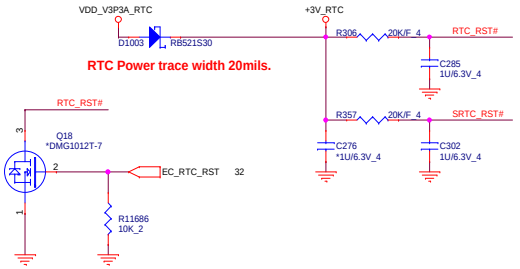


RTC Crystal (CLG)

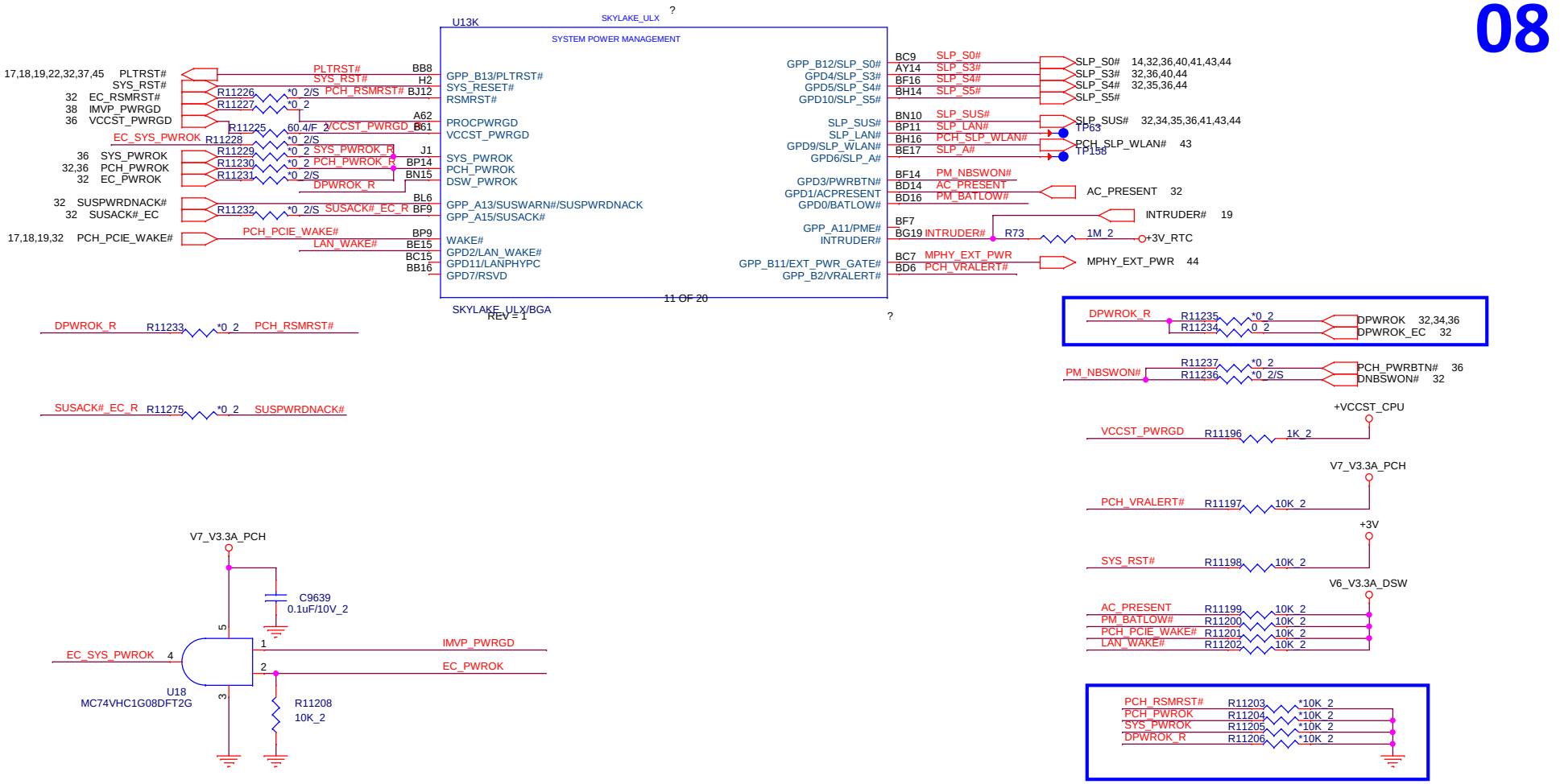




RTC Circuitry(RTC)



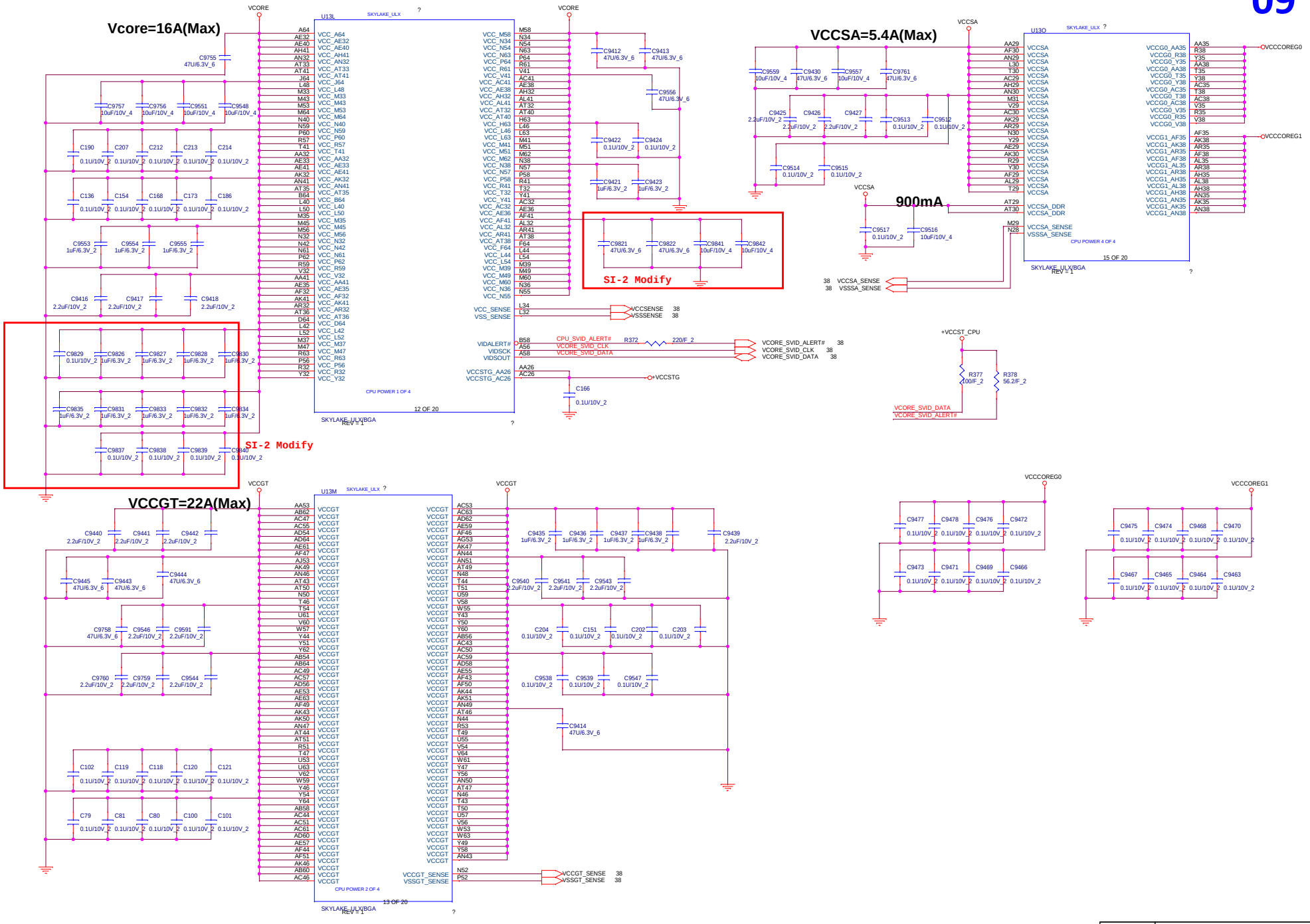
NB5 HW	PROJECT : Millhone Quanta Computer Inc.	
	Size	Document Number: SKL-Y CPU (CSI2/eMMC/CLK) — Rev: A
	Date: Friday, August 28, 2015	Sheet 7 of 48



PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	SKL-Y CPU (PWR MANAGE)	A
Date: Friday, August 28, 2015	Sheet 8 of 48	

NB5
HW



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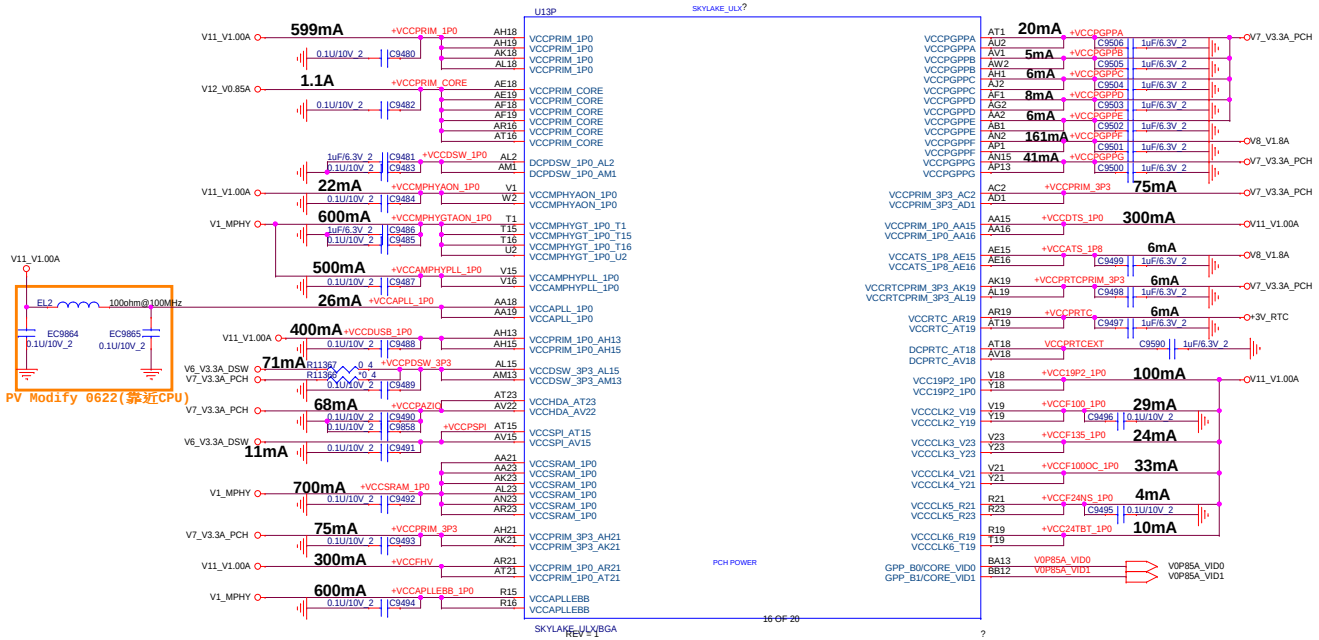
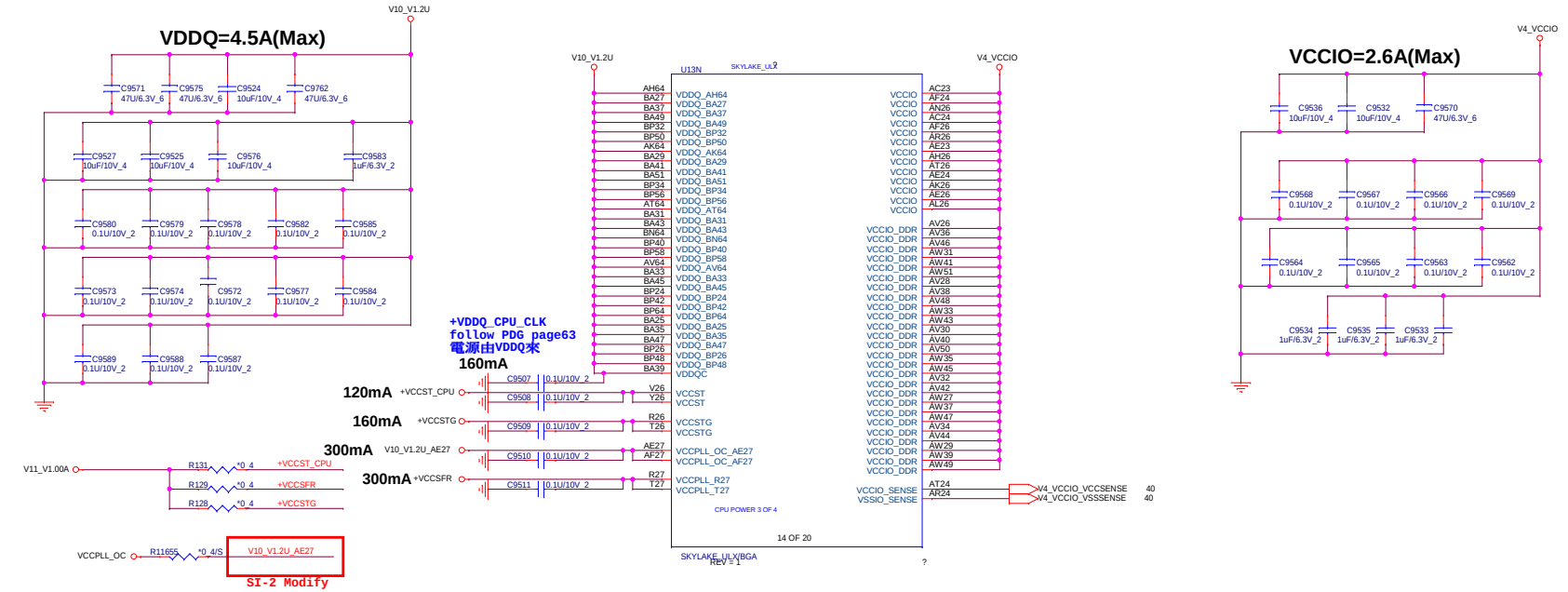
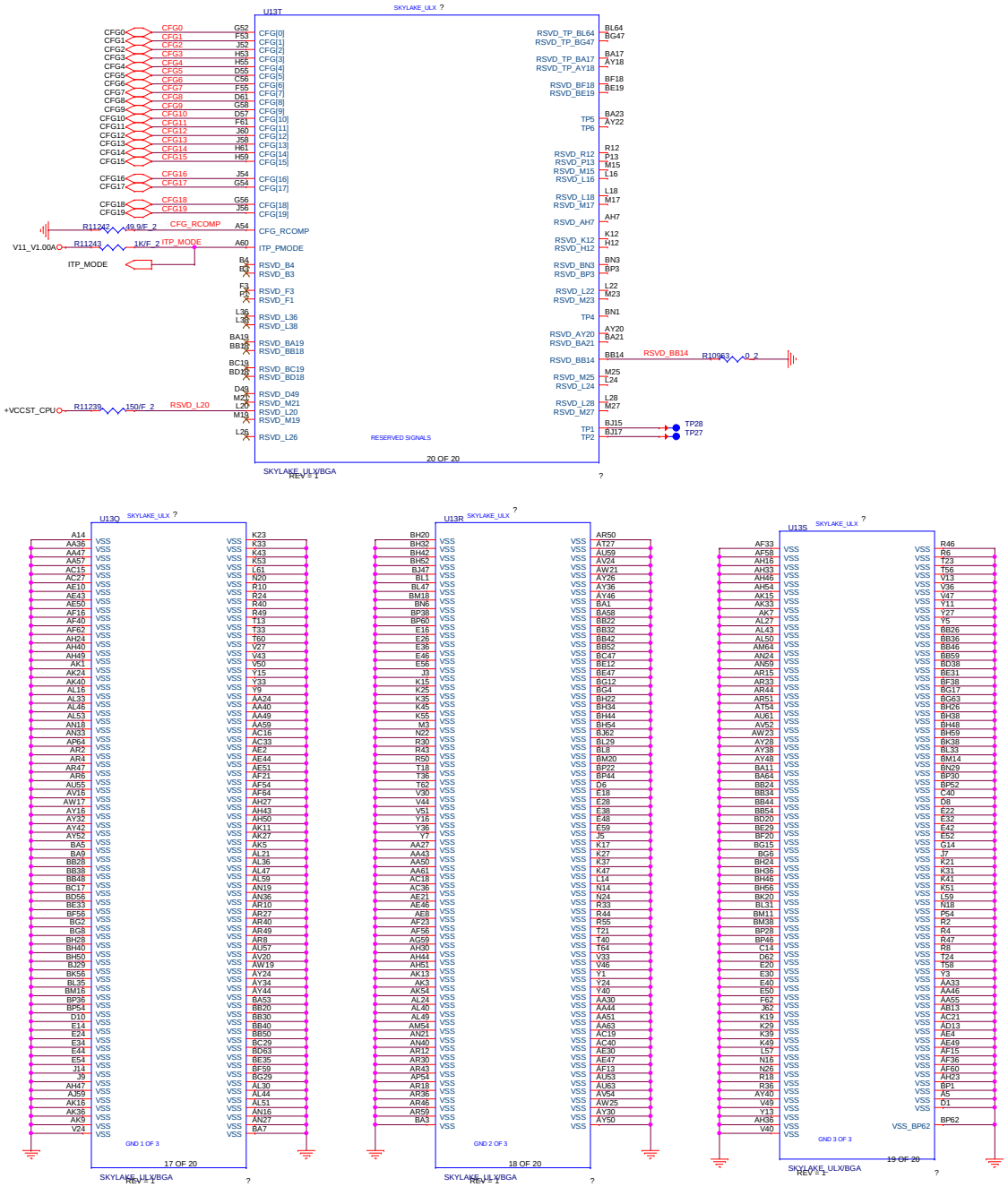
NB5 HW	PROJECT : Millhone Quanta Computer Inc.	
	Size	Document Number: SKL-Y CPU (PWR1) — Rev: A
	Date: Friday, August 28, 2015	Sheet 9 of 48



PV Modify 0622(靠近CPU)





11

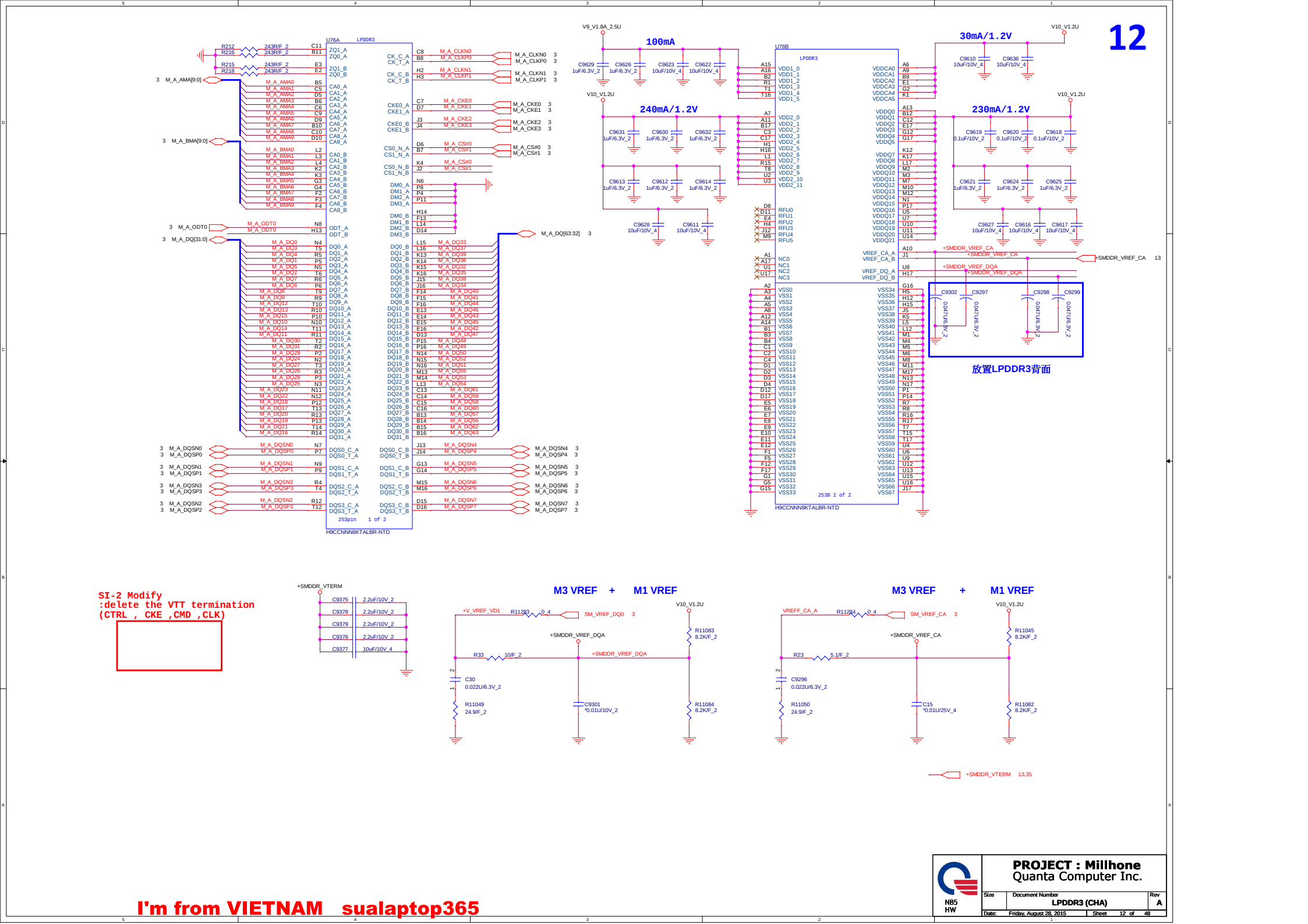
Processor Strapping

	1	0	
CFG4 eDP Enable	DISABLED	ENABLED	CFG4 R11269 1K/F_2
SPKR / GPP_B14	ENABLED	DISABLED	5,20 ACZ_SPK R11270 *10K_2 +3V
GSPI0_MOSI /GPP_B18	ENABLED	DISABLED	5 No_Reboot R11271 *10K_2 +3V
SMBALERT# /GPP_C2	ENABLED	DISABLED	Already Pull-high on Page.4
Boot BIOS Strap Bit /GPP_B22	LPC	SPI	(default:SPI)
SML0ALERT# / GPP_C5	ESPI	LPC	Already Pull-high on Page.4(default:LPC)
SML1ALERT# / PCHHOT#/ GPP_B23			Already Pull-high on Page.6
SPI0_MOSI			Already Pull-high on Page.4
SPI0_MISO			Already Pull-high on Page.4
SPI0_IO2			Already Pull-high on Page.4
SPI0_IO3			Already Pull-high on Page.4
HDA_SDO/ I2S_TXD0 **Security Flash Descriptors**	**DISABLED**	**ENABLED**	Already Pull-high on Page.5
DDPB_CTRLDATA / GPP_E19	ENABLED		Already Pull-high on Page.2
DDPC_CTRLDATA / GPP_E21	ENABLED		Already Pull-high on Page.2

NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	SKL-Y CPU (VSS/CFG/RSVD)	A
Date: Friday, August 28, 2015	Sheet 11 of 48	


12
U76A
LPDDR3
H9CCNNN8KTALBR-NTD
253pin 1 of 2
U76B
253B 2 of 2
100mA
240mA/1.2V
30mA/1.2V
230mA/1.2V
放置LPDDR3背面
SI-2 Modify
:delete the VTT termination
(CTRL , CKE ,CMD ,CLK)
M3 VREF + M1 VREF
M3 VREF + M1 VREF
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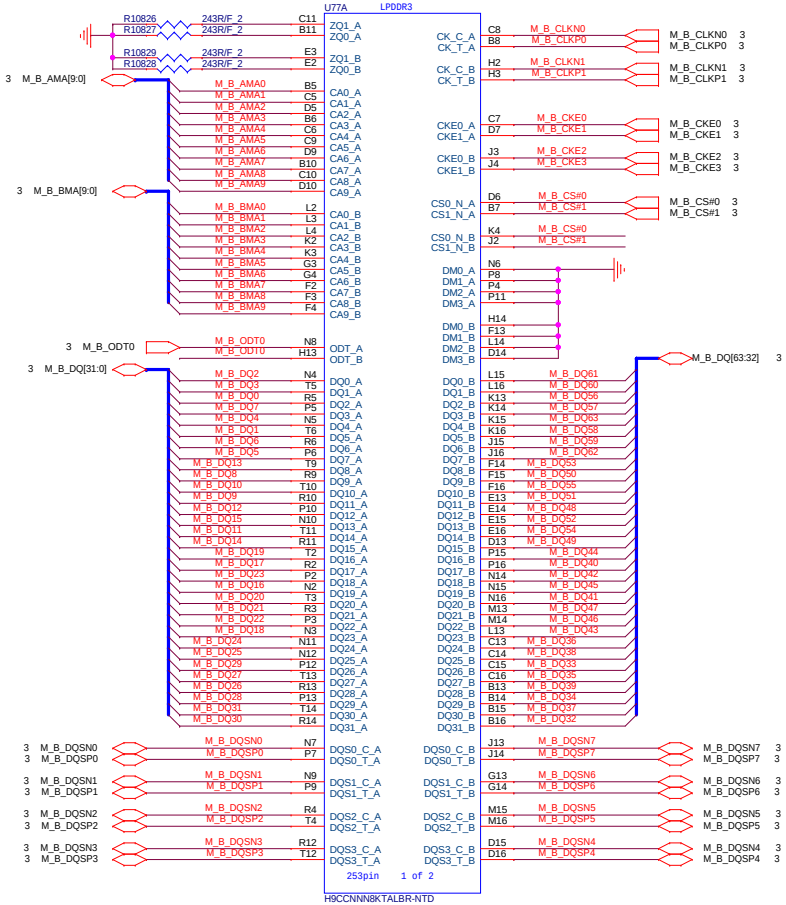
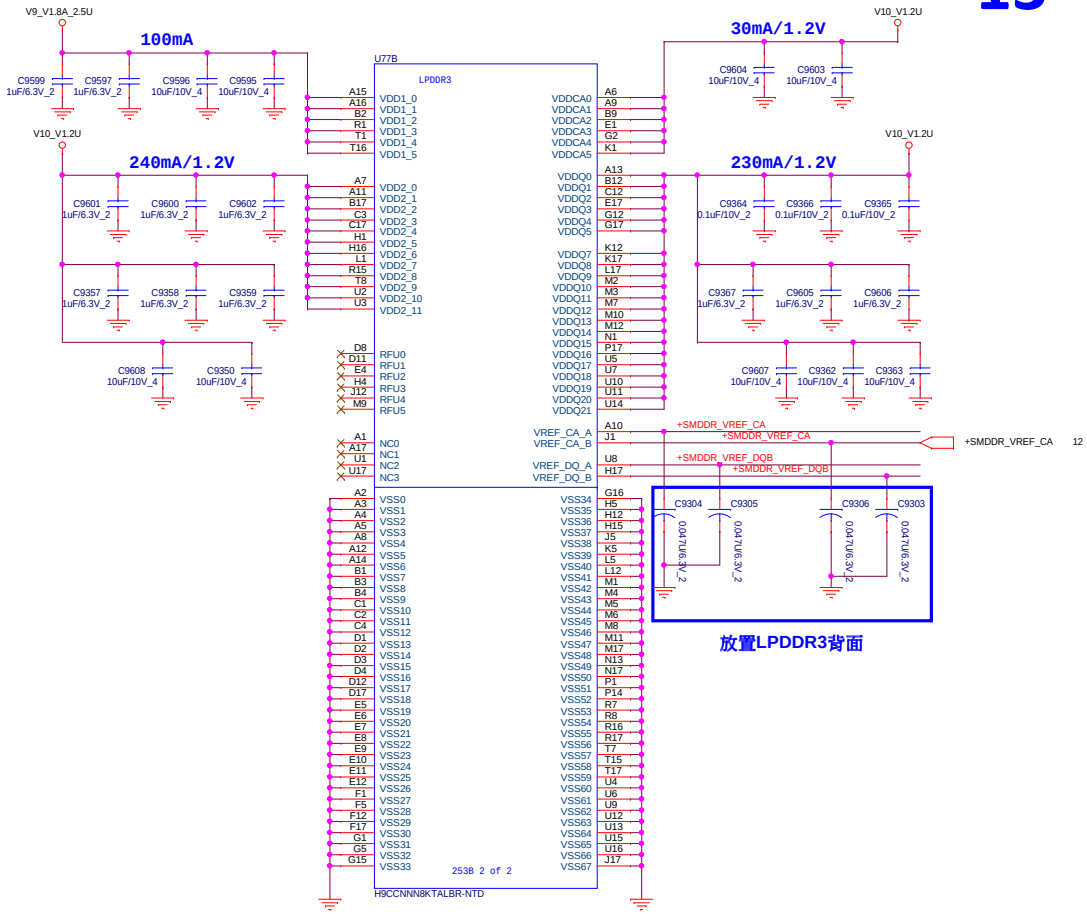
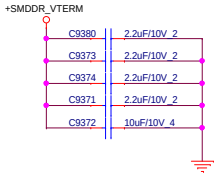
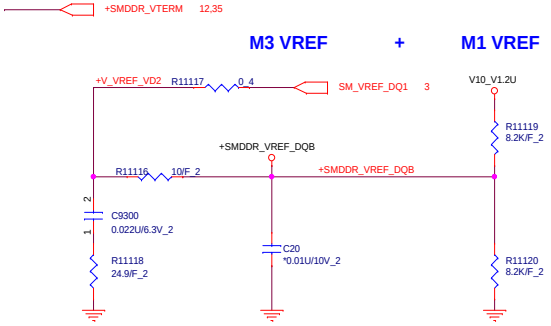
PROJECT : Millhone
Quanta Computer Inc.
N85
HW
Document Number
LPDDR3 (CHA)
Rev
A
Date: Friday, August 28, 2015
Sheet 12 of 48



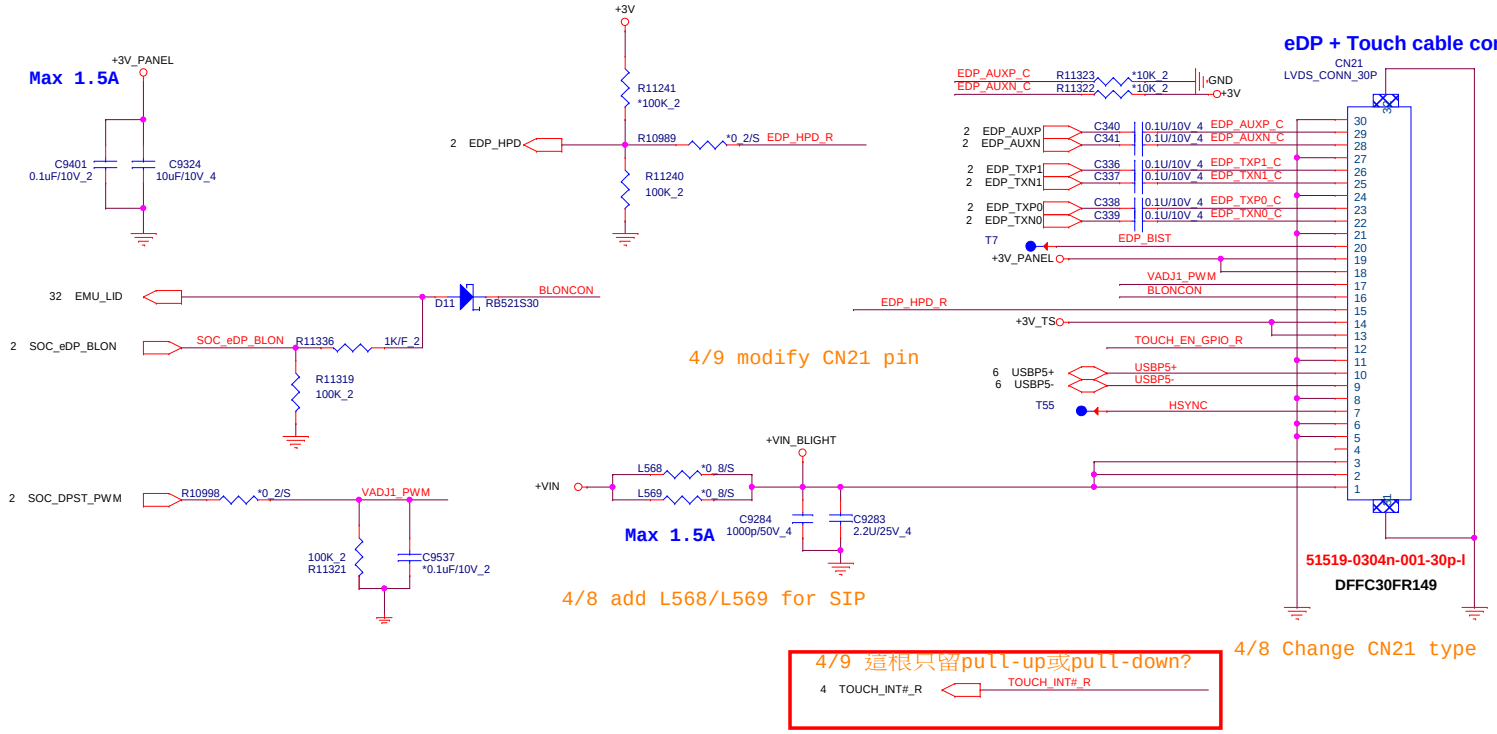




SI-2 Modify
:delete the VTT termination
(CTRL , CKE ,CMD ,CLK)



NB5 HW	PROJECT : Millhone Quanta Computer Inc.	
Size	Document Number LPDDR3 (CHB)	Rev A
Date: Friday, August 28, 2015	Sheet 13 of 48	

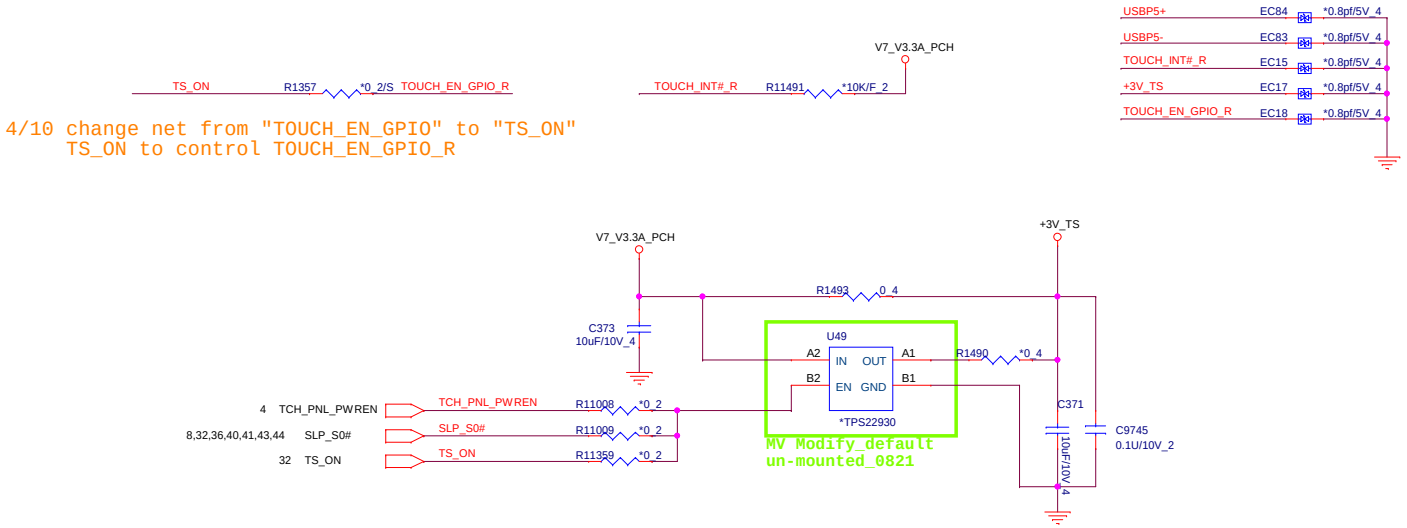


4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description
1	NC	No Connection (Reserved)
2	H_GND	High Speed Ground
3	LANE1_N	Complement Signal Link Lane 1
4	LANE1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	LANE0_N	Complement Signal Link Lane 0
7	LANE0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Channel
10	AUX_CH_N	Complement Signal Auxiliary Channel
11	H_GND	High Speed Ground
12	VCCS	Power Supply +3.3 V (typical)
13	VCCS	Power Supply +3.3 V (typical)
14	BIST	LCD Panel Self Test Enable
15	GND	Ground
16	GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	Backlight Ground
19	BL_GND	Backlight Ground
20	BL_GND	Backlight Ground
21	BL_GND	Backlight Ground
22	LED_EN	Backlight Enable Signal of LED Converter
23	LED_PWM	PWM Dimming Control Signal of LED Converter
24	NC	No Connection (Reserved)
25	NC	No Connection (Reserved)
26	LED_VCCS	Backlight Power
27	LED_VCCS	Backlight Power
28	LED_VCCS	Backlight Power
29	LED_VCCS	Backlight Power
30	NC	No Connection (Reserved)

Touch Panel ESD



+3V_TS
V7_V3.3A_PCH 2,4,5,6

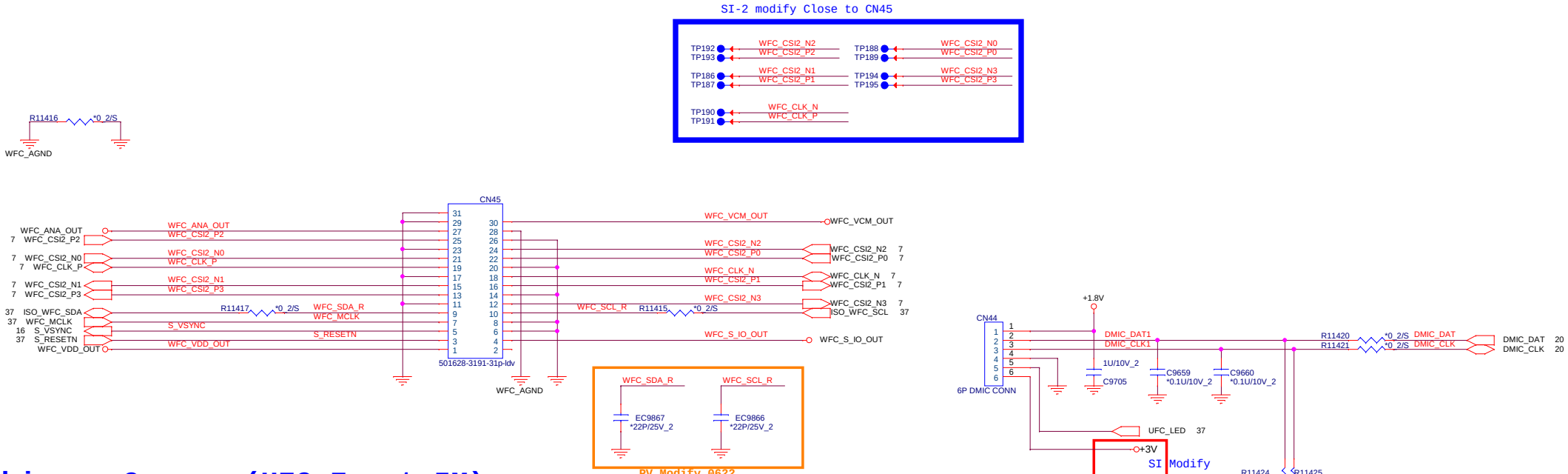
PROJECT : Millhone
Quanta Computer Inc.

NB5 HW

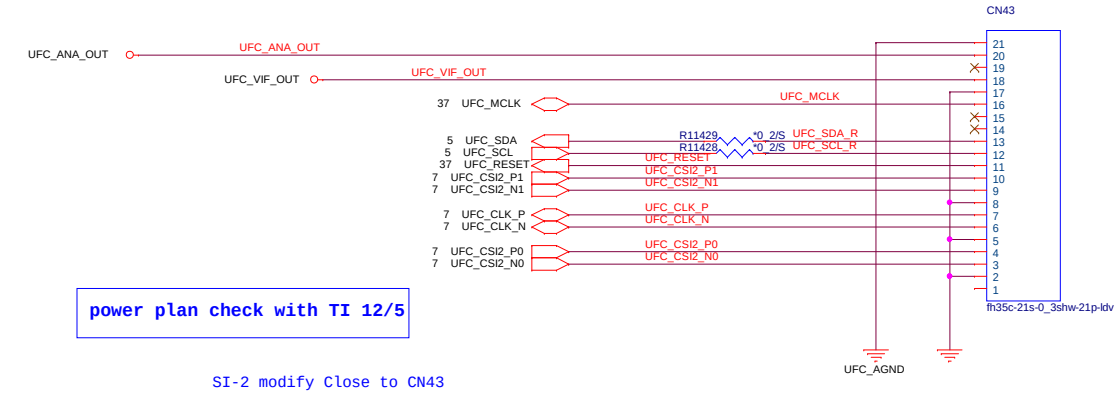
Size	Document Number	Rev
	eDP	A

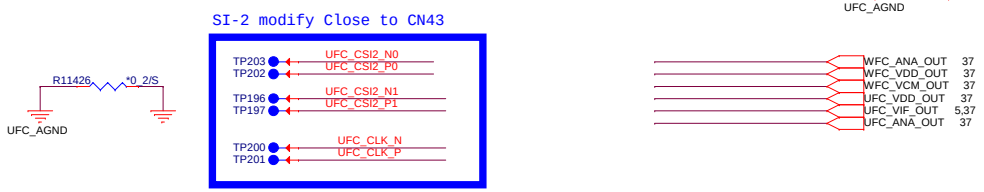
Date: Friday, August 28, 2015 Sheet 14 of 48

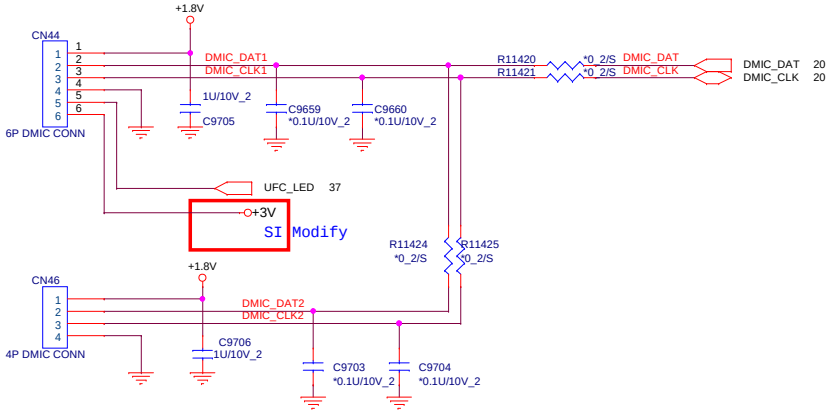
Chicony Camera (WFC,Rear 8M)



Chicony Camera (UFC,Front 5M)

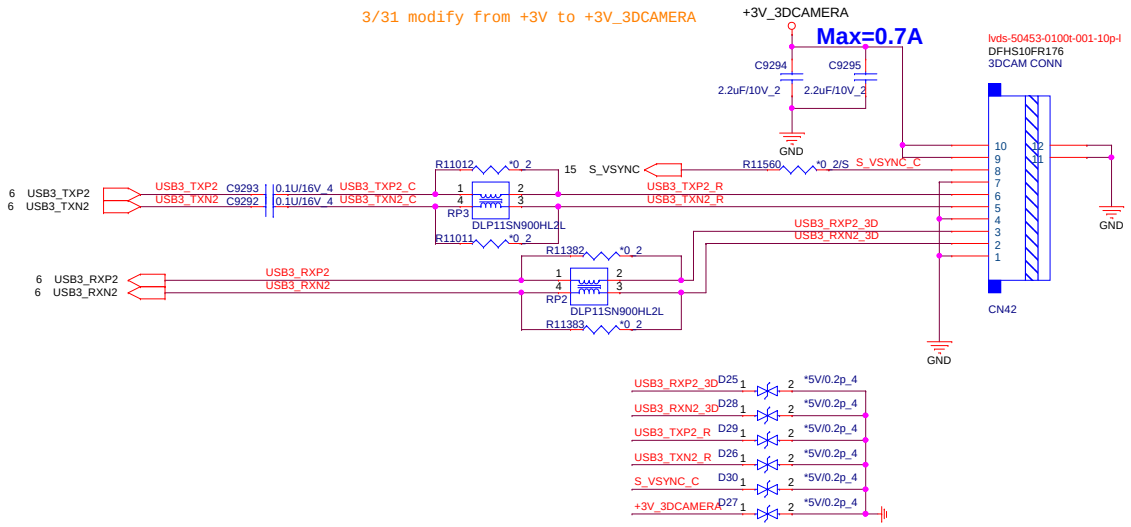






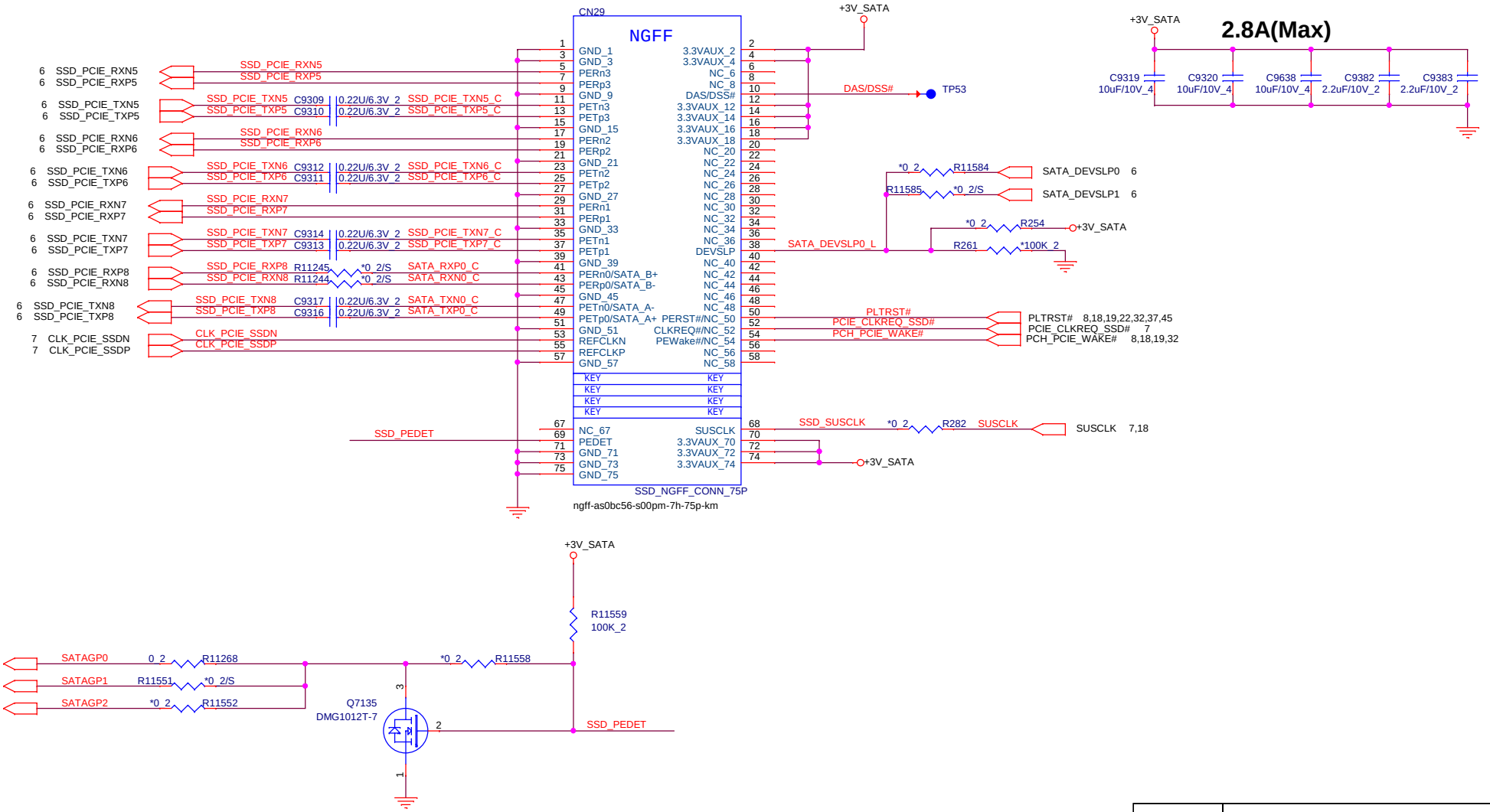
NB5 HW	PROJECT : Millhone Quanta Computer Inc.	
Size: Custom	Document Number: SkyCamera/DMIC	Rev: A
Date: Friday, August 28, 2015	Sheet 15 of 48	

Intel R200 3D camera



NB5 HW	**PROJECT : Millhone** Quanta Computer Inc.	
Size Custom	Document Number **Intel D R200 Camera**	Rev A
Date: Friday, August 28, 2015	Sheet 16 of 48	

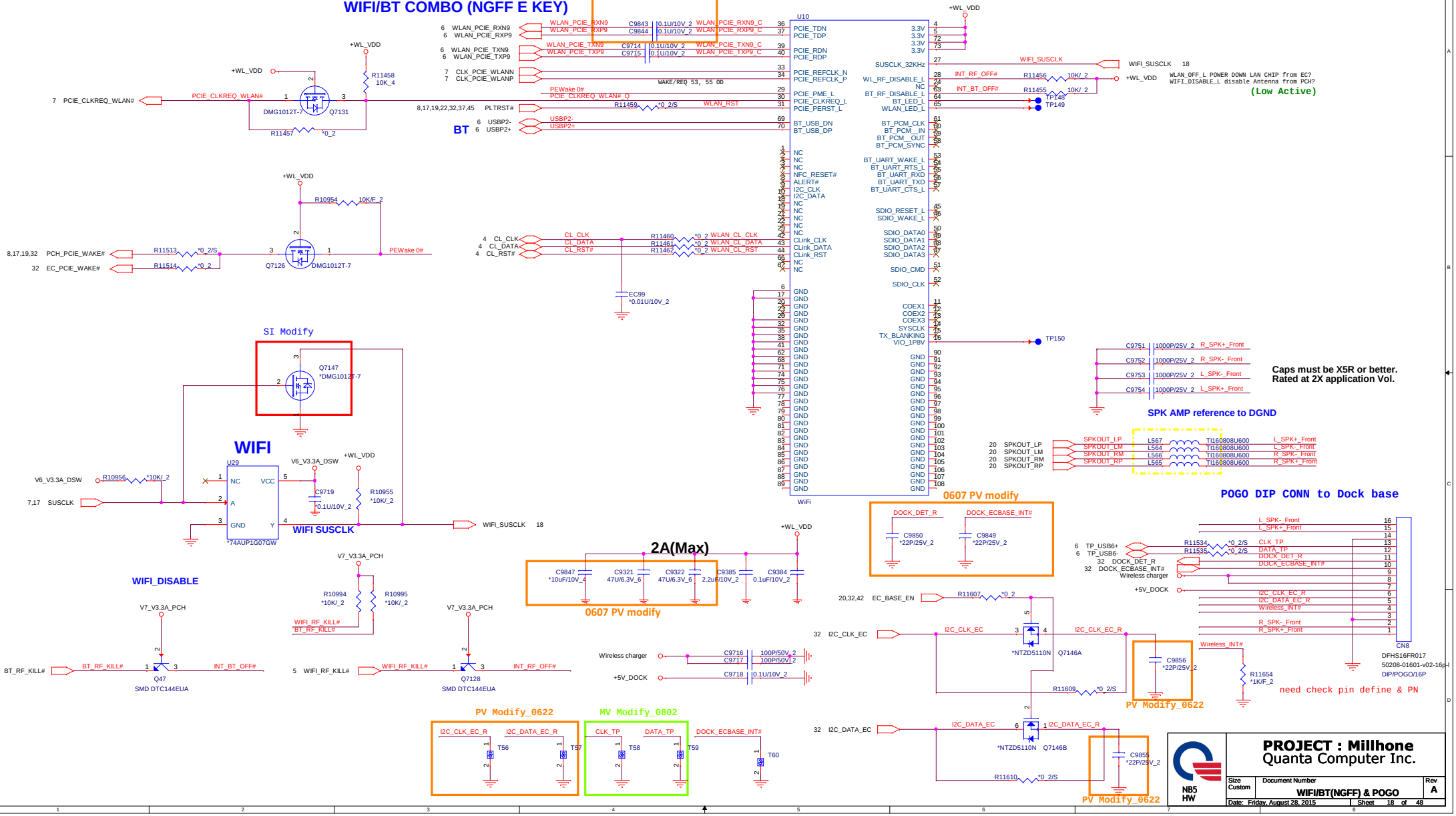
CONN: M KEY
MODULE: N/A



NB5 HW	**PROJECT : Millhone** Quanta Computer Inc.	
Size	Document Number **SSD (NGFF CONN)**	Rev **A**
Date: Friday, August 28, 2015	Sheet 17 of 48	

6/5 follow intel device guide

WIFI/BT COMBO (NGFF E KEY)



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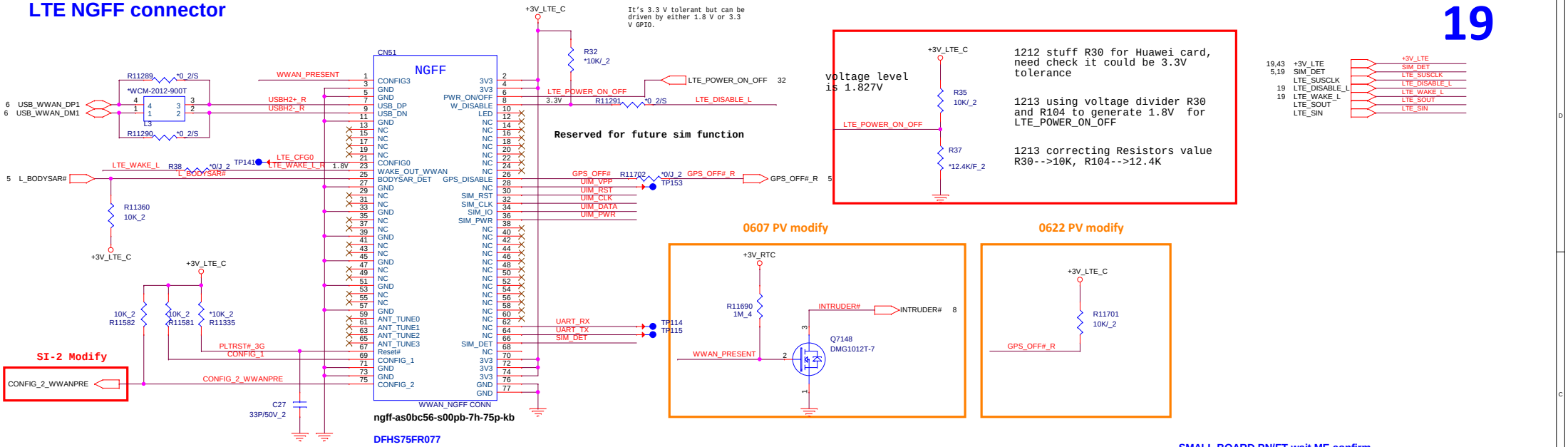
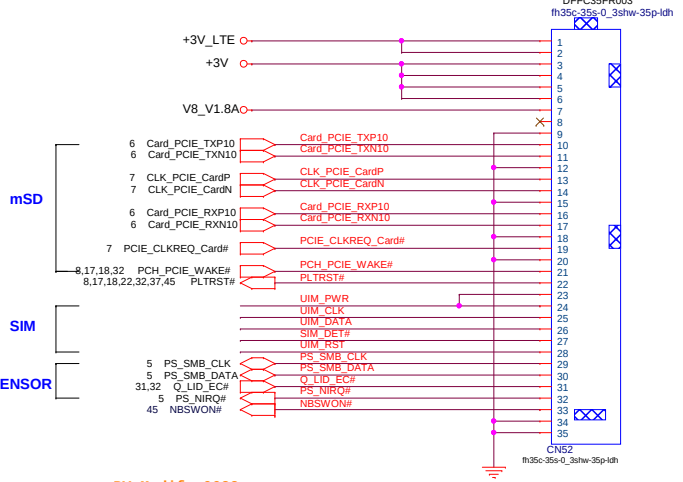
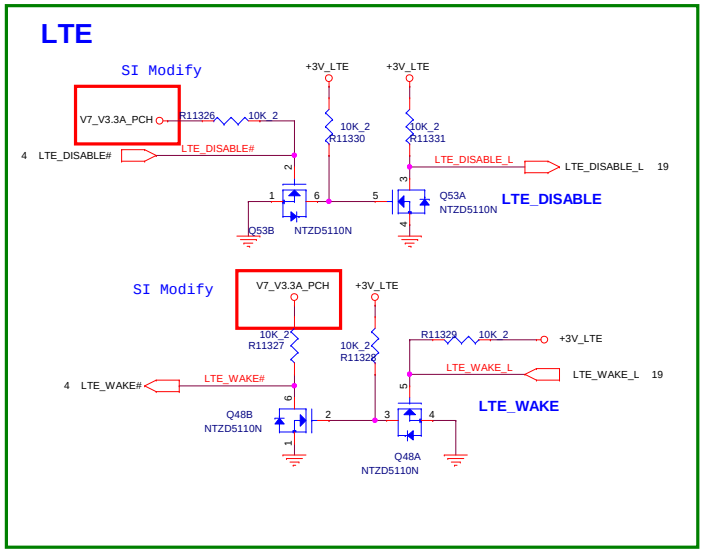
LTE NGFF connector

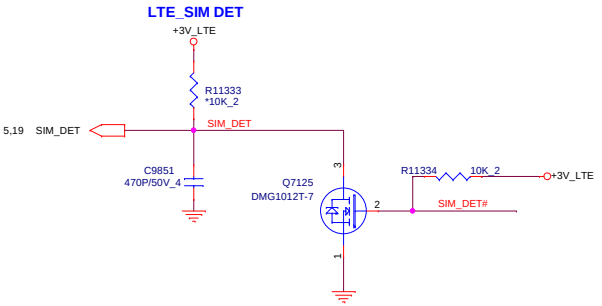


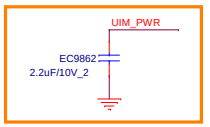
SMALL BOARD PN/FT wait ME confirm

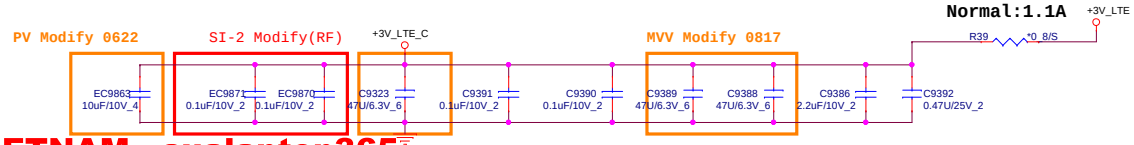


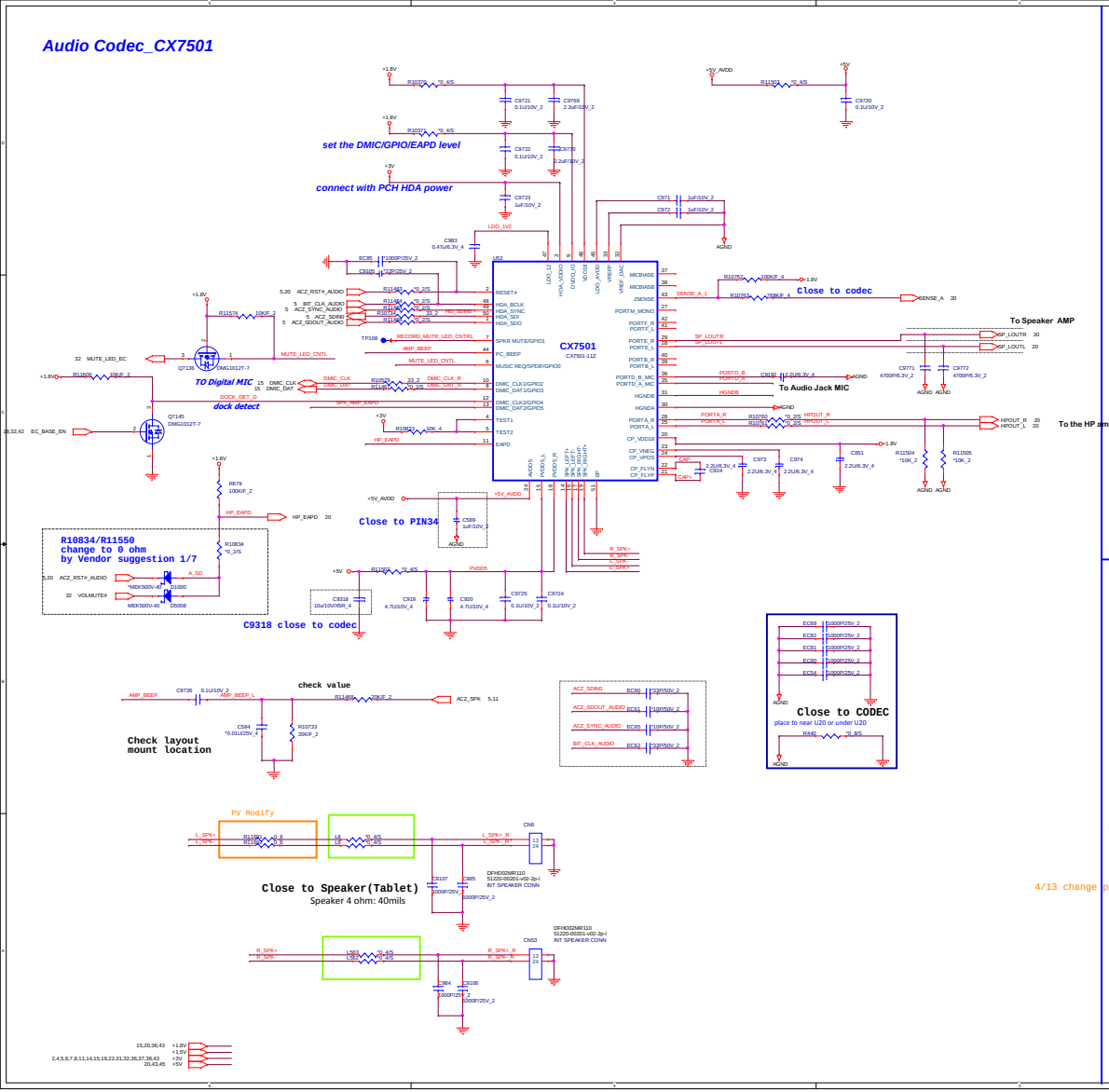
LTE

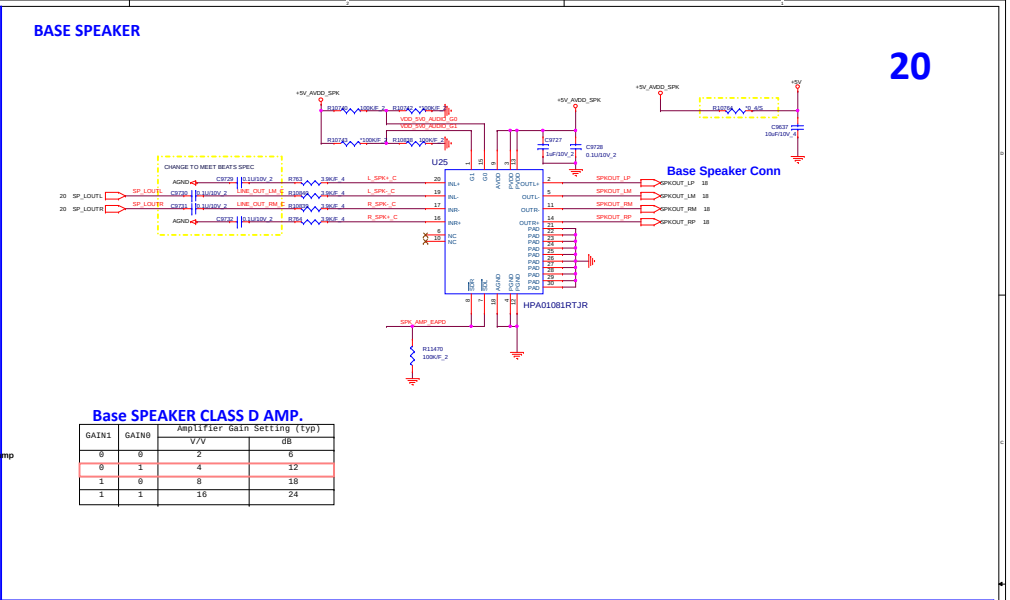




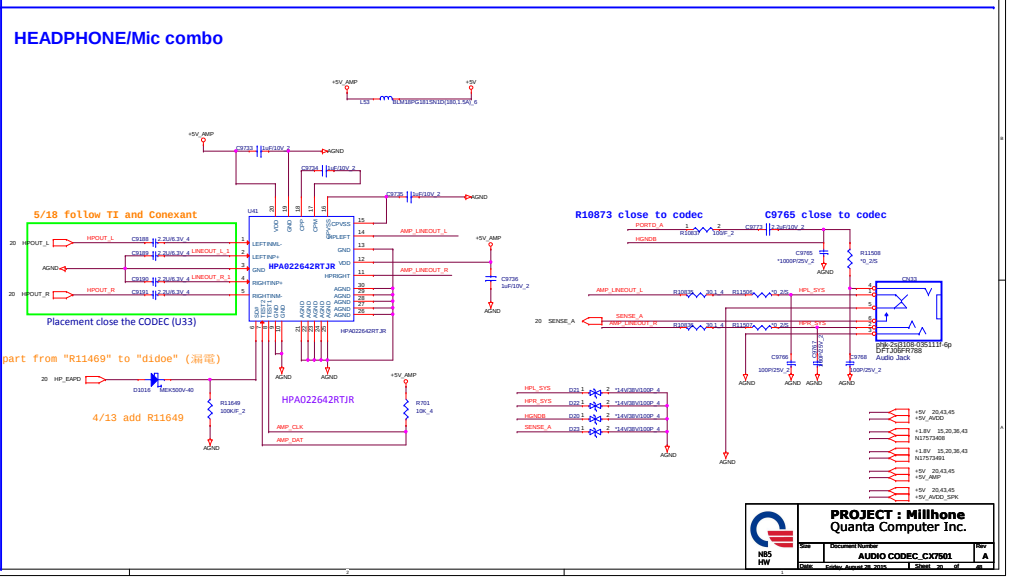








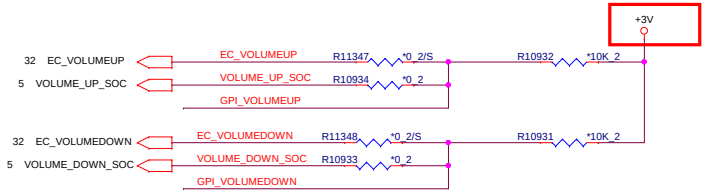
GAIN1	GAIN0	Amplifier Gain Setting (typ)	
		V/V	dB
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24



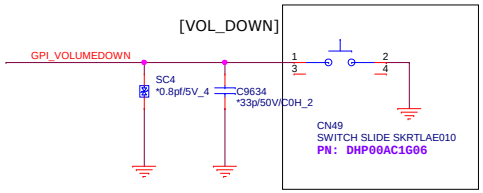
NB5
HW

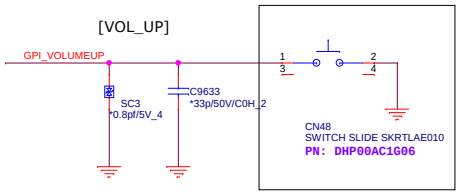
PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	NA	A
Date: Friday, August 28, 2015	Sheet 21 of 48	

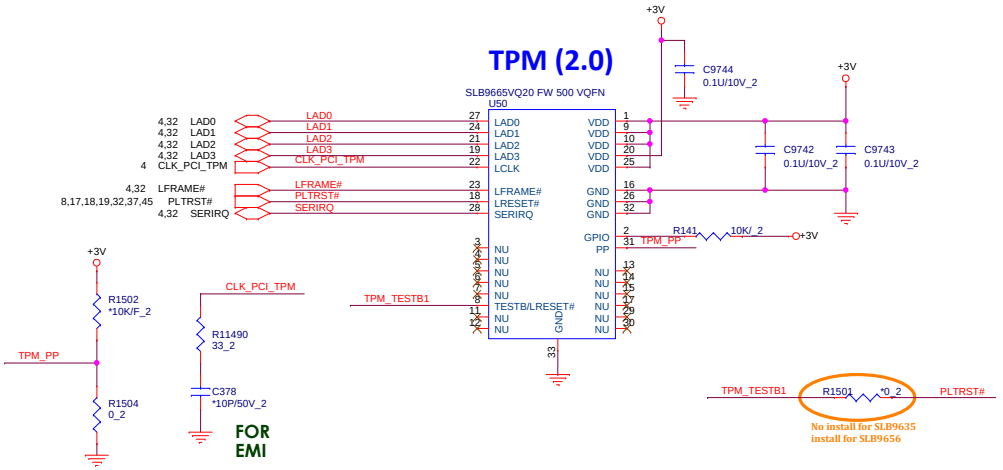


Volume BTN



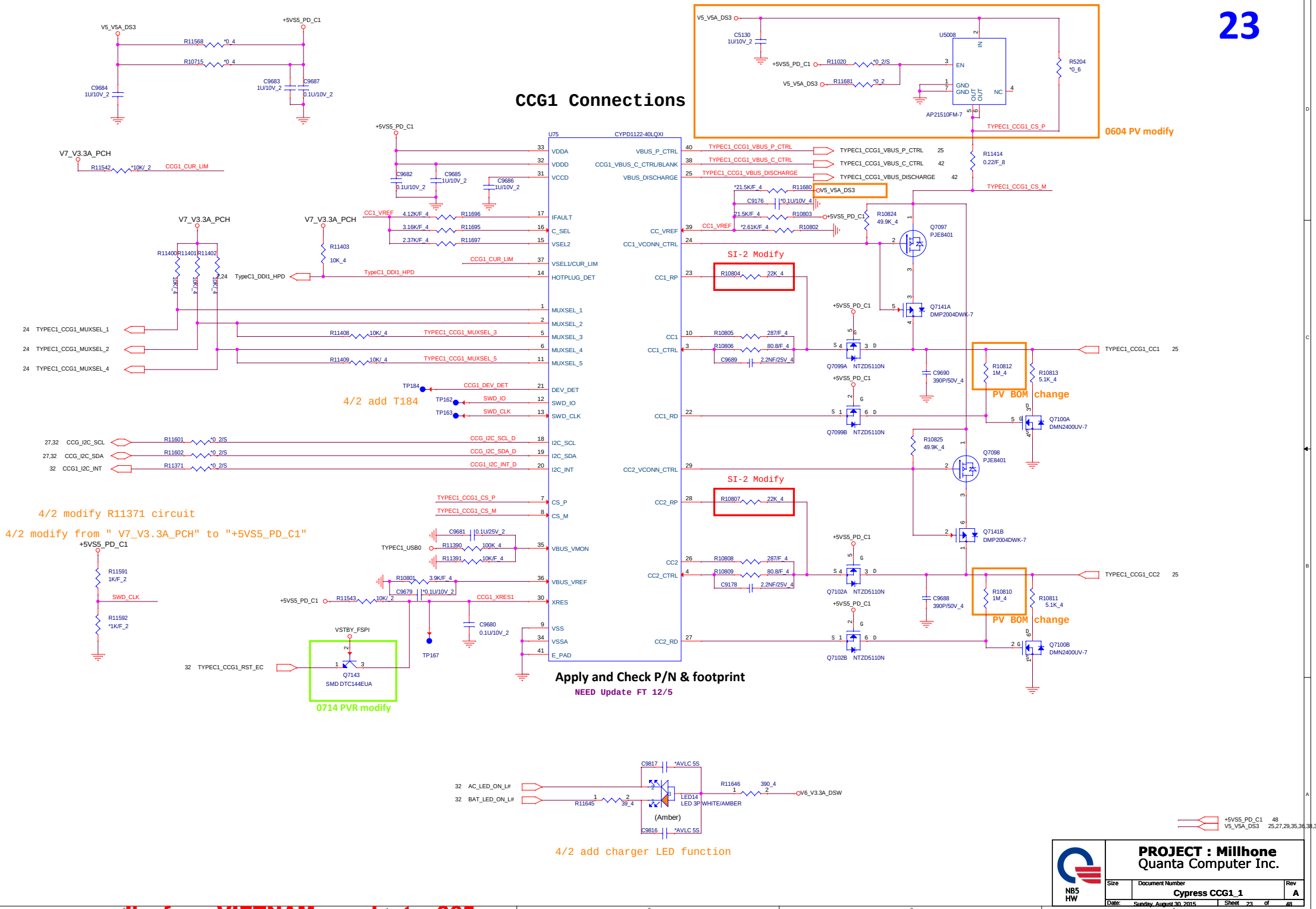


TPM (2.0)

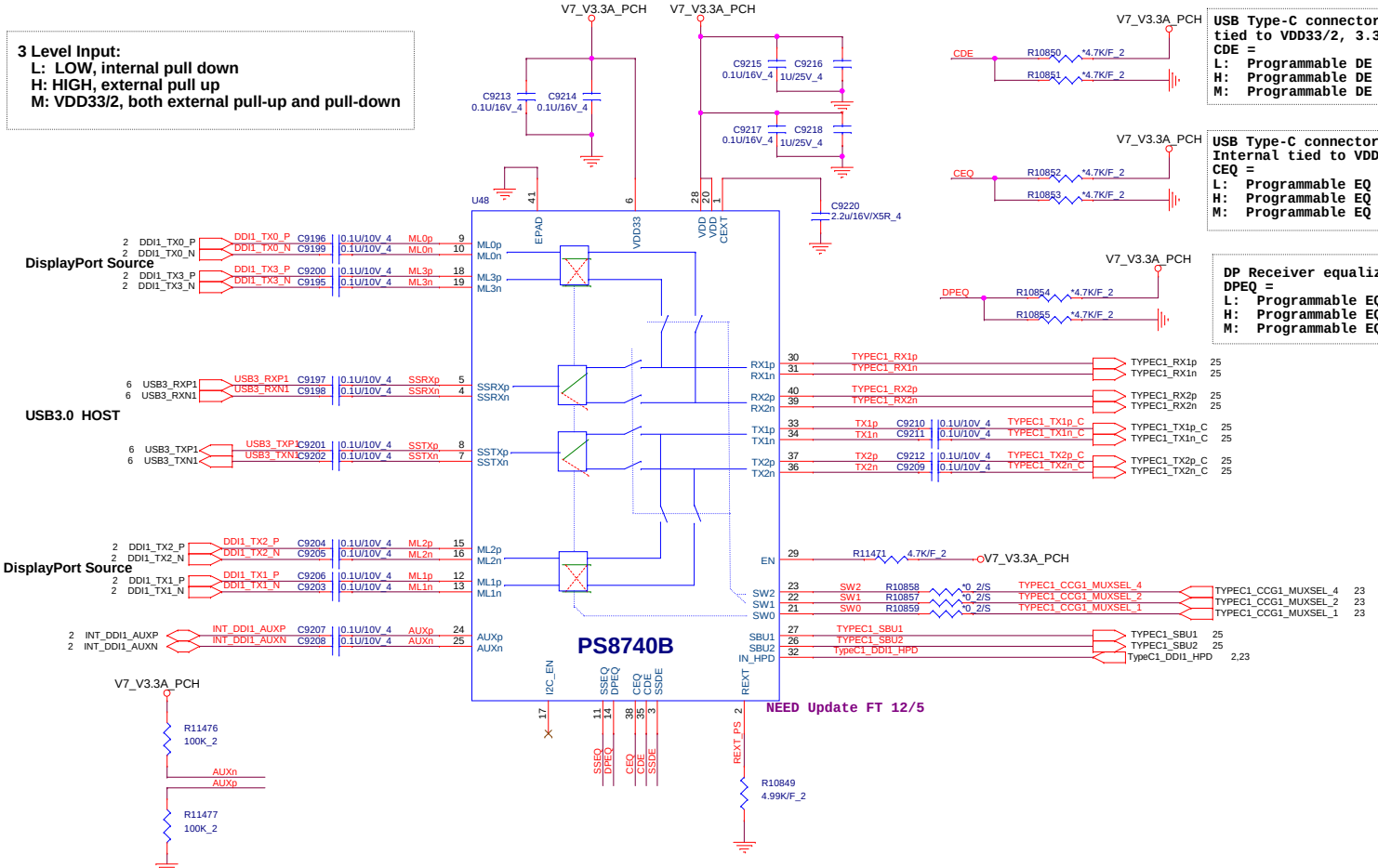


NB5 HW	PROJECT : Millhone Quanta Computer Inc.	
	Size / Document Number: Touch Screen/TPM/Volume	Rev: A
	Date: Sunday, August 30, 2015	Sheet 22 of 48

CCG1 Connections



3 Level Input:
- L: LOW, internal pull down
- H: HIGH, external pull up
- M: VDD33/2, both external pull-up and pull-down



USB Type-C connector facing TX channel De-emphasis setting; Internal tied to VDD33/2, 3.3V I/O.
CDE =
L: Programmable DE level#1
H: Programmable DE level#2
M: Programmable DE level#3 (default)

USB Type-C connector facing RX channel receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
CEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)

DP Receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
DPEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)

USB HOST facing TX channel De-emphasis setting; Internal tied to VDD33/2, 3.3V I/O.
SSDE =
L: Programmable DE level#1
H: Programmable DE level#2
M: Programmable DE level#3 (default)

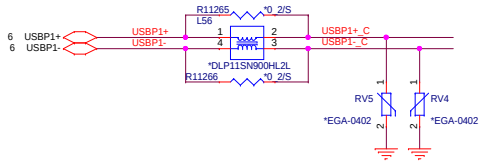
USB HOST facing RX channel receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
SSEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)

PS8740 Mode Selection			
SW2	SW1	SW0	
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	USB only on SS1 channels
L	H	H	USB only on SS2 channels
H	L	L	DP only; ML0 on SSRX2
H	L	H	DP only; ML0 on SSRX1
H	H	L	USB+2lanes DP;DP ML0 on SSRX2
H	H	H	USB+2lanes DP;DP ML0 on SSRX1

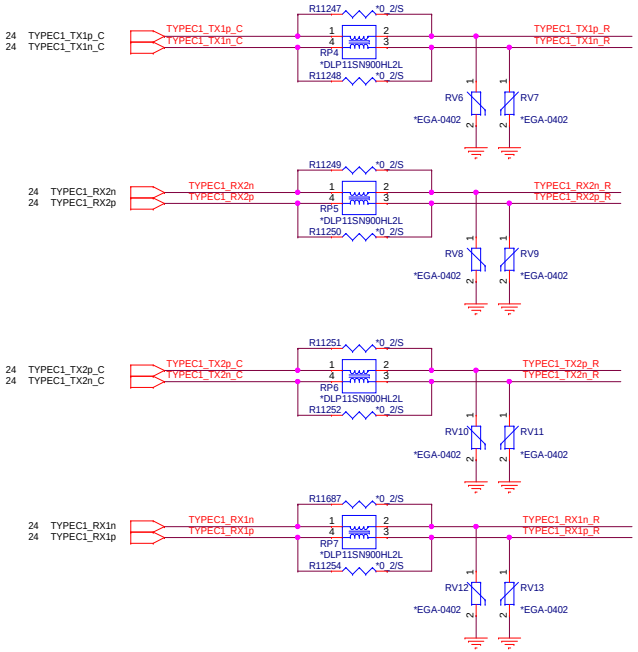
PS8740B Pin Control Mode

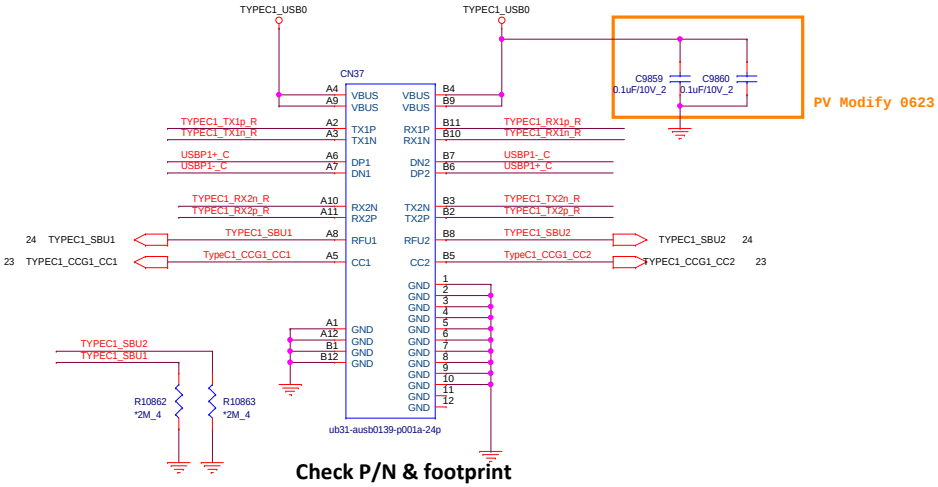
PROJECT : Millhone Quanta Computer Inc.		
NB5 HW	Size	Document Number: PS8740B Pin Control _1 — Rev: A
	Date: Sunday, August 30, 2015	Sheet 24 of 48

USB2.0 ESD



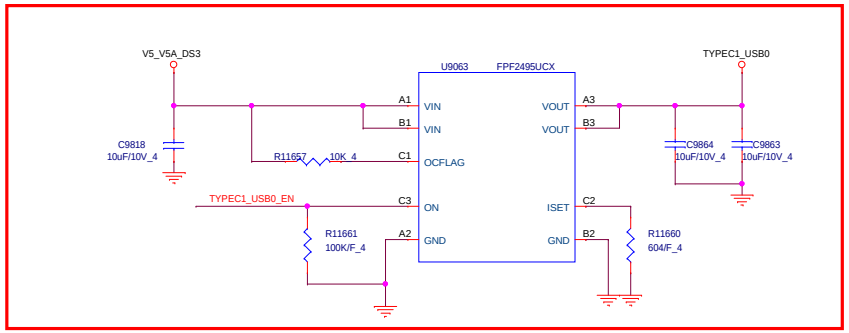
Type C1_HSIO_ ESD

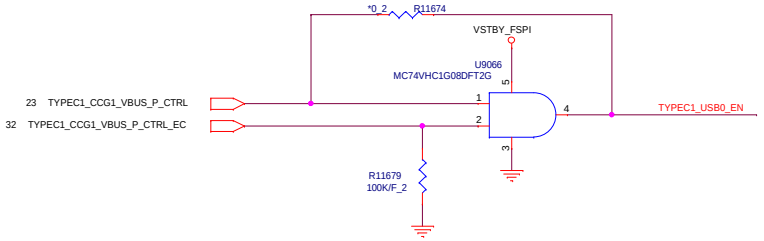




Check P/N & footprint

SI-2 Modify





NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	USB TYPE-C_1	A
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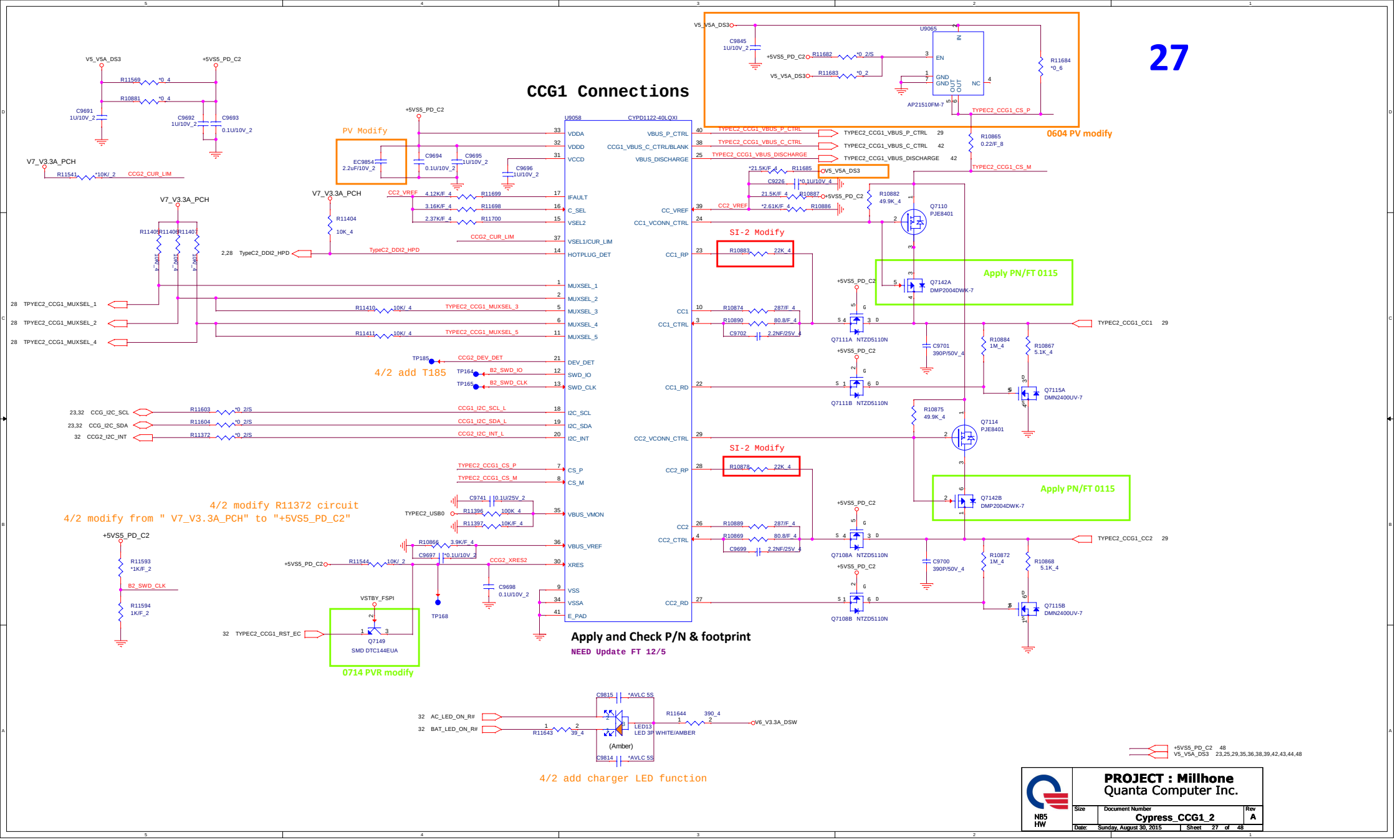
NB5
HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	VBUS Provider _1	A
Date: Friday, August 28, 2015	Sheet 26 of 48	



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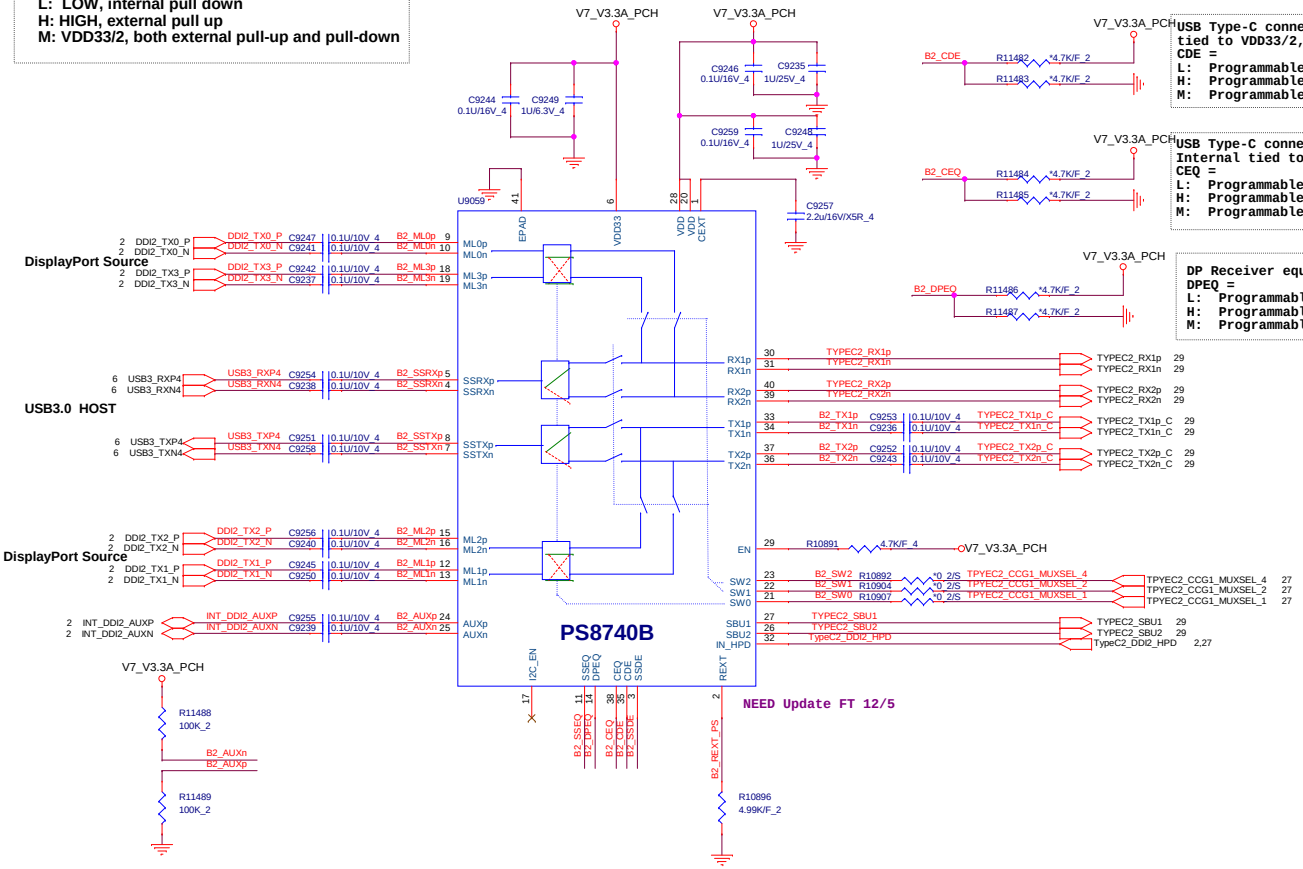
3 Level Input:
L: LOW, internal pull down
H: HIGH, external pull up
M: VDD33/2, both external pull-up and pull-down



USB Type-C connector facing TX channel De-emphasis setting; Internal tied to VDD33/2, 3.3V I/O.
CDE =
L: Programmable DE level#1
H: Programmable DE level#2
M: Programmable DE level#3 (default)

USB Type-C connector facing RX channel receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
CEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)

DP Receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
DPEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)

USB HOST facing TX channel De-emphasis setting; Internal tied to VDD33/2, 3.3V I/O.
SSDE =
L: Programmable DE level#1
H: Programmable DE level#2
M: Programmable DE level#3 (default)

USB HOST facing RX channel receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
SSEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)

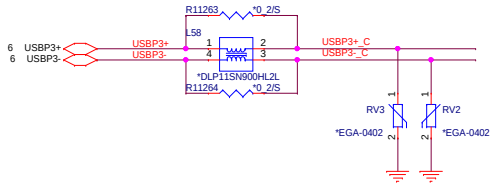
PS8740 Mode Selection			
SW2	SW1	SW0	
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	USB only on SS1 channels
L	H	H	USB only on SS2 channels
H	L	L	DP only; ML0 on SSRX2
H	L	H	DP only; ML0 on SSRX1
H	H	L	USB+2lanes DP;DP ML0 on SSRX2
H	H	H	USB+2lanes DP;DP ML0 on SSRX1

PS8740B Pin Control Mode

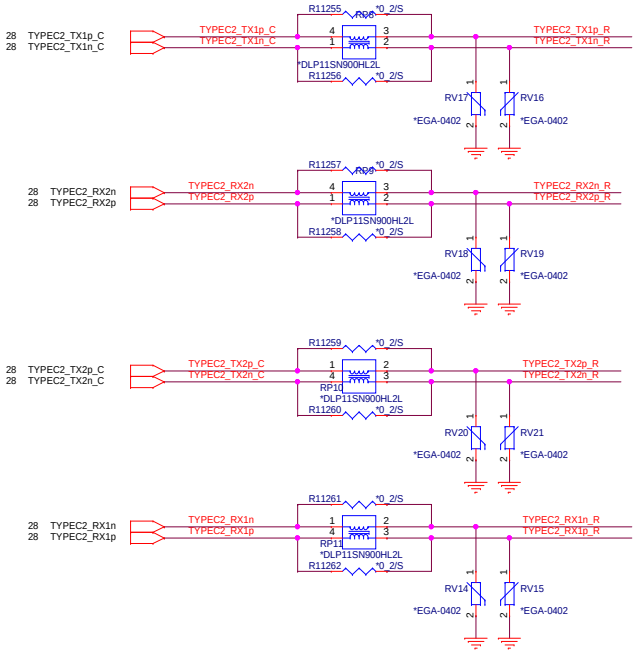
PROJECT : Millhone
Quanta Computer Inc.

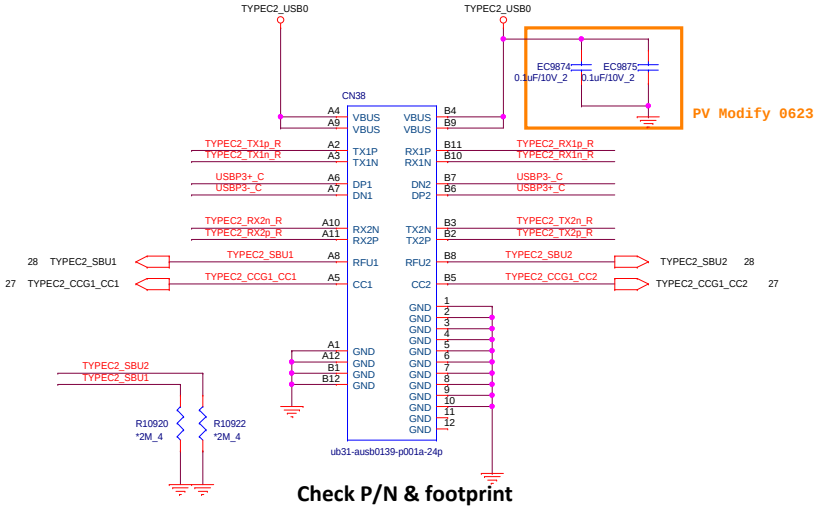
Size	Document Number	Rev
NB5 HW	PS8740B Pin Control_2	A
Date: Sunday, August 30, 2015	Sheet 28 of 48	

USB2.0_ ESD



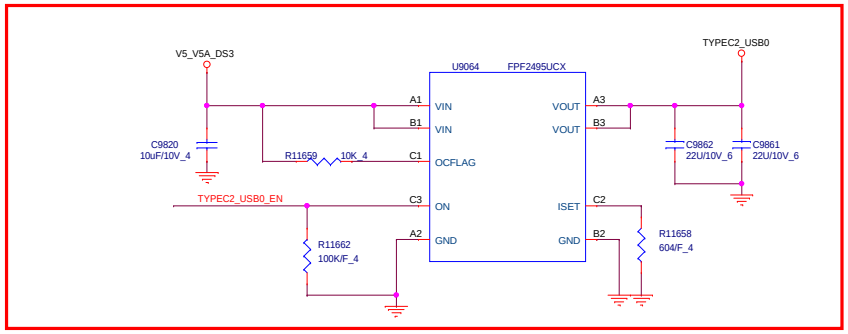
Type C2_HSIO_ ESD

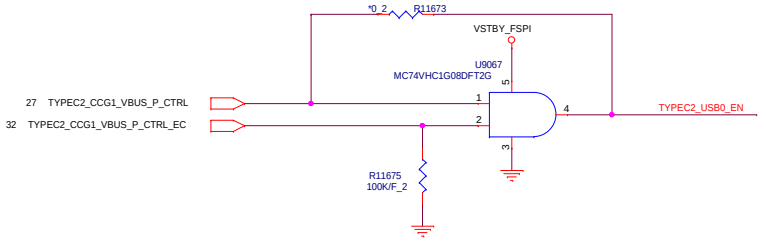




Check P/N & footprint

SI-2 Modify





NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

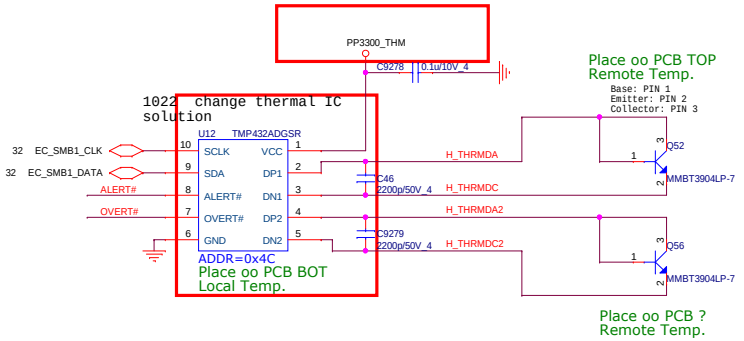
Size	Document Number	Rev
	USB TYPE-C_2	A
Date: Sunday, August 30, 2015	Sheet 29 of 48	

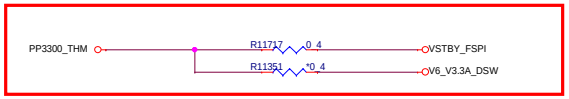
NB5
HW

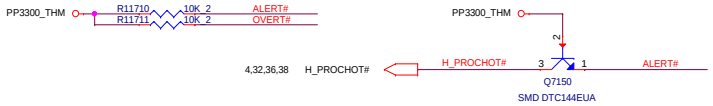
PROJECT : Millhone
Quanta Computer Inc.

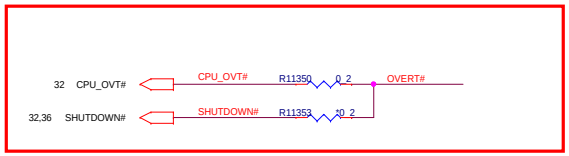
Size	Document Number	Rev
	VBUS Provider_2	A
Date: Friday, August 28, 2015	Sheet 30 of 48	

Thermal Sensor(THM)

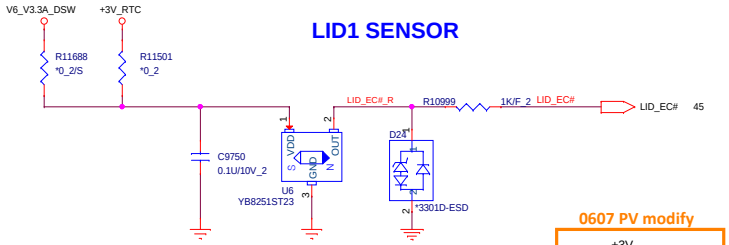




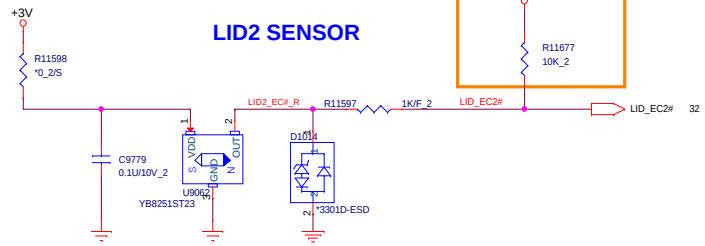




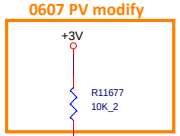
LID1 SENSOR



LID2 SENSOR

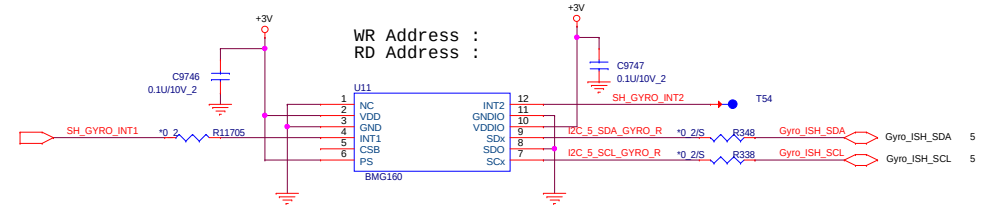


0607 PV modify



4/9 change net from "LID2_EC#_R" to "LID_EC#_R"

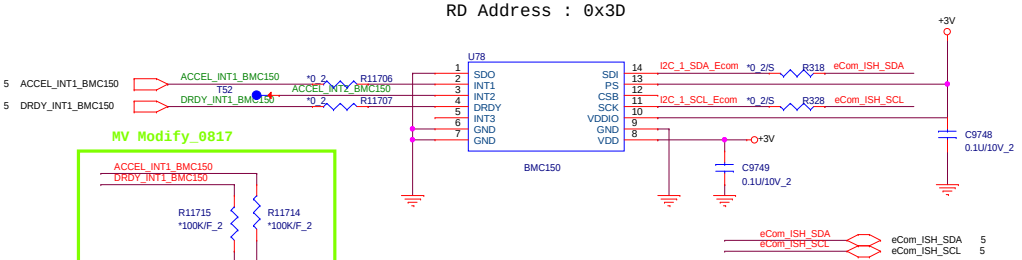
Gyroscope(BMG160)



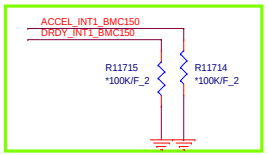
E-compass/Magnetometer/Accelerometer (BMC150)

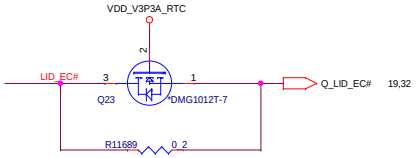
Keepout area is around 10mm

WR Address : 0x3C
RD Address : 0x3D



MV Modify_0817





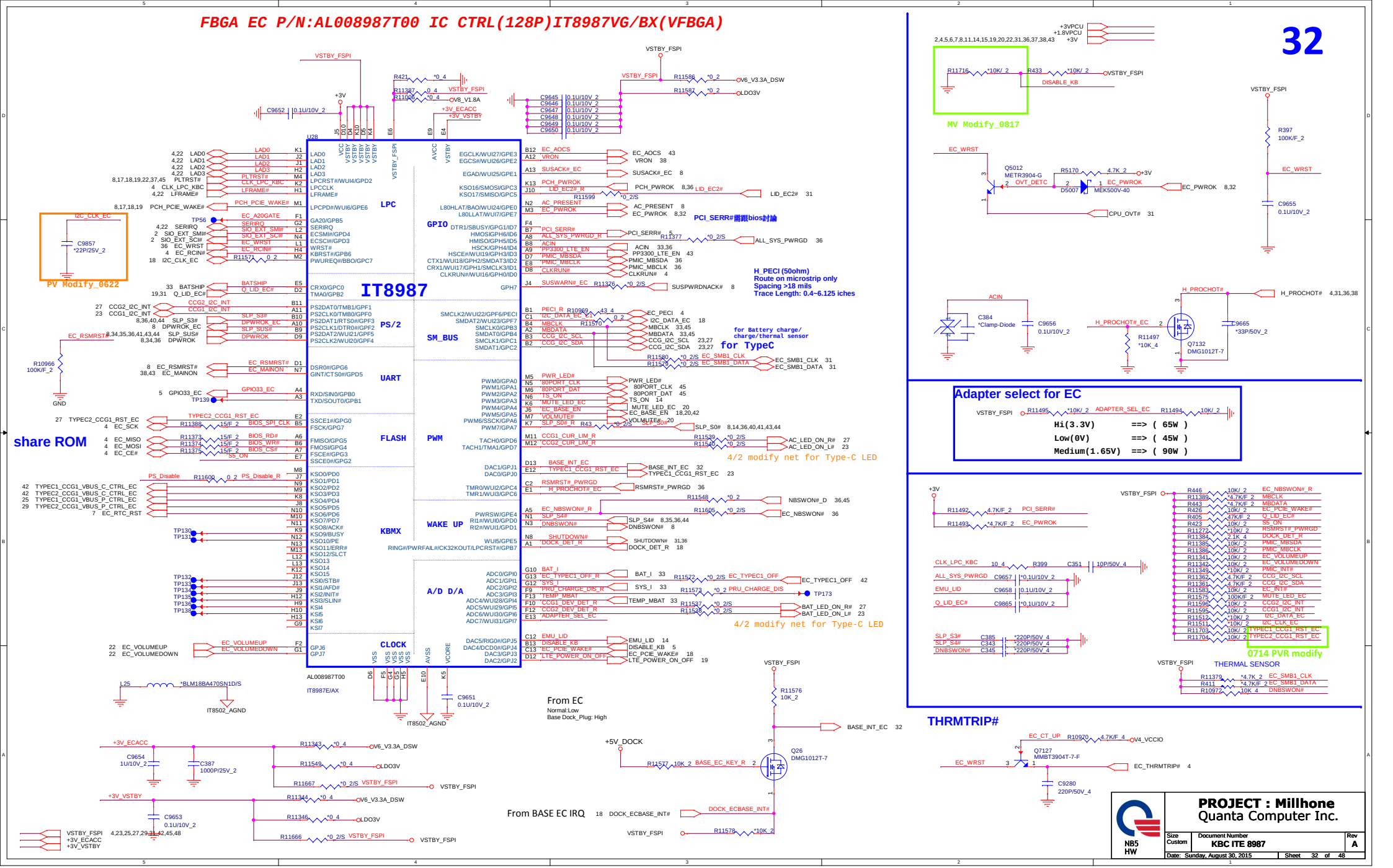
V6_V3.3A_DSW 4,8,10,18,23,27,32,34,35,36,40,41,43,48
PP3300_THM

NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	Gyro/eCompass	A
Date: Friday, August 28, 2015	Sheet 31 of 48	

FBGA EC P/N:AL008987T00 IC CTRL(128P)IT8987VG/BX(VFBGA)



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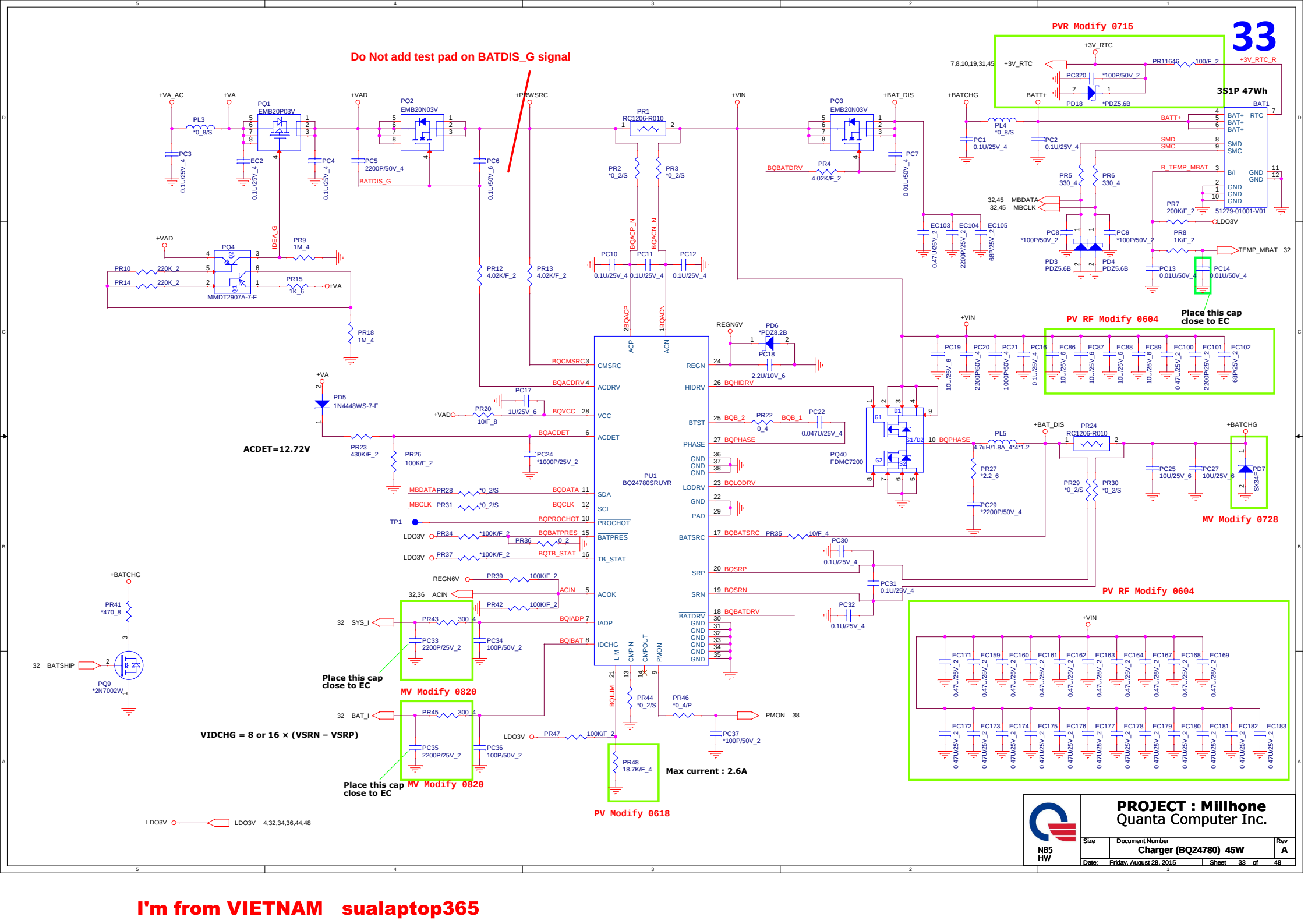
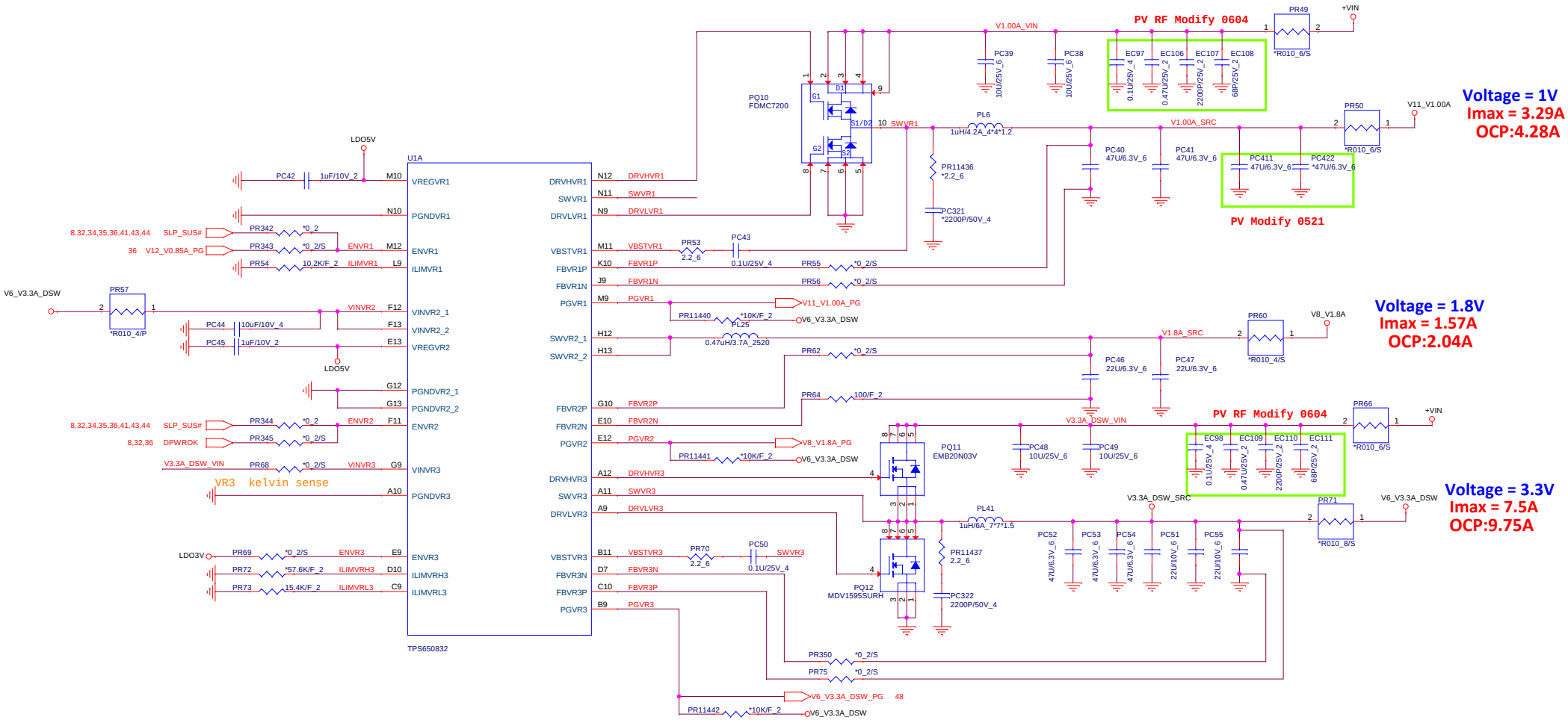
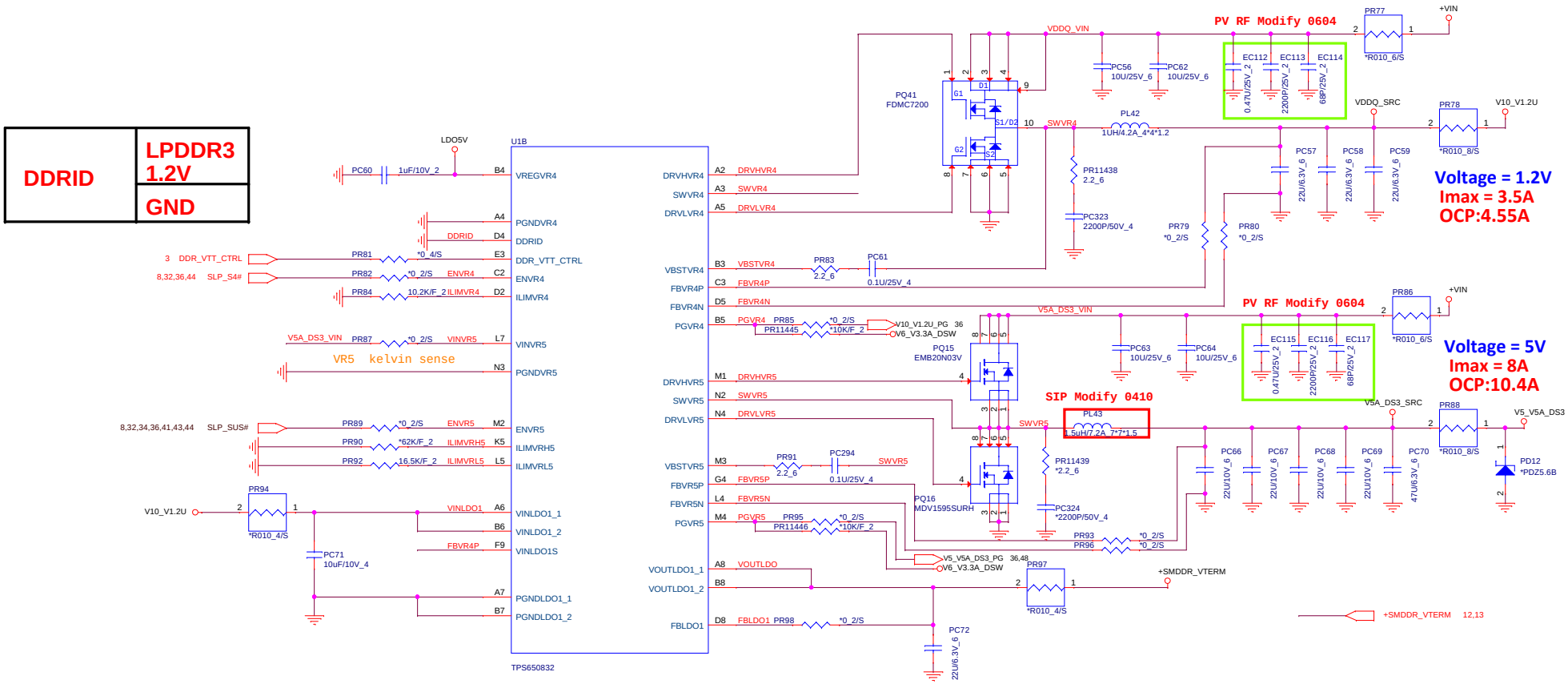
NB5 HW	PROJECT : Millhone Quanta Computer Inc.		
	Size: Custom	Document Number: KBC ITE 8987	Rev: A
	Date: Sunday, August 30, 2015	Sheet 32 of 48	

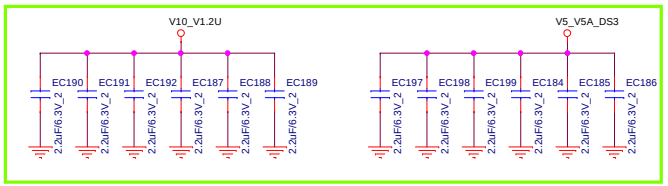

33
PVR Modify 0715
Do Not add test pad on BATDIS_G signal
3S1P 47Wh
PV RF Modify 0604
Place this cap close to EC
MV Modify 0728
PV RF Modify 0604
ACDET=12.72V
VIDCHG = 8 or 16 × (VSRN − VSRP)
MV Modify 0820
MV Modify 0820
PV Modify 0618
Max current : 2.6A
PROJECT : Millhone
Quanta Computer Inc.
NB5 HW
Charger (BQ24780)_45W
Friday, August 28, 2015
I'm from VIETNAM sualaptop365



DDRID	LPDDR3 1.2V
	GND



PV RF Modify 0604



V5_V5A_DS3 23,25,27,29,36,38,39,42,43,44,48
V5A_DS3_SRC

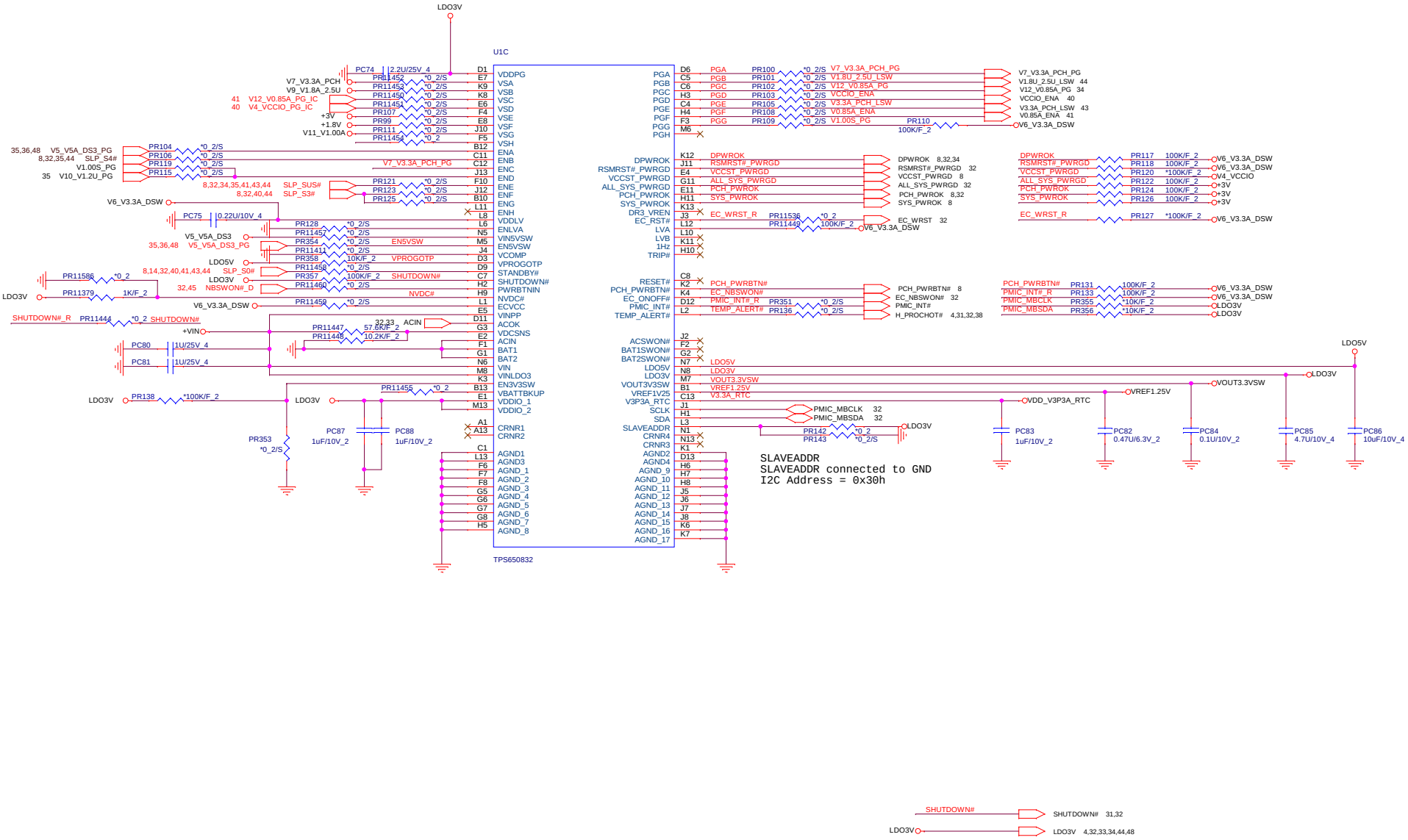
V10_V1.2U 10,12,13,44
VDDQ_SRC

+SMDDR_VTERM 12,13
VOUTLDO

NB5 HW

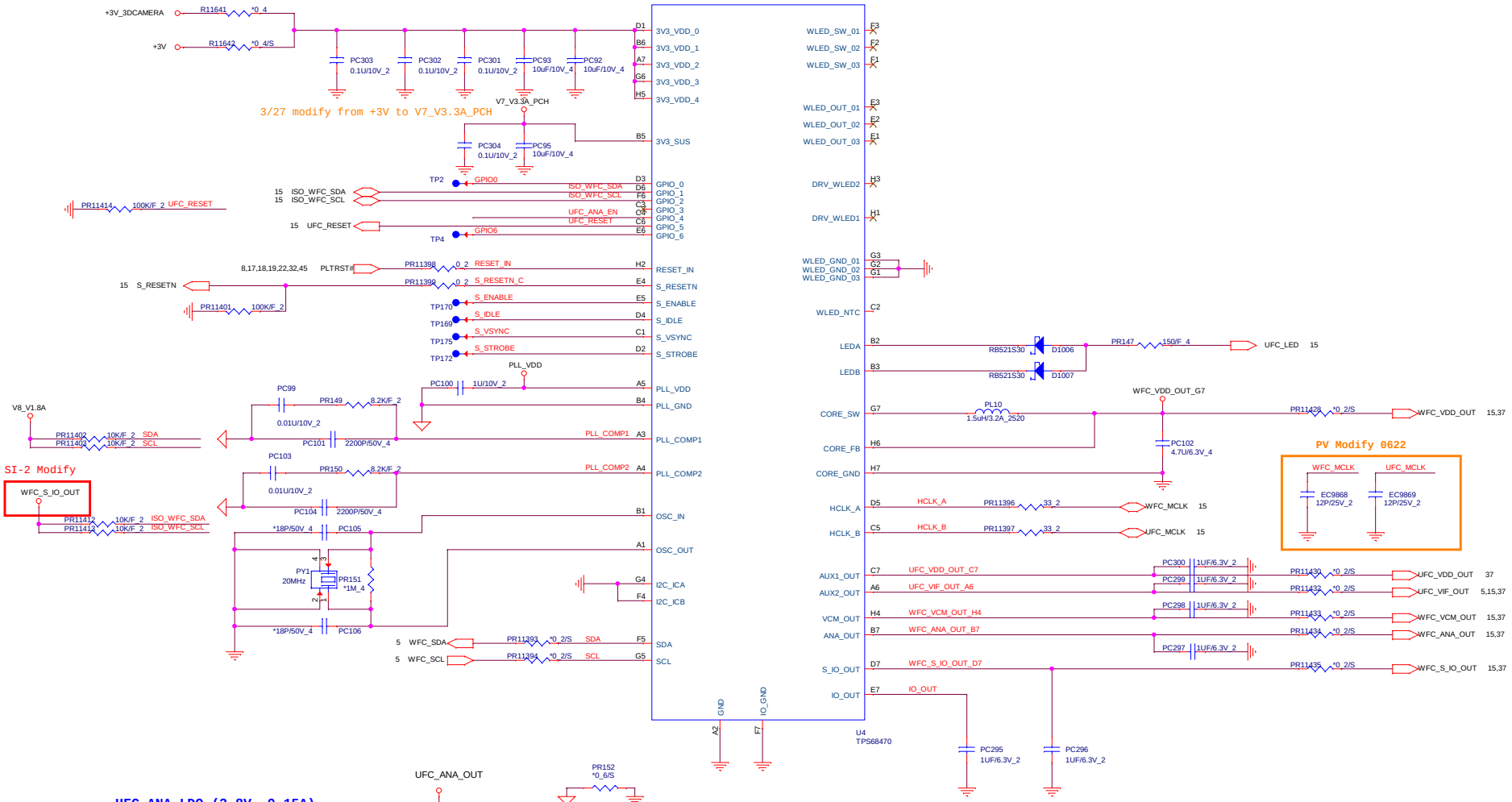
PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	System PMIC (TPS650832_2)	A
Date: Friday, August 28, 2015	Sheet 35 of 48	

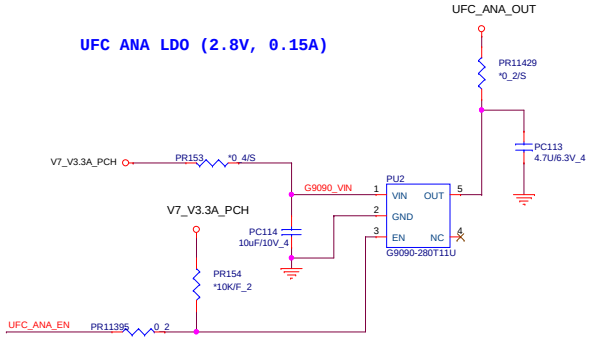


NB5 HW	PROJECT : Millhone Quanta Computer Inc.		
Size	Document Number System PMIC (TPS650832_3)	Rev A	
Date: Friday, August 28, 2015	Sheet 36 of 48		

3/27 modify from V7_V3.3A_PCH to +3V
4/1 add R11641/11642 reserve +3V_3DCAMERA



UFC ANA LDO (2.8V, 0.15A)



Net name	V(Typ.)	A(Typ.)
UFC_VDD_OUT	1.2V	0.15A
UFC_VIF_OUT	1.8V	0.05A
UFC_ANA_OUT	2.8V	A
WFC_VDD_OUT	1.2V	A
WFC_S_IO_OUT	1.8V	A
WFC_VCM_OUT	2.8V	0.5A
WFC_ANA_OUT	2.8V	0.2A

UFC_VDD_OUT 37
UFC_VDD_OUT_C7
WFC_VDD_OUT 15,37
WFC_VDD_OUT_G7
WFC_VCM_OUT 15,37
WFC_VCM_OUT_H4
WFC_ANA_OUT 15,37
WFC_ANA_OUT_B7
WFC_S_IO_OUT 15,37
WFC_S_IO_OUT_D7
UFC_VIF_OUT 5,15,37
UFC_VIF_OUT_A6
UFC_ANA_OUT 15
N18364051

PROJECT : Millhone
Quanta Computer Inc.
NB5 HW
Size
Document Number SKYCAM (TPS68470)
Rev A
Date: Friday, August 28, 2015
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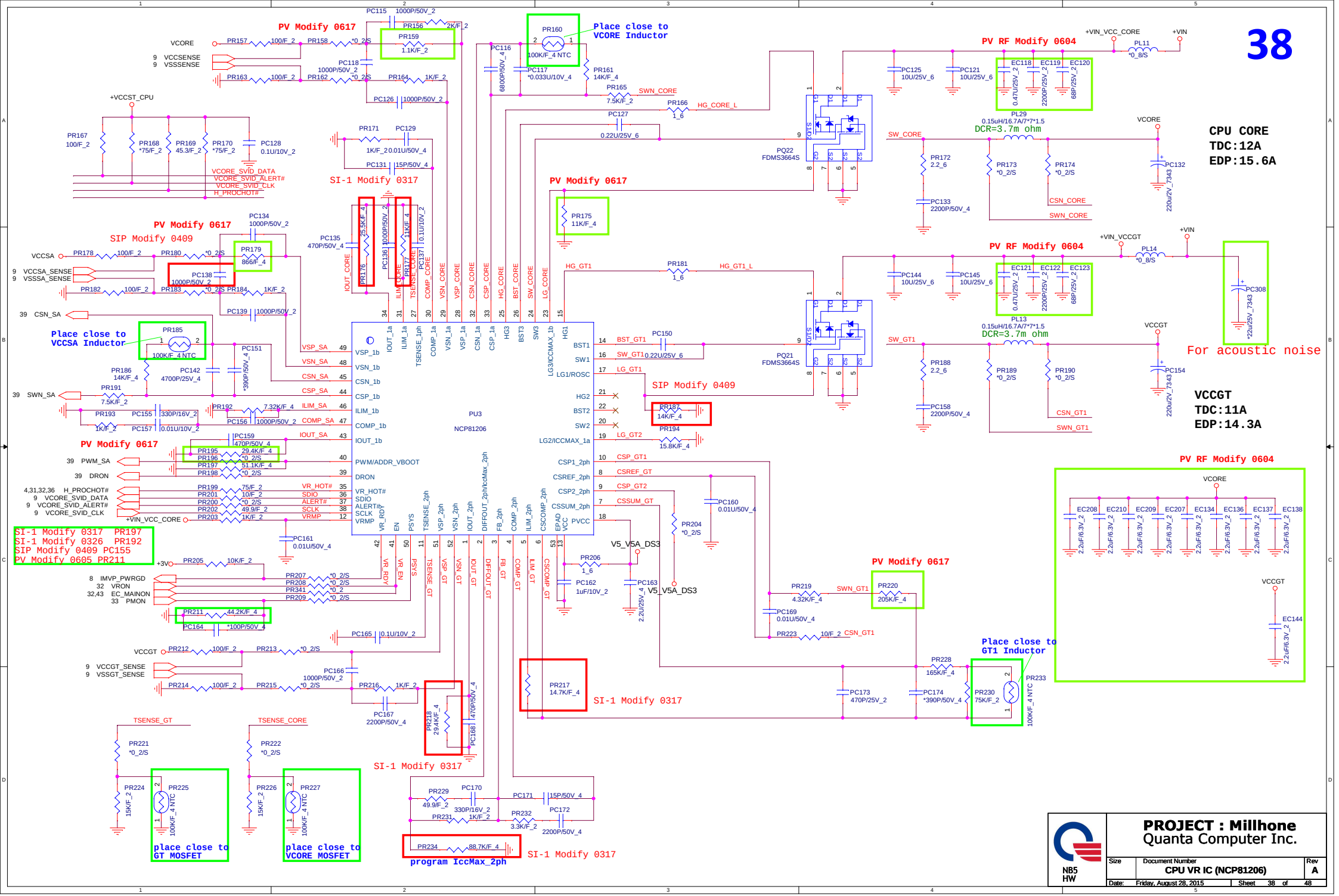
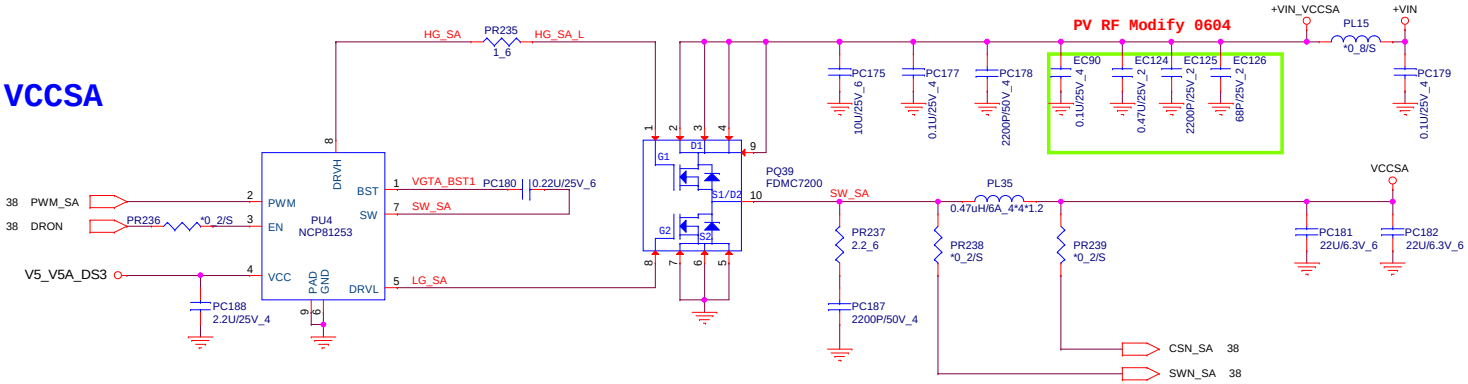
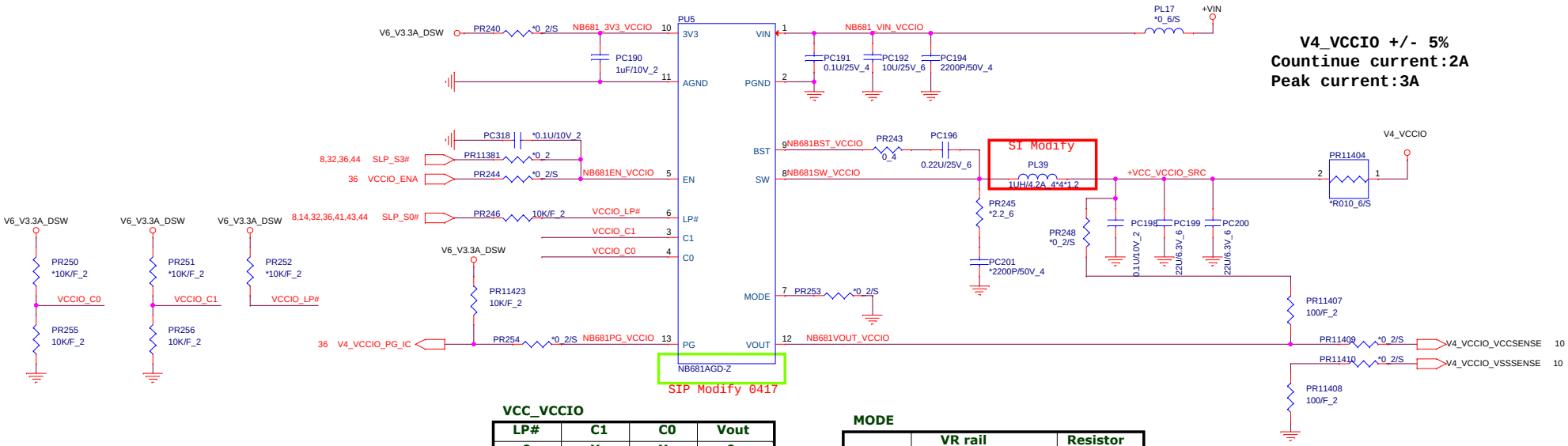

38
CPU CORE
TDC:12A
EDP:15.6A
VCCGT
TDC:11A
EDP:14.3A
For acoustic noise
PV Modify 0617
PV RF Modify 0604
SIP Modify 0409
SI-1 Modify 0317
Place close to VCORE Inductor
Place close to VCCSA Inductor
Place close to GT1 Inductor
place close to GT MOSFET
place close to VCORE MOSFET
program IccMax_2ph
PU3
NCP81206
SI-1 Modify 0317 PR197
SI-1 Modify 0326 PR192
SIP Modify 0409 PC155
PV Modify 0605 PR211
PROJECT : Millhone
Quanta Computer Inc.
NB5 HW
CPU VR IC (NCP81206)
Size
Document Number
Rev
A
Date: Friday, August 28, 2015
Sheet 38 of 48
I'm from VIETNAM sualaptop365

VCCSA



VCCSA
TDC:4A
EDP:5.2A

NB5 HW	**PROJECT : Millhone** Quanta Computer Inc.	
Size	Document Number +VCCSA (NCP81253)	Rev A
Date: Friday, August 28, 2015	Sheet 39 of 48	



VCC_VCCIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

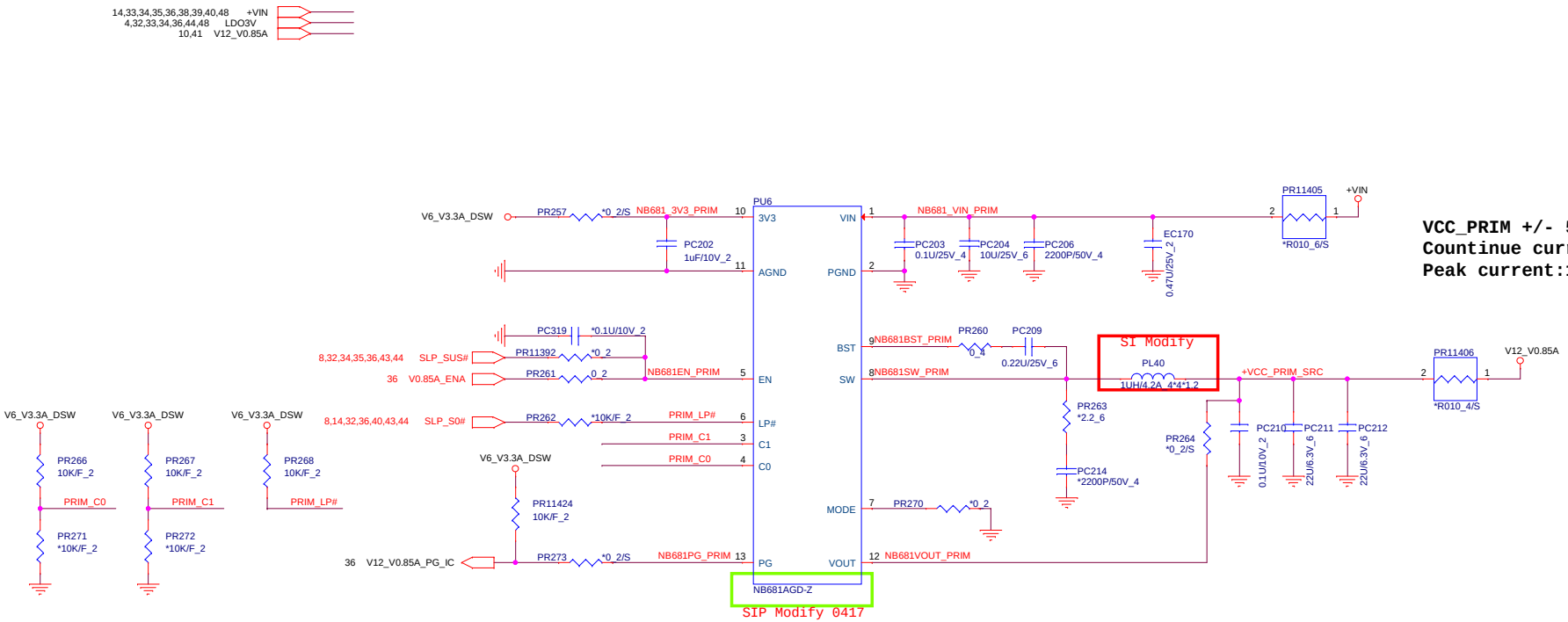
MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	+VCC_VCCIO (NB681)	A
Date: Friday, August 28, 2015	Sheet 40 of 48	



VCC_PRIM +/- 5%
Countinue current:1A
Peak current:1.5A

VccPRIM_CORE

LP#	C1	C0	Vout
0	X	X	0.7
1	0	0	0.85
1	0	1	0.9
1	1	0	0.95
1	1	1	1.00

MODE

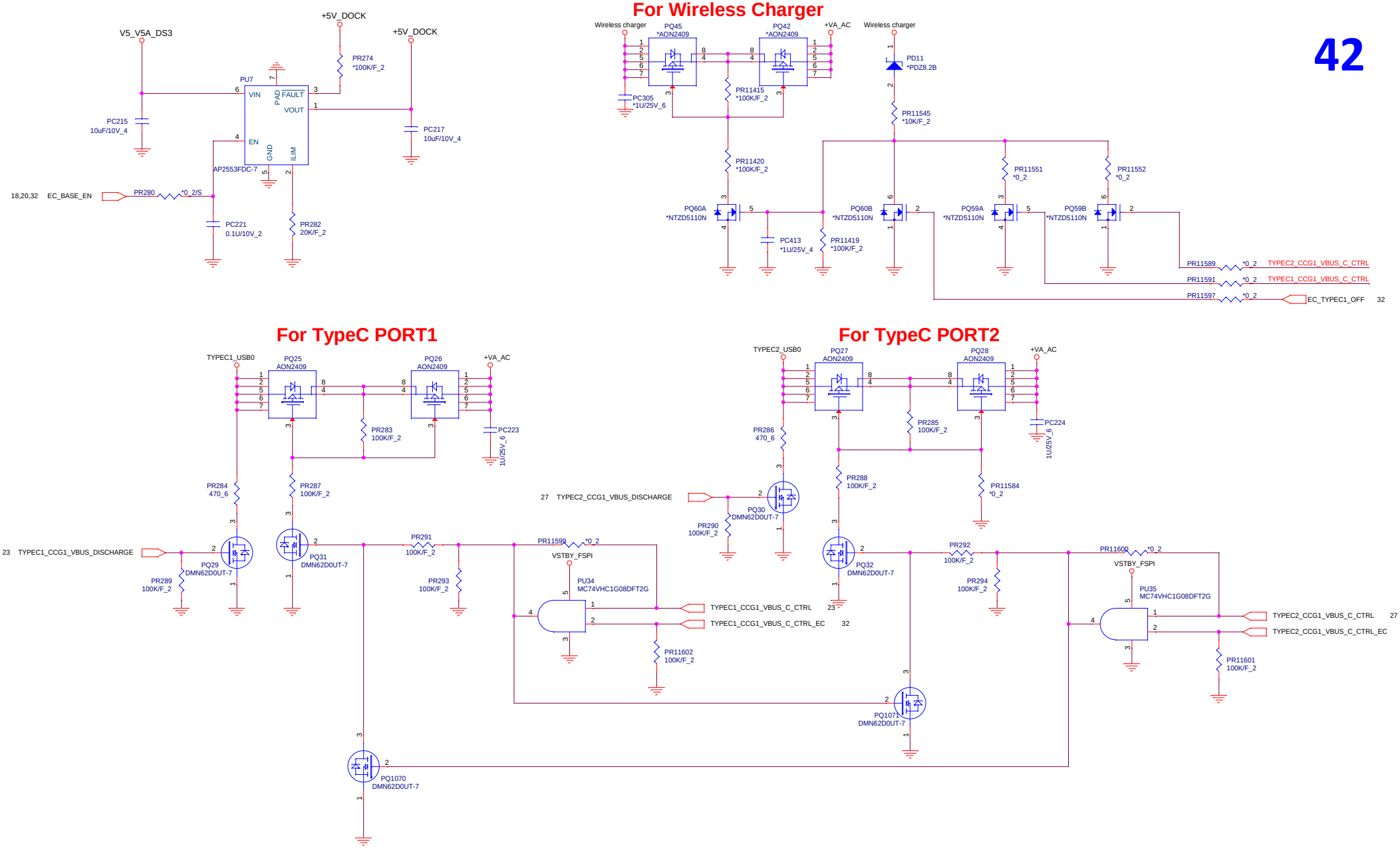
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

V12_V0.85A 10,41
+VCC_PRIM_SRC

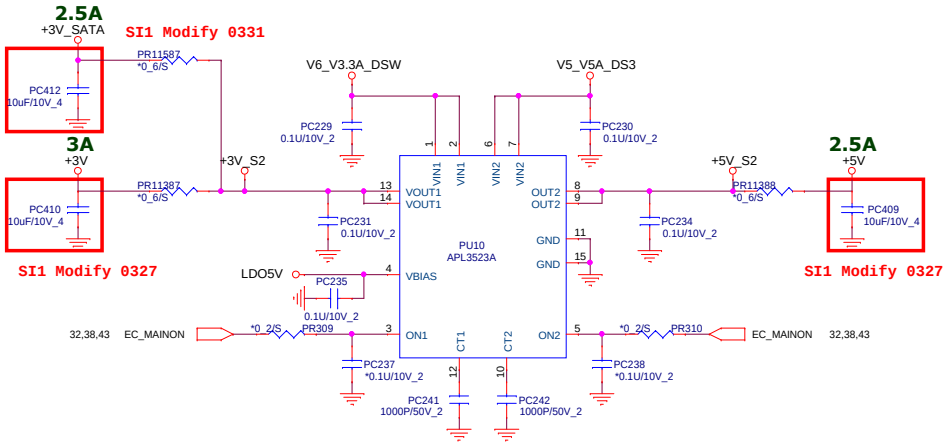
NB5 HW

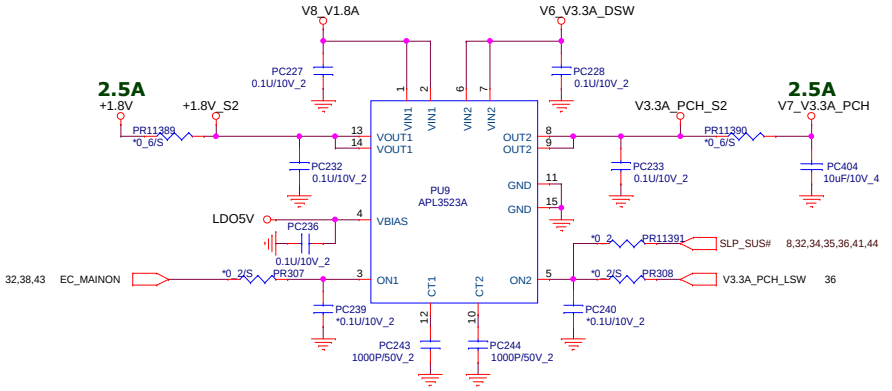
PROJECT : Millhone
Quanta Computer Inc.

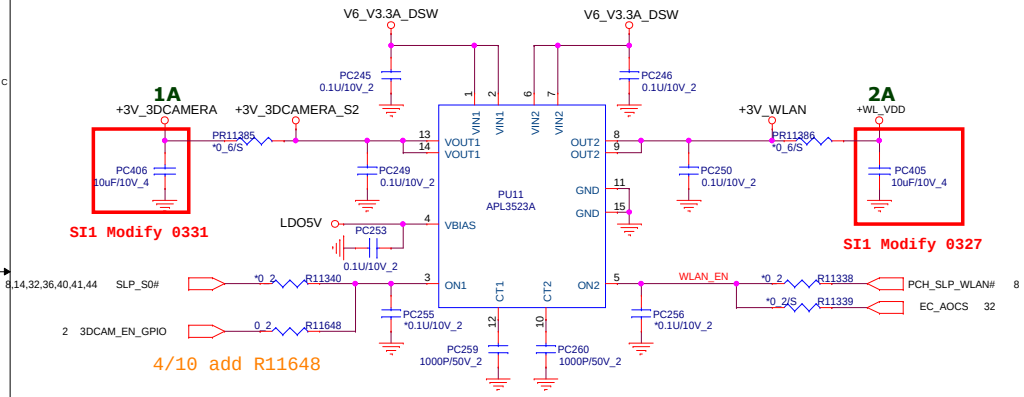
Size	Document Number	Rev
	+VCC_PRIM (NB681)	A
Date: Friday, August 28, 2015	Sheet 41 of 48	



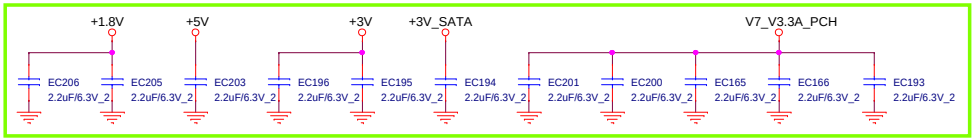
NB5 HW	PROJECT : Millhone Quanta Computer Inc.	
Size	Document Number POGO/BL (AP2553)	Rev A
Date: Friday, August 28, 2015	Sheet 42 of 48	

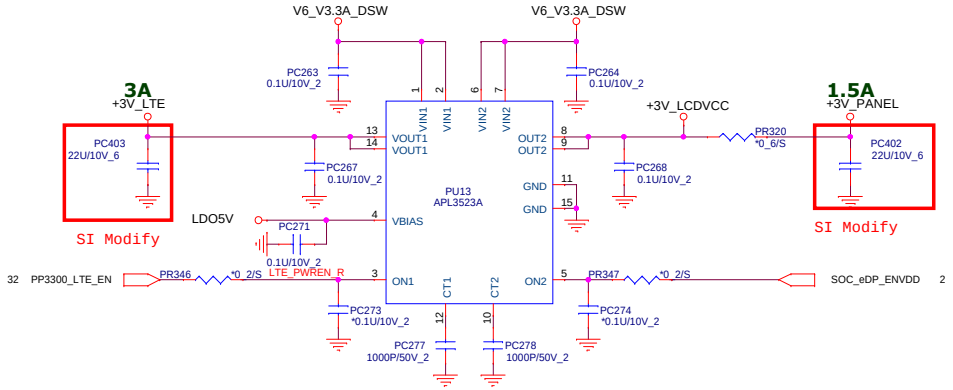






PV RF Modify 0622





+3V_3DCAMERA 16,37
+3V_3DCAMERA_S2
+3V_SATA 17
+3V_S2 43
+WL_VDD 18
+3V_WLAN
+3V_PANEL 14
+3V_LCDVCC
V7_V3.3A_PCH 2,4,5,6,8,10,14,18,19,23,24,27,28,36,37,44
V3.3A_PCH_S2
+3V 2,4,5,6,7,8,11,14,15,19,20,22,31,32,36,37,38,43
+3V_S2 43
+5V 20,43,45
+5V_S2
+1.8V 15,20,36
+1.8V_S2

2,4,5,6,7,8,11,14,15,19,20,22,31,32,36,37,38,43 +3V
20,43,45 +5V
14,33,34,35,36,38,39,40,41,48 +VIN
+3VS5
+5VS5
+3VLANVCC

NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	Load switch IC (APL3523A)	A
Date: Friday, August 28, 2015	Sheet 43 of 48	

PV Modify 0618

8,32,34,35,36,41,43 SLP_SUS# PR11630 *0_2
8,14,32,36,40,41,43,44 SLP_S0# PR11631 0_2
8,32,36,40 SLP_S3# PR11632 0_2
8,32,35,36,44 SLP_S4# PR11633 *0_2

LDO3V
PU24 MC74VHC1G08DFT2G

<= 65usec full load ready
TDC:0.16A

V11_V1.00A
R11545 47K/F_2
PC418 *0.1U/10V_2
PQ49 DMG1012T-7
PC317 0.1U/10V_2
PC316 0.1U/10V_2
+VCCSTG

SI-2 Modify 0420

<= 65usec full load ready
TDC:0.35A

V10_V1.2U
R11651 47K/F_2
PC419 *0.1U/10V_2
PQ1058 DMG1012T-7
PC416 0.1U/10V_2
PC417 0.1U/10V_2
VCCPLL_OC

SI-2 Modify 0420

V5_V5A_DS3
+VCCSTG
VCCPLL_OC

R11546 *1M/F_2
PR11422 *22_6
PR11593 *22_6
PQ48B *NTZD5110N
PQ48A *NTZD5110N
R11547 *2M_2
PQ1060 *DMN62D0UT-7

PV Modify 0521

PR11610 0_6
2.3A

V11_V1.00A
V8_V1.8A
PC281 0.1U/10V_2
PC282 0.1U/10V_2

1A

V1_MPHY
V1_MPHY_S2
PC424 22U/6.3V_6
PC284 *0.1U/10V_2
PC289 0.1U/10V_2
PC285 0.1U/10V_2
PC401 22U/6.3V_6
SI Modify

V1.8U_V2.5U_S2
V9_V1.8A_2.5U
PR332 0_6

PU16 APL3523A
VIN1 VIN1 VIN2 VIN2
VOUT1 VOUT1 OUT2 OUT2
GND GND
VBIAS
ON1 CT1 CT2 ON2

PV Modify 0618
LDO5V

8 MPHY_EXT_PWR
PR334 *0_2
PC290 *0.1U/10V_2
PC292 1000P/50V_2
PC293 1000P/50V_2
PC291 *0.1U/10V_2
PR335 *0_2
PR352 *0_2/S
SLP_S4# 8,32,35,36
V1.8U_2.5U_LSW 36

V7_V3.3A_PCH
MPHY_EXT_PWR PR11421 10K/F_2

PV RF Modify 0622

V9_V1.8A_2.5U
EC204 2.2uF/6.3V_2

PV Modify 0521

PR11611 *0_2/S

PV Modify 0618

8,14,32,36,40,41,43,44 SLP_S0# PR11634 *0_2
8,32,35,36,44 SLP_S4# PR11635 0_2

LDO3V
PU33 *MC74VHC1G08DFT2G

<= 65usec full load ready
TDC:0.1A

V11_V1.00A
R11650 47K/F_2
PC415 0.1U/10V_2
PQ1057 DMG1012T-7
+VCCST_CPU
+VCCSFR
PR11594 *0_4/S
PC414 0.1U/10V_2

V5_V5A_DS3
+VCCST_CPU
R11652 *1M/F_2
PR11592 *22_6
PQ1059B *NTZD5110N
PQ1059A *NTZD5110N
R11653 *2M_2

V9_V1.8A_2.5U 12,13,36
V1.8U_V2.5U_S2
V1_MPHY 10
V1_MPHY_S2

2,4,5,6,7,8,11,14,15,19,20,22,31,32,36,37,38,43 +3V
20,43,45 +5V
14,33,34,35,36,38,39,40,41,48 +VIN
+3VS5
+5VS5
+3VLANVCC

NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	Load switch IC (APL3523A)	A
Date: Friday, August 28, 2015	Sheet 44 of 48	

SCREW HOLE

H1 *H-C299D220P2
H3 *H-C300D158P2
H4 H-C197D126P2
H5 H-C197D126P2
H6 *H-TC299BC118D79P2
H7 *H-TC197BC79D79P2
H8 *H-TC197BC79D79P2
H10 *H-MILLHONE-2
H11 *H-MILLHONE-3
H12 *H-MILLHONE-4

P-Sensor Spring

4/14 modify H2
footprint to spad-re236x166np

H2 spad-re236x166np
H9 *H-MILLHONE-1
CS2 45

7/16 add gnd pad for RF

H13 spad-re236x166np
H14 spad-re236x166np
H15 spad-re236x166np
H16 spad-re236x166np
H17 spad-re236x166np
H18 spad-re236x166np

BOT SHIELDING PAD

PAD1 *PAD-MILLHONE-1-3P
PAD2 *PAD-MILLHONE-2-7P
PAD3 *PAD-MILLHONE-3-8P
PAD4 *PAD-MILLHONE-4-4P
PAD5 *PAD-MILLHONE-5-5P
PAD31 *PAD-MILLHONE-1-3P

CLIP WLAN SHIELDING

PAD6 emipad39x39-89x24-3p
PAD7 emipad39x39-89x24-3p
PAD8 emipad39x39-89x24-3p
PAD9 emipad39x39-89x24-3p
PAD10 emipad39x39-89x24-3p
PAD11 emipad39x39-89x24-3p

0720 PVR modify
0720 PVR modify
0720 PVR modify

CLIP THERMAL SHIELDING

PAD12 EMIPAD47X31-63X24-3P
PAD13 EMIPAD47X31-63X24-3P
PAD14 EMIPAD47X31-63X24-3P
PAD15 EMIPAD47X31-63X24-3P
PAD16 EMIPAD47X31-63X24-3P
PAD17 EMIPAD47X31-63X24-3P
PAD18 EMIPAD47X31-63X24-3P
PAD19 EMIPAD47X31-63X24-3P
PAD20 EMIPAD47X31-63X24-3P
PAD21 EMIPAD47X31-63X24-3P
PAD22 EMIPAD47X31-63X24-3P
PAD23 EMIPAD47X31-63X24-3P
PAD24 EMIPAD47X31-63X24-3P
PAD25 EMIPAD47X31-63X24-3P
PAD26 EMIPAD47X31-63X24-3P
PAD27 EMIPAD47X31-63X24-3P
PAD28 EMIPAD47X31-63X24-3P
PAD29 EMIPAD47X31-63X24-3P
PAD30 EMIPAD
PAD32 EMIPAD
PAD33 EMIPAD
PAD34 EMIPAD
PAD35 EMIPAD
PAD36 *EMIPAD
PAD37 EMIPAD
PAD38 EMIPAD

80 PORT

U9060 *74HCT164PW
C9774 *0.1U/10V_2
32,45 80PORT_DAT
32,45 80PORT_CLK
8,17,18,19,22,32,37,45 PLTRST#
LED4
LED5
LED6
LED7
LED8
LED9
LED10
LED11

CN54 6P DMIC CONN
80PORT_DAT 32,45
80PORT_CLK 32,45
PLTRST# 8,17,18,19,22,32,37,45

MV Modify_0817

VDD_V3P3A_RTC
+3V_RTC
R11563 *100K_2
R11525 *100K_2
R11527 *10K_2
*MMBT3904T-7-F/SOT523 Q7134
31 LID_EC#
R11526 *10K_2
U9061 *74LVC1G74GT
D1004 *RB521S30
D1005 RB521S30
VSTBY_FSPI

+3V_RTC 7,8,10,19,31,33
MMBT3906T-7-F/SOT523 Q12
R11566 4.7K_2
R11567 4.7K_2
D1015 RB521S30
NBSWON# 19
NBSWON#_D 32,36
R11529 4.7K_2
R11528 4.7K_2
MBCLK 32,33
MBDATA 32,33

Input				Output	
SD	RD	CP	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Input				Output	
SD	RD	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

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PROJECT :	Millhone
Quanta Computer Inc.	
NB5 HW	
Size	Document Number: SCREW/DEBUG
Rev	A
Date:	Sunday, August 30, 2015
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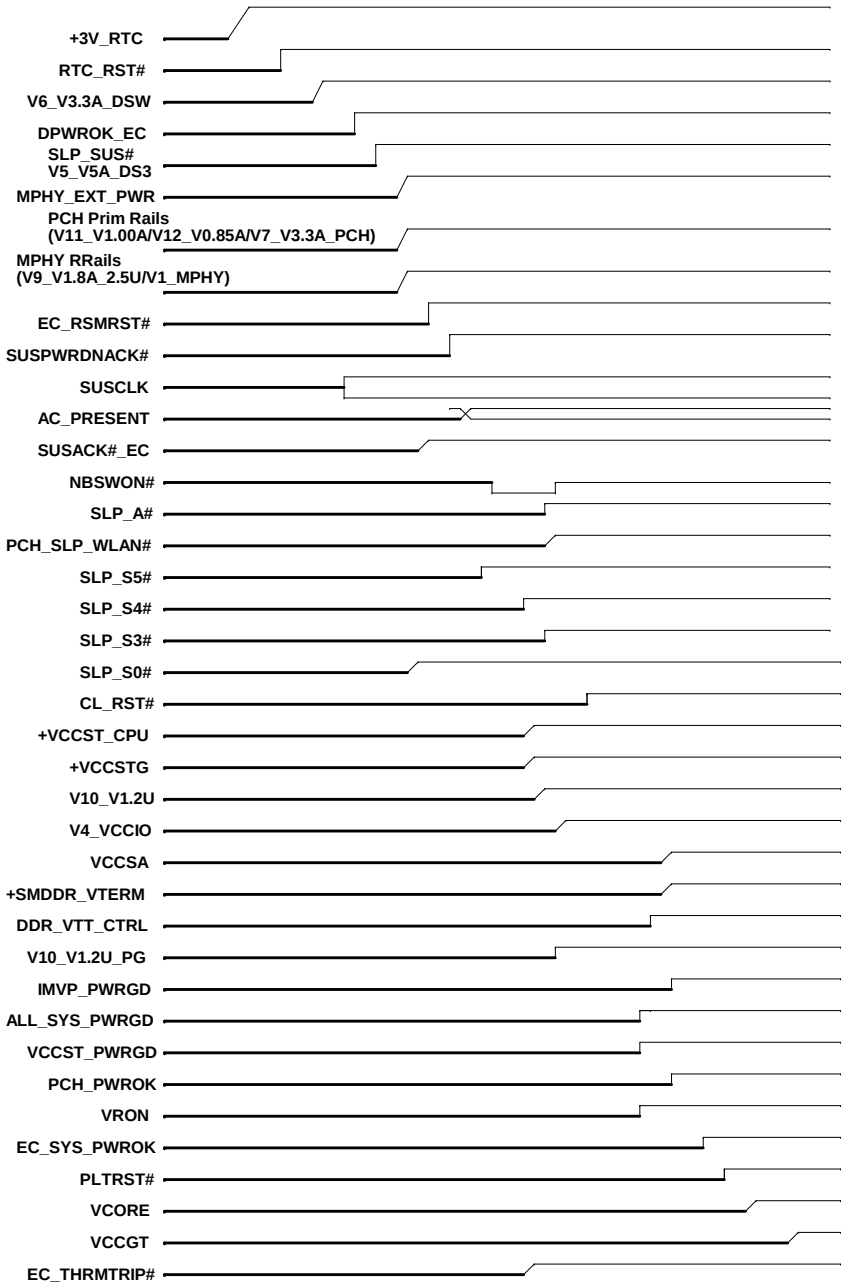
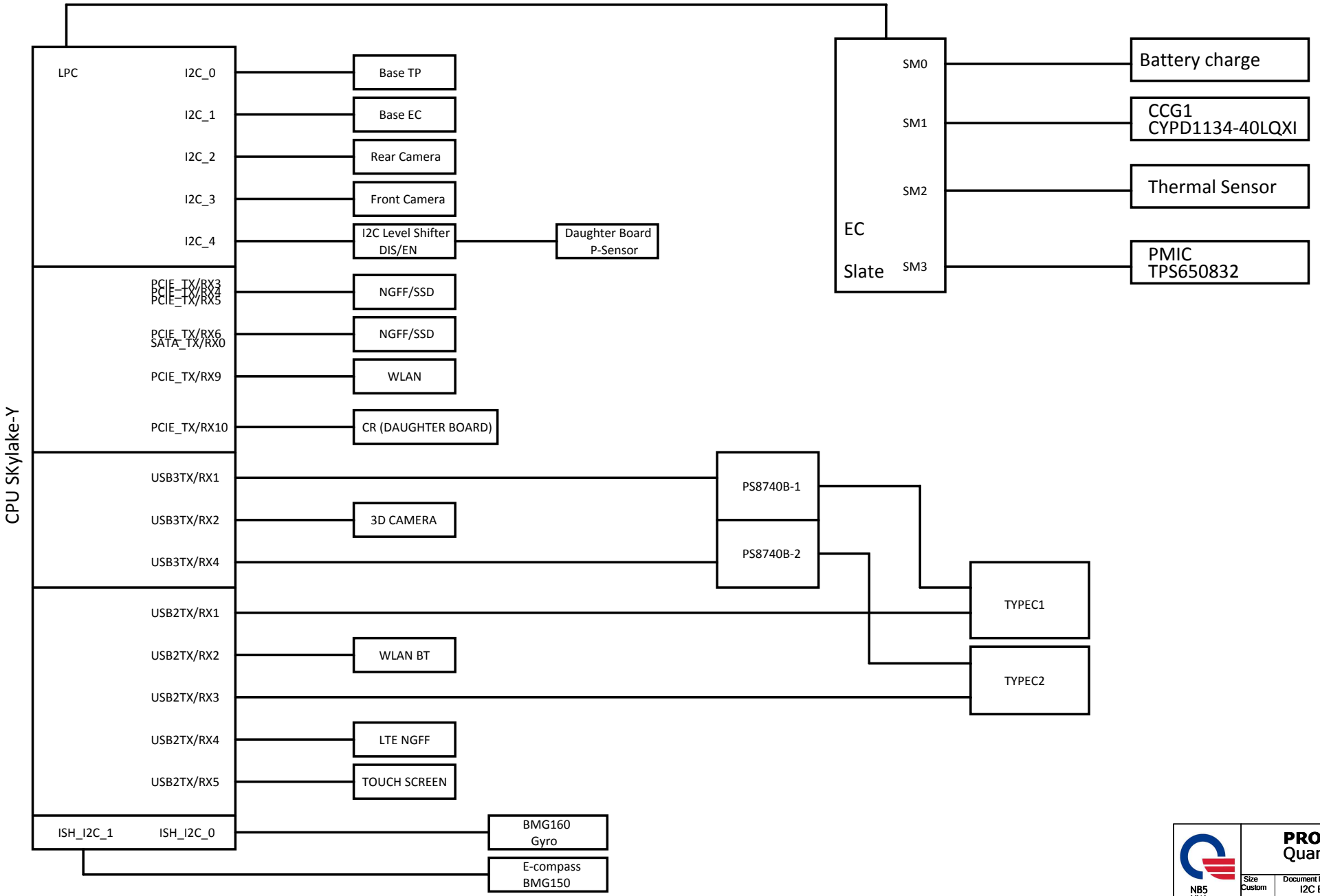
Millhone Power up sequence



PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
Custom	I2C Block diagram	1A
NB5		
Date: Friday, August 28, 2015	Sheet 46 of 48	

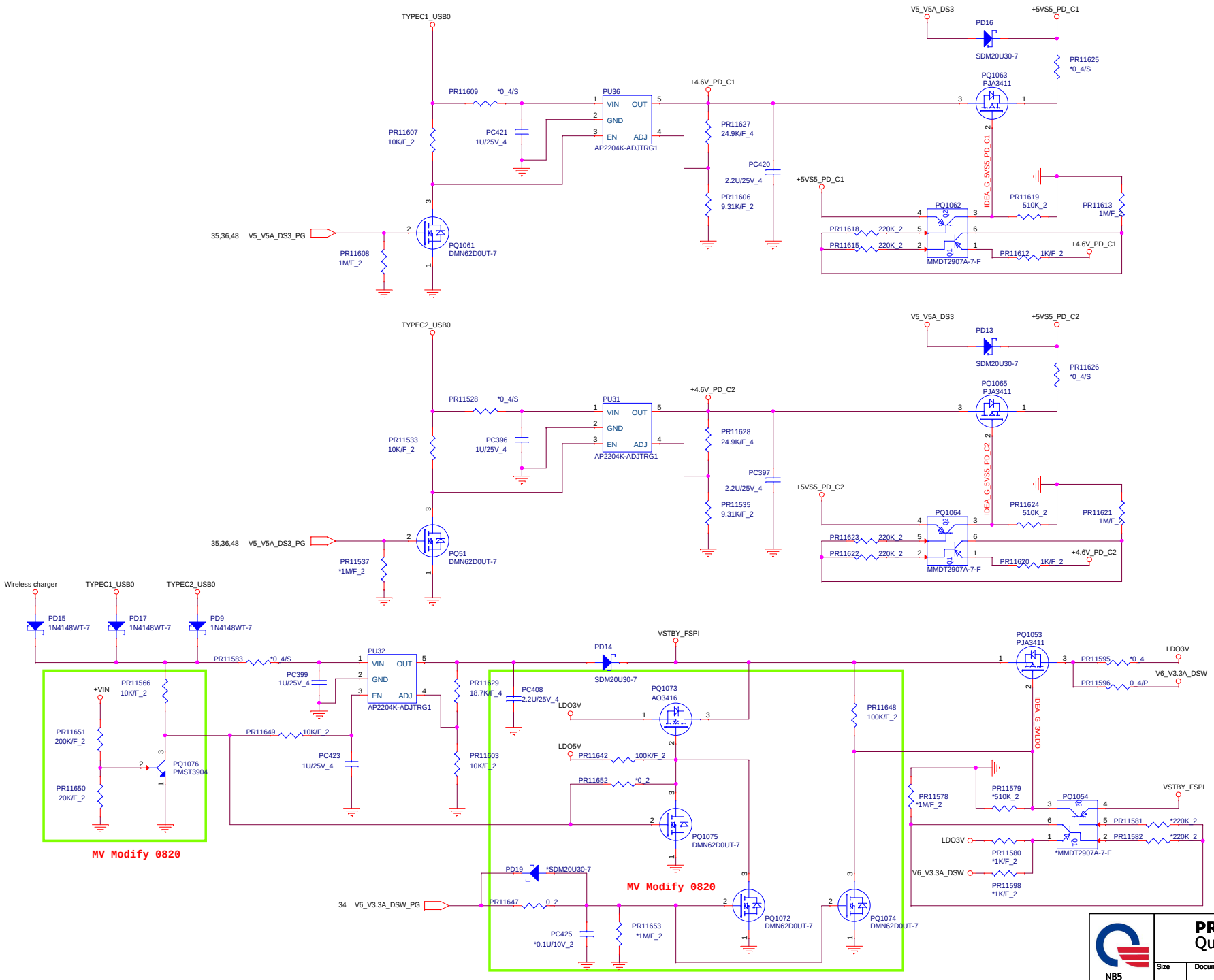


NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
Custom	I2C Block diagram	1A

Date: Friday, August 28, 2015 Sheet 47 of 48



NB5 HW

PROJECT : Millhone
Quanta Computer Inc.

Size	Document Number	Rev
	Dead Battery	A
Date: Friday, August 28, 2015	Sheet 48 of 48	