GA-78LMT-S2P

Revision : 3.11

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Title: COVER SHEET		
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Model Name:GA-78LMT-S2P

Component value change history

Version: 3.11

P-Code: U99098-0

Date	Change Item	Reason
2010.12.30	3.1A PVT BOM Release. PCB: 3.11	P BOM Release change from 78LMT-USB3 Rev 3.11 Remove USB 3.0 & EC CAP

Circuit or PCB layout change for next version

Date	Version	Change Item
2010.10.19	0.1 Gerber out	Modify from 78LMT-USB3-S2 3.11 Remove USB 3.0 Solder Mask Remove 1333+ (RS760=RS780L)

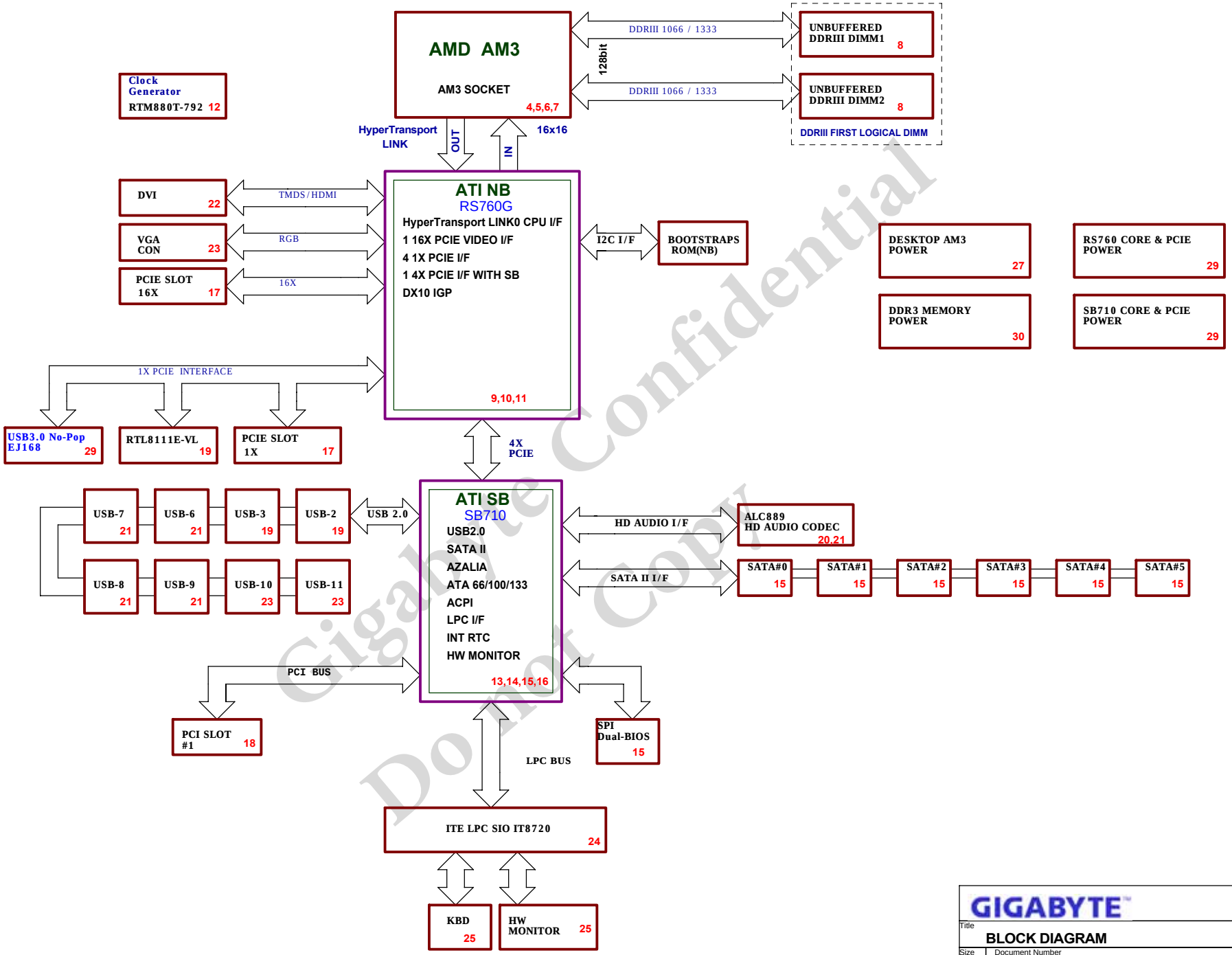
GIGABYTE

Title: BOM & PCB HISTORY

Size: Custom | Document Number: GA-78LMT-USB3 | Rev: 3.11

Date: Thursday, April 21, 2011 | Sheet 2 of 29

RS780L CUSTOMER DESKTOP DESIGN



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Title: BLOCK DIAGRAM

Size	Document Number	Rev
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] [9]
L0_CADIN_H[0..15] L0_CADIN_H[0..15] [9]

L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] [9]
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] [9]

M2CPUA

HYPERTRANSPORT

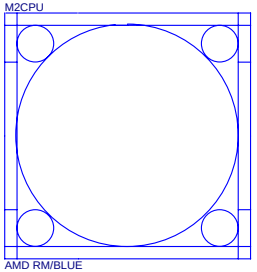
[9] L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 [9]
[9] L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 [9]
[9] L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 [9]
[9] L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 [9]
[9] L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 [9]
[9] L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 [9]
[9] L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 [9]
[9] L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 [9]
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AE5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/15u/[10SC1-A01942-01R_10SC1-A01942-02R]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPU



AMD RM/BLUE

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Title: CPU HYPER TRANSPORT

Size	Document Number	Rev
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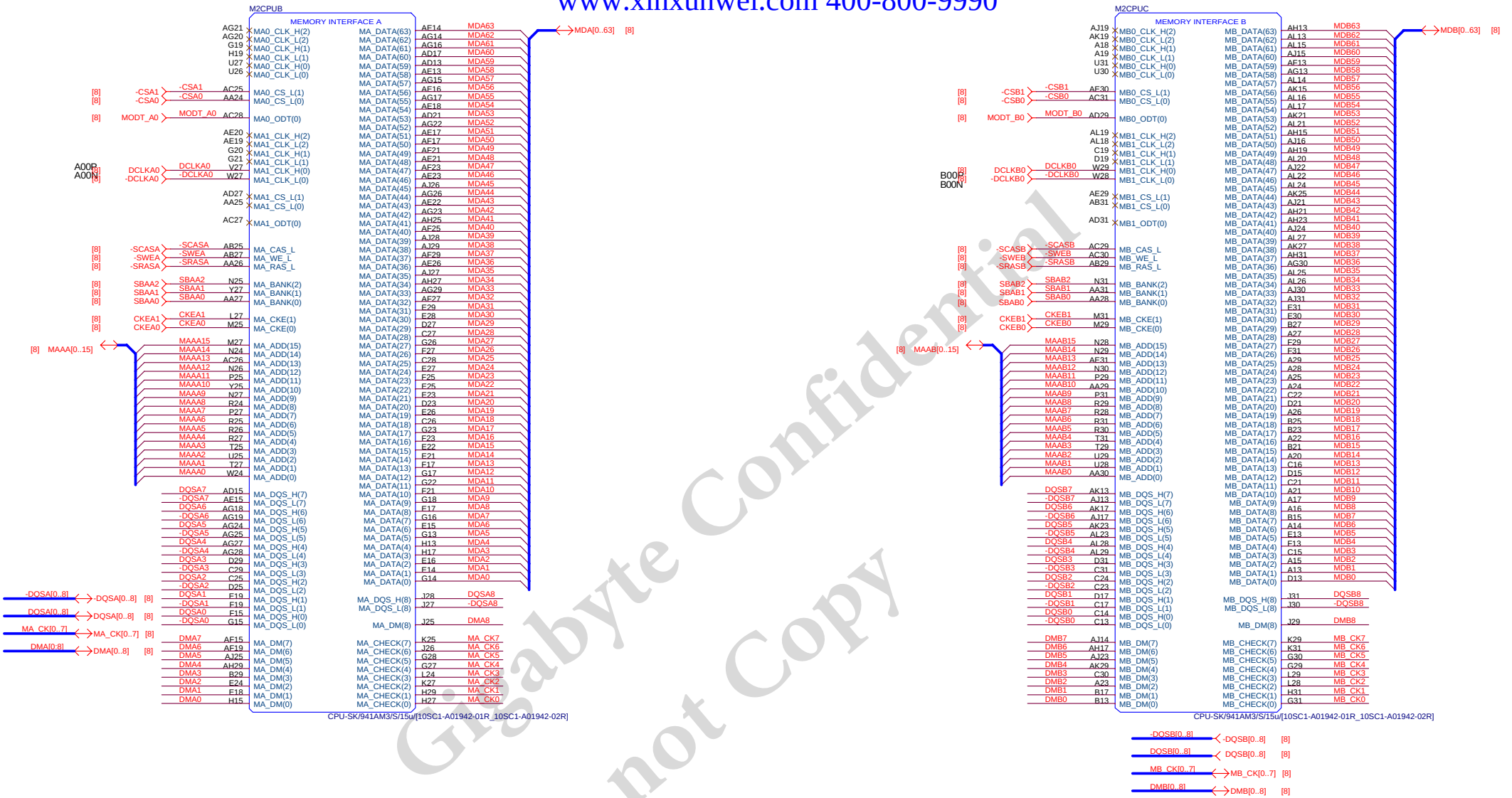

GIGABYTE

Title	CPU DDRII MEMORY		
Size: Custom	Document Number: GA-78LMT-USB3		Rev: 3.11
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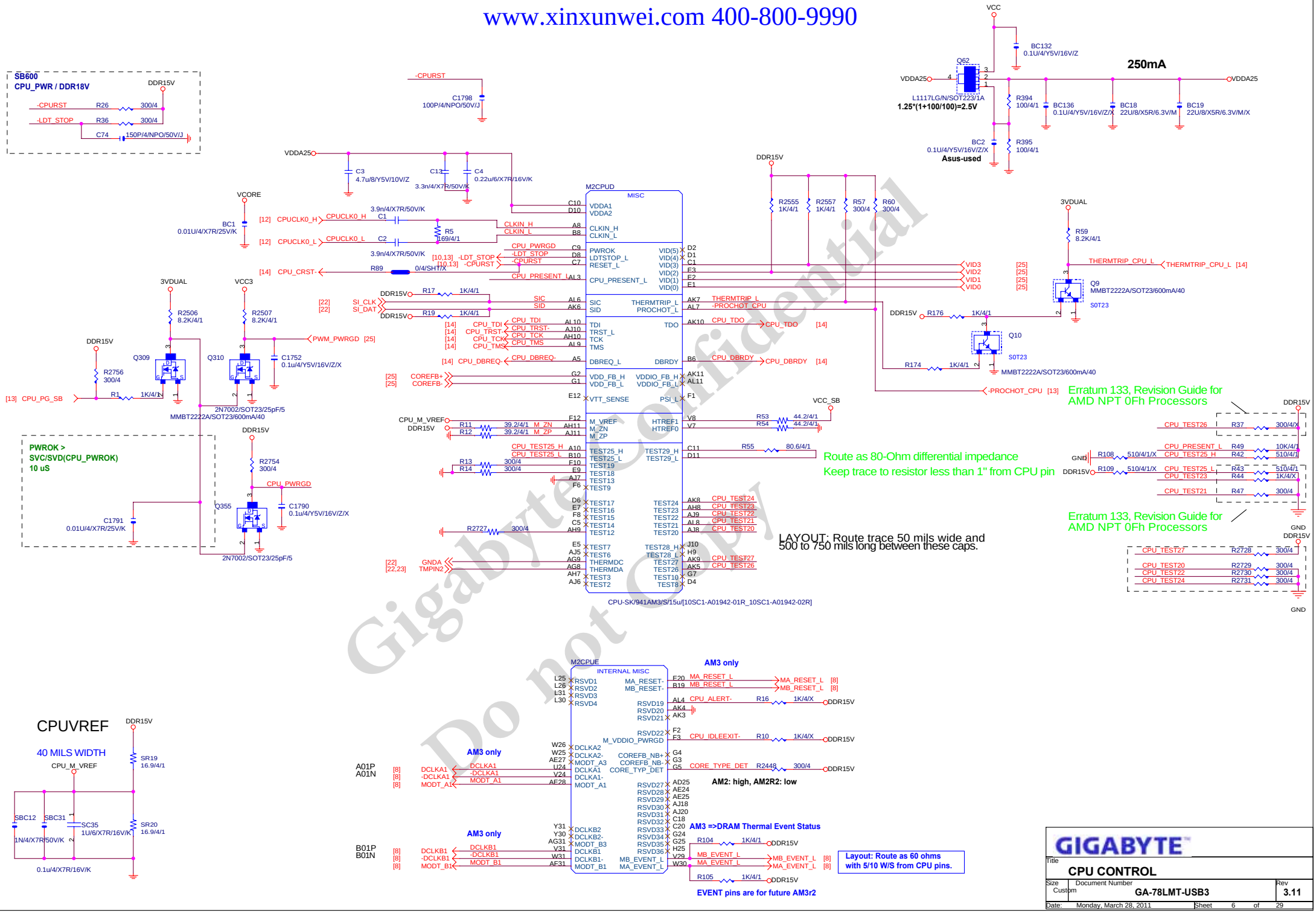

GIGABYTE

Title	CPU CONTROL	
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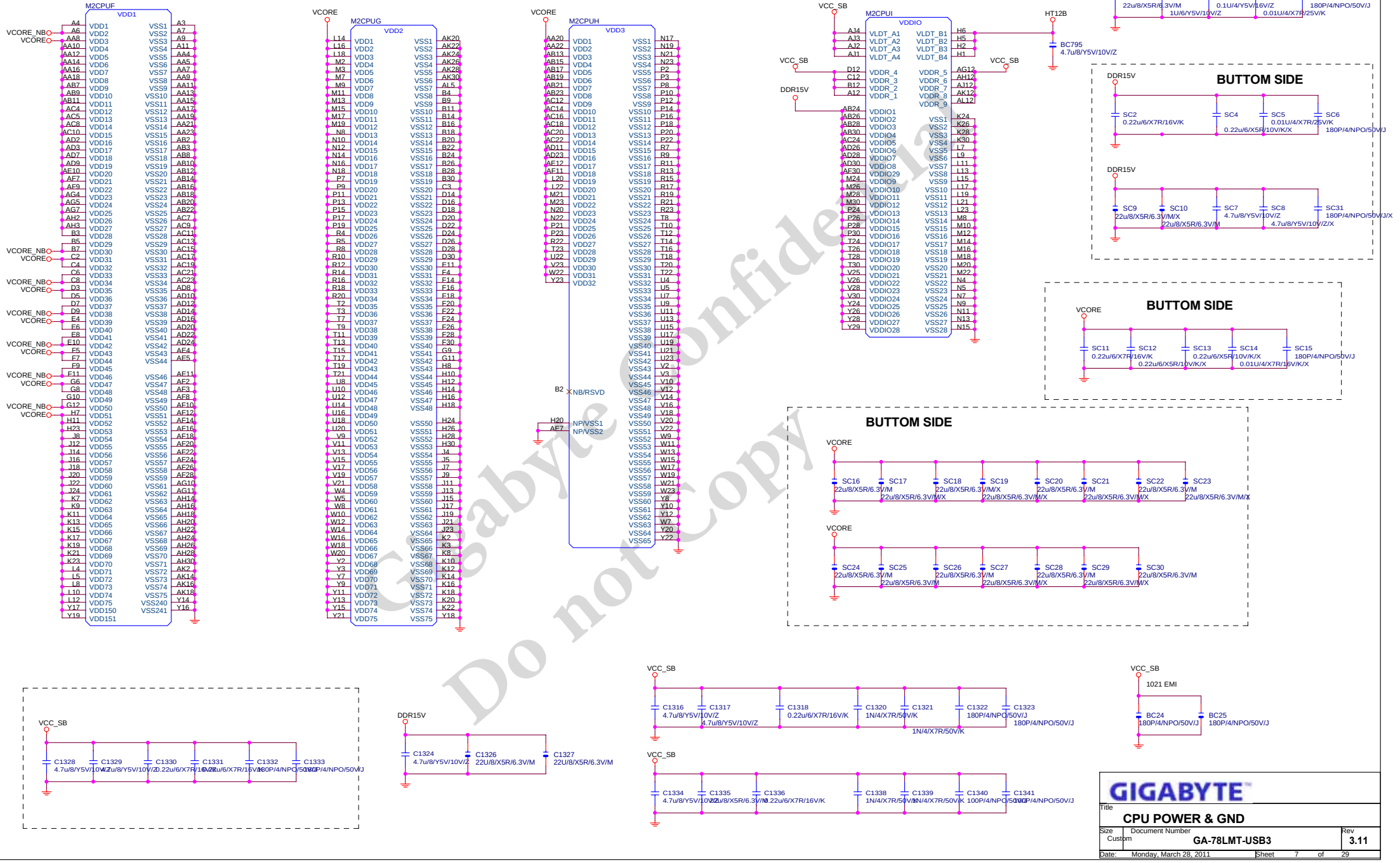
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



Title	CPU POWER & GND		
Size	Document Number		Rev
Custom	GA-78LMT-USB3		3.11
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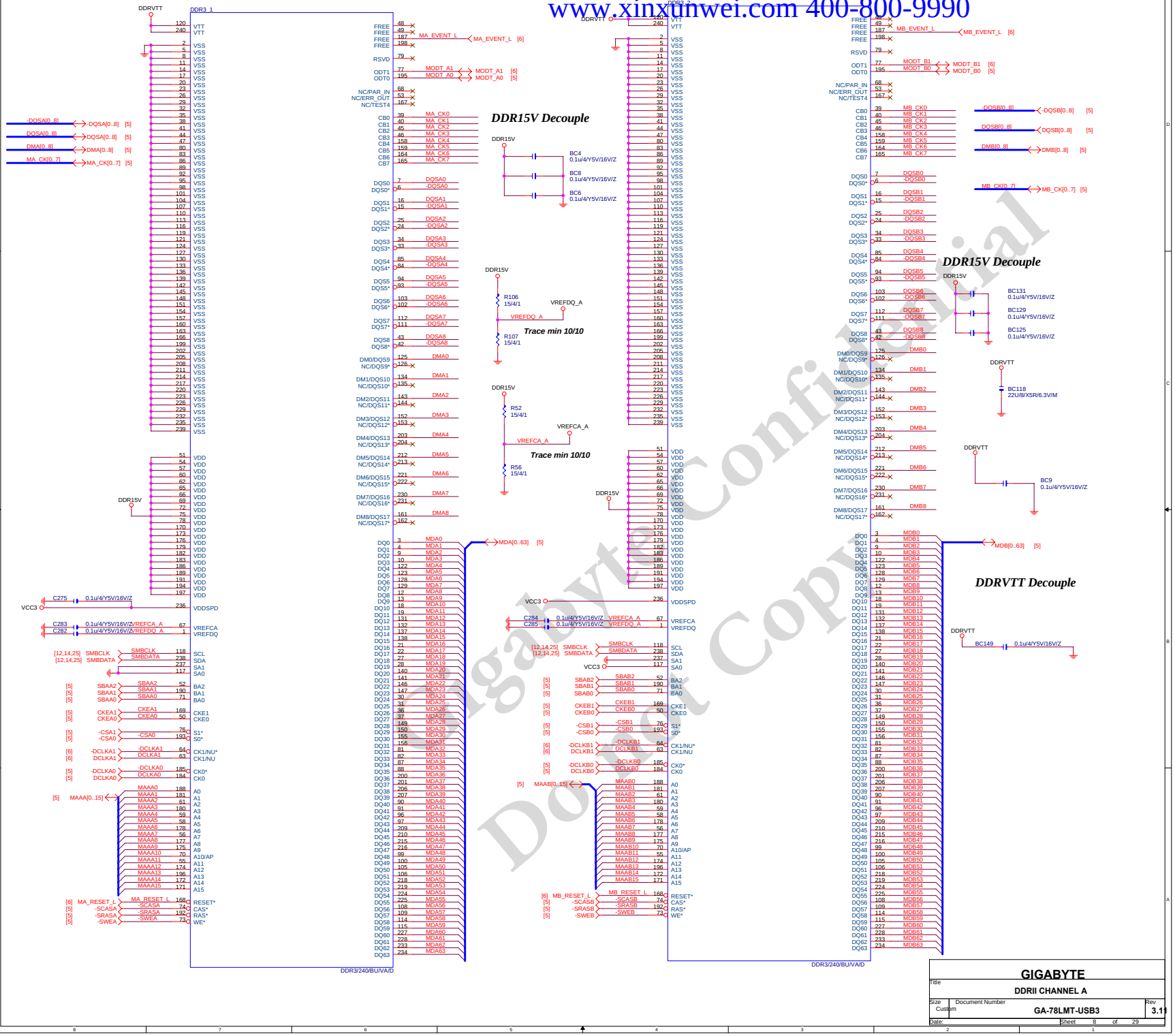
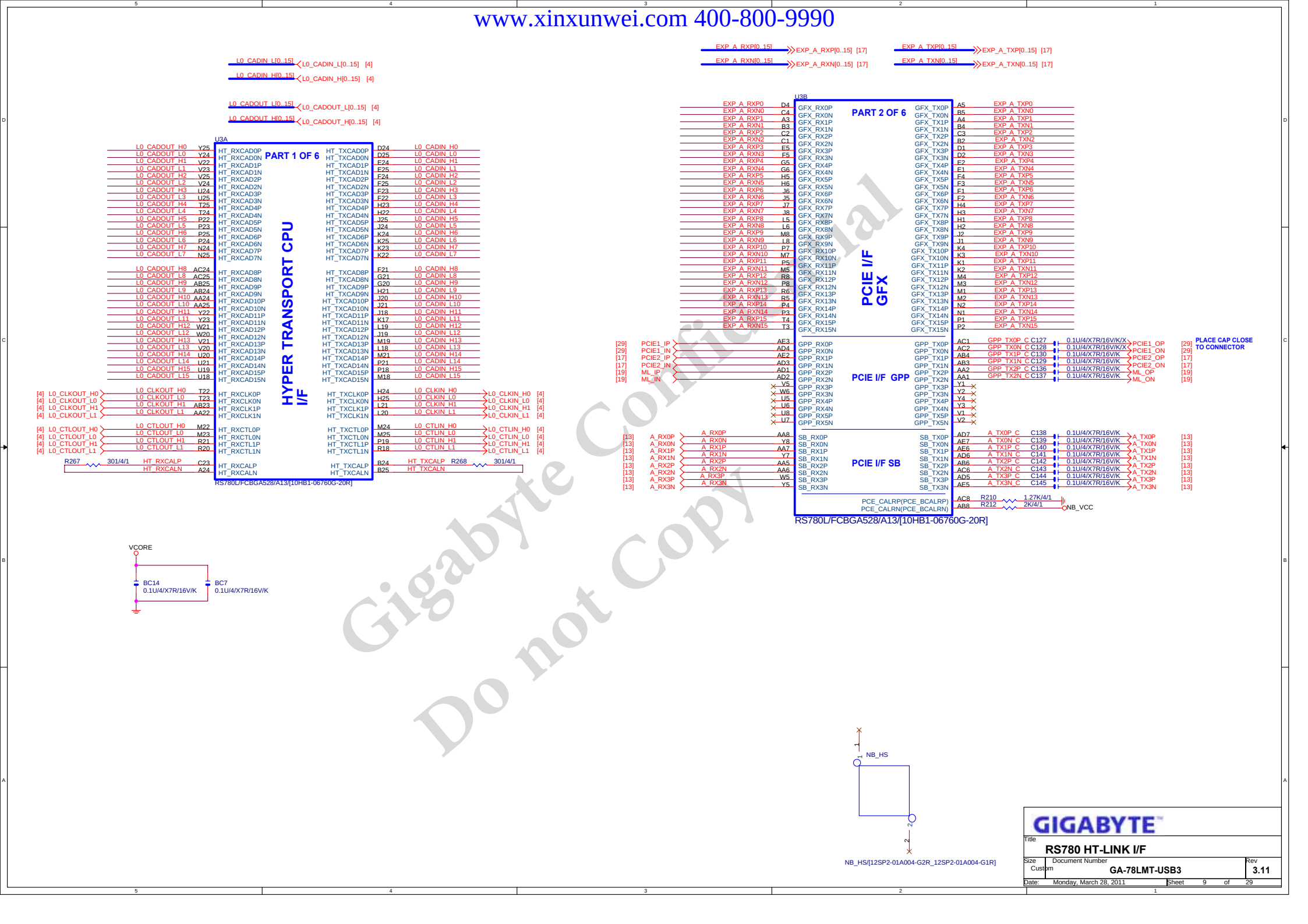


GIGABYTE			
Title: DDRII CHANNEL A			
Size: Custom	Document Number: GA-78LMT-USB3	Rev: 3.11	
Date:	Sheet 8 of 29		



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Title	RS780 HT-LINK I/F	
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RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

RS740_DFT_GPIO1 R272 150/4/1

Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly

[21] DAC_VSYNC R276 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly

R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

[21] DAC_HSYNC R285 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly

R219 (RX780_DFT_GPIO0)

EMI 20080103
SR4 0/6/SHT/X

U3C

PART 3 OF 6

CRT/TVOUT | PLL PWR | LVTM | PM | CLOCKs | MIS.

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

SR1~SR3 PLACED WITHIN 1" OF NB

SR3 150/4/1 SR2 150/4/1 SR1 140/4/1

NB_PWROK
EMI ESD ISSUE
C7 100P/4/NPO/50V/J/X

SBC34 1U/6/Y5V/10V/Z
BC139 SBC29 1U/6/Y5V/10V/Z
1U/6/Y5V/10V/Z

SBC35 10U/8/X5R/6.3V/K BC143 1U/6/Y5V/10V/Z SBC36 1U/6/Y5V/10V/Z SBC15 0.1u/4/Y5V/16V/Z

BC150 BC151 1U/6/Y5V/10V/Z 0.1U/4/Y5V/16V/Z
Q74 P8503BMG/SOT23/450pF/85m
R156 8.2K/4/1 +12V

BC145 0.1U/4/Y5V/16V/Z BC146 1U/6/Y5V/10V/Z

BC141 1U/6/Y5V/10V/Z

BC678 0.1U/4/Y5V/16V/Z

R159 150/4/1 REFCLKN R158 150/4/1

R2128 4.7K/4 R2127 4.7K/4
KR2 KR1 0/4/SHT/X 0/4/SHT/X

R265 8.2K/4/1_STRP_DATA

R312 33/4 R337 0/4
D9 AME385BEETZ/SOT23/2.5V
R331 100K/4/1
R116 39.2K/4/1/X

M1 SHIELD1 DVI
M2 SHIELD2
DVI-D/24P/SC/RA/D
DVI-30P-2 COMMON

U3D

PAR 4 OF 6

SBD_MEM/DVO_I/F

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

BC60 0.1u/4/Y5V/16V/Z BC61 0.1u/4/Y5V/16V/Z

ESD1 ESD2 ESD3 AZ1045-04F/MSOP10

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Title	RS780 SYSTEM I/F	
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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

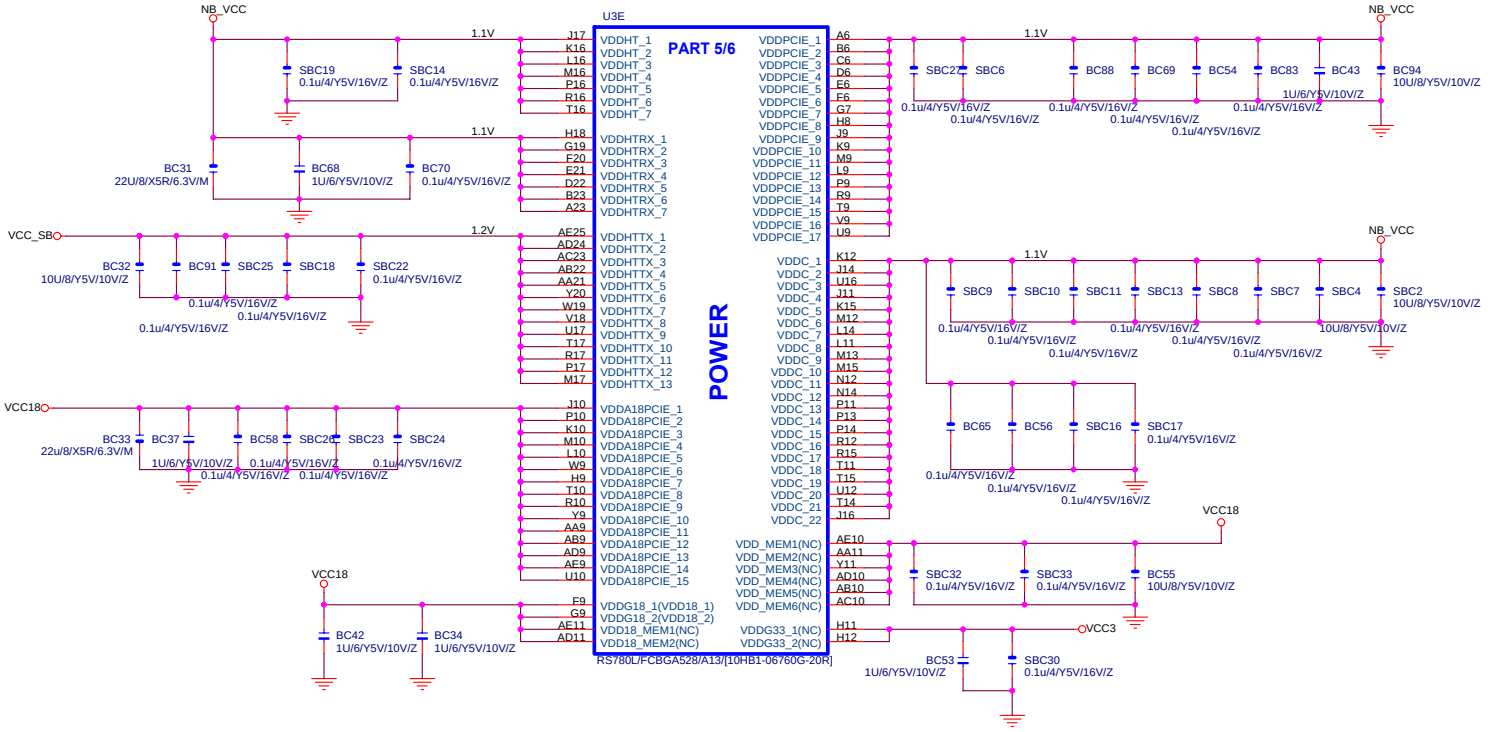
U3F — PART 6/6 — GROUND

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

Please use 1mm pad size, place all ELT test pads on bottom side only

U3E — PART 5/6 — POWER

RS780L/FCBGA528/A13/[10HB1-06760G-20R]



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Title	RS780 POWER & GND	
Size: Custom	Document Number: GA-78LMT-USB3	Rev: 3.11
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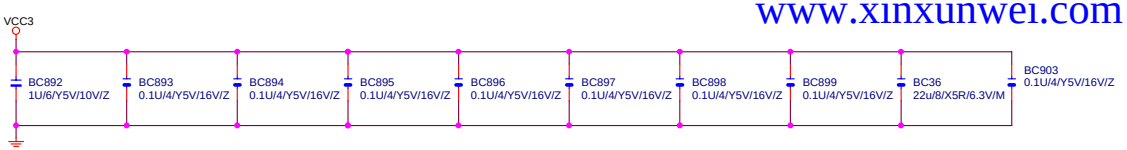
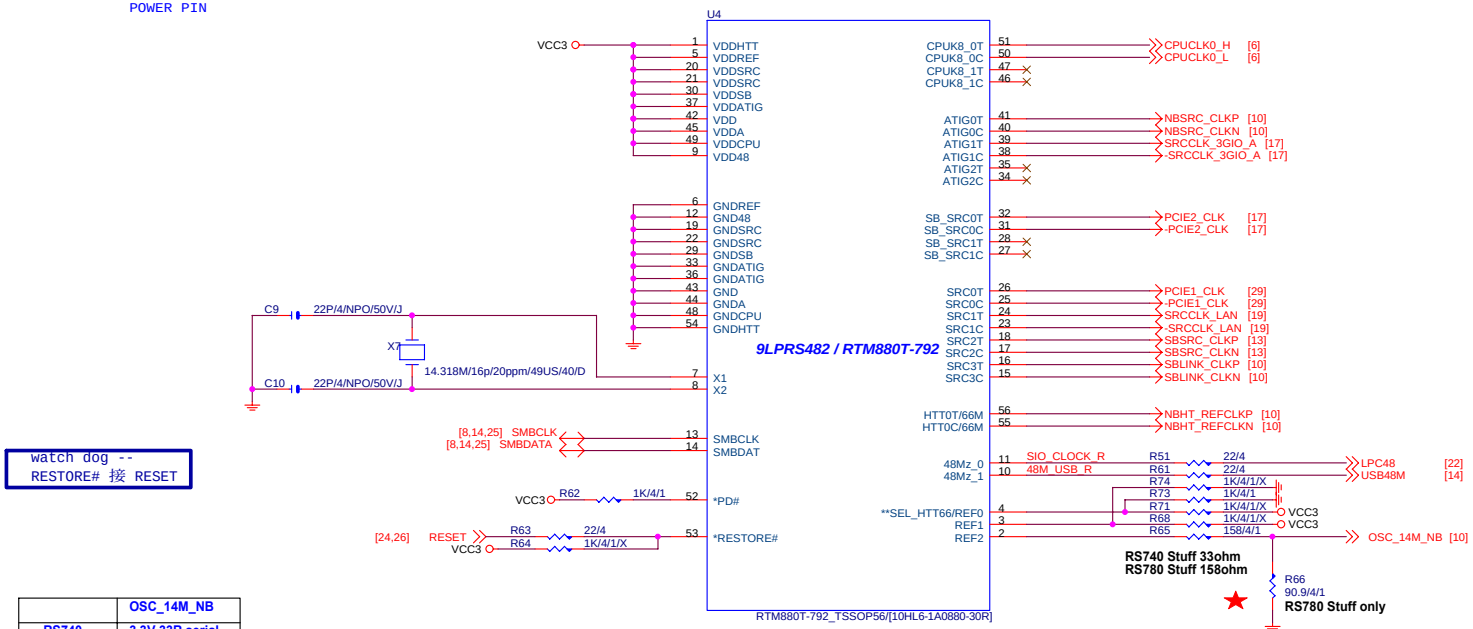


1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



watch dog -- RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

GIGABYTE

Title: ICS9LPRS477

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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK

SB_HS

SB_HS/[12SP2-030005-42R_12SP2-030005-43R]

U2A

SB700

Part 1 of 5

SB710/FCBGA528/A14/[10HB1-06B710-11R]

PCI CLKS

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

RTC XTAL

LPC

CPU

RTC

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

BIOS after boot setting
EC AOD-ACC

20mil 20mil

BAT54C/SOT23/200mA

20mil

BATTERY CR2032

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

GIGABYTE

Title: ATI SB710 PCIE/PCI/CPU/LPC

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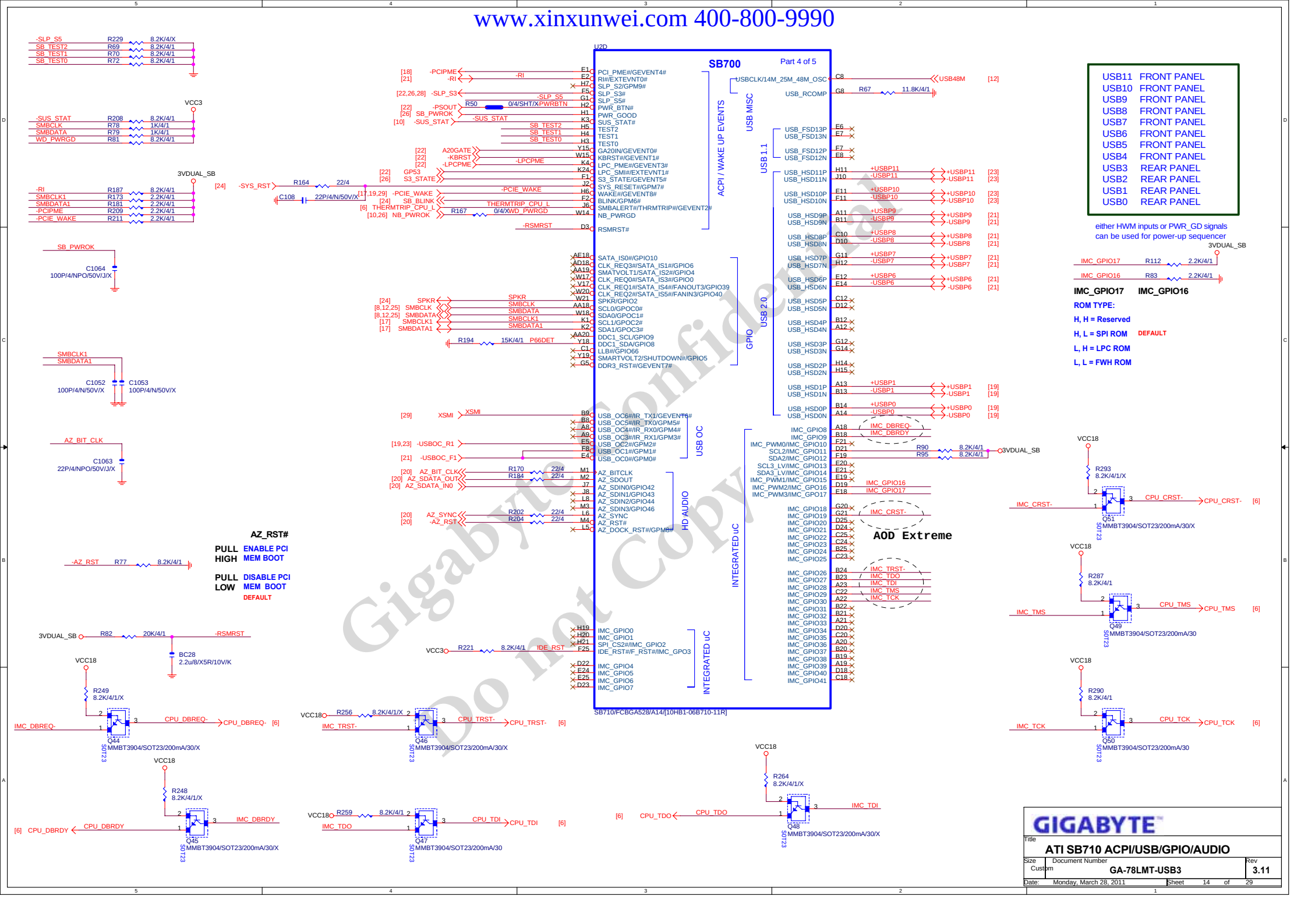

GIGABYTE

Title: ATI SB710 ACPI/USB/GPIO/AUDIO

Size	Document Number	Rev
Custom	GA-78LMT-USB3	3.11

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PLACE SATA AC COUPLING CAPS CLOSE TO SB600

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

U2B

SB700
Part 2 of 5

SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR

SB710/FCBGA528/A14/[10HB1-06B710-11R]

Title			
ATI SB710 SATA/IDE/HWM/SPI			
Size: Custom	Document Number: GA-78LMT-USB3	Rev: 3.11	
Date: Monday, March 28, 2011	Sheet 15 of 29		

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

U2C

SB700

Part 3 of 5

POWER

1.8V: Flash module mode
3.3V: IDE mode

SB710/FCBGA528/A14/[10HB1-06B710-11R]

U2E

SB700

GROUND

Part 5 of 5

SB710/FCBGA528/A14/[10HB1-06B710-11R]

GIGABYTE

Title: ATI SB700 POWER & GND

Size: Custom | Document Number: GA-78LMT-USB3 | Rev: 3.11

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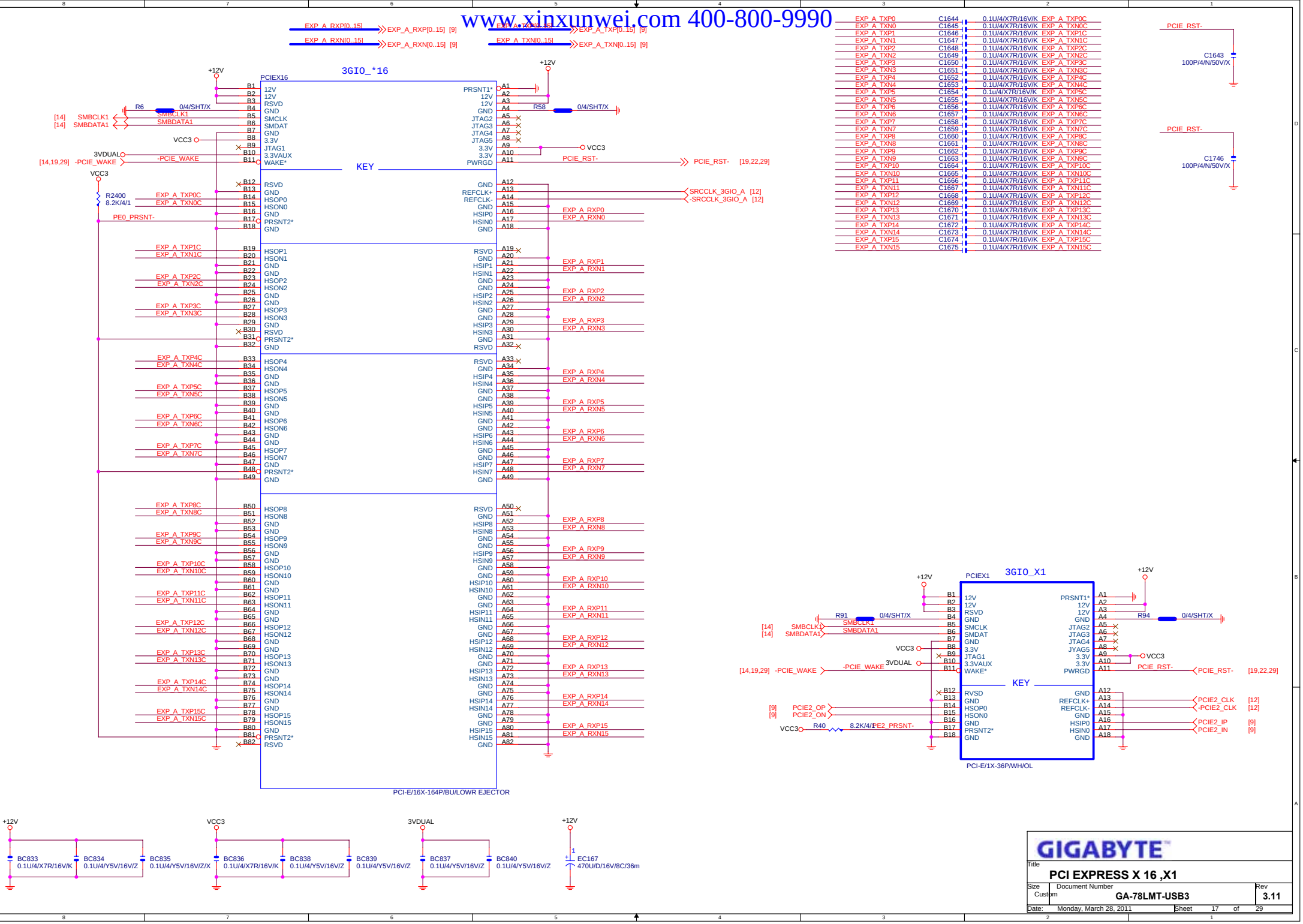

EXP_A_TXP0	C1644	0.1U/4/X7R/16V/K EXP_A_TXP0C
EXP_A_TXN0	C1645	0.1U/4/X7R/16V/K EXP_A_TXN0C
EXP_A_TXP1	C1646	0.1U/4/X7R/16V/K EXP_A_TXP1C
EXP_A_TXN1	C1647	0.1U/4/X7R/16V/K EXP_A_TXN1C
EXP_A_TXP2	C1648	0.1U/4/X7R/16V/K EXP_A_TXP2C
EXP_A_TXN2	C1649	0.1U/4/X7R/16V/K EXP_A_TXN2C
EXP_A_TXP3	C1650	0.1U/4/X7R/16V/K EXP_A_TXP3C
EXP_A_TXN3	C1651	0.1U/4/X7R/16V/K EXP_A_TXN3C
EXP_A_TXP4	C1652	0.1U/4/X7R/16V/K EXP_A_TXP4C
EXP_A_TXN4	C1653	0.1U/4/X7R/16V/K EXP_A_TXN4C
EXP_A_TXP5	C1654	0.1u/4/X7R/16V/K EXP_A_TXP5C
EXP_A_TXN5	C1655	0.1U/4/X7R/16V/K EXP_A_TXN5C
EXP_A_TXP6	C1656	0.1U/4/X7R/16V/K EXP_A_TXP6C
EXP_A_TXN6	C1657	0.1U/4/X7R/16V/K EXP_A_TXN6C
EXP_A_TXP7	C1658	0.1U/4/X7R/16V/K EXP_A_TXP7C
EXP_A_TXN7	C1659	0.1U/4/X7R/16V/K EXP_A_TXN7C
EXP_A_TXP8	C1660	0.1U/4/X7R/16V/K EXP_A_TXP8C
EXP_A_TXN8	C1661	0.1U/4/X7R/16V/K EXP_A_TXN8C
EXP_A_TXP9	C1662	0.1U/4/X7R/16V/K EXP_A_TXP9C
EXP_A_TXN9	C1663	0.1U/4/X7R/16V/K EXP_A_TXN9C
EXP_A_TXP10	C1664	0.1U/4/X7R/16V/K EXP_A_TXP10C
EXP_A_TXN10	C1665	0.1U/4/X7R/16V/K EXP_A_TXN10C
EXP_A_TXP11	C1666	0.1U/4/X7R/16V/K EXP_A_TXP11C
EXP_A_TXN11	C1667	0.1U/4/X7R/16V/K EXP_A_TXN11C
EXP_A_TXP12	C1668	0.1U/4/X7R/16V/K EXP_A_TXP12C
EXP_A_TXN12	C1669	0.1U/4/X7R/16V/K EXP_A_TXN12C
EXP_A_TXP13	C1670	0.1U/4/X7R/16V/K EXP_A_TXP13C
EXP_A_TXN13	C1671	0.1U/4/X7R/16V/K EXP_A_TXN13C
EXP_A_TXP14	C1672	0.1U/4/X7R/16V/K EXP_A_TXP14C
EXP_A_TXN14	C1673	0.1U/4/X7R/16V/K EXP_A_TXN14C
EXP_A_TXP15	C1674	0.1U/4/X7R/16V/K EXP_A_TXP15C
EXP_A_TXN15	C1675	0.1U/4/X7R/16V/K EXP_A_TXN15C

PCIE_RST- C1643 100P/4/N/50V/X

PCIE_RST- C1746 100P/4/N/50V/X

+12V	BC833	0.1U/4/X7R/16V/K
	BC834	0.1U/4/Y5V/16V/Z
	BC835	0.1U/4/Y5V/16V/Z/X
VCC3	BC836	0.1U/4/X7R/16V/K
	BC838	0.1U/4/Y5V/16V/Z
	BC839	0.1U/4/Y5V/16V/Z
3VDUAL	BC837	0.1U/4/Y5V/16V/Z
	BC840	0.1U/4/Y5V/16V/Z
+12V	EC167	470U/D/16V/8C/36m

GIGABYTE

Title: PCI EXPRESS X 16 ,X1

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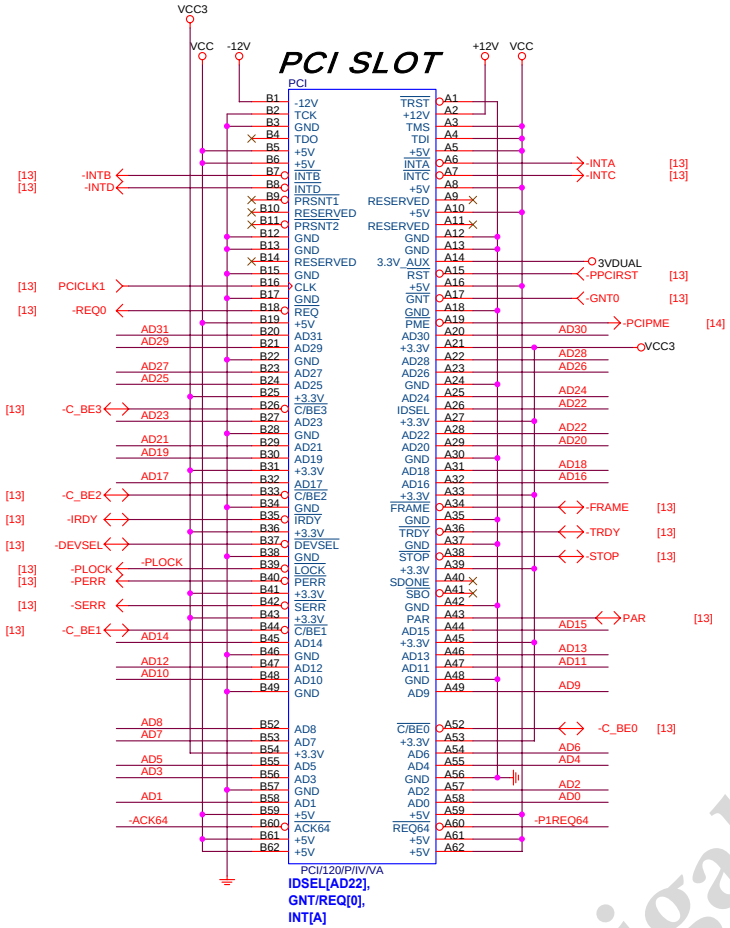
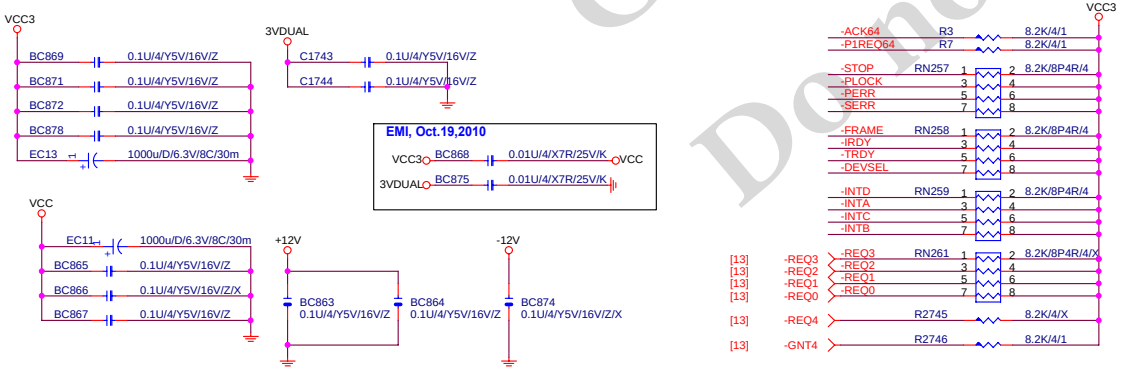
PCI SLOT 1,2





GIGABYTE			
Title: PCI SLOT 1,2			
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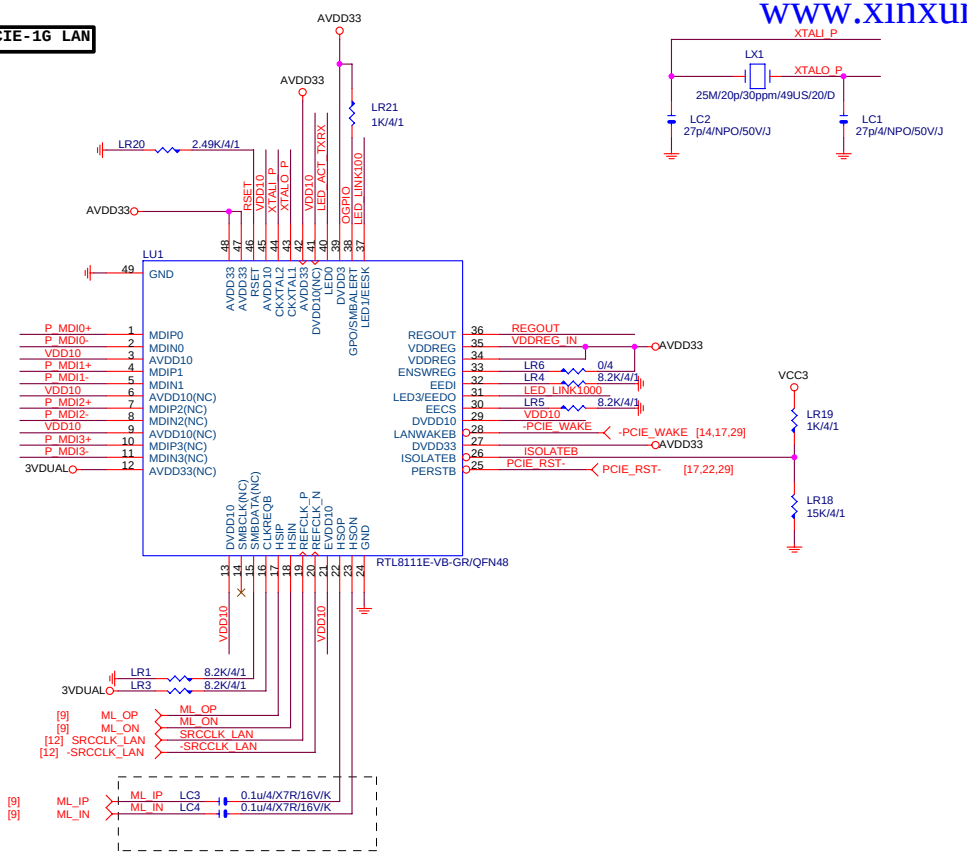
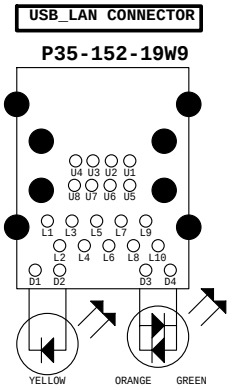
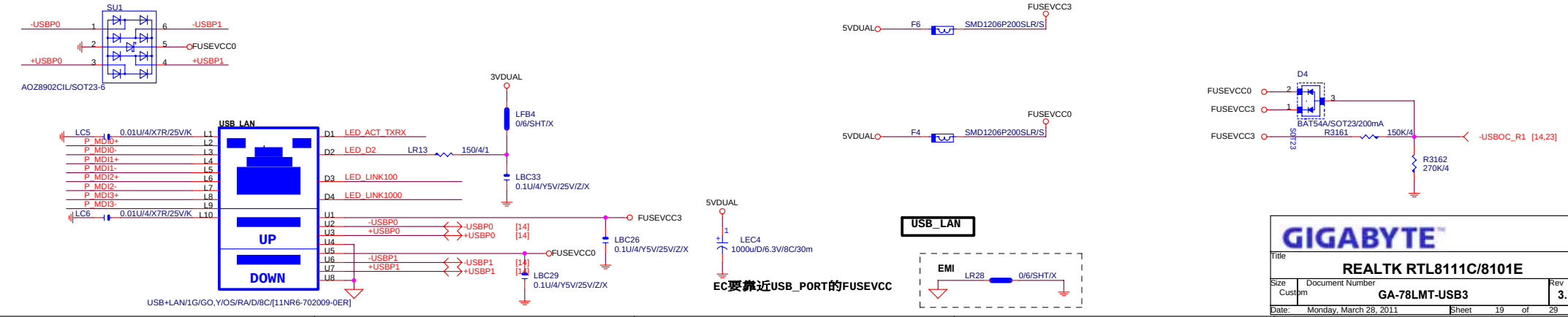
PCIE-1G LAN





USB_LAN CONNECTOR



Title	REALTK RTL8111C/8101E
Size	Custom
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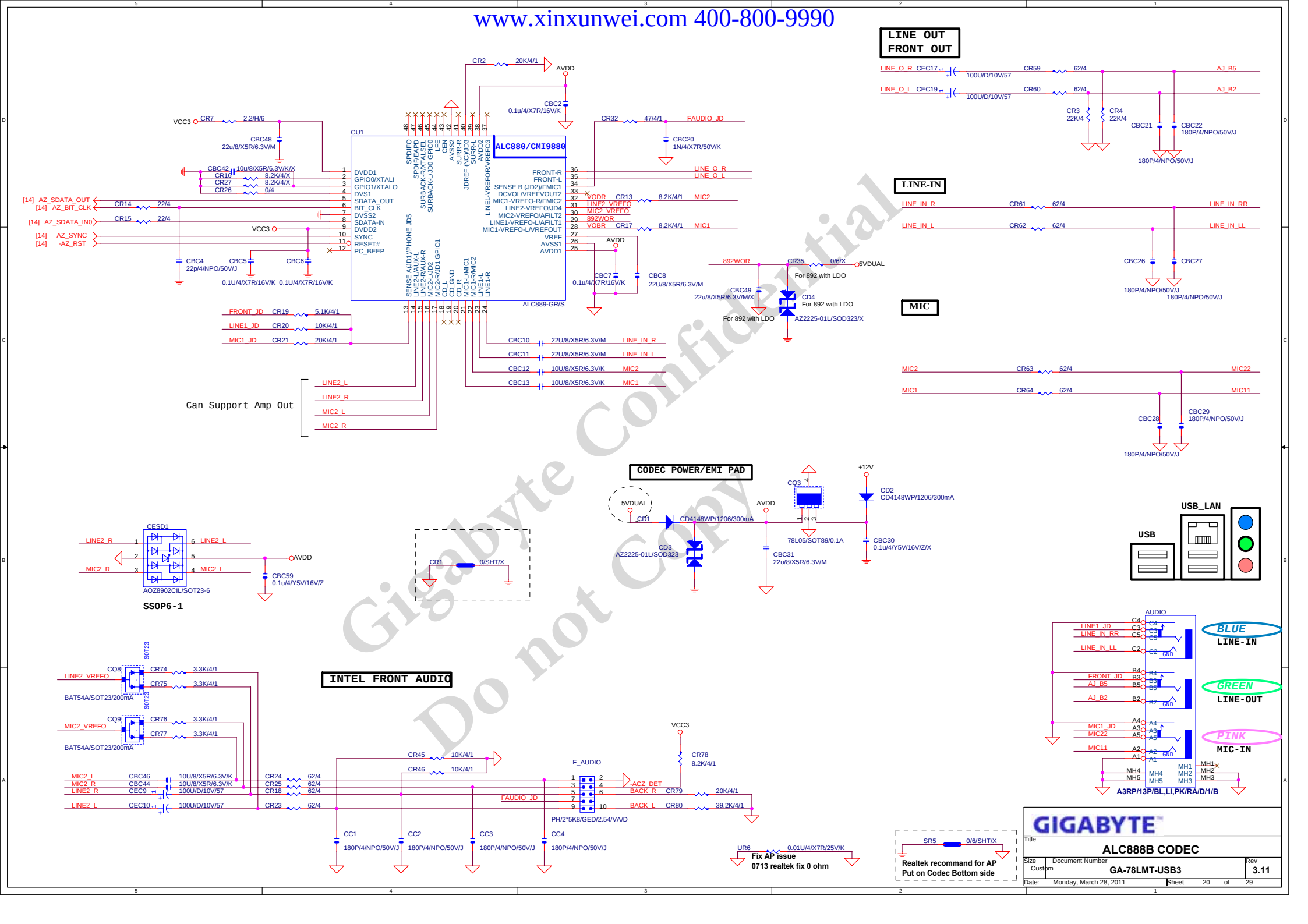

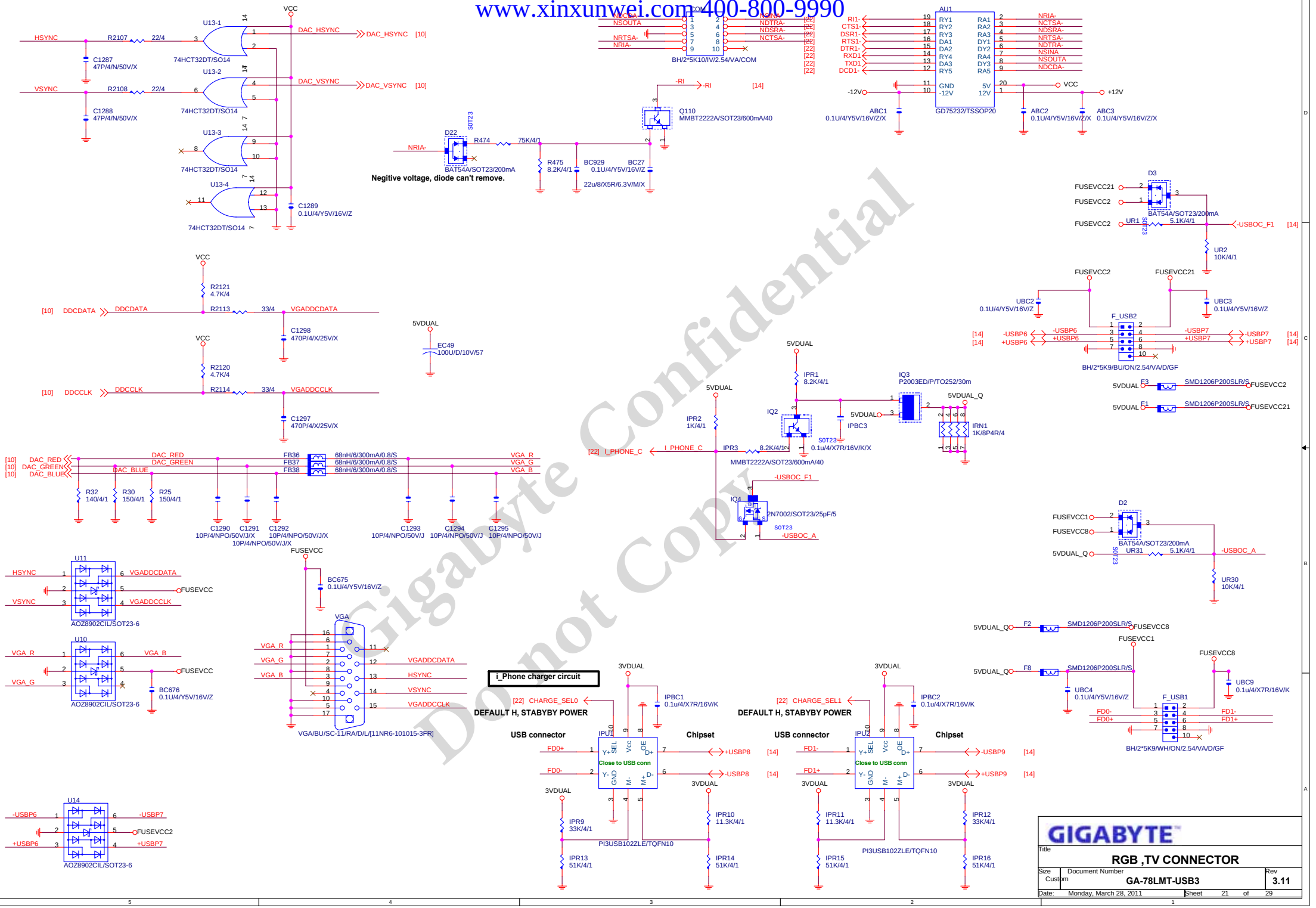

GIGABYTE

Title: RGB ,TV CONNECTOR

Size	Document Number	Rev
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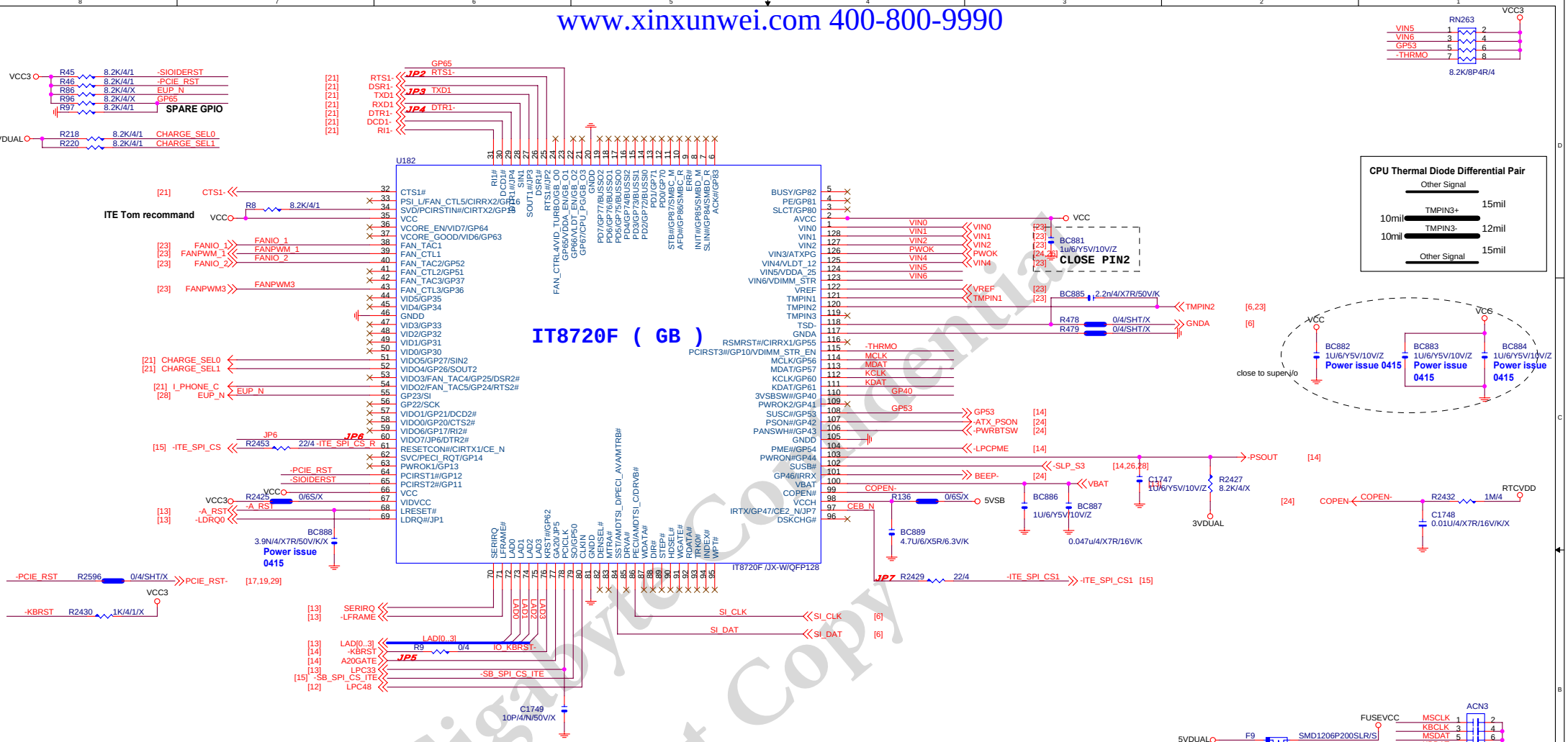

IT8720GB Power On Strapping Options

	Symbol	value	Description
JP1 Pin 69			
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

KB/MS/6P/PC99/OS/RA/D/2/[11NR6-802006-19R_11NR6-802006-1ER]

Title	ITE 8720 LPC IO		
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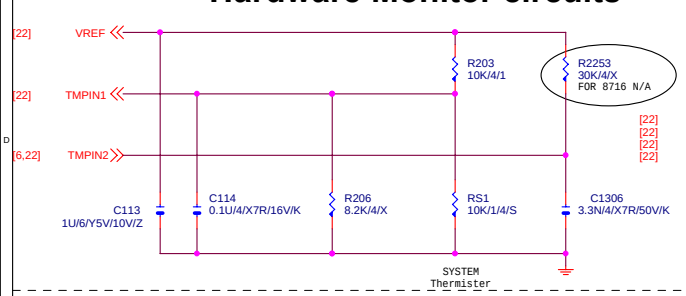
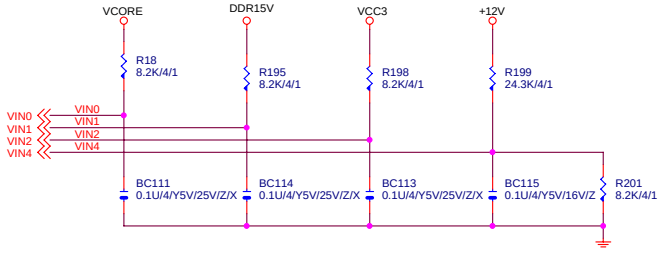
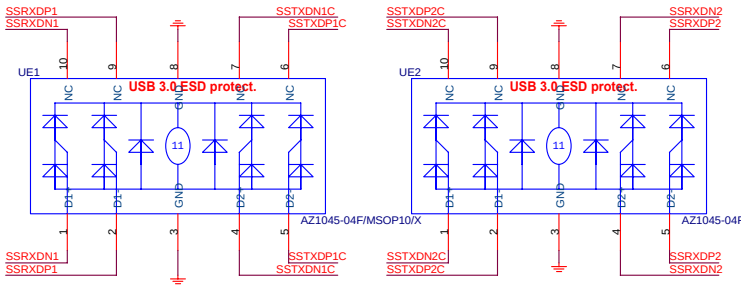
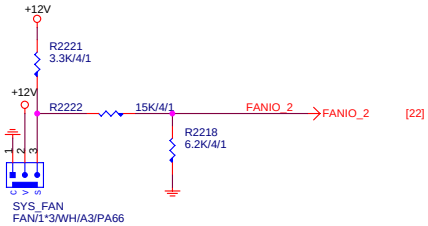
Hardware Monitor circuits

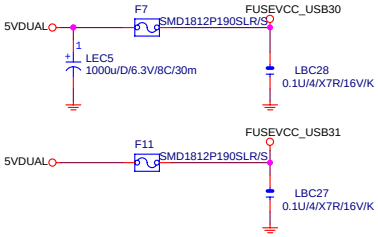


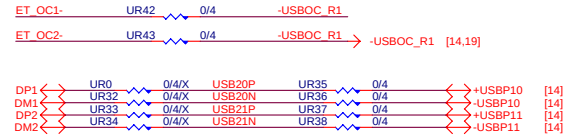




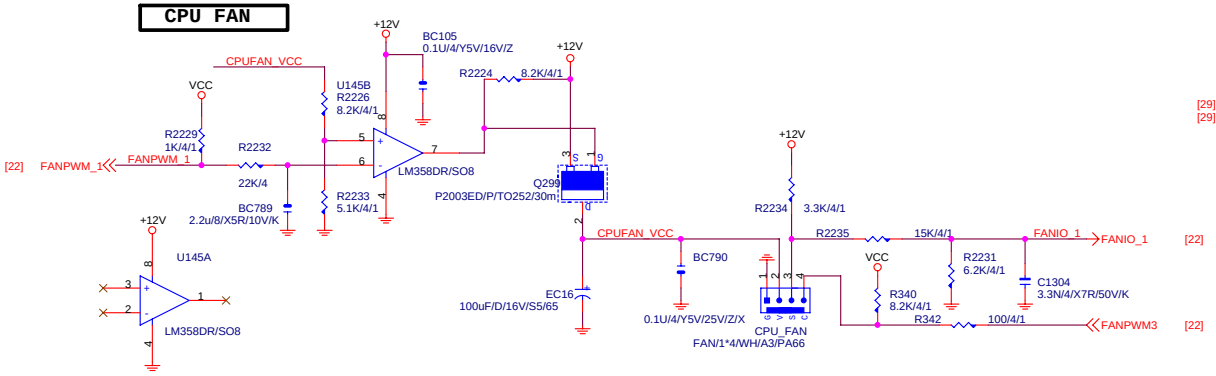
SYSTEM FAN

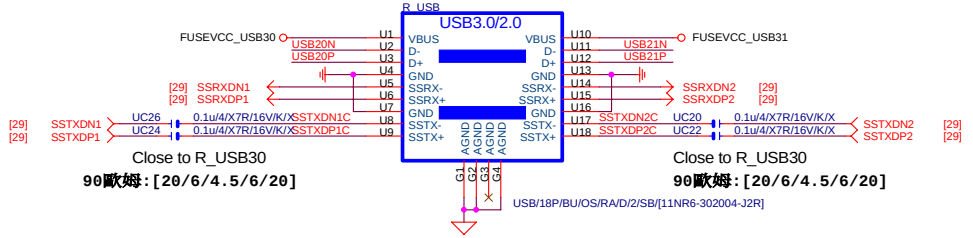


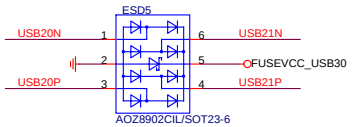




CPU FAN







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Title	FAN/HWMO ,KB/USB	
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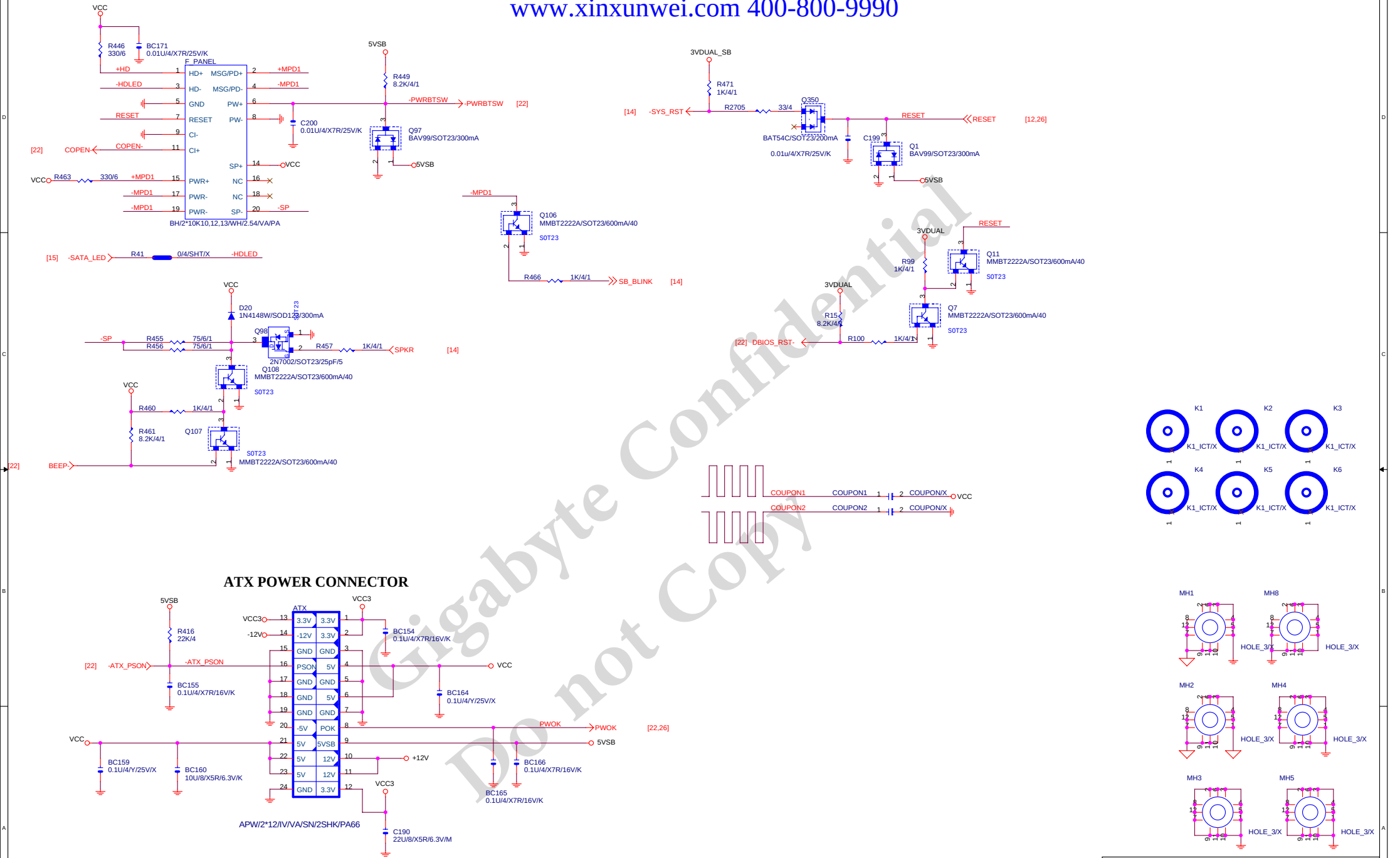

ATX POWER CONNECTOR

MH1 MH8 MH2 MH4 MH3 MH5
HOLE_3/X

GIGABYTE

Title	ATX, FRONT PANEL	
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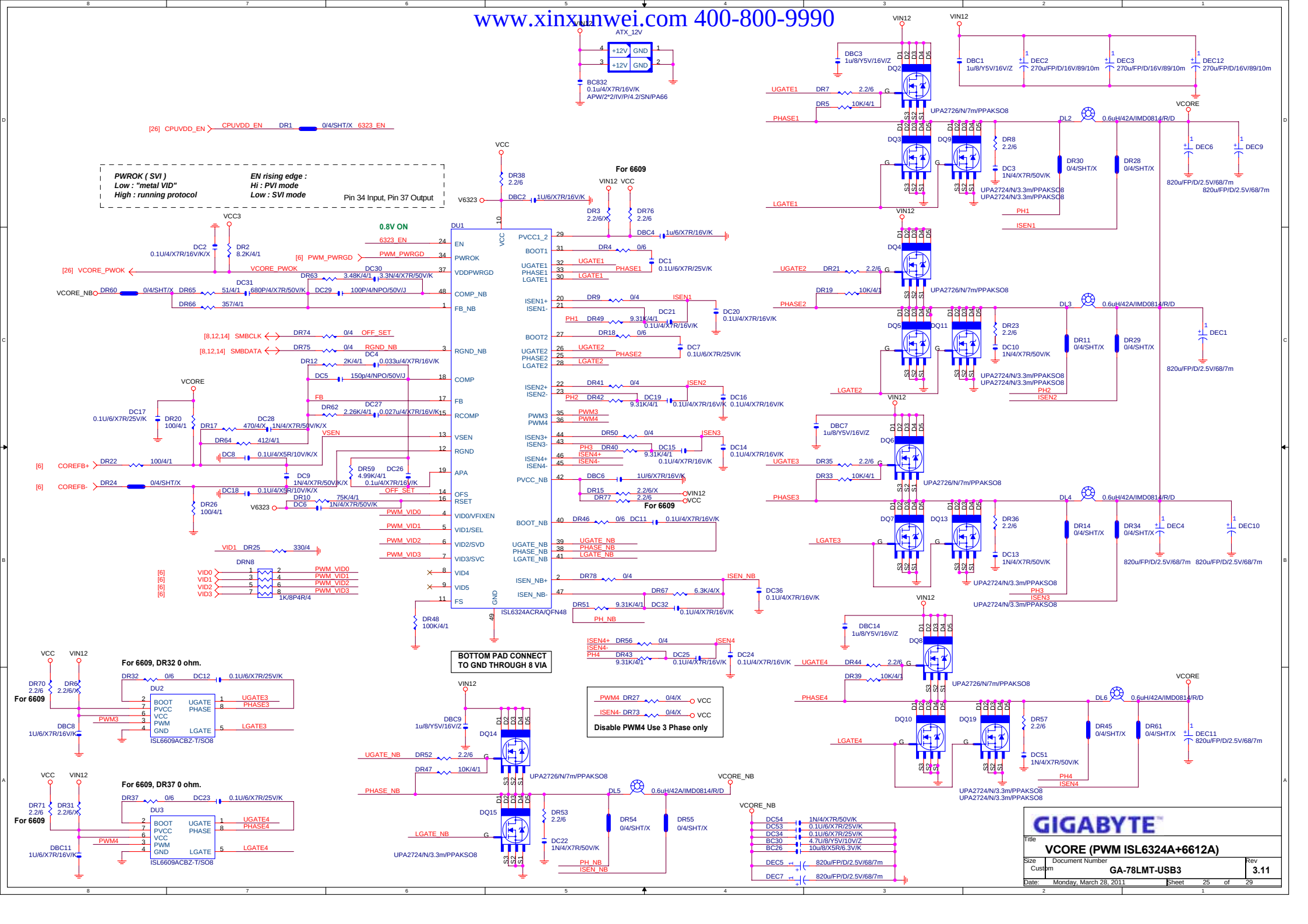

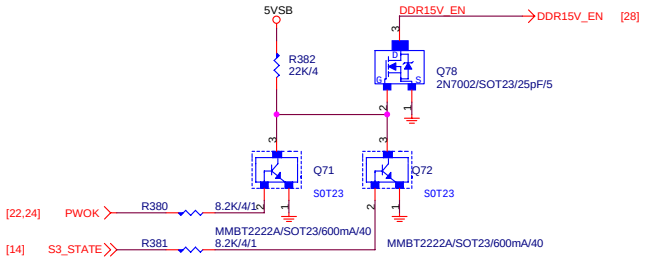

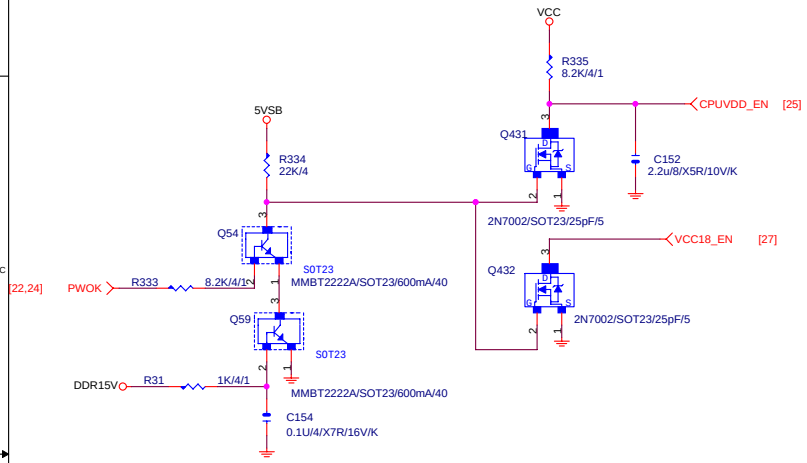

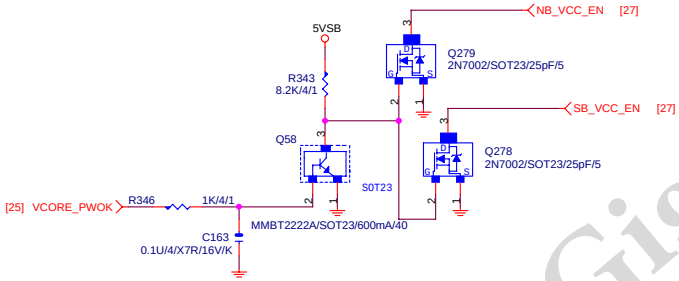

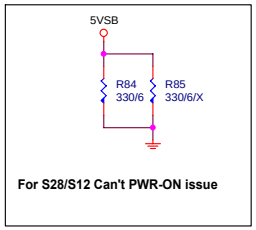

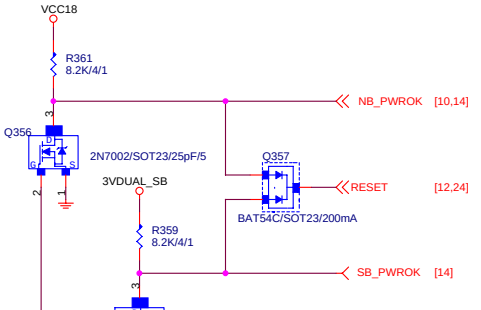

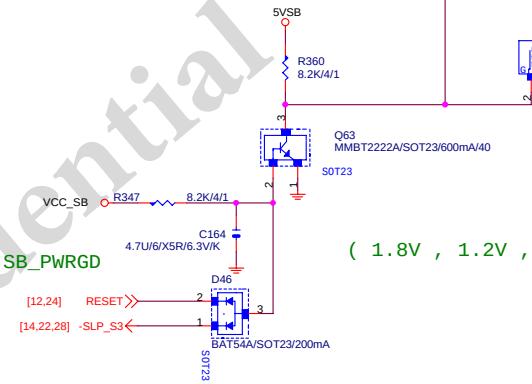

PWOK > NB_PWRGD / SB_PWRGD

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

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Title: POWER SEQUENCE

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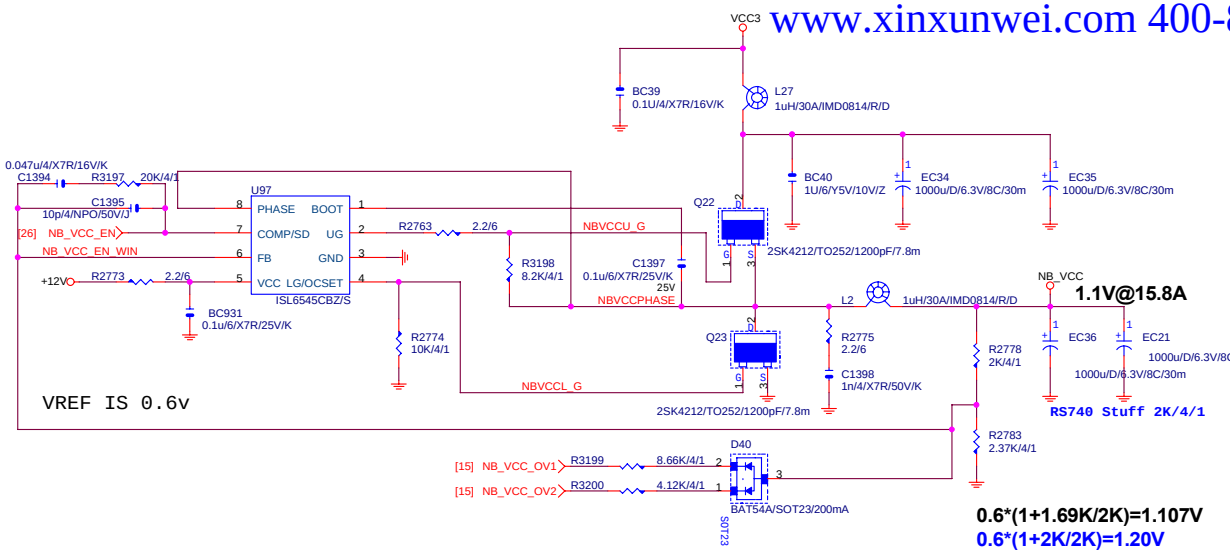
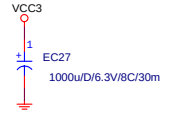
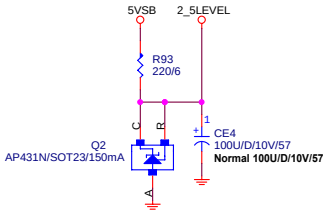


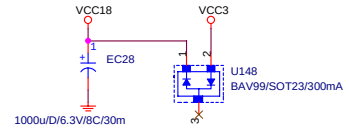
0.6*(1+1.69K/2K)=1.107V

0.6*(1+2K/2K)=1.20V

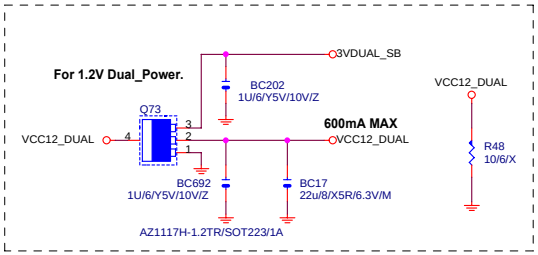
NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V

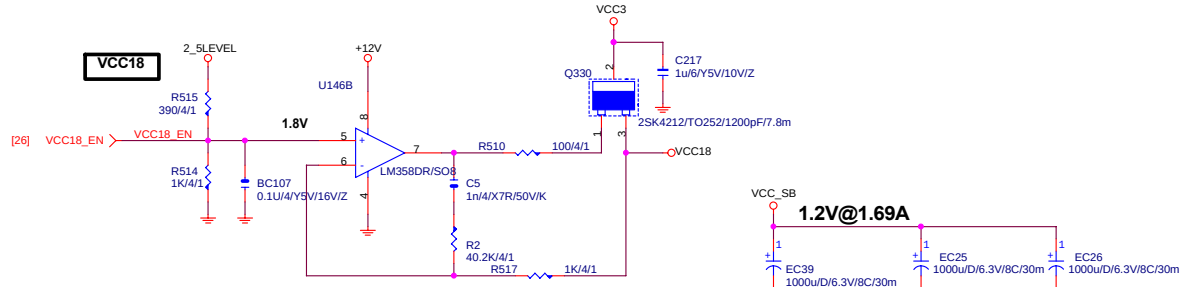


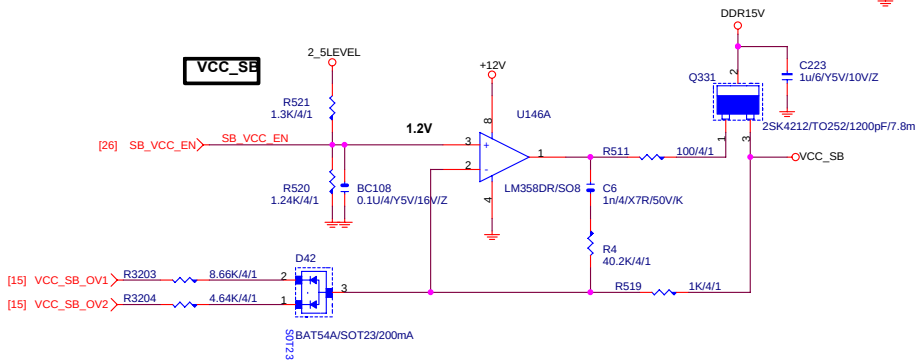




ATI for vcc3/vcc18 power ramp-up 2.1V







VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V

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Title: NB/SB POWER,VCC12HT,VDDA25,VCC12Dual

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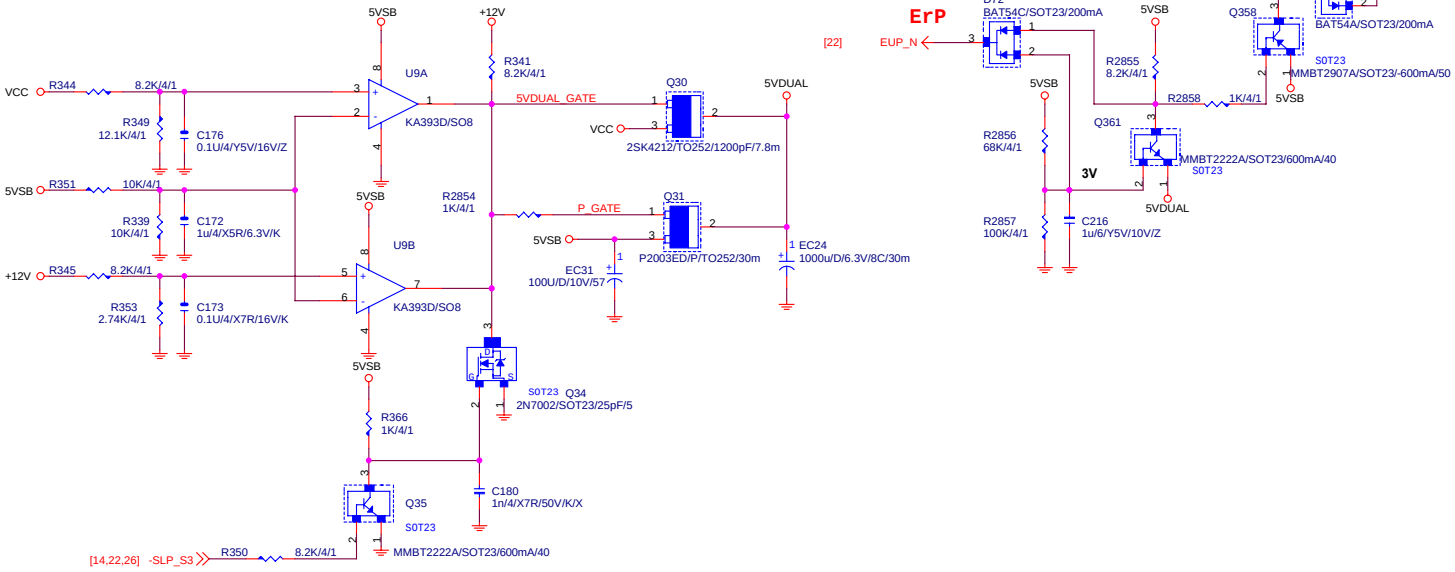
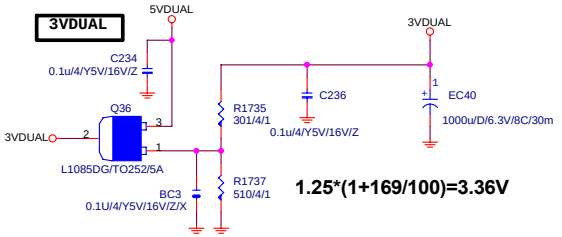
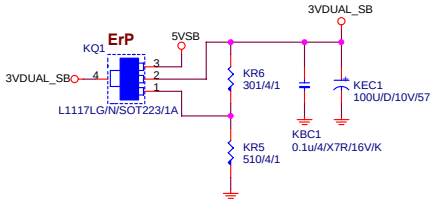
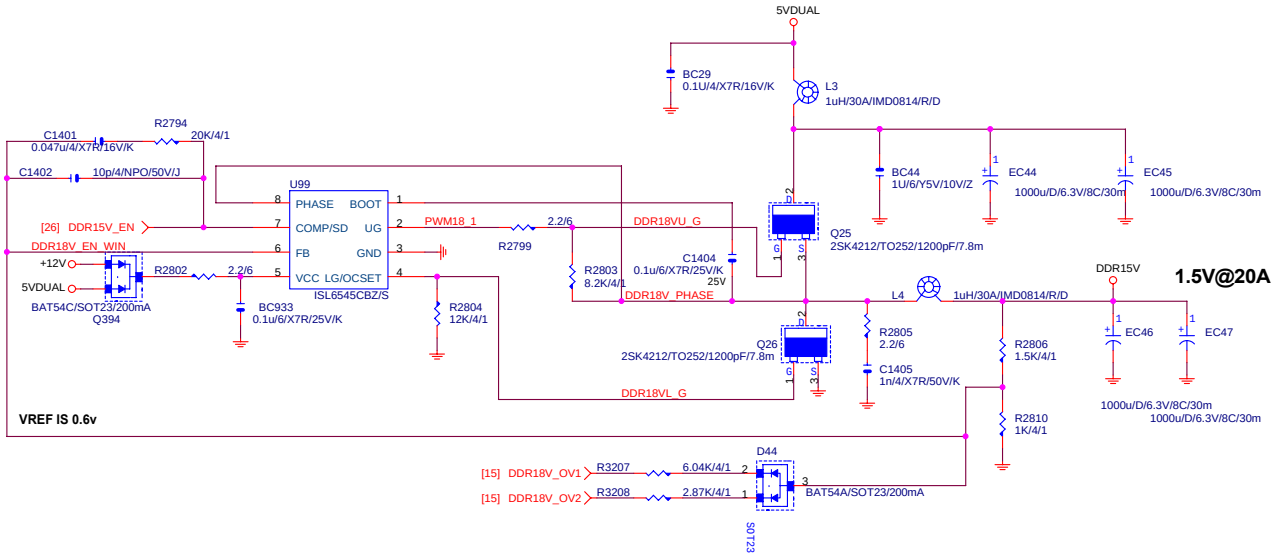
5VDUAL

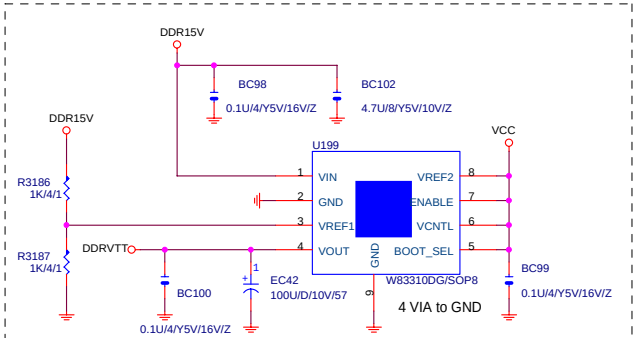


3VDUAL









0.6*(1+3K/1.43K)=1.859V

DDR18V_OV1	DDR18V_OV2	DDR18V
L	X	1.90V
X	L	2.00V
L	L	2.10V

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Title: DDRII POWER , VCC18

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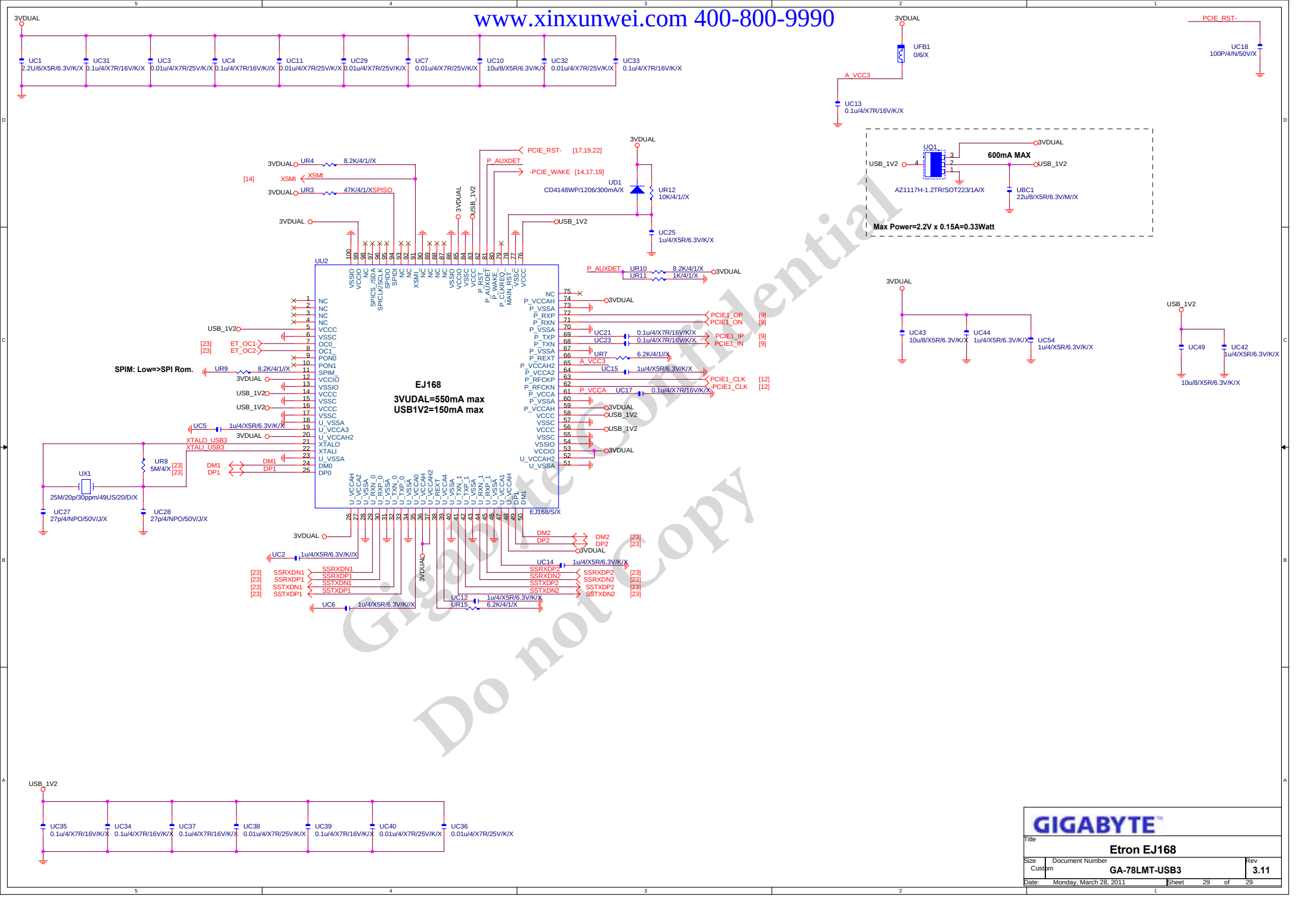

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Title	Etron EJ168	
Size: Custom	Document Number: GA-78LMT-USB3	Rev: 3.11
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