GA-78LMT-S2P

Revision : 5.11

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Title: COVER SHEET		
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Model Name:GA-78LMT-S2P

Component value change history

Version: 5.11

P-Code: U99098-0

Date	Change Item	Reason
2011.08.17	4.0A E_BOM Release. PCB: 4.0	Change From 78LMT-USB3 3.11 Remove USB3.0 / Change EC Cap LAN change to AR8151 Codec：ALC887
2011.09.23	4.0B P_BOM變更 Release. PCB:4.0	FIX SB OV RES R3203 :20K R3204: 10K CLK Change 9LPRS485C 電解改台固容
2011.10.18	4.0B ECN變更 Release. PCB:4.0	add PCB Vender "全誠信"
2011.10.18	4.0C MP BOM變更 Release. PCB:4.01	Change PCB to 4.01
2011.11.08	50A E- BOM change RT8868+RT9612,RT8120D	
	,MOS cgange Power pak, IO 8728 PCB 5.0	
2011.12.09	50B E- BOM release PCB 5.01	(1)R2804(Fix DDR OCP),DR112-->49.9K
		(2)DC58 , DC59 DC60 , DC61-->4.7n ,DR138 DR148 , DR151 , DR146 -->1 ohm
		(3)DR191 , DR101-->2K (4)R2774-->39K (5)DR200 , DR201 --> 0 ohm
		(5)DR104-->40.2K (6) Add" -REQ0" (7)Add R86 for MOS_OT
		(8)DR200 , DR201, R271改爲 short pad
		(9)DR104-->40.2K
2011.12.28	50C E- BOM release PCB 5.02	1.Choke Change 01R/03R (改回霧面) 2. IT8728 DX change IT8728EX 3.~~DEL OR28,OR29~~ 4.R153 change 1.5K(MOS_OT for 104 DC)
2012.08.01	51A E- BOM release PCB 5.1	LAN AR8151 to AR8161 / Fix ErP CTRL by IO

Circuit or PCB layout change for next version

Date	Version	Change Item
2011.08.16	4.0 Gerber out	change From 78LMT-USB3 3.11 (RS760=RS780L)
2011.10.19	4.01 Gerber out	Remove 108dB Wording
2011.11.07	5.0 Gerber out	PWM change RT8868+RT9612,RT8120D,IO8728DX
2011.12.08	5.01 Gerber out	(1.)Load line Control Circuit add DQ27 , (2.)OR24,OR26 pull to 3VDUAL_SB (Fix 5VDUAL be Shutdown & Can't entry ErP issue), (3.) DU1.Pin 23,22,21 Pull to VCC5 (4.) remove 108dB (5)Add D_5VSB
		(6)DR78、DR79、DR80、DR116 shortpad改mask
2011.12.27	5.02 Gerber out	1. EUP_N Change to GP21(OU1.57) 2. ~~CD4 Move to CR35.1 side~~ 3. OR36 Pull to 3VDUAL_SB 4. DRS1 GND 打在PWM 端 5. DEL MCLK/DAT Pull hi OR28,OR29,
2012.07.31	5.1 Gerber out	ErP CTRL by IO

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Title: BOM & PCB HISTORY

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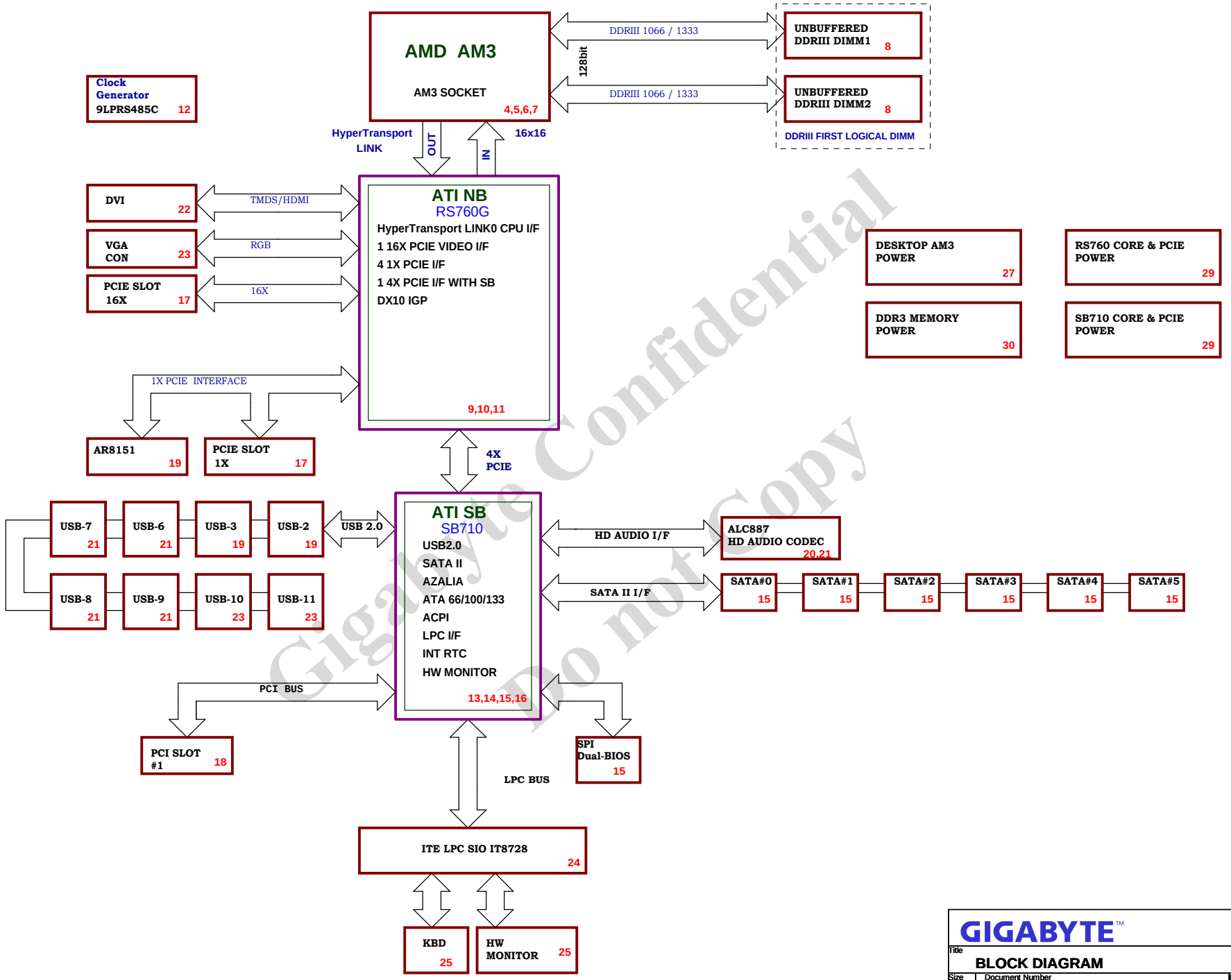
RS780L CUSTOMER DESKTOP DESIGN



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Title: BLOCK DIAGRAM

Size	Document Number	Rev
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] <9>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <9>

L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <9>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <9>

M2CPUA

HYPERTRANSPORT

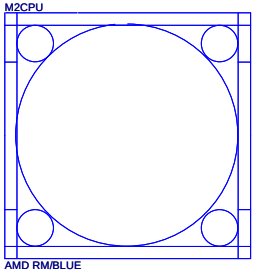
<9> L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 <9>
<9> L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 <9>
<9> L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 <9>
<9> L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 <9>
<9> L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 <9>
<9> L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 <9>
<9> L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 <9>
<9> L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 <9>
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE5	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF4	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AH6	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AG6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AH5	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH4	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)		L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/15u/[10SC1-A01942-01R_10SC1-A01942-02R]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPU



AMD RM/BLUE

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Title: CPU HYPER TRANSPORT

Size	Document Number	Rev
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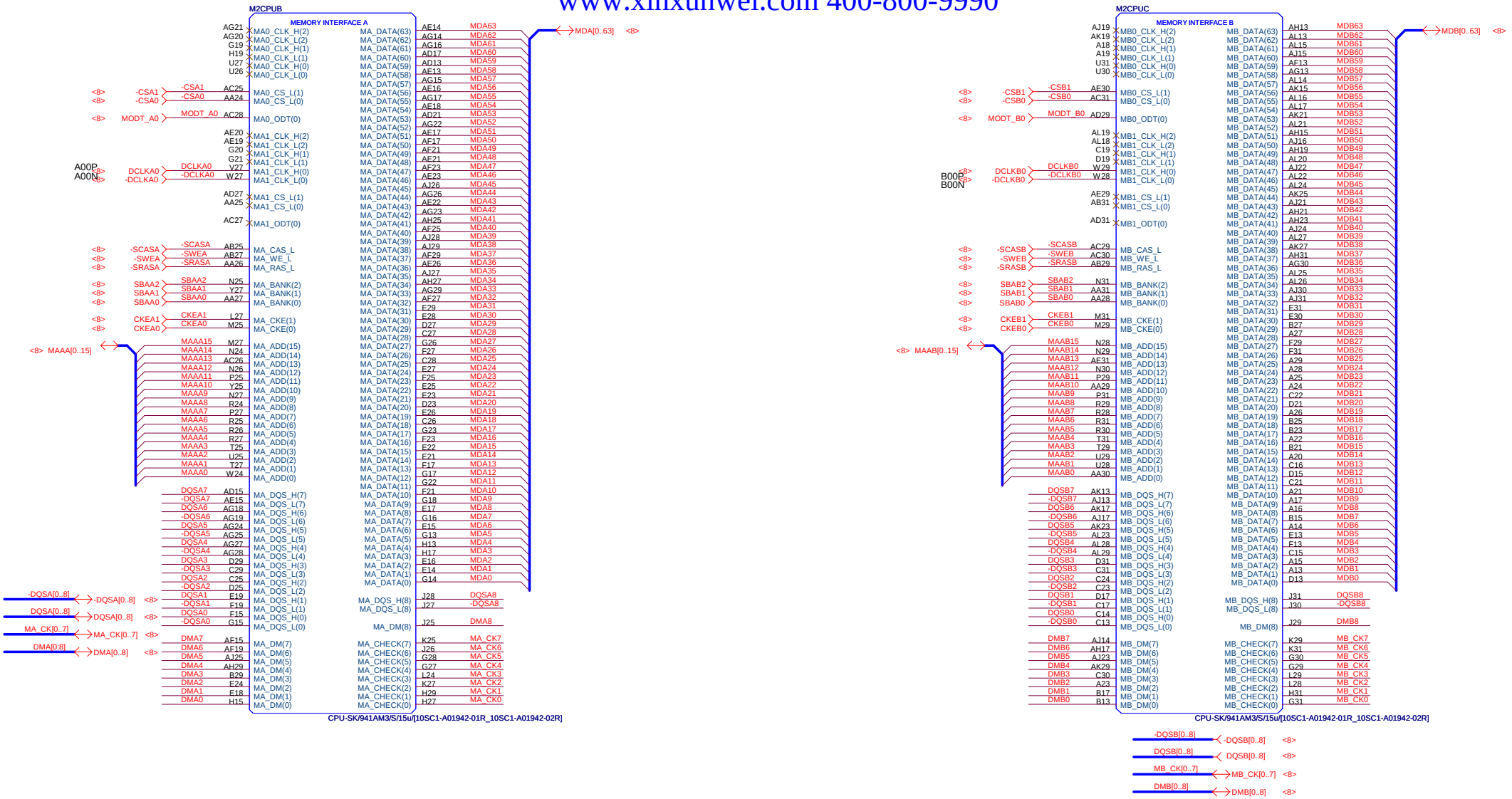

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Title	CPU DDRII MEMORY	
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SB600
CPU_PWR / DDR18V

DDR15V
-CPURST R26 300/4
-LDT_STOP R36 300/4
C74 150P/4/NPO/50V/J/X

-CPURST
C1798 100P4/NPO/50V/J

VCC
BC132 0.1U/4/Y5V/16V/Z
Q62
VDDA25
250mA
VDDA25
L1117LG/N/SOT223/1A
1.25*(1+100/100)=2.5V
R394 100/4/1
BC18 22U/8/X5R/6.3V/M
BC2 0.1U/4/Y5V/16V/Z/X Asus-used
R395 100/4/1

VDDA25
C3 4.7u/8/Y5V/10V/Z
C13 3.3n/4/X7R/50V/K
C4 0.22u/6/X7R/16V/K

VCORE
BC1 0.01U/4/X7R/25V/K
<12> CPUCLK0_H CPUCLK0_H C1 3.9n/4/X7R/50V/K
<12> CPUCLK0_L CPUCLK0_L C2 3.9n/4/X7R/50V/K
R5 169/4/1

M2CPUD
MISC
C10 VDDA1
D10 VDDA2
A8 CLKIN_H
B8 CLKIN_L
C9 PWROK
D8 LDTSTOP_L
C7 RESET_L
AL3 CPU_PRESENT_L
AL6 SIC
AK6 SID
AL10 TDI
AJ10 TRST_L
AH10 TCK
AL9 TMS
A5 DBREQ_L
G2 VDD_FB_H
G1 VDD_FB_L
E12 VTT_SENSE
F12 M_VREF
AH11 M_ZN
AJ11 M_ZP
A10 TEST25_H
B10 TEST25_L
F10 TEST19
E9 TEST18
AJ7 TEST13
F6 TEST9
D6 TEST17
E7 TEST16
F8 TEST15
C5 TEST14
AH9 TEST12
E5 TEST7
AJ5 TEST6
AG9 THERMDC
AG8 THERMDA
AH7 TEST3
AJ6 TEST2
D2 VID(5)
D1 VID(4)
C1 VID(3)
E3 VID(2)
E2 VID(1)
E1 VID(0)
AK7 THERMTRIP_L
AL7 PROCHOT_L
AK10 TDO
B6 DBRDY
AK11 VDDIO_FB_H
AL11 VDDIO_FB_L
F1 PSI_L
V8 HTREF1
V7 HTREF0
C11 TEST29_H
D11 TEST29_L
AK8 TEST24
AH8 TEST23
AJ9 TEST22
AL8 TEST21
AJ8 TEST20
J10 TEST28_H
H9 TEST28_L
AK9 TEST27
AK5 TEST26
G7 TEST10
D4 TEST8

CPU-SK/941AM3/S/15u/[10SC1-A01942-01R_10SC1-A01942-02R]

DDR15V
R2555 1K/4/1
R2557 1K/4/1
R57 300/4
R60 300/4
R87 1K/4X
R2556 1K/4X
R2558 1K/4X

3VDUAL
R59 8.2K/4/1
THERMTRIP_CPU_L
THERMTRIP_CPU_L <14>
Q9 MMBT2222A/SOT23/600mA/40
S0T23
DDR15V R176 1K/4/1
Q10
S0T23
R174 1K/4/1
MMBT2222A/SOT23/600mA/40
-PROCHOT_CPU <13,26>

VID3 <24>
VID2 <24>
VID1 <24>
VID0 <24>
THERMTRIP_L
-PROCHOT_CPU

Erratum 133, Revision Guide for AMD NPT 0Fh Processors

3VDUAL
VCC3
R2506 8.2K/4/1
R2507 8.2K/4/1
PWM_PWRGD <24>
C1752 0.1u/4/Y5V/16V/Z/X
DDR15V
R2756 300/4
<13> CPU_PG_SB
R1 1K/4/1
Q309
Q310
MMBT2222A/SOT23/600mA/40
2N7002/SOT23/25pF/5

PWROK >
SVC/SVD(CPU_PWROK)
10 uS

DDR15V
R2754 300/4
CPU_PWRGD
Q355
C1790 0.1u/4/Y5V/16V/Z/X
C1791 0.01U/4/X7R/25V/K/X
2N7002/SOT23/25pF/5

SI_CLK <22>
SI_DAT <22>
R17 1K/4/1
R19 1K/4/1
R49 1K/4/1 CPU_PRESENT_L
R75 1K/4/1 CPU_TDI
CPU_TRSTL
CPU_TCK
CPU_TMS
R35 1K/4/1 CPU_DBREQL
COREFB+ <24>
COREFB- <24>

CPU_M_VREF
R11 39.2/4/1 M_ZN
R12 39.2/4/1 M_ZP
R42 510/4/1 CPU_TEST25_H
R43 510/4/1 CPU_TEST25_L
R13 300/4 CPU_TEST18
R14 300/4 CPU_TEST19
R2727 1K/4/1 CPU_TEST12
GNDA <22>
TMPIN2 <22>

R53 44.2/4/1
R54 44.2/4/1
VCC_SB
R55 80.6/4/1/X

Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin

CPU_TEST24 R2731 1K/4/1
CPU_TEST23 R44 1K/4/1
CPU_TEST22 R2730 1K/4/1
CPU_TEST21 R47 1K/4/1
CPU_TEST20 R2729 1K/4/1
CPU_TEST27 R2728 1K/4/1
CPU_TEST26 R37 1K/4/1

M2CPUE
INTERNAL MISC
L25 RSVD1
L26 RSVD2
L31 RSVD3
L30 RSVD4
MA_RESET-
MB_RESET-
RSVD19
RSVD20
RSVD21
RSVD22
M_VDDIO_PWRGD
W26 DCLKA2
W25 DCLKA2-
AE27 MODT_A3
V24 DCLKA1
AE28 DCLKA1-
MODT_A1
Y31 DCLKB2
Y30 DCLKB2-
AG31 MODT_B3
V31 DCLKB1
W31 DCLKB1-
AE31 MODT_B1
COREFB_NB+
COREFB_NB-
CORE_TYP_DET
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
MB_EVENT_L
MA_EVENT_L
E20 MA_RESET_L
B19 MB_RESET_L
AL4 CPU_ALERT-
AK4
AK3
F2
F3 CPU_IDLEEXIT-
G4
G3
G5 CORE_TYPE_DET
AD25
AE24
AE25
AJ18
AJ20
C18
C20
G24
G25
H25
V29
W30

AM3 only
AM2: high, AM2R2: low
AM3 =>DRAM Thermal Event Status
R104 1K/4/1
MB_EVENT_L
MA_EVENT_L
R105 1K/4/1
EVENT pins are for future AM3r2

A01P
A01N
DCLKA1 <8>
-DCLKA1 <8>
MODT_A1 <8>
B01P
B01N
DCLKB1 <8>
-DCLKB1 <8>
MODT_B1 <8>

MA_RESET_L <8>
MB_RESET_L <8>
R16 1K/4/1
R21 1K/4/1
R10 1K/4/1
COREFB_NB+ <24>
COREFB_NB- <24>
R2448 300/4

Layout: Route as 60 ohms with 5/10 W/S from CPU pins.

CPUVREF
40 MILS WIDTH
DDR15V
SR19 16.9/4/1
CPU_M_VREF
SBC12
SBC31
SC35 1U/6/X7R/16V/K
SR20 16.9/4/1
1N/4/X7R/50V/K
0.1u/4/X7R/16V/K

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Title	CPU CONTROL	
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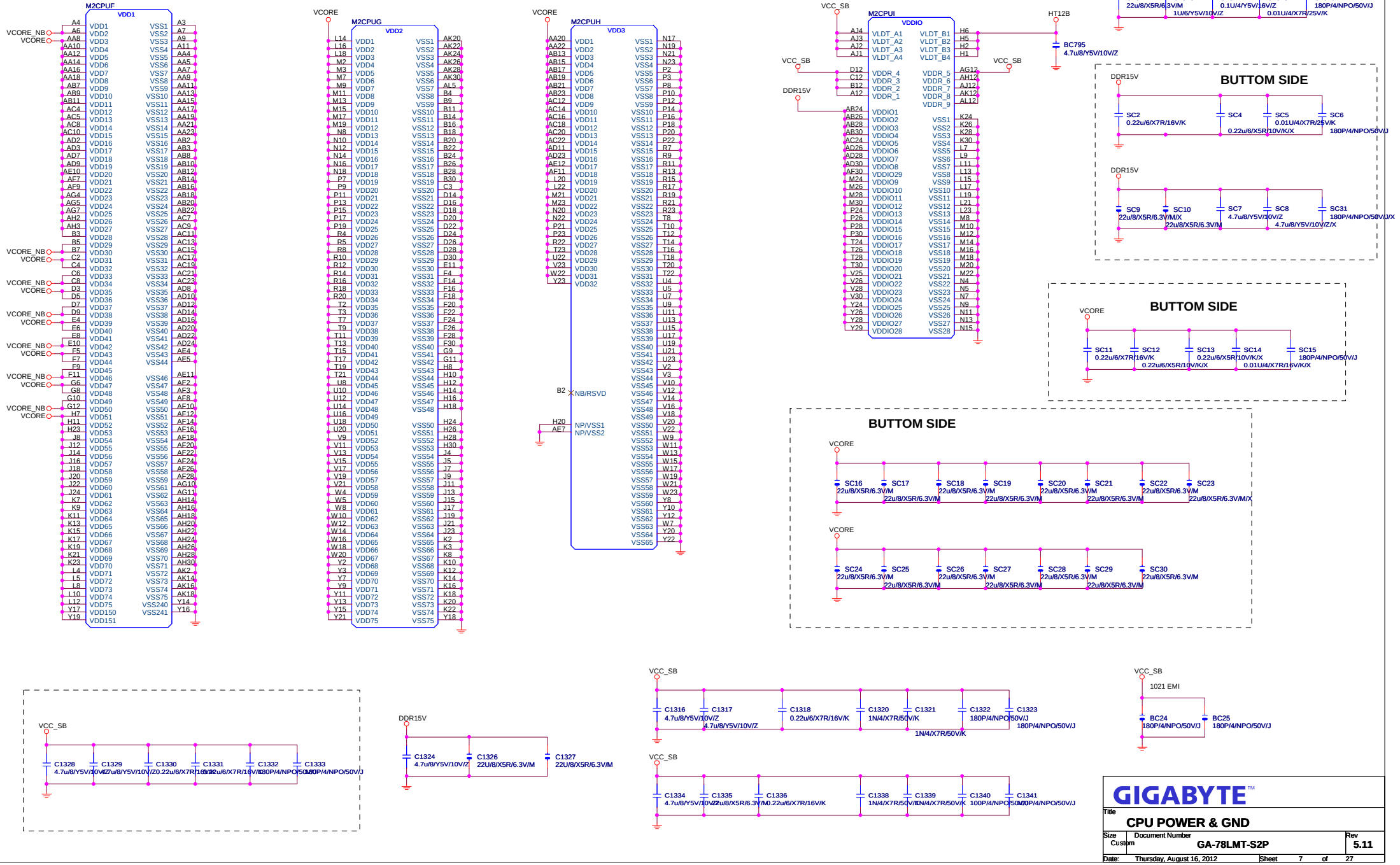
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



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Title: CPU POWER & GND			
Size: Custom	Document Number: GA-78LMT-S2P		Rev: 5.11
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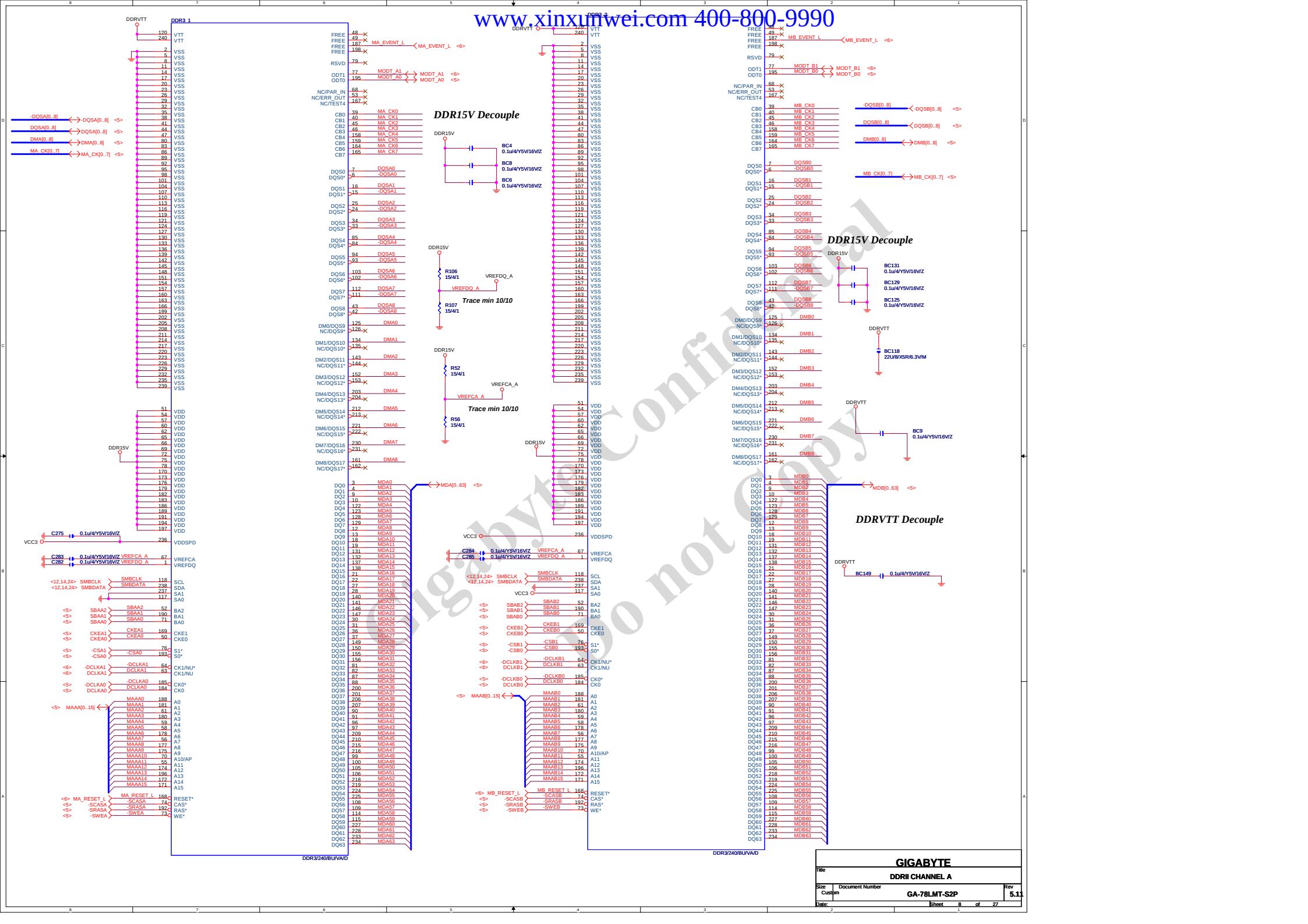

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Title: DDRII CHANNEL A		
Size: Custom	Document Number: GA-78LMT-S2P	Rev: 5.11
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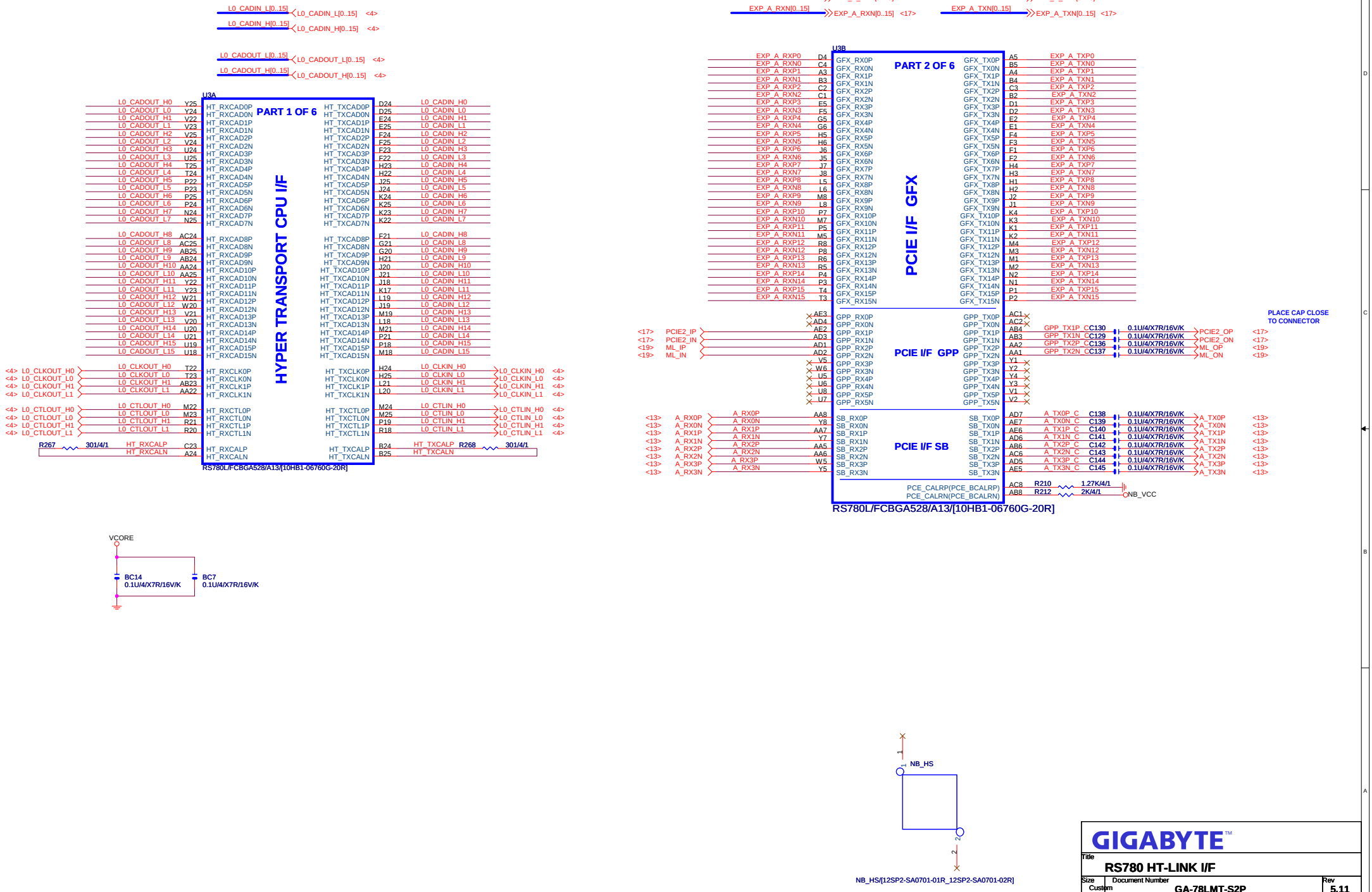

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Title	RS780 HT-LINK I/F	
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RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

RS740_DFT_GPIO1 R272 150/4/1

Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly

<21> DAC_VSYNC R276 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly

R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

<21> DAC_HSYNC R285 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly

R219 (RX780_DFT_GPIO0)

EMI 20080103
SR4 0/6/SHT/X

U3C

PART 3 OF 6

CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

U3D

PAR 4 OF 6

SBD_MEM/DVO_I/F

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

SR1~SR3 PLACED WITHIN 1' OF NB

SR3 150/4/1 SR2 150/4/1 SR1 140/4/1

NB_PWROK
EMI ESD ISSUE
C7 100P/4/NPO/50V/J/X

SBC34 1U/6/Y5V/10V/Z
BC139 1U/6/Y5V/10V/Z
SBC29 1U/6/Y5V/10V/Z

SBC35 10u/8/X5R/6.3V/K
BC143 1U/6/Y5V/10V/Z
SBC36 1U/6/Y5V/10V/Z
SBC15 0.1u/4/Y5V/16V/Z

BC150 1U/6/Y5V/10V/Z
BC151 0.1U/4/Y5V/16V/Z
BC145 0.1U/4/Y5V/16V/Z
BC146 1U/6/Y5V/10V/Z

Q74 P8503BMG/SOT23/450pF/85m
R156 8.2K/4/1 +12V

BC678 0.1U/4/Y5V/16V/Z
R2128 4.7K/4
R2127 4.7K/4
R312 33/4
D9 AME385BEETZ/SOT23/2.5V
R331 100K/4/1

M1 DVI-D/24P/SC/RA/D/SH
M2 M5 M6 M7 M8

ESD1 AOZ8902CIL/SOT23-6
ESD2 AZ1045-04F/MSOP10
ESD3 AZ1045-04F/MSOP10

R159 150/4/1
R158 150/4/1
REFCLKN

R271 0/4/SHT/X
R265 8.2K/4/1 STRP_DATA
R279 1.8K/4/1

BC141 1U/6/Y5V/10V/Z
BC60 0.1u/4/Y5V/16V/Z
BC61 0.1u/4/Y5V/16V/Z

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Title: RS780 SYSTEM I/F,STRAP

Size: Custom | Document Number: GA-78LMT-S2P | Rev: 5.11

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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

U3F — PART 6/6 — GROUND

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

Please use 1mm pad size, place all ELT test pads on bottom side only

U3E — PART 5/6 — POWER

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

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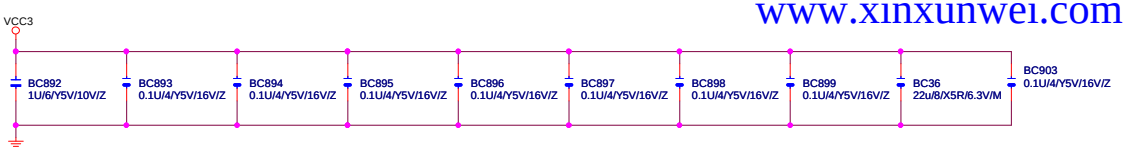
Title: RS780 POWER & GND

Size: Custom | Document Number: GA-78LMT-S2P | Rev: 5.11

Date: Thursday, October 04, 2012 | Sheet 11 of 27



1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

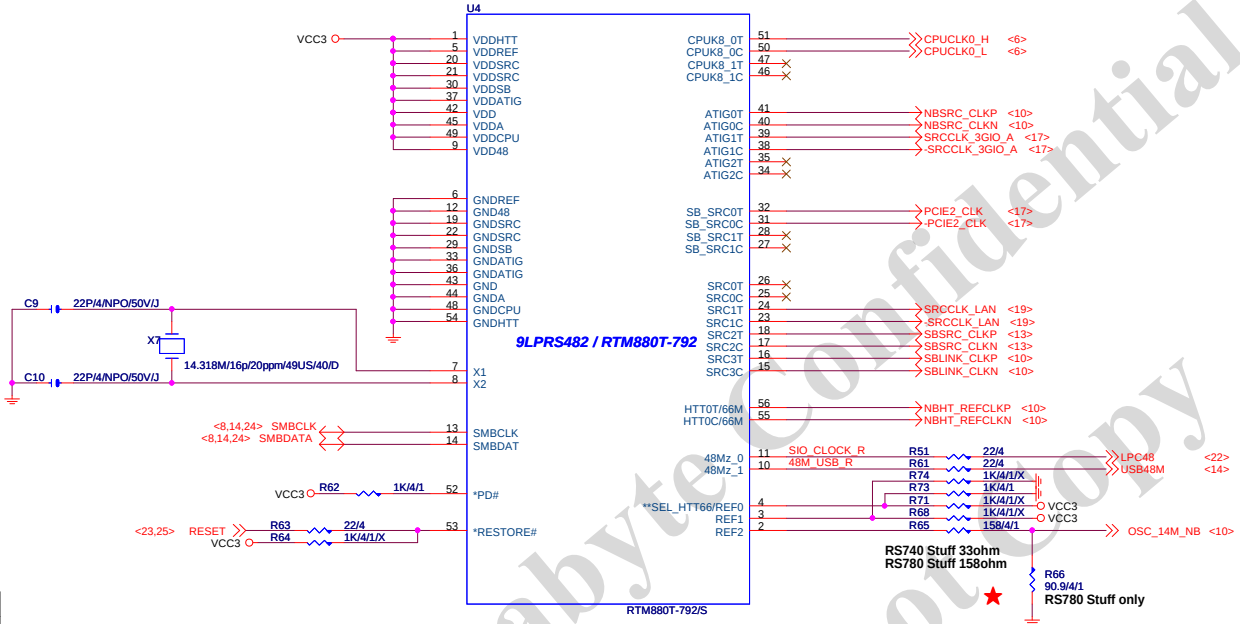
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



watch dog --
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

GIGABYTE™

Title: RTM880T-792

Size: Custom | Document Number: GA-78LMT-S2P | Rev: 5.11

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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK

SB_HS

SB_HS/[12SP2-030005-42R_12SP2-030005-43R]

U2A

SB700

Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

PCI CLKS

LPC

RTC XTAL

CPU

RTC

SB710/FCBGA528/A14/[10HB1-06B710-11R]

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

PCLK2 R126 8.2K/4/1

PCLK3 R124 8.2K/4/1

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

LPC_CLK0 R121 8.2K/4/1

LPC_CLK1 R115 8.2K/4/1

BIOS after boot setting
EC AOD-ACC

	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

20mil 20mil 20mil

BAT-SK/BK/P/S/D/SN

BATTERY CR2032

CLR_CMOS

PH/1*2/BK/2.54/VA/D

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

Title	ATI SB710 PCIE/PCI/CPU/LPC
Size	Custom
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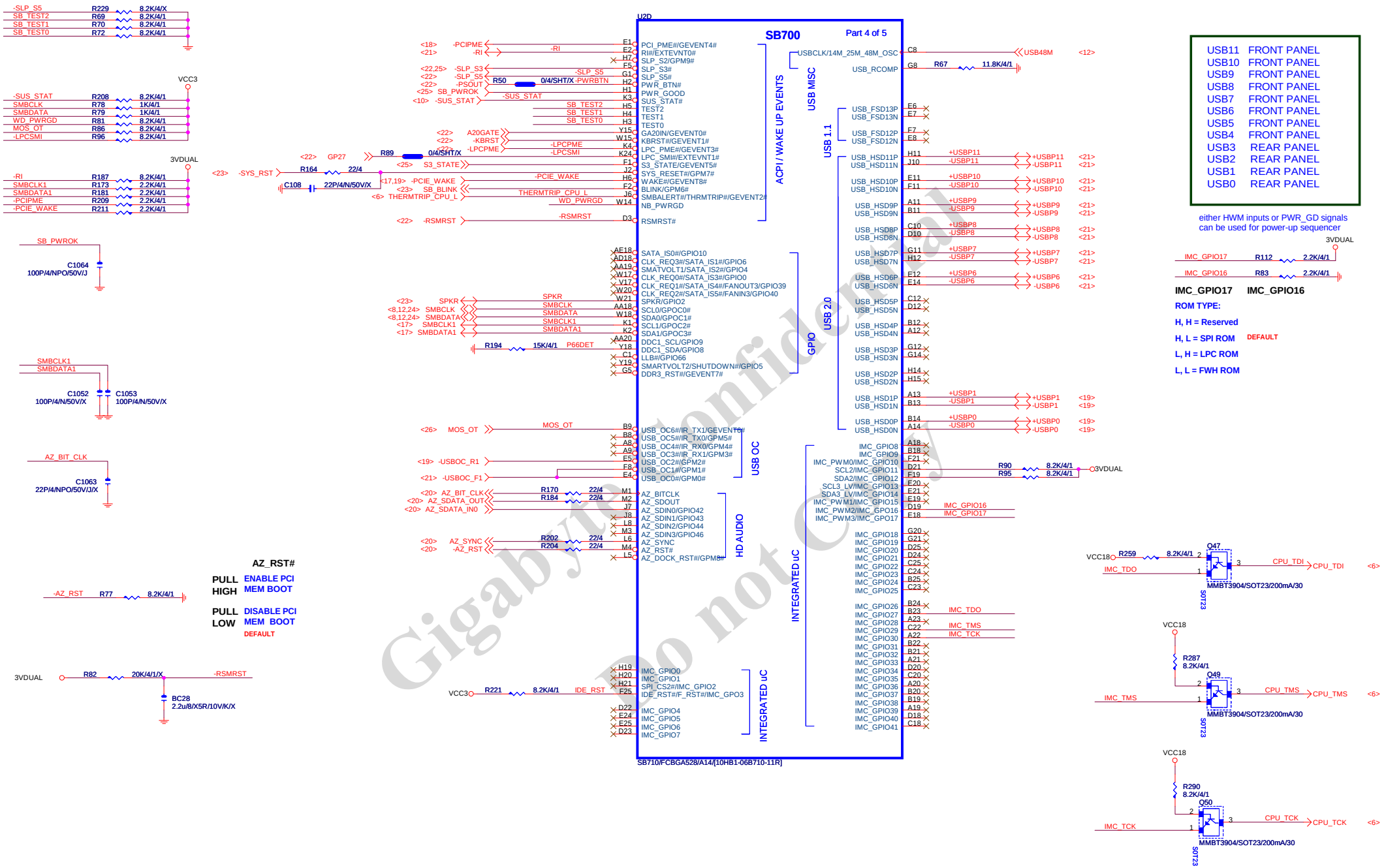

GIGABYTE™

Title: ATI SB710 ACPI/USB/GPIO/AUDIO

Size	Document Number	Rev
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Date: Thursday, August 16, 2012 Sheet 14 of 27

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

U2B
SB700
Part 2 of 5
SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR
SB710/FCBGA528/A14/[10HB1-06B710-11R]

M_BIOS
B_BIOS
16M/SPI/SO8/200mil/S

GIGABYTE

Title	ATI SB710 SATA/IDE/HWM/SPI	
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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

U2C

SB700

Part 3 of 5

POWER

1.8V: Flash module mode
3.3V: IDE mode

SB710/FCBGA528/A14/[10HB1-06B710-11R]

U2E

SB700

GROUND

Part 5 of 5

SB710/FCBGA528/A14/[10HB1-06B710-11R]

BAT54C/SOT23/200mA

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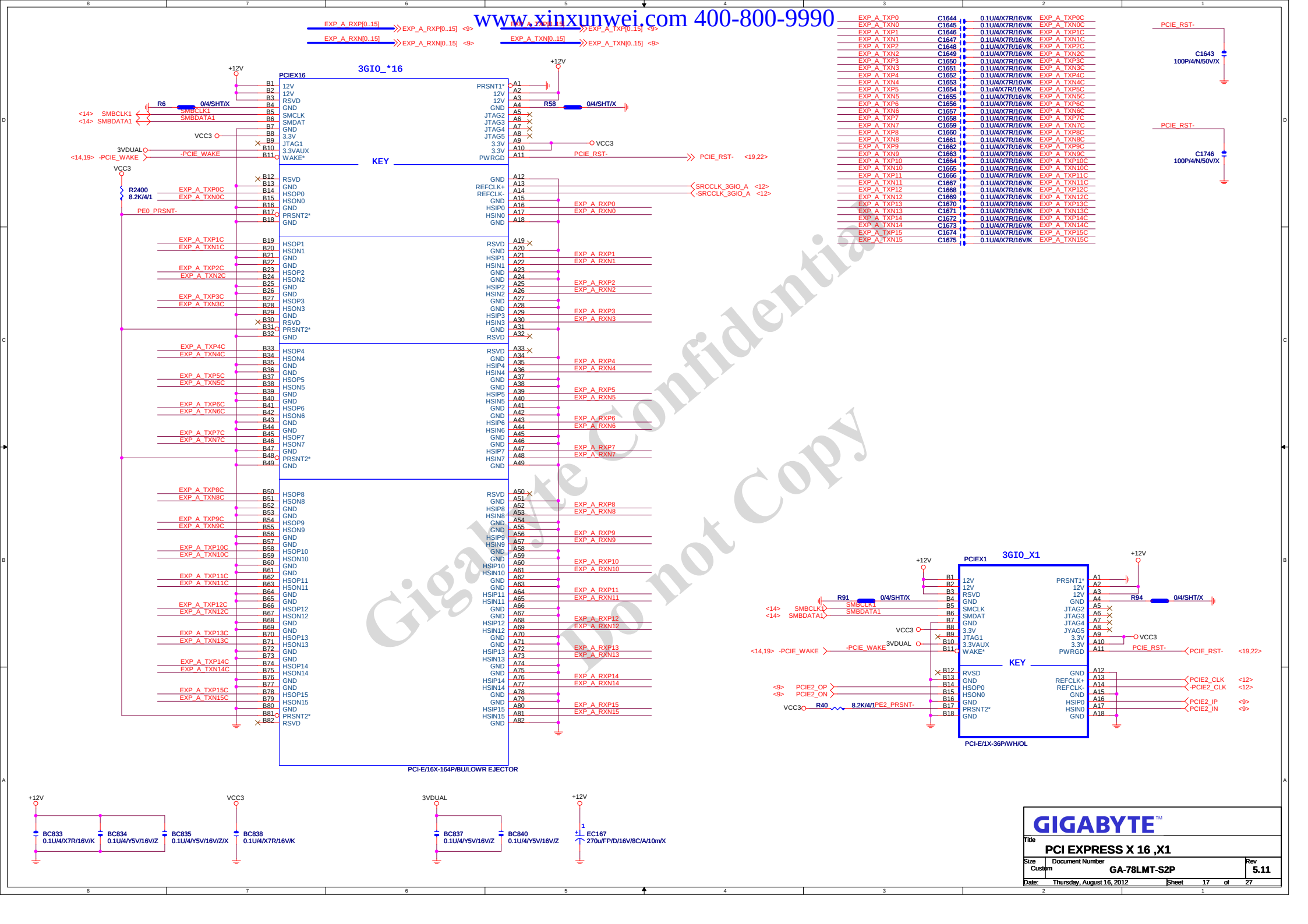
Title: ATI SB700 POWER & GND

Size: Custom | Document Number: GA-78LMT-S2P | Rev: 5.11

Date: Thursday, October 04, 2012 | Sheet 16 of 27



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Title: PCI EXPRESS X 16 ,X1

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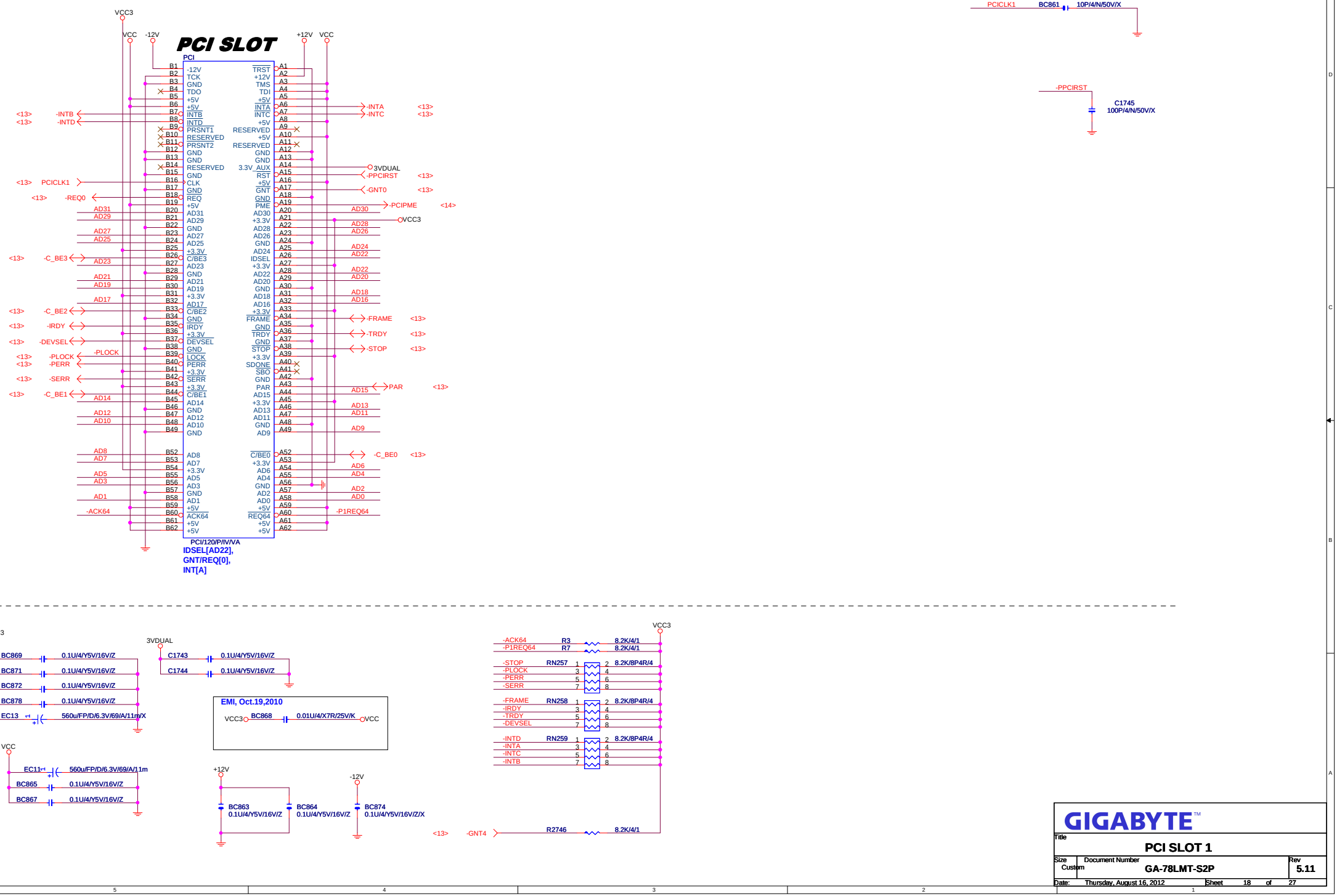
PCI SLOT 1,2



Title	PCI SLOT 1
Size	Custom
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LAN:AR8151/AR8161

離IC近越好

LA_ ML-->80歐姆:[15/5/5/5/15]

SRCCLK-->50歐姆:[18/4/10/4/18]

<12> -SRCCLK_LAN
<12> SRCCLK_LAN
<9> ML_OP
<9> ML_ON

LABC5 0.1u/4/X7R/16V/K
LABC4 1u/4/X5R/6.3V/K
LABC3 0.1u/4/X7R/16V/K
LABC6 0.1u/4/X7R/16V/K/X
AR8161-->N/A (LABC6)

LA_AVDDVCO
LABC7 0.1u/4/X7R/16V/K
LABC8 4.7u/6/X5R/6.3V/K
AR8161-->(0)

3VDUAL
LABC9 10u/6/X5R/6.3V/M
LABC10 1u/4/X5R/6.3V/K
LABC11 0.1u/4/X7R/16V/K

LA_LX
LA_LED_LINK100
LA_LED_ACT_TXRX
LA_DVDDL
LA_AVDDVCO
LA_AVDDL

LAU1

LA_ ML-->80歐姆:[15/5/5/5/15]

離IC近越好

3VDUAL
LABC33 100p/4/NPO/50V/J/X
LAR6 8.2K/4/1

<17,22> PCIE_RST-
<14,17> -PCIE_WAKE

AR8161-->N/A (LABC12)

LABC12 1u/4/X5R/6.3V/K/X
LABC15 1u/4/X5R/6.3V
LABC16 0.1u/4/X7R/16V/K
LABC18 1u/4/X5R/6.3V
LABC19 0.1u/4/X7R/16V/K
LAR10 2.37K/4/1

1	VDD3V	TX_P	30
2	PERST#	TX_N	29
3	WAKE#	NC	28
4	CLKREQ#	TESTMODE	27
5	VDDCT/ISOLAT	SMDATA	26
6	AVDDL_REG	SMCLK	25
7	XTLO	DVDDL/PPS	24
8	XTLI	LED2	23
9	AVDDH_REG	AVDDH	22
10	RBIAS	TRXN3	21

Atheros
AR8151/AR8161
AR8161-BL3A-R/QFN40/[10HP2-408161-10R]

LA_VDD33
LA_-CLKREQ
LA_VDDCT
LA_AVDDL
LA_XTALO
LA_XTALI
LA_AVDDH
LA_RBIAS

LA_ML_IP_C LAC12 0.1u/4/X7R/16V/K ML_IP <9>
LA_ML_IN_C LAC13 0.1u/4/X7R/16V/K ML_IN <9>

LA_PPS
LA_LED_LINK1000
LA_AVDDH
LA_MDI3-

LAR9 0/4/X
LABC14 LA_DVDDL 0.1u/4/X7R/16V/K
AR8161-->N/A (LAR9,LABC14)

LABC17 0.1u/4/X7R/16V/K

LAX1 25M/20p/30ppm/49US/20/D
LA_XTALI
LA_XTALO
LAC31 27p/4/NPO/50V/J
LAC32 27p/4/NPO/50V/J

LA_MDI0+ LA_MDI0- LA_AVDDL LA_MDI1+ LA_MDI1- LA_AVDD33 LA_MDI2+ LA_MDI2- LA_AVDDL LA_MDI3+ LA_MDI3-

LABC20 0.1u/4/X7R/16V/K/X
AR8161-->N/A (LABC20)

LABC21 0.1u/4/X7R/16V/K

LAR19 0/4/SHT/M/X
LAR20 0/4/X
3VDUAL
LA_AVDDH

AR8151:LA_AVDDH(LAR20)
AR8161:3VDUAL(LAR19)

LABC22 1u/4/X5R/6.3V/K

SCH BOM OPT:(二擇一使用)
-->(LAC30):M/B有CLK GEN 25M
-->(LAX1,LAC31,LAC32):M/B無CLK GEN 25M

LAN POWER

NEW DESIGN ONLY FOR INTERNAL SWR
AR8151:LAR3(0),LAR5(X)
AR8161:LAR5(0),LAR3/LAR4(X)

EMI Request
Put on LAR4

LA_LX_OUT
LAESD2
AZ2225-01L/SOD323/X

LAL1 4.7uH/1A/[10LC4-5A470B-01R_10LI5-12470B-01R]
LA_LX_OUT LA_LX
CLOSE LA_LX 200mil
LABC1 10u/6/X5R/6.3V/M
LABC2 0.1u/4/X7R/16V/K

LA_VDDCT
LAR3 0/4/X
AR8161-->N/A (LAR3,LAR4)
AR8151 POWER

LA_AVDD_CEN
LAR4 0/4/X

LA_DVDDL LA_AVDDL LA_AVDDVCO
LAR5 0/6/SHT/M/X AR8161-->(0)
LAFB2 0/6/SHT/M/X AR8161-->BEAD AR8151-->N/A
LAFB3 0/6/SHT/M/X AR8161-->BEAD AR8151-->0/6
AR8161 POWER

AR8161-->(0)
LA_AVDDH
LAR7 8.2K/4
LA_LED_ACT_TXRX
LA_LED_LINK100
LAR8 8.2K/4

AR8161-->(0)
VCC3
LAR1 30K/4/1
LAR2 0/4/SHT/M/X
LA_VDDCT
N_ISOLATEB <22>

Power domain chart

	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	

MDI : AR8161-->N/A

LA_MDI0+ LA_MDI0-
LAR11 49.9/4/1/X
LAR12 49.9/4/1/X
LA_MDI_RC0
LAC26 0.1u/4/X7R/16V/K/X

LA_MDI1+ LA_MDI1-
LAR13 49.9/4/1/X
LAR14 49.9/4/1/X
LAR15 49.9/4/1/X
LA_MDI_RC1
LAC27 0.1u/4/X7R/16V/K/X

LA_MDI2+ LA_MDI2-
LAR16 49.9/4/1/X
LA_MDI_RC2
LAC28 0.1u/4/X7R/16V/K/X

LA_MDI3+ LA_MDI3-
LAR17 49.9/4/1/X
LAR18 49.9/4/1/X
LA_MDI_RC3
LAC29 0.1u/4/X7R/16V/K/X

CLOSE LAN CHIP

USB_LAN CONNECTOR

3VDUAL
LFB4 0/6/SHT/X

LABC23 0.1u/4/X7R/16V/K
LA_AVDD_CEN
USB_LAN
LA_MDI0+ LA_MDI0- LA_MDI1+ LA_MDI1- LA_MDI2+ LA_MDI2- LA_MDI3+ LA_MDI3-
GND_L10
LABC25 0/4/SHT/M/X

D1 LA_LED_ACT_TXRX
D2 LA_LED_D2 LR13 150/4/1 LAN_3VDUAL_LED
D3 LA_LED_LINK100 LR21 150/4/1
D4 LA_LED_LINK1000 LR22 150/4/1
LBC33 0.1u/4/Y5V/25V/Z/X

UP
DOWN

U1 U2 -USBP0 -USBP0 <14>
U3 +USBP0 +USBP0 <14>
U4 U5 FUSEVCC
U6 -USBP1 -USBP1 <14>
U7 +USBP1 +USBP1 <14>
U8
LBC26 0.1u/4/Y5V/25V/Z/X
LBC29 0.1u/4/Y5V/25V/Z/X

USB+LAN/1G/GO,Y/OS/RA/D/8C/[11NR6-702009-0ER]

LAESD1
LA_LED_LINK100 LA_LED_ACT_TXRX
LAN_3VDUAL_LED
LA_LED_LINK1000 LA_LED_D2
AOZ8902CIL/SOT23-6

FUSEVCC
LEC4 560u/FP/D/6.3V/69/A/11m
EC要靠近USB_PORT的FUSEVCC

USB_LAN
EMI
LR28 0/6/SHT/X

SU1
-USBP0 -USBP1
FUSEVCC
+USBP0 +USBP1
AOZ8902CIL/SOT23-6

5VDUAL F6 SMD1812P260/6V FUSEVCC
FUSEVCC R3161 150K/4 -USBOC_R1 <14>
R3162 270K/4

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Title	AR8151	
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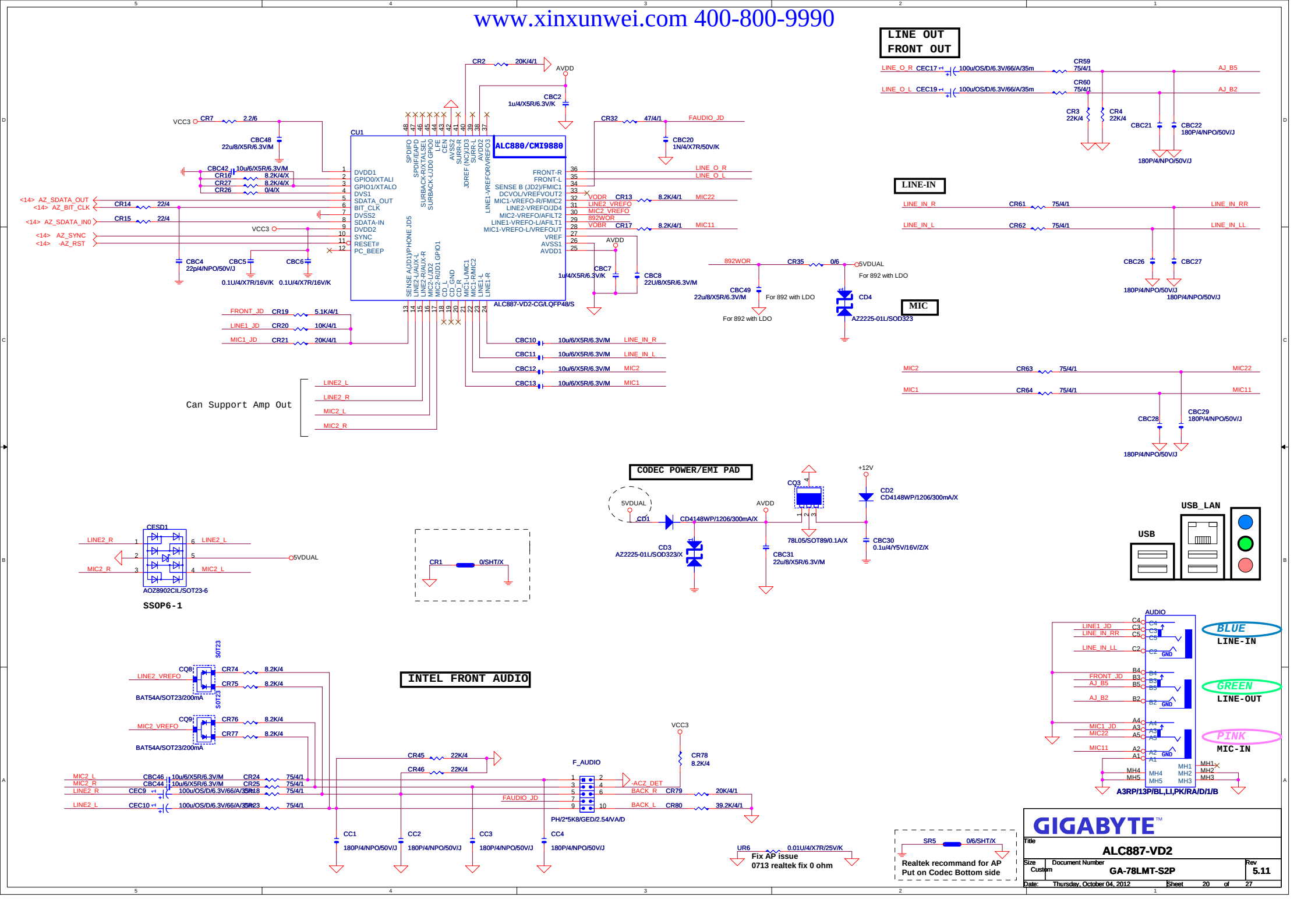
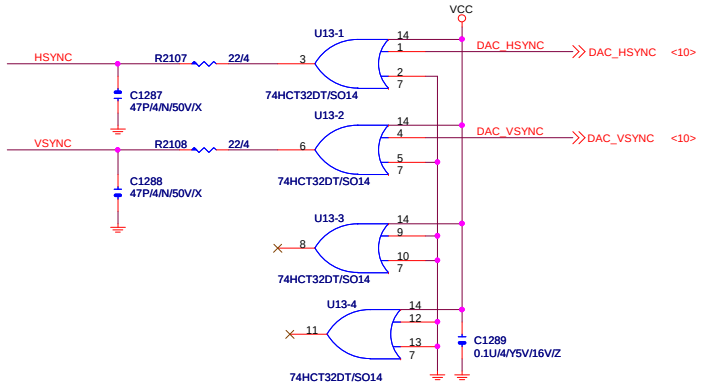
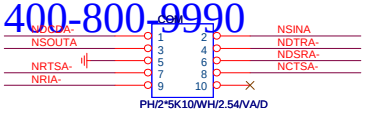
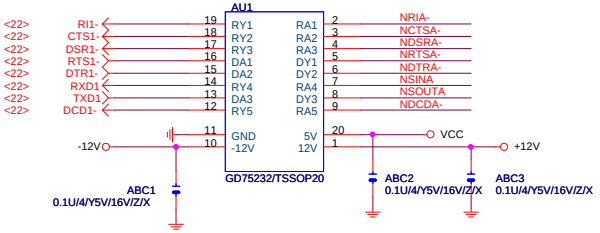
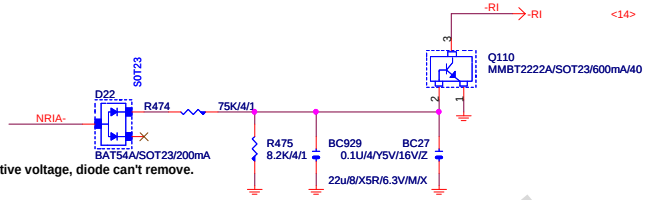
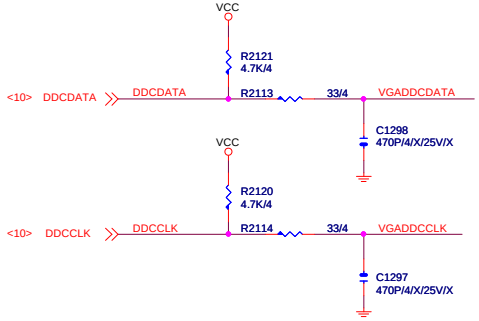


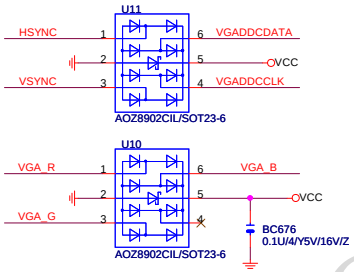


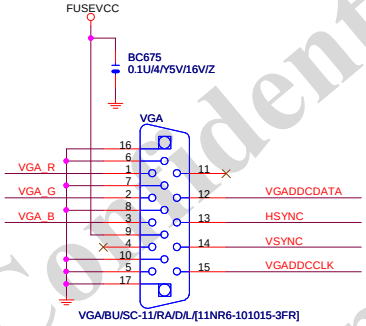


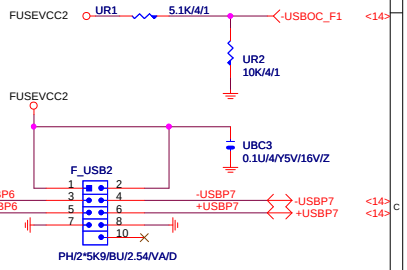


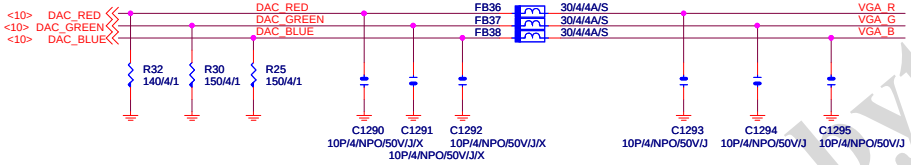


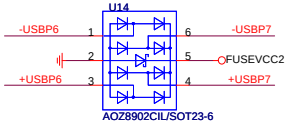


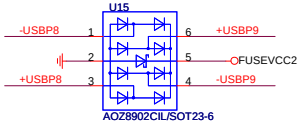


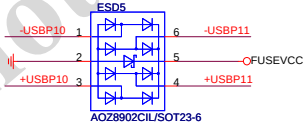


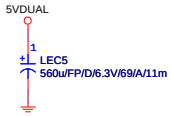


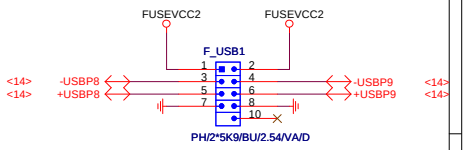




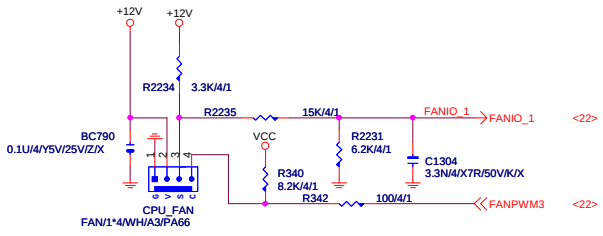




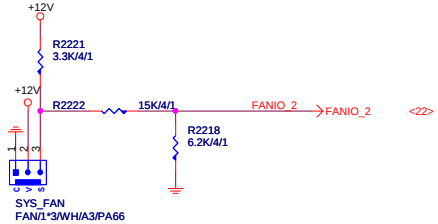


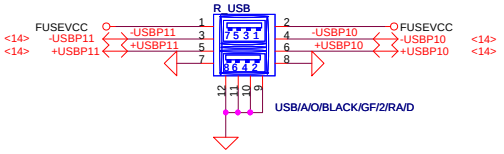


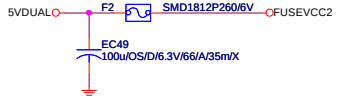
CPU_FAN



SYSTEM_FAN







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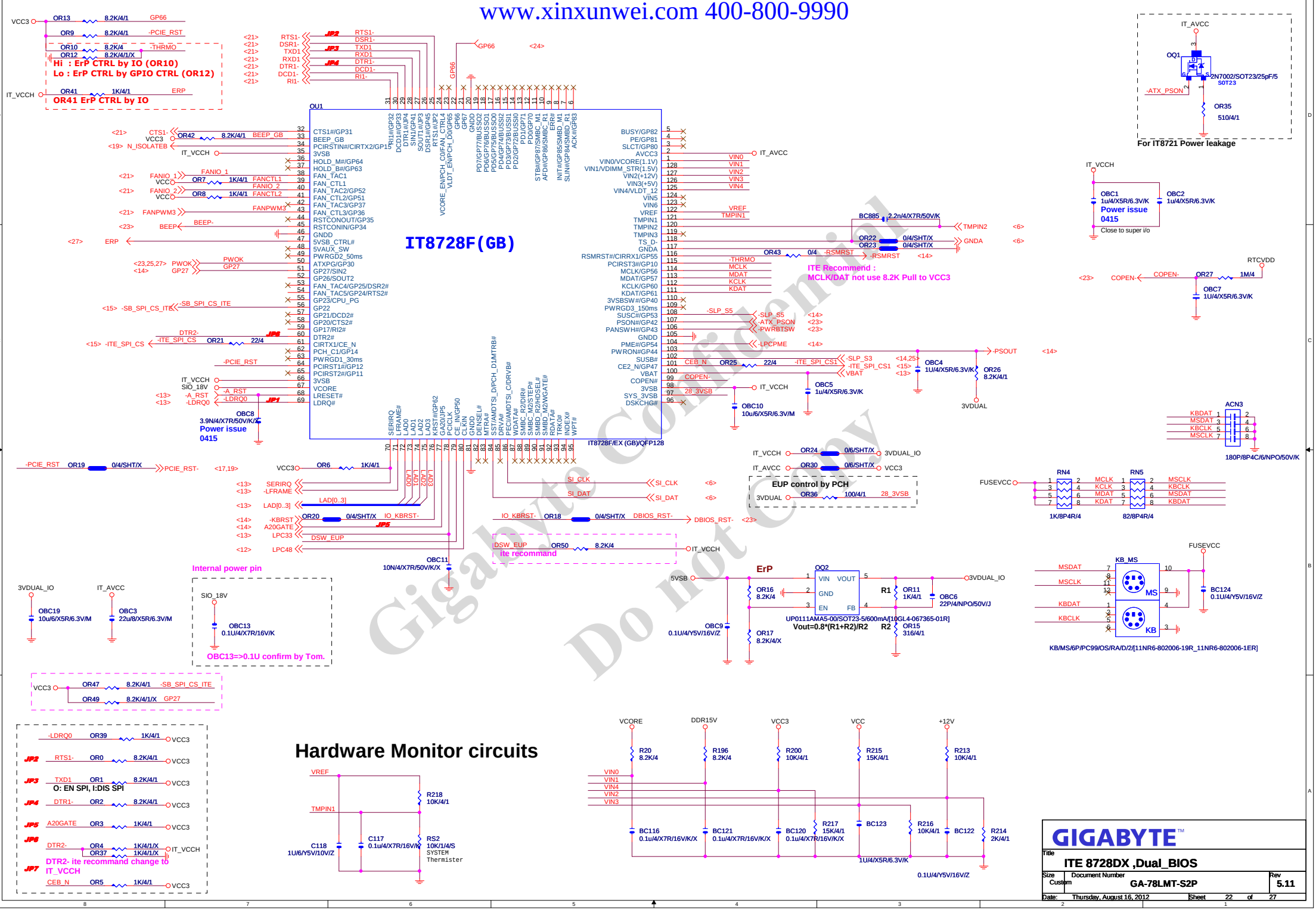

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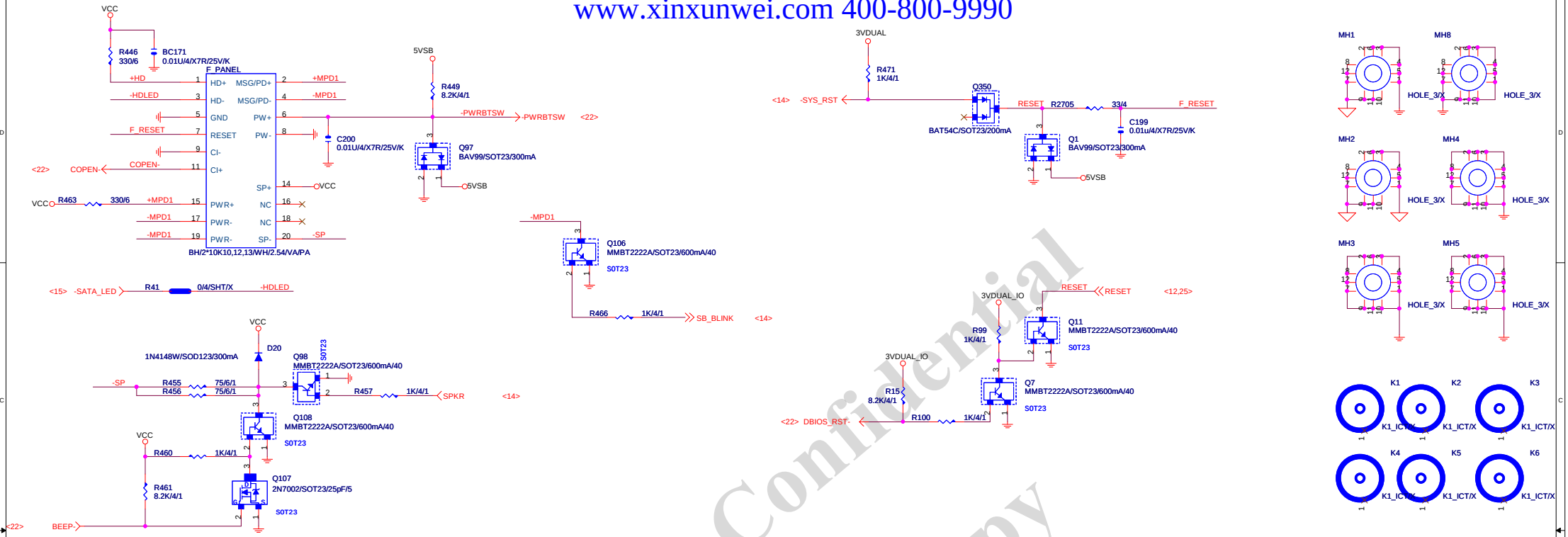
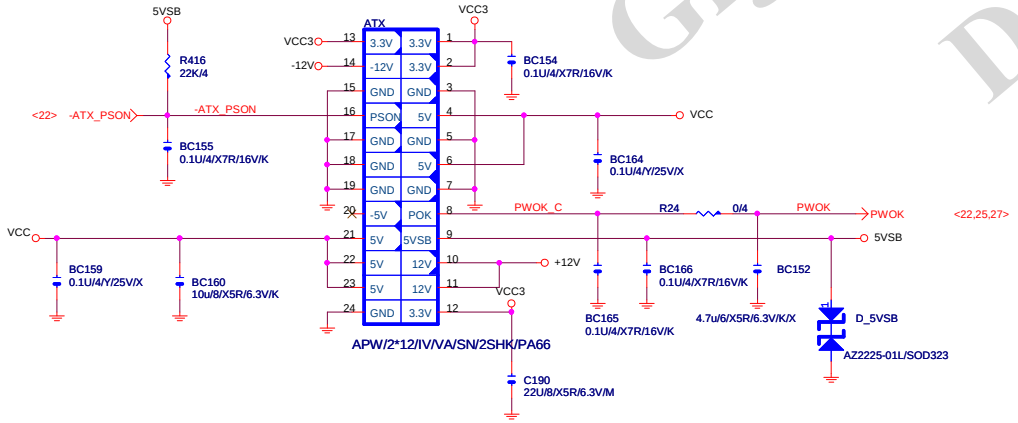
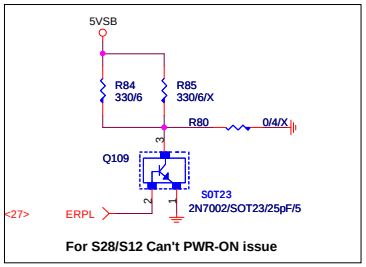
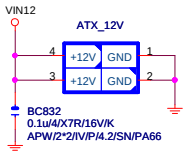


ATX POWER CONNECTOR







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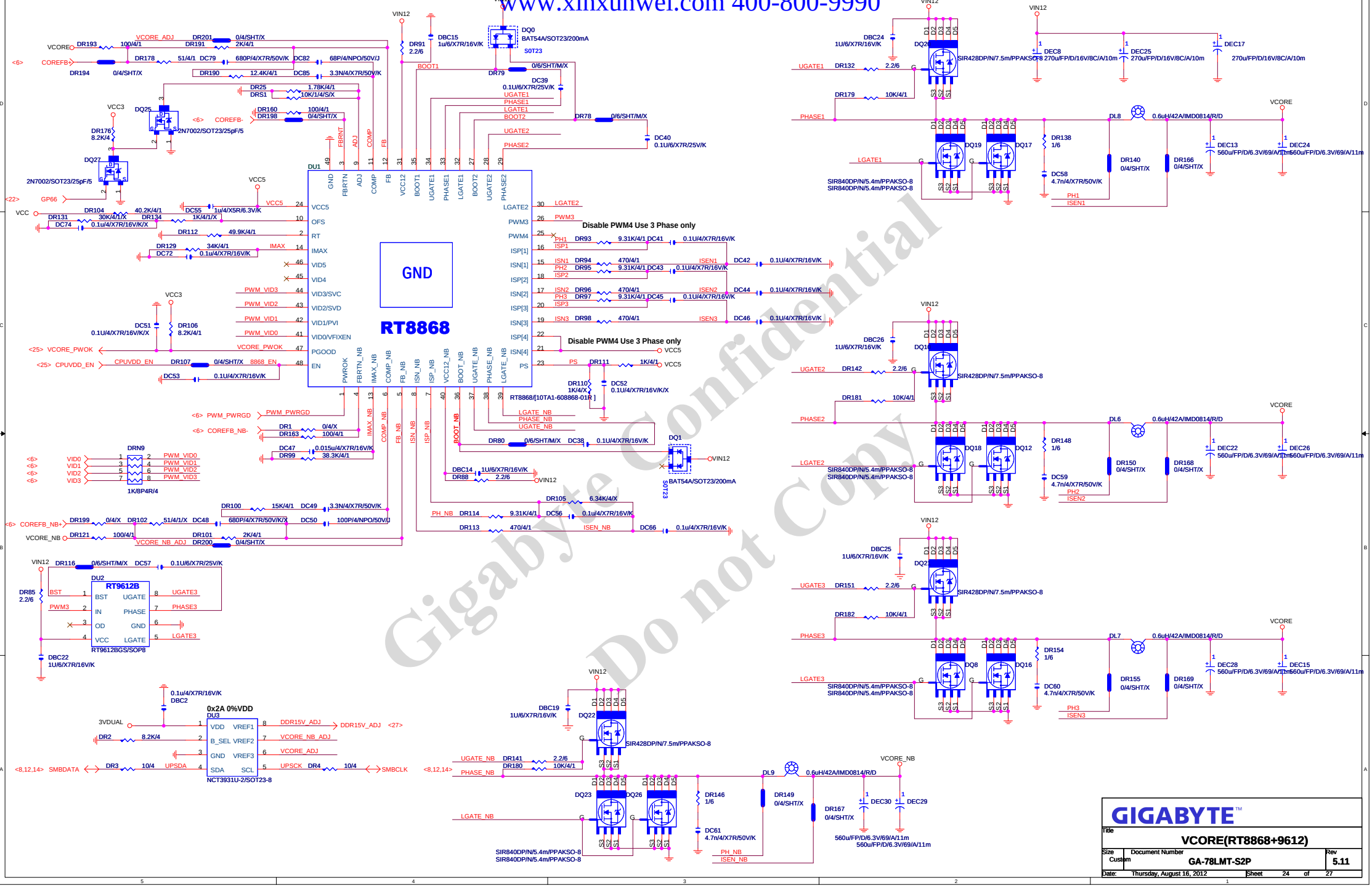

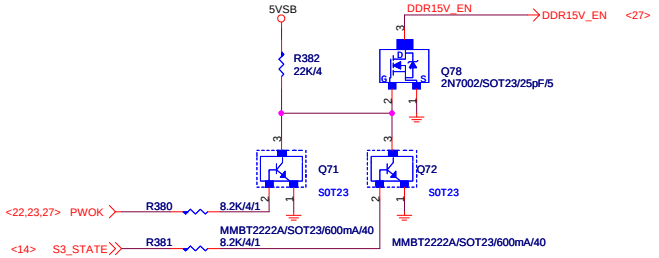

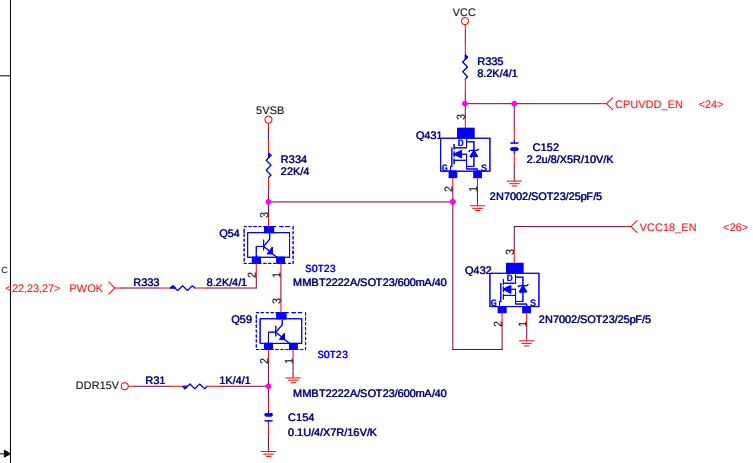

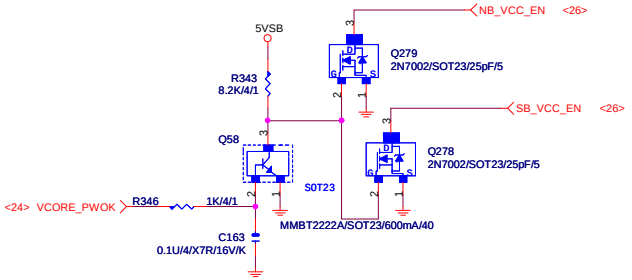

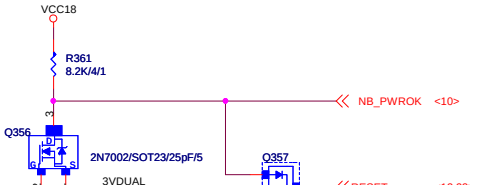

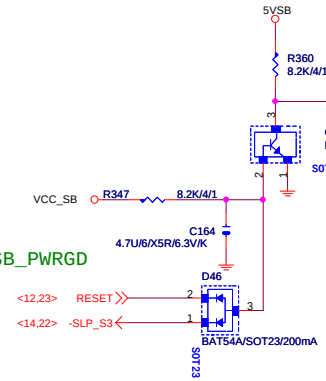

PWOK > NB_PWRGD / SB_PWRGD

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

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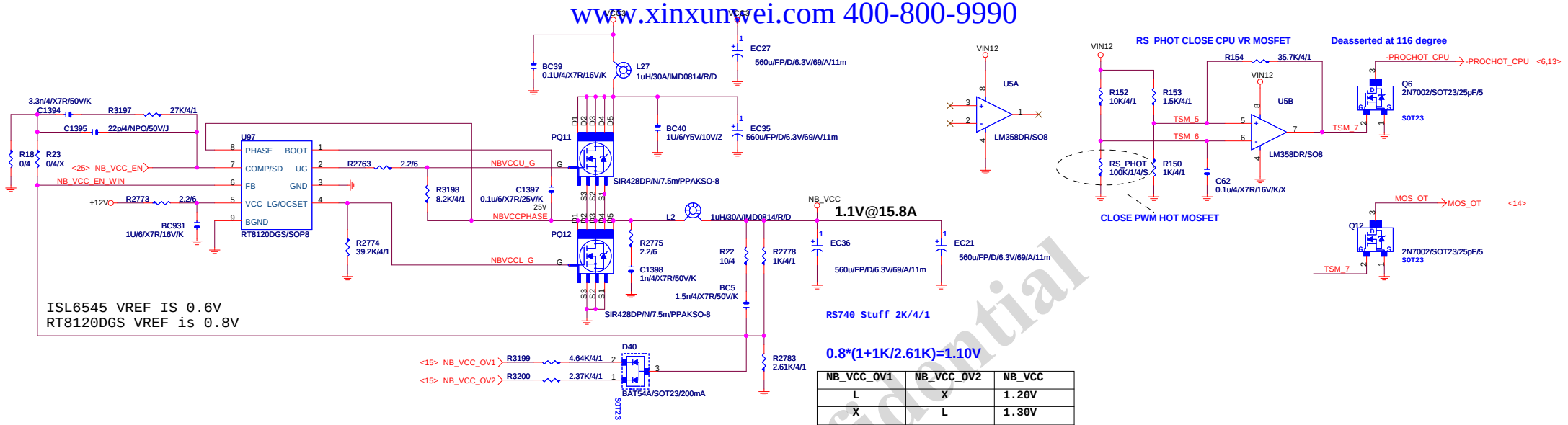
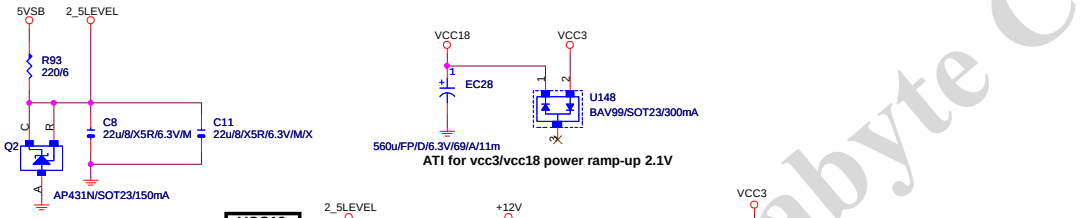
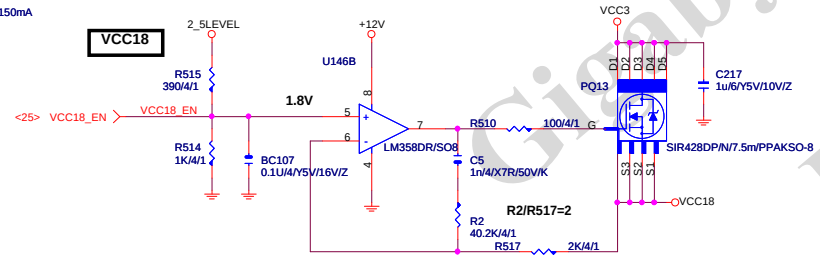
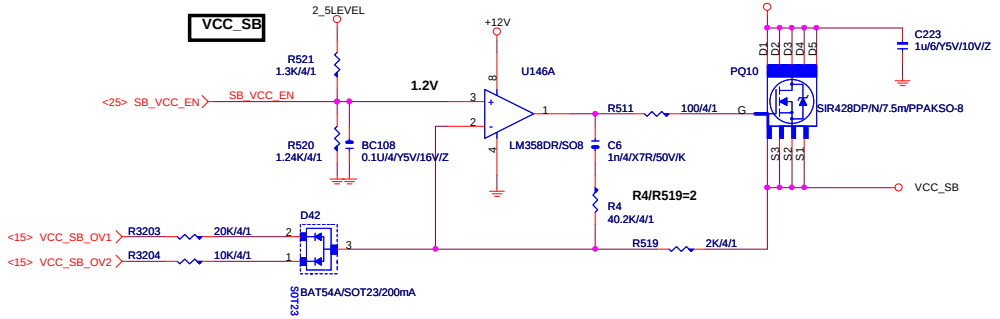
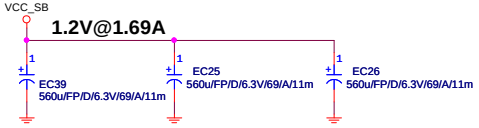


NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V

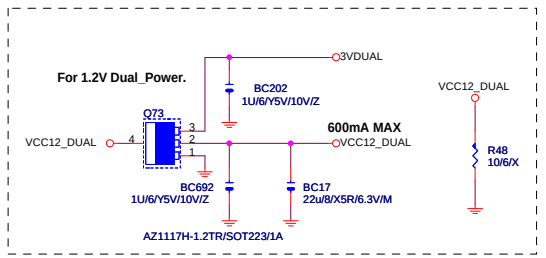








VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V



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