GA-78LMT-S2P

Revision : 3.12

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21	RGB, COM, F_USB
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Title: COVER SHEET

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Model Name:GA-78LMT-S2P

Component value change history

Version: 3.12

P-Code: U99098-0

Date	Change Item	Reason
2011.03.28	3.1D DVT BOM Release. PCB: 3.12	Change From 78LMT-USB3 3.11 Remove USB3.0 / Change EC Cap

Circuit or PCB layout change for next version

Date	Version	Change Item
2010.10.19	0.1 Gerber out	change From 78LMT-USB3 3.11 (RS760=RS780L)

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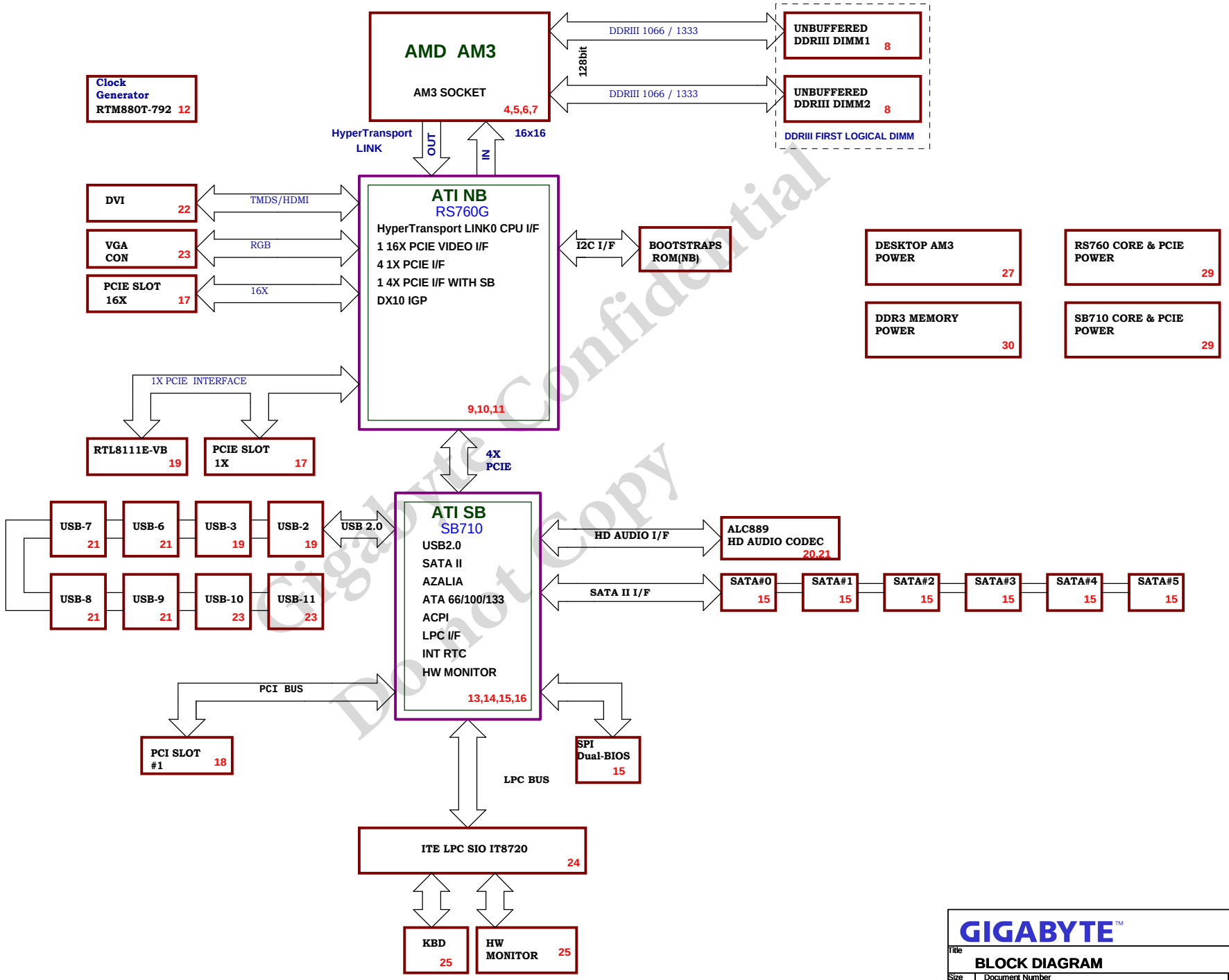
Title: BOM & PCB HISTORY

Size: Custom | Document Number: GA-78LMT-S2P | Rev: 3.12

Date: Monday, March 28, 2011 | Sheet 2 of 28

RS780L CUSTOMER DESKTOP DESIGN



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Title: BLOCK DIAGRAM

Size	Document Number	Rev
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] 9
L0_CADIN_H[0..15] L0_CADIN_H[0..15] 9

L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] 9
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] 9

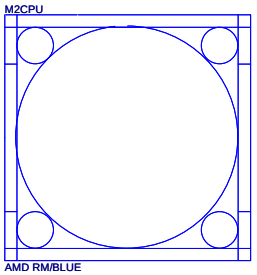
M2CPUA

HYPERTRANSPORT

9	L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 9
9	L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 9
9	L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 9
9	L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 9
9	L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 9
9	L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 9
9	L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 9
9	L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 9
		L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
		L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
		L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
		L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
		L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
		L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
		L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
		L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
		L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11	
		L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE5	L0_CADOUT_L11	
		L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF4	L0_CADOUT_H10	
		L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AH6	L0_CADOUT_L10	
		L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AG6	L0_CADOUT_H9	
		L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AH5	L0_CADOUT_L9	
		L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH4	L0_CADOUT_H8	
		L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)		L0_CADOUT_L8	
		L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
		L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
		L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
		L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
		L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
		L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
		L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
		L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
		L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
		L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
		L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
		L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
		L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
		L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
		L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
		L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/15u/[10SC1-A01942-01R_10SC1-A01942-02R]

M2CPU



AMD RM/BLUE

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

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Title	CPU HYPER TRANSPORT	
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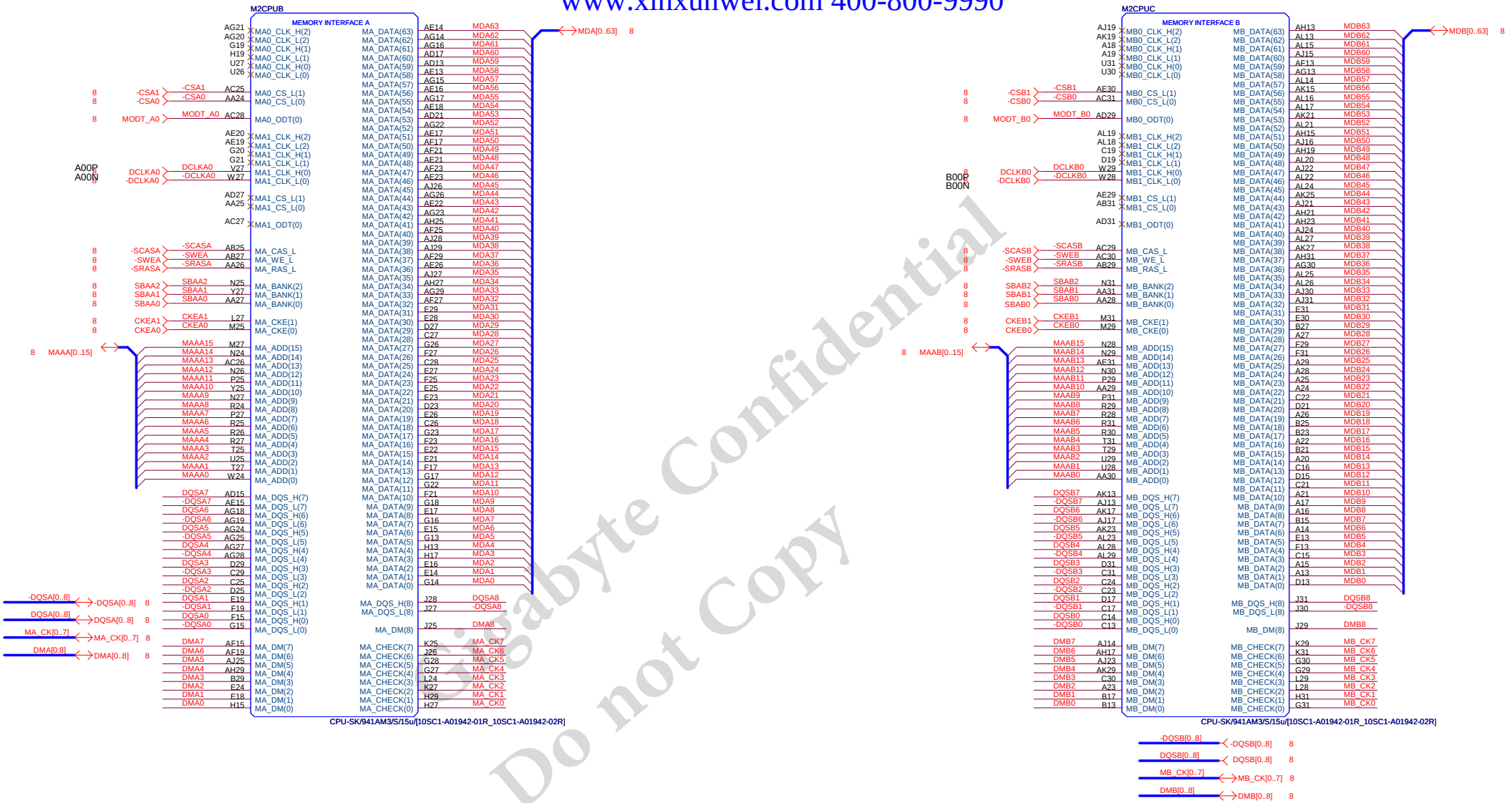
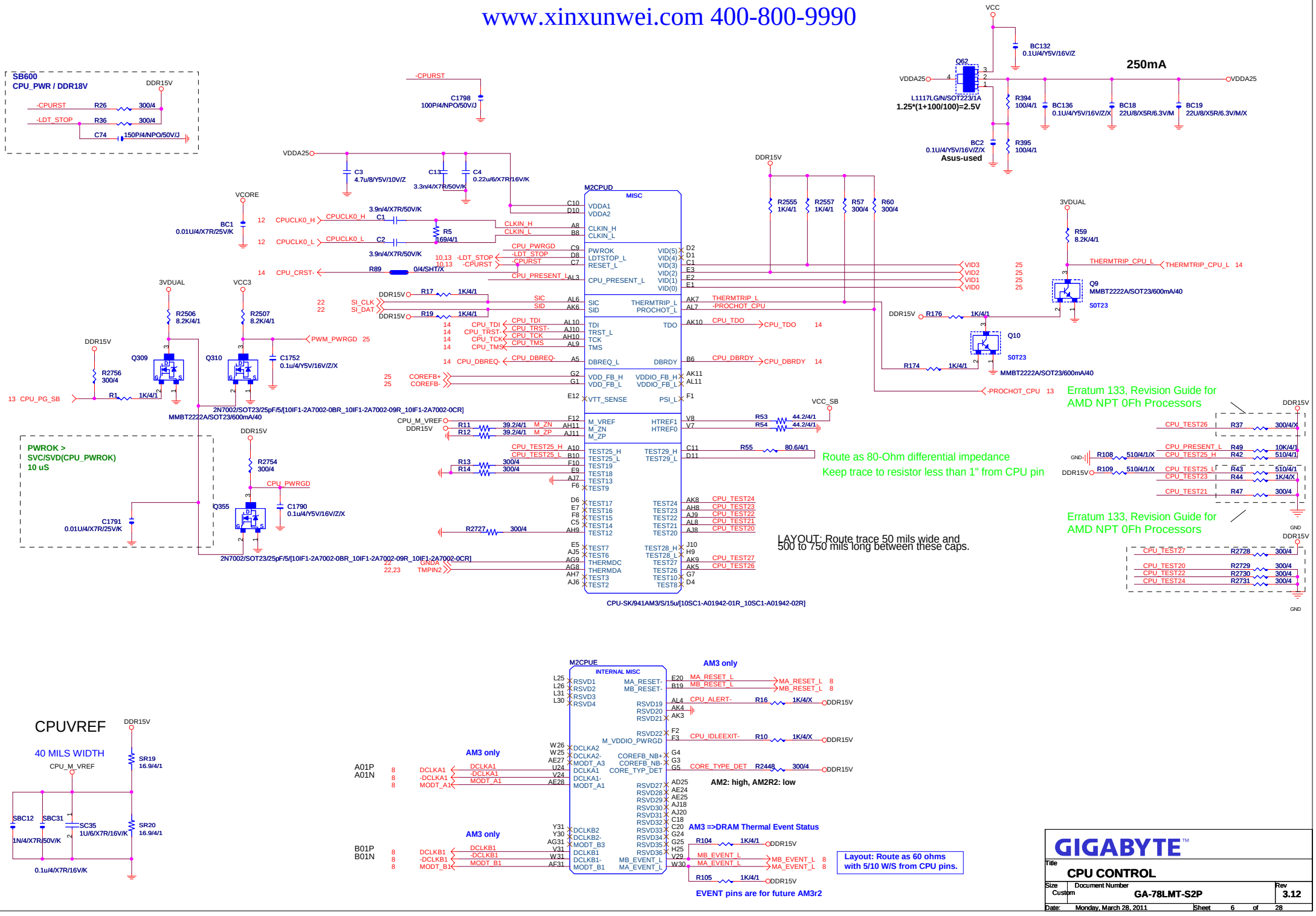
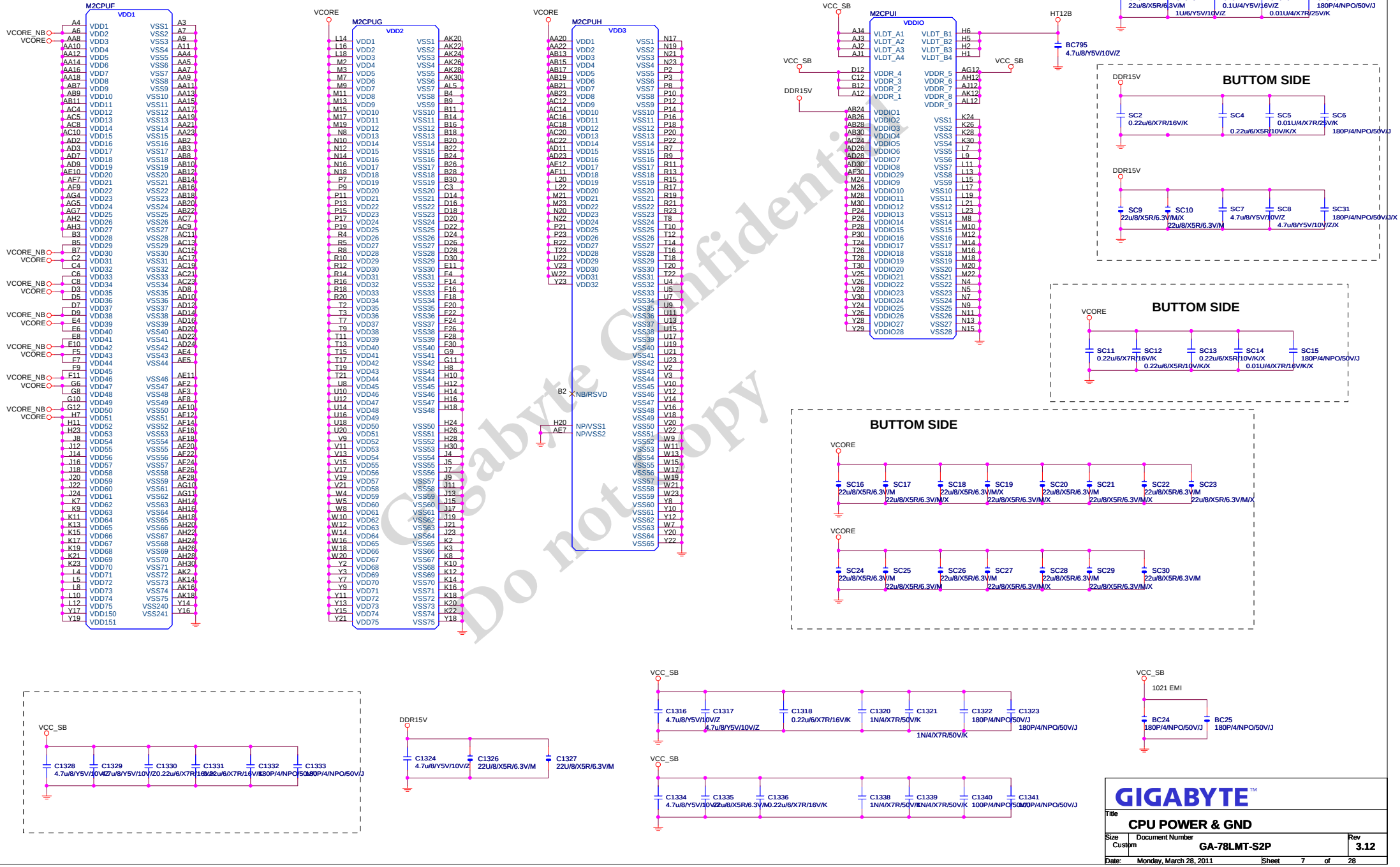


GIGABYTE™			
Title: CPU DDRII MEMORY			
Size: Custom	Document Number: GA-78LMT-S2P		Rev: 3.12
Date: Monday, March 28, 2011	Sheet 5 of 28		



VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



GIGABYTE™			
Title: CPU POWER & GND			
Size: Custom	Document Number: GA-78LMT-S2P		Rev: 3.12
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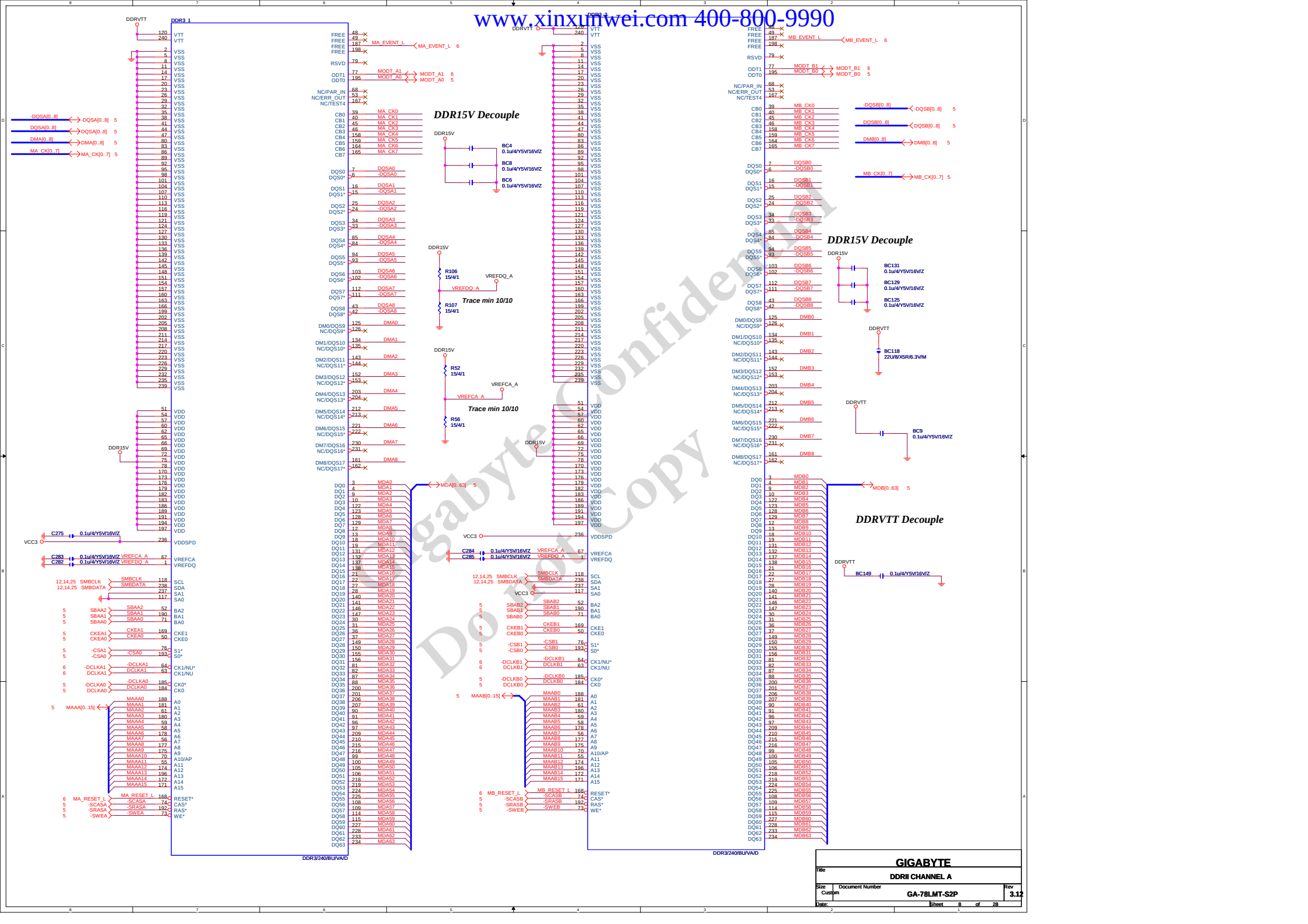

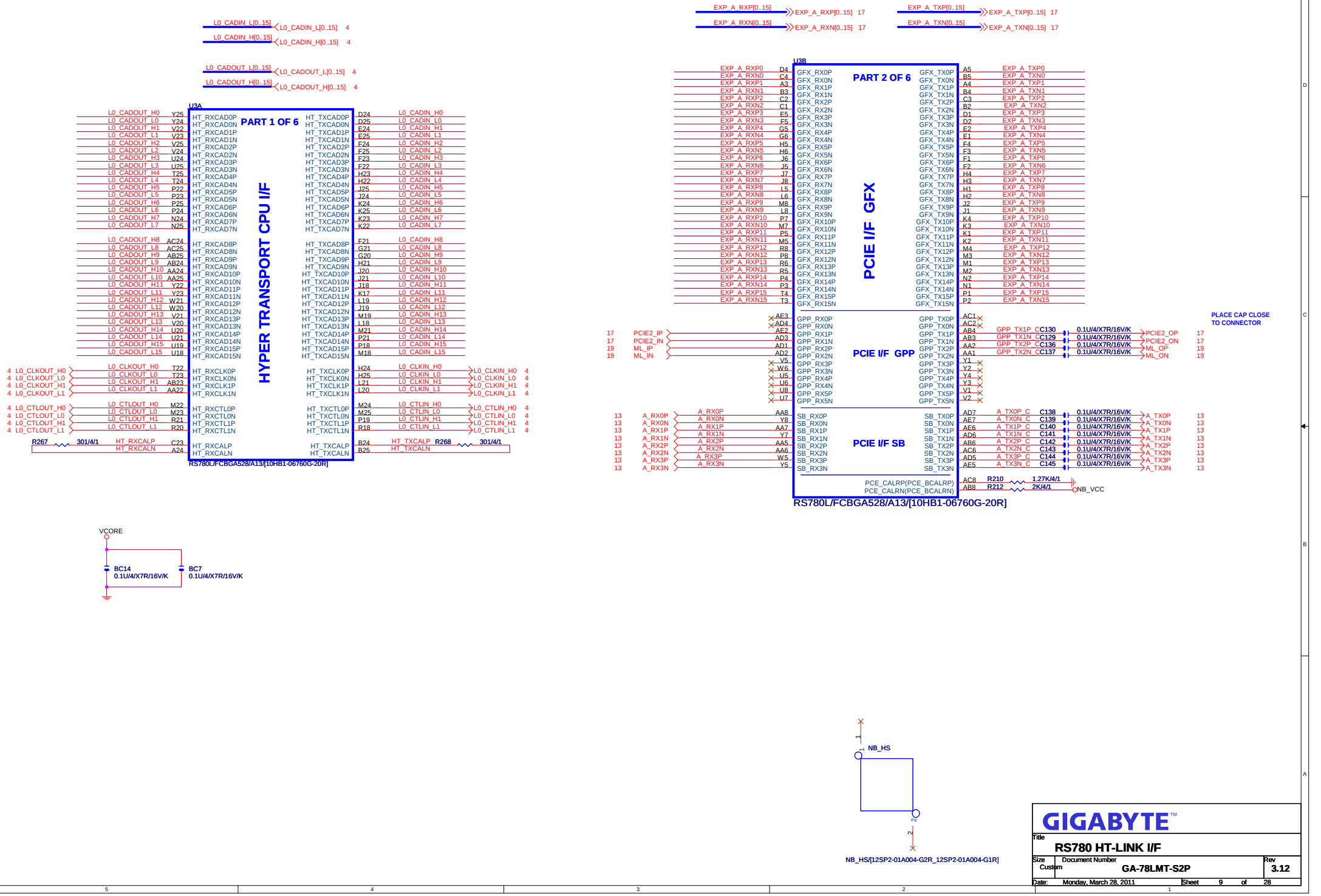

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Title	RS780 HT-LINK I/F
Size: Custom	Document Number: GA-78LMT-S2P
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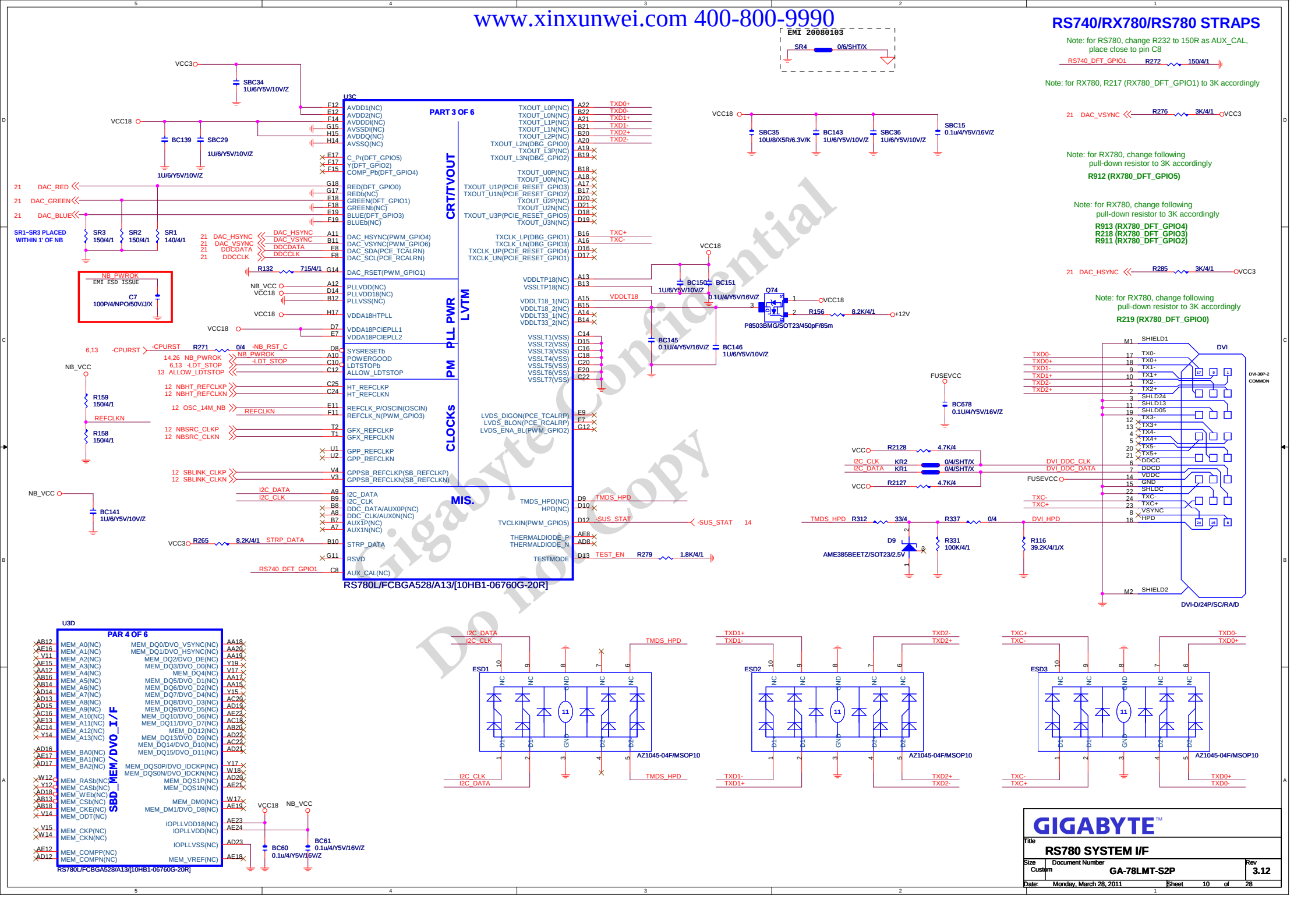

Title	RS780 SYSTEM I/F
Size	Custom
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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

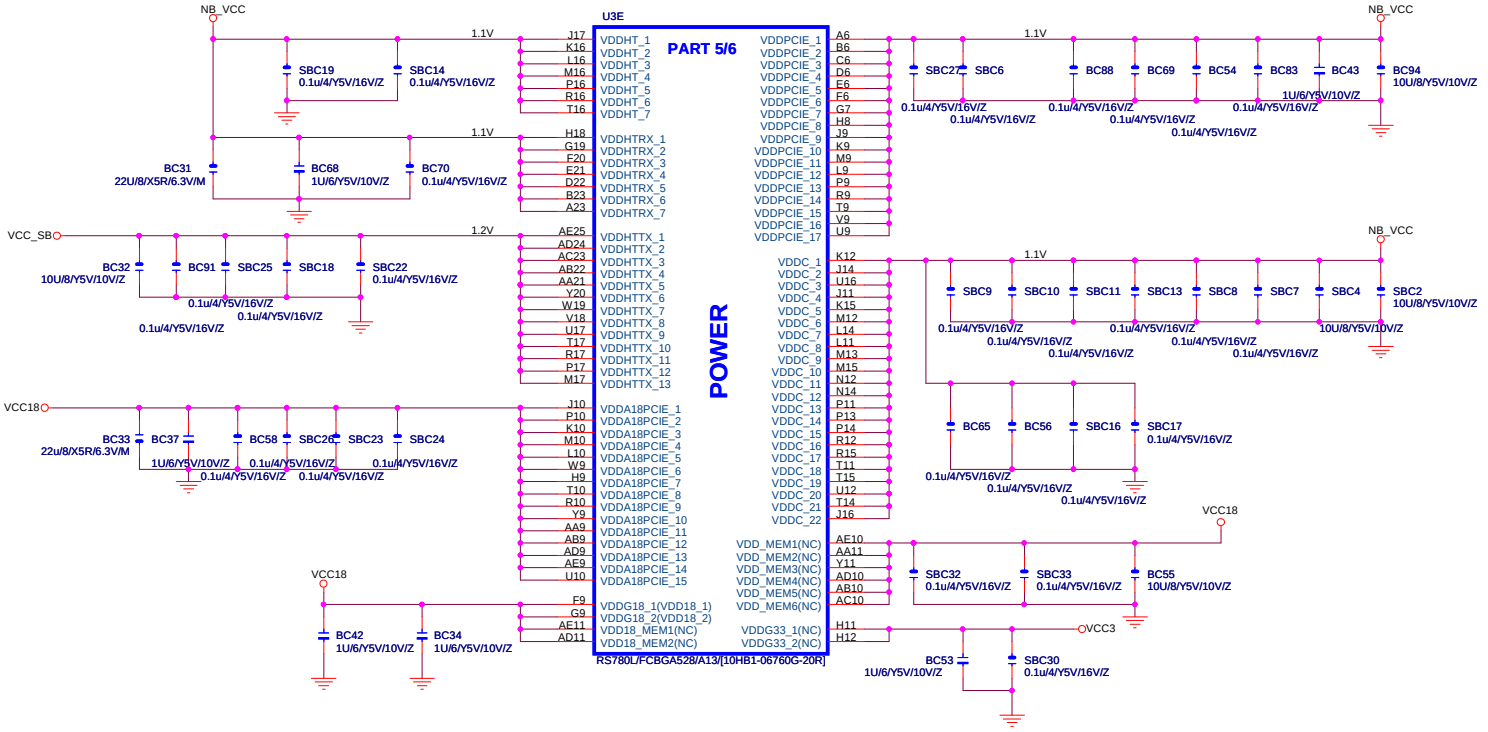
U3F — PART 6/6 — GROUND

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

Please use 1mm pad size, place all ELT test pads on bottom side only

U3E — PART 5/6 — POWER

RS780L/FCBGA528/A13/[10HB1-06760G-20R]



Title: **RS780 POWER & GND**

Size: Custom | Document Number: **GA-78LMT-S2P** | Rev: **3.12**

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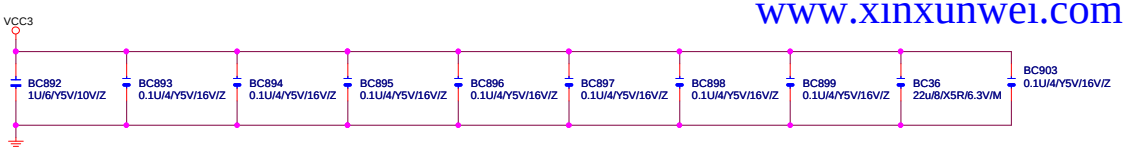


1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

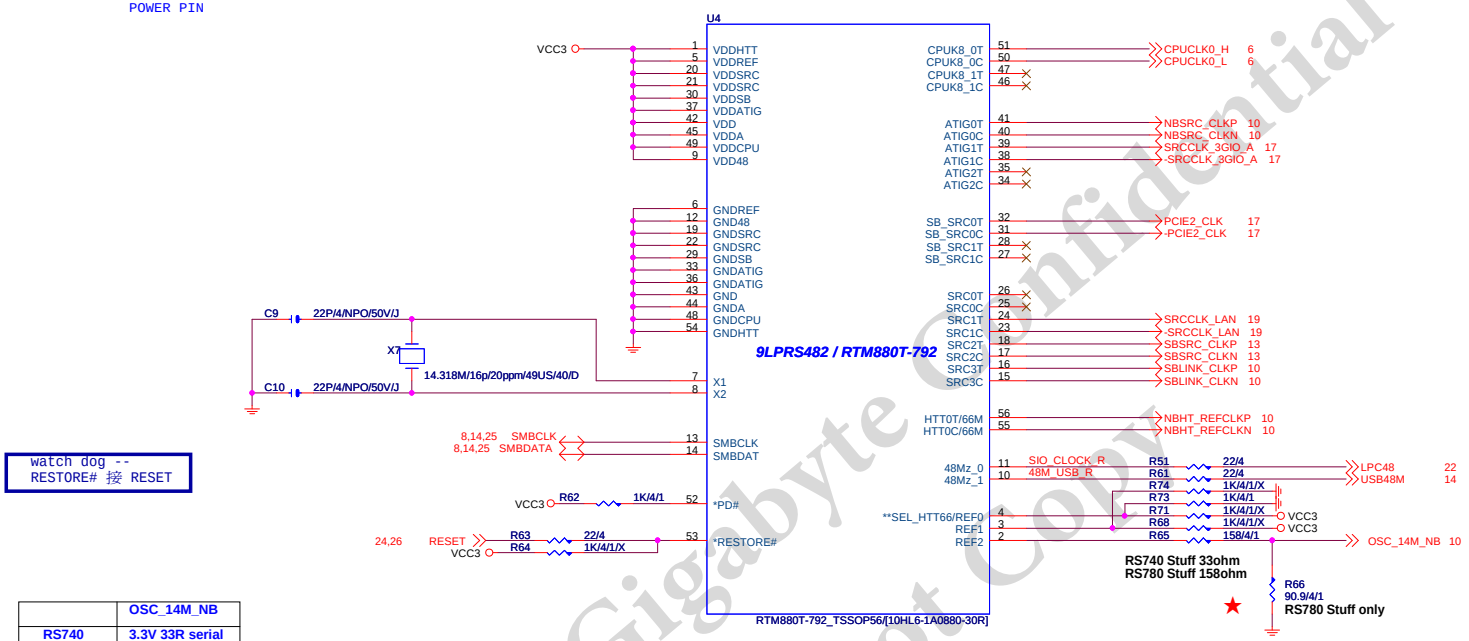
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



watch dog --
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

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Title	ICS9LPRS477	
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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK

SB_HS

SB_HS/[12SP2-030005-42R_12SP2-030005-43R]

U2A

SB700

Part 1 of 5

PCI CLKS

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC XTAL

CPU

RTC

A_RST# PCIE_TX0P PCIE_TX0N PCIE_TX1P PCIE_TX1N PCIE_TX2P PCIE_TX2N PCIE_TX3P PCIE_TX3N

PCIE_RX0P PCIE_RX0N PCIE_RX1P PCIE_RX1N PCIE_RX2P PCIE_RX2N PCIE_RX3P PCIE_RX3N

PCIE_CALRP PCIE_CALRN

PCIE_PVDD PCIE_PVSS

PCIE_RCLKP/NB_LNK_CLKP PCIE_RCLKN/NB_LNK_CLKN

NB_DISP_CLKP NB_DISP_CLKN

NB_HT_CLKP NB_HT_CLKN

CPU_HT_CLKP CPU_HT_CLKN

SLT_GFX_CLKP SLT_GFX_CLKN

GPP_CLK0P GPP_CLK0N

GPP_CLK1P GPP_CLK1N

GPP_CLK2P GPP_CLK2N

GPP_CLK3P GPP_CLK3N

25M_48M_66M_OSC

25M_X1

25M_X2

PCICLK0 PCICLK1 PCICLK2 PCICLK3 PCICLK4 PCICLK5/GPIO41

PCIRST#

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

CBE0# CBE1# CBE2# CBE3# FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR#

REQ0# REQ1# REQ2# REQ3#/GPIO70 REQ4#/GPIO71 GNT0# GNT1# GNT2# GNT3#/GPIO72 GNT4#/GPIO73 CLKRUN# LOCK#

INTE#/GPIO33 INTF#/GPIO34 INTG#/GPIO35 INTH#/GPIO36

LPCCLK0 LPCCLK1 LAD0 LAD1 LAD2 LAD3 LFRAME# LDRQ0# LDRQ1#/GNT5#/GPIO68 BMREQ#/REQ5#/GPIO65 SERIRQ

RTCCLK INTRUDER_ALERT# VBAT

ALLOW_LDTSTOP PROCHOT# LDT_PG LDT_STP# LDT_RST#

SB710/FCBGA528/A14/[10HB1-06B710-11R]

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

BIOS after boot setting EC AOD-ACC

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

GIGABYTE

Title: ATI SB710 PCIE/PCI/CPU/LPC

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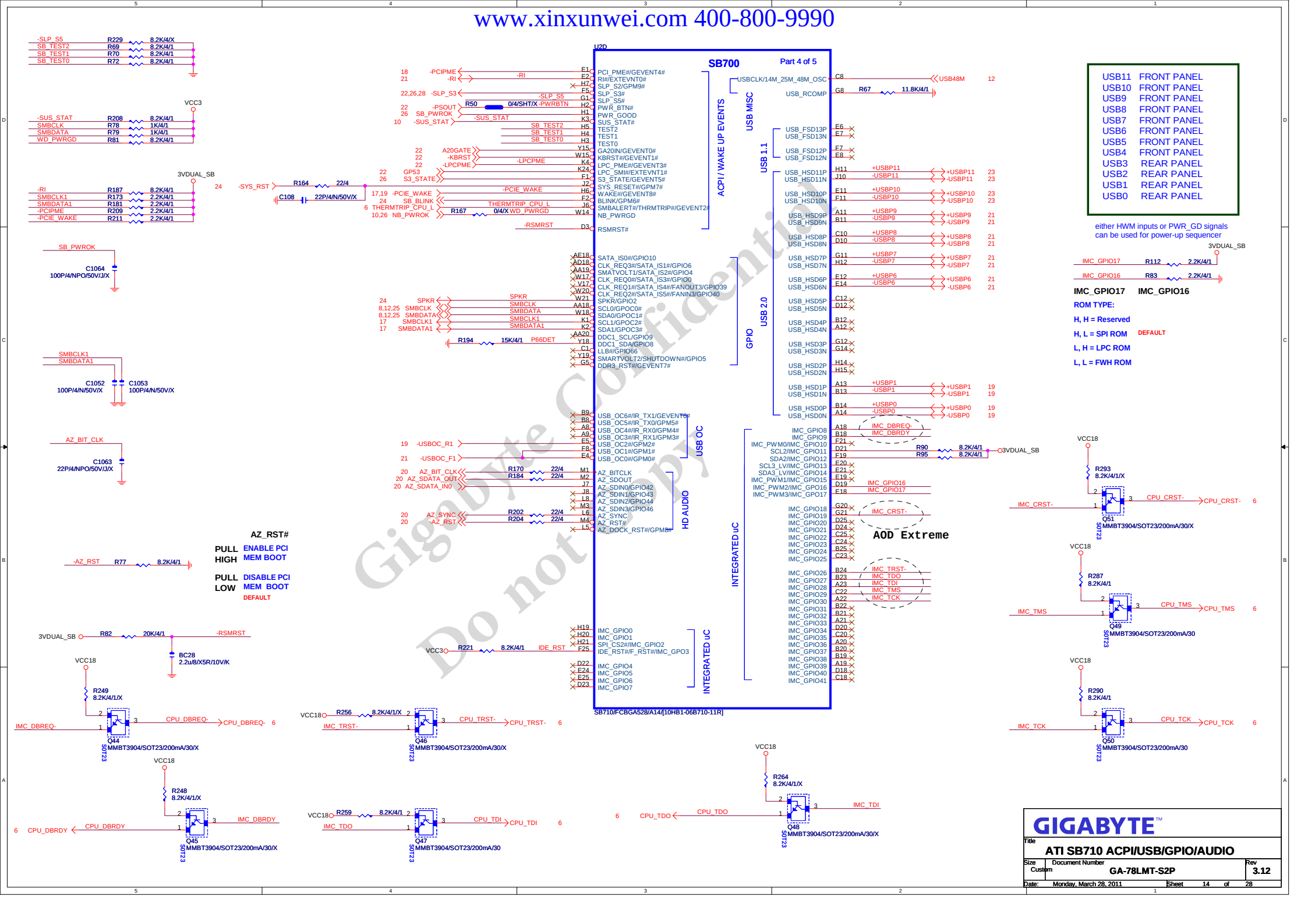

USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR_GD signals can be used for power-up sequencer

IMC_GPIO17 IMC_GPIO16

ROM TYPE:

H, H = Reserved

H, L = SPI ROM DEFAULT

L, H = LPC ROM

L, L = FWH ROM

AZ_RST#

PULL HIGH ENABLE PCI MEM BOOT

PULL LOW DISABLE PCI MEM BOOT DEFAULT

Title	ATI SB710 ACPI/USB/GPIO/AUDIO
Size	Custom
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PLACE SATA AC COUPLING CAPS CLOSE TO SB600

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

U2B

SB700
Part 2 of 5

SERIAL ATA
SATA_TX0P / SATA_TX0N
SATA_RX0N / SATA_RX0P
SATA_TX1P / SATA_TX1N
SATA_RX1N / SATA_RX1P
SATA_TX2P / SATA_TX2N
SATA_RX2N / SATA_RX2P
SATA_TX3P / SATA_TX3N
SATA_RX3N / SATA_RX3P
SATA_TX4P / SATA_TX4N
SATA_RX4N / SATA_RX4P
SATA_TX5P / SATA_TX5N
SATA_RX5N / SATA_RX5P
SATA_CAL
SATA_X1
SATA_X2
SATA_ACT#/GPIO67

SATA PWR
PLLVDD_SATA
XTLVDD_SATA

ATA 66/100/133
IDE_IORDY AA24 PIORDY
IDE_IRQ AA25 IRQ14
IDE_A0 Y22
IDE_A1 AB23
IDE_A2 Y23
IDE_DACK# AB24
IDE_DRQ AD25 PDDREQ
IDE_IOR# AC25
IDE_IOW# AC24
IDE_CS1# Y25
IDE_CS3# Y24
IDE_D0/GPIO15 AD24
IDE_D1/GPIO16 AD23
IDE_D2/GPIO17 AE22
IDE_D3/GPIO18 AC22
IDE_D4/GPIO19 AD21
IDE_D5/GPIO20 AE20
IDE_D6/GPIO21 AB20
IDE_D7/GPIO22 AD19 PDD7
IDE_D8/GPIO23 AE19
IDE_D9/GPIO24 AC20
IDE_D10/GPIO25 AD20
IDE_D11/GPIO26 AE21
IDE_D12/GPIO27 AB22
IDE_D13/GPIO28 AD22
IDE_D14/GPIO29 AE23
IDE_D15/GPIO30 AC23

SPI ROM
SPI_DI/GPIO12 G6 SB_SPI_DI_R R101 22/4 SB_SPI_DI
SPI_DO/GPIO11 D2 SB_SPI_DO_R R102 22/4 SB_SPI_DO
SPI_CLK/GPIO47 D1 SB_SPI_CLK_R R92 22/4 SB_SPI_CLK
SPI_HOLD#/GPIO31 E4
SPI_CS1#/GPIO32 F3 SB_SPI_CS R103 22/4 -SB_SPI_CS_ITE -SB_SPI_CS_ITE 22
LAN_RST#/GPIO13 U15
ROM_RST#/GPIO14 J1

HW MONITOR
FANOUT0/GPIO3 M8
FANOUT1/GPIO48 M5
FANOUT2/GPIO49 M7
FANIN0/GPIO50 P5
FANIN1/GPIO51 P8
FANIN2/GPIO52 R8
TEMP_COMM C6
TEMPIN0/GPIO61 B6
TEMPIN1/GPIO62 A6 VCC_SB_OV2 27
TEMPIN2/GPIO63 A5 VCC_SB_OV1 27
TEMPIN3/TALERT#/GPIO64 B5
VIN0/GPIO53 A4
VIN1/GPIO54 B4
VIN2/GPIO55 C4 NB_VCC_OV2 27
VIN3/GPIO56 D4 NB_VCC_OV1 27
VIN4/GPIO57 D5
VIN5/GPIO58 D6
VIN6/GPIO59 A7 DDR18V_OV2 28
VIN7/GPIO60 B7
AVDD F6 3VDUAL_SB
AVSS G7

SB710/FCBGA528/A14/[10HB1-06B710-11R]

R2194 1K/4/1 SATA_CAL
24 -SATA_LED

VCC_SB AA11
VCC3 W12

R168 10M/4
X6 25M/20p/30ppm/49US/20/D
C115 10P/4/NPO/50V/J
C119 10P/4/NPO/50V/J

BC112 1U/6/Y5V/10V/Z
SBC1 0.1u/4/Y5V/16V/Z
SBC3 0.1u/4/Y5V/16V/Z
BC119 0.1u/4/Y5V/16V/Z
BC117 1U/6/Y5V/10V/Z

VCC3
R183 4.7K/4/X PIORDY SB710 DG
R185 8.2K/4/X IRQ14 SB710 DG
R189 8.2K/4/1 PDD7 SB710 DG
R191 5.6K/4/X PDDREQ SB710 DG

M_BIOS
22 -ITE_SPI_CS
SB_SPI_DI
-BIOS_WP
CS# SO WP# VSS VDD HOLD# SCK SI
BC203 0.1U/4/Y5V/16V/Z
-SPI_HOLD0
SB_SPI_CLK
SB_SPI_DO
16M/SPI/SO8/200mil/S

B_BIOS
22 -ITE_SPI_CS1
SB_SPI_DI
-BIOS_WP
CS# SO WP# VSS VDD HOLD# SCK SI
-SPI_HOLD0
SB_SPI_CLK
SB_SPI_DO
16M/SPI/SO8/200mil/S

-SPI_HOLD0 R29 1K/4/1
SB_SPI_DO R34 1K/4/X
-BIOS_WP R38 1K/4/1
SB_SPI_DI R39 1K/4/X
-ITE_SPI_CS R28 220/4
-ITE_SPI_CS1 R33 220/4

SATA2_0 SATA2/7/BU/H/OP/VA/D/1/B
SATA2_1 SATA2/7/BU/H/OP/VA/D/1/B
SATA2_2 SATA2/7/BU/H/OP/VA/D/1/B
SATA2_3 SATA2/7/BU/H/OP/VA/D/1/B
SATA2_4 SATA2/7/BU/H/OP/VA/D/1/B
SATA2_5 SATA2/7/BU/H/OP/VA/D/1/B

SP_TX0P_C C1310 0.01U/4/X7R/25V/K
SP_TX0M_C C1309 0.01U/4/X7R/25V/K
SP_RX0M_C C1308 0.01U/4/X7R/25V/K
SP_RX0P_C C1302 0.01U/4/X7R/25V/K
SP_TX2P_C C1279 0.01U/4/X7R/25V/K
SP_TX2M_C C1278 0.01U/4/X7R/25V/K
SP_RX2M_C C1282 0.01U/4/X7R/25V/K
SP_RX2P_C C1283 0.01U/4/X7R/25V/K
SP_TX4P_C C1313 0.01U/4/X7R/25V/K
SP_TX4M_C C1314 0.01U/4/X7R/25V/K
SP_RX4M_C C1315 0.01U/4/X7R/25V/K
SP_RX4P_C C1303 0.01U/4/X7R/25V/K

SP_RX1P_C C1307 0.01U/4/X7R/25V/K
SP_RX1M_C C1311 0.01U/4/X7R/25V/K
SP_TX1M_C C1300 0.01U/4/X7R/25V/K
SP_TX1P_C C1286 0.01U/4/X7R/25V/K
SP_RX3P_C C1284 0.01U/4/X7R/25V/K
SP_RX3M_C C1285 0.01U/4/X7R/25V/K
SP_TX3M_C C1281 0.01U/4/X7R/25V/K
SP_TX3P_C C1280 0.01U/4/X7R/25V/K
SP_RX5P_C C1319 0.01U/4/X7R/25V/K
SP_RX5M_C C1312 0.01U/4/X7R/25V/K
SP_TX5M_C C1301 0.01U/4/X7R/25V/K
SP_TX5P_C C1296 0.01U/4/X7R/25V/K

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Title: ATI SB710 SATA/IDE/HWM/SPI

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Date: Monday, March 28, 2011 | Sheet 15 of 28

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

U2C

SB700

Part 3 of 5

POWER

1.8V: Flash module mode
3.3V: IDE mode

SB710/FCBGA528/A14/[10HB1-06B710-11R]

U2E

SB700

GROUND

Part 5 of 5

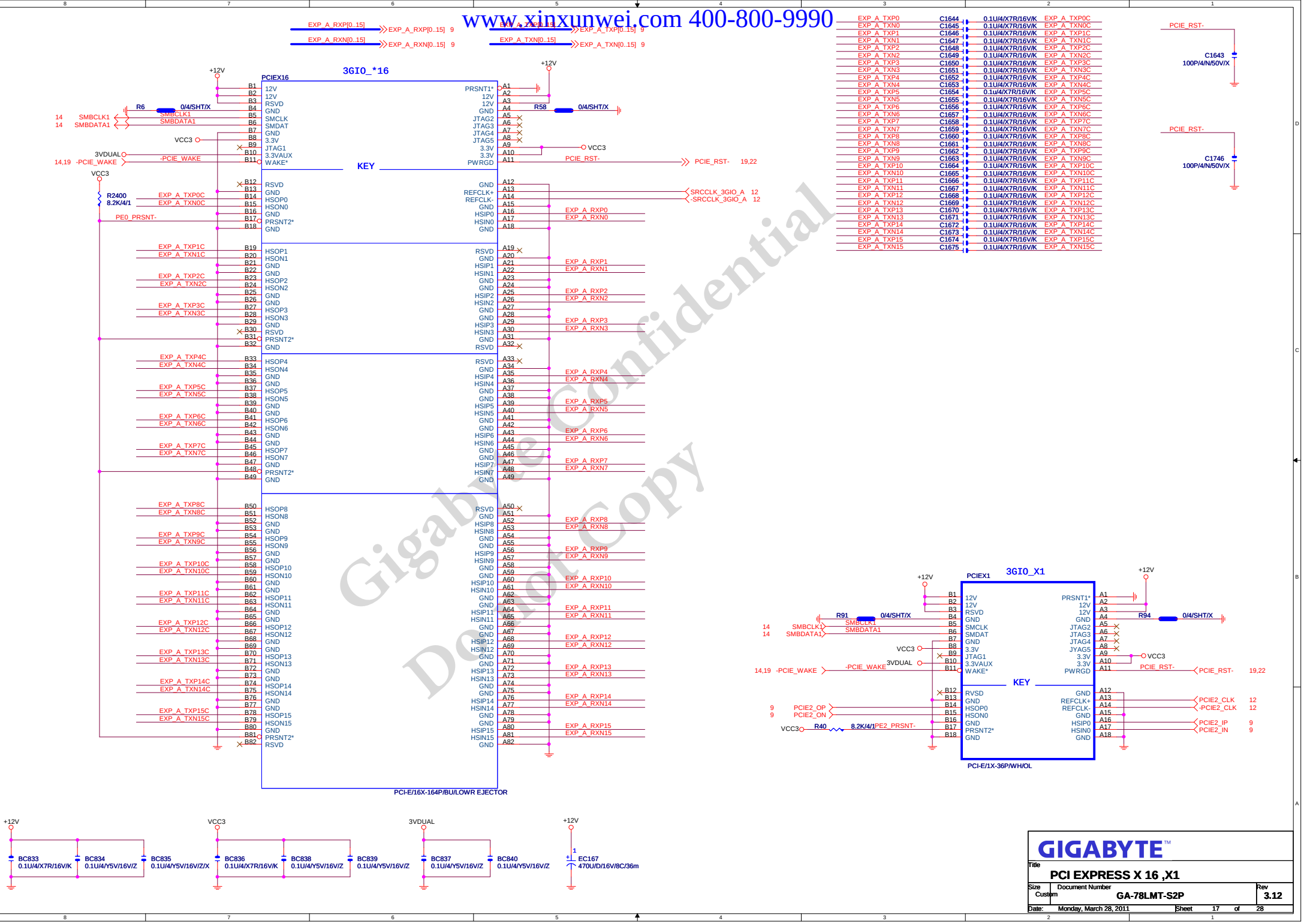
SB710/FCBGA528/A14/[10HB1-06B710-11R]

GIGABYTE™

Title: ATI SB700 POWER & GND

Size: Custom | Document Number: GA-78LMT-S2P | Rev: 3.12

Date: Monday, March 28, 2011 | Sheet 16 of 28



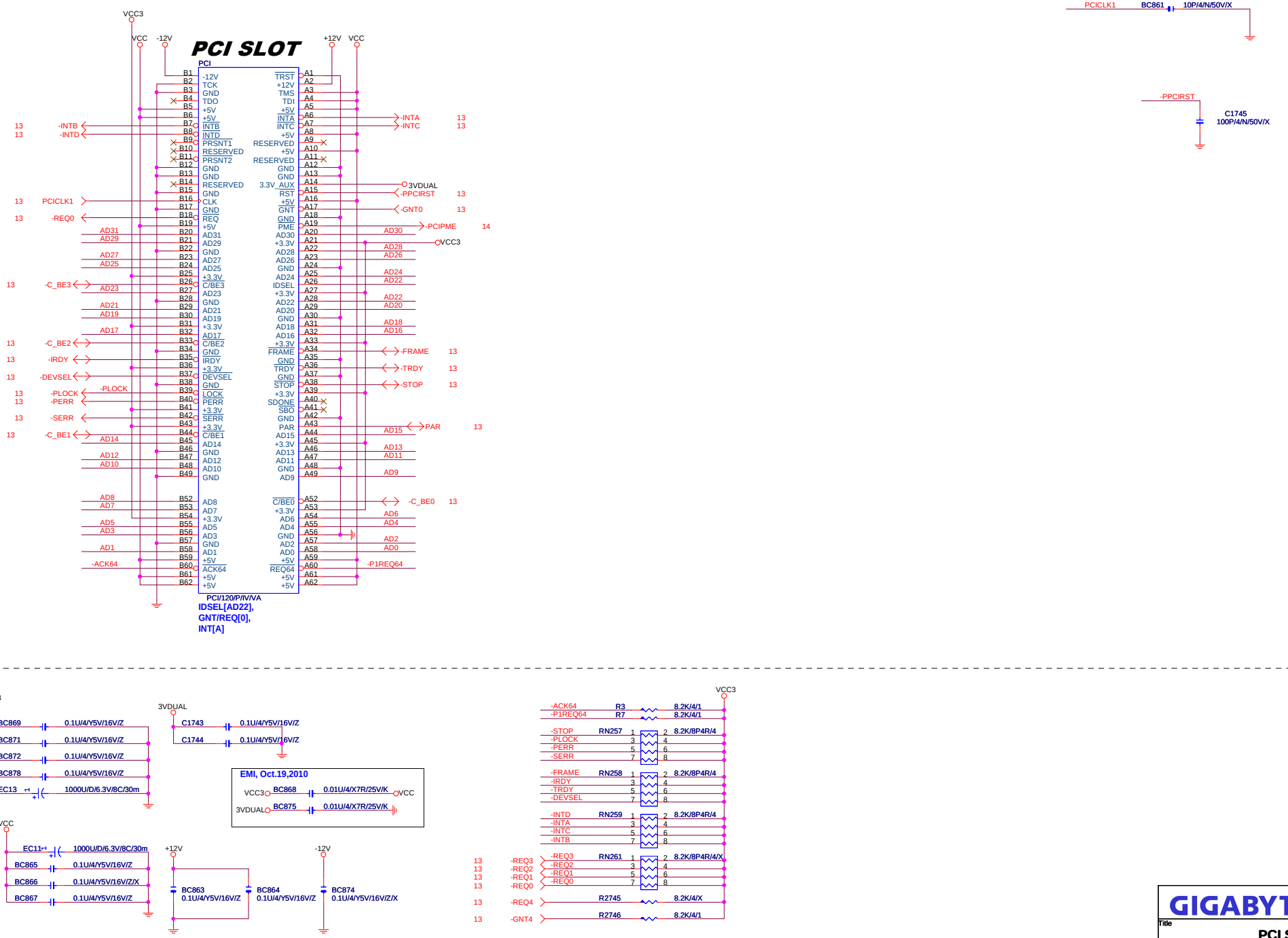
GIGABYTE™

Title: PCI EXPRESS X 16 ,X1

Size	Document Number	Rev
Custom	GA-78LMT-S2P	3.12

Date: Monday, March 28, 2011 Sheet 17 of 28

PCI SLOT 1,2



Title	PCI SLOT 1,2
Size	Custom
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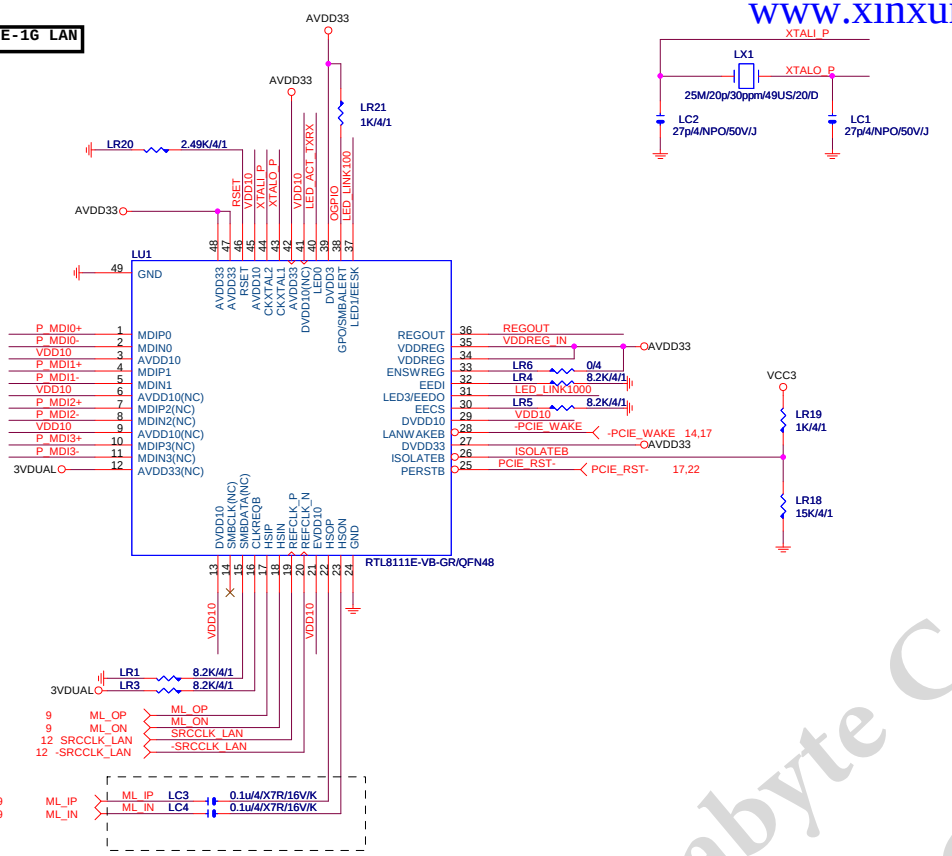
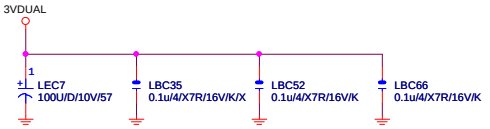
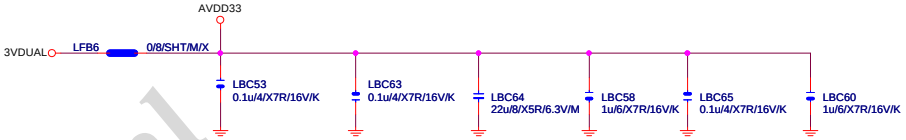
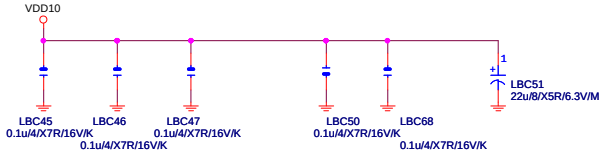
PCIE-1G LAN

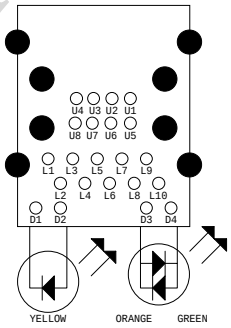


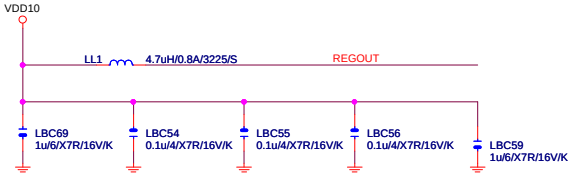




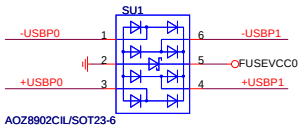


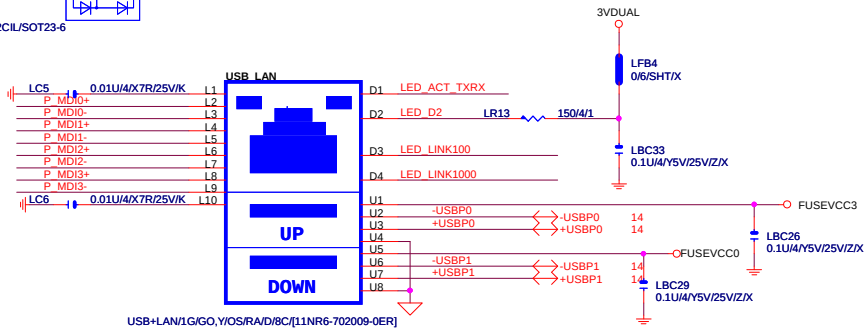
USB_LAN CONNECTOR

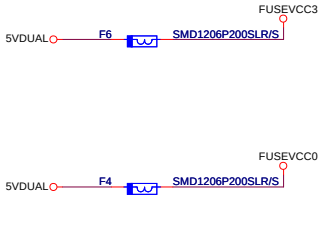


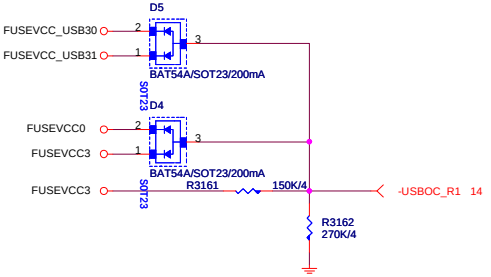


USB_LAN CONNECTOR









EC要靠近USB_PORT的FUSEVCC

USB_LAN

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Title	REALTK RTL8111C/8101E	
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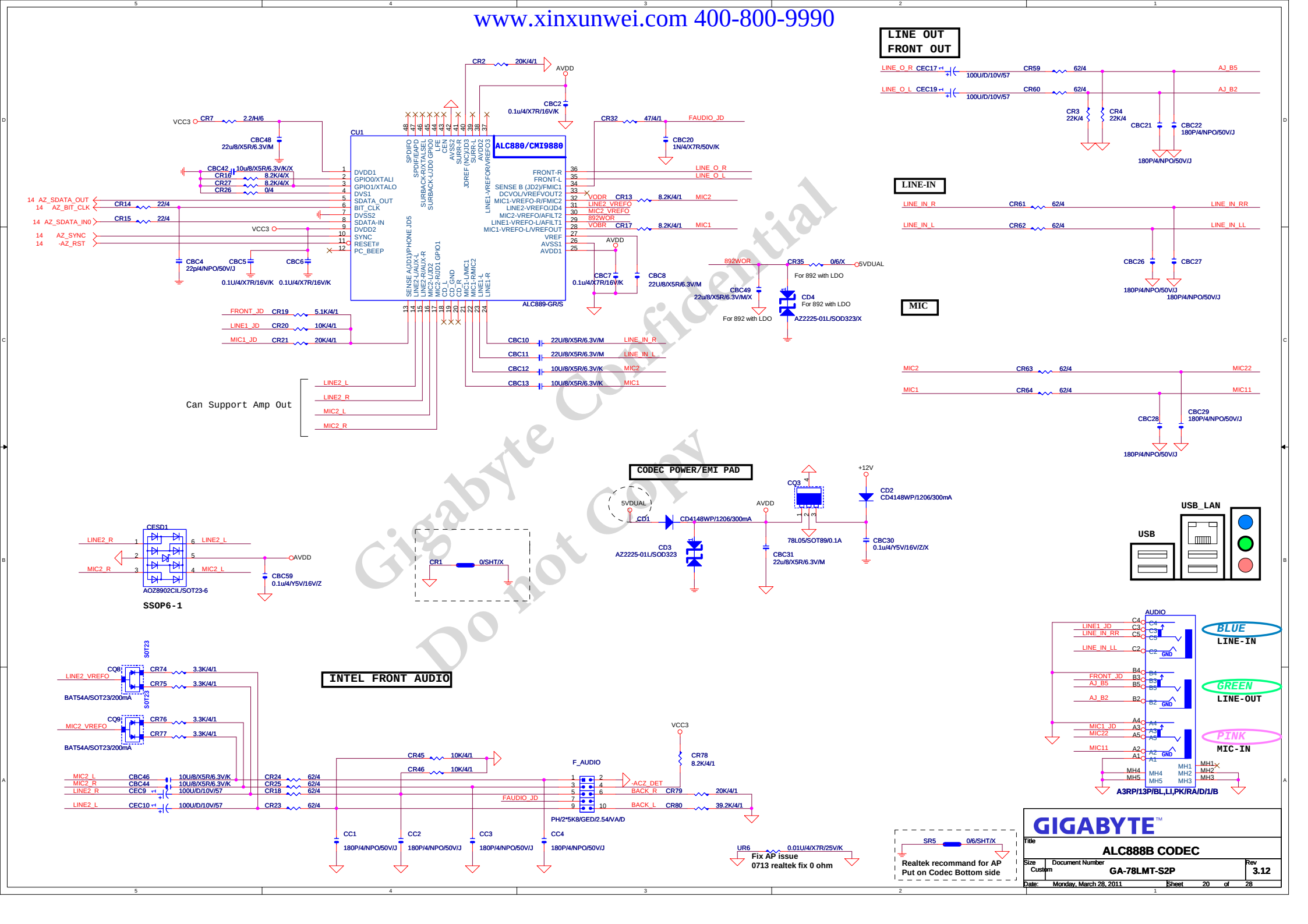

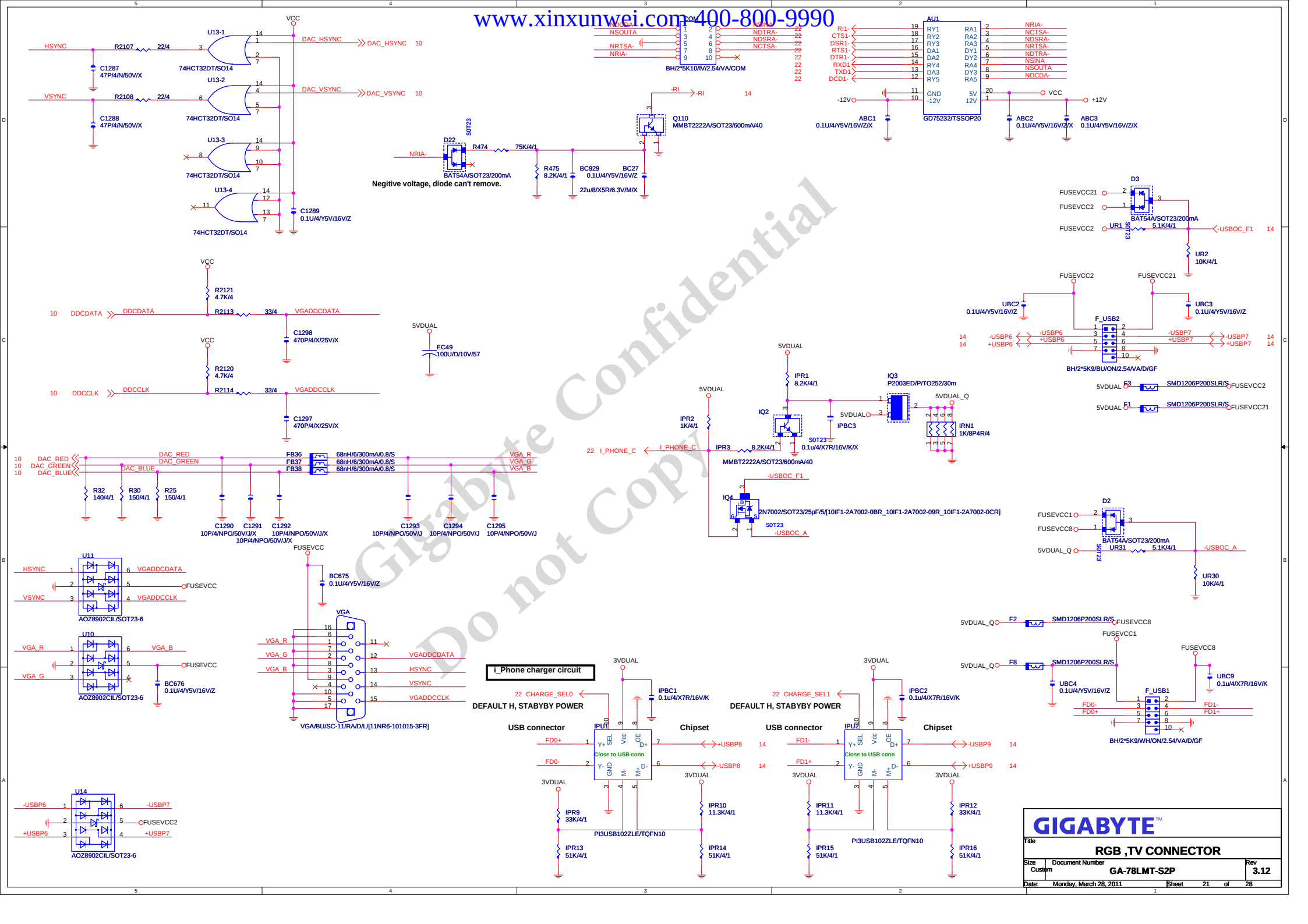

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Title	RGB ,TV CONNECTOR	
Size: Custom	Document Number: GA-78LMT-S2P	Rev: 3.12
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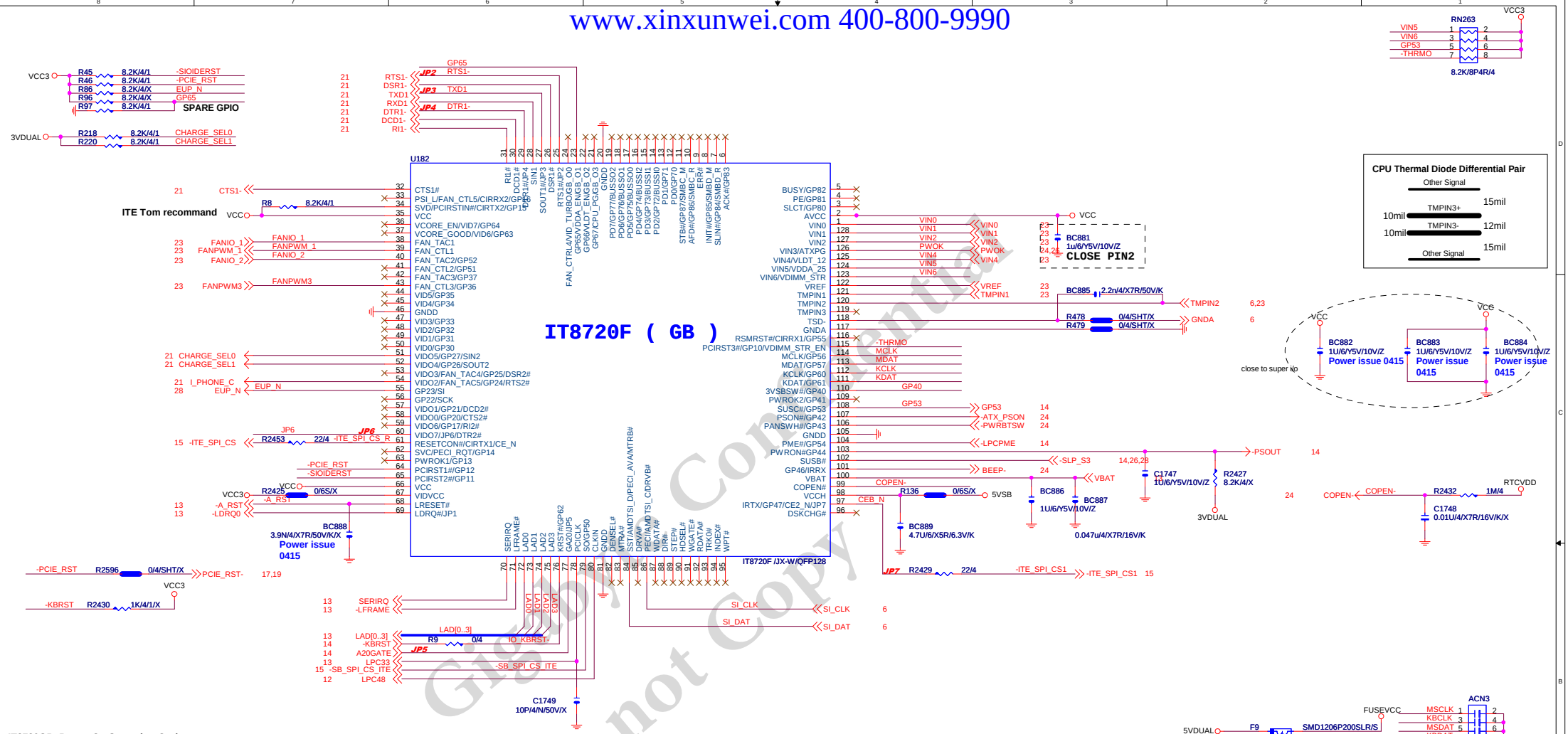

IT8720GB Power On Strapping Options

	Symbol	value	Description
JP1 Pin 69			
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

GIGABYTE			
Title	ITE 8720 LPC IO		
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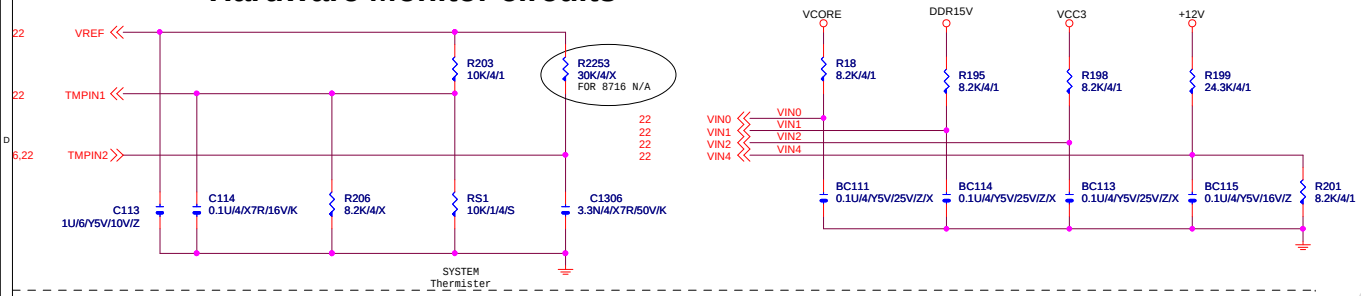
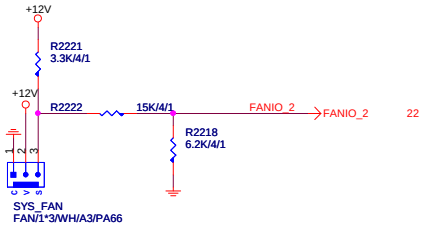
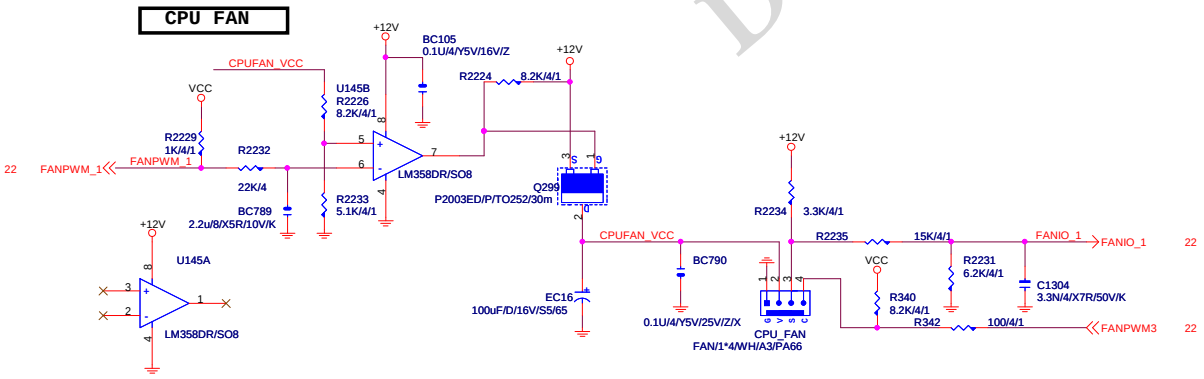
Hardware Monitor circuits

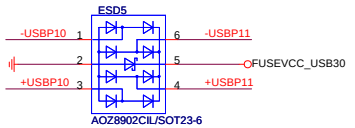


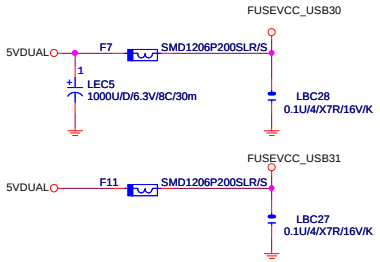
SYSTEM FAN

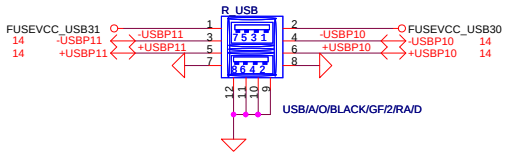


CPU FAN









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Title: FAN/HWMO ,KB/USB

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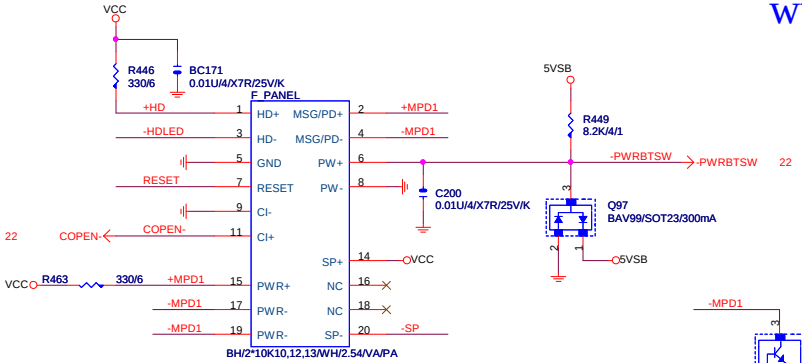
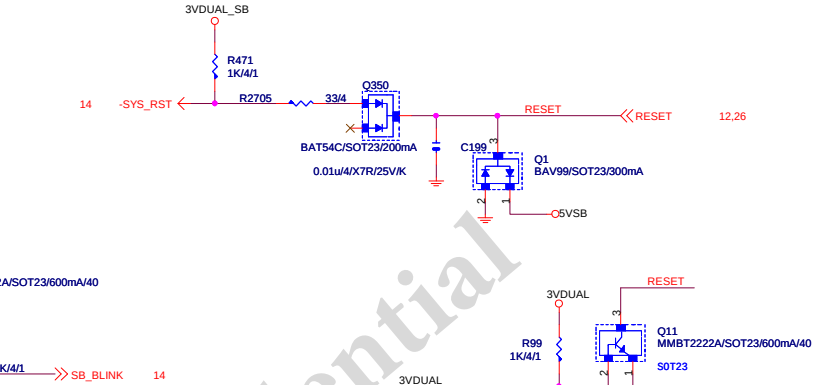
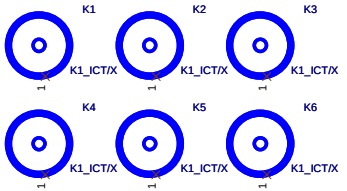
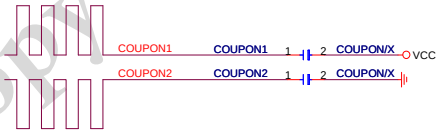
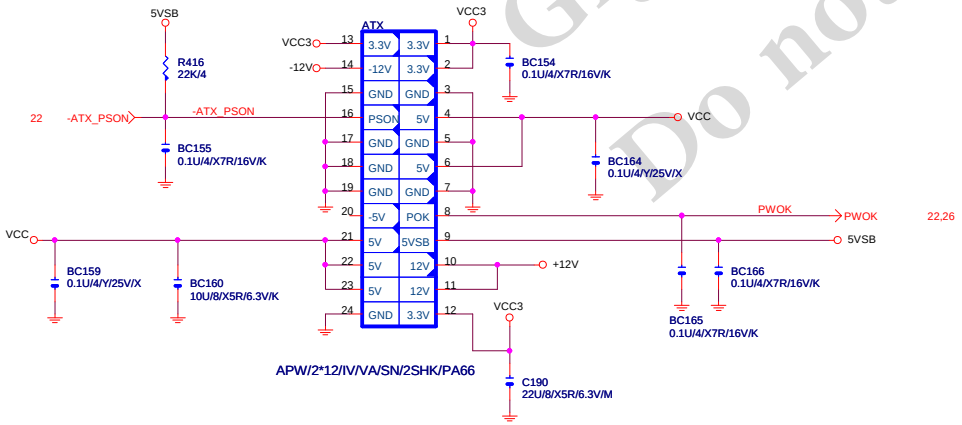


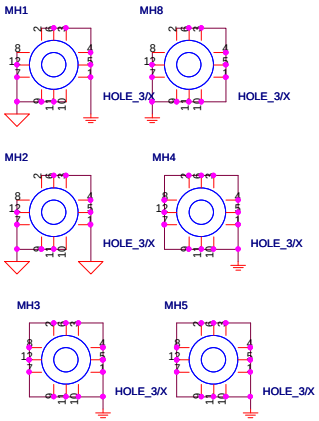






ATX POWER CONNECTOR





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Title	ATX, FRONT PANEL	
Size: Custom	Document Number: GA-78LMT-S2P	Rev: 3.12
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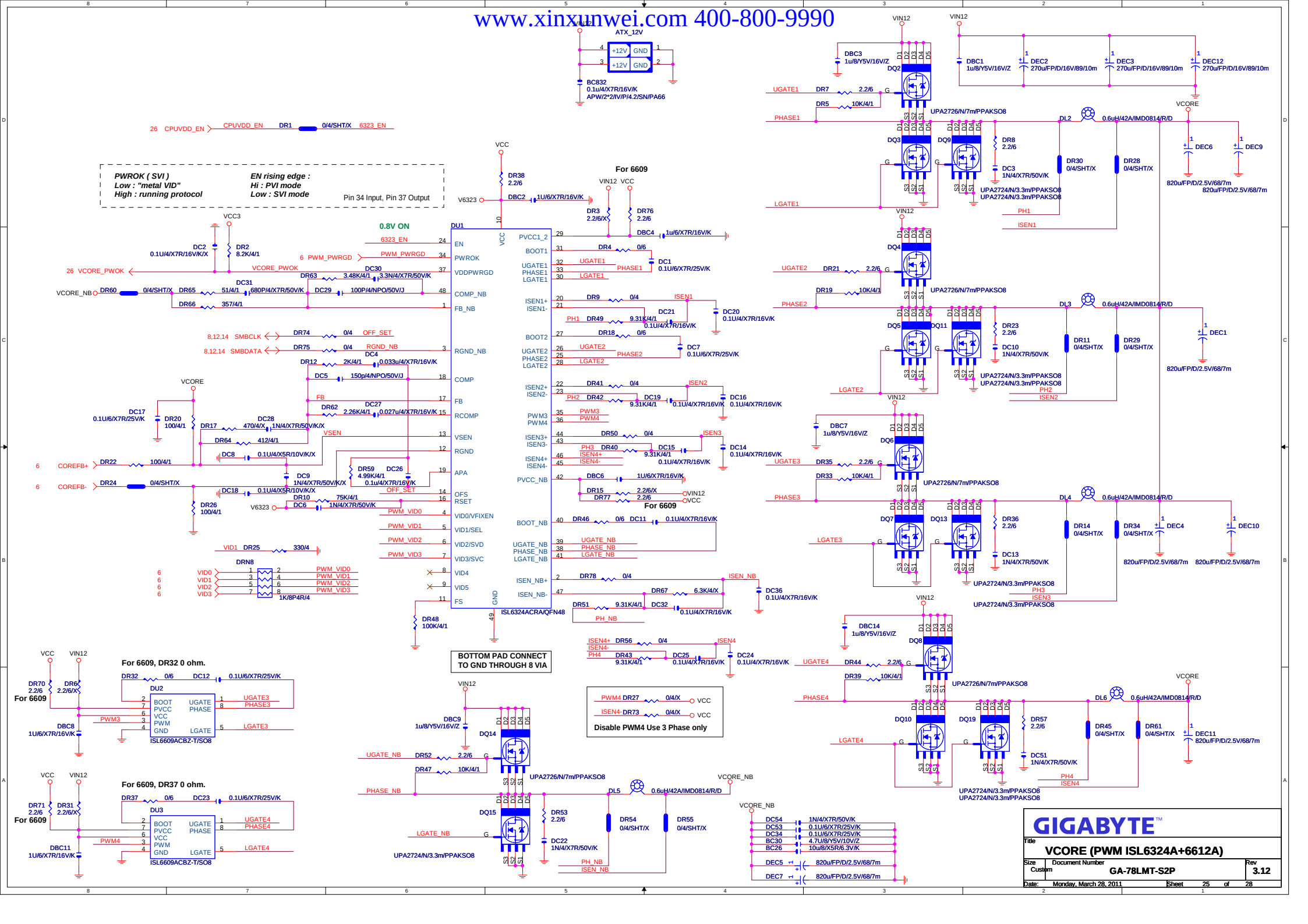

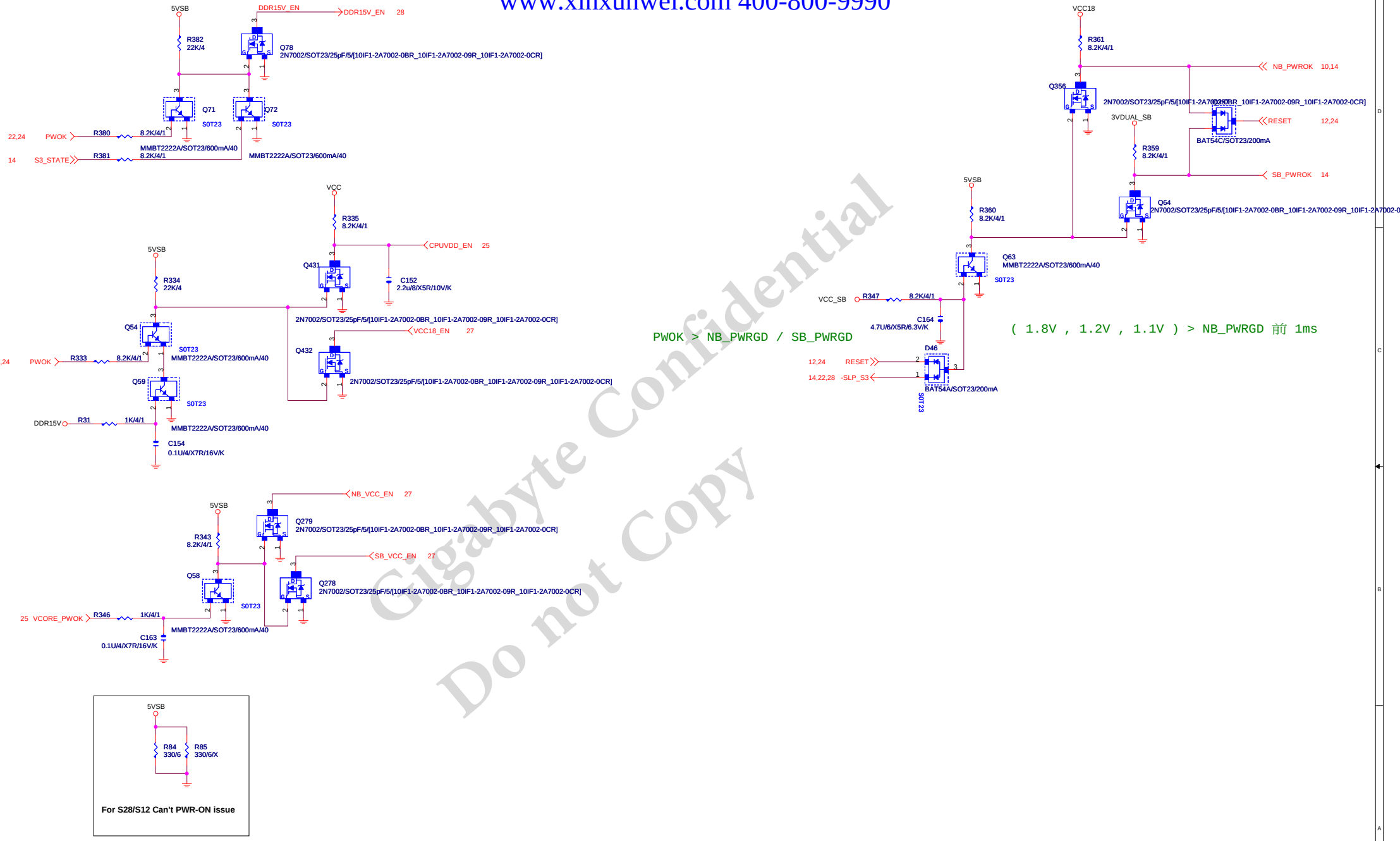

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Title: POWER SEQUENCE		
Size: Custom	Document Number: GA-78LMT-S2P	Rev: 3.12
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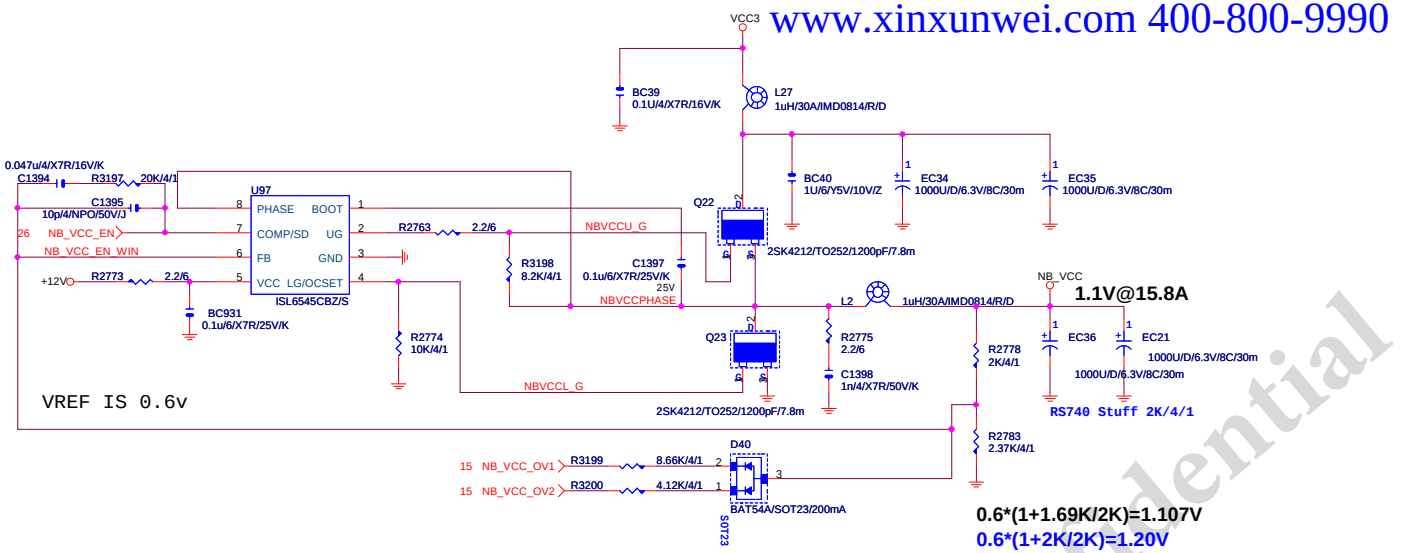
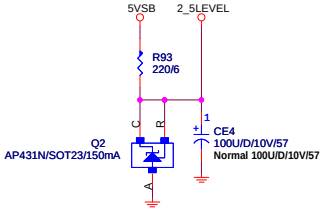
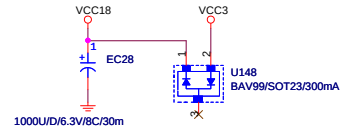


0.6*(1+1.69K/2K)=1.107V

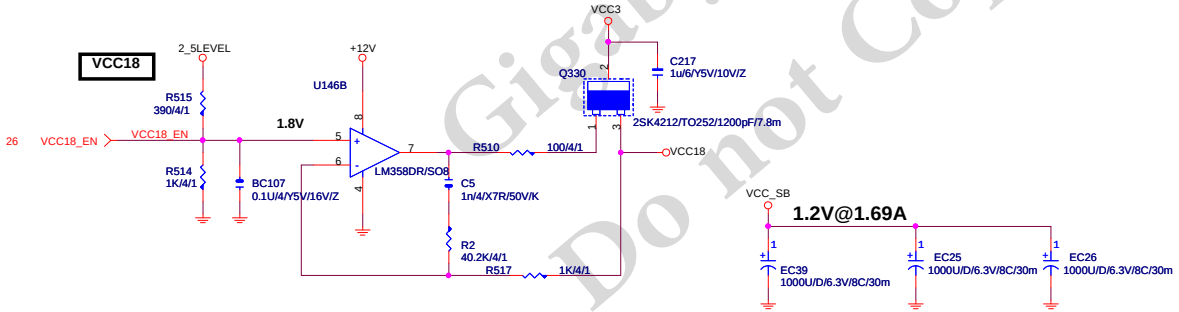
0.6*(1+2K/2K)=1.20V

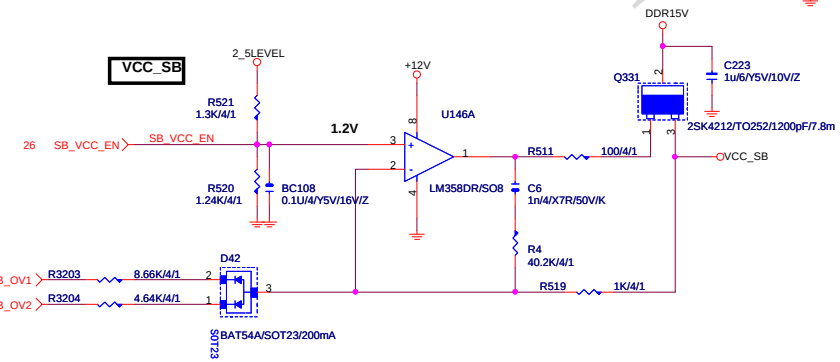
NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V



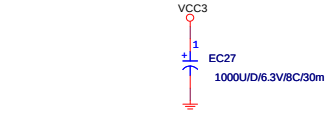


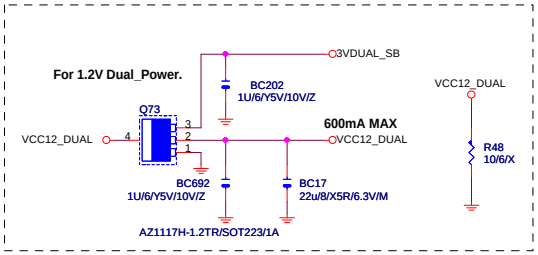
ATI for vcc3/vcc18 power ramp-up 2.1V





VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V





GIGABYTE™

Title: NB/SB POWER,VCC12HT,VDDA25,VCC12Dual

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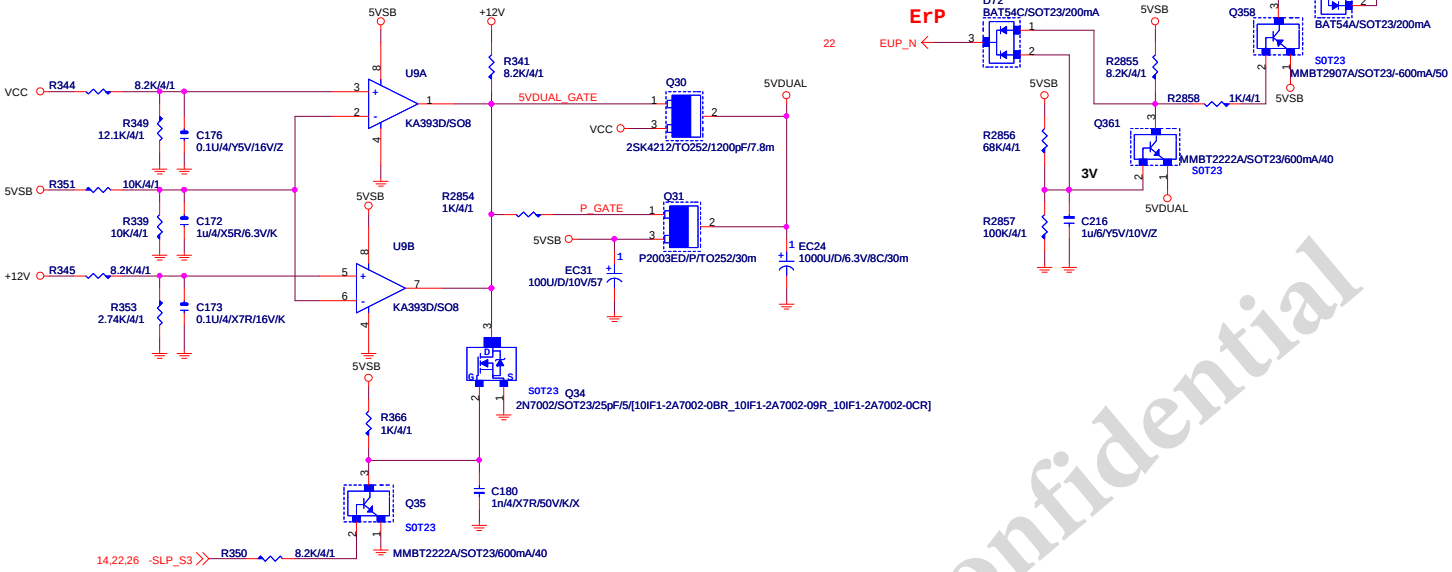
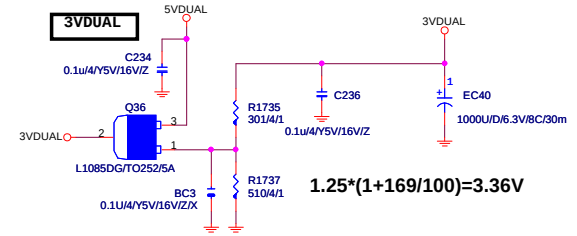
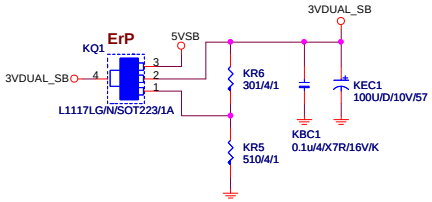
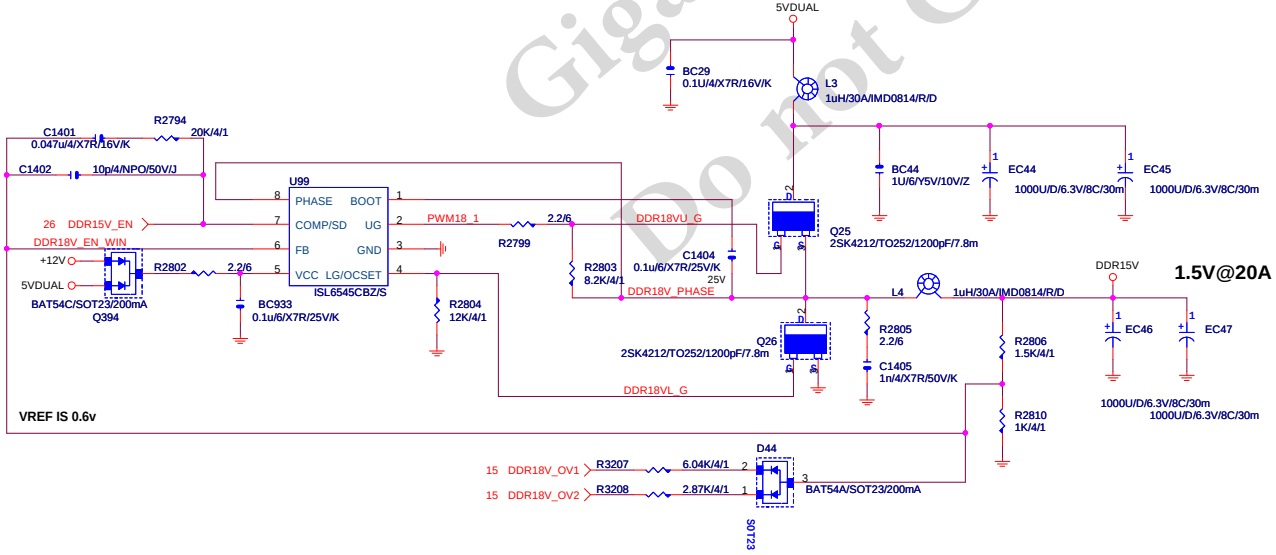
5VDUAL

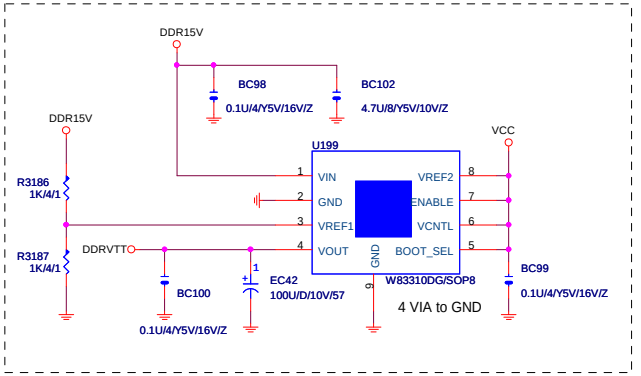


3VDUAL









0.6*(1+3K/1.43K)=1.859V

DDR18V_OV1	DDR18V_OV2	DDR18V
L	X	1.90V
X	L	2.00V
L	L	2.10V

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