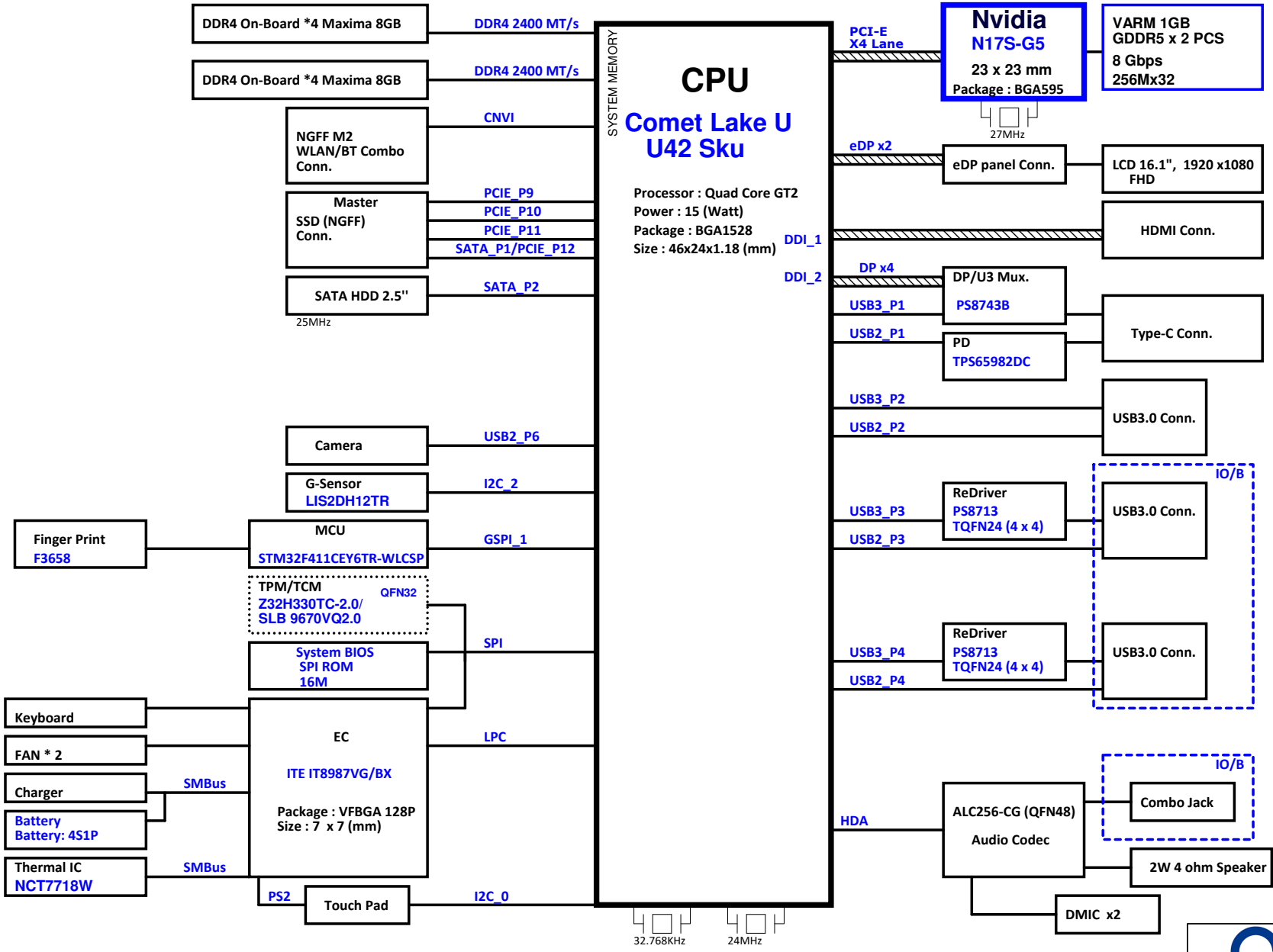
16.1" H97M Block Diagram



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Size	Document Number	Rev
	Block Diagram	3A

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+3.3V_SUS [4,5,11,12,13,14,15,16,26,28,33,36,39,40,44,45,51]
+3.3V_RUN [5,11,12,13,14,16,19,22,24,25,26,28,35,36,37,40,46,48,49,51,52]
+VCCSTG [6,7]
+VCCSTPLL [6,7,46,51]
+TP_PWR [37]

HDMI

DP

U20A

[25] INT_HDMI_TXN2 — AL5 DDI1_TXN_0
[25] INT_HDMI_TXP2 — AL6 DDI1_TXP_0
[25] INT_HDMI_TXN1 — AJ5 DDI1_TXN_1
[25] INT_HDMI_TXP1 — AJ6 DDI1_TXP_1
[25] INT_HDMI_TXN0 — AF6 DDI1_TXN_2
[25] INT_HDMI_TXP0 — AF5 DDI1_TXP_2
[25] INT_HDMI_CLKN — AE5 DDI1_TXN_3
[25] INT_HDMI_CLKP — AE6 DDI1_TXP_3

[32] INT_DP_TXN0 — AC4 DDI2_TXN_0
[32] INT_DP_TXP0 — AC3 DDI2_TXP_0
[32] INT_DP_TXN1 — AC1 DDI2_TXN_1
[32] INT_DP_TXP1 — AC2 DDI2_TXP_1
[32] INT_DP_TXN2 — AE4 DDI2_TXN_2
[32] INT_DP_TXP2 — AE3 DDI2_TXP_2
[32] INT_DP_TXN3 — AE1 DDI2_TXN_3
[32] INT_DP_TXP3 — AE2 DDI2_TXP_3

EDP_TXN_0 AG4 — INT_EDP_TXN0 [24]
EDP_TXP_0 AG3 — INT_EDP_TXP0 [24]
EDP_TXN_1 AG2 — INT_EDP_TXN1 [24]
EDP_TXP_1 AG1 — INT_EDP_TXP1 [24]
EDP_TXN_2 AJ4
EDP_TXP_2 AJ3
EDP_TXN_3 AJ2
EDP_TXP_3 AJ1

EDP_AUX AH4 — INT_EDP_AUXN [24]
EDP_AUX_P AH3 — INT_EDP_AUXP [24]
DISP_UTILS AM7
DDI1_AUX AC7
DDI1_AUX_P AC6
DDI2_AUX AD4 — INT_DP_AUXN [32]
DDI2_AUX_P AD3 — INT_DP_AUXP [32]
DDI3_AUX AG7
DDI3_AUX_P AG6

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6 INT_DP_HPD — INT_HDMI_HPD [25], INT_DP_HPD [31,32]
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6 SIO_EXT_SCI# — SIO_EXT_SCI# [40]
GPP_E17/EDP_HPD/DISP_MISC4 CM7 EDP_HPD — EDP_HPD [24]

EDP_BKLTEN CK11 — LCD_BL_EN [24,40]
EDP_VDDEN CG11 — DP_ENVDD [24]
EDP_BKLTCTL CH11 — LCD_PWM [24]

DISP_RCOMP AM6
GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DPPB_CTRLDATA
GPP_E20/DPPC_CTRLCLK CH4
GPP_E21/DPPC_CTRLDATA CH3
GPP_E22/DPPD_CTRLCLK CP4
GPP_E23/DPPD_CTRLDATA CN4
GPP_H16/DDPF_CTRLCLK CR26
GPP_H17/DDPF_CTRLDATA CP26

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DDPB_CTRLDATA/ GPP_E19
Display Port B Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.(Default)
1 = Port B is detected.

+3.3V_RUN — R383 2.2K_4 — DDPC_CTRLDATA

DISP_RCOMP signals should be shorted near balls and routed with typical impedance <20 mohms

+1.05V_RUN — R391 24.9/F_2 — EDP_RCOMP

[25] HDMI_SCL — CC8
[25] HDMI_SDA — CC9

DDPC_CTRLDATA — CH3

DDPC_CTRLDATA/ GPP_E21
This signal has a weak internal pull-down.
0 = Port C is not detected. (Default)
1 = Port C is detected.

+TS_POWER
R373 10K/F_2 — TOUCH_INT#
R398 100K_2 — TOUCH_RST

[24] TOUCH_RST — R396 *SP_2_NC — TOUCH_RST_C

+VCCSTG
R353 1K/F_2 — H_PROCHOT#
+VCCSTPLL
R390 1K/F_2 — PM_THRMTRIP#
+TP_PWR
R644 10K/F_2 — PCH_TP_INTR#
+3.3V_SUS
R546 10K/F_2 — DGPU_HOLD_RST#

+VCCSTPLL — TP50

R366 49.9/F_2 — CATERR# AA4
[40] EC_PECI — R354 499/F_2 — EC_PECI AR1
[40,42,46] H_PROCHOT# — PROCHOT# Y4
PM_THRMTRIP# BJ1

TP38 — XDP_BPM0_R U1
TP44 — XDP_BPM1_R U2
U3
U4

CE9
[24] TOUCH_INT# — R388 *SP_2_NC — TOUCH_INT#_C CN3
[37] PCH_TP_INTR# — PCH_TP_INTR# CB34
[19] DGPU_HOLD_RST# — DGPU_HOLD_RST# CC35

R137 49.9/F_2 — PROC_POPIRCOMP BP27
R133 49.9/F_2 — PCH_OPI_RCOMP BW25
R378 *49.9/F_2_NC — EDRAM_OPIO_RCOMP L5
R376 *49.9/F_2_NC — EOPIO_RCOMP N5

U20D

CATERR# PECI PROCHOT# THRMTRIP#
BPM#_0 BPM#_1 BPM#_2 BPM#_3
GPP_E3/CPU_GP0 GPP_E7/CPU_GP1 GPP_B3/CPU_GP2 GPP_B4/CPU_GP3
PROC_POPIRCOMP PCH_OPIRCOMP OPCE_RCOMP OPC_RCOMP

PROC_TCK T6 — PROC_TDI U6 — PROC_TDO Y5 — PROC_TMS T5 — PROC_TRST# AB6
PCH_JTAG_TCK W6
PCH_TCK U5 — PCH_TDI W5 — PCH_TDO P5 — PCH_TMS Y6 — PCH_TRST# P6 — PCH_JTAGX

PROC_PREQ# W2 — XDP_PRDY#_CPU
PROC_PRDY# W1 — XDP_PREQ#_CPU

TP10 TP8 TP51 TP37 TP9 TP12 TP39 TP45

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CFL_U_43E_IL_IP_DDR4

Reserve EDP_HPD opposites circuit!

+3.3V_SUS
SIO_EXT_SCI# R399 10K/F_2
EDP_HPD R403 100K_2
INT_DP_HPD R400 *100K_2_NC

Place near CPU

+VCCSTG
PROC_TDI R44 51_2
PROC_TDO R370 100/F_2
PROC_TMS R362 51_2
PROC_TCK R50 51_2

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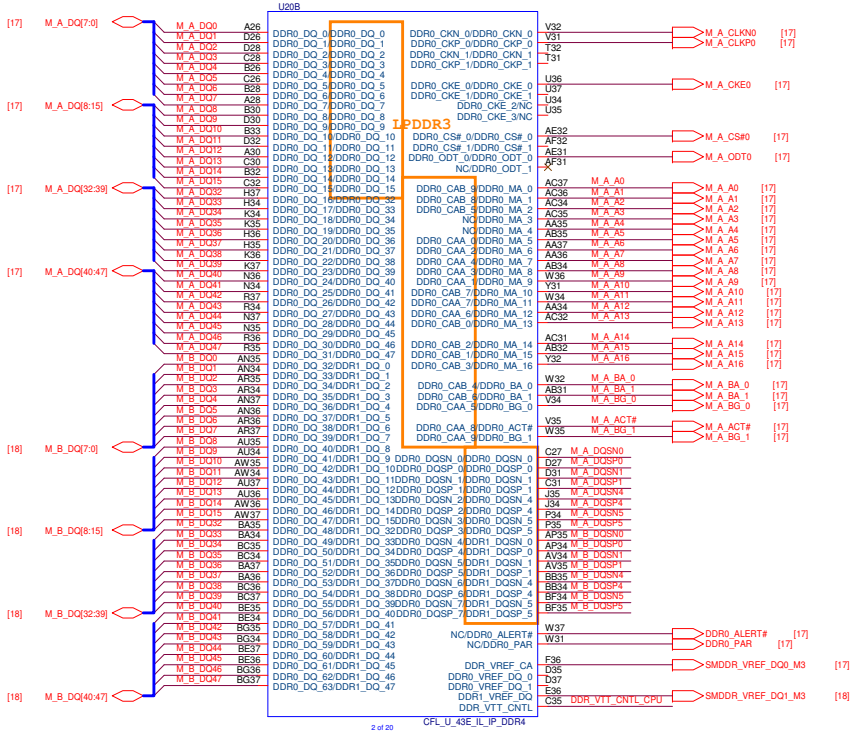
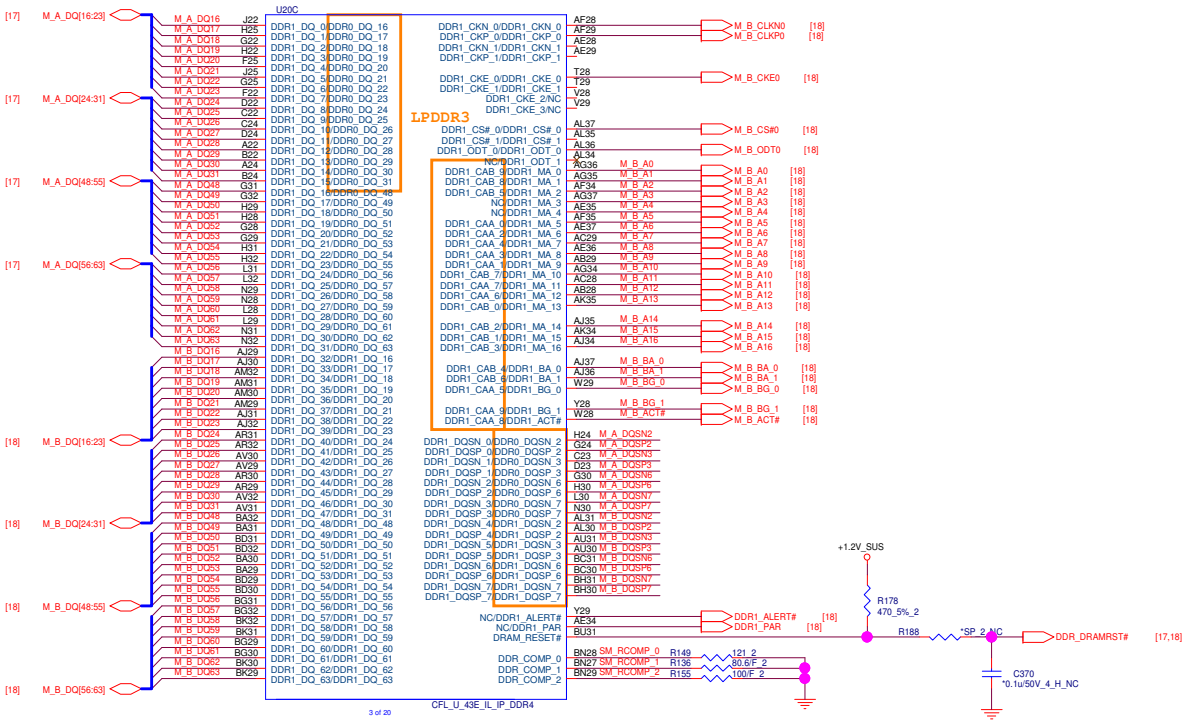
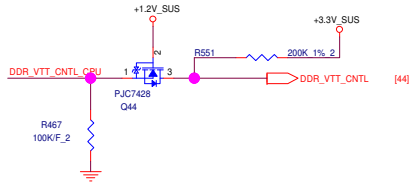
WHL ULT Processor (DDR4) (Non-Interleaved)

WHL ULT Processor (MEM-A)



WHL ULT Processor (MEM-B)





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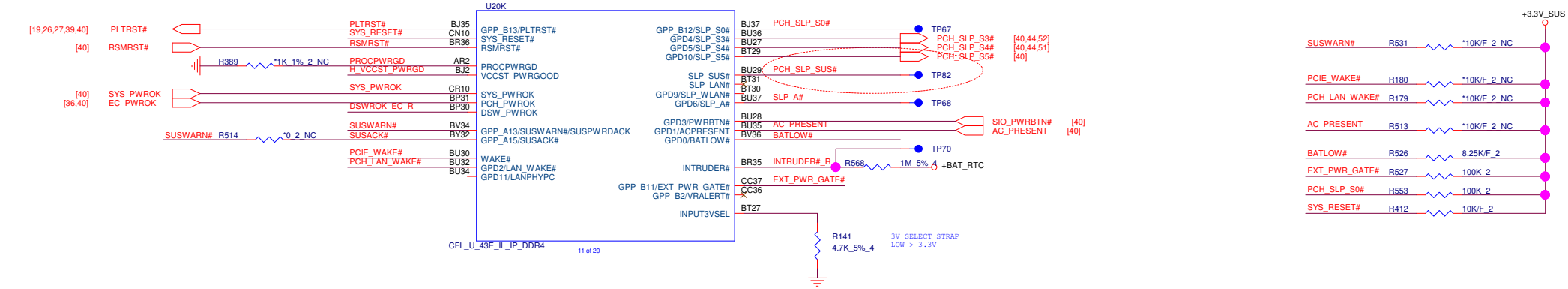
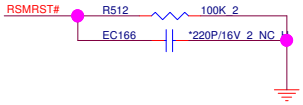
+3.3V_SUS [3,4,11,12,13,14,15,16,26,28,33,36,39,40,44,45,51]
+3.3V_RUN [3,11,12,13,14,16,19,22,24,25,26,28,35,36,37,40,46,48,49,51,52]
+VCCSTPLL [3,6,7,46,51]
+BAT_RTC [14,15]

05

PCH Pull-high/low(CLG)



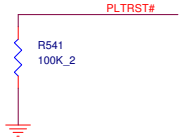
RSMRST#



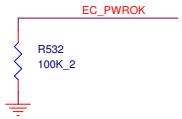
DSW_PWROK

PLTRST#

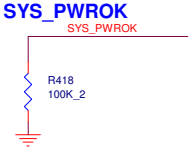
Rise/Fall time less than 100ns

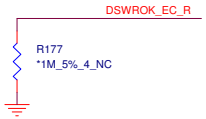


PCH_PWROK

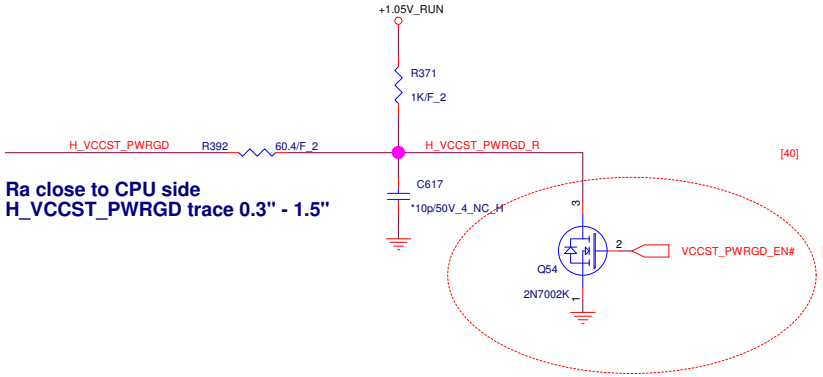


SYS_PWROK



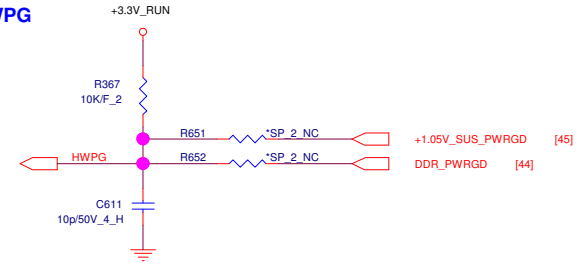


2/3 R616 need change to 1M follow CRB



Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

HWPG



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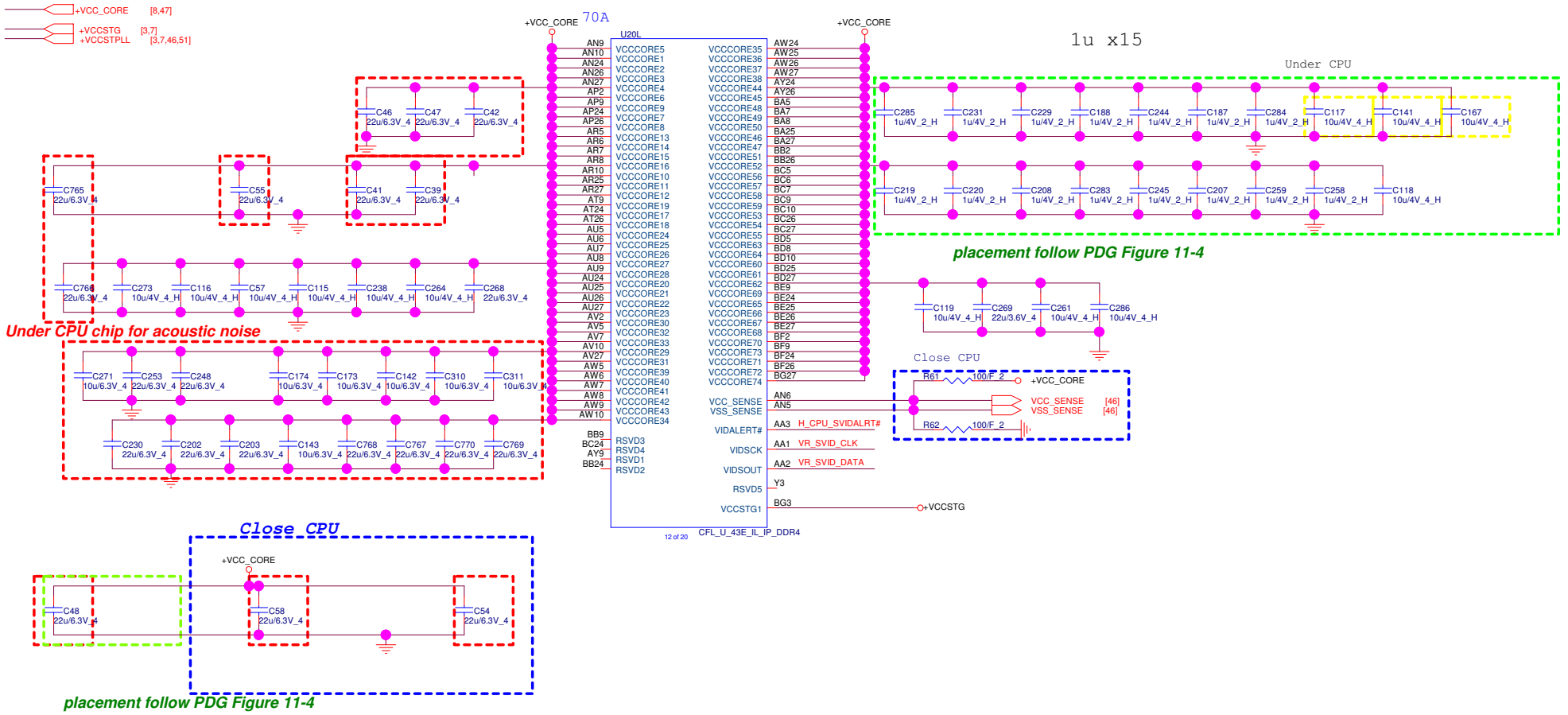

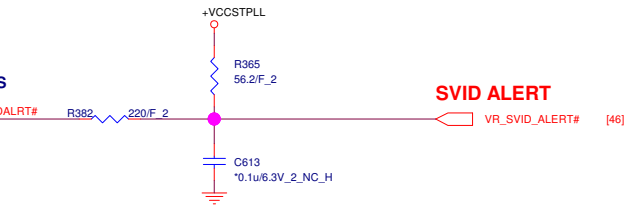

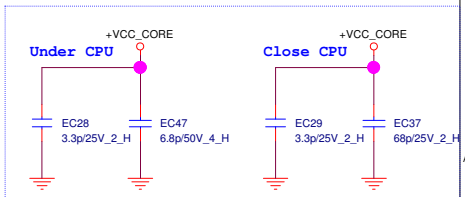

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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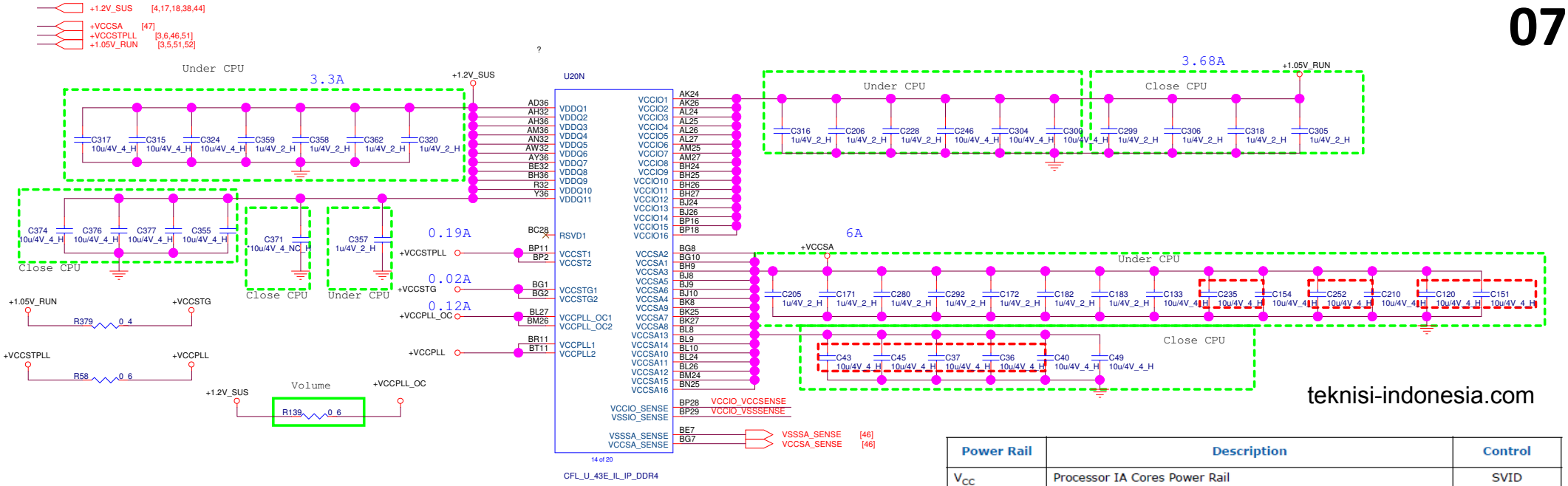
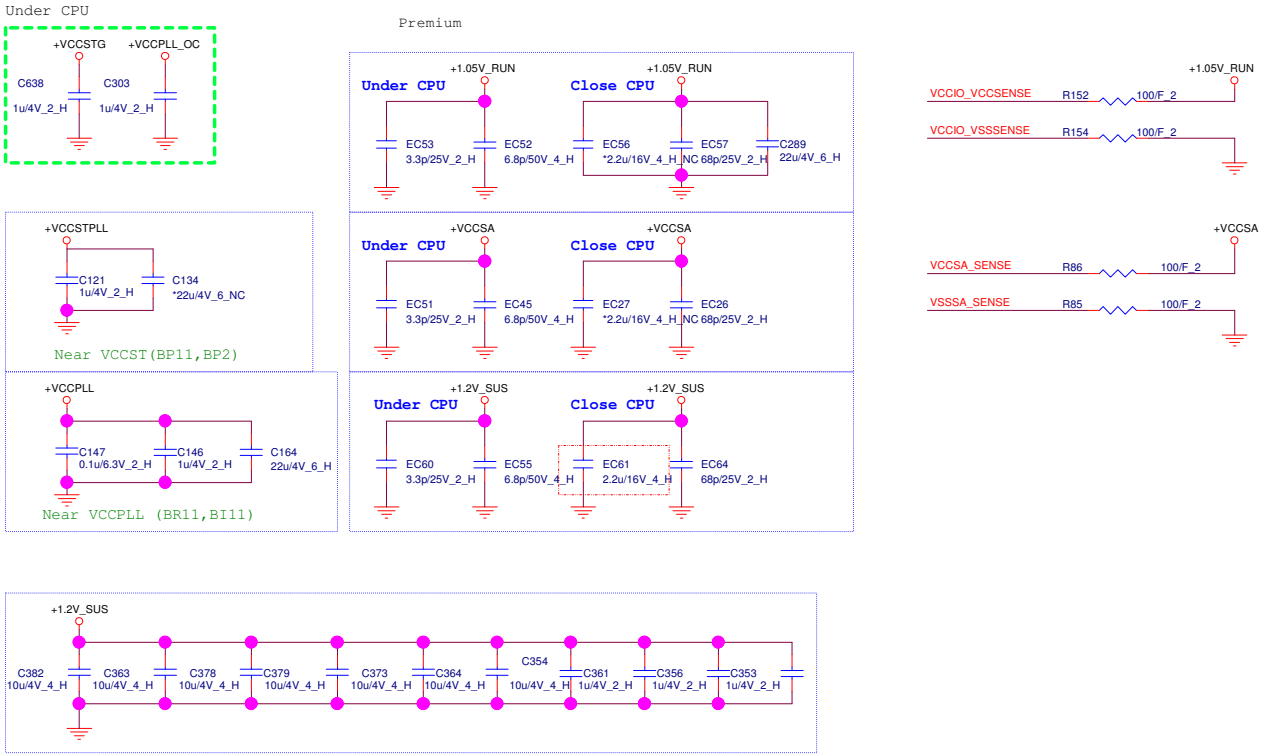


Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



Close to CPU

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+VCCGT [47,52]
+VCC_CORE [6,47]

31A

Under CPU

C221 10u/4V_4_H, C222 10u/4V_4_H, C132 10u/4V_4_H, C162 10u/4V_4_H, C129 10u/4V_4_H, C131 10u/4V_4_H, C163 10u/4V_4_H, C159 10u/4V_4_H, C161 10u/4V_4_H, C160 10u/4V_4_H, C128 10u/4V_4_H, C130 10u/4V_4_H

Close CPU

C650 47u/6.3V_6_H, C645 47u/6.3V_6_H, C601 47u/6.3V_6_H, C665 47u/6.3V_6_H, C647 47u/6.3V_6_H, C642 47u/6.3V_6_H

C114 22u/6.3V_4_H, C155 22u/6.3V_4_H, C192 22u/6.3V_4_H, C138 22u/6.3V_4_H, C180 22u/6.3V_4_H, C618 22u/6.3V_4_H, C614 22u/6.3V_4_H

+VCC_CORE

C223 22u/6.3V_4_H, C635 10u/4V_4_H, C255 22u/6.3V_4_H, C241 22u/6.3V_4_H, C619 10u/4V_4_H, C633 10u/4V_4_H, C254 22u/6.3V_4_H

C240 22u/6.3V_4_H, C637 10u/4V_4_H, C632 10u/4V_4_H, C634 10u/4V_4_H, C627 10u/4V_4_H, C636 10u/4V_4_H, C626 10u/4V_4_H

+VCCGT

C165 1u/4V_2_H, C644 1u/4V_2_H, C649 1u/4V_2_H, C135 1u/4V_2_H, C663 1u/4V_2_H, C646 1u/4V_2_H

C184 1u/4V_2_H, C616 1u/4V_2_H, C144 1u/4V_2_H, C185 1u/4V_2_H, C652 1u/4V_2_H, C186 1u/4V_2_H

U20M

A5	VCCGT8	VCCGT58	D15
A6	VCCGT9	VCCGT59	D17
A8	VCCGT10	VCCGT60	D18
A11	VCCGT1	VCCGT61	D20
A12	VCCGT2	VCCGT64	E4
A14	VCCGT3	VCCGT69	F5
A15	VCCGT4	VCCGT70	F6
A17	VCCGT5	VCCGT71	F7
A18	VCCGT6	VCCGT72	F8
A20	VCCGT7	VCCGT65	F11
AA9	VCCGT11	VCCGT66	F14
AB2	VCCGT13	VCCGT67	F17
AB8	VCCGT14	VCCGT68	F20
AB9	VCCGT15	VCCGT73	G11
AB10	VCCGT12	VCCGT74	G12
AC8	VCCGT16	VCCGT75	G14
AD9	VCCGT17	VCCGT76	G15
AE8	VCCGT19	VCCGT77	G17
AE9	VCCGT20	VCCGT78	G18
AE10	VCCGT18	VCCGT79	G20
AF2	VCCGT22	VCCGT87	H5
AF8	VCCGT23	VCCGT88	H6
AF10	VCCGT21	VCCGT89	H7
AG8	VCCGT24	VCCGT90	H8
AG9	VCCGT25	VCCGT80	H11
AH9	VCCGT26	VCCGT81	H12
AJ8	VCCGT28	VCCGT82	H14
AJ10	VCCGT27	VCCGT83	H15
AK2	VCCGT29	VCCGT84	H17
AK9	VCCGT30	VCCGT85	H18
AL8	VCCGT32	VCCGT86	H20
AL9	VCCGT33	VCCGT95	J7
AL10	VCCGT31	VCCGT96	J8
AM8	VCCGT34	VCCGT91	J11
B3	VCCGT39	VCCGT92	J14
B4	VCCGT40	VCCGT93	J17
B6	VCCGT41	VCCGT94	J20
B8	VCCGT42	VCCGT98	K2
B11	VCCGT35	VCCGT97	K11
B14	VCCGT36	VCCGT100	L7
B17	VCCGT37	VCCGT101	L8
B20	VCCGT38	VCCGT99	L10
C2	VCCGT49	VCCGT102	M9
C3	VCCGT51	VCCGT104	N7
C6	VCCGT52	VCCGT105	N8
C7	VCCGT53	VCCGT106	N9
C8	VCCGT54	VCCGT103	N10
C11	VCCGT43	VCCGT107	P2
C12	VCCGT44	VCCGT108	P8
C14	VCCGT45	VCCGT109	R9
C15	VCCGT46	VCCGT111	T8
C17	VCCGT47	VCCGT112	T9
C18	VCCGT48	VCCGT110	T10
C20	VCCGT50	VCCGT114	U8
D4	VCCGT62	VCCGT113	U10
D7	VCCGT63	VCCGT115	V2
D11	VCCGT55	VCCGT116	V9
D12	VCCGT56	VCCGT117	W8
D14	VCCGT57	VCCGT118	W9
Y10	VCCGT119	VCCGT120	Y8
		VCCGT_SENSE	E3
		VSSGT_SENSE	D2

CFL_U_43E_IL_IP_DDR4

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+VCC_CORE

+VCCGT

R33 100/F_2 VCCGT_SENSE [46]

R40 100/F_2 VSSGT_SENSE [46]

Under CPU

+VCCGT

EC44 3.3p/25V_2_H, EC46 6.8p/50V_4_H

Close CPU

+VCCGT

EC161 *2.2u/16V_4_H, EC160 NC 68p/25V_2_H

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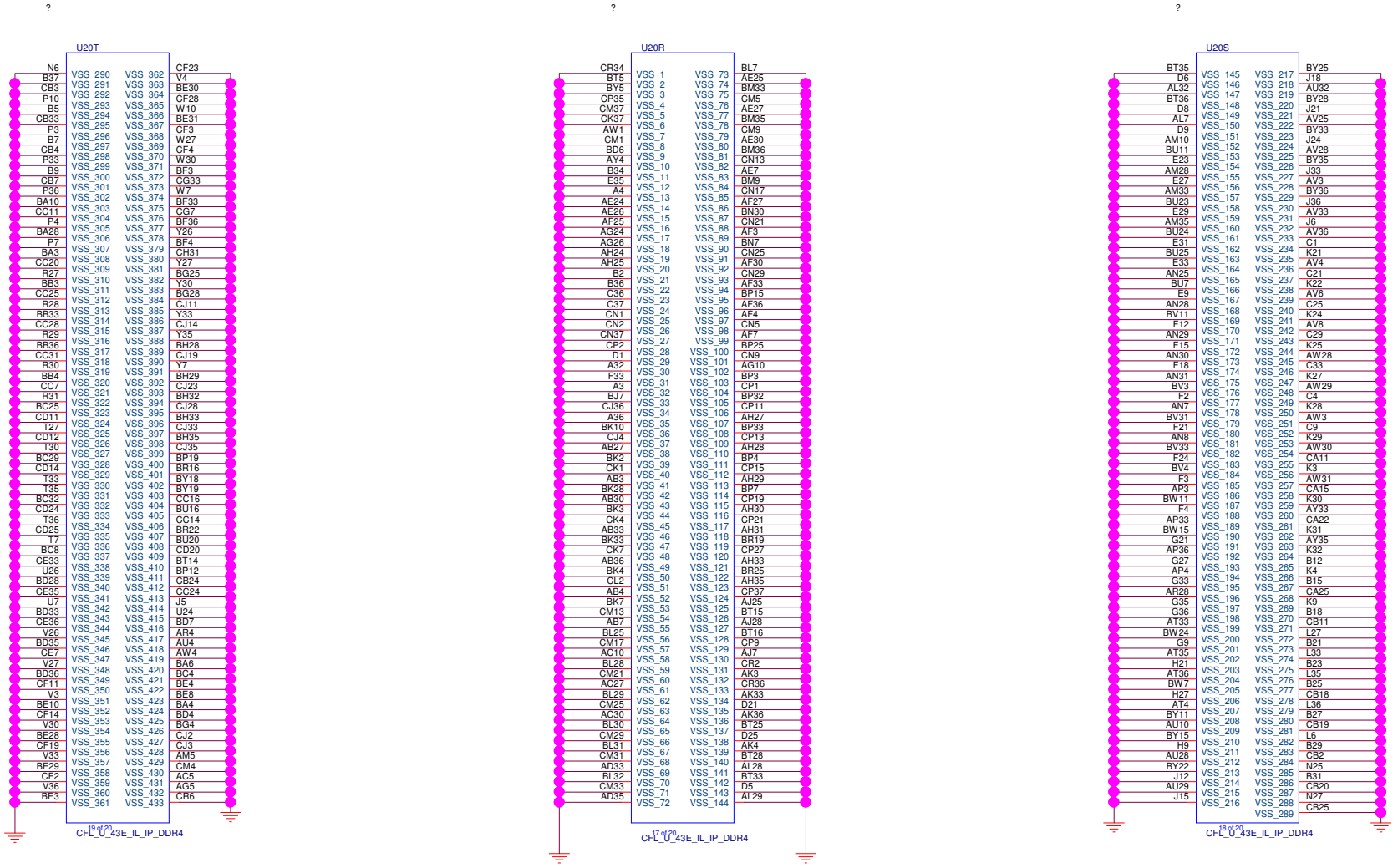

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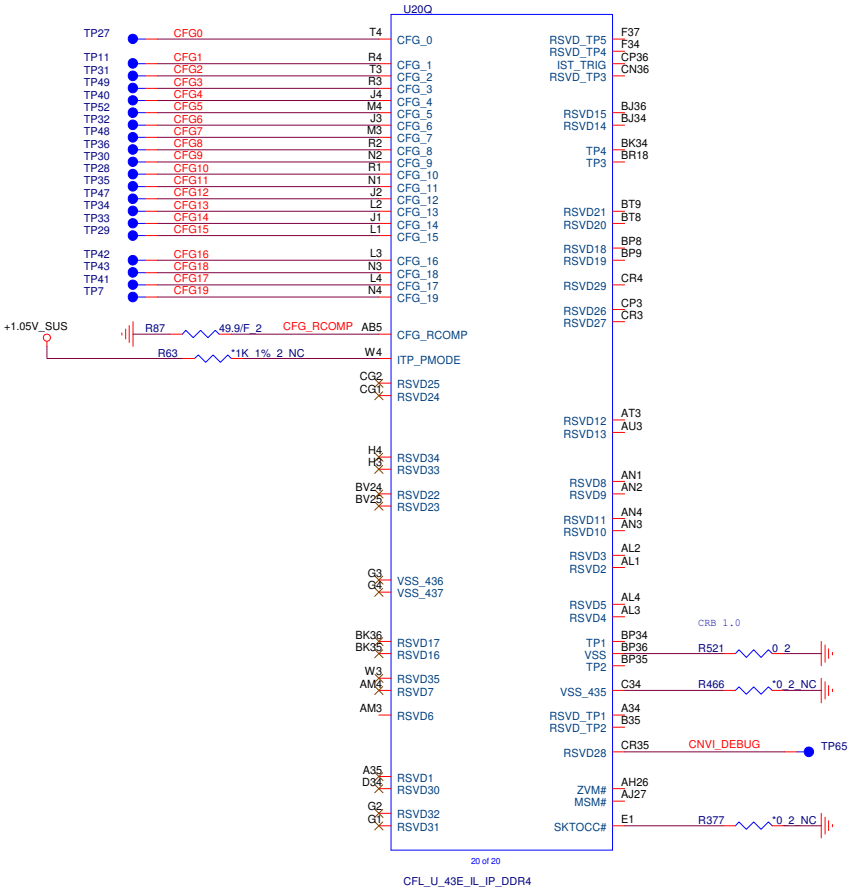
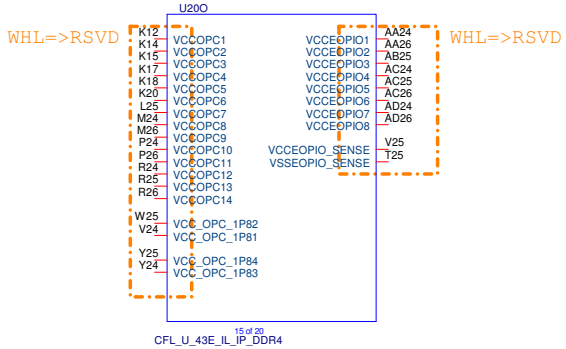
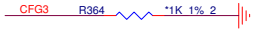
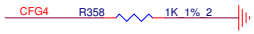




Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

Quanta Computer Inc.
PROJECT : H97M

Size	Document Number	Rev
	CML-U 8/15 (RSV)	3A

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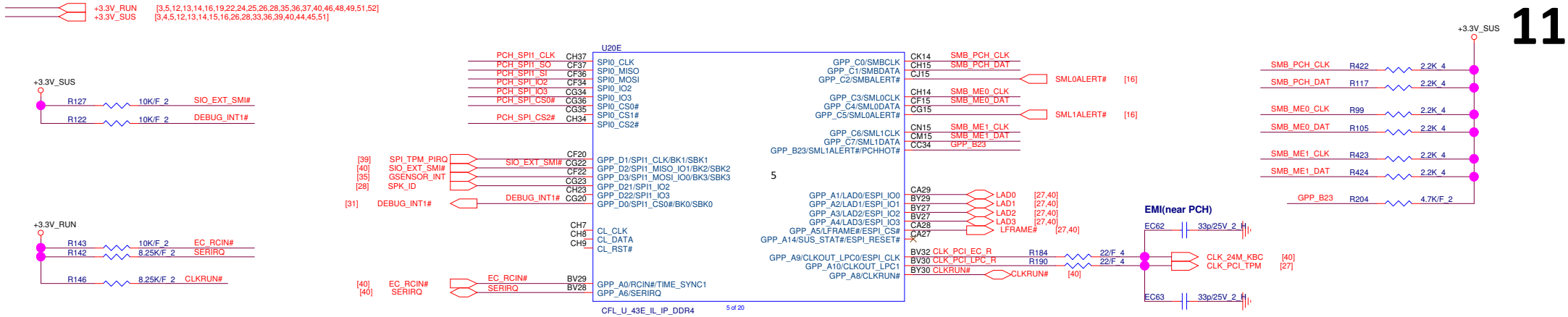
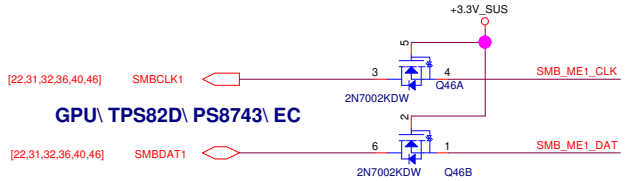


SMBus/Pull-up(CLG)



GPU\ TPS82D\ PS8743\ EC

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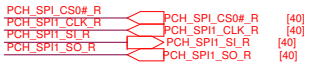
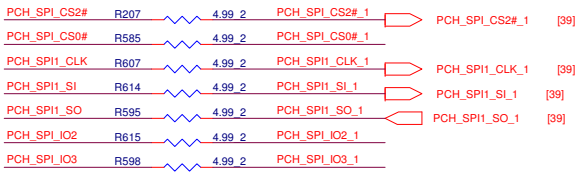
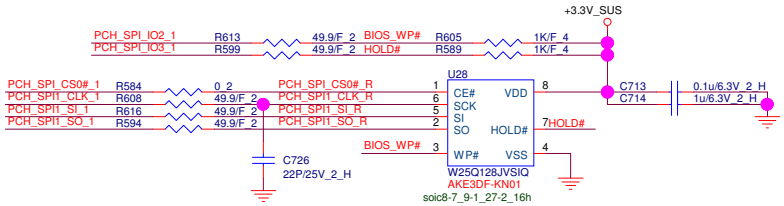
Vender	Size	P/N
MXIC	16MB	(MX25L12873GM2I-08GH)
Winbond	16MB	AKE3DF-KN01(W25Q128JVSIQ)
Socket		DG008000011

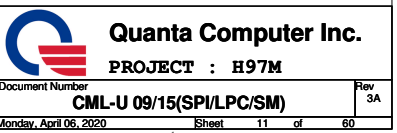
EC side





PCH SPI ROM(CLG)





WHLake (GPIO)

+3.3V_RUN [3,5,11,13,14,16,19,22,24,25,26,28,35,36,37,40,46,48,49,51,52]
+3.3V_SUS [3,4,5,11,13,14,15,16,26,28,33,36,39,40,44,45,51]
+1.8V_SUS [14,15,27,28,45,49]

U20F

M.2 CNVI MODES
LOW-> INTEGRATED CNVI ENABLE
HIGH-> INTEGRATED CNVI DISABLE

Touch pad
Touch Panel
G Sensor

2/7 add for HW STRAP

HDA interface

HDA_RESET#(codec pin11)
Stuff R421 and EC133 for 255
NC R421 and EC133 for 256

close to ball
close to codec
close to ball

U20G

Model	GPU_ID
N17S-G5	0
N17S-G2	1

Model	RAM_D_ID1	RAM_D_ID0
16G (SDP)	0	1
8G (SDP)	1	0
16G (DDP)	1	1

Model	RAM_ID1	RAM_ID0
Hynix	0	0
Samsung	0	1
Micron	1	0
NANYA	1	1

Quanta Computer Inc.
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Size | Document Number: CML-U 10/15(GPIO\HDA) | Rev 3A
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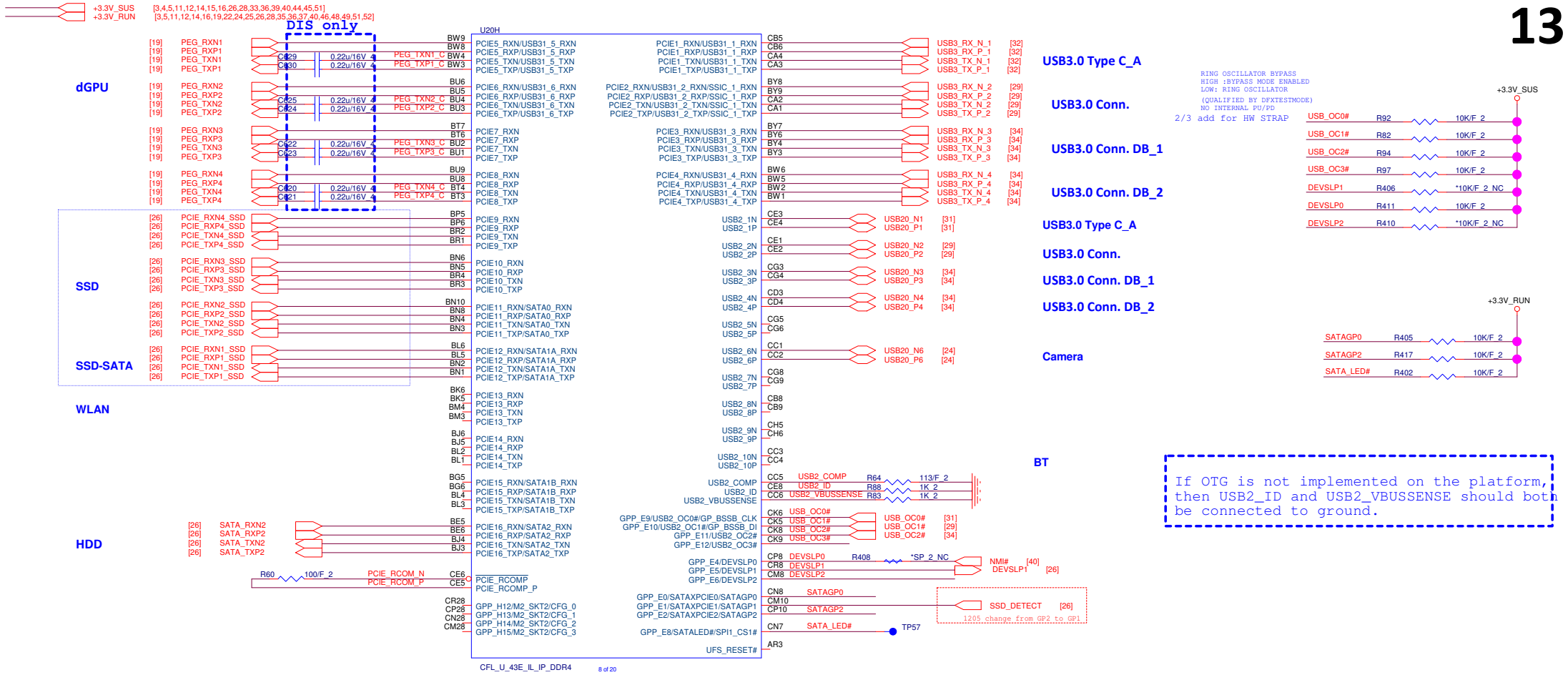

PCI-E Port Mapping Table

Port				Function
1	USB3 #1/PCIe #1	Type C		Type C
2	USB3 #2/PCIe #2			USB3 Conn.
3	USB3 #3/PCIe #3			USB3 Conn.
4	USB3 #4/PCIe #4			USB3 Conn.
5	USB3 #5/PCIe #5	x2	x4	dGPU
6	USB3 #6/PCIe #6			
7	PCIe #7	x2		
8	PCIe #8			
9	PCIe #9	x2	x4	SSD
10	PCIe #10			
11	PCIe #11/SATA #0	x2		
12	PCIe #12/SATA #1A			
13	PCIe #13	x2	x4	NC
14	PCIe #14			NC
15	PCIe #15/SATA #1B	x2		NC
16	PCIe #16/SATA #2			HDD

CLK RQ Port	Function
Port0	dGPU
Port1	SSD
Port2	NC
Port3	NC
Port4	NC
Port5	NC

USB2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping
USB_OC0#	Port 1
USB_OC1#	Port 2
USB_OC2#	Port 3
USB_OC3#	

SATA DEVSLP[2:0] PIN

Pin	Default Port Mapping
DEVSLP0	DEVSLP Port0
DEVSLP1	DEVSLP Port1 (SSD)
DEVSLP2	DEVSLP Port2

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3.0 Type C
PORT-2	With USB3.0 Conn.
PORT-3	USB3.0 Conn. DB_1
PORT-4	USB3.0 Conn. DB_2
PORT-5	NC
PORT-6	Camera
PORT-7	NC
PORT-8	NC
PORT-9	NC
PORT-10	BT

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+3.3V_RUN [3,5,11,12,13,16,19,22,24,25,26,28,35,36,37,40,46,48,49,51,52]
+3.3V_SUS [3,4,5,11,12,13,15,16,26,28,33,36,39,40,44,45,51]
+1.8V_SUS [12,15,27,28,45,49]
+3.3V_LDO [43]

VGA
SSD
WLAN

CLK_REQ/Strap Pin

+3.3V_RUN
R153 10K/F_2 PCIE_CLKREQ_VGA#
R145 10K/F_2 PCIE_CLKREQ_SSD#

[19] CLK_VGA_N
[19] CLK_VGA_P
[19] PCIE_CLKREQ_VGA#
[26] CLK_PCIE_SSDN
[26] CLK_PCIE_SSDP
[26] PCIE_CLKREQ_SSD#

U20J
CFL_U_43E_IL_IP_DDR4 10 of 20

CLKOUT_PCIE_N_0 AW2
CLKOUT_PCIE_P_0 AY3
GPP_B5/SRCCLKREQ0# CF32
CLKOUT_PCIE_N_1 BC1
CLKOUT_PCIE_P_1 BC2
GPP_B6/SRCCLKREQ1# CE32
CLKOUT_PCIE_N_2 BD3
CLKOUT_PCIE_P_2 BC3
GPP_B7/SRCCLKREQ2# CF30
CLKOUT_PCIE_N_3 BH3
CLKOUT_PCIE_P_3 BH4
GPP_B8/SRCCLKREQ3# CE31
CLKOUT_PCIE_N_4 BA1
CLKOUT_PCIE_P_4 BA2
GPP_B9/SRCCLKREQ4# CE30
CLKOUT_PCIE_N_5 BE1
CLKOUT_PCIE_P_5 BE2
GPP_B10/SRCCLKREQ5# CF31

CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
GPD8/SUSCLK BT32
XTAL_IN CK3
XTAL_OUT CK2
CLK_BIASREF CJ1
CLKIN_XTAL CM3
RTCX1 BN31
RTCX2 BN32
SRTCRST# BR37
RTCRST# BR34

AU1 CK_XDP_N_R
AU2 CK_XDP_P_R
TP53
TP46
SUSCLK_32K [27]
XTAL24_IN
XTAL24_OUT
XCLK_BIASREF
PULSAR_38P4M_REFCLK
R384 60.4/F_2
RTC_X1
RTC_X2
SRTC_RST#
RTC_RST#

2/3 follow CRB

PULSAR_38P4M_REFCLK
PULSAR_38P4M_REFCLK [27]
0525_Intel check
R387 10K_4
Close to CPU

U20I
CFL_U_43E_IL_IP_DDR4 9 of 20

[27] CNV_WR_LANE0_DN CR30
[27] CNV_WR_LANE0_DP CP30
CNV_WR_D0N
CNV_WR_D0P
[27] CNV_WR_LANE1_DN CM30
[27] CNV_WR_LANE1_DP CN30
CNV_WR_D1N
CNV_WR_D1P
[27] CNV_WT_LANE0_DN CN32
[27] CNV_WT_LANE0_DP CM32
CNV_WT_D0N
CNV_WT_D0P
[27] CNV_WT_LANE1_DN CP33
[27] CNV_WT_LANE1_DP CN33
CNV_WT_D1N
CNV_WT_D1P
[27] CNV_WR_CLK_DN CN31
[27] CNV_WR_CLK_DP CP31
CNV_WR_CLKN
CNV_WR_CLKP
[27] CNV_WT_CLK_DN CP34
[27] CNV_WT_CLK_DP CN34
CNV_WT_CLKN
CNV_WT_CLKP
R461 150/F_2
CNV_WT_RCOMP CP32
CNV_WT_RCOMP CR32
CNV_WT_RCOMP_0 CP20
CNV_WT_RCOMP_1 CK19
GPP_F0/CNV_PA_BLANKING CG17
GPP_F1
GPP_F2
[33] NRST#_MCU
GPP_C8/UART0_RXD CR14
GPP_C9/UART0_TXD CP14
GPP_C10/UART0_RTS# CN14
GPP_C11/UART0_CTS# CM14
GPP_F8/CNV_MFUART2_RXD CJ17
GPP_F9/CNV_MFUART2_TXD CH17
GPP_F23 CF17
GPP_F23/A4WP_PRESENT
EMMC_RCOMP

GPP_H18/CPU_C10_GATE# CN27
GPP_H19/TIMESYNC_0 CM27
GPP_H21 CP25
GPP_H22 CN26
GPP_H23 CM26
GPP_F10 CK17
GPD7 BV35
GPP_F3 CN20
GPP_D4/IMGCLKOUT0/BK4/SBK4 CG25
GPP_H20/IMGCLKOUT_1 CH25
GPP_F12/EMMC_DATA0 CR20
GPP_F13/EMMC_DATA1 CM20
GPP_F14/EMMC_DATA2 CN19
GPP_F15/EMMC_DATA3 CM19
GPP_F16/EMMC_DATA4 CN18
GPP_F17/EMMC_DATA5 CR18
GPP_F18/EMMC_DATA6 CP18
GPP_F19/EMMC_DATA7 CM18
GPP_F20/EMMC_RCLK CM16
GPP_F21/EMMC_CLK CP16
GPP_F11/EMMC_CMD CR16
GPP_F22/EMMC_RESET# CN16
EMMC_RCOMP CK15

CPU_C10_GATE# TP64
GPP_H21 R132 4.7K_5%_4
GPP_H23 TP15
GPP_F10 TP58
HW STRAP HIGH-> 24MHz
2/1 follow CRB
3/16 add board ID9 for on board memory
+3.3V_SUS
GPD7
R427 200/F_2

+3.3V_SUS
R533 100K_4
GPD7
R511 *20K_1%_4_NC
XTAL INPUT MODE (HVM Only)
LOW: XTAL INPUT IS SINGLE ENDED
HIGH: XTAL IS ATTACHED
2/3 add for HW STRAP

+1.8V_SUS
R103 *100K_4_NC
GPP_F23
R113 100K_4
2/3 add follow CRB

RTC Clock 32.768KHz

C369 18p/25V_2_H
C368 18p/25V_2_H
Y5 32.768KHZ/20ppm
R189 10M_2
RTC_X1
RTC_X2

RTC Circuitry(RTC)

30mils

RTC Power trace width 20mils.

+BAT_RTC
+3.3V_LDO
D16 SDM20U30-7
R576 20K/F_2
R550 20K/F_2
C704 1u/10V_4_H
C717 1u/10V_4_H
C703 1u/10V_4_H
RTC_RST#
SRTC_RST#
+3.3V_LDO
C712 0.1u/6.3V_2_H

RTC_RST#
[40] EC_RTC_RST
R590 100K_2
Q47 2N7002KW
RTC RESET

External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

XTAL24_IN R386 0_4 XTAL24_IN_R
XTAL24_OUT R385 0_4 XTAL24_OUT_R
C609 27p/25V_2_H
R372 1M/F_2
Y6 24MHZ/20ppm
C608 27p/25V_2_H

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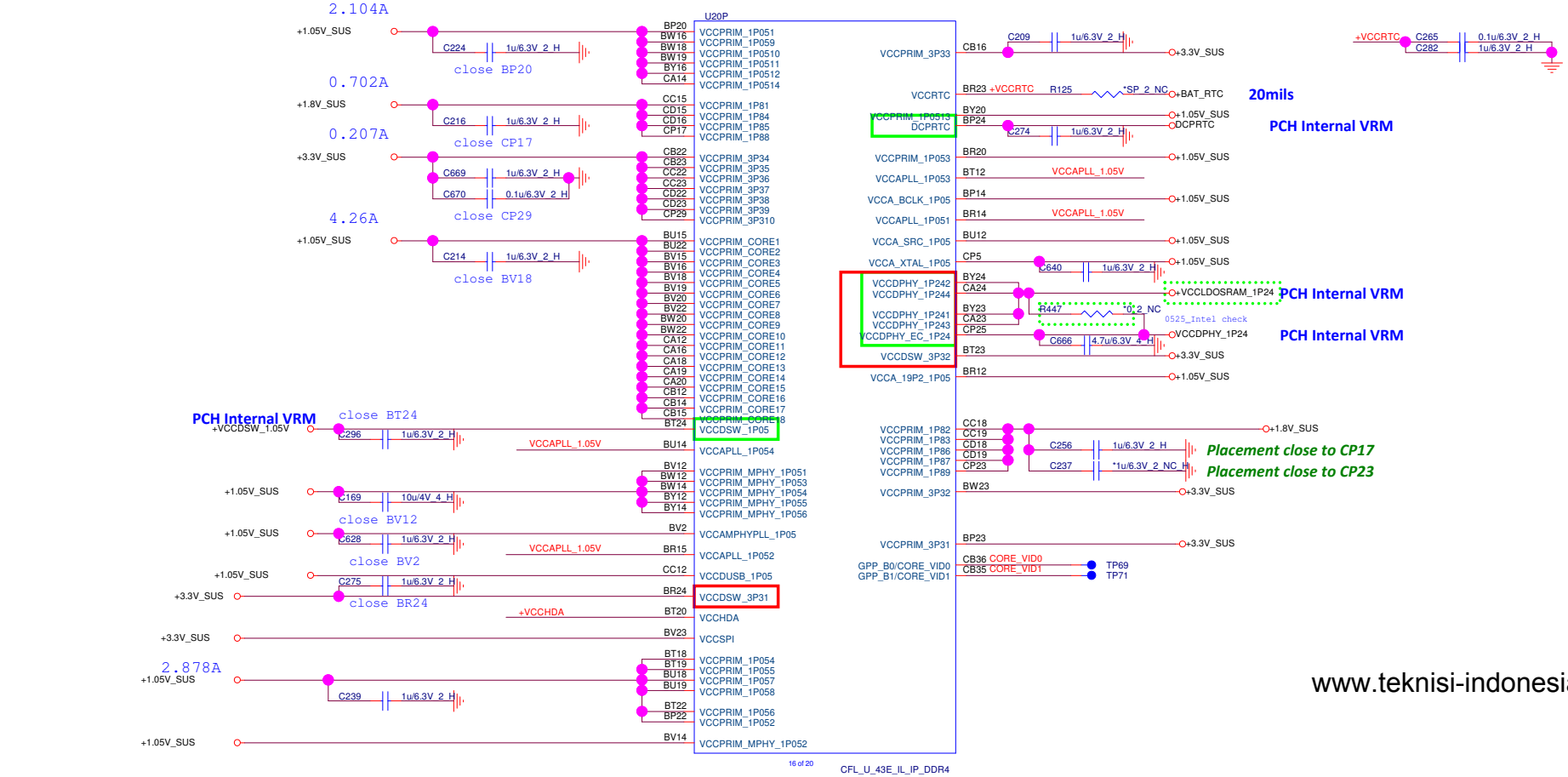
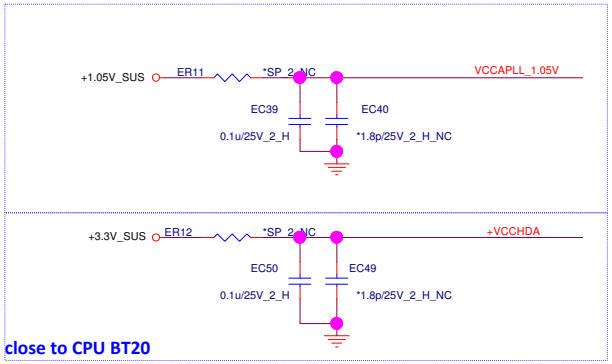
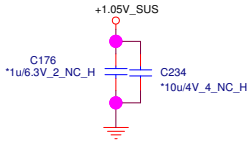
+3.3V_RUN [3,5,11,12,13,14,16,19,22,24,25,26,28,35,36,37,40,46,48,49,51,52]
+3.3V_SUS [3,4,5,11,12,13,14,16,26,28,33,36,39,40,44,45,51]
+1.8V_SUS [12,14,27,28,45,49]
+BAT_RTC [5,14]







Quanta Computer Inc.
PROJECT : H97M

Size	Document Number	Rev
	CML-U 14/15(PCH POWER)	3A

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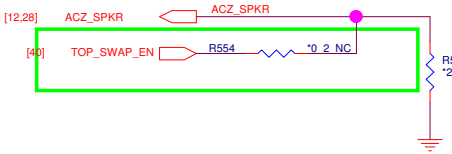
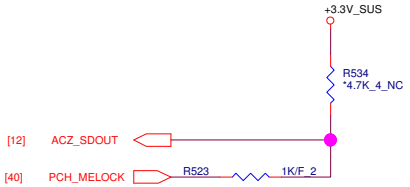
+3.3V_SUS [3,4,5,11,12,13,14,15,26,28,33,36,39,40,44,45,51]
+3.3V_RUN [3,5,11,12,13,14,19,22,24,25,26,28,35,36,37,40,46,48,49,51,52]

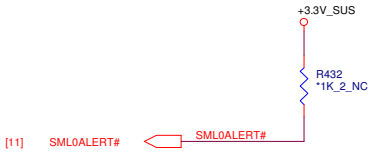
Functional Strap Definitions



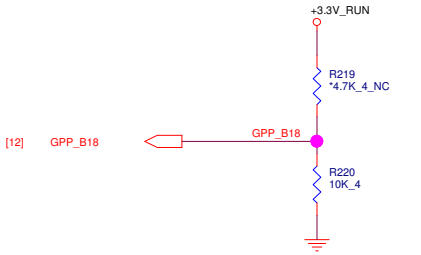
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



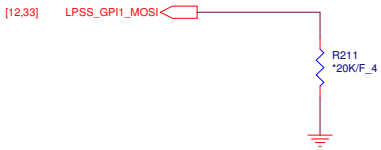
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

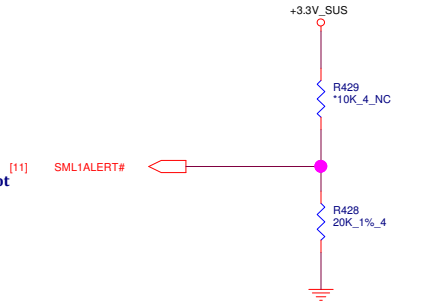


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

Quanta Computer Inc.
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Size	Document Number	Rev
	CML-U 15/15(Straps)	3A

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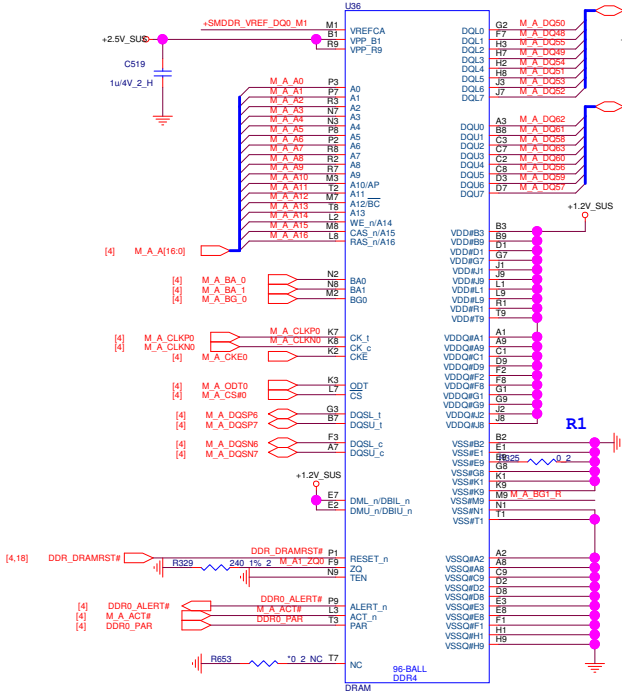
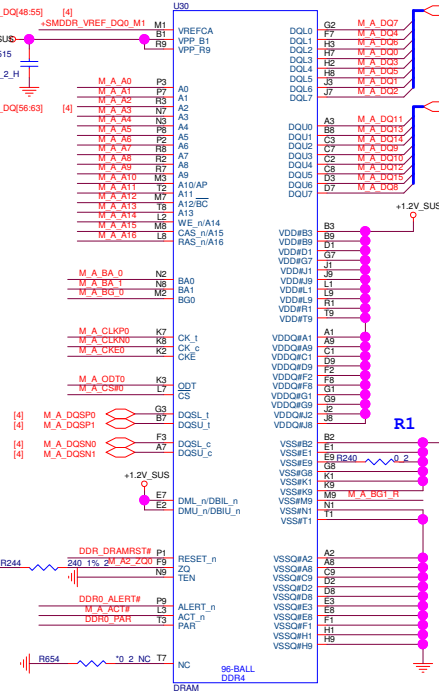
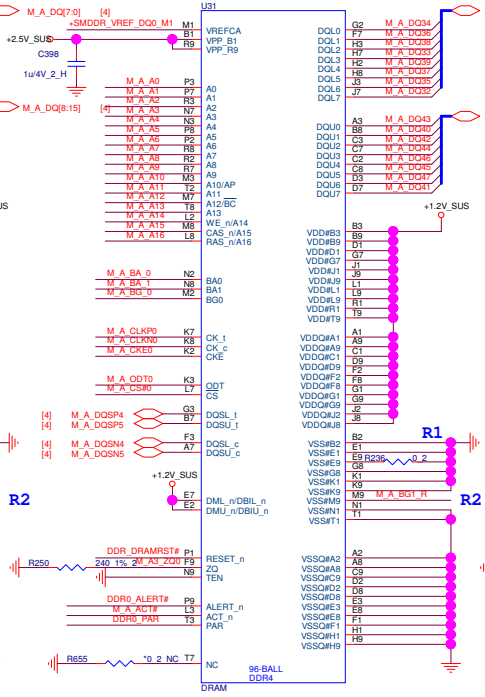
BYTE6_48-55
BYTE7_56-63



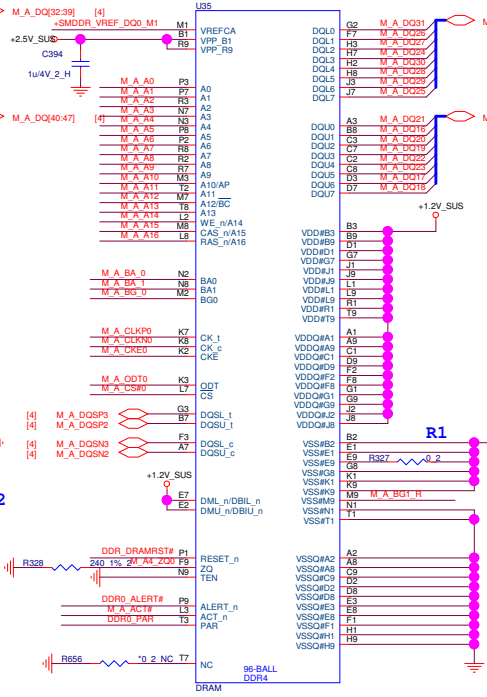
BYTE0_0-7
BYTE1_8-15



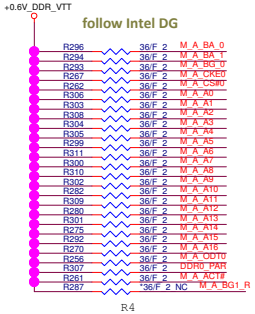
BYTE4_32-39
BYTE5_40-47



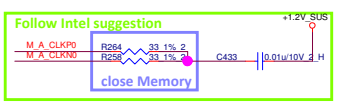
BYTE3_24-31
BYTE2_16-23

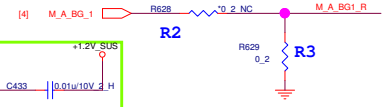


follow Intel DG



Follow Intel suggestion



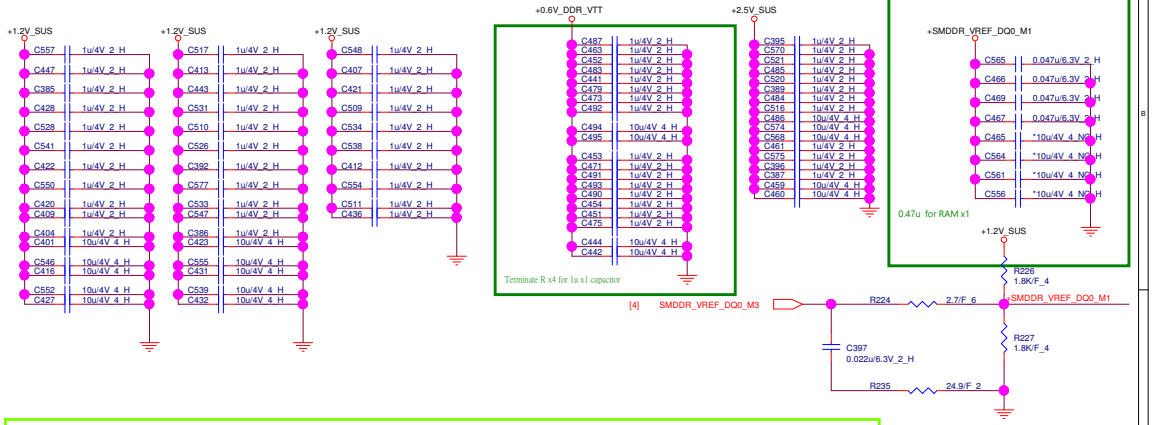


Option for 16Gbx16 die
Close DDR ball

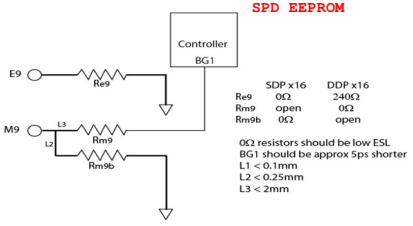
Memory 8G & Memory 16G TABLE

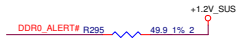
	SDP 8G	DDP 16G
R1	0Ω CS00001JE18	240Ω CS12401FE00
R2	UNINSTAL	INSTAL
R3	INSTAL	UNINSTAL
R4	UNINSTAL	INSTAL
T7	UNINSTAL	INSTAL

Place these Caps near Channel A Memory



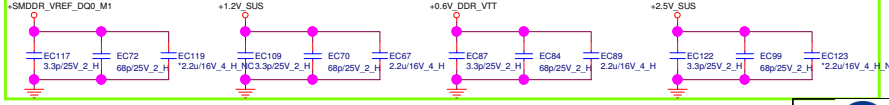
SPD EEPROM

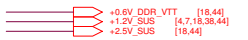




Vendor	P/N	Vendor P/N
Hynix 8G		H5AN8G6NCJR-VK
SAMSUNG 8G		K4A8G165WC-BCTD
Micron 8G		MT40A512M16LY-075:E
NANYA 8G		NT5AD512M16A4-HR
Hynix 16G		H5ANAG6NCMR-VK
SAMSUNG 16G		K4AAG165WB-MCTDT00
Micron 16G		MT40A1G16KNR-075:E

RF





Quanta Computer Inc.
PROJECT : H97M

Size	Document Number	Rev
	DDR4_A	3A

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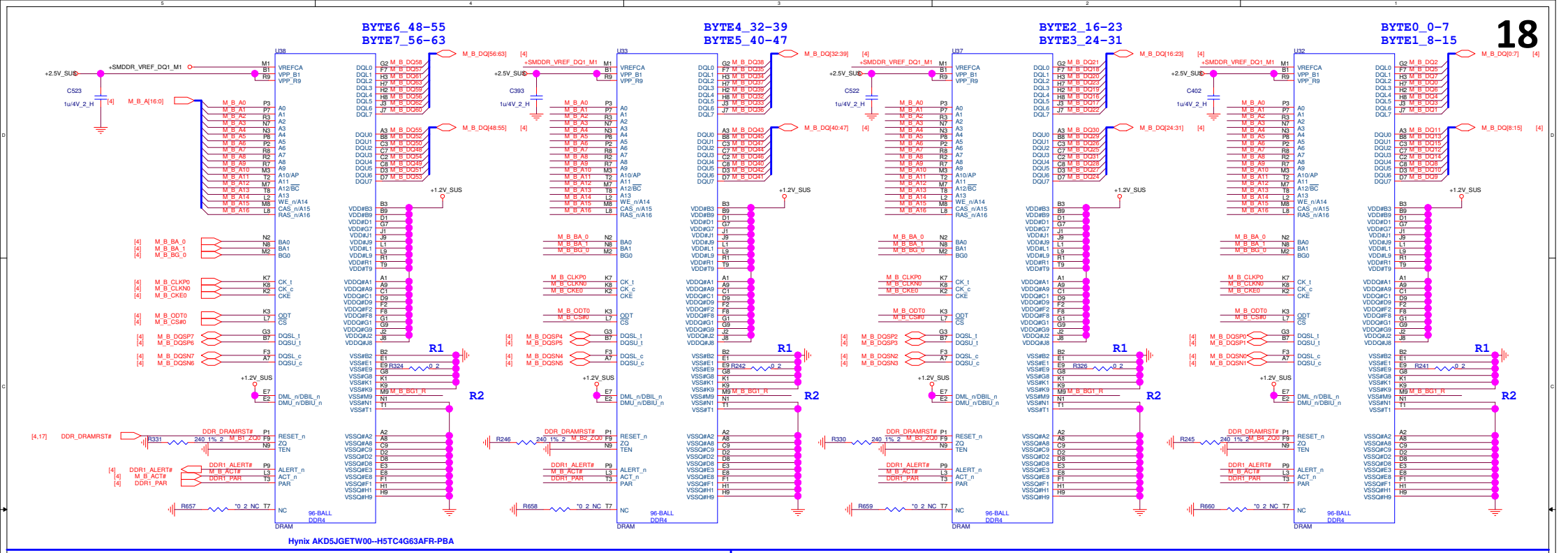
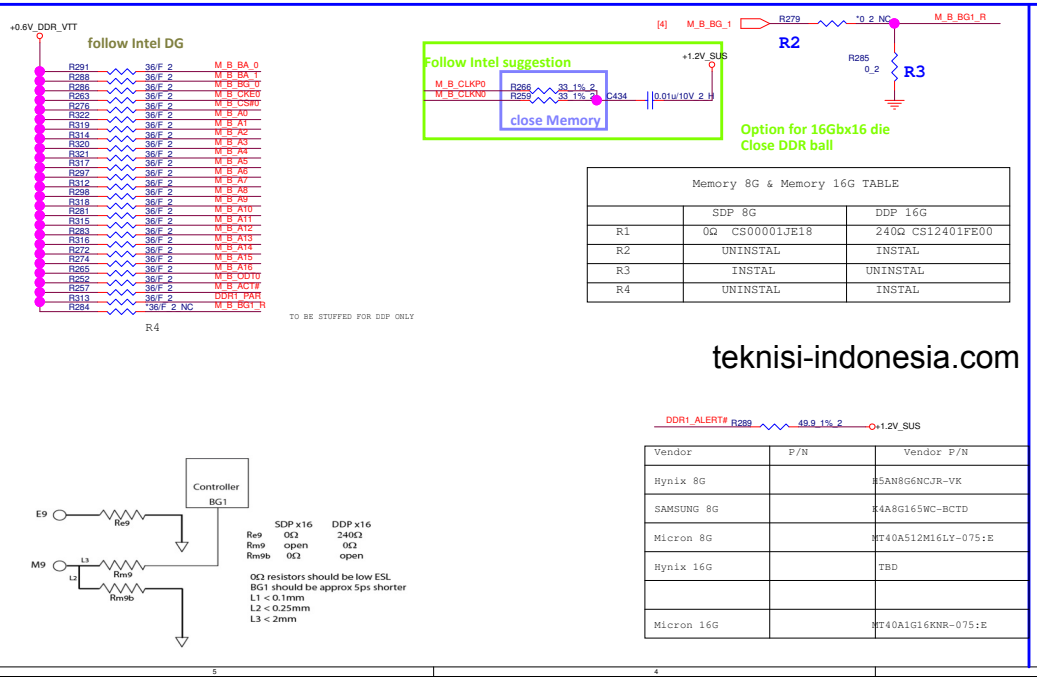
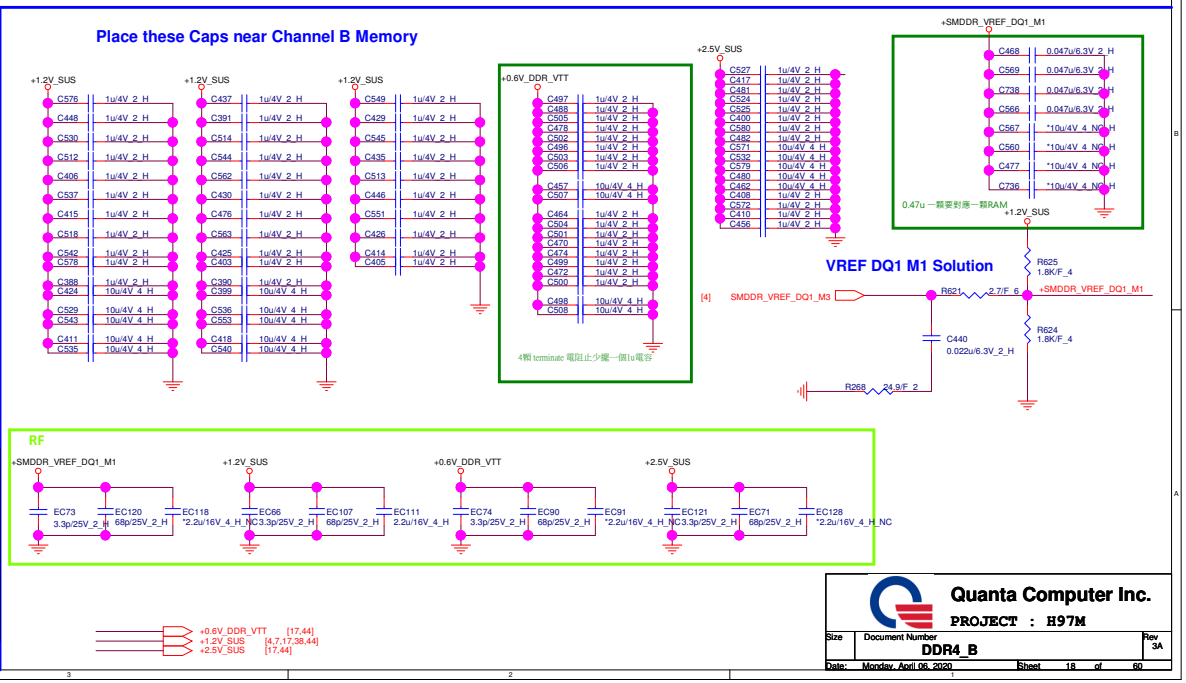




Memory 8G & Memory 16G TABLE		
	SDP 8G	DDP 16G
R1	0Ω CS00001JE18	240Ω CS12401FE00
R2	UNINSTAL	INSTAL
R3	INSTAL	UNINSTAL
R4	UNINSTAL	INSTAL

Vendor	P/N	Vendor P/N
Hynix 8G		H5AN8G6NCJR-VK
SAMSUNG 8G		K4A8G165WC-BCTD
Micron 8G		MT40A512M16LY-075:E
Hynix 16G		TBD
Micron 16G		MT40A1G16KNR-075:E



Quanta Computer Inc.	
PROJECT : H97M	
Size	Document Number: DDR4_B
Rev	3A
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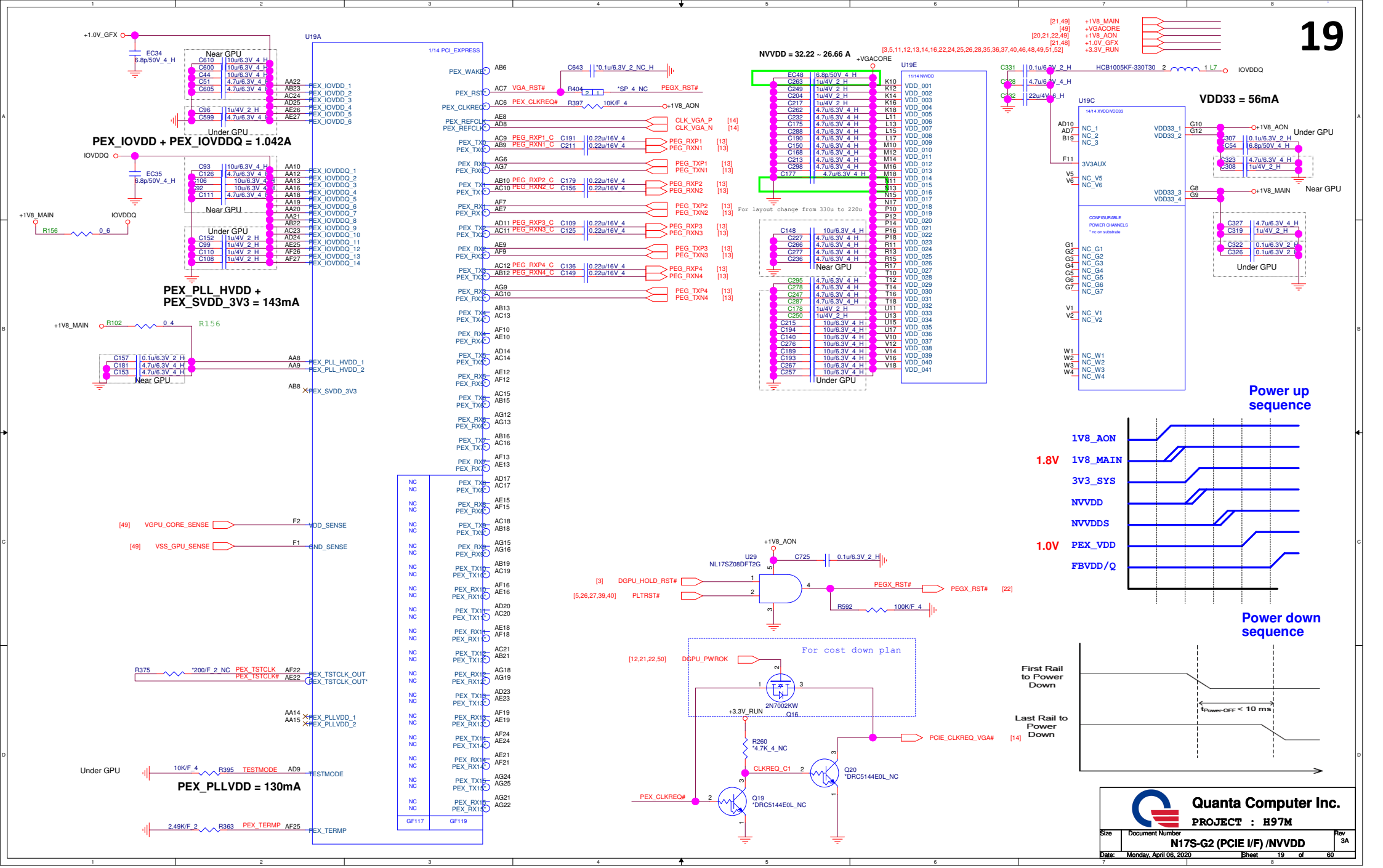
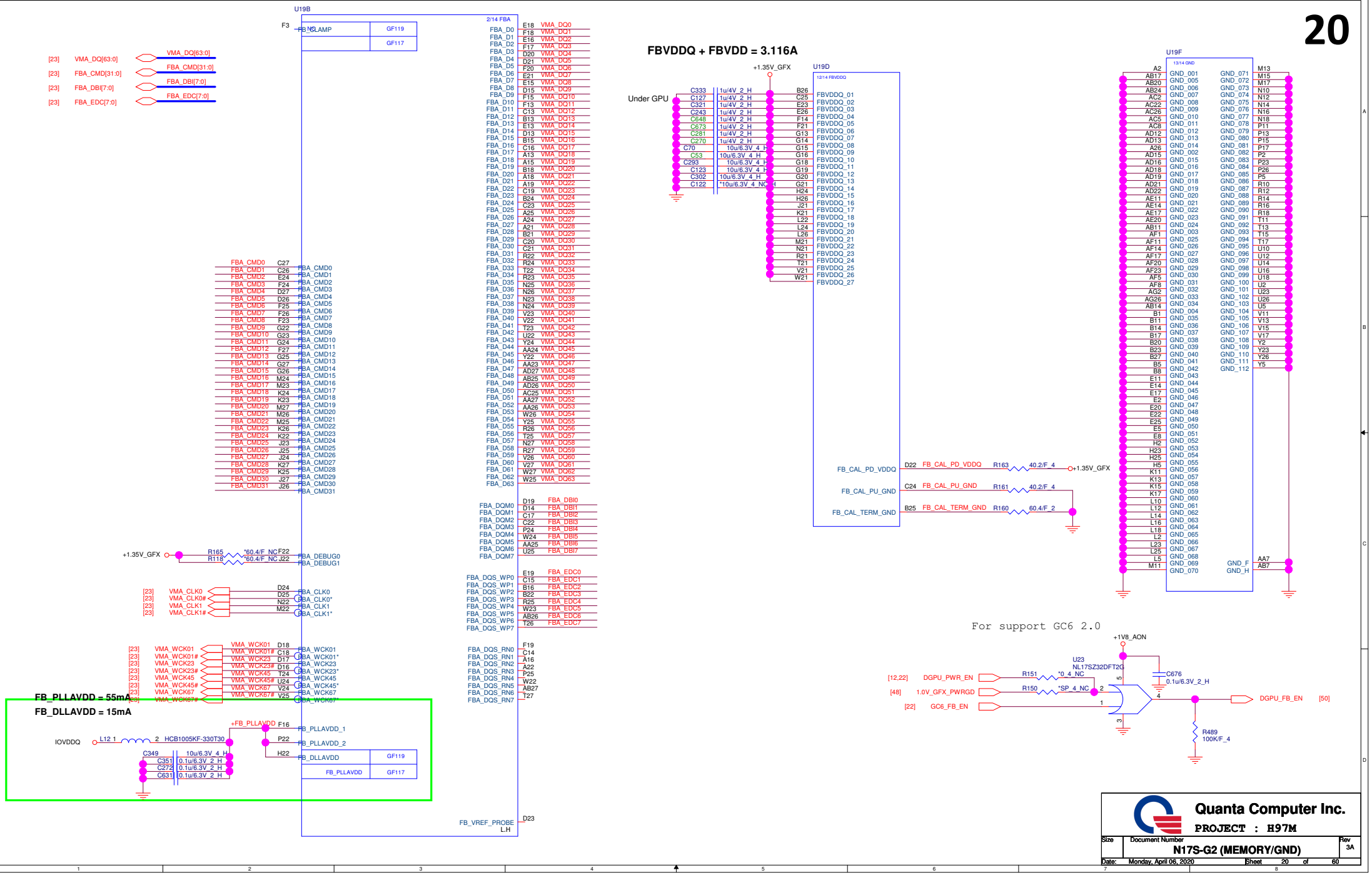

PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
NVVDD = 32.22 ~ 66.6 A
VDD33 = 56mA
Power up sequence
1V8_AON
1V8_MAIN
3V3_SYS
NVVDD
NVVDDS
PEX_VDD
FBVDD/Q
1.8V
1.0V
Power down sequence
First Rail to Power Down
Last Rail to Power Down
tPower-OFF < 10 ms
For cost down plan
Quanta Computer Inc.
PROJECT : H97M
N17S-G2 (PCIE I/F) /NVVDD
Monday, April 06, 2020

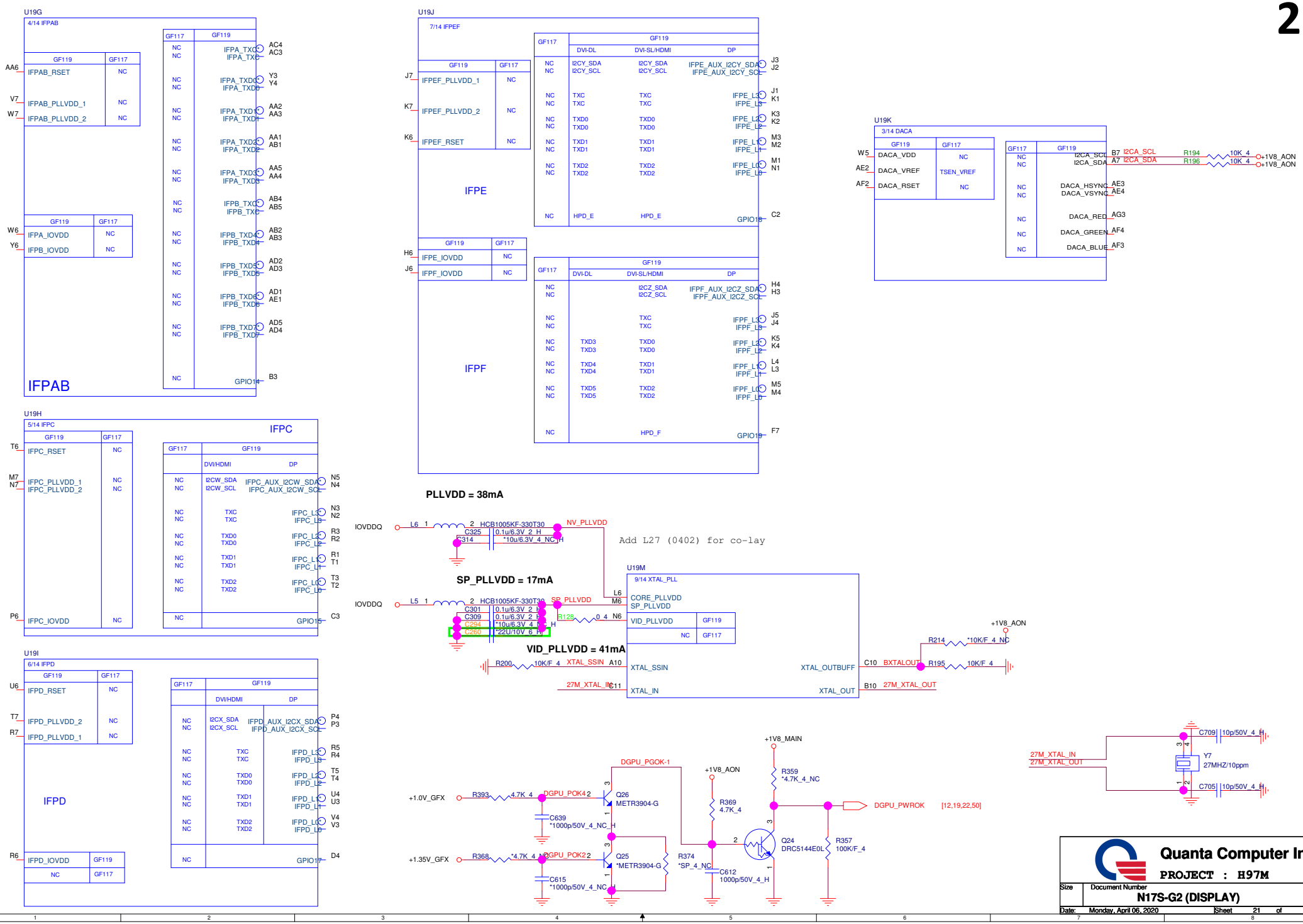


Quanta Computer Inc.

PROJECT : H97M

Size	Document Number	Rev
	N17S-G2 (MEMORY/GND)	3A

Date: Monday, April 06, 2020 Sheet 20 of 60



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Size	Document Number	Rev
	N17S-G2 (DISPLAY)	3A

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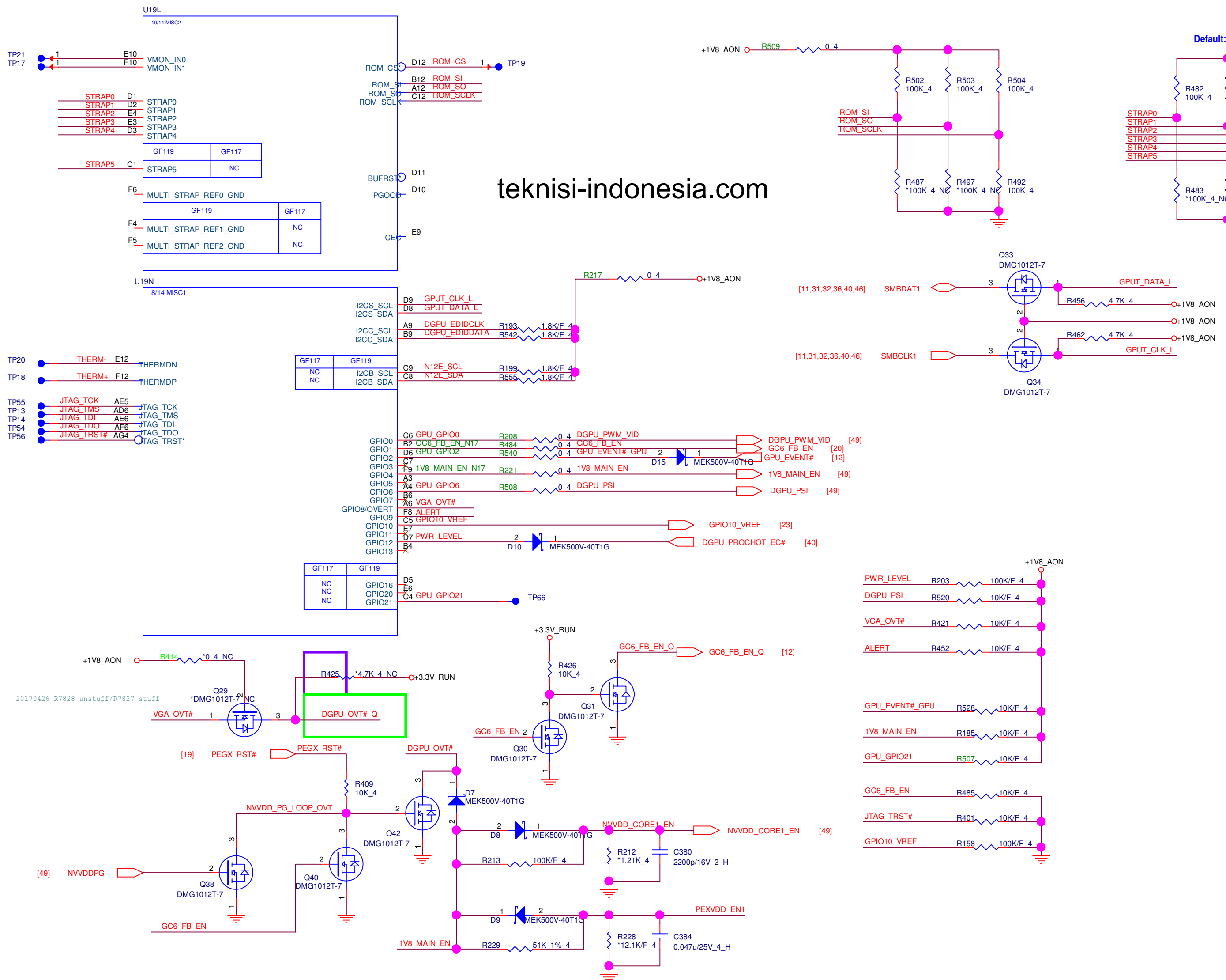
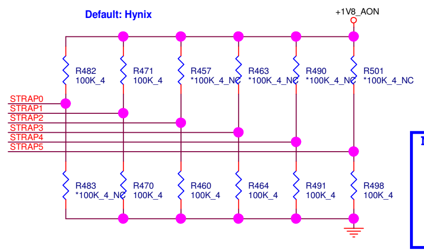




N17 Strap setting

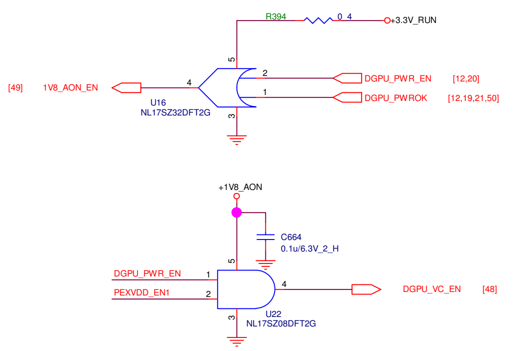
```
ROM_SI    = Stuff 100K Pull Up    CS41002JB20
ROM_SO    = Stuff 100K Pull Up    CS41002JB20
ROM_SCLK  = Stuff 100K Pull Up and 100K Pull Down

STRAP1    = VRAM TABLE
STRAP2    = VRAM TABLE
STRAP3    = VRAM TABLE
STRAP4    = Stuff 100K Pull Down  CS41002JB20
STRAP5    = Stuff 100K Pull Down  CS41002JB20
STRAP6    = Stuff 100K Pull Down  CS41002JB20
```

Memory Density	Config.	Vendor	V'PN	Die Revisoin	Strap
8Gb	256Mx32	MICRON	MT51J256M32HF-80:B	B-die	0x9
		HYNIX	H5GC8H24AJR-R2C	A-die	0xA
		SAMSUNG	K4G80325FC-HC25	C-die	0xB

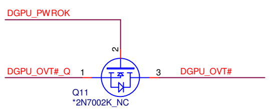
Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)



NVVDD POWER GOOD LOOPBACK

Overt temp ckt for NVVDD and NVVDDS



Quanta Computer Inc.

PROJECT : H97M

Size	Document Number	Rev
	N17S-G2 (GPIO/STRAPS)	3A
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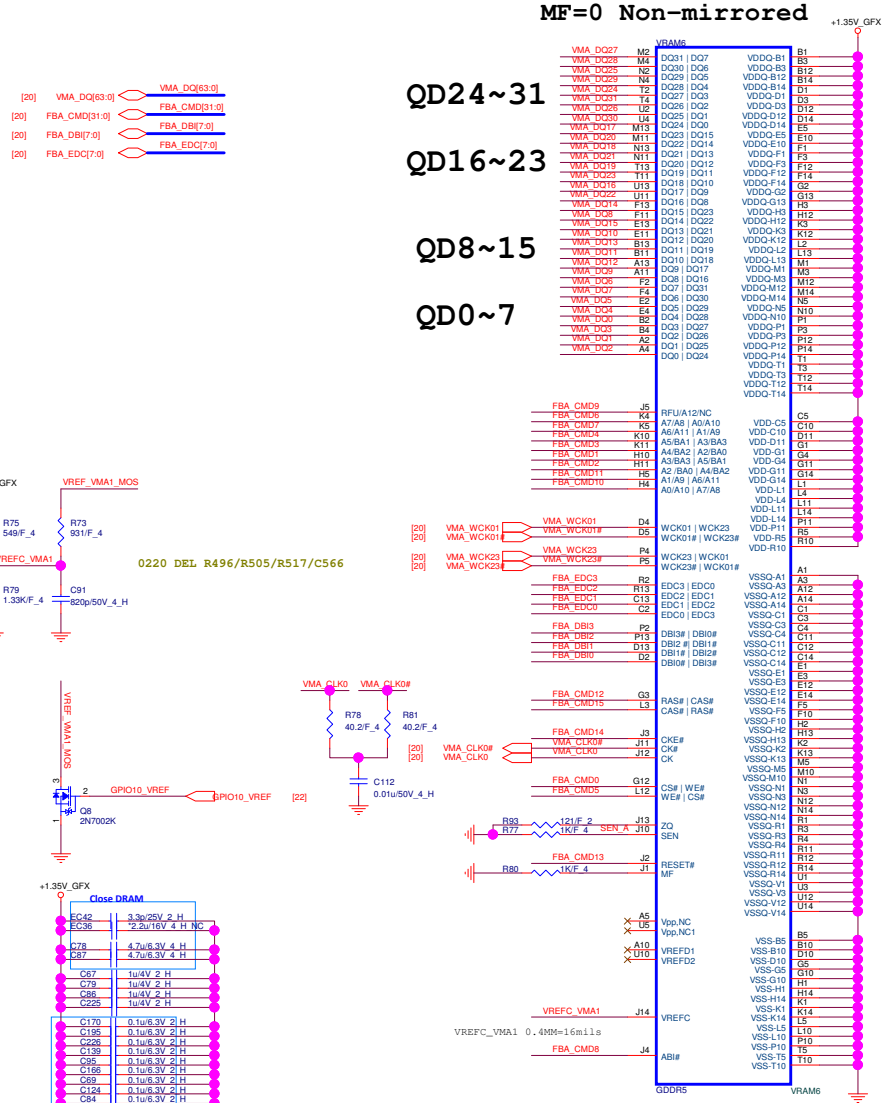
CHANNEL A: 2G GDDR5

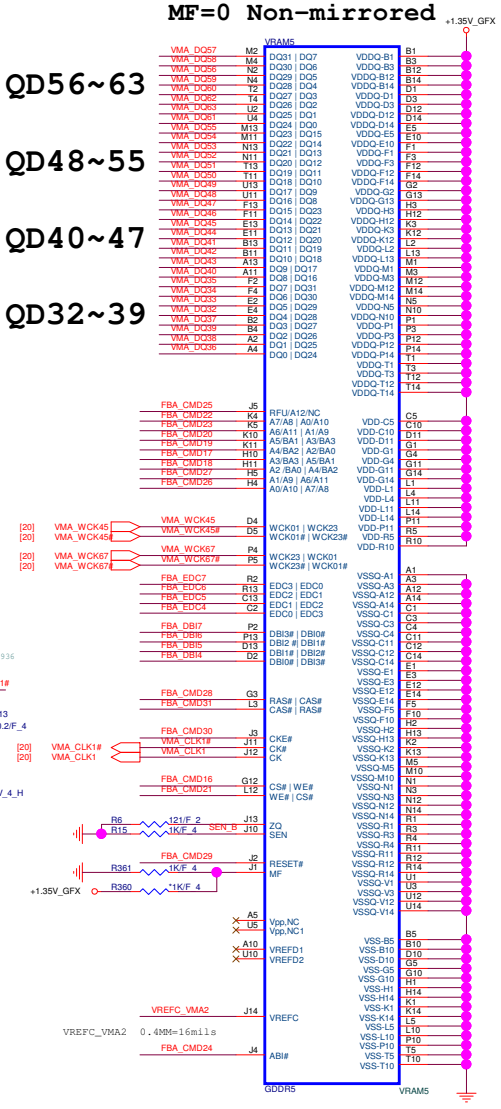
MF=0 Non-mirrored

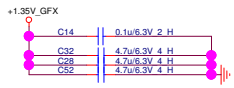
QD24~31
QD16~23
QD8~15
QD0~7

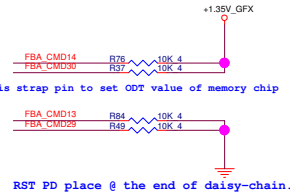


MF=0 Non-mirrored

QD56~63
QD48~55
QD40~47
QD32~39







GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

GDDR5 CMD Mapping Table
<0..31> <32..63> MEMORY

12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	ABI*
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
13	29	RESET*
14	30	CKE*

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	GDDR5x32-VRAM	3A

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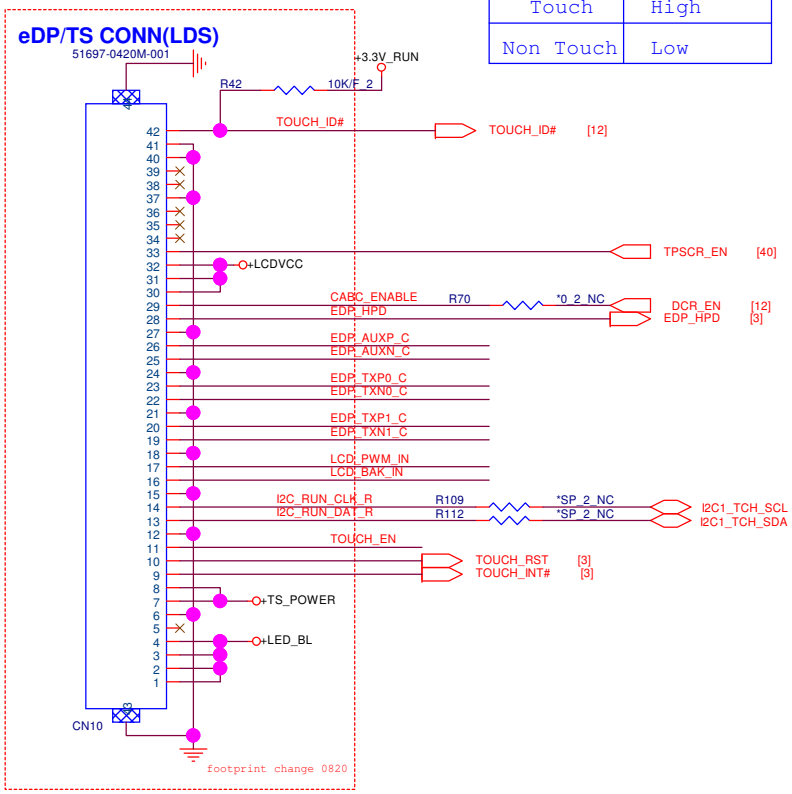
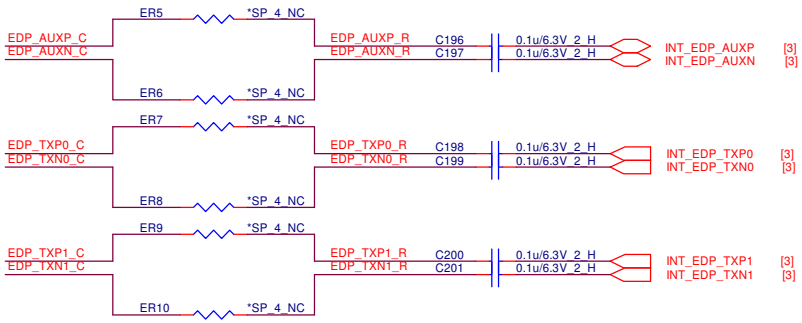
eDP

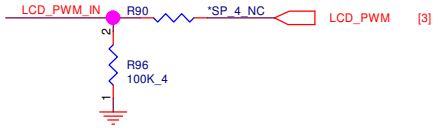
	TOUCH_ID#
Touch	High
Non Touch	Low

eDP/TS CONN(LDS)

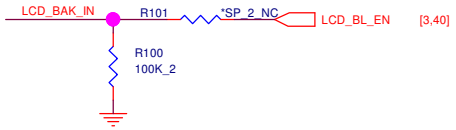




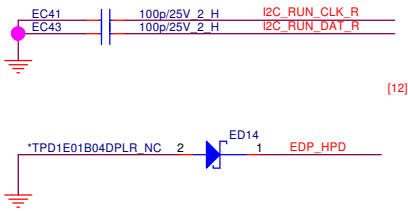
Backlight Control(LDS)



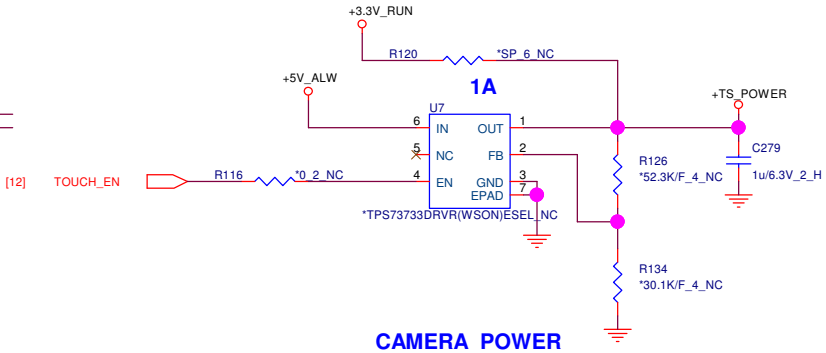
Backlight Enable(LDS)

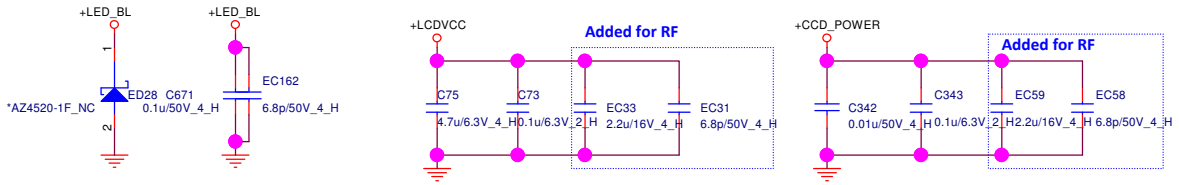


Touch screen I2C I/F

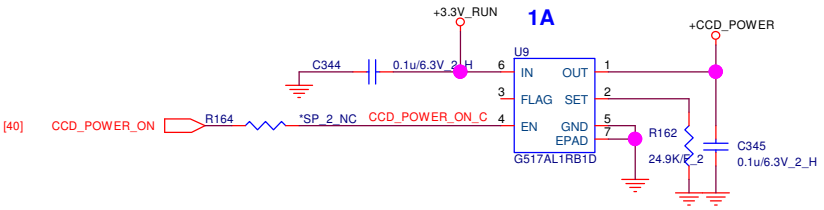


TOUCH Panel POWER

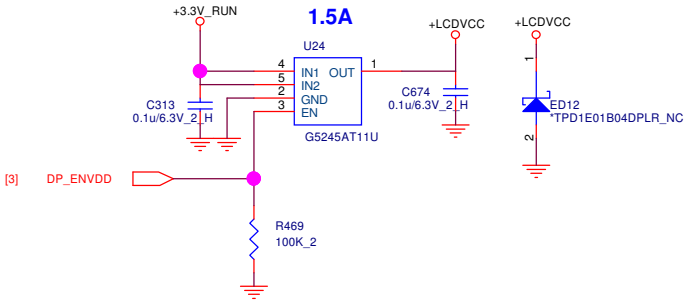




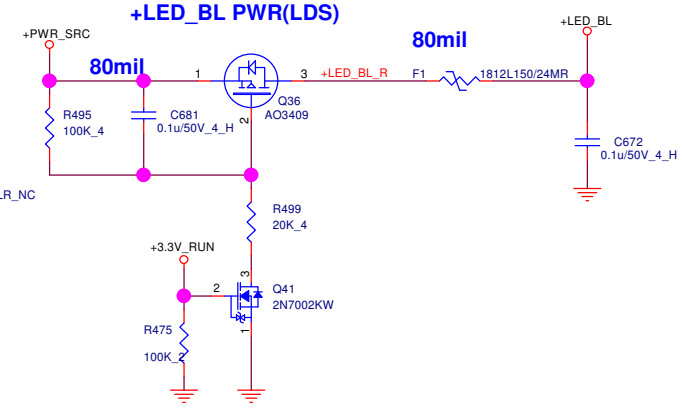
CAMERA POWER

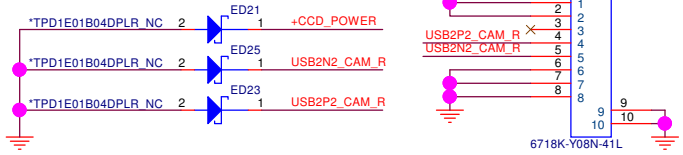


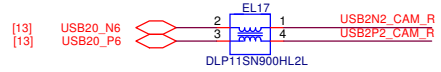
+LCD_VCC PWR(LDS)



+LED_BL PWR(LDS)







Quanta Computer Inc.

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	eDP / Camera	3A
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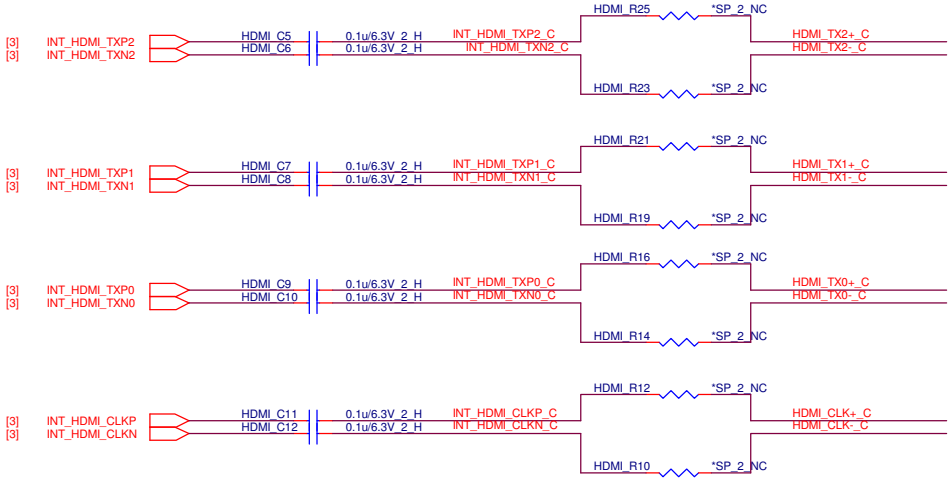
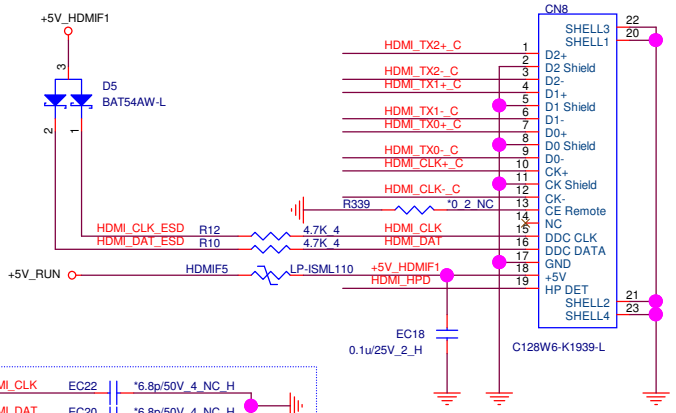
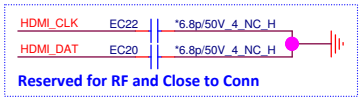
HDMI

+3.3V_RUN [3,5,11,12,13,14,16,19,22,24,26,28,35,36,37,40,46,48,49,51,52]
+5V_RUN [26,28,37,48,49,50,51,52]

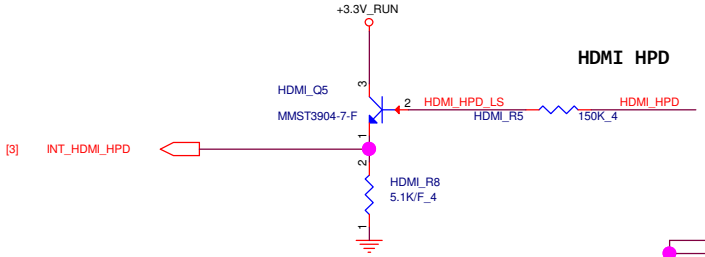


HDMI Conn.(HDM)

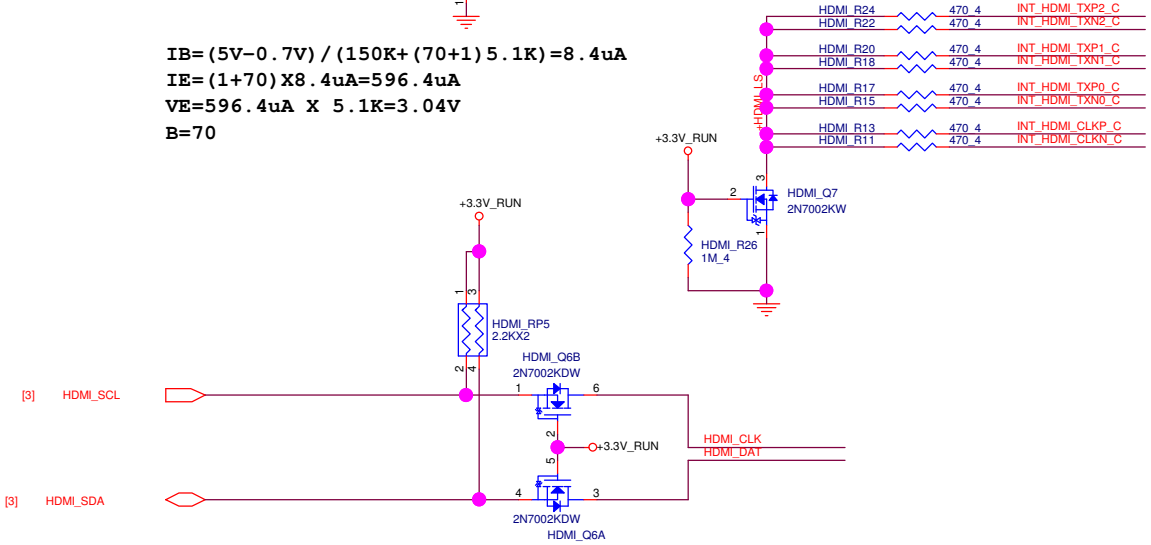




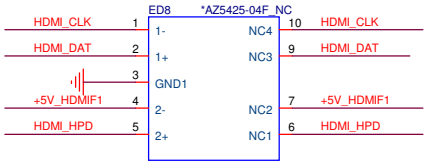
HDMI_HPD spec VinH_min=2.0V

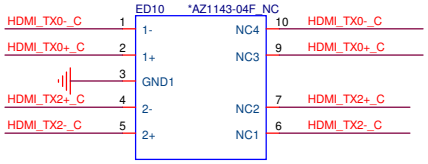


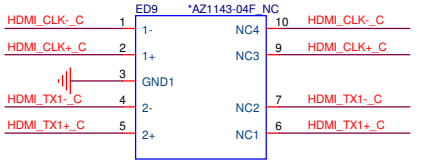
IB=(5V-0.7V)/(150K+(70+1)5.1K)=8.4uA
IE=(1+70)X8.4uA=596.4uA
VE=596.4uA X 5.1K=3.04V
B=70



ESD Function for HDMI







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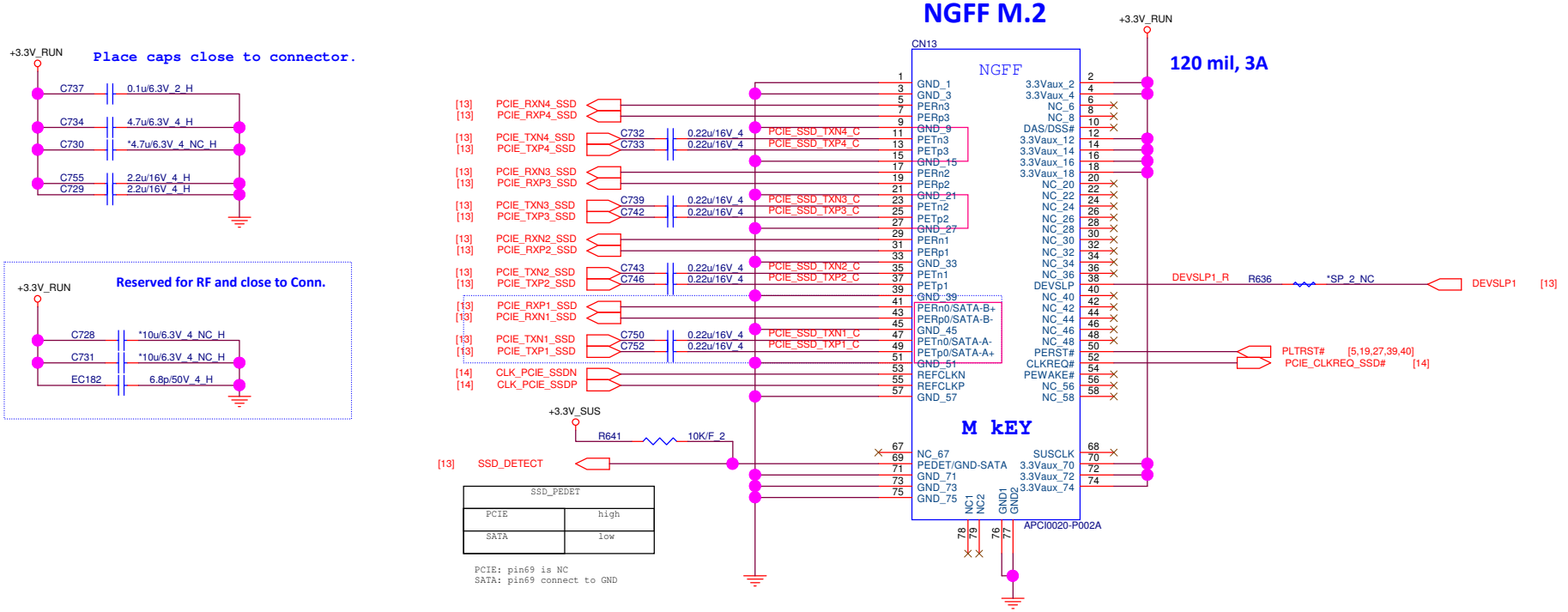
NGFF M.2



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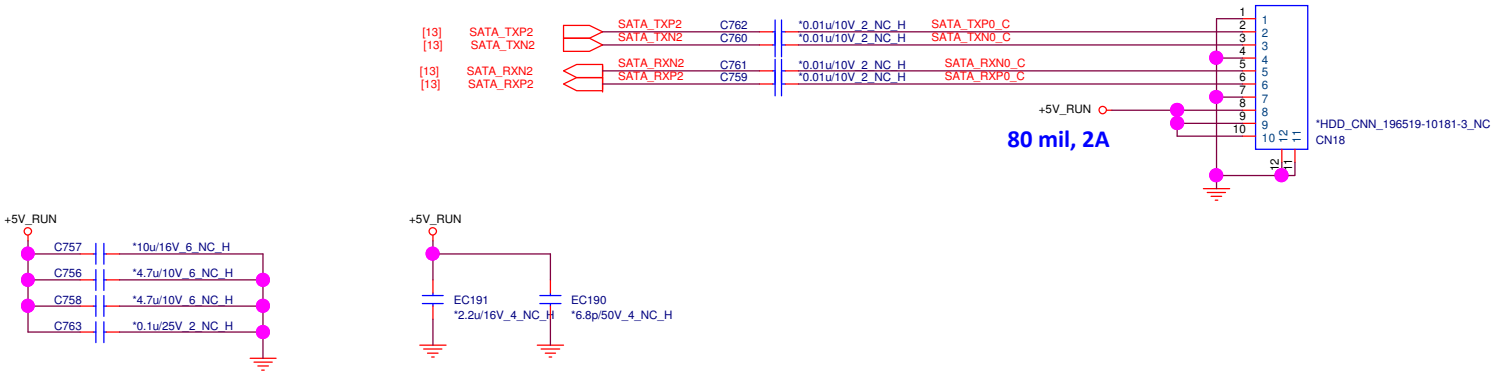
SATA HDD Connector 20pin(HDD)



Quanta Computer Inc.		
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Size	Document Number: PCIe SSD(NGFF)	Rev: 3A
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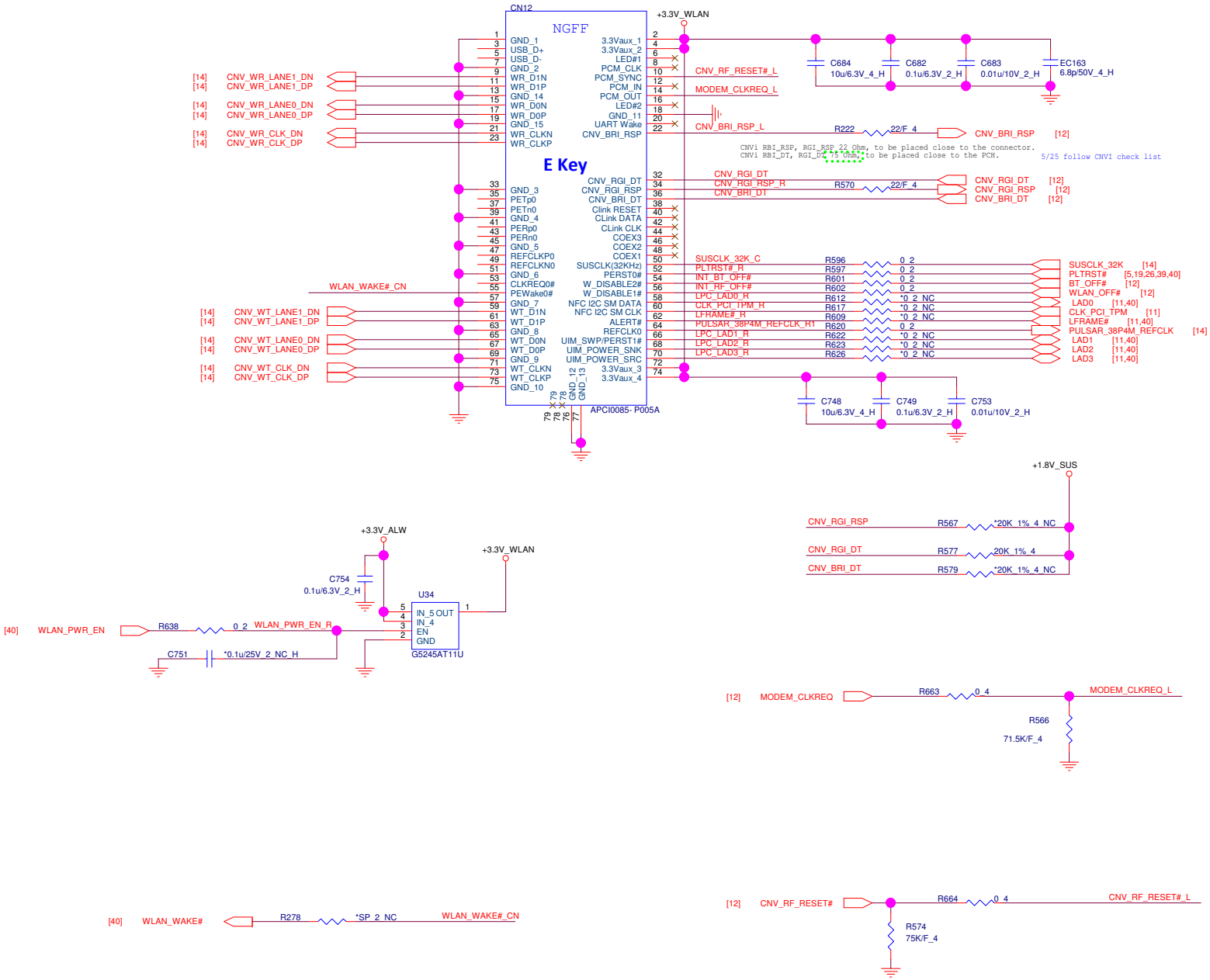
WLAN/BT



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Size	Document Number: WLAN/BT — Rev: 3A
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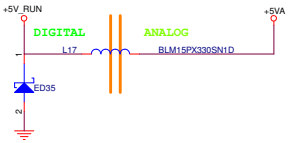
CODEC (ALC256)

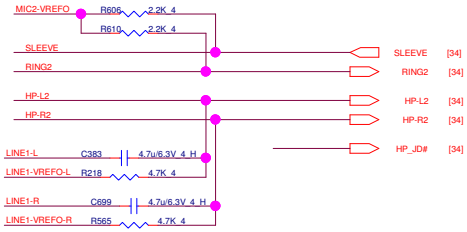
Codec PWR 5V(ADO)

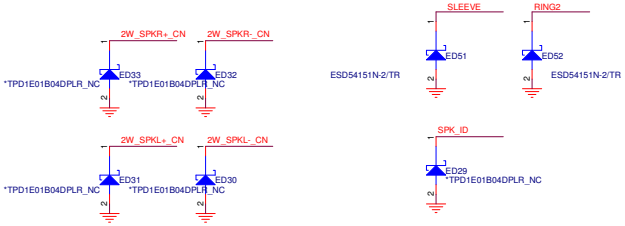


ALC255/ALC256

Codec PWR 1.8V(ADO)

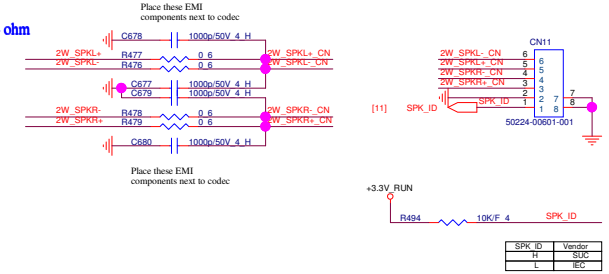
HEADPHONE/MIC/LINE combo (ADO)



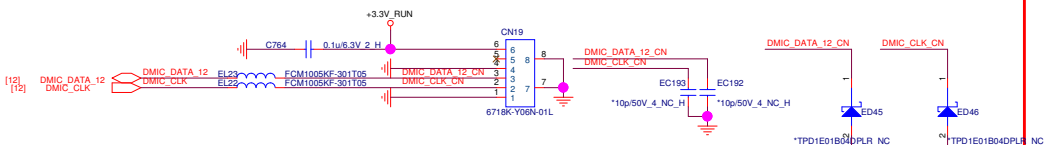


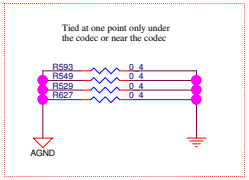
trace width of SLEEVE & RING2 are required at least 40mil and its length should be asshort as possible

2W 4 ohm



DMIC





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Size	Document Number: Codec ALC255/ALC256	Rev 3A
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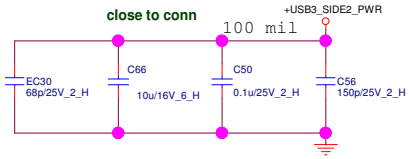
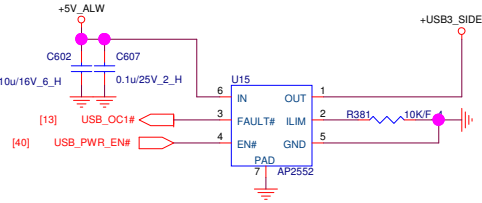
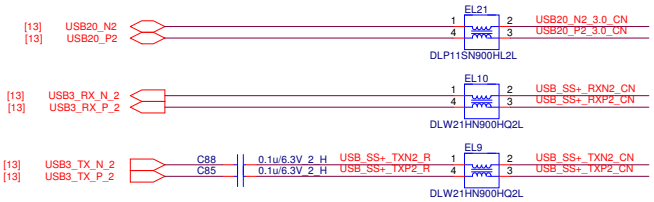
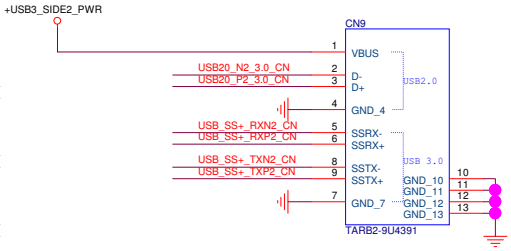
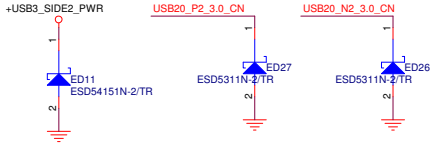
USB3.0/2.0 COMBO





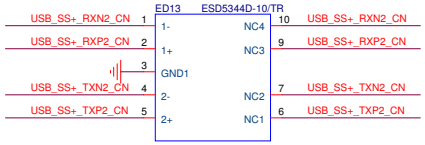






ESD Function for USB3.0

Need closed to CNN



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Size	Document Number	Rev
	USB3.0	3A
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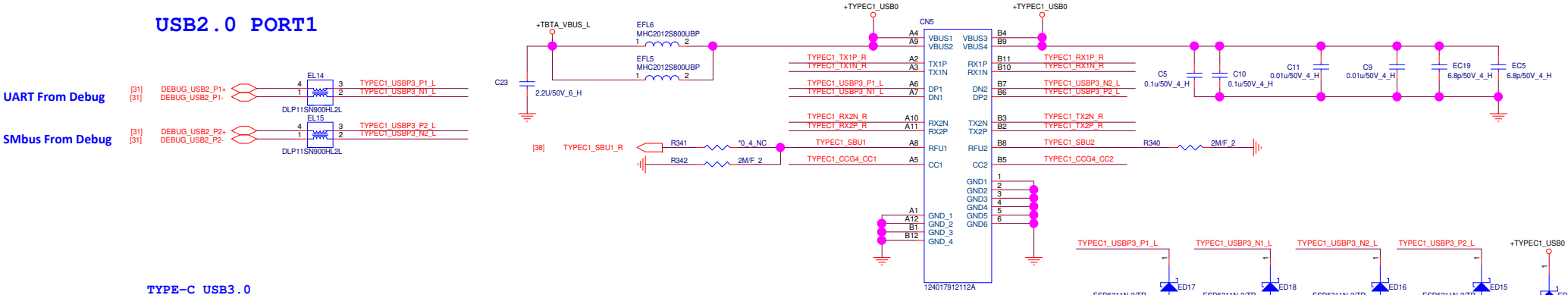
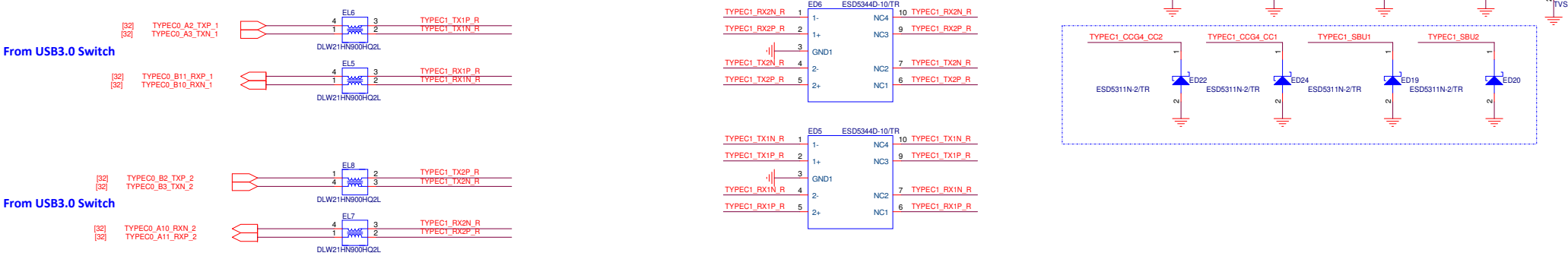
USB TYPE C Connector

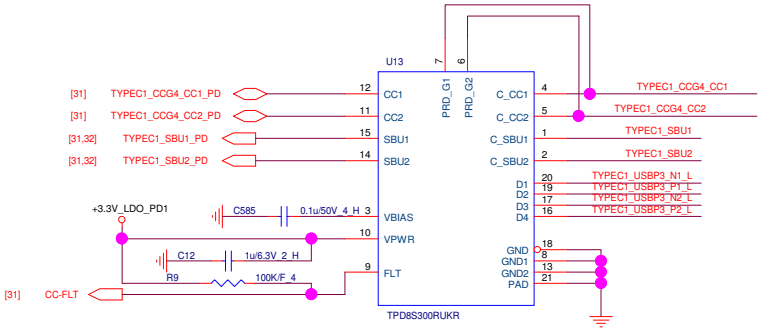
USB2.0 PORT1



TYPE-C USB3.0



type-c short-Vbus and CC protection



Quanta Computer Inc.

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	USB TYPE-C (1/3)	3A

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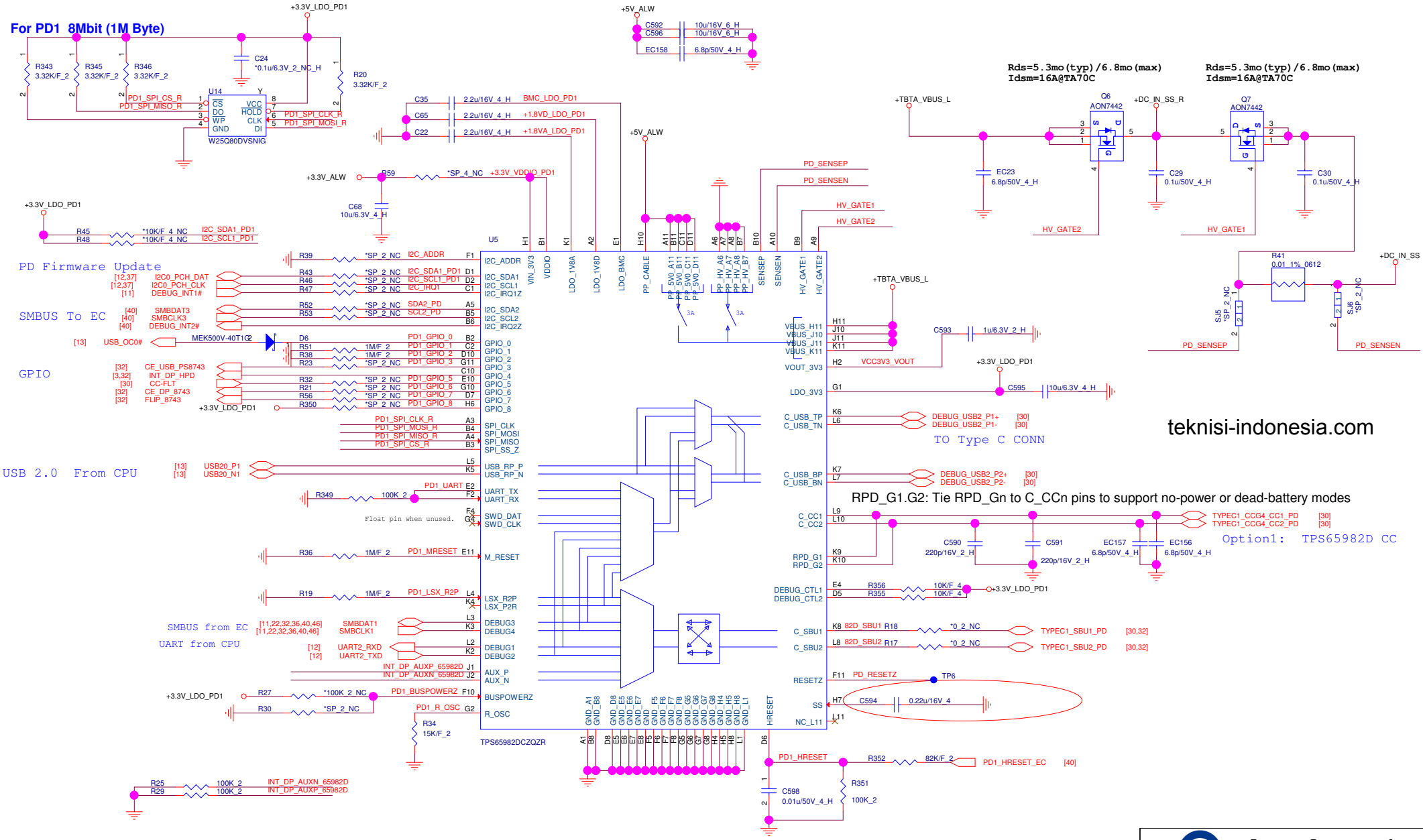
For PD1 8Mbit (1M Byte)
+3.3V_LDO_PD1
U14
W25Q80DVSNIG
PD1_SPI_CS_R
PD1_SPI_MISO_R
PD1_SPI_CLK_R
PD1_SPI_MOSI_R
R343 3.32K/F_2
R345 3.32K/F_2
R346 3.32K/F_2
C24 *0.1u/6.3V_2_NC_H
R20 3.32K/F_2
+5V_ALW
C592 10u/16V_6_H
C596 10u/16V_6_H
EC158 6.8p/50V_4_H
C35 2.2u/16V_4_H BMC_LDO_PD1
C65 2.2u/16V_4_H +1.8VD_LDO_PD1
C22 2.2u/16V_4_H +1.8VA_LDO_PD1
R59 *SP_4_NC +3.3V_VDDIO_PD1
C68 10u/6.3V_4_H
R45 *10K/F_4_NC I2C_SDA1_PD1
R48 *10K/F_4_NC I2C_SCL1_PD1
U5
PD Firmware Update
SMBUS To EC
GPIO
USB 2.0 From CPU
SMBUS from EC
UART from CPU
I2C_ADDR
I2C_SDA1
I2C_SCL1
I2C_IRQ1Z
I2C_SDA2
I2C_SCL2
I2C_IRQ2Z
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SS_Z
USB_RP_P
USB_RP_N
UART_TX
UART_RX
SWD_DAT
SWD_CLK
M_RESET
LSX_R2P
LSX_P2R
DEBUG3
DEBUG4
DEBUG1
DEBUG2
AUX_P
AUX_N
BUSPOWERZ
R_OSC
TPS65982DCZQZR
PD_SENSEP
PD_SENSEN
HV_GATE1
HV_GATE2
VBUS_H11
VBUS_J10
VBUS_J11
VBUS_K11
VOUT_3V3
LDO_3V3
C_USB_TP
C_USB_TN
C_USB_BP
C_USB_BN
C_CC1
C_CC2
RPD_G1
RPD_G2
DEBUG_CTL1
DEBUG_CTL2
C_SBU1
C_SBU2
RESETZ
SS
NC_L11
HRESET
+TBTA_VBUS_L
VCC3V3_VOUT
DEBUG_USB2_P1+
DEBUG_USB2_P1-
DEBUG_USB2_P2+
DEBUG_USB2_P2-
TO Type C CONN
RPD_G1.G2: Tie RPD_Gn to C_CCn pins to support no-power or dead-battery modes
Option1: TPS65982D CC
TYPEC1_CCG4_CC1_PD
TYPEC1_CCG4_CC2_PD
TYPEC1_SBU1_PD
TYPEC1_SBU2_PD
PD1_RESETZ
TP6
C594 0.22u/16V_4
PD1_HRESET
PD1_HRESET_EC
C598 0.01u/50V_4_H
R351 100K_2
R352 82K/F_2
Rds=5.3mo(typ)/6.8mo(max)
Idsm=16A@TA70C
Q6 AON7442
Q7 AON7442
EC23 6.8p/50V_4_H
C29 0.1u/50V_4_H
C30 0.1u/50V_4_H
+DC_IN_SS_R
+DC_IN_SS
R41 0.01_1%_0612
C593 1u/6.3V_2_H
C595 10u/6.3V_4_H
C590 220p/16V_2_H
C591 220p/16V_2_H
EC157 6.8p/50V_4_H
EC156 6.8p/50V_4_H
R356 10K/F_4
R355 10K/F_4
R18 *0_2_NC
R17 *0_2_NC
R349 100K_2
R36 1M/F_2
R19 1M/F_2
R27 *100K_2_NC
R30 *SP_2_NC
R34 15K/F_2
R25 100K_2
R29 100K_2
INT_DP_AUXN_65982D
INT_DP_AUXP_65982D
Float pin when unused.
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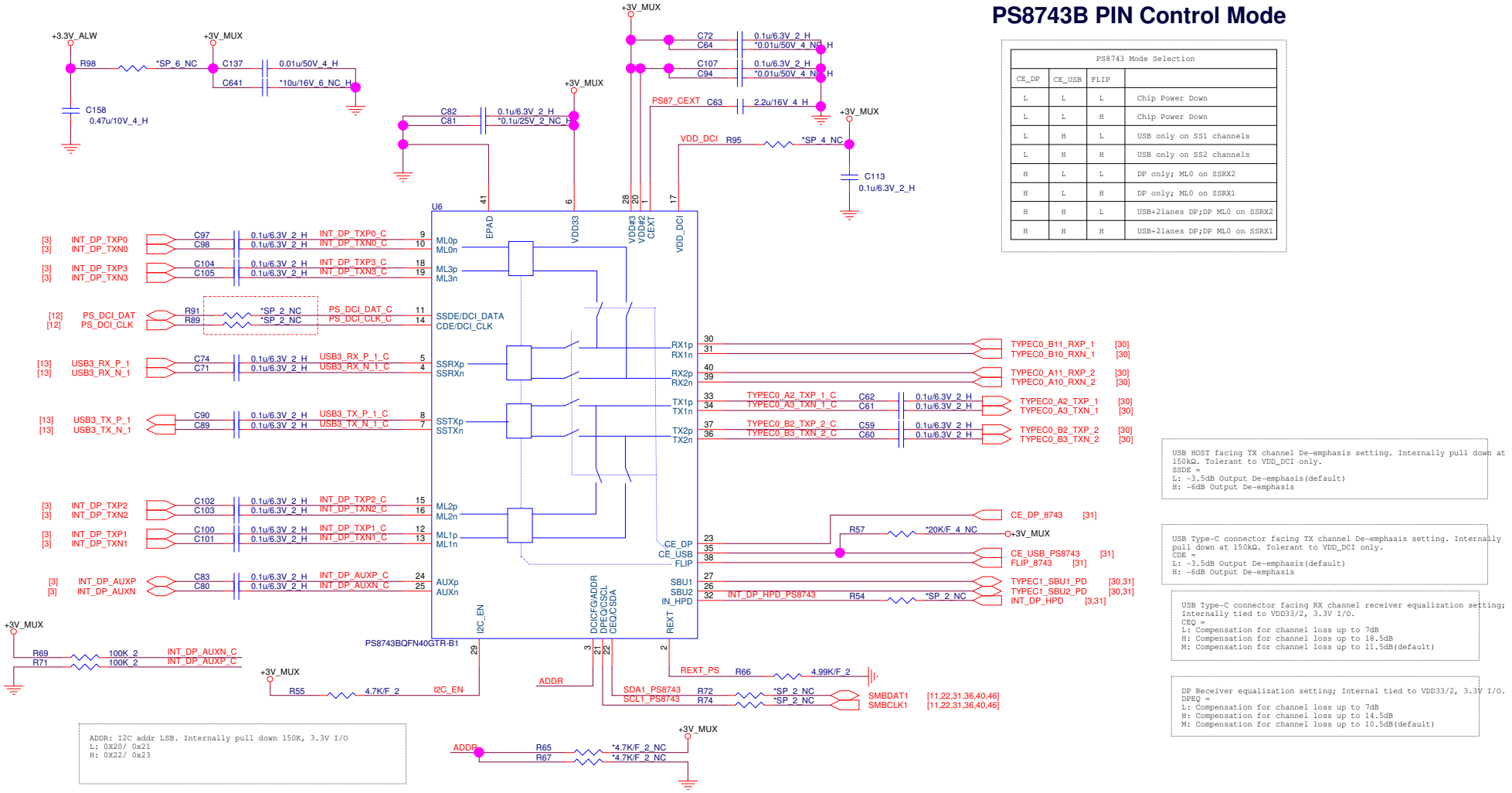
PS8743B PIN Control Mode

PS8743 Mode Selection			
CE_DP	CE_USB	FLIP	
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	USB only on SS1 channels
L	H	H	USB only on SS2 channels
H	L	L	DP only; ML0 on SSRX2
H	L	H	DP only; ML0 on SSRX1
H	H	L	USB+2lanes DP;DP ML0 on SSRX2
H	H	H	USB+2lanes DP;DP ML0 on SSRX1



USB HOST facing TX channel De-emphasis setting. Internally pull down at 150kΩ. Tolerant to VDD_DCI only.
SSDE =
L: -3.5dB Output De-emphasis(default)
H: -6dB Output De-emphasis

USB Type-C connector facing TX channel De-emphasis setting. Internally pull down at 150kΩ. Tolerant to VDD_DCI only.
CDE =
L: -3.5dB Output De-emphasis(default)
H: -6dB Output De-emphasis

USB Type-C connector facing RX channel receiver equalization setting; Internally tied to VDD33/2, 3.3V I/O.
CEQ =
L: Compensation for channel loss up to 7dB
H: Compensation for channel loss up to 18.5dB
M: Compensation for channel loss up to 11.5dB(default)

DP Receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
DPEQ =
L: Compensation for channel loss up to 7dB
H: Compensation for channel loss up to 14.5dB
M: Compensation for channel loss up to 10.5dB(default)

ADDR: I2C addr LSB. Internally pull down 150K, 3.3V I/O
L: 0X20/ 0x21
H: 0X22/ 0x23

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	Type C MUX_PS8743B (3/3)	3A
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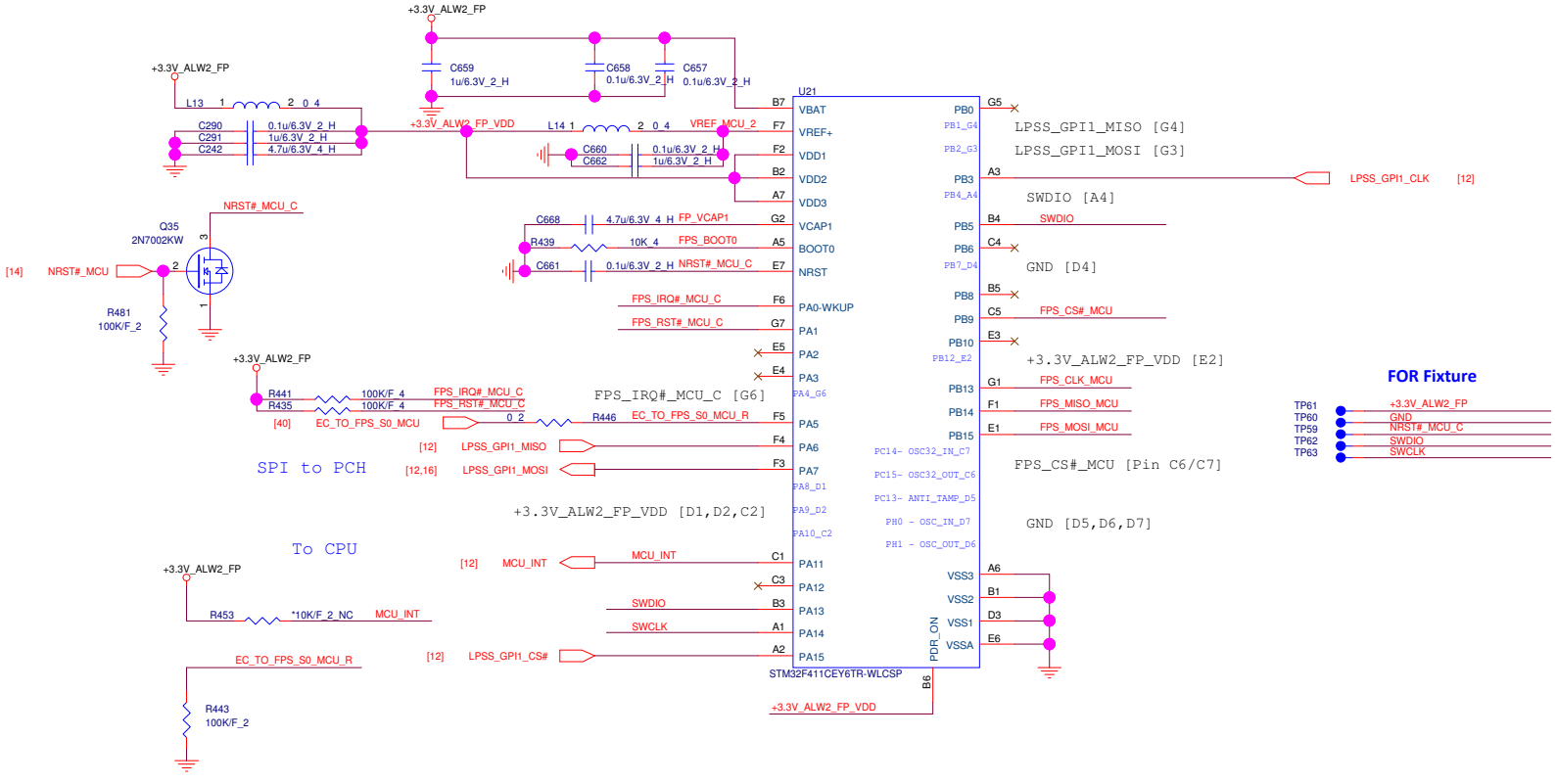

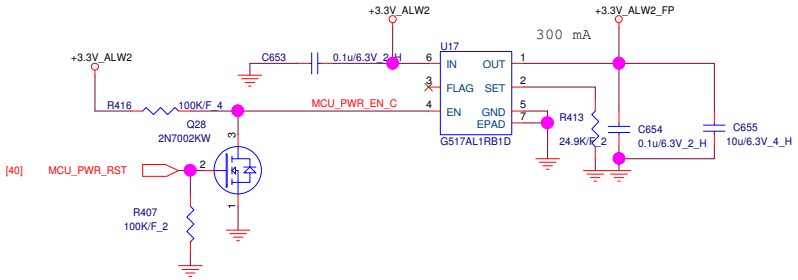

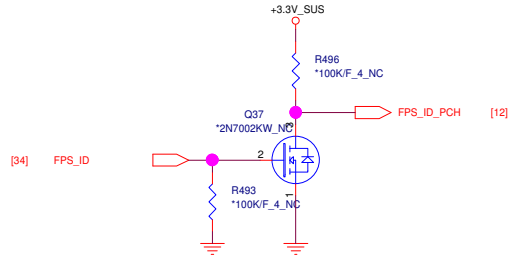

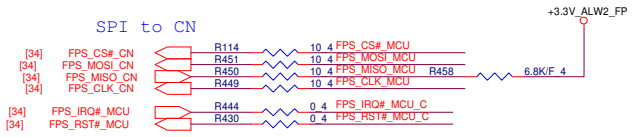

FPS_IRQ#_MCU

Pin F6 / G6

+3.3V_ALW2_FP_VDD

Pin /F2/B2/A7/D1/D2/C2/E2/B6

GND

Pin /D4/D5/D6/D7/A6/B1/D3/E6

SWDIO

Pin /B4/C4/B3

SPI2-->CS(PB9/PC14/PC15)
SPI2-->MOSI(PB15)
SPI2-->MISO(PB14)
SPI2-->SCK(PB13)

SPI1-->CS(PA15)
SPI1-->MOSI(PA7)
SPI1-->MISO(PA6)
SPI1-->SCK(PB3)

GSPI1_MISO_MCU pin F4/G4
GSPI1_MOSI_MCU pin F3/G3

FPS_RST#_MCU-->Pin G7
MCU_INT#_R-->Pin C1
EC_TO_FPS_S0_MCU_R-->Pin G5

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Size	Document Number	Rev
	MCU_STM32F411CEU6TR	3A
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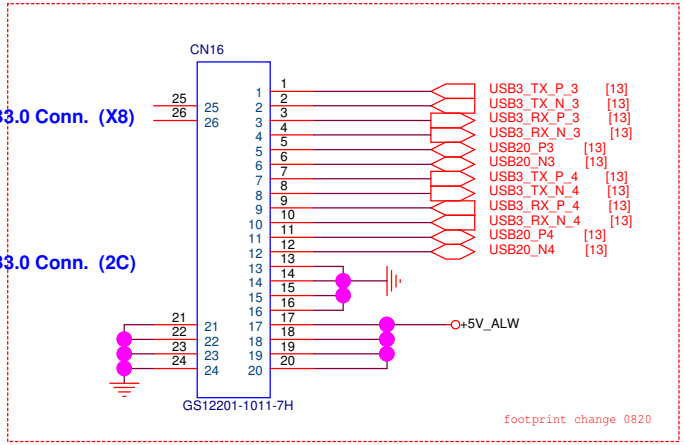
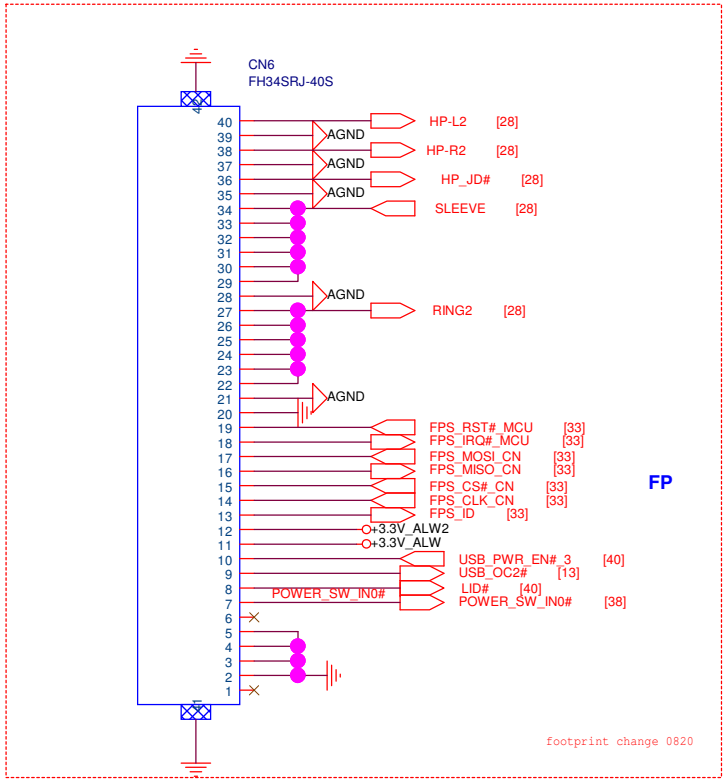
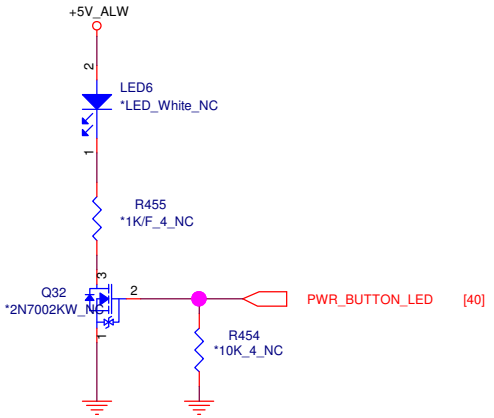
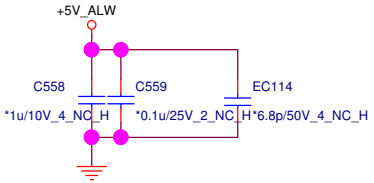
MB TO DB conn





Power button LED





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	34- I/O DB	3A
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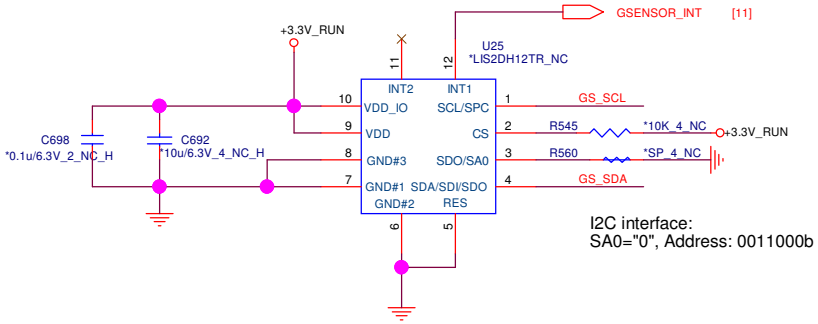
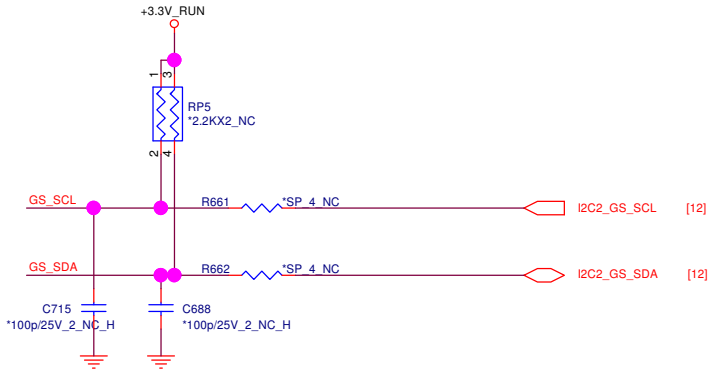
LIS2DH12TR



I2C interface:
SA0="0", Address: 0011000b



NC : C692, C715, C688

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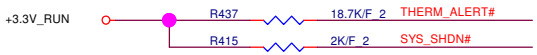
Thermal IC

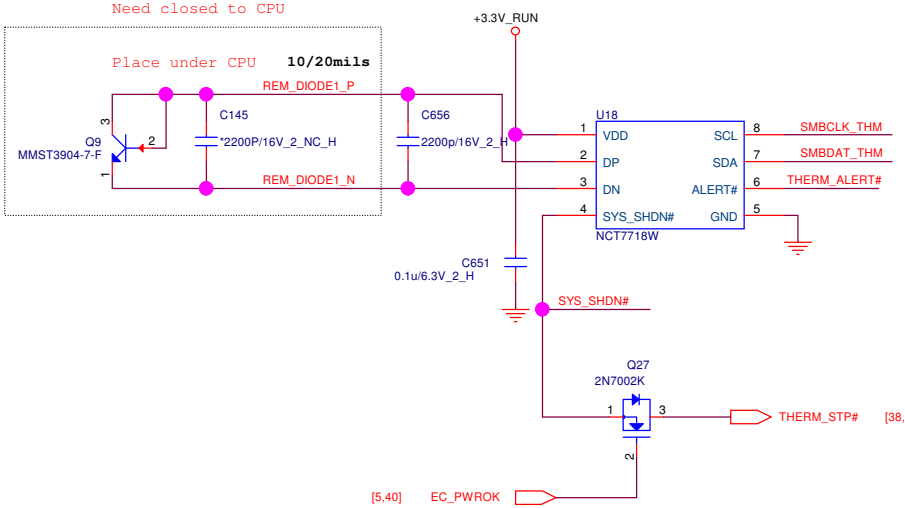
OTP 85 degree C

OTP 85 degree : R526= 18.7K, R527= 2K

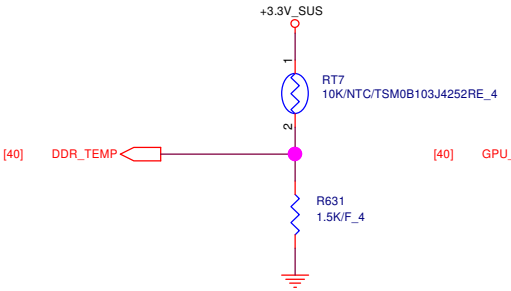


SYS_SHD# / ALERT#	2K	7.5K	10.5K	14K	18.7K
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

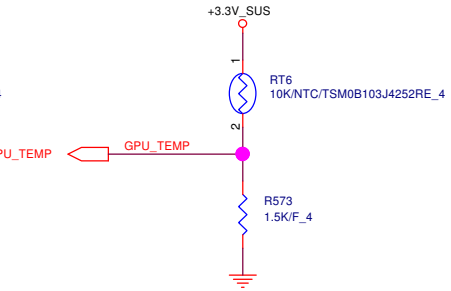
Need closed to CPU



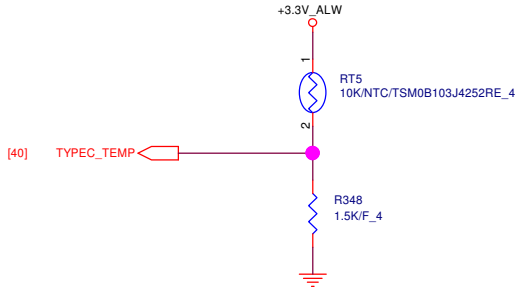
For DDR use

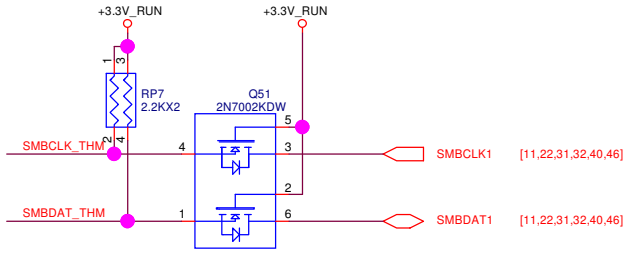


For GPU use



For Type C use





Quanta Computer Inc.

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	Thermal	3A

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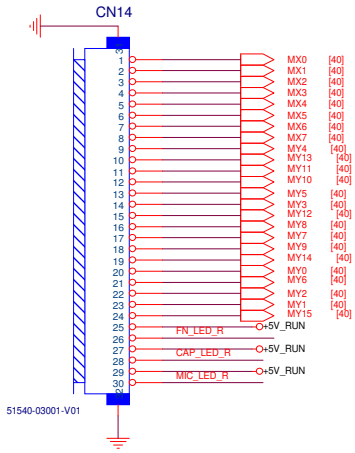
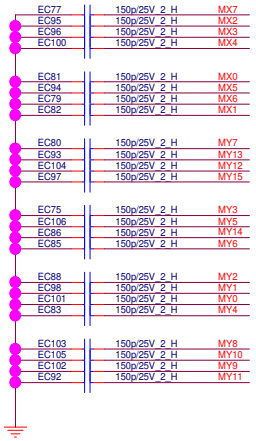
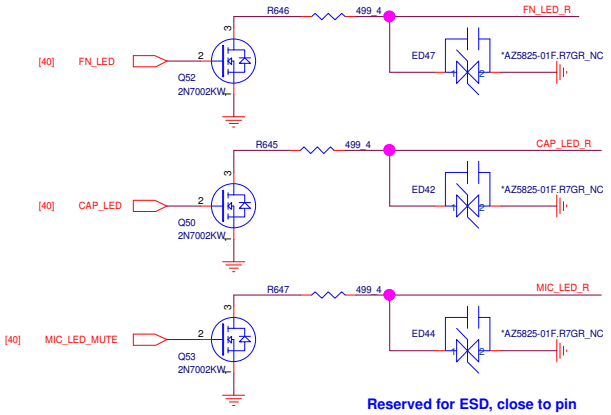
Keyboard Connector



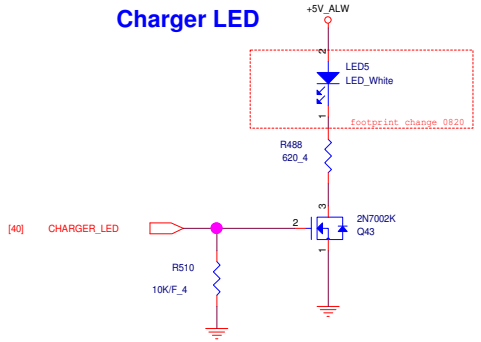
Close to KB conn

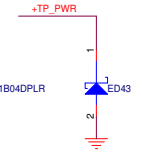




Reserved for ESD, close to pin

Charger LED





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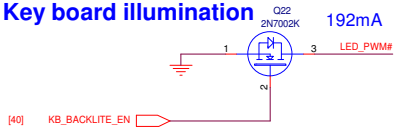
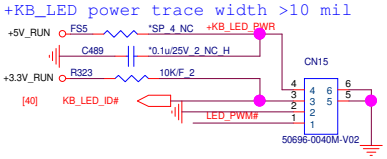
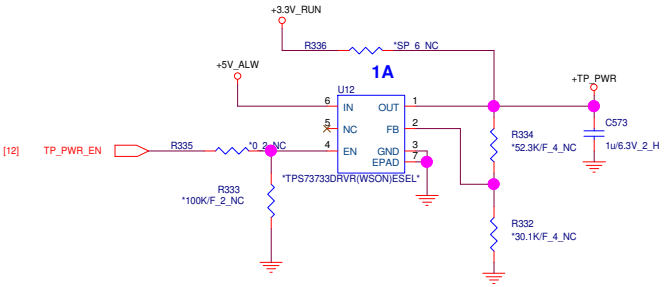
Key board illumination

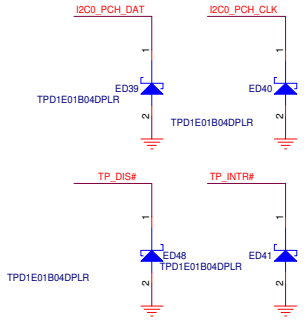


Key Board BL

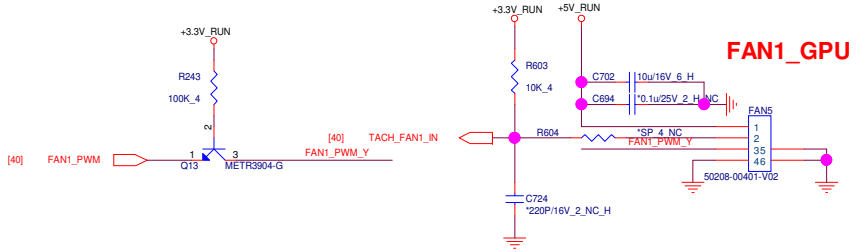


Click Pad POWER

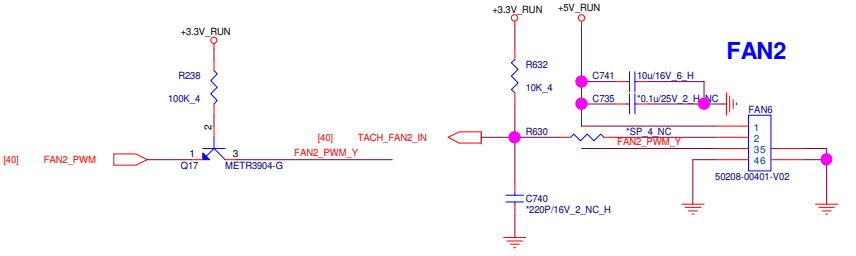




FAN1_GPU

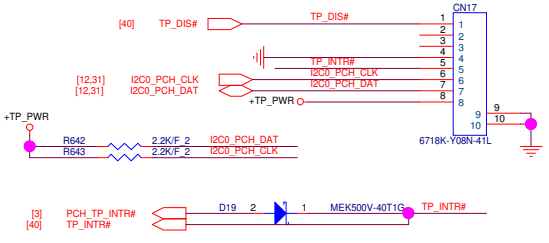


FAN2



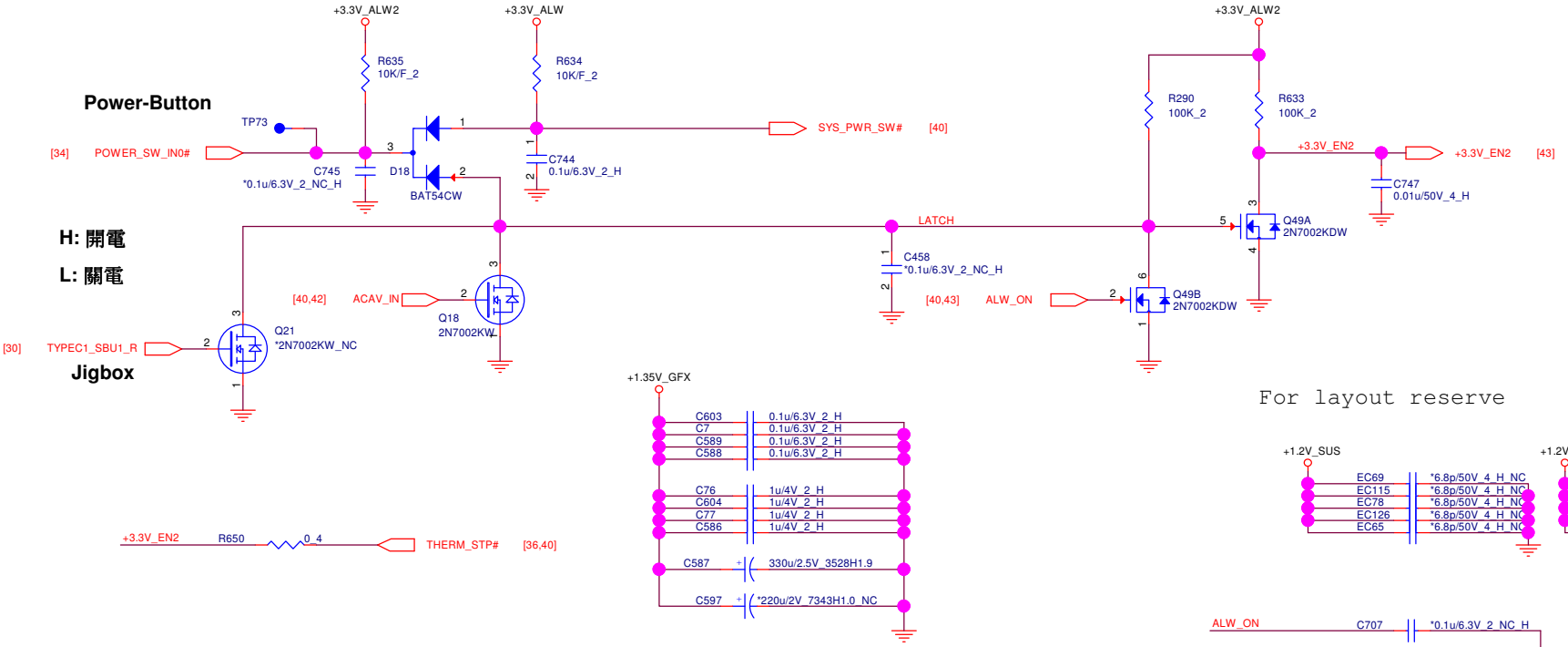
Click Pad

12/25: del PS2 function

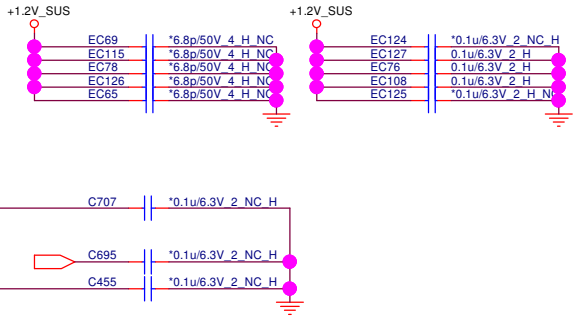


Quanta Computer Inc.		
PROJECT : H97M		
Size	Document Number: KB/TP/THERMAL/LID	Rev: 3A
Date: Monday, April 06, 2020	Sheet 37 of 60	

3.3VALW_ON POWER LOGIC



For layout reserve

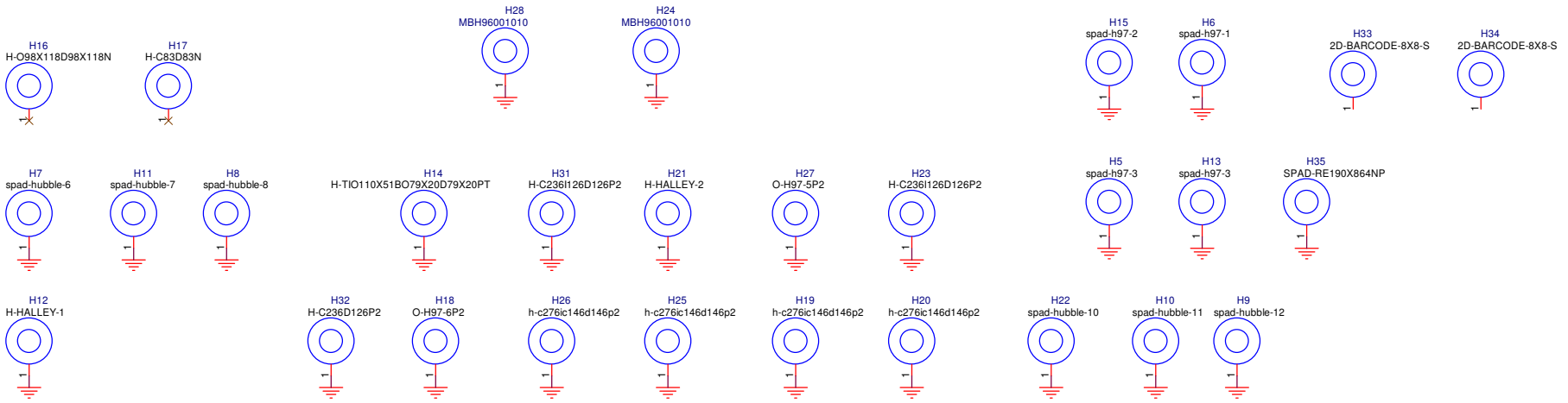


NUT

HOLE

SSD

WLAN

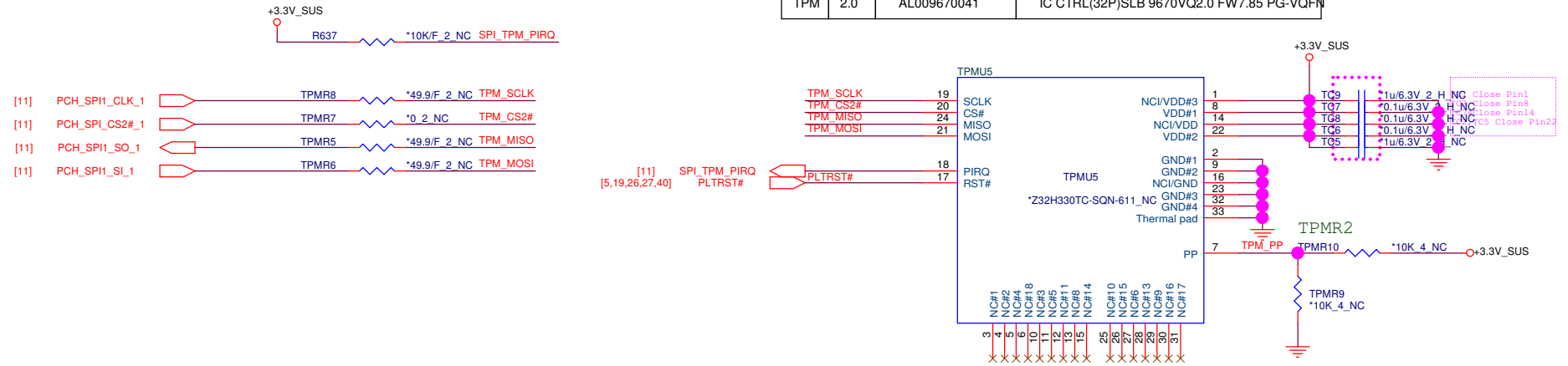


Quanta Computer Inc.		
PROJECT : H97M		
Size	Document Number: 3VALW ON/RTC/LED/HOLE	Rev: 3A
Date: Monday, April 06, 2020	Sheet 38 of 60	

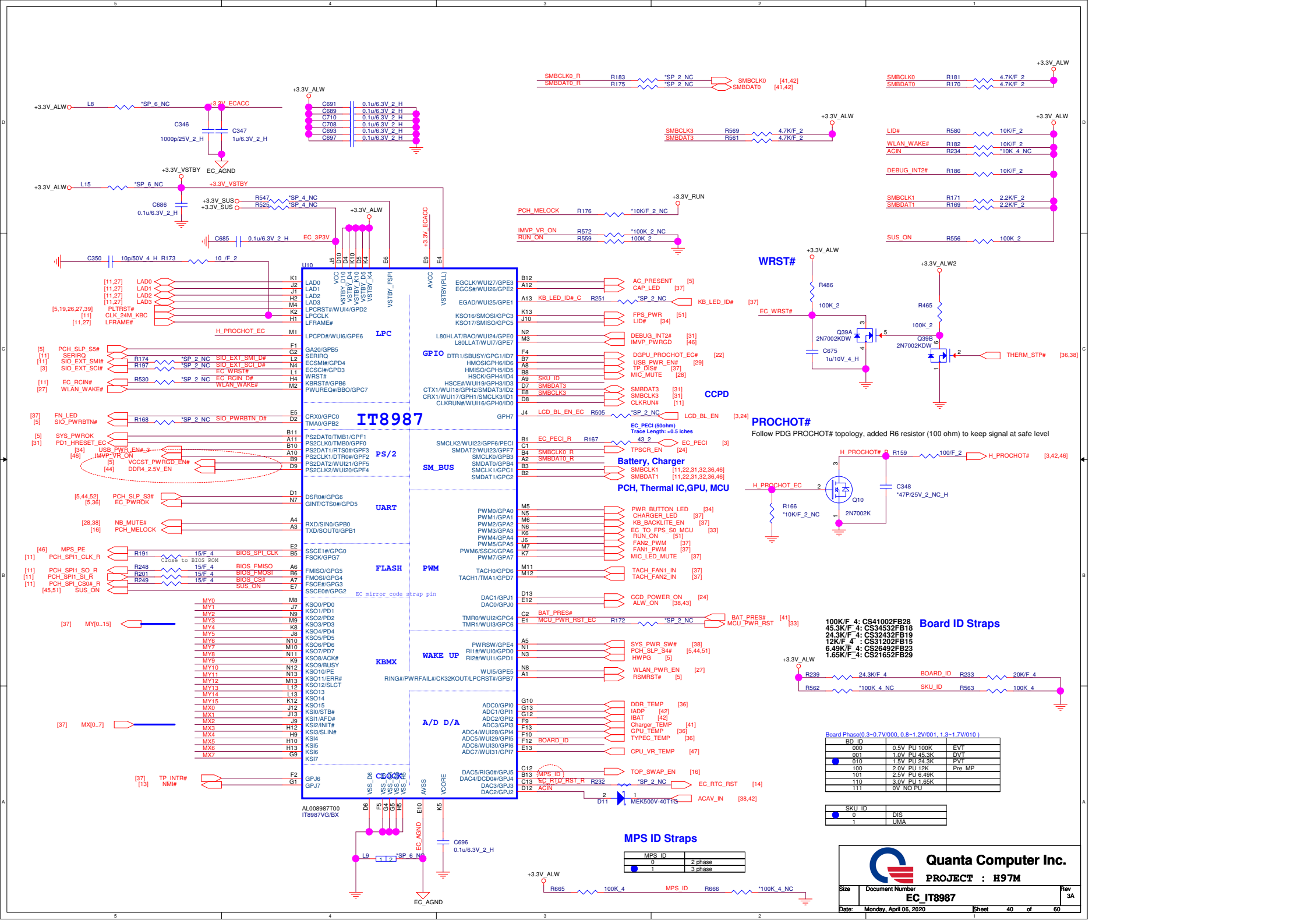
TPM

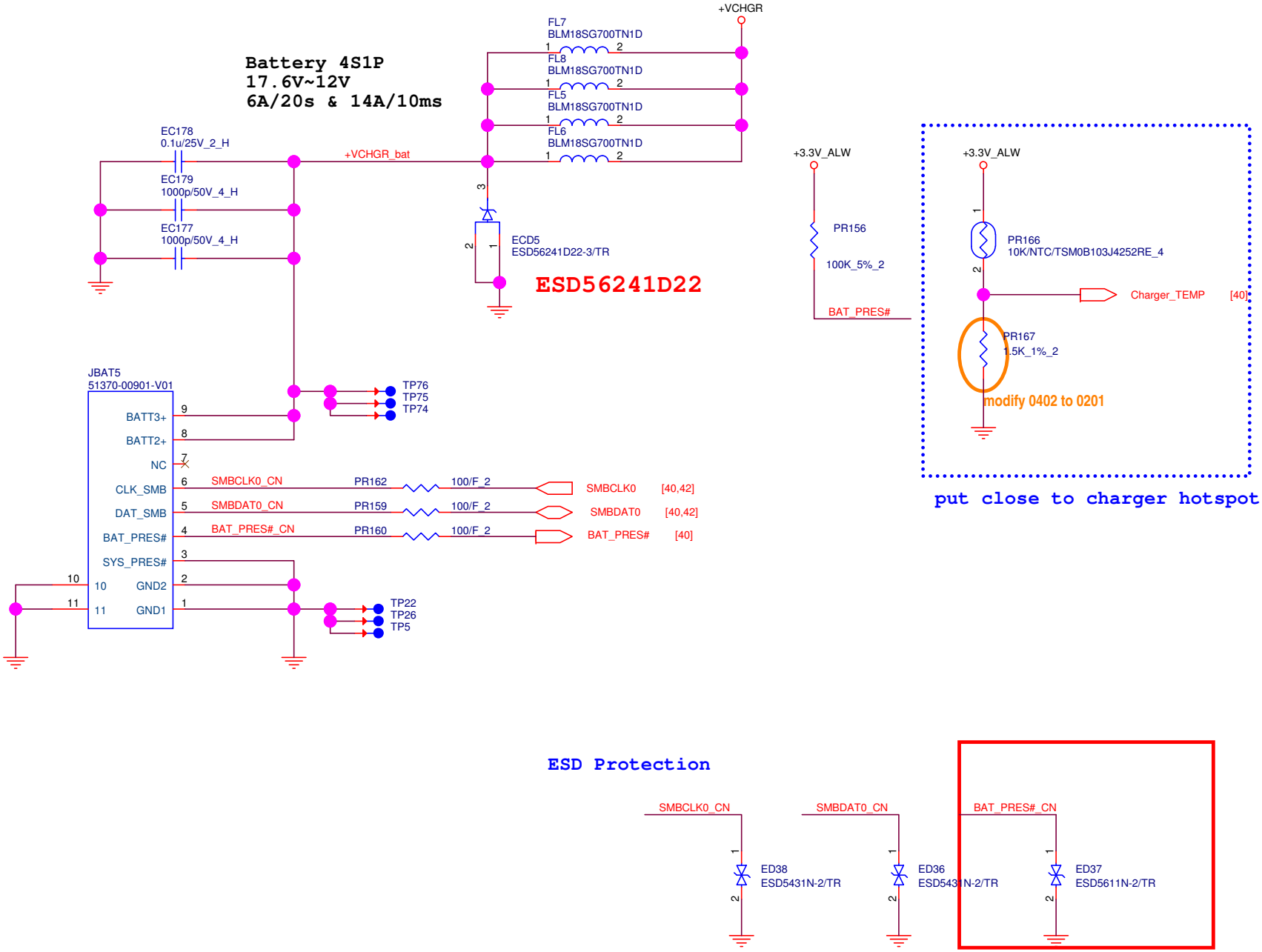
TPM Configuration

		QPN	Description
TCM		AL000330012	IC OTHER(32P) Z32H330TC-SQN-611(QFN)
TPM	2.0	AL000330011	IC OTHER(32P) Z32H330TC-2.0 SQN-726(QFN)
TPM	2.0	AL009670041	IC CTRL(32P)SLB 9670VQ2.0 FW7.85 PG-VQFN

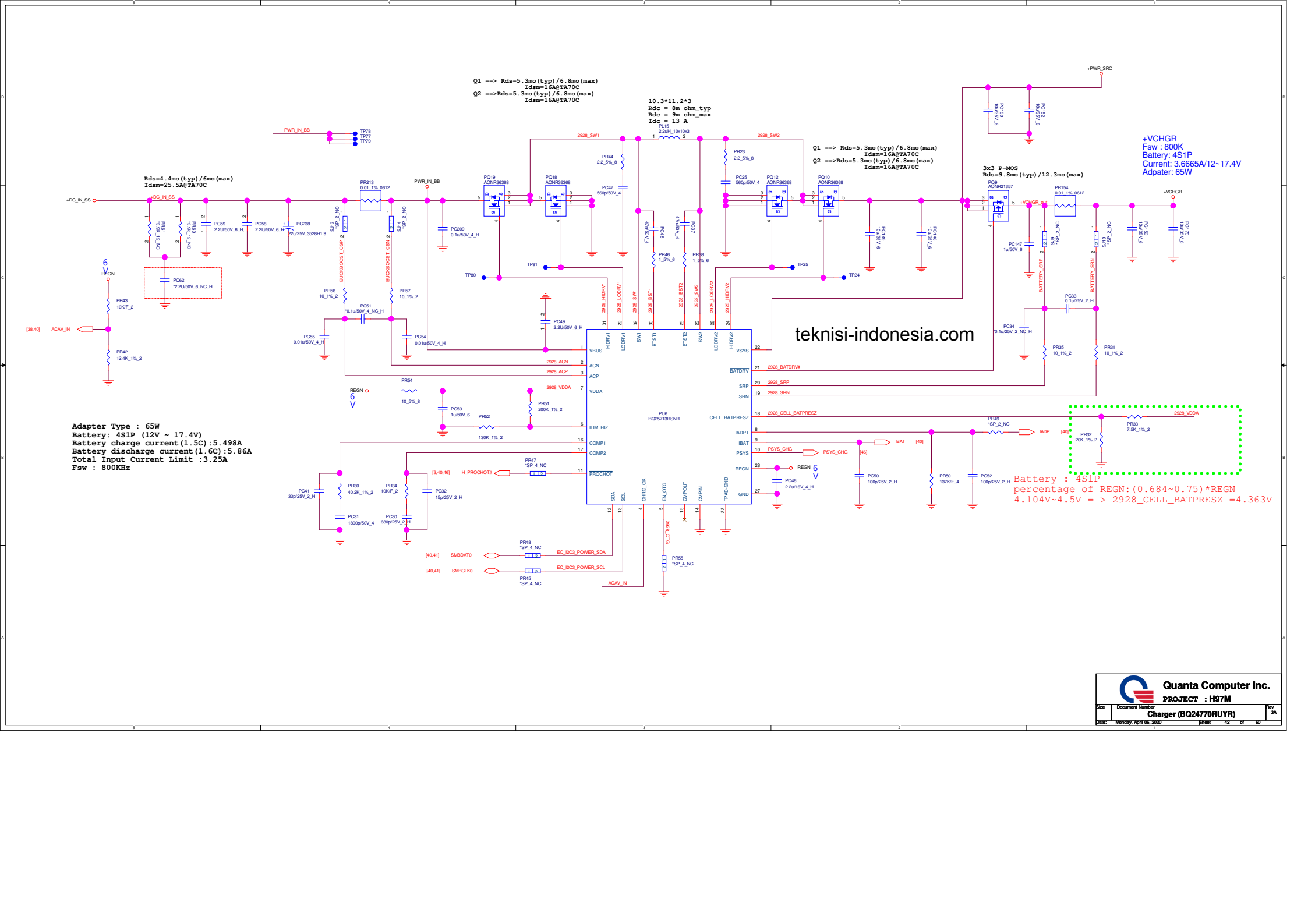


Quanta Computer Inc.			
PROJECT : H97M			
Size	Document Number: TPM		Rev: 3A
Date: Monday, April 06, 2020	Sheet 39 of 60		


IT8987
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
CCPD
Battery, Charger
PCH, Thermal IC,GPU, MCU
WRST#
PROCHOT#
Follow PDG PROCHOT# topology, added R6 resistor (100 ohm) to keep signal at safe level
Board ID Straps
100K/F_4: CS41002FB28
45.3K/F_4: CS34532FB18
24.3K/F_4: CS32432FB19
12K/F_4 : CS31202FB15
6.49K/F_4: CS26492FB23
1.65K/F_4: CS21652FB29
MPS ID Straps
Quanta Computer Inc.
PROJECT : H97M
EC_IT8987
Monday, April 06, 2020



Quanta Computer Inc.		
PROJECT : H97M		
Size	Document Number: DCin & Bat	Rev: 3A
Date: Monday, April 06, 2020	Sheet 41 of 60	


Q1 ==> Rds=5.3mo(typ)/6.8mo(max)
Idsm=16A@TA70C
Q2 ==>Rds=5.3mo(typ)/6.8mo(max)
Idsm=16A@TA70C
10.3*11.2*3
Rdc = 8m ohm_typ
Rdc = 9m ohm_max
Idc = 13 A
Q1 ==> Rds=5.3mo(typ)/6.8mo(max)
Idsm=16A@TA70C
Q2 ==>Rds=5.3mo(typ)/6.8mo(max)
Idsm=16A@TA70C
3x3 P-MOS
Rds=9.8mo(typ)/12.3mo(max)
Rds=4.4mo(typ)/6mo(max)
Idsm=25.5A@TA70C
+VCHGR
Fsw : 800K
Battery: 4S1P
Current: 3.6665A/12~17.4V
Adpater: 65W
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Adapter Type : 65W
Battery: 4S1P (12V ~ 17.4V)
Battery charge current(1.5C):5.498A
Battery discharge current(1.6C):5.86A
Total Input Current Limit :3.25A
Fsw : 800KHz
Battery : 4S1P
percentage of REGN:(0.684~0.75)*REGN
4.104V~4.5V = > 2928_CELL_BATPRESZ =4.363V
Quanta Computer Inc.
PROJECT : H97M
Charger (BQ24770RUYR)
Rev 3A
Monday, April 06, 2020
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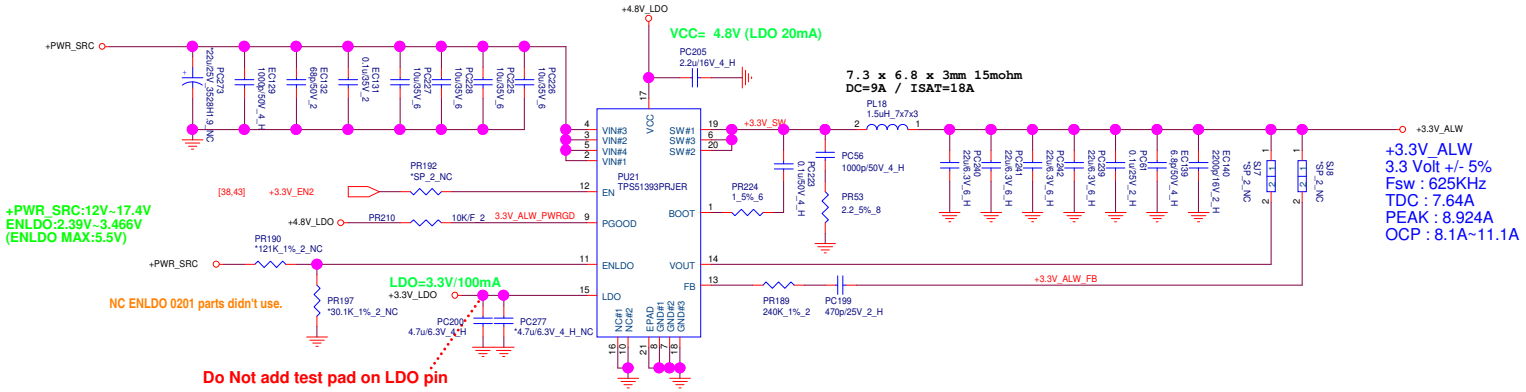
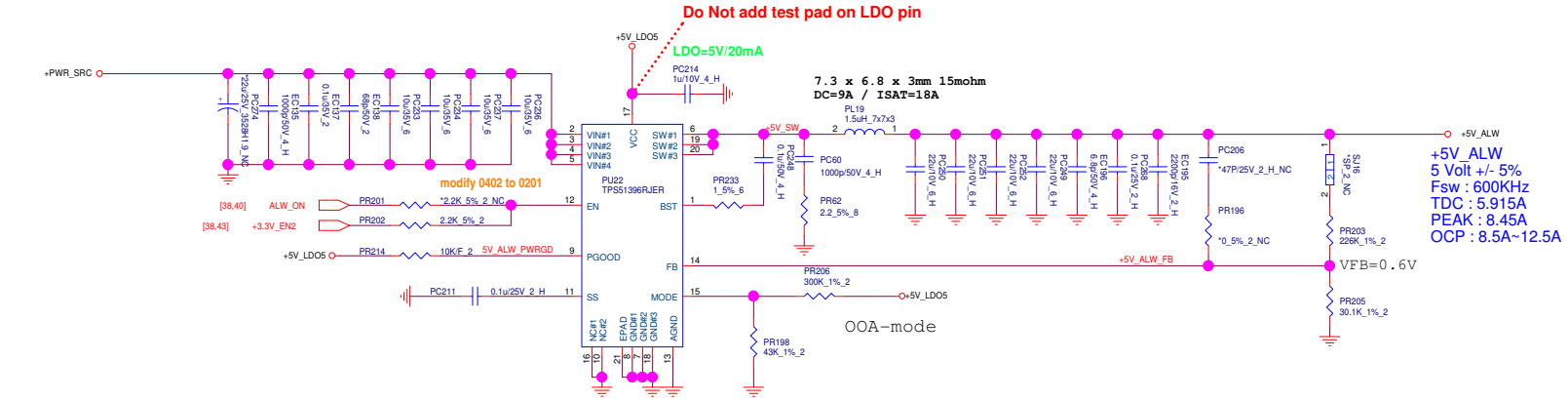
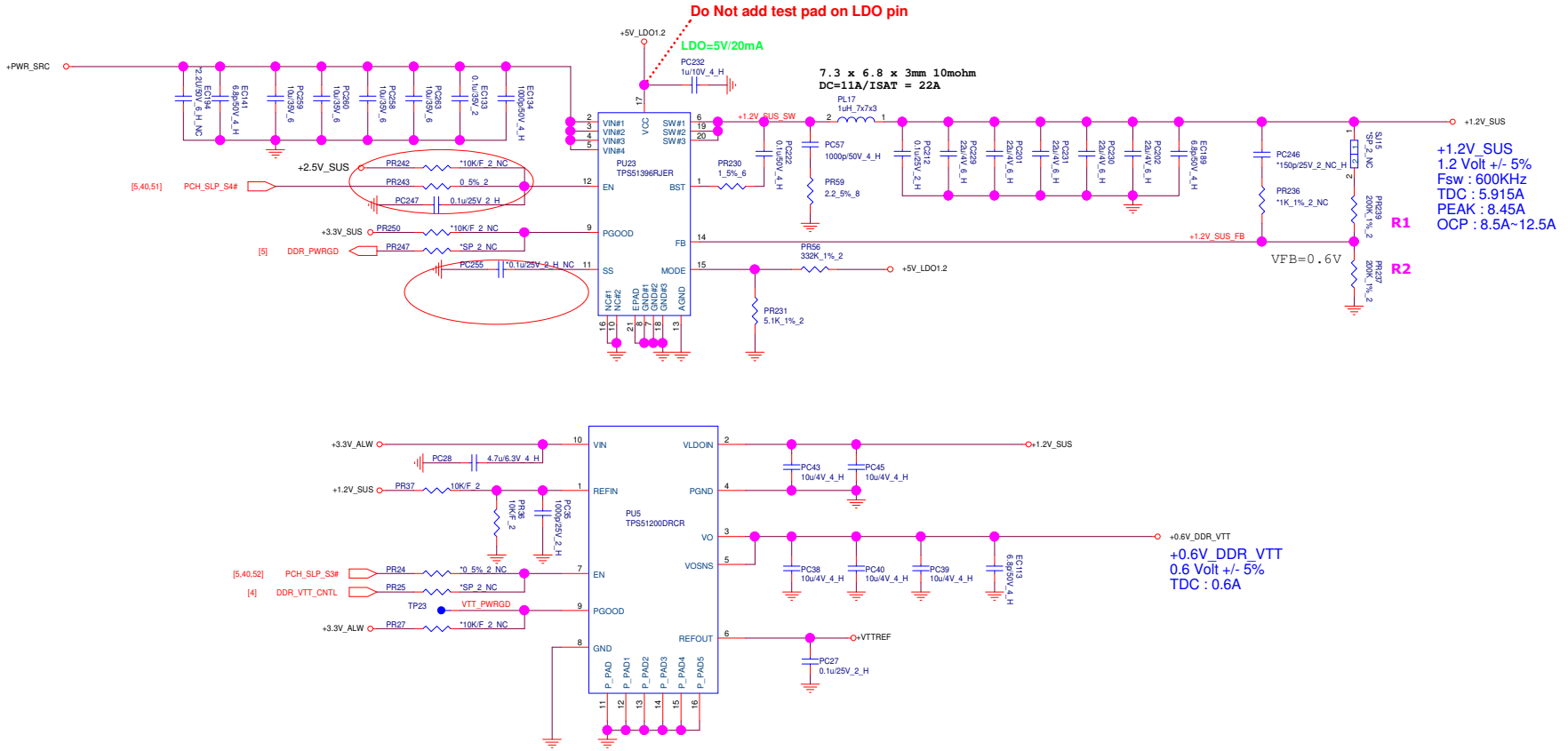
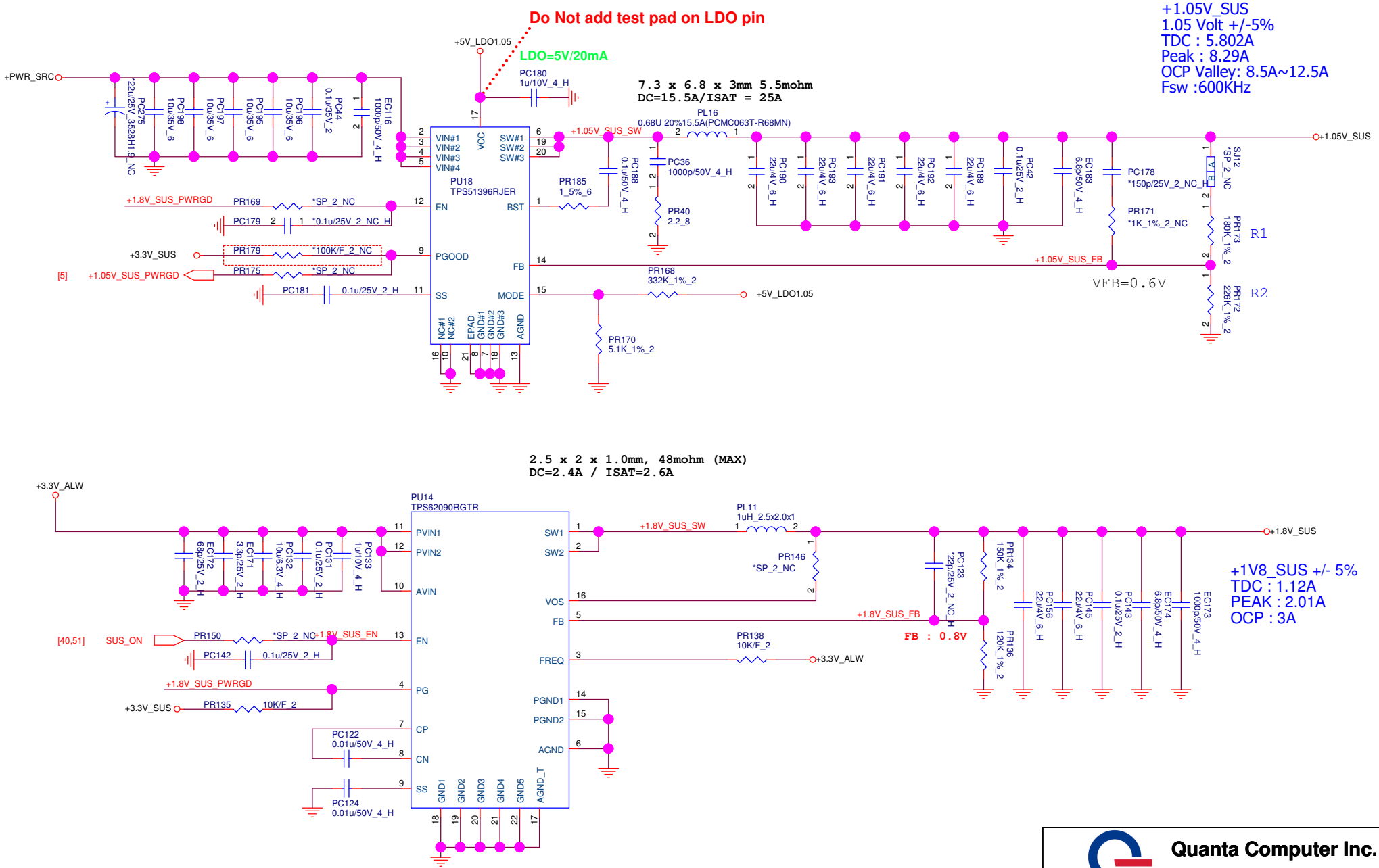




Quanta Computer Inc.		
PROJECT : H97M		
Size	Document Number: +3V(TPS51393RJER)/+5V(TPS51396RJER)	Rev: 3A
Date: Monday, April 06, 2020	Sheet 43 of 60	



Quanta Computer Inc.			
PROJECT : H97M			
Size	Document Number		Rev
	VDDQ(TPS51396)/VTT(TPS51200)		3A
Date: Monday, April 06, 2020		Sheet 44 of 60	


Do Not add test pad on LDO pin
+5V_LDO1.05
LDO=5V/20mA
PC180
1u/10V_4_H
7.3 x 6.8 x 3mm 5.5mohm
DC=15.5A/ISAT = 25A
PL16
0.68U 20%15.5A(PCMC063T-R68MN)
+1.05V_SUS
1.05 Volt +/-5%
TDC : 5.802A
Peak : 8.29A
OCP Valley: 8.5A~12.5A
Fsw :600KHz
+PWR_SRC
PU18
TPS51396RJER
VIN#1
VIN#2
VIN#3
VIN#4
VCC
SW#1
SW#2
SW#3
EN
BST
PGOOD
FB
SS
MODE
NC#1
NC#2
EPAD
GND#1
GND#2
GND#3
AGND
+1.05V_SUS_SW
+1.8V_SUS_PWRGD
PR169
*SP_2_NC
PC179
*0.1u/25V_2_NC_H
+3.3V_SUS
PR179
*100K/F_2_NC
[5]
PR175
PC181
0.1u/25V_2_H
PR185
1_5%_6
PC36
1000p/50V_4_H
PR40
2.2_8
PR168
332K_1%_2
+5V_LDO1.05
PR170
5.1K_1%_2
+1.05V_SUS_FB
PC178
*150p/25V_2_NC_H
PR171
*1K_1%_2_NC
VFB=0.6V
PR173
180K_1%_2
R1
PR172
226K_1%_2
R2
2.5 x 2 x 1.0mm, 48mohm (MAX)
DC=2.4A / ISAT=2.6A
+3.3V_ALW
PU14
TPS62090RGTR
PVIN1
PVIN2
AVIN
SW1
SW2
VOS
FB
FREQ
PGND1
PGND2
AGND
EN
PG
CP
CN
SS
GND1
GND2
GND3
GND4
GND5
AGND_T
PL11
1uH_2.5x2.0x1
+1.8V_SUS_SW
PR146
*SP_2_NC
PR138
10K/F_2
+1.8V_SUS_FB
FB : 0.8V
PR134
150K_1%_2
PR136
120K_1%_2
+1.8V_SUS
[40,51]
SUS_ON
PR150
*SP_2_NC
+1.8V_SUS_EN
PC142
0.1u/25V_2_H
+1.8V_SUS_PWRGD
PR135
10K/F_2
PC122
0.01u/50V_4_H
PC124
0.01u/50V_4_H
+1V8_SUS +/- 5%
TDC : 1.12A
PEAK : 2.01A
OCP : 3A
Quanta Computer Inc.
PROJECT : H97M
Size
Document Number
+1.05V_SUS / +1.8V_SUS
Rev
3A
Date: Monday, April 06, 2020
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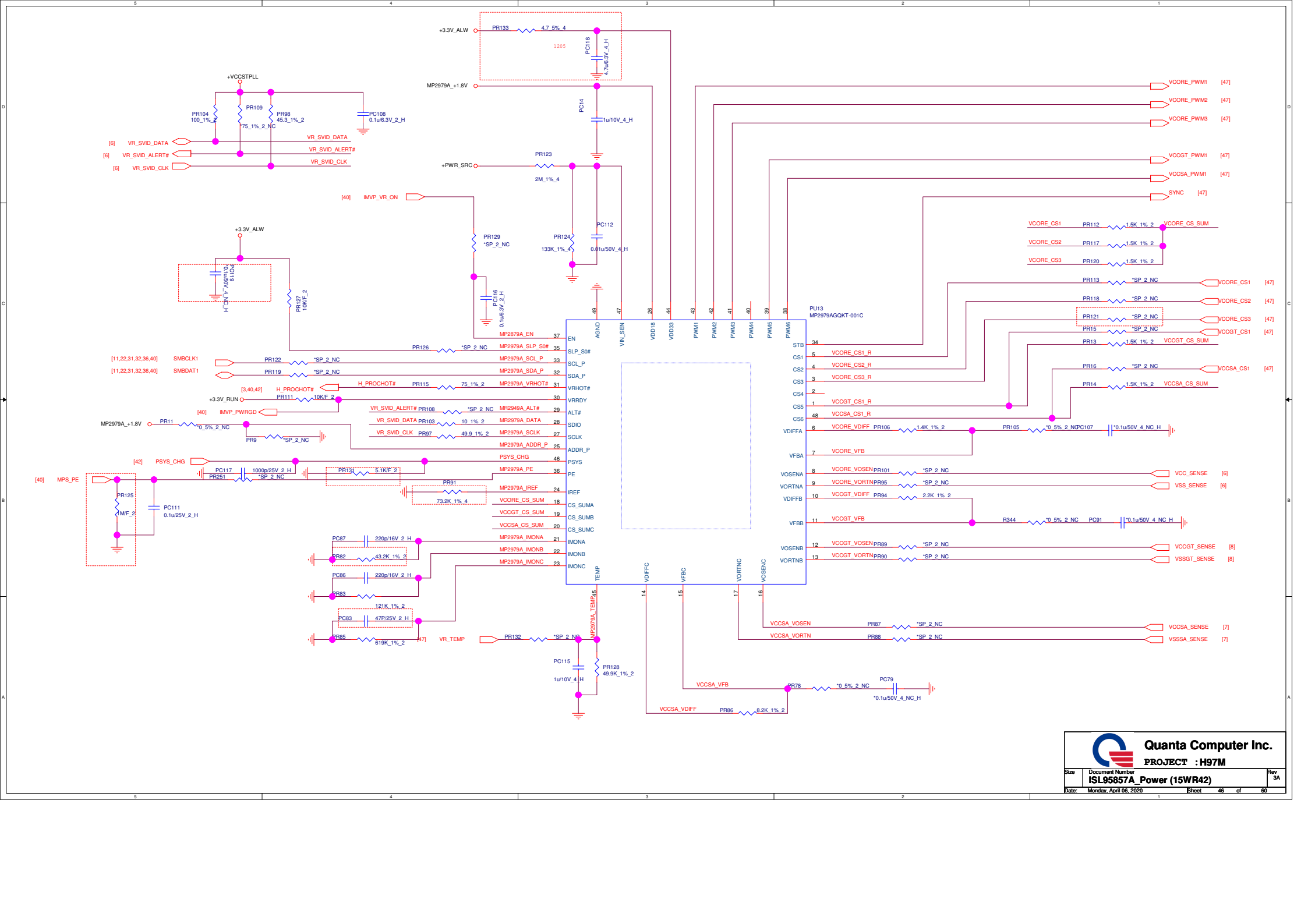
+3.3V_ALW
PR133
4.7_5%_4
1205
PC118
4.7u/6.3V_4_H
MP2979A_+1.8V
PC14
1u/10V_4_H
+VCCSTPLL
PR104
100_1%_2
PR109
*75_1%_2_NC
PR98
45.3_1%_2
PC108
0.1u/6.3V_2_H
[6] VR_SVID_DATA
[6] VR_SVID_ALERT#
[6] VR_SVID_CLK
VR_SVID_DATA
VR_SVID_ALERT#
VR_SVID_CLK
+PWR_SRC
PR123
2M_1%_4
[40] IMVP_VR_ON
PR129
*SP_2_NC
PR124
133K_1%_4
PC112
0.01u/50V_4_H
PC116
0.1u/6.3V_2_H
PC119
0.01u/50V_4_NC_H
PR127
10K/F_2
+3.3V_ALW
PU13
MP2979AGQKT-001C
AGND
VIN_SEN
VDD18
VDD33
PWM1
PWM2
PWM3
PWM4
PWM5
PWM6
EN
SLP_S0#
SCL_P
SDA_P
VRHOT#
VRRDY
ALT#
SDIO
SCLK
ADDR_P
PSYS
PE
IREF
CS_SUMA
CS_SUMB
CS_SUMC
IMONA
IMONB
IMONC
TEMP
VDIFFC
VFBC
VORTNC
VOSENC
STB
CS1
CS2
CS3
CS4
CS5
CS6
VDIFFA
VFBA
VOSENA
VORTNA
VDIFFB
VFBB
VOSENB
VORTNB
MP2879A_EN
MP2979A_SLP_S0#
MP2979A_SCL_P
MP2979A_SDA_P
MP2979A_VRHOT#
MR2949A_ALT#
MP2979A_DATA
MP2979A_SCLK
MP2979A_ADDR_P
PSYS_CHG
MP2979A_PE
MP2979A_IREF
VCORE_CS_SUM
VCCGT_CS_SUM
VCCSA_CS_SUM
MP2979A_IMONA
MP2979A_IMONB
MP2979A_IMONC
MP2979A_TEMP
VCORE_PWM1 [47]
VCORE_PWM2 [47]
VCORE_PWM3 [47]
VCCGT_PWM1 [47]
VCCSA_PWM1 [47]
SYNC [47]
VCORE_CS1_R
VCORE_CS2_R
VCORE_CS3_R
VCCGT_CS1_R
VCCSA_CS1_R
VCORE_VDIFF
VCORE_VFB
VCORE_VOSEN
VCORE_VORTN
VCCGT_VDIFF
VCCGT_VFB
VCCGT_VOSEN
VCCGT_VORTN
VCCSA_VOSEN
VCCSA_VORTN
VCORE_CS1
VCORE_CS2
VCORE_CS3
PR112 1.5K_1%_2
PR117 1.5K_1%_2
PR120 1.5K_1%_2
VCORE_CS_SUM
PR113 *SP_2_NC
PR118 *SP_2_NC
PR121 *SP_2_NC
PR15 *SP_2_NC
PR13 1.5K_1%_2
VCCGT_CS_SUM
PR16 *SP_2_NC
PR14 1.5K_1%_2
VCCSA_CS_SUM
VCORE_CS1 [47]
VCORE_CS2 [47]
VCORE_CS3 [47]
VCCGT_CS1 [47]
VCCSA_CS1 [47]
PR106 1.4K_1%_2
PR105 *0_5%_2_NC
PC107 *0.1u/50V_4_NC_H
PR101 *SP_2_NC
PR95 *SP_2_NC
VCC_SENSE [6]
VSS_SENSE [6]
PR94 2.2K_1%_2
R344 *0_5%_2_NC
PC91 *0.1u/50V_4_NC_H
PR89 *SP_2_NC
PR90 *SP_2_NC
VCCGT_SENSE [8]
VSSGT_SENSE [8]
PR87 *SP_2_NC
PR88 *SP_2_NC
VCCSA_SENSE [7]
VSSSA_SENSE [7]
PR78 *0_5%_2_NC
PC79 *0.1u/50V_4_NC_H
VCCSA_VFB
VCCSA_VDIFF
PR86 8.2K_1%_2
PR126 *SP_2_NC
PR122 *SP_2_NC
PR119 *SP_2_NC
[11,22,31,32,36,40] SMBCLK1
[11,22,31,32,36,40] SMBDAT1
[3,40,42] H_PROCHOT#
H_PROCHOT# PR115 75_1%_2
PR111 10K/F_2
+3.3V_RUN
[40] IMVP_PWRGD
MP2979A_+1.8V
PR11 *0_5%_2_NC
PR9 *SP_2_NC
VR_SVID_ALERT# PR108 *SP_2_NC
VR_SVID_DATA PR103 10_1%_2
VR_SVID_CLK PR97 49.9_1%_2
[42] PSYS_CHG
PC117 1000p/25V_2_H
PR251 *SP_2_NC
PR131 5.1K/F_2
PR91 73.2K_1%_4
[40] MPS_PE
PR125 1M/F_2
PC111 0.1u/25V_2_H
PC87 220p/16V_2_H
PR82 43.2K_1%_2
PC86 220p/16V_2_H
PR83 121K_1%_2
PC83 47P/25V_2_H
PR85 619K_1%_2
[47] VR_TEMP
PR132 *SP_2_NC
MP2979A_TEMP
PC115 1u/10V_4_H
PR128 49.9K_1%_2
Quanta Computer Inc.
PROJECT : H97M
Size
Document Number
ISL95857A_Power (15WR42)
Rev 3A
Date: Monday, April 06, 2020
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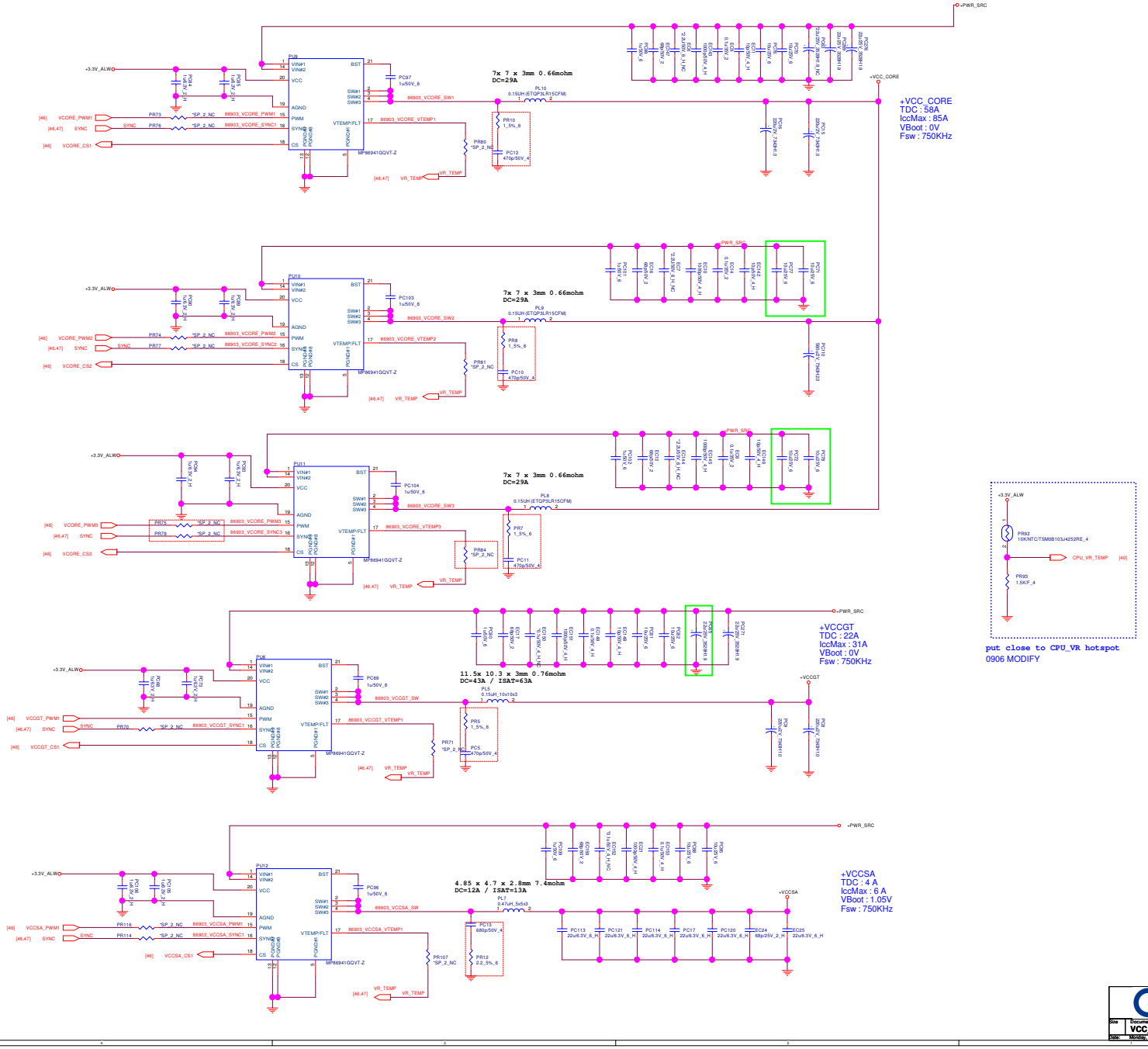
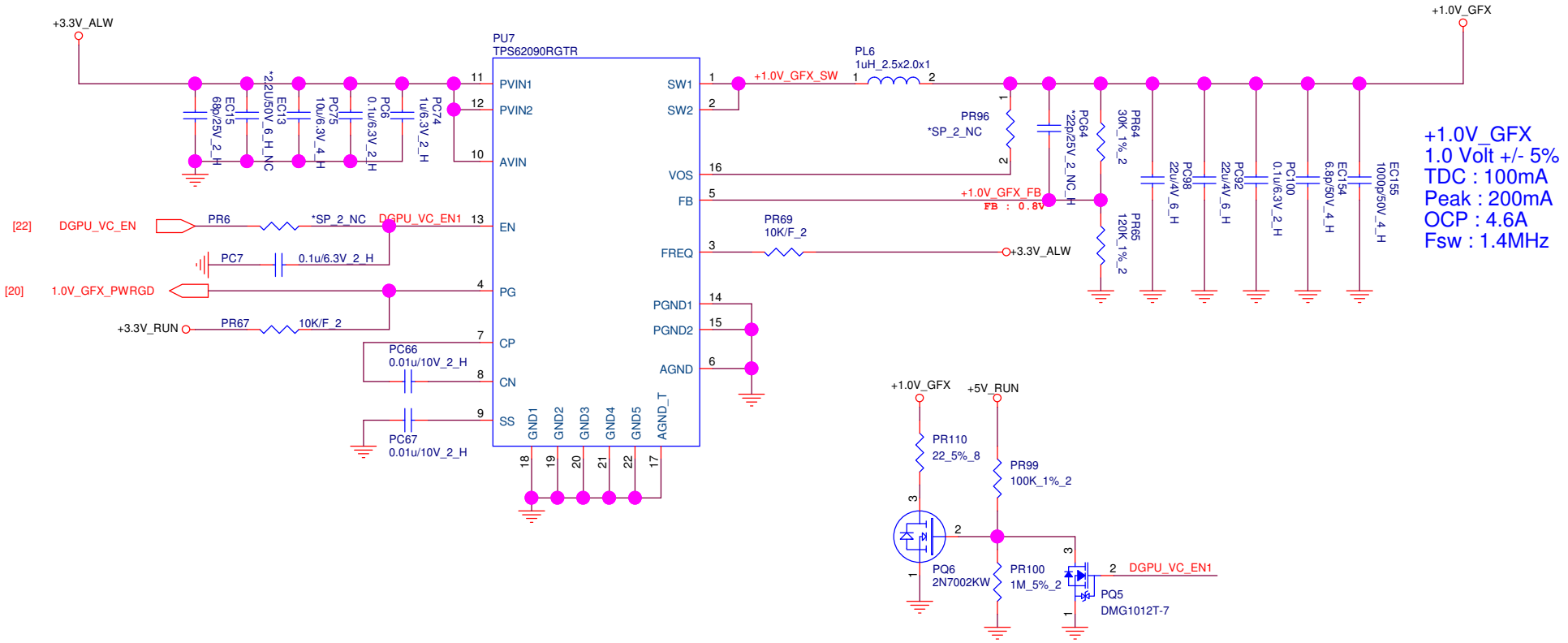


Quanta Computer Inc.	
PROJECT : H97M	
Size	Document Number: VCC_CORE (ISL95857AHRTZ-T) Rev: 3A
Date: Monday, April 06, 2020	Sheet 47 of 60

2.5 x 2 x 1.0mm, 48mohm (MAX)
DC=2.4A / ISAT=2.6A



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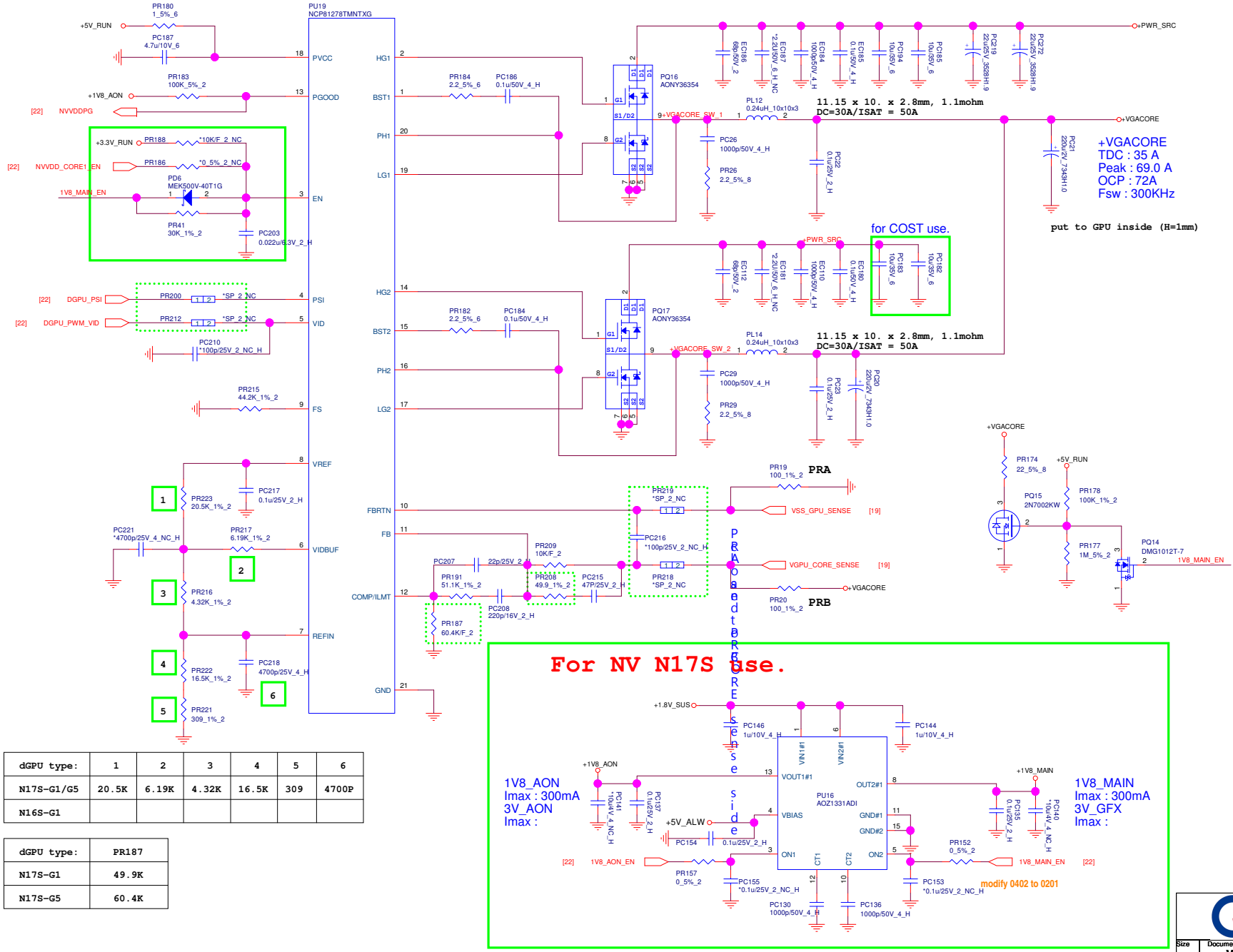
Quanta Computer Inc.
PROJECT : H97M

Size	Document Number	Rev
	1.0V_GFX (TPS62090RGTR)	3A
Date: Monday, April 06, 2020	Sheet 48 of 60	



dGPU type:	1	2	3	4	5	6
N17S-G1/G5	20.5K	6.19K	4.32K	16.5K	309	4700P
N16S-G1						

dGPU type:	PR187
N17S-G1	49.9K
N17S-G5	60.4K

Quanta Computer Inc.

PROJECT : H97M

Size	Document Number	Rev
	VGA CORE (NCP81278TMNTXG)	3A

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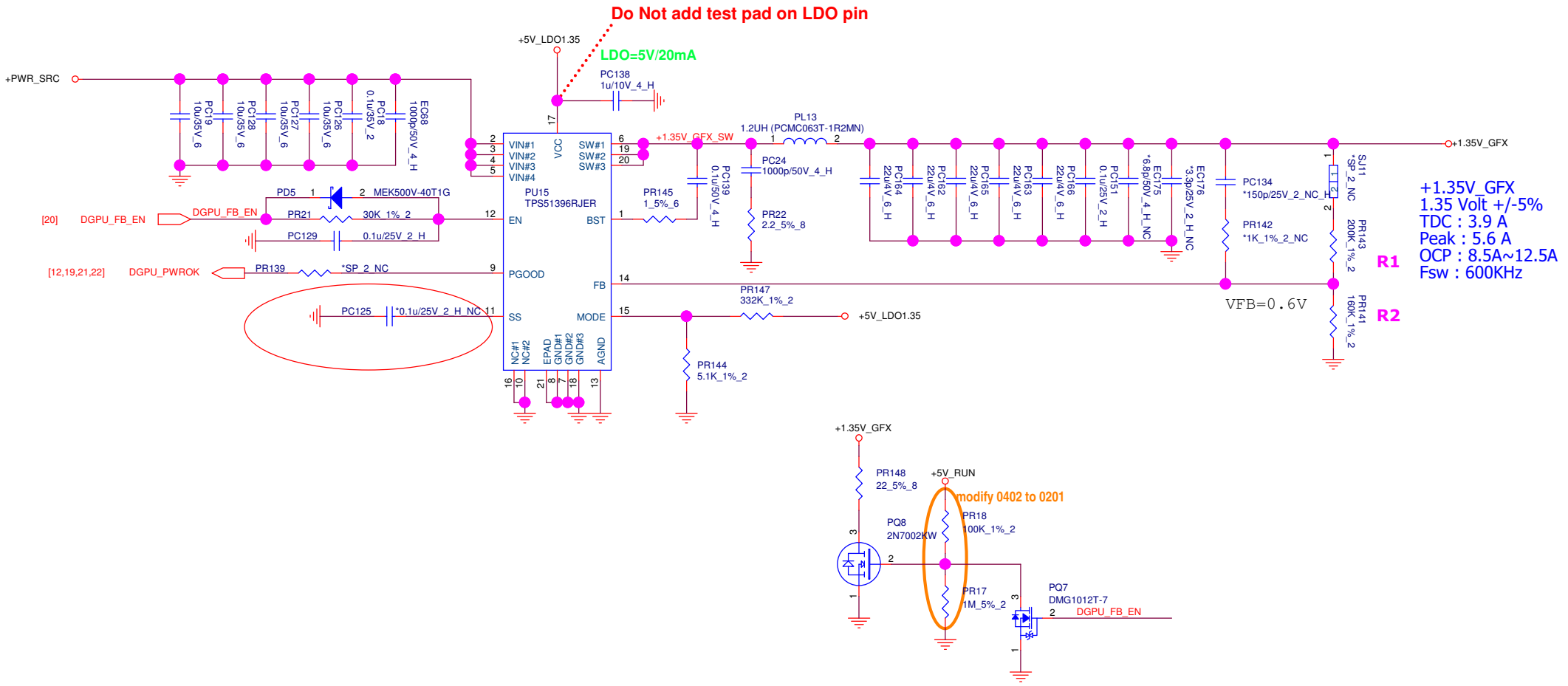
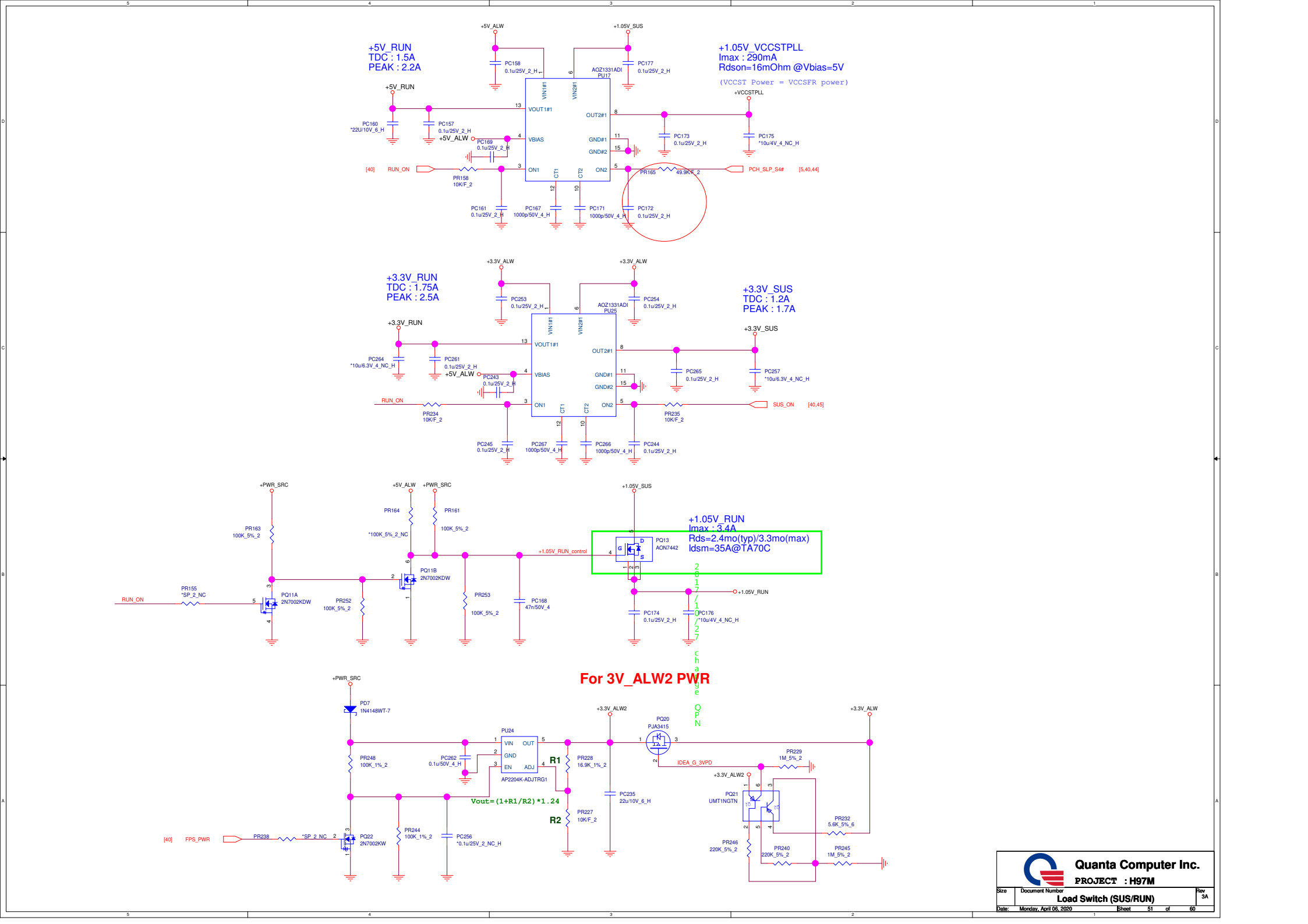


Quanta Computer Inc.		
PROJECT : H97M		
Size	Document Number: +1.35V_GFX (TPS51396RJER)	Rev: 3A
Date: Monday, April 06, 2020	Sheet 50 of 60	


+5V_RUN
TDC : 1.5A
PEAK : 2.2A
+1.05V_VCCSTPLL
Imax : 290mA
Rdson=16mOhm @Vbias=5V
(VCCST Power = VCCSFR power)
AOZ1331ADI
PU17
+3.3V_RUN
TDC : 1.75A
PEAK : 2.5A
+3.3V_SUS
TDC : 1.2A
PEAK : 1.7A
AOZ1331ADI
PU25
+1.05V_RUN
Imax : 3.4A
Rds=2.4mo(typ)/3.3mo(max)
Idsm=35A@TA70C
PQ13
AON7442
2017/11/27 change
For 3V_ALW2 PWR
PU24
AP2204K-ADJTRG1
Vout=(1+R1/R2)*1.24
R1
R2
PQ20
PJA3415
PQ21
UMT1NGTN
PQ22
2N7002KW
PQ11A
2N7002KDW
PQ11B
2N7002KDW
PD7
1N4148WT-7
Quanta Computer Inc.
PROJECT : H97M
Load Switch (SUS/RUN)
Rev 3A
Monday, April 06, 2020
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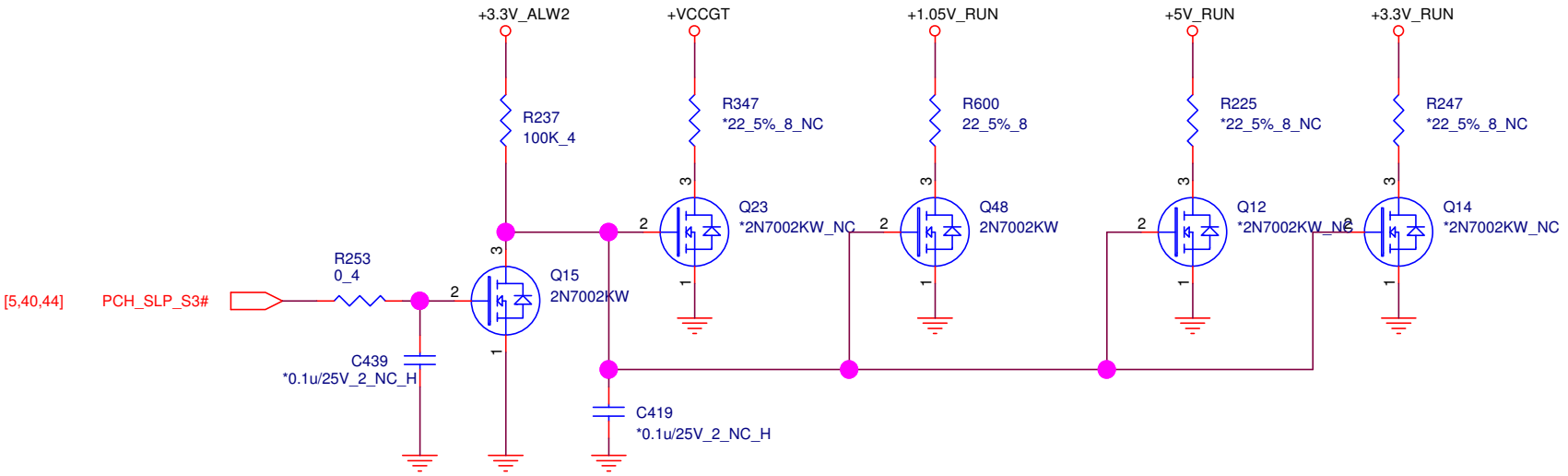

Quanta Computer Inc.

PROJECT : H97M

Size	Document Number	Rev
	Discharge	3A

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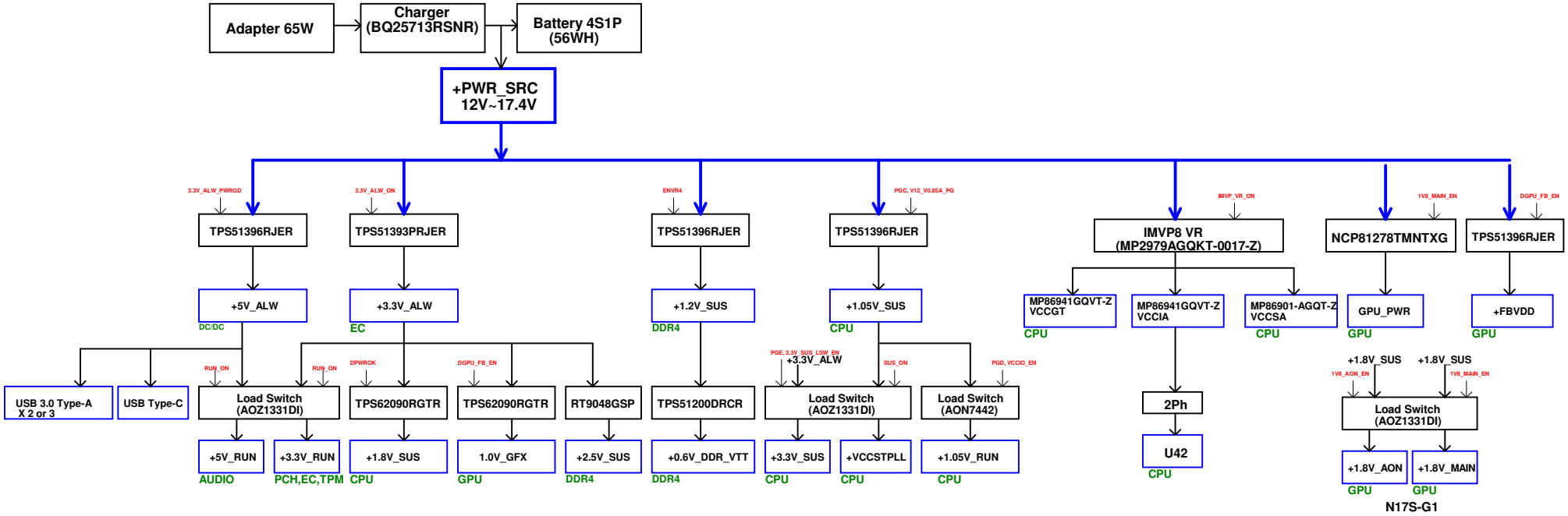
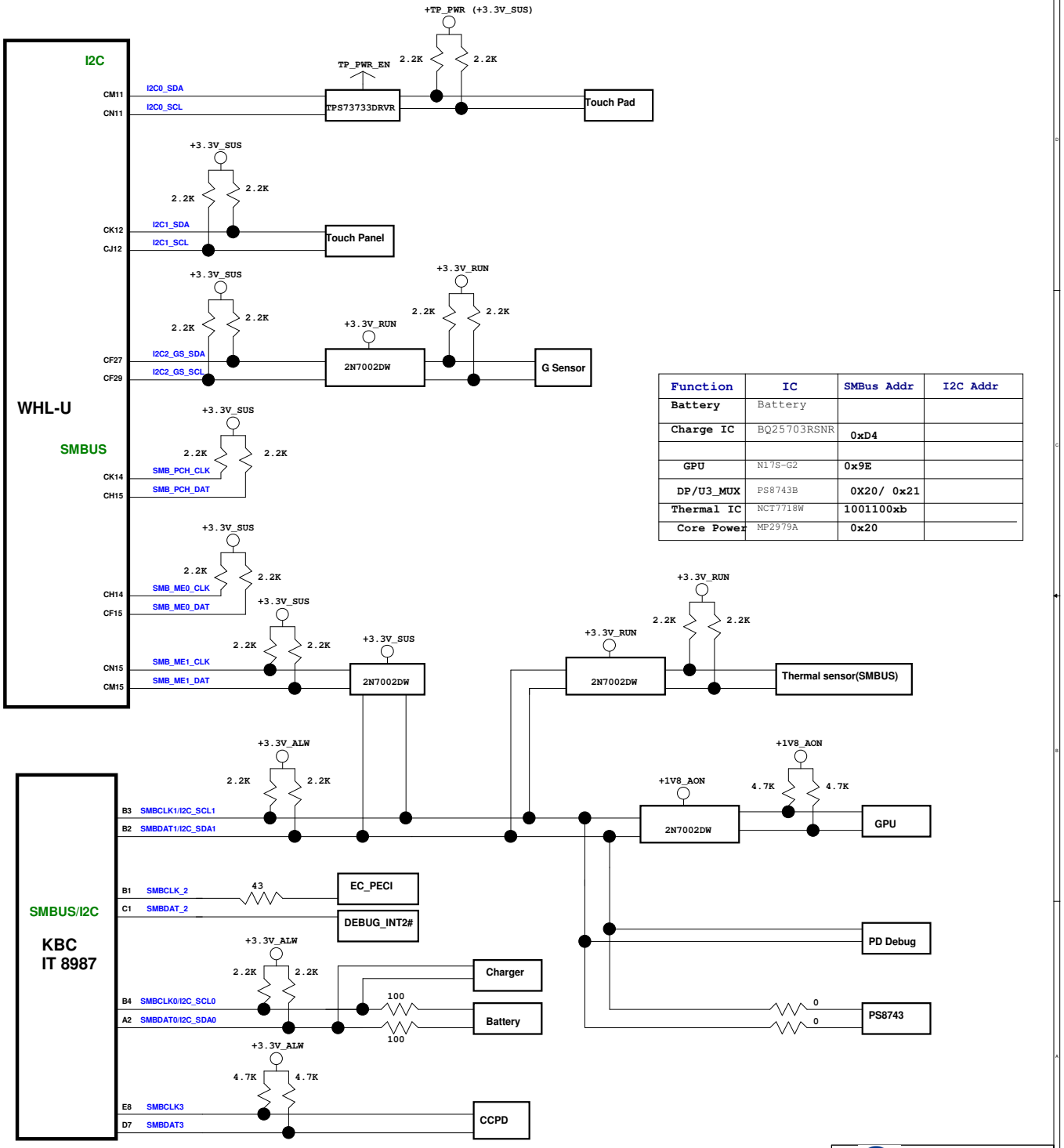


Quanta Computer Inc.
PROJECT : H97M
Power Block Diagram



Function	IC	SMBus Addr	I2C Addr
Battery	Battery		
Charge IC	BQ25703RSNR	0xD4	
GPU	N17S-G2	0x9E	
DP/U3_MUX	PS8743B	0X20/ 0x21	
Thermal IC	NCT7718W	1001100xb	
Core Power	MP2979A	0x20	

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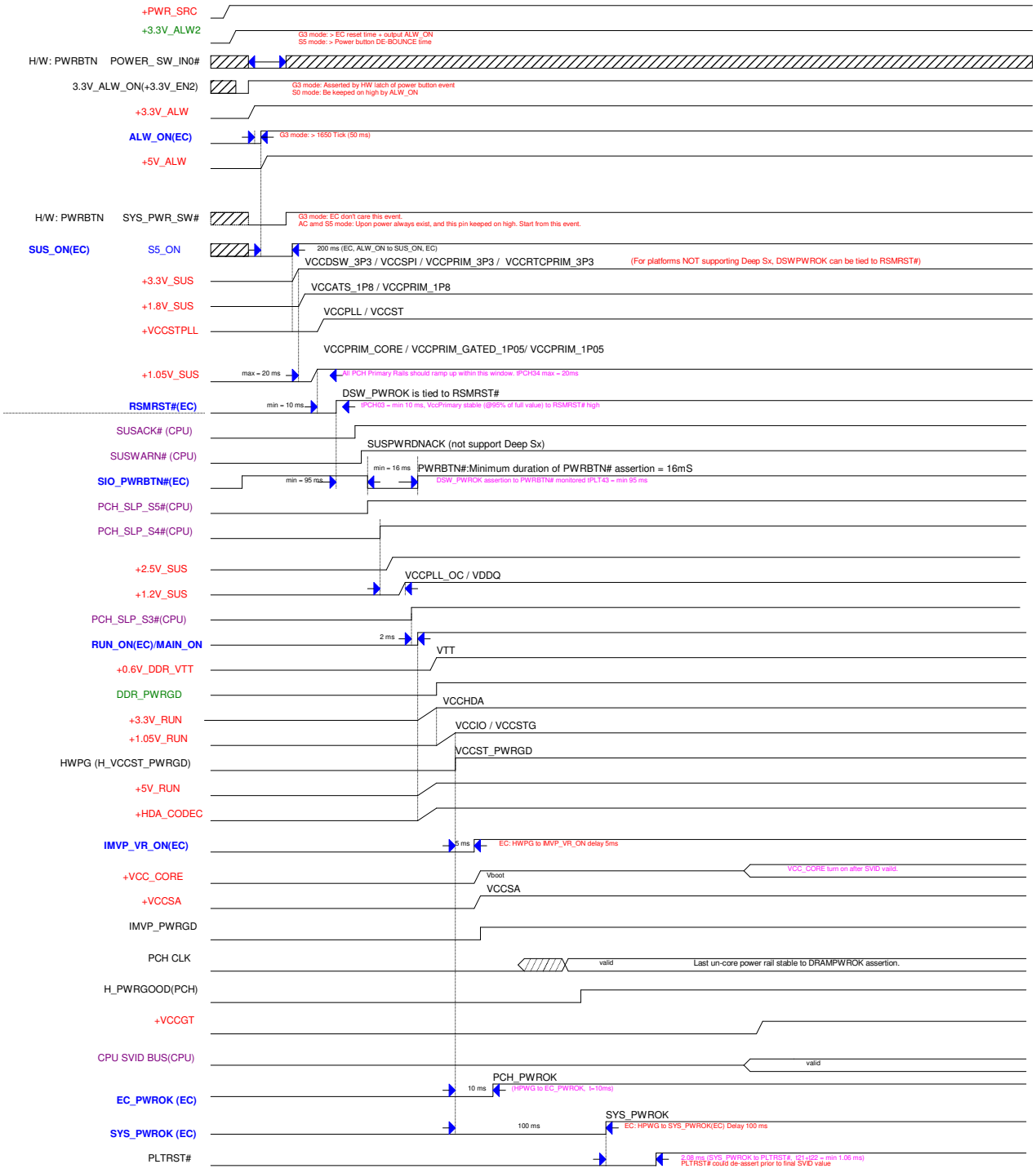
Voltage Rails

Power Rail	Voltage	S0	S3	S5	G3	Ctl Signal	DEVICES
+RTC_VCC	3V	ON	ON	ON	OFF		PCH, EC
+PWR_SRC	19V~7.4V	ON	ON	ON	OFF	Plug in	D to D
+5V_ALW	5V	ON	ON	ON	OFF	ALW_ON	D to D
+3.3V_ALW	3.3V	ON	ON	ON	OFF	+3.3V_EN2	EC
+3.3V_SUS	3.3V	ON	ON	OFF	OFF	SUS_ON	EC,TPM
+1.05V_SUS	1.05V	ON	ON	OFF	OFF	+1.8V_SUS_PWRGD	PCH
+1.8V_SUS	1.8V	ON	ON	OFF	OFF	SUS_ON	PCH
+1.2V_SUS	1.2V	ON	ON	OFF	OFF	+2.5V_SUS	DDR4
+0.6V_DDR_VTT	0.6V	ON	OFF	OFF	OFF	DDR_VTT_CNTL	DDR4
+2.5V_SUS	2.5V	ON	ON	OFF	OFF	PCH_SLP_S4#	DDR4
+VCC_CORE	0.65~1.3V	ON	OFF	OFF	OFF	IMVP_VR_ON	CPU
+VCCSA	1.05V	ON	OFF	OFF	OFF	IMVP_VR_ON	CPU
+VCCGT	0.65~1.3V	ON	OFF	OFF	OFF	IMVP_VR_ON	CPU
+1.05V_RUN	1.05V	ON	OFF	OFF	OFF	RUN_ON	CPU
+5V_RUN	5V	ON	OFF	OFF	OFF	RUN_ON	CODEC,KB
+3.3V_RUN	3.3V	ON/OFF	OFF	OFF	OFF	RUN_ON	PCH,EC
+VGACORE	GPU power	ON/OFF	OFF	OFF	OFF	1V8_MAIN_EN	GPU
+1.35V_GFX	FBVDD	ON/OFF	OFF	OFF	OFF	DGPU_FB_EN	GPU
+1.0V_GFX	1.0V	ON/OFF	OFF	OFF	OFF	DGPU_VC_EN	GPU
+1V8_AON	1.8V	ON/OFF	OFF	OFF	OFF	1V8_AON_EN	GPU
+1V8_MAIN	1.8V	ON/OFF	OFF	OFF	OFF	1V8_MAIN_EN	GPU

PSequence G3 to S0



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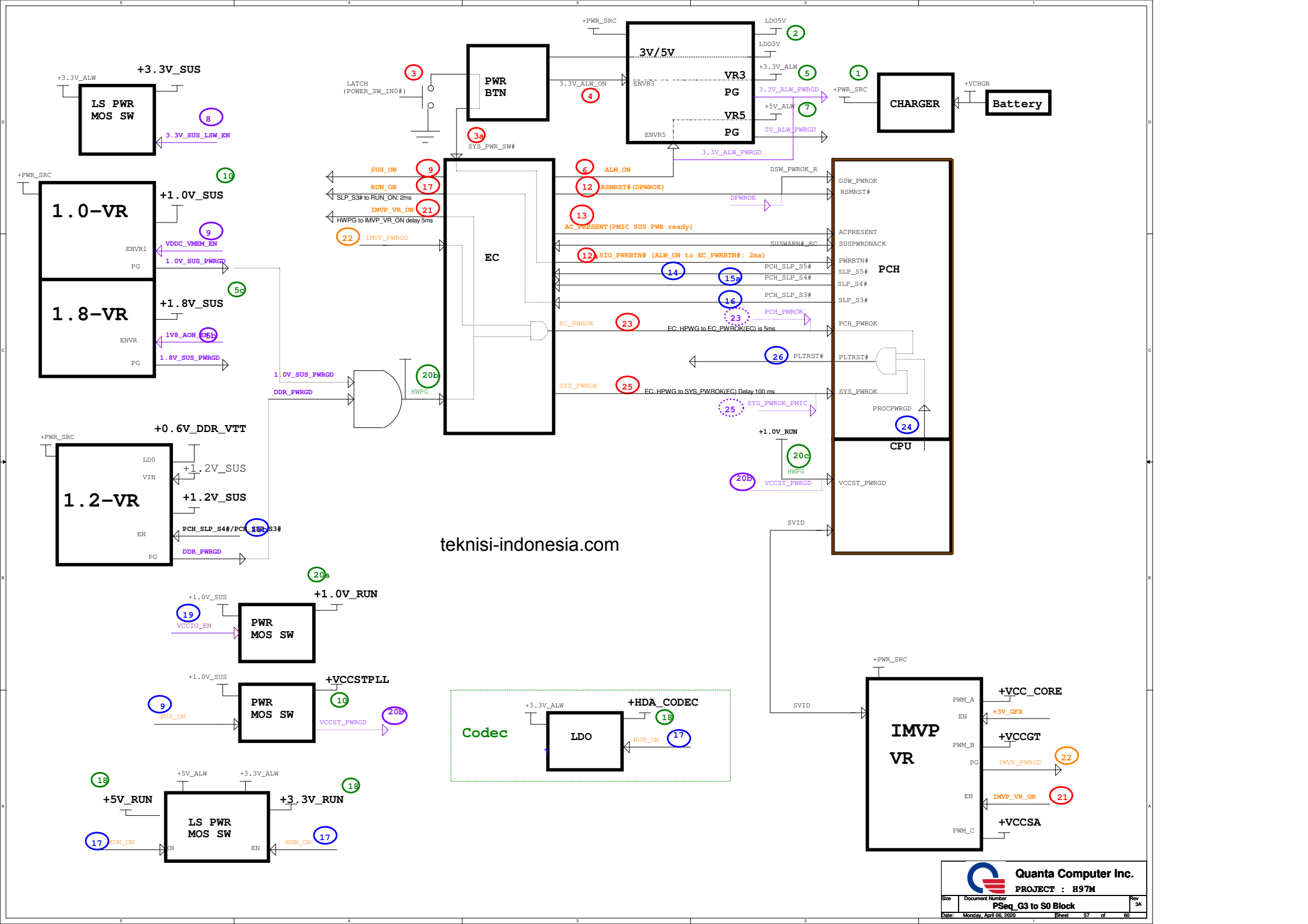
+3.3V_SUS
+3.3V_ALW
LS PWR MOS SW
3.3V_SUS_LSW_EN
+PWR_SRC
1.0-VR
+1.0V_SUS
VDDC_VMEM_EN
1.0V_SUS_PWRGD
ENVR1
PG
1.8-VR
+1.8V_SUS
1V8_AON_EN
1.8V_SUS_PWRGD
ENVR
+0.6V_DDR_VTT
1.2-VR
+1.2V_SUS
LDO
VIN
EN
PCH_SLP_S4#/PCH_SLP_S3#
DDR_PWRGD
1.0V_SUS_PWRGD
DDR_PWRGD
HWPG
LATCH (POWER_SW_IN0#)
PWR BTN
SYS_PWR_SW#
3V/5V
3.3V_ALW_ON
ENVR3
VR3 PG
ENVR5
VR5 PG
LDO5V
LDO3V
+3.3V_ALW
3.3V_ALW_PWRGD
+5V_ALW
5V_ALW_PWRGD
CHARGER
Battery
+VCHGR
SUS_ON
RUN_ON
SLP_S3# to RUN_ON: 2ms
IMVP_VR_ON
HWPG to IMVP_VR_ON delay 5ms
IMVP_PWRGD
EC
ALW_ON
RSMRST#(DPWROK)
DPWROK
AC_PRESENT(PMIC SUS PWR ready)
SUSWARN#_EC
SIO_PWRBTN# (ALW_ON to EC_PWRBTN#: 2ms)
PCH_SLP_S5#
PCH_SLP_S4#
PCH_SLP_S3#
PCH_PWROK
EC_PWROK
EC: HPWG to EC_PWROK(EC) is 5ms
PLTRST#
SYS_PWROK
EC: HPWG to SYS_PWROK(EC) Delay 100 ms
SYS_PWROK_PMIC
DSW_PWROK_R
DSW_PWROK
RSMRST#
ACPRESENT
SUSPWRDNACK
PWRBTN#
SLP_S5#
SLP_S4#
SLP_S3#
PCH
PROCPWRGD
CPU
VCCST_PWRGD
SVID
+1.0V_RUN
PWR MOS SW
VCCIO_EN
+VCCSTPLL
Codec
LDO
+HDA_CODEC
RUN_ON
+5V_RUN
+3.3V_RUN
LS PWR MOS SW
IMVP VR
+PWR_SRC
PWM_A
EN
PWM_B
PG
PWM_C
+VCC_CORE
+3V_GFX
+VCCGT
IMVP_PWRGD
IMVP_VR_ON
+VCCSA
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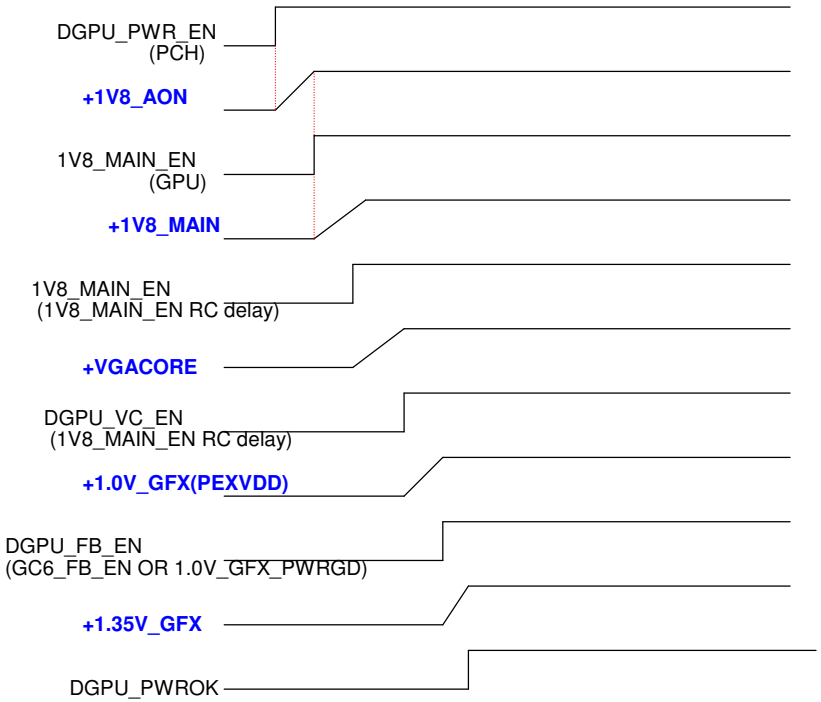
GPU Power UP sequence



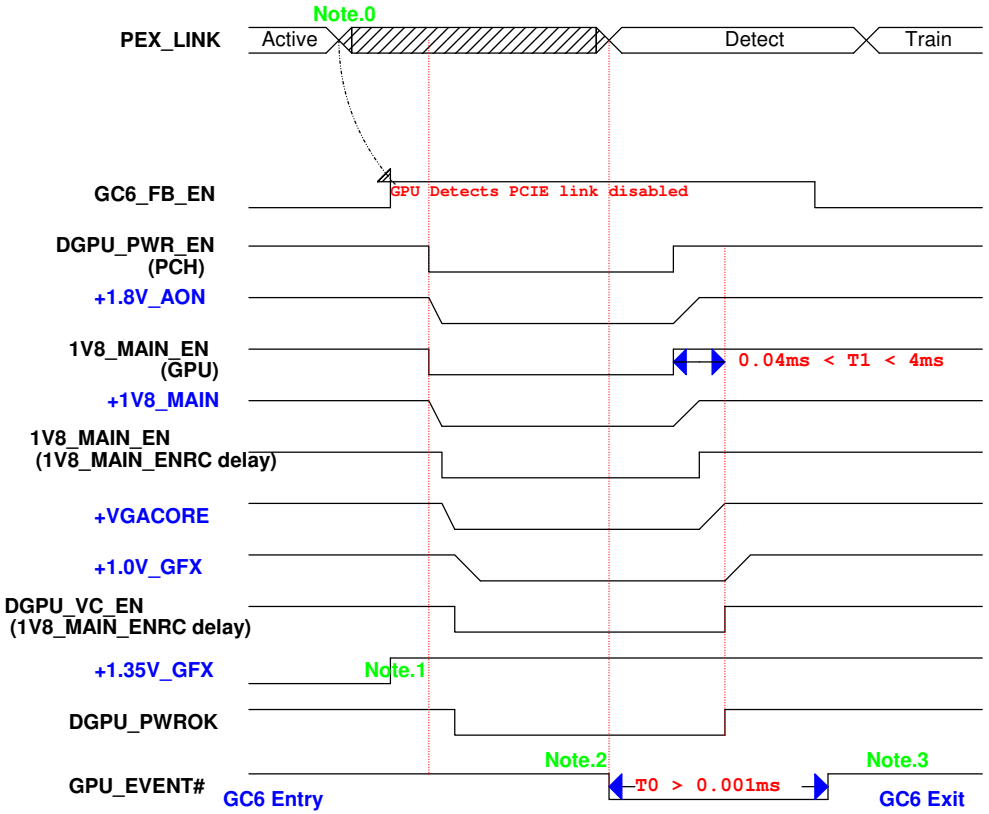
Note:

- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- t1 (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_PGOOD) must NOT exceed 4ms.
- The ramp-up overshoot should not exceed the silicon reliability limit voltage.
- Power up NVVDD must be 90% before PEX_DVDD and NVVDDS can start ramp-up.
- Power up 1V8_AON must be 90% before 3V3 ramp up
- All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU CANNOT have any 3.3V leakage paths before 1V8_AON is present.
- No signal should be applied to the GPU before power rails are fully ramped.
- Refer to the JEDEC Memory Specification for memory-related power sequencing.
- The propagation delay between 1V8_MAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power up and power down.
- FBVDD/Q and 1V8_AON don't need power cycle for GC6 2.1

The following power-down sequence is required:

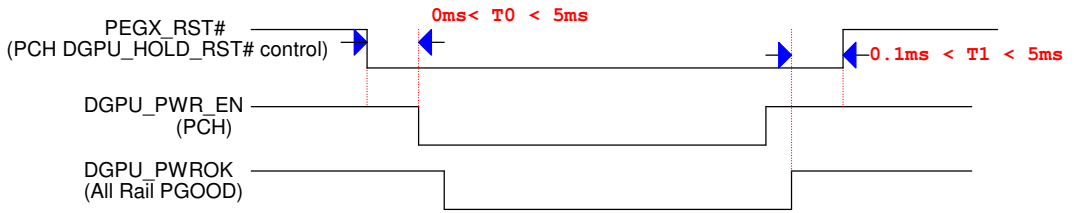
- NVVDDS/PEX_DVDD must power down before NVVDD; all other power rails can power down together with NVVDD.
- 1V8_MAIN must power down after NVVDD powers down.
- The propagation delay between 1V8_MAIN_EN and the NVVDD_EN pin needs to be less than 300us during both power-up and power-down.
- For GDDR5X, VPP must be equal to or higher than FBVDD/Q at all times; use gate logic and discharge circuit as needed.
- All 3.3V devices that connect to the GPU must be ramped down before 1V8_AON; GPU CANNOT have any 3.3V leakage paths after 1.8V_AON and 1.8V_MAIN power-down.
- Power down of NVVDDS and PEX_DVDD must be less than 10% before NVVDD can start ramp-down.
- Power down of 3V3 must be less than 10% before 1V8_AON can start ramp-down.

GPU GC62.1 Entry/Exit sequence



Note.0 : GPU driver ACPI call SBIOS to disables PCIE link.
Note.1 : When GC6 2.0 mode, +1.35V_GFX enabled by GC6_FB_EN
Note.2 : GPU driver ACPI call SBIOS then confirm entry complete by sensing GC6_FB_EN =1, Enable PCIE Link. Then PCH asserts GPU_EVENT#
Note.3 : SBIOS detects GC6_FB_EN =0, then De-asserts GPU_EVENT#
P.S. The entire entry and exit sequence must complete within 200 ms

Optimus GPU On/Off sequence



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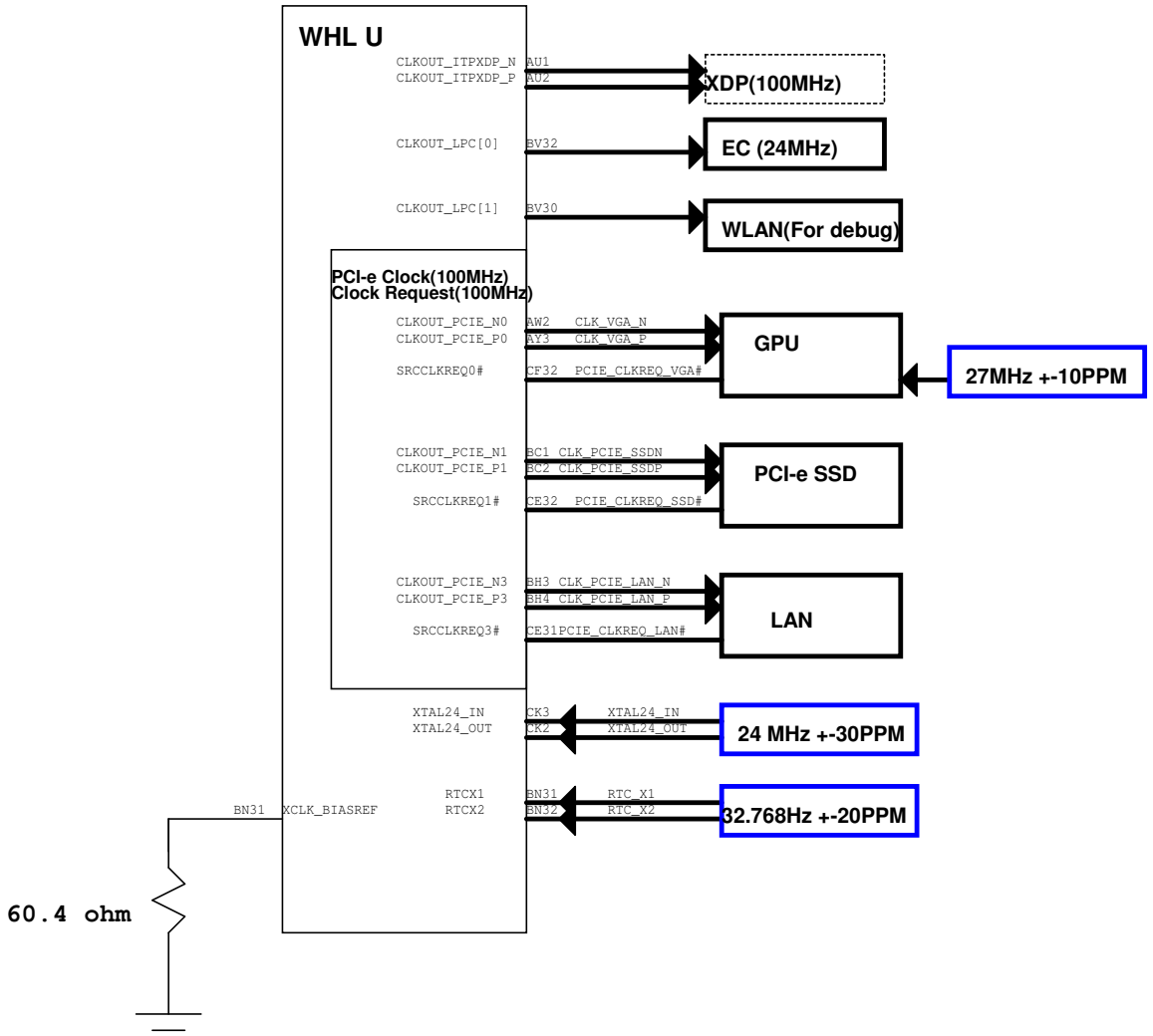

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