MS-7677 Mini ITX Ver: 1.0

Intel -SugarBay plamform

CPU:

INTEL-Sandy bridge LGA1155

System Chipset:

INTEL-Cougar Point

OnBoard Chipset:

HD Audio Codec:RTL889

LAN-Lewisville 82579

SIO:Fintek F171808A

Flash ROM: 64 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X1) Slot * 1

PWM:

VRD12 - ISL6364CR+1Phase

ACPI:

UPI

Other:

SATA(SATA2-300MB/s) *4

USB2.0 *6

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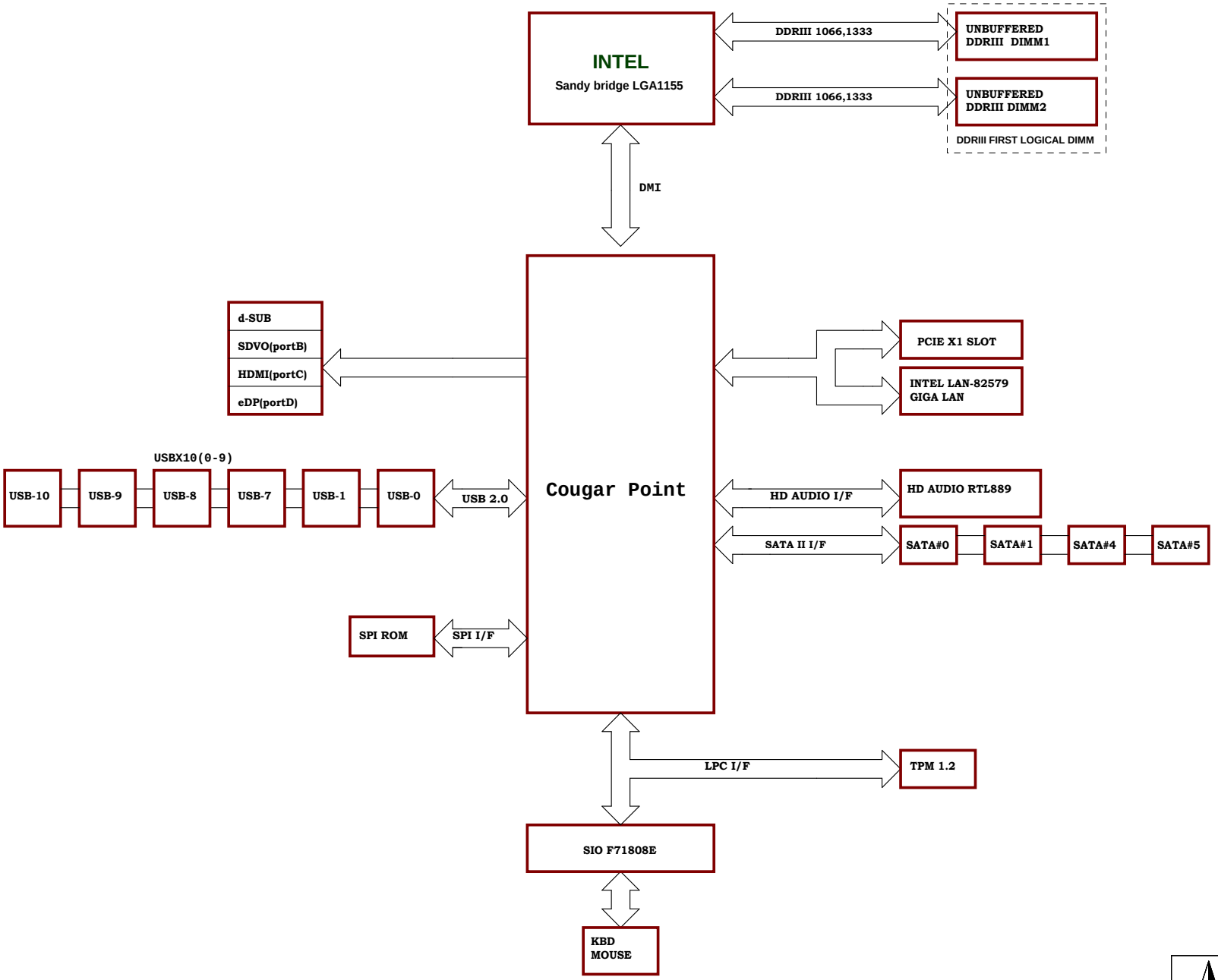

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Size	Document Description	Rev
Custom	Block Diagram	10

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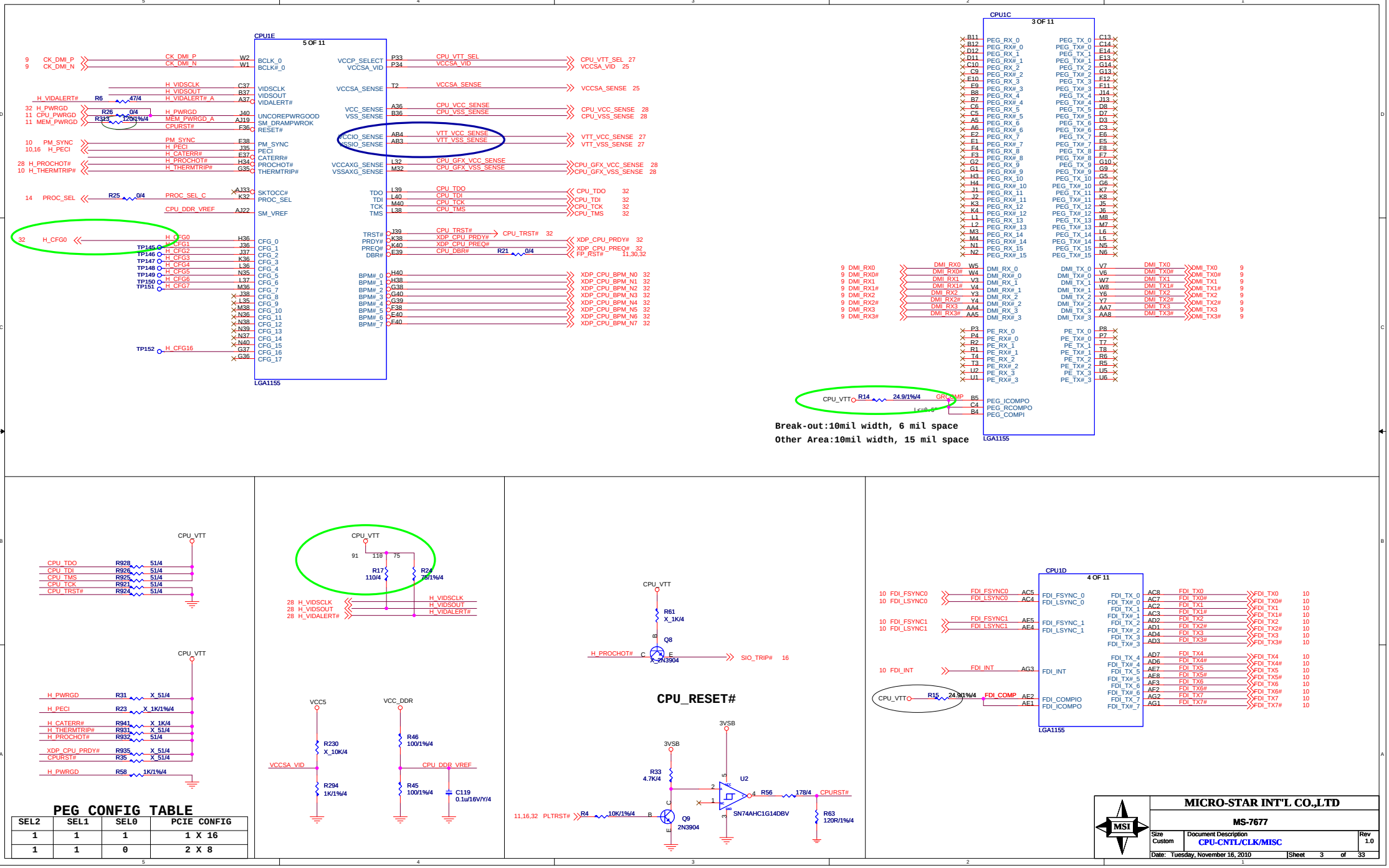
CPU1E
5 OF 11
LGA1155
CPU1C
3 OF 11
LGA1155
Break-out:10mil width, 6 mil space
Other Area:10mil width, 15 mil space
CPU1D
4 OF 11
LGA1155
CPU_RESET#
PEG CONFIG TABLE
SEL2 SEL1 SEL0 PCIE CONFIG
1 1 1 1 X 16
1 1 0 2 X 8
MICRO-STAR INT'L CO.,LTD
MS-7677
CPU-CNTL/CLK/MISC
Size Custom
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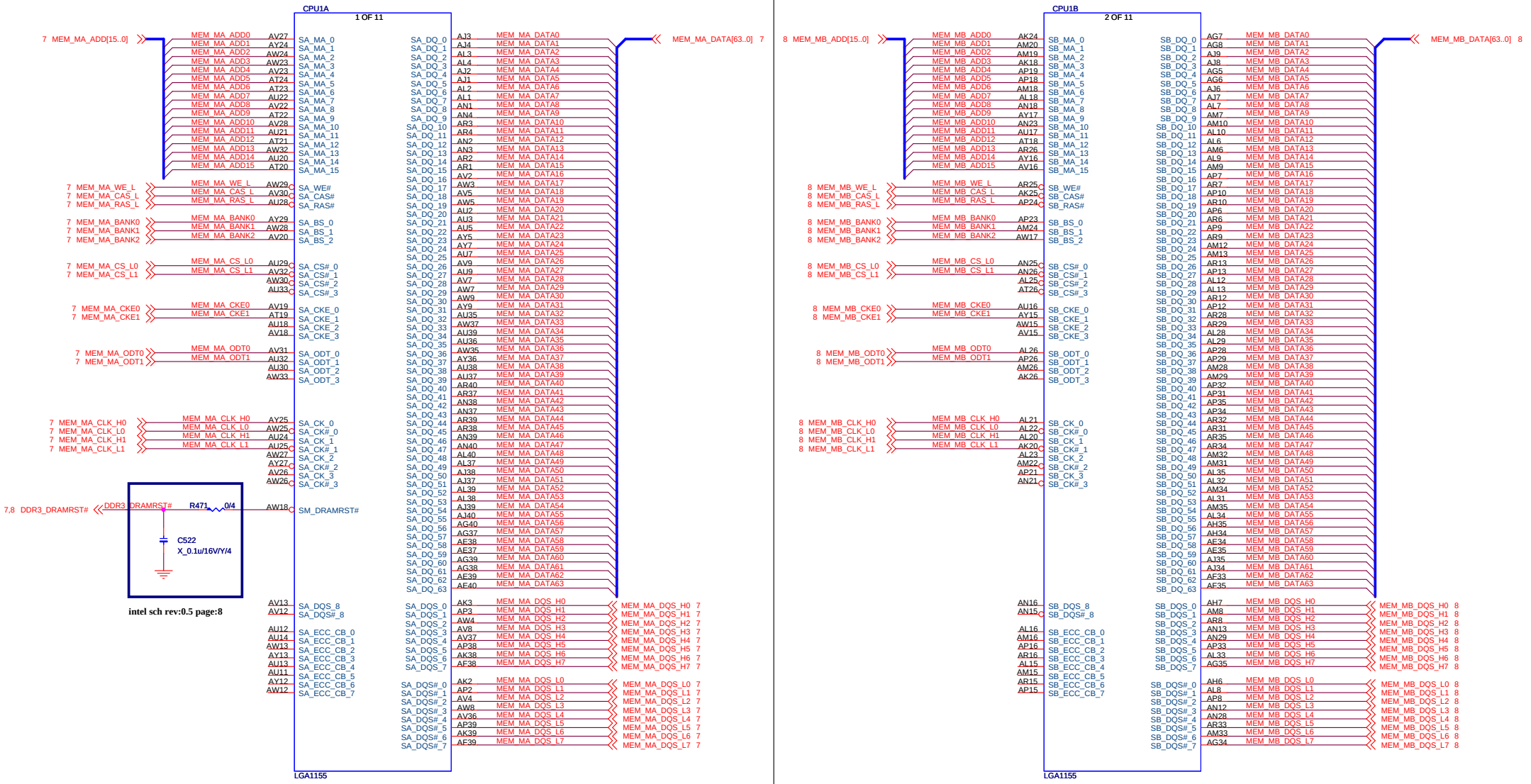

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Model	MS-7677
Size	Custom
Document Description	CPU-Memory
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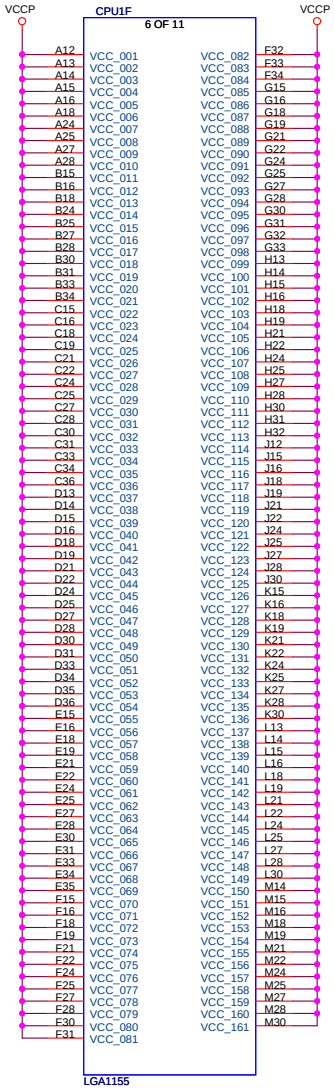
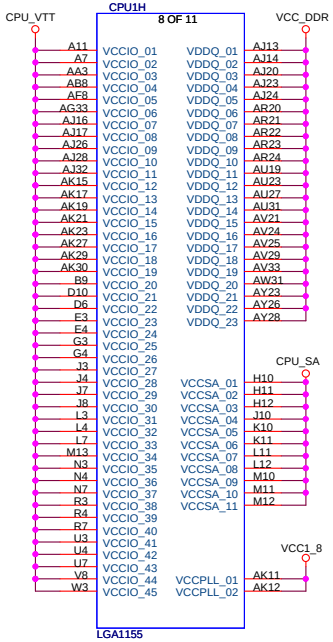
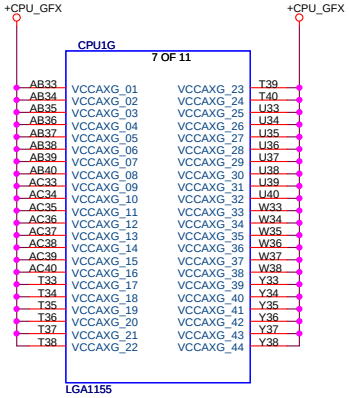
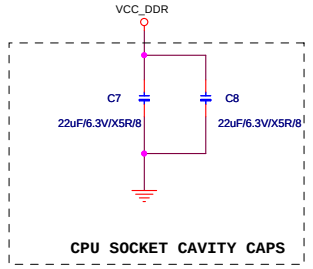


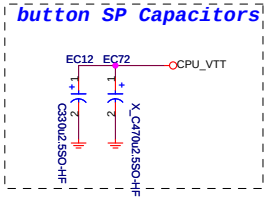


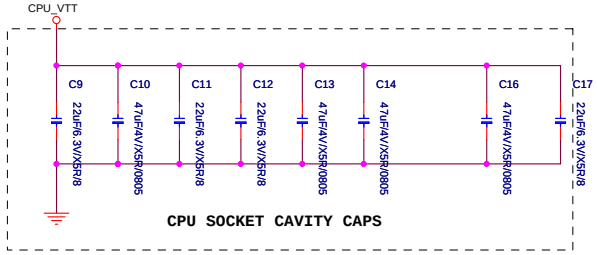


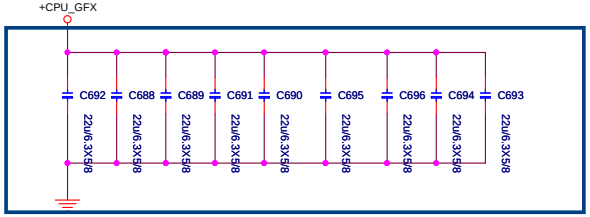
+1.5V_DDR3-Decoupling



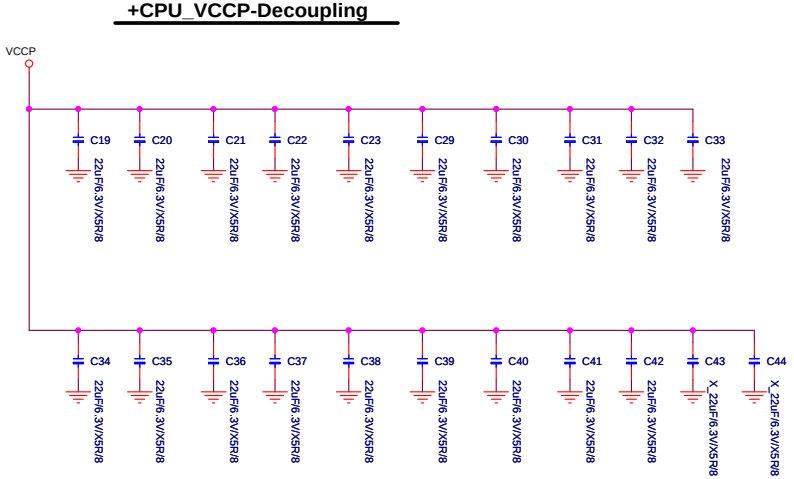
+CPU_VTT Decoupling

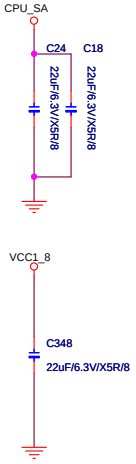






+CPU_VCCP-Decoupling





PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY

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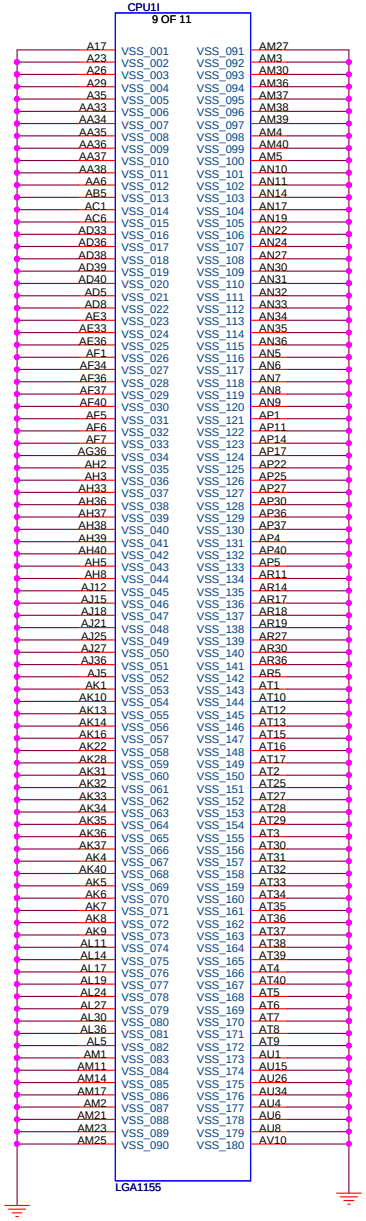

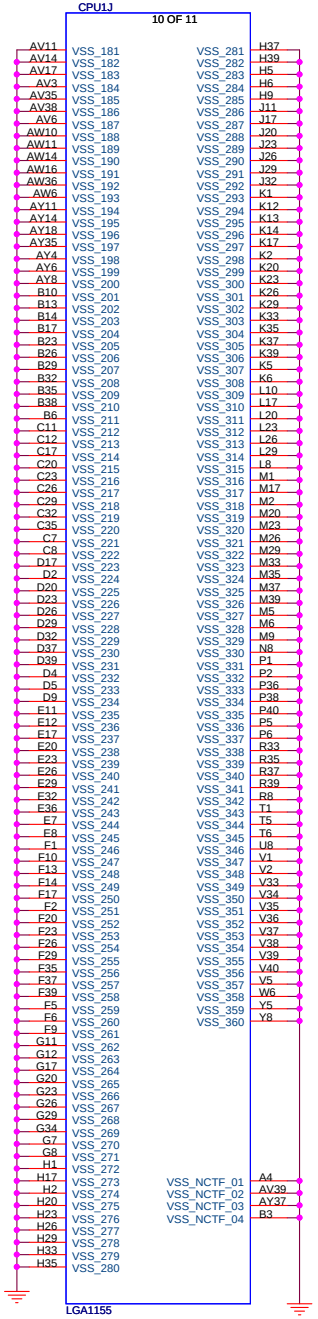

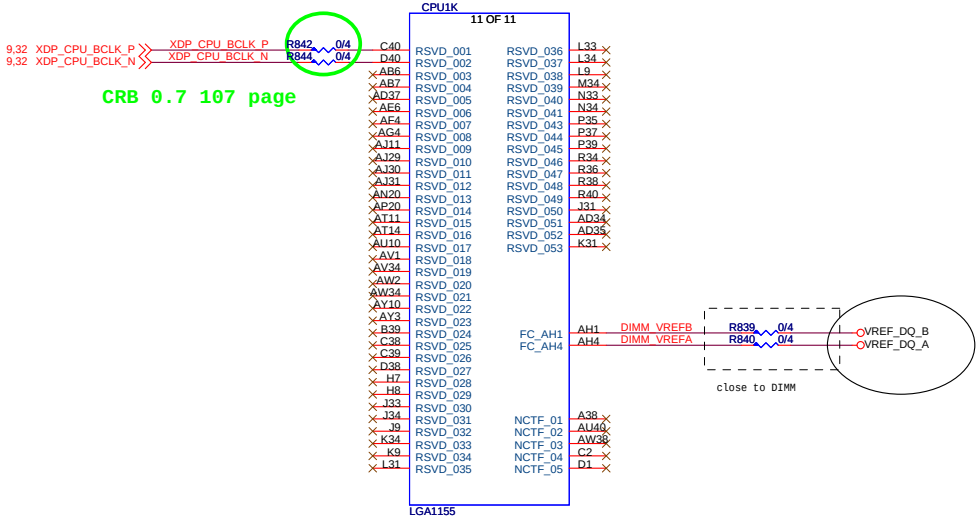

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MS-7677			
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DDRIII DIMM_A0

Place close to DIMM1

VCC_DDR
- C46 2.2u/6
- C47 220P/25V/4
- C48 2.2u/6
- C49 2.2u/6
- C50 0.1u/16V/Y/4
- C51 0.1u/16V/Y/4
- C52 0.1u/16V/Y/4

VREF_CA_A — R27 1K/1%/4 — VCC_DDR
- C102 0.1u/16V/Y/4
- R28 1K/1%/4

VREF_DQ_A — R29 1K/1%/4 — VCC_DDR
- C101 0.1u/16V/Y/4
- R30 1K/1%/4
- C53 2.2u/6

VCC3
- C45 0.1u/16V/Y/4

4 MEM_MA_DATA[63..0] → MEM_MA_DATA[63..0]

VCC_DDR: 51 54 57 60 63 66 69 72 75 78 170 173 176 179 182 185 186 189 191 194 197

VCC3: 236

VTT_DDR: 120 240

68 53 167 79 48 49 187 198

DIMM1

DDR3

MEM_MA_DATA0	3	DQ0	
MEM_MA_DATA1	4	DQ1	
MEM_MA_DATA2	9	DQ2	
MEM_MA_DATA3	10	DQ3	
MEM_MA_DATA4	122	DQ4	
MEM_MA_DATA5	123	DQ5	
MEM_MA_DATA6	128	DQ6	
MEM_MA_DATA7	129	DQ7	
MEM_MA_DATA8	12	DQ8	
MEM_MA_DATA9	13	DQ9	
MEM_MA_DATA10	18	DQ10	
MEM_MA_DATA11	19	DQ11	
MEM_MA_DATA12	131	DQ12	
MEM_MA_DATA13	132	DQ13	
MEM_MA_DATA14	137	DQ14	
MEM_MA_DATA15	138	DQ15	
MEM_MA_DATA16	21	DQ16	
MEM_MA_DATA17	22	DQ17	
MEM_MA_DATA18	27	DQ18	
MEM_MA_DATA19	28	DQ19	
MEM_MA_DATA20	140	DQ20	
MEM_MA_DATA21	141	DQ21	
MEM_MA_DATA22	146	DQ22	
MEM_MA_DATA23	147	DQ23	
MEM_MA_DATA24	30	DQ24	
MEM_MA_DATA25	31	DQ25	
MEM_MA_DATA26	36	DQ26	
MEM_MA_DATA27	37	DQ27	
MEM_MA_DATA28	149	DQ28	
MEM_MA_DATA29	150	DQ29	
MEM_MA_DATA30	155	DQ30	
MEM_MA_DATA31	156	DQ31	
MEM_MA_DATA32	81	DQ32	
MEM_MA_DATA33	82	DQ33	
MEM_MA_DATA34	87	DQ34	
MEM_MA_DATA35	88	DQ35	
MEM_MA_DATA36	200	DQ36	
MEM_MA_DATA37	201	DQ37	
MEM_MA_DATA38	206	DQ38	
MEM_MA_DATA39	207	DQ39	
MEM_MA_DATA40	90	DQ40	
MEM_MA_DATA41	91	DQ41	
MEM_MA_DATA42	96	DQ42	
MEM_MA_DATA43	97	DQ43	
MEM_MA_DATA44	209	DQ44	
MEM_MA_DATA45	210	DQ45	
MEM_MA_DATA46	215	DQ46	
MEM_MA_DATA47	216	DQ47	
MEM_MA_DATA48	99	DQ48	
MEM_MA_DATA49	100	DQ49	
MEM_MA_DATA50	105	DQ50	
MEM_MA_DATA51	106	DQ51	
MEM_MA_DATA52	218	DQ52	
MEM_MA_DATA53	219	DQ53	
MEM_MA_DATA54	224	DQ54	
MEM_MA_DATA55	225	DQ55	
MEM_MA_DATA56	108	DQ56	
MEM_MA_DATA57	109	DQ57	
MEM_MA_DATA58	114	DQ58	
MEM_MA_DATA59	115	DQ59	
MEM_MA_DATA60	227	DQ60	
MEM_MA_DATA61	228	DQ61	
MEM_MA_DATA62	233	DQ62	
MEM_MA_DATA63	234	DQ63	

VSS: 2 5 8 11 14 17 20 23 26 29 32 35 38 41 44 47 80 83 86 89 92 95 98 101 104 107 110 113 116 119 121 124 127 130 133 136 139 142 145 148 151 154 157 160 163 166 199 202 205 208 211 214 217 220 223 226 229 232 235 239

MEC1 MEC2 MEC3 MEC4

VDDSPD: 236

VTT: 120 240

NC/PAR_IN 68
NC/ERR_OUT 53
NC/TEST4 167
RSVD 79
FREE1 48
FREE2 49
FREE3 187
FREE4 198

A0	188	MEM_MA_ADD0
A1	181	MEM_MA_ADD1
A2	61	MEM_MA_ADD2
A3	180	MEM_MA_ADD3
A4	59	MEM_MA_ADD4
A5	58	MEM_MA_ADD5
A6	178	MEM_MA_ADD6
A7	56	MEM_MA_ADD7
A8	177	MEM_MA_ADD8
A9	175	MEM_MA_ADD9
A10/AP	70	MEM_MA_ADD10
A11	55	MEM_MA_ADD11
A12	174	MEM_MA_ADD12
A13	196	MEM_MA_ADD13
A14	172	MEM_MA_ADD14
A15	171	MEM_MA_ADD15

MEM_MA_ADD[15..0] 4

CB0	39	
CB1	40	
CB2	45	
CB3	46	
CB4	158	
CB5	159	
CB6	164	
CB7	165	

DQS0	7	MEM_MA_DQS_H0
DQS0#	6	MEM_MA_DQS_L0
DQS1	16	MEM_MA_DQS_H1
DQS1#	15	MEM_MA_DQS_L1
DQS2	25	MEM_MA_DQS_H2
DQS2#	24	MEM_MA_DQS_L2
DQS3	34	MEM_MA_DQS_H3
DQS3#	33	MEM_MA_DQS_L3
DQS4	85	MEM_MA_DQS_H4
DQS4#	84	MEM_MA_DQS_L4
DQS5	94	MEM_MA_DQS_H5
DQS5#	93	MEM_MA_DQS_L5
DQS6	103	MEM_MA_DQS_H6
DQS6#	102	MEM_MA_DQS_L6
DQS7	112	MEM_MA_DQS_H7
DQS7#	111	MEM_MA_DQS_L7
DQS8	43	
DQS8#	42	

MEM_MA_DQS_H0 4
MEM_MA_DQS_L0 4
MEM_MA_DQS_H1 4
MEM_MA_DQS_L1 4
MEM_MA_DQS_H2 4
MEM_MA_DQS_L2 4
MEM_MA_DQS_H3 4
MEM_MA_DQS_L3 4
MEM_MA_DQS_H4 4
MEM_MA_DQS_L4 4
MEM_MA_DQS_H5 4
MEM_MA_DQS_L5 4
MEM_MA_DQS_H6 4
MEM_MA_DQS_L6 4
MEM_MA_DQS_H7 4
MEM_MA_DQS_L7 4

DM0/DQS9	125
NC/DQS9#	126
DM1/DQS10	134
NC/DQS10#	135
DM2/DQS11	143
NC/DQS11#	144
DM3/DQS12	152
NC/DQS12#	153
DM4/DQS13	203
NC/DQS13#	204
DM5/DQS14	212
NC/DQS14#	213
DM6/DQS15	221
NC/DQS15#	222
DM7/DQS16	230
NC/DQS16#	231
DM8/DQS17	161
NC/DQS17#	162

ODT0	195	MEM_MA_ODT0
ODT1	77	MEM_MA_ODT1
CKE0	50	MEM_MA_CKE0
CKE1	169	MEM_MA_CKE1
CS0#	193	MEM_MA_CS_L0
CS1#	76	MEM_MA_CS_L1
BA0	71	MEM_MA_BANK0
BA1	190	MEM_MA_BANK1
BA2	52	MEM_MA_BANK2

MEM_MA_ODT0 4
MEM_MA_ODT1 4
MEM_MA_CKE0 4
MEM_MA_CKE1 4
MEM_MA_CS_L0 4
MEM_MA_CS_L1 4
MEM_MA_BANK0 4
MEM_MA_BANK1 4
MEM_MA_BANK2 4

WE#	73	MEM_MA_WE_L
RAS#	192	MEM_MA_RAS_L
CAS#	74	MEM_MA_CAS_L
RESET#	168	DDR3_DRAMRST#

MEM_MA_WE_L 4
MEM_MA_RAS_L 4
MEM_MA_CAS_L 4
DDR3_DRAMRST# 4,8

CK0	184	MEM_MA_CLK_H0
CK0#	185	MEM_MA_CLK_L0
CK1(NU)	63	MEM_MA_CLK_H1
CK1#(NU)	64	MEM_MA_CLK_L1

MEM_MA_CLK_H0 4
MEM_MA_CLK_L0 4
MEM_MA_CLK_H1 4
MEM_MA_CLK_L1 4

VREFDQ	1	VREF_DQ_A
VREFCA	67	VREF_CA_A
SCL	118	SMBCLK_DDR
SDA	238	SMBDATA_DDR
SA1	237	
SA0	117	

C54 0.1u/16V/Y/4
C55 0.1u/16V/Y/4

DDEIII-240_BLUE-R

DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

8 SMBCLK_DDR → SMBCLK_DDR R34 33/4 → SMBCLK 11,15,18,25,32

8 SMBDATA_DDR → SMBDATA_DDR R36 33/4 → SMBDATA 11,15,18,25,32

MSI

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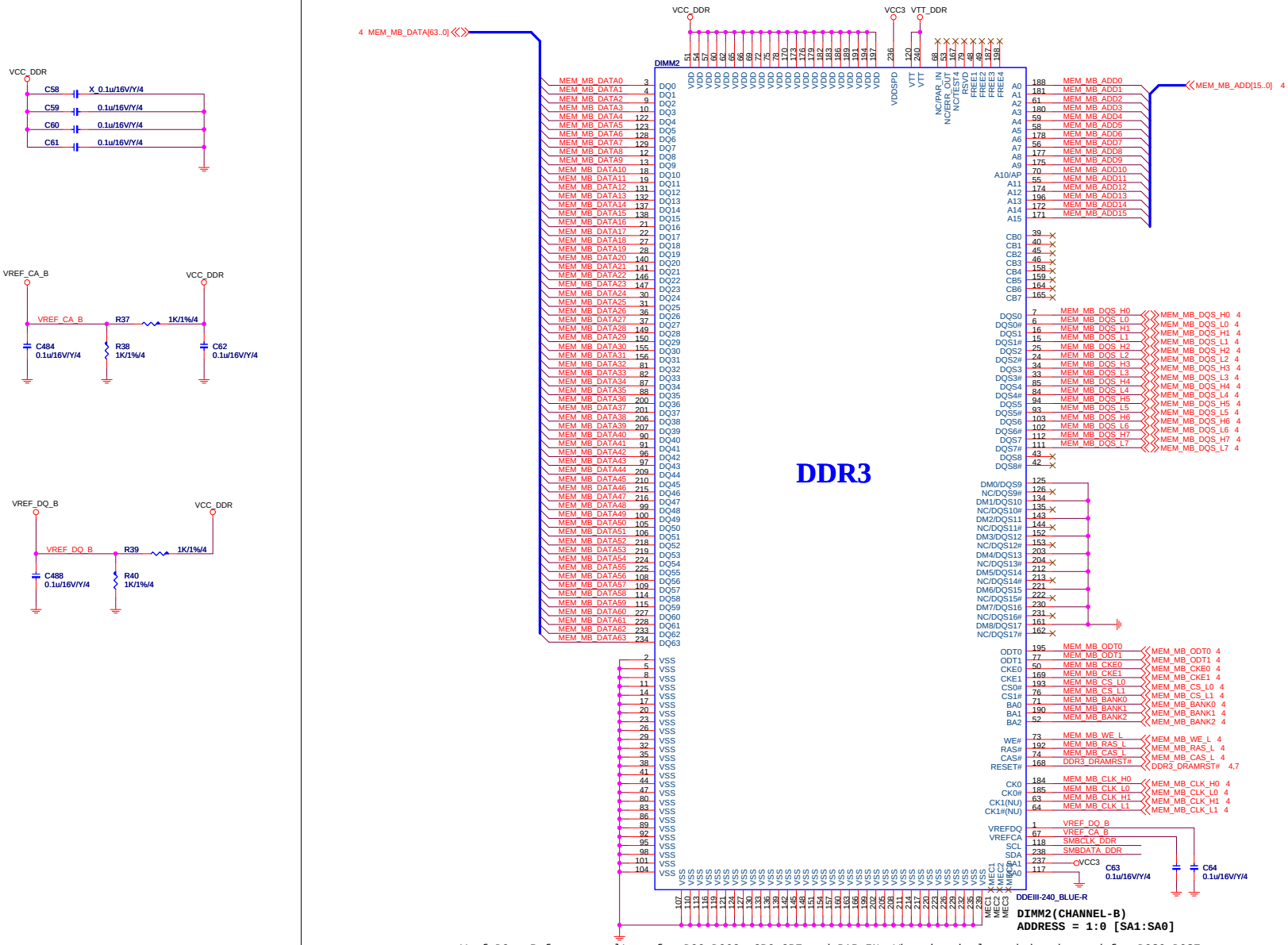
DDRIII DIMM_B0



Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.

Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

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MS-7677		
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CGPT1B
2 OF 9
PCI-E
USB
DMI
Cougar Point
CGPT1G
7 OF 9
CLOCK
CLOCK_IN
Programmable output clock to 48MHZ
Cougar Point
PCICLK LOOPBACK
CGPT1A
1 OF 9
PCI
Cougar Point
no clock gen pull down
For PCH XDP
Place near SB
MICRO-STAR INT'L CO.,LTD
MS-7677
CP PCI/E/DMI/USB/CLK
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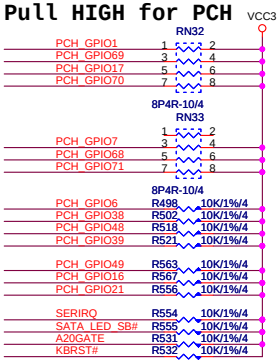
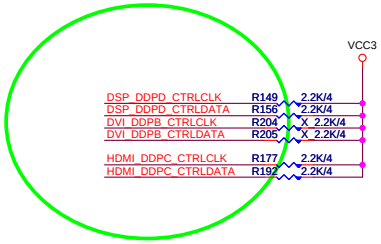
Pull HIGH for PCH



GPIO FOR BIOS

No VGA(pull down)

Enable VGA (CTRLCLK/DATA PULL HIGH)



MICRO-STAR INT'L CO.,LTD	
MS-7677	
Size: Custom	Document Description: CP SATA/HOST/FAN/GPIO/VGA
Rev: 1.0	
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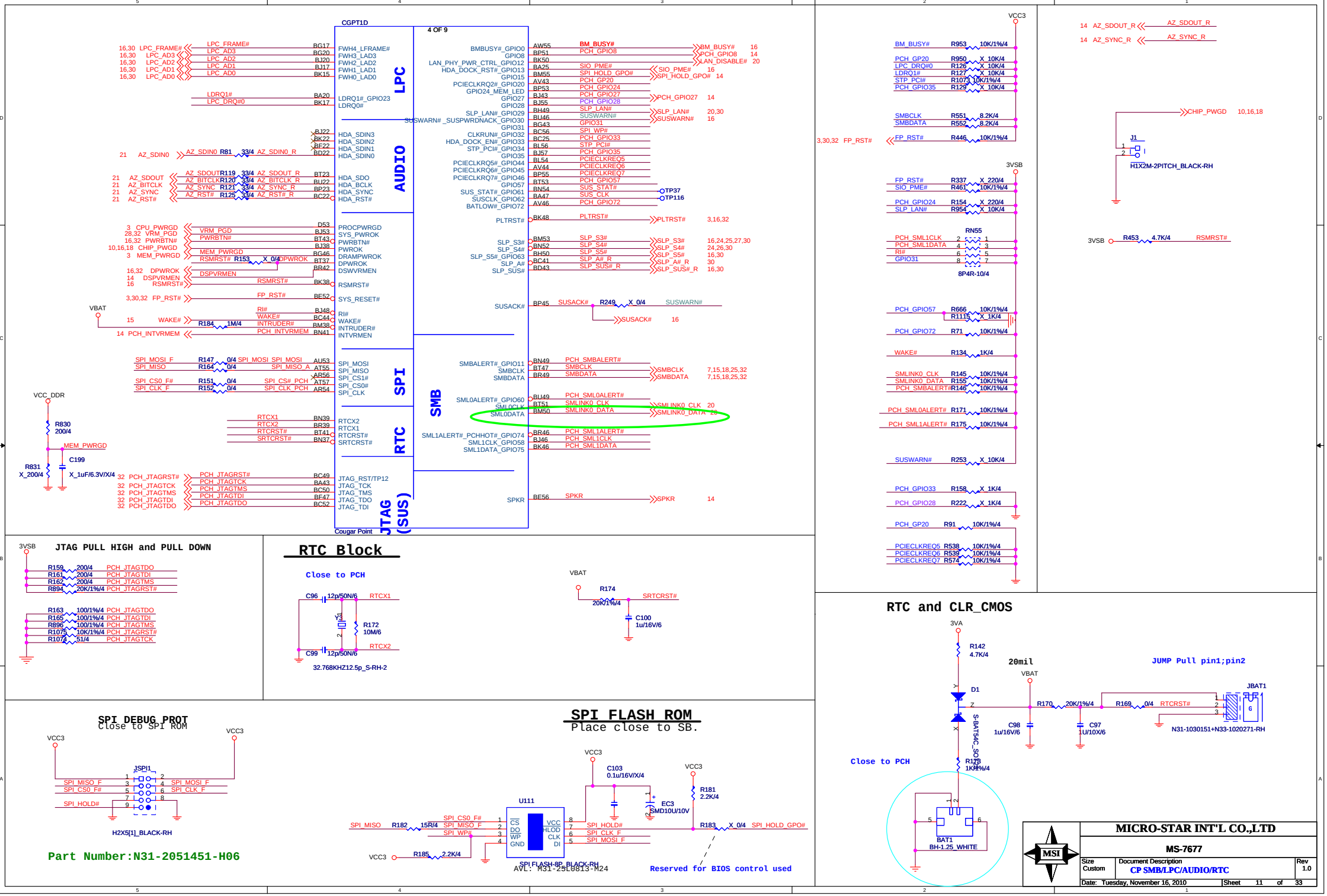

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Custom	CP SMB/LPC/AUDIO/RTC	1.0

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Table 3-7. VCCPLL Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Electrolytic 220µF	1	77mΩ	3.3nH	Output	North of processor - as close to RM keep-out as possible	1
10µF 0805 X5R	1	3mΩ	0.51nH	Output		1,2,3

Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

PCH_1P05
L1 X_1uH/50mA/0.4Ohm/8
VCCAFDIPLL
C105 10uF/6.3V/X5R/8
R255 X_0/4 VCCACLK NO THIS PIN
R194 X_0/8 VCCAPLLDMI2
C195 X_10uF/6.3V/X5R/8
C194 X_1uF/6.3V/X5R/4
R196 0/8 VCCCLKDMI
C197 10uF/6.3V/X5R/8
C196 1uF/6.3V/X4
R187 0/8 VCCA_DPLLA
EC4 100u/16V/6.3*5/O
C108 1uF/6.3V/X/4
R188 0/8 VCCA_DPLLB
EC5 100u/16V/6.3*5/O
C109 1uF/6.3V/X/4

PCH_1P05
DMI PLL FILTER
L28 X_L1U_500mA_0805
VCCAPLLEXP
C114 X_10uF/6.3V/X5R/8
C198 X_1uF/6.3V/X5R/4
SATA PLL FILTER
L29 X_L10U_100mA_0805
VCCAPLLSATA
C115 X_10uF/6.3V/X5R/8
C116 X_1uF/6.3V/X5R/4

5VREF & 5VREF_SUS Sequencing Circuit

VCC3 — Q63 2N3904 — C759 1u/6.3V/4 — VCC5 — R975 10/4 — 5VREF
3VSB — Q64 2N3904 — C764 0.1u/16V/X/4 — 5VSB — R969 100/1%/4 — 5VREF_SUS
ATX_5VSB — R972 X_100/1%/4

VCC3 — CP18 X_COPPER — +3.3V_DAC
Near ball AF1
C118 0.1u/16X7R/4

POWER

CGPT1H 8 OF 9 — Cougar Point

C171 1uF/6.3V/X/4, 10uF/6.3V/X5R/8
C175 1uF/6.3V/X/4, 10uF/6.3V/X5R/8
C354
C355 10uF/6.3V/X5R/8
C150 1uF/6.3V/X/4
C149 1uF/6.3V/X/4 C151
C113 1uF/6.3V/X/4
PCH_1P05

C167 4.7u/6.3X5/6
C166 0.1u/16V/Y/4
CPU_VTT — D55 V_PROC_IO, B56 V_PROC_IO_NCTF
CPU_VTT — B41 VCCDMI_02, E41 VCCDMI_01
C110 1uF/6.3V/X/4 — VCCAPLLDMI2 A19, VCCCLKDMI AJ20
5VREF BF1, 5VREF_SUS BT25
+3.3V_DAC — VCCACLK AT1, AL5
VCCA_DPLLA AB1, VCCA_DPLLB AC2
VCCAPLLSATA U56
VCCAPLLEXP B53
VCCAFDIPLL C54
C148 0.1u/16V/Y/4, C168 1uF/6.3V/X/4 — 3VSB — AV28 VCCSUSHDA
VCC3 — AN52 VCCSPI
VCC1_8 — R197 0/8 — R2 VCCVRM_04, R54 VCCVRM_03, R56 VCCVRM_02, AJ1 VCCVRM_01
C121 1uF/6.3V/X/4 — DCPSUS A39, TP120 AT41, TP119 AA32 — DCPSUS_03, DCPSUS_02, DCPSUS_01
C122 0.1u/16X7R/4 — DCPRTC BR54, BT56 — DCPRTC, DCPRTC_NCTF
TP121 AV41 — DCPSUSBYP
C123 0.1u/16X7R/4 — DCPSST BA46 — DCPSST
C165 0.1u/16V/Y/4, C161 1uF/6.3V/X/4 — VBAT, 3VA — BU42 VCCRTC, AV40 VCCDSW3_3
C155 0.1u/16X7R/4
PCH_1P05 — AG15 VCCDIFFCLKN_03, AE17 VCCDIFFCLKN_02, AE15 VCCDIFFCLKN_01
C174 1uF/6.3V/X/4
PCH_1P05 — CP17 X_COPPER — VCCSSC — AE20 VCCSSC_02, AC20 VCCSSC_01
C173 1uF/6.3V/X/4
VCCNAND — R189 0/6, R190 X_0/6 — VCC1_8, VCC3
VCCDFTERM T57, T55 — VCCNAND

VCC3_3_10 AV20, VCC3_3_09 AU20, VCC3_3_08 A12, VCC3_3_07 AU22, VCC3_3_06 AU38, VCC3_3_05 BD20, VCC3_3_04 BD17, VCC3_3_03 BC17, VCC3_3_02 AE57, VCC3_3_01
C170 1uF/6.3V/X/4
C177 0.1u/16V/Y/4
C152 1uF/6.3V/X/4 — VCC3
C158 0.1u/16V/Y/4, C157 0.1u/16V/Y/4, C124 0.1u/16V/Y/4

VCCSUS3_3_011 BT35, VCCSUS3_3_010 AU38, VCCSUS3_3_009 AT40, VCCSUS3_3_008 BM36, VCCSUS3_3_007 BK36, VCCSUS3_3_006 BJ36, VCCSUS3_3_005 AY33, VCCSUS3_3_004 AY31, VCCSUS3_3_003 AY32, VCCSUS3_3_002 AY30, VCCSUS3_3_001 U31
3VSB
C147 0.1u/16V/Y/4
C153 2.2u/6.3X5/4
C154 2.2u/6.3X5/4
C156 0.1u/16V/Y/4

PCH_1P05
VCCCORE_022 AR34, VCCCORE_021 AR32, VCCCORE_020 AN34, VCCCORE_019 AN32, VCCCORE_018 AL34, VCCCORE_017 AL32, VCCCORE_016 AJ36, VCCCORE_015 AJ34, VCCCORE_014 AJ32, VCCCORE_013 AG34, VCCCORE_012 AG32, VCCCORE_011 AE36, VCCCORE_010 AE34, VCCCORE_009 AE32, VCCCORE_008 AE30, VCCCORE_007 AE28, VCCCORE_006 AE24, VCCCORE_005 AC32, VCCCORE_004 AC30, VCCCORE_003 AC28, VCCCORE_002 AC26, VCCCORE_001 AC24
C172 1uF/6.3V/X/4

VCCASW_023 AU36, VCCASW_022 AU30, VCCASW_021 AR38, VCCASW_020 AR36, VCCASW_019 AR30, VCCASW_018 AR28, VCCASW_017 AR26, VCCASW_016 AR24, VCCASW_015 AN28, VCCASW_014 AN26, VCCASW_013 AN24, VCCASW_012 AN22, VCCASW_011 AL28, VCCASW_010 AL24, VCCASW_009 AJ28, VCCASW_008 AJ26, VCCASW_007 AJ24, VCCASW_006 AG28, VCCASW_005 AG26, VCCASW_004 AG24, VCCASW_003 AU34, VCCASW_002 AV36, VCCASW_001 AU32
C169 1uF/6.3V/X/4
C178 1uF/6.3V/X/4

PCH decoupling cap

VBAT — C342 0.1u/16V/Y/4, C343 1uF/10V/Y5V/6
CPU_VTT — C136 4.7u/10V/X5R/8, C132 0.1u/16V/Y/4, C341 0.1u/16V/Y/4
3VSB — C130 0.1u/16V/Y/4, C131 0.1u/16V/Y/4
PCH_1P05 — C336 1uF/10V/Y5V/6, C133 1uF/10V/Y5V/6, C134 10uF/6.3V/X5R/8, C135 4.7u/10V/X5R/8, C340 10uF/6.3V/X5R/8, C137 1uF/10V/Y5V/6, C138 0.1u/16V/Y/4, C139 X_0.1u/16V/Y/4, C140 X_0.1u/16V/Y/4, C141 0.1u/16V/Y/4

VCC3 — C125 0.1u/16V/Y/4, C126 X_0.1u/16V/Y/4, C127 X_0.1u/16V/Y/4, C128 X_0.1u/16V/Y/4, C129 0.1u/16V/Y/4, C337 4.7u/10V/X5R/8, C338 1uF/10V/Y5V/6

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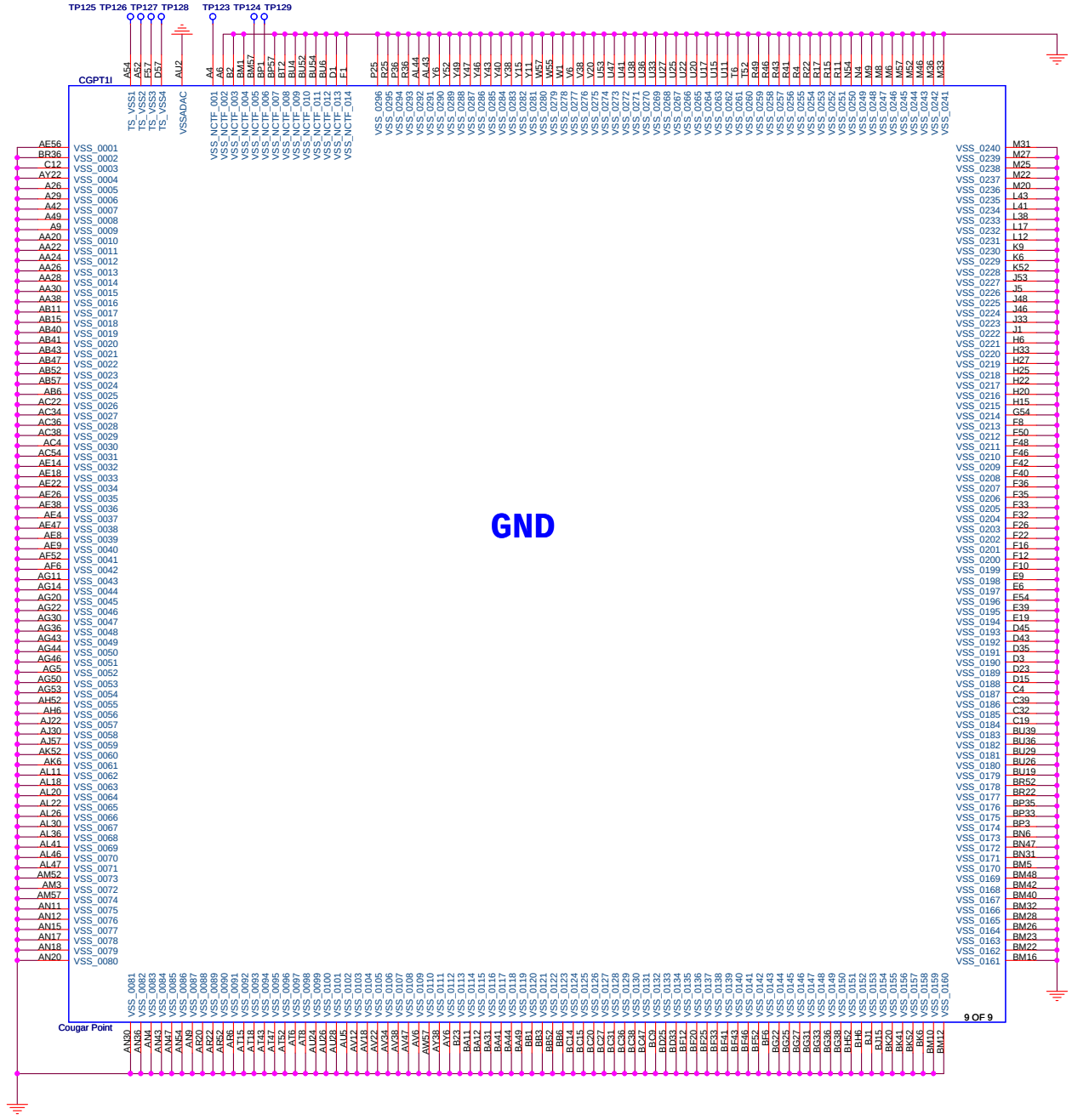
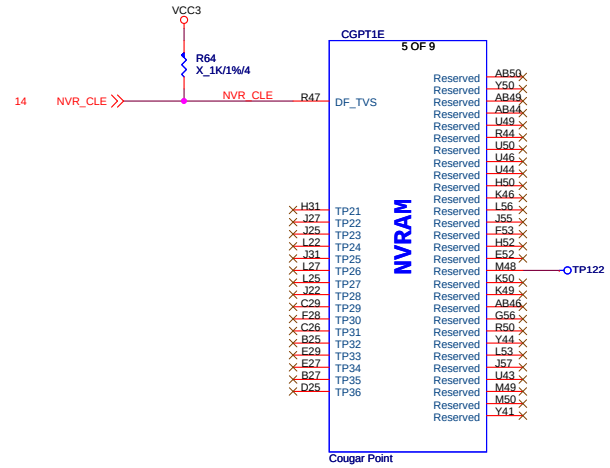


DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



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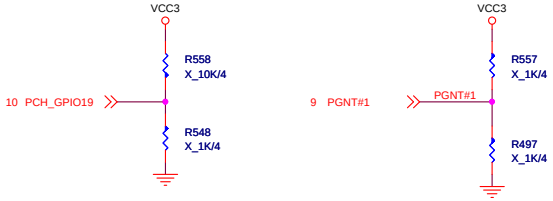
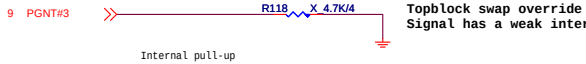
CP REQUIRED STRAPS

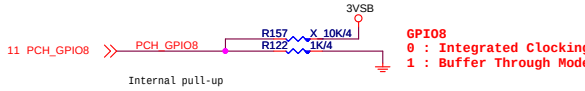
BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating



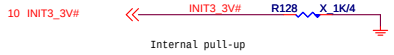
DMI AC/DC MODE
0 : AC
1 : DC *



Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



INT3_3V#
0 : ????????????????
1 : ???????????????? *

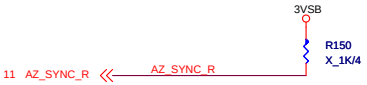
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

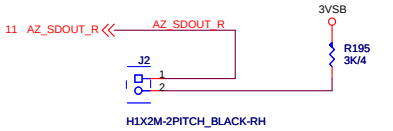
When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.



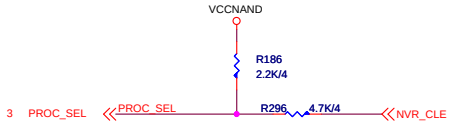
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

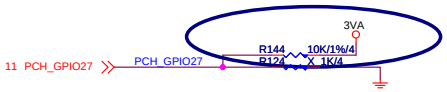
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



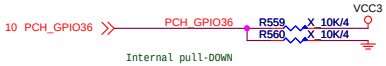
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



In Deep Sleep Power Well.

If not used,require a weak pull-up(8.2k~10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high

Cougar point EDS PAGE:93 This signal should not be pull high

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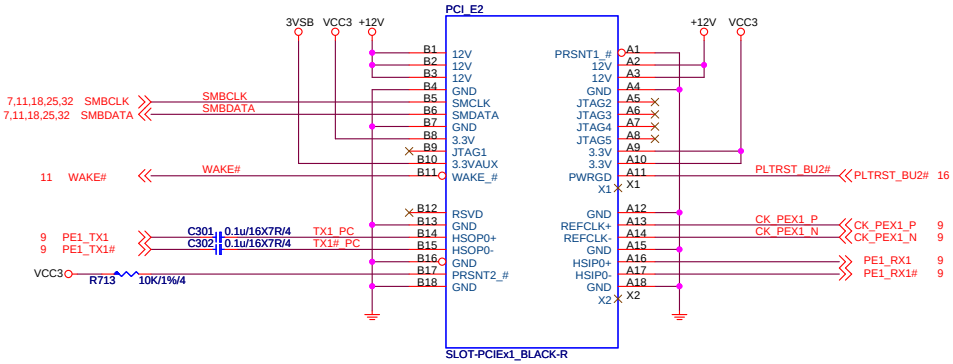
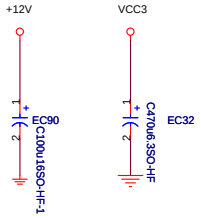
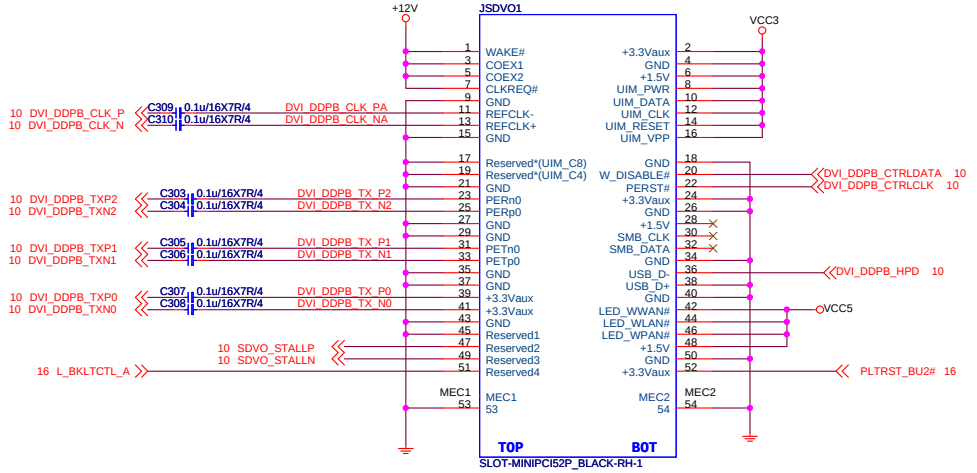
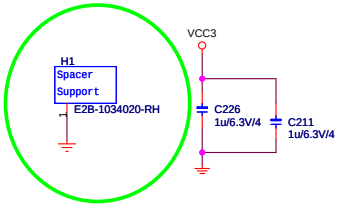
PCI EXPRESS x1-PORT1





SDVO connect





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	MS-7677	
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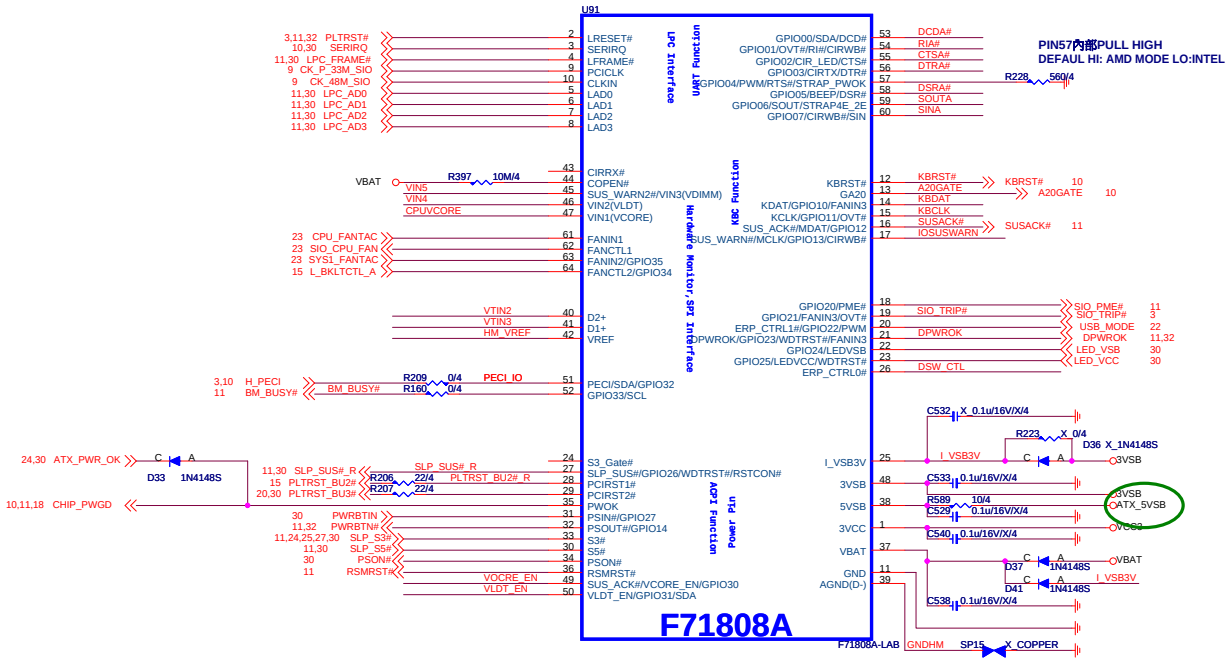
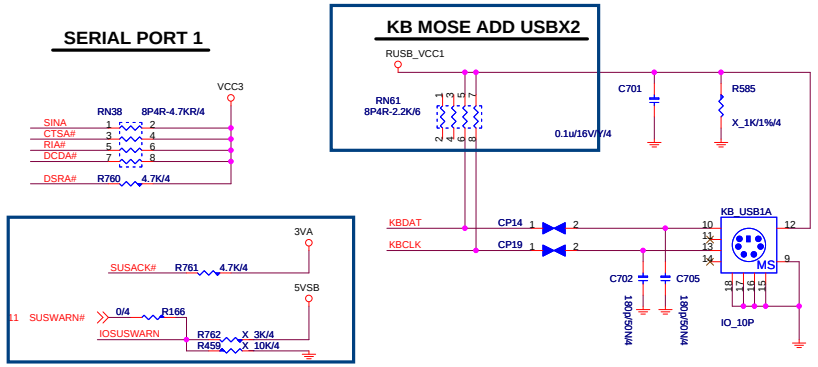
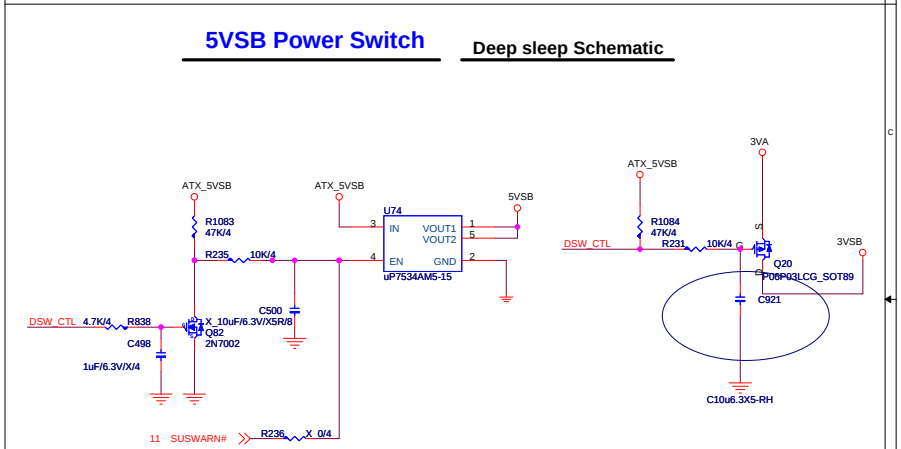
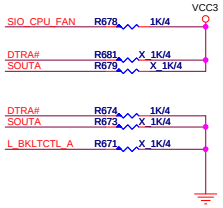




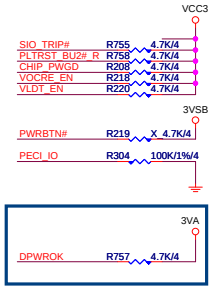


LPC I/O STRAPPING RESISTOR

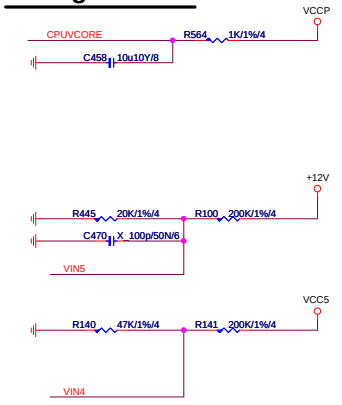
POWER-ON TRIP



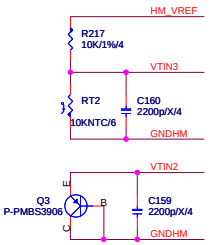
PIN	Function	NET Name	HI	LO
64	L_BKLTCTL_A	FANCTL2	PWM FAN	LINEAR FAN
62	SIO_CPU_FAN	FANCTL1	PWM FAN	not support linear fan
56	DTRA#	FAN40_100	FAN SPEED DUTY:40%	FAN SPEED DUTY:100%
59	STRAP4E_2E	Config 4E/2E	4E(DEFAUL)	2E
57	STRAP_PWOK	STRAP_PWOK	AMD (DEFAUL)	INTEL



Voltage Detect



Thermal Resistor



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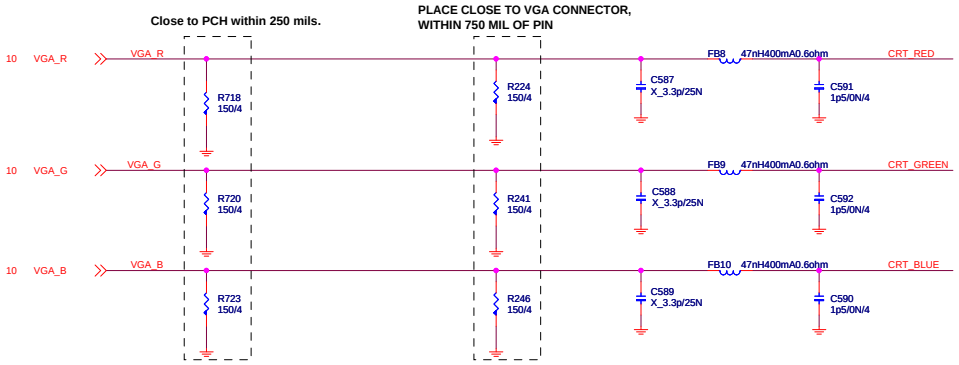

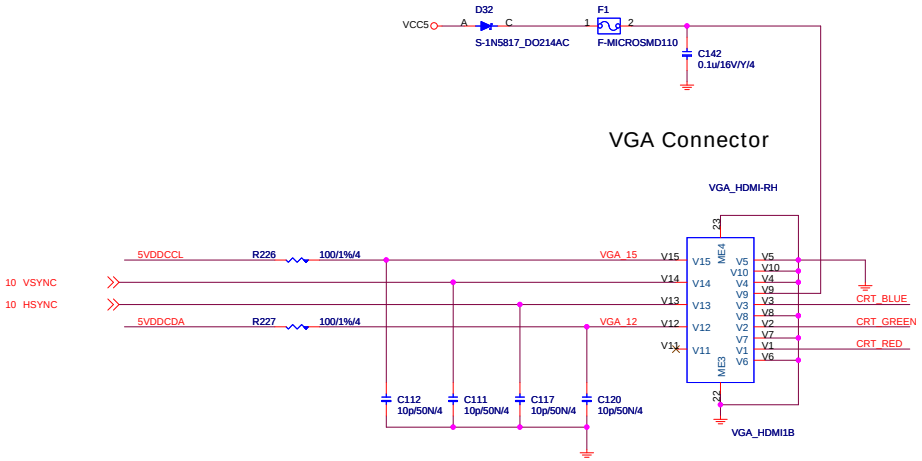

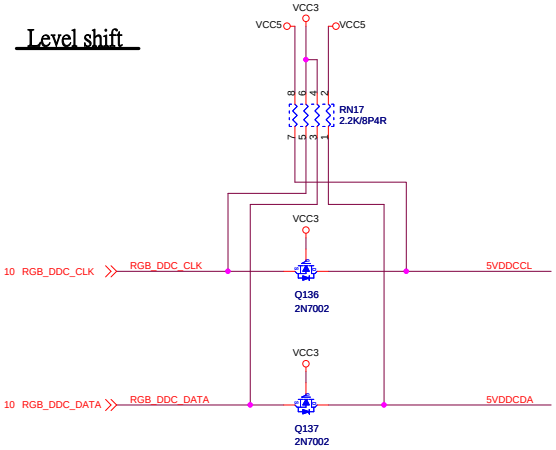

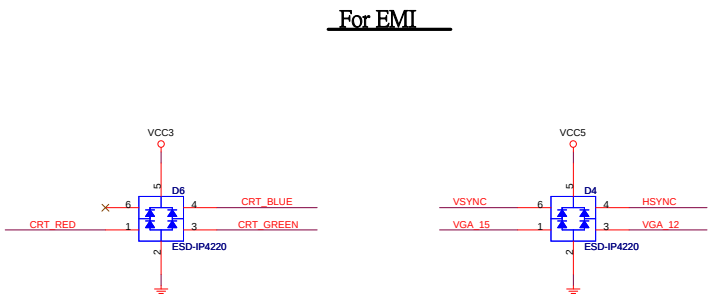

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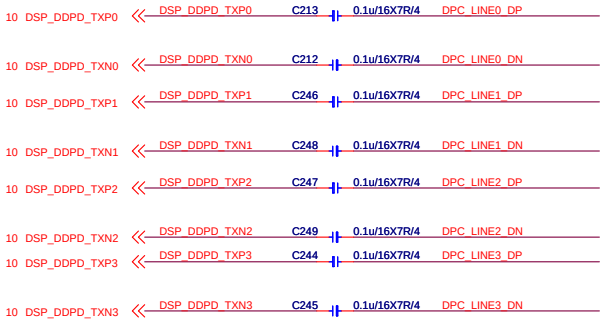
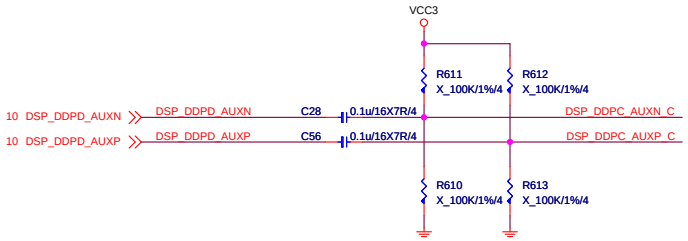
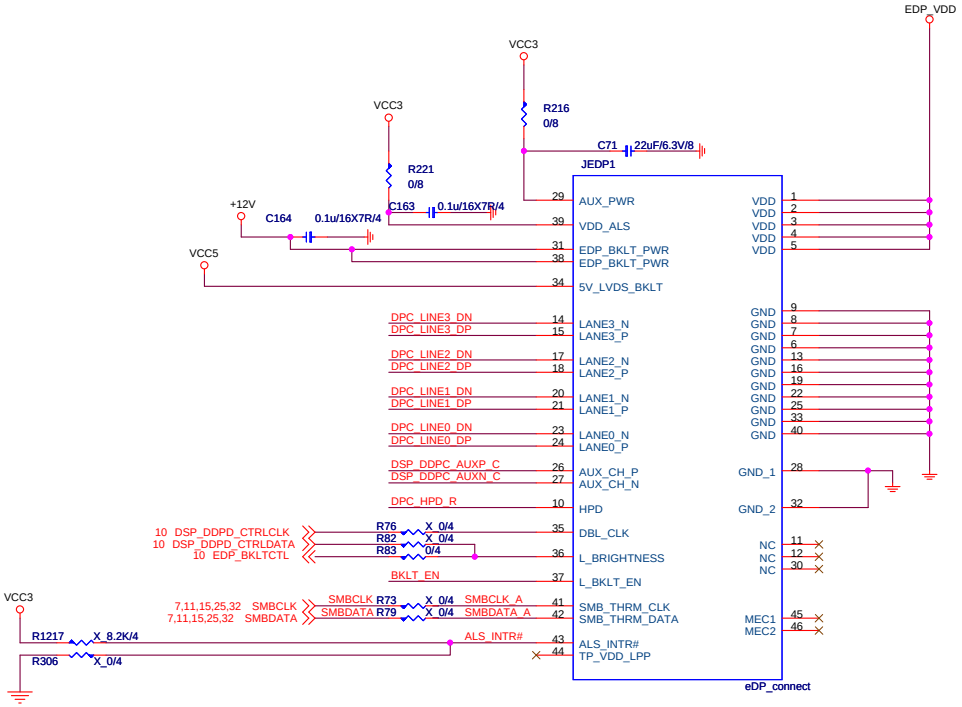
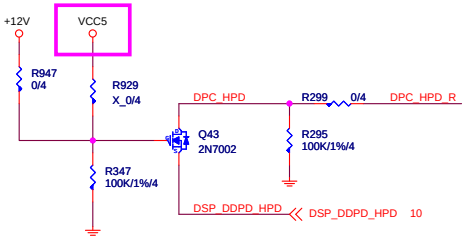
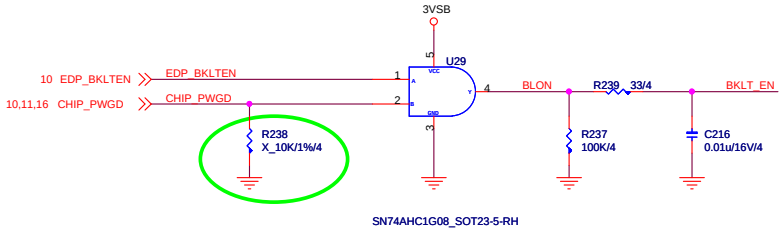


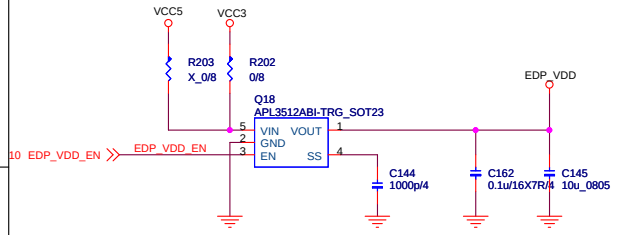




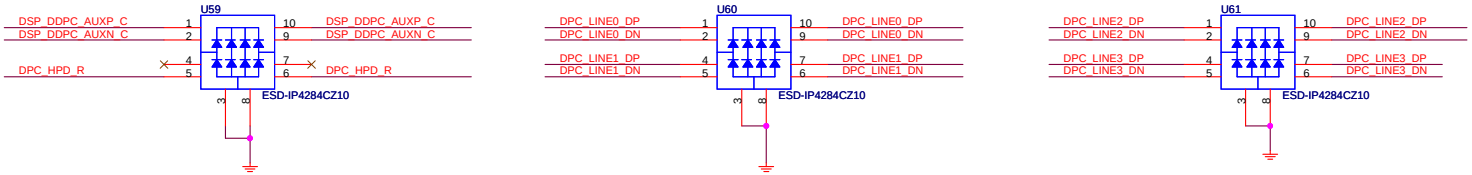




EDP POWER



For EMI



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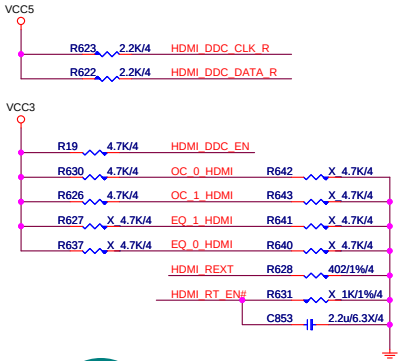
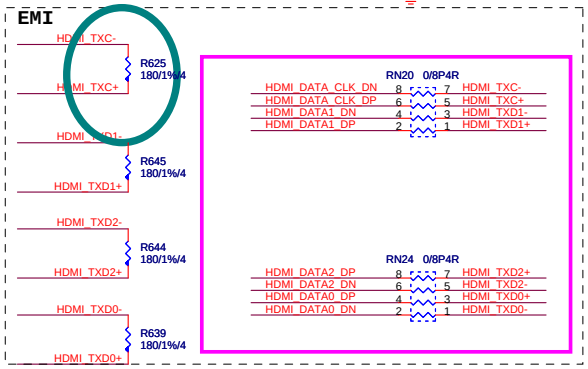
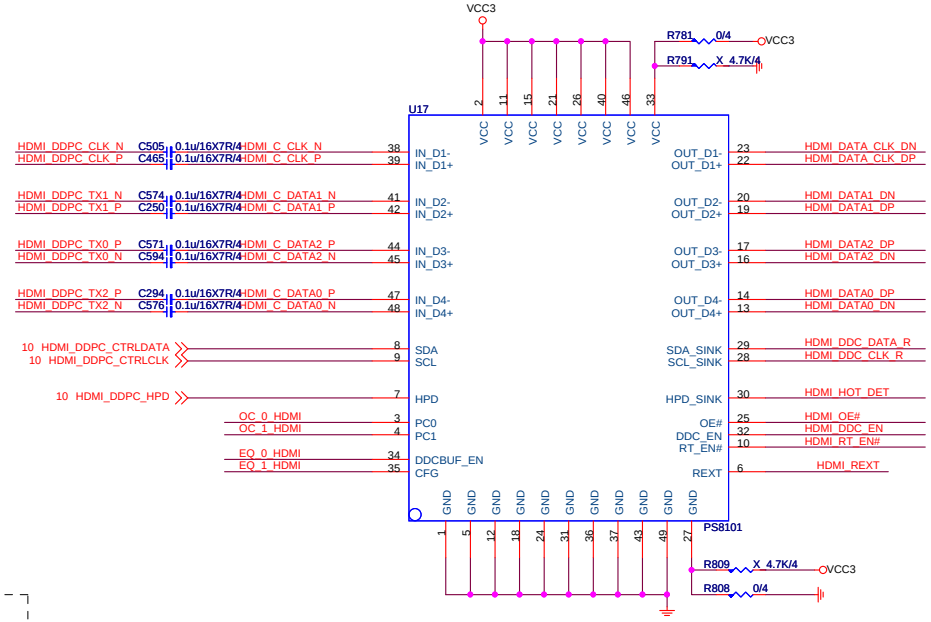
HDMI level shifter







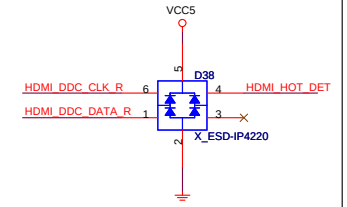
PERICOM料號:B0B-411LS2C-P22.
PARADE料號:B0B-081010C-P97.

	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

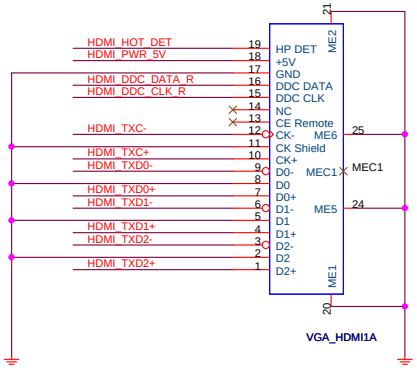
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

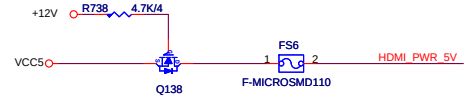
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

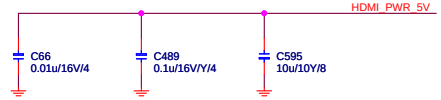
reserve

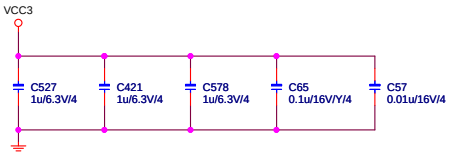


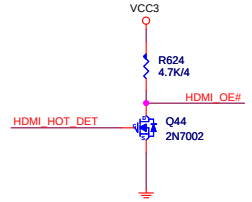
VGA_HDMI-RH











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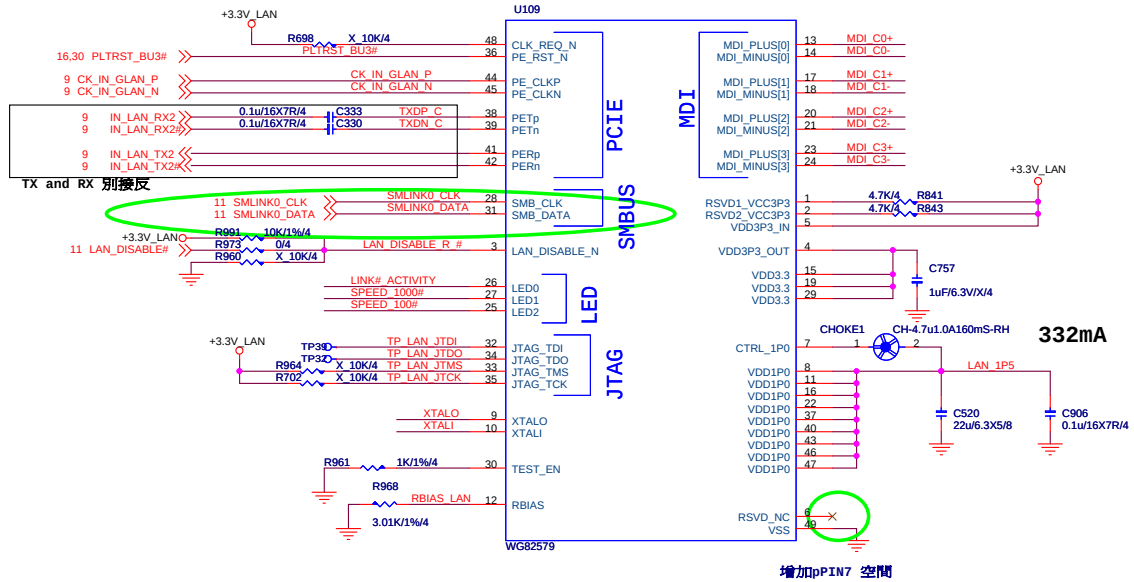
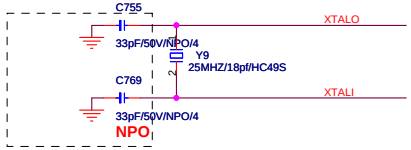
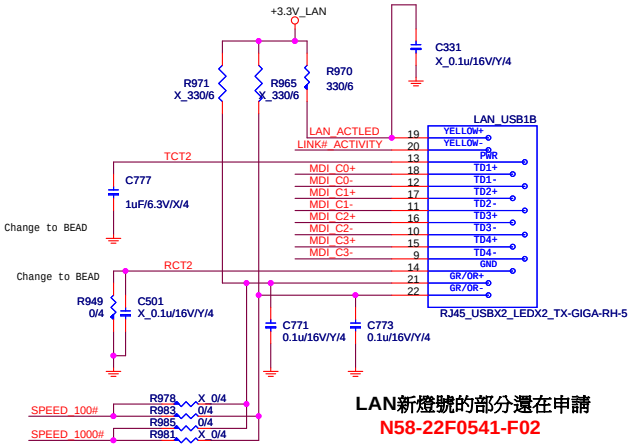
Vo = Vref (1+R2/R1) + Iadj x R2

If CLK_REQ_N is connected to PCIECLKRQ[1:2]#, the CLK_REQ_N pull-up resistor should be connected to +V3.3s

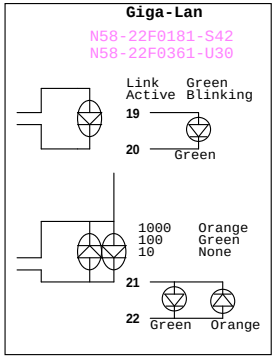




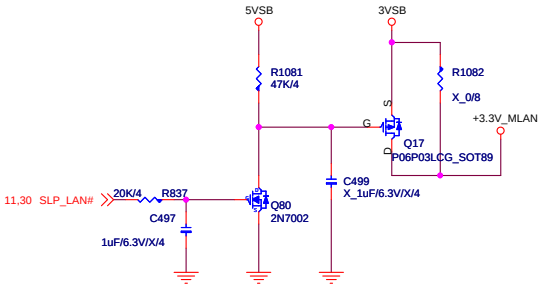


LAN新燈號的部分還在申請

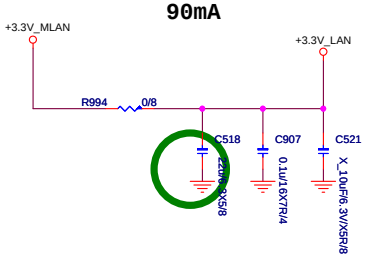
N58-22F0541-F02



+3.3V_LAN



90mA



Note:These caps closed to PHY

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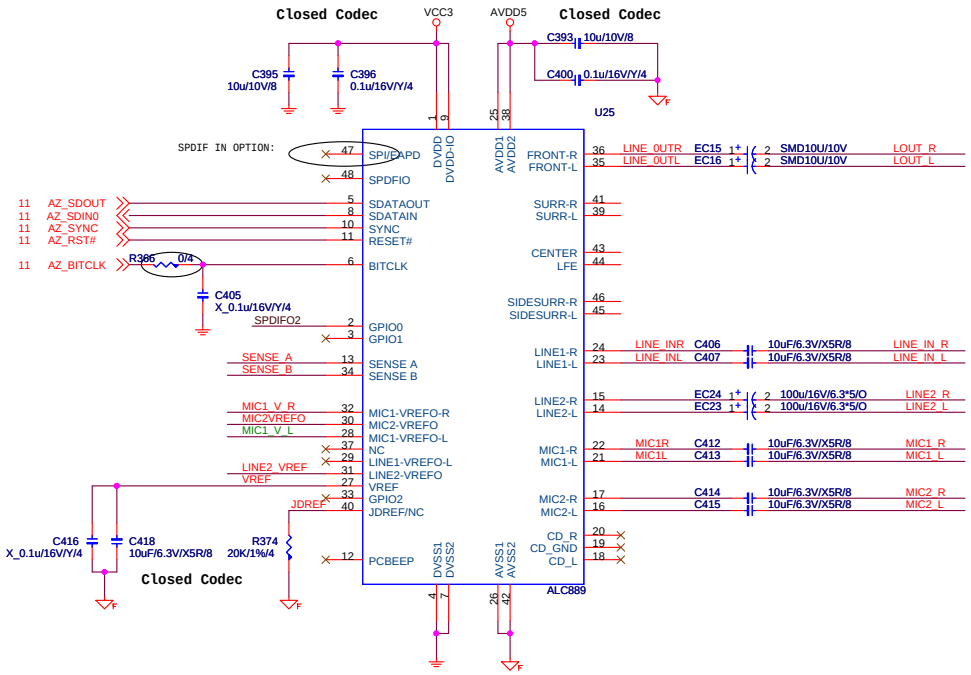

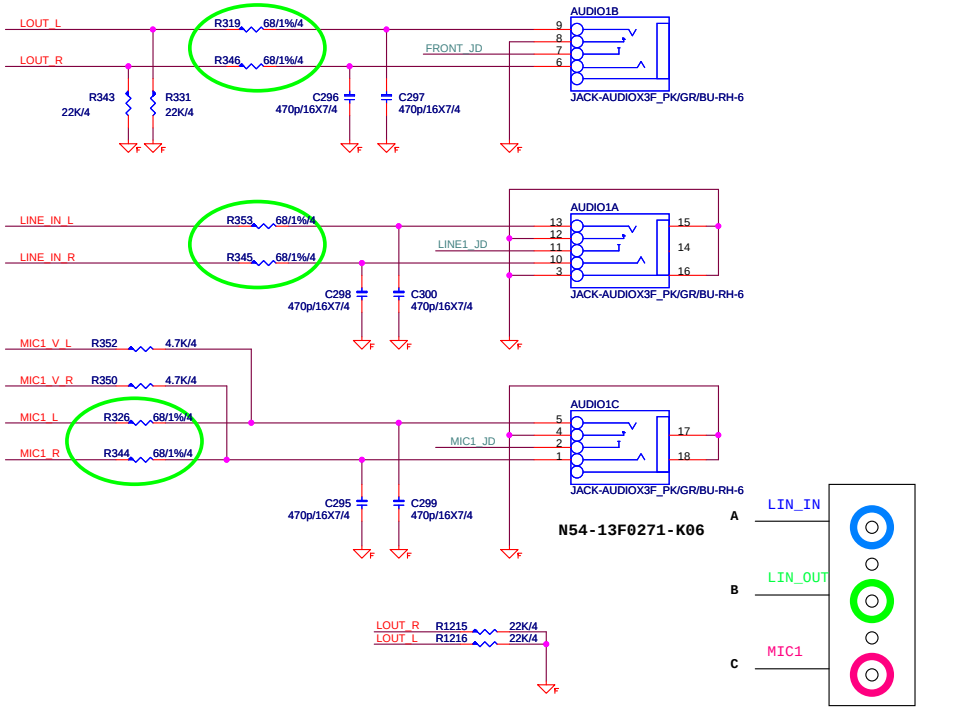

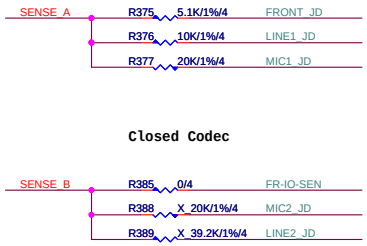

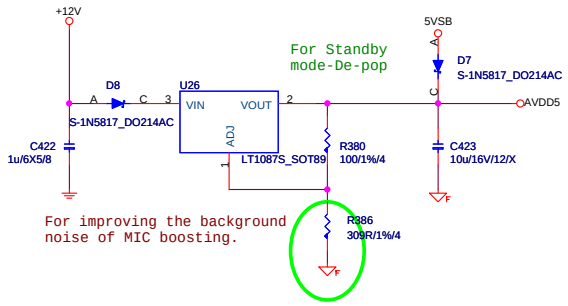

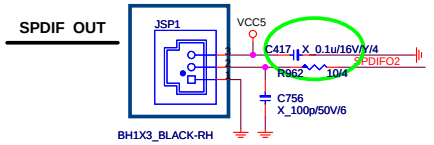

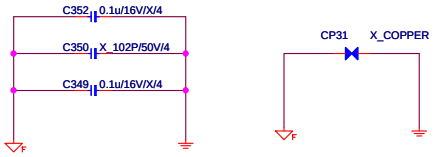

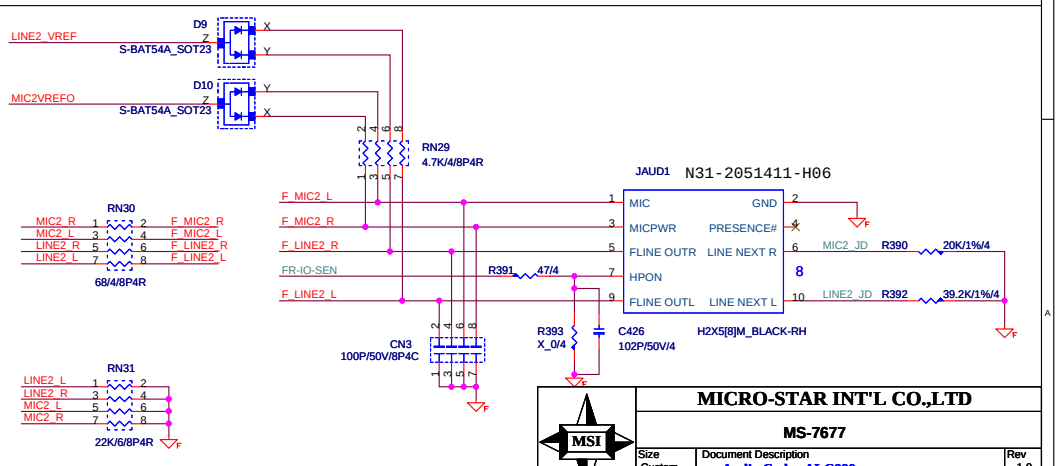

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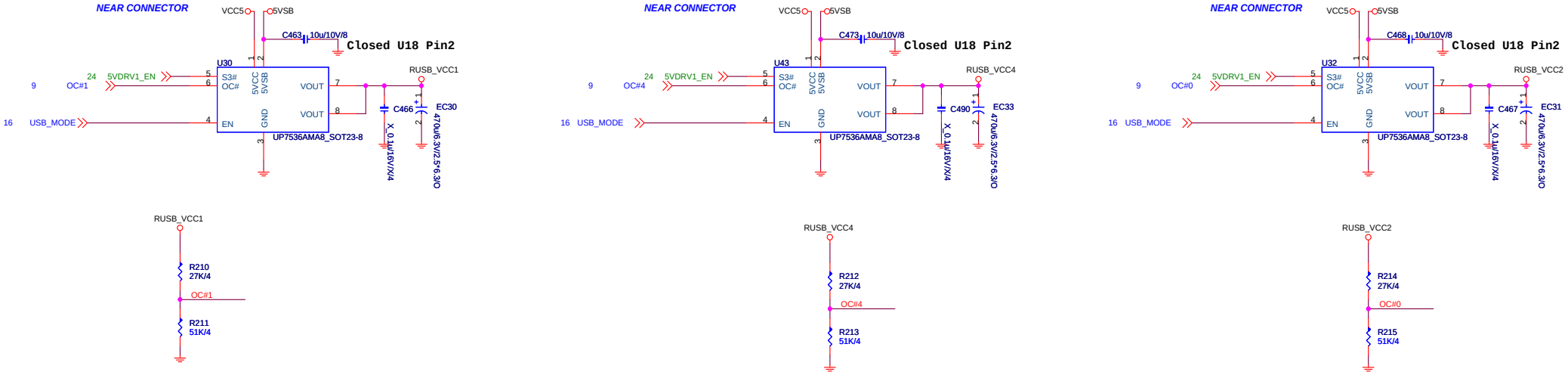
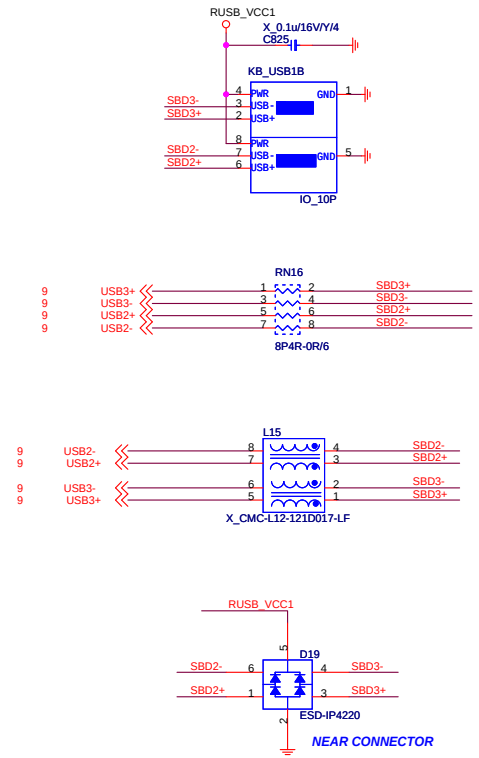
Rear USB Connector

USB POWER FOR PORT

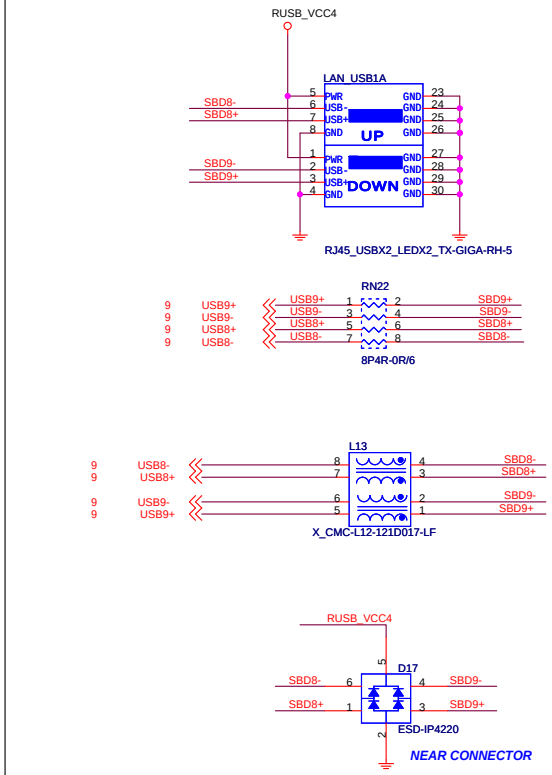


REAR USB

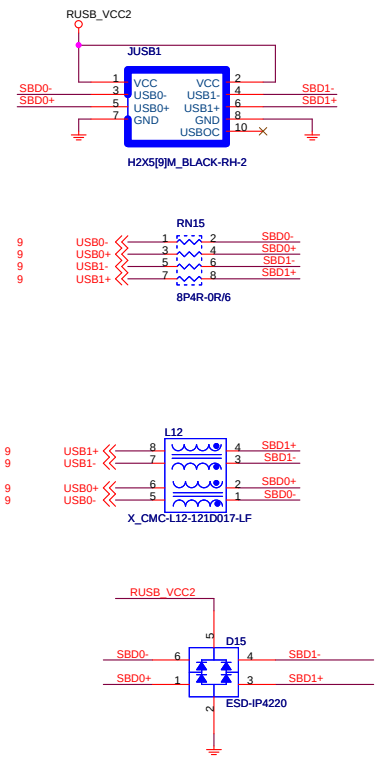
PS2&USBX2 PORT(6,7)

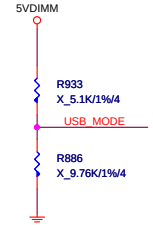


REAR USB PORT 8,9 (With LAN)



REAL USB PORT 0,1





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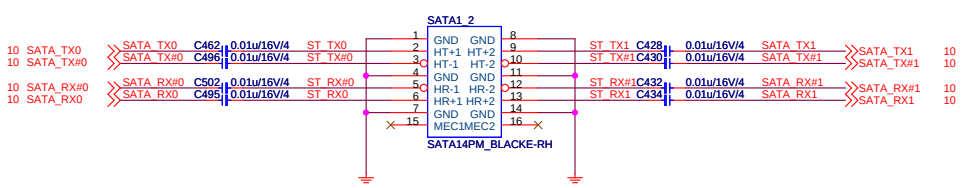
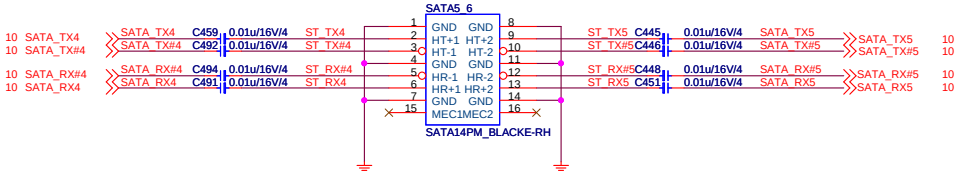
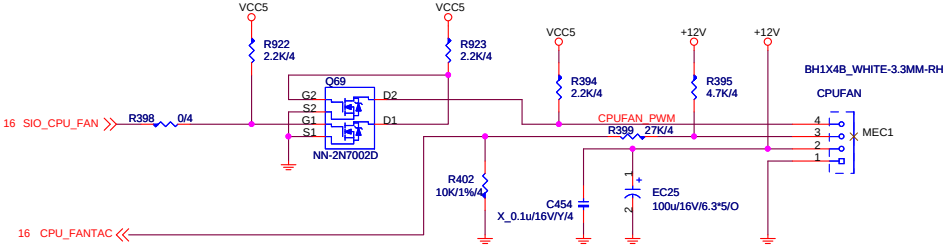
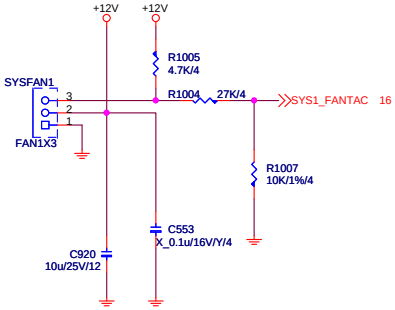




CPU FAN-COUNTROL CIRCUIT



SYS FAN CIRCUIT



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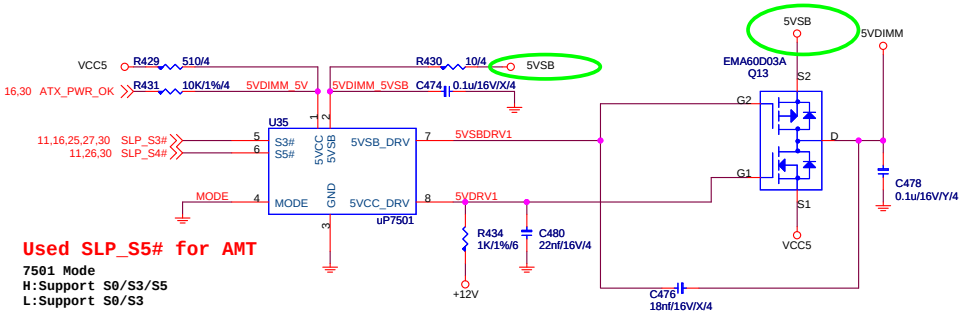
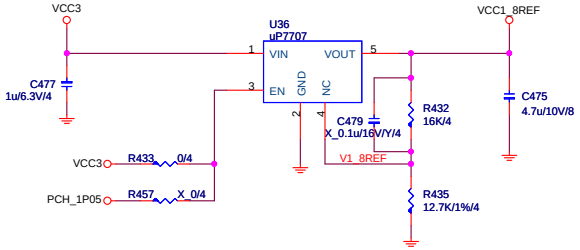
5VDIMM FOR DDR



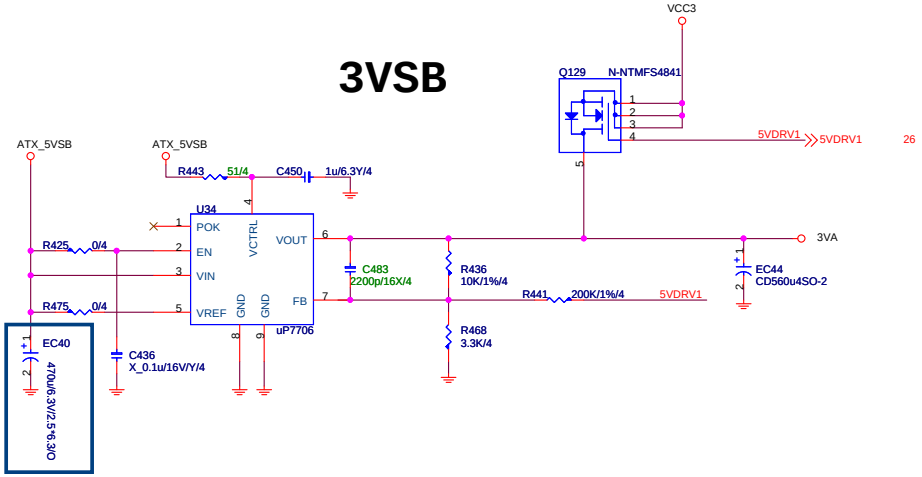
Used SLP_S5# for AMT

7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

VCC1_8REF

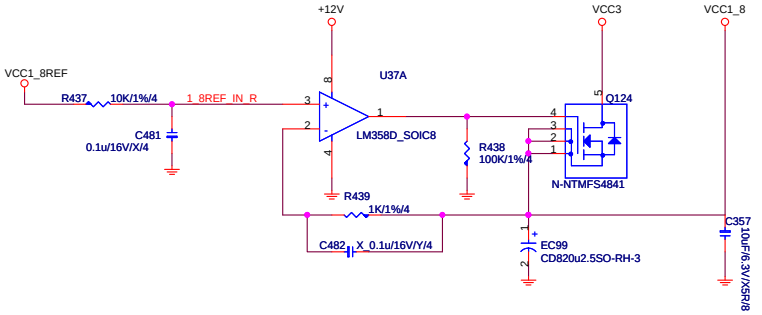


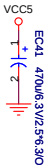
3VSB



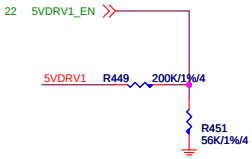
CPU_PLL_1_8

1.5A





USB MODE



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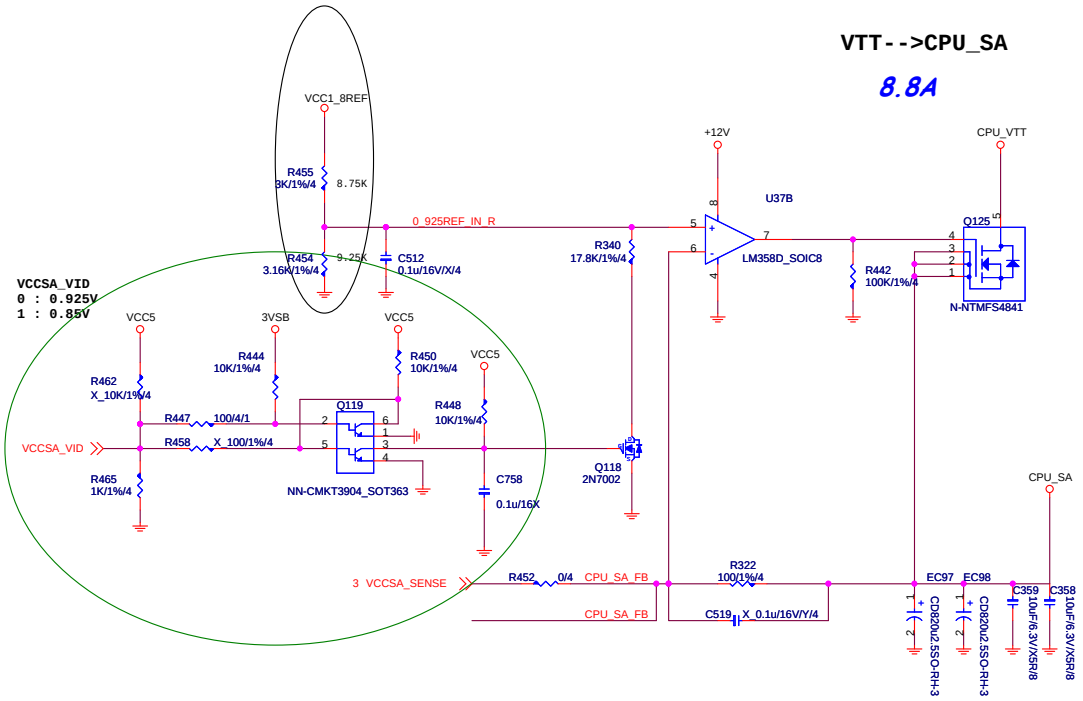
CPU_SA Power

VTT-->CPU_SA

8.8A

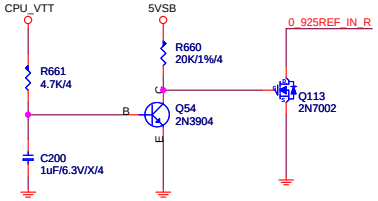


page 5

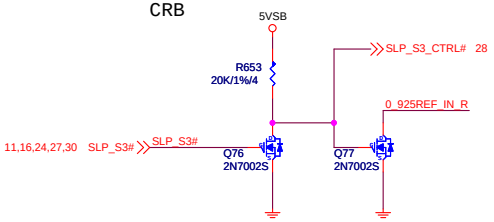
Table 3-10. VCCSA Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	1	7mΩ	1.4nH	Output	As close to RM keep-out as possible	1
10µF 0805 X5R	2	3mΩ	0.5nH	Output	Inside processor socket cavity	1,2,3

Waitting CPU_VTT Ready



CRB



CP Power

PCH+PCH_ME

DDR-->PCH

6.2A+1.8A=8A

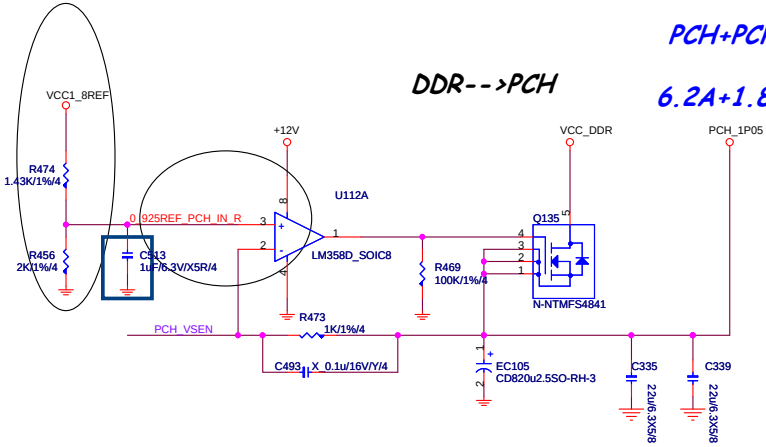


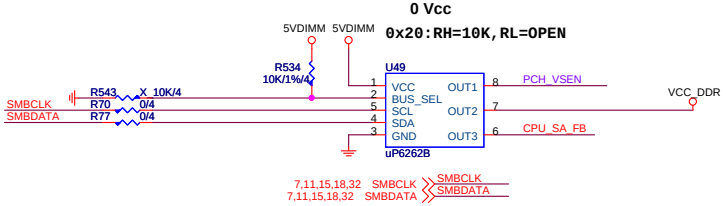
Table 4-1. V1.05A_PCH Plane Decoupling Recommendations

Bulk Decoupling Location	Qty x µF (size)	ESR, m
1.05S rail for VccCore & VccIO (dedicated)(AMT sku)	1x820uF	21mohm (bulk)
1.05A rail for VccASW (dedicated)(AMT sku)	2x22uF MLCC	
1.05S rail merge with 1.05A rail (non- AMT sku)	1X560uF 2x 22uF MLCC	7mohm (bulk)

Note: Bulk electrolytic capacitors (tantalum or aluminum based) render an aggregate ESR that matches the motherboard impedance budget. Other electrolytic capacitors that render motherboard impedance match can be deemed suitable as long as ripple current ratings and attach rate renders Bulk ESR not significantly different that those shown.

UPI VOLTAGE CONSOLE

0 Vcc



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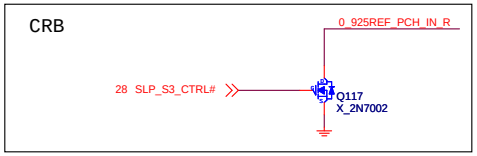

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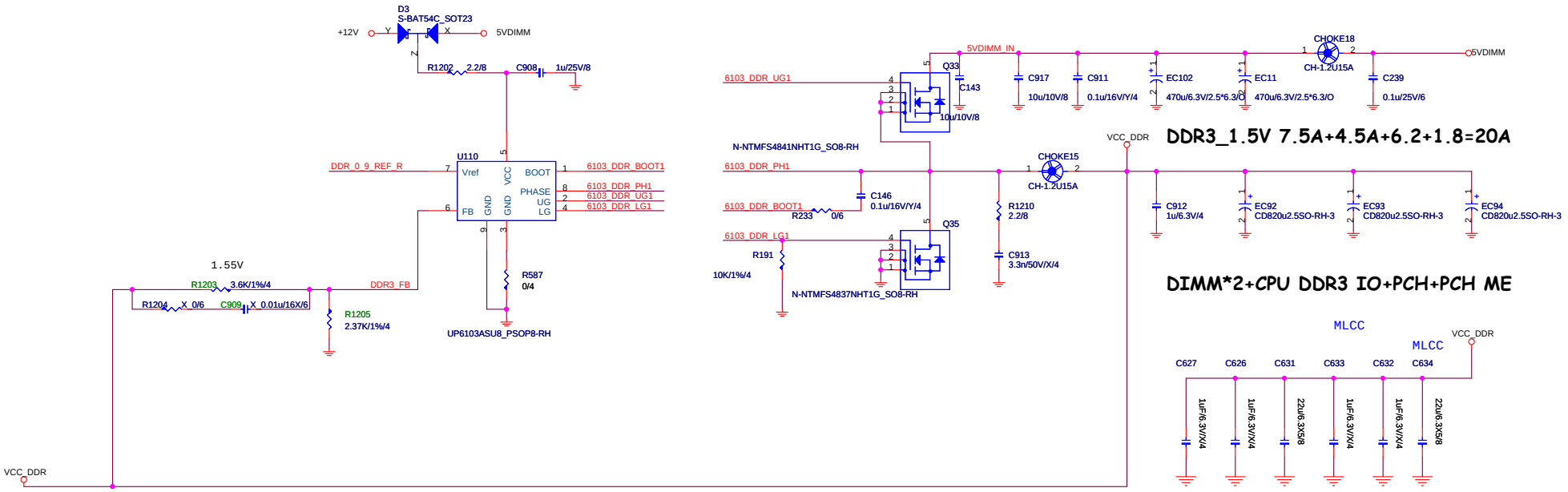
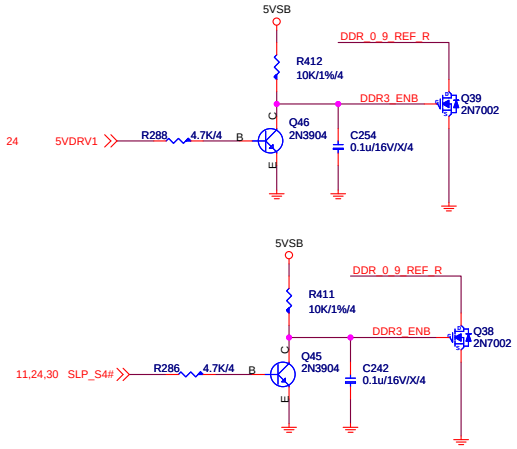
DDR Power



Intel Power on for 5v droop issue

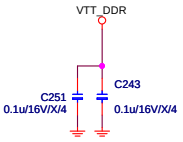


Meet Intel Power Down Sequence

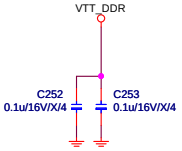
Table 3-11. VDDQ Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 1000µF	3	5mΩ	1.8nH	Output	Close to power pins	1,2
22µF 0805 X5R	9	5mΩ	0.55nH	Output		

ChannalA DDR VTT Power CAP



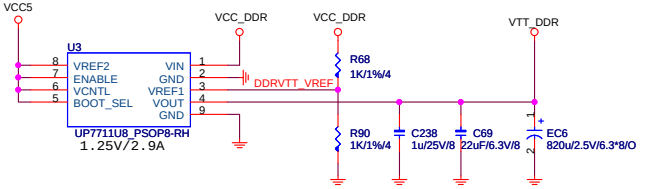
ChannalB DDR VTT Power CAP



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*4=0.8A



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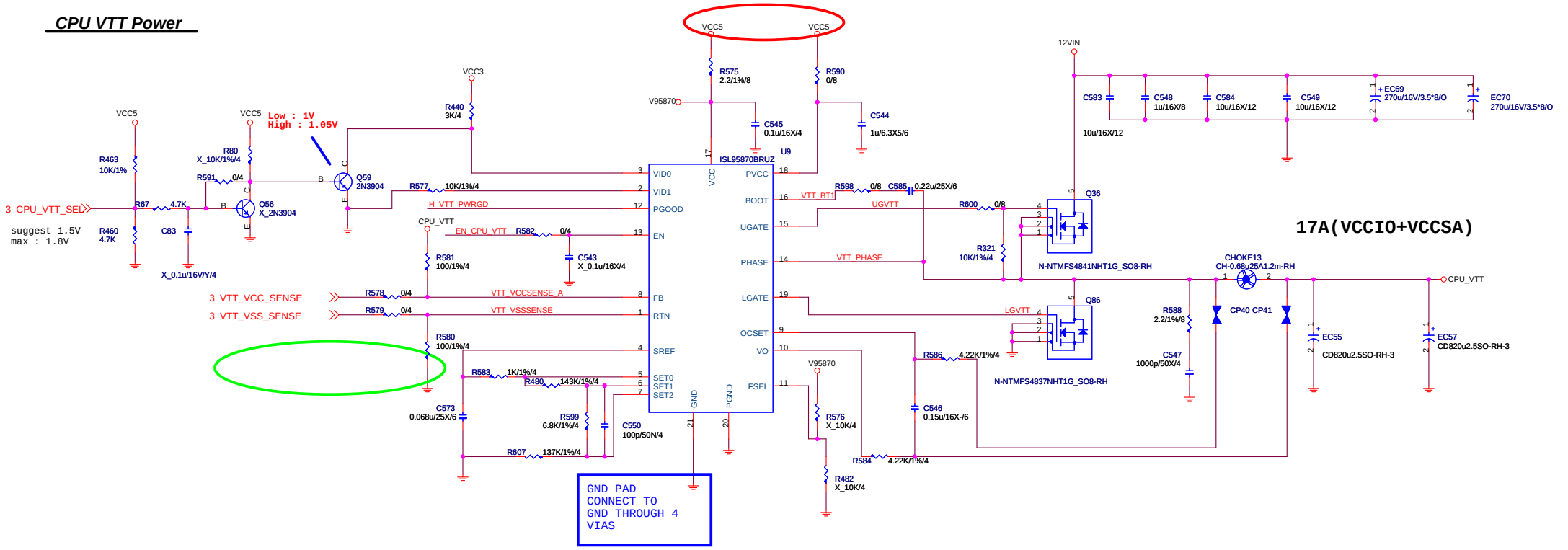
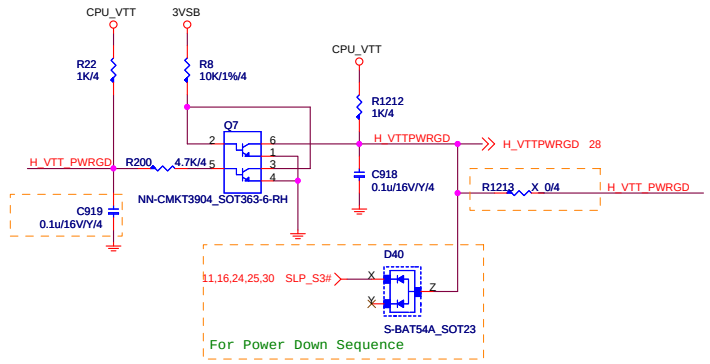
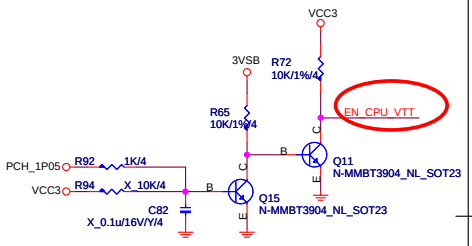
CPU VTT Power







1. Rocest = Iout*DCR/Iocset ; Iocset = 10uA

If DCR = 1m ; Iout = 20A, Rocest = 20A*1m/10uA --> Rocest = 2K

2. Csen = L/Rocset*DCR

If DCR = 1m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

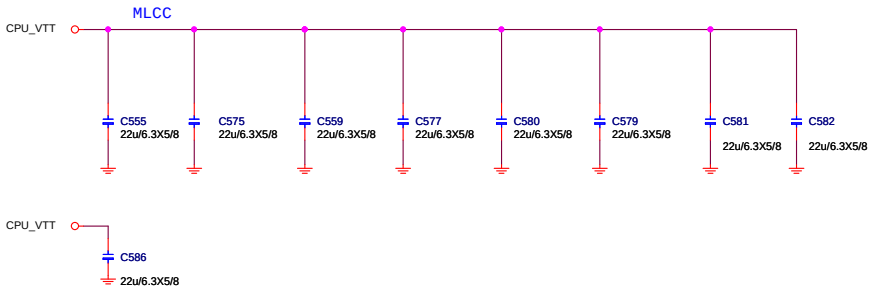


Table 3-6. VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2 3
0805 placeholders	16				Backside	

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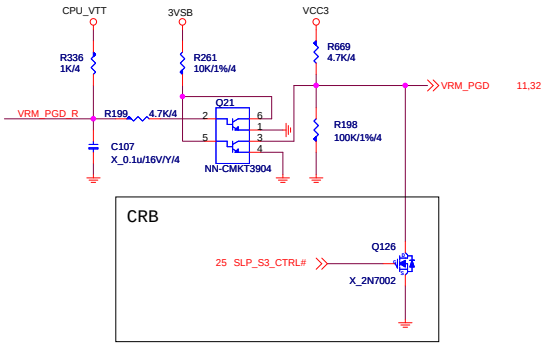
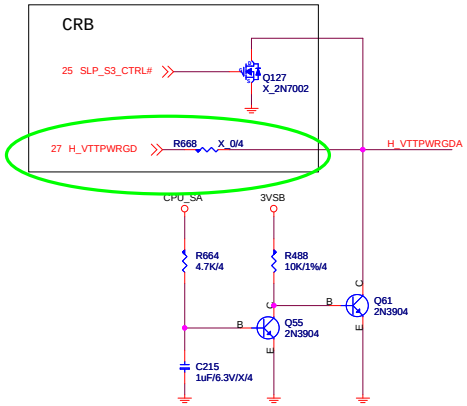
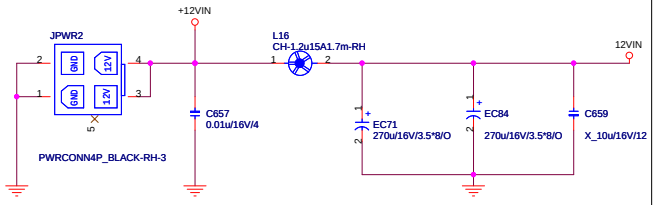
VCCP 65W
VCCAXG MAX:25A

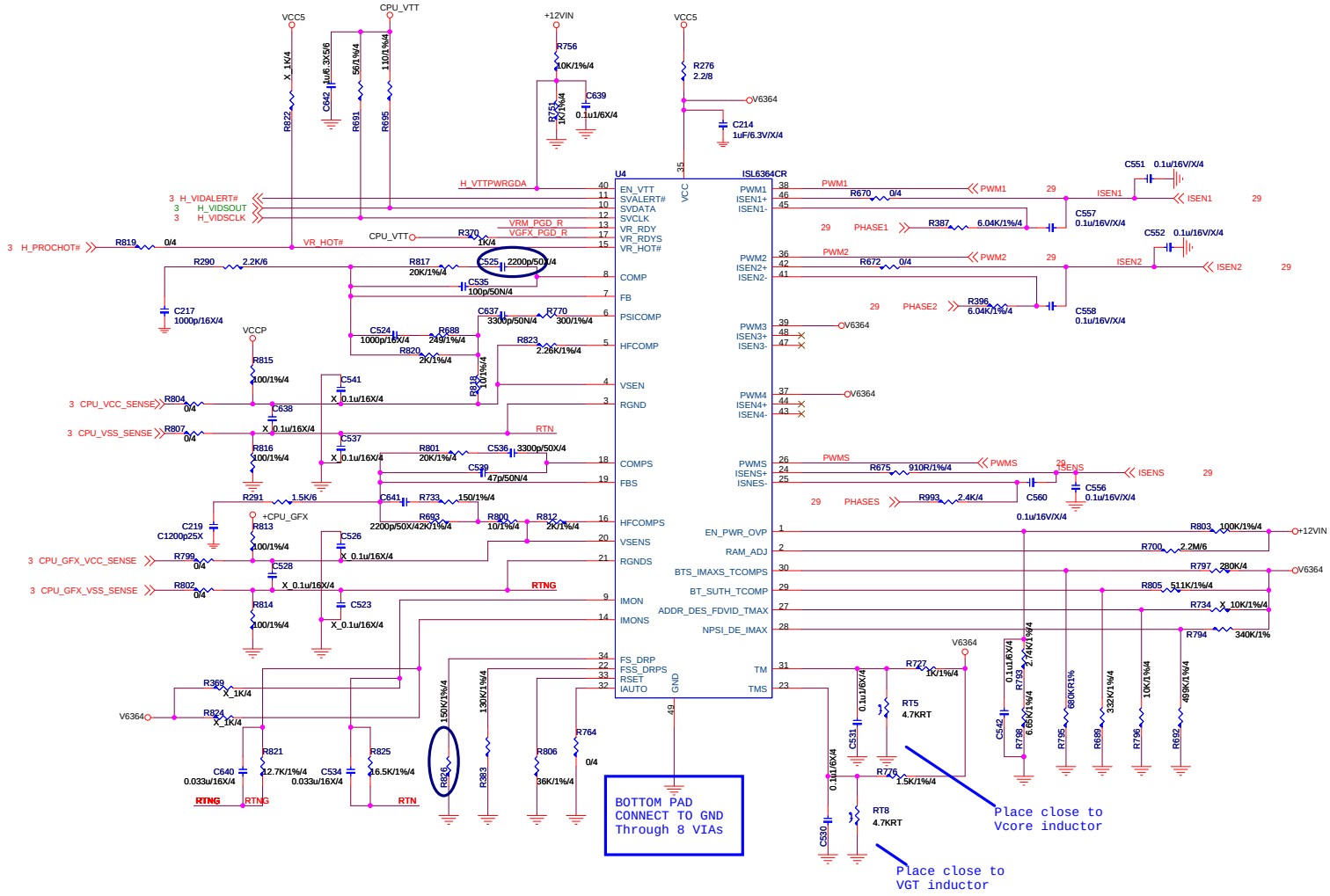
VRMPWRGD LEVEL SHIFT





4 PIN POWER CONNECT





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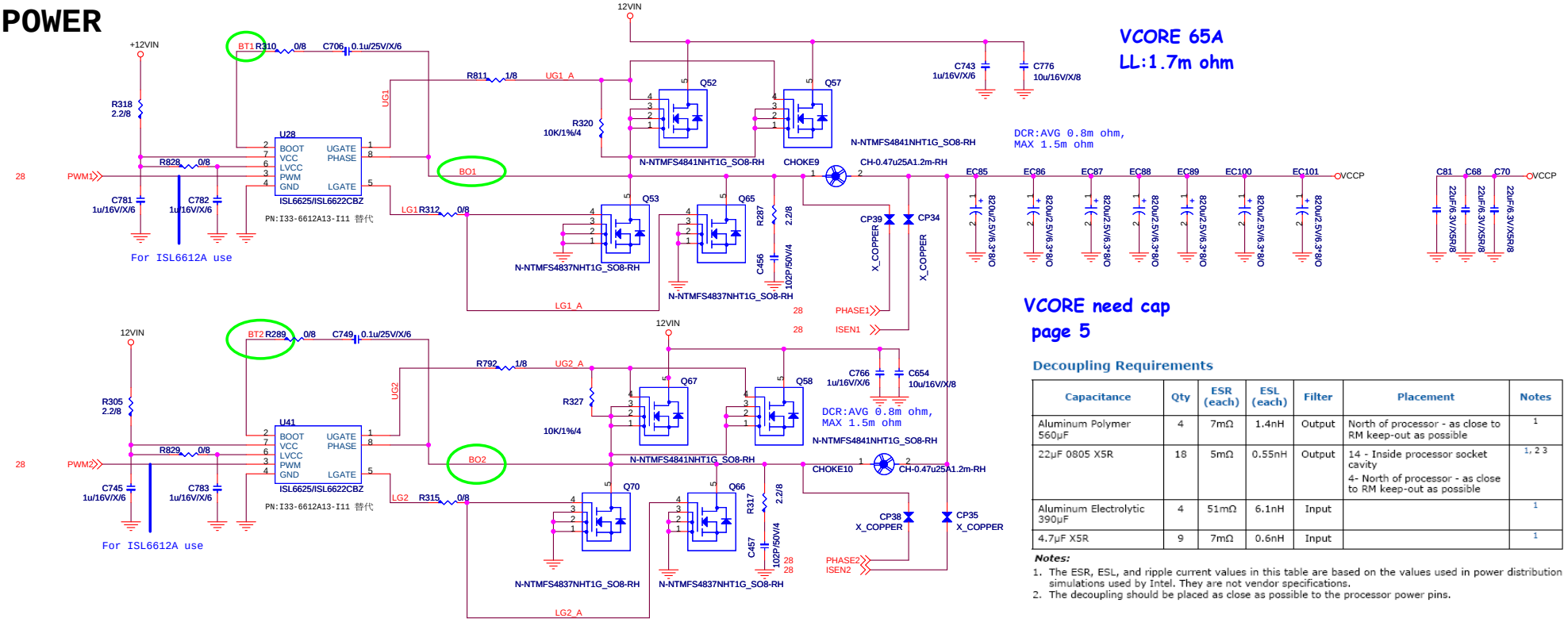
VCCP POWER



VCORE 65A
LL:1.7m ohm

VCORE need cap
page 5

Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

Notes:

1. The ESR, ESL, and ripple current values in this table are based on the values used in power distribution simulations used by Intel. They are not vendor specifications.
2. The decoupling should be placed as close as possible to the processor power pins.

GFX POWER

VCCAXG SVID:25A TDC:35A

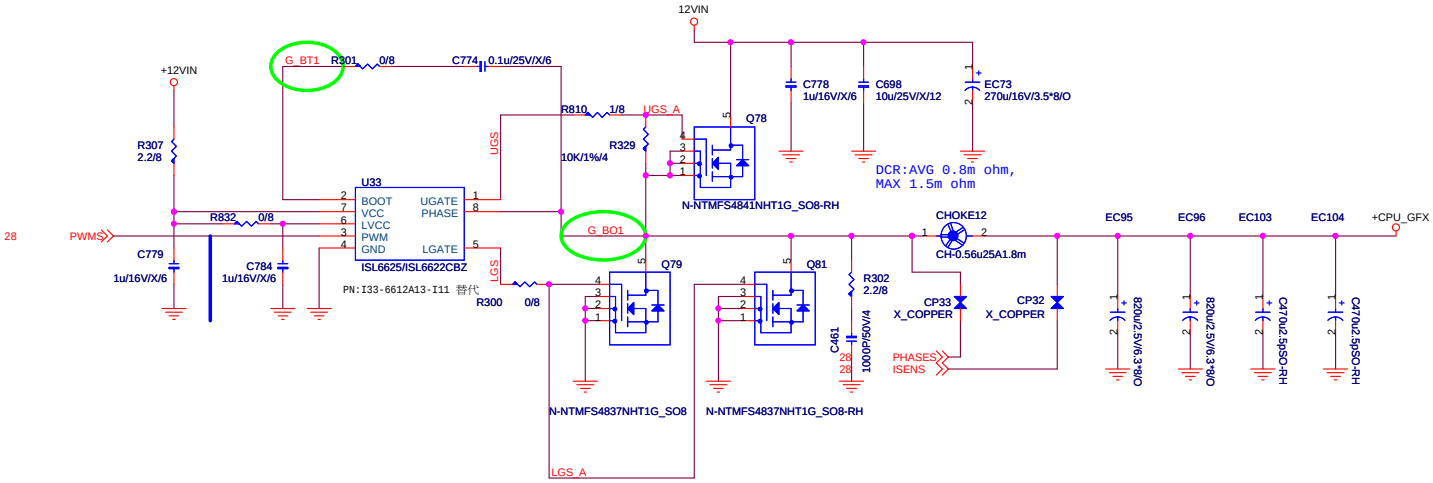
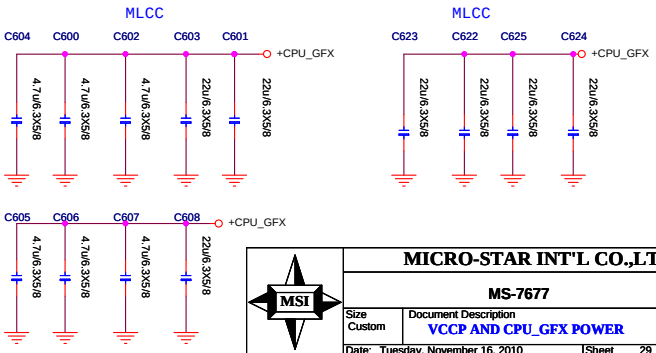


Table 3-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - Inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1



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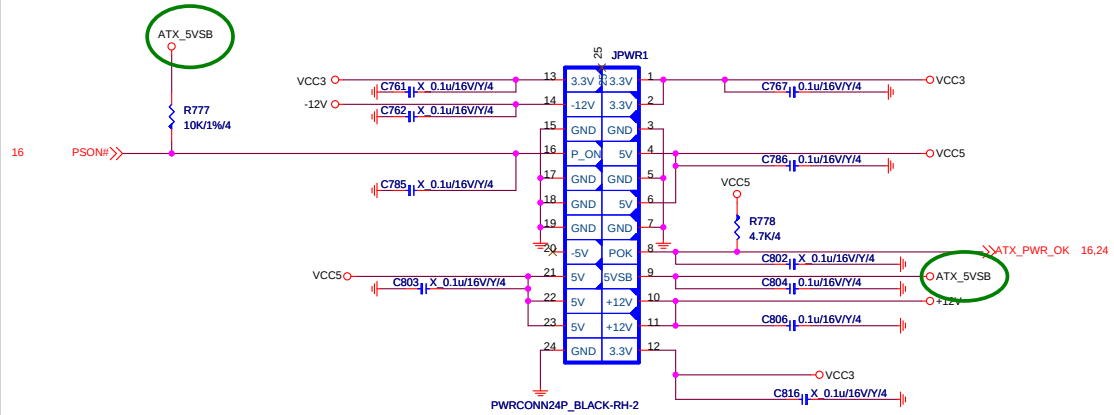
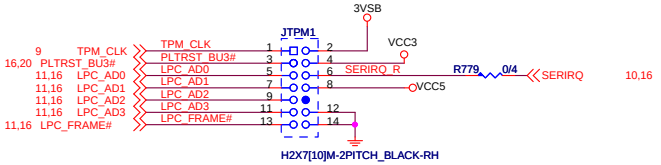
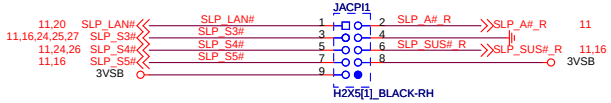
ATX POWER CONNECTOR



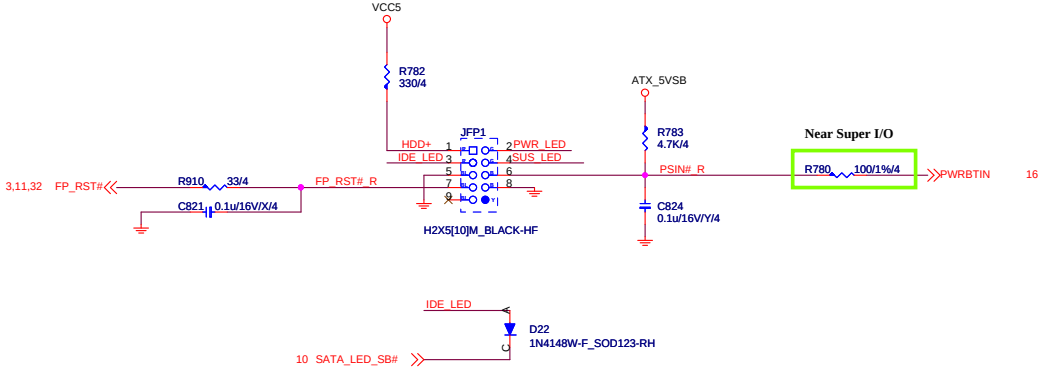
TPM



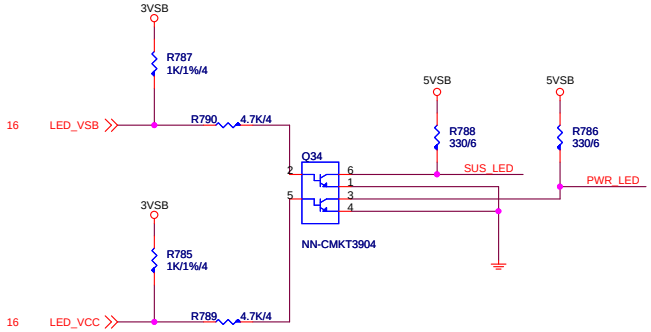
FOR INTEL TEST



FRONT PANNEL



LED (for Fintek 71882)



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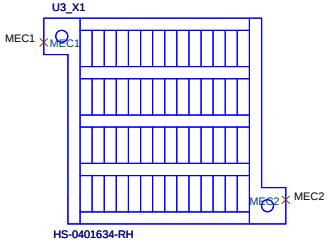
PCB1

7677-0c

PK0-076770B-K10,慶生,10,寶安恩斯邁廠(MSIS)
PK0-076770B-G37,精成,23,寶安恩斯邁廠(MSIS)
PK0-076770B-E48,競華,23,寶安恩斯邁廠(MSIS)

U3_X1



HS-0401634-RH

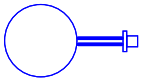
CPU_H1

CPU_H1

BIOS1_1

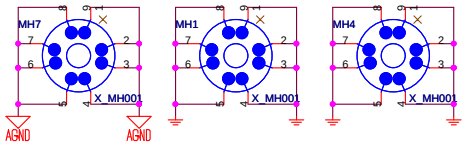
W25Q32BVSSIG

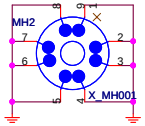
BAT1_X1



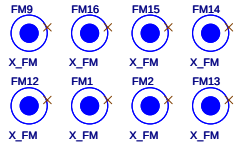
BAT-CR2032

Mounting Holes

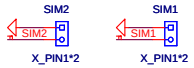




Optical Fiducial Marks-120



Simulation



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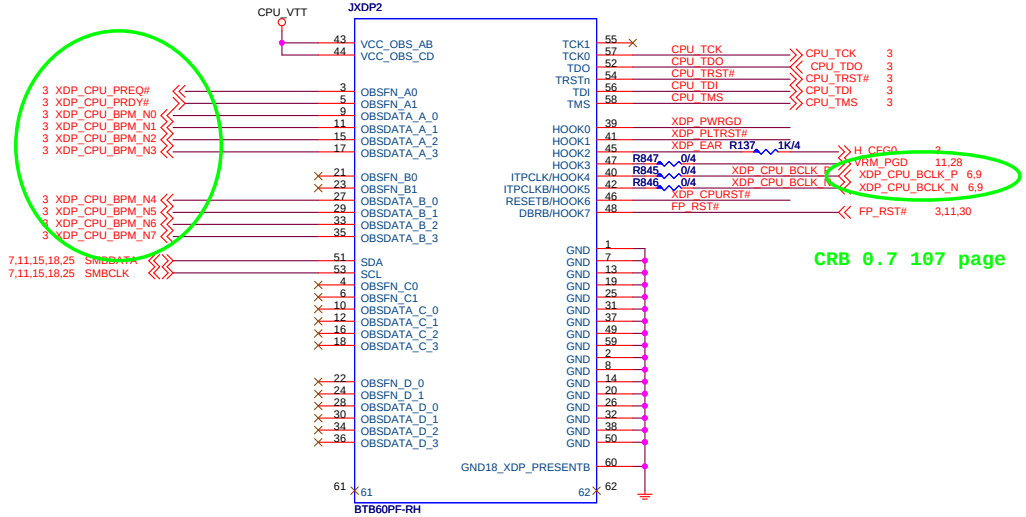
Reserve debug port 5020



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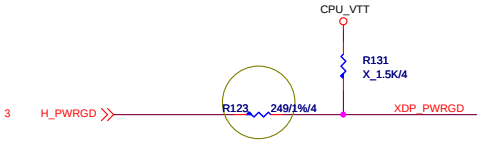

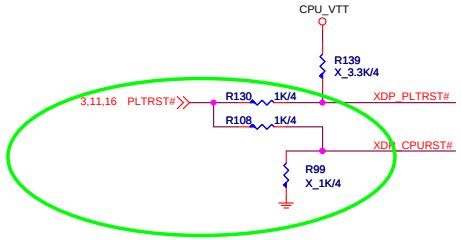

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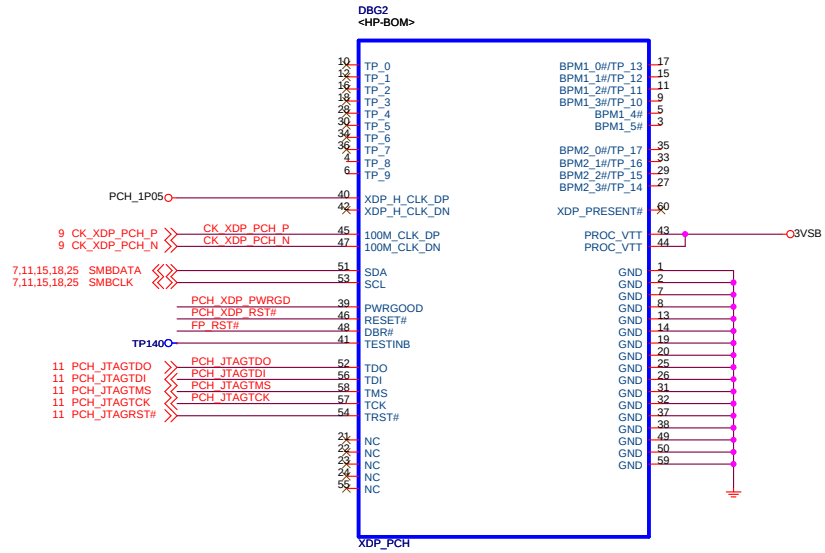
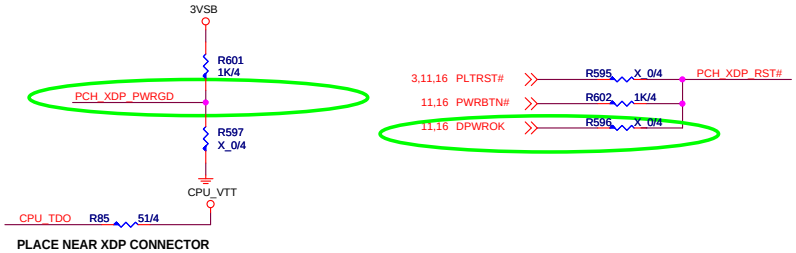


PCH XDP PWRGD/RESET



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