Nirvana 13 Discrete GDDR5 Schematics Document

Sandy Bridge
Intel PCH

2011-01-18
REV : A00

DY :None Installed
10mW: External circuit for 10mW solution installed.
GSENSOR_ADI: Stuff for ADI G-Sensor
VCCSA_PWM: Stuff for VCCSA PWM solution.
P2800A1: Stuff for P2800EA1

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover		
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Nirvana 13 Block Diagram (Discrete 8 layers)

PCB LAYER VT1316+VT1317

DIS
L1:Top L2:GND L3:Signal L4:Signal L5:VCC L6:Signal L7:GND L8:Bottom

Seymour:512M (64M*32b*2)

GDDR5 VRAM 512MB 88

GDDR5 1.25GHZ

AMD Graphic
SEYMOUR-XT-S3
83,84,85,86,87

PCIe x 16
(Discrete)

Intel CPU
Sandy Bridge
4,5,6,7,8,9,10,11,12,13

Project Code: 91.4ID01.001
PCB P/N : 10244
Revision : -1

DDRIII 1066/1333 Channel A
DDRIII 1066/1333 Channel B

DDRIII Slot 1 1066/1333 14
DDRIII Slot 2 1066/1333 15

FDIx4x2
DMIx4

HDMI 51
LCD 49
CRT 50

HDMI
(HDMI V1.3)
LVDS(Single Channel)
RGB CRT

Intel
PCH
Cougar Point
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25,26

(On Daughter Board)

PCIE x 1
10/100/1000 LOM
Realtek RTL8111E-VB
RJ45 CONN

PCIE x 1
USB3.0 Controller
NEC uPD720200F1
USB3.0 x 2

PCIE x 1,USB2.0 x 1
Mini-Card
WWAN
SIM
82

PCIE x 1,USB2.0 x 1
Mini-Card
802.11a/b/g 65

USB2.0 x 1
USB CHARGE
PI5USB14550 57
ESATA/USB Combo 57

SATA x 1

SD/MMC+/MS/MS Pro/xD/SDXC (8 in 1) 74
Card Reader RTS5138 32
Bluetooth V3.0 63
Finger Print 64
CAMERA w/ Digital MIC 49

USB 2.0 x 1
USB 2.0 x 1
USB 2.0 x 1
USB 2.0 x 1
USB2.0 x 4

HDA

SPI
LPC Bus
SMBus

SATA x 2
HDD 56
ODD 56

CODEC
IDT
92HD87B1
29

HP
MIC IN
1CH SPEAKER

Flash ROM 4MB 60

Free Fall Sensor 79

KBC
NUVOTON
NPCE795PA
27
ADC
DAC

Thermal Sensor
Main:ENEP2800 28

Touch PAD 69
Int. KB 69

FAN Controller
Main: G991P11U 28
Fan 55

CPU DC/DC 42	
INPUTS	OUTPUTS
5V_S5	VCC_CORE

SYSTEM DC/DC VT1316+VT1317 44	
INPUTS	OUTPUTS
5V_S5	VCC_GFXCORE

SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
5V_S5	0D85V_S0

VGA VT357 92	
INPUTS	OUTPUTS
5V_S0	VGA_CORE

SYSTEM DC/DC VT358/RT9026 46	
INPUTS	OUTPUTS
5V_S5/5V_S5	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC VT357 45	
INPUTS	OUTPUTS
5V_S5	1D05V_VTT

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC TPS51427 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

SYSTEM DC/DC TPS51311 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9731 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0

Switches 36,93	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5 1D8V_S0 1D5V_S3	1D5V_S0 5V_S0 3D3V_S0 1D8V_VGA_S0 1D5V_VGA_S0

<Core Design>

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.1_0

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Enable when Pull-up.
INIT3_3V#	Weak internal pull-up. This signal should not be pulled low. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
INTVRMEN	**Integrated 1.05 V VRM Enable / Disable** Integrated 1.05 V VRMs is enabled when high. This signal should always be pulled high
DF_TVS	**DMI and FDI Tx/Rx Termination Voltage** Weak internal pull-down. It needs to be connected to PROC_SELECT with a 1K±5% pull-up resistor to PCH VCCPNAND rail and a 4.7K±5% series resistor.
SATA1GP /GPIO19	**Boot BIOS Strap bit 0** This Signal has a weak internal pull-up. Note: This field determines the destination of accesses to the BIOS memory range. This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC
HDA_SDO	Signal has a weak internal pull-down. Default: the security measures defined in the Flash Descriptor will be in effect. Pull-up: the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing or debug environments ONLY.
HDA_SYNC	**On-Die PLL Voltage Regulator Voltage Select** This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low. Needs to be pulled High for Huron River platform.
GPIO15	**TLS Confidentiality** Low – Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High – Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: A strong pull-up may be needed for GPIO functionality
DSWVRMEN	**Deep S4/S5 Well On-Die Voltage Regulator Enable** This signal enables the internal Deep Sleep 1.05 V regulators. This signal must be always pulled-up to VccRTC.
GPIO28	**On-Die PLL Voltage Regulator** This signal has a weak internal pull-up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail.

Processor Strapping

Huron River Schematic Checklist Rev1_0

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	0
CFG[4]	**Display Port Presence strap**	**1:** Disabled – No Physical Display Port attached to Embedded Display Port. **0:** Enabled – An external Display Port device is connectd to the Embedded Display Port	1
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 – Device 1 functions 1 and 2 disabled 10 : x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01 : Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 – Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 ~ 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5	6V~14.1V 6V~14.1V 5V 5V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	X
LANE2	LAN (I/O Board)
LANE3	Mini Card2(WWAN)
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	X
1	ESATA / USB COMBO
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	X
9	X
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery Capacity Board		KBC_SDA1/KBC_SCL1 KBC_SDA1/KBC_SCL1
EC SMBus 2 PCH MXM LCD Thermal Sensor		KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2
PCH SMBus CK505 Clock Generator SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

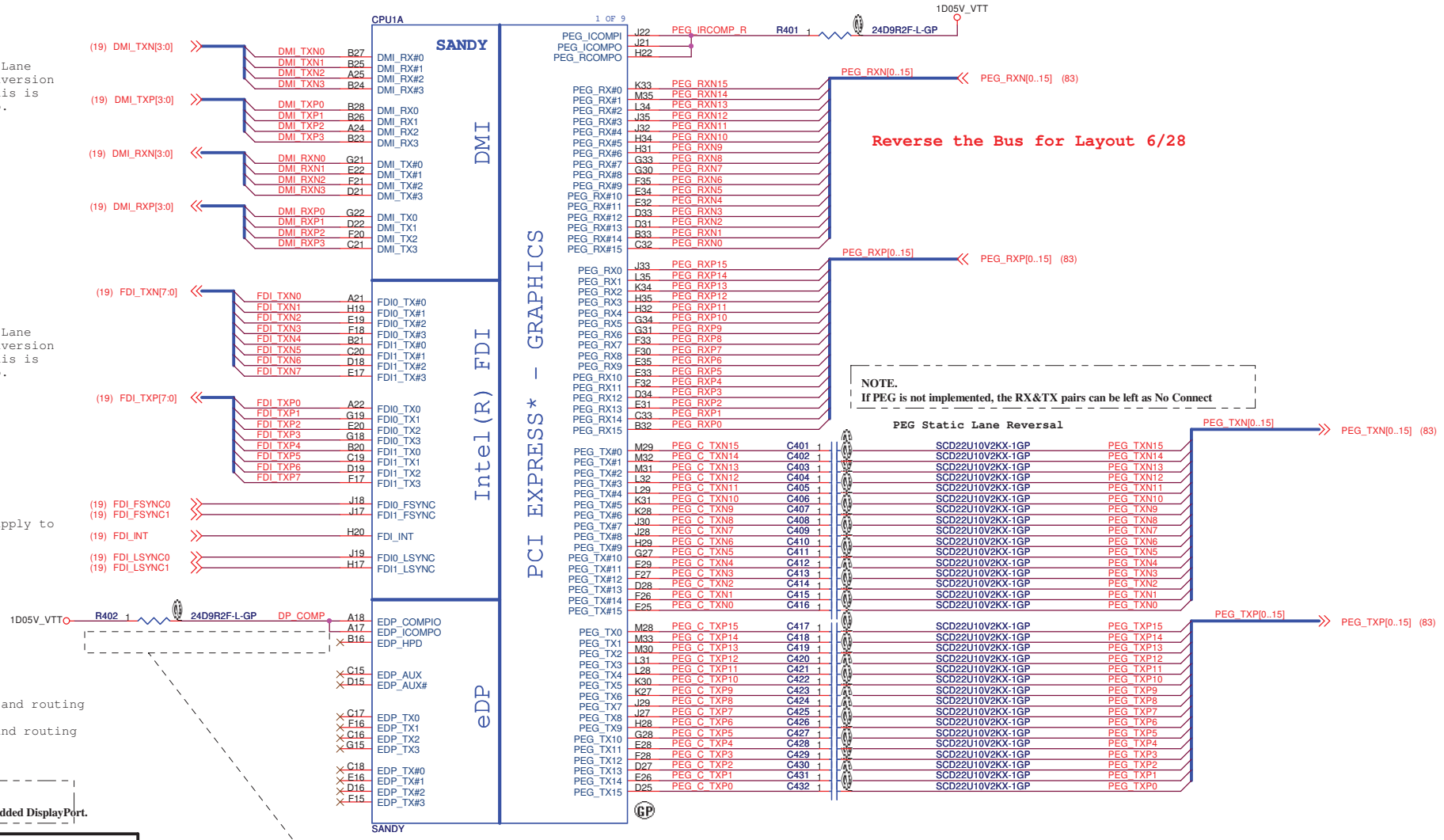
Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.



NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

<Core Design>

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Title		
CPU 1/7(PEG/DMI/FDI/eDP)		
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SSID = CPU

Disabling Guidelines:

If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

CPU1B — SANDY — 2 OF 9

MISC: SNB_IVB#, SKTOCC#
THERMAL: CATERR#, PECI, PROCHOT#, THERMTRIP#
PWR MANAGEMENT: PM_SYNC, UNCOREPWRGOOD, SM_DRAMPWROK, RESET#
CLOCKS: BCLK, BCLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#
DDR3 MISC: SM_DRAMRST#, SM_RCOMP0, SM_RCOMP1, SM_RCOMP2
JTAG & BPM: PRDY#, PREQ#, TCK, TMS, TRST#, TDI, TDO, DBR#, BPM#0–BPM#7

1D05V_VTT
R501 1 — H_PROHOT# — 62R2J-GP
C502 SC47P50V2JN-3GP

CRB : 47pf
CEKLT:43pf

(18) H_SNB_IVB# — C26 SNB_IVB#
TPAD14-GP TP501 — SKTOCC#_R — AN34 SKTOCC#
TPAD14-GP TP502 — H_CATERR# — AL33 CATERR#
(22,27) H_PECI — AN33 PECI
(27,40,42) H_PROCHOT# — R513 — H_PROCHOT#_R — AL32 PROCHOT#
56R2J-4-GP
Connect EC to PROCHOT# through inverting OD buffer.
(22,36) H_THERMTRIP# — AN32 THERMTRIP#

R503 — H_CPUPWRGD_R — 10KR2J-3-GP
(19) H_PM_SYNC — AM34 PM_SYNC
(22,36) H_CPUPWRGD — R504 — H_CPUPWRGD_R — AP33 UNCOREPWRGOOD
0R0402-PAD
(19,37) PM_DRAM_PWRGD — R505 DY 0R2J-2-GP — VDDPWRGOOD — V8 SM_DRAMPWROK
(37) VDDPWRGOOD
(18,27,65,71,82,83) PLT_RST# — R510 — 1K5R2F-2-GP — BUF_CPU_RST# — AR33 RESET#
R509 750R2F-GP
DY C501 SC220P50V2KX-3GP

SANDY

BCLK, BCLK# — A28, A27 — CLK_EXP_P (20), CLK_EXP_N (20)
DPLL_REF_SSCLK — A16 CLK_DP_P_R
DPLL_REF_SSCLK# — A15 CLK_DP_N_R
RN502 — SRN1KJ-7-GP — 1D05V_VTT
20110104 A00:
merge R512,R514 to RN502 1k array resistor.
20110113 A00:
Swap RN502 base on swap report.

SM_DRAMRST# — R8 — R502 4K99R2F-L-GP — SM_DRAMRST# (37)
SM_RCOMP0 — AK1 — SM_RCOMP_0 R506 — 140R2F-GP
SM_RCOMP1 — A5 — SM_RCOMP_1 R507 — 25D5R2F-GP
SM_RCOMP2 — A4 — SM_RCOMP_2 R508 — 200R2F-L-GP
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

PRDY# — AP29
PREQ# — AP27
TCK — AR26 XDP_TCLK
TMS — AR27 XDP_TMS
TRST# — AP30 XDP_TRST#
TDI — AR28 XDP_TDI
TDO — AP26 XDP_TDO
DBR# — AL35 XDP_DBRESET#
BPM#0 — AT28
BPM#1 — AR29
BPM#2 — AR30
BPM#3 — AT30
BPM#4 — AP32
BPM#5 — AR31
BPM#6 — AT31
BPM#7 — AR32
GP

1D05V_VTT
RN501 — SRN51J-1-GP
XDP_TDI 1 8
XDP_TMS 2 7
XDP_TDO 3 6
XDP_TCLK 4 5
XDP_TRST# — R511 — 51R2J-2-GP

3D3V_S0
XDP_DBRESET# — R516 — 10KR2J-3-GP

Buffered reset to CPU

1D05V_VTT
DY R518 75R2J-1-GP
3D3V_S0
DY C503 SCD1U10V2KX-5GP
U501 — 74VHC1G09DFT2G-GP — 73.01G09.AAH
IN B, VCC, IN A, DY, GND, OUT Y
(18,27,65,71,82,83) PLT_RST#
BUFO_CPU_RST# — R517 DY 43R2J-GP — BUF_CPU_RST#
DY R515 0R2J-2-GP

XDP_DBRESET# — XDP_DBRESET# (19)

<Core Design>

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Title: CPU 2/7(THERMAL/CLOCK/PM)
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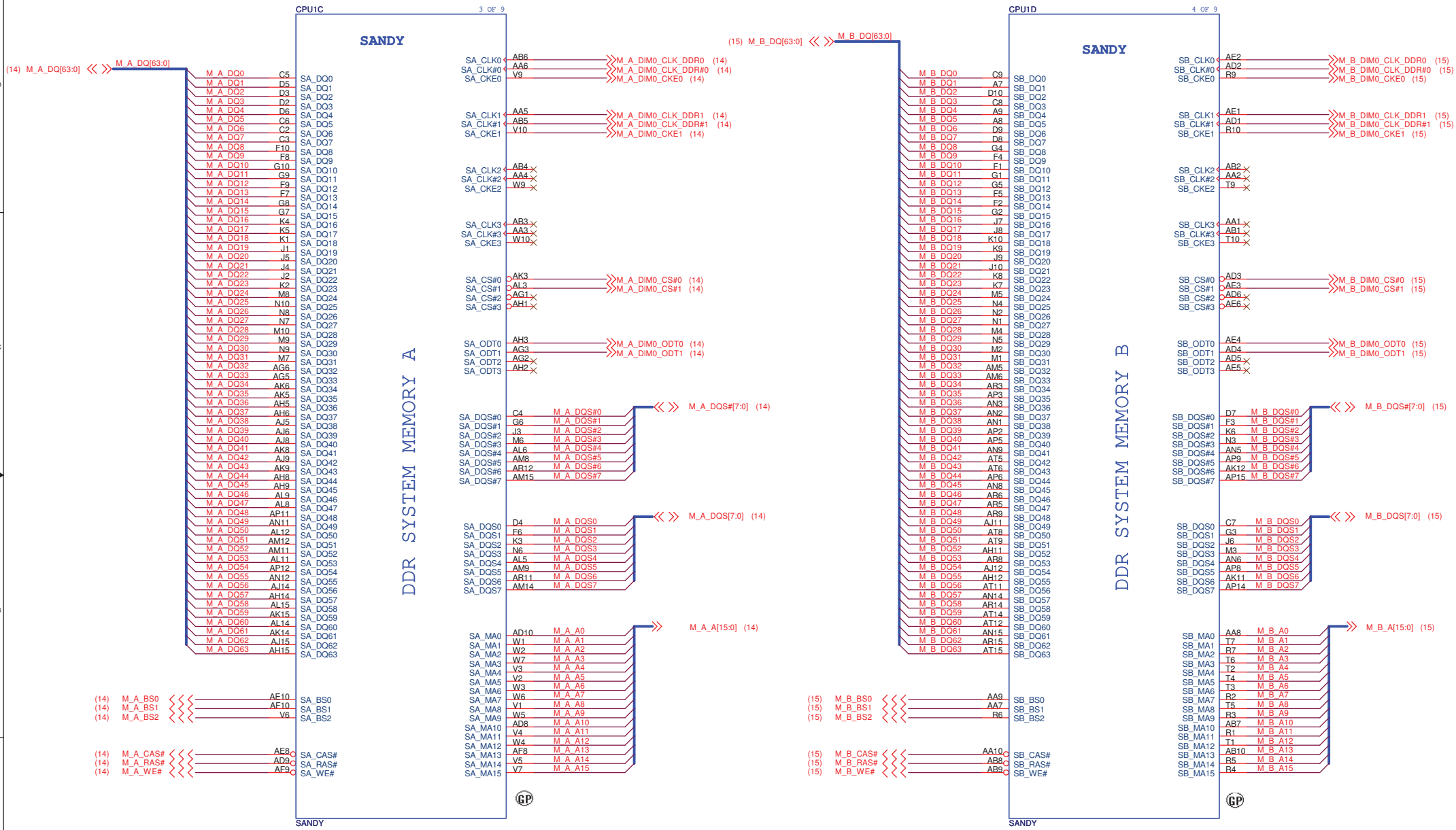
SSID = CPU



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Title: CPU 3/7(DDR)

Size | Document Number: Nirvana 13 | Rev: A00

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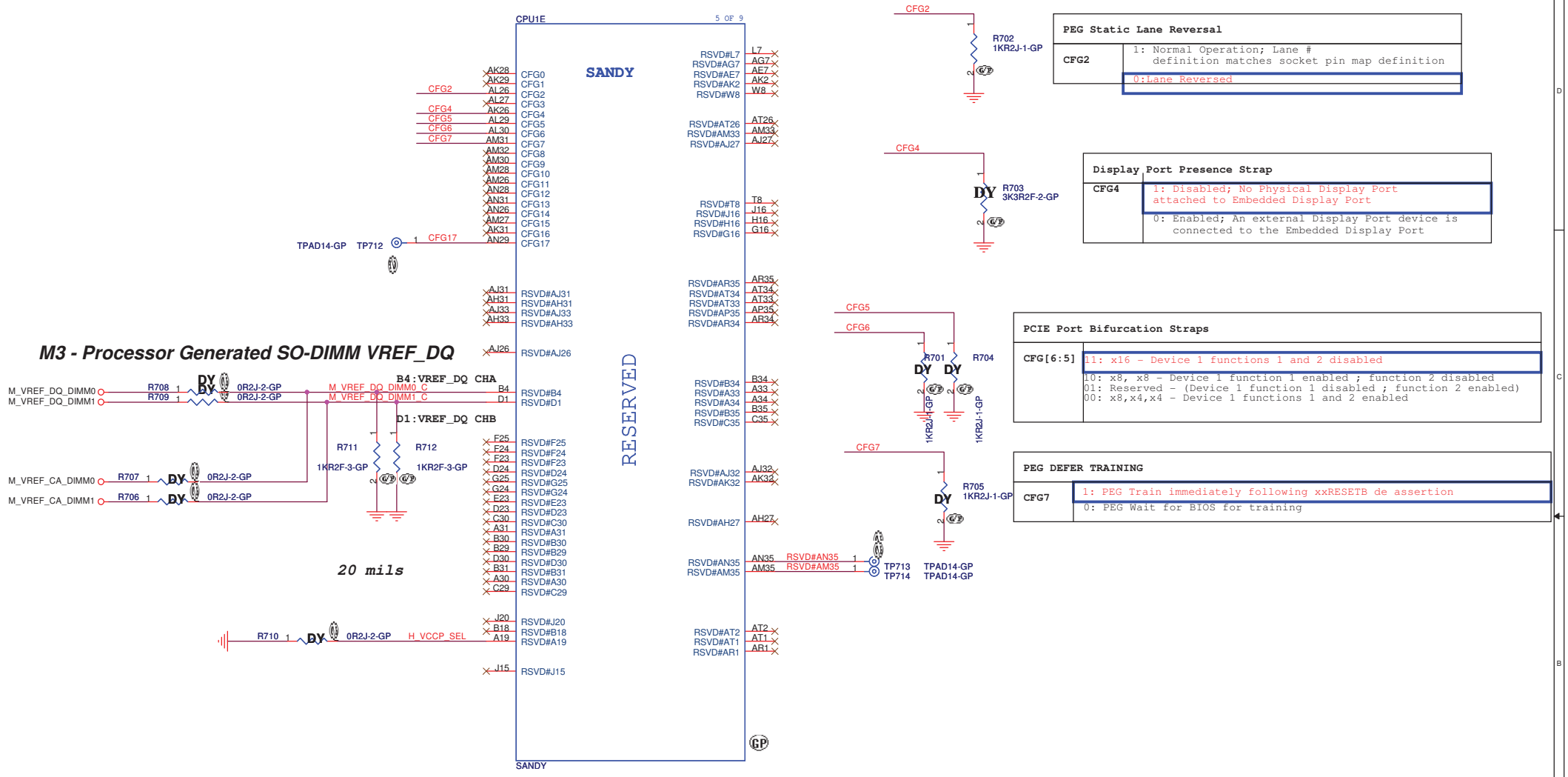
SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

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Title: CPU 4/7(RESERVED)

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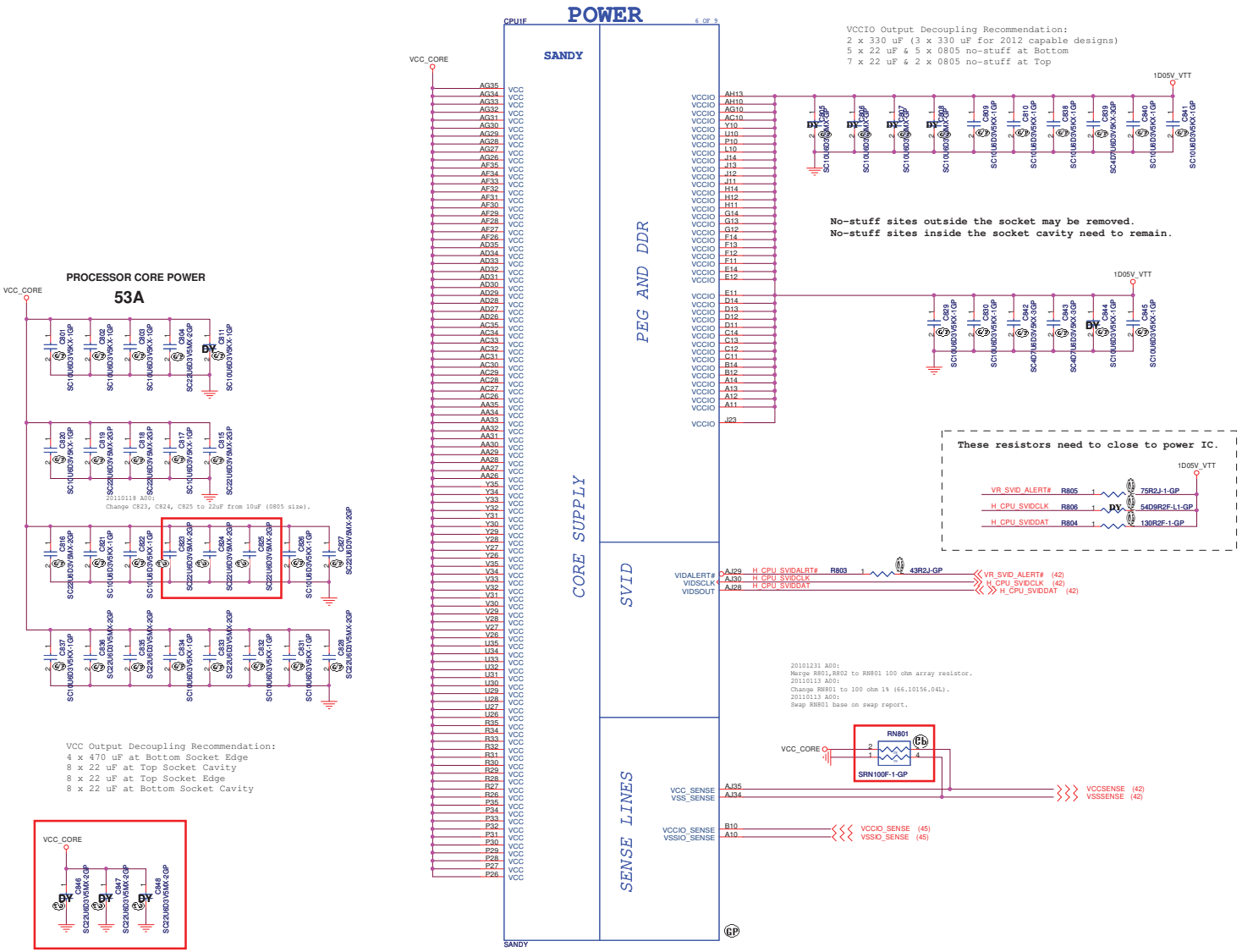
Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

POWER



<Core Design>

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Title: CPU 5/7(VCC_CORE)

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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

POWER

20101231 A00:
Merge R906,R907 to RN902 100 ohm array resistor.
20110113 A00:
Change RN801 to 100 ohm 1% (66.10156.04L).

RN902 SRN100F-1-GP: VCC_AXG_SENSE, VSS_AXG_SENSE → VCC_GFXCORE

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

VCC_GFXCORE

PROCESSOR VAXG: 33A

C901 SC10U6D3V5KX-1GP; C902 SC4D7U6D3V5KX-3GP; C903 SC4D7U6D3V5KX-3GP; C904 SC4D7U6D3V5KX-3GP; C905 SC22U6D3V5MX-2GP; C906 SC4D7U6D3V5KX-3GP

C908 SC10U6D3V3MX-GP; C920 SC10U6D3V3MX-GP; C921 SC10U6D3V3MX-GP

CPU1G — 7 OF 9 — SANDY

VAXG: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17

SENSE LINES: VAXG_SENSE AK35 → VCC_AXG_SENSE (42); VSSAXG_SENSE AK34 → VSS_AXG_SENSE (42)

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF: SM_VREF AL1 → +V_SM_VREF_CNT (37)

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS: VDDQ AF7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

PROCESSOR VDDQ: 10A

1D5V_S0 → C909 SC10U6D3V3MX-GP; C910 SC10U6D3V3MX-GP; C911 SC10U6D3V3MX-GP; C912 SC10U6D3V5KX-1GP; C913 SC10U6D3V5KX-1GP; C914 SC4D7U6D3V5KX-3GP; TC901 SC330U2VDM-4-GP; C907 SCD1U10V2KX-5GP; C918 SCD1U10V2KX-5GP; C919 SCD1U10V2KX-5GP; C925 SCD1U10V2KX-5GP; C926 SCD1U10V2KX-5GP → 1D5V_S3

79.33719.20L
2nd = 77.C3371.13L

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL: VCCSA M27, M26, L26, J26, J25, J24, H26, H25

0D85V_S0

PROCESSOR VCCSA: 6A

C916 SC10U6D3V5KX-1GP; C915 SC10U6D3V5KX-1GP; C917 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C923 SC10U6D3V5KX-1GP; C922 SC1U10V2KX-1GP; C924 SC1U10V2KX-1GP

1.8V RAIL: VCCPLL B6, A6, A2

MISC: VCCSA_SENSE H23 → VCCUSA_SENSE (48)

FC_C22 / VCCSA_VID1: C22 H_FC_C22 → H_FC_C22 (48); C24 VCCSA_SEL → VCCSA_SEL (48)

RN901 SRN1KJ-7-GP

SANDY

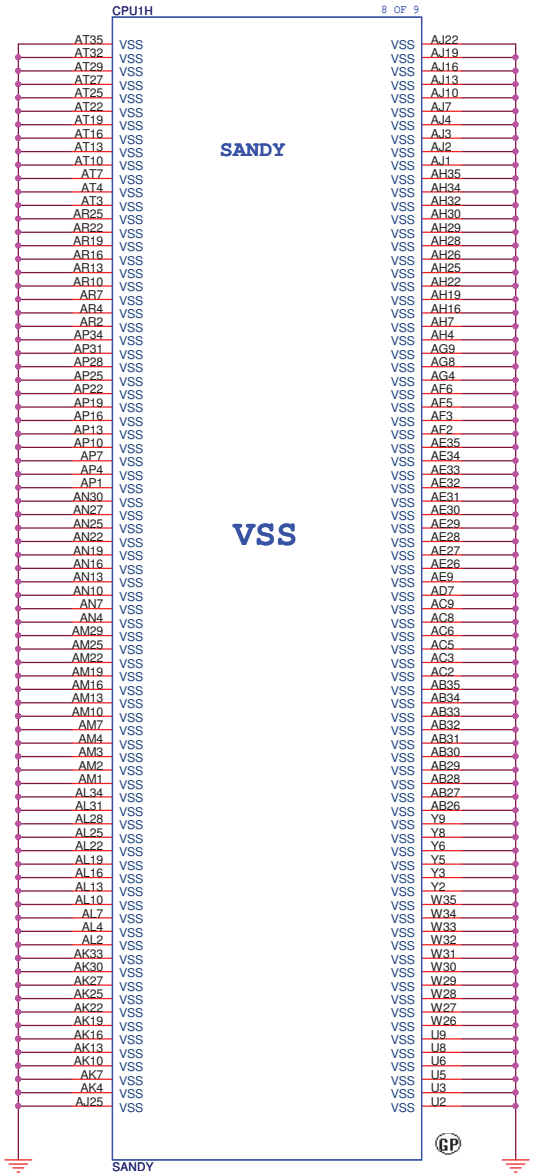
VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

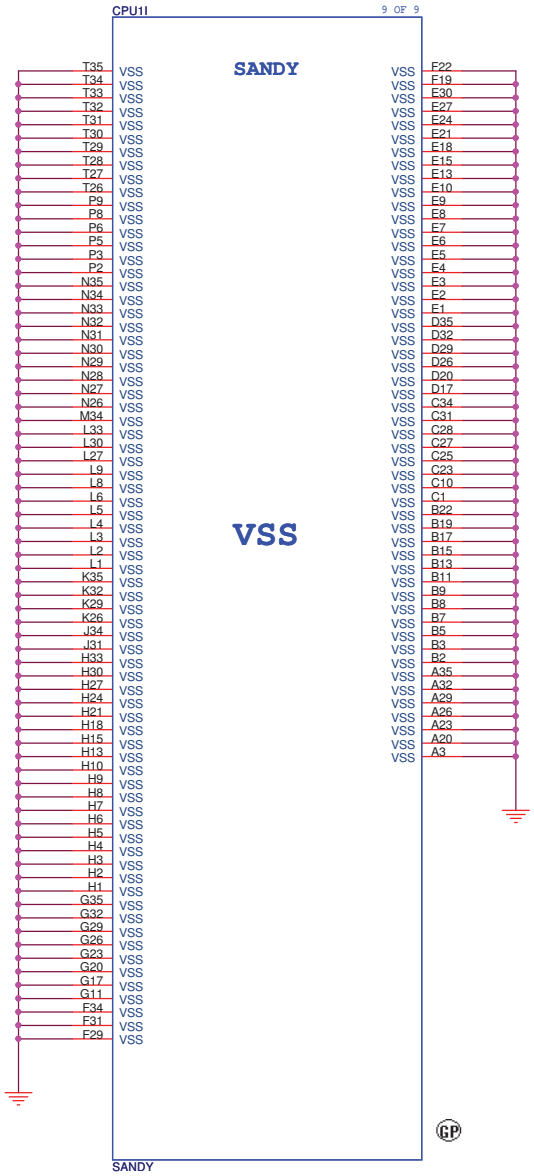
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU 6/7(VCC_GFX_CORE)
Size | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 9 of 104

SSID = CPU





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU 7/7(VSS)	
Size	Document Number: Nirvana 13	Rev: A00
Date: Tuesday, January 04, 2011	Sheet 10 of 104	

(Blanking)

Remove the XDP connector for space saving 6/28

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *XDP*

Size: A3 | Document Number: NIRVANA 13 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 11 of 104

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Nirvana 13*	*A00*

Date: Tuesday, January 04, 2011 Sheet 12 of 104

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<Core Design>

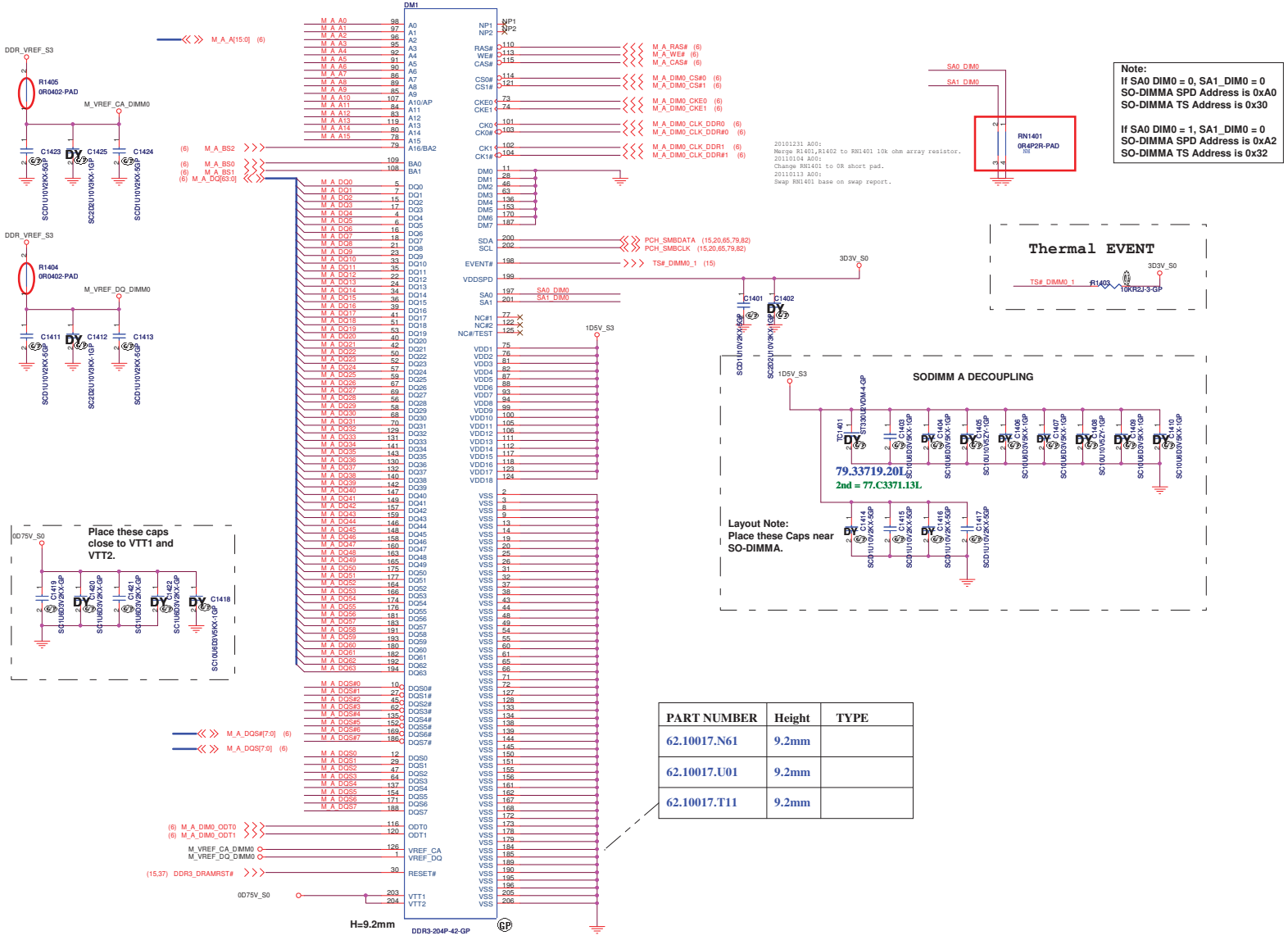
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 13 of 104

SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

20101231 A00:
Merge R1401,R1402 to RN1401 10k ohm array resistor.
20110104 A00:
Change RN1401 to 0R short pad.
20110113 A00:
Swap RN1401 base on swap report.

20101224 A00:
0402 0R pad: R1404 R1405.

PART NUMBER	Height	TYPE
62.10017.N61	9.2mm	
62.10017.U01	9.2mm	
62.10017.T11	9.2mm	

<Core Design>

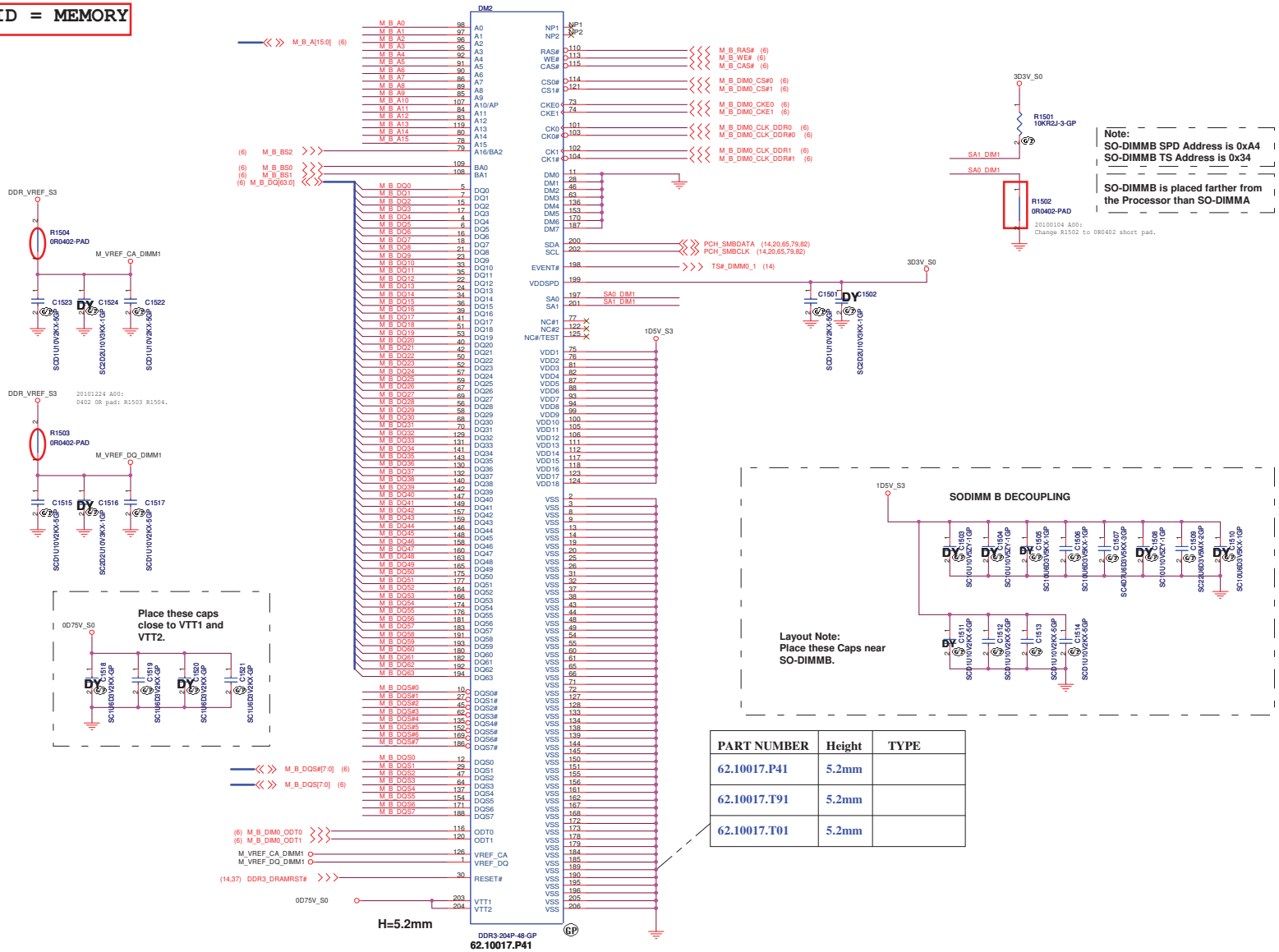
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-DIMM1 SOCKET1

Size	Document Number	Rev
	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 14 of 104

SSID = MEMORY



PART NUMBER	Height	TYPE
62.10017.P41	5.2mm	
62.10017.T91	5.2mm	
62.10017.T01	5.2mm	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-DIMM2 SOCKET2

Size | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 18, 2011 | Sheet 15 of 104

(Blanking)

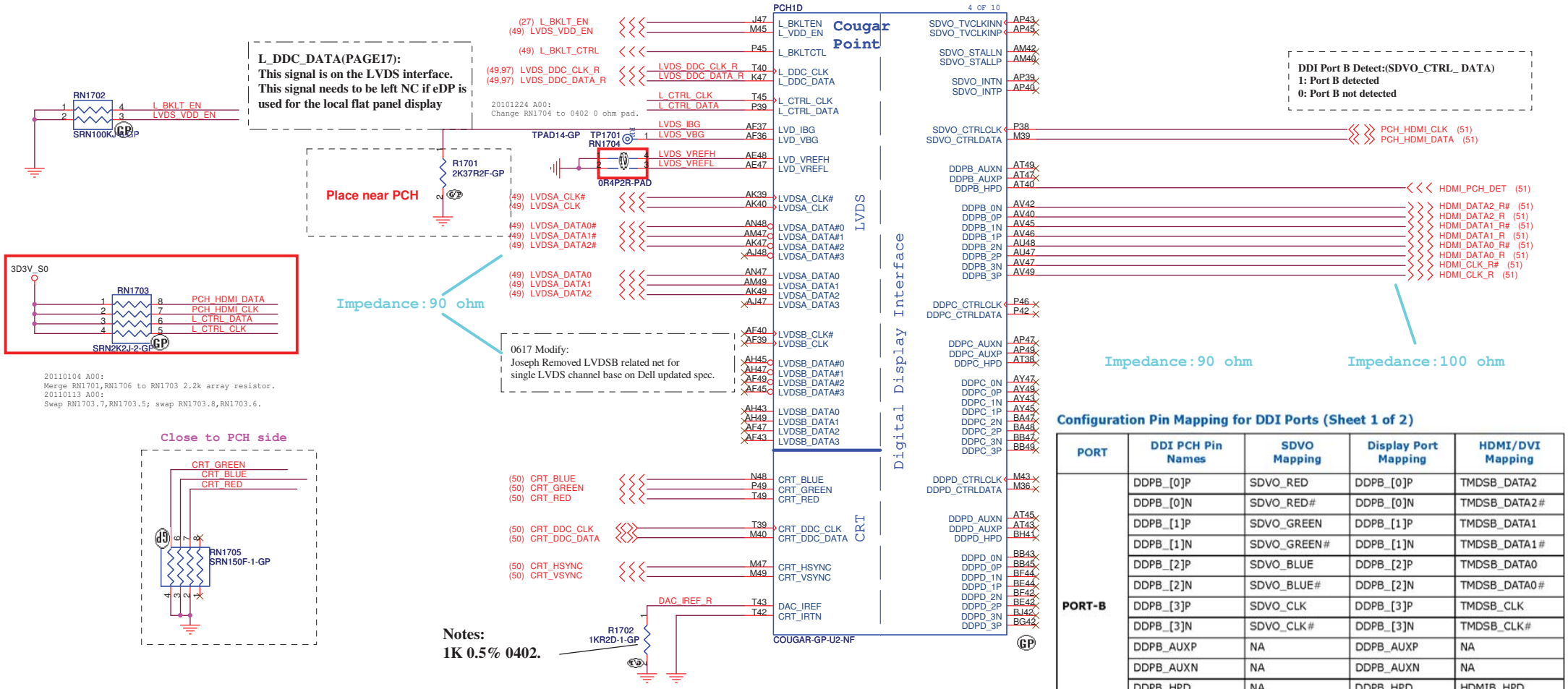
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 16 of 104



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 1/9(LVDS/CRT/DDI)

Size | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 18, 2011 | Sheet 17 of 104

SSID = PCH

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

RN1801 SRN8K2J-2-GP: INT_PIRQB#, INT_PIRQF#, INT_PIRQA# → INT_PIRQD#, INT_PIRQE#, INT_PIRQC#, INT_PIRQG#; 3D3V_S0

R1801 4K7R2J-2-GP DY PCI_GNT3#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

R1802 1KR2J-1-GP DY BBS_BIT1
R1803 1KR2J-1-GP DY BBS_BIT0 (21)

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

RN1803 SRN10KJ-5-GP: DGPU_HOLD_RST#, DGPU_PWR_EN#

PCH1E — Cougar Point — 5 OF 10

RSVD: TP1–TP20, TP21–TP24, TP25–TP40

NVRAM: RSVD, DF_TVS, NV_ALE, NV_CLE, NV_RCOMP → TP1803 TPAD14-GP

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB: USBP0N–USBP13N, USBP0P–USBP13P → USB_PN1 (57), USB_PP1 (57), USB_PN2 (64), USB_PP2 (64), USB_PN3 (63), USB_PP3 (63), USB_PN4 (82), USB_PP4 (82), USB_PN5 (32), USB_PP5 (32), USB_PN11 (65), USB_PP11 (65), USB_PN12 (49), USB_PP12 (49)

USBRBIAS# C33 — USB_RBIAS — R1811 22D6R2F-L1-GP — USBRBIAS B33

OC0#/GPIO59 A14 → USB_OC#0_1 (61)
OC1#/GPIO40 K20 → USB_OC#2_3
OC2#/GPIO41 B17 → USB_OC#4_5
OC3#/GPIO42 C16 → USB_OC#6_7
OC4#/GPIO43 L16 → USB_OC#8_9
OC5#/GPIO9 A16 → USB_OC#10_11
OC6#/GPIO10 D14 → USB_OC#12_13
OC7#/GPIO14 C14 → FFS_INT2_R (79)

PCI: PIRQA# K40 ← INT_PIRQA#; PIRQB# K38 ← INT_PIRQB#; PIRQC# H38 ← INT_PIRQC#; PIRQD# G38 ← INT_PIRQD#
R1814 8K2R2J-3-GP (3D3V_S0)

REQ1#/GPIO50 C46 ← DGPU_SELECT# (83) DGPU_HOLD_RST# TPAD14-GP TP1807
REQ2#/GPIO52 C44 ← DGPU_PWR_EN# (93) DGPU_PWR_EN#
REQ3#/GPIO54 E40

GNT1#/GPIO51 D47 ← BBS_BIT1
GNT2#/GPIO53 E42 ← DGPU_PWM_SELECT# TPAD14-GP TP1806
GNT3#/GPIO55 F46 ← PCI_GNT3# TPAD14-GP TP1801

PIRQE#/GPIO2 G42 ← R1812 0R0402-PAD ← INT_PIRQE# (79) HDD_FALL_INT1
PIRQF#/GPIO3 G40 ← R1813 0R0402-PAD ← INT_PIRQF# (56) SATA_ODD_DA#
PIRQG#/GPIO4 C42 ← R1815 0R0402-PAD ← INT_PIRQG# (82) USB30_SMI#
PIRQH#/GPIO5 D44 ← R1817 0R0402-PAD ← INT_PIRQH# (69) KB_LED_BL_DET

PME# K10 ← TPAD14-GP TP1802 ← PCI_PME#
PLTRST# C6 ← PCI_PLTRST#

CLKOUT_PCI0 H49 → CLK_PCI_LPC_R → R1805 22R2J-2-GP → CLK_PCI_LPC (65,71,97)
CLKOUT_PCI1 H43 → CLK_PCI_FB_R → CLK_PCI_FB (20)
CLKOUT_PCI2 J48 → CLK_PCI_KBC_R → CLK_PCI_KBC (27)
CLKOUT_PCI3 K42
CLKOUT_PCI4 H40

COUGAR-GP-U2-NF

RN1804 SRN22-3-GP

20101231 A00:
Merge R1804,R1806 to RN1804 22 ohm array resistor.
20110113 A00:
Swap RN1804 base on swap report.

KBC CLK EMI

EC1801 DY SC4D7P50V2CN-1GP
EC1802 DY SC4D7P50V2CN-1GP

20101224 A00:
0402 0R pad: R1807.

R1807 0R0402-PAD: (5,27,65,71,82,83) PLT_RST# → PCI_PLTRST#

R1816 100KR2J-1-GP DY
C1801 SC220P50V2KX-3GP DY

R1818 10KR2J-3-GP FFS_INT2_R

RN1802 SRN8K2J-2-GP: USB_OC#2_3, USB_OC#6_7, USB_OC#0_1 → USB_OC#12_13, USB_OC#8_9, USB_OC#10_11, USB_OC#4_5; 3D3V_S5

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

1D8V_S0
R1808 2K2R2J-2-GP
R1809 1KR2J-1-GP NV_CLE → H_SNB_IVB# (5)

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

1D8V_S0
R1810 1KR2J-1-GP DY NV_ALE

Danbury Technology: Disabled when Low. Enable when High.

USB Table

Pair	Device
0	X
1	E-SATA / USB Combo
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	X
9	X
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 2/9(PCI/USB/NVRAM)
Size: Document Number: Nirvana 13 Rev: A00
Date: Tuesday, January 18, 2011 Sheet 18 of 104

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

(4) DMI_RXN[3:0]
(4) DMI_RXP[3:0]
(4) DMI_TXN[3:0]
(4) DMI_TXP[3:0]

FDI_TXN[7:0] (4)
FDI_TXP[7:0] (4)

PCH1C — 3 OF 10 — Cougar Point

DMI: DMI0RXN BC24, DMI1RXN BE20, DMI2RXN BG18, DMI3RXN BG20; DMI0RXP BE24, DMI1RXP BC20, DMI2RXP BJ18, DMI3RXP BJ20; DMI0TXN AW24, DMI1TXN AW20, DMI2TXN BB18, DMI3TXN AV18; DMI0TXP AY24, DMI1TXP AY20, DMI2TXP AY18, DMI3TXP AU18

FDI: FDI_RXN0 BJ14, FDI_RXN1 AY14, FDI_RXN2 BE14, FDI_RXN3 BH13, FDI_RXN4 BC12, FDI_RXN5 BJ12, FDI_RXN6 BG10, FDI_RXN7 BG9; FDI_RXP0 BG14, FDI_RXP1 BB14, FDI_RXP2 BE14, FDI_RXP3 BG13, FDI_RXP4 BE12, FDI_RXP5 BG12, FDI_RXP6 BJ10, FDI_RXP7 BH9; FDI_INT AW16; FDI_FSYNC0 AV12, FDI_FSYNC1 BC10; FDI_LSYNC0 AV14, FDI_LSYNC1 BB10

1D05V_VTT
R1901 1 49D9R2F-GP DMI_COMP_R — BJ24 DMI_ZCOMP
R1902 1 750R2F-GP RBIAS_CPY — BG25 DMI_IRCOMP; BH21 DMI2RBIAS

System Power Management

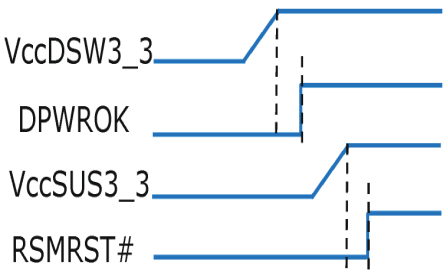
DSWVRMEN A18 DSWODVREN
DPWROK E22 PCH_DPWROK — R1910 0R0402-PAD PM_RSMRST# — DY R1911 10KR2J-3-GP — RTC_AUX_S5
WAKE# B9 PCH_WAKE# (27)
CLKRUN#/GPIO32 N3 PM_CLKRUN# (27)
SUS_STAT#/GPIO61 G8 PM_SUS_STAT# — TP1901 TPAD14-GP
SUSCLK/GPIO62 N14 SUS_CLK — R1913 0R0402-PAD — PCH_SUSCLK_KBC (27)
SLP_S5#/GPIO63 D10 PM_SLP_S5# — TP1902 TPAD14-GP
SLP_S4# H4 PM_SLP_S4# (27,46)
SLP_S3# F4 PM_SLP_S3# (27,36,37,46,47)
SLP_A# G10 PM_SLP_A# — TP1903 TPAD14-GP
SLP_SUS# G16 PM_SLP_SUS# — TP1904 TPAD14-GP
PMSYNCH AP14 H_PM_SYNC H_PM_SYNC (5)
SLP_LAN#/GPIO29 K14 PM_SLP_LAN# — TP1905 TPAD14-GP

1 DY R1926 10KR2J-3-GP SYS_PWROK
1 DY R1904 100KR2J-1-GP PWROK
SUS_PWR_ACK — R1903 0R0402-PAD — SUSACK# C12 SUSACK#
(5) XDP_DBRESET# — R1925 0R0402-PAD — SYS_RESET# K3 SYS_RESET#
3D3V_S0 — DY R1905 10KR2J-3-GP
(36) SYS_PWROK — R1923 DY 0R2J-2-GP — P12 SYS_PWROK
(27,36) S0_PWR_GOOD — R1924 0R0402-PAD — PWROK L22 PWROK
(45,46,47) RUNPWROK — R1907 DY 0R2J-2-GP — R1906 0R0402-PAD — MEPWROK L10 APWROK
(5,37) PM_DRAM_PWRGD B13 DRAMPWROK
PM_RSMRST# C21 RSMRST#
(27) SUS_PWR_ACK K16 SUSWARN#/SUSPWRDNACK/GPIO30
(27) PM_PWRBTN# E20 PWRBTN#
(27) AC_PRESENT H20 ACPRESENT/GPIO31
BATLOW# E10 BATLOW#/GPIO72
PM_RI# A10 RI#

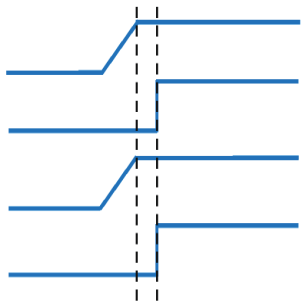
COUGAR-GP-U2-NF

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

Deep S4/S5 Supported



Deep S4/S5 **Not** Supported



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN – On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
R1917 1 330KR2J-L1-GP
DSWODVREN — R1918 1 DY 330KR2J-L1-GP

PM_RSMRST# — R1912 0R0402-PAD — RSMRST#_KBC (27)

3D3V_S0
PM_CLKRUN# — R1919 1 8K2R2J-3-GP

3D3V_S5
RN1901 SRN10KJ-6-GP: 8 BATLOW#, 7 PM_RI#, 6 PCH_WAKE#, 5 SUS_PWR_ACK
R1921 1 100KR2J-1-GP AC_PRESENT
R1922 DY 1 10KR2J-3-GP PM_PWRBTN#
R1920 DY 1 10KR2J-3-GP PM_SLP_LAN#
R1908 1 10KR2J-3-GP PM_RSMRST#

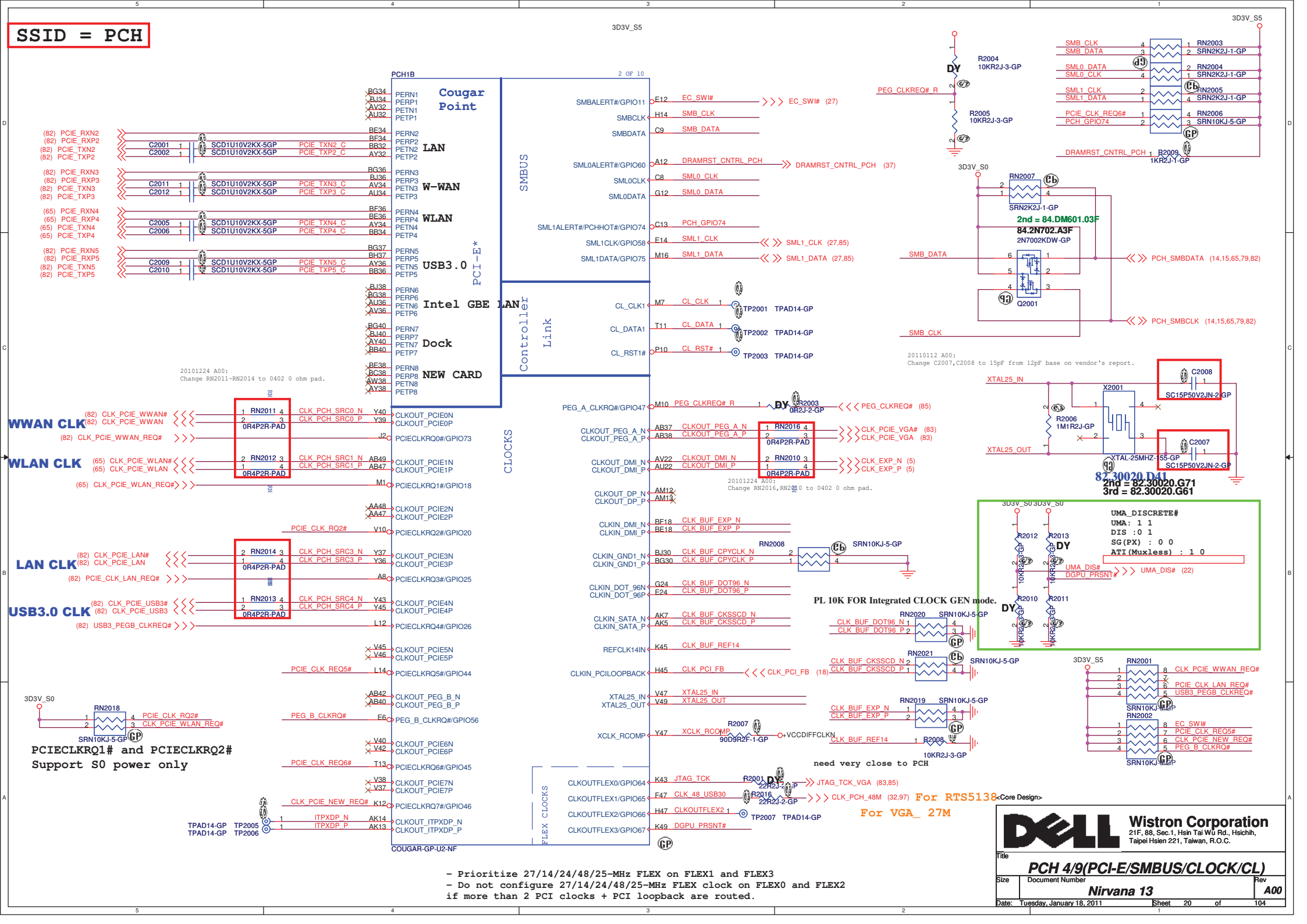
PCH_SUSCLK_KBC — EC1901 DY SC4D7P50V2CN-1GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 3/9(DM I/FDI/PM)
Size: | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 19 of 104

SSID = PCH



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 4/9(PCI-E/SMBUS/CLOCK/CL)

Size	Document Number	Rev
	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 20 of 104

SSID = PCH

20110110 A00:
Merge R2115,R2116 to RN2101.
20110113 A00:
Swap RN2101 base on swap report.

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Notes:
ME_UNLOCK (HDA_SDO) connect to EC.
Make sure EC drive this pin "low" all the time.

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

NO REBOOT STRAP

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

2nd = 82.30001.691
3rd = 82.30001.861
2ND = 84.2N702.031

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 5/9(SPI/RTC/LPC/SATA/IHDA)
Size: | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 21 of 104

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	GSENSOR_ADI	GSENSOR_ST
R2205	DY	10K
R2206	100K	DY

3D3V_S0 — R2202 100KR2J-1-GP — SATA_ODD_PRSNT#

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_A20GATE, H_RCIN#

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

3D3V_S0 — R2220 10KR2J-3-GP — PCH_GPIO48

20100104 A00:
Merge RN2201,R2222,R2223 to 10k array resistor.
20110113 A00:
Combine PCH_TEMP_ALERT#,MFG_MODE to RN2202.
Combine EC_SCI#,DGPU_HPD_INTR# to RN2204

3D3V_S0 — RN2202 SRN10KJ-5-GP — PCH_TEMP_ALERT#, MFG_MODE

RN2204 SRN10KJ-5-GP — EC_SCI#, DGPU_HPD_INTR#

DBC_EN — R2214 10KR2J-3-GP DY

20100104 A00:
Merge RN2215,R2216 to RN2201 10k array resistor.

3D3V_S5 — RN2201 SRN10KJ-5-GP — RTC_DET#, PCH_GPIO57

R2217 10KR2J-3-GP DY

PCH_GPIO15 — R2201 1KR2J-1-GP

3G_EN — R2221 10KR2J-3-GP

For thermal sensor detection.

3D3V_S0 — R2224 10KR2J-3-GP DY — VRAM_SIZE1 — R2225 10KR2J-3-GP DY

PCH1F — 6 OF 10 — Cougar Point — COUGAR-GP-U2-NF

(21) S_GPIO	S_GPIO	R2218 100R2J-2-GP	GPIO0 T7
(21,27) EC_SMI#	EC_SMI#		A42
	DGPU_HPD_INTR#		H36
(27) EC_SCI#	EC_SCI#		E38
	ICC_EN#		C10
(60) RTC_DET#	RTC_DET#		C4
	PCH_GPIO15		G2
(56) SATA_ODD_PRSNT#		R2213 0R0402-PAD	PCH_GPIO16 U2
(86,92,93) DGPU_PWROK	DGPU_PWROK		D40
(49) DBC_EN	DBC_EN		T5
(82) 3G_EN	3G_EN		E8
TPAD14-GP TP2203	PCH_GPIO27		E16
	PLL_ODVR_EN		P8
(21) PSW_CLR#	PSW_CLR#		K1
(21) FP_DET#			K4
	DMI_OVRVLTG		V8
	FDI_OVRVLTG		M5
	MFG_MODE		N2
	GSENSOR_DET		M3
	PCH_GPIO48		V13
	PCH_TEMP_ALERT#		V3
	PCH_GPIO57		D6

GAP-OPEN — G2201

TPAD14-GP TP2206	PCH_NCTF_1		A4
			A44
			A45
			A46
			A5
			A6
			B3
			B47
			BD1
			BD49
TPAD14-GP TP2207	PCH_NCTF_2		BE1
TPAD14-GP TP2208	PCH_NCTF_3		BE49
TPAD14-GP TP2209	PCH_NCTF_4		BF1
			BF49

NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47,BD1,BD49,BE1,BE49,BF1,BF49

BG2,BG48,BH3,BH47,BJ4,BJ44,BJ45,BJ46,BJ5,BJ6,C2,C48

D1,D49,E1,E49,F1,F49

C40	SATA_ODD_PWRGT (56)		TACH4/GPIO68
B41	UMA_DIS# (20)		TACH5/GPIO69
C41	VRAM_SIZE1	TP2204 TPAD14-GP	TACH6/GPIO70
A40	VRAM_SIZE2	TP2205 TPAD14-GP	TACH7/GPIO71
			GPIO8
			LAN_PHY_PWR_CTRL/GPIO12
			GPIO15
			SATA4GP/GPIO16
			TACH0/GPIO17
			SCLOCK/GPIO22
			GPIO24/MEM_LED
			GPIO27
			GPIO28
			STP_PCI#/GPIO34
			GPIO35
			SATA2GP/GPIO36
			SATA3GP/GPIO37
			SLOAD/GPIO38
			SDATAOUT0/GPIO39
			SDATAOUT1/GPIO48
			SATA5GP/GPIO49
			GPIO57

GPIO — CPU/MISC — NCTF

P4	H_A20GATE (27)		A20GATE
AU16	H_PECI_R	DY R2203 0R2J-2-GP — H_PECI (5,27)	PECI
P5	H_RCIN# (27)		RCIN#
AY11	H_CPUPWRGD (5,36)		PROCPWRGD
AY10	PCH_THERMTRIP_R	R2204 390R2J-1-GP — H_THERMTRIP# (5,36)	THRMTRIP#
T14	INIT3_3V#	TP2201 TPAD14-GP	INIT3_3V#
AH8			TS_VSS1
AK11			TS_VSS2
AH10			TS_VSS3
AK10	TS_VSS_1	R2219 0R0402-PAD	TS_VSS4
P37			NC_1

BG2	NCTF_VSS#BG2
BG48	NCTF_VSS#BG48
BH3	NCTF_VSS#BH3
BH47	NCTF_VSS#BH47
BJ4	NCTF_VSS#BJ4
BJ44	NCTF_VSS#BJ44
BJ45	NCTF_VSS#BJ45
BJ46	NCTF_VSS#BJ46
BJ5	NCTF_VSS#BJ5
BJ6	NCTF_VSS#BJ6
C2	NCTF_VSS#C2
C48	NCTF_VSS#C48
D1	NCTF_VSS#D1
D49	NCTF_VSS#D49
E1	NCTF_VSS#E1
E49	NCTF_VSS#E49
F1	NCTF_VSS#F1
F49	NCTF_VSS#F49

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

3D3V_S0 — R2205 10KR2J-3-GP — GSENSOR_ST, GSENSOR_DET — R2206 100KR2J-1-GP — GSENSOR_ADI

3D3V_S0 — R2207 10KR2J-3-GP DY — FDI_OVRVLTG — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

3D3V_S0 — R2209 10KR2J-3-GP DY — DMI_OVRVLTG — R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

ICC_EN# — R2211 1KR2J-1-GP

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN — DY R2212 1KR2J-1-GP

<Core Design>

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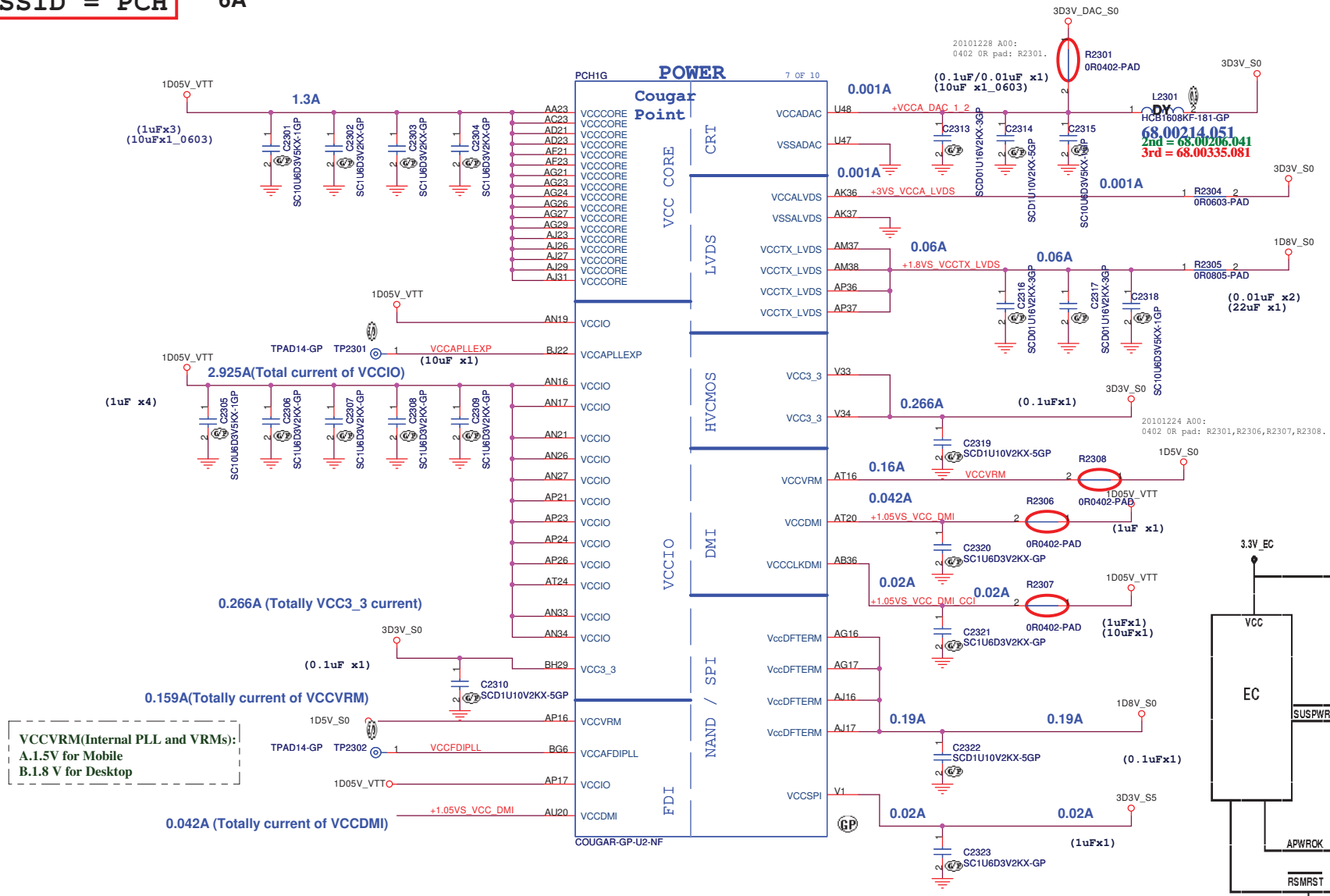
Title: PCH 6/9(GPIO/CPU)

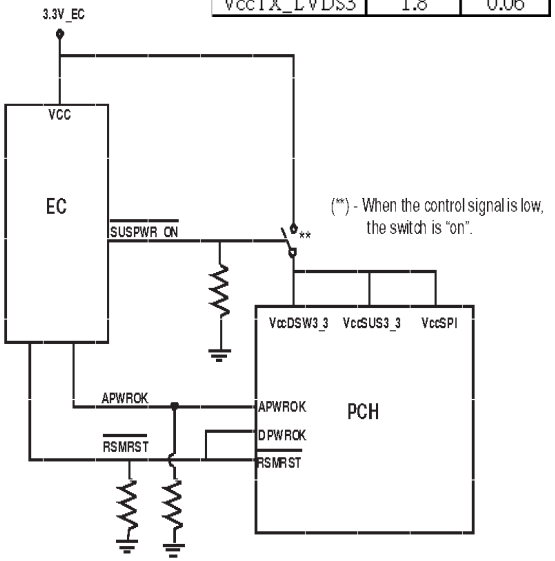
Size	Document Number	Rev
	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 22 of 104

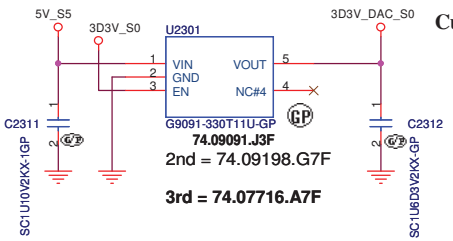
SSID = PCH 6A

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06





3.3V CRT LDO



Current Limit=360mA

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Title: PCH 7/9(POWER1)

Size | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 23 of 104

SSID = PCH

POWER

PCH1J

COUGAR-GP-U2-NF

10 OF 10

Cougar Point

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

20101224 A00:
0402 0R pad: R2404,R2405.

<Core Design>

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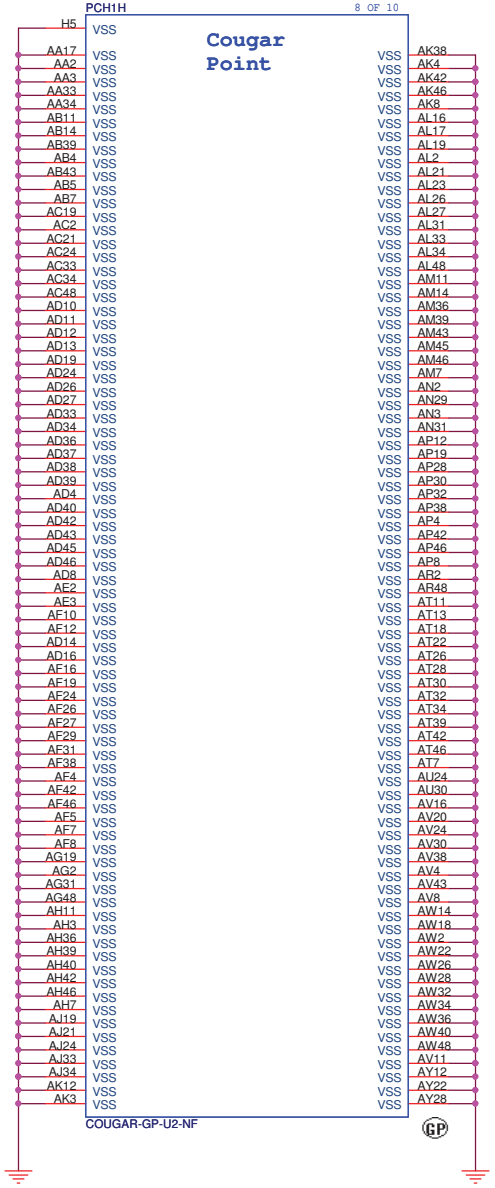
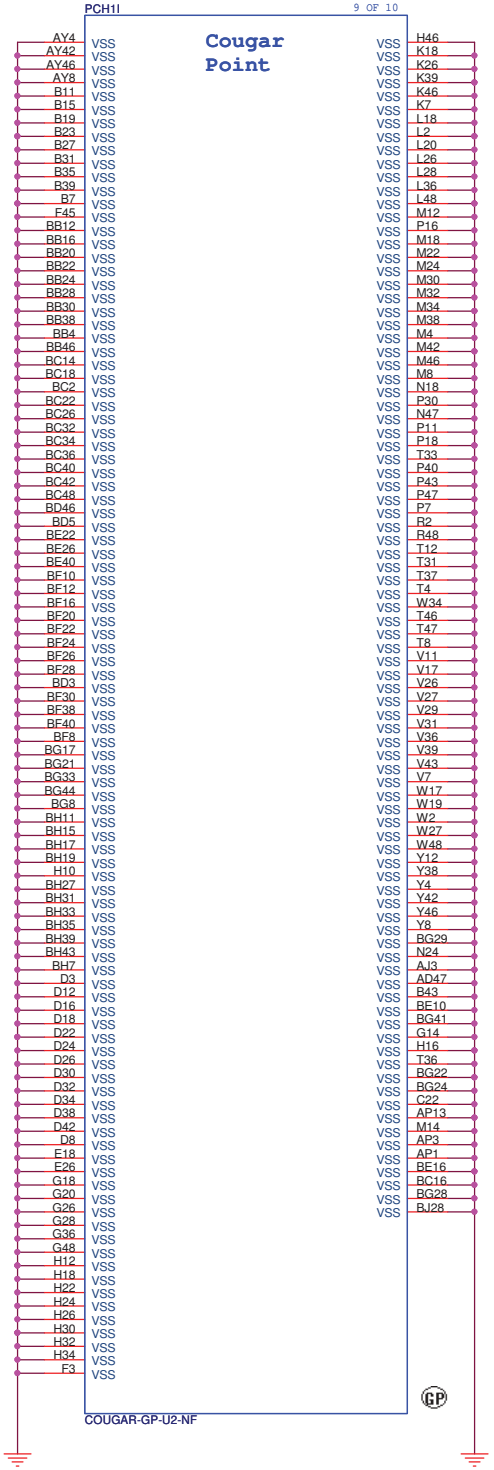
Title: PCH 8/9(POWER2)

Size | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 24 of 104

SSID = PCH





<Core Design>

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Title: PCH 9/9(VSS)

Size | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 25 of 104

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 26 of 104

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DQ15_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DQ15_ATI	100.0K	20.0K(64.20025.6DL)	2.75V
DQ15_NVIDIA	100.0K	33.0K	2.48V
DN15_UMA	100.0K	47.0K(64.47025.6DL)	2.24V
DN15_ATI	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
DN13_UMA	100.0K	143.0K	1.358V
DN13_ATI	100.0K	174.0K	1.204V
DQ15_Ventura	100.0K	215.0K	1.048V

NOTES:
The NPCE795P GPIO/PWM outputs that are connected to LEDs have high drive buffers (20mA) and can be connected directly to the LEDs.

Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

ROSA Multi GPIO setting

NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,E51_TXD.

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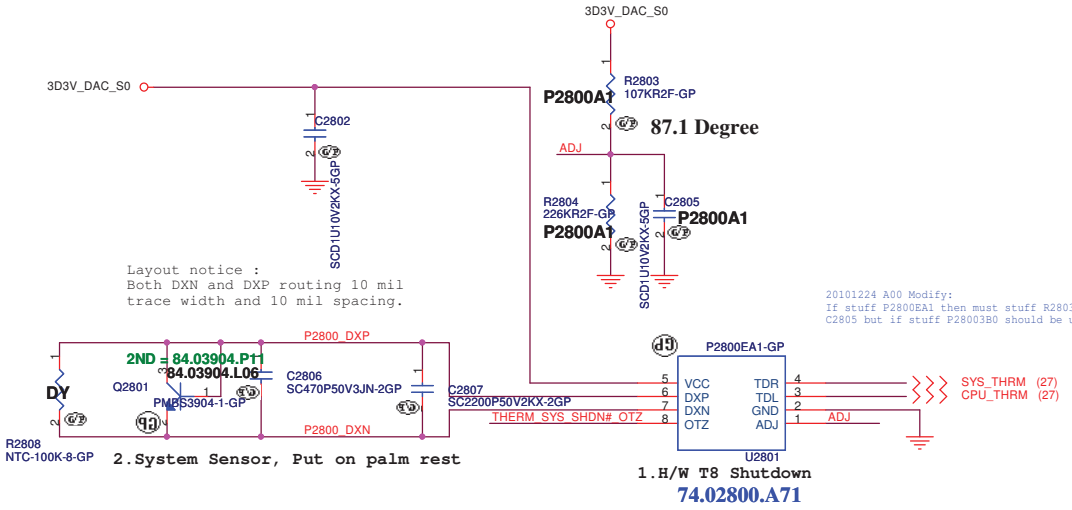
Title: KBC Nuvoton NPCE785P

Size: A2 | Document Number: Nirvana 13 | Rev: A00

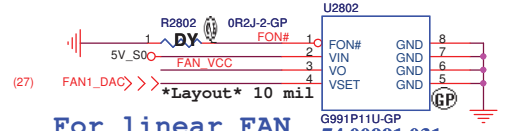
Date: Tuesday, January 18, 2011 | Sheet 27 of 104

SSID = Thermal

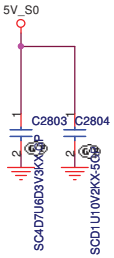
Thermal sensor P2800

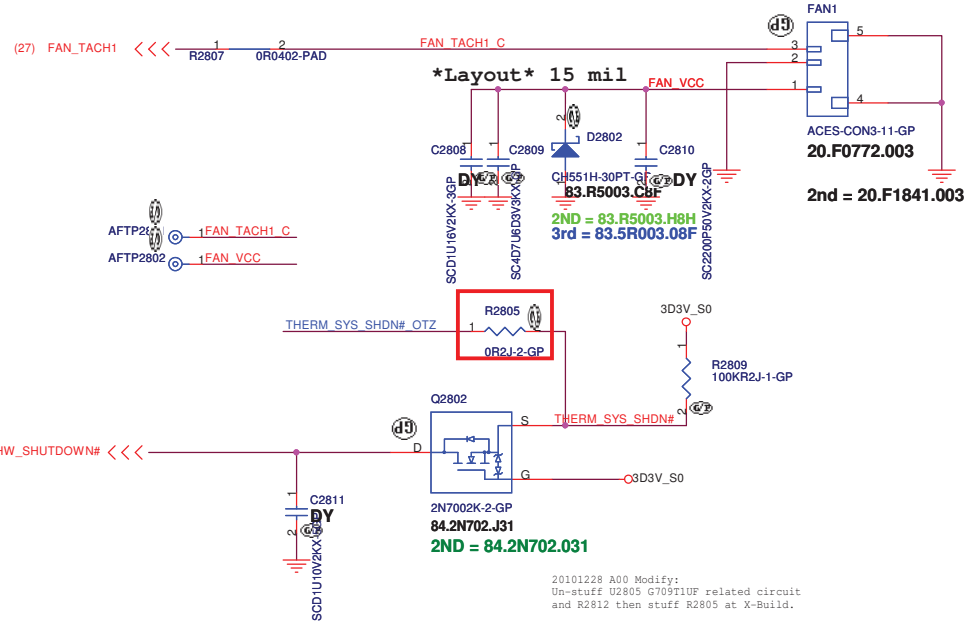


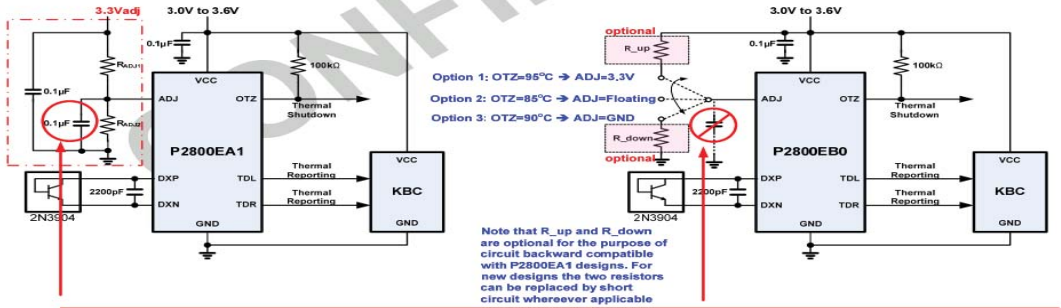
Fan controller



PIN#	I/O	FUNCTION
1	I	Internal Pull-high (P2793A). The IC will be functioning when /FON voltage is above 1.6V. When /FON is low(<0.4V), VOUT will be fully on
2	O	Input Voltage
3	O	Output Voltage
4	I	The voltage on this input pin controls the VOUT voltage by the formula: VOUT=1.6 * VSET When VSET is under 0.8V, the IC will be shutdown
5,6,7,8	O	Ground





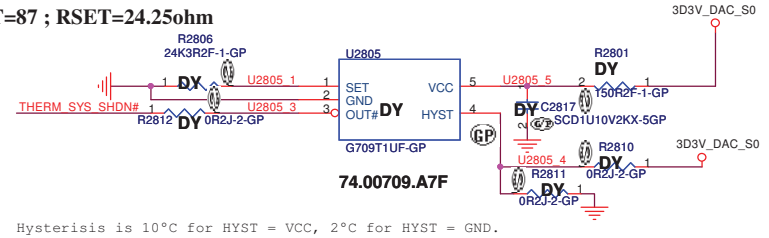


Note:
The original 0.1uF capacitor for P2800EA1 deisgn must be REMOVED on the ADJ pin of P2800EB0

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

RSET = 0.0012T 2 — 0.9308T + 96.147
T=87 ; RSET=24.25ohm



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Title: THERMAL P2800 / Fan control

Size	Document Number	Rev
A3	Nirvana 13	A00

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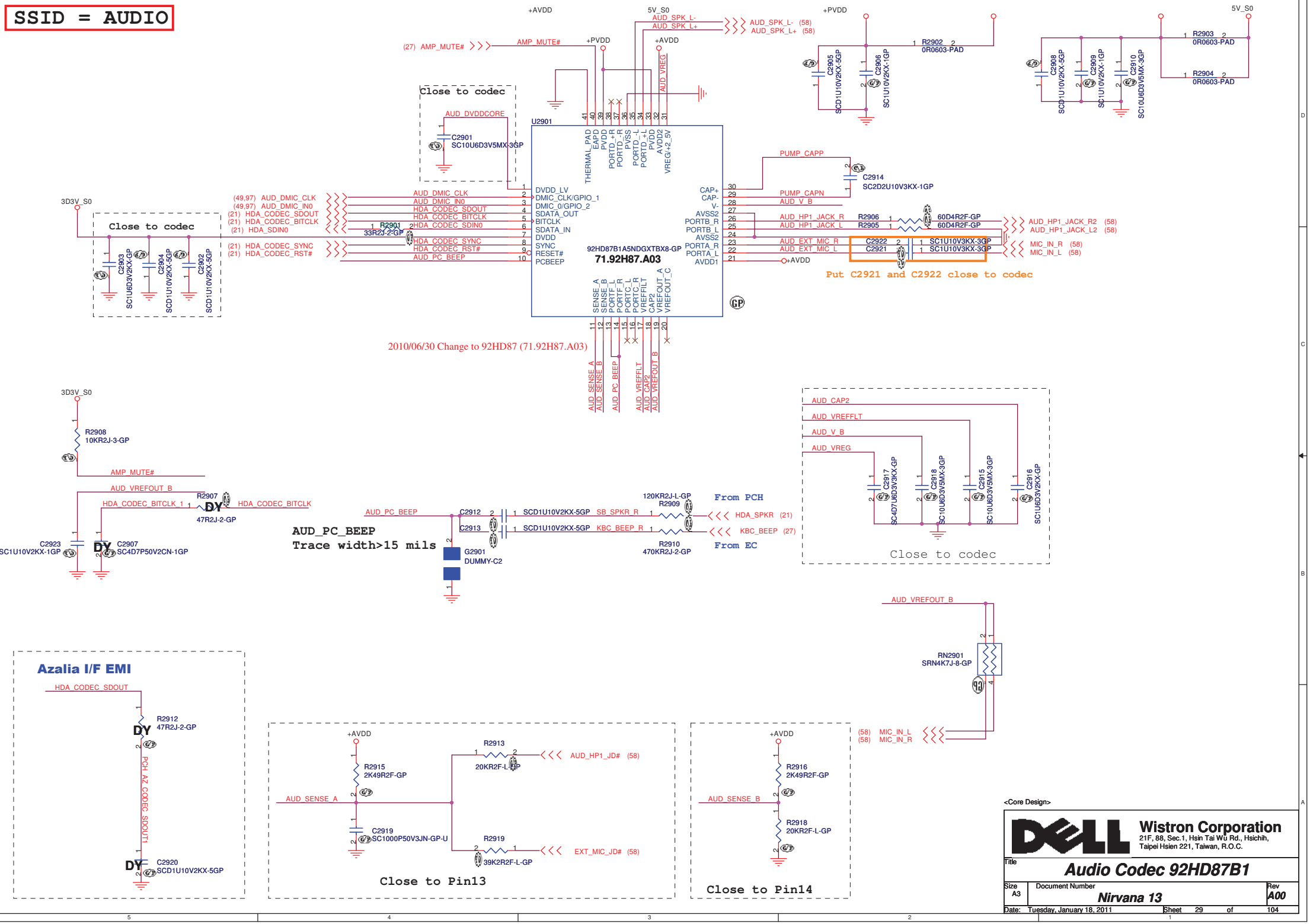
SSID = AUDIO



<Core Design>

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Title: Audio Codec 92HD87B1

Size	Document Number	Rev
A3	Nirvana 13	A00

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Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

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Title
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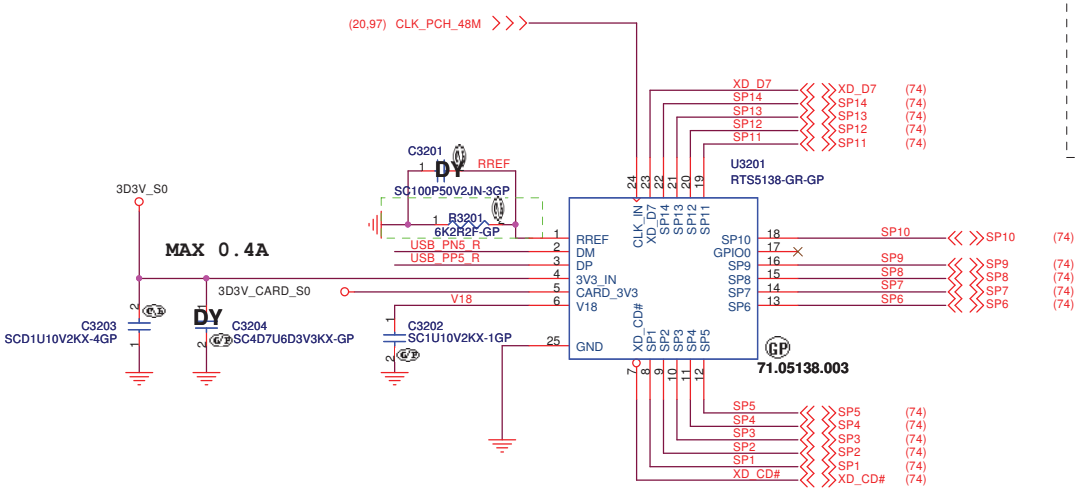
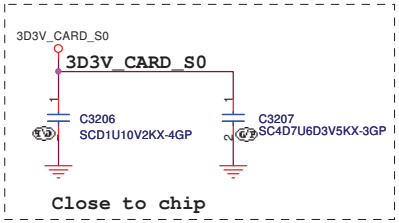
Size	Document Number	Rev
A3	*Nirvana 13*	*A00*

Date: Tuesday, January 04, 2011 Sheet 31 of 104

SSID = SDIO

48MHz clock input trace of characteristic impedance (Zo) must be 50 ±15%.



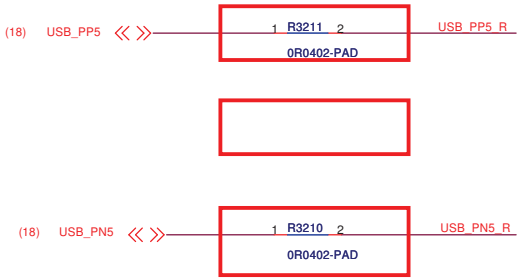


PIN	TYPE	FUNCTION	RTS5138 NET
1	SD	SD-DAT2	SP13
2	SD	SD-CD/DAT3	SP12
3	MMC_PLUS	MMC-DAT4	SP11
4	SD	SD-CMD	SP10
5	MMC_PLUS	MMC-DAT5	SP9
6	SD	SD-VSS	POWER
7	SD	SD-VDD	POWER
8	MemoryStick	MS-VSS	POWER
9	MemoryStick	MS-VCC	POWER
10	MemoryStick	MS-SCLK	SP1
11	MemoryStick	MS-DATA3	SP5
12	MemoryStick	MS-INS	SP2
13	MemoryStick	MS-DATA2	SP8
14	MemoryStick	MS-DATA0	SP9
15	MemoryStick	MS-DATA1	SP12
16	MemoryStick	MS-BS	SP14
17	MemoryStick	MS-VSS	POWER
18	SD	SD-CLK	SP8
19	MMC_PLUS	MMC-DAT6	SP7
20	SD	SD-VSS	POWER
21	MMC_PLUS	MMC-DAT7	SP5
22	SD	SD-DAT0	SP4
23	SD	SD-DAT1	SP3
24	SD	SD-COM(SW)	
25	SD	SD-CD(SW)	SP6
26	XD	XD-GND	POWER
27	XD	XD-CD	XD_CD#
28	XD	XD-R/-B	SP1
29	XD	XD-RE	SP2
30	XD	XD-CE	SP3
31	XD	XD-CLE	SP4
32	XD	XD-ALE	SP5
33	XD	XD-WE	SP6
34	XD	XD-WP	SP7
35	XD	XD-GND	POWER
36	XD	XD-D0	SP8
37	XD	XD-D1	SP9
38	XD	XD-D2	SP10
39	XD	XD-D3	SP11
40	XD	XD-D4	SP12
41	XD	XD-D5	SP13
42	XD	XD-D6	SP14
43	XD	XD-D7	XD-D7
44	XD	XD-VCC	POWER
45	SD	SD-WP(SW)	SP1

The maximum range of the PMOS output current
1. xD-Picture Card: 250mA
2. SD/MMC Card: 250mA
3. MS/MSPRO/Duo-HG: 250mA

POWER TRACE
1.RTS5138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
2.RTS5138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
3.RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum).
Keep the trace routing lengths as short as possible.
4.RTS5138: pin 1(RREF) trace fixed width is 12 mils (minimum).
5.RTS5138: pin 1(RREF) trace must far away 48MHz clock trace.
6.De-coupling and Bulk capacitor should place near to RT5138 chip and Combo Socket.
7.It is recommended that use of ferrites bead on power trace.
8.Via size: Pad>=32 mils, Finished hole>=16 mils.

The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance (Zdiff) is 90Ω± 10%



20101227 A00:
Change R3210,R3211 to 0R 0402 pad.
20100104 A00:
Remove TR3201.

<Core Design>

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Title: **Card Reader RTS5138**

Size	Document Number	Rev
A3	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 32 of 104

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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A3	*Nirvana 13*	*A00*

Date: Tuesday, January 04, 2011 Sheet 33 of 104

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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A3	***Nirvana 13***	***A00***

Date: Tuesday, January 04, 2011 Sheet 34 of 104

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<Core Design>

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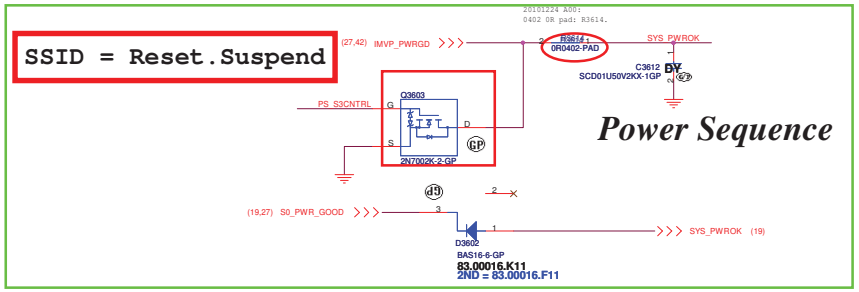
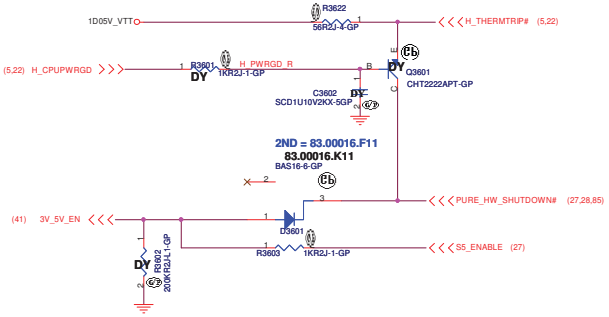
Title: *Reserved*		
Size: A3	Document Number: *Nirvana 13*	Rev: *A00*
Date: Tuesday, January 04, 2011	Sheet 35 of 104	

SSID = Reset.Suspend

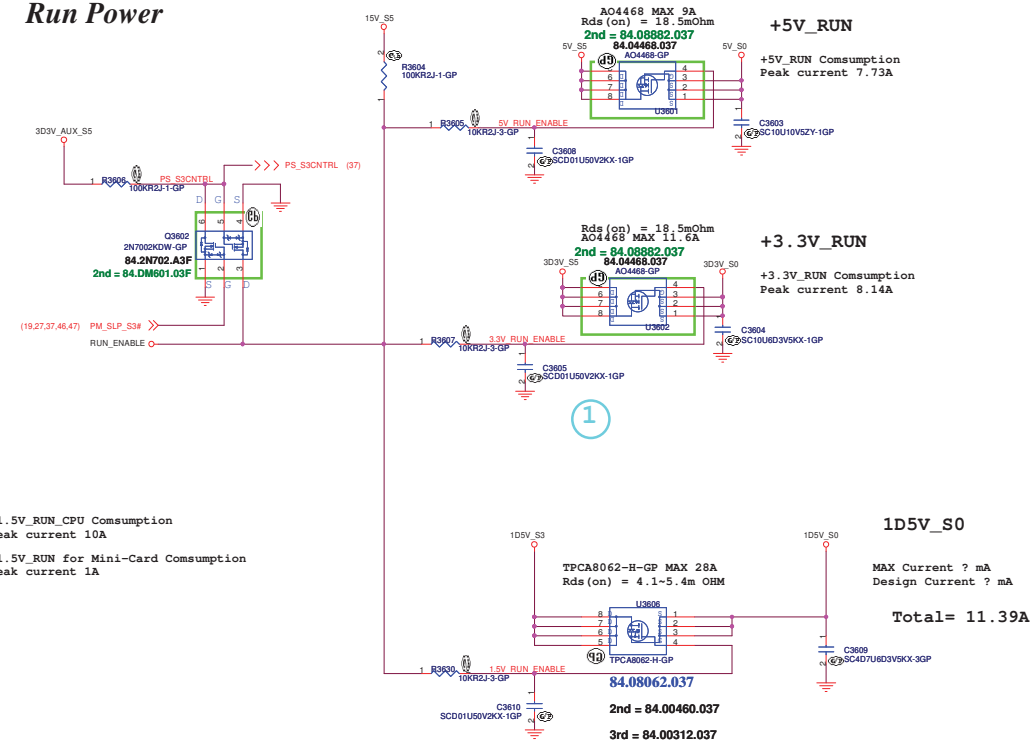
Power Sequence





SSID = Reset.Suspend

Run Power



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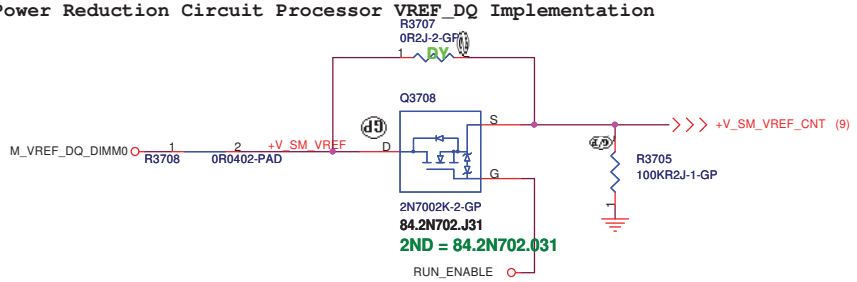
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

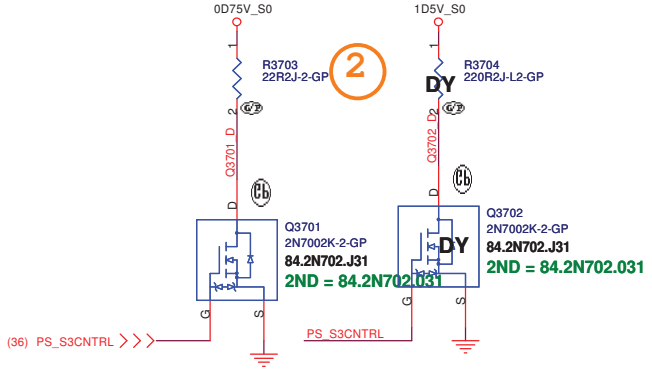
Size: A2 | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 18, 2011 | Sheet 36 of 104

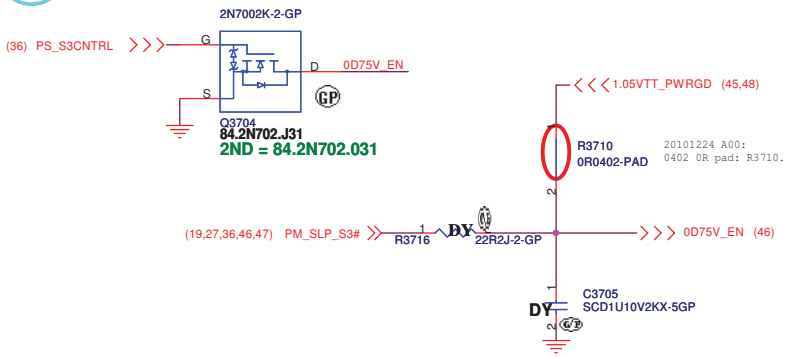
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



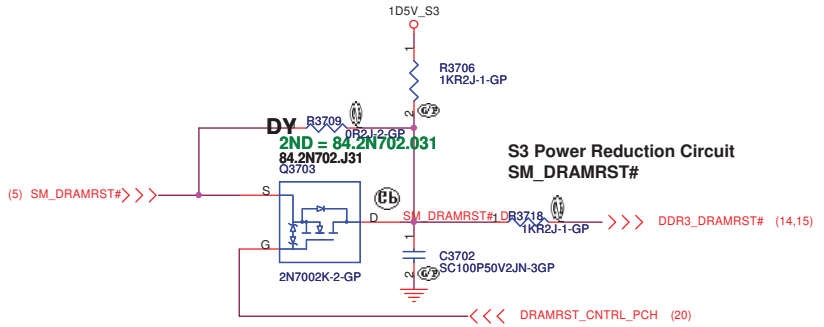
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

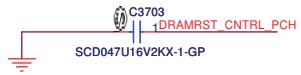


5 S3 Power Reduction

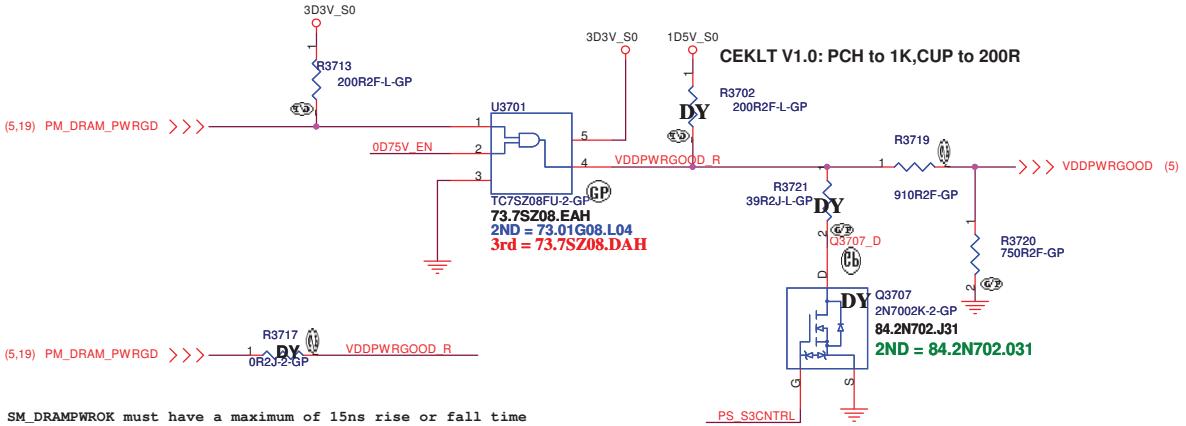


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK





Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: S3 Power Reduction

Size	Document Number	Rev
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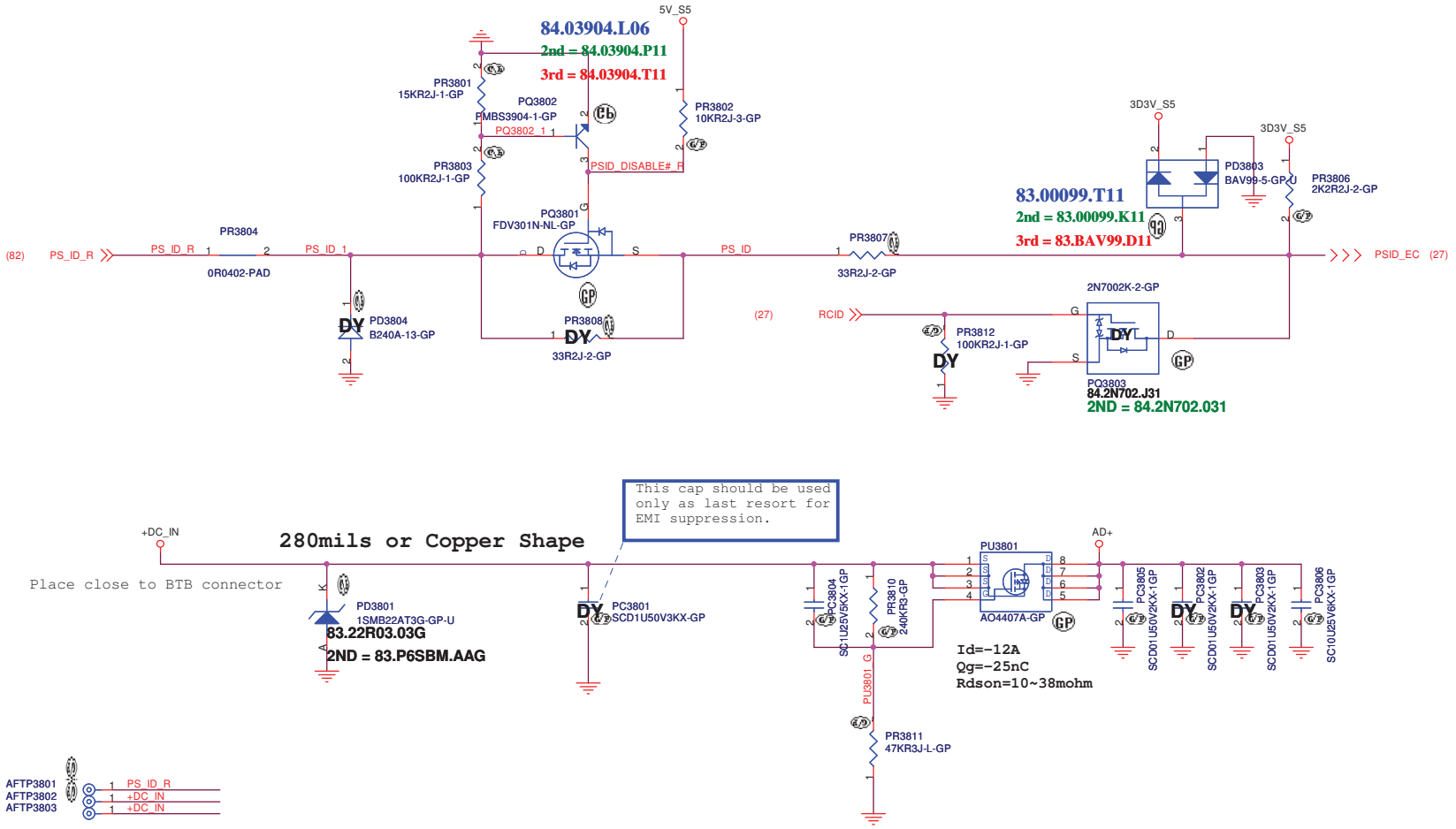

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN Jack	
Size: A3	Document Number: Nirvana 13	Rev: A00
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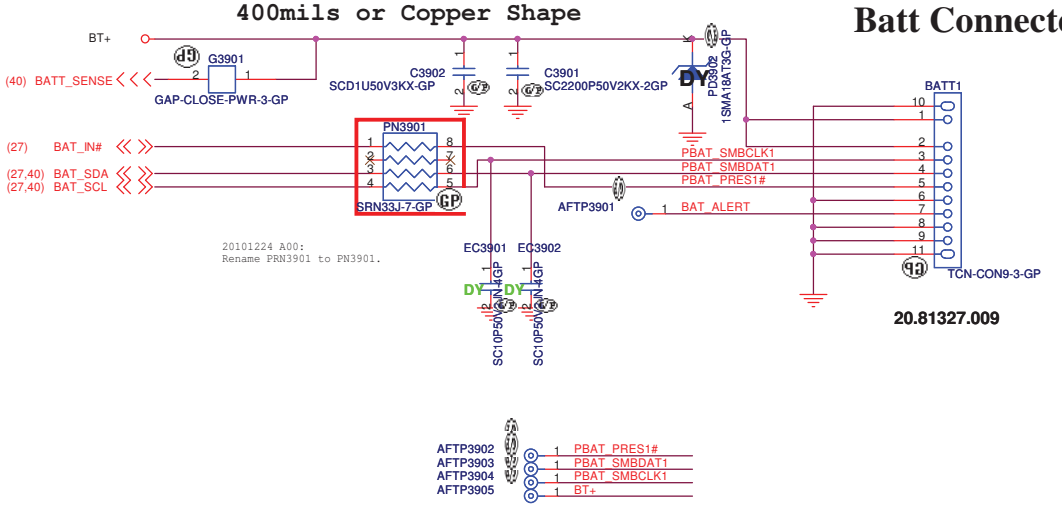
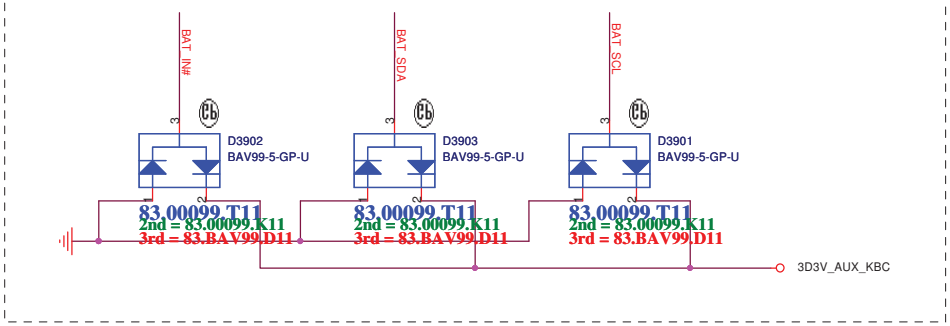
Batt Connecter



For actual location, need to be swap all pin

Placement: Close to Batt Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BATT CONN		
Size: A3	Document Number: Nirvana 13	Rev: A00
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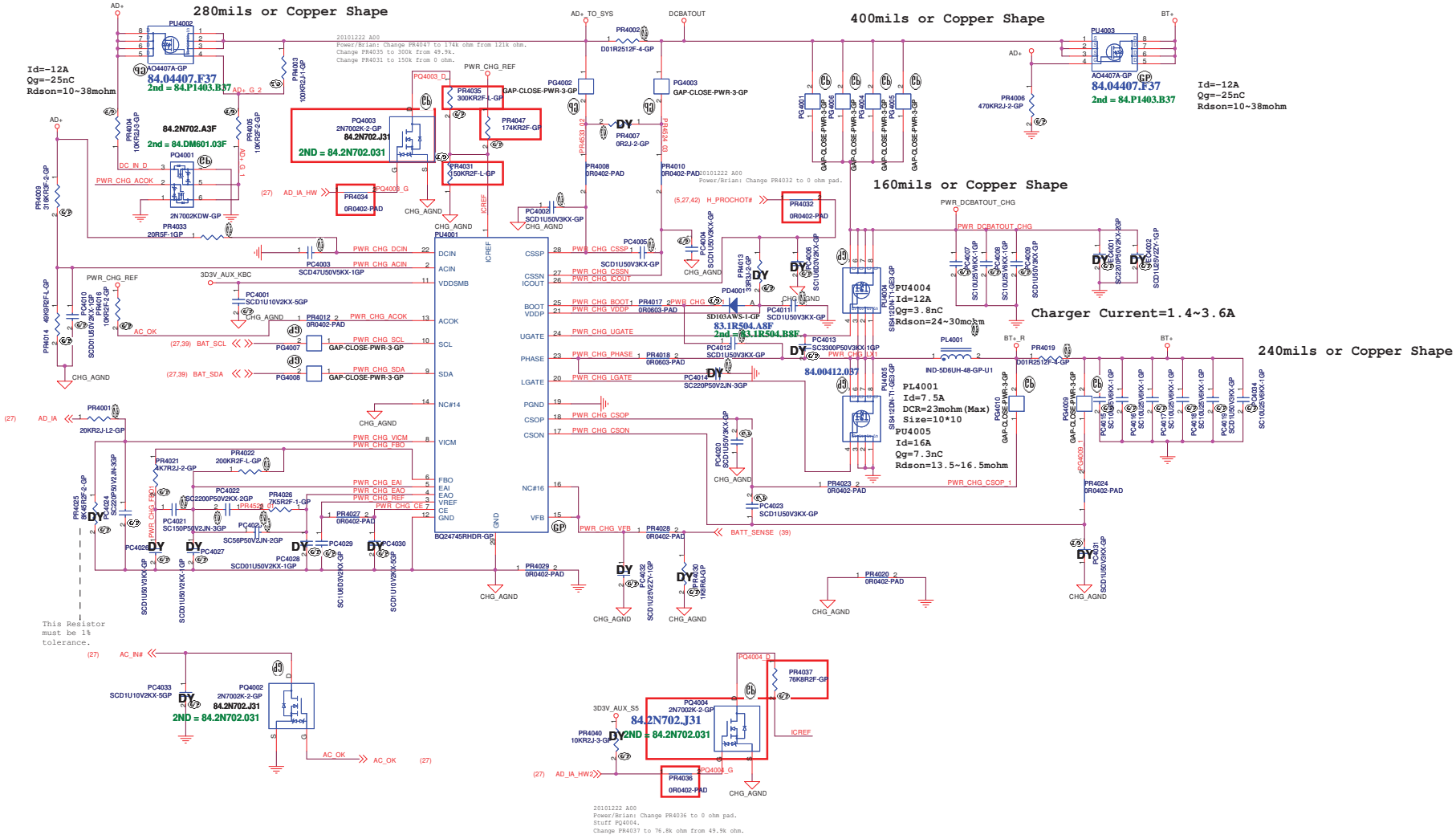
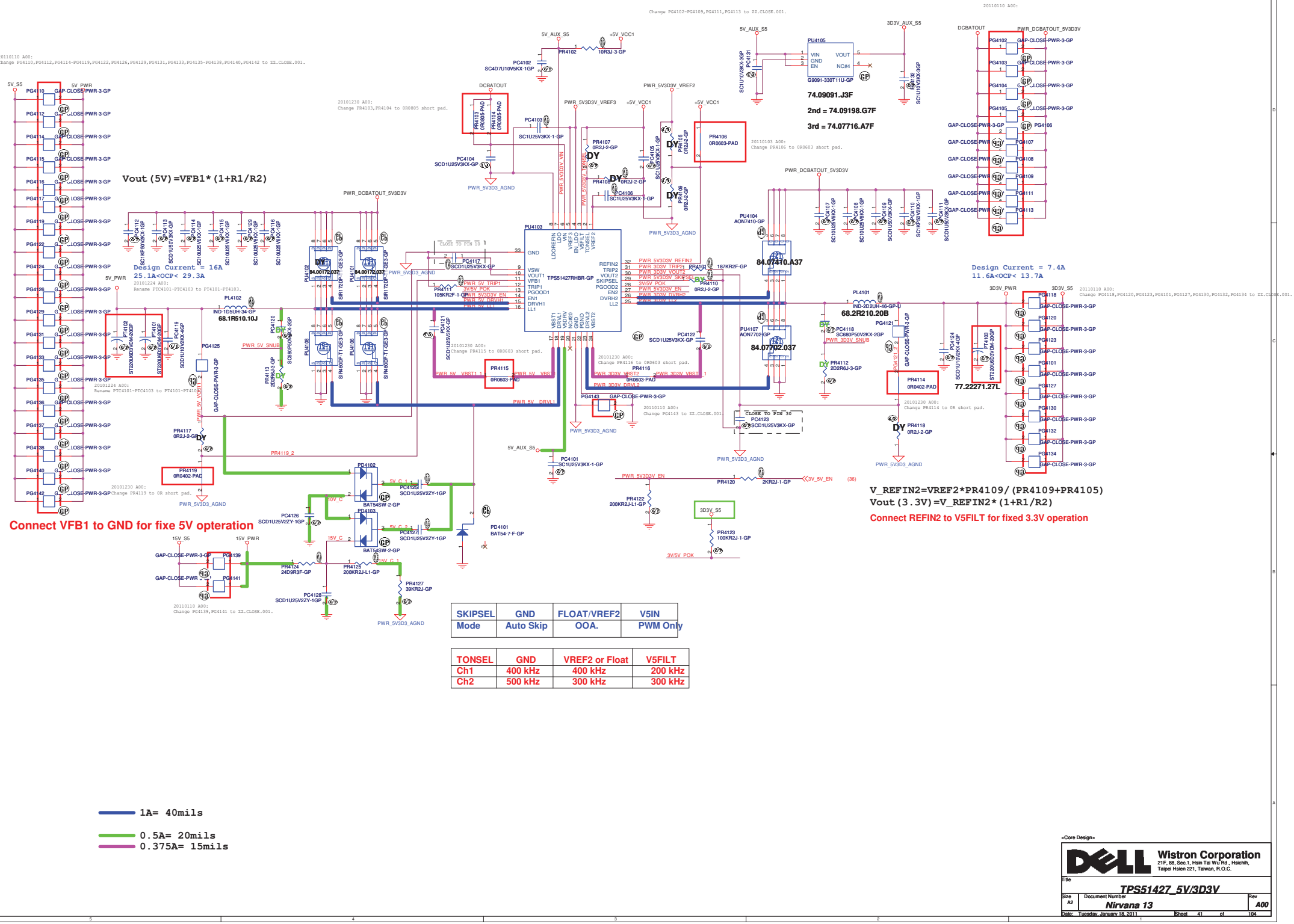
SSID = Charger



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CHARGER BQ24745		
Size	Document Number	Rev
	Nirvana 13	A00
Date: Tuesday, January 18, 2011	Sheet 40 of 104	



SKIPSEL	GND	FLOAT/VREF2	V5IN
Mode	Auto Skip	OOA.	PWM Only

TONSEL	GND	VREF2 or Float	V5FILT
Ch1	400 kHz	400 kHz	200 kHz
Ch2	500 kHz	300 kHz	300 kHz

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51427_5V/3D3V

Size: A2 | Document Number: Nirvana 13 | Rev: A00

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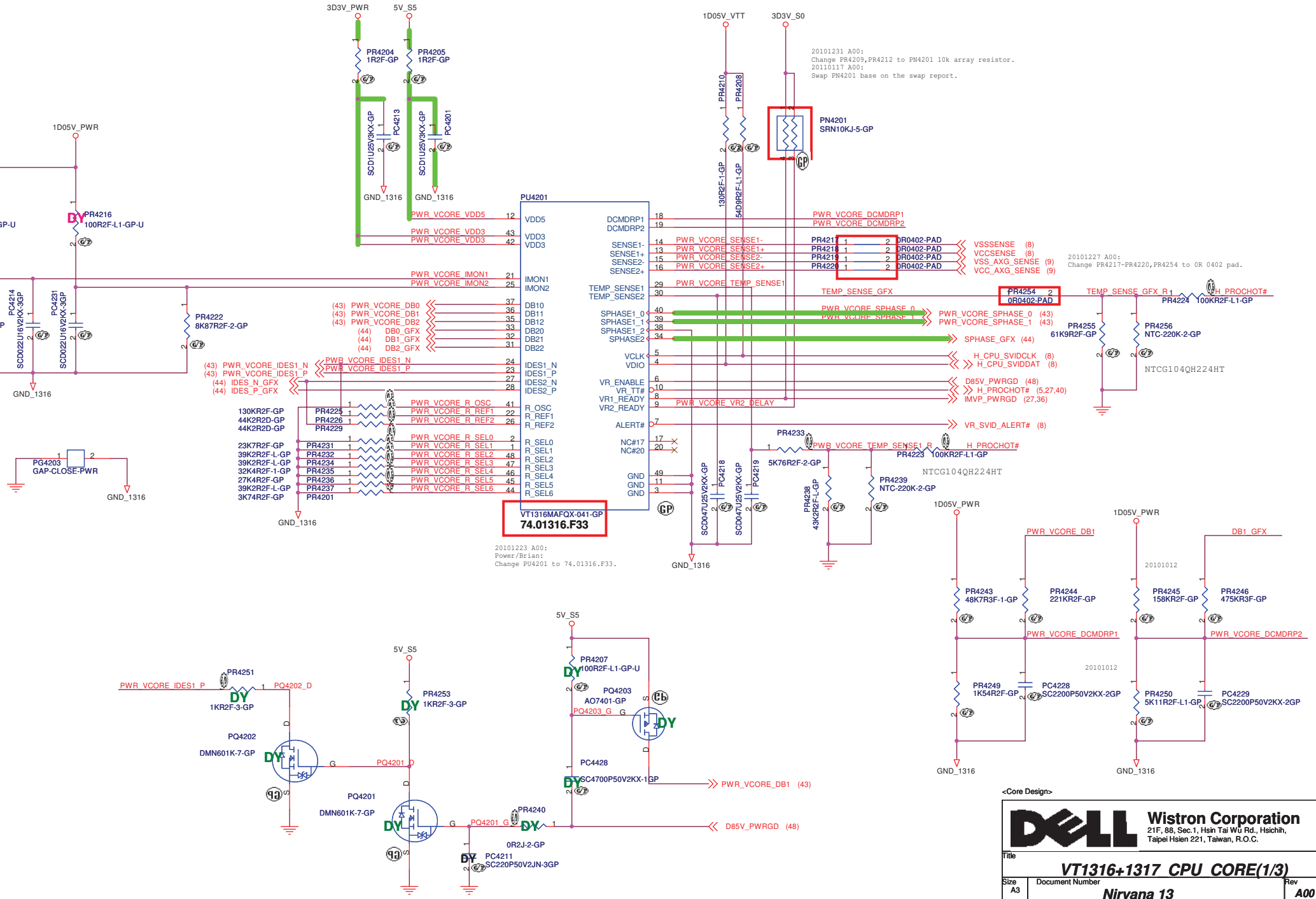
SSID = CPU.Regulator



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317_CPU_CORE(1/3)

Size	Document Number	Rev
A3	Nirvana 13	A00

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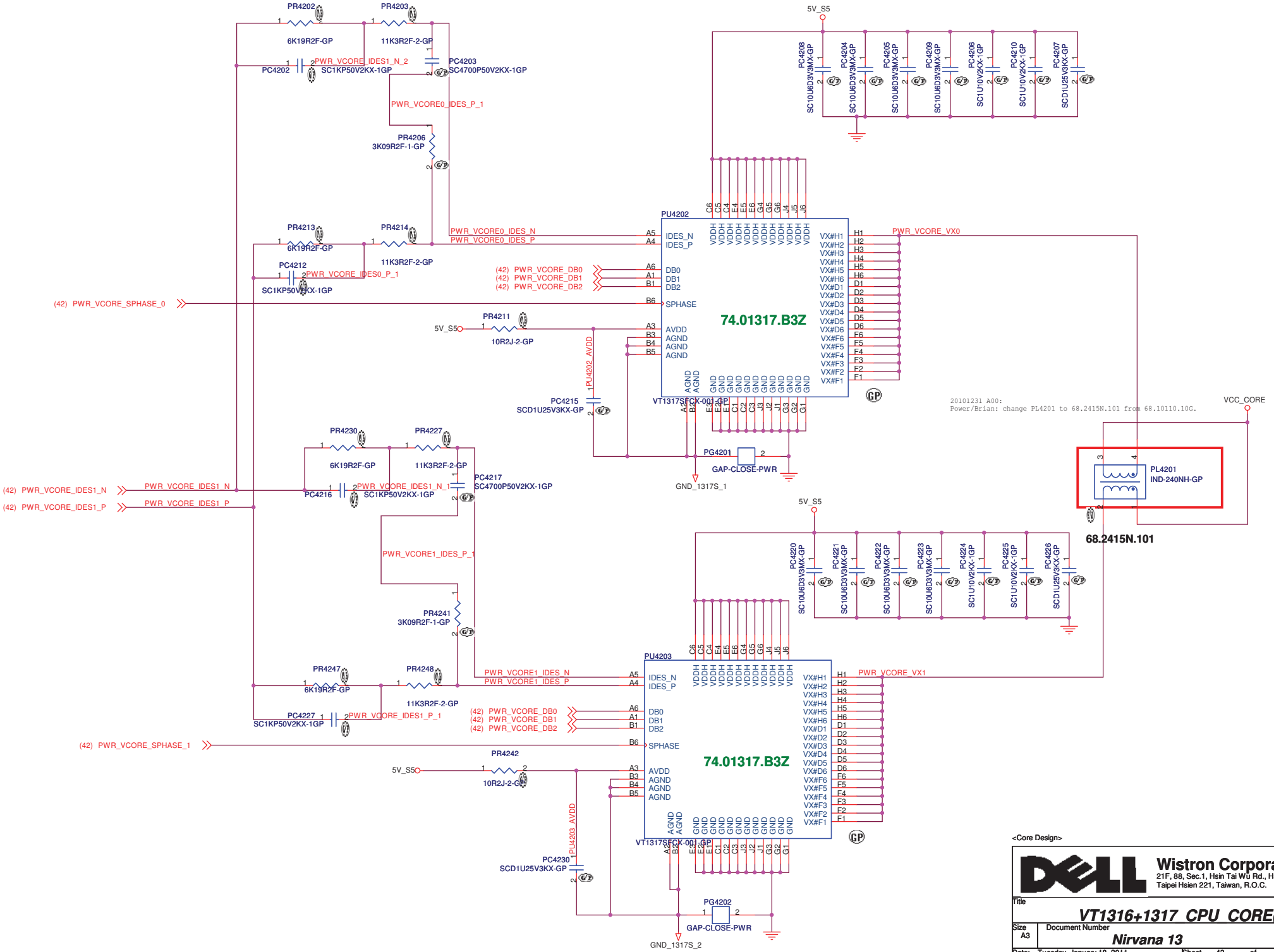
PR4202
PR4203
6K19R2F-GP
11K3R2F-2-GP
PC4202
SC1KP50V2KX-1GP
PWR_VCORE_IDES1_N_2
PC4203
SC4700P50V2KX-1GP
PWR_VCORE0_IDES_P_1
PR4206
3K09R2F-1-GP
5V_S5
PC4208
PC4204
PC4205
PC4209
PC4206
PC4210
PC4207
SC10U6D3V3MX-GP
SC1U10V2KX-1GP
SCD1U25V3KX-GP
PU4202
PR4213
PR4214
PC4212
PWR_VCORE0_IDES_N
PWR_VCORE0_IDES_P
PWR_VCORE_IDES0_P_1
(42) PWR_VCORE_DB0
(42) PWR_VCORE_DB1
(42) PWR_VCORE_DB2
(42) PWR_VCORE_SPHASE_0
IDES_N
IDES_P
DB0
DB1
DB2
SPHASE
AVDD
AGND
VDDH
GND
VX#H1
VX#H2
VX#H3
VX#H4
VX#H5
VX#H6
VX#D1
VX#D2
VX#D3
VX#D4
VX#D5
VX#D6
VX#F6
VX#F5
VX#F4
VX#F3
VX#F2
VX#F1
PWR_VCORE_VX0
74.01317.B3Z
VT1317SFCX-001-GP
PR4211
10R2J-2-GP
PU4202_AVDD
PC4215
SCD1U25V3KX-GP
PG4201
GAP-CLOSE-PWR
GND_1317S_1
20101231 A00:
Power/Brian: change PL4201 to 68.2415N.101 from 68.10110.10G.
VCC_CORE
PL4201
IND-240NH-GP
68.2415N.101
PR4230
PR4227
6K19R2F-GP
11K3R2F-2-GP
PC4216
SC1KP50V2KX-1GP
PC4217
SC4700P50V2KX-1GP
(42) PWR_VCORE_IDES1_N
(42) PWR_VCORE_IDES1_P
PWR_VCORE_IDES1_N
PWR_VCORE_IDES1_P
PWR_VCORE_IDES1_N_1
PWR_VCORE1_IDES_P_1
PR4241
3K09R2F-1-GP
PC4220
PC4221
PC4222
PC4223
PC4224
PC4225
PC4226
PU4203
PR4247
PR4248
PC4227
PWR_VCORE1_IDES_N
PWR_VCORE1_IDES_P
PWR_VCORE_IDES1_P_1
(42) PWR_VCORE_SPHASE_1
PWR_VCORE_VX1
PR4242
PU4203_AVDD
PC4230
PG4202
GAP-CLOSE-PWR
GND_1317S_2
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VT1316+1317_CPU_CORE(2/3)
Size
A3
Document Number
Nirvana 13
Rev
A00
Date: Tuesday, January 18, 2011
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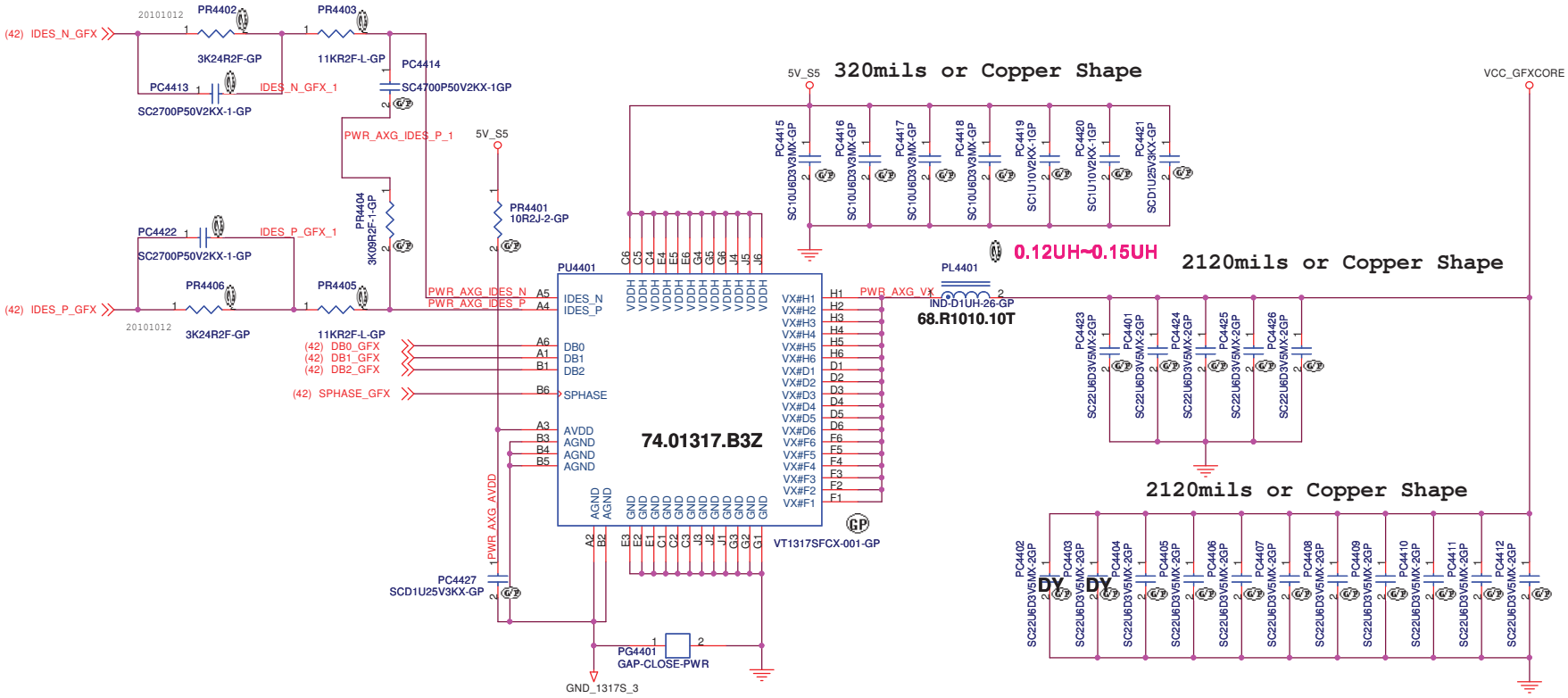

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317 AXG CORE(3/3)

Size	Document Number	Rev
A3	Nirvana 13	A00

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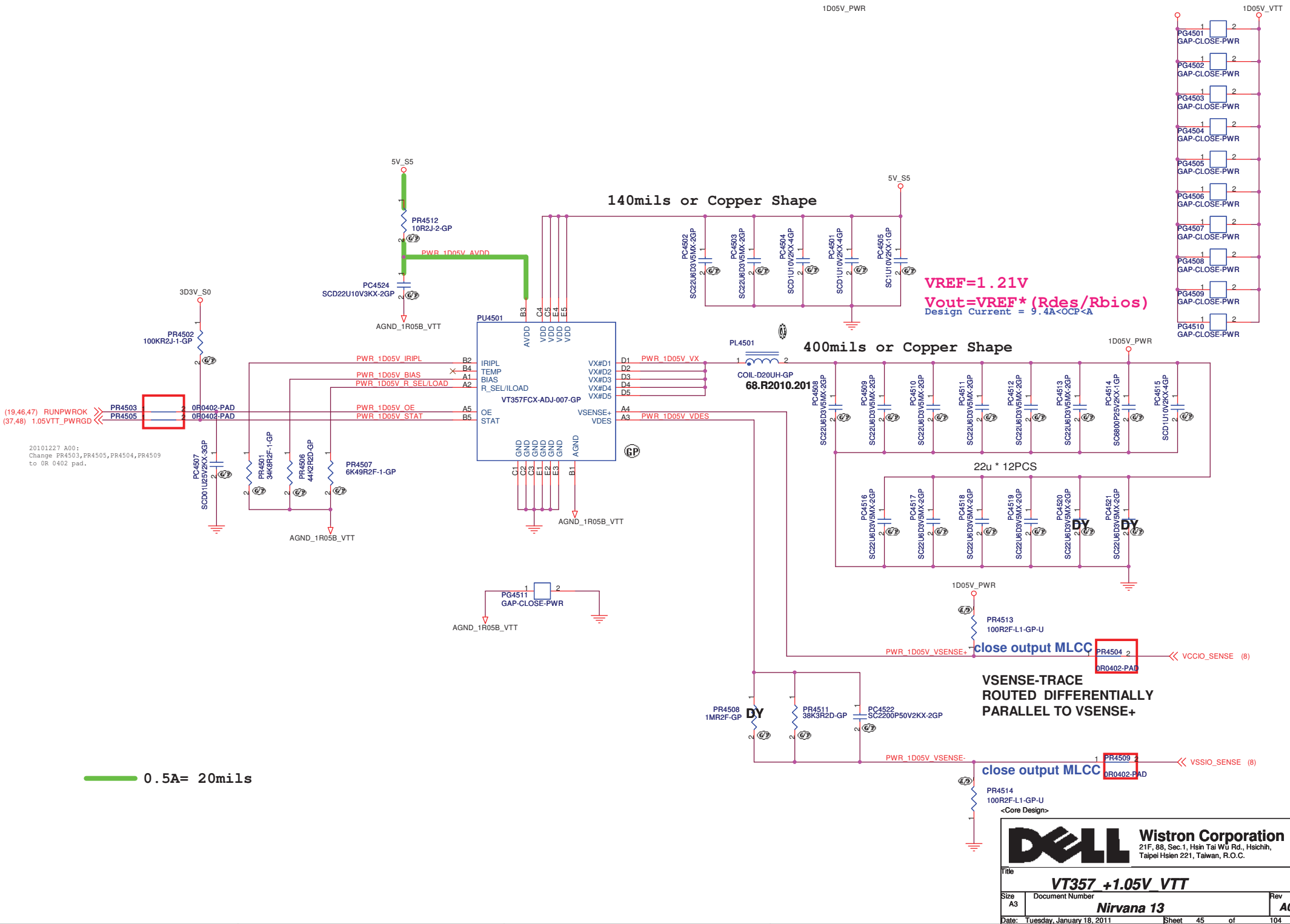
1D05V_PWR
1D05V_VTT
PG4501 GAP-CLOSE-PWR
PG4502 GAP-CLOSE-PWR
PG4503 GAP-CLOSE-PWR
PG4504 GAP-CLOSE-PWR
PG4505 GAP-CLOSE-PWR
PG4506 GAP-CLOSE-PWR
PG4507 GAP-CLOSE-PWR
PG4508 GAP-CLOSE-PWR
PG4509 GAP-CLOSE-PWR
PG4510 GAP-CLOSE-PWR
5V_S5
PR4512 10R2J-2-GP
PWR_1D05V_AVDD
PC4524 SCD22U10V3KX-2GP
AGND_1R05B_VTT
140mils or Copper Shape
PC4502 SC22U6D3V5MX-2GP
PC4503 SC22U6D3V5MX-2GP
PC4504 SCD1U10V2KX-4GP
PC4501 SCD1U10V2KX-4GP
PC4505 SC1U10V2KX-1GP
VREF=1.21V
Vout=VREF*(Rdes/Rbios)
Design Current = 9.4A<OCP<A
3D3V_S0
PR4502 100KR2J-1-GP
PU4501
PWR_1D05V_IRIPL
PWR_1D05V_BIAS
PWR_1D05V_R_SEL/LOAD
PWR_1D05V_OE
PWR_1D05V_STAT
IRIPL
TEMP
BIAS
R_SEL/ILOAD
OE
STAT
VT357FCX-ADJ-007-GP
VX#D1
VX#D2
VX#D3
VX#D4
VX#D5
VSENSE+
VDES
PWR_1D05V_VX
PWR_1D05V_VDES
PL4501
COIL-D20UH-GP
68.R2010.201
400mils or Copper Shape
PC4508 SC22U6D3V5MX-2GP
PC4509 SC22U6D3V5MX-2GP
PC4510 SC22U6D3V5MX-2GP
PC4511 SC22U6D3V5MX-2GP
PC4512 SC22U6D3V5MX-2GP
PC4513 SC22U6D3V5MX-2GP
PC4514 SC6800P25V2KX-1GP
PC4515 SCD1U10V2KX-4GP
22u * 12PCS
PC4516 SC22U6D3V5MX-2GP
PC4517 SC22U6D3V5MX-2GP
PC4518 SC22U6D3V5MX-2GP
PC4519 SC22U6D3V5MX-2GP
PC4520 SC22U6D3V5MX-2GP
PC4521 SC22U6D3V5MX-2GP
DY
(19,46,47) RUNPWROK
(37,48) 1.05VTT_PWRGD
PR4503 0R0402-PAD
PR4505 0R0402-PAD
20101227 A00:
Change PR4503,PR4505,PR4504,PR4509
to 0R 0402 pad.
PC4507 SCD01U25V2KX-3GP
PR4501 34K8R2F-1-GP
PR4506 44K2R2D-GP
PR4507 6K49R2F-1-GP
PG4511 GAP-CLOSE-PWR
PR4513 100R2F-L1-GP-U
close output MLCC
PWR_1D05V_VSENSE+
PR4504 0R0402-PAD
VCCIO_SENSE (8)
VSENSE-TRACE
ROUTED DIFFERENTIALLY
PARALLEL TO VSENSE+
PR4508 1MR2F-GP
PR4511 38K3R2D-GP
PC4522 SC2200P50V2KX-2GP
PWR_1D05V_VSENSE-
PR4509 0R0402-PAD
VSSIO_SENSE (8)
PR4514 100R2F-L1-GP-U
<Core Design>
0.5A= 20mils
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VT357_+1.05V_VTT
Size A3
Document Number
Nirvana 13
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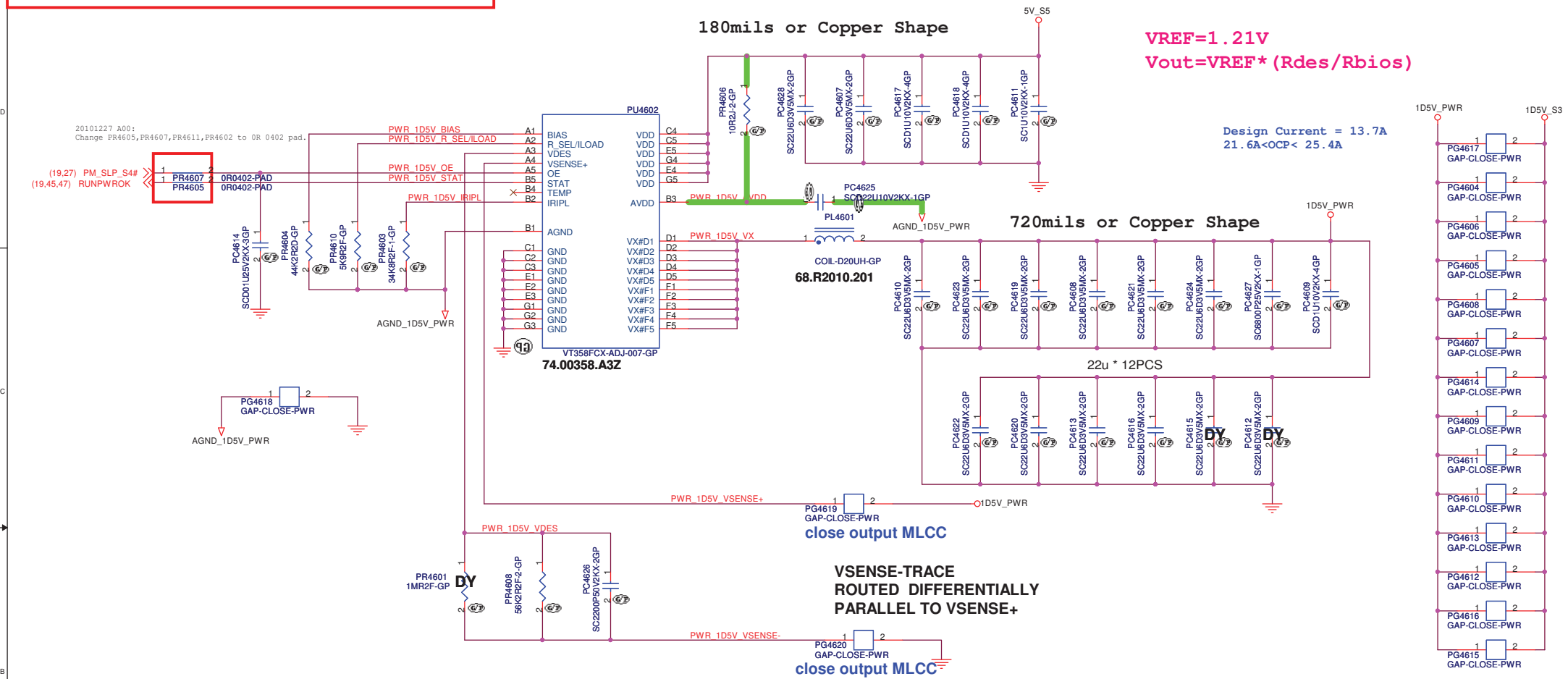
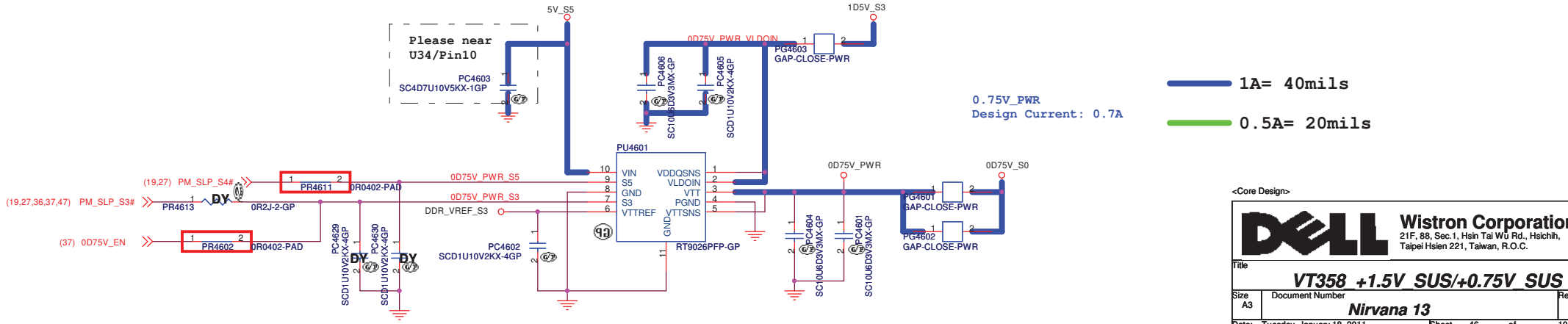
SSID = PWR.Plane.Regulator_1p5v0p75v



RT9026 for 0D75V_S0



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT358_+1.5V_SUS/+0.75V_SUS

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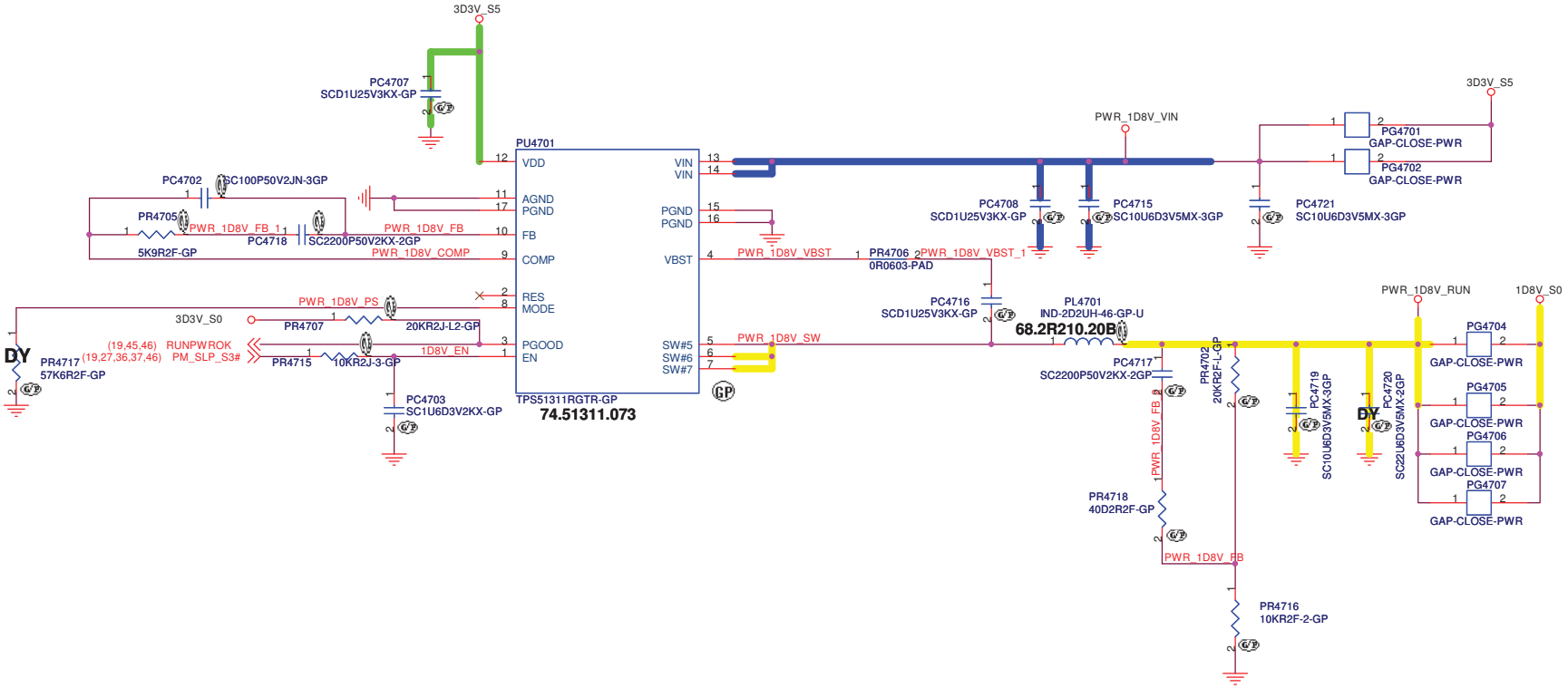
SSID = PWR.Plane.Regulator_1p8v

1A= 40mils
1.5A= 60mils
0.5A= 20mils



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51311 +1.8V RUN

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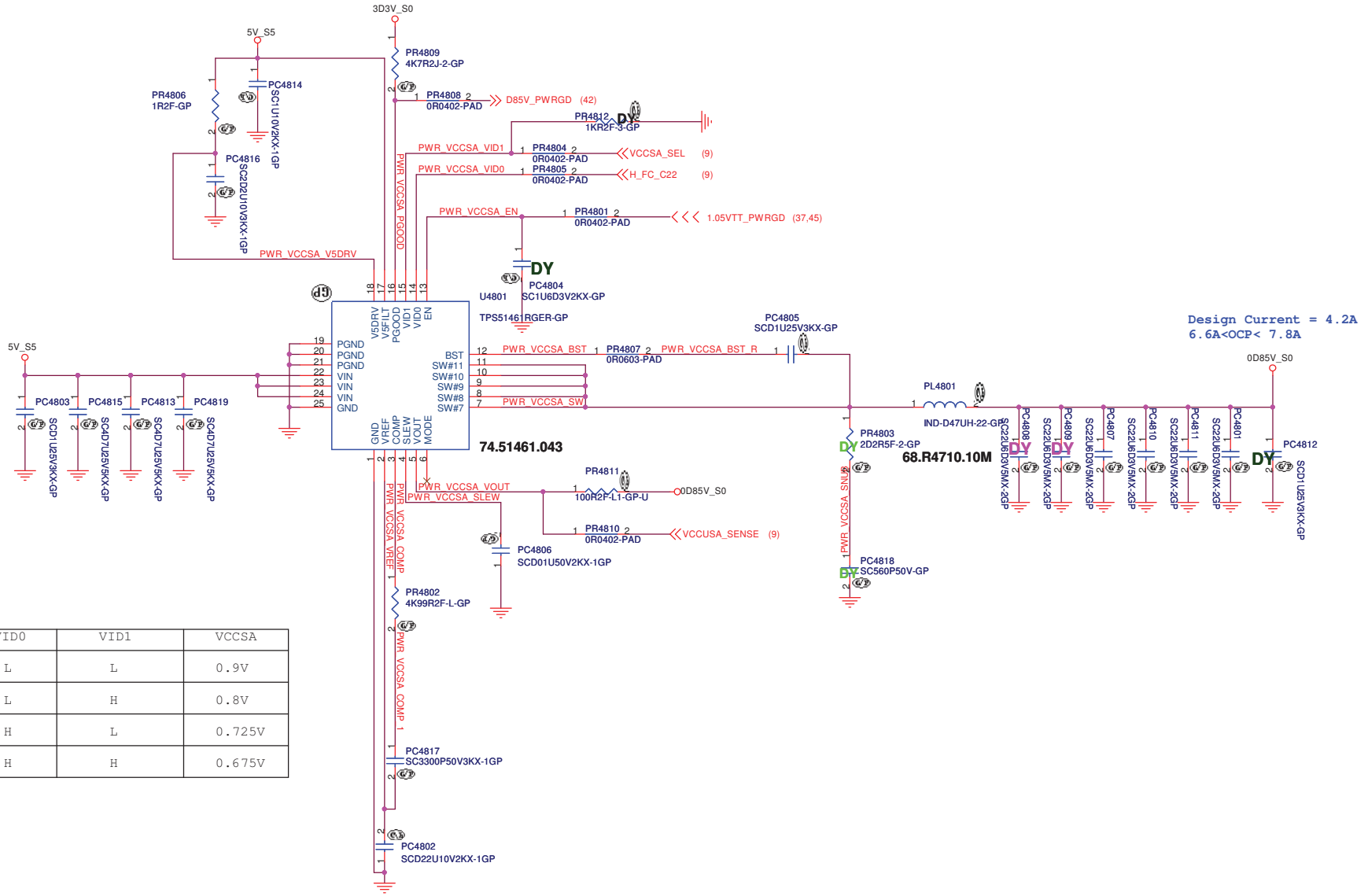
TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5916_VCCSA	
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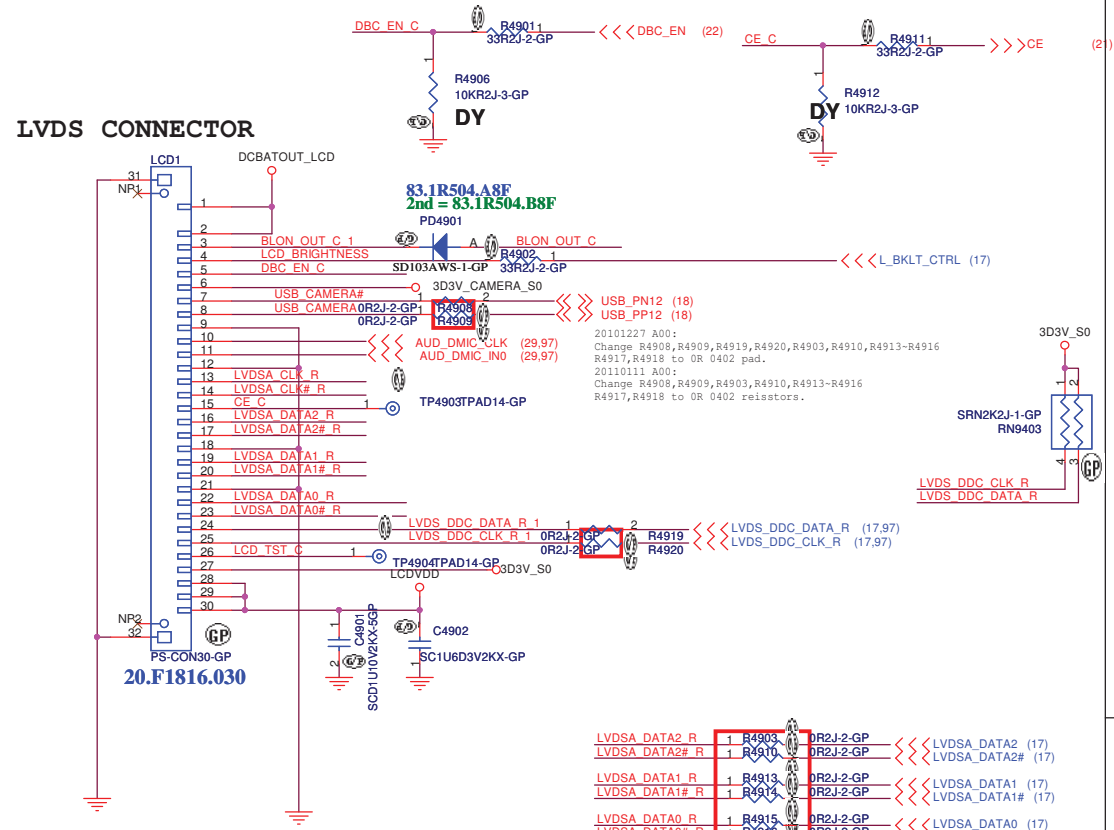
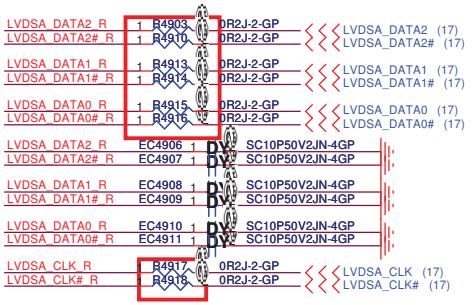
SSID = VIDEO

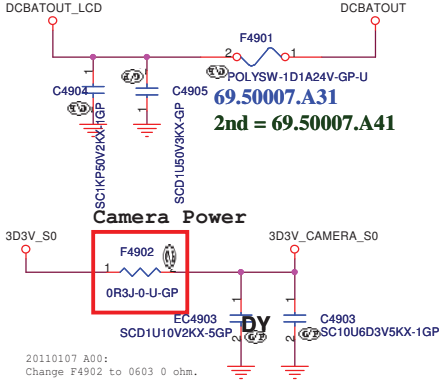
LVDS CONNECTOR



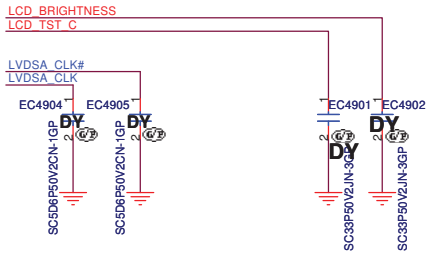


CAMERA and DIGITAL MIC PIN DEFINE!

Pin No.	Name	Pin Type	Function Description
1	Diag_Loop	PWD	Cable Connection Detection
2	D+	Data Pin	USB Data transmission
3	D-	Data Pin	USB Data transmission
4	USB+3.3V	Power Pin	Power Supply
5	DMIC_CLK	Data Pin	Digital MIC CLOCK
6	DMIC-GND	GND	Digital MIC GND
7	DMIC_DATA	Data Pin	Digital MIC DATA
8	GND	GND	System Ground

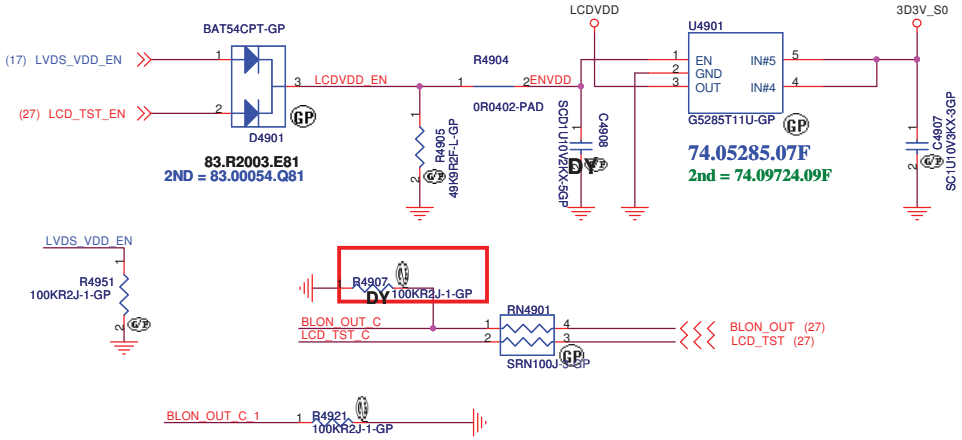


For EMI request
Close to LVDS connector



SSID = VIDEO

LCD POWER for ROSA

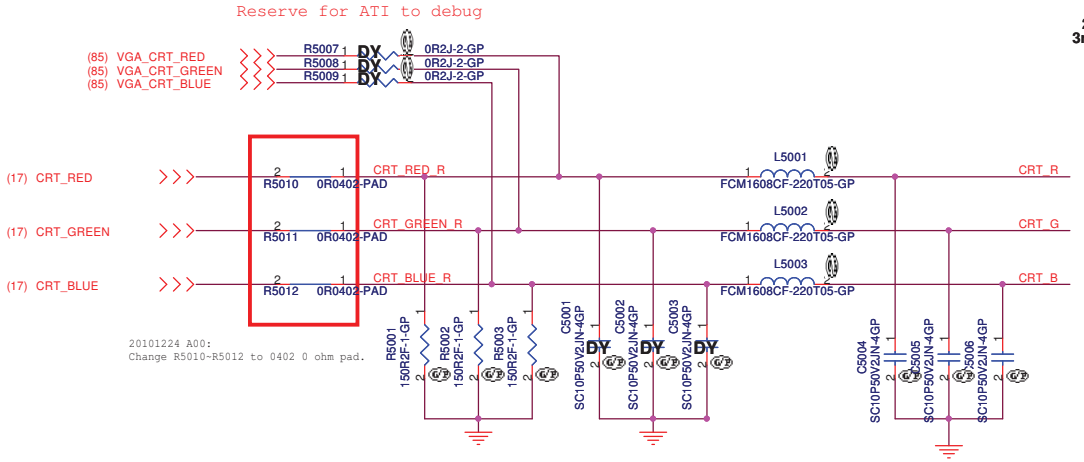


20100104 A00:
Remove TR4902.

<Core Design>

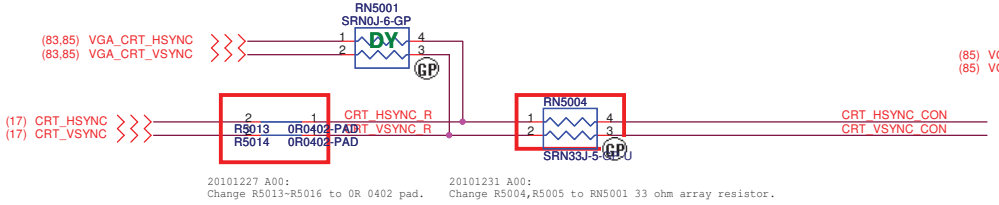
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

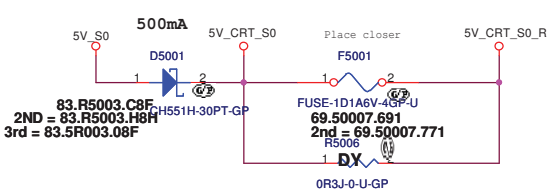
Title	LCD/Inverter Connector	
Size A3	Document Number: Nirvana 13	Rev: A00
Date: Tuesday, January 18, 2011	Sheet 49 of 104	

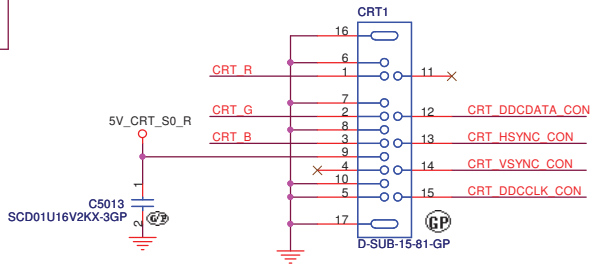


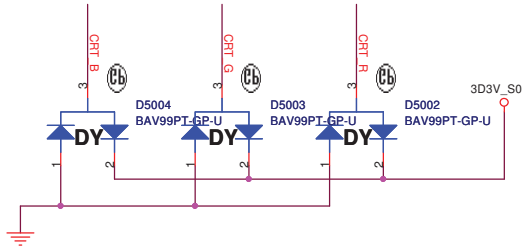
Reduce layout branch trace.
Keep reserved component near main signal

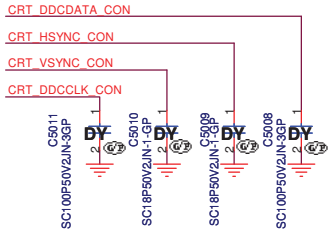
CRT Hsync & Vsync level shift



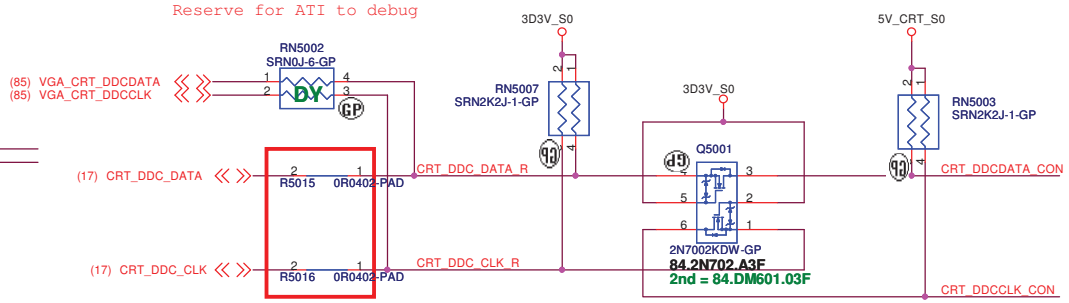








CRT DDCDATA & DDCCLK level shift



<Core Design>

Wistron Corporation
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Title: CRT Connector

Size	Document Number	Rev
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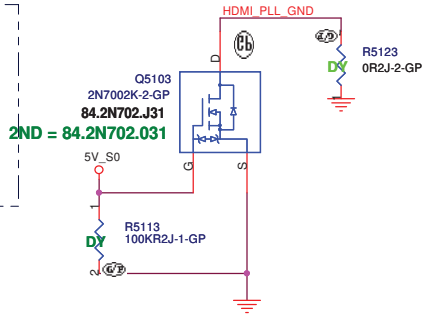
Date: Tuesday, January 18, 2011 Sheet 50 of 104

SSID = VIDEO

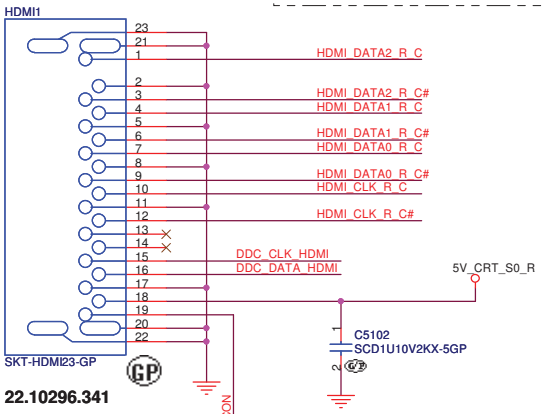
HDMI Level Shifter & CONNECTOR

Removed LEVEL SHIFTER base on DELL feedback spec.
(No support 220MHZ deep color mode, so can be removed
HDMI LEVEL SHIFTER circuit.

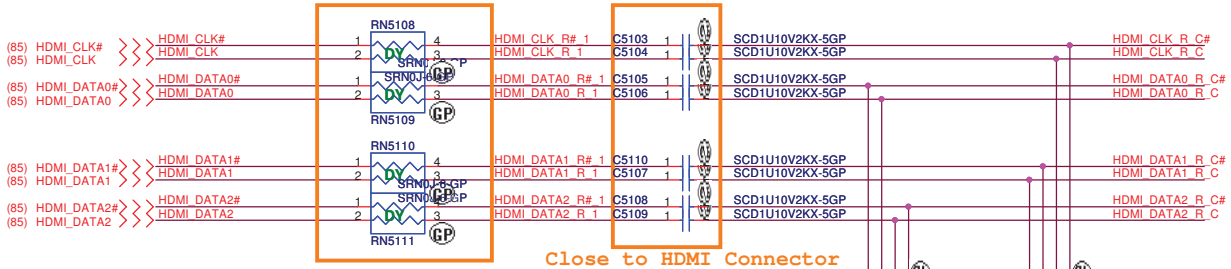


HDMI CONN

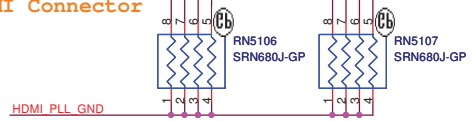
Removed HDMI_IN# CIRCUIT
connect to KBC GPIO.



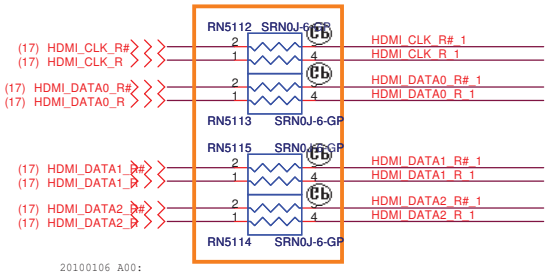
Close to GPU



Close to HDMI Connector

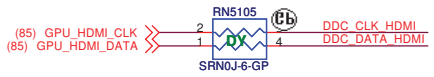


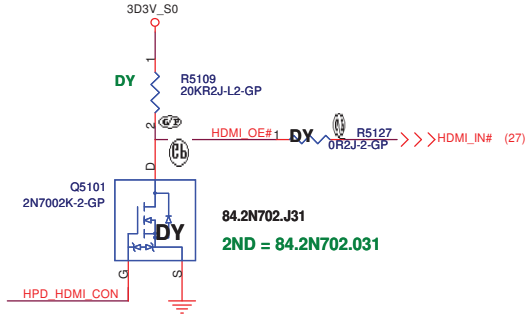
Close to PCH



20100106 A00:
Remove RN5112~RN5115.
20110111 A00:
Change RN5112~RN5115 to 0R array resistors.

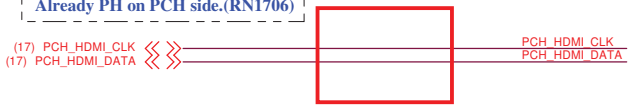
ATI GPU has 5V Tolerance

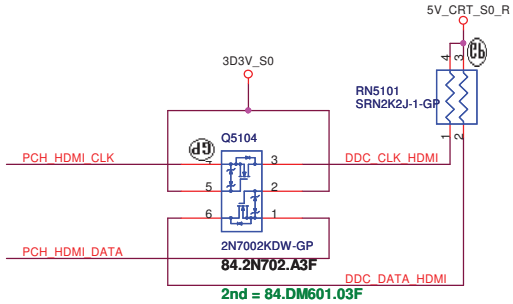


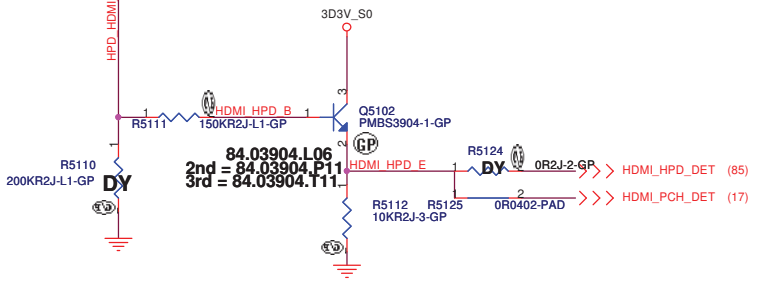


20101224 A00:
Change RN5117,RN5112~RN5115 to 0402 0 ohm pad.
20110111 A00:
Change RN5117 to 0 ohm resistor.
20110118 A00:
Remove RN5117 for PCH_HDMI_CLK and PCH_HDMI_DATA.

Already PH on PCH side.(RN1706)







Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

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Title: HDMI Level Shifter/Connector
Size: A3 | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 51 of 104

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<Core Design>

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Title

Reserved

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<Core Design>

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Title: LVDS Switch

Size: A3 | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 53 of 104

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<Core Design>

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Title: *Reserved*

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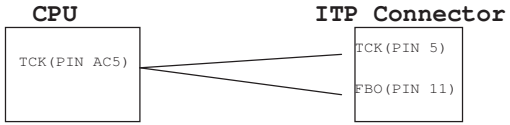
Date: Tuesday, January 04, 2011 Sheet 54 of 104

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP

Size: A3 | Document Number: Nirvana 13 | Rev: A00

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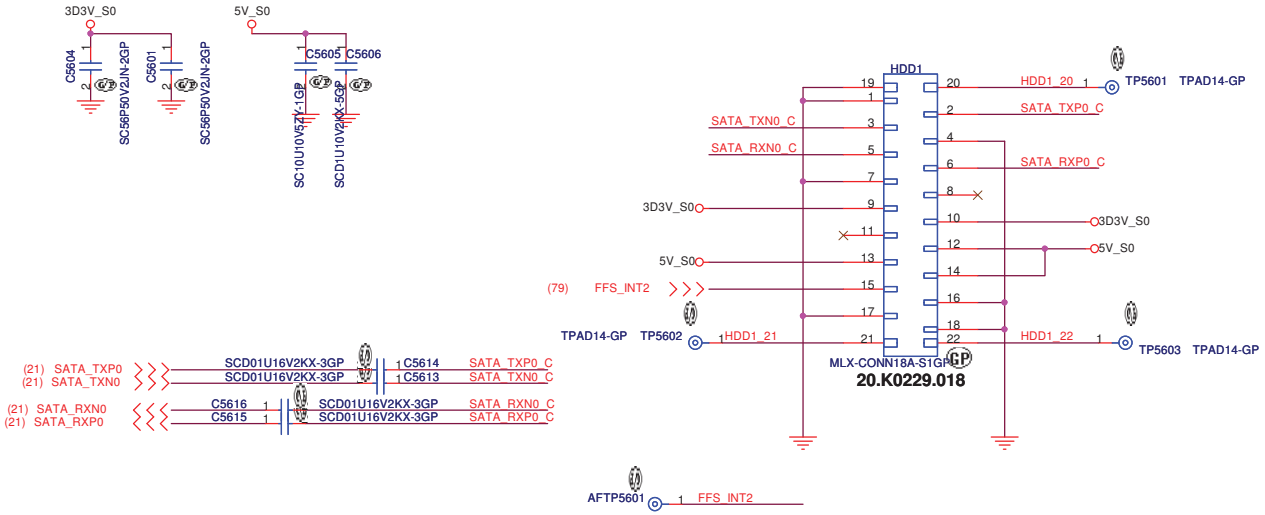
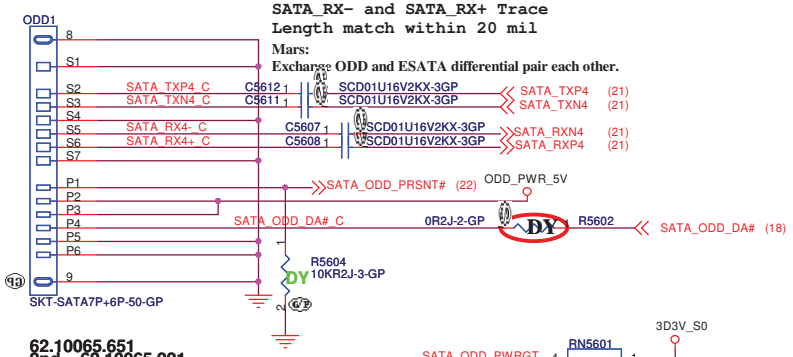
SSID = SATA

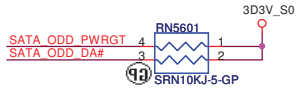
SATA HDD Connector



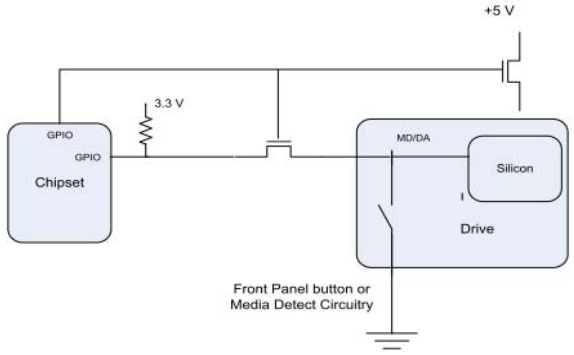
ODD Connector



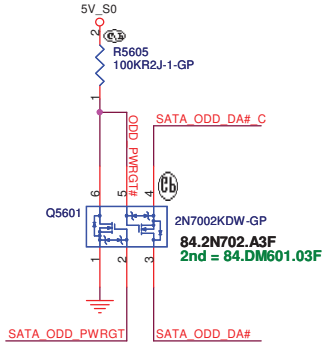
62.10065.651
2nd = 62.10065.221



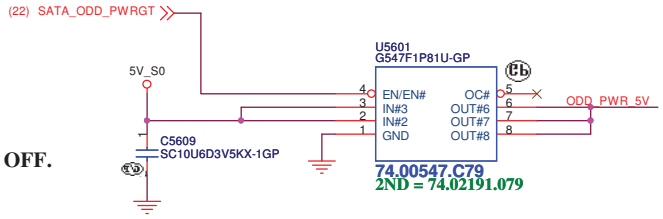
SUPPORT ZERO SATA ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



SATA Zero Power ODD



Current limit
Active High
typ =>2A

<Core Design>

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Title: HDD/ODD

Size	Document Number	Rev
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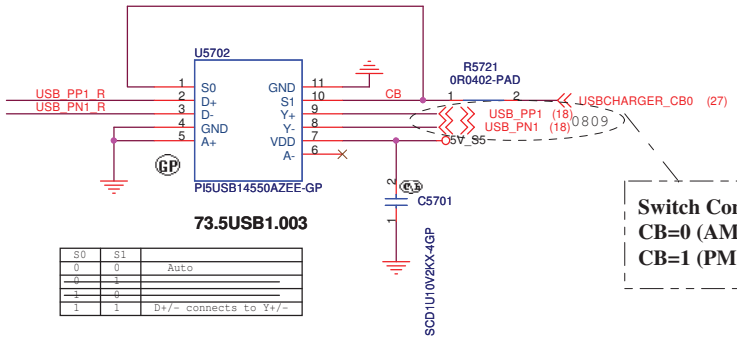
SSID = ESATA

USB CHARGER

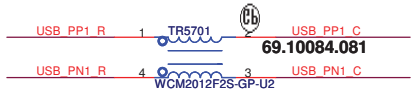


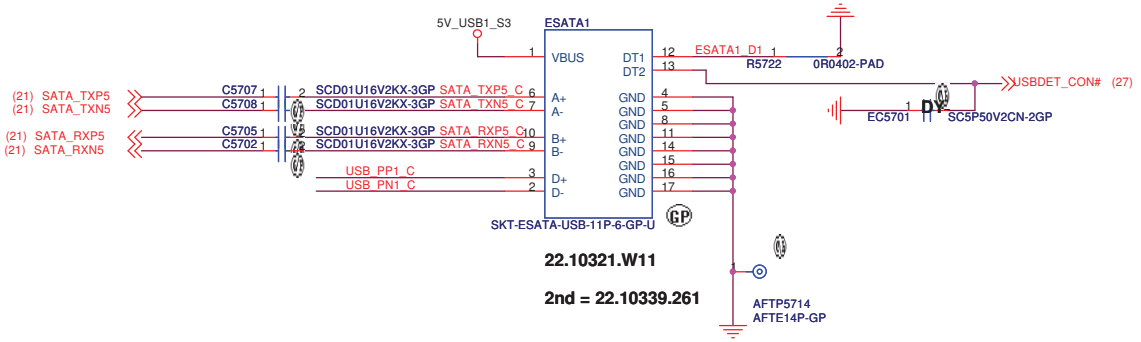
S0	S1	
0	0	Auto
0	1	
1	0	
1	1	D+/- connects to Y+/-

Switch Control Bit:
CB=0 (AM):auto detection charger identification active.
CB=1 (PM):connect DP/DM to TDP/TDM.

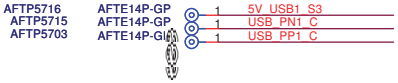
ESATA CONN

20100104 A00:
Remove R5718,R5719





close to ESATA1



<Core Design>

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Title		
USB/ESATA		
Size: A3	Document Number: Nirvana 13	Rev: A00
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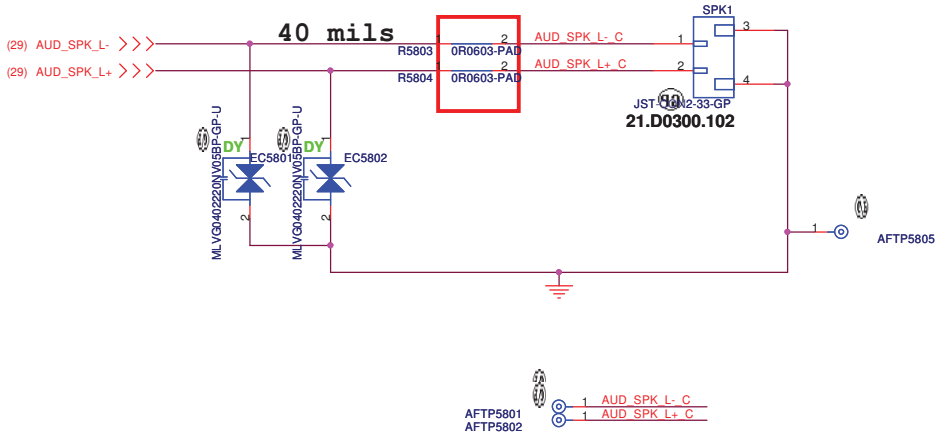
SSID = AUDIO

Speaker Connector

20101224 A00:
Change R5803,R5804 to 0603 0 ohm pad.

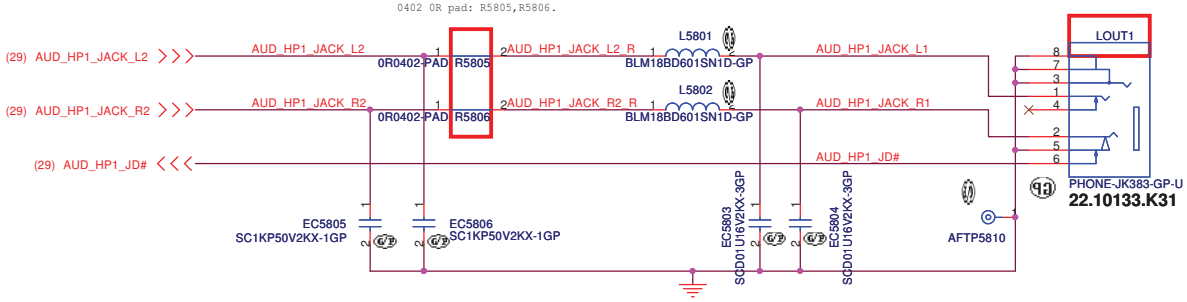


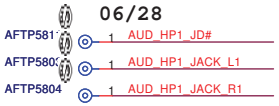
06/28

LINE OUT

20101224 A00:
Rename LINEOUT1 to LOUT1.

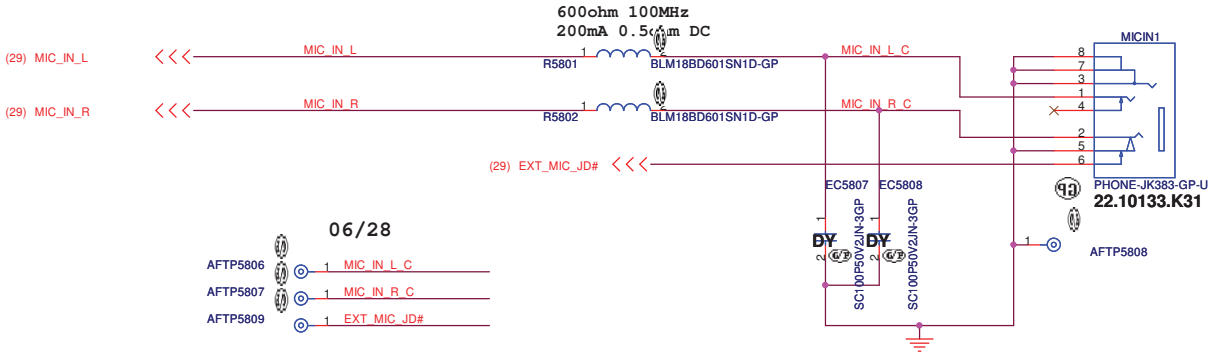
20101224 A00:
0402 0R pad: R5805,R5806.





06/28

MIC IN



06/28

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack		
Size: A3	Document Number: Nirvana 13	Rev: A00
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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

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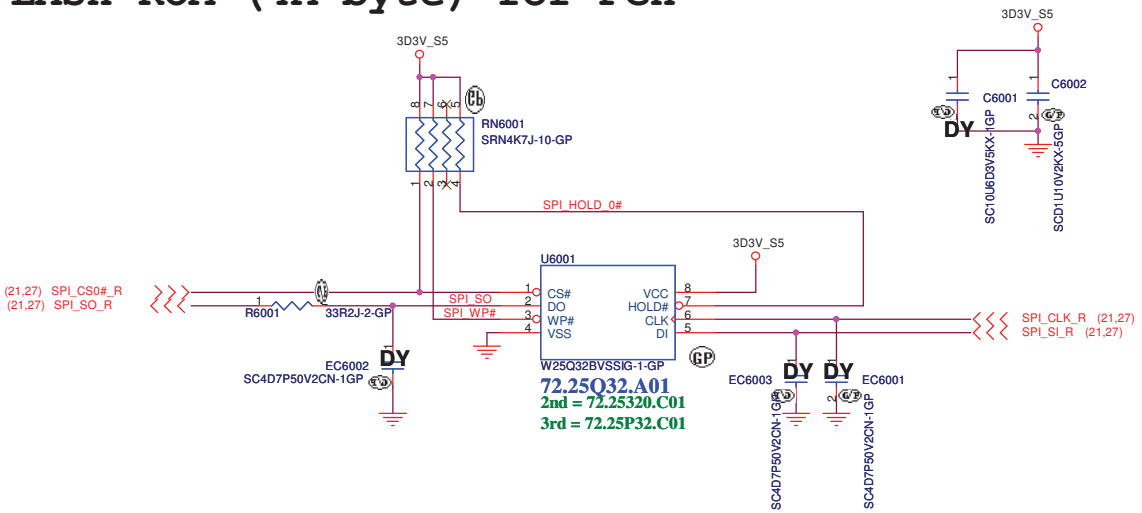
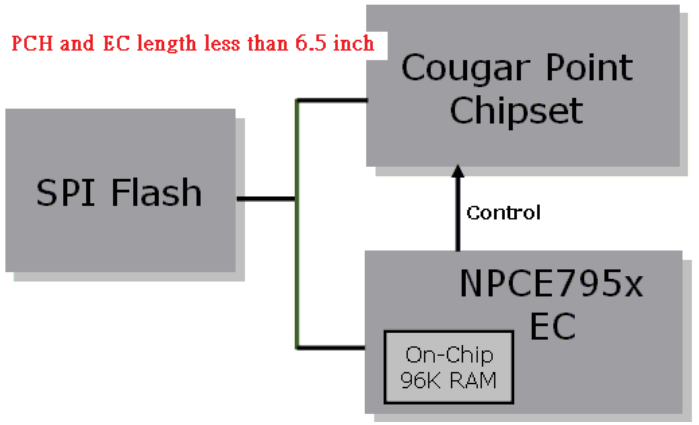
SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH

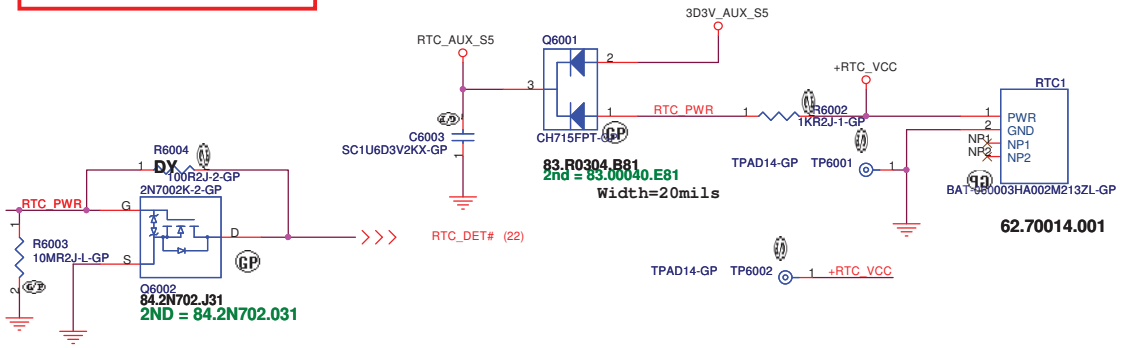


Priority	Wistron P/N	Manufacturer	Vendor P/N
1	72.25Q32.A01	WINDBOND	W25Q32BVSSIG
2	72.25320.C01	MXIC	MX25L3206EM2I-12G
3	72.25P32.C01	NUMONYX	M25PX32-VMW6F

Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil



SSID = RBATT



<Core Design>

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Title: Flash/RTC

Size	Document Number	Rev
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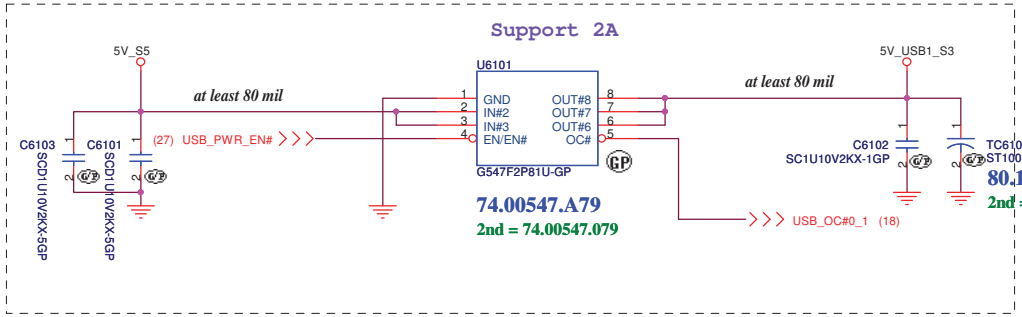
SSID = USB

Close to ESATA Combo connector

USB POWER SW
Main G547F2P81U-GP P/N:74.00547.A79



<Core Design>

Wistron Corporation
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Title: USB2.0 Power SW

Size | Document Number: Nirvana 13 | Rev: A00

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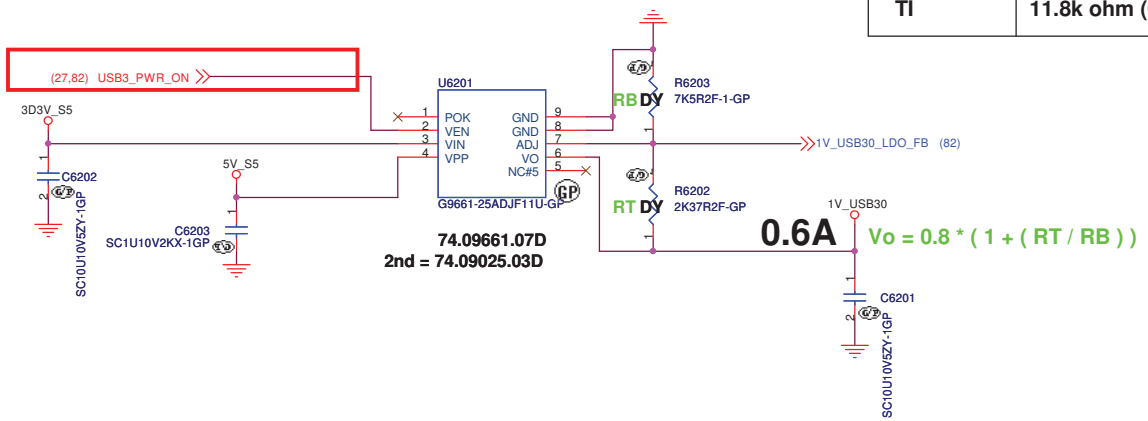
1V_USB30 LDO

20101227 A00:
Change R6205 to 0R 0402 pad.
20101228 A00:
VGA_THRM change to USB_PWR_EN.
20101229 A00:
Remove R6205,R6201 and rename USB3_PWR_ON from USB_PWR_EN.

USB3.0 Host	RT (R6202)	RB (R6203)	VOUT
NEC	2.37k ohm (64.23715.6DL)	7.5k ohm (64.75015.6DL)	1.05V
TI	11.8k ohm (64.11825.6DL)	30.9k ohm (64.30925.6DL)	1.1V



<Core Design>

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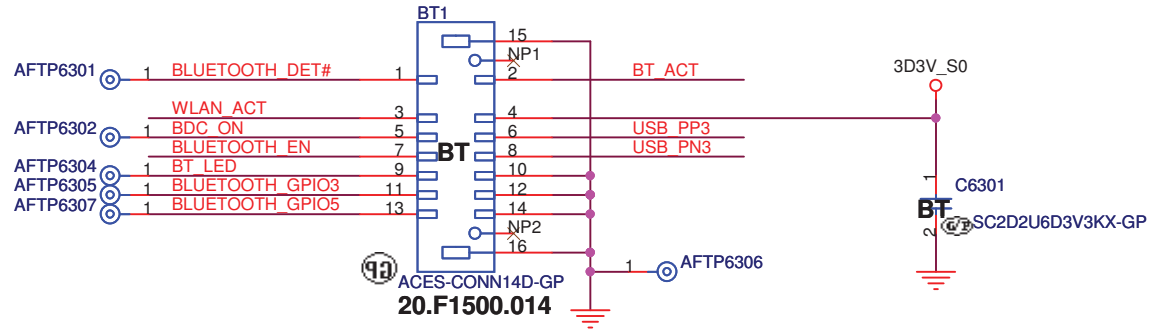
Title: USB 3.0 Port

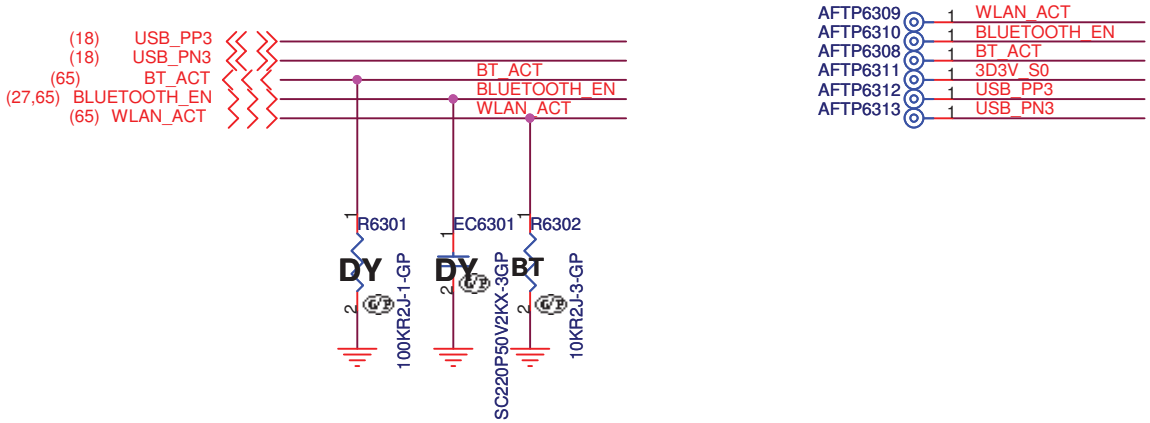
Size: A3 | Document Number: Nirvana 13 | Rev: A00

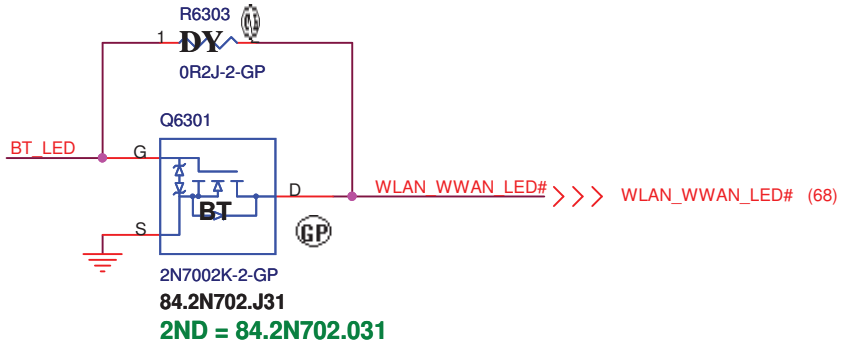
Date: Tuesday, January 18, 2011 | Sheet 62 of 104

SSID = User.Interface

Bluetooth Module







<Core Design>

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Title: Bluetooth

Size	Document Number	Rev
A4	Nirvana 13	A00

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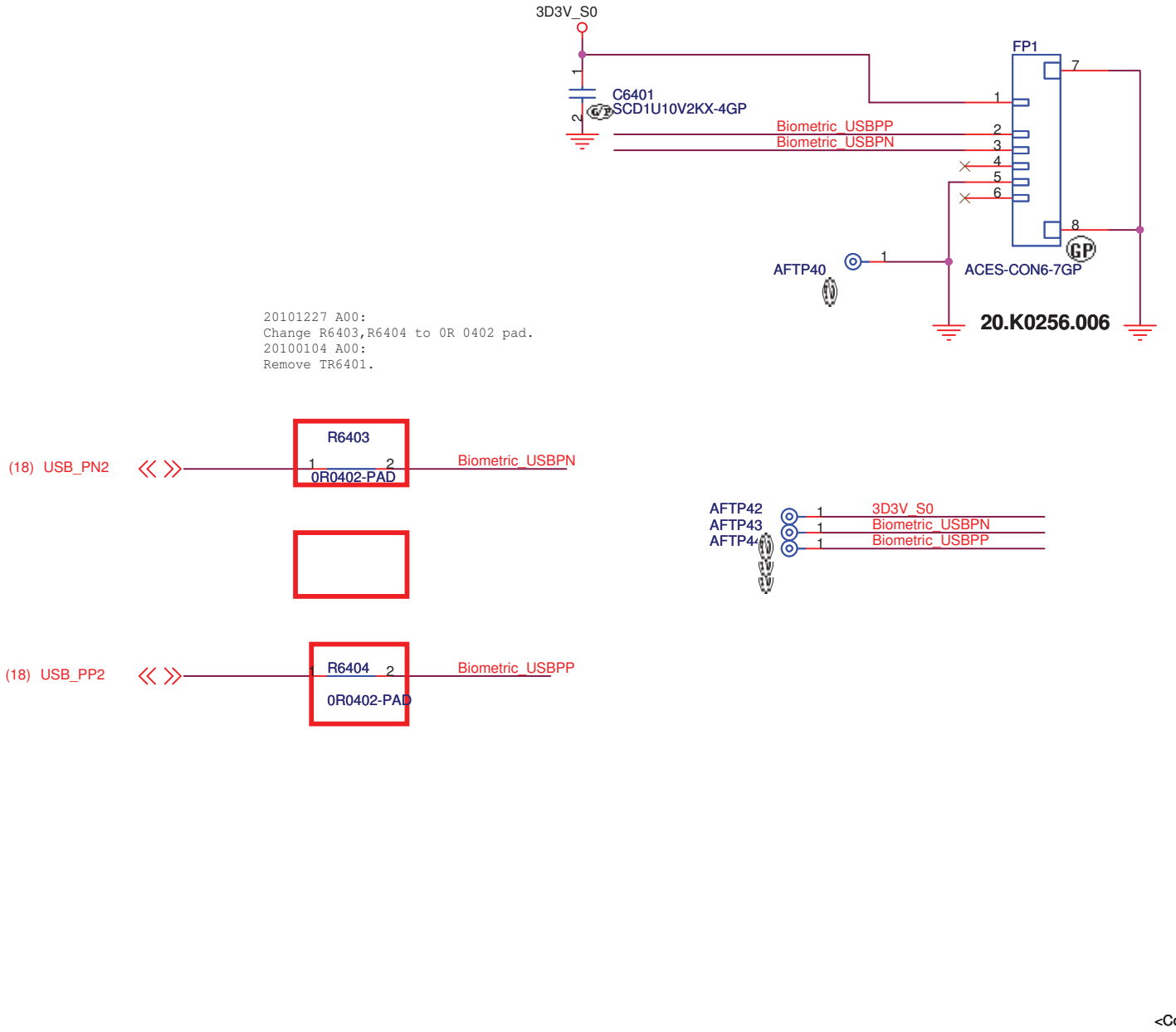

<Core Design>

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Title: ***Finger Printer Conn***

Size	Document Number	Rev
A4	***Nirvana 13***	***A00***

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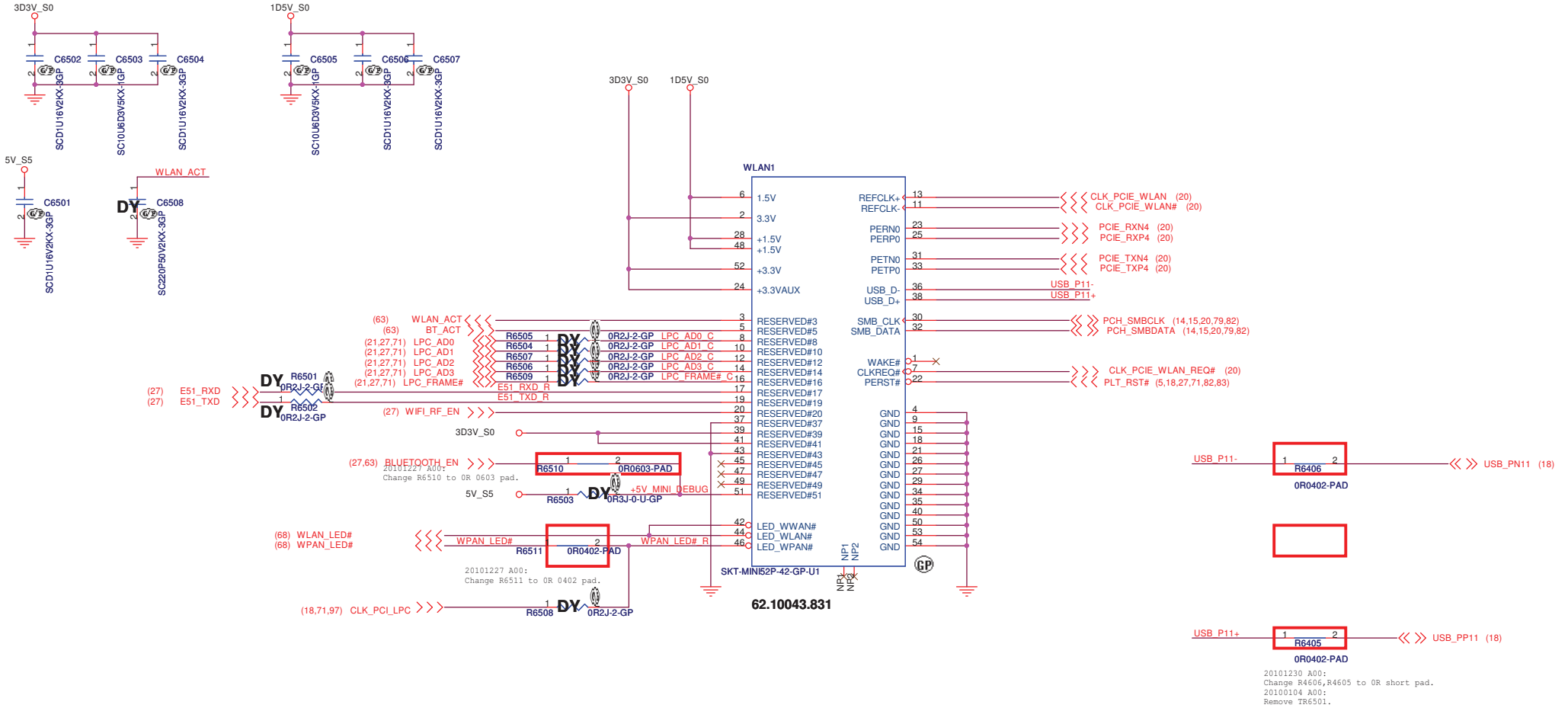
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>

Wistron Corporation
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Title: MINICARD(WLAN)/ITP CONN

Size	Document Number	Rev
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

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A3	Nirvana 13	A00

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Nirvana 13***	***A00***

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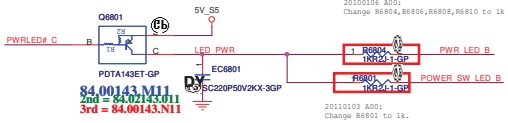
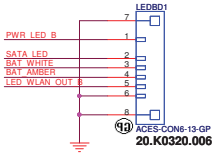
SSID = User.Interface

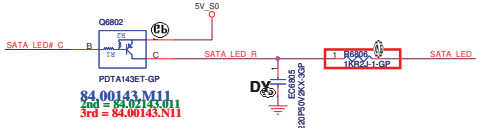
Power LED(White)

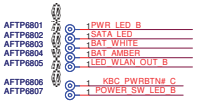


LED BD Connector

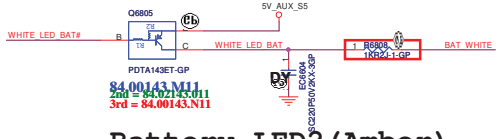


SATA HDD LED(White)

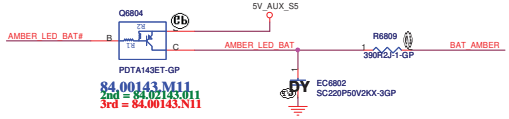




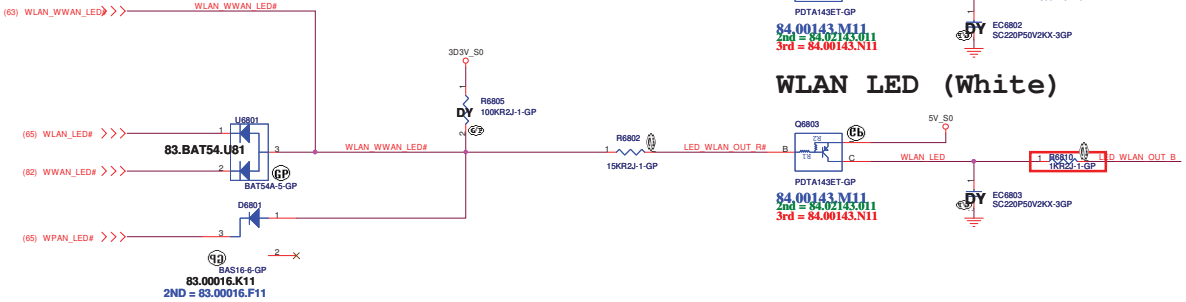
Battery LED1(White)



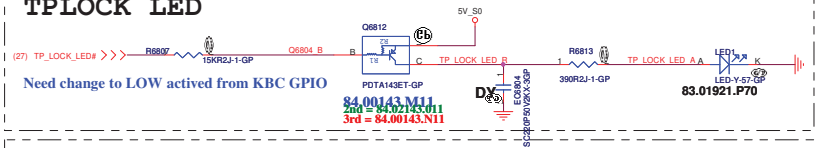
Battery LED2(Amber)



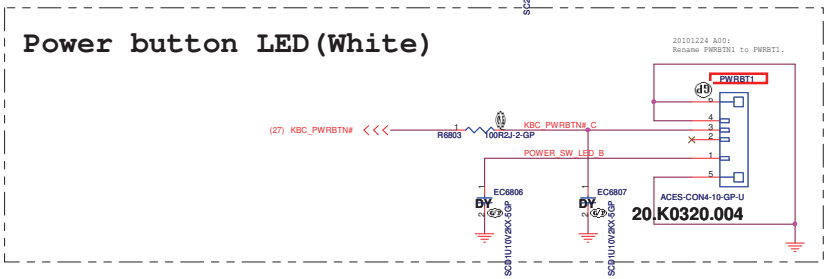
WLAN LED (White)



TPLOCK LED



Power button LED(White)



<Core Design>

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Title: LED Bord/Power Button

Size: A2 | Document Number: Nirvana 13 | Rev: A00

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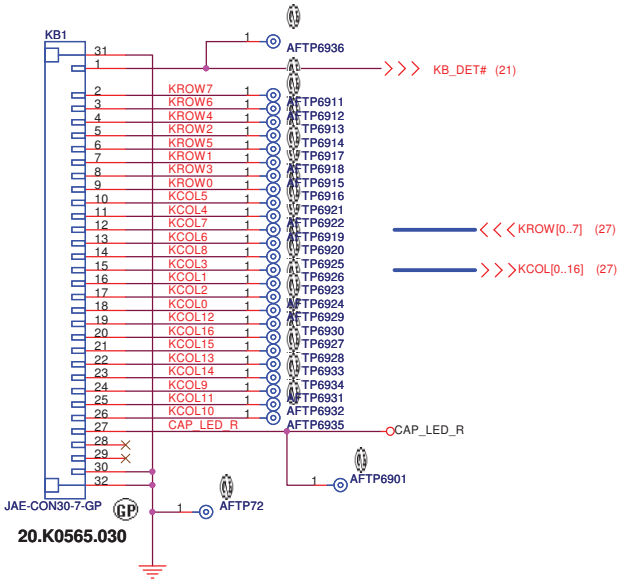
SSID = KBC

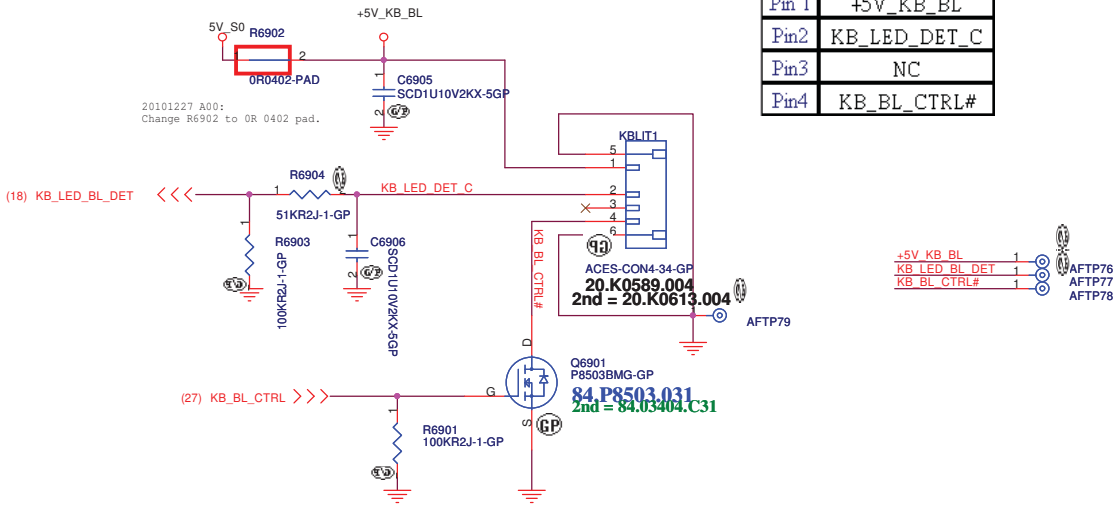
Internal KeyBoard Connector

PIN No.	Description
1	Diag_Loop=GPIO_1(TPC)
2	KSI[7] = KBD S8
3	KSI[6] = KBD S7
4	KSI[4] = KBD S5
5	KSI[2] = KBD S3
6	KSI[5] = KBD S6
7	KSI[1] = KBD S2
8	KSI[3] = KBD S4
9	KSI[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	CapsLock LED
28	N/C
29	N/C
30	GND

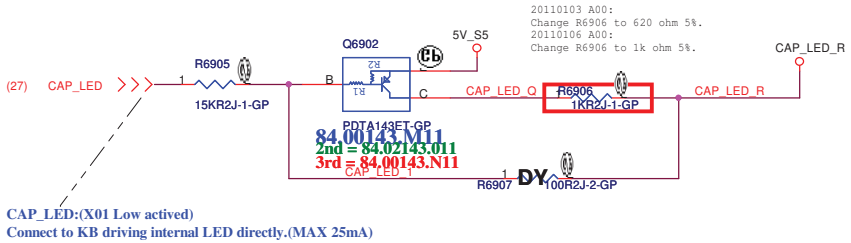


KB Backlight Connector

MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#



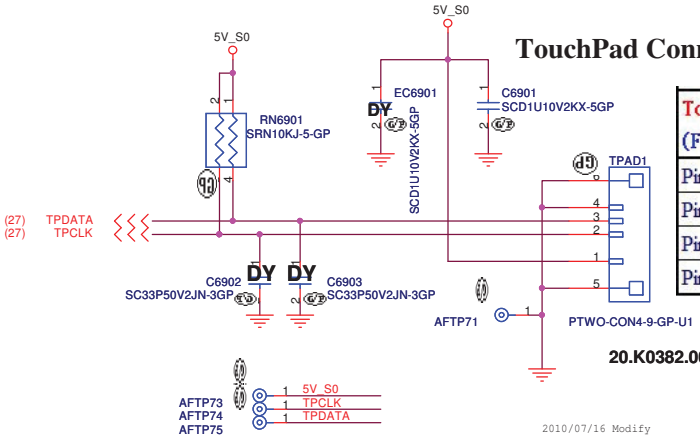
CAP LED CONTROL



TouchPad LOCKED

TouchPad Connector

Touch Pad CN1 CONN. (FFC)	
Pin 1	5V_S0
Pin 2	TPCLK
Pin 3	TPDATA
Pin 4	GND



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad/Media Board

Size	Document Number	Rev
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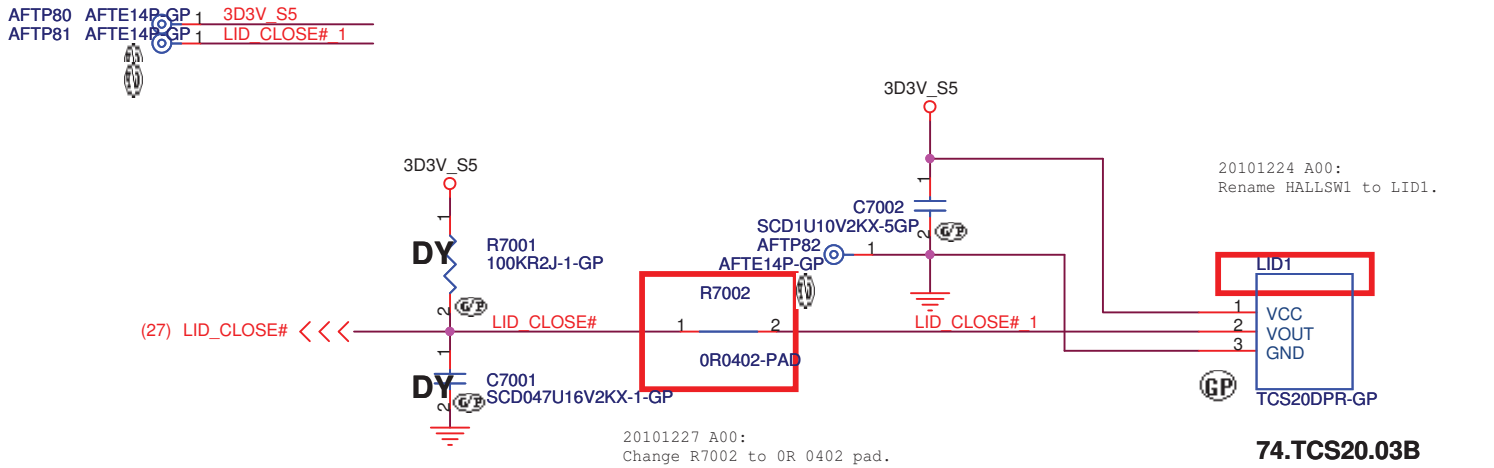

74.TCS20.03B

2nd = 74.09132.A7B

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***		
Size: A4	Document Number: ***Nirvana 13***	Rev: ***A00***
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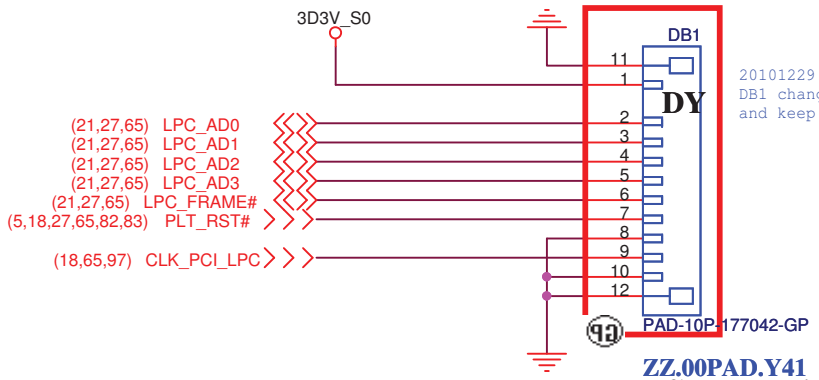

20101229 A00 Modify:
DB1 change to ZZ.00PAD.Y41(solder mask type)
and keep un-stuff at X-Build stage.

ZZ.00PAD.Y41
PCB Footprint = PAD-10P-177042

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug CONN***		
Size: A4	Document Number: ***Nirvana 13***	Rev: ***A00***
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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 72 of 104

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

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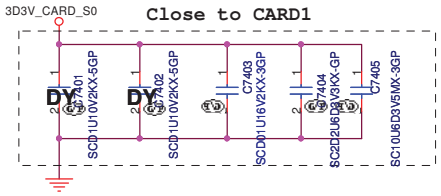
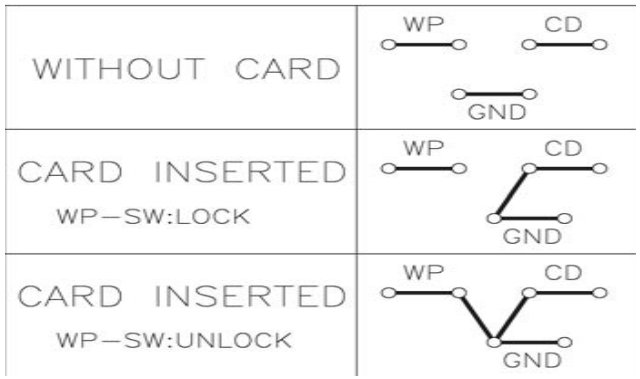
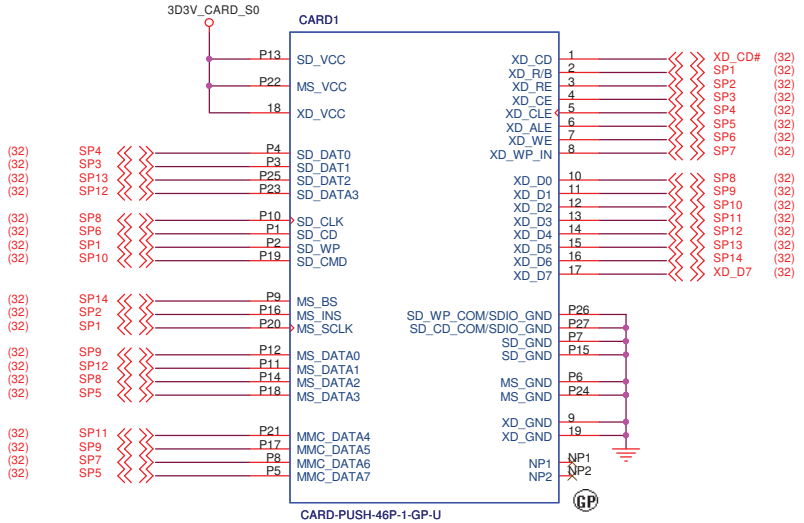
SSID = SDIO



SD/XD/MS/MMC+ Card Reader

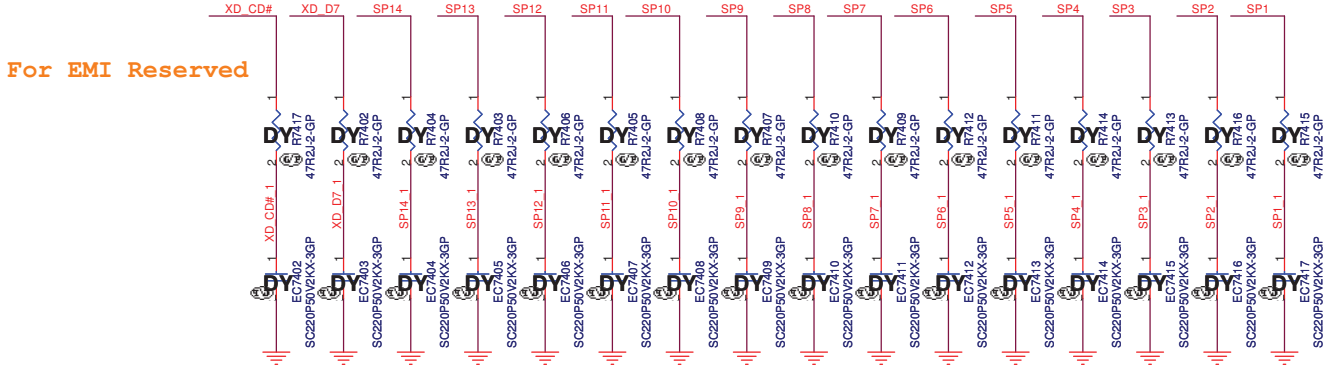
PIN	TYPE	FUNCTION	RTS5138 NET
1	SD	SD-DAT2	SP13
2	SD	SD-CD/DAT3	SP12
3	MMC_PLUS	MMC-DAT4	SP11
4	SD	SD-CMD	SP10
5	MMC_PLUS	MMC-DAT5	SP9
6	SD	SD-VSS	POWER
7	SD	SD-VDD	POWER
8	MemoryStick	MS-VSS	POWER
9	MemoryStick	MS-VCC	POWER
10	MemoryStick	MS-SCLK	SP1
11	MemoryStick	MS-DATA3	SP5
12	MemoryStick	MS-INS	SP2
13	MemoryStick	MS-DATA2	SP8
14	MemoryStick	MS-DATA0	SP9
15	MemoryStick	MS-DATA1	SP12
16	MemoryStick	MS-BS	SP14
17	MemoryStick	MS-VSS	POWER
18	SD	SD-CLK	SP8
19	MMC_PLUS	MMC-DAT6	SP7
20	SD	SD-VSS	POWER
21	MMC_PLUS	MMC-DAT7	SP5
22	SD	SD-DAT0	SP4
23	SD	SD-DAT1	SP3
24	SD	SD-COM(SW)	
25	SD	SD-CD(SW)	SP6
26	XD	XD-GND	POWER
27	XD	XD-CD	XD_CD#
28	XD	XD-R/-B	SP1
29	XD	XD-RE	SP2
30	XD	XD-CE	SP3
31	XD	XD-CLE	SP4
32	XD	XD-ALE	SP5
33	XD	XD-WE	SP6
34	XD	XD-WP	SP7
35	XD	XD-GND	POWER
36	XD	XD-D0	SP8
37	XD	XD-D1	SP9
38	XD	XD-D2	SP10
39	XD	XD-D3	SP11
40	XD	XD-D4	SP12
41	XD	XD-D5	SP13
42	XD	XD-D6	SP14
43	XD	XD-D7	XD-D7
44	XD	XD-VCC	POWER
45	SD	SD-WP(SW)	SP1





20.I0129.001

2nd = 20.I0135.001



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size: A3 | Document Number: Nirvana 13 | Rev: A00

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<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 75 of 104

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<Core Design>

Wistron Corporation
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Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

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<Core Design>

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Title: *Reserved*

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<Core Design>

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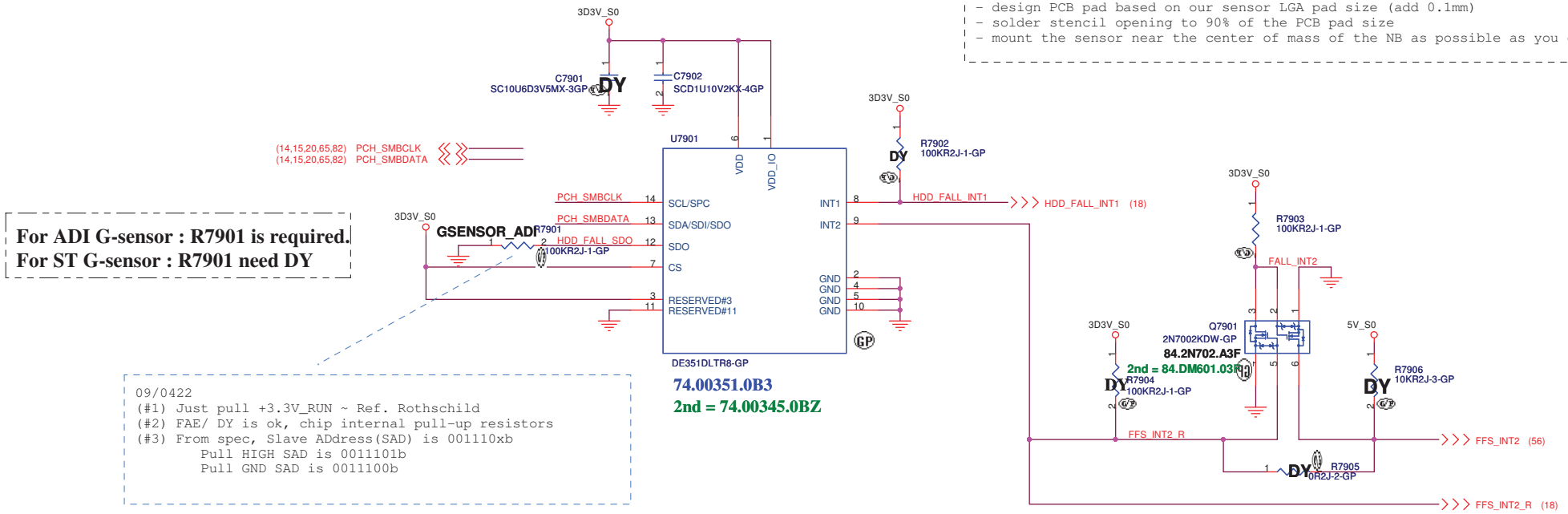
SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
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Title: Free Fall Sensor		
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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<Core Design>

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Title

Reserved

Size	Document Number	Rev
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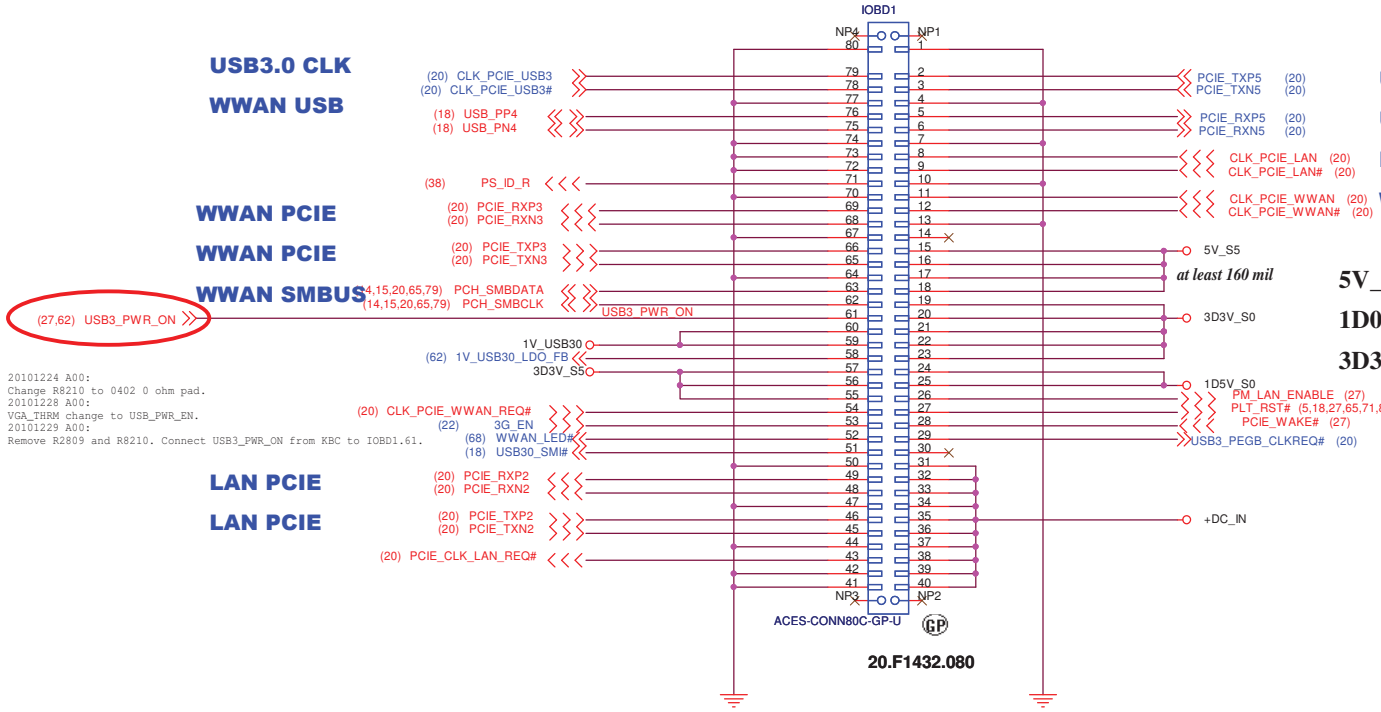
IO Board CONN 80 pin



USB3.0 PCIE
USB3.0 PCIE
LAN CLK
WWAN CLK

20101224 A00:
Change R8210 to 0402 0 ohm pad.
20101228 A00:
VGA_THRM change to USB_PWR_EN.
20101229 A00:
Remove R2809 and R8210. Connect USB3_PWR_ON from KBC to IOBD1.61.

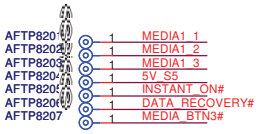
5V_USB FOR USB3.0 POWER at least 4A

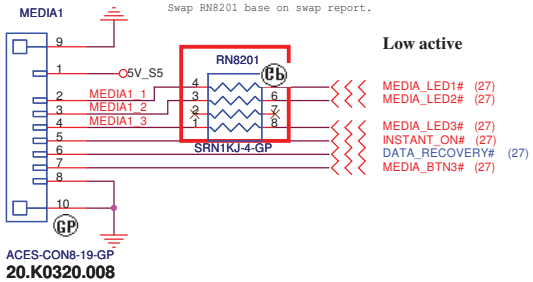
1D05V_VTT FOR USB3.0 POWER at least ?A

3D3V_S5 FOR LAN POWER at least over 3pin amount.

1D5V_S0 FOR USB3.0 POWER at least ?A

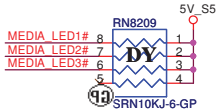
Media Button Board Connector

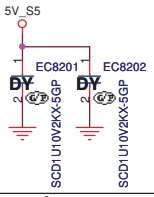


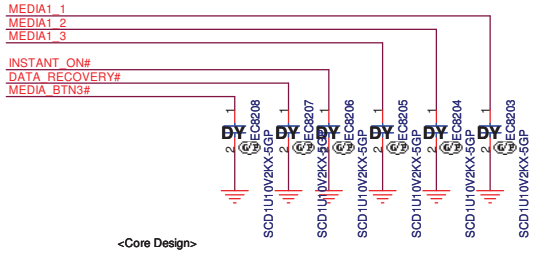


20110103 A00:
Change R8201~R8203 to 1k.
20110104 A00:
Merge R8201~R8203 to RN8201 1k array resistor.
20110113 A00:
Swap RN8201 base on swap report.

Low active







<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
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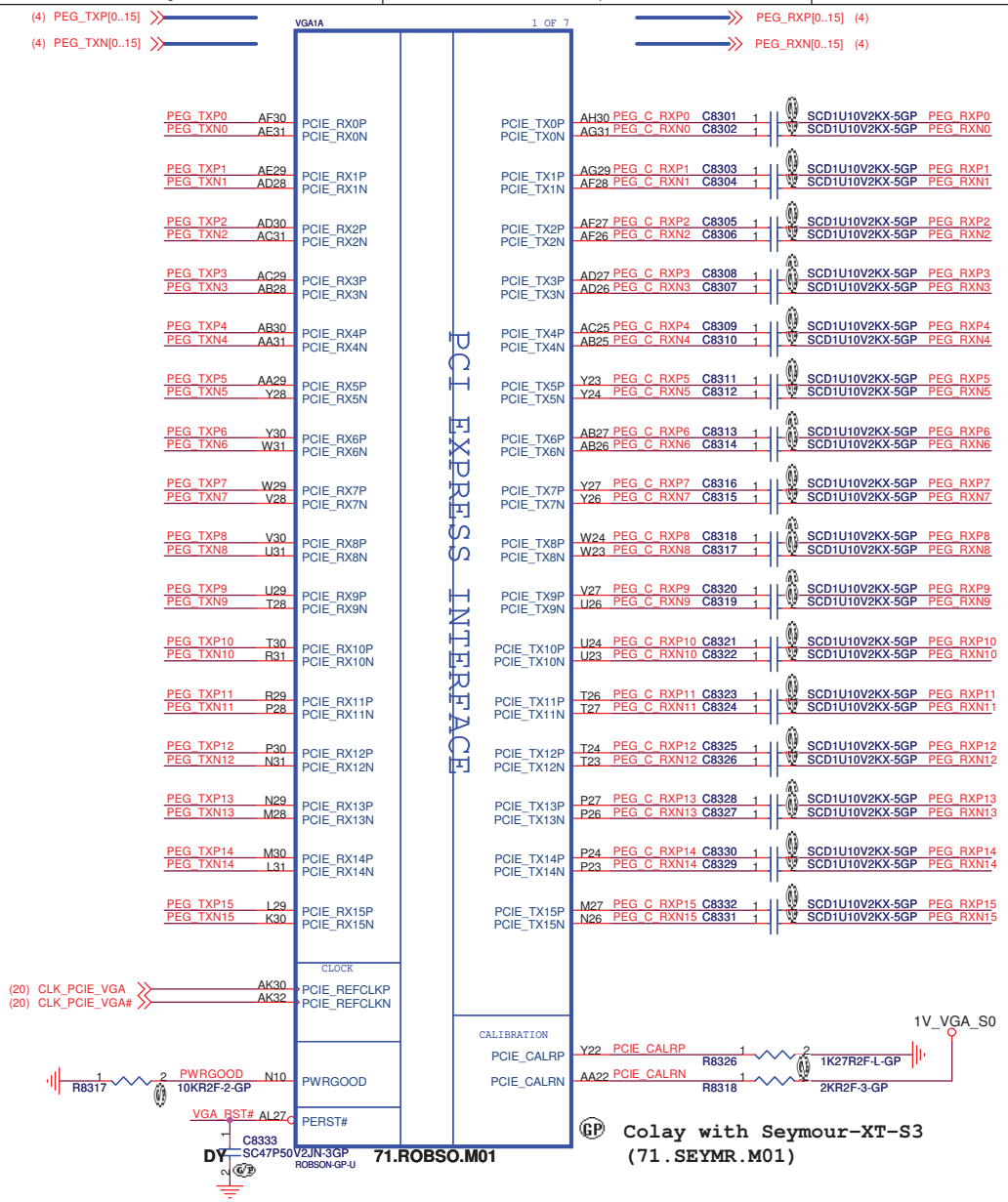


CONFIGURATION STRAPS

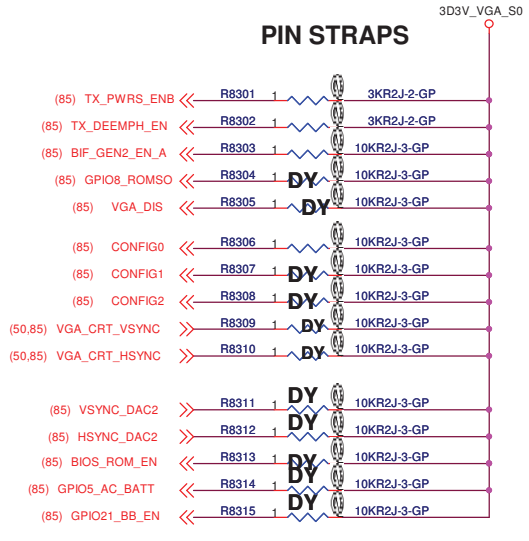
0= DO NOT INSTALL RESISTOR

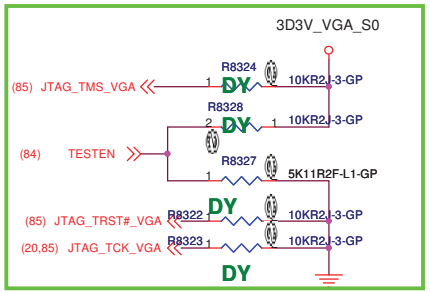
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS

1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

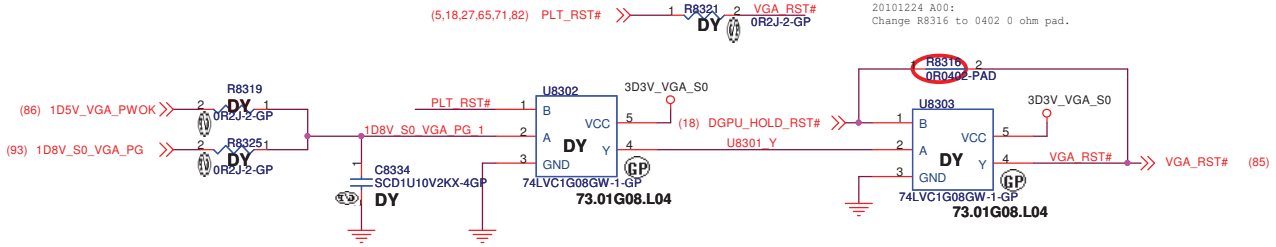




JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

dGPU reset for PX/SG transitions



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU PEG/STRAPPING(1/5)

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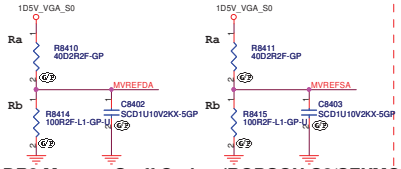
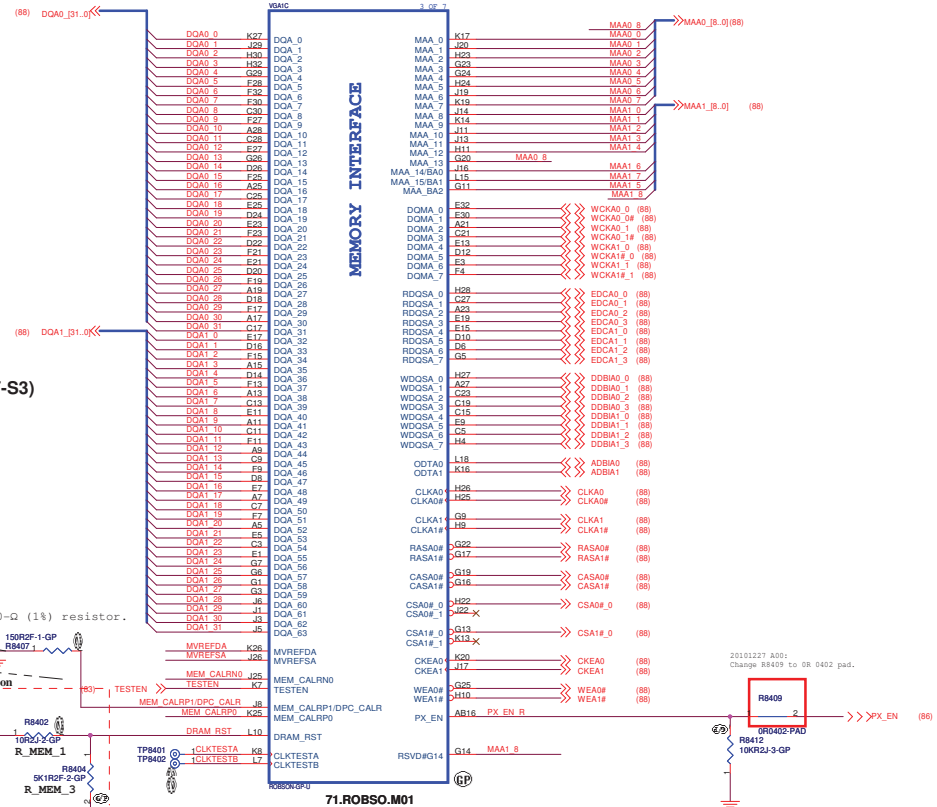
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

	DDR5	DDR3
MVDDQ	1.5V	1.5V/1.8V
Ra	40.2R	40.2R
Rb	100R	100R



71.ROBSO.M01

Colay with Seymour-XT-S3
(71.SEYMR.M01)

**This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM	120pF	120pF

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R_MEM_2

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size	Document Number	Rev
A2	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 84 of 104

MEMORY ID Table

DVPDATA[0:3]	Description
0001	GDDR5 1.25GHZ Hynix-H5GQ2H24MFR-T2C 64M*32
0000	GDDR5 1.25GHZ SAMSUNG-K4G20325FC-HC04 64M*32

DVPDATA[0:3] Default:Pull down

For Seymour,
DPC_PVDD is DPC_VDD18
DPC_PVSS and all DPC_VSSR are DP_VSSR

MEM_ID Control

Hynix_512

LVDS Interface

71.ROBSO.M01

VGA18 — M93-S3/M92-S2 / M93-S3/M92-S2 / M92-S2/M93-S3 / M92-S2/M93-S3 / M92-S2/M93-S3

DVCNTL_0/DVPDATA_18
DVCNTL_1/NC#L9
DVCNTL_2/TESTEN#2
DVDATA_12/DVPDATA_16
DVDATA_11/DVPDATA_20
DVDATA_10/DVPDATA_22
DVDATA_9/DVPDATA_12
DVDATA_8/DVPDATA_14
DVDATA_7/DVPCNTL_0
DVDATA_6/DVPDATA_8
DVDATA_5/DVPDATA_6
DVDATA_4/DVPDATA_4
DVDATA_3/DVPDATA_19
DVDATA_2/DVPDATA_21
DVDATA_1/DVPDATA_2
DVDATA_0/DVPDATA_0
DVO

TXCAP_DPA3P / TXCAM_DPA3N
DPA
TX0P_DPA2P / TX0M_DPA2N
TX1P_DPA1P / TX1M_DPA1N
TX2P_DPA0P / TX2M_DPA0N
TXCBP_DPB3P / TXCBM_DPB3N
DPB
TX3P_DPB2P / TX3M_DPB2N
TX4P_DPB1P / TX4M_DPB1N
TX5P_DPB0P / TX5M_DPB0N

DPC_PVSS/DVPDATA_11
DPC_VDD18#1/DVPDATA10
DPC_VDD18#2/DVPDATA23
DPC_VDD18#1/DVPDATA15
DPC_VDD18#2/DVPDATA17
DPC_VSSR#1/DVPCLK
DPC_VSSR#2/DVPDATA5
DPC_VSSR#3/GND
DPC_VSSR#4/GND
DPC_VSSR#5/DVPCNTL_MV0
DPC

I2C

GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_HPD3
GPIO_17_THERMAL_INT
GPIO_18_HPD5
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB

DAC1
R/R#
G/G#
B/B#
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1DI
VSS1DI

DAC2
R2/NC#AM12
R2#/NC#AK12
G2/NC#AL11
G2#/NC#AJ11
B2/NC#AK10
B2#/NC#AL9
C/NC#AH12
Y/NC#AM10
COMP/NC#AJ9
H2SYNC
V2SYNC
VSS2DI/NC#AC19
A2VDD/NC#AE20
A2VDDQ/NC#AE17
A2VSSQ
R2SET/NC#AG13

VGA_CRT_RED (50)
VGA_CRT_GREEN (50)
VGA_CRT_BLUE (50)
VGA_CRT_HSYNC (50,83)
VGA_CRT_VSYNC (50,83)
GPU_RSET
AVDD_A2VDDQ
AVSSQ
HSYNC_DAC2 (83)
VSYNC_DAC2 (83)
VSS2DI_GPU
A2VDD_GPU
A2VDDQ_GPU
RSET
50 mA
130 mA
1.5 mA

M92-S2/M93-S3 — PLL/CLOCK

DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
VREFG
XTALIN
XTALOUT
THERMAL
DPLUS
DMINUS
TS_FDO
TSVDD
TSVSS

DDC/AUX

DDC1CLK / DDC1DATA — DDC1 channel for CRT
AUX1P / AUX1N
DDC2CLK / DDC2DATA — DDC2 channel for HDMI
AUX2P / AUX2N
DDCCLK_AUX5P / DDCDATA_AUX5N
DDCCLK / DDCDATA
NC#AD20/DDCCLK_AUX3P
NC#AC20/DDCDATA_AUX3N

GPU_HDMI_CLK (51)
GPU_HDMI_DATA (51)

DDC1/DDC2/DDC6 have 5V-tolerant

71.ROBSO.M01
Colay with Seymour-XT-S3
(71.SEYMR.M01)

1Mbit SERIAL EEPROM is optional for Seymour GDDR5 Design

1Mbit SERIAL EEPROM is required for Park/Robson GDDR5 Design

NOTE: Designs that do not include an EEPROM must still provide access to the ROM interface signals for debug purposes

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

Clock Input Configuration -GDDR5 with Park, Robson and Seymour
a) 27MHz (3.3V) oscillator connected to XO_IN, AND
b) 100MHz (3.3V) oscillator (no spread or spread) connected to XO_IN2

100 MHz Spread Selection Table

S1	S0	Down Spread%
L	L	OFF
L	M	-0.5
L	H	-2.5
M	L	-0.25
M	M	-0.75
M	H	-1.0
H	L	-1.5
H	M	-2.0
H	H	-3.0

71.64088.003

<Core Design>

Wistron Corporation
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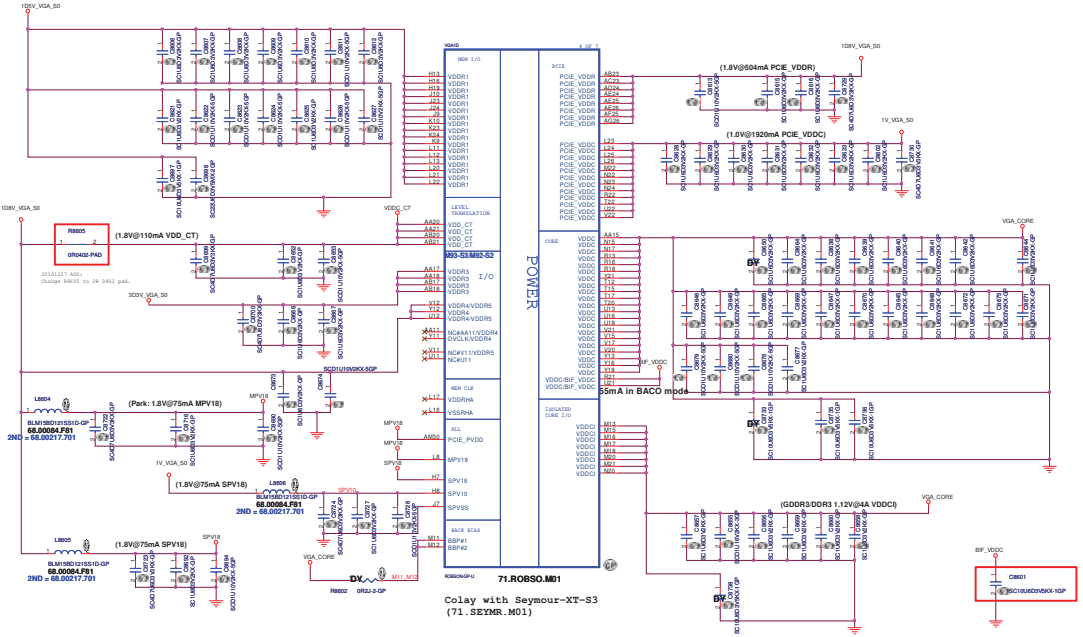
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A1 | Document Number: Nirvana 13 | Rev: A00

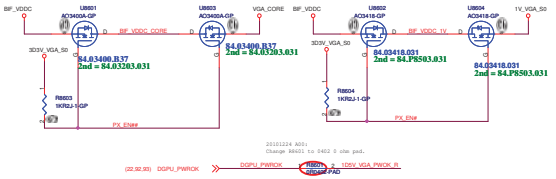
Date: Tuesday, January 18, 2011 | Sheet 85 of 104

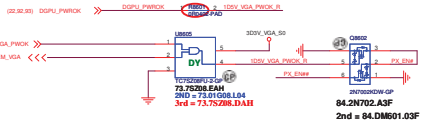


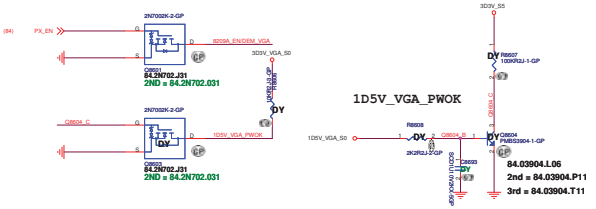
FX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

	PX_EN	8209A_EN/DEM_VGA	1D5V_VGA_PWOK_R	PX_EN#	PX_EN##	BIF_VDDC
Non-BACO	0	1	1	0	1	VGA_Core
BACO	1	0	0	1	0	1V_VGA

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN## = High, BIF_VDDC = VGA_CORE







<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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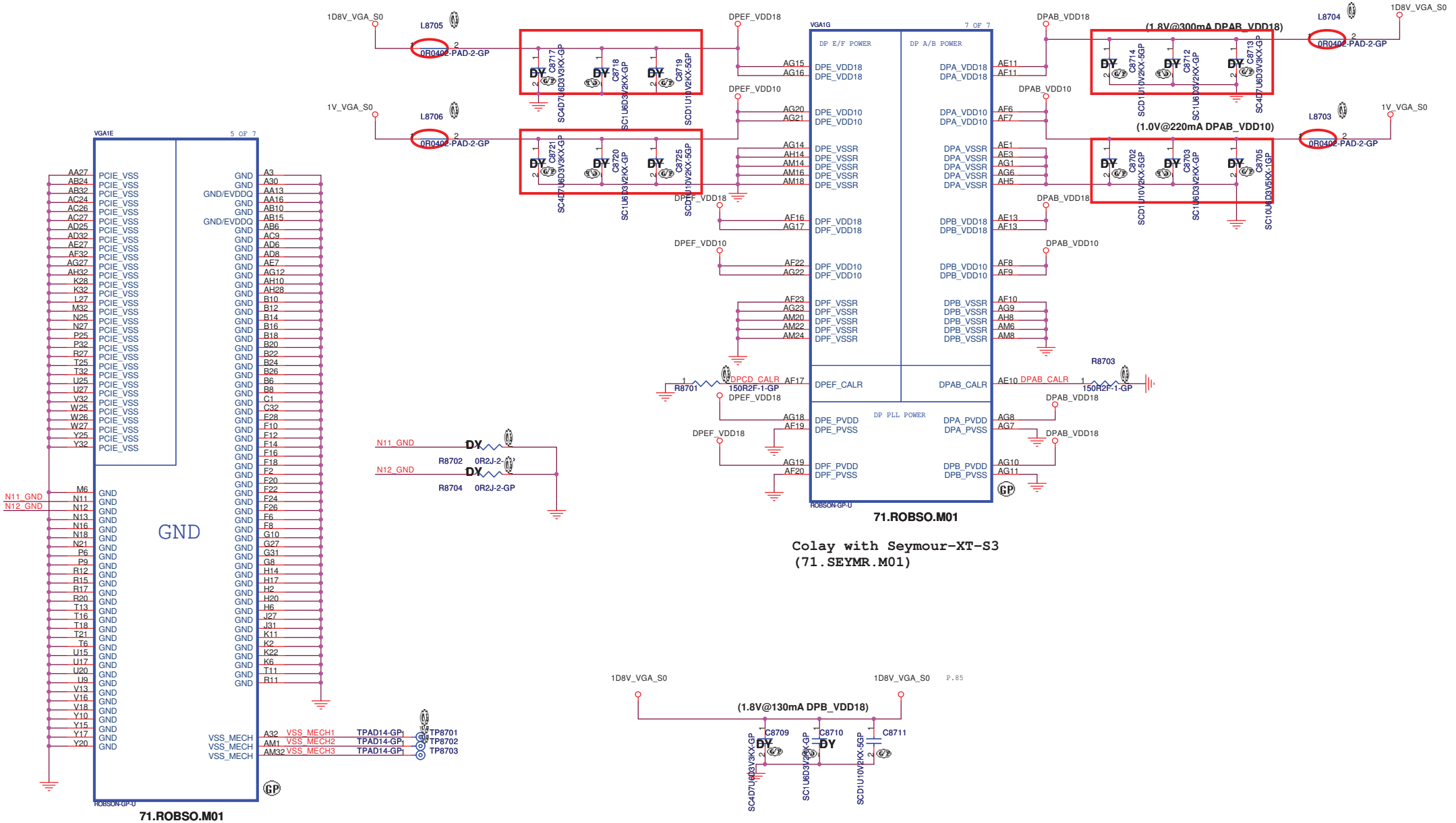
Title: GPU_POWER(4/5)

Size	Document Number	Rev
A1	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 8 of 104

20101224 A00:
Change L8703,L8704,L8705,L8706 to 0402 0 ohm pad.
Un-stuff DPx_VDD18 caps.



Colay with Seymour-XT-S3
(71.SEYMR.M01)

Colay with Seymour-XT-S3
(71.SEYMR.00U)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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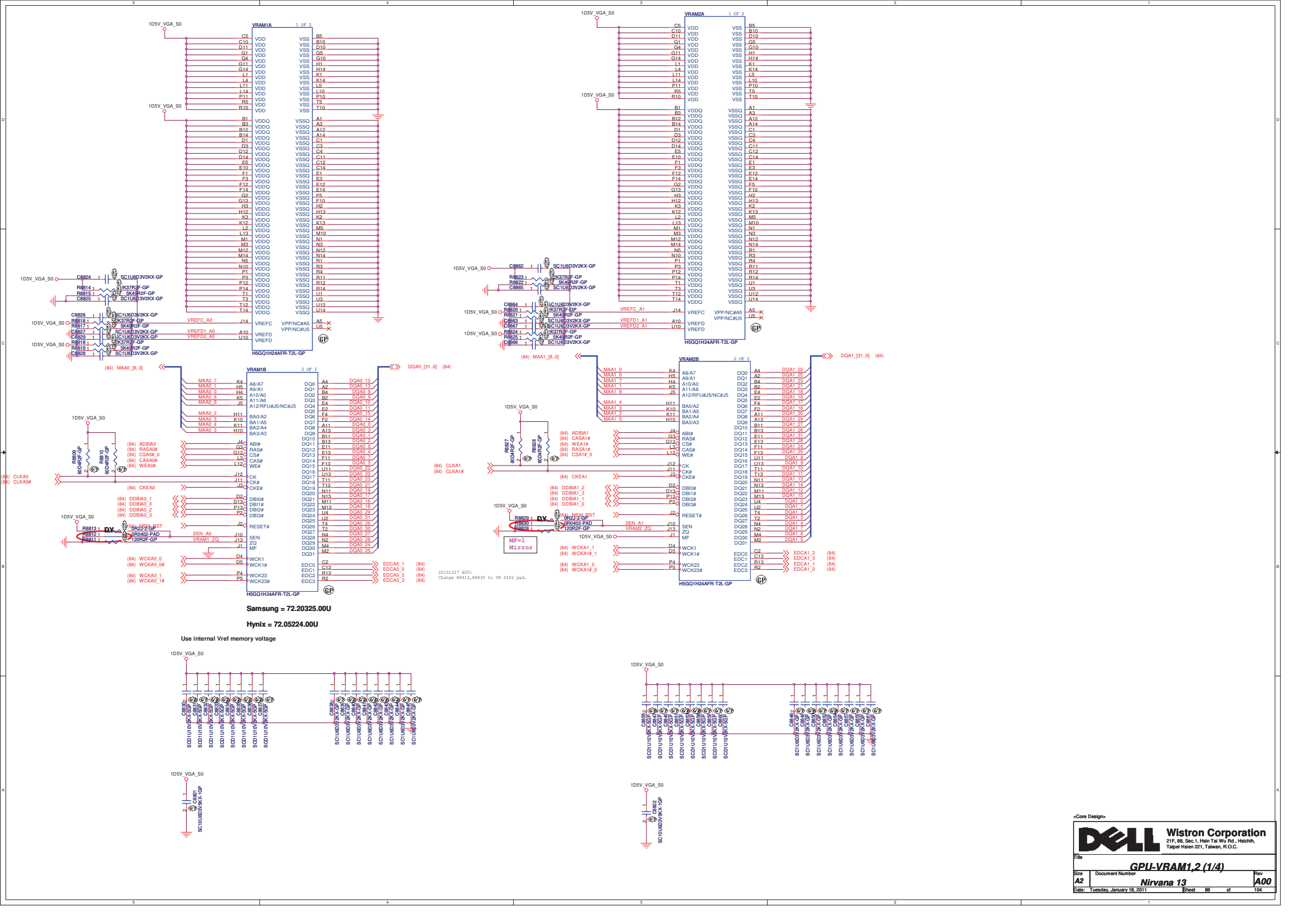
Title	GPU_DPPWR/GND(5/5)	
Size: A3	Document Number: Nirvana 13	Rev: A00
Date: Tuesday, January 04, 2011	Sheet 87 of 104	


VRAM1A
VRAM2A
VRAM1B
VRAM2B
H5GQ1H24AFR-T2L-GP
Samsung = 72.20325.00U
Hynix = 72.05224.00U
Use internal Vref memory voltage
MF=1
Mirror
20101227 A00:
Change R8812,R8830 to 0R 0402 pad.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU-VRAM1,2 (1/4)
Size
A2
Document Number
Nirvana 13
Rev
A00
Date: Tuesday, January 18, 2011
Sheet 88 of 104

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<Core Design>

Wistron Corporation
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Title
RESERVED

Size	Document Number	Rev
A3	Nirvana 13	A00

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Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 90 of 104

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<Core Design>

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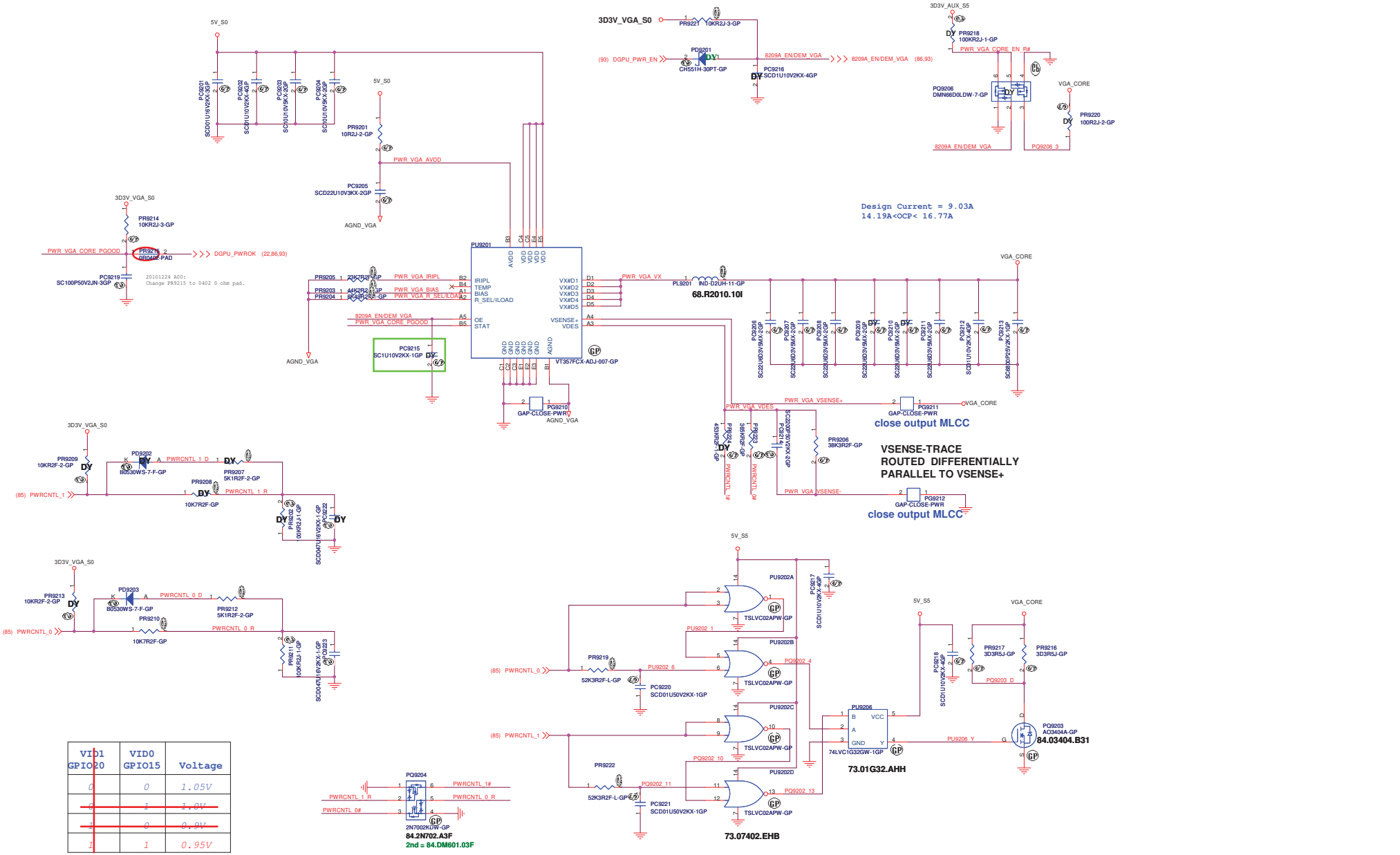
Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Tuesday, January 04, 2011 | Sheet 91 of 104



VID1 GPIO20	VID0 GPIO15	Voltage
0	0	1.05V
0	1	1.0V
1	0	0.9V
1	1	0.95V

PR9206	38.3	kohm
PR9224	DY	
PR9223	365	kohm

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: VT357_+VGA_CORE

Size: A2 | Document Number: Nirvana 13 | Rev: A00

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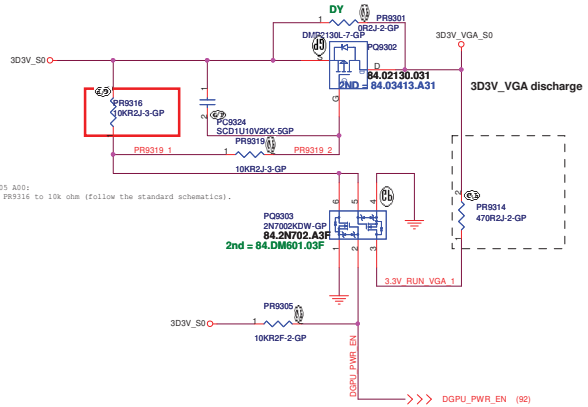
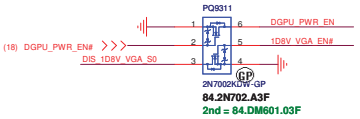
3D3V_S0 to 3D3V_VGA_S0 Transfer

Power on sequence for Robson-XT and SEYMOUR-XT:
3D3V_VGA_S0 --> 1V_VGA_S0 --> 1D8V_VGA_S0

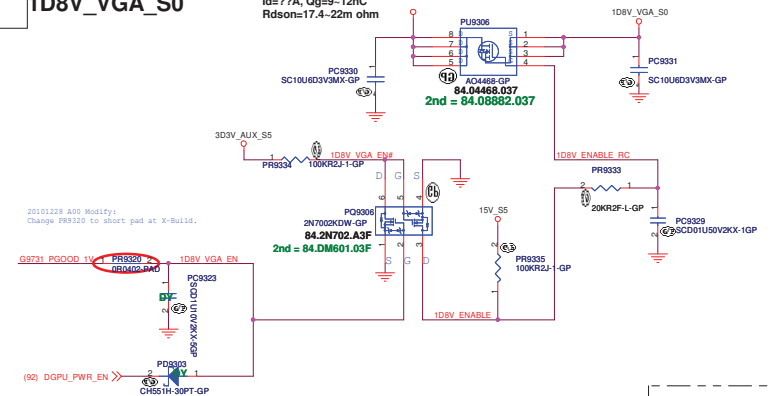


	DGPU_PWR_EN#
dGPU mode	L
IGPU	H
IGPU with BACO	L

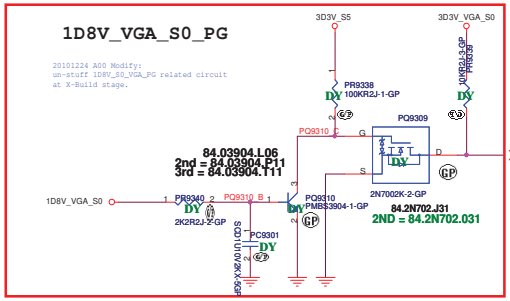


1D8V_VGA_S0

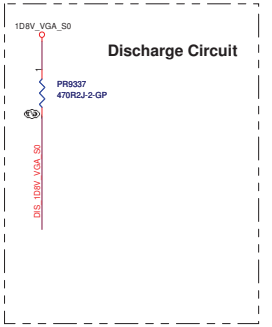
AO4468, SO-8
Id=??A, Qg=9~12nC
Rdson=17.4~22m ohm



1D8V_VGA_S0_PG



Discharge Circuit



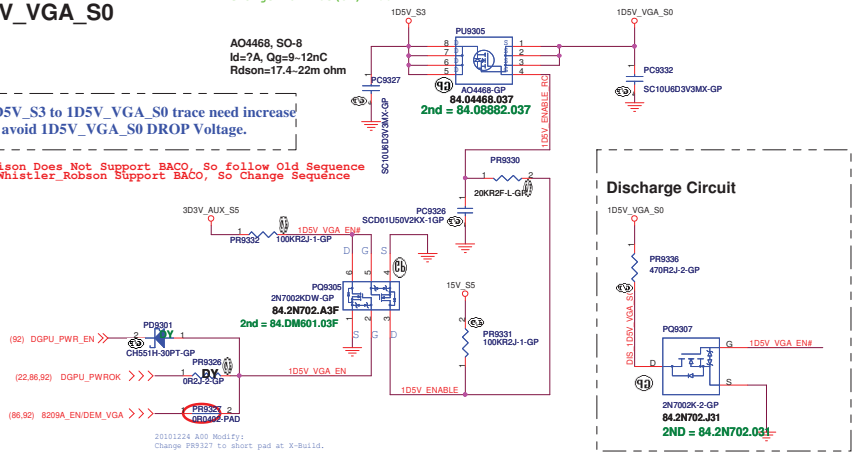
1D5V_VGA_S0

change low Rds(on) MOSFET

AO4468, SO-8
Id=?A, Qg=9~12nC
Rdson=17.4~22m ohm

1D5V_S3 to 1D5V_VGA_S0 trace need increase to avoid 1D5V_VGA_S0 DROP Voltage.

Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence



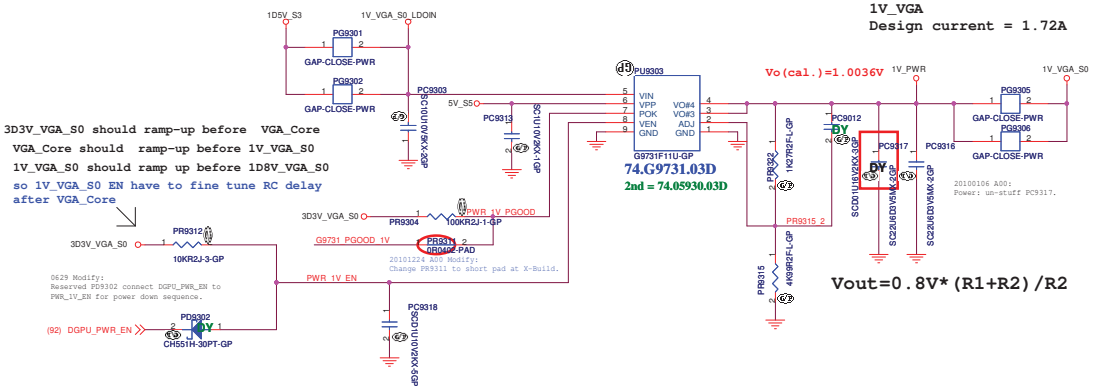
Discharge Circuit

G9731 for 1V_VGA_S0

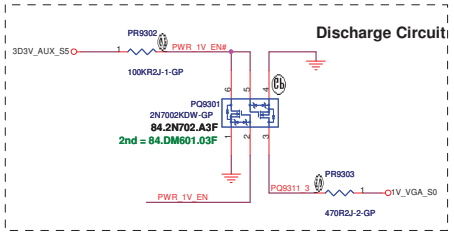
Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence

1V_VGA
Design current = 1.72A

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core



Discharge Circuit



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
A2	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 93 of 104

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<Core Design>

Wistron Corporation
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Title	***Reserved***	
Size	Document Number: ***Nirvana 13***	Rev: ***A00***
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(Blanking)

<Core Design>

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Title

Reserved

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(Blanking)

<Core Design>

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Title
Reserved

Size	Document Number	Rev
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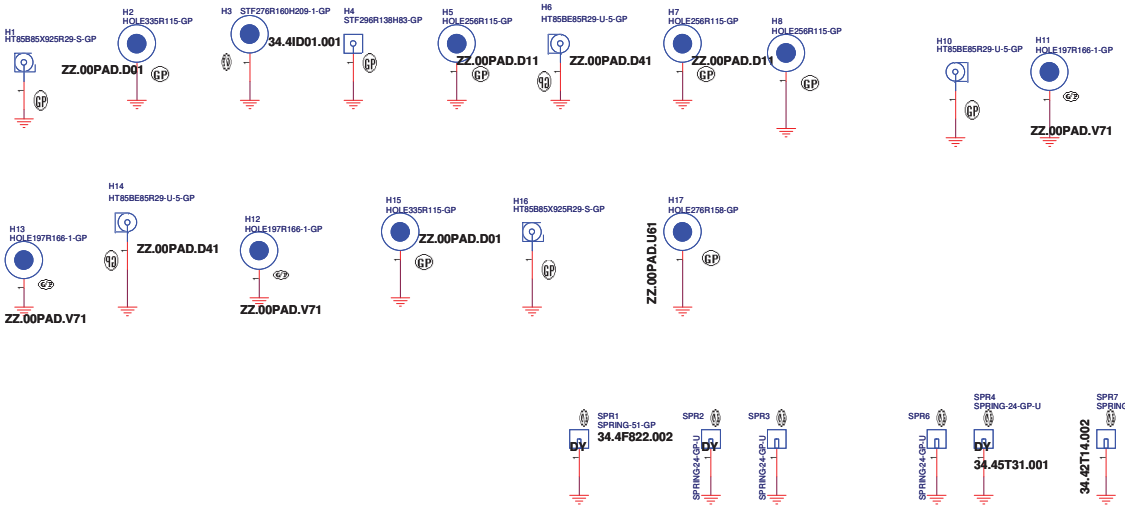
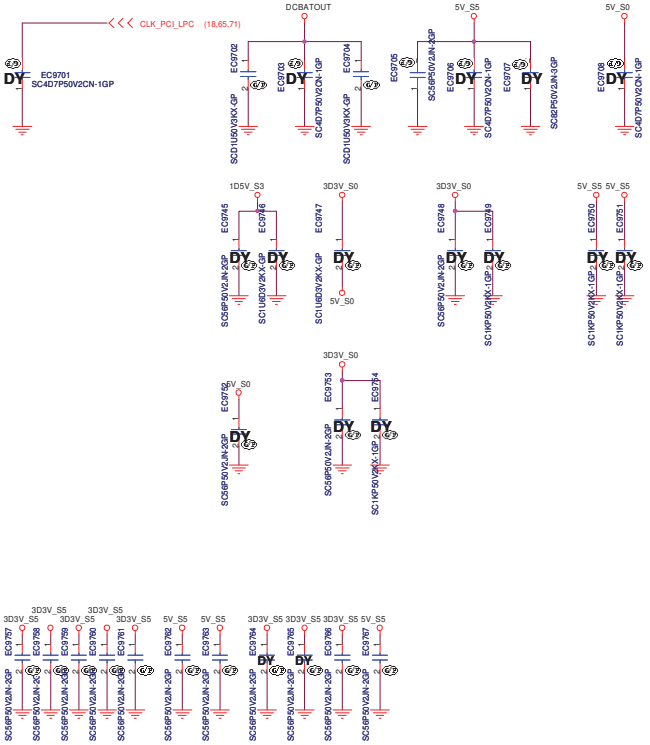
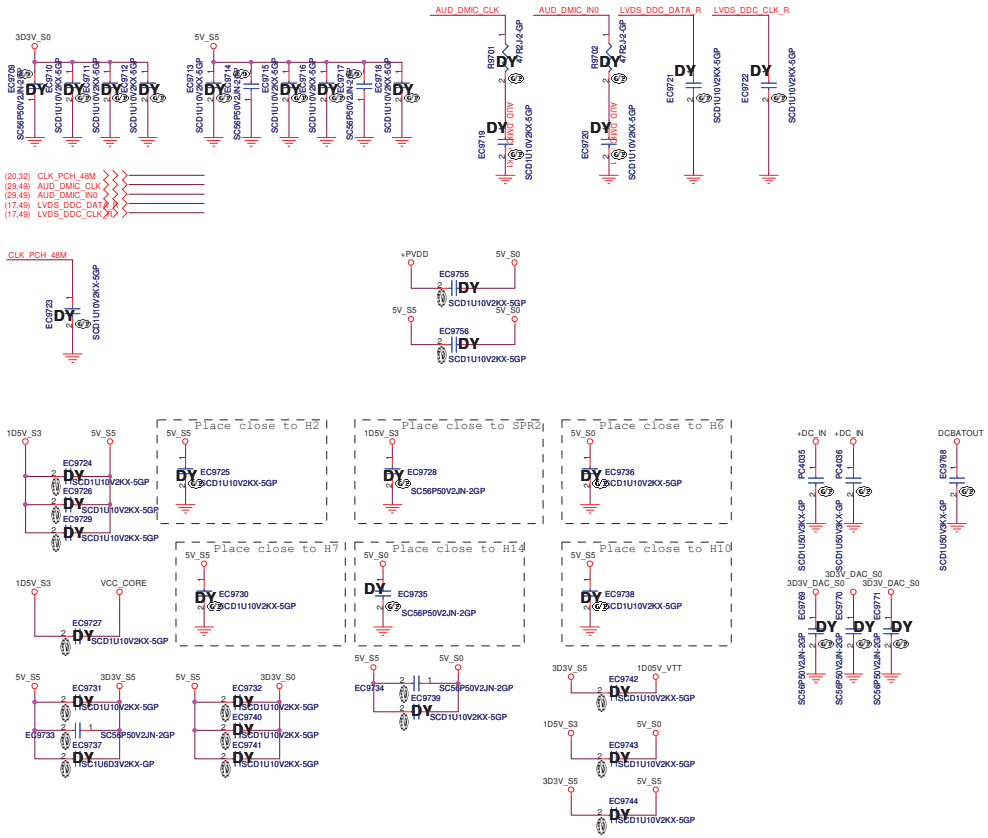


RF Request



EMI Request



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

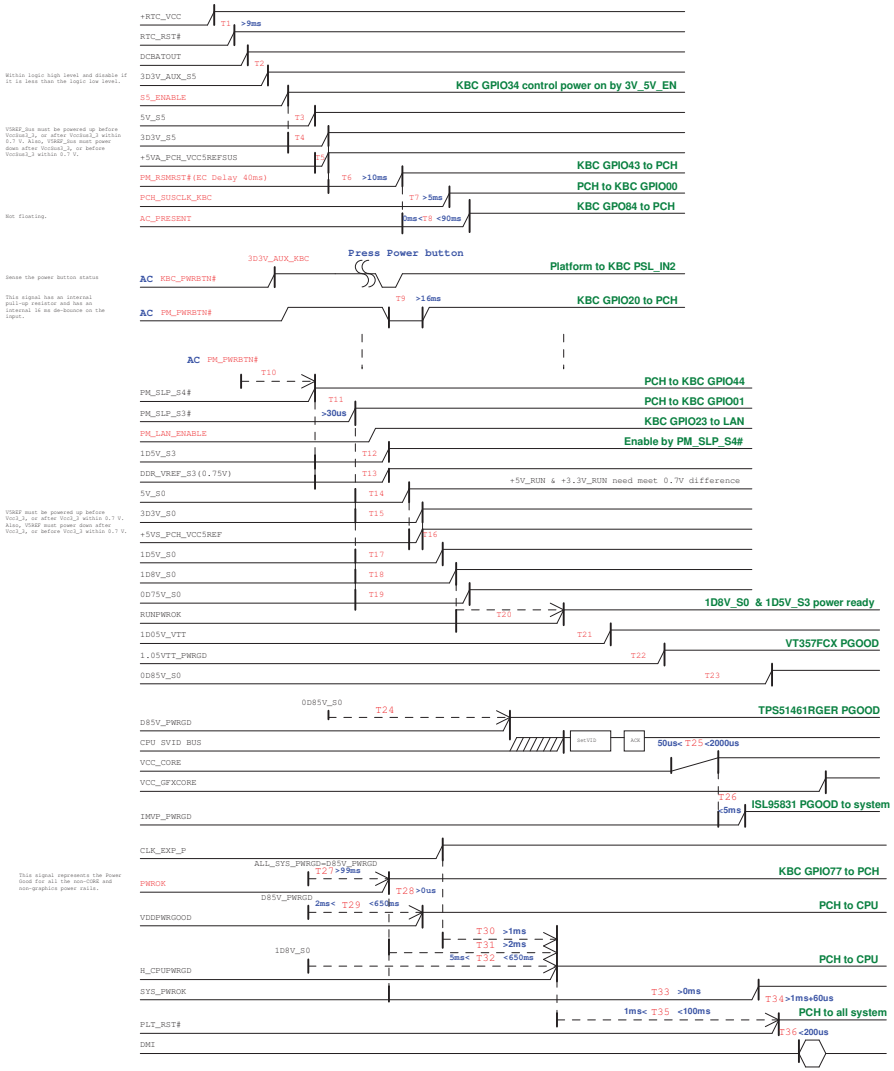
Size	Document Number	Rev
A2	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 97 of 104

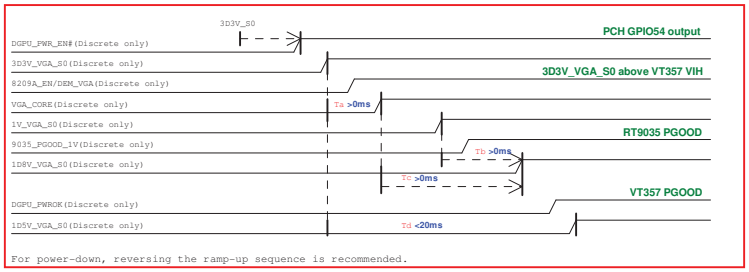
Huron River Platform Power Sequence

(AC mode)

red word: KBC GPIO



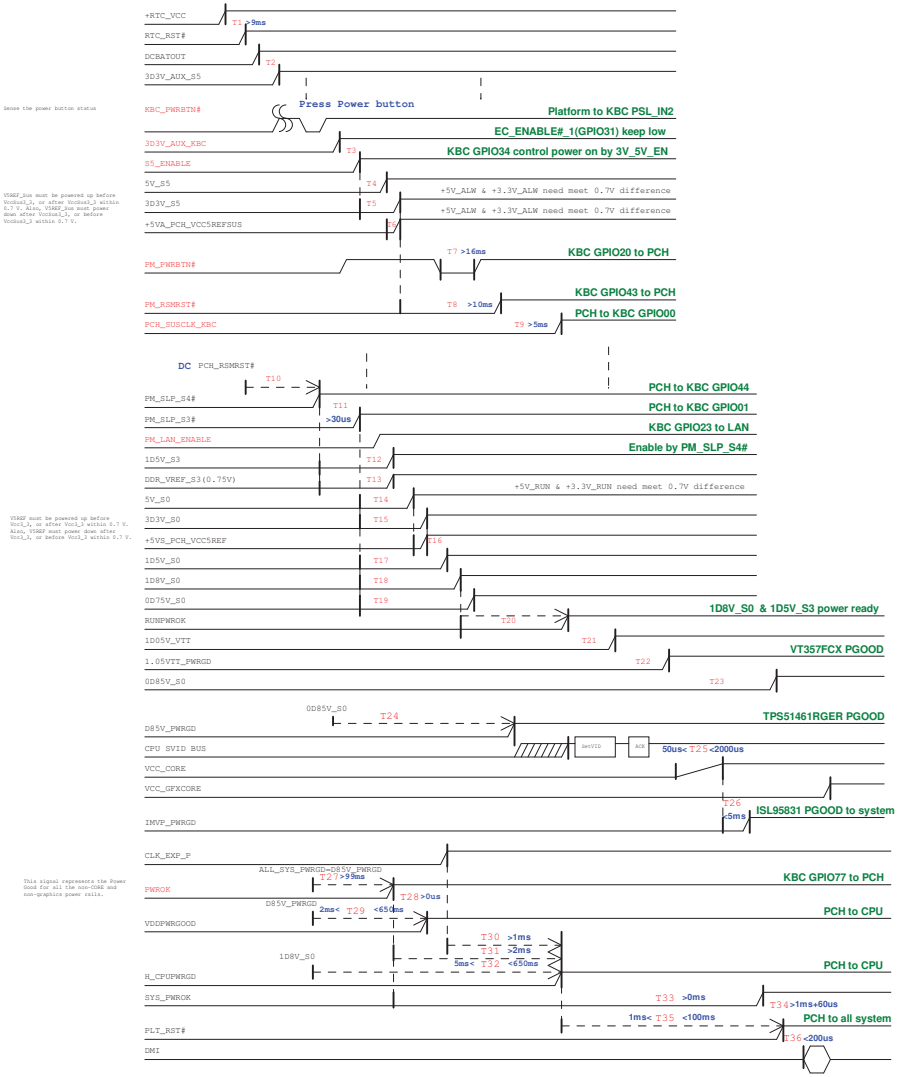
Robson XT Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

red word: KBC GPIO



<Core Design>

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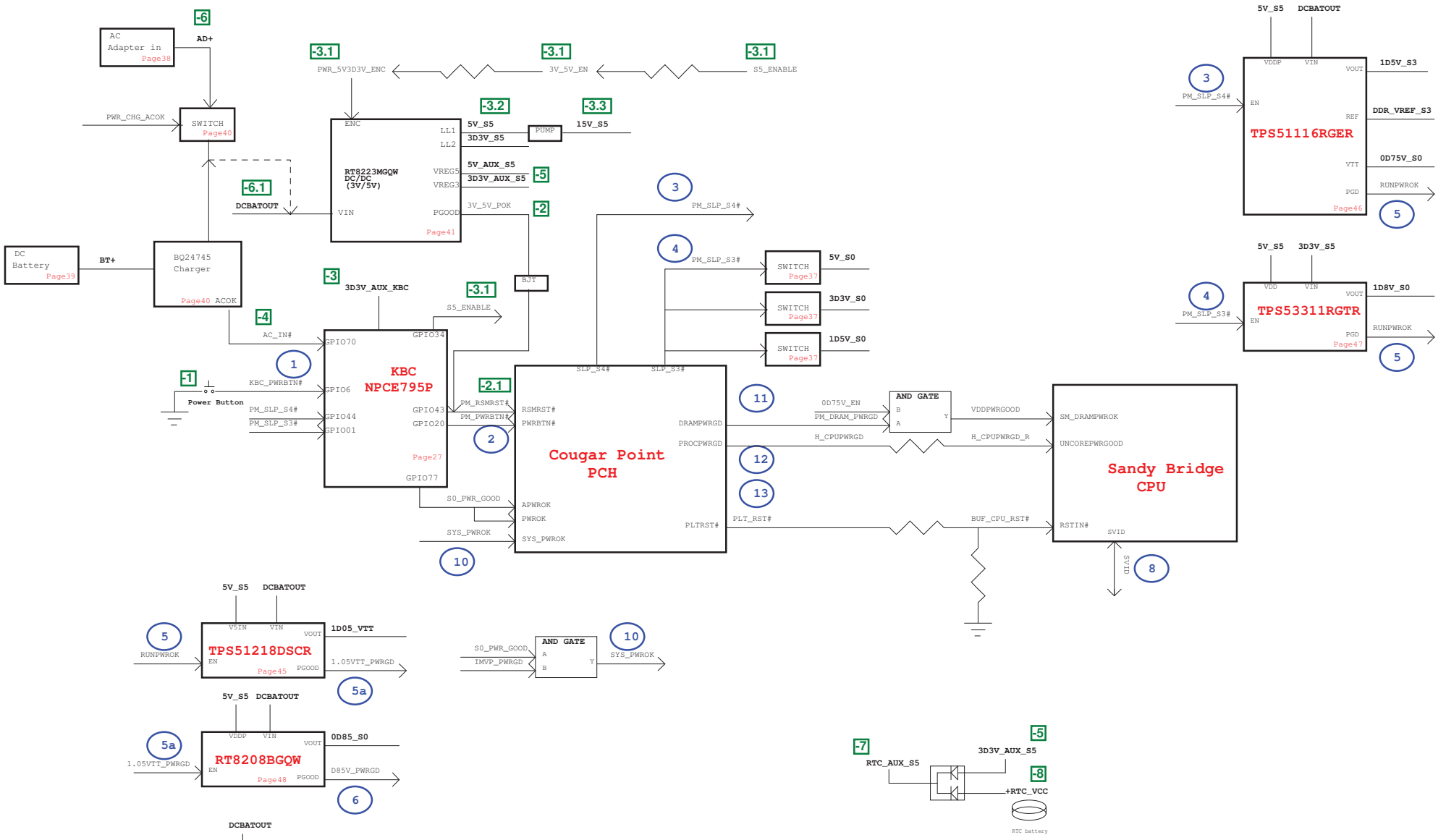
Title: Power Sequence

Size: A1 | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 26, 2010 | Sheet 9/9 of 9/9

Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13

<Core Design>

Wistron Corporation
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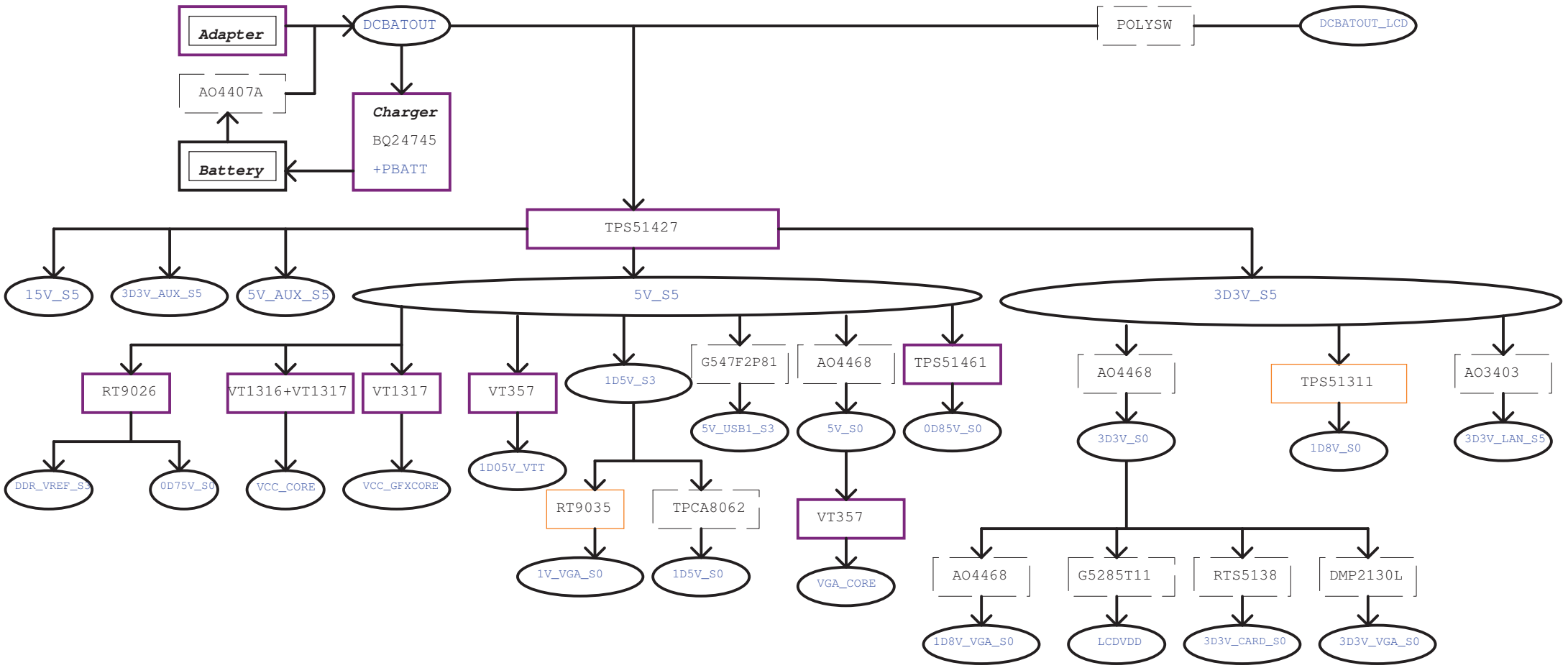
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Up Sequence Diagram

Size: A2 | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 04, 2011 | Sheet 99 of 104



Power Shape

Regulator	LDO	Switch

<Core Design>

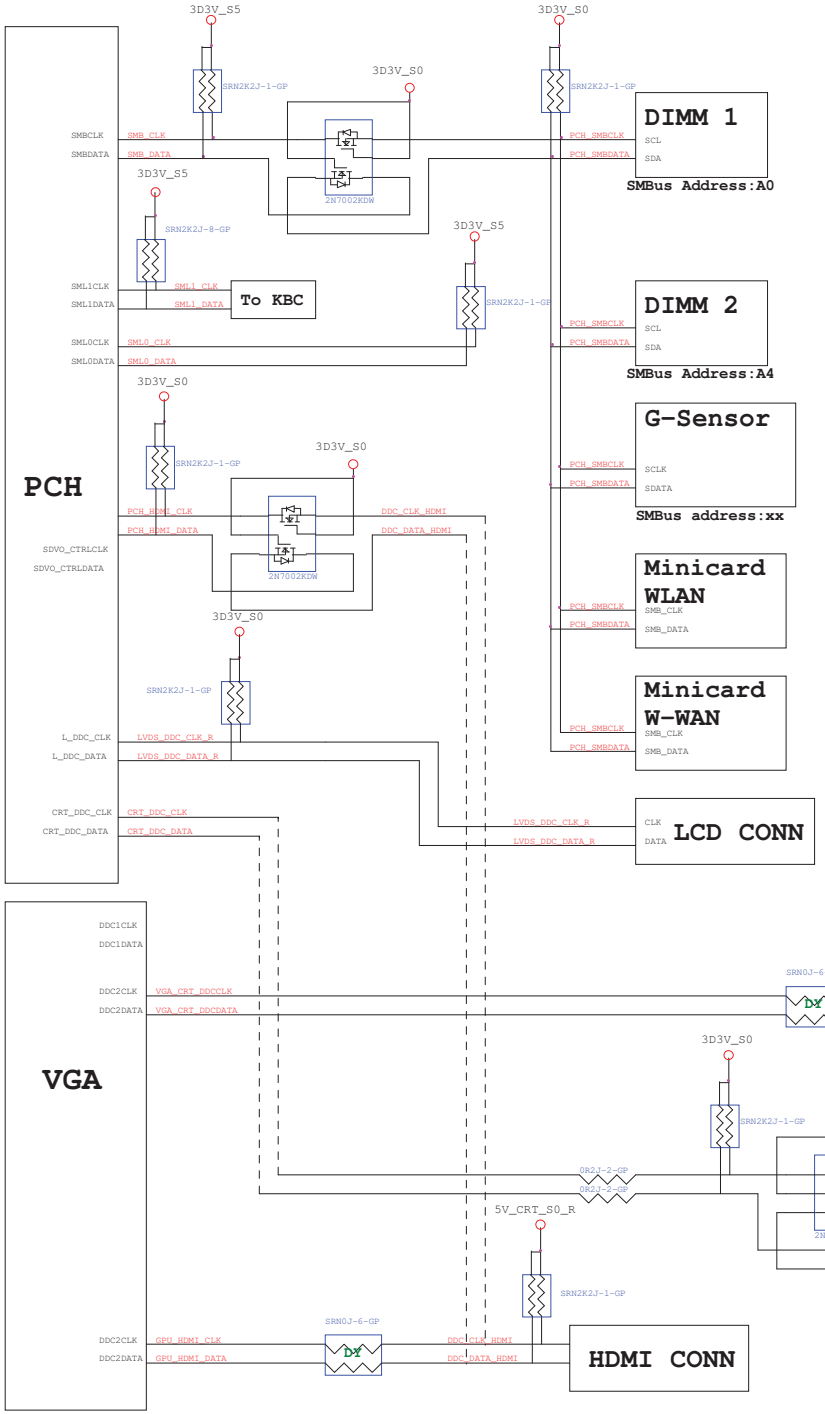
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power Block Diagram*

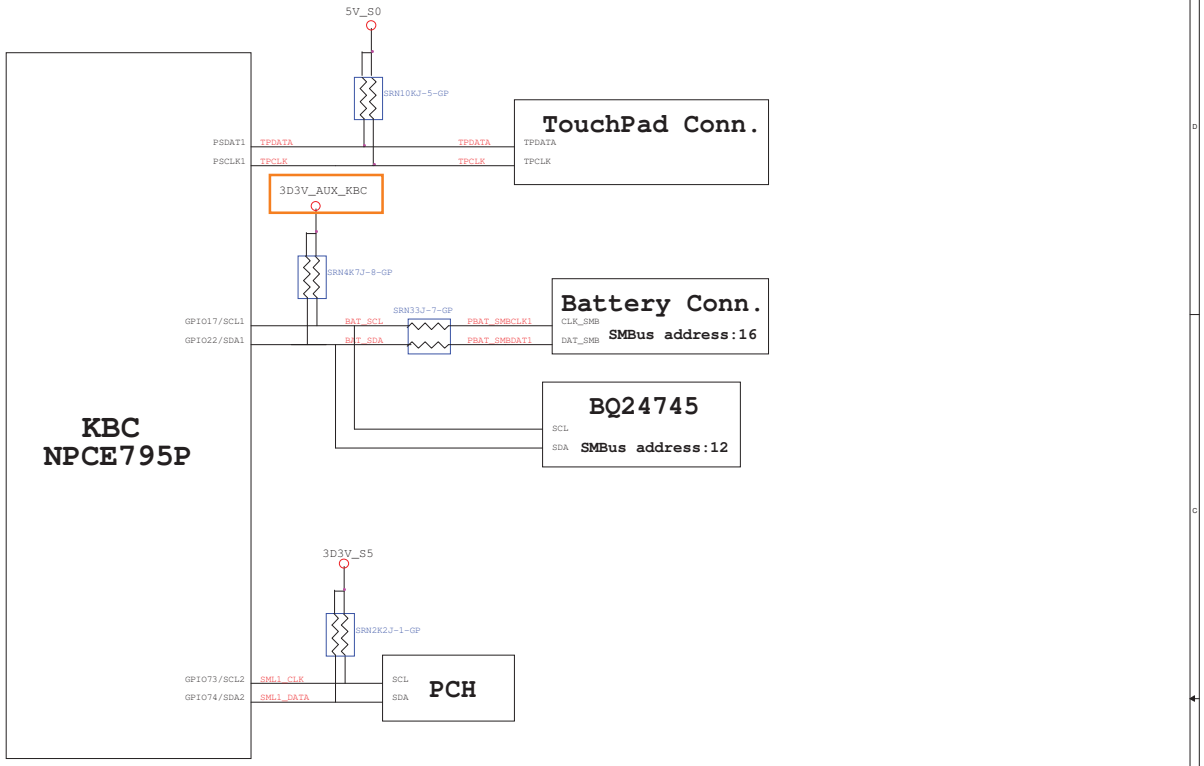
Size	Document Number	Rev
A3	*Nirvana 13*	*A00*

Date: Tuesday, January 04, 2011 Sheet 100 of 104

PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram
Size: A2
Document Number: Nirvana 13
Rev: A00
Date: Tuesday, January 04, 2011
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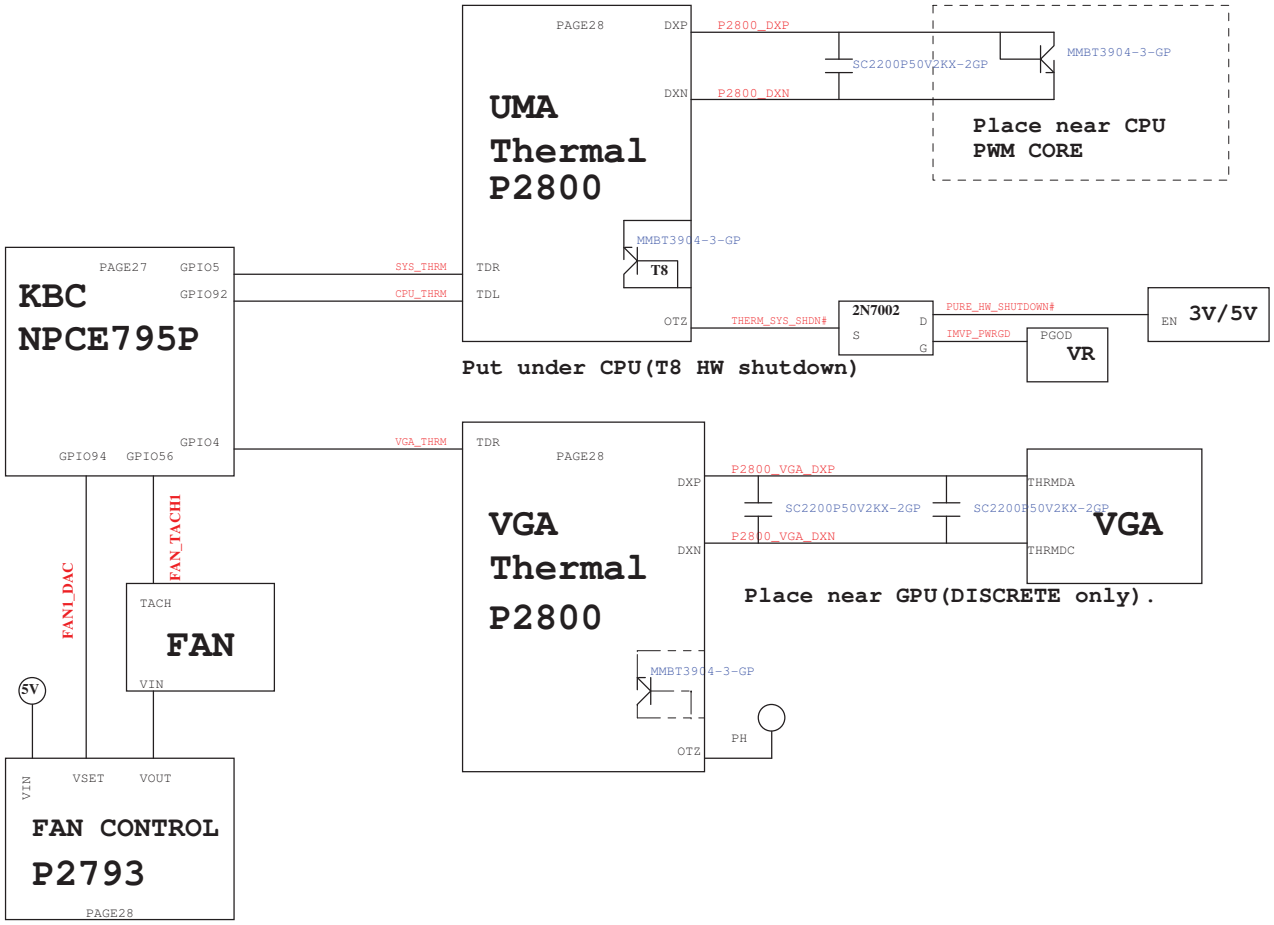
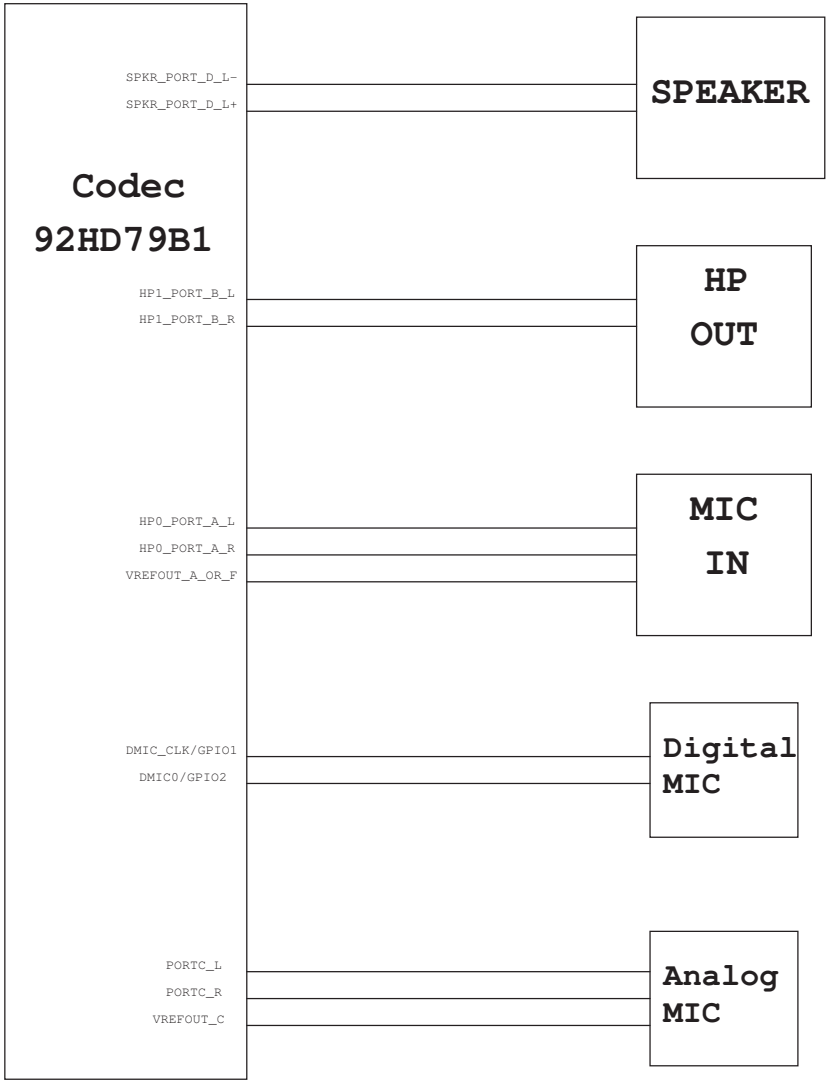
Thermal Block Diagram



Audio Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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Version	Date	Page	Function	Change Item
A00	20101222	40	Power	Power/Brian: Change PR4047 to 174k ohm from 121k ohm. Change PR4035 to 300k from 49.9k. Change PR4031 to 150k from 0 ohm. Change PR4034 to 0 ohm pad. Stuff PQ4003. Change PR4036 to 0 ohm pad. Stuff PQ4004. Change PR4037 to 76.8k ohm from 49.9k ohm. Change PR4032 to 0 ohm pad.
A00	20101222	42	Power	Power/Brian: Change PU4201 to 74.01316.F33.
A00	20101224	85	EE	Un-stuff THERMTRIP_VGA related circuit at A00 stage for fixed auto shut down issue.
A00	20101224		EE	Change all of 0ohm to short pad at X-build stage: 0402: R1404 R1405 R1503 R1504 R5010~R5012 R1807 R2301 R2306 R2307 R2308 R2404 R2405 R2735 R2737 R2758 R2759 R2760 R3614 R3710 R8210, R8506,R8509, L8703,L8704,L8705,L8706, R8316,R8601, PR9215 0603: R5803 R5804 R8507 Parallel resistor: RN1704 RN2010 RN2011 RN2012 RN2013 RN2014 RN2016 RN5117,RN5112,RN5113,RN5114,RN5115
A00	20101224	93	EE	Un-stuff 1D8V_S0_VGA_PG related circuit at X-Build stage.
A00	20101224		EE	Rename PRN3901 to PN3901. Rename PTC4101~PTC4103 to PT4101~PT4103. Rename LINEOUT1 to LOUT1. Rename PWRBTN1 to PWRBT1. Rename HALLSW1 to LID1.
A00	20101224	27	EE	Change R2724 to 47K from 33K.
A00	20101224	28	EE	If stuff P2800EA1 then must stuff R2803,R2804 C2805 but if stuff P28003B0 should be un-stuff.
A00	20101224	93	EE	Change PR9311,PR9327 to short pad at X-Build.
A00	20101227	32,42,46 62,64,65 70,84~86 88	EE	Change R3210,R3211,PR4217~PR4220,PR4254;PR4605,PR4607,PR4611,PR4602;R4908,R4909,R4919,R4920,R4903,R4910,R4913~R4916R4917,R4918; R5013~R5016; R6205; R6403,R6404;R6511;R6902;R7002;R8409;R8524;R8605 ;R8812,R8830to 0R 0402 pad.
A00	20101228	93	EE	Change PR9320 to short pad at X-Build.
A00	20101228	23	EE	0402 0R pad: R2301.
A00	20101228	27,62,82	EE	VGA_THRM change to USB_PWR_EN.
A00	20101228	27	EE	Change R2756,R2763,R2766 to 0R short pad.
A00	20101228	28	EE	Un-stuff U2805 G709T1UF related circuit and R2812 then stuff R2805 at X-Build.
A00	20101229	86	EE	Change C8601 to 10uF 0805 size.
A00	20101229	71	EE	DB1 change to ZZ.00PAD.Y41(solder mask type) and keep un-stuff at X-Build stage.
A00	20101229	27,62,82	EE	Rename USB_PWR_EN to USB3_PWR_ON. Remove R6205,R620. Remove R2809 and R8210. Connect USB3_PWR_ON from KBC to IOBD1.61.
A00	20101230	41,65,85	EE	Change PR4119 to 0R short pad. Change PR4114 to 0R short pad. Change R6406,R6405 to 0R short pad. Change PR4115 to 0R0603 short pad. Change PR4116 to 0R0603 short pad. Change R6510 to 0R 0603 pad. Change R8512 to 0R0603 short pad. Change PR4103,PR4104 to 0R0805 short pad.
A00	20101231	43	Power	Power/Brian: change PL4201 to 68.2415N.101 from 68.10110.10G.
A00	20101231	42,50,18 14,9,8	EE	Change PR4209,PR4212 to PN4201 10k array resistor. Change R5004,R5005 to RN5001 33 ohm array resistor. Merge R1804,R1806 to RN1804 22 ohm array resistor. Merge R1401,R1402 to RN1401 10k ohm array resistor. Merge R906,R907 to RN902 100 ohm array resistor. Merge R801,R802 to RN801 100 ohm array resistor.
A00	20110103	68,82	EE	Change R6801,R8201~R8203 to 1k.
A00	20110103	41	Power	Change PR4106 to 0R0603 short pad.
A00	20110104	5	EE	merge R512,R514 to RN502 1k array resistor.
A00	20110104	8	EE	Swap VCC_CORE to RN801.4 and VCCSENSE to RN801.1.
A00	20110104	9	EE	Swap VCC_GFXCORE to RN902.1 and VCC_AXG_SENSE to RN902.4.
A00	20110104	14	EE	Change RN1401 to 0R short pad.
A00	20110104	15	EE	Change R1502 to 0R0402 short pad.
A00	20110104	17	EE	Merge RN1701,RN1706 to RN1703 2.2k array resistor.
A00	20110104	22	EE	Merge RN2201,R2222,R2223 to 10k array resistor.

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

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A00	20110104	22	EE	Merge RN2215,R2216 to RN2201 10k array resistor.
A00	20110104	32,49,57 64,65	EE	Remove TR3201,TR4902,R5718,R5719,TR6401,TR6501.
A00	20110104	68,69	EE	Change R6804,R6806,R6808,R6810,R6906 to 620 ohm 5%.
A00	20110104	82	EE	Merge R8201~R8203 to RN8201 1k array resistor.
A00	20110105	85	EE	Change L8507 to 0 ohm short pad, un-stuff C8526,C8527,Un-stuff C8501 C8502 C8504 C8506 C8511.
A00	20110105	93	EE	Change PR9316 to 10k ohm (follow the standard schematics).
A00	20110105	85	EE	Un-stuff C8536,C8533,C8534 and change L8501 to 0 ohm short pad.
A00	20110106	93	Power	Un-stuff PC9317.
A00	20110107	51	EE	Remove RN5112~RN5115.
A00	20110107	68,69	EE	Change R6804,R6806,R6808,R6810,R6906 to 1k ohm 5%.
A00	20110107	49	EE	Change F4902 to 0603 0 ohm.
A00	20110110	21	EE	Merge R2115,R2116 to RN2101.
A00	20110110	41	Power	Change PG4110,PG4112,PG4114~PG4119,PG4122,PG4126,PG4129,PG4131,PG4133,PG4135~PG4138,PG4140,PG4142,PG4102~PG4109,PG4111,PG4113,PG4118,PG4120,PG4123,PG4101,PG4127,PG4130,PG4132,PG4134, PG4139,PG4141 to ZZ.CLOSE.001.
A00	20110111	49,51	EE	Change R4908,R4909,R4903,R4910,R4913~R4916 R4917,R4918 to 0R 0402 reisstors. Change RN5112~RN5115 to 0R array resistors. Change RN5117 to 0 ohm resistor.
A00	20110112	20	EE	Change C2007,C2008 to 15pF from 12pF base on vendor's report.
A00	20110112	85	EE	Change C8524,C8525 to 18pF from 12pF base on vendor's report.
A00	20110113	8,9	EE	Change RN801,RN902 to 100 ohm 1% (66.10156.04L).
A00	20110113	22	EE	Combine PCH_TEMP_ALERT#,MFG_MODE to RN2202. Combine EC_SCI#,DGPU_HPD_INTR# to RN2204.
A00	20110113	5,8,14, 21,42,17 18,82	EE	Swap RN502,RN801,RN1401,RN1804,RN2101,PN4201, RN8201 base on swap report. Swap RN1703.7,RN1703.5. swap RN1703.8,RN1703.6
A00	20110117	42	EE	Swap PN4201 base on the swap report.
A00	20110118	8	EE	Change C823, C824, C825 to 22uF from 10uF (0805 size). Reserve C846~C848 22uF (0805 size).
A00	20110118	51	EE	Remove RN5117 for PCH_HDMI_CLK and PCH_HDMI_DATA.

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

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