Lenovo IdeaPad B570 Z570 V570

Sandy Bridge

Intel PCH Cougar Point

2011-01-19

REV : XXX

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX

BOM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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Size A3	Document Number LZ57	Rev -1
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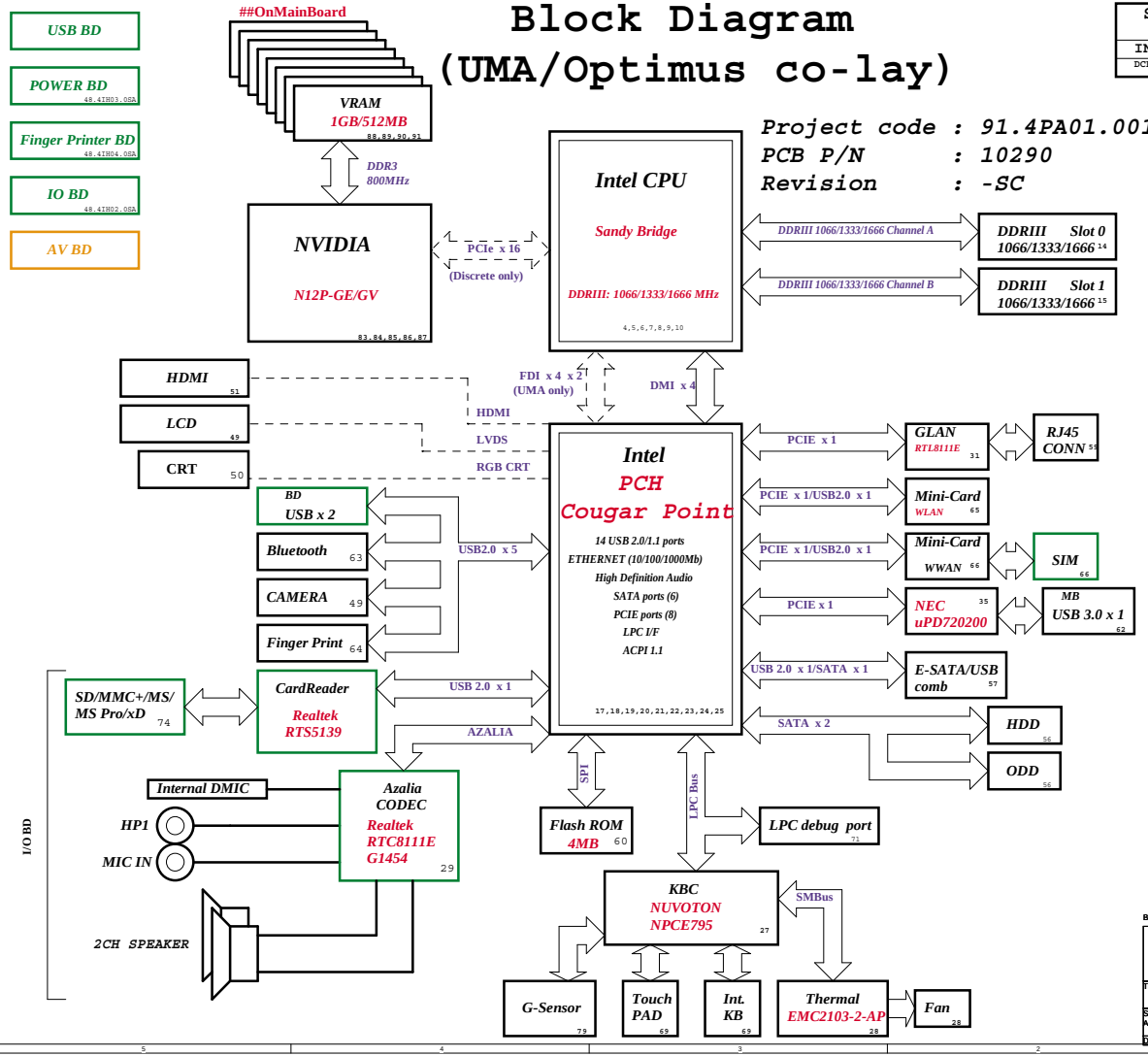
Block Diagram (UMA/Optimus co-lay)

Project code : 91.4PA01.001
PCB P/N : 10290
Revision : -SC



SYSTEM DC/DC RT8208B 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6111CQHC 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183AQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6111C 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

LDO RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S5
3D3V_S0	1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ ~~10 kΩ weak pull-up resistor~~
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I2 C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

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PCI EXPRESS* - GRAPHICS

DMI

Intel(R) FDI

eDP

62.10055.321

1D05V_VTT

R401 1 — 24D9R2F-L-GP

R402 1 — 24D9R2F-L-GP — DY

R403 1 — Do Not Stuff

DP_COMP — A18

eDP_HPD — A17 — B16

PEG_ICOMPI — J22 — PEG_IRCOMP_R

PEG_ICOMPO — J21

PEG_RCOMPO — H22

PEG_RXN[0..15] — PEG_RXN[0..15] 83

PEG_RXP[0..15] — PEG_RXP[0..15] 83

PEG_TXN[0..15] — PEG_TXN[0..15] 83

PEG_TXP[0..15] — PEG_TXP[0..15] 83

PEG_RX#0	K33	PEG_RXN15	PEG_TX#0	M29	PEG_C_TXN15	C401	PEG_TXN15
PEG_RX#1	M35	PEG_RXN14	PEG_TX#1	M32	PEG_C_TXN14	C402	PEG_TXN14
PEG_RX#2	L34	PEG_RXN13	PEG_TX#2	M31	PEG_C_TXN13	C403	PEG_TXN13
PEG_RX#3	J35	PEG_RXN12	PEG_TX#3	L32	PEG_C_TXN12	C404	PEG_TXN12
PEG_RX#4	J32	PEG_RXN11	PEG_TX#4	L29	PEG_C_TXN11	C405	PEG_TXN11
PEG_RX#5	H34	PEG_RXN10	PEG_TX#5	K31	PEG_C_TXN10	C406	PEG_TXN10
PEG_RX#6	H31	PEG_RXN9	PEG_TX#6	K28	PEG_C_TXN9	C407	PEG_TXN9
PEG_RX#7	G33	PEG_RXN8	PEG_TX#7	J30	PEG_C_TXN8	C408	PEG_TXN8
PEG_RX#8	G30	PEG_RXN7	PEG_TX#8	J28	PEG_C_TXN7	C409	PEG_TXN7
PEG_RX#9	F35	PEG_RXN6	PEG_TX#9	H29	PEG_C_TXN6	C410	PEG_TXN6
PEG_RX#10	E34	PEG_RXN5	PEG_TX#10	G27	PEG_C_TXN5	C411	PEG_TXN5
PEG_RX#11	E32	PEG_RXN4	PEG_TX#11	F29	PEG_C_TXN4	C412	PEG_TXN4
PEG_RX#12	D33	PEG_RXN3	PEG_TX#12	F27	PEG_C_TXN3	C413	PEG_TXN3
PEG_RX#13	D31	PEG_RXN2	PEG_TX#13	D28	PEG_C_TXN2	C414	PEG_TXN2
PEG_RX#14	B33	PEG_RXN1	PEG_TX#14	F26	PEG_C_TXN1	C415	PEG_TXN1
PEG_RX#15	C32	PEG_RXN0	PEG_TX#15	E25	PEG_C_TXN0	C416	PEG_TXN0
PEG_RX0	J33	PEG_RXP15	PEG_TX0	M28	PEG_C_TXP15	C417	PEG_TXP15
PEG_RX1	L35	PEG_RXP14	PEG_TX1	M33	PEG_C_TXP14	C418	PEG_TXP14
PEG_RX2	K34	PEG_RXP13	PEG_TX2	M30	PEG_C_TXP13	C419	PEG_TXP13
PEG_RX3	H35	PEG_RXP12	PEG_TX3	L31	PEG_C_TXP12	C420	PEG_TXP12
PEG_RX4	H32	PEG_RXP11	PEG_TX4	L28	PEG_C_TXP11	C421	PEG_TXP11
PEG_RX5	G34	PEG_RXP10	PEG_TX5	K30	PEG_C_TXP10	C422	PEG_TXP10
PEG_RX6	G31	PEG_RXP9	PEG_TX6	K27	PEG_C_TXP9	C423	PEG_TXP9
PEG_RX7	F33	PEG_RXP8	PEG_TX7	J29	PEG_C_TXP8	C424	PEG_TXP8
PEG_RX8	F30	PEG_RXP7	PEG_TX8	J27	PEG_C_TXP7	C425	PEG_TXP7
PEG_RX9	E35	PEG_RXP6	PEG_TX9	H28	PEG_C_TXP6	C426	PEG_TXP6
PEG_RX10	E33	PEG_RXP5	PEG_TX10	G28	PEG_C_TXP5	C427	PEG_TXP5
PEG_RX11	E32	PEG_RXP4	PEG_TX11	E28	PEG_C_TXP4	C428	PEG_TXP4
PEG_RX12	D34	PEG_RXP3	PEG_TX12	F28	PEG_C_TXP3	C429	PEG_TXP3
PEG_RX13	E31	PEG_RXP2	PEG_TX13	D27	PEG_C_TXP2	C430	PEG_TXP2
PEG_RX14	C33	PEG_RXP1	PEG_TX14	E26	PEG_C_TXP1	C431	PEG_TXP1
PEG_RX15	B32	PEG_RXP0	PEG_TX15	D25	PEG_C_TXP0	C432	PEG_TXP0

19 DMI_TXN[3:0]	DMI_TXN0 B27	DMI_RX#0	DMI_TX#0
	DMI_TXN1 B25	DMI_RX#1	DMI_TX#1
	DMI_TXN2 A25	DMI_RX#2	DMI_TX#2
	DMI_TXN3 B24	DMI_RX#3	DMI_TX#3
19 DMI_TXP[3:0]	DMI_TXP0 B28	DMI_RX0	DMI_TX0
	DMI_TXP1 B26	DMI_RX1	DMI_TX1
	DMI_TXP2 A24	DMI_RX2	DMI_TX2
	DMI_TXP3 B23	DMI_RX3	DMI_TX3
19 DMI_RXN[3:0]	DMI_RXN0 G21	DMI_TX#0	DMI_RX#0
	DMI_RXN1 E22	DMI_TX#1	DMI_RX#1
	DMI_RXN2 F21	DMI_TX#2	DMI_RX#2
	DMI_RXN3 D21	DMI_TX#3	DMI_RX#3
19 DMI_RXP[3:0]	DMI_RXP0 G22	DMI_TX0	DMI_RX0
	DMI_RXP1 D22	DMI_TX1	DMI_RX1
	DMI_RXP2 F20	DMI_TX2	DMI_RX2
	DMI_RXP3 C21	DMI_TX3	DMI_RX3
19 FDI_TXN[7:0]	FDI_TXN0 A21	FDI0_TX#0	FDI1_TX#0
	FDI_TXN1 H19	FDI0_TX#1	FDI1_TX#1
	FDI_TXN2 E19	FDI0_TX#2	FDI1_TX#2
	FDI_TXN3 F18	FDI0_TX#3	FDI1_TX#3
	FDI_TXN4 B21		
	FDI_TXN5 C20		
	FDI_TXN6 D18		
	FDI_TXN7 E17		
19 FDI_TXP[7:0]	FDI_TXP0 A22	FDI0_TX0	FDI1_TX0
	FDI_TXP1 G19	FDI0_TX1	FDI1_TX1
	FDI_TXP2 E20	FDI0_TX2	FDI1_TX2
	FDI_TXP3 G18	FDI0_TX3	FDI1_TX3
	FDI_TXP4 B20		
	FDI_TXP5 C19		
	FDI_TXP6 D19		
	FDI_TXP7 F17		
19 FDI_FSYNC0	J18	FDI0_FSYNC	
19 FDI_FSYNC1	J17	FDI1_FSYNC	
19 FDI_INT	H20	FDI_INT	
19 FDI_LSYNC0	J19	FDI0_LSYNC	
19 FDI_LSYNC1	H17	FDI1_LSYNC	
		EDP_COMPIO	
		EDP_ICOMPO	
		EDP_HPD	
	C15	EDP_AUX	
	D15	EDP_AUX#	
	C17	EDP_TX0	
	E16	EDP_TX1	
	C16	EDP_TX2	
	G15	EDP_TX3	
	C18	EDP_TX#0	
	E16	EDP_TX#1	
	D16	EDP_TX#2	
	F15	EDP_TX#3	

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Title	CPU (PCIE/DMI/FDI)		
Size A3	Document Number LZ57		Rev -1
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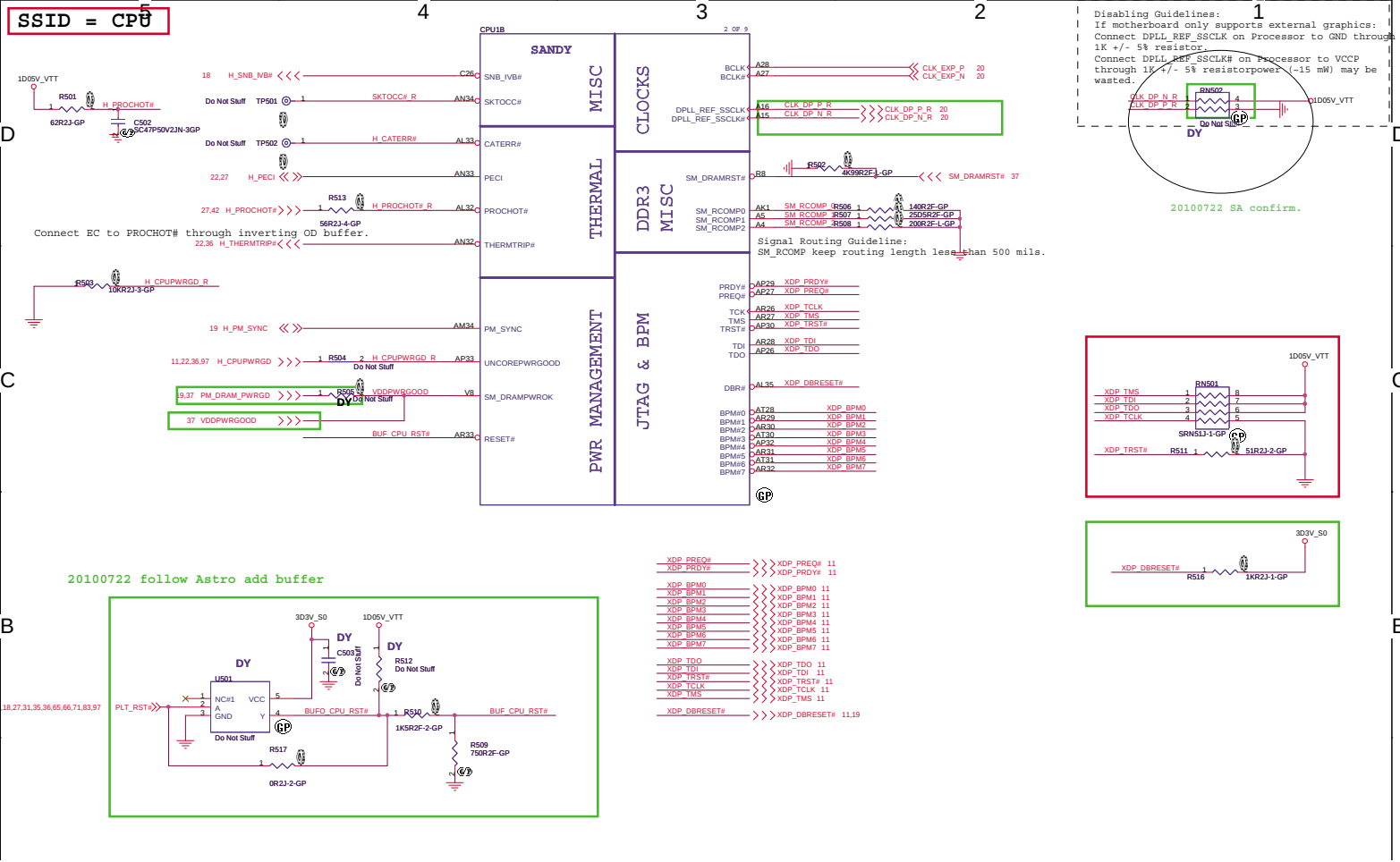
SSID = CPU



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Title	CPU (THERMAL/CLOCK/PM)	
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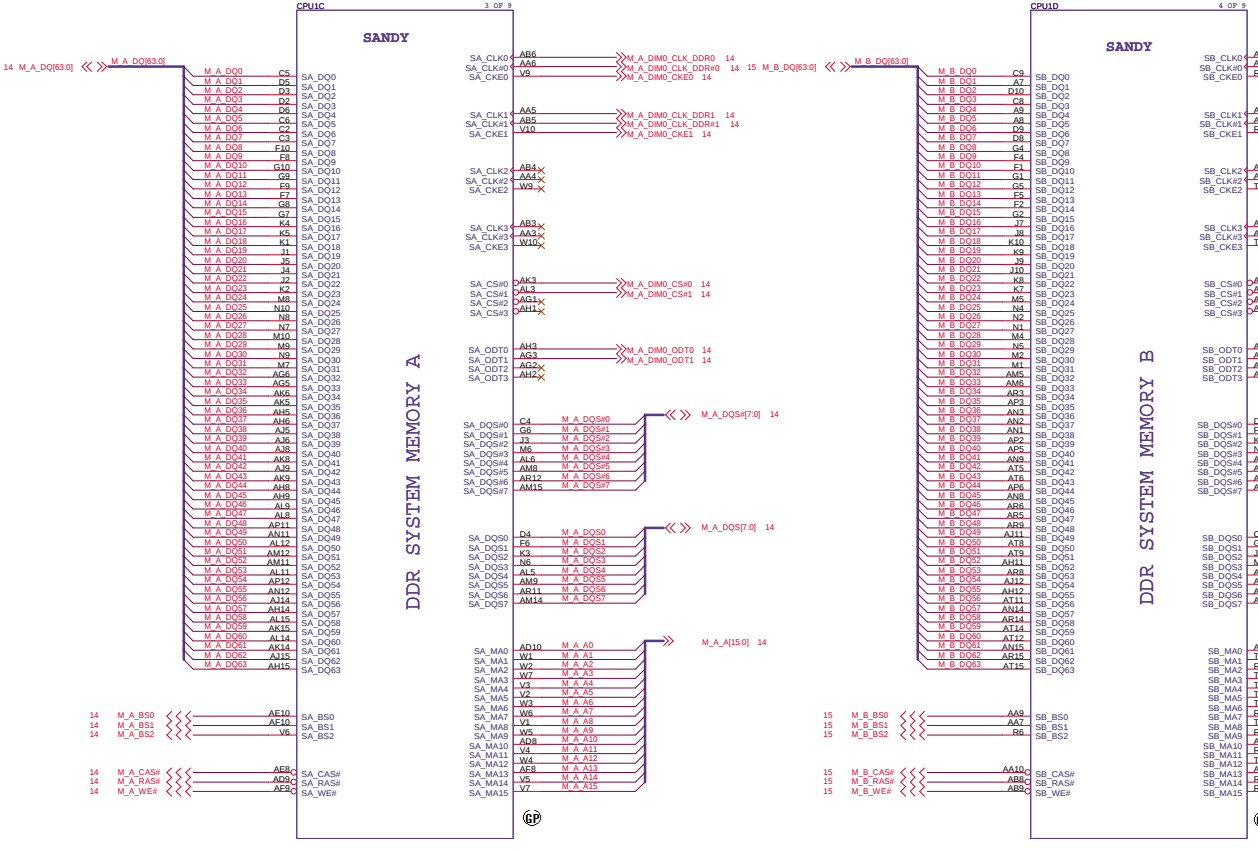
SSID = CPU



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Title	CPU (DDR)	
Size A3	Document Number LZ57	Rev -1
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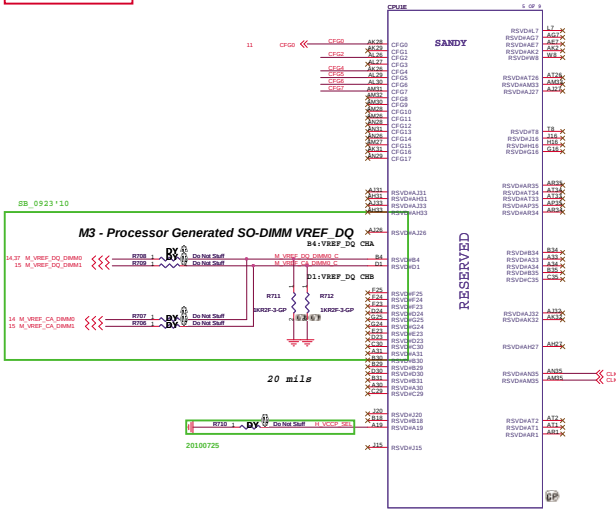
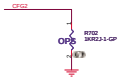
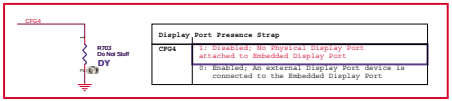
SSID = CPU

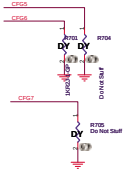




PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled , function 2 disabled
	01: Reserved - (Device 1 function 1 disabled , function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

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Title: CPU (RESERVED)

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SSID = CPU

POWER

CPU1F

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SANDY

PROCESSOR CORE POWER

53A

VCC_CORE

C801 SC10U6D3V5K-1GP
C802 SC10U6D3V5K-1GP
C803 SC10U6D3V5K-1GP
C804 SC10U6D3V5K-1GP
C811 SC10U6D3V5K-1GP
C815 SC10U6D3V5K-1GP
C817 SC10U6D3V5K-1GP
C818 SC10U6D3V5K-1GP
C819 SC10U6D3V5K-1GP
C820 SC10U6D3V5K-1GP
C816 SC10U6D3V5K-1GP
C821 SC10U6D3V5K-1GP
C822 SC10U6D3V5K-1GP
C823 SC10U6D3V5K-1GP
C824 SC10U6D3V5K-1GP
C825 SC10U6D3V5K-1GP
C826 SC10U6D3V5K-1GP
C827 SC10U6D3V5K-1GP
C837 SC10U6D3V5K-1GP
C836 SC10U6D3V5K-1GP
C835 SC10U6D3V5K-1GP
C834 SC10U6D3V5K-1GP
C833 SC10U6D3V5K-1GP
C832 SC10U6D3V5K-1GP
C831 SC10U6D3V5K-1GP
C828 SC10U6D3V5K-1GP

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCC_CORE

CORE SUPPLY

AG35 VCC
AG34 VCC
AG33 VCC
AG32 VCC
AG31 VCC
AG30 VCC
AG29 VCC
AG28 VCC
AG27 VCC
AG26 VCC
AE35 VCC
AE34 VCC
AE33 VCC
AE32 VCC
AE31 VCC
AE30 VCC
AE29 VCC
AE28 VCC
AE27 VCC
AE26 VCC
AD35 VCC
AD34 VCC
AD33 VCC
AD32 VCC
AD31 VCC
AD30 VCC
AD29 VCC
AD28 VCC
AD27 VCC
AD26 VCC
AC35 VCC
AC34 VCC
AC33 VCC
AC32 VCC
AC31 VCC
AC30 VCC
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AC28 VCC
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AC26 VCC
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AA34 VCC
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AA29 VCC
AA28 VCC
AA27 VCC
AA26 VCC
Y35 VCC
Y34 VCC
Y33 VCC
Y32 VCC
Y31 VCC
Y30 VCC
Y29 VCC
Y28 VCC
Y27 VCC
Y26 VCC
V35 VCC
V34 VCC
V33 VCC
V32 VCC
V31 VCC
V30 VCC
V29 VCC
V28 VCC
V27 VCC
V26 VCC
U35 VCC
U34 VCC
U33 VCC
U32 VCC
U31 VCC
U30 VCC
U29 VCC
U28 VCC
U27 VCC
U26 VCC
R35 VCC
R34 VCC
R33 VCC
R32 VCC
R31 VCC
R30 VCC
R29 VCC
R28 VCC
R27 VCC
R26 VCC
P35 VCC
P34 VCC
P33 VCC
P32 VCC
P31 VCC
P30 VCC
P29 VCC
P28 VCC
P27 VCC
P26 VCC

PEG AND DDR

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

C805 SC10U6D3V5K-1GP
C806 Do Not Stuff
C807 SC10U6D3V5K-1GP
C808 Do Not Stuff
C809 SC10U6D3V5K-1GP
C810 Do Not Stuff
C838 SC10U6D3V5K-1GP
C839 Do Not Stuff
C840 SC10U6D3V5K-1GP
C841 SC10U6D3V5K-1GP

VCCIO AH13
VCCIO AH10
VCCIO AG10
VCCIO AC10
VCCIO Y10
VCCIO U10
VCCIO P10
VCCIO L10
VCCIO J14
VCCIO J13
VCCIO J12
VCCIO J11
VCCIO H14
VCCIO H12
VCCIO H11
VCCIO G14
VCCIO G13
VCCIO G12
VCCIO F14
VCCIO F13
VCCIO F12
VCCIO F11
VCCIO E14
VCCIO E12
VCCIO E11
VCCIO D14
VCCIO D13
VCCIO D12
VCCIO D11
VCCIO C14
VCCIO C13
VCCIO C12
VCCIO C11
VCCIO B14
VCCIO B12
VCCIO A14
VCCIO A13
VCCIO A12
VCCIO A11
VCCIO J23

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

C812 Do Not Stuff
C813 SC10U6D3V5K-1GP
C814 SC10U6D3V5K-1GP
C829 SC10U6D3V5K-1GP
C830 SC10U6D3V5K-1GP
C842 SC10U6D3V5K-1GP
C843 SC10U6D3V5K-1GP
C844 SC10U6D3V5K-1GP
C845 Do Not Stuff

R804 need to close to CPU

1D05V_VTT

H_CPU_SVIDDAT R804 1 130R2F-1-GP

S-HS_20100610 V1.0

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 1 43R2J-GP VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT H_CPU_SVIDDAT 42

SENSE LINES

VCC_CORE

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 VCCSENSE 42
VSS_SENSE AJ34 VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 VCCIO_SENSE 45
VSSIO_SENSE A10 VSSIO_SENSE 45

BOM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 8 of 102

SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

POWER

CPU1G — SANDY — GRAPHICS — 7 OF 9

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 Do Not Stuff; C902 SC10U6D3V5KX-1GP; C903 Do Not Stuff; C904 SC10U6D3V5KX-1GP; C905 SC10U6D3V5KX-1GP; C906 SC10U6D3V5KX-1GP; C907 SC10U6D3V5KX-1GP; C908 SC10U6D3V5KX-1GP; C918 SC10U6D3V5KX-1GP; C919 SC10U6D3V5KX-1GP; C920 SC10U6D3V5KX-1GP; C921 SC10U6D3V5KX-1GP

VAXG: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17

SENSE LINES

VAXG_SENSE — AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE — AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF — AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

VDDQ: AE7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

C909 SC10U6D3V5KX-1GP; C910 SC10U6D3V5KX-1GP; C911 SC10U6D3V5KX-1GP; C912 Do Not Stuff; C913 Do Not Stuff; C914 SC10U6D3V5KX-1GP

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

C916 Do Not Stuff; C915 SC10U6D3V5KX-1GP; C917 SC10U6D3V5KX-1GP; TC903 ST330U2VDM-4-GP

VCCSA: M27, M26, L26, J26, J25, J24, H26, H25

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0

R902 100R2F-L1-GP-U — Notice:pull-high 100k or 10k

MISC

VCCSA_SENSE — H23 — VCCSA_SENSE — VCCSA_SENSE 48

FC_C22 — C22 — H_FC_C22 — H_FC_C22 48
VCCSA_VID1 — C24 — VCCSA_SEL — VCCSA_SEL 48

RN901 SRN1KJ-7-GP

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

VCCPLL: B6, A6, A2

TC902 ST330U2VDM-4-GP; C923 SC10U6D3V5KX-1GP; C922 SC10U6D3V5KX-1GP; C924 Do Not Stuff

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

Close to CPU

VCC_GFXCORE — R906 100R2F-L1-GP-U — VCC_AXG_SENSE — VSS_AXG_SENSE — R907 100R2F-L1-GP-U

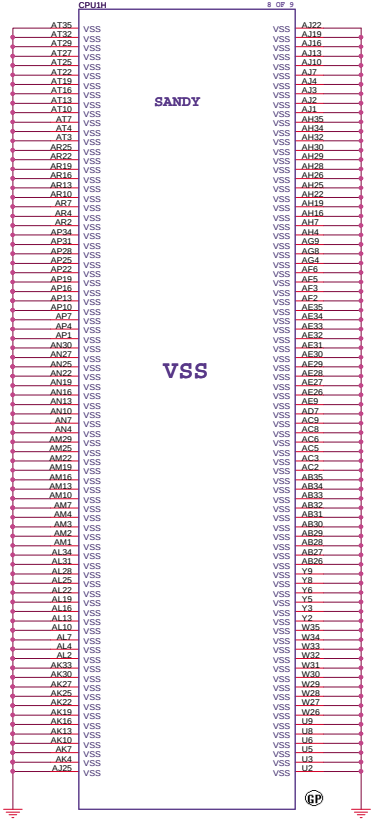
S-HR_20100609 V1.0

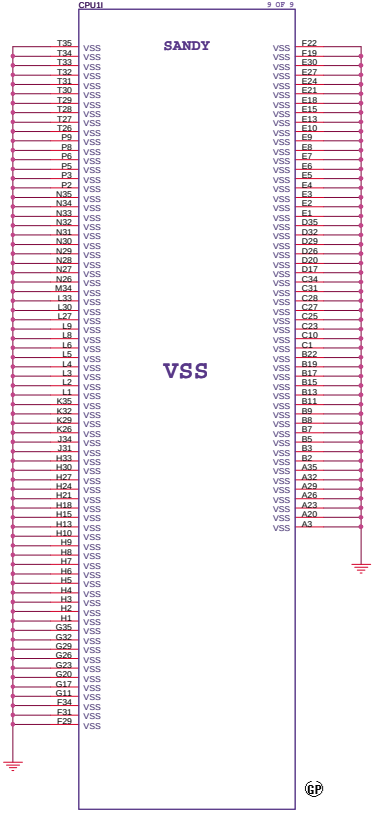
20100721 standard schematic update

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (VCC_GFXCORE)
Size A3 / Document Number	LZ57
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 9 of 102

SSID = CPU





BOM

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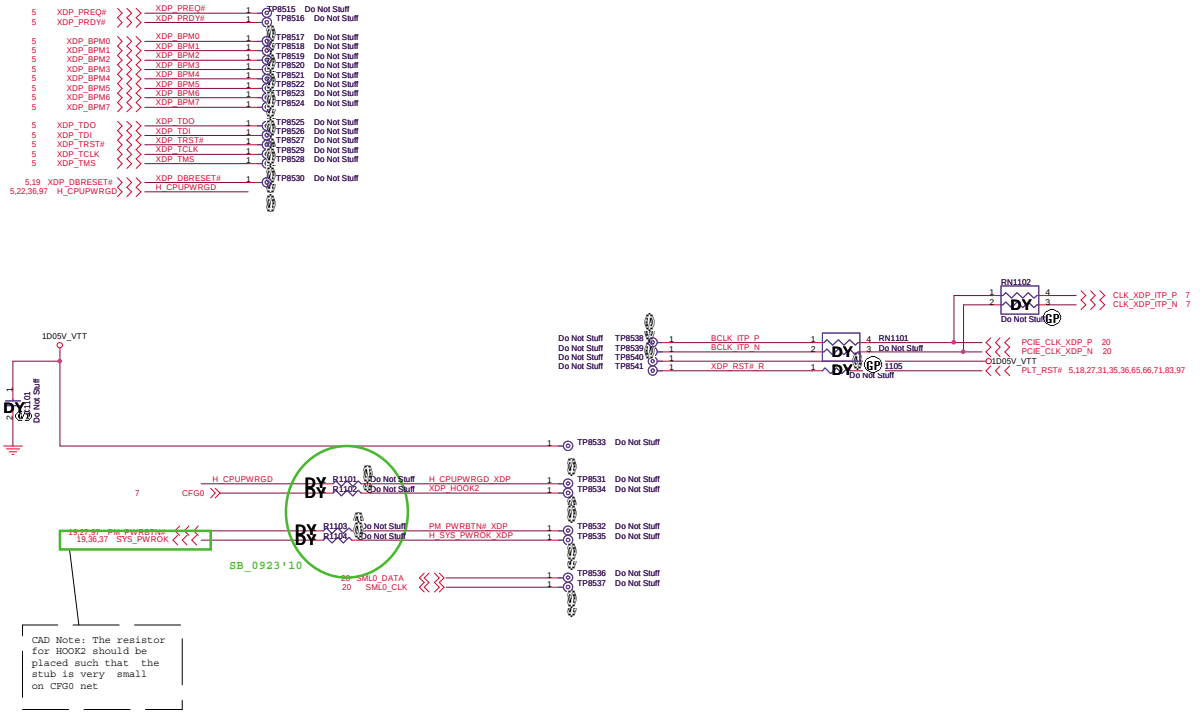
Title	***CPU (VSS)***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 10 of 102	



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Title	XDP	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 11 of 102	

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Title

Reserved

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 12 of 102

(Blanking)

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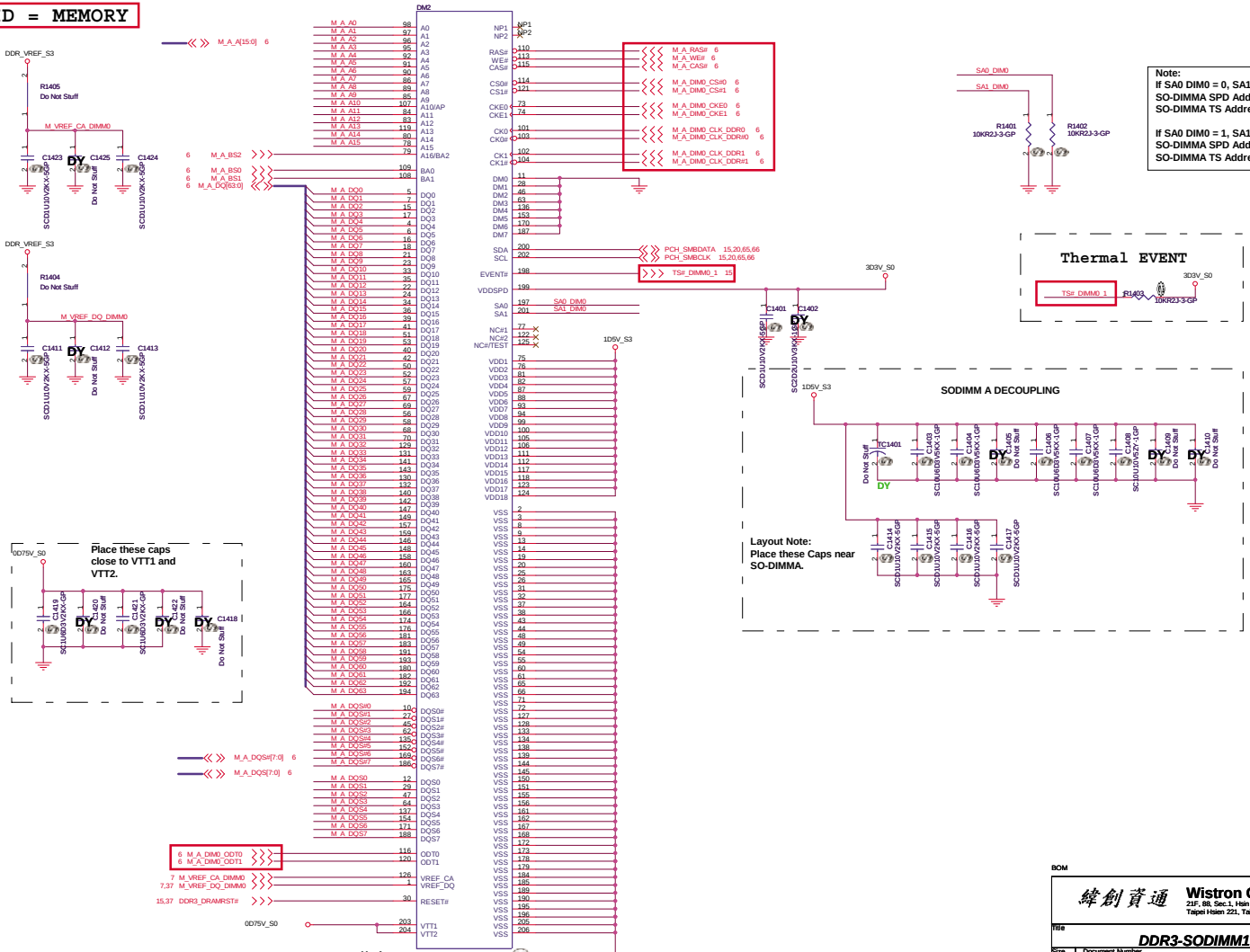
Title

Reserved

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 13 of 102

SSID = MEMORY



BOM

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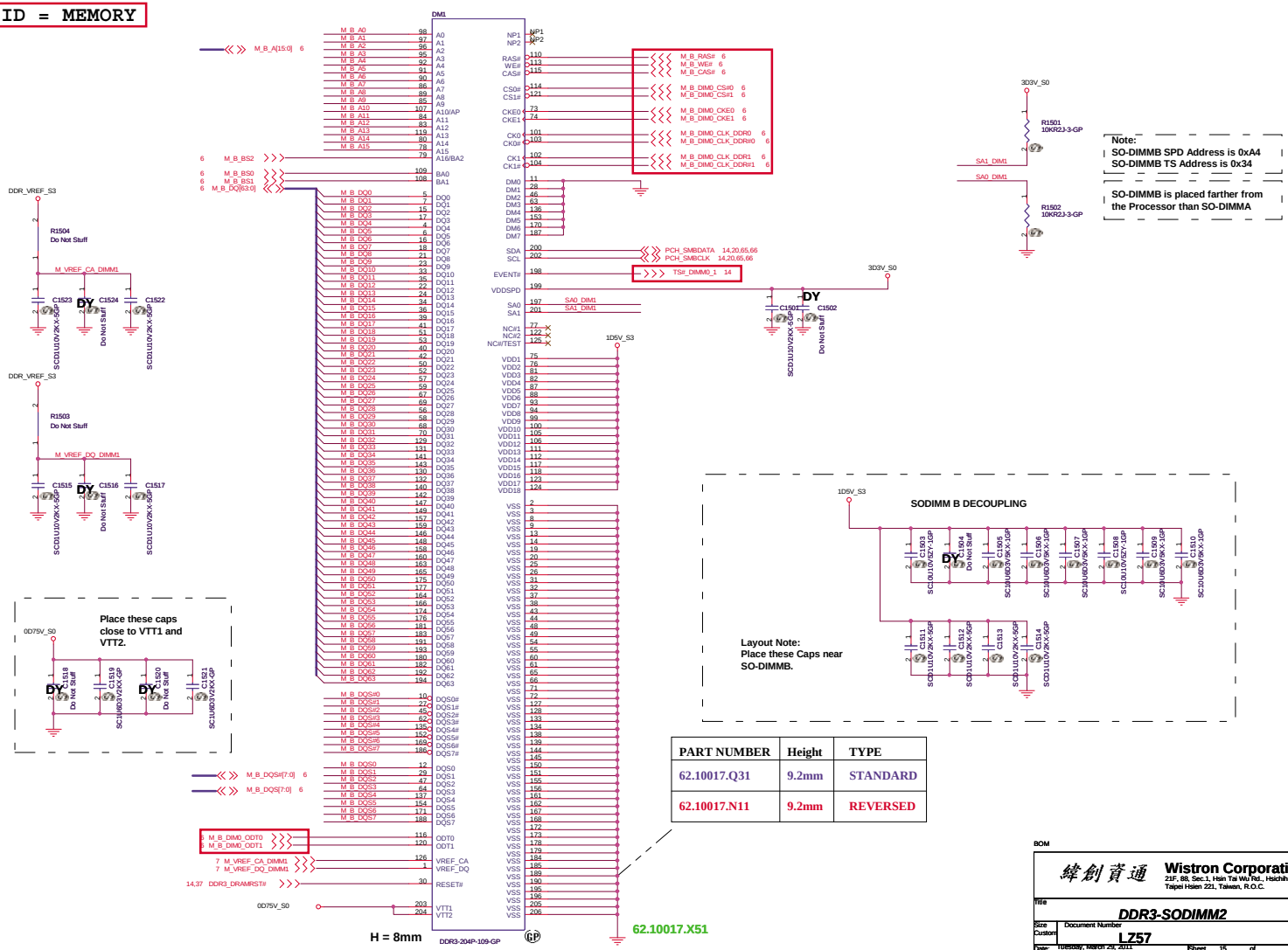
Title: **DDR3-SODIMM1**

Size	Document Number	Rev
Custom	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 14 of 102

SSID = MEMORY



PART NUMBER	Height	TYPE
62.10017.Q31	9.2mm	STANDARD
62.10017.N11	9.2mm	REVERSED

BOM

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Title: DDR3-SODIMM2

Size: Custom | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 15 of 102

(Blanking)

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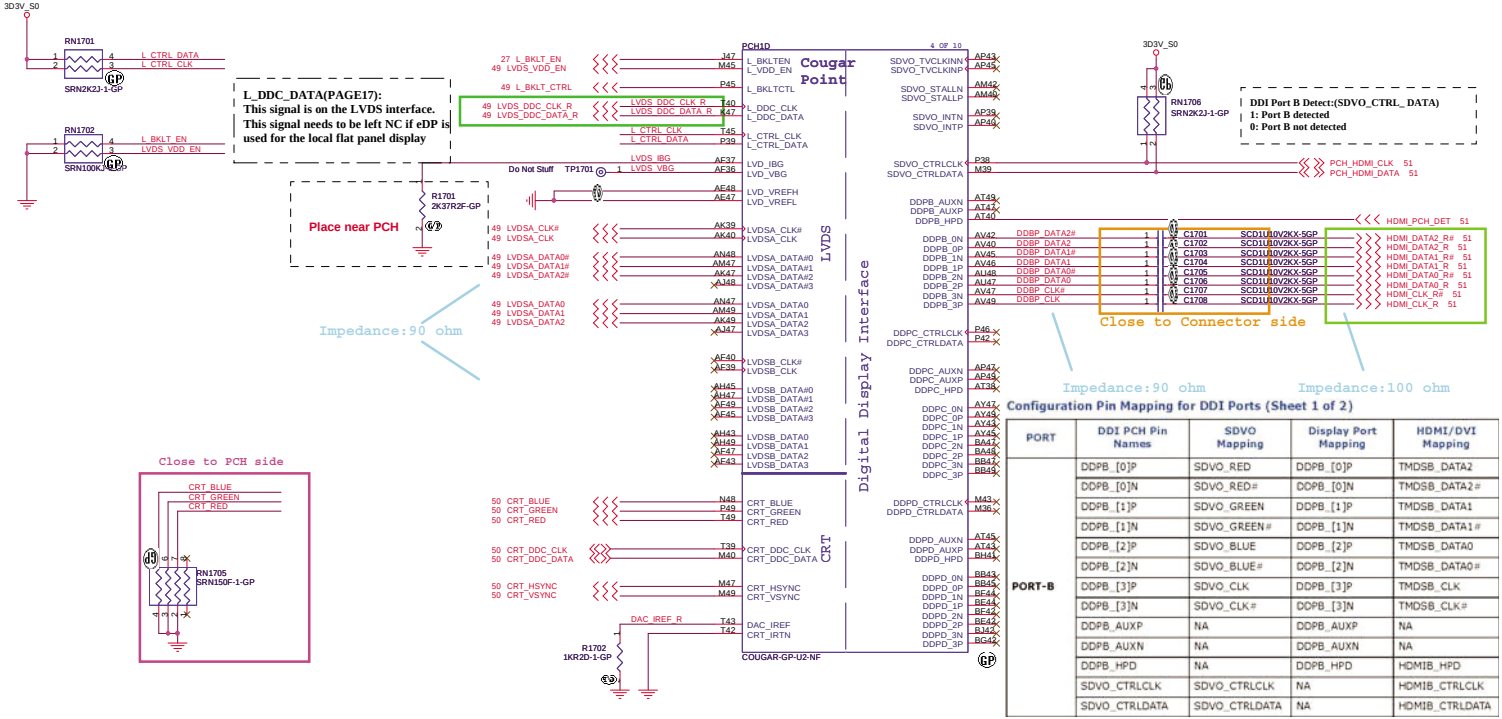
Title

DDR3-SODIMM2

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 16 of 102



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

BOM

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Title: **PCH (LVDS/CRT/DDI)**

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 17 of 102

SSID = PCH

20100725 Annie modify

CRB : 2.2K
CEKLT: 1K

+V_NVRAM_VCCQ
R1808 2K2R2J-2-GP
NV_CLE 1 R1809 1K2R2J-1-GP H_SNB_IVB# 5

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

RN1801 SRN8K2J-2-GP
INT_PIRQA# 1 / INT_PIRQE# 2 / INT_PIRQC# 3 / INT_PIRQB# 4 / 5 — 10 3D3V_S0 / 9 INT_PIRQH# / 8 INT_PIRQG# / 7 INT_PIRQD# / 6 INT_PIRQF#
3D3V_S0

R1801 DY 1 Do Not Stuff PCI_GNT3#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

RN1803 SRN10KJ-5-GP
DGPU_HOLD_RST# 1 / DGPU_PWR_EN# 2 — 3 / 4

R1802 DY Do Not Stuff BBS_BIT1
R1803 DY Do Not Stuff BBS_BIT0 BBS_BIT0 21

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

3D3V_S0
R1814 DY Do Not Stuff
INT_PIRQA# / INT_PIRQB# / INT_PIRQC# / INT_PIRQD#

93 DGPU_HOLD_RST# Do Not Stuff TP1805
93 DGPU_PWR_EN# Do Not Stuff TP1804
DGPU_SELECT# / DGPU_PWR_EN# / BBS_BIT1 / DGPU_PWM_SELECT# / GNT3#

SC_1026'10
78 dGPU_LED / 27,56 SATA_ODD_DAS_S# / 35 USB30_SM# / 49 DCR_EN#
R1818 / R1813 / R1815 / R1817 — 22R2J-2-GP
INT_PIRQE# / INT_PIRQF# / INT_PIRQG# / INT_PIRQH# / PCI_PME#
Do Not Stuff TP1801

SC_1025'10
PCI PLTRST#
65,71 CLK_PCI_LPC / 20 CLK_PCI_FB / 27 CLK_PCI_KBC
R1804 / R1805 / R1806 — 22R2J-2-GP
CLK_PCI_LPC_R / CLK_PCI_FB_R / CLK_PCI_KBC_R

EC1802 DY Do Not Stuff
EC1801 DY Do Not Stuff
KBC CLK EMI

3D3V_S0
U1801 DY Do Not Stuff
VCC / GND / A / B / Y
27,31,35,36,65,66,71,83,97 PLT_RST# — PCI PLTRST#
R1807 0R2J-2-GP
R1816 DY Do Not Stuff
C1801 DY Do Not Stuff
C1802 DY Do Not Stuff
20100629

PCH1E — 5 OF 10
Cougar Point
RSVD / NVRAM / PCI / USB
COUGAR-GP-U2-NF

RSVD#AV5 AV5 NV_ALE
DF_TVS AY1 NV_CLE
RSVD#AV10 AV10 NV_RCOMP 1 TP1803 Do Not Stuff

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	X
1	USB Ext. port 1 (Left Side)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	E-SATA /USB Ext. port 4
9	USB Ext. port 2(CardReader BD
10	USB Ext. port 3(RJ45_BD)
11	Mini Card1 (WLAN)
12	CAMERA
13	X

USB_PN1 62 / USB_PP1 62 / USB_PN2 64 / USB_PP2 64 / USB_PN3 63 / USB_PP3 63 / USB_PN4 66 / USB_PP4 66 / USB_PN5 82 / USB_PP5 82
USB_PN8 57 / USB_PP8 57 / USB_PN9 82 / USB_PP9 82 / USB_PN10 82 / USB_PP10 82 / USB_PN11 65 / USB_PP11 65 / USB_PN12 49 / USB_PP12 49
USBRBIAS# USB_RBIAS 1 R1811 22D6R2F-L1-GP
USBRBIAS
OC0#/GPIO59 USB_OC#0 1 — USB_OC#0_1 62
OC1#/GPIO40 USB_OC#2 3
OC2#/GPIO41 USB_OC#4 5
OC3#/GPIO42 USB_OC#6 7
OC4#/GPIO43 USB_OC#8 9 — USB_OC#8_9 62
OC5#/GPIO9 USB_OC#10 11 — USB_OC#10_11 61
OC6#/GPIO10 USB_OC#12 13 — USB_OC#12_13 61
OC7#/GPIO14 PCH_GPIO14

SW programing USB_OC#12_13 for USB 9

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

R1820 0R2J-2-GP
LZ57 6L
-1_1209'10

RN1802 SRN10KJ-L3-GP
USB_OC#2 3 / USB_OC#4 5 / USB_OC#6 7 / USB_OC#10 11 — 10 3D3V_S5 / 9 USB_OC#12_13 / 8 USB_OC#8 9 / 7 PCH_GPIO14 / 6 USB_OC#0 1
3D3V_S5

+V_NVRAM_VCCQ
Danbury Technology:
Disabled when Low.
Enable when High.
R1810 DY Do Not Stuff
NV_ALE

BOM

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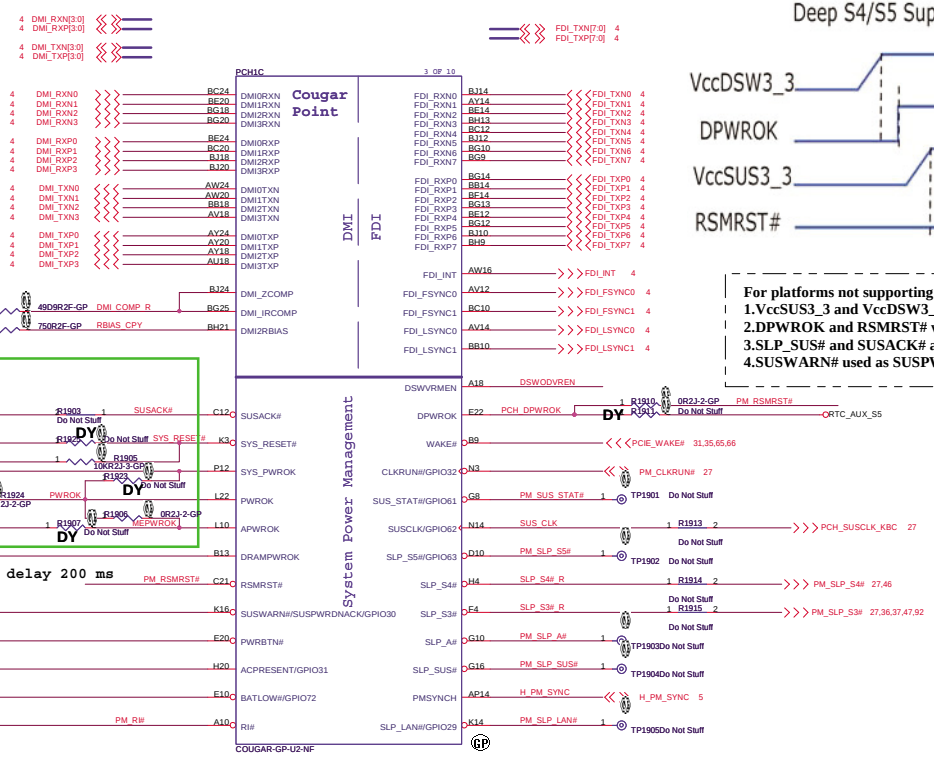
Taipei Hsien 221, Taiwan, R.O.C.

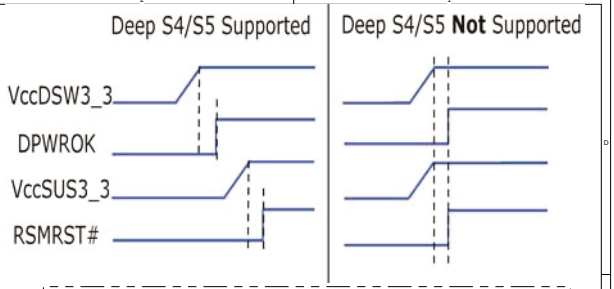
Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: LZ57 | Rev: -1
Date: Tuesday, March 29, 2011 | Sheet 18 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

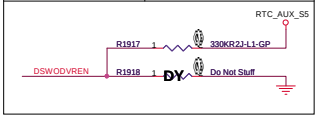


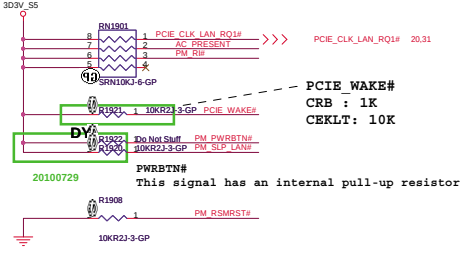
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

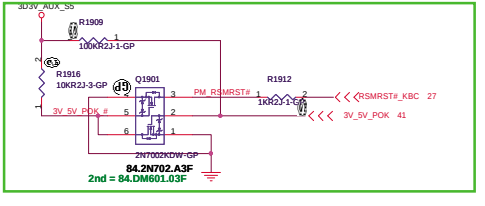
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

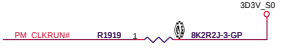




PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

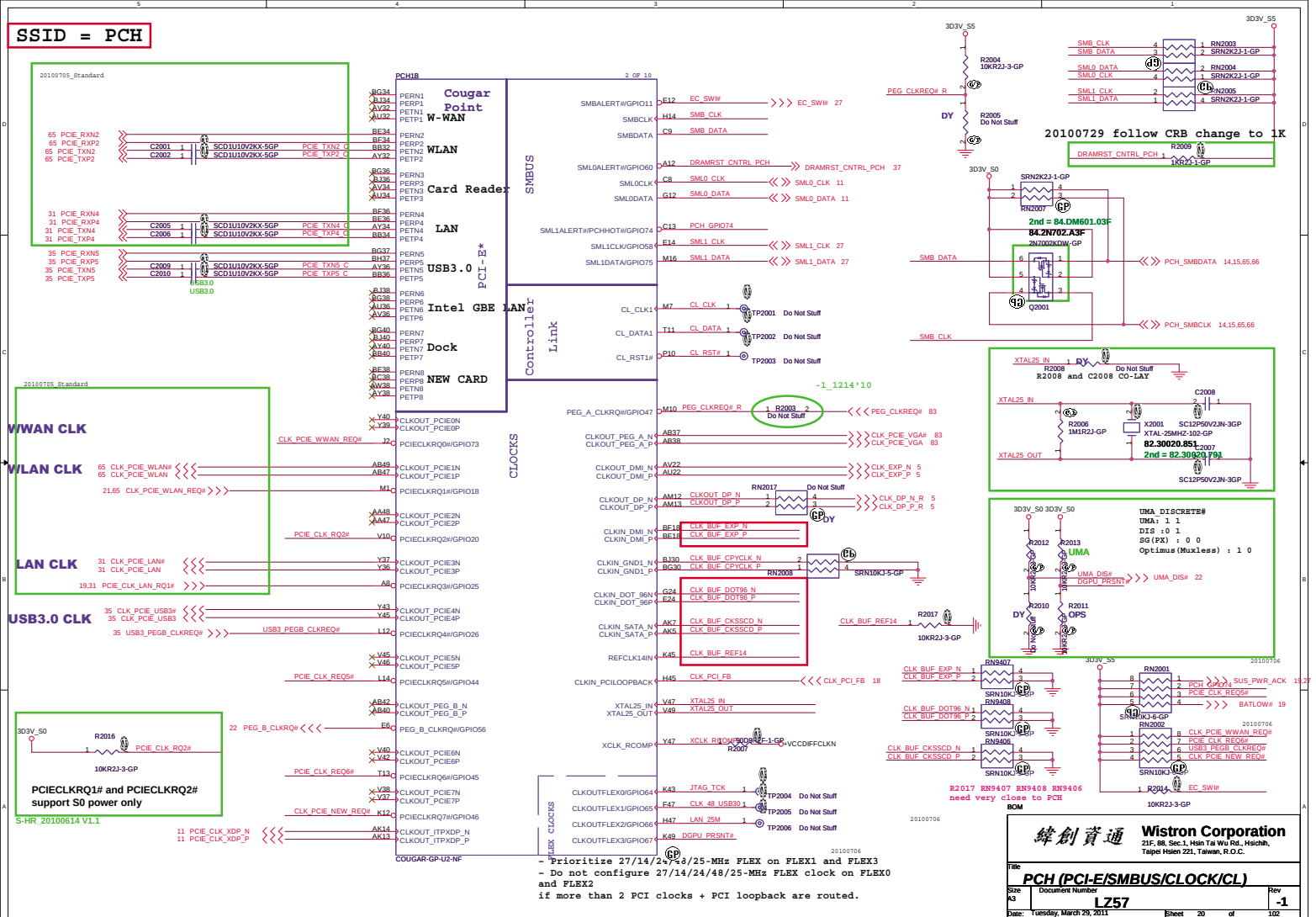




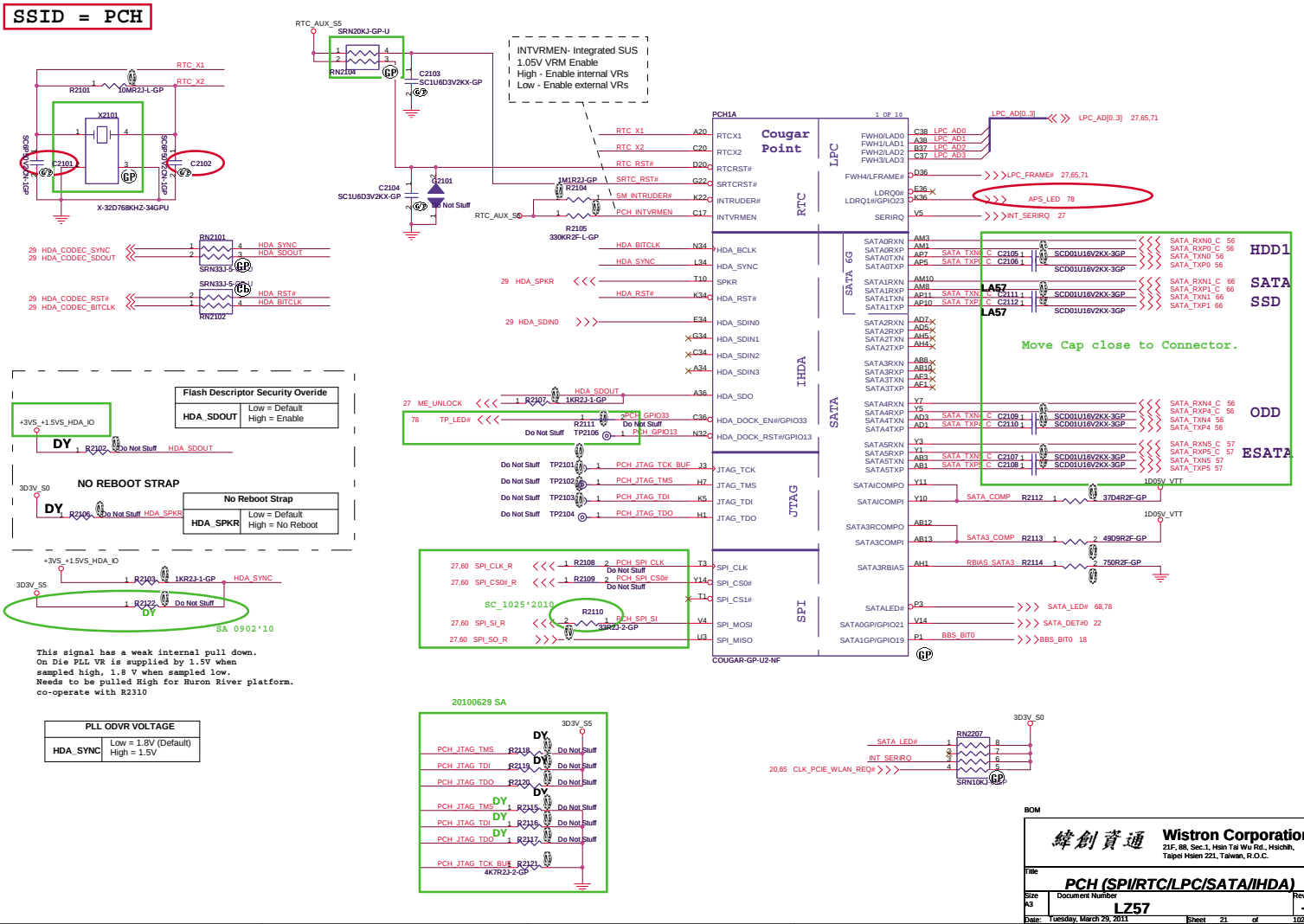
BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH (DM I/FDI/PM)
Size A3 / Document Number	LZ57
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 19 of 102

SSID = PCH


PCH1B
Cougar Point
W-WAN
WLAN
Card Reader
LAN
USB3.0
Intel GBE LAN
Dock
NEW CARD
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR-GP-U2-NF
20100705_Standard
WWAN CLK
WLAN CLK
LAN CLK
USB3.0 CLK
PCIECLKRQ1# and PCIECLKRQ2# support S0 power only
S-HR_20100614 V1.1
20100729 follow CRB change to 1K
2nd = 84.DM601.03F
84.2N702.A3F
2nd = 82.30020.791
82.30020.851
UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0
R2017 RN9407 RN9408 RN9406 need very close to PCH
- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2
if more than 2 PCI clocks + PCI loopback are routed.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (PCI-E/SMBUS/CLOCK/CL)
Size A3
Document Number LZ57
Rev -1
Date: Tuesday, March 29, 2011
Sheet 20 of 102

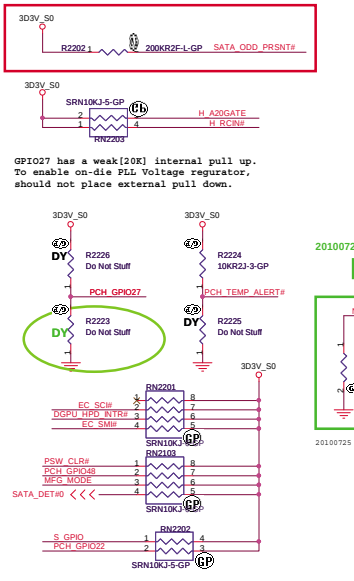
SSID = PCH

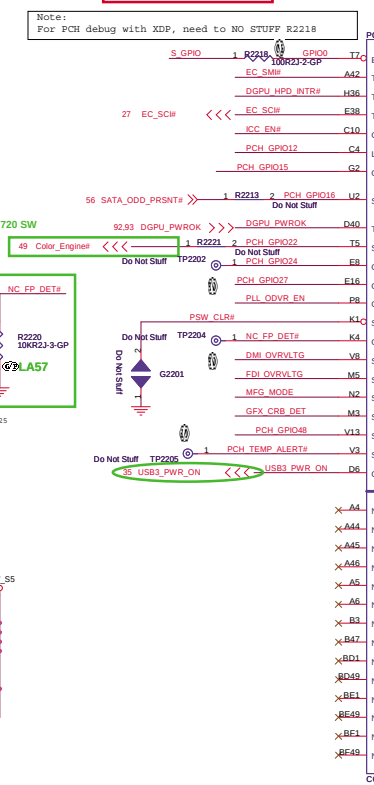

RTC_AUX_S5
SRN20KJ-GP-U
RN2104
C2103
SC1U6D3V2KX-GP
INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs
RTC_X1
RTC_X2
R2101
10MR2J-L-GP
X2101
C2101
C2102
X-32D768KHZ-34GPU
C2104
SC1U6D3V2KX-GP
D2101
Do Not Stuff
1M1R2J-GP
R2104
RTC_AUX_S5
R2105
330KR2F-L-GP
PCH1A
1 OF 10
Cougar Point
RTC
LPC
SATA 6G
IHDA
SATA
JTAG
SPI
COUGAR-GP-U2-NF
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
SRTC_RST#
SM_INTRUDER#
PCH_INTVRMEN
HDA_BITCLK
HDA_SYNC
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
SERIRQ
LPC_AD[0..3]
LPC_FRAME#
APS_LED
INT_SERIRQ
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATA3RCOMPO
SATA3COMPI
SATA3RBIAS
SATALED#
SATA0GP/GPIO21
SATA1GP/GPIO19
SCD01U16V2KX-3GP
HDD1
SATA SSD
ODD
ESATA
LA57
Move Cap close to Connector.
SATA_COMP
SATA3_COMP
RBIAS_SATA3
SATA_LED#
SATA_DET#0
BBS_BIT0
1D05V_VTT
37D4R2F-GP
49D9R2F-GP
750R2F-GP
RN2101
SRN33J-5-GP
RN2102
HDA_CODEC_SYNC
HDA_CODEC_SDOUT
HDA_CODEC_RST#
HDA_CODEC_BITCLK
HDA_SYNC
HDA_SDOUT
HDA_RST#
HDA_BITCLK
HDA_SPKR
HDA_SDIN0
ME_UNLOCK
TP_LED#
R2107
1KR2J-1-GP
R2111
TP2106
PCH_GPIO33
PCH_GPIO13
Flash Descriptor Security Overide
HDA_SDOUT
Low = Default
High = Enable
+3VS_+1.5VS_HDA_IO
DY
R2102
Do Not Stuff
NO REBOOT STRAP
3D3V_S0
R2106
HDA_SPKR
No Reboot Strap
HDA_SPKR
Low = Default
High = No Reboot
R2103
1KR2J-1-GP
R2122
3D3V_S5
SA 0902'10
This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310
PLL ODVR VOLTAGE
HDA_SYNC
Low = 1.8V (Default)
High = 1.5V
PCH_JTAG_TCK_BUF
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
TP2101
TP2102
TP2103
TP2104
SPI_CLK_R
SPI_CS0#_R
SPI_SI_R
SPI_SO_R
R2108
R2109
PCH_SPI_CLK
PCH_SPI_CS0#
SC_1025'2010
R2110
33R2J-2-GP
PCH_SPI_SI
20100629 SA
R2118
R2119
R2120
R2115
R2116
R2117
R2121
4K7R2J-2-GP
RN2207
SRN10KJ-5-GP
SATA_LED#
INT_SERIRQ
CLK_PCIE_WLAN_REQ#
BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (SPI/RTC/LPC/SATA/IHDA)
Size
A3
Document Number
LZ57
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 21 of 102

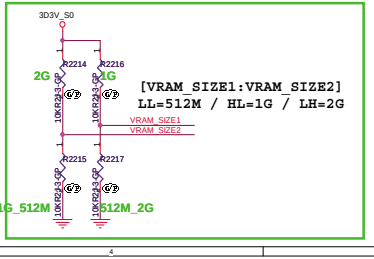
SSID = PCH

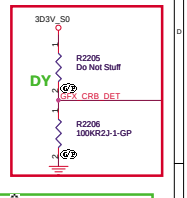
Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY









SB 0923'10

PCH_THERMTRIP_R R2222 1 01D05V_VTT
DY
Do Not Stuff

20100729 follow Annie CRB

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

BOM

緯創資通 Wistron Corporation
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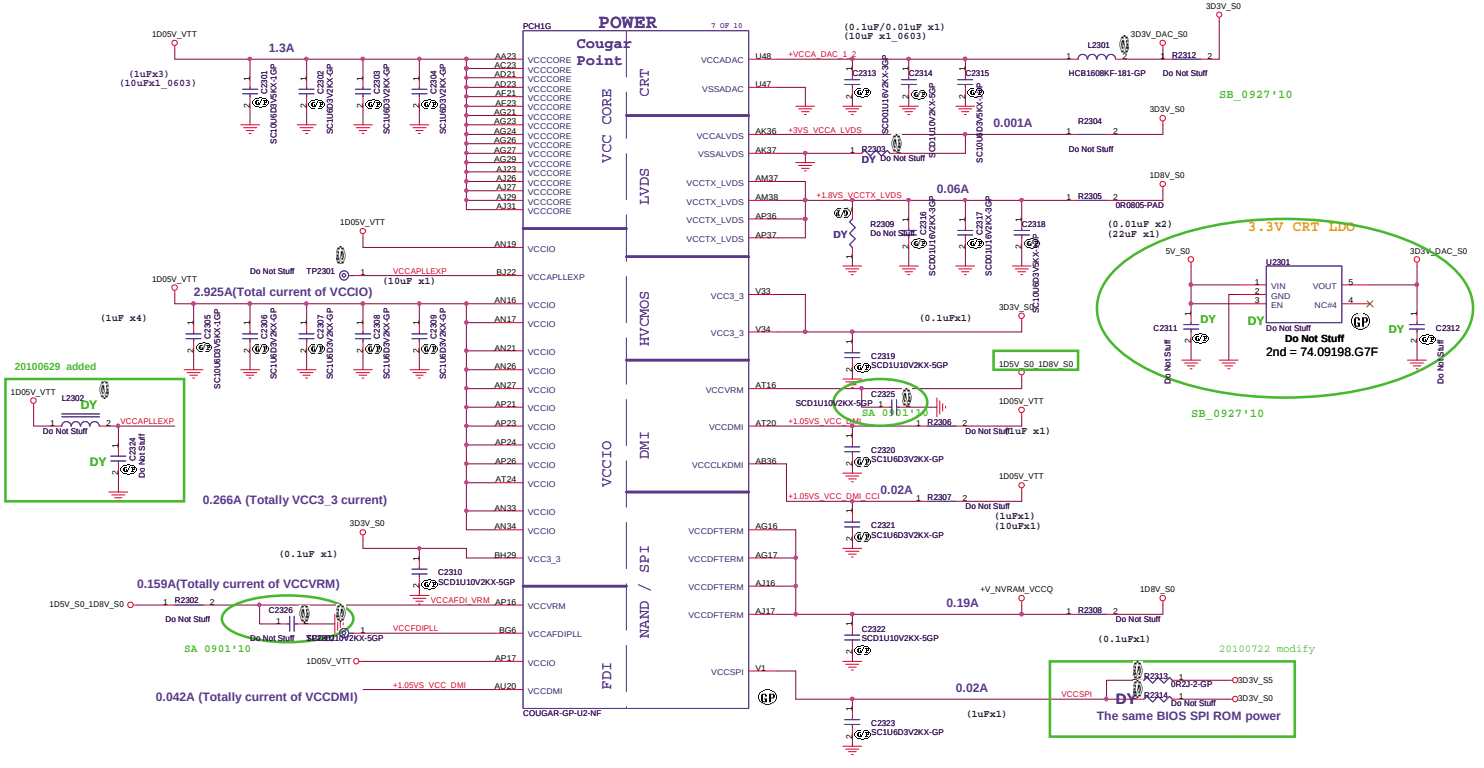
Title: PCH (GPIO/CPU)

Size	Document Number	Rev
A3	LZ57	-1

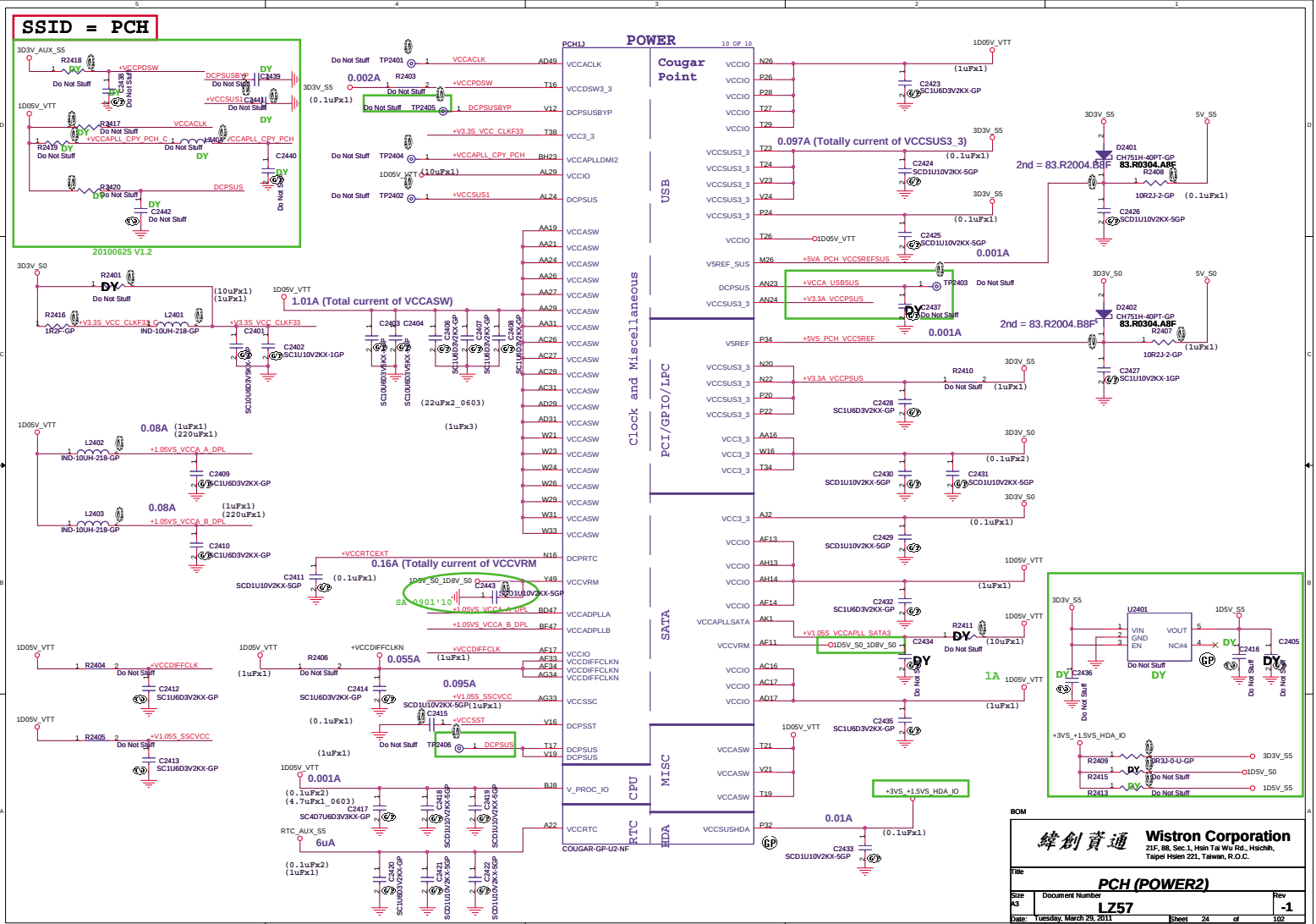
Date: Tuesday, March 29, 2011 Sheet 22 of 102

SSID = PCH 6A



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH (POWER1)
Size A3 / Document Number	LZ57
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 23 of 102


SSID = PCH
POWER
PCH1J
10 OF 10
Cougar Point
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
HDA
RTC
COUGAR-GP-U2-NF
0.002A
0.097A (Totally current of VCCSUS3_3)
1.01A (Total current of VCCASW)
0.08A
0.16A (Totally current of VCCVRM
0.055A
0.095A
0.001A
6uA
1A
0.01A
2nd = 83.R2004.B8F
83.R0304.A8F
20100625 V1.2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (POWER2)
LZ57
-1
Tuesday, March 29, 2011
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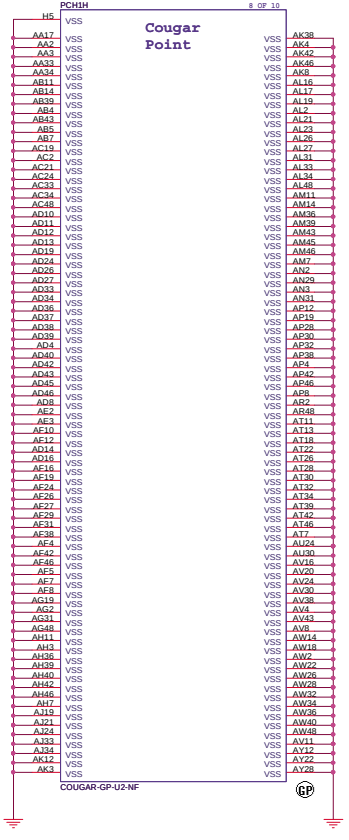
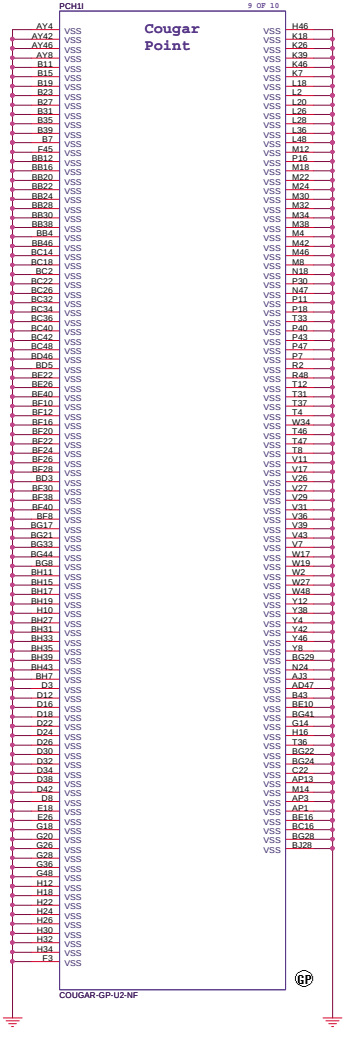
SSID = PCH





BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PCH (VSS)***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 25 of 102	

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BOM

緯創資通 Wistron Corporation
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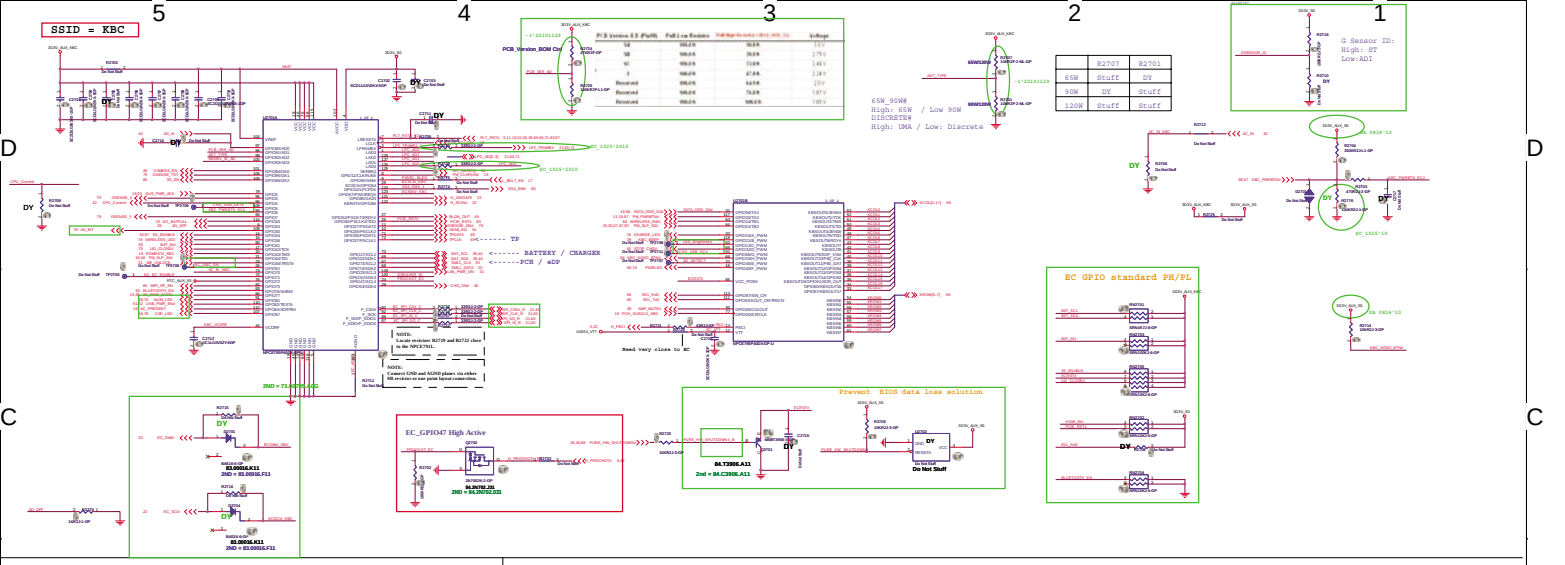
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 26 of 102



	R2707	R2701
65W	Stuff	DY
90W	DY	Stuff
120W	Stuff	Stuff

LILI Multi GPIO setting

Model_ID_BOM Ctrl OPS: 64.14335.6DL

MODEL_ID_AD(Pin100)	Pull-Low Register	Pull-High Register	Voltage
V/W S7 UMA	100.0 K	64.9 K	2.001 V
V/W S7 OPTIMUS	100.0 K	76.8 K	1.847 V
Z S7 UMA	100.0 K	100.0 K	1.650 V
Z S7 OPTIMUS	100.0 K	143.0 K(64.14335.L0L)	1.32 V

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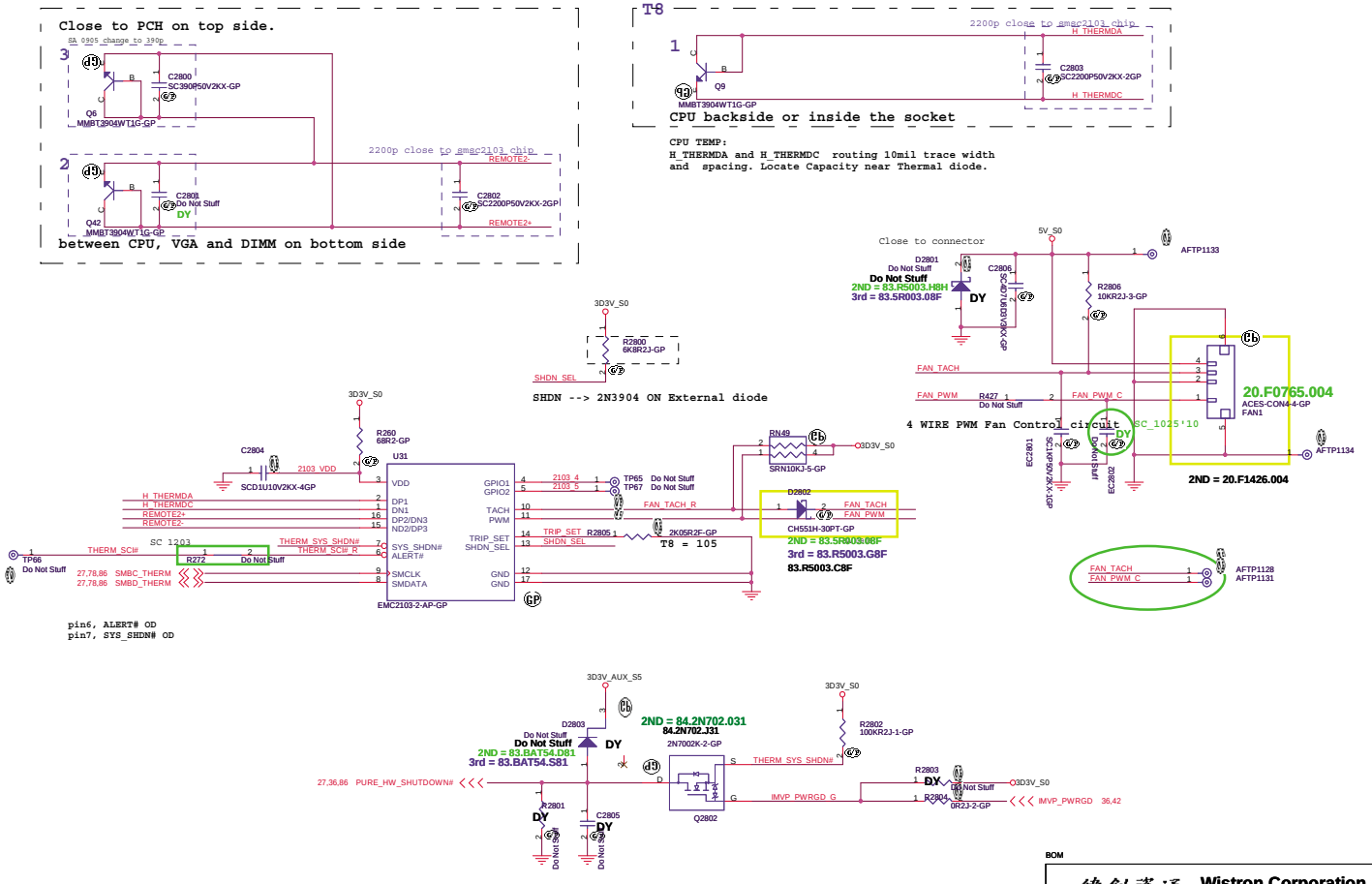
KBC Nuvoton NPCE785

L257 -1

SSID = Thermal

Thermal sensor



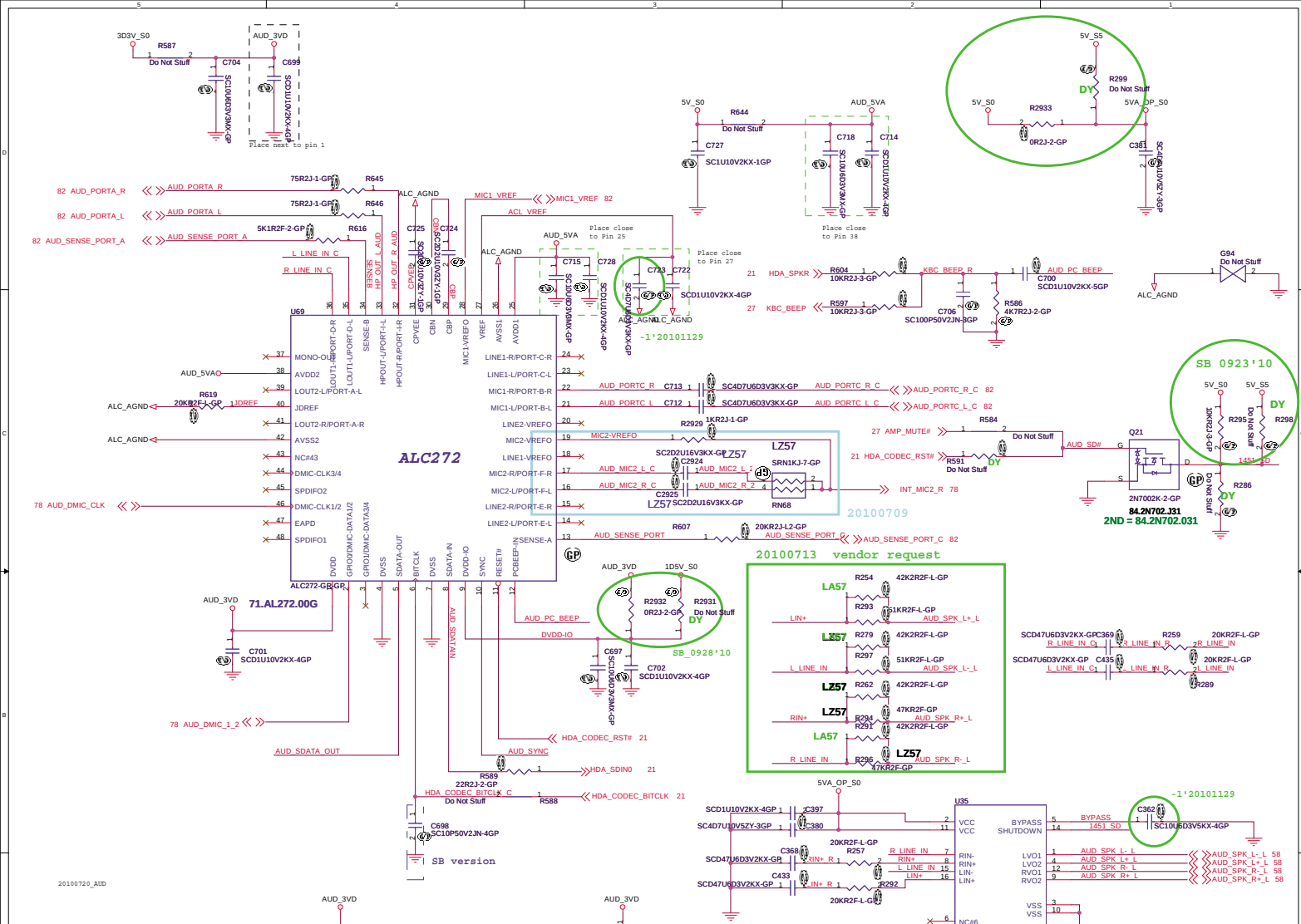
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal P2800/Fan Controllor P2793*

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 28 of 102


ALC272
U69
ALC272-GR-GP
71.AL272.00G
20100713 vendor request
20100709
SB 0923'10
SB_0928'10
SB version
U35
20100720_AUD

blanking

BOM

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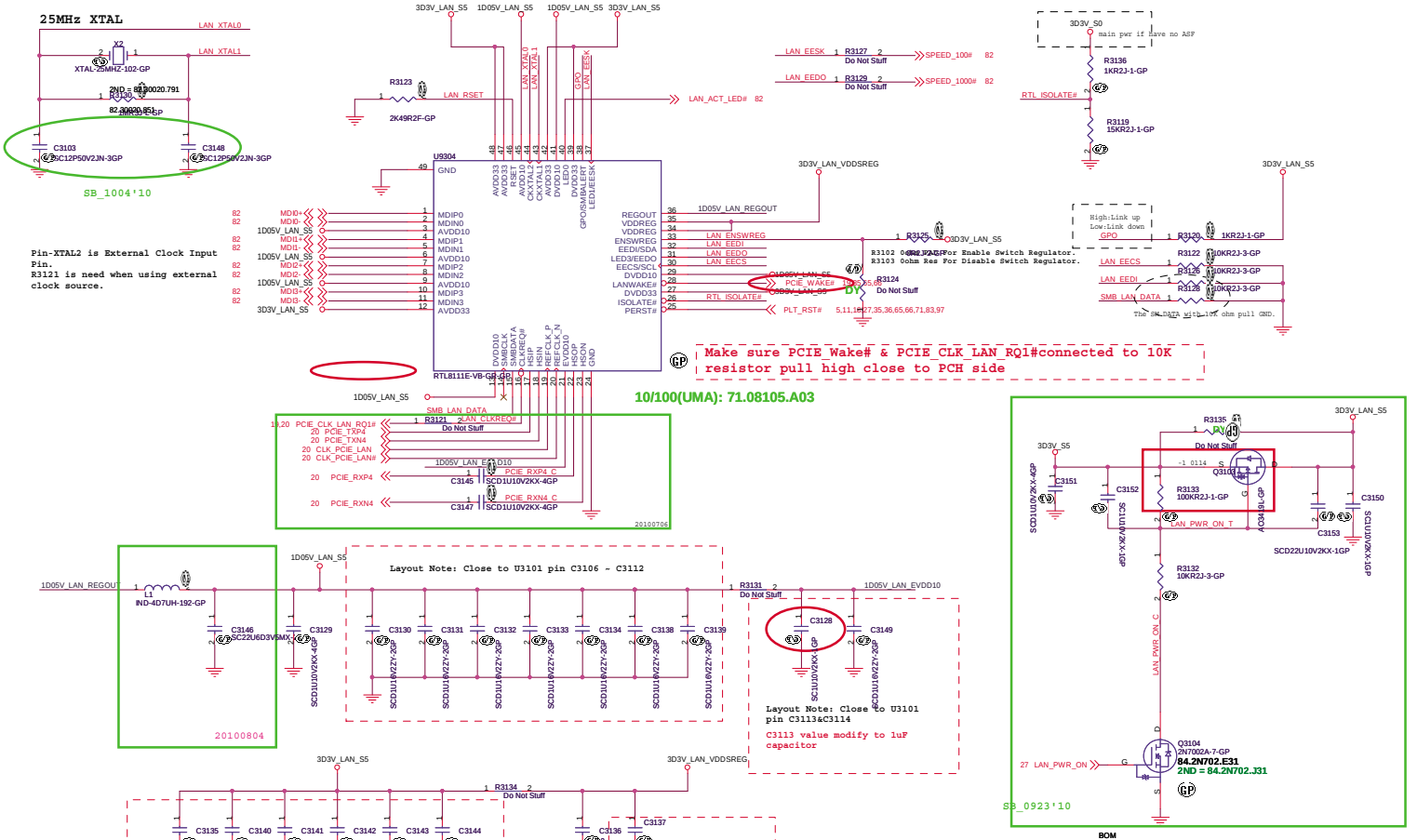
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 30 of 102



BOM

緯創資通	Wistron Corporation 21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LAN RTL8111E	
Size A3	Document Number LA57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 31 of 102	

BOM

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***RTS5159 (CARD READER)***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 32 of 102	

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 33 of 102

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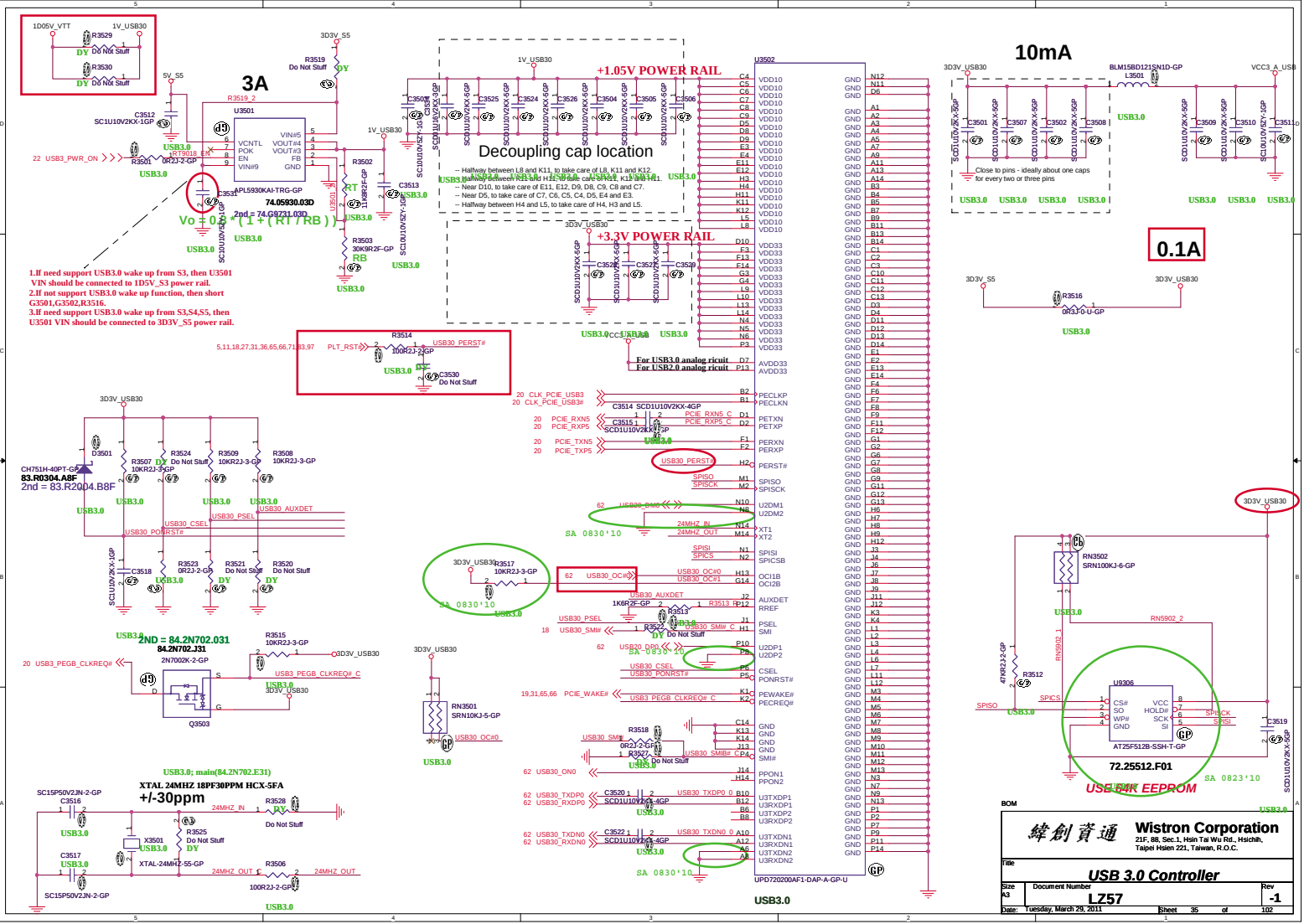
BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 34 of 102	



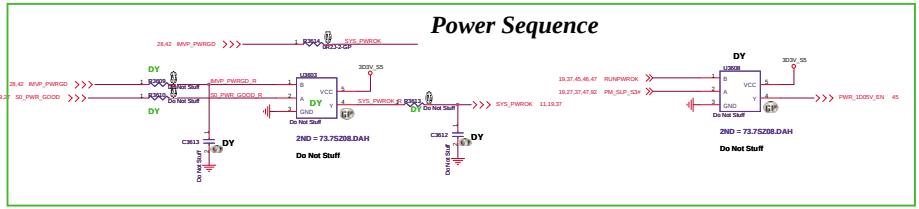
BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

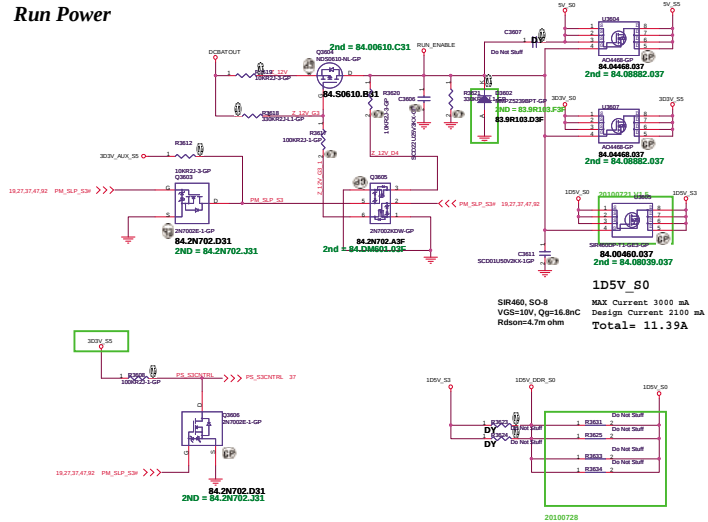
Title: USB 3.0 Controller

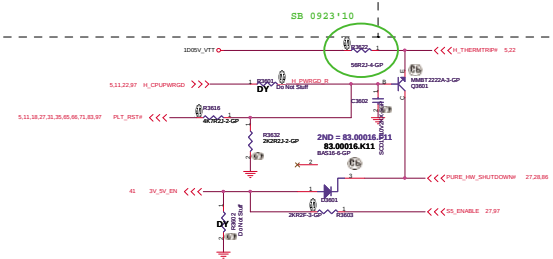
Size: A3 | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 35 of 102



SSID = Reset.Suspend





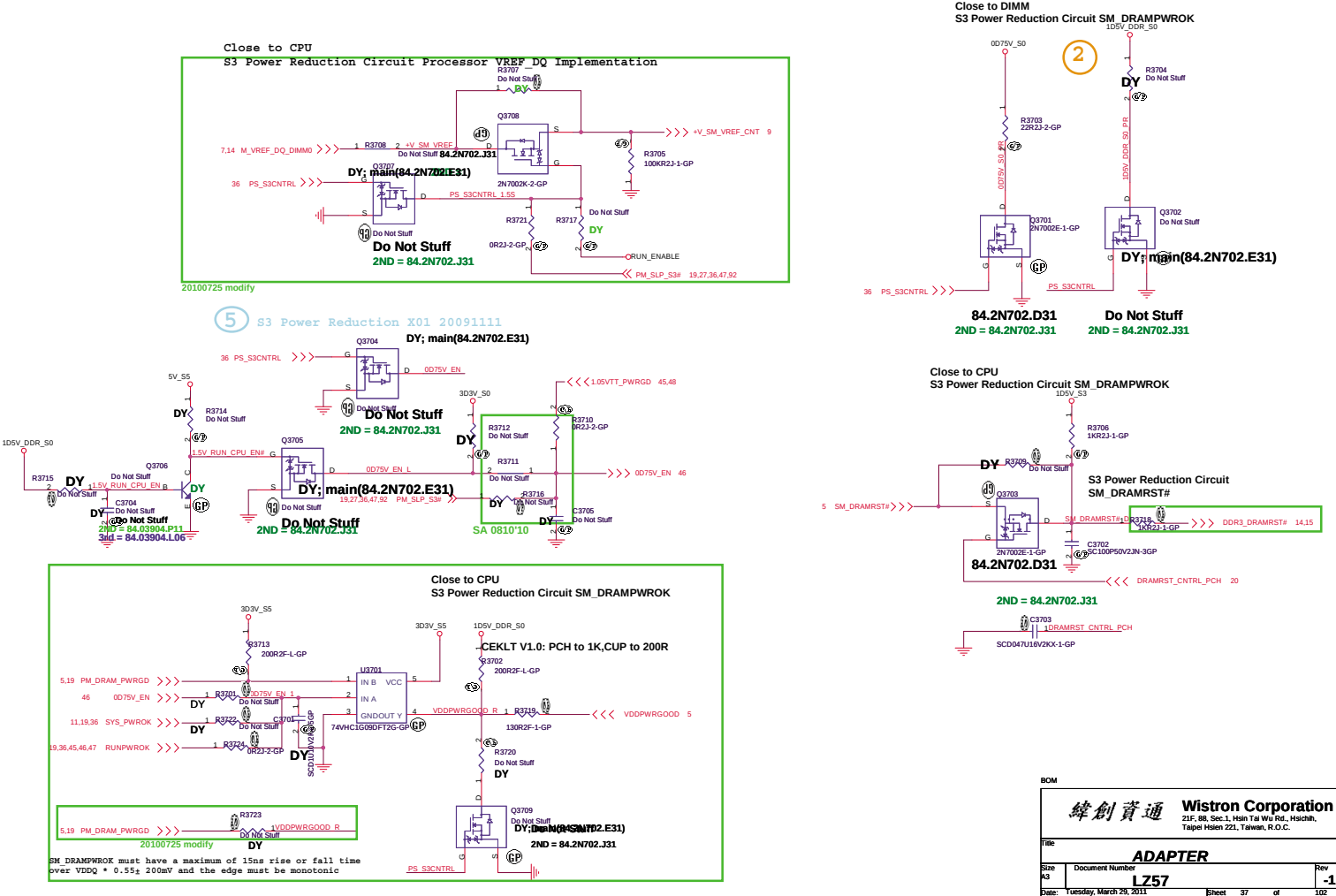
BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

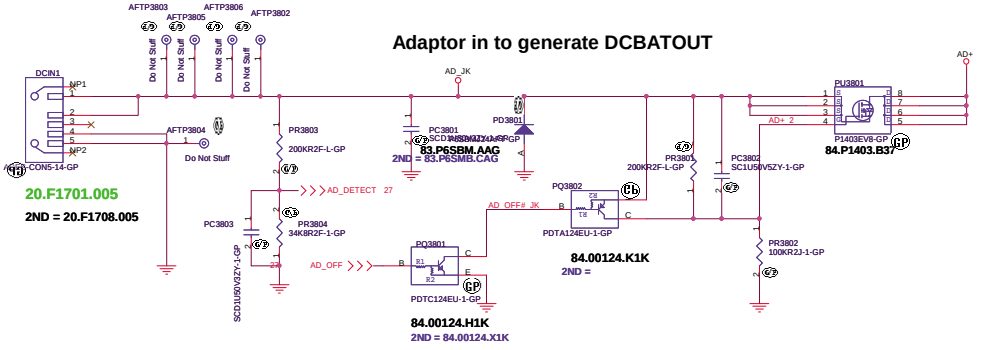
Title: Power Plane Enable

Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 04, 2008 Sheet 38 of 100

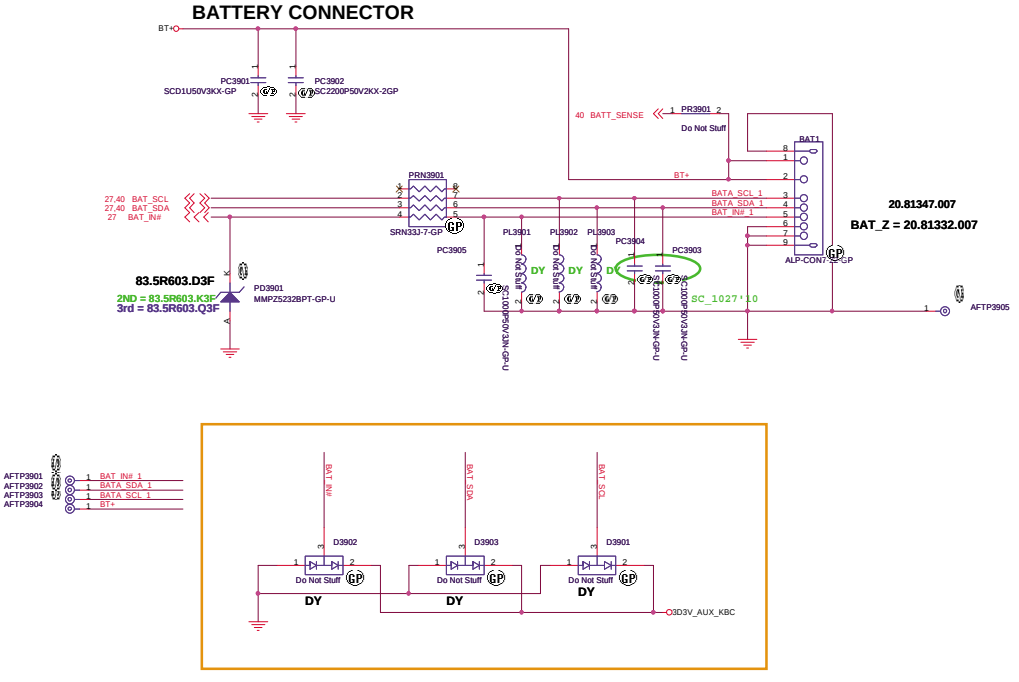

Close to CPU
S3 Power Reduction Circuit Processor VREF DQ Implementation
R3707
Do Not Stuff
DY
Q3708
+V_SM_VREF_CNT 9
7,14 M_VREF_DQ_DIMM0
R3708
+V_SM_VREF
Do Not Stuff 84.2N702.J31
R3705
100KR2J-1-GP
DY; main(84.2N702.E31)
Q3707
2N7002K-2-GP
36 PS_S3CNTRL
PS_S3CNTRL_1.5S
Do Not Stuff
R3721
R3717
DY
Do Not Stuff
0R2J-2-GP
RUN_ENABLE
PM_SLP_S3# 19,27,36,47,92
Do Not Stuff
2ND = 84.2N702.J31
20100725 modify
5 S3 Power Reduction X01 20091111
DY; main(84.2N702.E31)
Q3704
36 PS_S3CNTRL
0D75V_EN
Do Not Stuff
Do Not Stuff
2ND = 84.2N702.J31
5V_S5
R3714
Do Not Stuff
1.05VTT_PWRGD 45,48
3D3V_S0
R3712
Do Not Stuff
R3710
0R2J-2-GP
1D5V_DDR_S0
R3715
DY
Do Not Stuff
Q3706
Do Not Stuff
1.5V_RUN_CPU_EN
1.5V_RUN_CPU_EN#
Q3705
0D75V_EN_L
R3711
Do Not Stuff
0D75V_EN 46
DY
C3704
Do Not Stuff
DY; main(84.2N702.E31)
19,27,36,47,92 PM_SLP_S3#
R3716
Do Not Stuff
DY
C3705
Do Not Stuff
Do Not Stuff
2ND = 84.03904.P11
3rd = 84.03904.L06
Do Not Stuff
2ND = 84.2N702.J31
SA 0810'10
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK
3D3V_S5
R3713
200R2F-L-GP
3D3V_S5
1D5V_DDR_S0
CEKLT V1.0: PCH to 1K,CUP to 200R
R3702
200R2F-L-GP
U3701
5,19 PM_DRAM_PWRGD
46 0D75V_EN
11,19,36 SYS_PWROK
19,36,45,46,47 RUNPWROK
R3701
0D75V_EN
Do Not Stuff
R3722
C3701
Do Not Stuff
R3724
0R2J-2-GP
IN B
VCC
IN A
GNDOUT Y
74VHC1G09DFT2G-GP
VDDPWRGOOD_R
R3719
130R2F-1-GP
VDDPWRGOOD 5
R3720
Do Not Stuff
DY
Q3709
Do Not Stuff
DY; main(84.2N702.E31)
2ND = 84.2N702.J31
PS_S3CNTRL
R3723
5,19 PM_DRAM_PWRGD
VDDPWRGOOD_R
Do Not Stuff
DY
20100725 modify
SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK
1D5V_DDR_S0
0D75V_S0
2
R3704
Do Not Stuff
DY
R3703
22R2J-2-GP
0D75V_S0_P2
1D5V_DDR_S0_P2
Q3701
2N7002E-1-GP
Q3702
Do Not Stuff
DY; main(84.2N702.E31)
36 PS_S3CNTRL
PS_S3CNTRL
84.2N702.D31
2ND = 84.2N702.J31
Do Not Stuff
2ND = 84.2N702.J31
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK
1D5V_S3
R3706
1KR2J-1-GP
R3709
DY
Do Not Stuff
S3 Power Reduction Circuit
SM_DRAMRST#
5 SM_DRAMRST#
Q3703
SM_DRAMRST#
R3718
1KR2J-1-GP
DDR3_DRAMRST# 14,15
2N7002E-1-GP
C3702
SC100P50V2JN-3GP
84.2N702.D31
DRAMRST_CNTRL_PCH 20
2ND = 84.2N702.J31
C3703
DRAMRST_CNTRL_PCH
SCD047U16V2KX-1-GP
BOM
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ADAPTER
Size
A3
Document Number
LZ57
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 37 of 102

Adaptor in to generate DCBATOUT



BOM

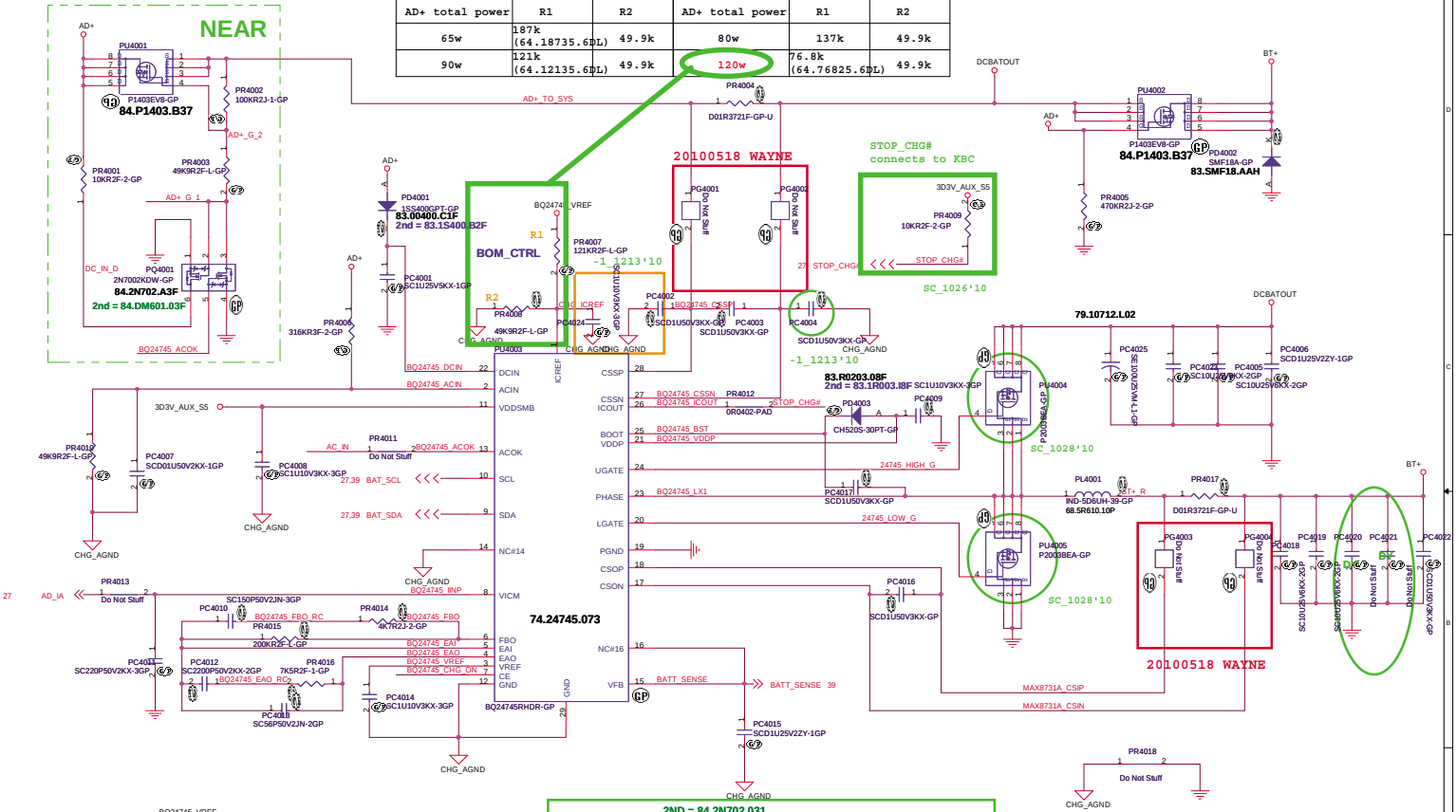
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DCIN_JACK***	
Size	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 38 of 102	



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BATT_CONN	
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 39 of 102	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k (64.18735.6DL)	49.9k	80w	137k	49.9k
90w	121k (64.12135.6DL)	49.9k	120w	76.8k (64.76825.6DL)	49.9k



BOM

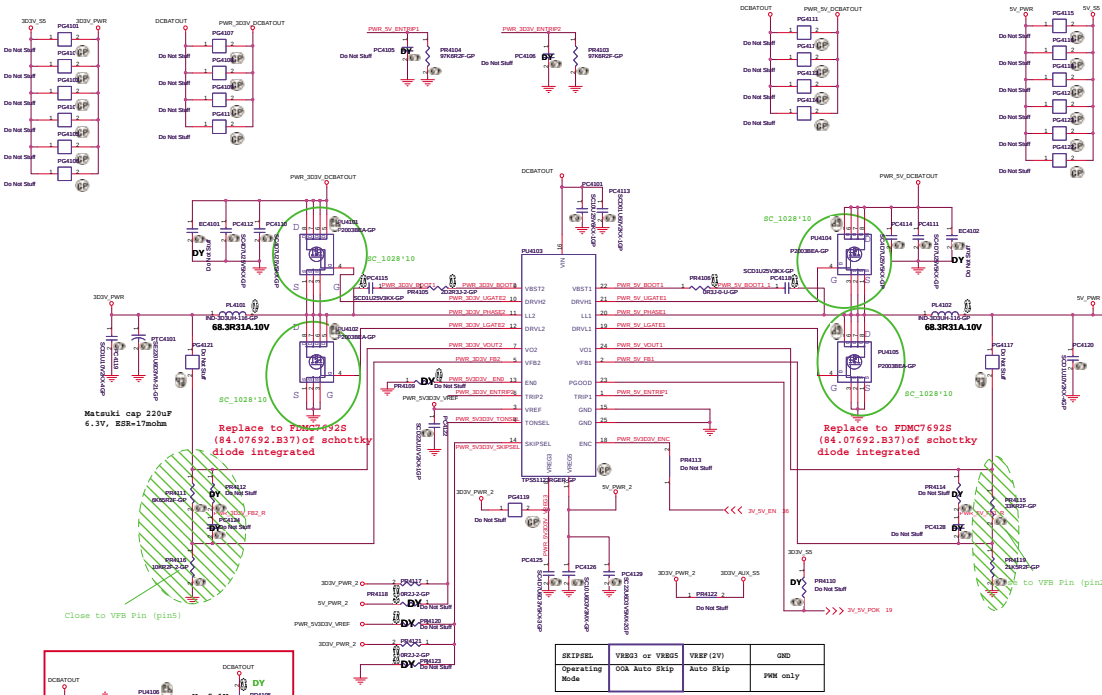
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

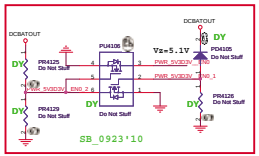
Title: *Charger_BQ24745*

Size | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 40 of 102

SSID = PWR.Plane.Regulator_5v3p3v





SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

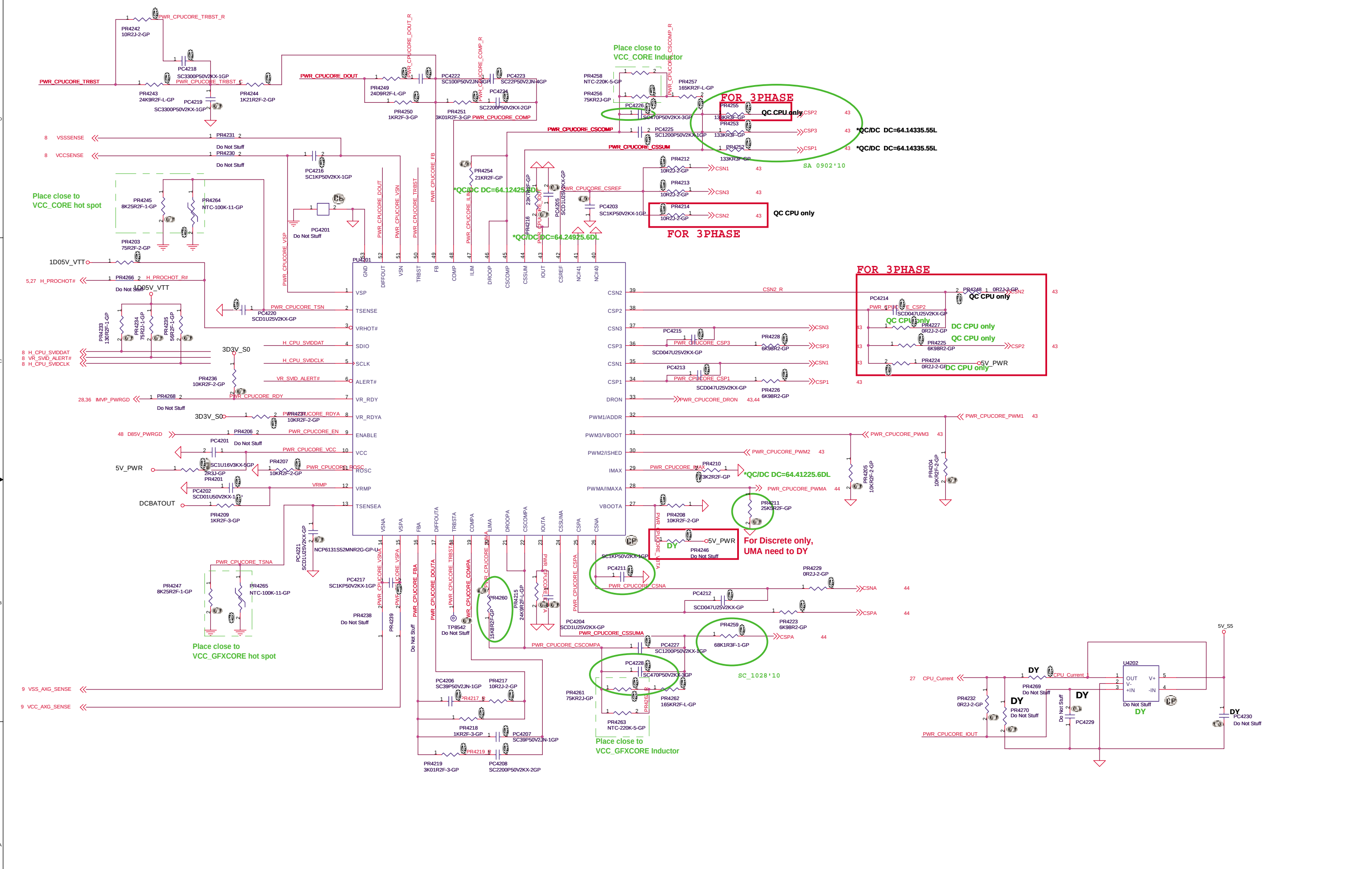
BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 3D3V5V

Size	Document Number	Rev
	LZ57	-1

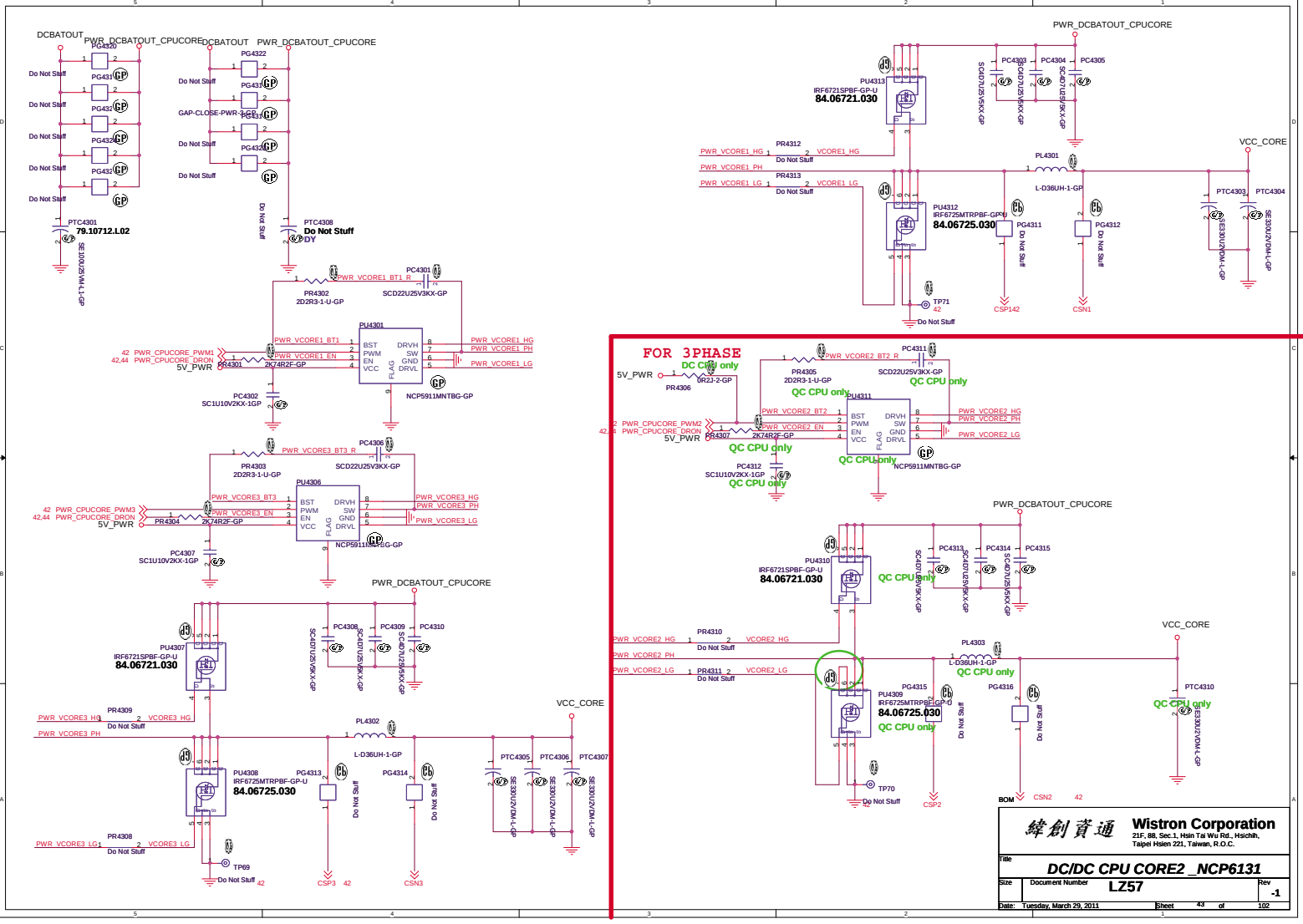
Date: Tuesday, March 29, 2011 Sheet 41 of 100

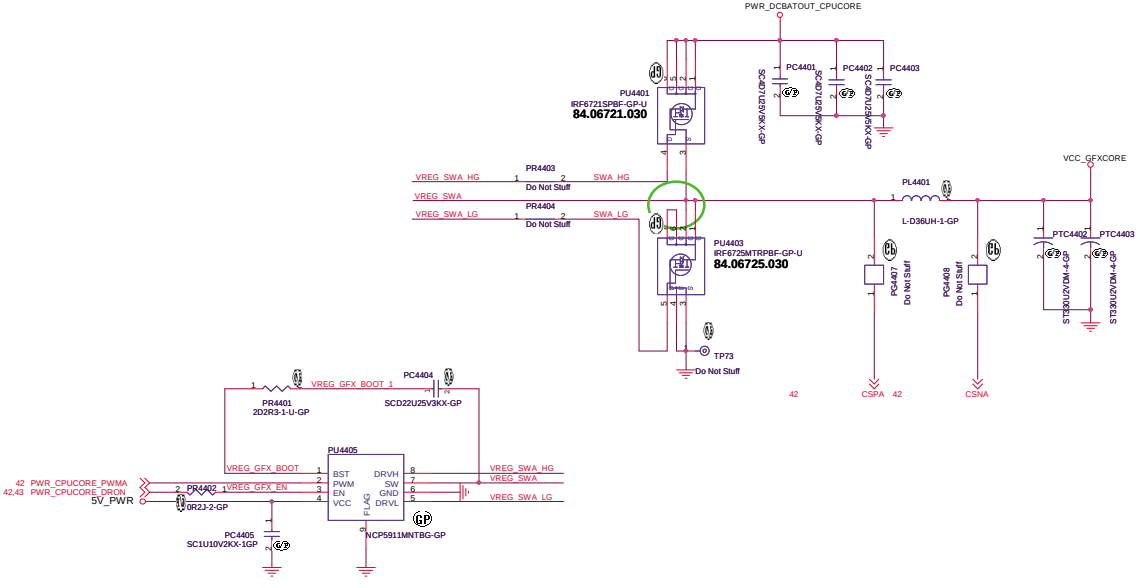


BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

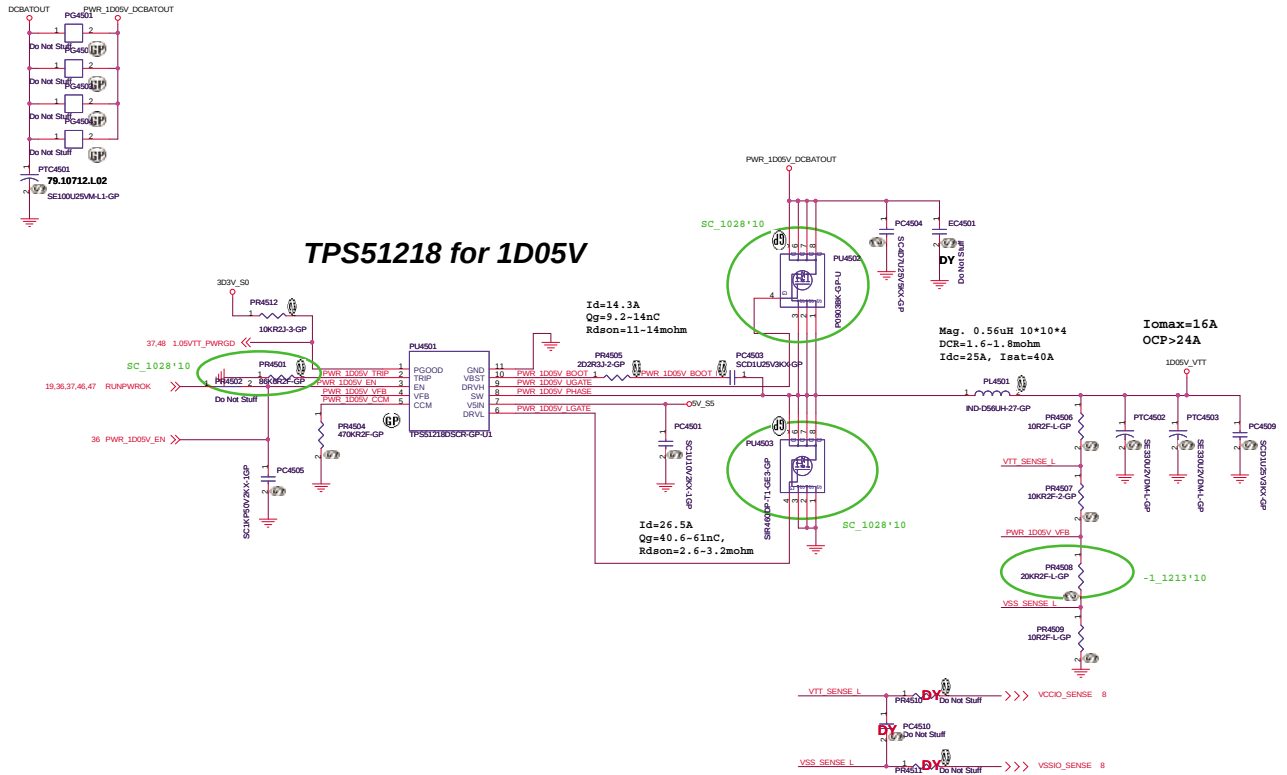
Title	DC/DC CPU CORE1 _NCP6131	
Size	Document Number: LZ57	Rev -1
Date: Thursday, March 31, 2011	Sheet 42 of 102	


DCBATOUT
PWR_DCBATOUT_CPUCORE
PG4320
PG4321
PG4322
PG4323
PG4324
PG4325
PG4326
PG4327
Do Not Stuff
GAP-CLOSE-PWR-3-GP
PTC4301
79.10712.L02
SE100U25VM-L-GP
PTC4308
Do Not Stuff
0Y
PC4301
SCD22U25V3KX-GP
PR4302
2D2R3-1-U-GP
PU4301
NCP5911MNTBG-GP
PWR_VCORE1_BT1
PWR_VCORE1_BT1_R
PWR_VCORE1_EN
PWR_VCORE1_HG
PWR_VCORE1_PH
PWR_VCORE1_LG
42 PWR_CPUCORE_PWM1
42,44 PWR_CPUCORE_DRON
5V_PWR
PR4301
2K74R2F-GP
PC4302
SC1U10V2KX-1GP
PC4306
SCD22U25V3KX-GP
PR4303
2D2R3-1-U-GP
PU4306
PWR_VCORE3_BT3
PWR_VCORE3_BT3_R
PWR_VCORE3_EN
PWR_VCORE3_HG
PWR_VCORE3_PH
PWR_VCORE3_LG
42 PWR_CPUCORE_PWM3
42,44 PWR_CPUCORE_DRON
PR4304
2K74R2F-GP
PC4307
SC1U10V2KX-1GP
PU4307
IRF6721SPBF-GP-U
84.06721.030
PC4308
PC4309
PC4310
SC4D7U25V5KX-GP
PR4309
PWR_VCORE3_HG
VCORE3_HG
PWR_VCORE3_PH
PU4308
IRF6725MTRPBF-GP-U
84.06725.030
PG4313
PG4314
PL4302
L-D36UH-1-GP
PTC4305
PTC4306
PTC4307
SE330U2VDM-L-GP
PR4308
PWR_VCORE3_LG
VCORE3_LG
TP69
CSP3 42
CSN3
VCC_CORE
PU4313
IRF6721SPBF-GP-U
84.06721.030
PC4303
PC4304
PC4305
PR4312
PWR_VCORE1_HG
VCORE1_HG
PWR_VCORE1_PH
PR4313
PWR_VCORE1_LG
VCORE1_LG
PL4301
L-D36UH-1-GP
PU4312
IRF6725MTRPBF-GP-U
84.06725.030
PG4311
PG4312
PTC4303
PTC4304
SE330U2VDM-L-GP
TP71
42
CSP142
CSN1
FOR 3PHASE
DC CPU only
5V_PWR
PR4306
0R2J-2-GP
PR4305
2D2R3-1-U-GP
QC CPU only
PC4311
SCD22U25V3KX-GP
PU4311
PWR_VCORE2_BT2
PWR_VCORE2_BT2_R
PWR_VCORE2_EN
PWR_VCORE2_HG
PWR_VCORE2_PH
PWR_VCORE2_LG
42 PWR_CPUCORE_PWM2
42,44 PWR_CPUCORE_DRON
PR4307
2K74R2F-GP
PC4312
SC1U10V2KX-1GP
NCP5911MNTBG-GP
PU4310
IRF6721SPBF-GP-U
84.06721.030
PC4313
PC4314
PC4315
PR4310
VCORE2_HG
PR4311
VCORE2_LG
PL4303
L-D36UH-1-GP
PU4309
IRF6725MTRPBF-GP-U
84.06725.030
PG4315
PG4316
PTC4310
SE330U2VDM-L-GP
TP70
42
CSP2
CSN2
BOM
Do Not Stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC/DC CPU CORE2 _NCP6131
Size
Document Number
LZ57
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 43 of 102



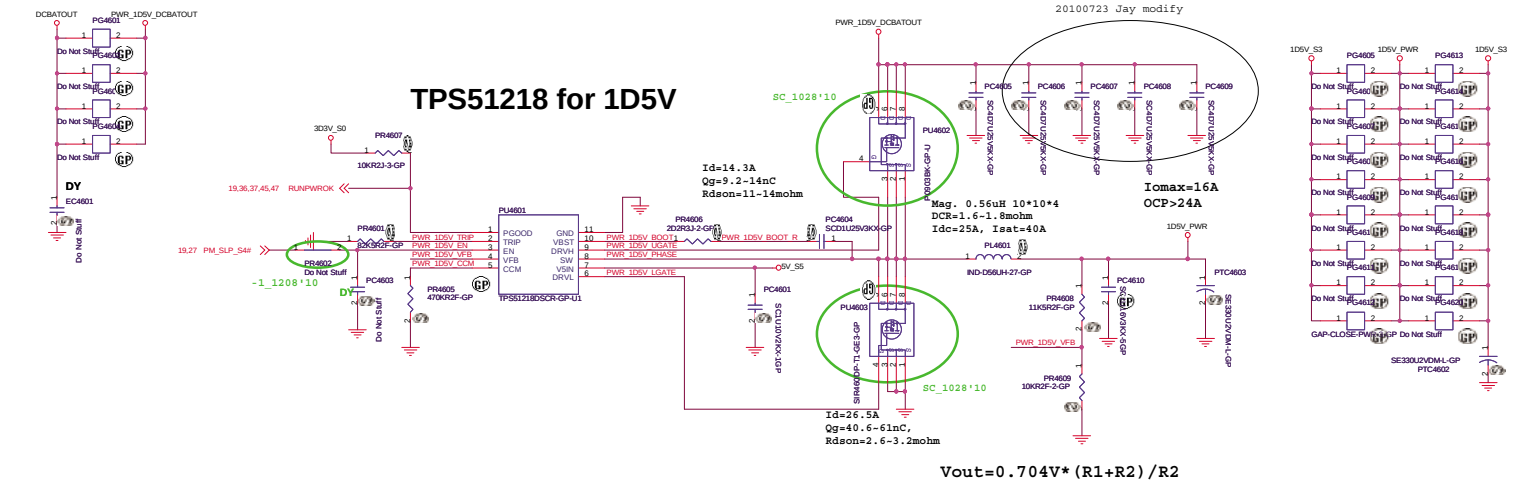
BOM

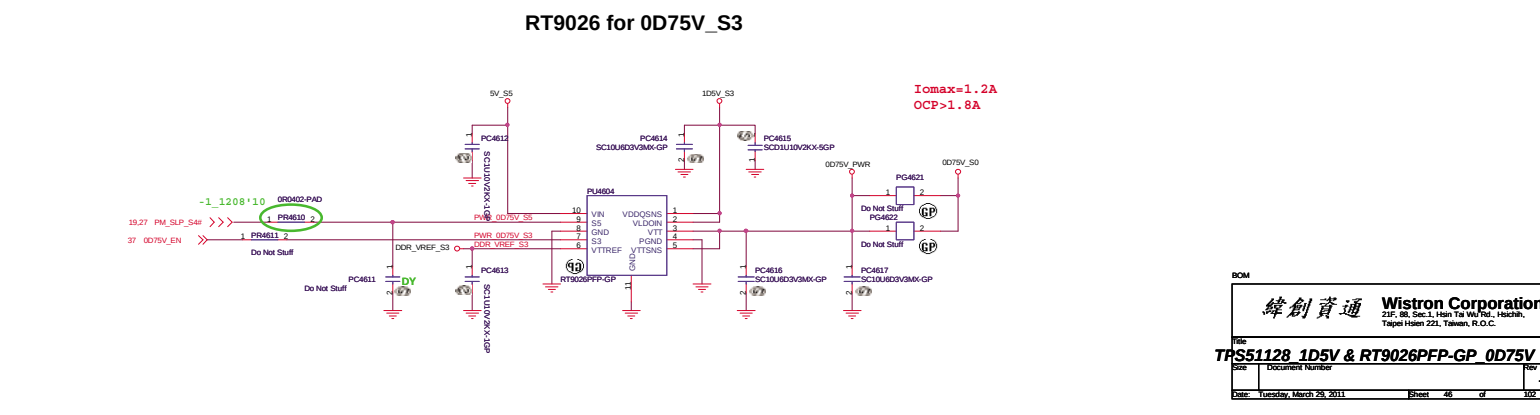
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DC/DC CPU CORE3 _NCP6131***	
Size	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 44 of 102	



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***TPS51218_1D05V***
Size / Document Number	Rev -1
Date: Tuesday, March 29, 2011	Sheet 45 of 102





BOM

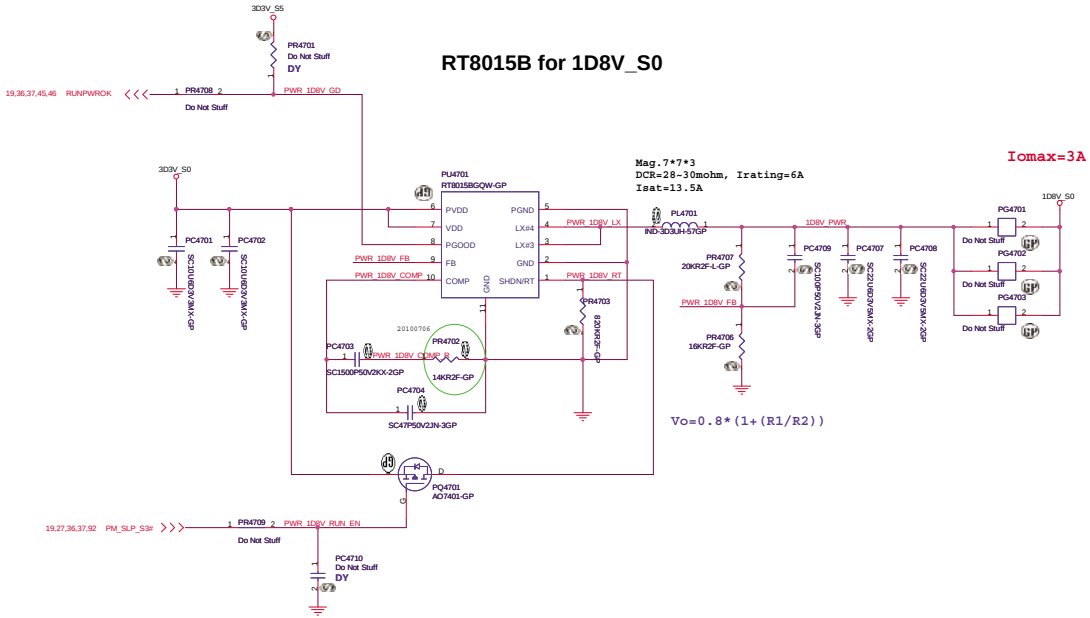
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51128_1D5V & RT9026PFP-GP_0D75V***

Size	Document Number	Rev
		-1

Date: Tuesday, March 29, 2011 Sheet 46 of 102

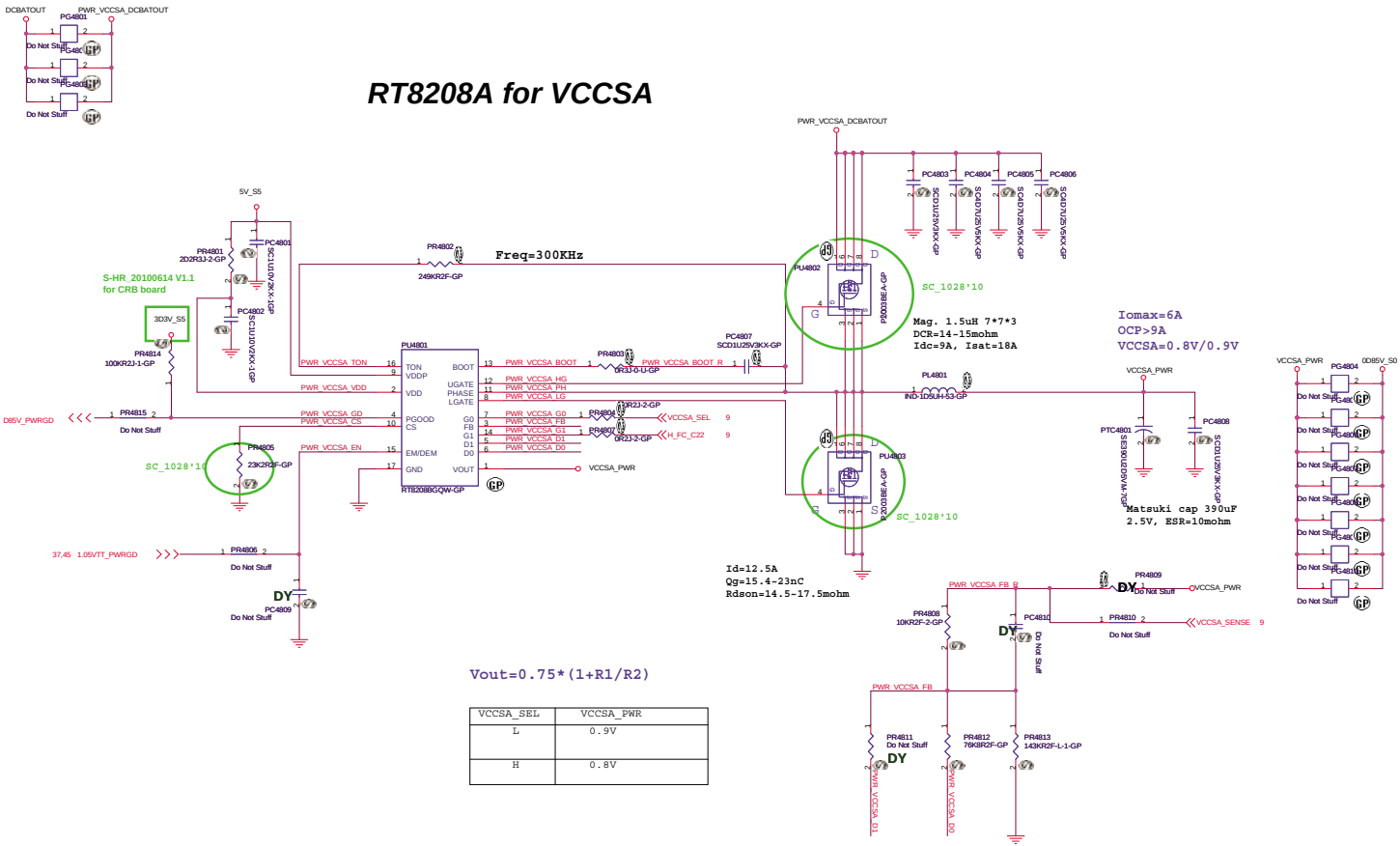
RT9025 for 1D8V_S0



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***1D8V_RT9025***	
Size	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 47 of 102	

RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

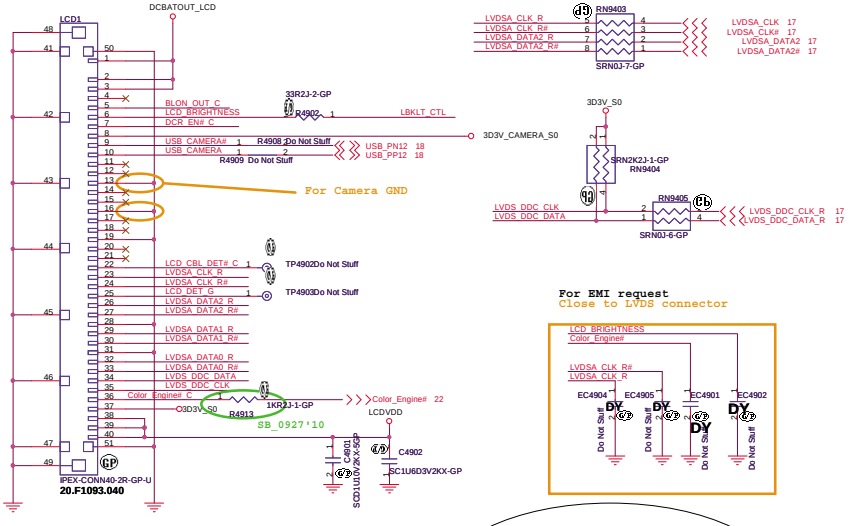
VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

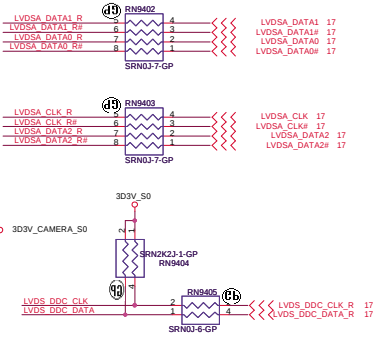
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8208B_VCCSA		
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 48 of 102	

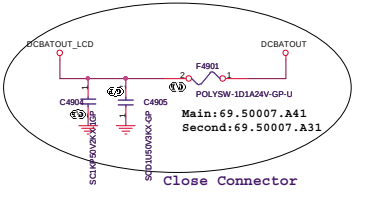
SSID = VIDEO

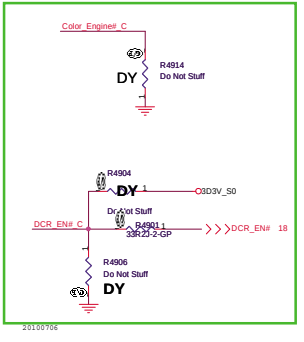
LVDS CONNECTOR



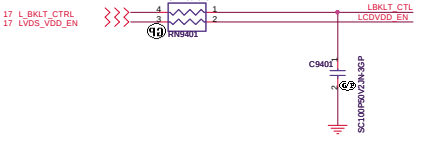


For EMI request
Close to LVDS connector

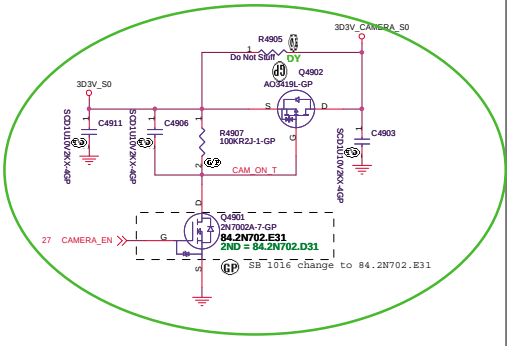




Panel BL brightness/Power En/BL En

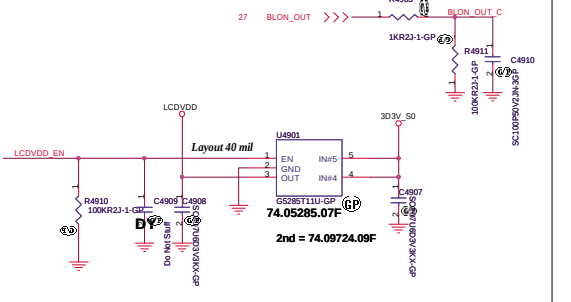


CAMERA POWER



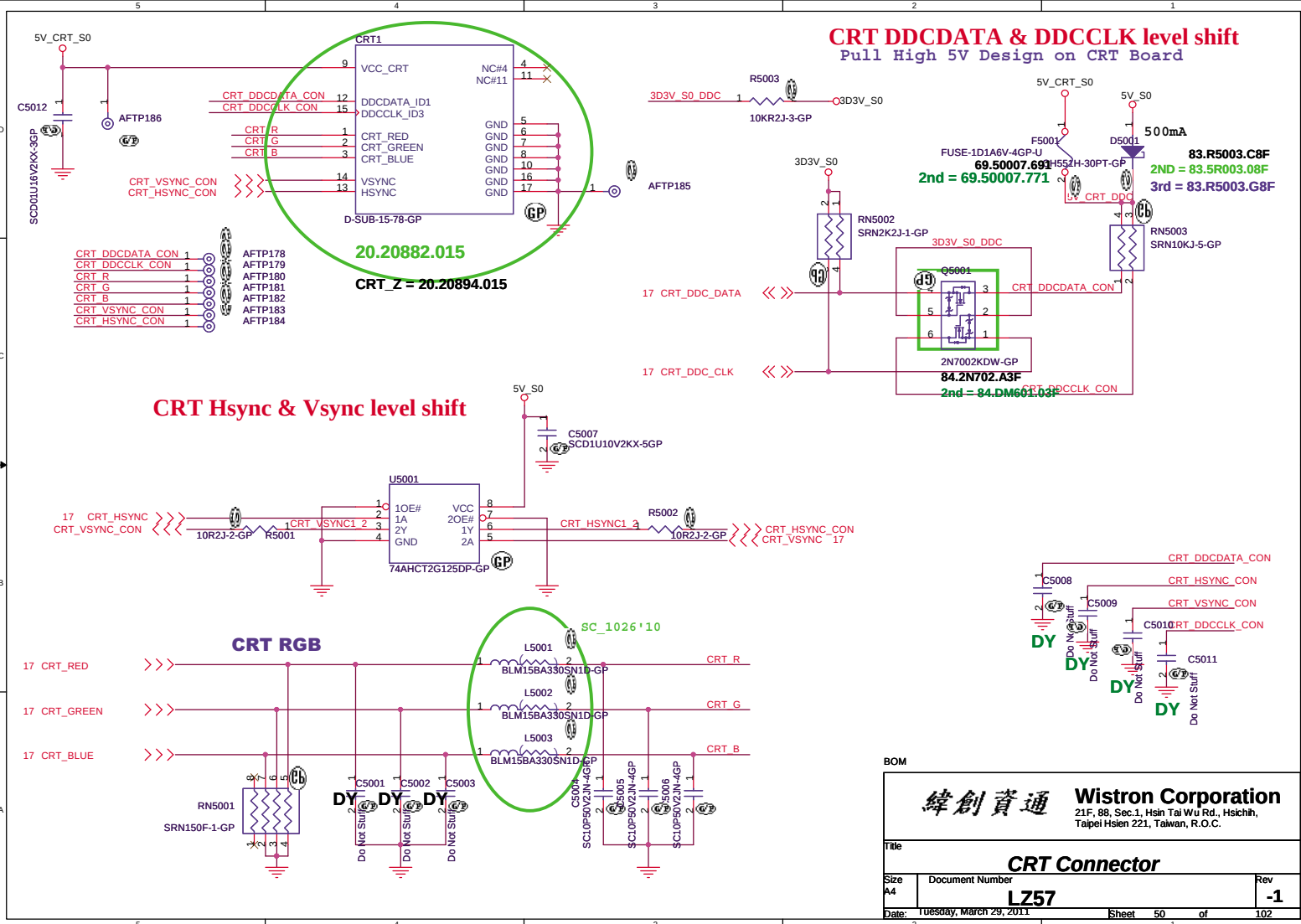
SB 0923'10

SSID = VIDEO



BOM

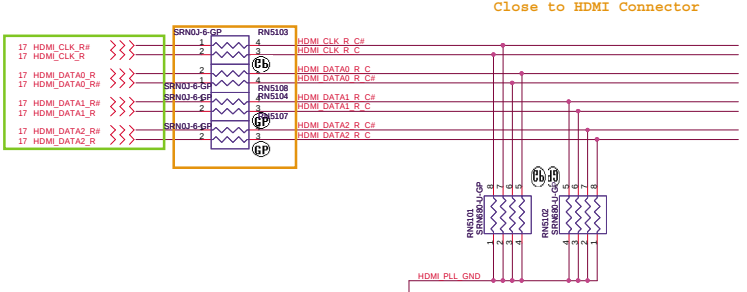
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LCD Connector**	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 49 of 102	

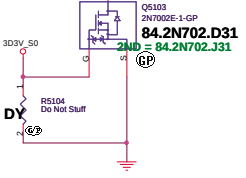

CRT DDCDATA & DDCCLK level shift
Pull High 5V Design on CRT Board
CRT Hsync & Vsync level shift
CRT RGB
CRT1
D-SUB-15-78-GP
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
NC#4
NC#11
GND
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_R
CRT_G
CRT_B
CRT_VSYNC_CON
CRT_HSYNC_CON
5V_CRT_S0
C5012
SCD01U16V2KX-3GP
AFTP186
AFTP185
AFTP178
AFTP179
AFTP180
AFTP181
AFTP182
AFTP183
AFTP184
20.20882.015
CRT_Z = 20.20894.015
R5003
3D3V_S0_DDC
3D3V_S0
10KR2J-3-GP
5V_S0
F5001
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
D5001
500mA
83.R5003.C8F
2ND = 83.5R003.08F
3rd = 83.R5003.G8F
RN5002
SRN2K2J-1-GP
RN5003
SRN10KJ-5-GP
Q5001
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
17 CRT_DDC_DATA
17 CRT_DDC_CLK
CRT_DDCDATA_CON
CRT_DDCCLK_CON
C5007
SCD1U10V2KX-5GP
U5001
74AHCT2G125DP-GP
1OE#
1A
2Y
GND
VCC
2OE#
1Y
2A
17 CRT_HSYNC
CRT_VSYNC_CON
10R2J-2-GP
R5001
CRT_VSYNC1_2
CRT_HSYNC1_2
R5002
CRT_HSYNC_CON
CRT_VSYNC 17
SC_1026'10
L5001
L5002
L5003
BLM15BA330SN1D-GP
17 CRT_RED
17 CRT_GREEN
17 CRT_BLUE
CRT_R
CRT_G
CRT_B
RN5001
SRN150F-1-GP
C5001
C5002
C5003
DY
Do Not Stuff
C5004
C5005
C5006
SC10P50V2JN-4GP
C5008
C5009
C5010
C5011
CRT_DDCDATA_CON
CRT_HSYNC_CON
CRT_VSYNC_CON
CRT_DDCCLK_CON
BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT Connector
Size
A4
Document Number
LZ57
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 50 of 102

SSID = VIDEO

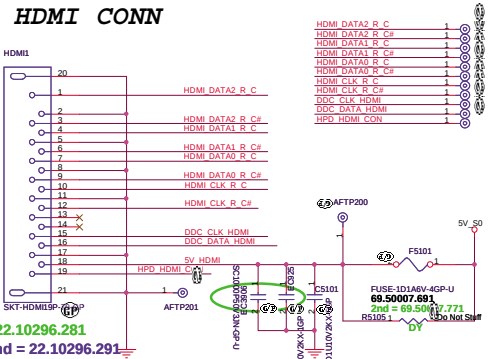
HDMI CONNECTOR

HDMI Passive Level Shifter

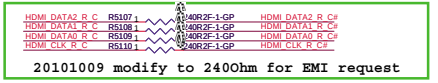


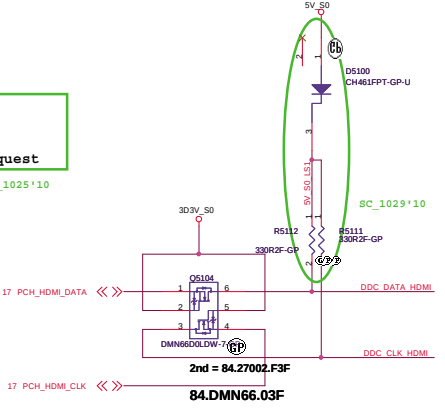


HDMI CONN

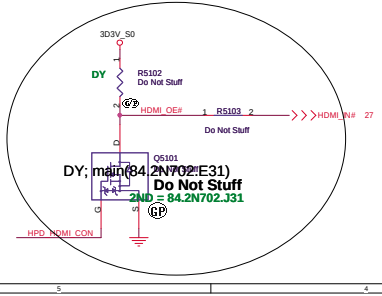


HDMI DDC Passive Level Shifter

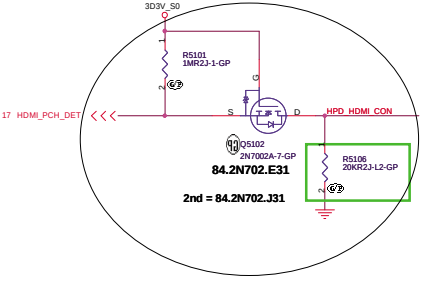




20100727 modify, KBC isn't use.



20100727 follow intel design guide



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI Level Shifter/Connector	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 51 of 102	

(Blanking)

(Blanking)

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	S-VIDEO	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 53 of 102	

(Blanking)

BOM

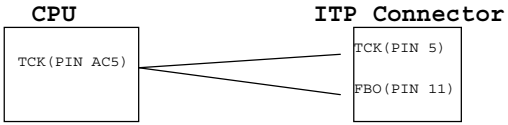
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 54 of 102	

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



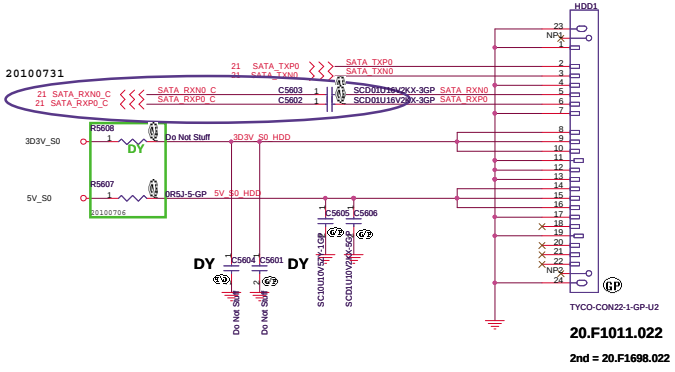
BOM

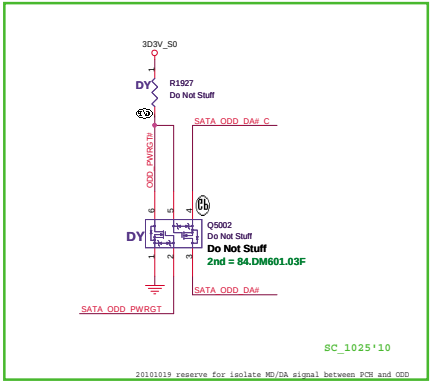
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ITP	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 55 of 102	

SSID = SATA

SATA HDD Connector



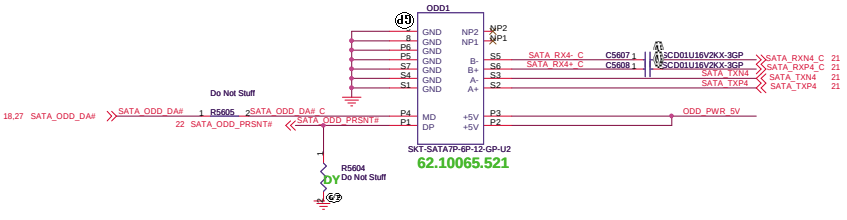


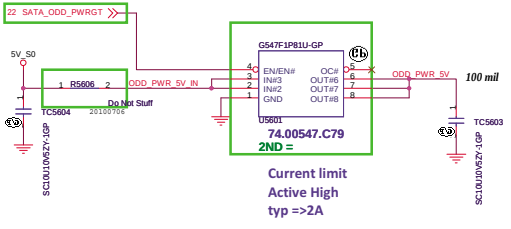
ODD Connector

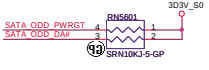
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

SATA Zero Power ODD



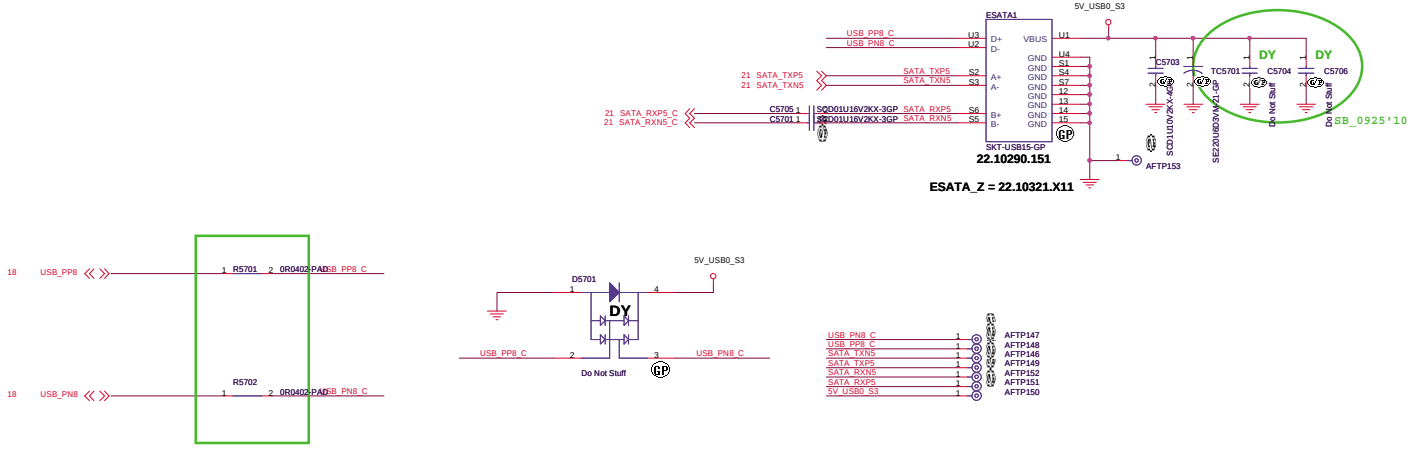




SUPPORT ZERO SATA ODD

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD/ODD	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 56 of 102	



BOM

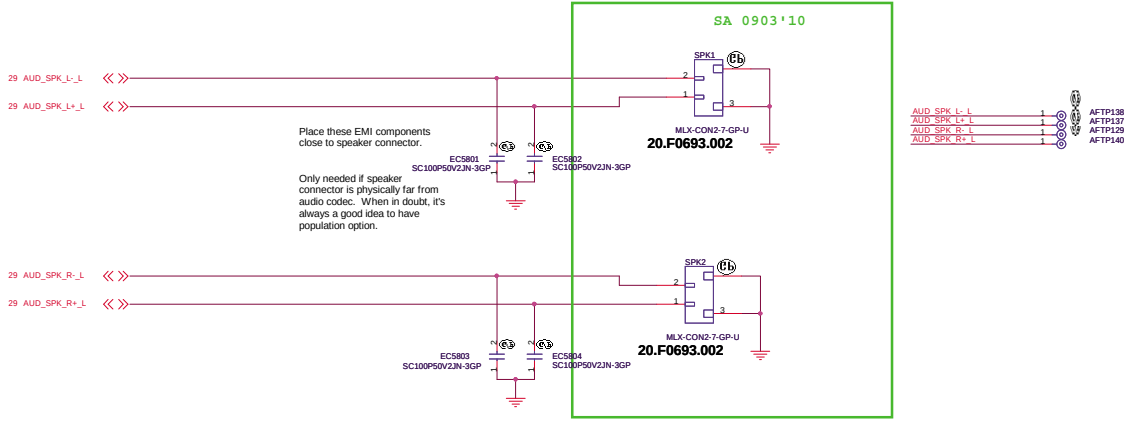
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **E-SATA/LUSB**

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 57 of 102

INTERNAL STEREO SPEAKERS



BOM

緯創資通	**Wistron Corporation** 21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MIC/SPEAKER/AUDIO JACK***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 58 of 102	

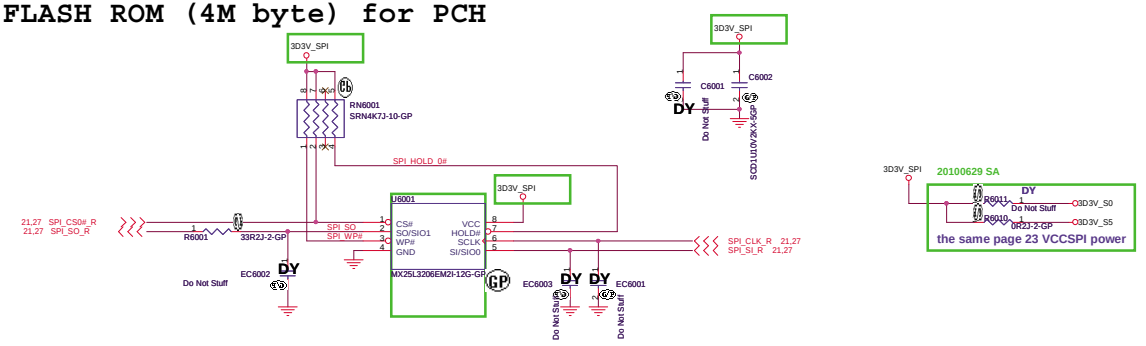
Reserved

BOM

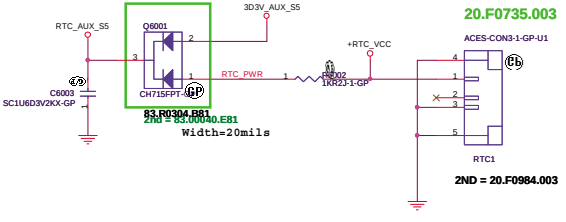
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Reserved***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 59 of 102	

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT

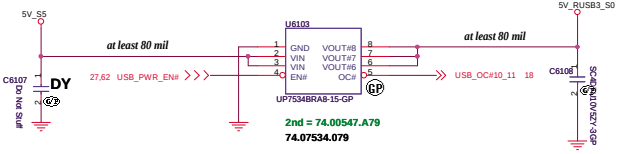


BOM

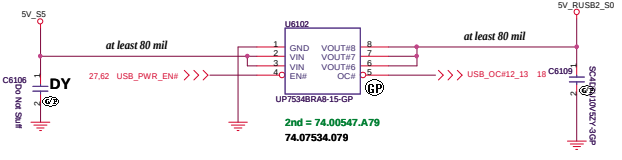
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Flash/RTC	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 60 of 102	

SSID = USB

RJ45_USB Board USB Power



I/O Board USB Power

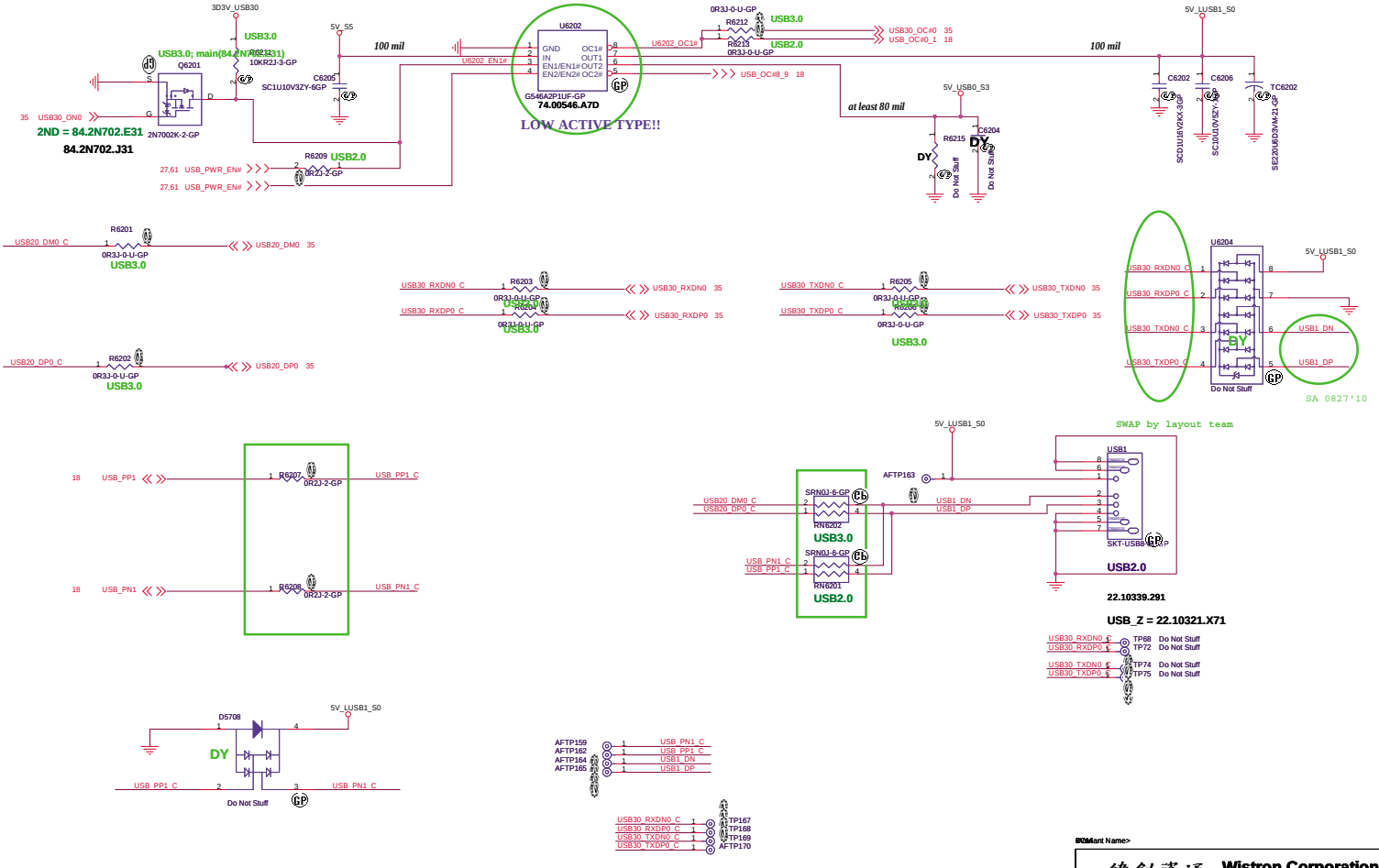


BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB Power SW	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 61 of 102	

Left Side USB Power Switch



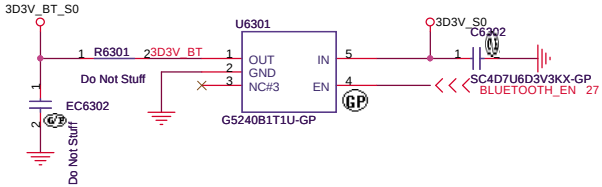
BOM Plant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB 2.0/3.0 Port***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 62 of 102	

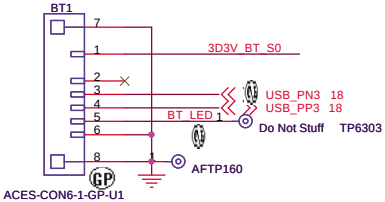
SSID = User.Interface

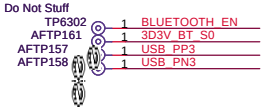
Bluetooth Module conn.

Bluetooth Module



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request



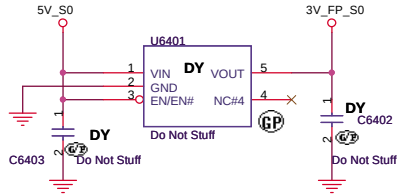


20.F0772.006

2ND = 20.F1804.006

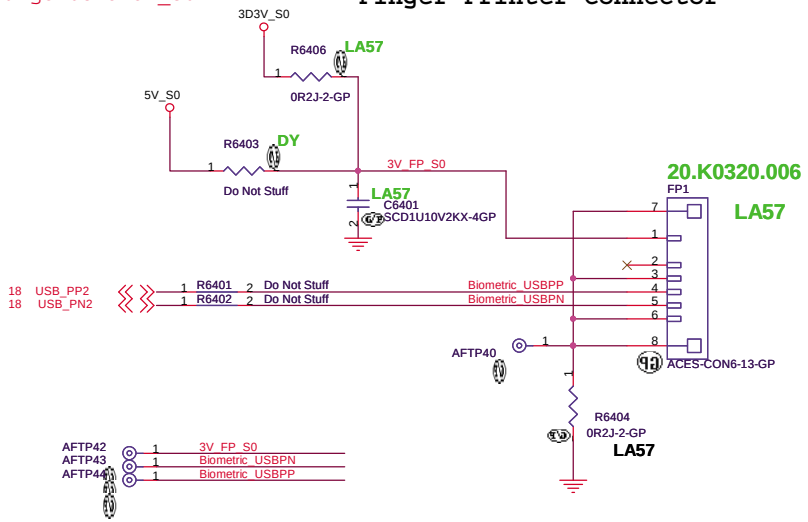
BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Bluetooth	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 63 of 102	



LA47 change to 3D3V_S0

Finger Printer Connector

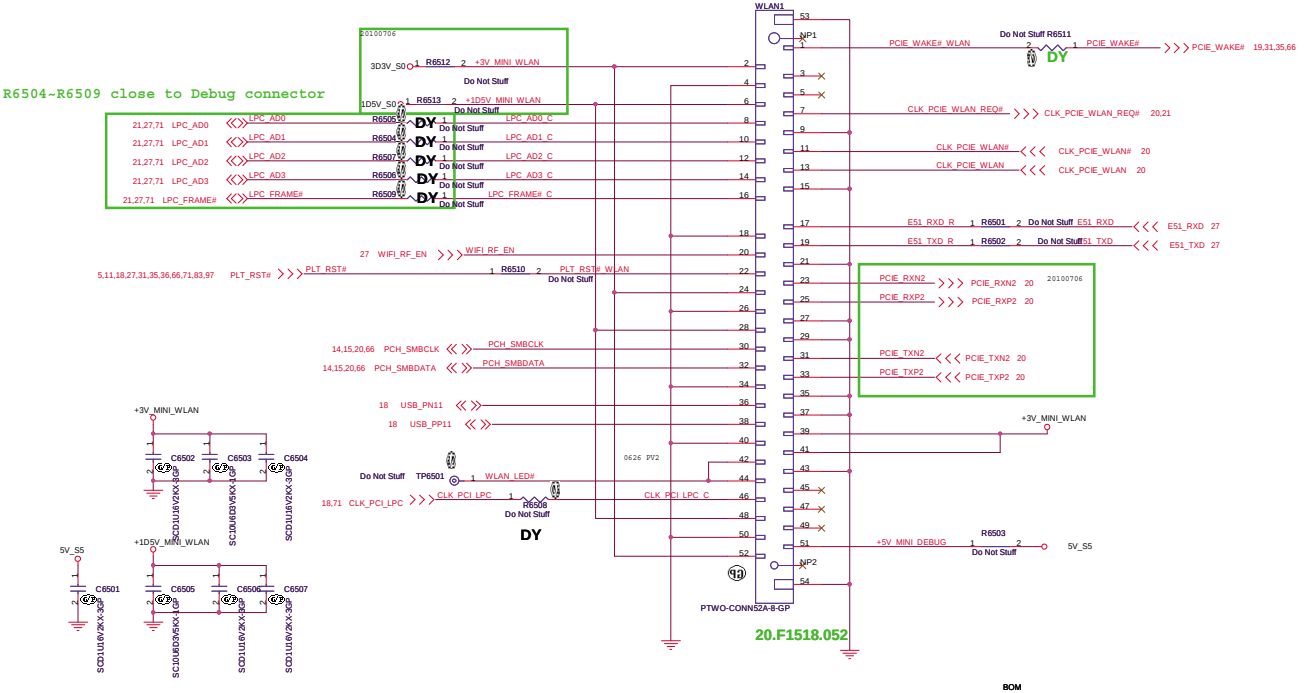


BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RESERVED***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 64 of 102	

SSID = Wireless

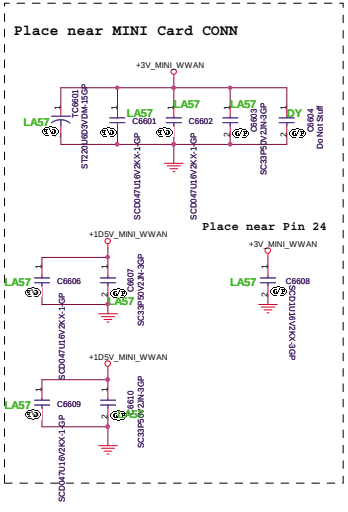
Mini Card Connector(802.11a/b/g/n)

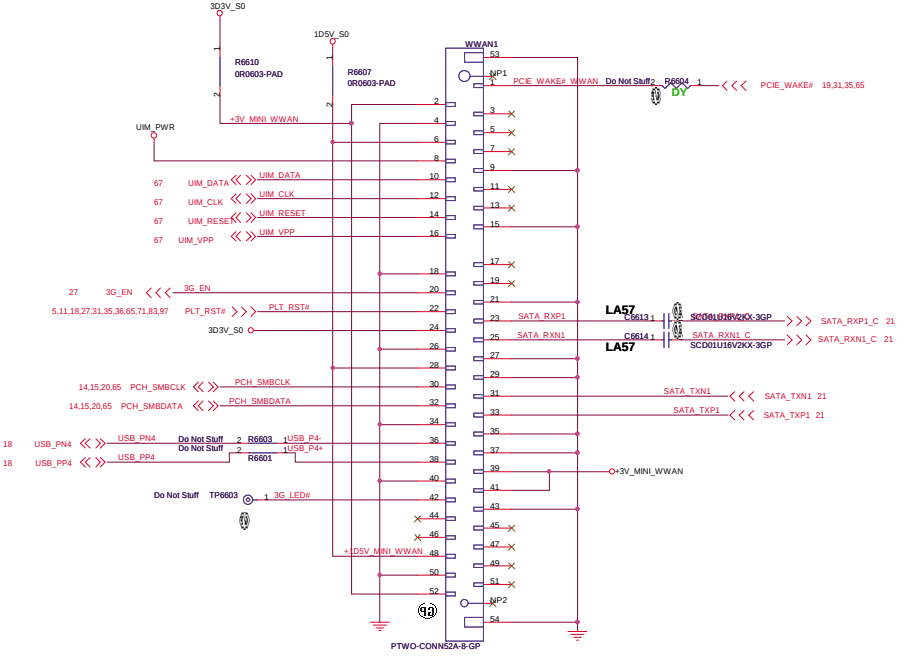


BOM		
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINICARD(WLAN)/ITP CONN	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 65 of 102	

SSID = Wireless

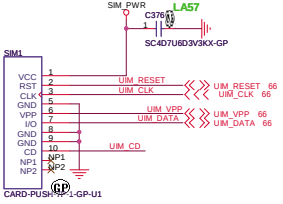
Mini Card Connector(WWAN)





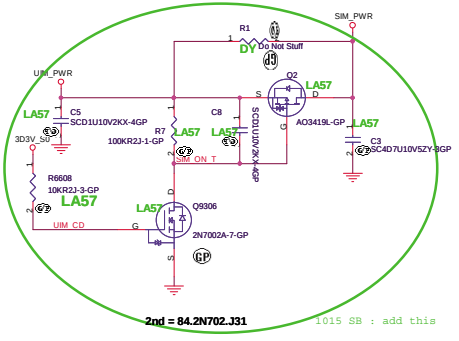
BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	WWAN Connector
Size A3 / Document Number	LZ57
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 66 of 102



LA57

20.I0073.001



2nd = 84.2N702.J31

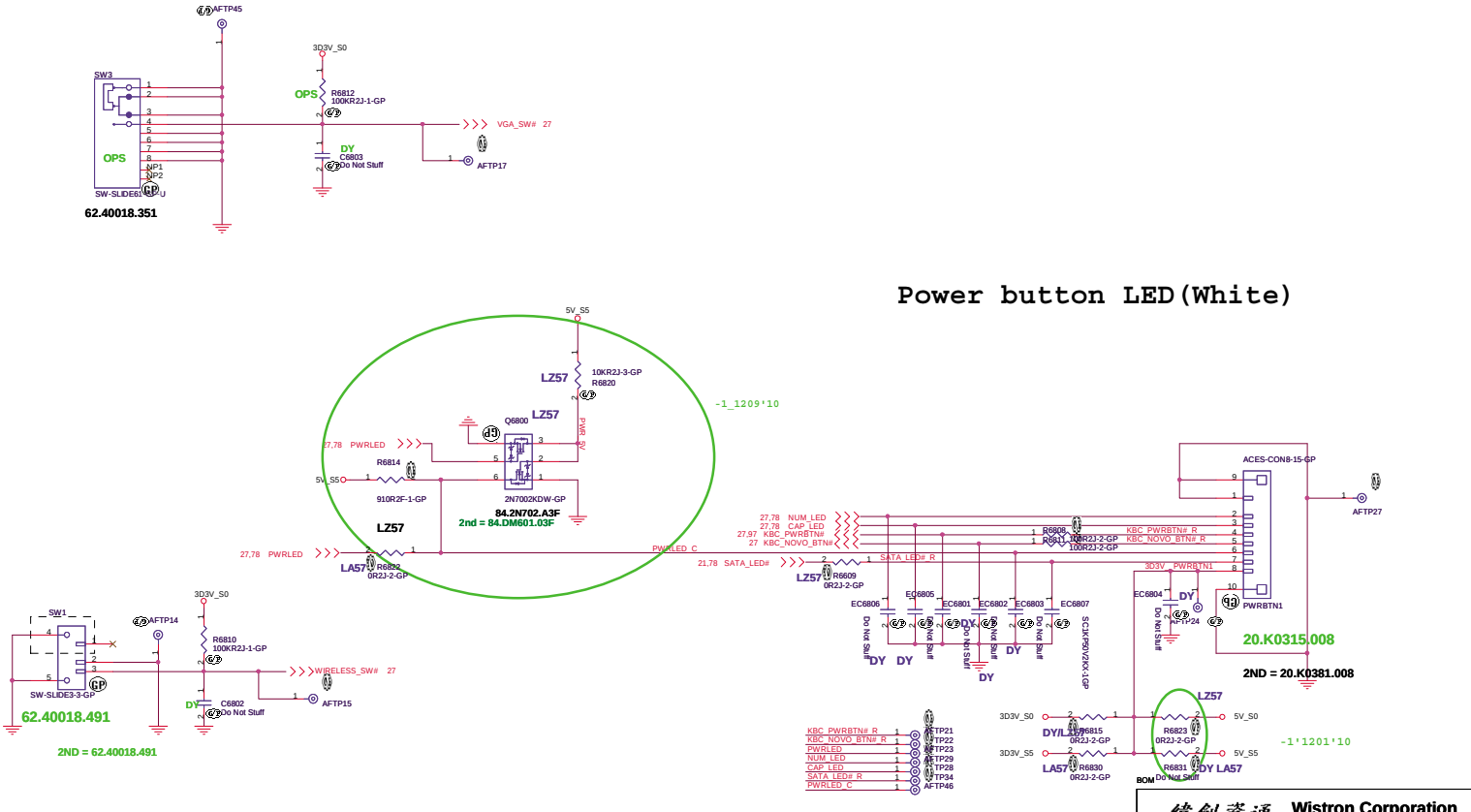
1015 SB : add this

84.2N702.E31

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SIM CARD***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 67 of 102	

SSID = User.Interface



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

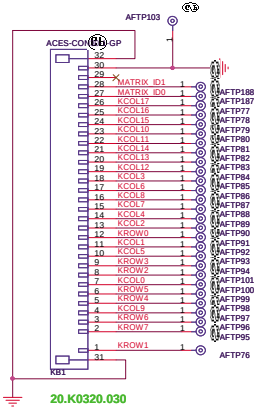
Title: LED Bard/Power Button

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 68 of 102

SSID = KBC

Internal KeyBoard Connector

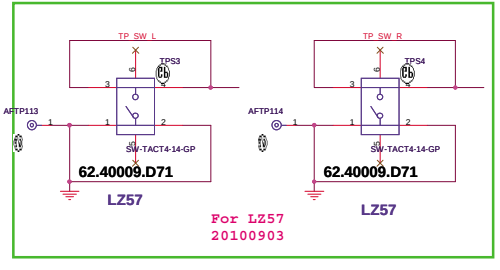


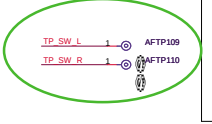
20.K0320.030

ID KEY MATRIX	SENSE			
	27	28	29	30
	ID0	ID1	ID2	GND
US	GND	GND	X	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

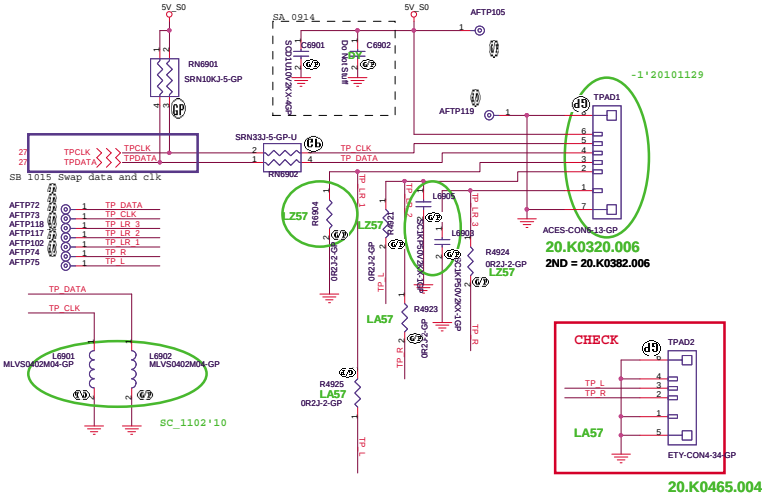
KROW[0..7] 27

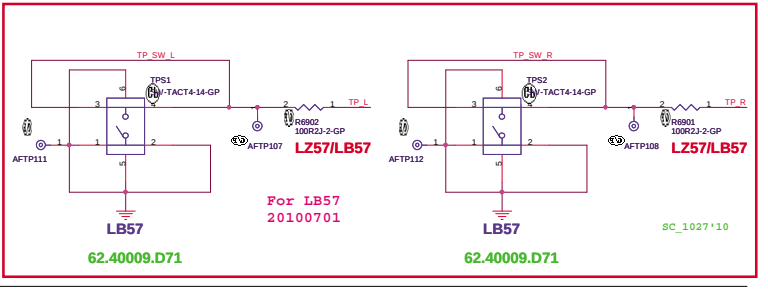
KCOL[0..17] 27





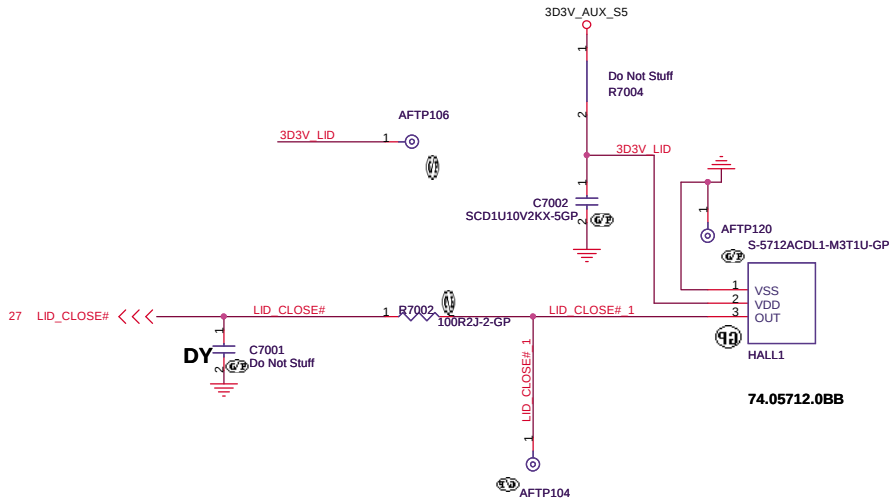
SSID = Touch.Pad





BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Key Board/Touch Pad	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 69 of 102	



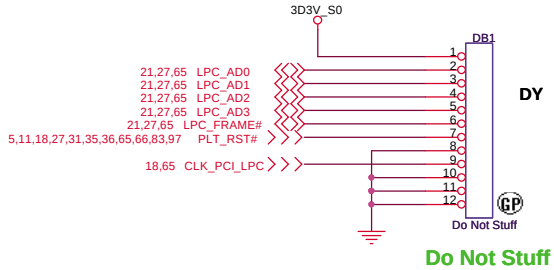
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 70 of 102



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Dubug connector***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 71 of 102	

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 72 of 102	

(Blanking)

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 73 of 102

BOM

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***CARD Reader CONN***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 74 of 102	

BOM

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***New Card***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 75 of 102	

(Blanking)

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 76 of 102	

(Blanking)

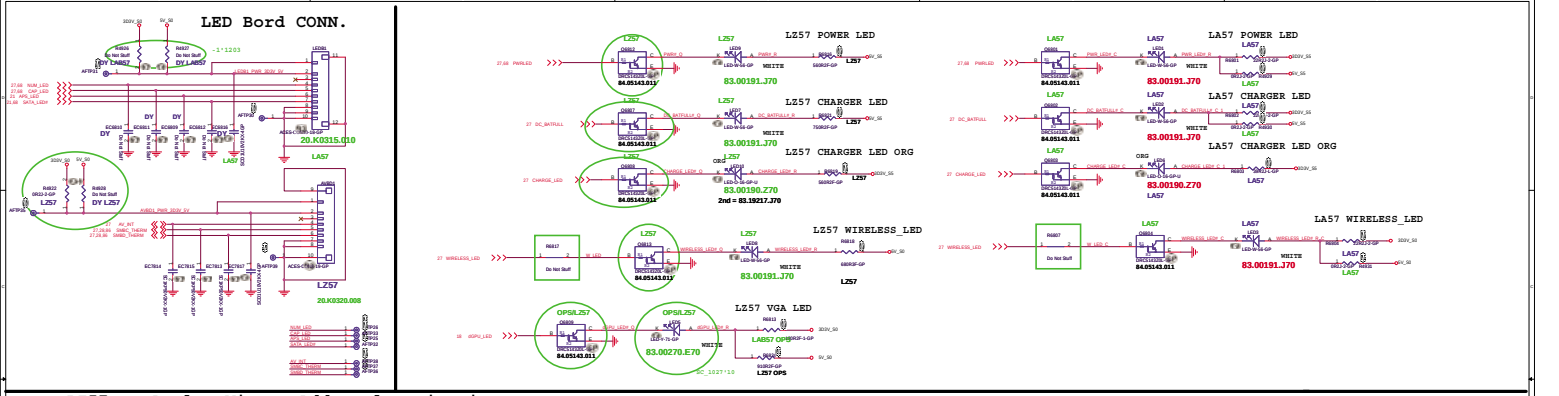
BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

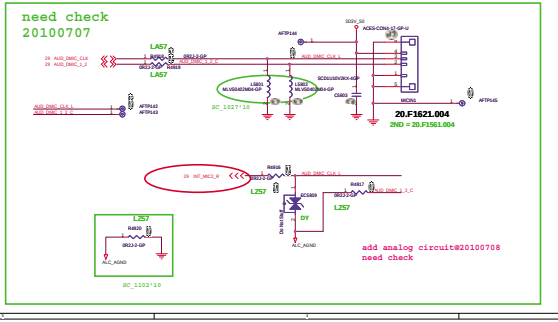
Title: ***Reserved***

Size	Document Number	Rev
A4	LZ57	-1

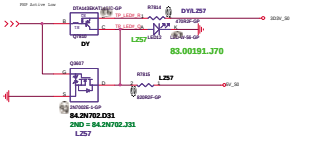
Date: Tuesday, March 29, 2011 Sheet 77 of 102



LZ57 => Analog Mic => Add analog circuit.
LA57 => Digital Mic



LZ57 Touch Pad LED



ACMs Designer

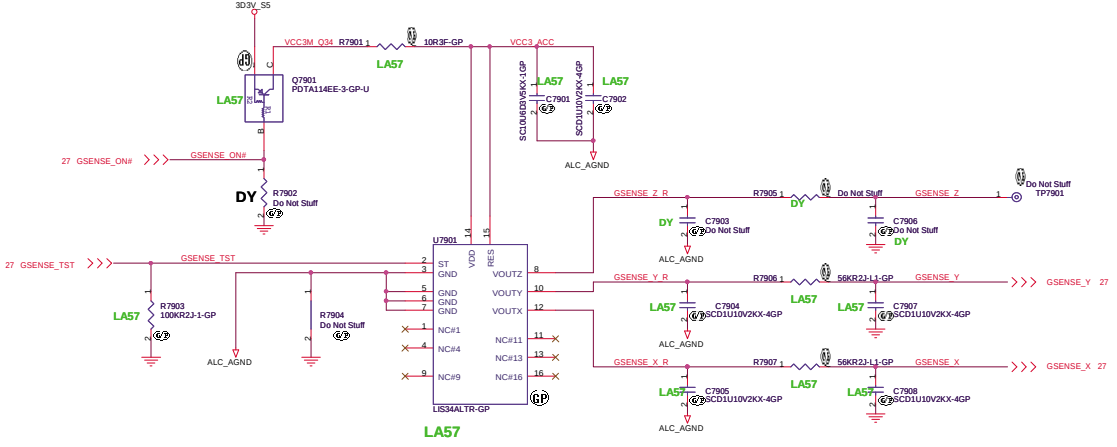
Wistron Corporation
20F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

LEDB/LED

Size	Document Number	Rev
	LZ57	-1

Date: Thursday, March 25, 2010 Sheet 26 of 28

G-Sensor



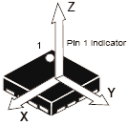
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G-Sensor

Size	Document Number	Rev
Custom	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 79 of 102

(Blanking)

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 80 of 102	

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

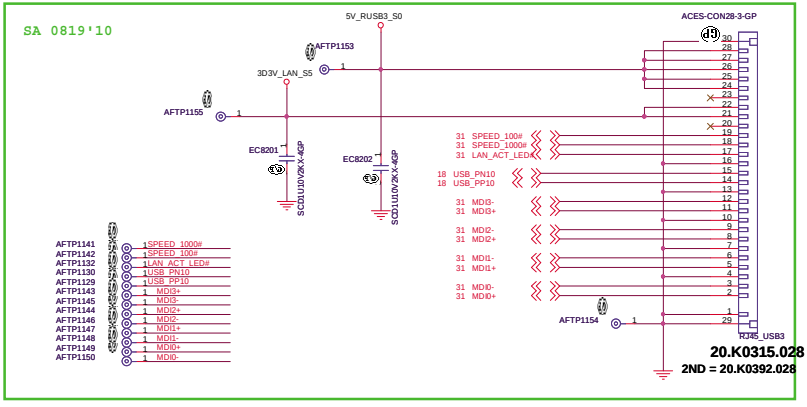
Title

Reserved

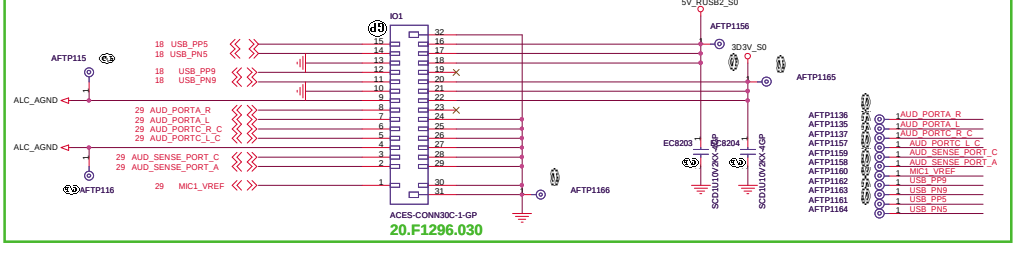
Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 81 of 102

RJ45_USB CONN.

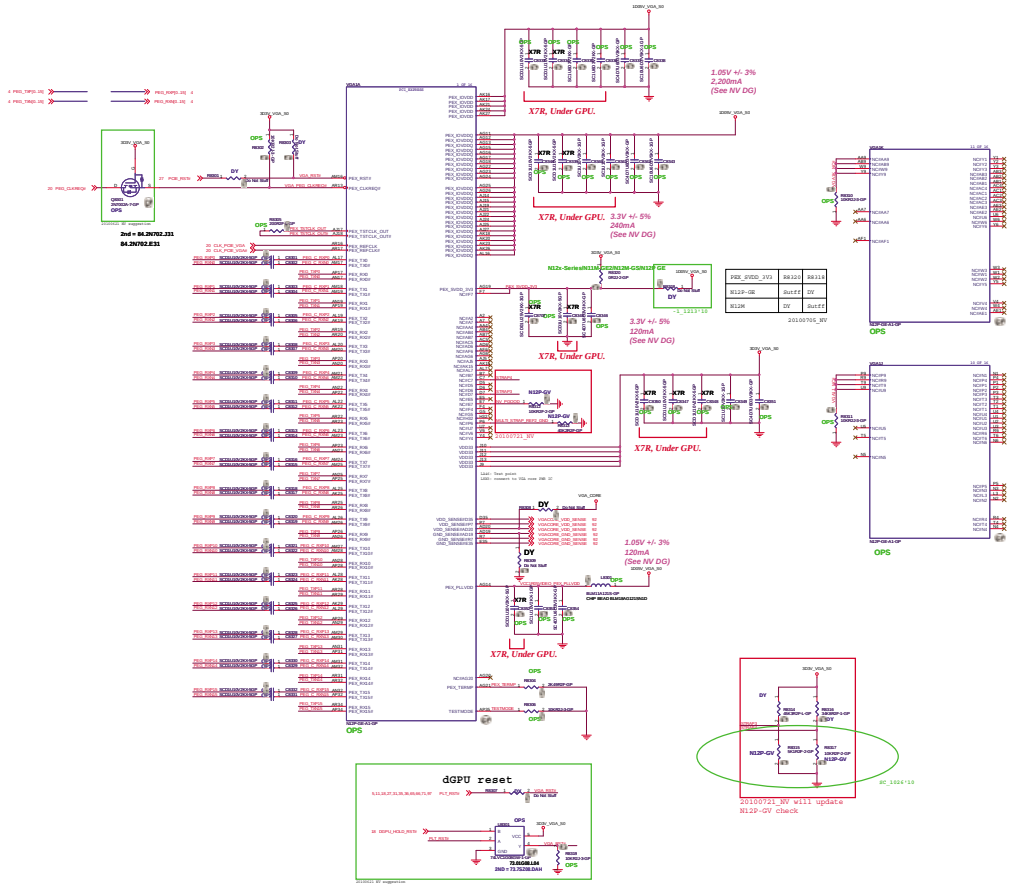


Card Reader Board CONN.

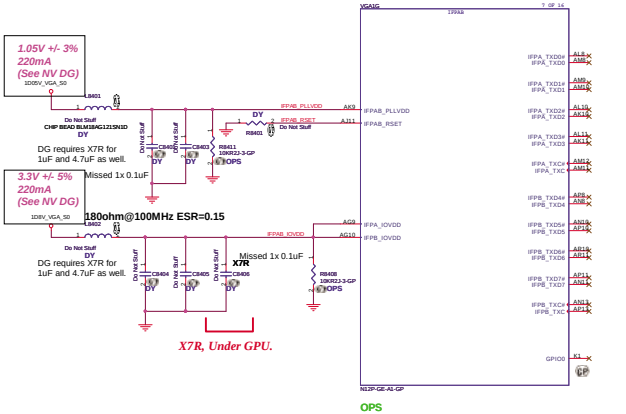


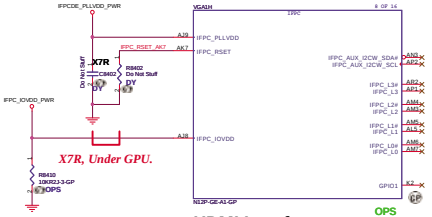
BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	IO Board Connector	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 82 of 102	

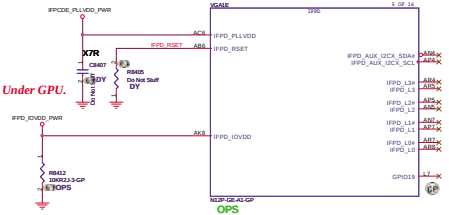

1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
3.3V +/- 5%
240mA
(See NV DG)
3.3V +/- 5%
120mA
(See NV DG)
1.05V +/- 3%
120mA
(See NV DG)
2nd = 84.2N702.331
84.2N702.E31
N12x-Series(N11M/N12P/N12M-GS/N12P-GE
PEX_SVDD_3V3 R9325 R9316
N12P-GE Suff DY
N12M DY Suff
20100705_NV
20100721_NV will update
N12P-GV check
dGPU reset
Wistron Corporation
N12P-GE(1/6): PEG I/F
LZ57
-3

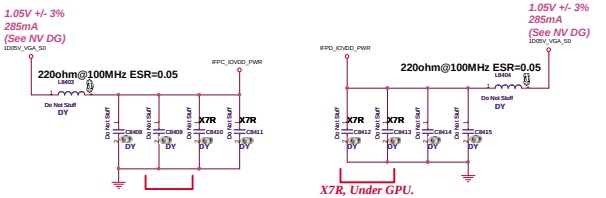
LVDS Interface

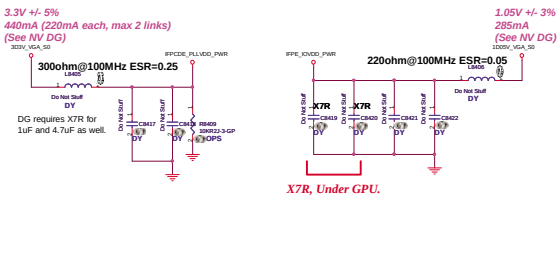


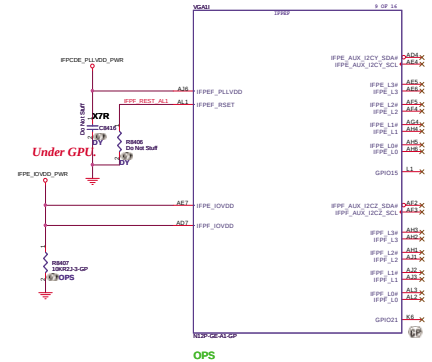


HDMI Interface



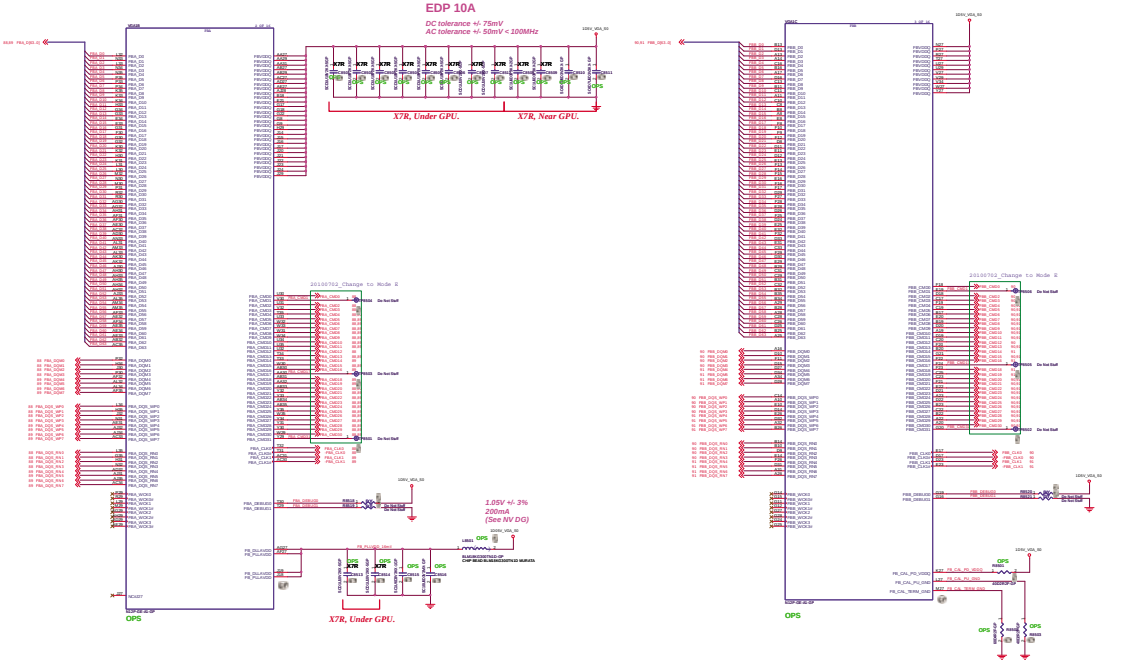


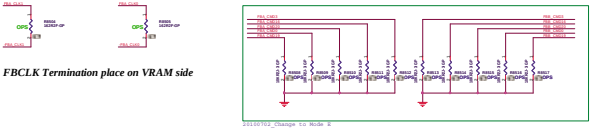




BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	N12P-Q1/Q3 (2/6): DIGITAL OUT
Size: A2	Document Number: LZ57
Rev: -1	
Date: Tuesday, March 29, 2011	Sheet 84 of 102

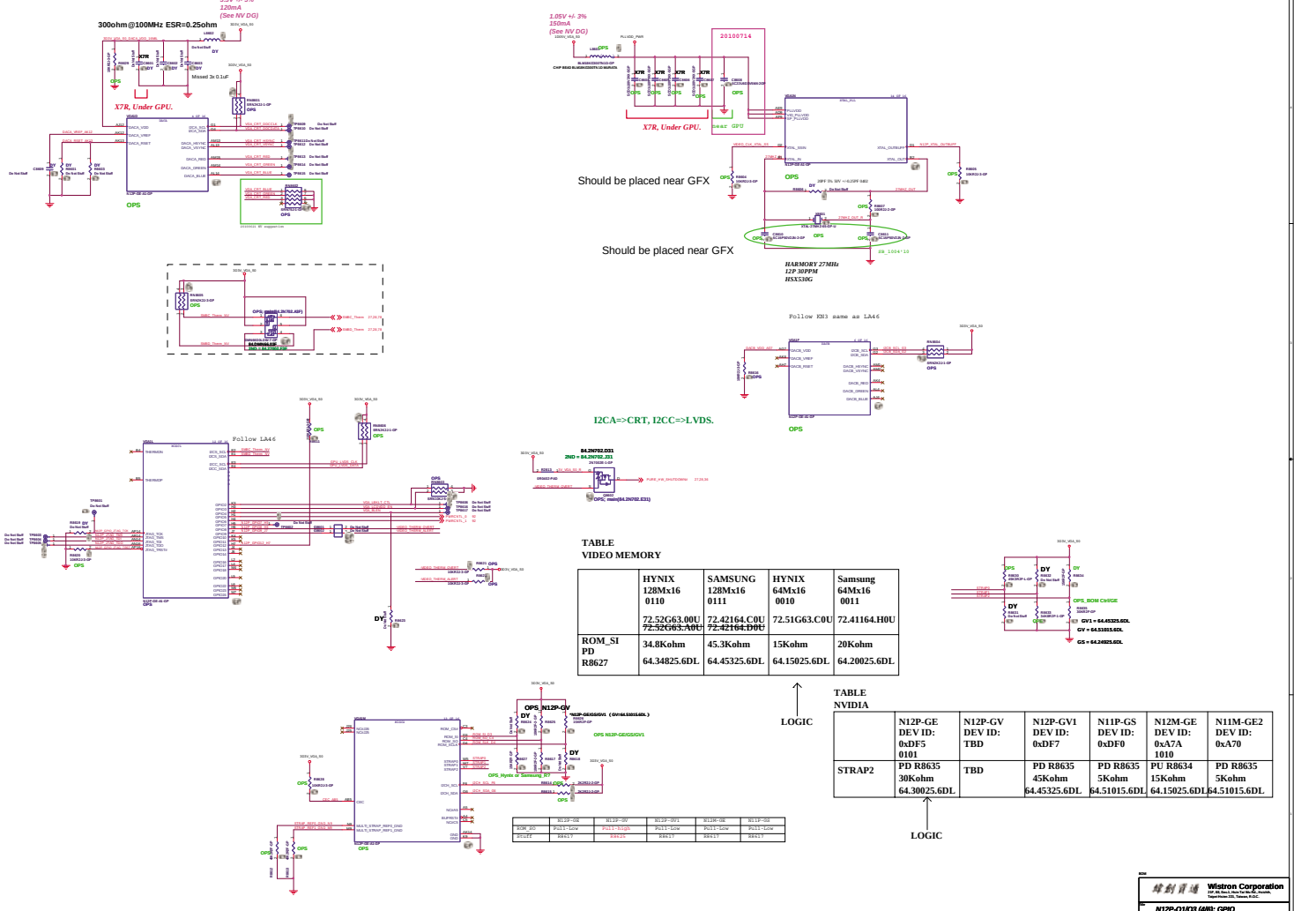




FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

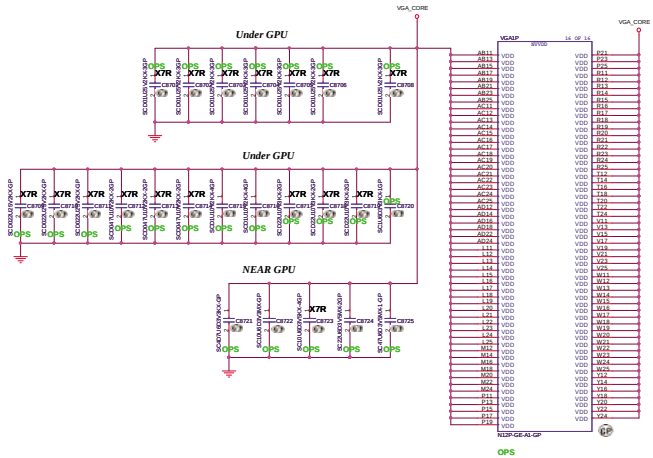
Wistron Corporation		
N12P-Q1/Q3 (3/6): VRAM IF		
LZ57		3

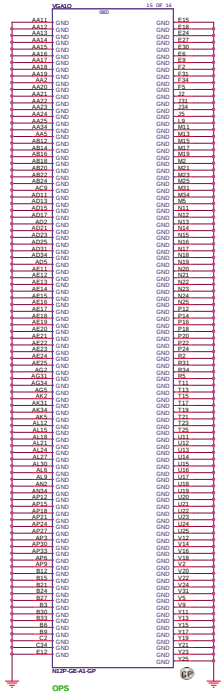


	HYNIX 128Mx16 0110 72.52G63.00U ~~72.52G63.A0U~~	SAMSUNG 128Mx16 0111 72.42164.C0U ~~72.42164.D0U~~	HYNIX 64Mx16 0010 72.51G63.C0U	Samsung 64Mx16 0011 72.41164.H0U
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: TBD	N12P-GV1 DEV ID: 0xDF7	N11P-GS DEV ID: 0xDF0	N12M-GE DEV ID: 0xA7A 1010	N11M-GE2 DEV ID: 0xA70
STRAP2	PD R8635 30Kohm 64.30025.6DL	TBD	PD R8635 45Kohm 64.45325.6DL	PD R8635 5Kohm 64.51015.6DL	PU R8634 15Kohm 64.15025.6DL	PD R8635 5Kohm 64.51015.6DL

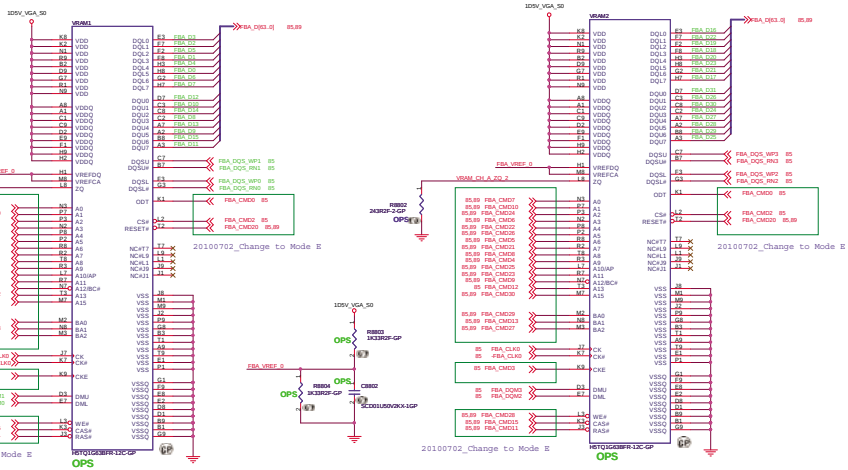
	N12P-GE	N12P-GV	N12P-GV1	N11P-GE	N11P-GS
ROM_SO	Pull-Low	Pull-high	Pull-Low	Pull-Low	Pull-Low
Stuff	R8617	R8625	R8617	R8617	R8617



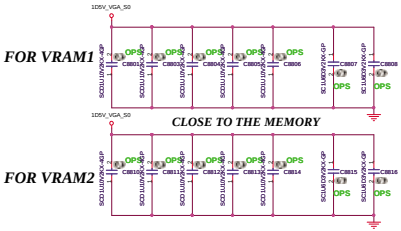


BOM

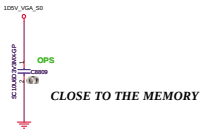
蜂創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title:	N12P-Q1/Q3 (5/6): POWER		
Size: A2	Document Number: LZ57		Rev: -1
Date: Tuesday, March 29, 2011	Sheet 87 of 100		



FB CMD mapping Mode D-N12x



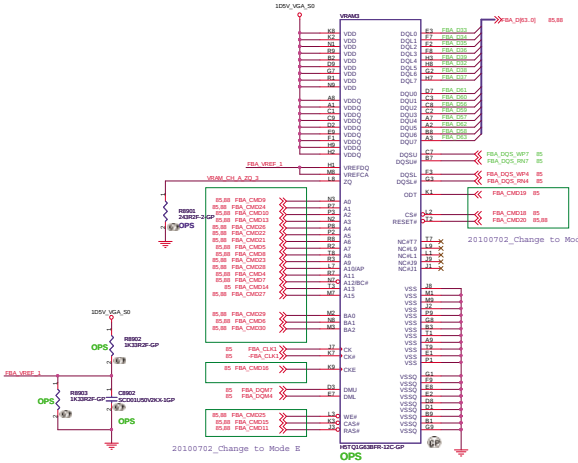
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

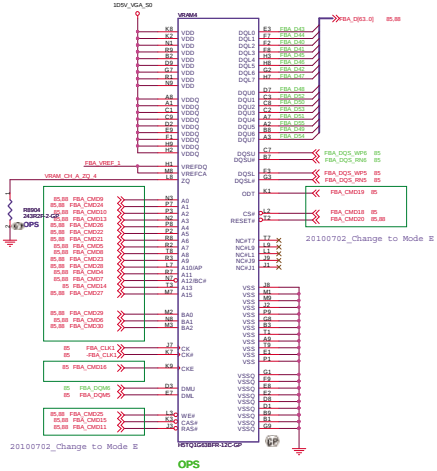


VIDEO FRAME BUFFER PORT A

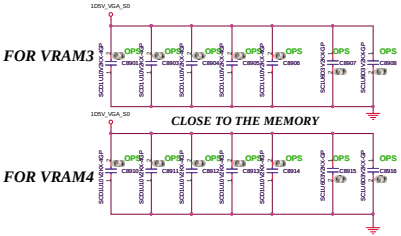
BOM

蜂創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	VRAM CHANNEL-A		
Size A2	Document Number LZ57		Rev -1
Date: Tuesday, March 29, 2011	Sheet 88 of 102		





FB CMD mapping Mode D-N12x



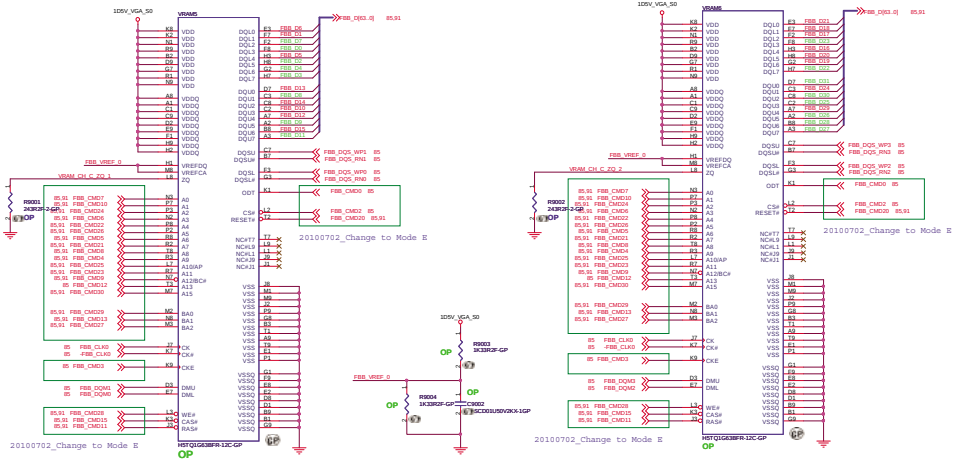
CLOSE TO THE MEMORY

CLOSE TO THE MEMORY

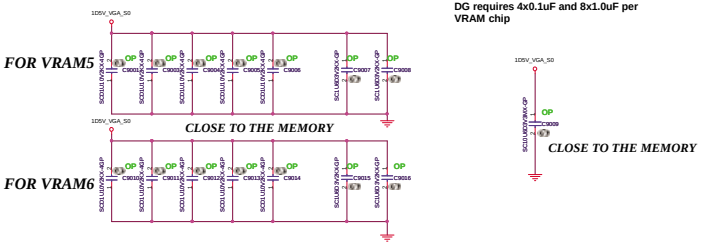
VIDEO FRAME BUFFER PORT A

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	VRAM CHANNEL-A	
Size A2	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 89 of 102	



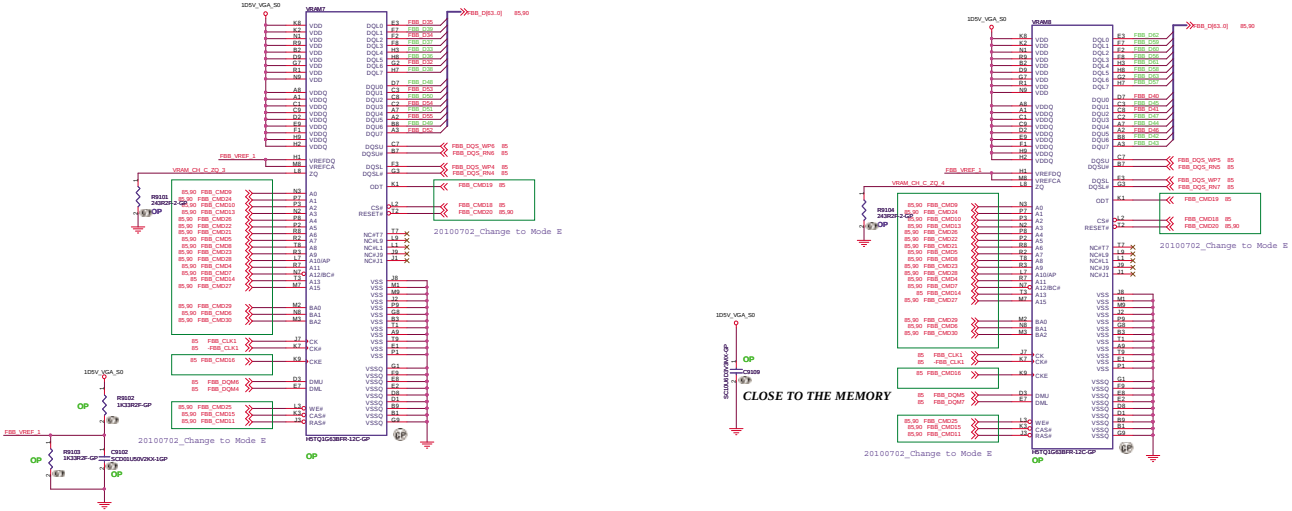
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

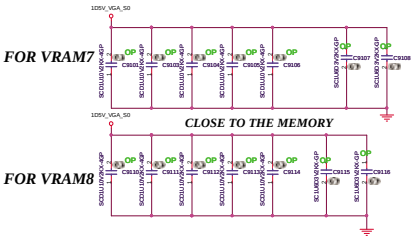


VIDEO FRAME BUFFER PORT C

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	VRAM CHANNEL-C
Size	Document Number Rev



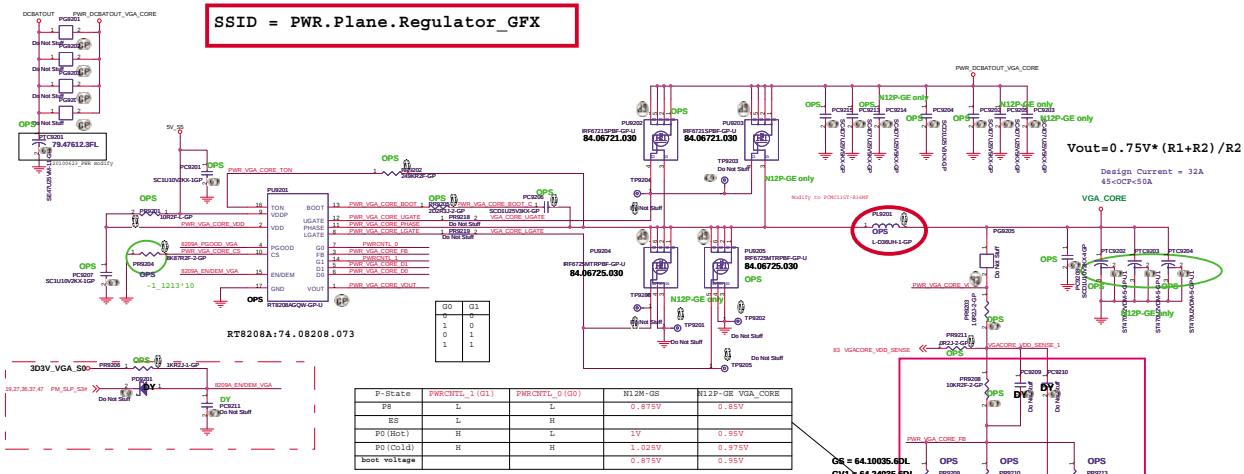


VIDEO FRAME BUFFER PORT C

BOM

緯創資通	Wistron Corporation 22F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VRAM CHANNEL-C	
Size A2	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 31 of 102	

SSID = PWR.Plane.Regulator_GFX



P-State	PWRCNTL_1(G1)	PWRCNTL_0(G0)	N12M-GS	N12P-GE VGA_CORE
P8	L	L	0.875V	0.85V
KS	L	H		
P0(Hot)	H	L	1V	0.95V
P0(Cold)	H	H	1.025V	0.975V
boot voltage			0.875V	0.95V

P-State	N12P-GE	N12P-GV	N12P-GV1	N12M-GS	N12M-GE	N11M-GE2
P0(Cold)	0.998V	1.025	0.925	1V	1.00V	1.00V
P0(Hot)	0.971V	1	0.875	1.025V		
P8	0.86V	0.85V	0.825V	0.875V	0.85V	0.85V
P12	0.86V	0.85V	0.825V		0.85V	0.85V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

	N12P-GE	N12P-GV1	N12P-GV	N12P-GS
P0(Cold)	0.998V	0.946V	1.048V	
P0(Hot)	0.971V	0.915V	1.011V	
P8/P12	0.86V	0.833V	0.86V	
Boot Voltage	0.971V	0.915V	0.86V	
PR9209	270k(64.27035.6DL)	240k(64.24035.6DL)	200k(64.20035.6DL)	
PR9210	68k(64.68025.6DL)	90.9k(64.90925.6DL)	68k(64.68025.6DL)	
PR9213	68k(64.68025.6DL)	90.9k(64.90925.6DL)	49.9k(64.49925.6DL)	

BOM

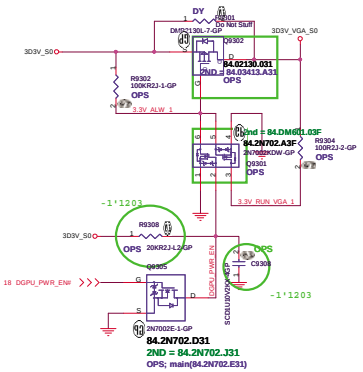
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC_VGA CORE_RT8208B

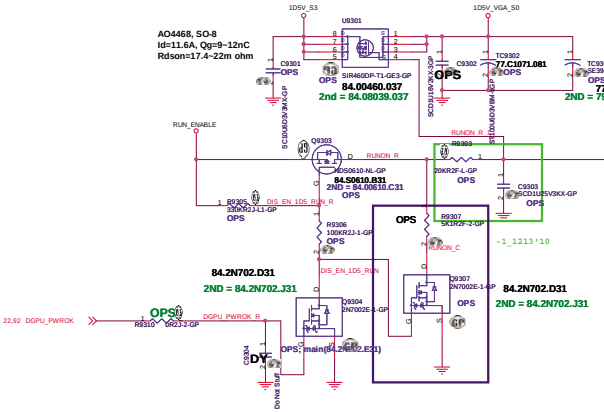
Size: | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 52 of 102

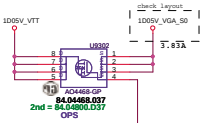
+3VS to 3.3V_DELAY Transfer



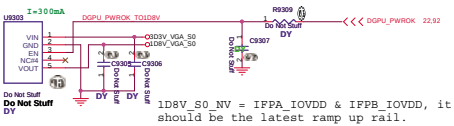
1D5V_VGA_S0



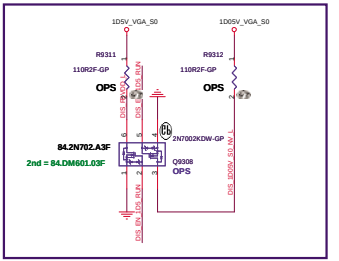
1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.



BOM

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER VGA BOARD

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BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 26, 2013 Sheet 54 of 102

(Blanking)

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT Switch***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 95 of 102	

BOM

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***TOUCH PANEL***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 96 of 102	

CPU Plate

H13 Do Not Stuff — Do Not Stuff
H14 Do Not Stuff — Do Not Stuff
H15 Do Not Stuff — Do Not Stuff

VGA Std-Off

H10 STF237R128H42-GP — OPS — 34.4GD01.101
H11 STF237R128H42-GP — 34.4GD01.101

Check test point

3D3V_S0		TP8507	Do Not Stuff
3D3V_AUX_S5		TP8508	Do Not Stuff
3D3V_S5		TP8509	Do Not Stuff
5V_S5		TP8510	Do Not Stuff
11,19,27	PM_PWRBTN#	TP8511	Do Not Stuff
5,11,22,36	H_CPUPWRGD	TP8512	Do Not Stuff
27,36	S5_ENABLE	TP8513	Do Not Stuff
5,11,18,27,31,35,36,65,66,71,83	PLT_RST#	TP8514	Do Not Stuff

Test Point放在Dimm Door打開可量測處

Structure boss

H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff
H5 Do Not Stuff
H6 Do Not Stuff
H12 Do Not Stuff
H7 Do Not Stuff
H8 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff

MiniPCI Std-Off

H4 STF237R113H63-GP — 34.44P03.101

Do Not Stuff
H16
Do Not Stuff

H17
Do Not Stuff
Do Not Stuff

S1 SP2ING-71-GP — DY
S2 SP2ING-63-GP — 34.4Y806.001
S3 SP2ING-63-GP — 34.4Y806.001

SC_1101'10

POWER TESTING POINT--TOP

27,68 KBC_PWRBTN#
TP9701 Do Not Stuff
TP9700 Do Not Stuff

POWER TESTING POINT--Bottom

27,68 KBC_PWRBTN#
TP9702 Do Not Stuff
TP9703 Do Not Stuff

AD+

EC9708	EC9709	EC9710	EC9711	EC9712	EC9713
DY	DY	DY	DY	DY	
Do Not Stuff	Do Not Stuff	Do Not Stuff	Do Not Stuff	Do Not Stuff	SCD1U25V2KX-GP

DCBATOUT

				AD_JK		
EC9720	EC9719	EC9718	EC9717	EC9716	EC9715	
DY	DY			DY		
Do Not Stuff	Do Not Stuff	SCD1U25V2KX-GP	SCD1U25V2KX-GP	SCD1U25V2KX-GP	Do Not Stuff	

SA 0904'10

DCBATOUT
EC9714 — SCD1U25V2KX-GP
SA 0809'10

BOM

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Title: UNUSED PARTS/EMI Capacitors

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(Blanking)

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Title: *Change History*

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A4	LZ57	-1

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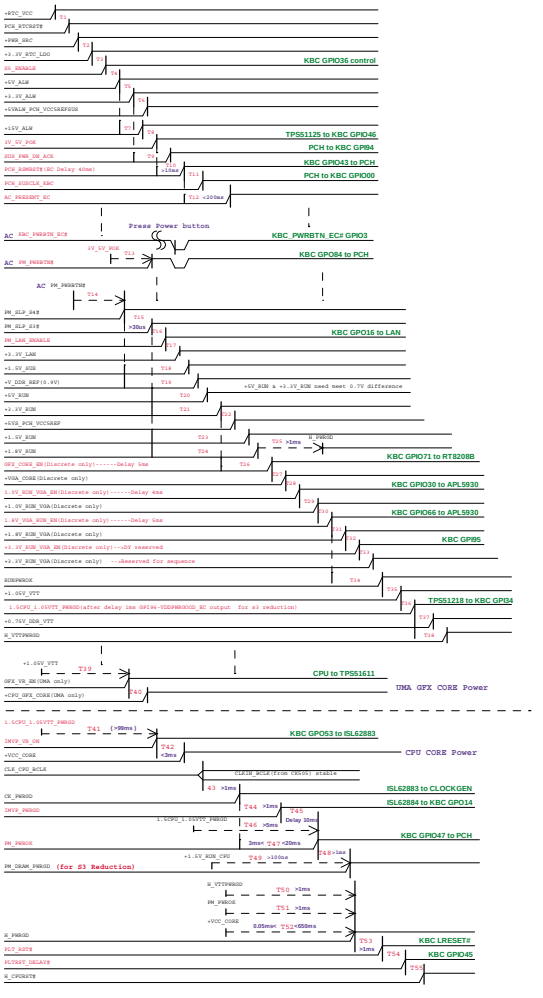
Intel-Power Up Sequence

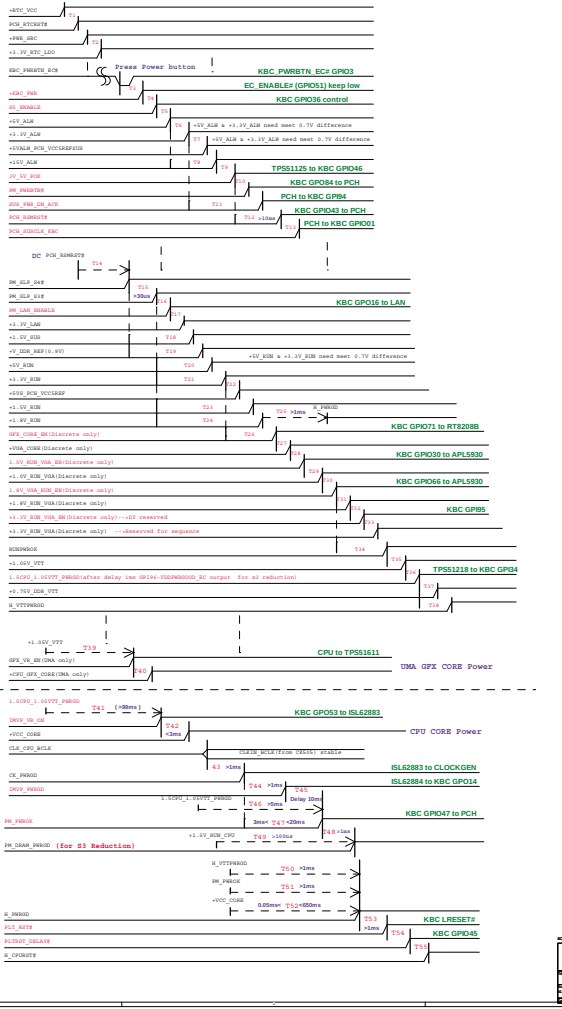
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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Title: Power Sequence

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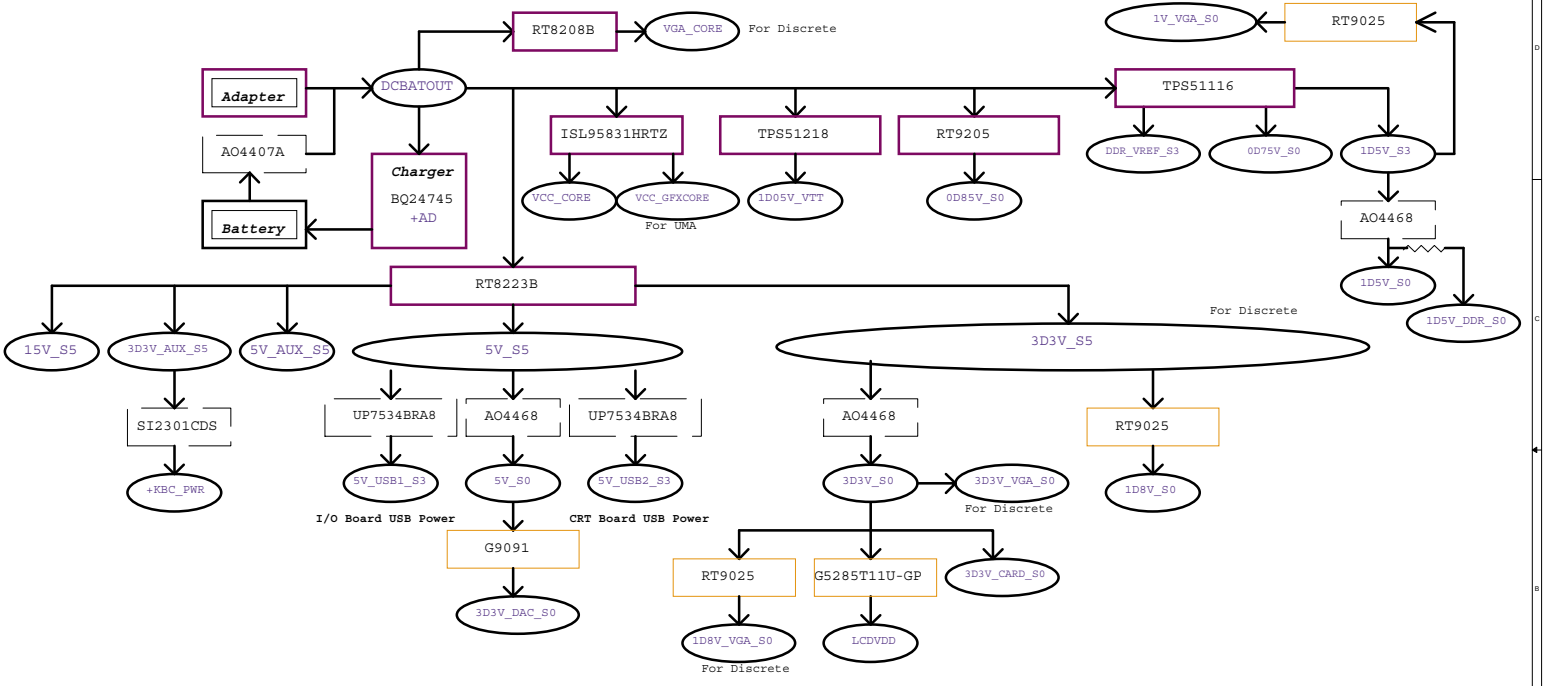

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Title	Power Block Diagram	
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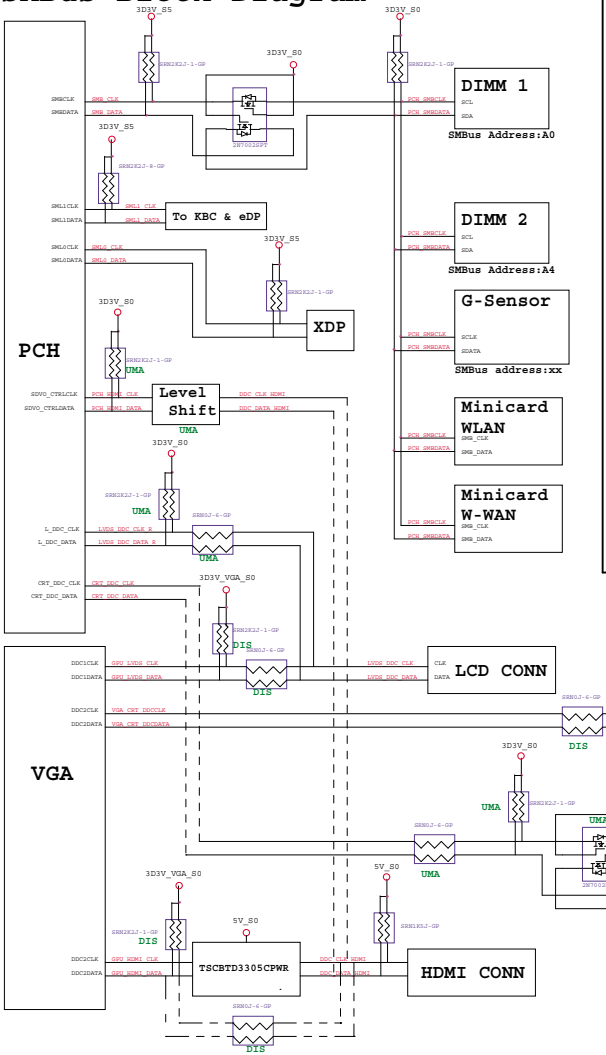
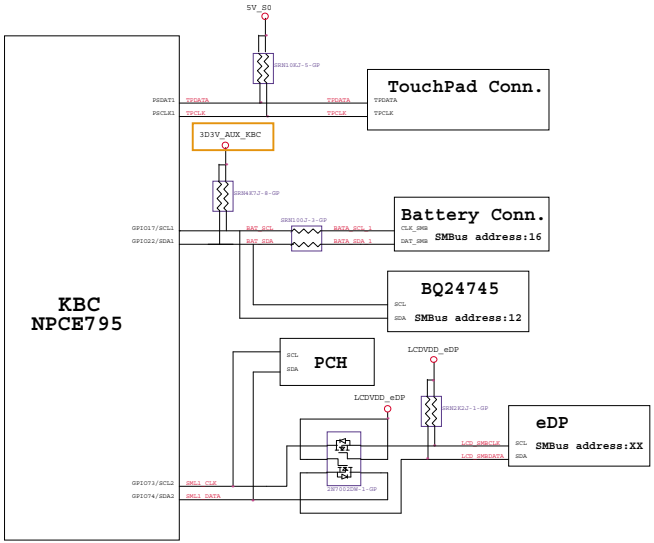
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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File		
	SMBUS Block Diagram	
Size C	Document Number LZ57	Rev -1
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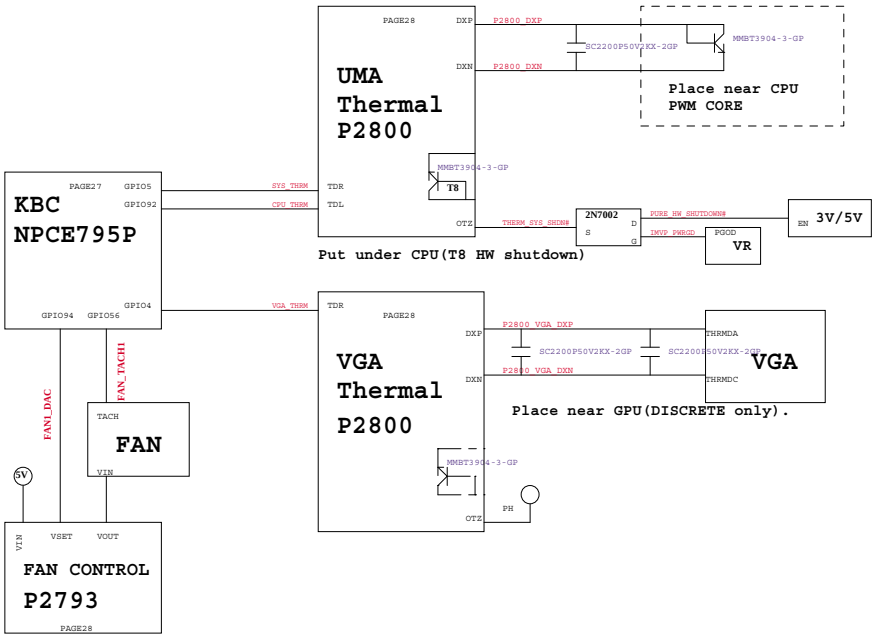
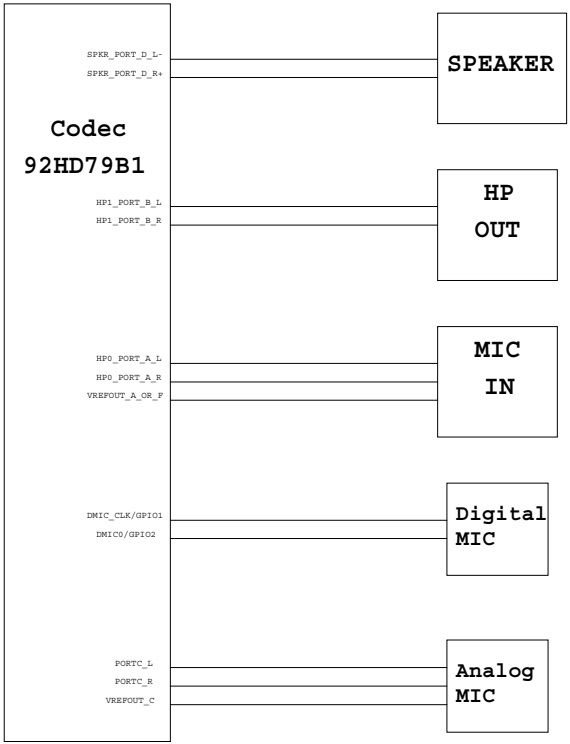
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
Size: Custom	Document Number: LZ57	Rev: -1
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