GA-F2A58M-HD2

Revision : 3.0

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PAGE	TITLE

APU_VDDIO_SUS=DDR15V

APU_VTT_SUS=DDRVTT
APU_VDDP_RUN=APU_VDDR_RUN=APU_VDDP

+1.1V_RUN=FCH_VDD_11_RUN=VCC_SB

+3.3V_RUN=VCC3
+3.3V_ALW=3VDUAL

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Title: COVER SHEET		
Size: Custom	Document Number: GA-F2A58M-HD2	Rev: 3.0
Date: Wednesday, February 05, 2014	Sheet 1 of	GIGABYTE

Model Name:GA-F2A58M-HD2

Component value change history

Version: 3.0
P-Code: U98126-0

Date	Change Item	Reason
2014.01.29	30A E-BOM release PCB:3.0	BOM Modify form F2A55M-HD2 30D
		1.MR19 0/4->0/8 short pad -DDR 2.FNR6 0/4->0/6 short pad -FAN 3.DCR1,DR1,DER1,DR3,DFR1,CR51,DAR1,DBR1->0/6 short pad & mask -VCORE MOS 4.R1,MOATC3,PR91,PR100 0ohm change to shorpad 5.Hudson 55 change to Bolton 58 chip
2014.03.13	30B P-BOM release PCB:3.0	1.SIO change 8620 CX 2.F_AUDIO change 11NH2-000205-M1R/M2R 3.COM change 11NH2-000205-23R/28R

Circuit or PCB layout change for next version

Date	Change Item	Reason
2014.01.28	Rev 3.0 Gerber-out	Modify form F2A55M-HD2 3.03 1.F_PANEL IO_BLINK 2.IO_BLINK change to SIO GP91 3.0ohm change shortpad & mask 4.文字面 5.MOS footprint change <Q_TDSON8-GDS-T> 6.DVI footprint change <DVI-30P-4P-1>

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Title	BOM & PCB HISTORY	
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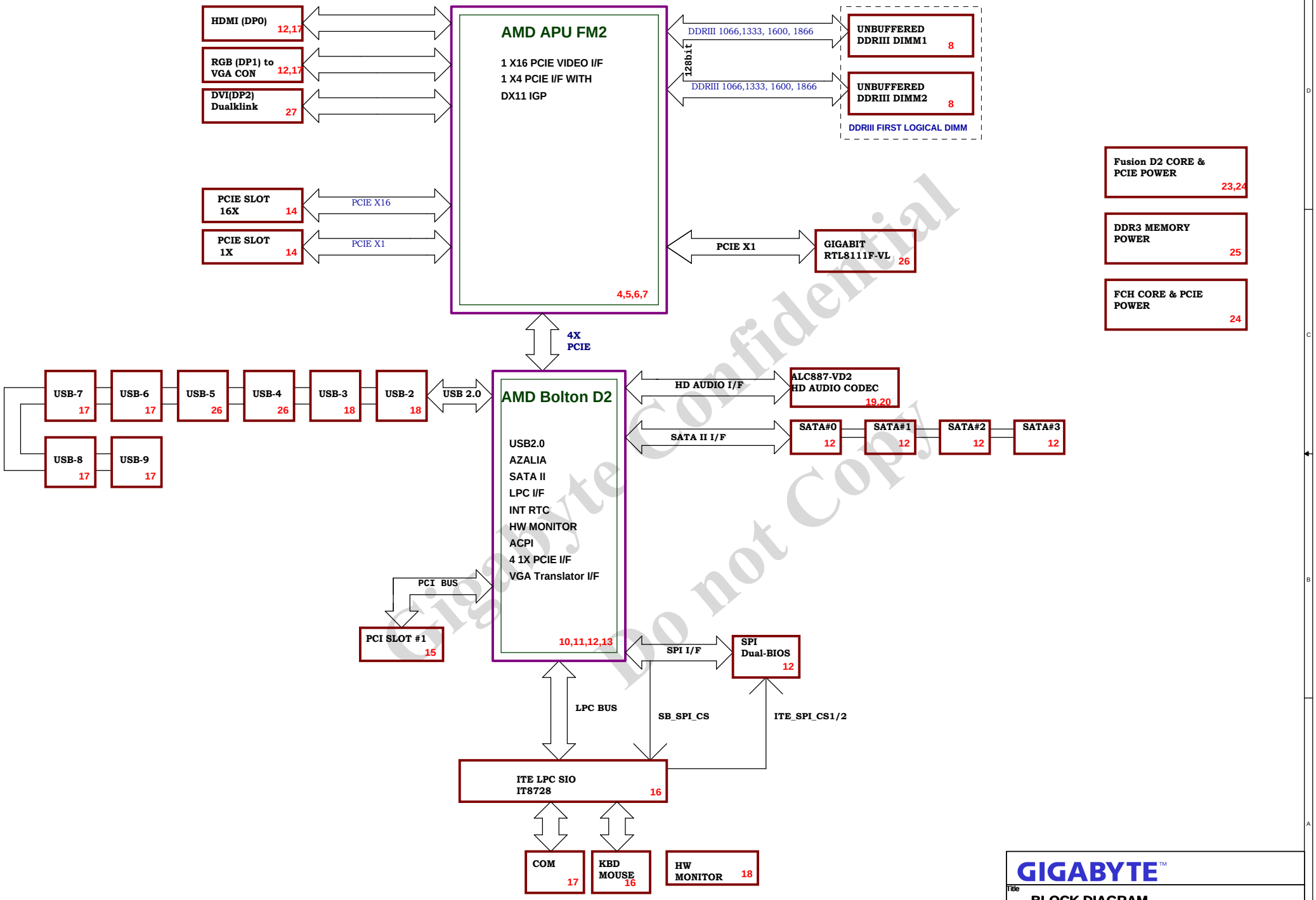
AMD Fusion Hudson CUSTOMER DESKTOP REFERENCE DESIGN



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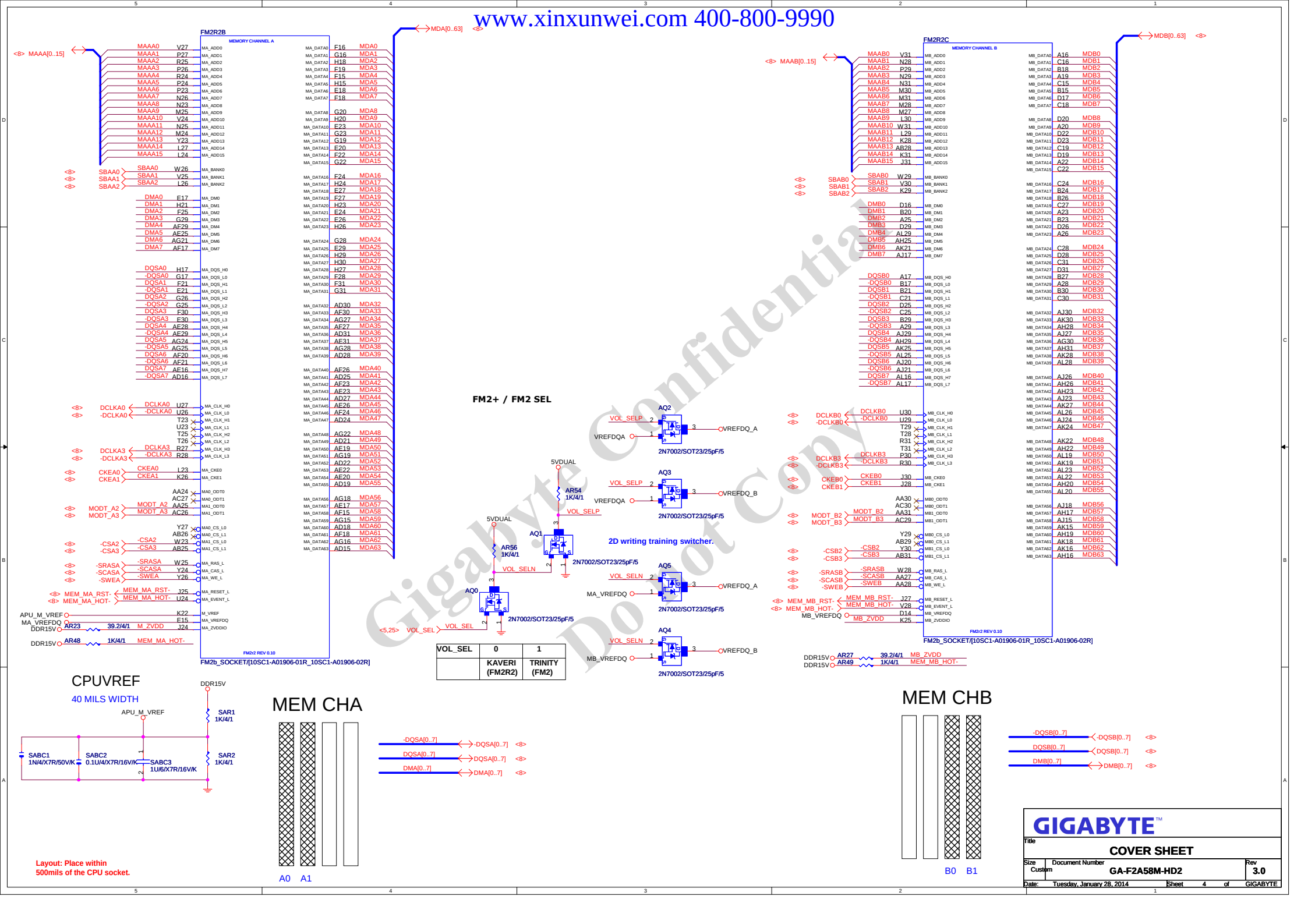
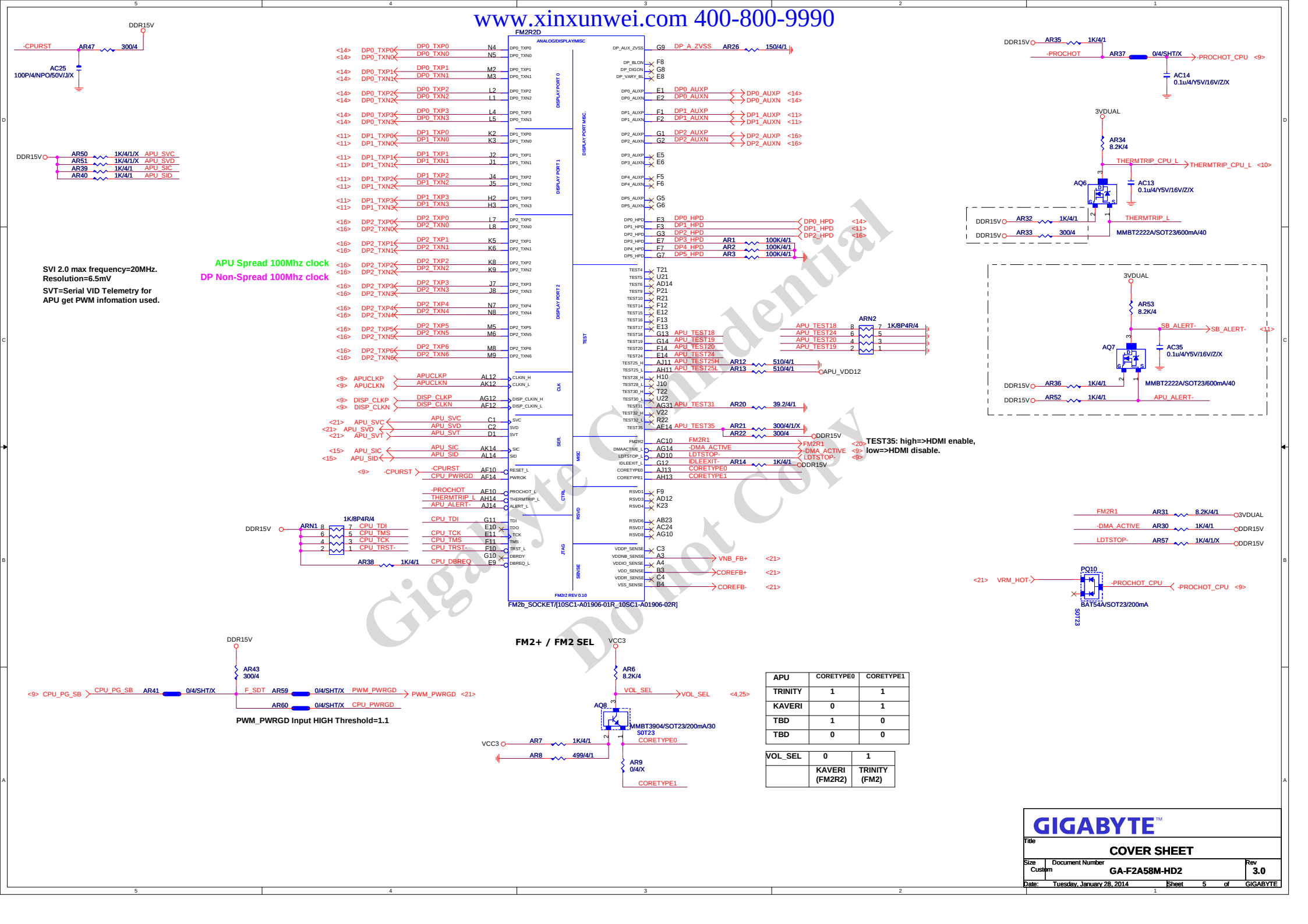
Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	GA-F2A58M-HD2	3.0

Date: Thursday, March 13, 2014 Sheet 3 of GIGABYTE





APU	CORETYPE0	CORETYPE1
TRINITY	1	1
KAVERI	0	1
TBD	1	0
TBD	0	0

VOL_SEL	0	1
	KAVERI (FM2R2)	TRINITY (FM2)

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Title	FM1_FCH	
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DDR15V=1.25V/1.35V/1.5V(DDR3)

GND:232 pin,
VCORE:99 pin,
VCORE_NB: 30 pin,
DDR15V:49 pin,
VDDP:9 pin, VDDR:9 pin, VDDA25:2 pin,
VDDNB_CAP:2 pin,Total:430 pin.

Place close N13, M14 pin inside the backplate cavity opeining.

Check Power from AMD

FM2b_SOCKET/[10SC1-A01906-01R_10SC1-A01906-02R]

AMD RM/BLACK/[12KRC-04K812-31R_12KRC-04K812-32R]

PCIE_X16 Cross Moat CAP

BUTTOM SIDE

Title	CPU POWER & GND		
Size: Custom	Document Number: GA-F2A58M-HD2		Rev: 3.0
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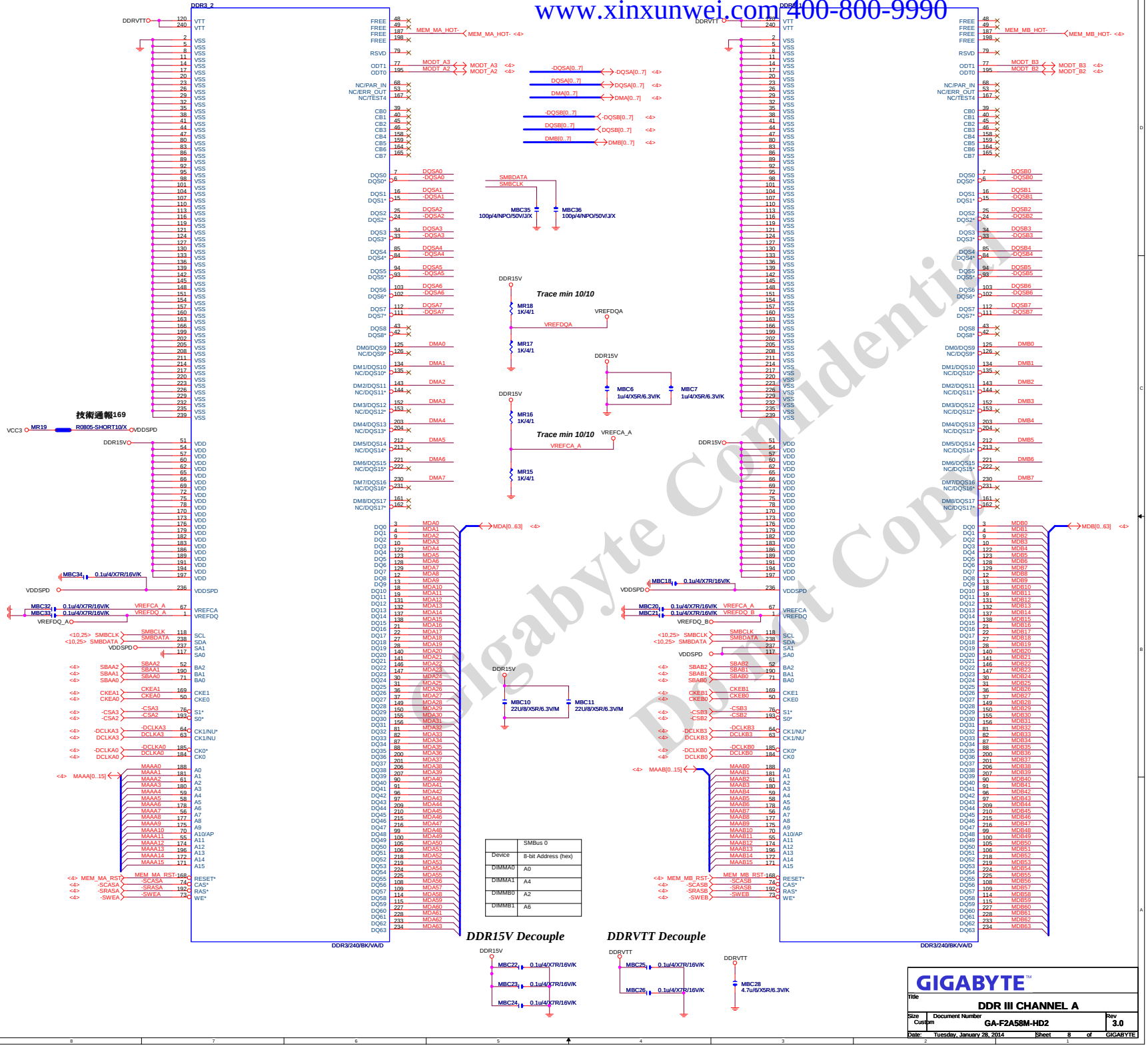

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Title: DDR III CHANNEL A

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Date: Tuesday, January 28, 2014 | Sheet 8 of | GIGABYTE

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

For APU PCI_E devices.

U1E HUDSON-2 Part 1 of 5

PCI EXPRESS INTERFACES

PR2 33/4 PR3 33/4

PC3 PC4 PC5 PC6 PC7 PC8 PC9 PC10 0.1U/4/X7R/16V/K

UMI_TXP0 UMI_TXN0 UMI_TXP1 UMI_TXN1 UMI_TXP2 UMI_TXN2 UMI_TXP3 UMI_TXN3

PR5 590/4/1 PR4 2K/4/1

PCI INTERFACE

PCI CLKS

PR13 33/4 -PPCIRST

AD[0..31]

PR45 2K/4/1

CLOCK GENERATOR

PR94 22/4 LPC48_C

25MHZ_X1 25MHZ_X2

PR7 1M/4

218-0755099/S[10HB1-060BT2-10R]

LPC

PR0 8.2K/4/X

APU

Note: LDT_STP# leave NC--DG1.0

SS PLUS

PR27 100K/4/1

PBC2 0.1U/4/X7R/16V/K

S.B HEATSINK

SB_HS

SB_HS/[12SP2-SA0301-01R_12SP2-SA0301-02R_12SP2-SA0301-03R]

RTC_XI RTC_XO

PR6 20M/4

PX1 32.768K/12.5p/20ppm/TF38/35K/D

PC13 18P/4/NPO/50V/J PC14 18P/4/NPO/50V/J

PX1 SHW/D0.64*5.08*6.74

PX2 25M/20p/30ppm/49US/20/D

PC15 22P/4/NPO/50V/J PC16 22P/4/NPO/50V/J

3VDUAL RTC_CLK PR90 8.2K/4/X PR97 2.2K/4/1

Pull down for S5+ Mode

VCC3 PCLK1 PR14 8.2K/4

Low: Force PCIE GEN1, Up: Allow PCIE GEN2

PCLK3 PR92 8.2K/4

PCLK3	
PULL HIGH	USE DEBUG STRAPS
PULL LOW	IGNORE DEBUG STRAPS DEFAULT

VCC3 PCLK4 PR17 8.2K/4/X PR96 8.2K/4/1

CLKGEN Mode: Only for integrated clock mode.

LPC_CLK0 PR20 8.2K/4

3VDUAL LPC_CLK1 PR95 8.2K/4/1

	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
	AOD Extreme	
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

20mil 20mil 20mil

3VDUAL PQ1 RTCVDD PR28 1K/4/1

VBAT VBAT_2 RB 1K/4/1 BAT54C/SOT23/200mA PBC24 0.1U/6/X7R/25V/K PBC25 1U/6/Y5V/10V/Z

BAT BAT-SK/BK/P/S/D/SN

CR2032 BAT CR2032

CLR_CMOS RTCVDD PH/1*2/BK/2.54/VA/D

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

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Title: ATI SB700 PCIE/PCI/CPU/LPC

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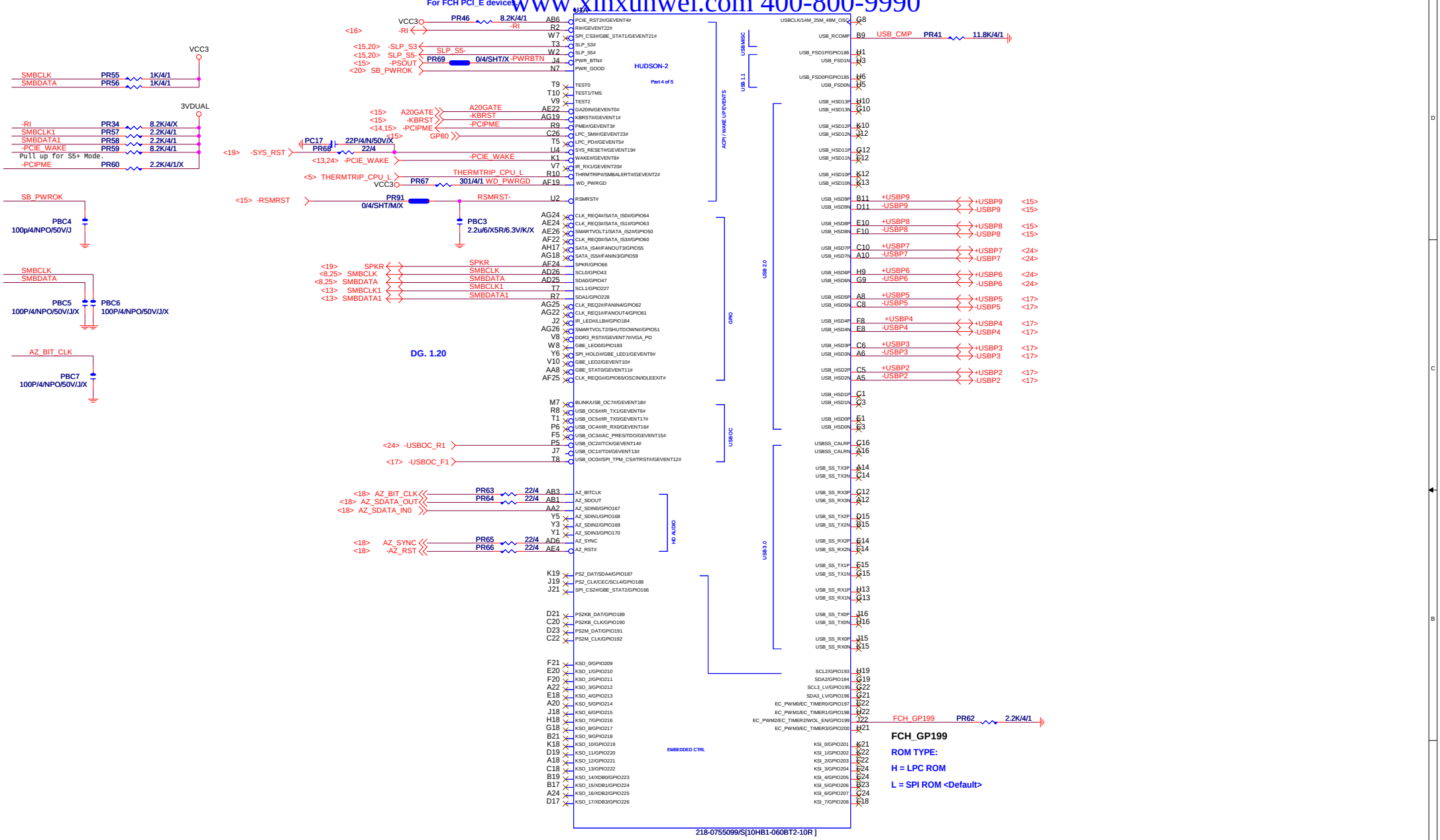

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Title	ATI SB700 ACPI/USB/GPIO/AUDIO	
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U1B

HUDSON-2

Part 2 of 5

SATA 6~7 for Hudson D4.

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U1

RGMII NOT SUPPORT. DG:1.20

10" Max for FCH VGA.

218-0755099/S[10HB1-060BT2-10R]

M_BIOS

64M/SPI/SO8/200mil/S

B_BIOS

64M/SPI/SO8/200mil/S

SATA2_0

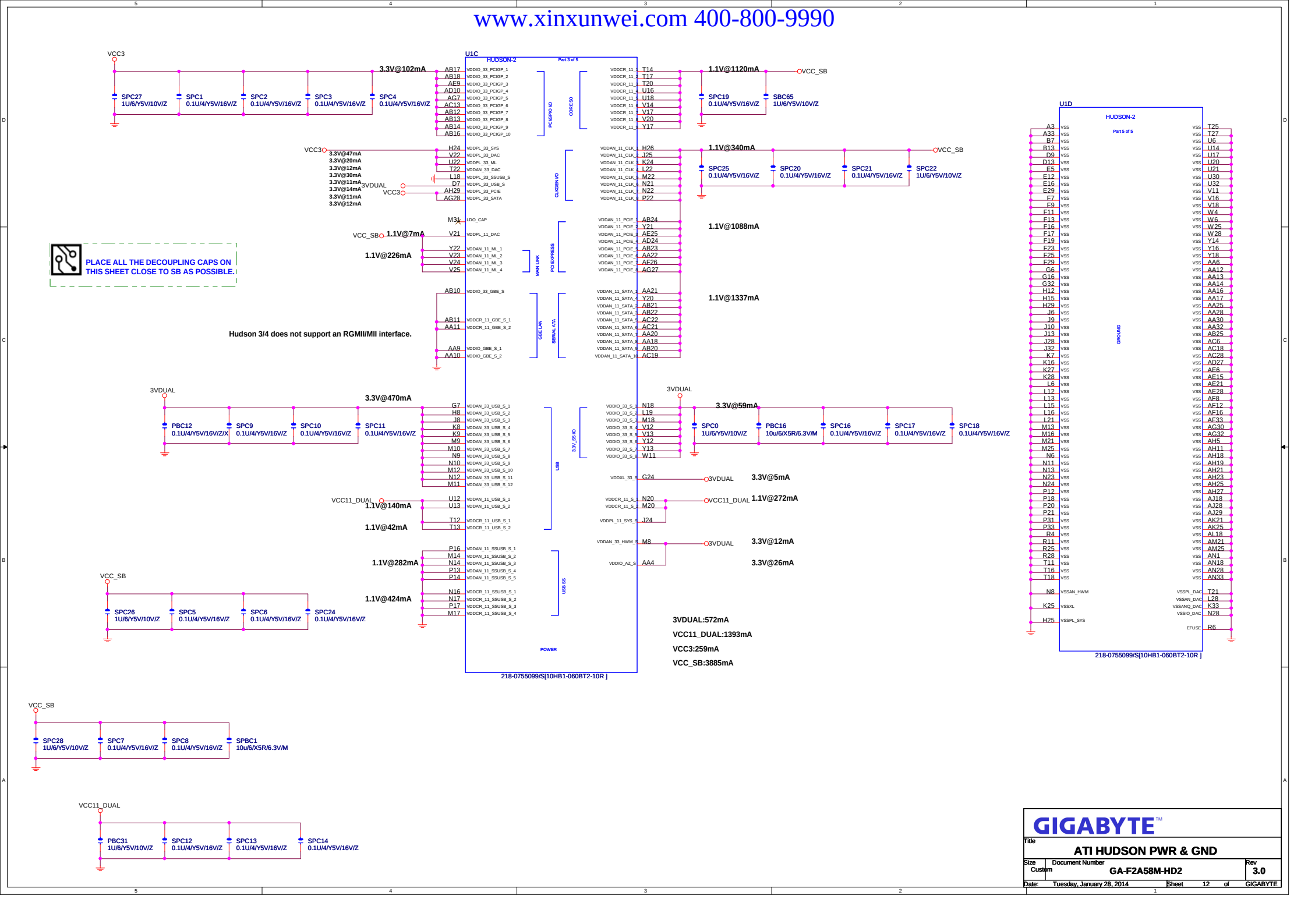
SATA2_1

SATA2_2

SATA2_3

SATA2/7/BK/H/OP/VA/D/1/B

Title	HUDSON D3 SATA/HWM/SPI	
Size: Custom	Document Number: GA-F2A58M-HD2	Rev: 3.0
Date: Tuesday, January 28, 2014	Sheet 11 of GIGABYTE	



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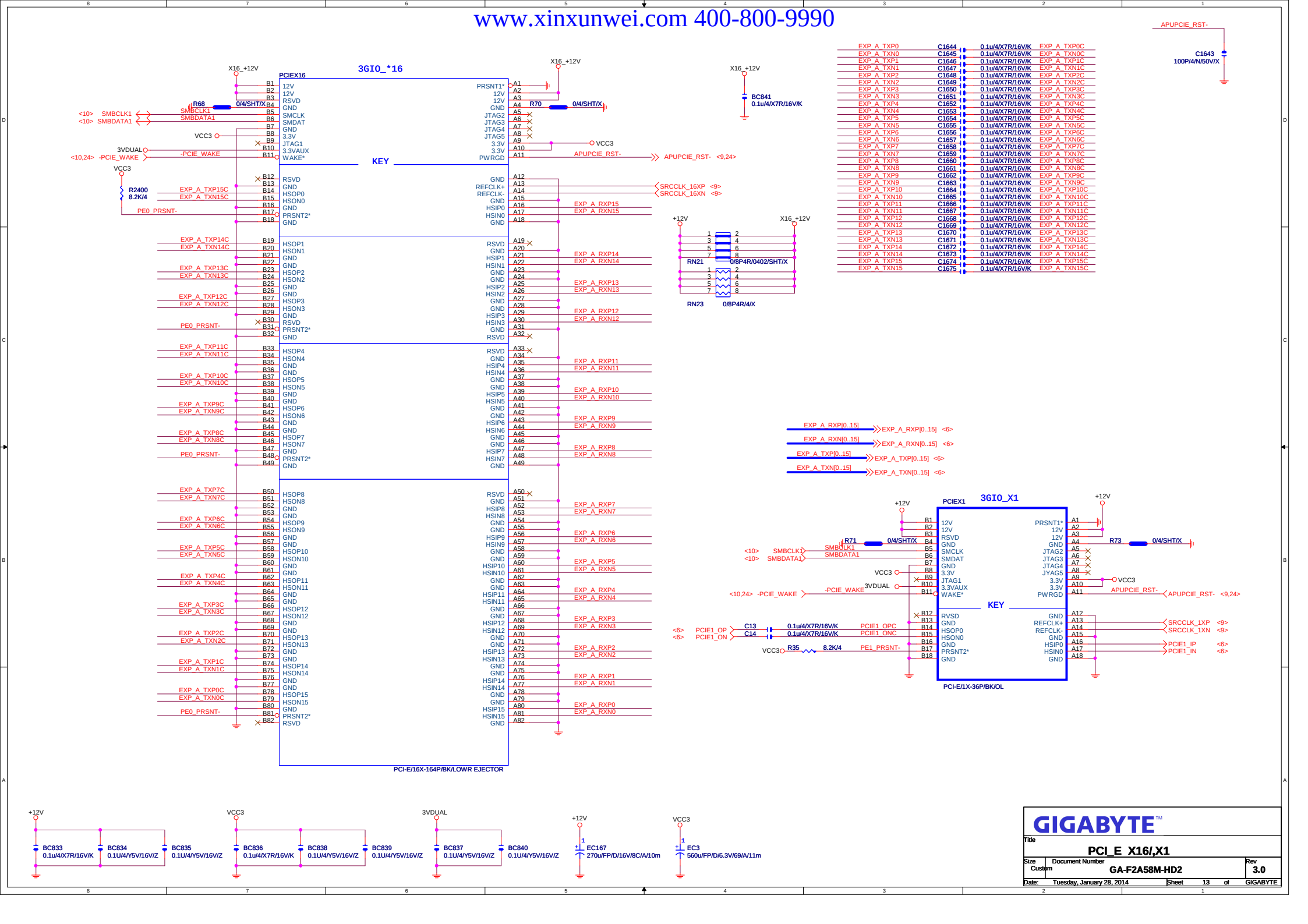
Title	ATI HUDSON PWR & GND	
Size: Custom	Document Number: GA-F2A58M-HD2	Rev: 3.0
Date: Tuesday, January 28, 2014	Sheet 12 of GIGABYTE	



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Title	PCI_E X16/,X1	
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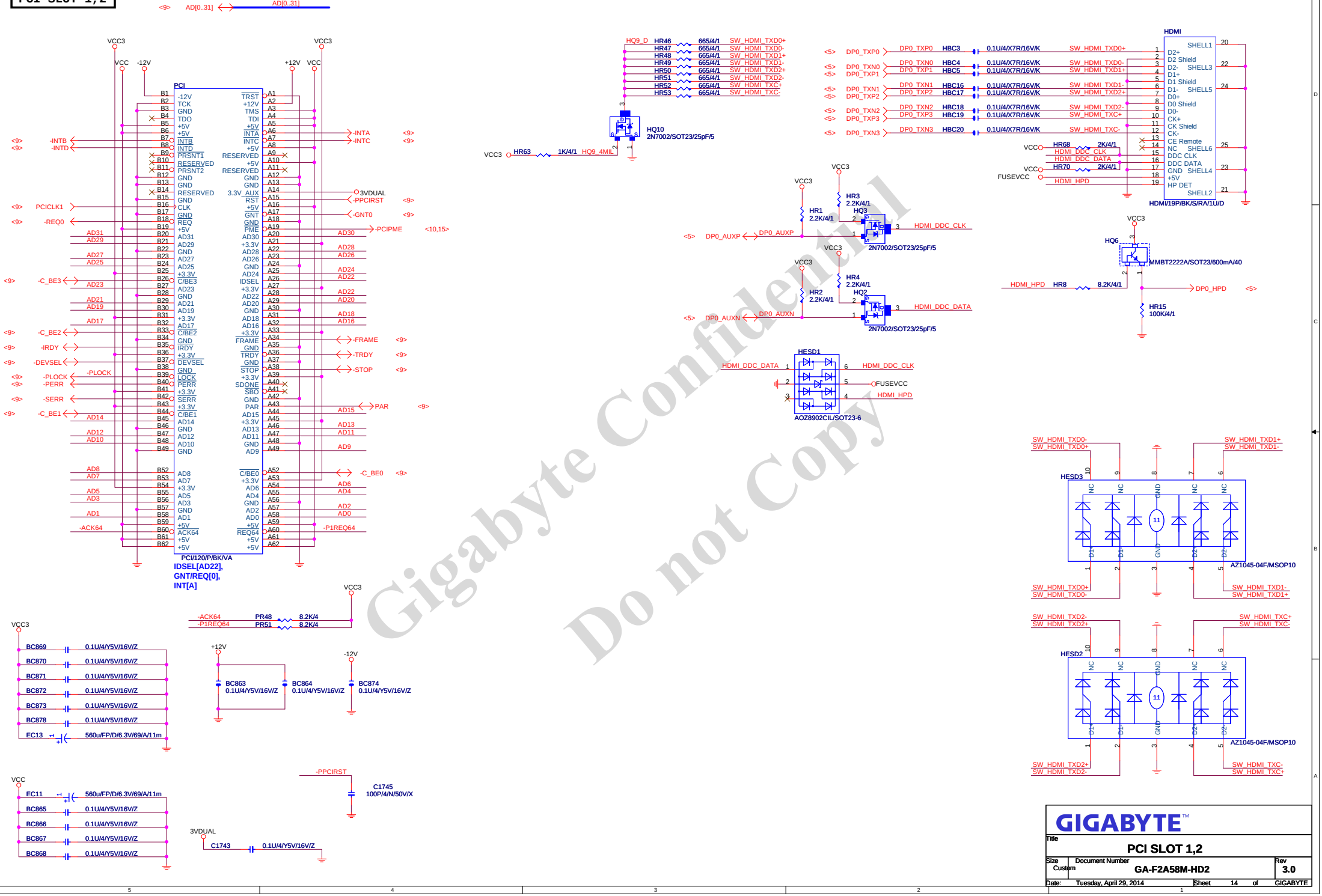
PCI SLOT 1,2



ite recommand OD pull high

IT8620E_BX

IT8620E/CX/S

SIO

EUP control by PCH

CPU Thermal Diode Differential Pair

For IT8721 Power leakage

OBC7 ite recommand 0.01u change to 1u

OBC13=>0.1U confirm by Tom.

Power issue 0415

JP5 Internal pull up

JP5 High: UV/OV by BIOS setting.
Low: UV/OV by HW strap.

O: EN SPI, I:DIS SPI

ErP

UP0111AMA5-00/SOT23-5/600mA/[10GL4-060111-00R_10GL4-067365-01R]
Vout=0.8*(R1+R2)/R2

For Erp patch

AOZ8902CIL/SOT23-6

KB/USB/A/PC99(DUAL)/GF/2/RA/D

8.2K/8P4R/4

Hardware Monitor circuits

SYSTEM Thermister

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Title	ITE 8728 LPC IO
Size	Custom
Document Number	GA-F2A58M-HD2
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Date:	Thursday, February 27, 2014
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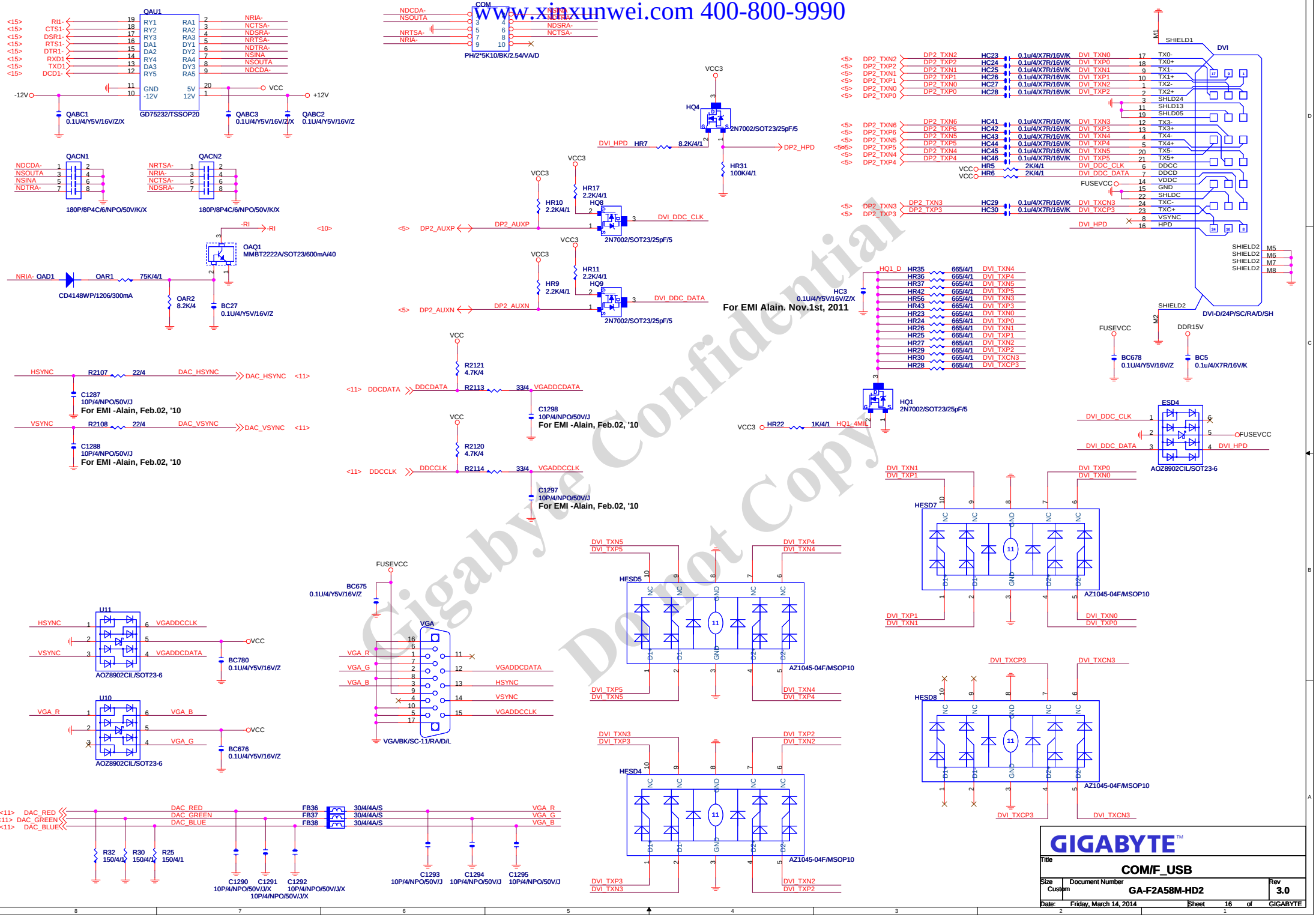
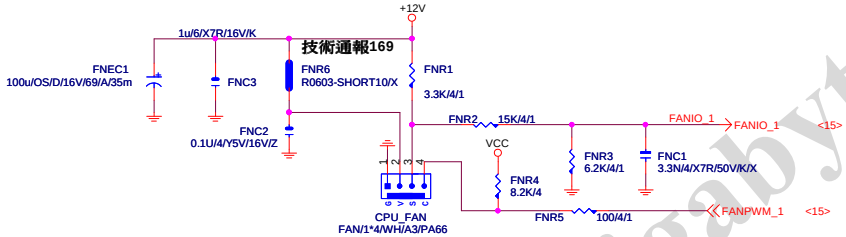


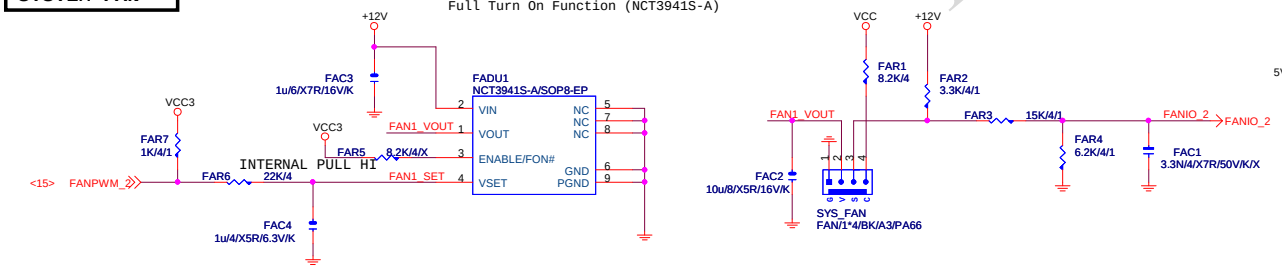
CPU FAN



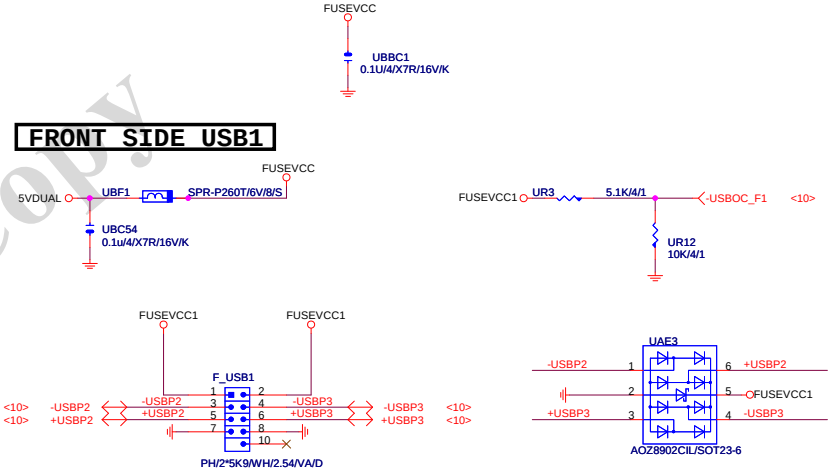
SYSTEM FAN

Linear SYS_FAN

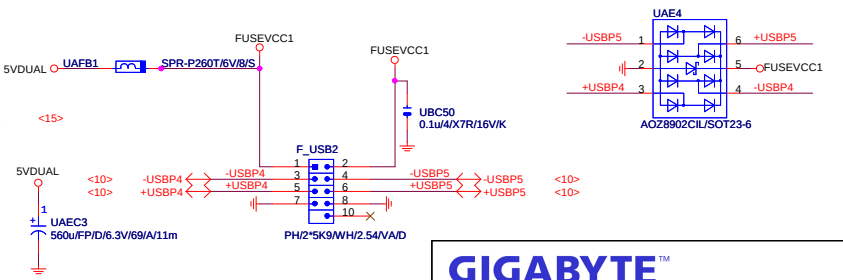
Enable Function (NCT3941S)
Full Turn On Function (NCT3941S-A)



FRONT SIDE USB1



FRONT SIDE USB2



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Title	FAN/HWMO R_USB	
Size: Custom	Document Number: GA-F2A58M-HD2	Rev: 3.0
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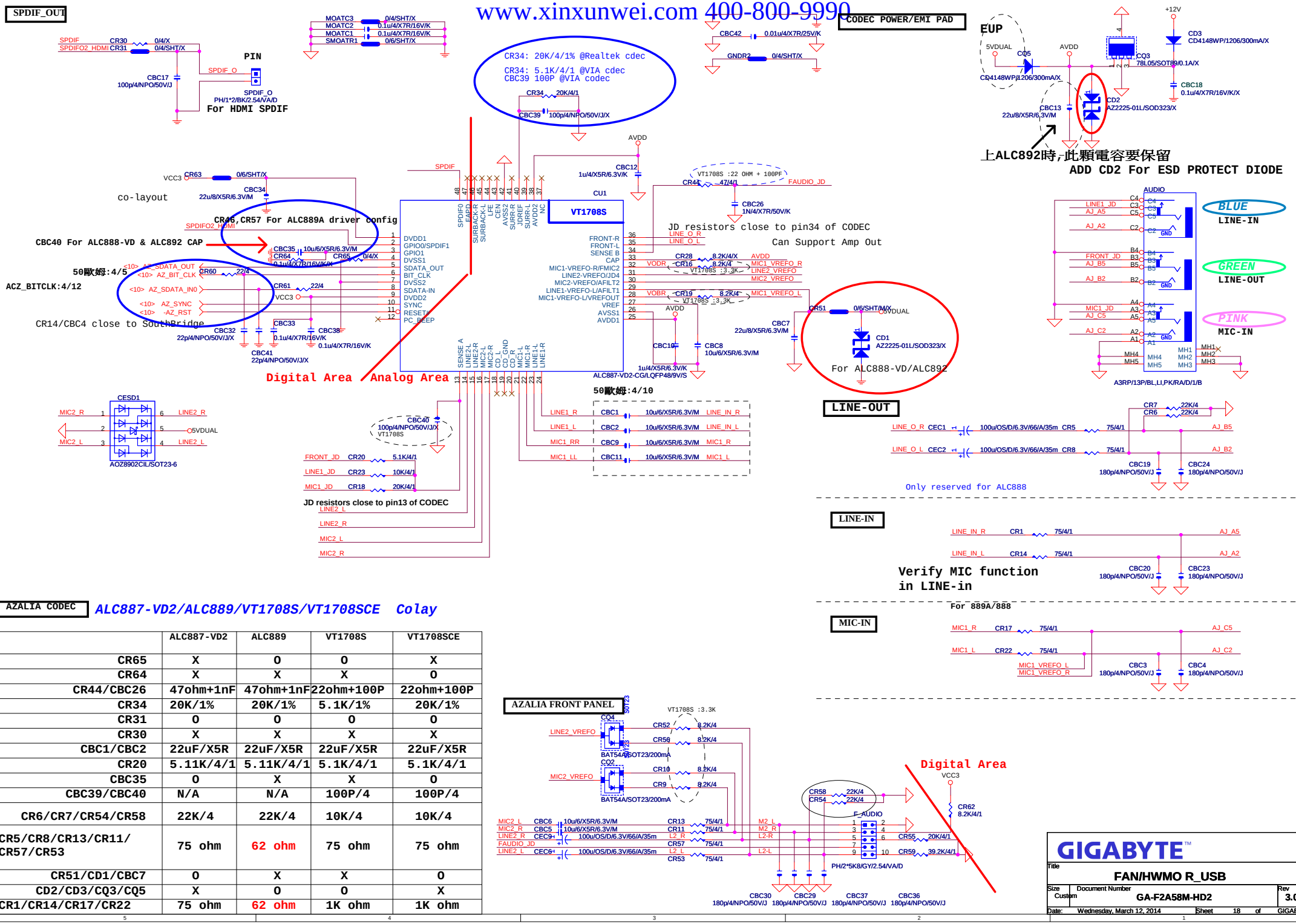

AZALIA CODEC

ALC887-VD2/ALC889/VT1708S/VT1708SCE Colay

	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR65	X	0	0	X
CR64	X	X	X	0
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR34	20K/1%	20K/1%	5.1K/1%	20K/1%
CR31	0	0	0	0
CR30	X	X	X	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR20	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CBC35	0	X	X	0
CBC39/CBC40	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	10K/4	10K/4
CR5/CR8/CR13/CR11/ CR57/CR53	75 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	0	X	X	0
CD2/CD3/CQ3/CQ5	X	0	0	X
CR1/CR14/CR17/CR22	75 ohm	62 ohm	1K ohm	1K ohm

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Title: FAN/HWMO R_USB

Size: Custom | Document Number: GA-F2A58M-HD2 | Rev: 3.0

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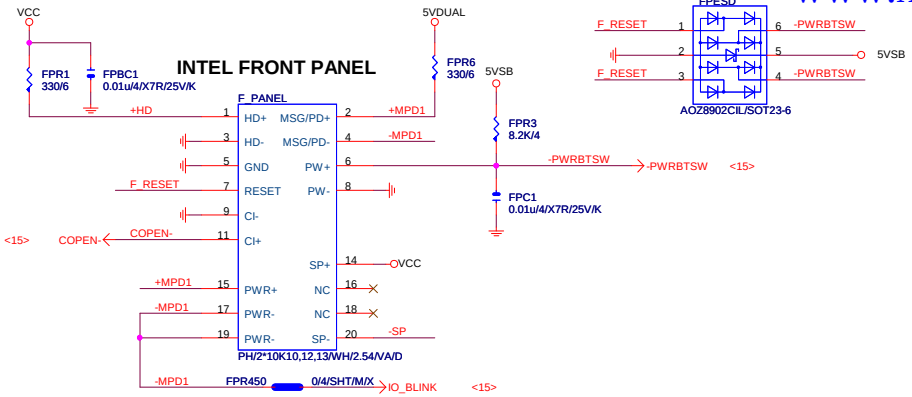
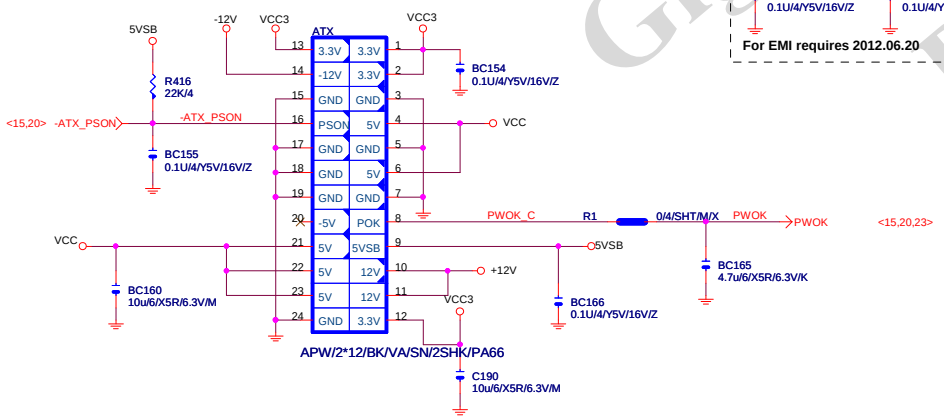
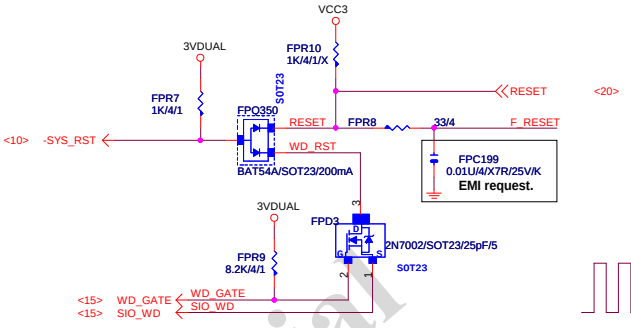
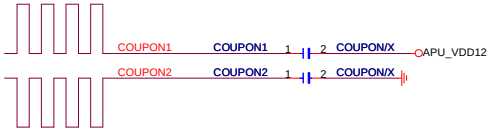
INTEL FRONT PANEL

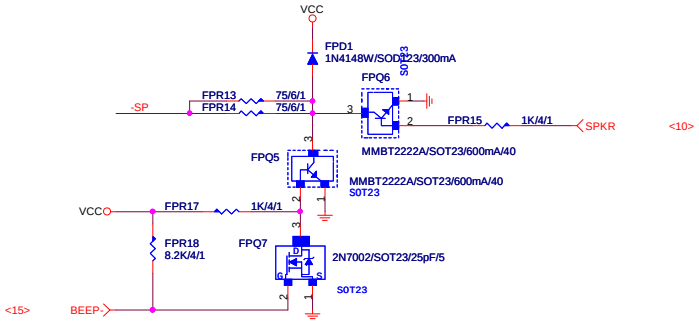


ATX POWER CONNECTOR

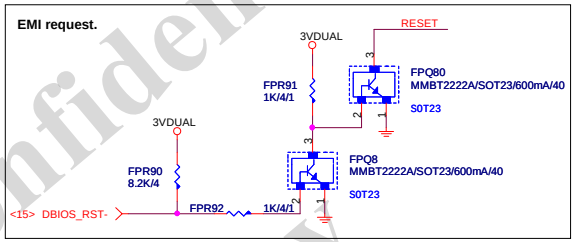


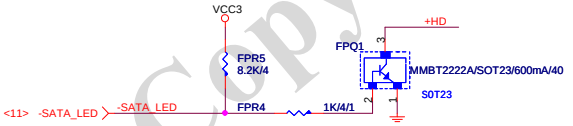


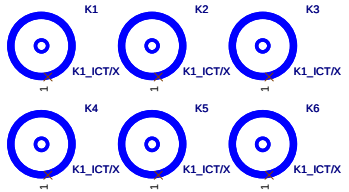


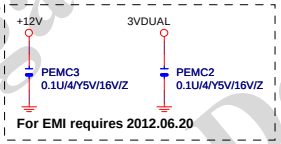


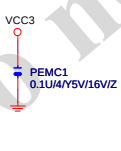
For SPKR voltage issue. FPQ6=>2222, FPQ7=>7002

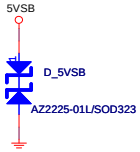


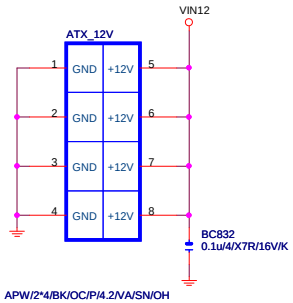


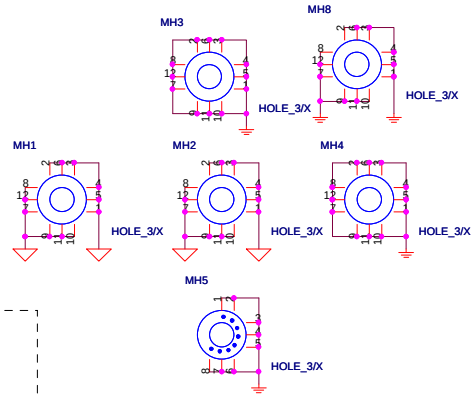


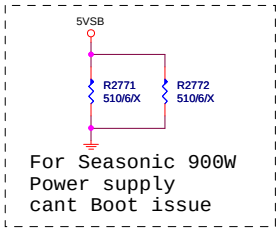












GIGABYTE™

Title: ATX, FRONT PANEL		
Size: Custom	Document Number: GA-F2A58M-HD2	Rev: 3.0
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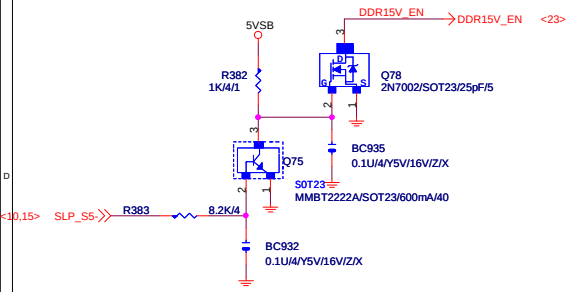

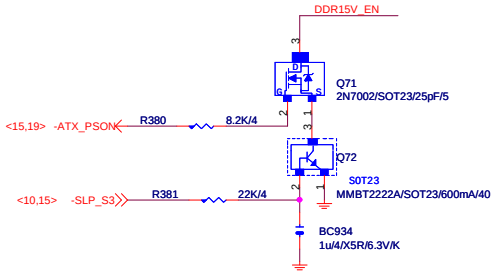

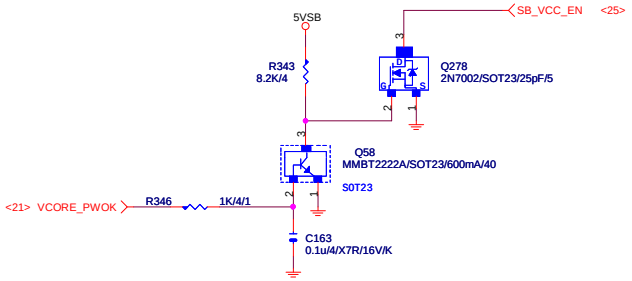

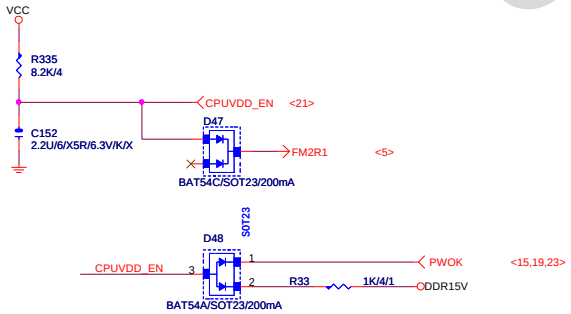

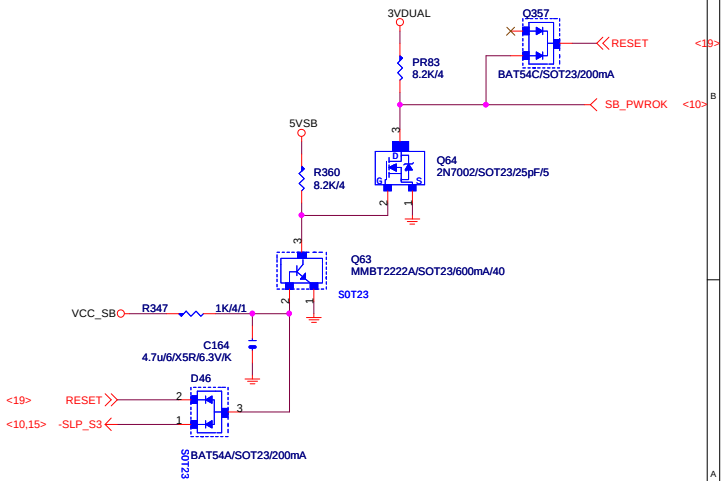

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Title: POWER SEQUENCE

Size	Document Number	Rev
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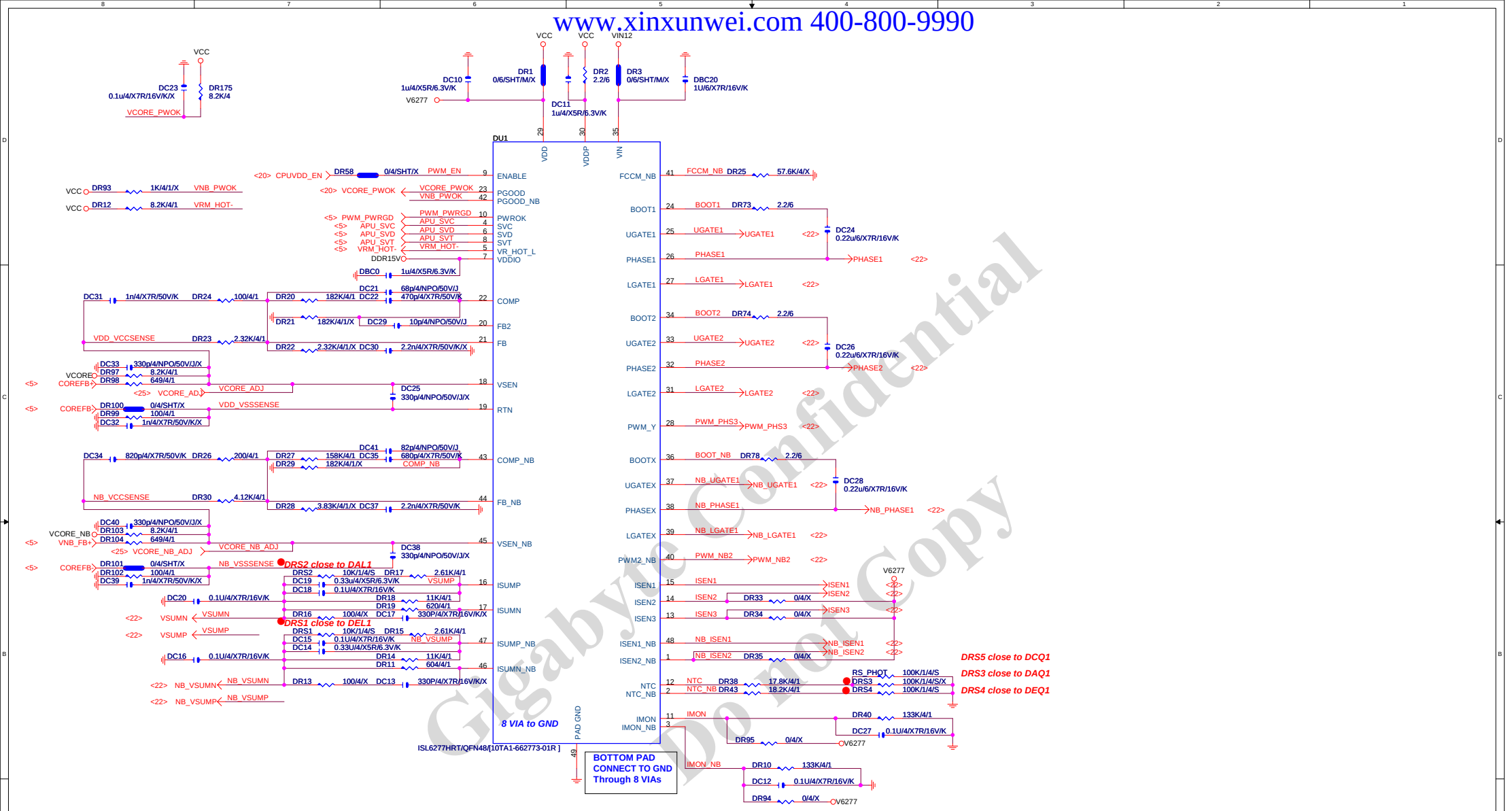

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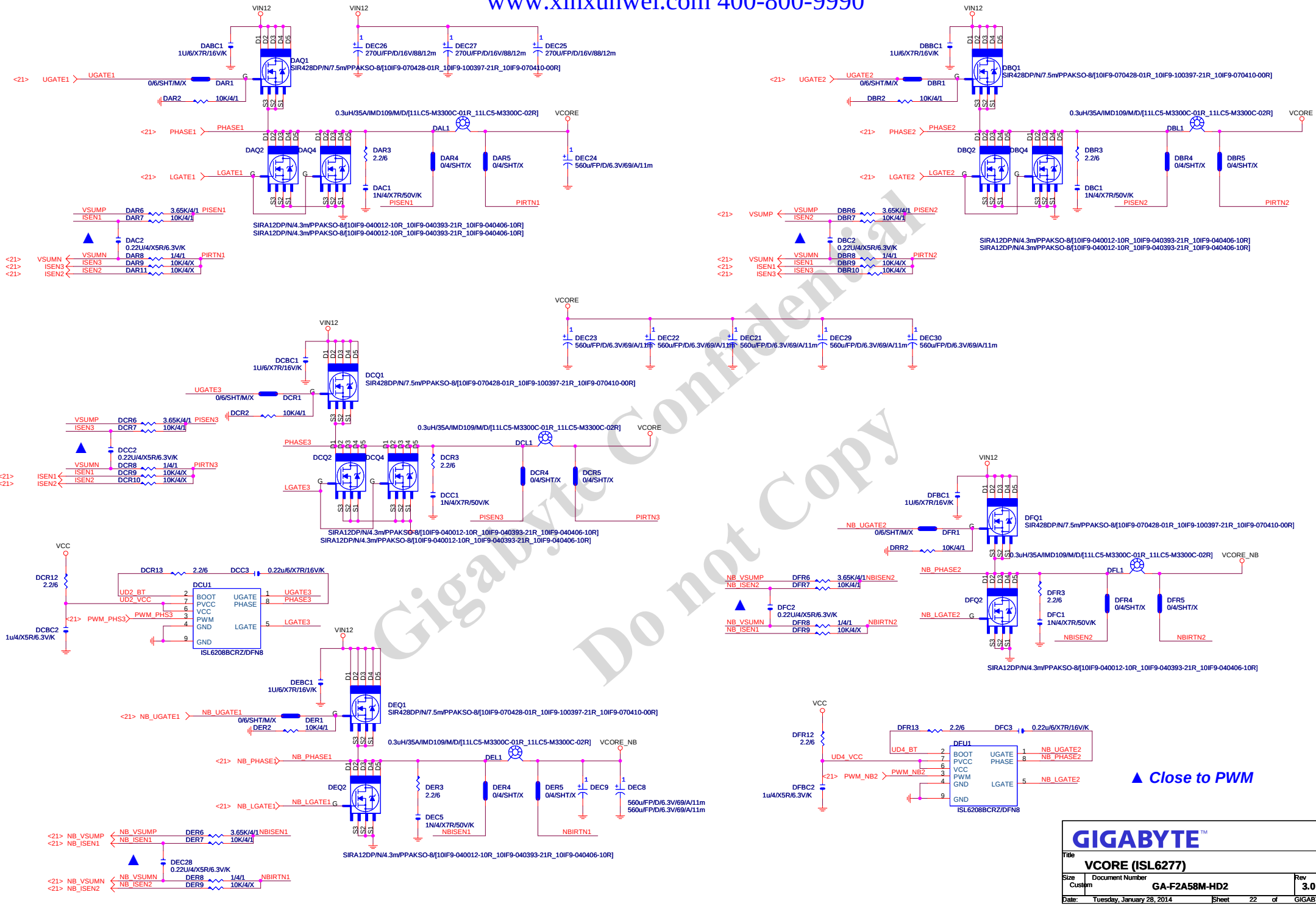
Title	VCORE (ISL6277)	
Size: Custom	Document Number: GA-F2A58M-HD2	Rev: 3.0
Date: Tuesday, January 28, 2014	Sheet 21 of	GIGABYTE



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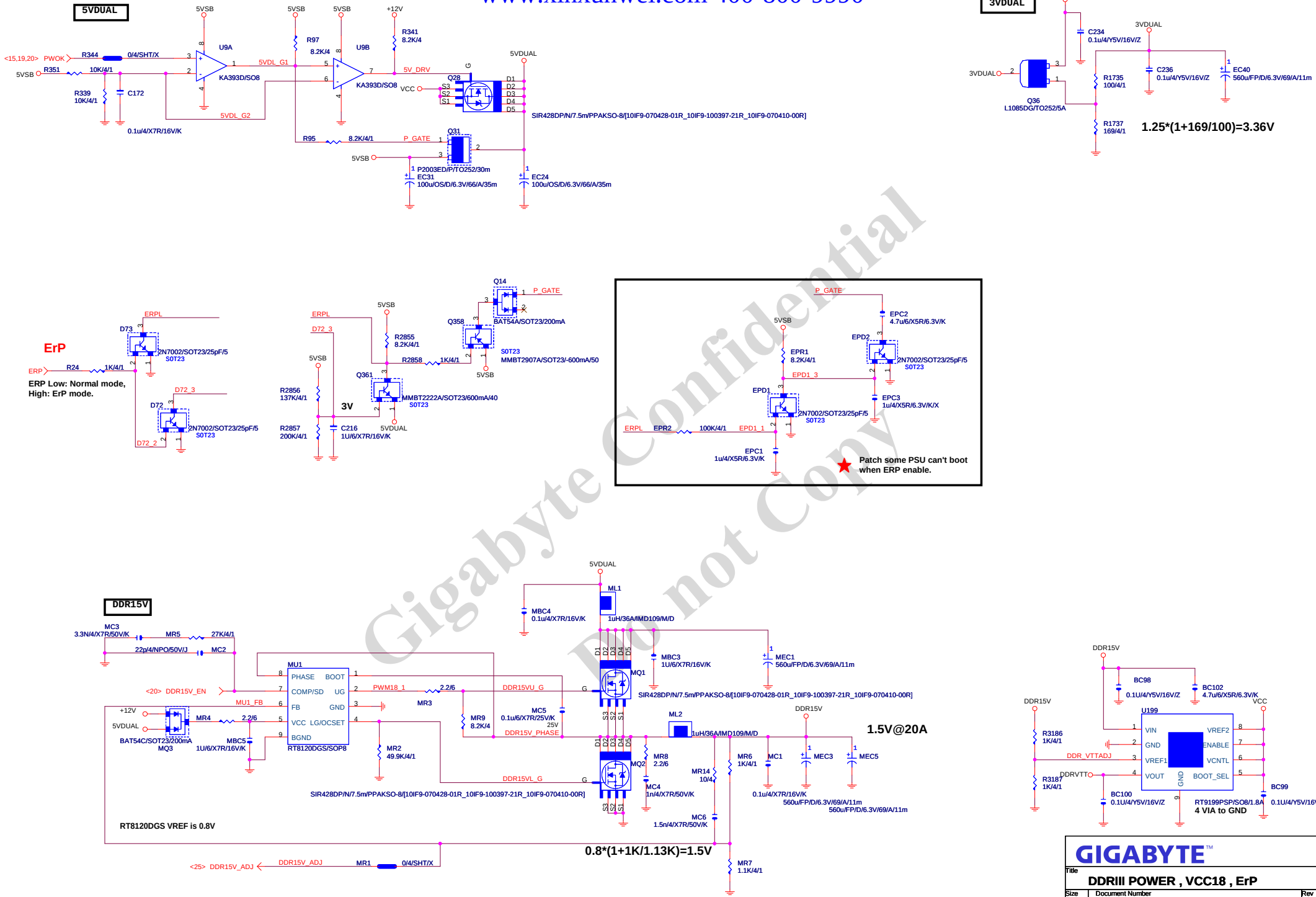
Title	VCORE (ISL6277)	
Size: Custom	Document Number: GA-F2A58M-HD2	Rev: 3.0
Date: Tuesday, January 28, 2014	Sheet 22 of GIGABYTE	



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Title	DDRIII POWER , VCC18 , ErP	
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Date: Tuesday, January 28, 2014	Sheet 23 of GIGABYTE	

PCIE-1G LAN

Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

LAU1 RTL8111F-VL-CG/QFN48

FOR DSM MODE (DEEP SLUMBER MODE)

ENABLE SW

80歐姆:[15/5/5/5/15]

SRCCLK 50歐姆:[18/4/10/4/18]

離IC近越好

(CLOSE LU1)

(PIN3,6,9,13,29,41,45)

CLOSE LL2

(PIN21)

USB_LAN

AOZ8902CIL/SOT23-6

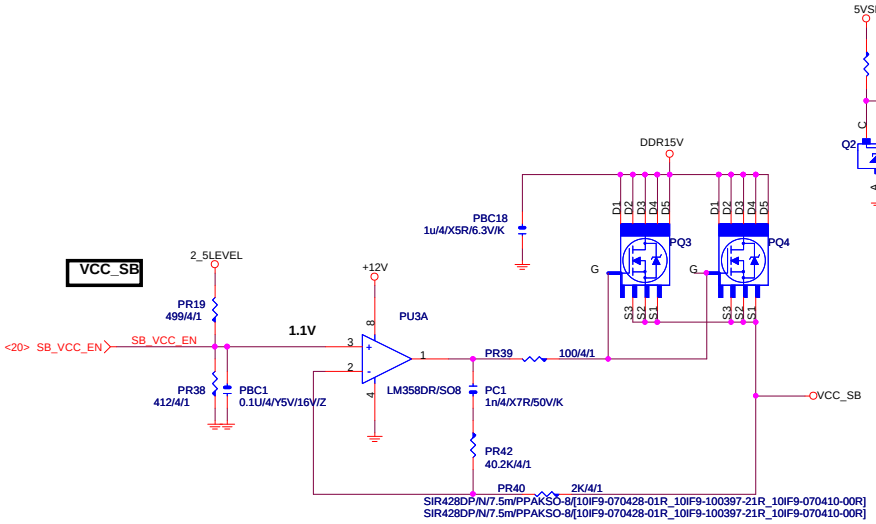
AOZ8902CIL/SOT23-6X

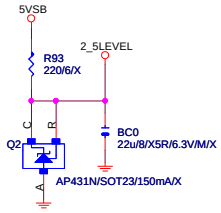
AZ2225-01L/SOD323/X

USB+LAN/1G/GO,Y/OS/RA/D/1

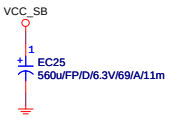
EMI

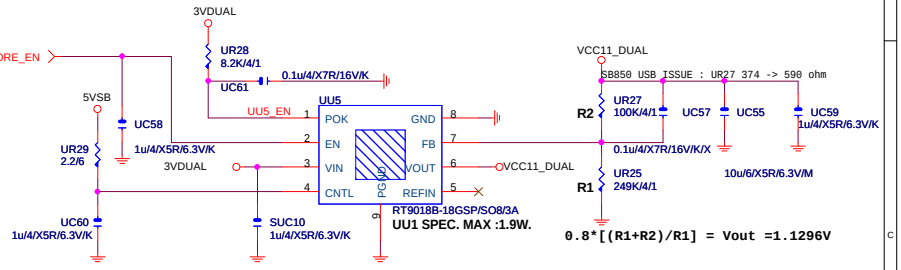
Title	REALTK RTL8111E-VL
Size	Custom
Document Number	GA-F2A58M-HD2
Rev	3.0
Date:	Tuesday, January 28, 2014
Sheet	24 of GIGABYTE



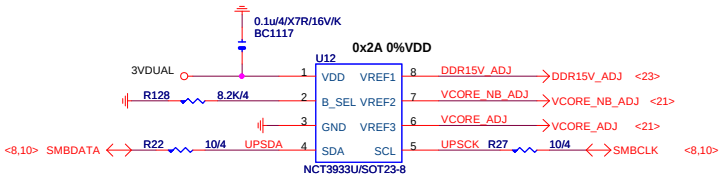


1.2V@1.69A

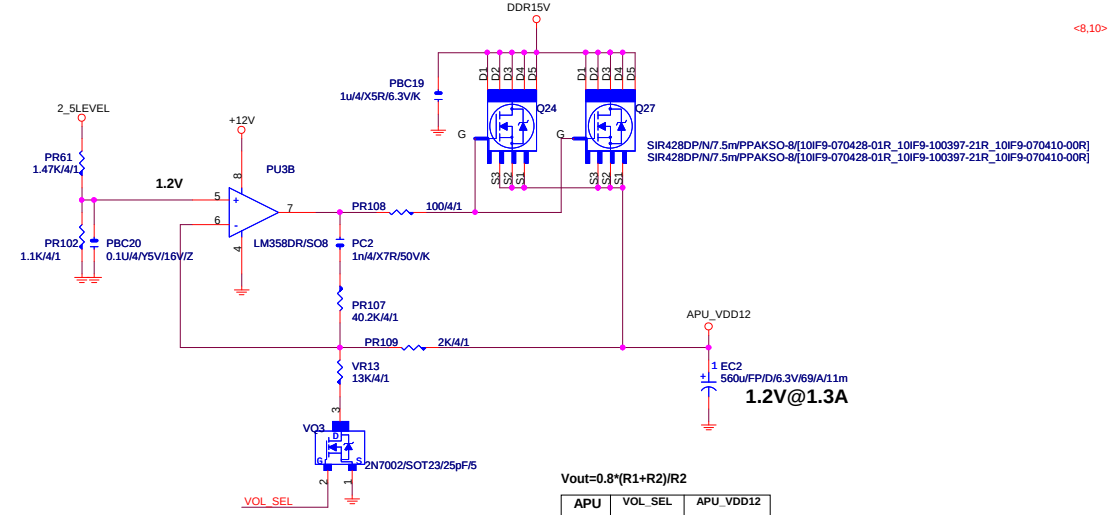




【技術通報R&D技術通報156】
RT9018(RICHTEK)與NCT3730(NUVOTON),
EM5103GE(EMC)做共用,針對PIN7(FB)分壓阻值部份
(R1/R2)須做修改爲100K以上電阻值

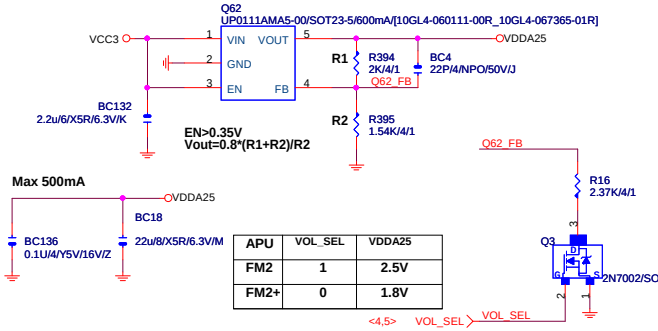


APU_VDDP



Vout=0.8*(R1+R2)/R2

APU	VOL_SEL	APU_VDD12
FM2	1	1.2V
FM2+	0	1.05V



APU	VOL_SEL	VDDA25
FM2	1	2.5V
FM2+	0	1.8V

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Title	SB POWER,VCC12HT,VDDA25,VCC12Dual	
Size: Custom	Document Number: GA-F2A58M-HD2	Rev: 3.0
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