Archer

DTX(9.6"x7.9")

(Version: A)

CONTENT	SHEET

CPU: **Intel Conroe, Wolfdale, Yorkfield processors in LGA775 Package.**
TDP=95W

System Chipset:

North Bridge ... Eaglelake-G41
South Bridge ... ICH7

Main Memory:

Dual Channel / DDR-III * 2

On Board Device:

Clock Generator ... IDTCV186-2APAG8
Super I/O ... IT8721F/BX
LAN-BCM57760
HDA Codec ... ALC662
BIOS ... SPI Flash ROM(8M)

Expansion Slots:

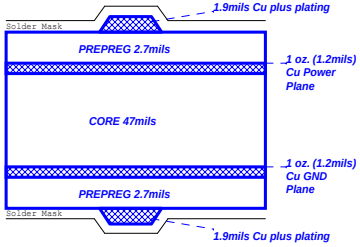
PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT * 1

PWM Controller:

Controller ... NCP5395TMNR2G (3Phase)

Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
DMI - 95ohm : 15/4/8/4/15

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Title		
Cover Sheet		
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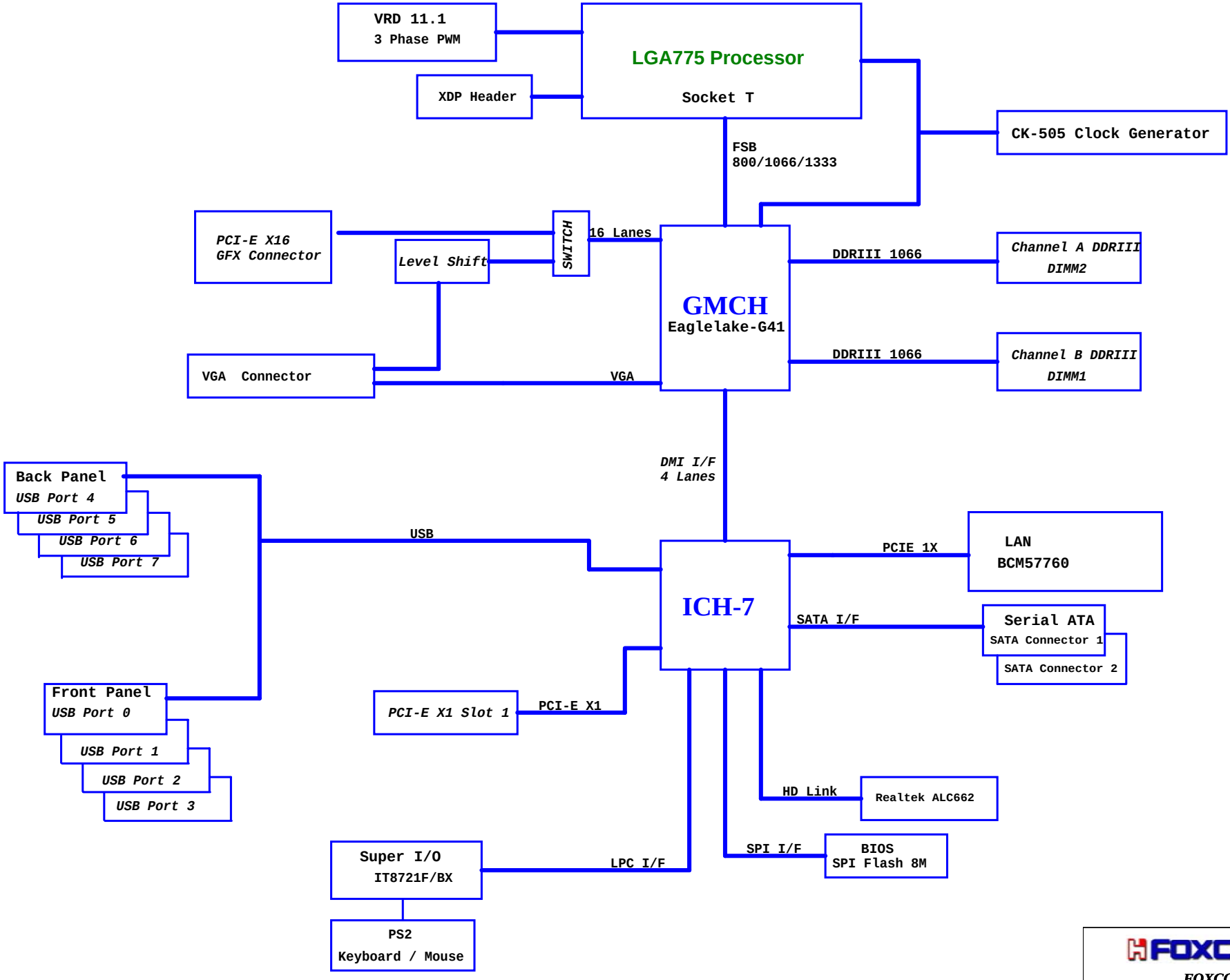

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Title	Block Diagram	
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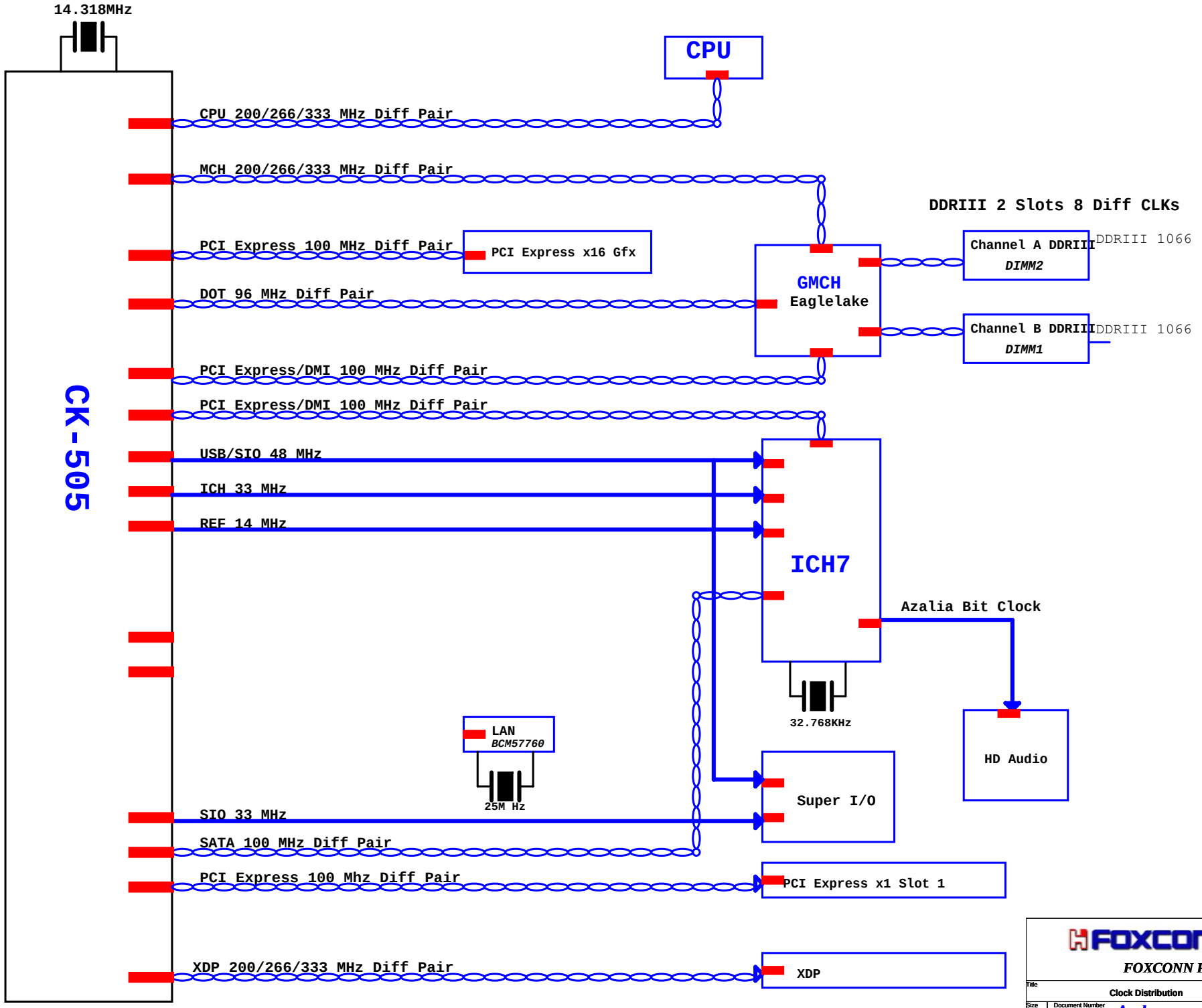

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Title	Clock Distribution	
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uATX P/S

5V

5VSB

5V_DUAL
Icc(Max)=
4.345A(S0,S1)
22mA(S3)

Single Phase Switch
5VDUAL to 1.5V_STR
Ivdd(Max)=14A
Ivdd(Max)=650mA(S3)
LDO
1.5V to 0.75V
Ivterm(Max)=0.42A

DDR3 Channel A

Vdd (Core)=1.5V
Ivdd(Max)=1.8A(per channel)

Vtt (Core)
0.75V
Ivterm(Max)=210mA
(per channel)

DDR3 Channel B

Vdd (Core)=1.5V
Ivdd(Max)=1.8A(per channel)

Vtt (Core)
0.75V
Ivterm(Max)=210mA
(per channel)

HDA Codec

Vcc
5V
Icc(Max)=200mA

Vcc
3.3V
Icc(Max)=40mA

LDO
12V
to 5V

BCM57760 Lan

3.3V_SB
700mA

AVDD12 /DVDD12/EVDD12
340mA

12V

VRD 11.1
Switching
3 Phase

Linear 1.8V
to 1.2V
6A

GMCH 1.1V
21.34A
Switching

3.3V

Linear 1.5V
to 1.5V
TBD A

Linear 15V
to 1.05V
TBD A

RTC
Battery

Proceessor

Vccp (CPU Vcore)
Voltage=1.15~1.5V
Icc(Max)=70A
3-Phases Swithing

1.2V FSB
Vtt=4.6A

Eaglelake GMCH

FSB_Vtt
1.2V FSB Vtt
Icc(Max)=1.3A

1.5V_STR 3.73A

Vcore (Core Logic)
1.1V
Icc(Max)=13.8A(Integrated)
*1.1V (DMI&PCIe)
VCCA_EXP 2.47A
1.1V
VCC_CL 4.3A

3.3V VCCA_DAC 66mA
3.3V VCC3_3 15.8mA

ICH7

VCC1_5A (USB and SATA)
0.97A

VCC1_5B (PCIE)
0.74A

VCCDMIPLL (DMI)
TBD A 1.5V

1.05V (Core)
Vcc1_05 1.31A

1.2V (FSB_Vtt)
V_CPU_IO 14mA

RTC=TBD uA

3.3V
VccSus3_3 0.7A

3.3V
VCC3_3 0.58A

5V Ref 6mA

5VRefSus 10mA

CK505

Vdd (Core)
3.3V
Ivdd(Max)=250mA

Super I/O

5V_SYS

5V_SB_SYS

3D3_SYS

5V

5VSB

USB2.0 8 Ports

+5V DUAL=4A(S0, S1)
+5V DUAL=20mA(S3)

5V_DUAL
Icc(Max)=
TBD A(S0,S1)
22mA(S3)

PS2

+5V DUAL=345mA(S0, S1)
+5V DUAL=2mA(S3)

PCI Express X16 slot (1)

+12V=5.5A

3.3VSB
Icc(Max)=0.375A(wake)
Icc(Max)=0.02A(no wake)

+3.3V=3A

12V

3.3V

PCI Express X1 Per slot (1)

+12V=0.5A

3.3VSB
Icc(Max)=0.375A(wake)
Icc(Max)=0.02A(no wake)

+3.3V=3A

PCI Slot(2)

-12V
Icc(Max)=0.1A

5V
Icc(Max)=5A

3.3V
Icc(Max)=7.6A

12V
Icc(Max)=0.5A

3.3VSB
Icc(Max)=0.375A(wake)
Icc(Max)=0.02A(no wake)

-12V

5V

5V_DUAL to
3.3SB TBD A

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Title: Power Delivery Map

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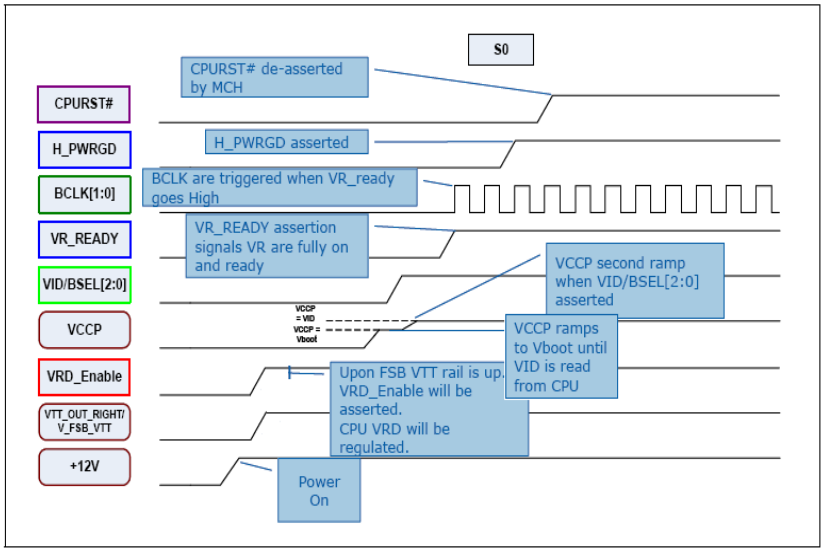
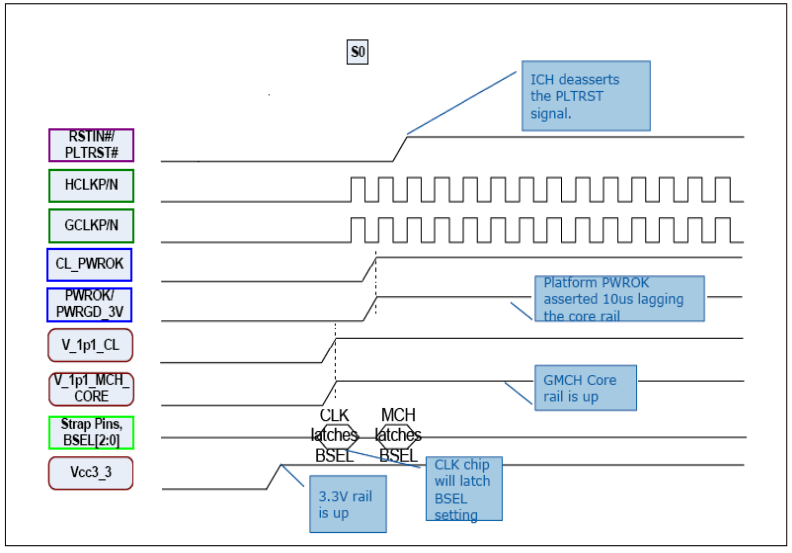
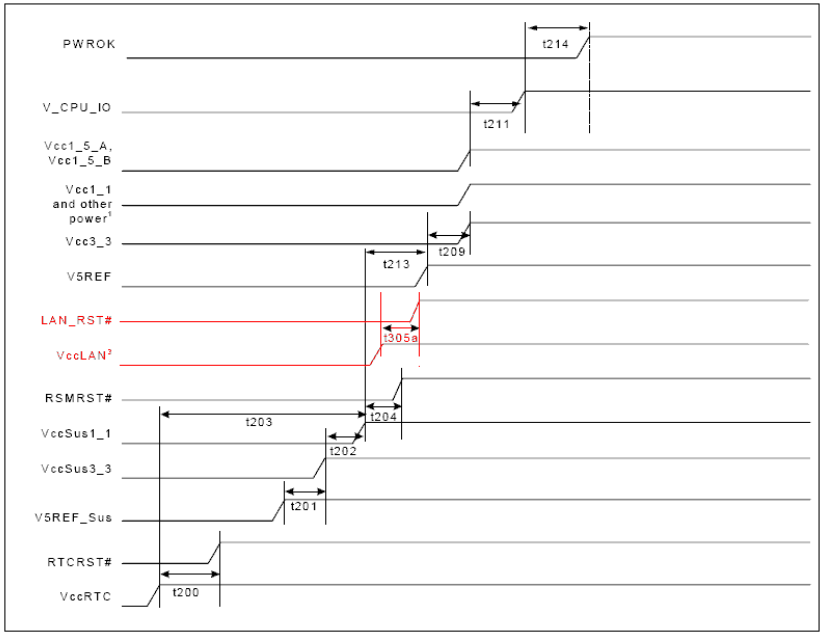
Eaglelake Platform Sequencing:- CPU VR Sequencing Diagram



Eaglelake Platform Sequencing:- GMCH Sequencing Diagram



Power Sequencing and Reset Signal Timings



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Title: Platform Sequence		
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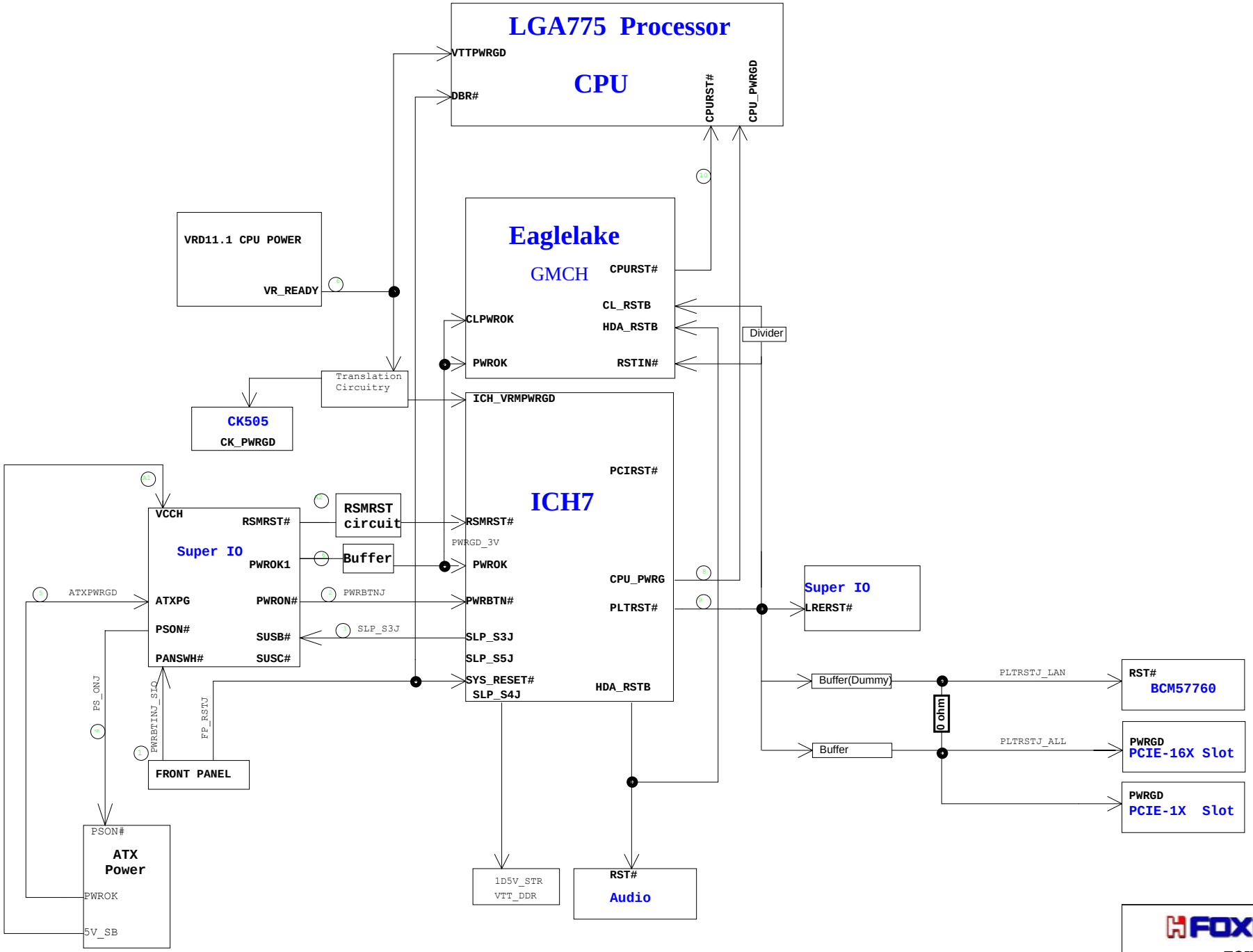

FOXCONN PCEG

Title	Reset Map	
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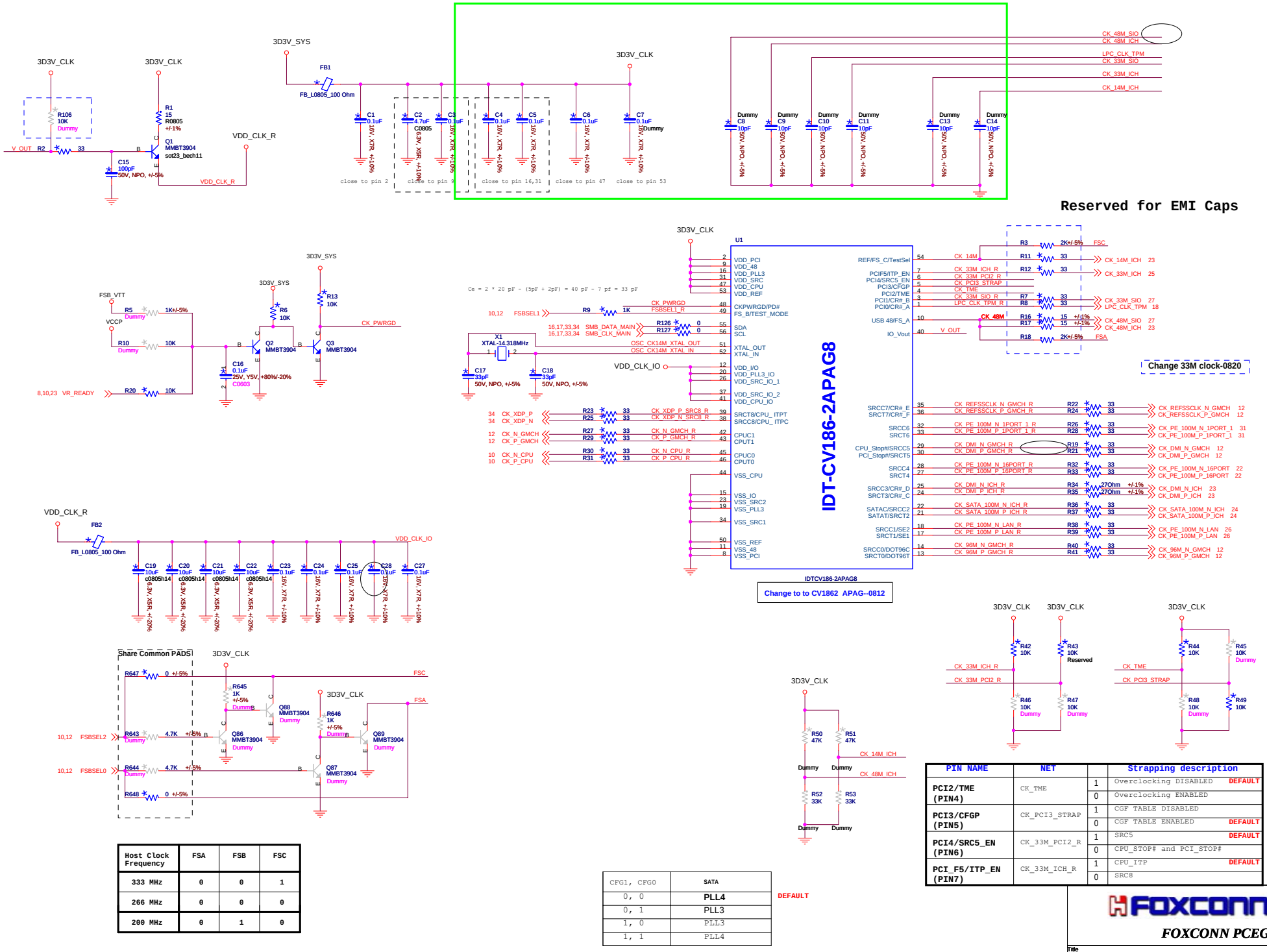

Host Clock Frequency	FSA	FSB	FSC
333 MHz	0	0	1
266 MHz	0	0	0
200 MHz	0	1	0

CFG1, CFG0	SATA
0, 0	PLL4
0, 1	PLL3
1, 0	PLL3
1, 1	PLL4

DEFAULT

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	CK_TME	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI3/CFGP (PIN5)	CK_PCI3_STRAP	1	CGF TABLE DISABLED
		0	CGF TABLE ENABLED DEFAULT
PCI4/SRC5_EN (PIN6)	CK_33M_PCI2_R	1	SRC5 DEFAULT
		0	CPU_STOP# and PCI_STOP#
PCI_F5/ITP_EN (PIN7)	CK_33M_ICH_R	1	CPU_ITP DEFAULT
		0	SRC8

FOXCONN PCEG

Title: CK505 ClockGen

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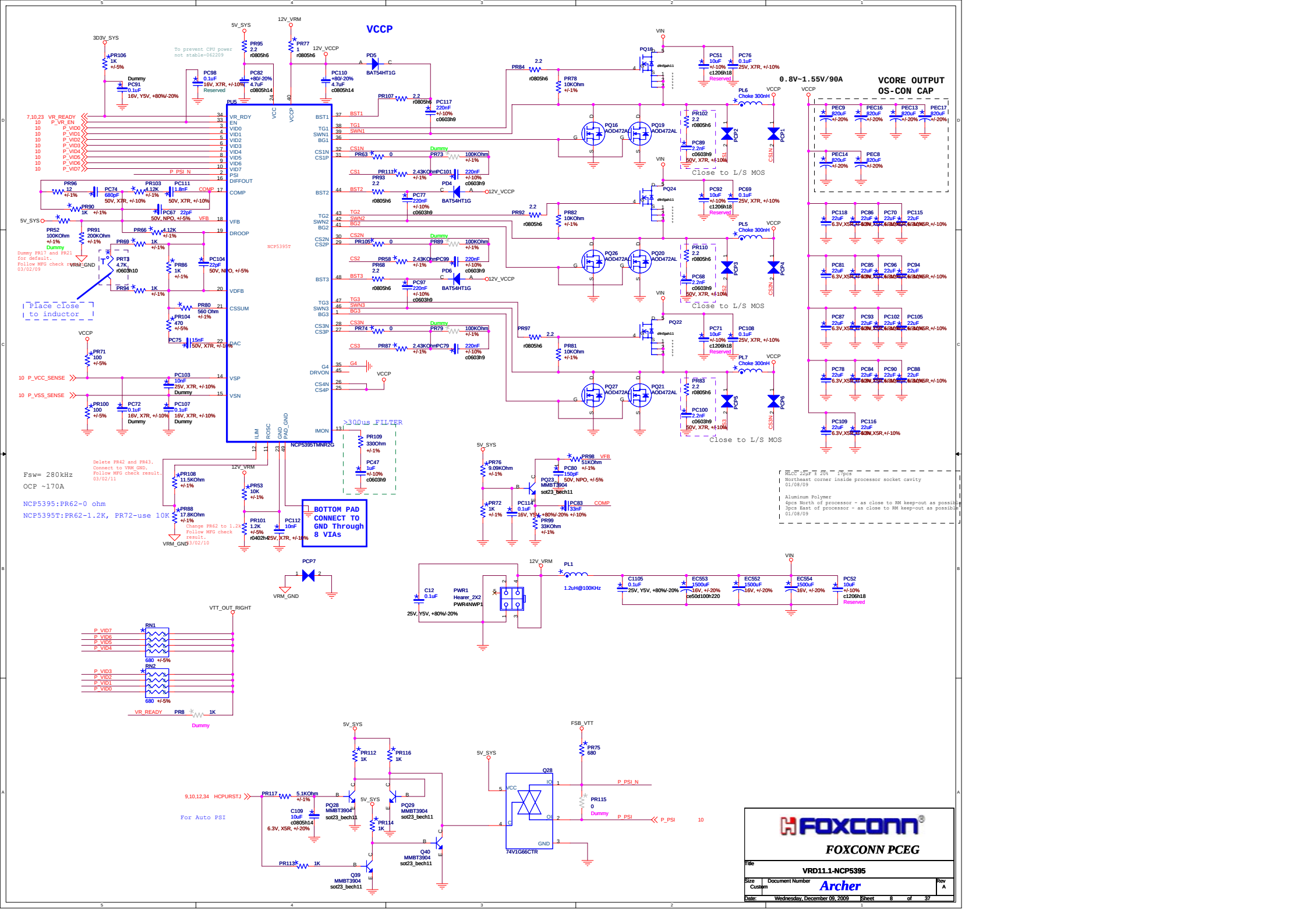
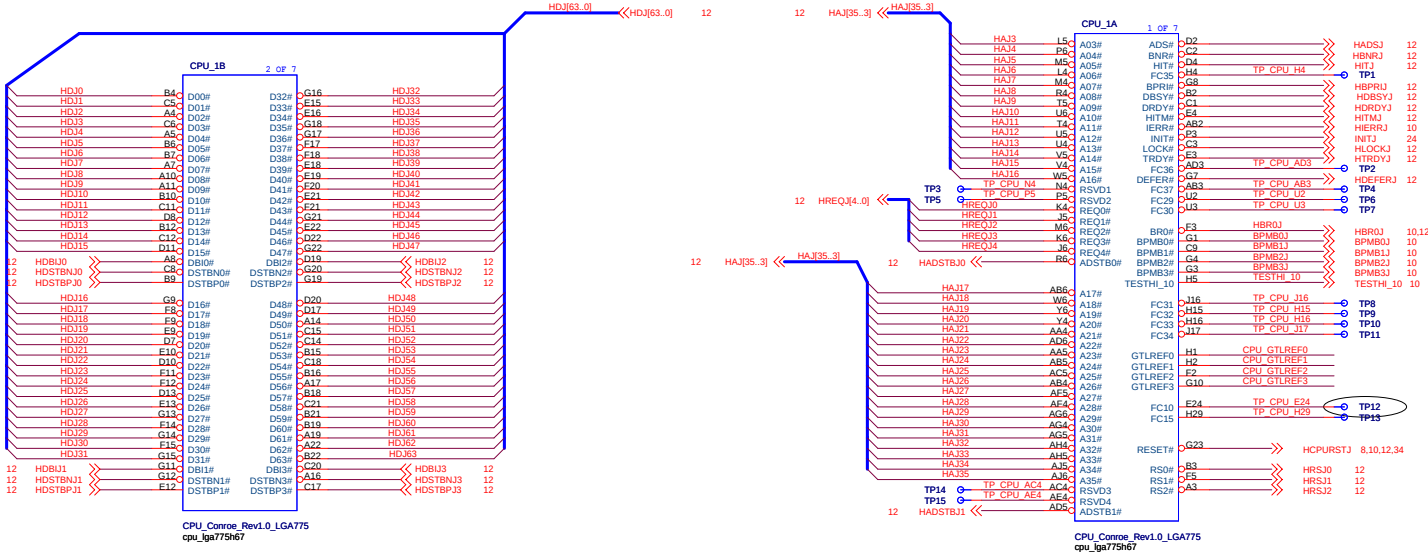
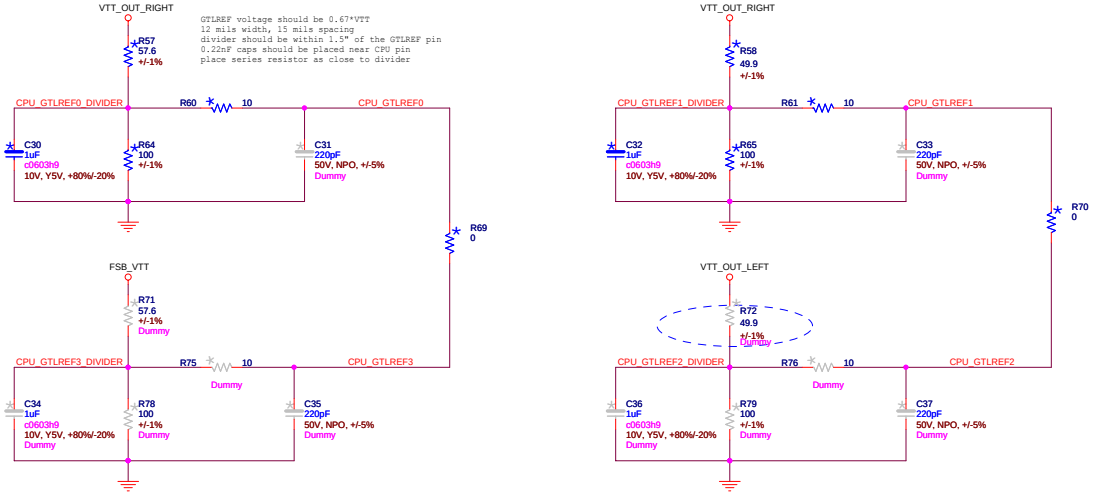
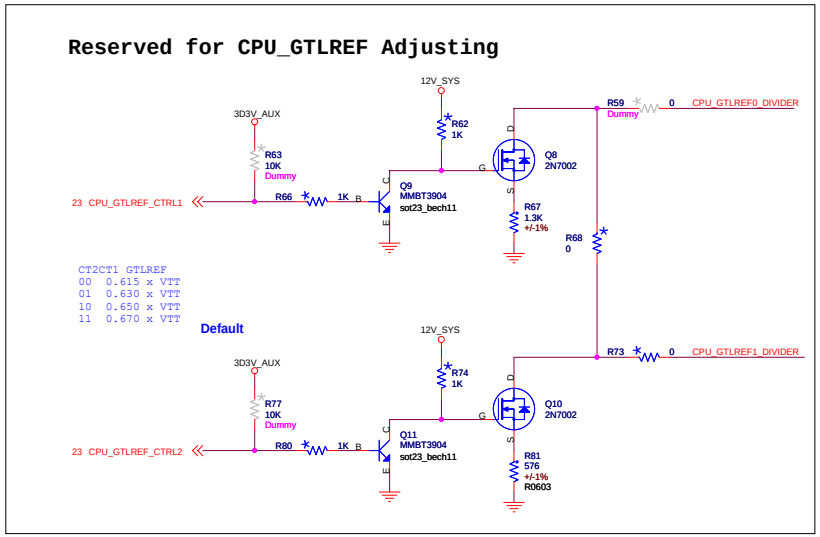

VCCP
VCORE OUTPUT
OS-CON CAP
0.8V~1.55V/90A
Close to L/S MOS
Place close to inductor
>300us FILTER
BOTTOM PAD CONNECT TO GND Through 8 VIAs
Fsw= 280kHz
OCP ~170A
NCP5395:PR62-0 ohm
NCP5395T:PR62-1.2K, PR72-use 10K
For Auto PSI
NCP5395T
NCP5395TMNR2G
FOXCONN PCEG
VRD11.1-NCP5395
Archer







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Title	LGA775 -1	
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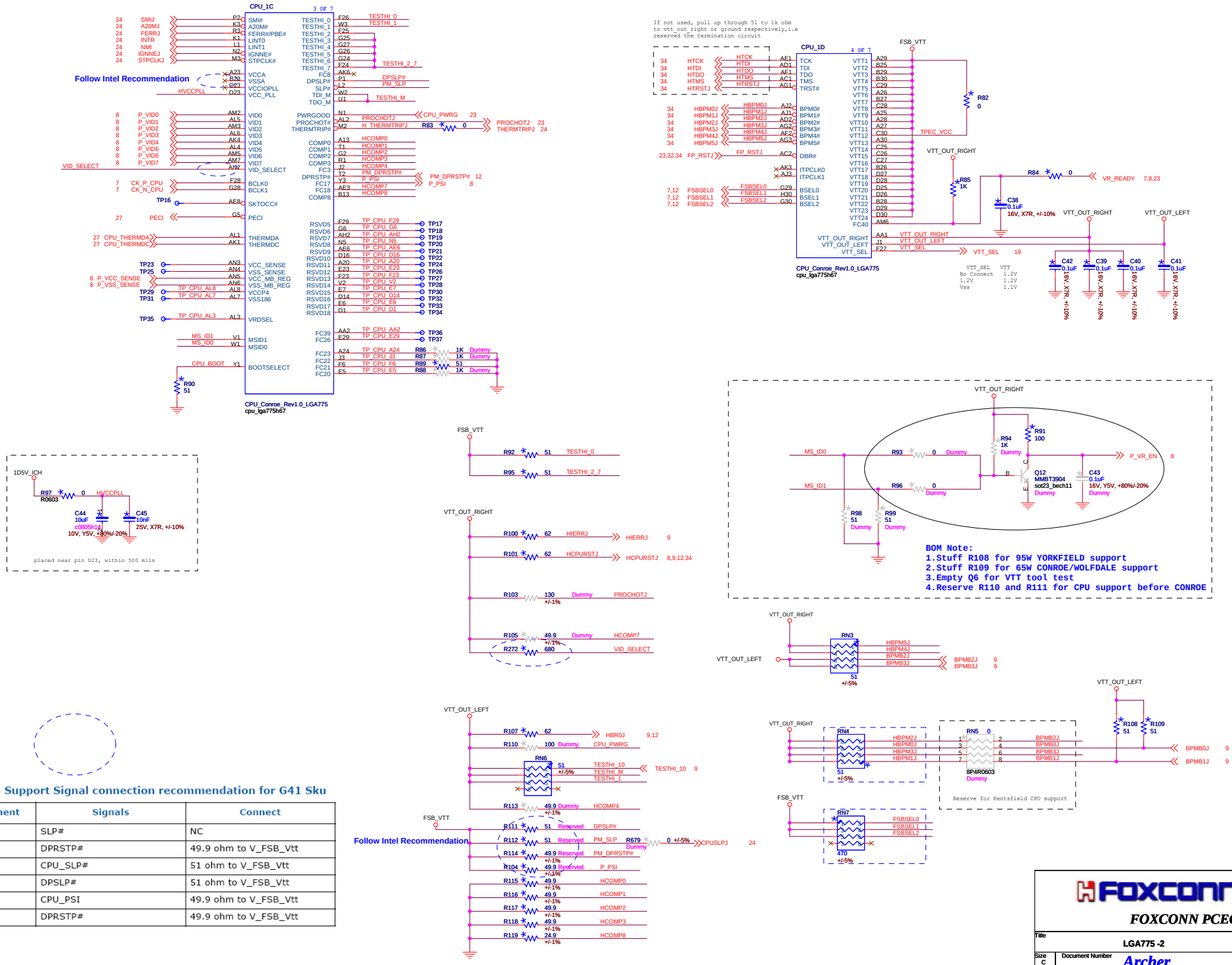

No C3/C4 Support Signal connection recommendation for G41 Sku

Component	Signals	Connect
MCH	SLP#	NC
MCH	DPRSTP#	49.9 ohm to V_FSB_Vtt
CPU	CPU_SLP#	51 ohm to V_FSB_Vtt
CPU	DPSLP#	51 ohm to V_FSB_Vtt
CPU	CPU_PSI	49.9 ohm to V_FSB_Vtt
CPU	DPRSTP#	49.9 ohm to V_FSB_Vtt

FOXCONN PCEG

Title: LGA775 -2

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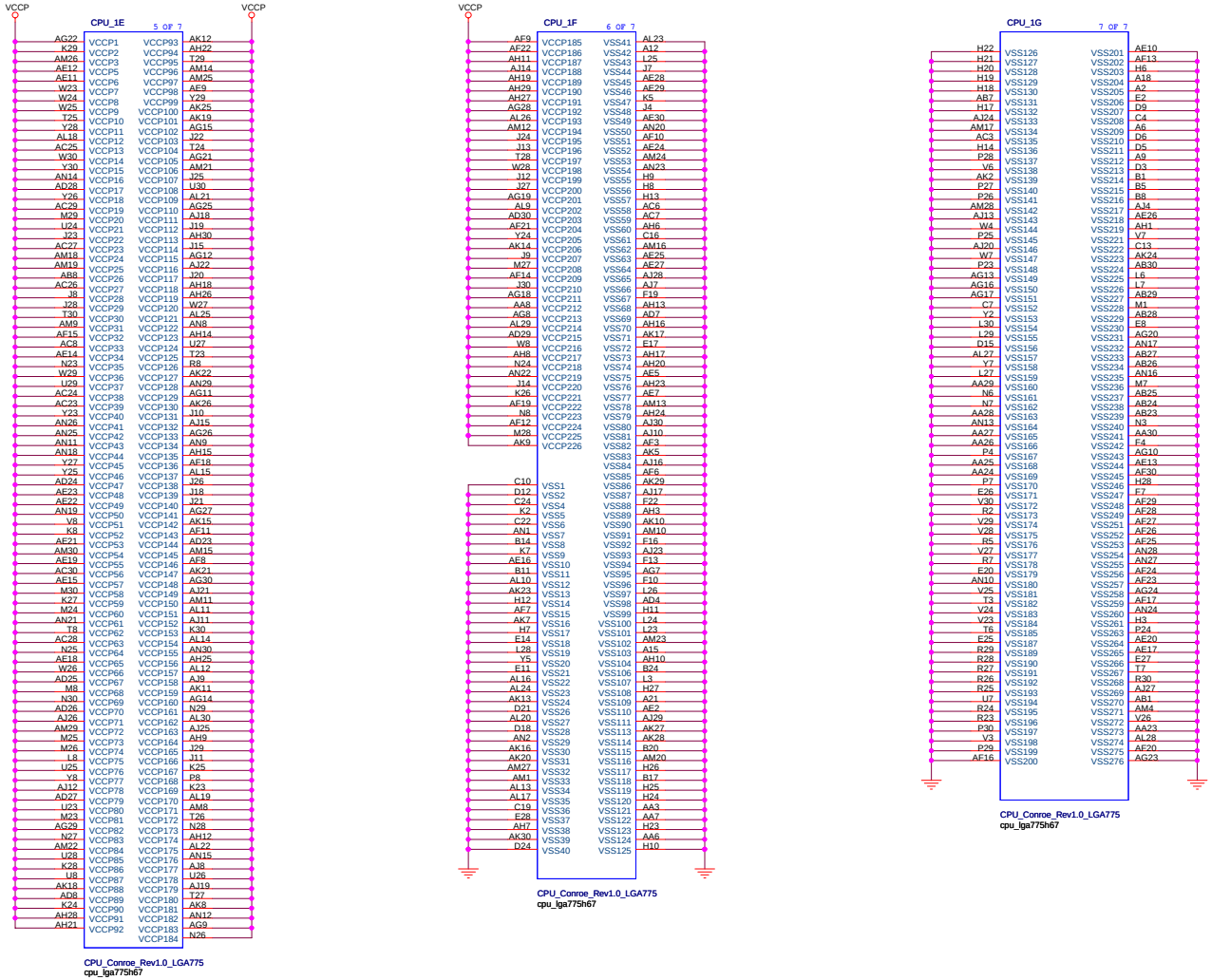

FOXCONN PCEG

Title	LGA775 -3	
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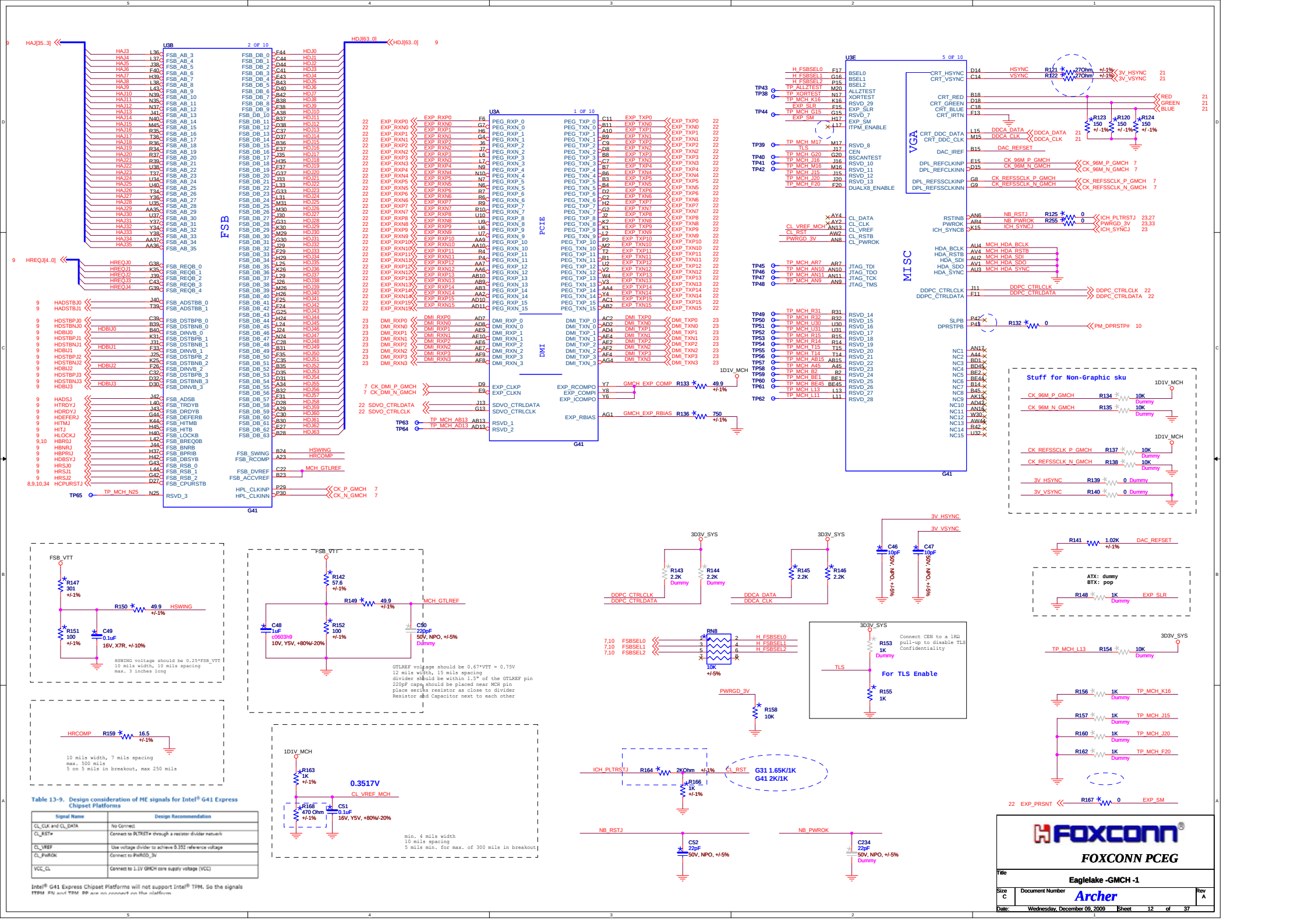

Table 13-9. Design consideration of ME signals for Intel® G41 Express Chipset Platforms

Signal Name	Design Recommendation
CL_CLK and CL_DATA	No Connect
CL_RST#	Connect to PLTRST# through a resistor divider network
CL_VREF	Use voltage divider to achieve 0.352 reference voltage
CL_PWROK	Connect to PWRGD_3V
VCC_CL	Connect to 1.1V GMCH core supply voltage (VCC)

Intel® G41 Express Chipset Platforms will not support Intel® TPM. So the signals TPM_EN and TPM_PP are no connect on the platform.

FOXCONN PCEG

Title	Eaglelake -GMCH -1		
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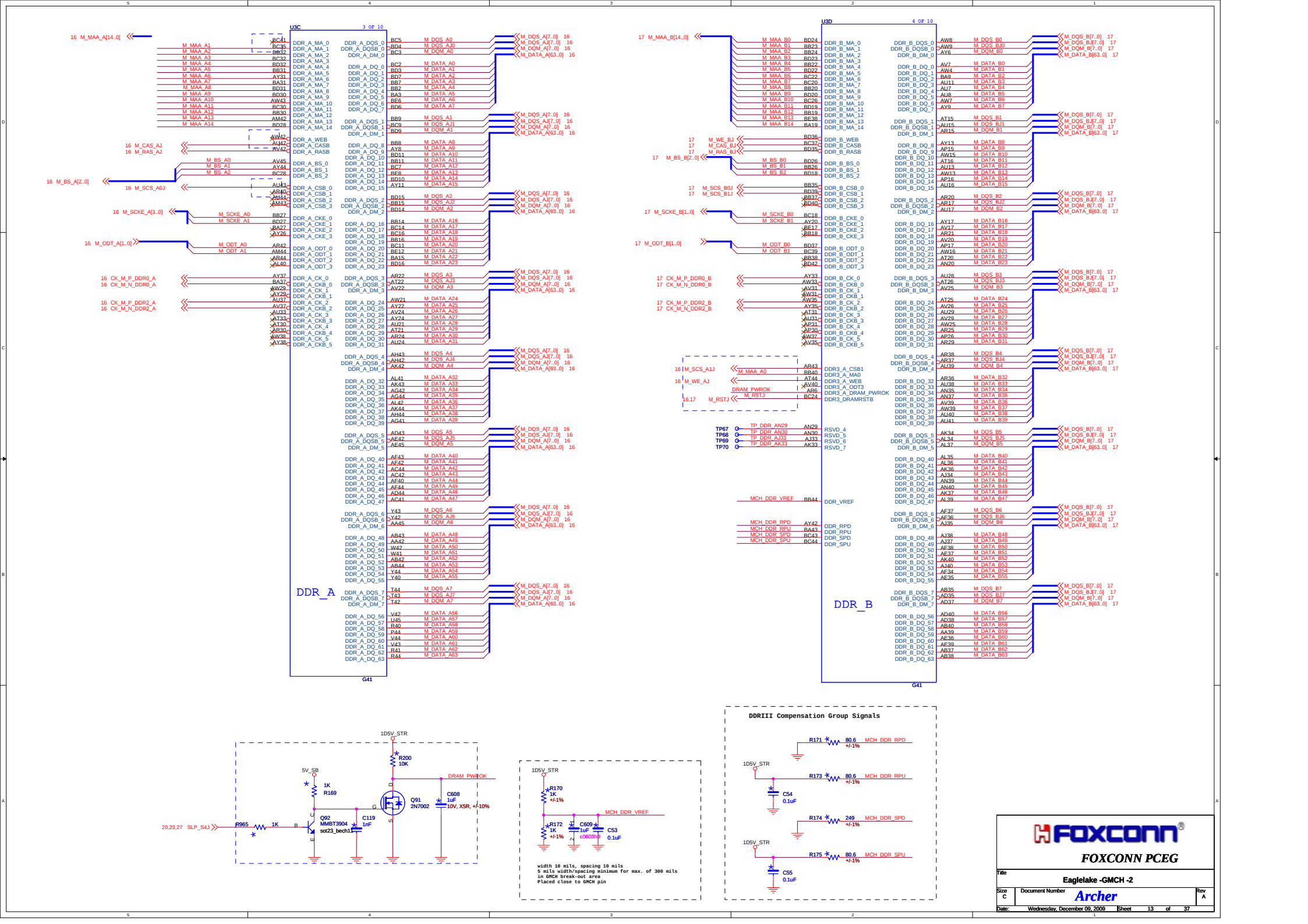
U3C
3 OF 10
DDR_A
G41
U3D
4 OF 10
DDR_B
G41
DDRIII Compensation Group Signals
R171 80.6 +/-1% MCH_DDR_RPD
R173 80.6 +/-1% MCH_DDR_RPU
C54 0.1uF
R174 249 +/-1% MCH_DDR_SPD
R175 80.6 +/-1% MCH_DDR_SPU
C55 0.1uF
1D5V_STR
R200 10K
5V_SB
R169 1K
Q91 2N7002
Q92 MMBT3904 sot23_bech1
C608 1uF 10V, X5R, +/-10%
C119 1nF
R965 1K
20,23,27 SLP_S4J
DRAM_PWROK
R170 1K +/-1%
R172 1K +/-1%
C609 1uF c0603h0
C53 0.1uF
MCH_DDR_VREF
width 10 mils, spacing 10 mils
5 mils width/spacing minimum for max. of 300 mils
in GMCH break-out area
Placed close to GMCH pin
FOXCONN PCEG
Title
Eaglelake -GMCH -2
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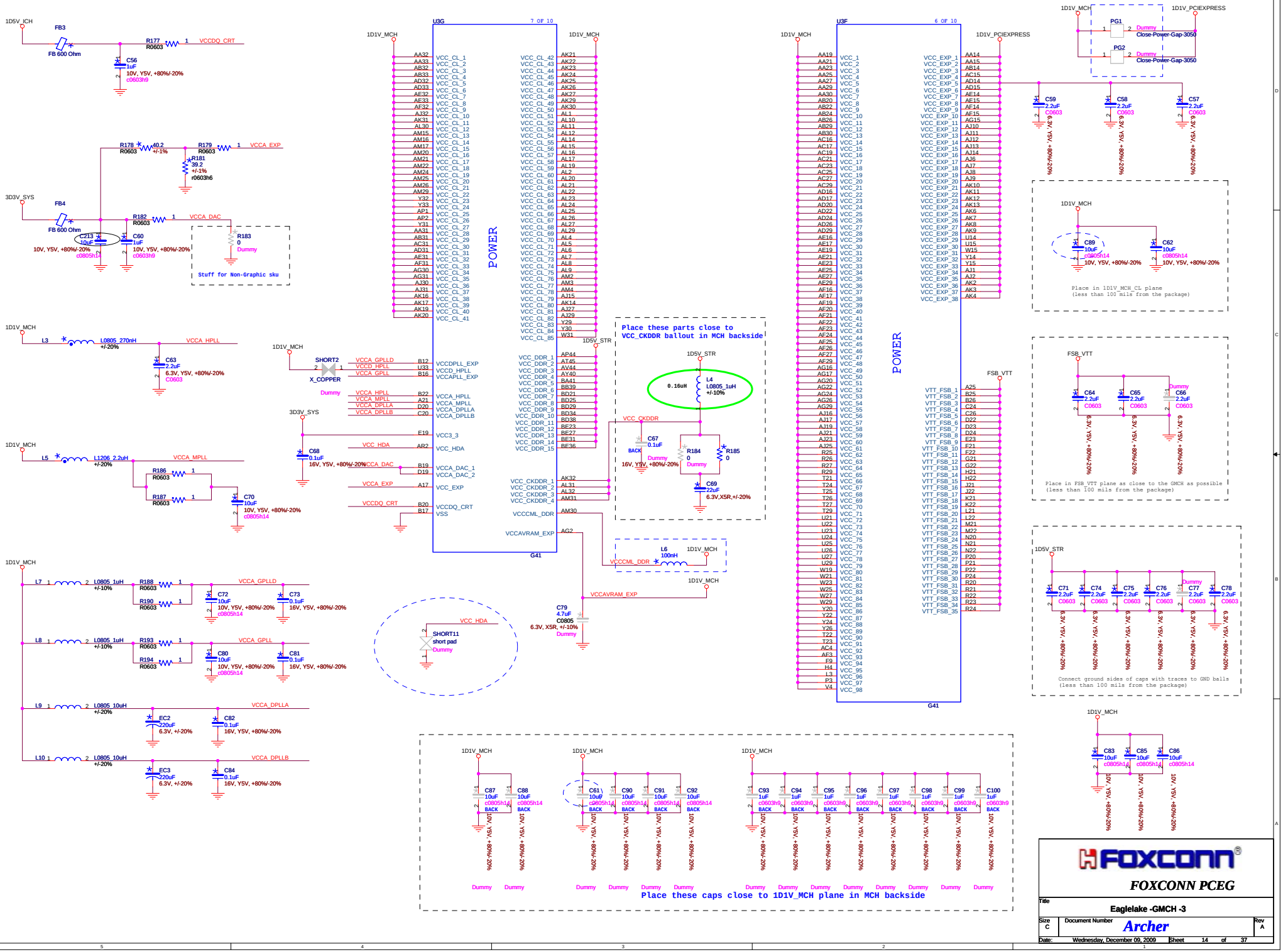

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Title	Eaglelake -GMCH -3	
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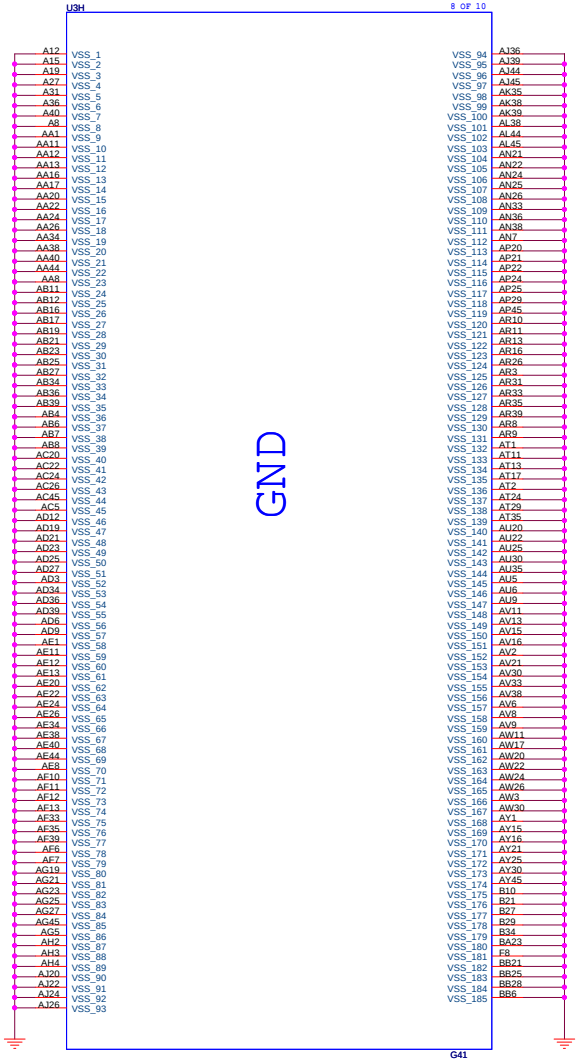

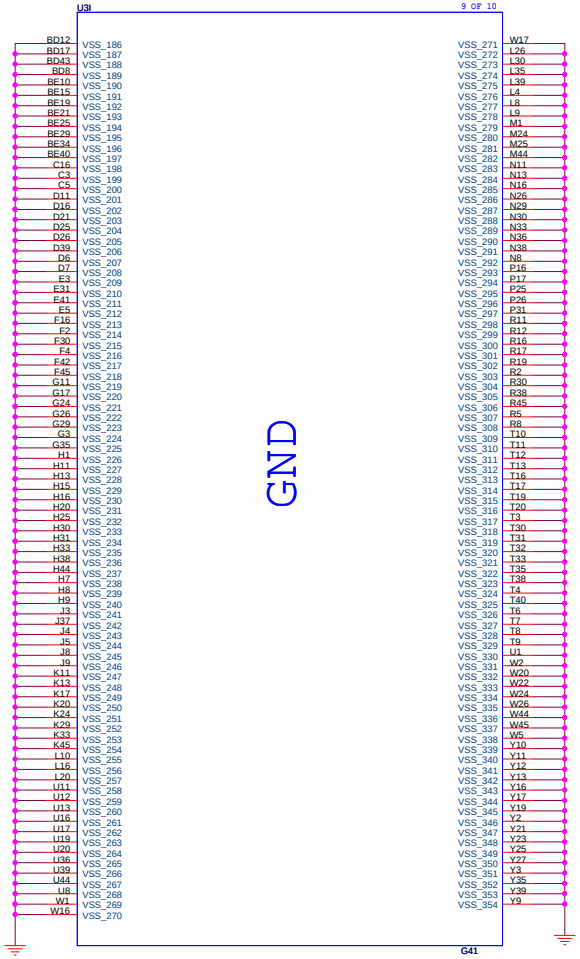

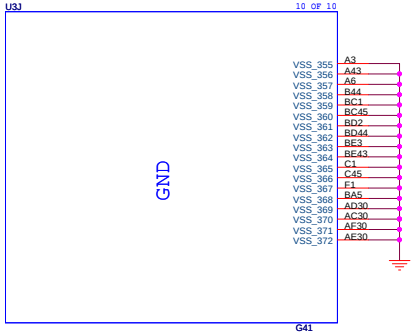

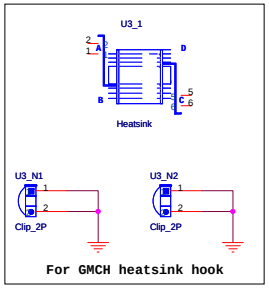

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Title: Eaglelake -GMCH -4		
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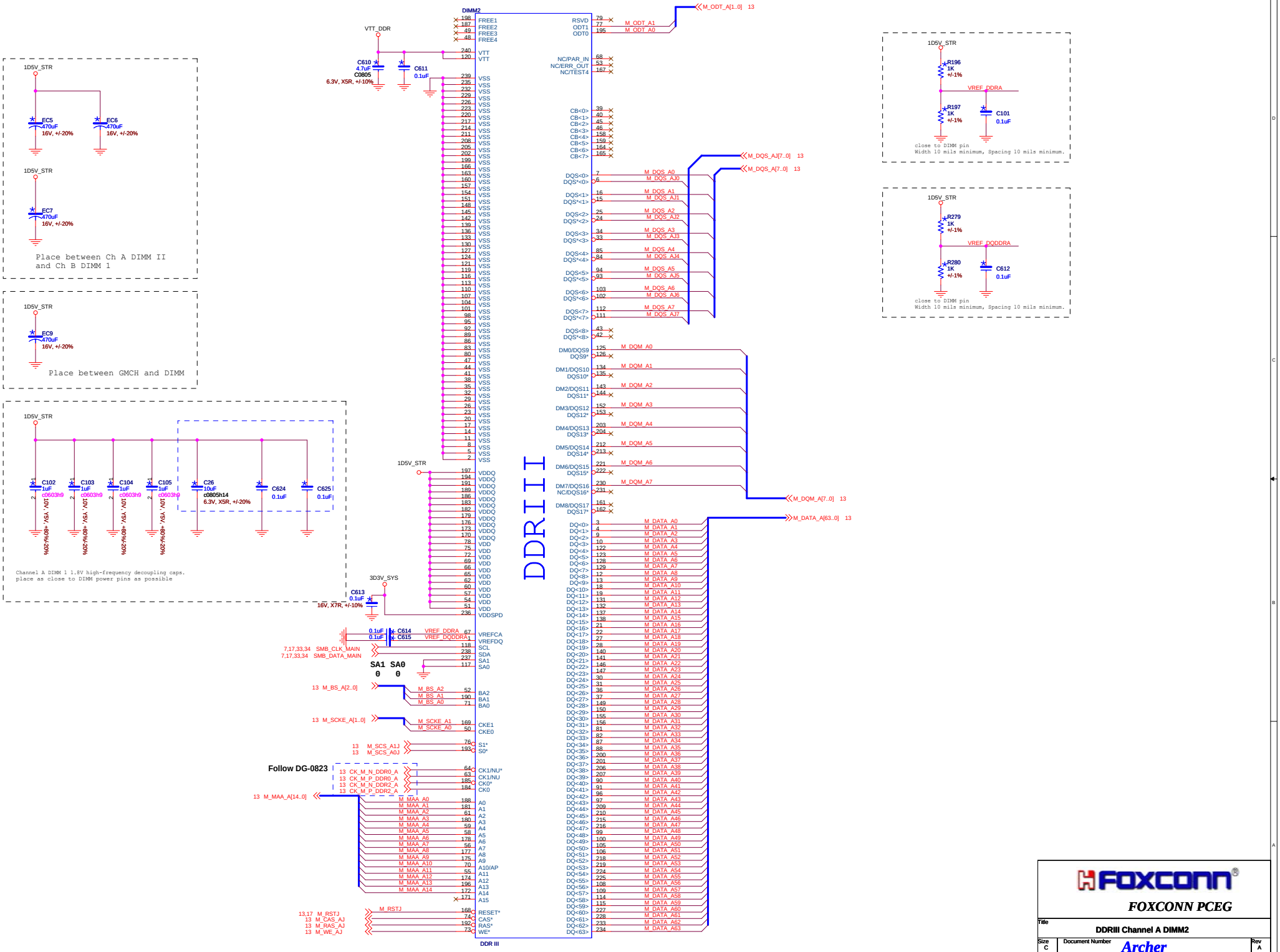
DIMM2
DDR III
DDR III
1D5V_STR
EC5 470uF 16V, +/-20%
EC6 470uF 16V, +/-20%
EC7 470uF 16V, +/-20%
Place between Ch A DIMM II and Ch B DIMM 1
EC9 470uF 16V, +/-20%
Place between GMCH and DIMM
C102 1uF c0603h9
C103 1uF c0603h9
C104 1uF c0603h9
C105 1uF c0603h9
C26 10uF c0805h14 6.3V, X5R, +/-20%
C624 0.1uF
C625 0.1uF
Channel A DIMM 1 1.8V high-frequency decoupling caps.
place as close to DIMM power pins as possible
VTT_DDR
C610 4.7uF C0805 6.3V, X5R, +/-10%
C611 0.1uF
3D3V_SYS
C613 0.1uF 16V, X7R, +/-10%
C614 0.1uF
C615 0.1uF
VREF_DDRA
VREF_DQDDRA
SA1 SA0
0 0
Follow DG-0823
M_ODT_A[1..0] 13
M_DQS_AJ[7..0] 13
M_DQS_A[7..0] 13
M_DQM_A[7..0] 13
M_DATA_A[63..0] 13
13 M_BS_A[2..0]
13 M_SCKE_A[1..0]
13 M_MAA_A[14..0]
7,17,33,34 SMB_CLK_MAIN
7,17,33,34 SMB_DATA_MAIN
13,17 M_RSTJ
13 M_CAS_AJ
13 M_RAS_AJ
13 M_WE_AJ
1D5V_STR
R196 1K +/-1%
VREF_DDRA
R197 1K +/-1%
C101 0.1uF
close to DIMM pin
Width 10 mils minimum, Spacing 10 mils minimum.
1D5V_STR
R279 1K +/-1%
VREF_DQDDRA
R280 1K +/-1%
C612 0.1uF
close to DIMM pin
Width 10 mils minimum, Spacing 10 mils minimum.
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FOXCONN PCEG
Title
DDRIII Channel A DIMM2
Size C
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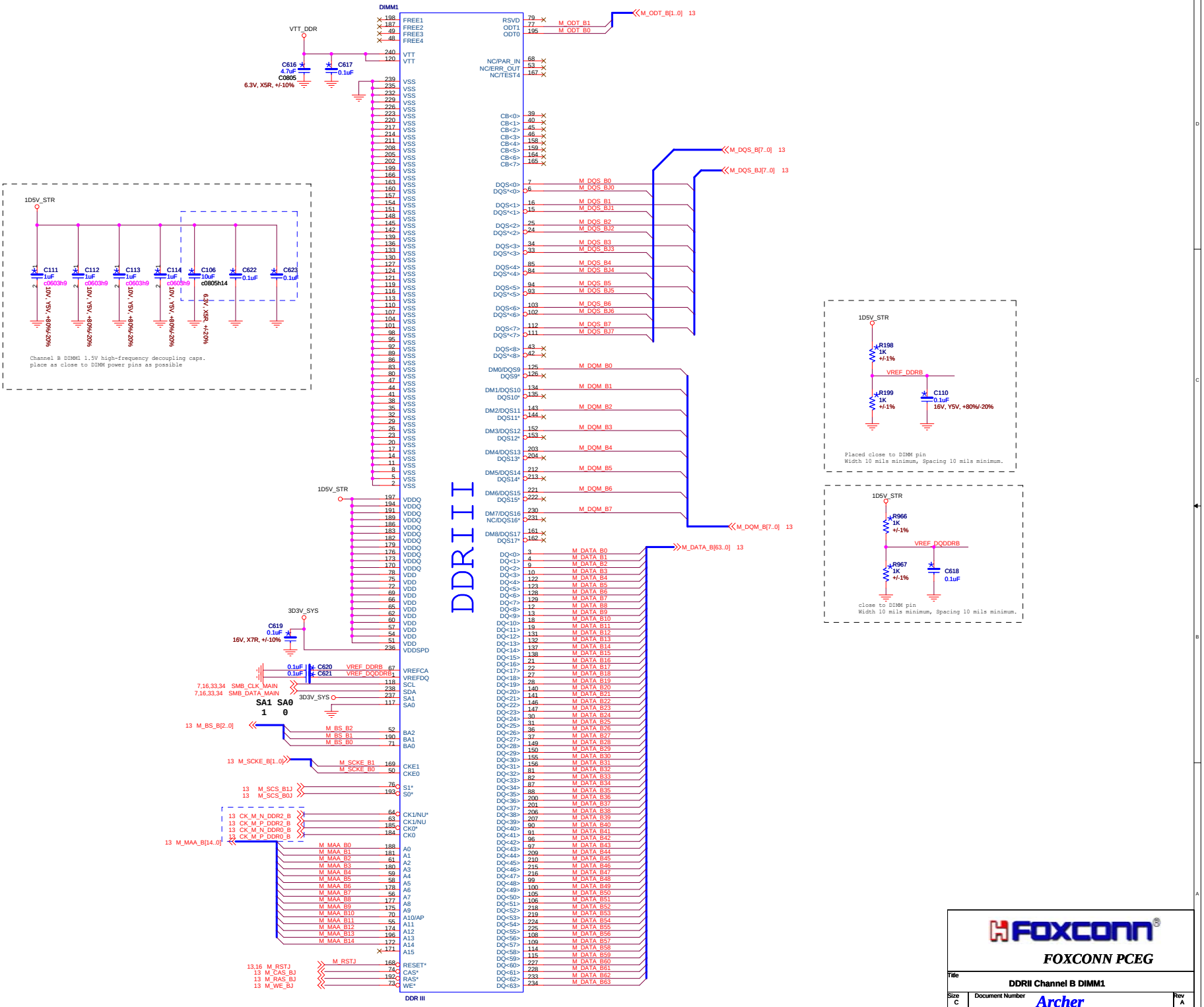

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Title	DDRII Channel B DIMM1		
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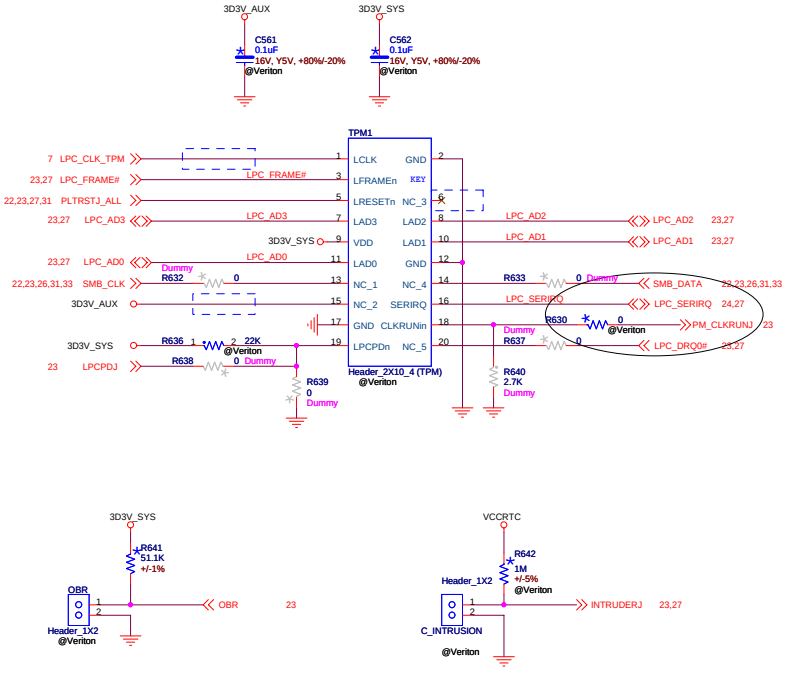

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Title	TPM/OBR/INTRUDER	
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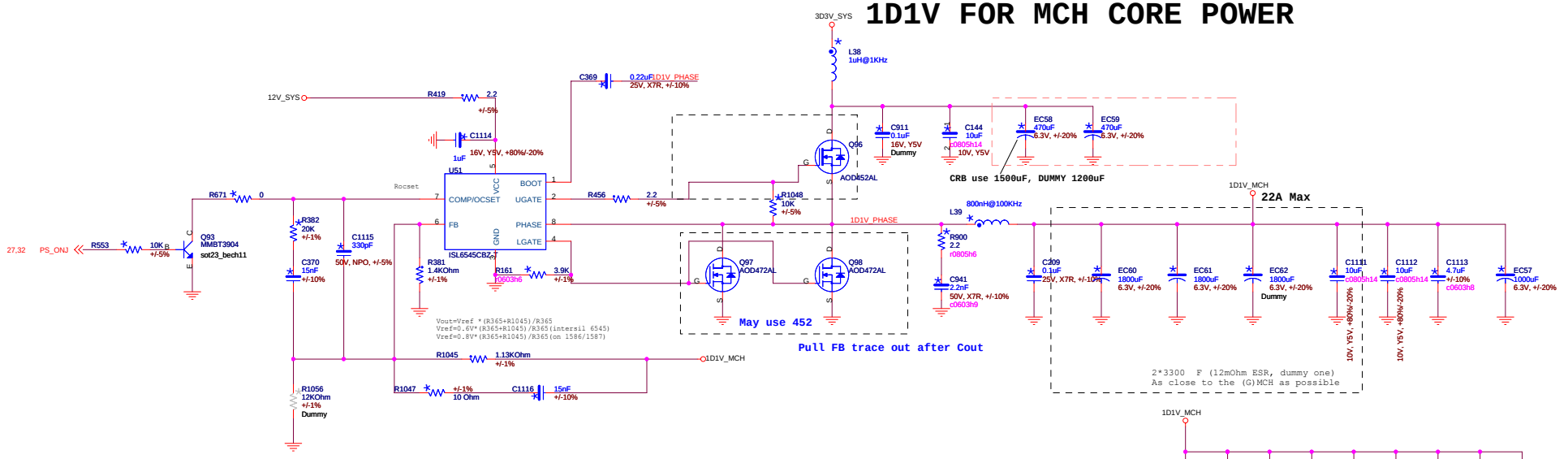
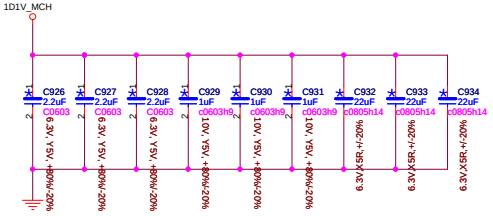
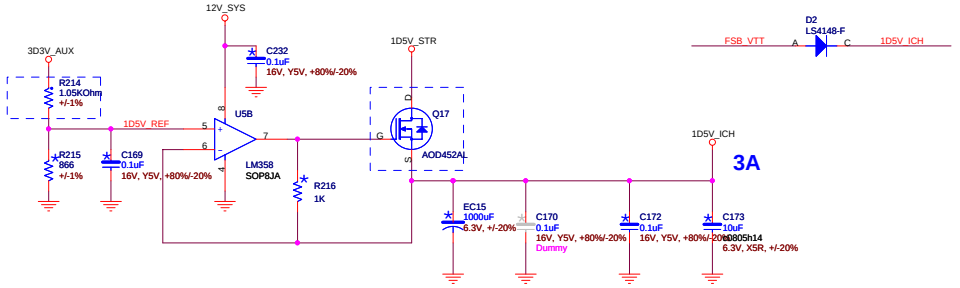
1D1V FOR MCH CORE POWER

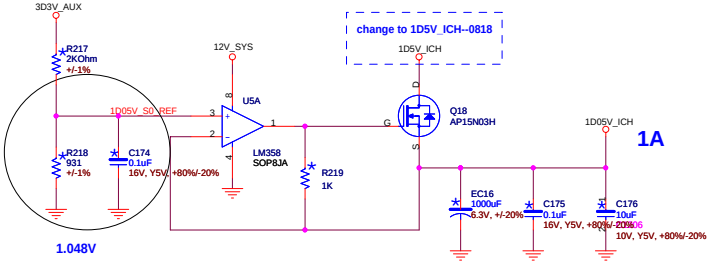




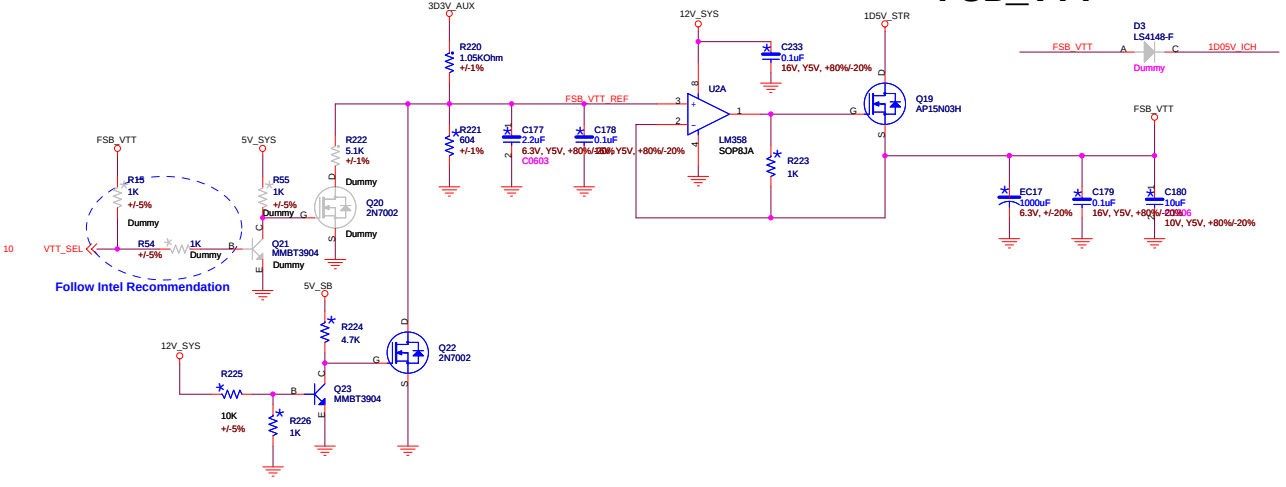
1D5V_ICH



1D05V_ICH



FSB_VTT



FOXCONN PCEG			
Title: 1D1V/1D5V/FSB_VTT			
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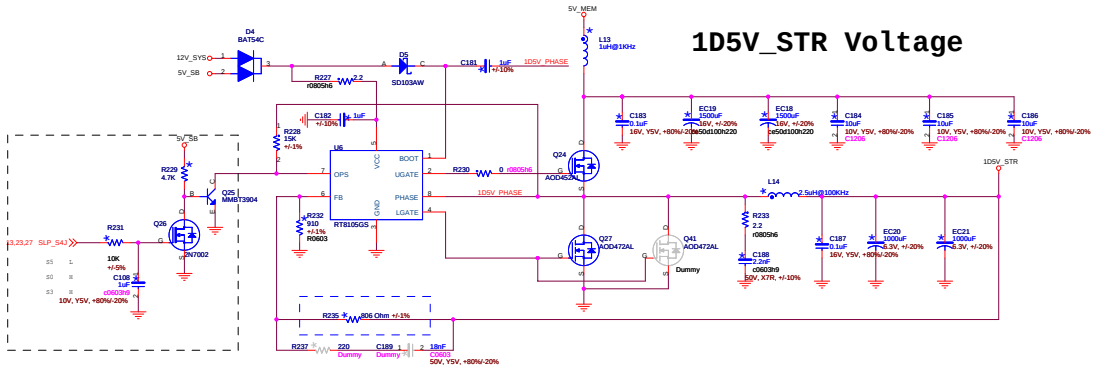
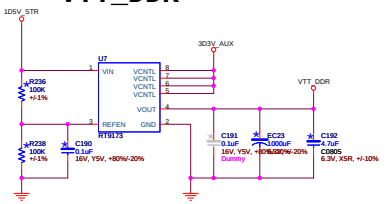
1D5V_STR Voltage

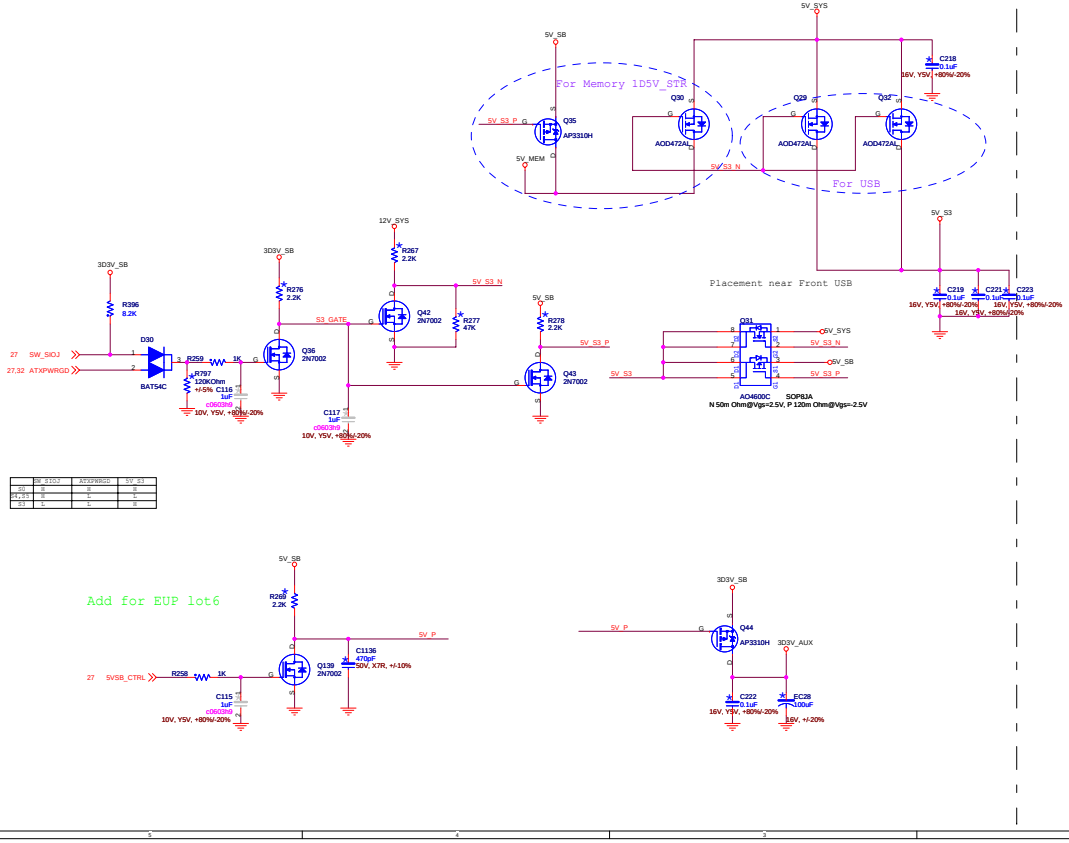


VOUT= 0.8V(1+R235/R232)
1.508V

VTT_DDR

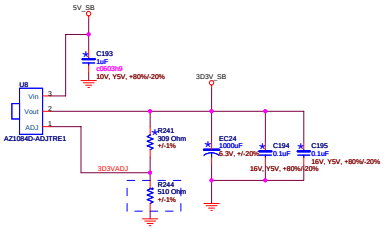


5V_MEM/5V_S3/3D3V_AUX



	SW_SIOJ	ATXPWRGD	5V_S3
S0	H	H	H
S1,S3	H	L	L
S5	L	L	L

3D3V_DUAL

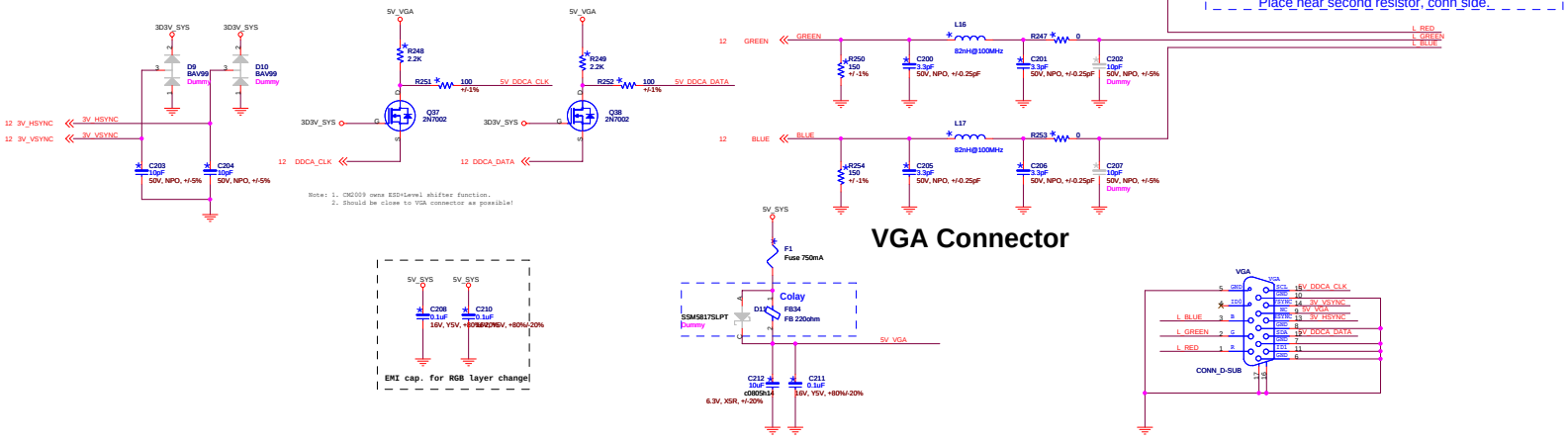


FOXCONN®
FOXCONN PCEG

Title	STR1D5V/3D3_DUAL/5V_S3	
Size: Custom	Document Number: Archer	Rev: A
Date: Wednesday, December 09, 2009	Sheet 20 of 37	

The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.

RGB routing
1. from GMCH to the first 150 ohm resistor: 7.5 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 4 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 700 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced



VGA Connector

The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.

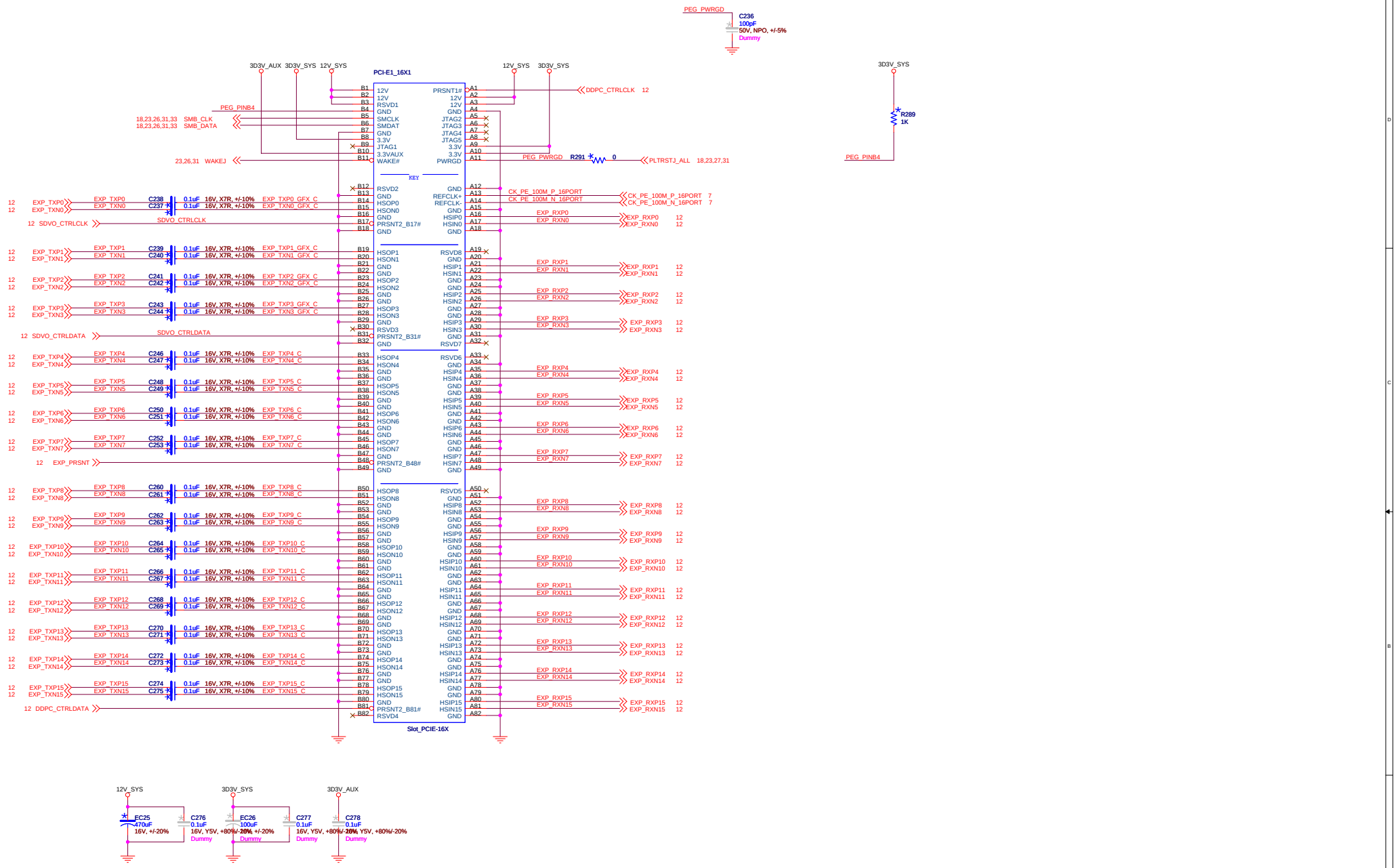
FOXCONN

FOXCONN PCEG

Title: VGA/DVI-D Connector

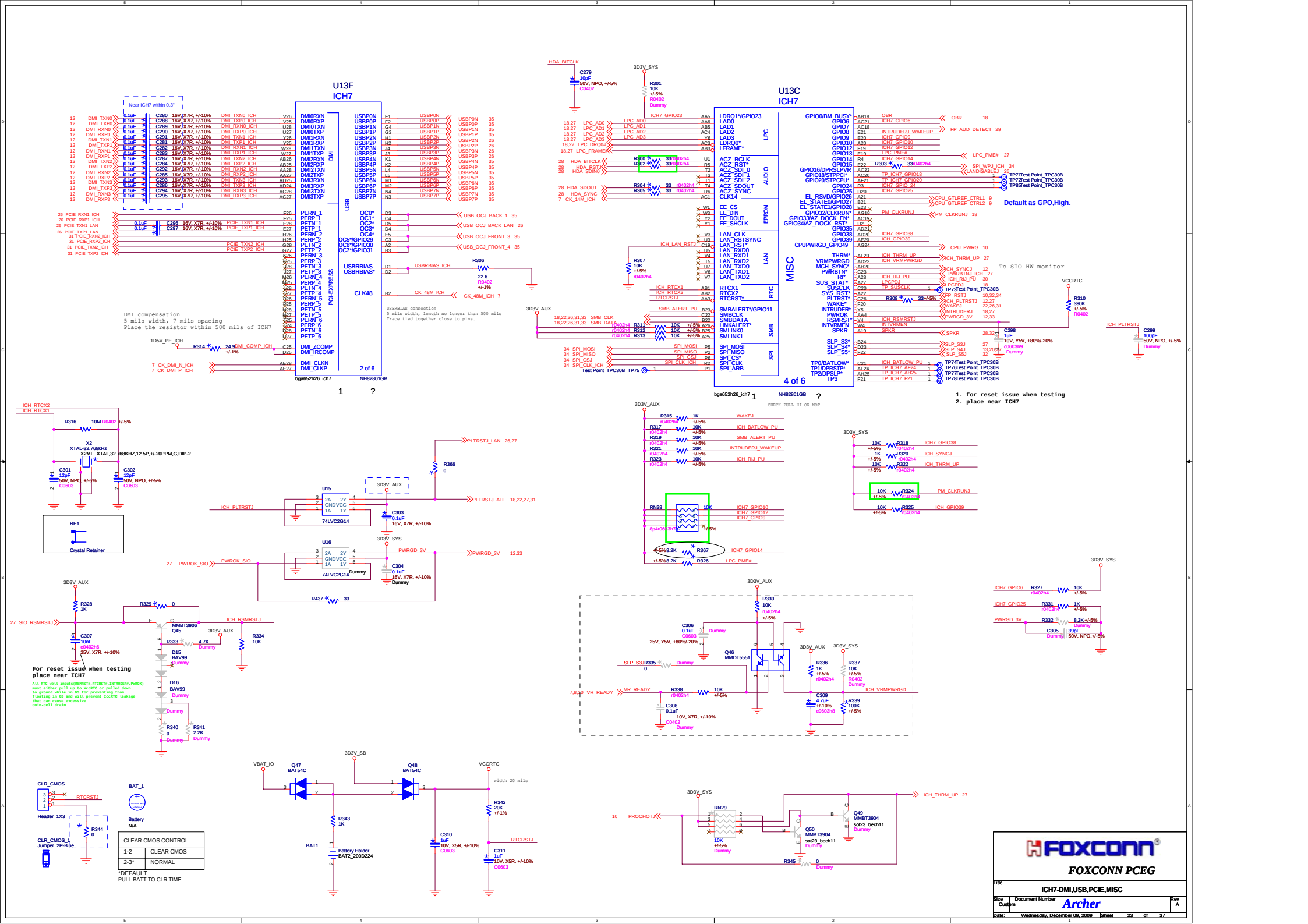
Size: Custom | Document Number: Archer | Rev: A

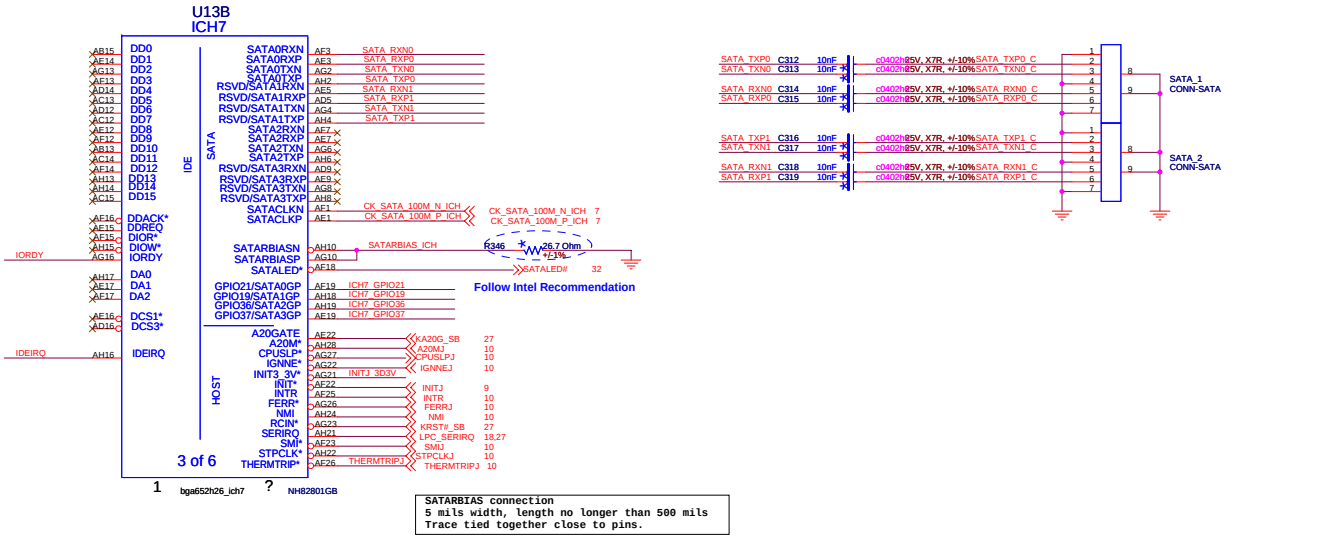
Date: Wednesday, December 09, 2009 | Sheet 21 of 37



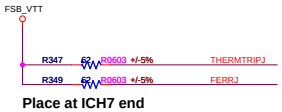
FOXCONN PCEG

Title	PCI-E x16 Slot / Genll Switch	
Size C	Document Number Archer	Rev A
Date: Wednesday, December 09, 2009	Sheet 22 of 37	

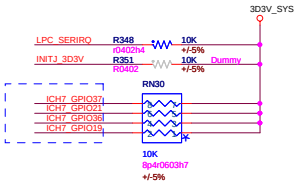

U13F
ICH7
U13C
ICH7
MISC
DMI compensation
5 mils width, 7 mils spacing
Place the resistor within 500 mils of ICH7
USBRBIAS connection
5 mils width, length no longer than 500 mils
Trace tied together close to pins.
Default as GPO,High.
To SIO HW monitor
1. for reset issue when testing
2. place near ICH7
For reset issue when testing
place near ICH7
CLEAR CMOS CONTROL
1-2 CLEAR CMOS
2-3* NORMAL
*DEFAULT
PULL BATT TO CLR TIME
FOXCONN PCEG
ICH7-DMI,USB,PCIE,MISC
Archer
Wednesday, December 09, 2009

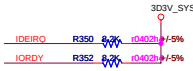


SATARBIAS connection
5 mils width, length no longer than 500 mils
Trace tied together close to pins.

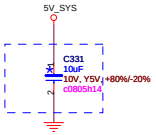


Place at ICH7 end

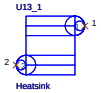




IDE data lines should be matched to strobes(IORJ, RDY)within +/- 250 mils, strobes should be matched to their complement within +/- 10 mils



For ICH heatsink hook



FOXCONN PCEG

Title	ICH7-HOST& SATA	
Size: Custom	Document Number: Archer	Rev: A
Date: Wednesday, December 09, 2009	Sheet 24 of 37	

Strapping Options Flash		
GNT5#	GNT4#	
0	1	SPI
1	0	PCI
1	1	LPC

Default SPI

U13A
ICH7

PCI

1 of 6

Default: floating

J7	BIOS Memory Range Strap
Short	PCI (BIOS Porting)
Open	LPC (Default) internal pull up 11

VCCDMIPLL LRC Filter

Place LRC near pin A628

ICH7 Core decoupling caps.

PCI-E decoupling caps.

Place near D28, T28, AD28

Place near B27

VCC1_5_B LC Filter

Place LC near pin D28 L26 >0.74A <0.02 Ohm

0302 add R2046 colay L26 jim

DMI decoupling caps.

Place near A628

0302 change R613 to 10 Ohm jim

place cap. near pin F6 within 40 mils

place cap. near pin AD17 within 40 mils

USB decoupling caps.

Place near A1

Place near C1

Place near E3

U13D
ICH7

POWER

5 of 6

SATA decoupling caps.

Place near AH5

Place near AH9

Place near AH11

Place near AD2

Audio decoupling caps.

Place near U6

IDE decoupling caps.

Place near A615

CPU decoupling caps.

Place near AE23 and AE26

Place near AH26

RTC decoupling caps.

Place near W5

LAN decoupling caps.

Place near V1

PCI decoupling caps.

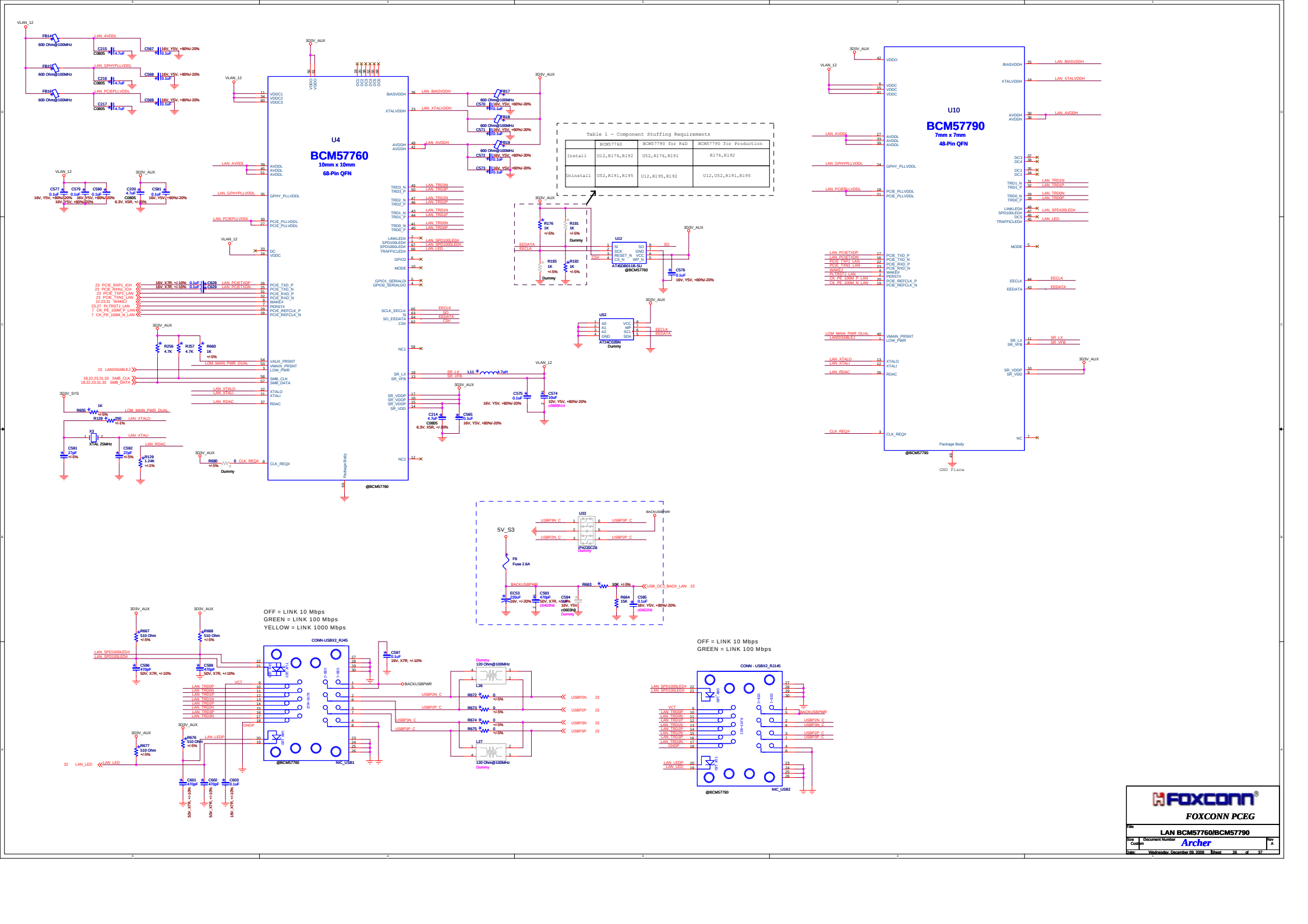
Place near A5, B7, B13, B16

U13E
ICH7

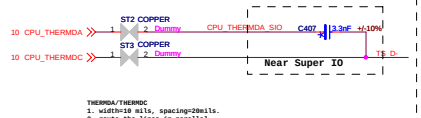
6 of 6

FOXCONN PCEG

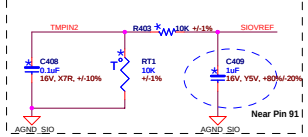
Title	ICH7-PCI & POWER		
Size	Document Number		Rev
Custom	Archer		A
Date:	Wednesday, December 06, 2006	Sheet	25 of 37


U4
BCM57760
10mm x 10mm
68-Pin QFN
U10
BCM57790
7mm x 7mm
48-Pin QFN
Table 1 - Component Stuffing Requirements
BCM57760
BCM57790 for R&D
BCM57790 for Production
Install
U12,R176,R192
U52,R176,R191
R176,R192
Uninstall
U52,R191,R195
U12,R195,R192
U12,U52,R191,R195
OFF = LINK 10 Mbps
GREEN = LINK 100 Mbps
YELLOW = LINK 1000 Mbps
OFF = LINK 10 Mbps
GREEN = LINK 100 Mbps
CONN-USBX2_RJ45
NIC_USB1
NIC_USB2
@BCM57760
@BCM57790
FOXCONN PCEG
LAN BCM57760/BCM57790
Archer
Wednesday, December 09, 2009

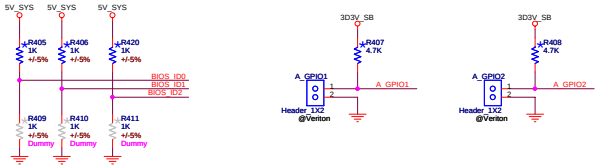
CPU Temperature Monitor



System Temperature Monitor



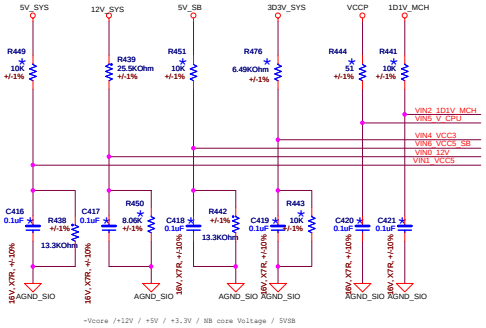
BIOS ID Schematic

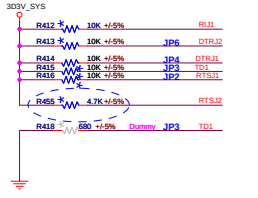


Power On Strapping Options

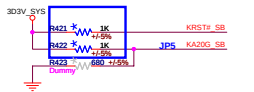
	Symbol	value	Description
JP1 (pin 38)	Flashseg1_EN	1	Disable
		0	Flash I/F Address Segment1 is enable
JP2 (pin 122)	VIDO_SEL	1	Disable VIDOUT pins
		0	Enable VIDOUT pins
JP3 (pin 124)	CHIP_SEL	--	Chip selection in configuration.
JP4 (pin 126)	K8PWR_EN	1	K8 power sequence function is disable
		0	K8 power sequence function is enable
JP3 &JP5 (pin124&pin 46)	FAN_CTL_SEL	11	The default of EC index 15h/16h/17h is 40h
		10	The default of EC index 15h/16h/17h is 7Fh(Fan off)
		01	The default of EC index 15h/16h/17h is 00h(Fan full speed)
		00	The default of EC index 15h/16h/17h is 20h
JP5 (pin 46)	WDT_EN	1	Disable WDT to reset PWROK
		0	Enable WDT to reset PWROK
JP6 (pin 29)	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function

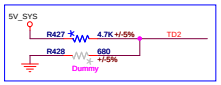
Voltage Monitor

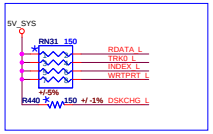


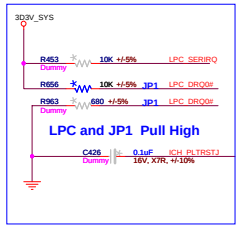


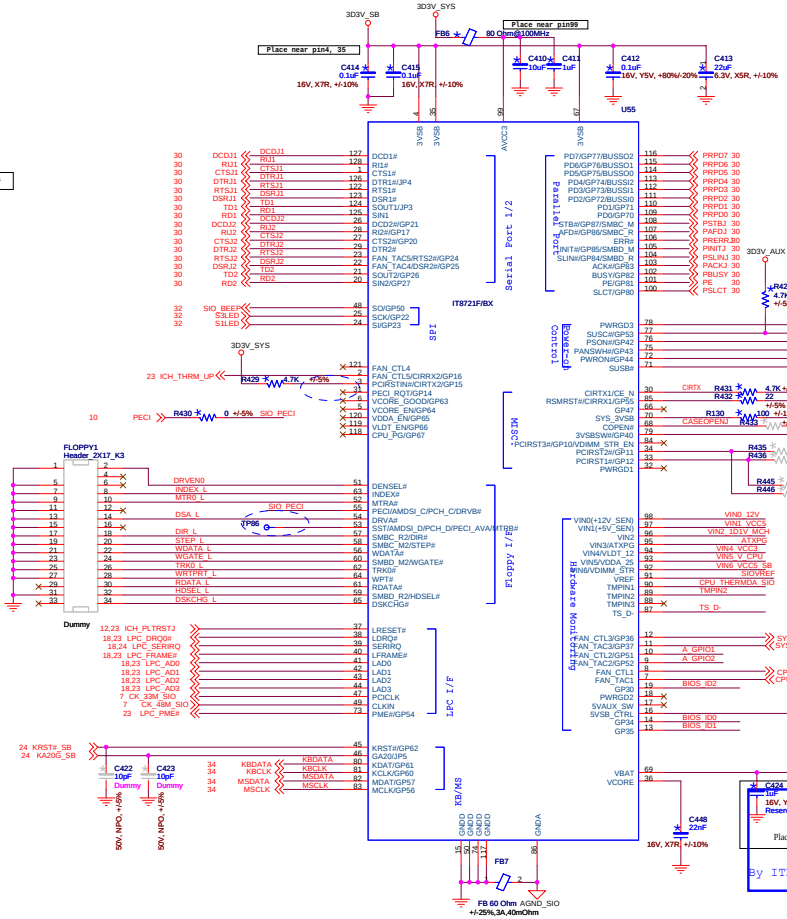
Reserved for FAN initial speed, 40h

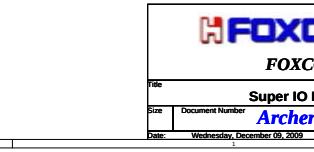


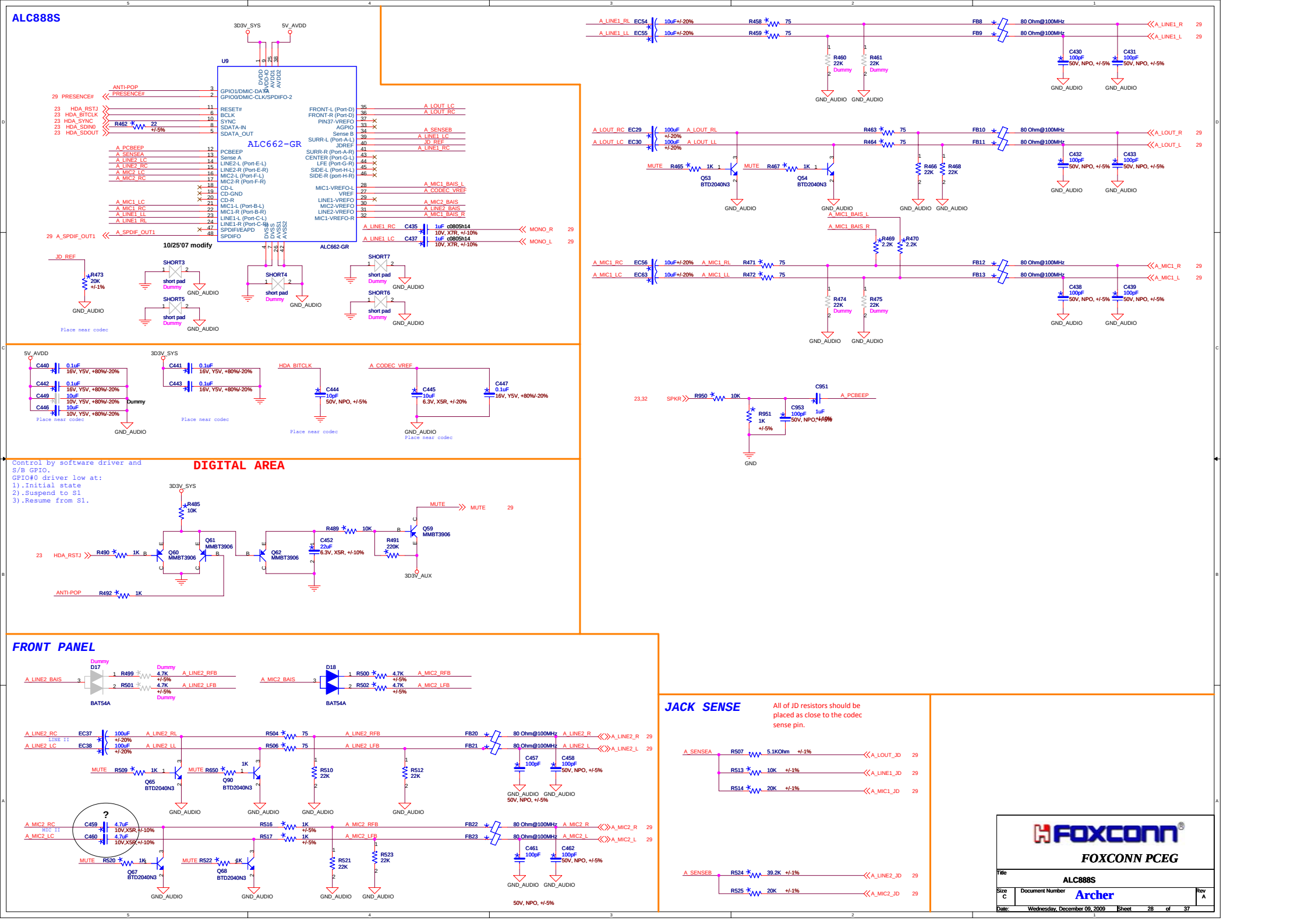











ALC888S
U9
ALC662-GR
10/25'07 modify
DIGITAL AREA
Control by software driver and S/B GPIO.
GPIO#0 driver low at:
1).Initial state
2).Suspend to S1
3).Resume from S1.
FRONT PANEL
JACK SENSE
All of JD resistors should be placed as close to the codec sense pin.
FOXCONN PCEG
Title
ALC888S
Size C
Document Number Archer
Rev A
Date: Wednesday, December 09, 2009
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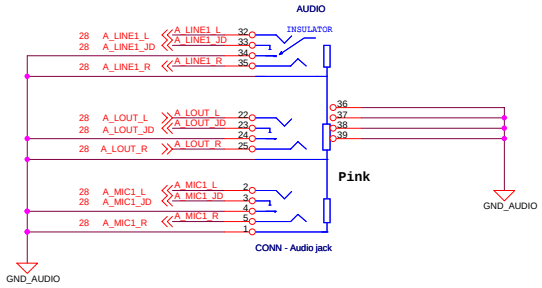
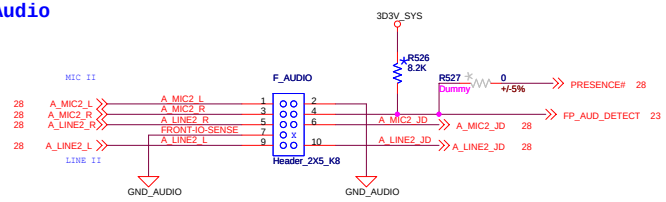
Audio CONN (3 Port)



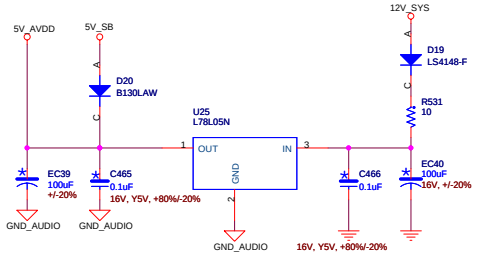
Audio Jack

Front_Audio

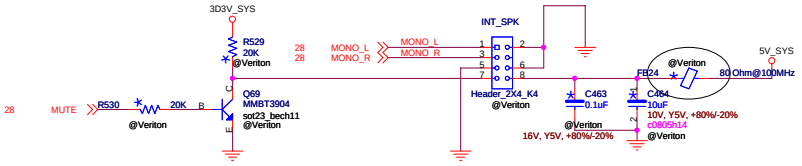


SPDIF_OUT

12V to 5V Power Regulator



Internal Speaker Header for Acer

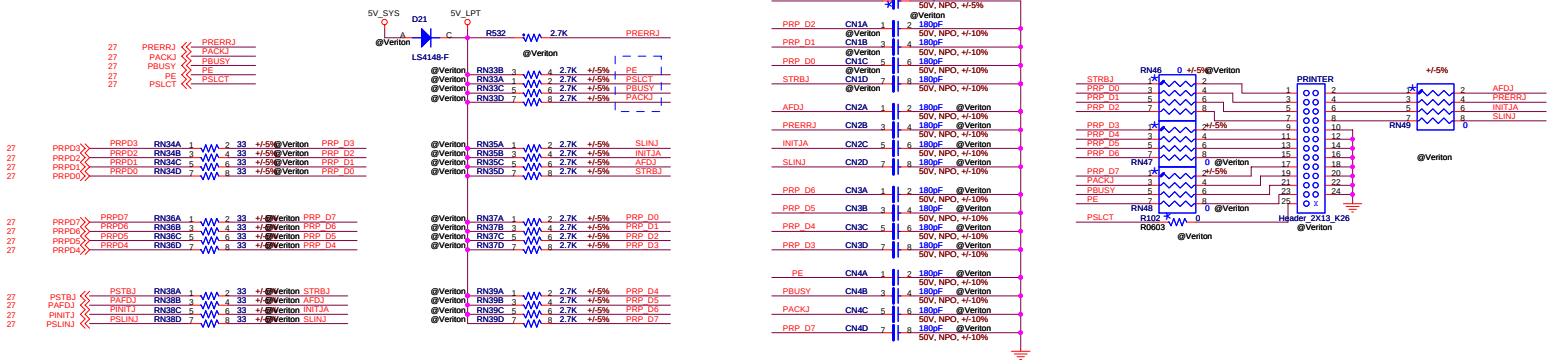


FOXCONN®

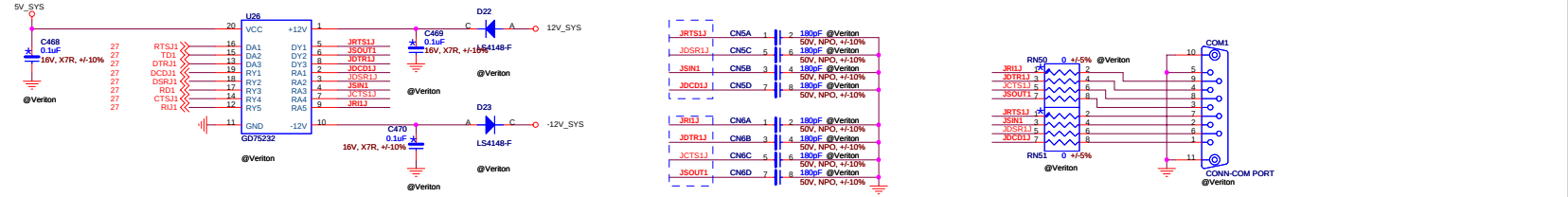
FOXCONN PCEG

Title: Audio Conn		
Size: C	Document Number: Archer	Rev: A
Date: Wednesday, December 09, 2009	Sheet 29 of 37	

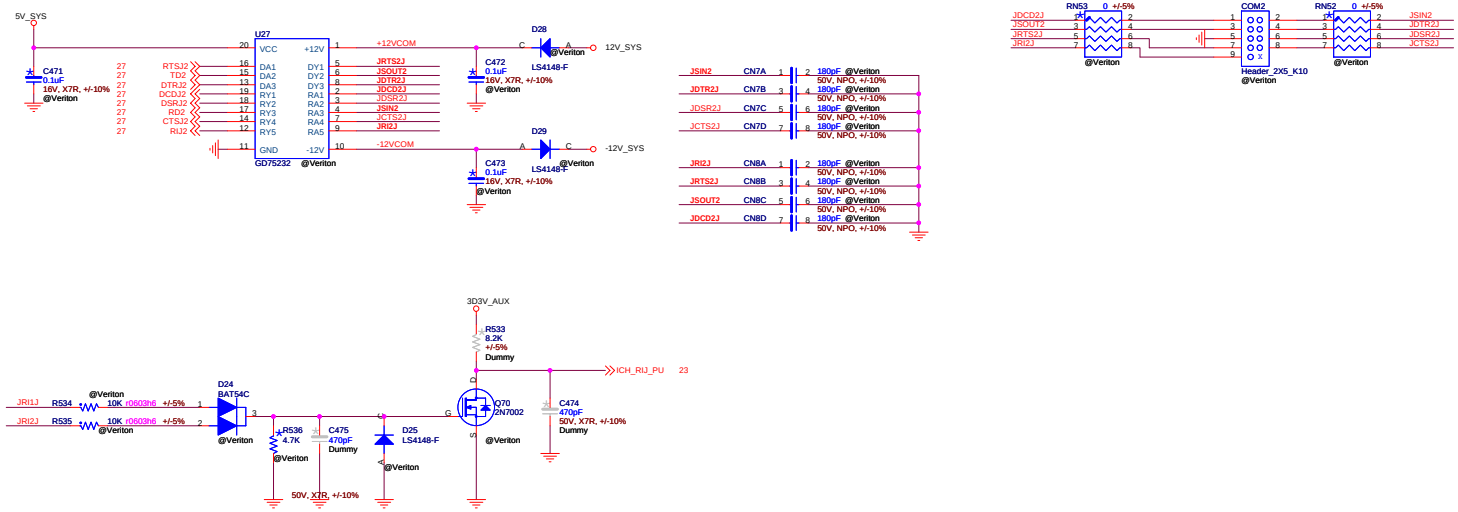
LPT CONN



Serial Port #1



Serial Port #2



FOXCONN PCEG

Title: Serial/Parallel Conn

Size: Custom | Document Number: Archer | Rev: A

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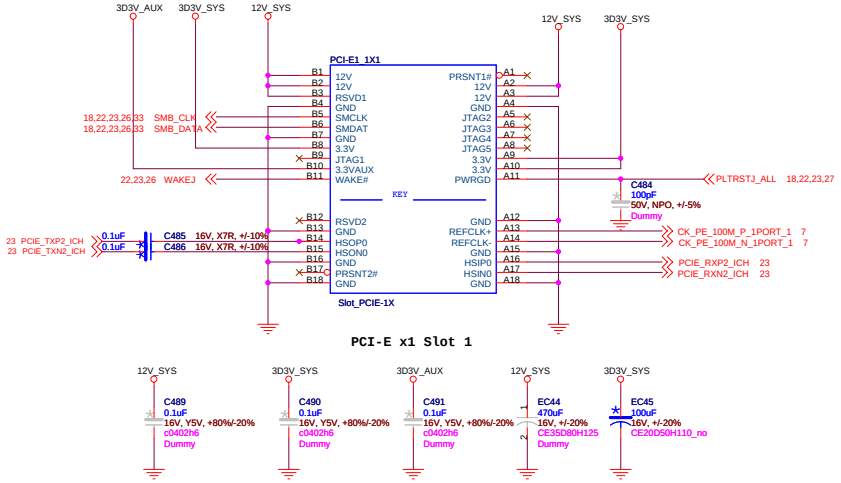
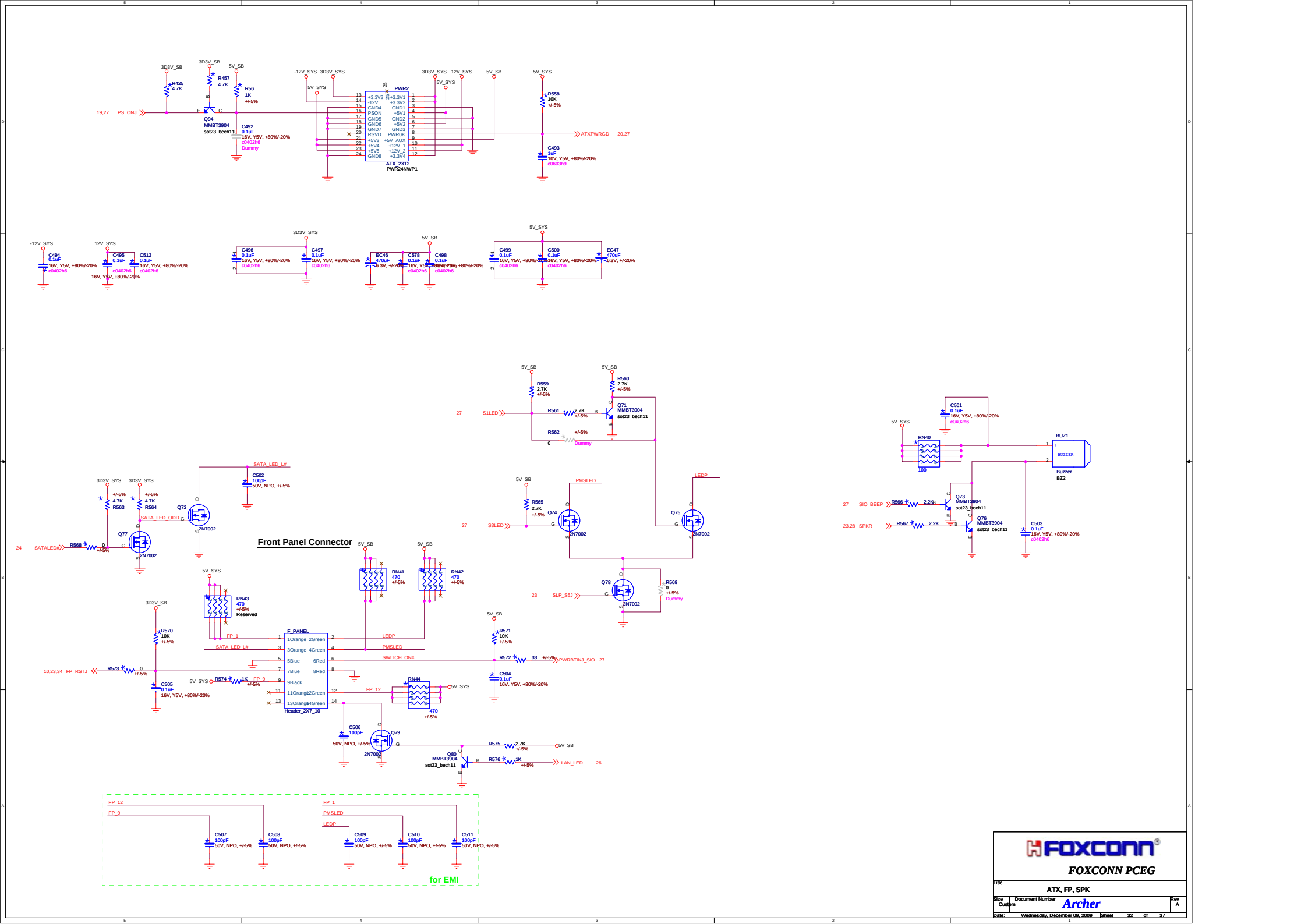
PCIE 1X Slot



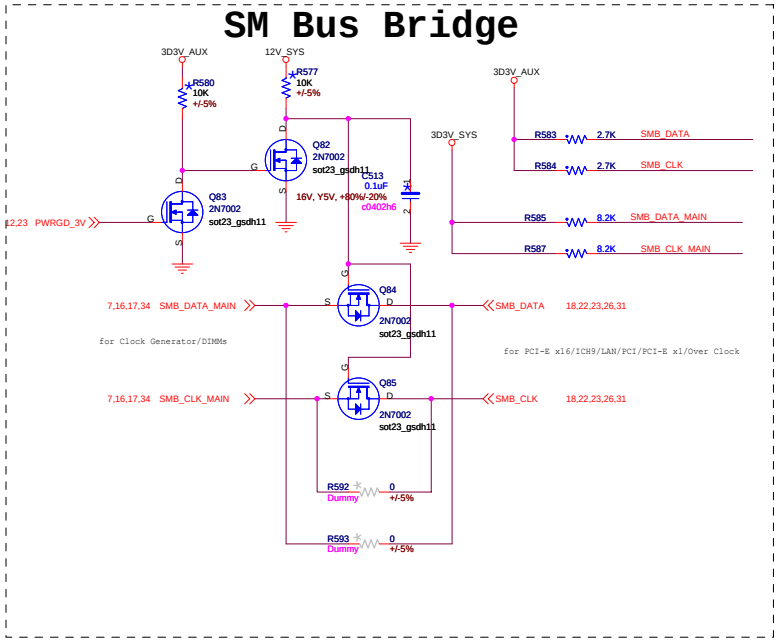
PCI-E x1 Slot 1

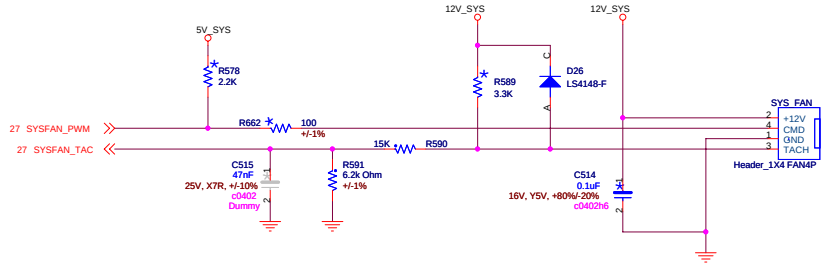
FOXCONN PCEG

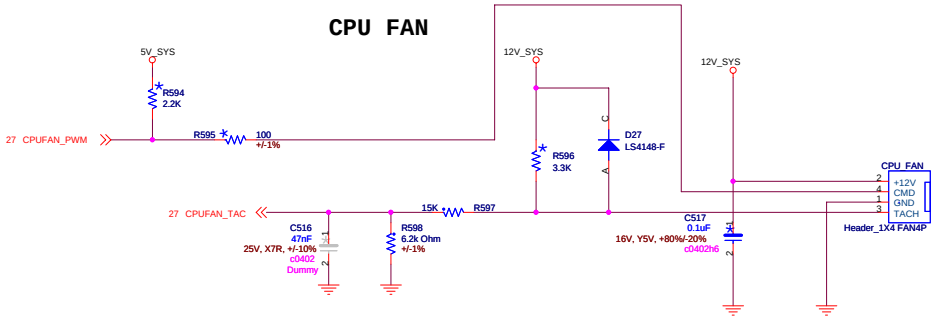
Title	PCI/PCIE 1X Slot	
Size C	Document Number Archer	Rev A
Date: Wednesday, December 09, 2009	Sheet 31 of 37	


Front Panel Connector
PWR2
ATX_2X12
PWR24NWP1
F_PANEL
Header_2X7_10
for EMI
FOXCONN PCEG
ATX, FP, SPK
Archer
Wednesday, December 09, 2009

System FAN







Peak fan current draw: 1.5A
Average fan current draw: 1.1A
Fan start-up current draw: 2.2A
Fan start-up current draw maximum duration: 1.0 second
Fan header voltage: 12V +/- 10%

4-pin FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense
pin4. Control

FOXCONN PCEG

Title: CPU / System Fan		
Size: C	Document Number: Archer	Rev: A
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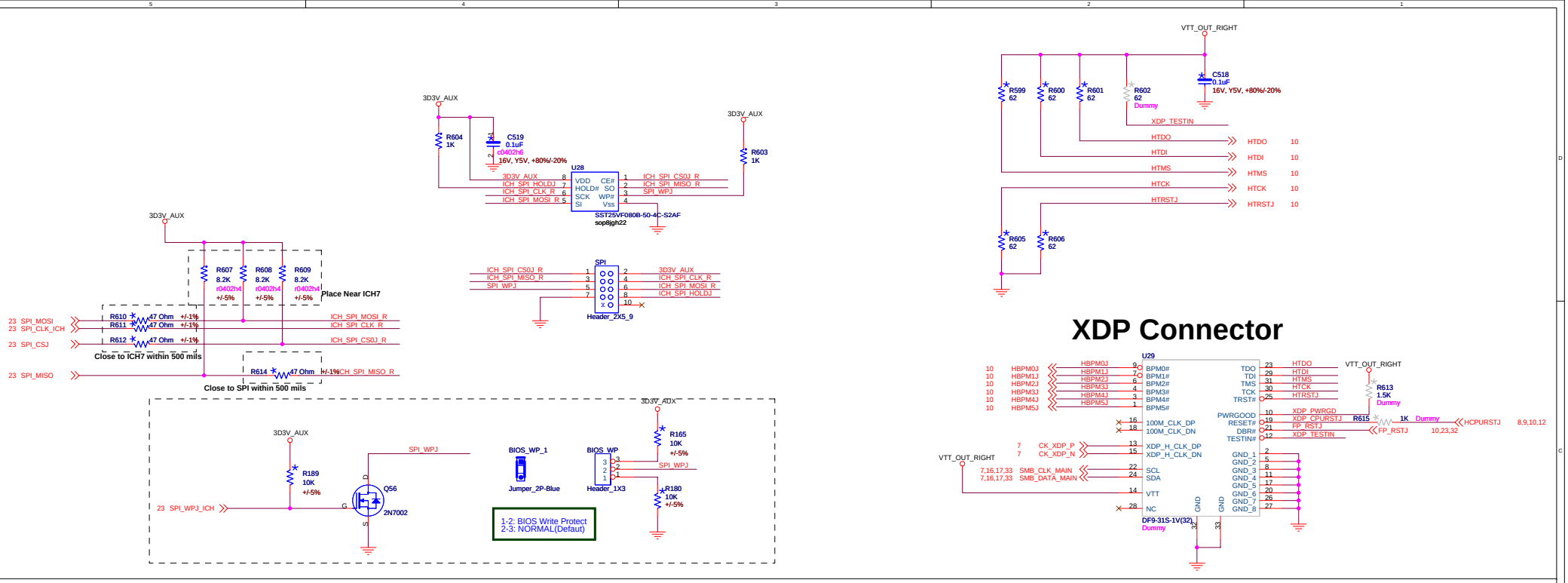
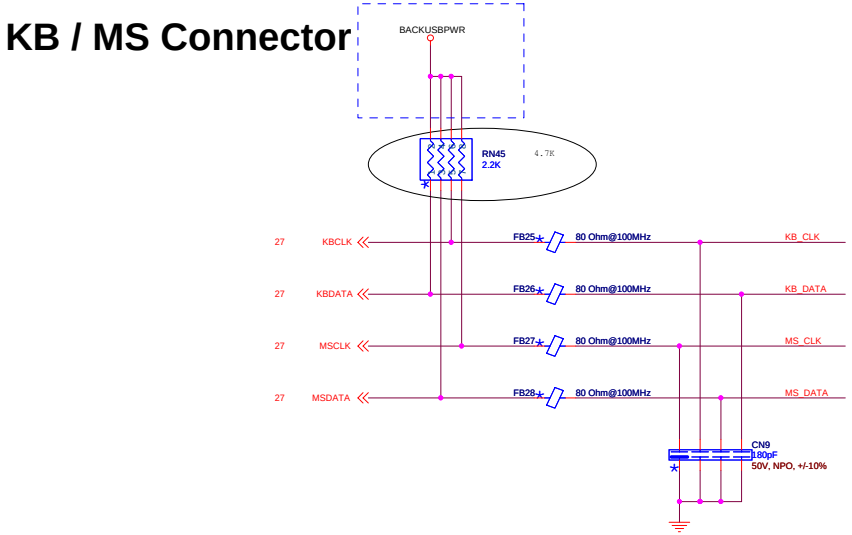
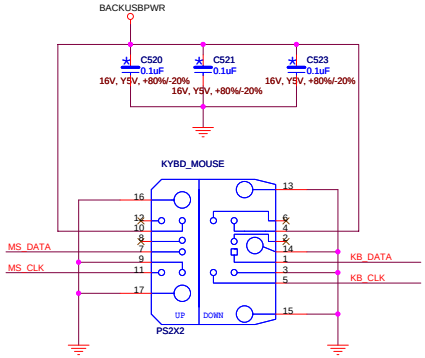


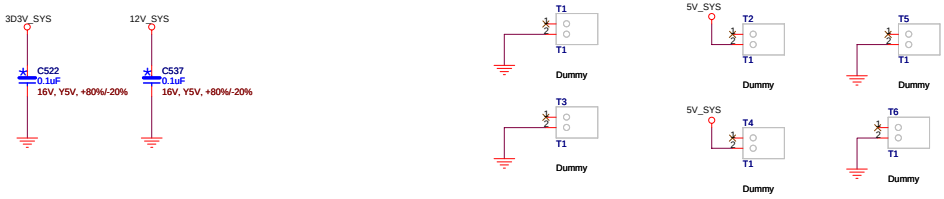
XDP Connector

KB / MS Connector





GREEN	PURPLE
Mouse	Keyboard



FOXCONN

FOXCONN PCEG

Title: KB/MS, TPM, XDP

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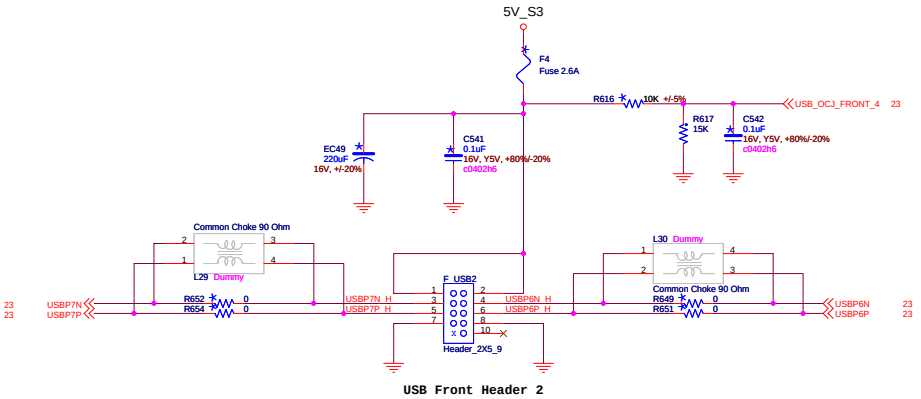
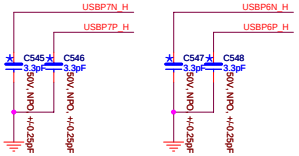
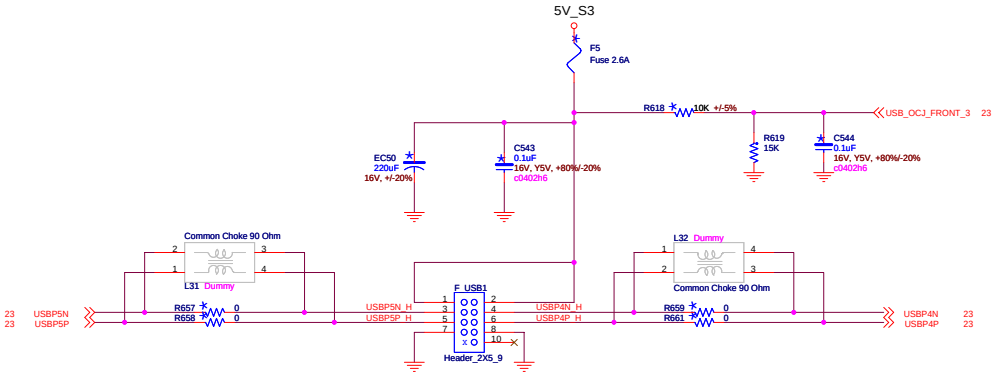
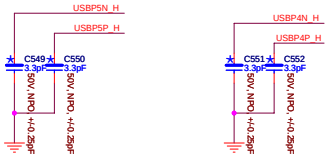


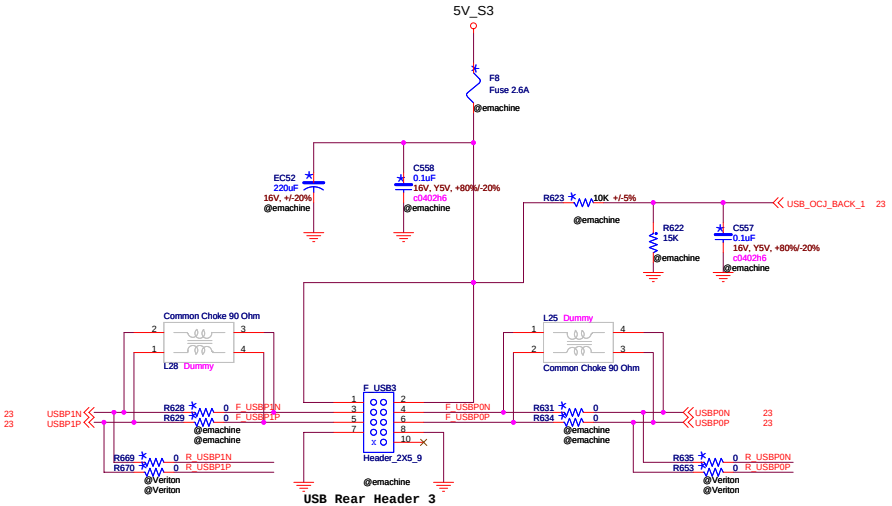
USB Front Header 2



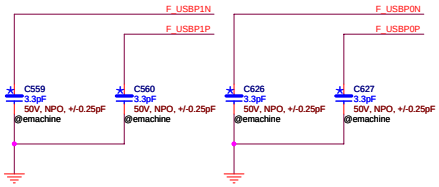


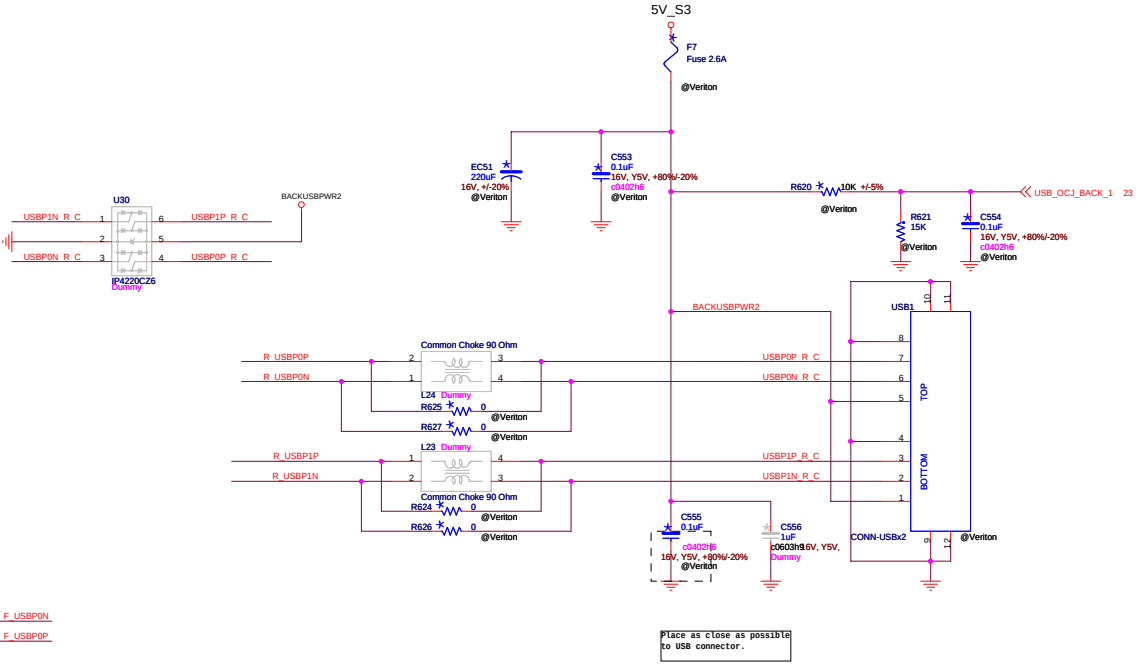
USB Front Header 1





USB Rear Header 3





Place as close as possible to USB connector.

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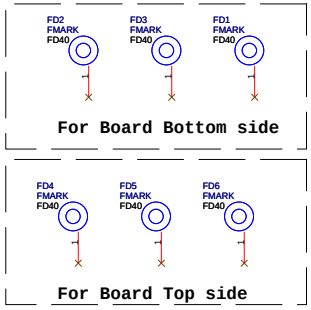
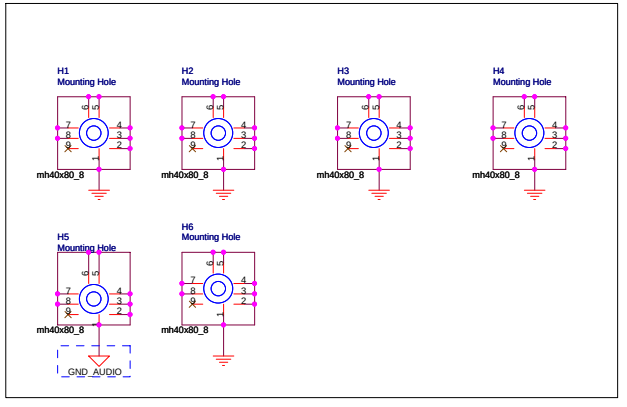
ICH7 GPIO Summary

Name	Power Well	Type	Description
GPIO0	3.3V	I/O	
GPIO1	3.3V	I/O	
GPIO2	5V	I/OD	
GPIO3	5V	I/OD	
GPIO4	5V	I/OD	
GPIO5	5V	I/OD	
GPIO6	3.3V	I/O	
GPIO7	3.3V	I/O	
GPIO8	3.3V_SB	I/O	
GPIO9	3.3V_SB	I/O	
GPIO10	3.3V_SB	I/O	
GPIO11	3.3V_SB	I/O	
GPIO12	3.3V_SB	I/O	
GPIO13	3.3V_SB	I/O	
GPIO14	3.3V_SB	I/O	
GPIO15	3.3V_SB	I/O	
GPIO16	3.3V	I/O	
GPIO17	3.3V	I/O	
GPIO18	3.3V	I/O	
GPIO19	3.3V	I/O	
GPIO20	3.3V	I/O	
GPIO21	3.3V	I/O	
GPIO22	3.3V	I/O	
GPIO23	3.3V	I/O	
GPIO24	3.3V_SB	I/O	
GPIO25	3.3V_SB	I/O	
GPIO26	3.3V_SB	I/O	
GPIO27	3.3V_SB	I/O	
GPIO28	3.3V_SB	I/O	
GPIO29	3.3V_SB	I/O	
GPIO30	3.3V_SB	I/O	
GPIO31	3.3V_SB	I/O	
GPIO32	3.3V	I/O	
GPIO33	3.3V	I/O	
GPIO34	3.3V	I/O	
GPIO35	3.3V	I/O	
GPIO36	3.3V	I/O	
GPIO37	3.3V	I/O	
GPIO38	3.3V	I/O	
GPIO39	3.3V	I/O	
GPIO40	3.3V_SB	I/O	
GPIO41	3.3V_SB	I/O	
GPIO42	3.3V_SB	I/O	
GPIO43	3.3V_SB	I/O	
GPIO44	3.3V_SB	N/A	
GPIO45	3.3V_SB	N/A	
GPIO46	3.3V_SB	N/A	
GPIO47	3.3V_SB	N/A	
GPIO48	3.3V	I/O	
GPIO49	3.3V	I/O	
GPIO50	5.5V	I/O	
GPIO51	3.3V	I/O	
GPIO52	5.5V	I/O	
GPIO53	3.3V	I/O	
GPIO54	5.5V	I/O	
GPIO55	3.3V	I/O	
GPIO56	3.3V_SB	I/O	
GPIO57	3.3V_SB	I/O	
GPIO58	3.3V_SB	I/O	
GPIO59	3.3V_SB	I/O	
GPIO60	3.3V_SB	I/O	

PCI Routing Summary

	PCI1	PCI2
INTAJ	A	E
INTBJ	B	F
INTCJ	C	G
INTDJ	D	H
INTEJ		
INTFJ		
INTGJ		
INTHJ		
REG#/GNT#	0	1
IDSEL	22	24





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Title	GPIO / IRQ / IDSEL Map	
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1.Connect MS1 Pin3 to GND.

2.Dummy L23,L24.

3.Change R214 to 1.05K
  Change R244 to 510 OHM
  Change Q17 to AOD 452

4.Change U15 PWR to 3D3V_SB

5.Change FP1 to 340600D00-GRV-G

6.U11 Rev. to B0

7.Change R231 to 10k,Q26 to 2N7002,Add C108

8.Reserved R329,Dummy Q45,D15,D16,R333,R340,R341.Change C307 to 0.01u

9.Reserved R424

10.Change EXP_TXP[7..4]_GFX Connection

11.Change DIMM2 CLK Connection

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