H61H2-CM

Rev : 1.0.

ECS CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
V.A	2010/07/29	Base on H67(H61)H2-CM MRS v1.1 2010-08-13
V.1.0	2010/10/26	1:change PWM RT8859AGQW+RT9619APS to ISL6364CRZ +ISL6612ACBZ solution ; 2:change IT8893E BX to CX; 3:change RTL8111E VB to VL version and change RTL8105E VC to VL version; 4:add Power & SI & bug solution; 5:add colay onboard TPM function;
V.1.0.	2010/12/08	1:add STP64 for METS test

1-3. Cougar Point Desktop SKUs

Feature Set		SKU Name(s)					
		Q67	Q65	B65	H67	P67	H61
PCI Express* 2.0 Ports		8	8	8	8	8	6[9]
PCI Interface		Yes	Yes	Yes	No[10]	No[10]	No[10]
USB 2.0 Ports		14	14	12[6]	14	14	10[7]
Total number of SATA ports		6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)		2[4]	1[5]	1[5]	2[4]	2[4]	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)		4	5	5	4	4	4[8]
HDMI/DVI/VGA/DisplayPort*/eDP*		Yes	Yes	Yes	Yes	No	Yes
Integrated Graphics Support with PAVP		Yes	Yes	Yes	Yes	No	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes	No
	RAID 0/1/5/10 Support	Yes	No	No	Yes	Yes	No
Intel® AT		Yes	Yes	No	No	No	No
Intel® AMT 7.0		Yes	No	No	No	No	No
Intel® Remote PC Assist Technology - Proactive		Yes	No	Yes	No	No	No
Intel® Remote PC Assist Technology - Reactive		No	No	Yes	Yes	No	No

NOTES:

1. Contact your local Intel Field Sales Representative for currently available PCH SKUs.
2. Table above shows feature differences between the PCH SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs
3. The PCH provides hardware support for AHCI functionality when enabled by appropriate system configurations and software drivers.
4. SATA 6 Gb/s support on port 0 and port 1. SATA ports 0 and 1 also support 3 Gb/s and 1.5 Gb/s.
5. SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s and 1.5 Gb/s.
6. USB ports 6 and 7 are disabled.
7. USB ports 6, 7, 12 and 13 are disabled.
8. SATA ports 2 and 3 are disabled.
9. PCIe ports 7 and 8 are disabled.
10. PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCIe-to-PCI bridge. See section 5.1.9 for more details.

NOTE:
Design by
428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev1_5
443554_443554_Cougar_Point_Chipset_Family_EDS_Rev_1.2

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Title: Cover Page

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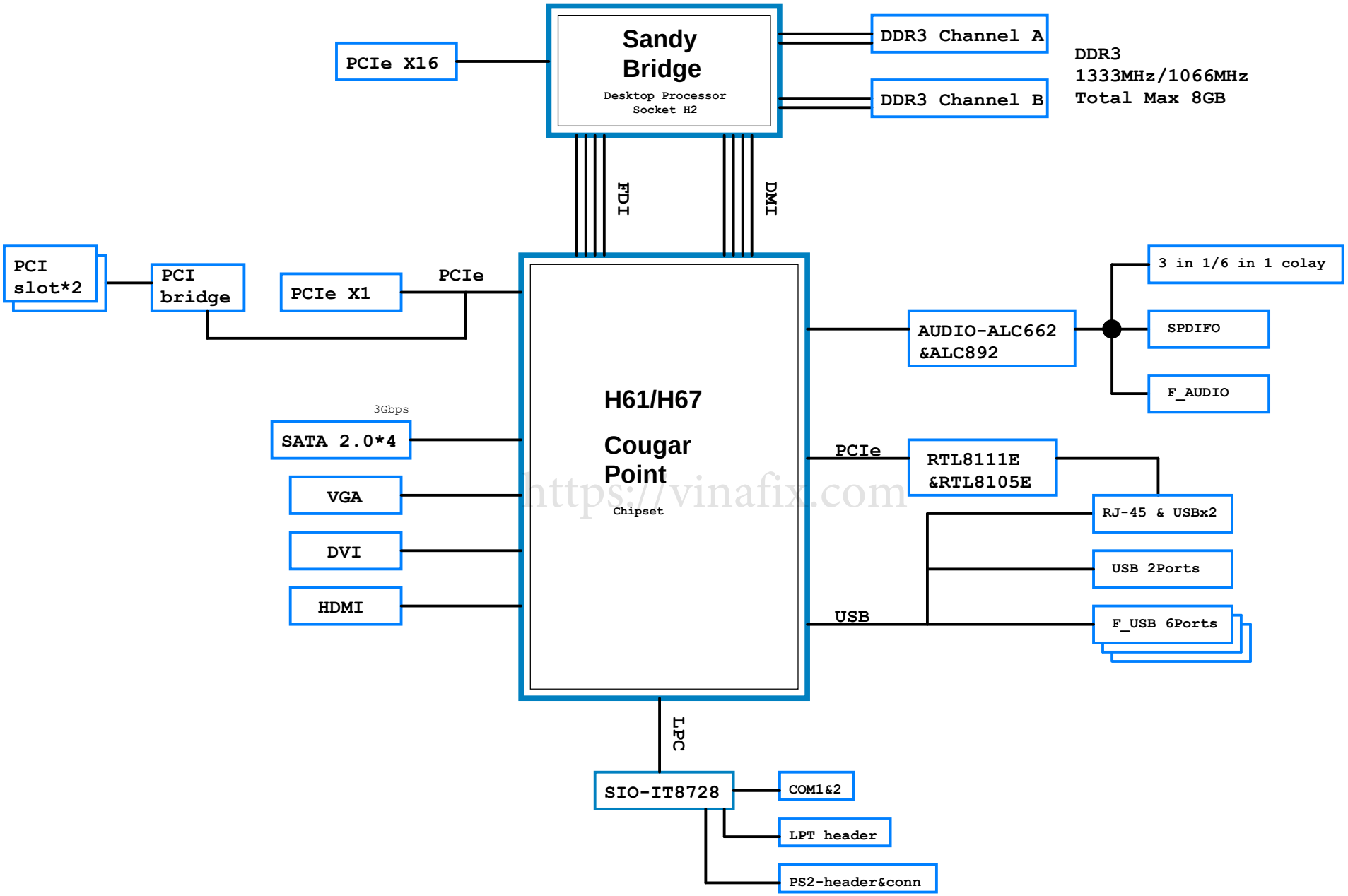

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Title: Block Diagram

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PCH-GPIO function

	Pin Name	Power Well	Usage	Default Status
	GPIO7	VCC3	SPI_WP0_L	GPI
	GPIO9	3VSB	USB_OC_L5	Native
	GPIO10	3VSB	USB_OC_L6	Native
✶	GPIO12	3VSB	GP12_BOMDET4	Native
	GPIO13	3VSB	LPC_PME_L	GPI
	GPIO14	3VSB	USB_OC_L7	Native
	GPIO16	VCC3	Reserve for TPM	GPI
	GPIO23	VCC3	F_AUD_DETECT_SB	GPI
	GPIO24	3VSB	PCH_SKTOCC_L	GPO
	GPIO40	3VSB	USB_OC_L1	Native
	GPIO41	3VSB	USB_OC_L2	Native
	GPIO42	3VSB	USB_OC_L3	Native
	GPIO43	3VSB	USB_OC_L4	Native
	GPIO49	VCC3	Reserve for TPM	GPI
✶	GPIO57	3VSB	GP57_5V_DETECT	GPI
	GPIO59	3VSB	USB_OC_L0	Native
	GPIO61	VCC3	LPCPD_L	Native
✶	GPIO72	3VSB	GPIO72_BOMDET5	Native

SIO-GPIO function

	Pin Name	Power Well	Usage	Default Status
	GP16	VCC3	SIO_BEEP	
	GP23	3VSB	Power LED	
	GP22	3VSB	Power LED	
	GP40	3VSB	+DIMM_5VDUAL_Control	
✶	GP34	VCC3	RESERVE	
✶	GP35	VCC3	RESERVE	
✶	GP36	VCC3	RESERVE	
✶	GP37	VCC3	RESERVE	

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Title: GPIO Function Map

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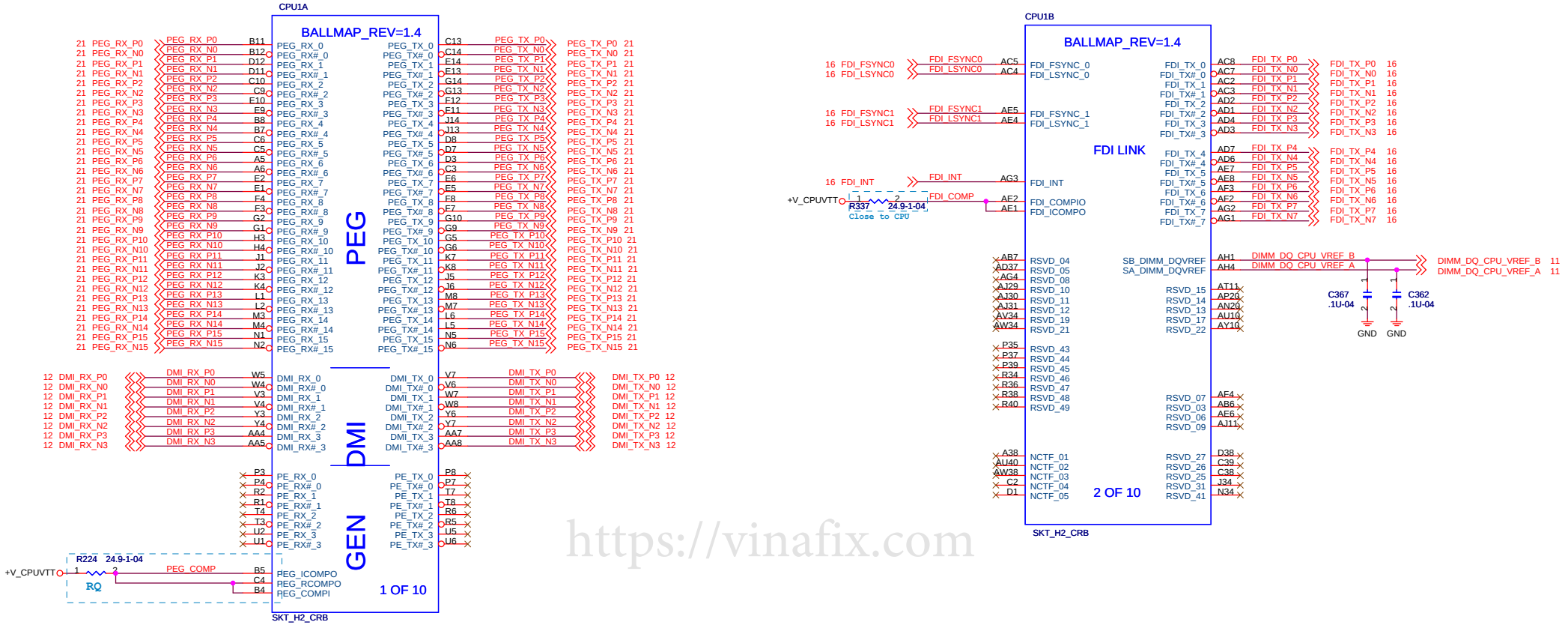

SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.

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Title	CPU - DMI/FDI/PEG		
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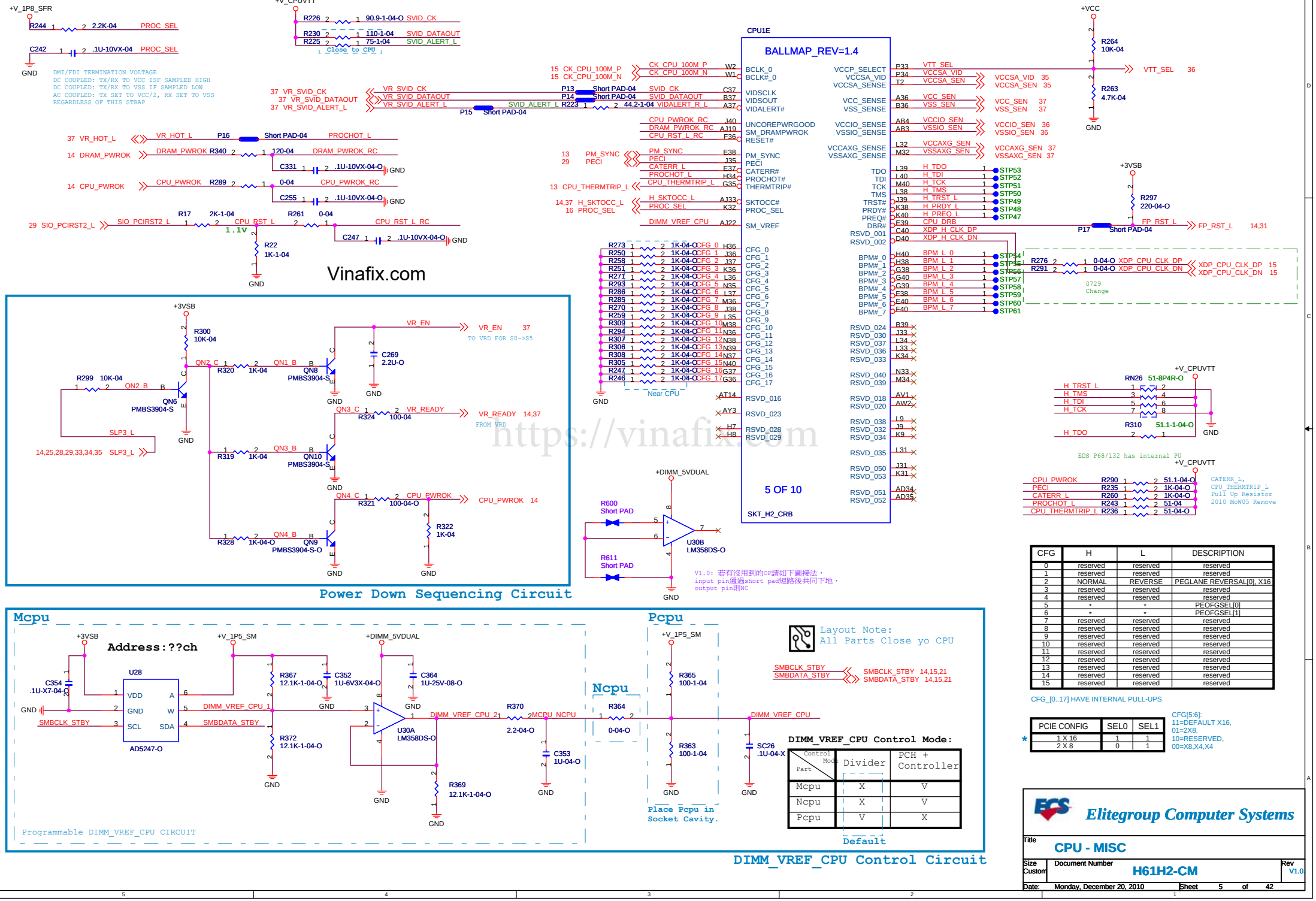
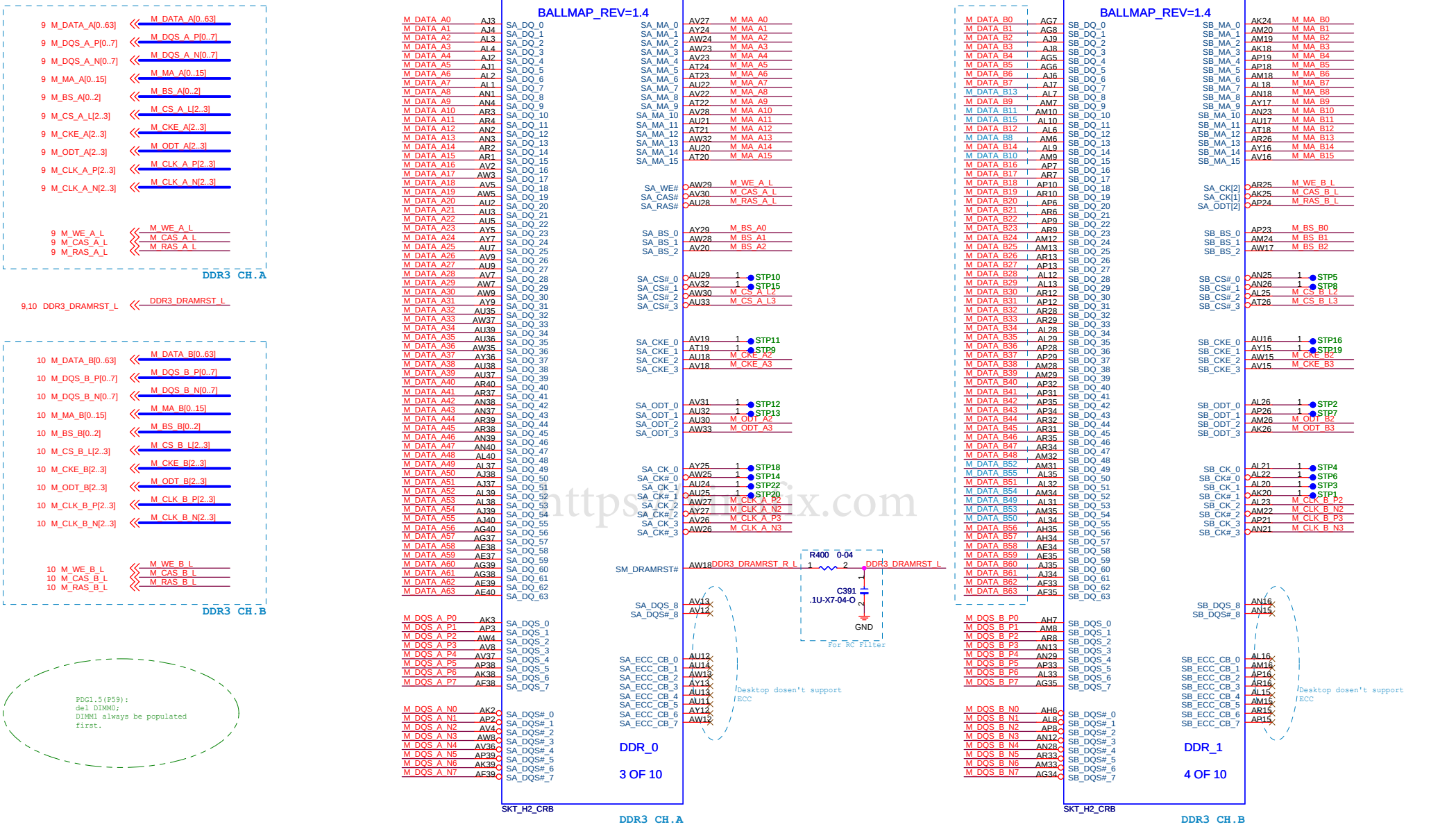


CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved



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Title	CPU - DDR3	
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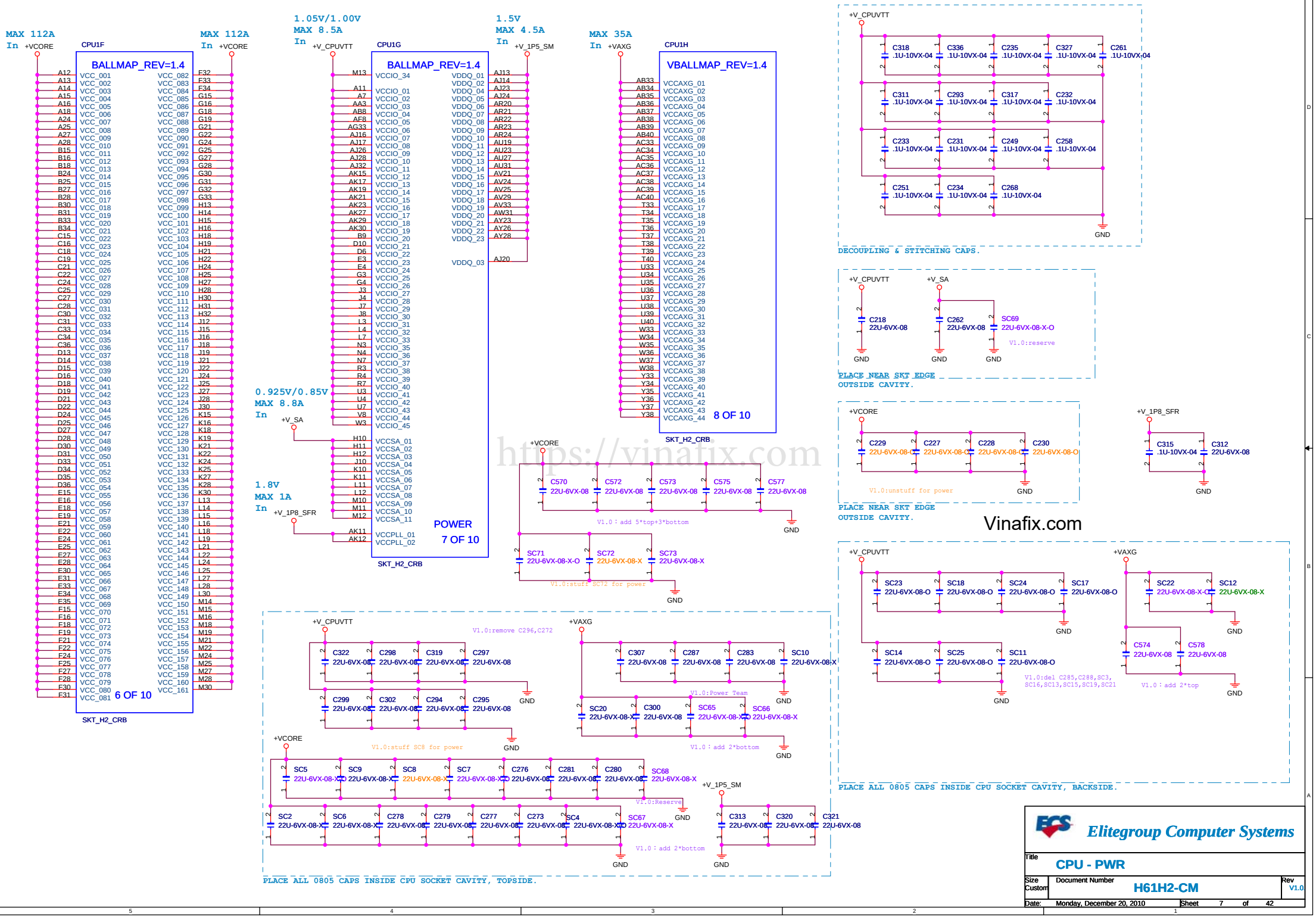
MAX 112A
In +VCORE
CPU1F
BALLMAP_REV=1.4
SKT_H2_CRB
6 OF 10
MAX 112A
In +VCORE
1.05V/1.00V
MAX 8.5A
In +V_CPUVTT
CPU1G
BALLMAP_REV=1.4
SKT_H2_CRB
1.5V
MAX 4.5A
In +V_1P5_SM
0.925V/0.85V
MAX 8.8A
In +V_SA
1.8V
MAX 1A
In +V_1P8_SFR
POWER
7 OF 10
MAX 35A
In +VAXG
CPU1H
VBALLMAP_REV=1.4
SKT_H2_CRB
8 OF 10
+V_CPUVTT
C318 .1U-10VX-04
C336 .1U-10VX-04
C235 .1U-10VX-04
C327 .1U-10VX-04
C261 .1U-10VX-04
C311 .1U-10VX-04
C293 .1U-10VX-04
C317 .1U-10VX-04
C232 .1U-10VX-04
C233 .1U-10VX-04
C231 .1U-10VX-04
C249 .1U-10VX-04
C258 .1U-10VX-04
C251 .1U-10VX-04
C234 .1U-10VX-04
C268 .1U-10VX-04
GND
DECOUPLING & STITCHING CAPS.
+V_CPUVTT
+V_SA
C218 22U-6VX-08
C262 22U-6VX-08
SC69 22U-6VX-08-X-O
V1.0:reserve
GND
PLACE NEAR SKT EDGE
OUTSIDE CAVITY.
+VCORE
C229 22U-6VX-08-O
C227 22U-6VX-08-O
C228 22U-6VX-08-O
C230 22U-6VX-08-O
V1.0:unstuff for power
GND
PLACE NEAR SKT EDGE
OUTSIDE CAVITY.
+V_1P8_SFR
C315 .1U-10VX-04
C312 22U-6VX-08
GND
+VCORE
C570 22U-6VX-08
C572 22U-6VX-08
C573 22U-6VX-08
C575 22U-6VX-08
C577 22U-6VX-08
V1.0 : add 5*top+3*bottom
SC71 22U-6VX-08-X-O
SC72 22U-6VX-08-X
SC73 22U-6VX-08-X
V1.0:stuff SC72 for power
GND
https://vinafix.com
Vinafix.com
+V_CPUVTT
+VAXG
SC23 22U-6VX-08-O
SC18 22U-6VX-08-O
SC24 22U-6VX-08-O
SC17 22U-6VX-08-O
SC22 22U-6VX-08-X-O
SC12 22U-6VX-08-X
SC14 22U-6VX-08-O
SC25 22U-6VX-08-O
SC11 22U-6VX-08-O
C574 22U-6VX-08
C578 22U-6VX-08
V1.0:del C285,C288,SC3,
SC16,SC13,SC15,SC19,SC21
V1.0 : add 2*top
GND
PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY, BACKSIDE.
+V_CPUVTT
V1.0:remove C296,C272
C322 22U-6VX-08
C298 22U-6VX-08
C319 22U-6VX-08
C297 22U-6VX-08
C299 22U-6VX-08
C302 22U-6VX-08
C294 22U-6VX-08
C295 22U-6VX-08
GND
+VAXG
C307 22U-6VX-08
C287 22U-6VX-08
C283 22U-6VX-08
SC10 22U-6VX-08-X
V1.0:Power Team
SC20 22U-6VX-08-X
C300 22U-6VX-08
SC65 22U-6VX-08-X
SC66 22U-6VX-08-X
V1.0 : add 2*bottom
GND
+VCORE
V1.0:stuff SC8 for power
SC5 22U-6VX-08-X
SC9 22U-6VX-08-X
SC8 22U-6VX-08-X
SC7 22U-6VX-08-X
C276 22U-6VX-08
C281 22U-6VX-08
C280 22U-6VX-08
SC68 22U-6VX-08-X
V1.0:Reserve
SC2 22U-6VX-08-X
SC6 22U-6VX-08-X
C278 22U-6VX-08
C279 22U-6VX-08
C277 22U-6VX-08
C273 22U-6VX-08
SC4 22U-6VX-08-X
SC67 22U-6VX-08-X
V1.0 : add 2*bottom
+V_1P5_SM
C313 22U-6VX-08
C320 22U-6VX-08
C321 22U-6VX-08
GND
PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY, TOPSIDE.
Elitegroup Computer Systems
Title
CPU - PWR
Size Custom
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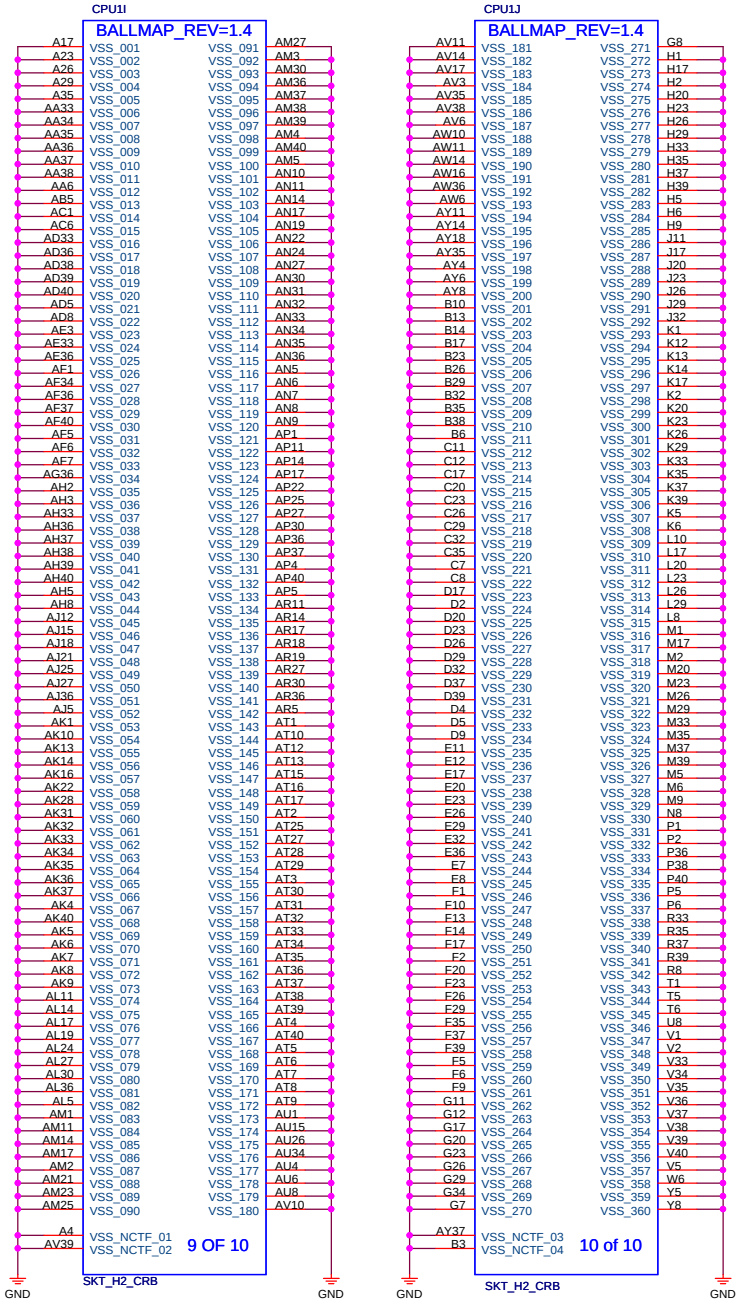

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Title: CPU - GND			
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CHANNEL A DIMM

CH.A	SA1	SA0
DIMM0	L	L
DIMM1	L	H

M_DQS_A_P[0..7] M_DQS_A_P[0..7] 6
M_DQS_A_N[0..7] M_DQS_A_N[0..7] 6

The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.

M_DATA_A[0..63] M_DATA_A[0..63] 6

Desktop dosen't support ECC

DDR3-240P DIMM1

+V_SM_VTT
0.75V
MAX 1A

+V_1P5_SM
1.5V
MAX 15A
S3 1.0A

+VCC3
11 DIMM_VREF_CA_A
11 DIMM_VREF_DQ_A
10,15,19 SMBCLK_MAIN
10,15,19 SMBDATA_MAIN

6 M_ODT_A[2..3] M_ODT_A[2..3]
6 M_CS_A_L[2..3] M_CS_A_L[2..3]
6 M_CKE_A[2..3] M_CKE_A[2..3]
6 M_CLK_A_P[2..3] M_CLK_A_P[2..3]
6 M_CLK_A_N[2..3] M_CLK_A_N[2..3]

6 M_BS_A[0..2] M_BS_A[0..2]

M_MA_A[0..15] M_MA_A[0..15] 6

M_WE_A_L M_WE_A_L 6
M_RAS_A_L M_RAS_A_L 6
M_CAS_A_L M_CAS_A_L 6
DDR3_DRAMRST_L DDR3_DRAMRST_L 6,10

M_CLK_A_P2
M_CLK_A_N2
M_CLK_A_P3
M_CLK_A_N3

Design note:
DIMM: CH A BANK 2
CH A SMB ADDRESS 001
CH A SPD READ/WR: 0*A3, 0*A2
SPD=SERIAL PRESENCE DETECT

+V_1P5_SM
V1.0:unstuff
C417 1U-10VX-04
C415 1U-10VX-04
C421 1U-10VX-04
C386 1U-10VX-04
C389 1U-10VX-04
+V_SM_VTT
C368 4.7U-25VX5-08
C372 .1U-04
CH A V_SM_VTT DECOUPLING CAPS

+V_1P5_SM
V1.0:unstuff
C454 22U-6VX-08
C457 22U-6VX-08
C424 22U-6VX-08
C414 22U-6VX-08
C446 22U-6VX-08
Between CHA&CHB

+VCC3
C445 .1U-04-O
C404 .1U-04-O
PLACE BETWEEN CHA &CHB.
DO NOT PUNCH VIA.

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Title	DDR3 - CHA DIMM1		
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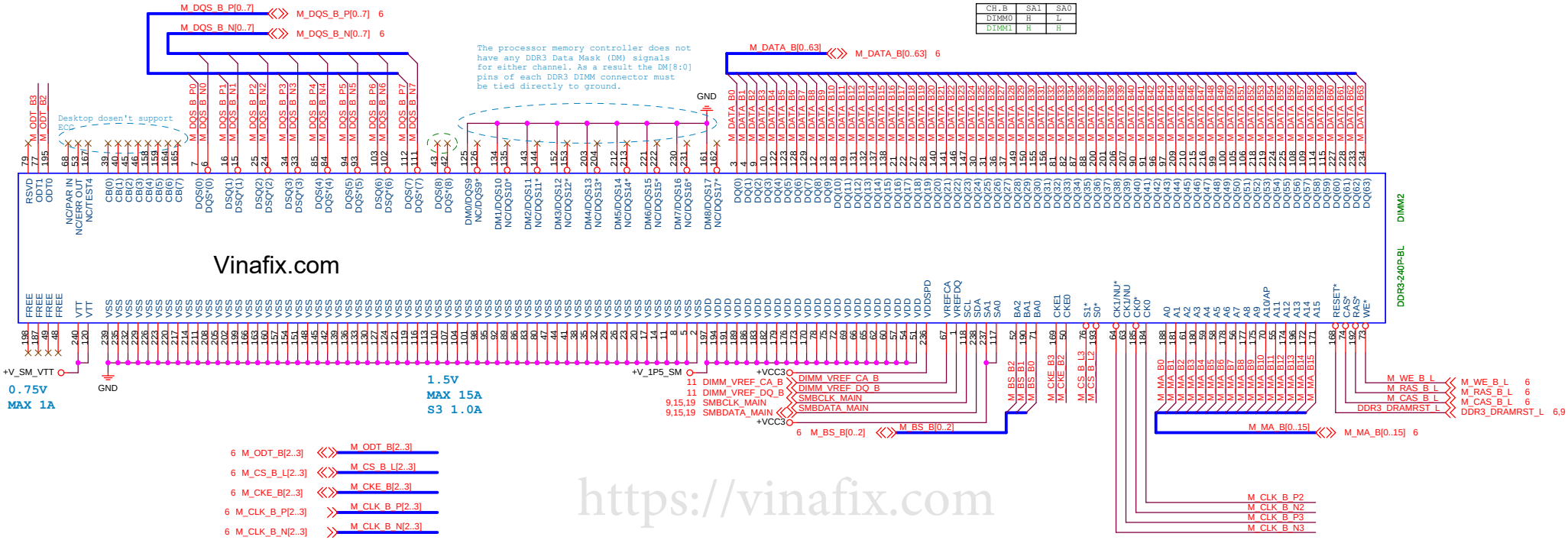
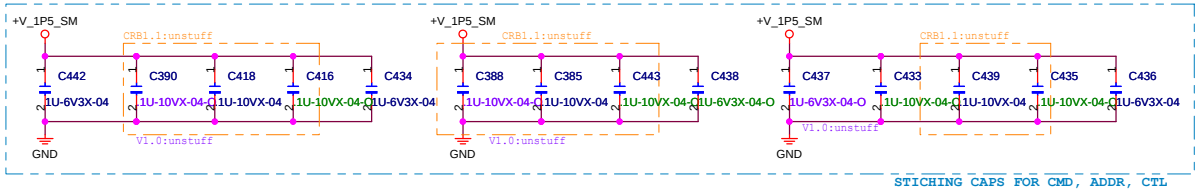
CHANNEL B DIMMs

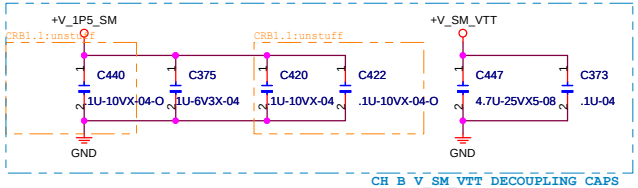


CH.B	SA1	SA0
DIMM0	H	L
DIMM1	H	H

6 M_ODT_B[2..3] M_ODT_B[2..3]
6 M_CS_B_L[2..3] M_CS_B_L[2..3]
6 M_CKE_B[2..3] M_CKE_B[2..3]
6 M_CLK_B_P[2..3] M_CLK_B_P[2..3]
6 M_CLK_B_N[2..3] M_CLK_B_N[2..3]

Design note:
DIMM: CH B BANK 2
CH B SMB ADDRESS 011
CH B SPD READ/WR: 0*A7, 0*A6
SPD=SERIAL PRESENCE DETECT





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Title: DDR3 - CHB DIMM1

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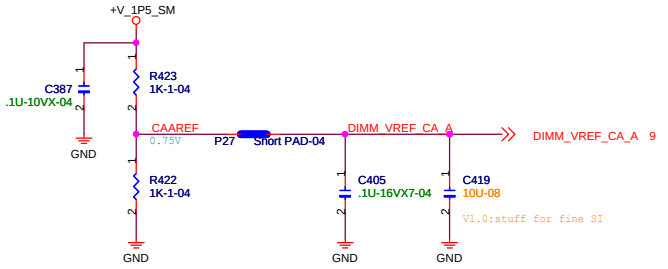
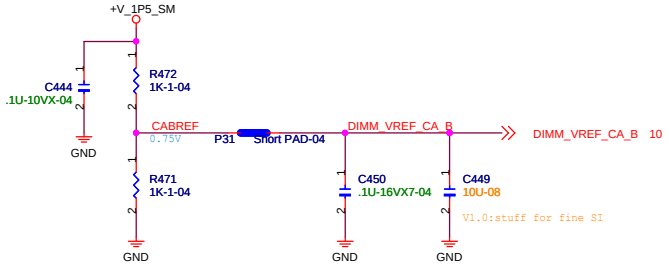
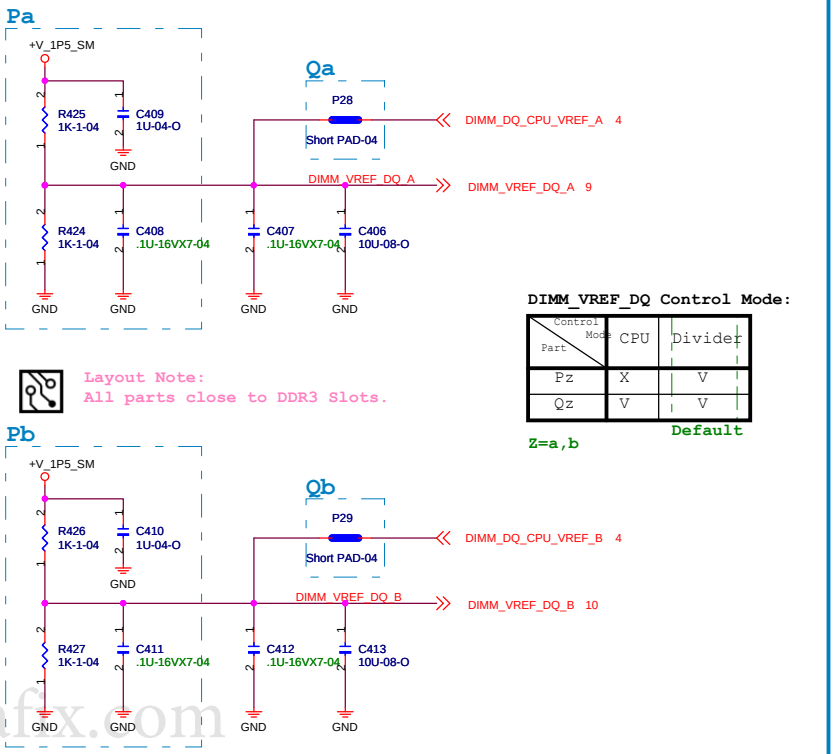




DIMM_VREF_CA Circuit



DIMM_VREF_DQ Control Mode:

Part \ Control Mode	CPU	Divider
Pz	X	V
Qz	V	V

Default

Z=a,b

DIMM_VREF_DQ Control Circuit

0729
REMOVE Programmable VREFDQ circuit For PDG 1.5 update

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Title: DDR3 - VREF		
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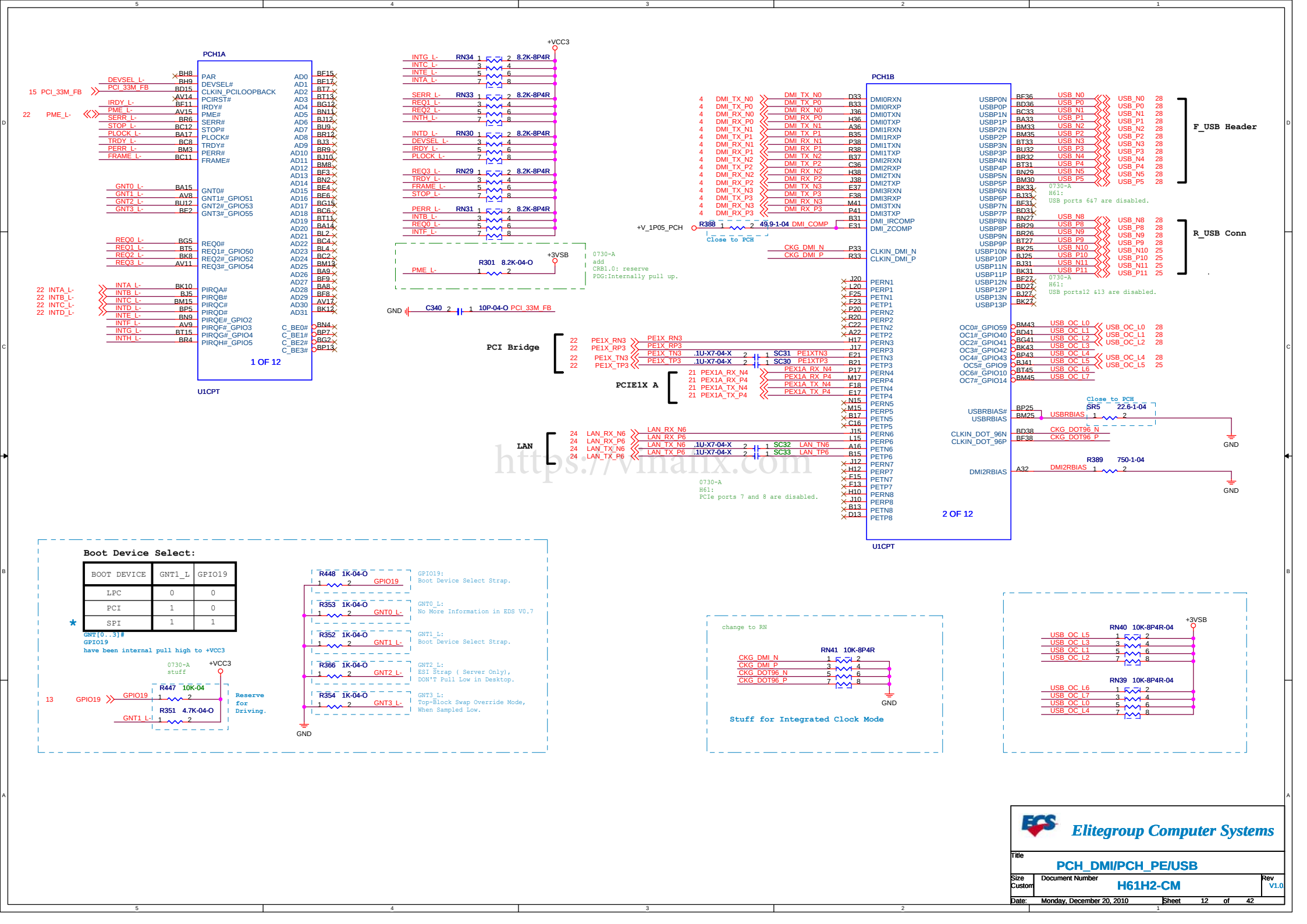
PCH1A
1 OF 12
U1CPT
PCH1B
2 OF 12
PCI Bridge
PCIE1X A
LAN
F_USB Header
R_USB Conn
Boot Device Select:
Stuff for Integrated Clock Mode
Elitegroup Computer Systems
PCH_DMI/PCH_PE/USB
H61H2-CM
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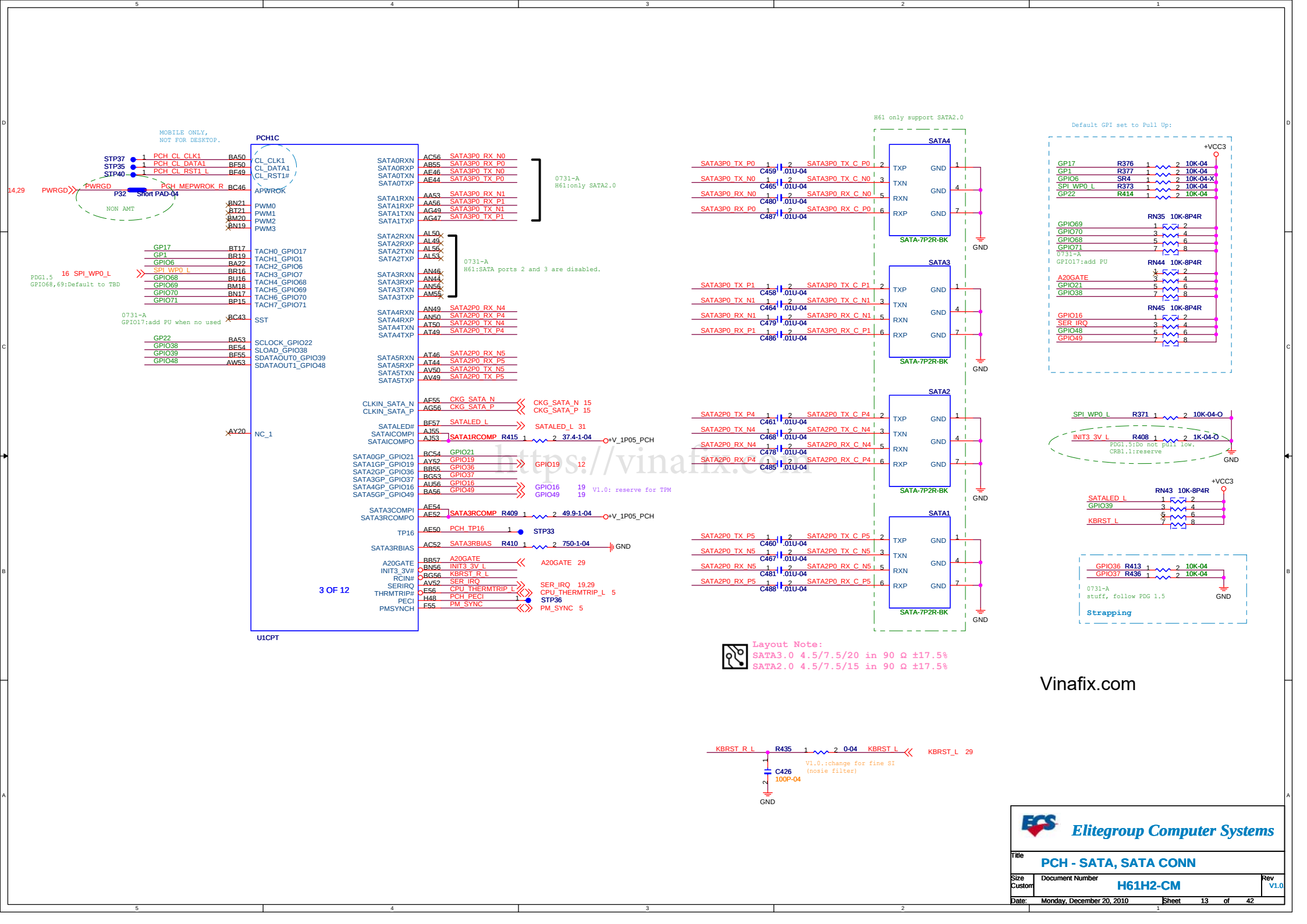
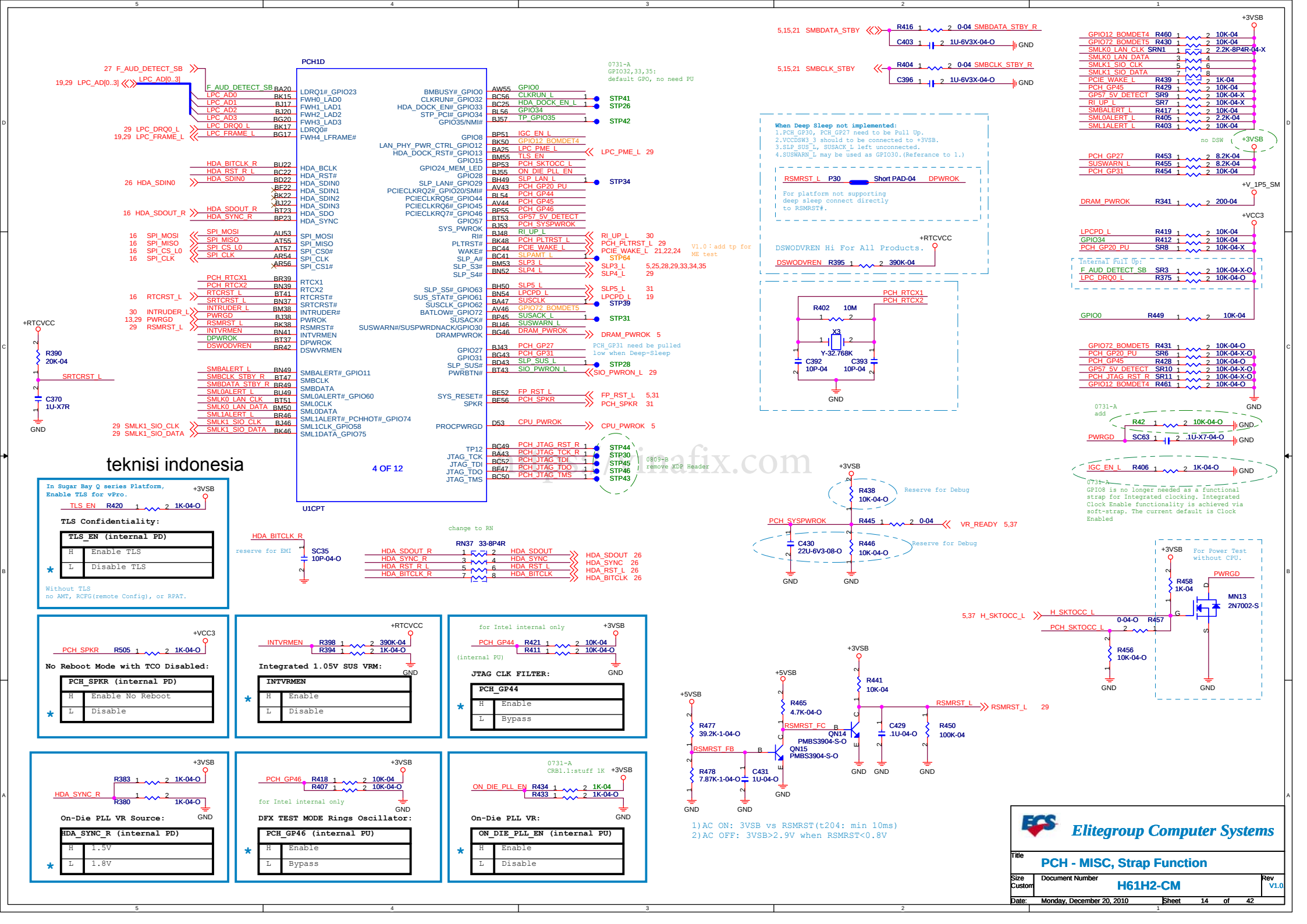

MOBILE ONLY,
NOT FOR DESKTOP.
PCH1C
STP37 1 PCH_CL_CLK1 BA50 CL_CLK1
STP35 1 PCH_CL_DATA1 BB50 CL_DATA1
STP40 1 PCH_CL_RST1_L BF49 CL_RST1#
14,29 PWRGD PWRGD PCH_MEPWROK_R BC46 APWROK
P32 Short PAD-04
NON AMT
BN21 PWM0
BT21 PWM1
BM20 PWM2
BN19 PWM3
GP17 BT17 TACH0_GPIO17
GP1 BR19 TACH1_GPIO1
GPIO6 BA22 TACH2_GPIO6
PDG1.5 16 SPI_WP0_L SPI_WP0_L BR16 TACH3_GPIO7
GPIO68,69:Default to TBD
GPIO68 BU16 TACH4_GPIO68
GPIO69 BM18 TACH5_GPIO69
GPIO70 BN17 TACH6_GPIO70
GPIO71 BP15 TACH7_GPIO71
0731-A
GPIO17:add PU when no used
BC43 SST
GP22 BA53 SCLOCK_GPIO22
GPIO38 BE54 SLOAD_GPIO38
GPIO39 BF55 SDATAOUT0_GPIO39
GPIO48 AW53 SDATAOUT1_GPIO48
AY20 NC_1
SATA0RXN AC56 SATA3P0_RX_N0
SATA0RXP AB55 SATA3P0_RX_P0
SATA0TXN AE46 SATA3P0_TX_N0
SATA0TXP AE44 SATA3P0_TX_P0
0731-A
H61:only SATA2.0
SATA1RXN AA53 SATA3P0_RX_N1
SATA1RXP AA56 SATA3P0_RX_P1
SATA1TXN AG49 SATA3P0_TX_N1
SATA1TXP AG47 SATA3P0_TX_P1
SATA2RXN AL50
SATA2RXP AL49
SATA2TXN AL56
SATA2TXP AL53
0731-A
H61:SATA ports 2 and 3 are disabled.
SATA3RXN AN46
SATA3RXP AN44
SATA3TXN AN56
SATA3TXP AM55
SATA4RXN AN49 SATA2P0_RX_N4
SATA4RXP AN50 SATA2P0_RX_P4
SATA4TXN AT50 SATA2P0_TX_N4
SATA4TXP AT49 SATA2P0_TX_P4
SATA5RXN AT46 SATA2P0_RX_N5
SATA5RXP AT44 SATA2P0_RX_P5
SATA5TXN AV50 SATA2P0_TX_N5
SATA5TXP AV49 SATA2P0_TX_P5
CLKIN_SATA_N AE55 CKG_SATA_N CKG_SATA_N 15
CLKIN_SATA_P AG56 CKG_SATA_P CKG_SATA_P 15
SATALED# BF57 SATALED_L SATALED_L 31
SATAICOMPI AJ55
SATAICOMPO AJ53 SATA1RCOMP R415 1 2 37.4-1-04 +V_1P05_PCH
SATA0GP_GPIO21 BC54 GPIO21
SATA1GP_GPIO19 AY52 GPIO19 GPIO19 12
SATA2GP_GPIO36 BB55 GPIO36
SATA3GP_GPIO37 BG53 GPIO37
SATA4GP_GPIO16 AU56 GPIO16 GPIO16 19
SATA5GP_GPIO49 BA56 GPIO49 GPIO49 19
V1.0: reserve for TPM
SATA3COMPI AE54
SATA3RCOMPO AE52 SATA3RCOMP R409 1 2 49.9-1-04 +V_1P05_PCH
TP16 AE50 PCH_TP16 1 STP33
SATA3RBIAS AC52 SATA3RBIAS R410 1 2 750-1-04 GND
A20GATE BB57 A20GATE A20GATE 29
INIT3_3V# BN56 INIT3_3V_L
RCIN# BG56 KBRST_R_L
SERIRQ AV52 SER_IRQ SER_IRQ 19,29
THRMTRIP# E56 CPU_THERMTRIP_L CPU_THERMTRIP_L 5
PECI H48 PCH_PECI 1 STP36
PMSYNCH E55 PM_SYNC PM_SYNC 5
3 OF 12
U1CPT
H61 only support SATA2.0
SATA4
SATA3P0_TX_P0 C459 .01U-04 SATA3P0_TX_C_P0
SATA3P0_TX_N0 C465 .01U-04 SATA3P0_TX_C_N0
SATA3P0_RX_N0 C480 .01U-04 SATA3P0_RX_C_N0
SATA3P0_RX_P0 C487 .01U-04 SATA3P0_RX_C_P0
TXP TXN RXN RXP GND
SATA-7P2R-BK
SATA3
SATA3P0_TX_P1 C458 .01U-04 SATA3P0_TX_C_P1
SATA3P0_TX_N1 C464 .01U-04 SATA3P0_TX_C_N1
SATA3P0_RX_N1 C479 .01U-04 SATA3P0_RX_C_N1
SATA3P0_RX_P1 C486 .01U-04 SATA3P0_RX_C_P1
SATA-7P2R-BK
SATA2
SATA2P0_TX_P4 C461 .01U-04 SATA2P0_TX_C_P4
SATA2P0_TX_N4 C468 .01U-04 SATA2P0_TX_C_N4
SATA2P0_RX_N4 C478 .01U-04 SATA2P0_RX_C_N4
SATA2P0_RX_P4 C485 .01U-04 SATA2P0_RX_C_P4
SATA-7P2R-BK
SATA1
SATA2P0_TX_P5 C460 .01U-04 SATA2P0_TX_C_P5
SATA2P0_TX_N5 C467 .01U-04 SATA2P0_TX_C_N5
SATA2P0_RX_N5 C481 .01U-04 SATA2P0_RX_C_N5
SATA2P0_RX_P5 C488 .01U-04 SATA2P0_RX_C_P5
SATA-7P2R-BK
Layout Note:
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%
KBRST_R_L R435 1 2 0-04 KBRST_L KBRST_L 29
V1.0.:change for fine SI
(nosie filter)
C426 100P-04
GND
Default GPI set to Pull Up:
+VCC3
GP17 R376 10K-04
GP1 R377 10K-04
GPIO6 SR4 10K-04-X
SPI_WP0_L R373 10K-04
GP22 R414 10K-04
RN35 10K-8P4R
GPIO69
GPIO70
GPIO68
GPIO71
0731-A
GPIO17:add PU
RN44 10K-8P4R
A20GATE
GPIO21
GPIO38
RN45 10K-8P4R
GPIO16
SER_IRQ
GPIO48
GPIO49
SPI_WP0_L R371 10K-04-O
INIT3_3V_L R408 1K-04-O
PDG1.5:Do not pull low.
CRB1.1:reserve
GND
+VCC3
RN43 10K-8P4R
SATALED_L
GPIO39
KBRST_L
GPIO36 R413 10K-04
GPIO37 R436 10K-04
0731-A
stuff, follow PDG 1.5
GND
Strapping
Vinafix.com
https://vinafix.com
Elitegroup Computer Systems
Title
PCH - SATA, SATA CONN
Size Custom
Document Number
H61H2-CM
Rev V1.0
Date: Monday, December 20, 2010
Sheet 13 of 42


PCH1D
U1CPT
4 OF 12
F_AUD_DETECT_SB
LPC_AD[0..3]
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_DRQ0_L
LPC_FRAME_L
HDA_BITCLK_R
HDA_RST_R_L
HDA_SDIN0
HDA_SDOUT_R
HDA_SYNC_R
SPI_MOSI
SPI_MISO
SPI_CS_L0
SPI_CLK
PCH_RTCX1
PCH_RTCX2
RTCRST_L
SRTCRST_L
INTRUDER_L
PWRGD
RSMRST_L
INTVRMEN
DPWROK
DSWODVREN
SMBALERT_L
SMBCLK_STBY_R
SMBDATA_STBY_R
SML0ALERT_L
SMLK0_LAN_CLK
SMLK0_LAN_DATA
SML1ALERT_L
SMLK1_SIO_CLK
SMLK1_SIO_DATA
SMBDATA_STBY
SMBCLK_STBY
SMLK0_LAN_CLK
SRN1
SMLK0_LAN_DATA
SMLK1_SIO_CLK
SMLK1_SIO_DATA
PCIE_WAKE_L
PCH_GP45
GP57_5V_DETECT
RI_UP_L
SMBALERT_L
SML0ALERT_L
SML1ALERT_L
PCH_GP27
SUSWARN_L
PCH_GP31
DRAM_PWROK
LPCPD_L
GPIO34
PCH_GP20_PU
PCH_GP26
F_AUD_DETECT_SB
LPC_DRQ0_L
GPIO0
GPIO72_BOMDET5
PCH_GP20_PU
PCH_GP45
GP57_5V_DETECT
PCH_JTAG_RST_R
GPIO12_BOMDET4
PCH_RTCX1
PCH_RTCX2
R402 10M
X3
Y-32.768K
C392 10P-04
C393 10P-04
GND
RSMRST_L P30
Short PAD-04
DPWROK
DSWODVREN Hi For All Products.
DSWODVREN R395 390K-04
+RTCVCC
+3VSB
+V_1P5_SM
+VCC3
R390 20K-04
C370 1U-X7R
SRTCRST_L
R420 1K-04-O
TLS_EN
TLS Confidentiality:
TLS_EN (internal PD)
H Enable TLS
L Disable TLS
Without TLS
no AMT, RCFG(remote Config), or RPAT.
In Sugar Bay Q series Platform,
Enable TLS for vPro.
HDA_BITCLK_R
reserve for EMI
SC35 10P-04-O
change to RN
RN37 33-8P4R
HDA_SDOUT_R
HDA_SYNC_R
HDA_RST_R_L
HDA_BITCLK_R
HDA_SDOUT
HDA_SYNC
HDA_RST_L
HDA_BITCLK
R438 10K-04-O
Reserve for Debug
PCH_SYSPWROK
R445 0-04
VR_READY 5,37
C430 22U-6V3-08-O
R446 10K-04-O
R458 1K-04
PWRGD
MN13 2N7002-S
H_SKTOCC_L
PCH_SKTOCC_L
R457 0-04-O
R456 10K-04-O
For Power Test without CPU.
PCH_SPKR R505 1K-04-O
No Reboot Mode with TCO Disabled:
PCH_SPKR (internal PD)
H Enable No Reboot
L Disable
INTVRMEN
R398 390K-04
R394 1K-04-O
Integrated 1.05V SUS VRM:
INTVRMEN
H Enable
L Disable
for Intel internal only
PCH_GP44
R421 10K-04
R411 10K-04-O
(internal PU)
JTAG CLK FILTER:
PCH_GP44
H Enable
L Bypass
R383 1K-04-O
R380 1K-04-O
HDA_SYNC_R
On-Die PLL VR Source:
HDA_SYNC_R (internal PD)
H 1.5V
L 1.8V
PCH_GP46
R418 10K-04
R407 10K-04-O
for Intel internal only
DFX TEST MODE Rings Oscillator:
PCH_GP46 (internal PU)
H Enable
L Bypass
ON_DIE_PLL_EN
R434 1K-04
R433 1K-04-O
On-Die PLL VR:
ON_DIE_PLL_EN (internal PU)
H Enable
L Disable
R477 39.2K-1-04-O
R478 7.87K-1-04-O
C431 1U-04-O
R465 4.7K-04-O
RSMRST_FC
RSMRST_FB
QN14
QN15
PMBS3904-S-O
R441 10K-04
C429 .1U-04-O
R450 100K-04
RSMRST_L
+5VSB
GND
1)AC ON: 3VSB vs RSMRST(t204: min 10ms)
2)AC OFF: 3VSB>2.9V when RSMRST<0.8V
R42 10K-04-O
SC63 1U-X7-04-O
IGC_EN_L R406 1K-04-O
no DSW
0731-A
GPIO32,33,35:
default GPO, no need PU
When Deep Sleep not implemented:
1.PCH_GP30, PCH_GP27 need to be Pull Up.
2.VCCDSW3_3 should to be connected to +3VSB.
3.SLP_SUS_L, SUSACK_L left unconnected.
4.SUSWARN_L may be used as GPIO30.(Reference to 1.)
For platform not supporting deep sleep connect directly to RSMRST#.
PCH_GP31 need be pulled low when Deep-Sleep
V1.0 : add tp for ME test
0809-B
remove XDP Header
GPIO8 is no longer needed as a functional strap for Integrated clocking. Integrated Clock Enable functionality is achieved via soft-strap. The current default is Clock Enabled
Internal Pull Up:
teknisi indonesia
Elitegroup Computer Systems
PCH - MISC, Strap Function
H61H2-CM
V1.0
Monday, December 20, 2010
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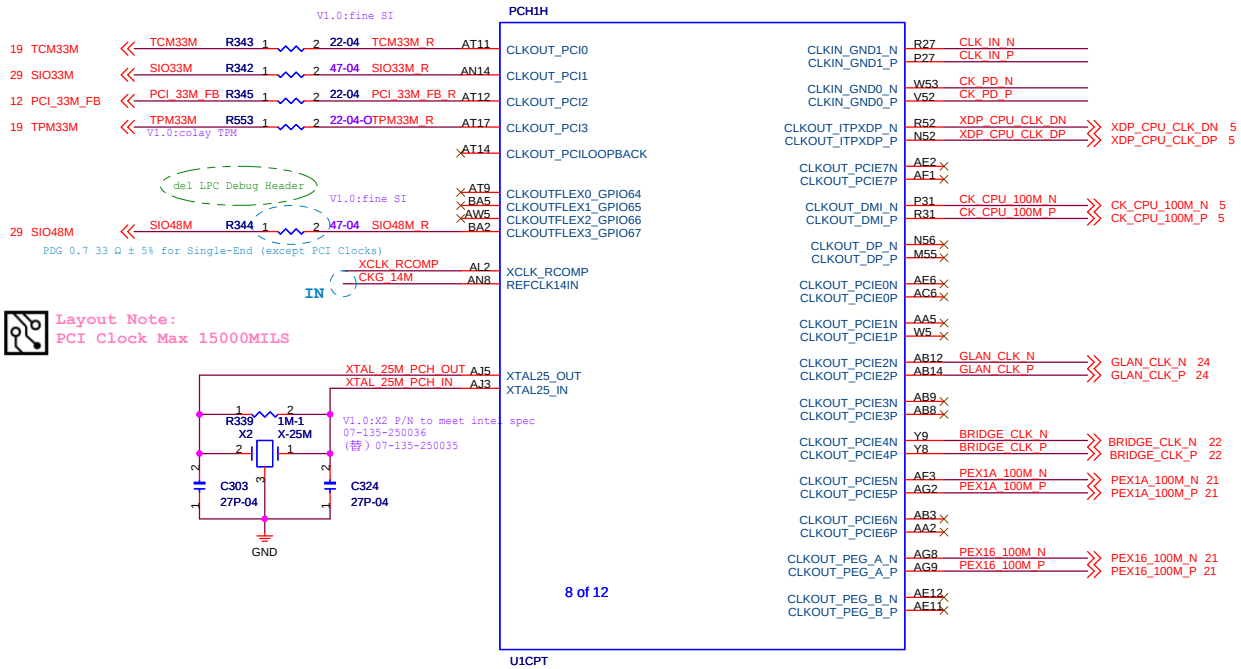
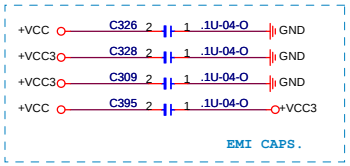
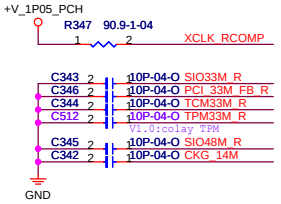
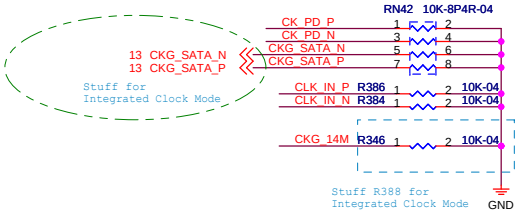
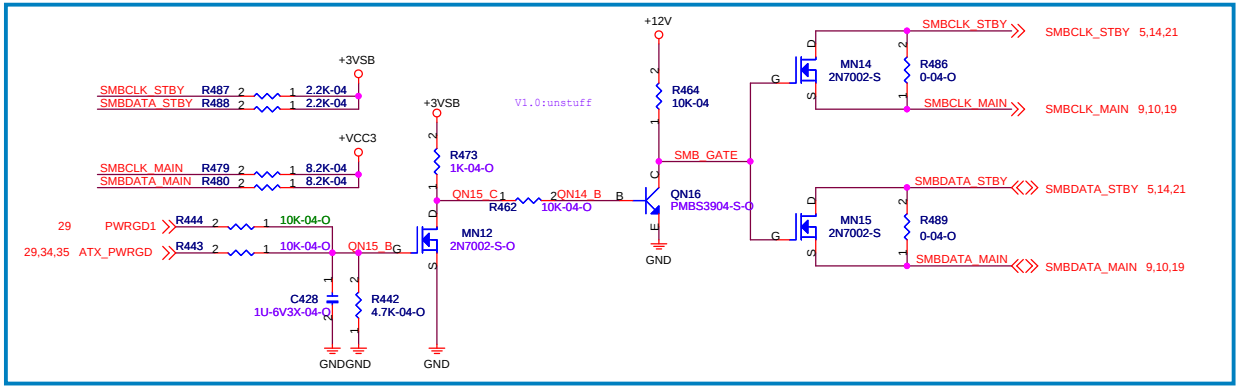




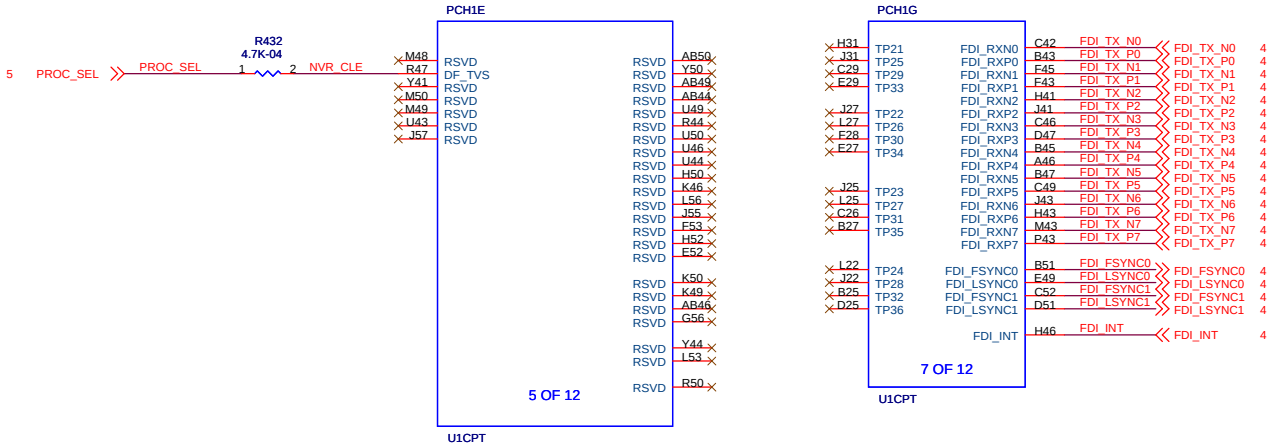


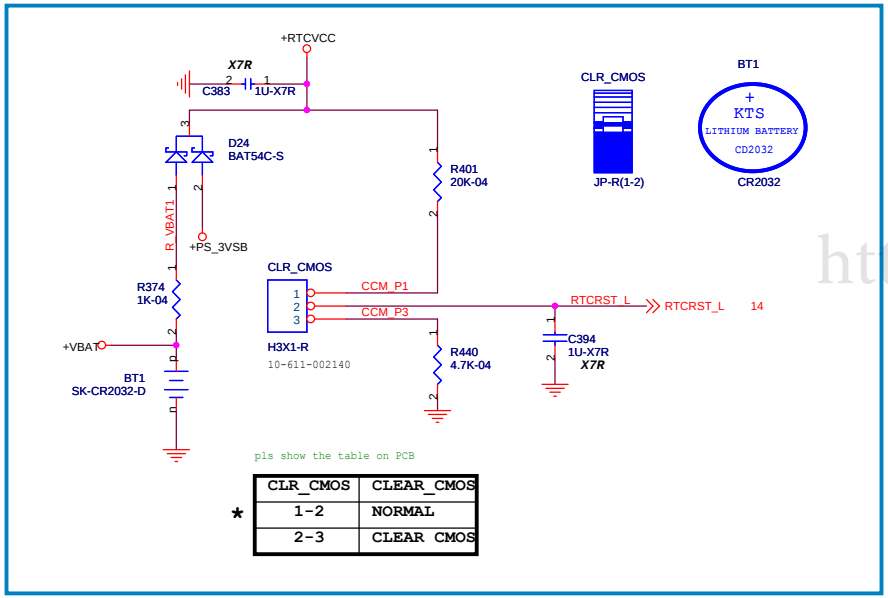




SMBUS Logic Circuit

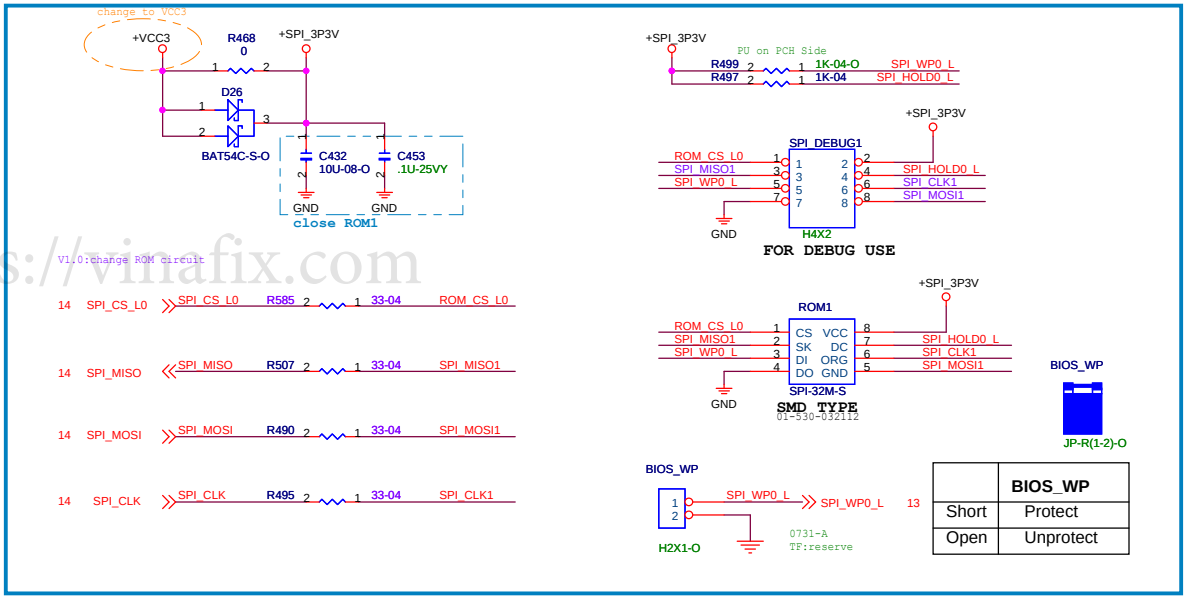
Elitegroup Computer Systems			
Title: PCH - CLK IO,SMbu			
Size: Custom	Document Number: H61H2-CM		Rev: V1.0
Date: Monday, December 20, 2010	Sheet 15 of 42		





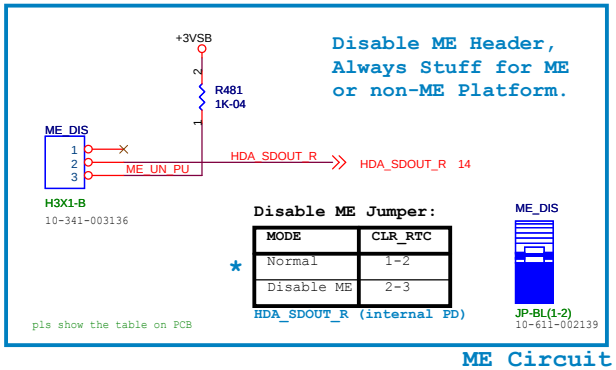
CLR_CMOS	CLEAR_CMOS
1-2	NORMAL
2-3	CLEAR CMOS

CLR_CMOS Circuit



	BIOS_WP
Short	Protect
Open	Unprotect

SPI ROM Circuit



MODE	CLR_RTC
Normal	1-2
Disable ME	2-3

ME Circuit

Elitegroup Computer Systems

Title: FDI,CLR_CMOS,ROM

Size: Custom | Document Number: H61H2-CM | Rev: V1.0

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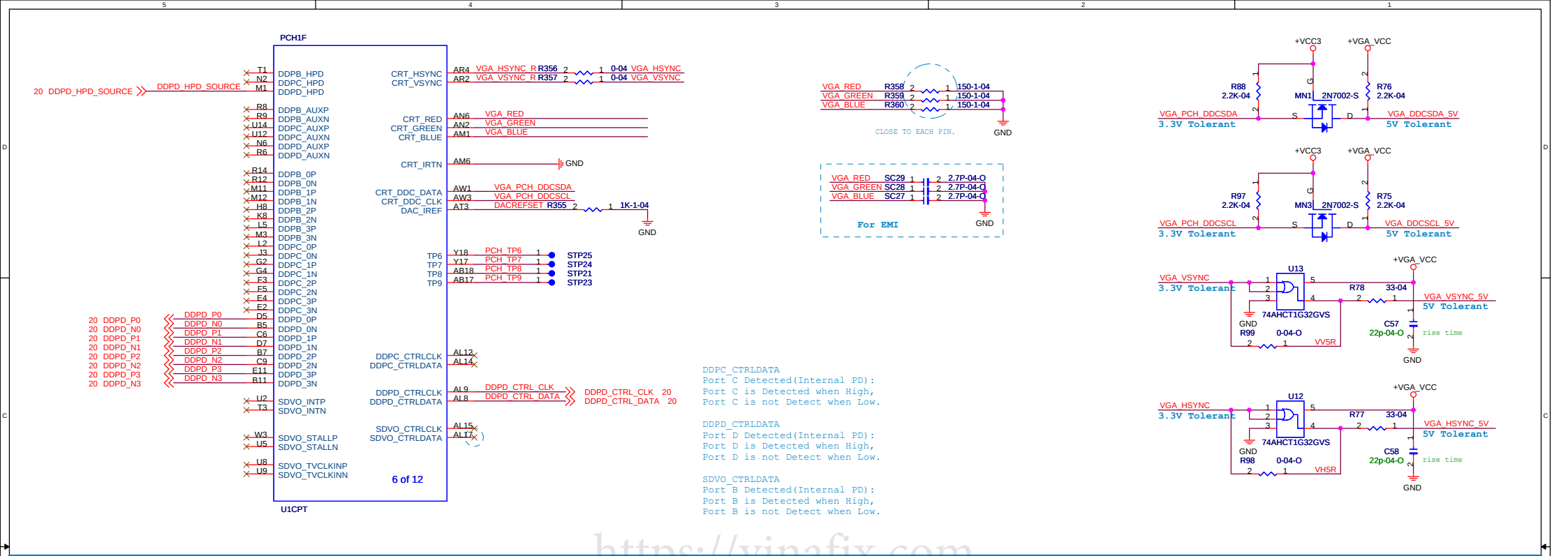
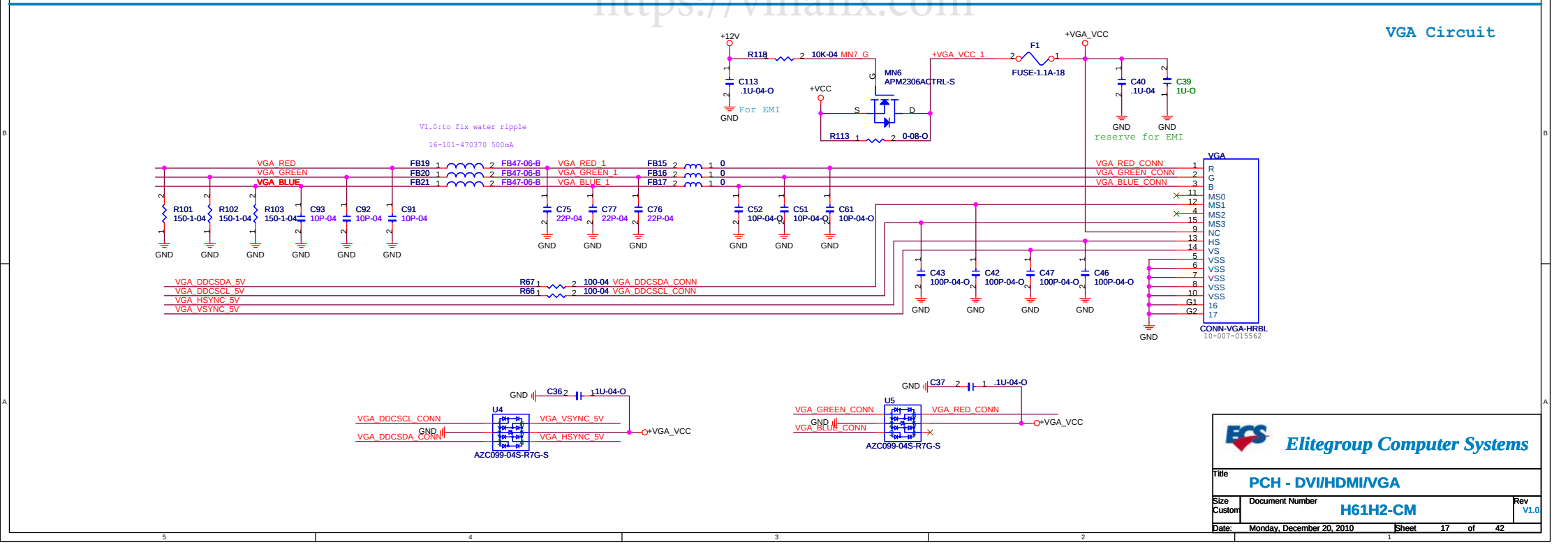
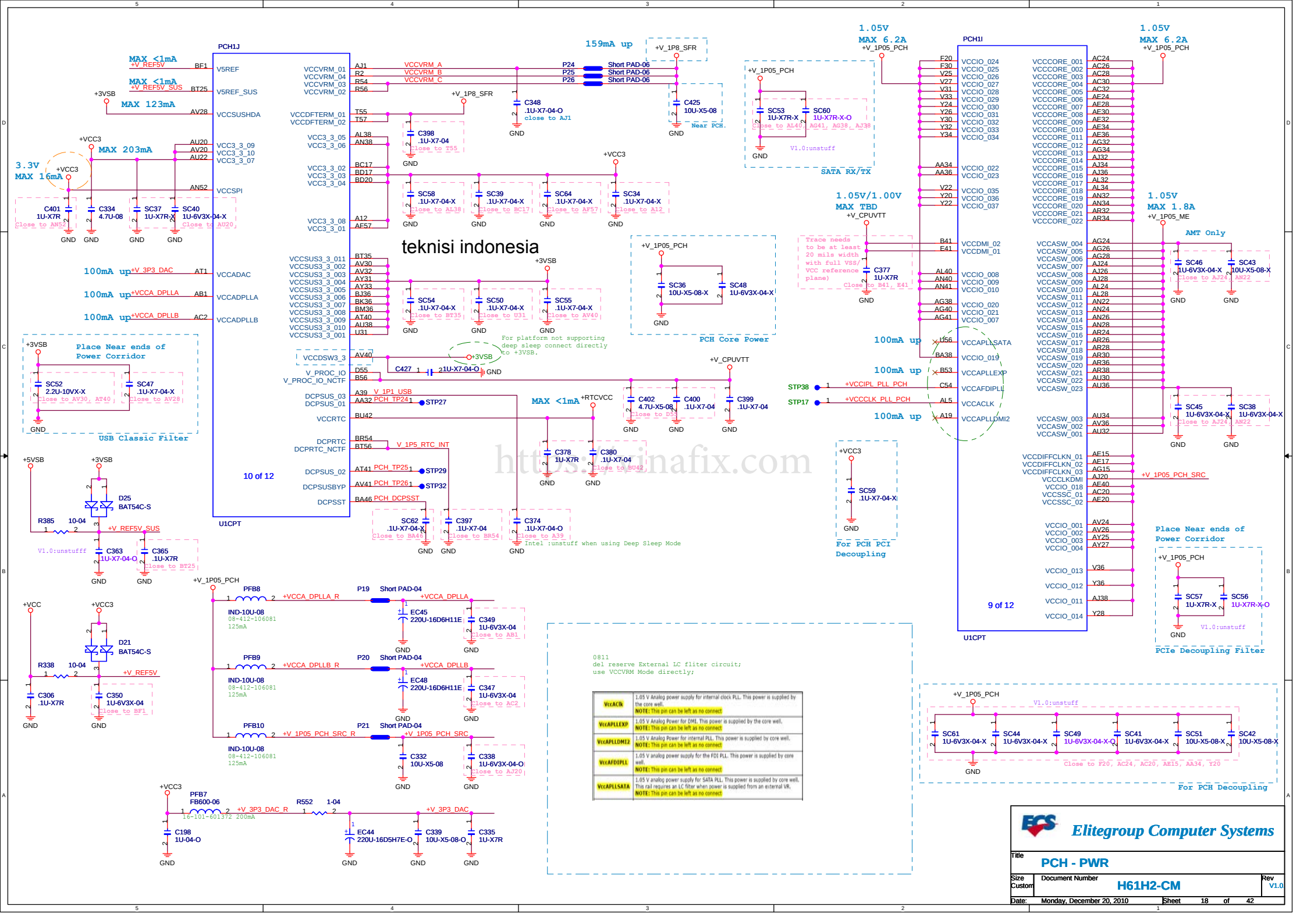
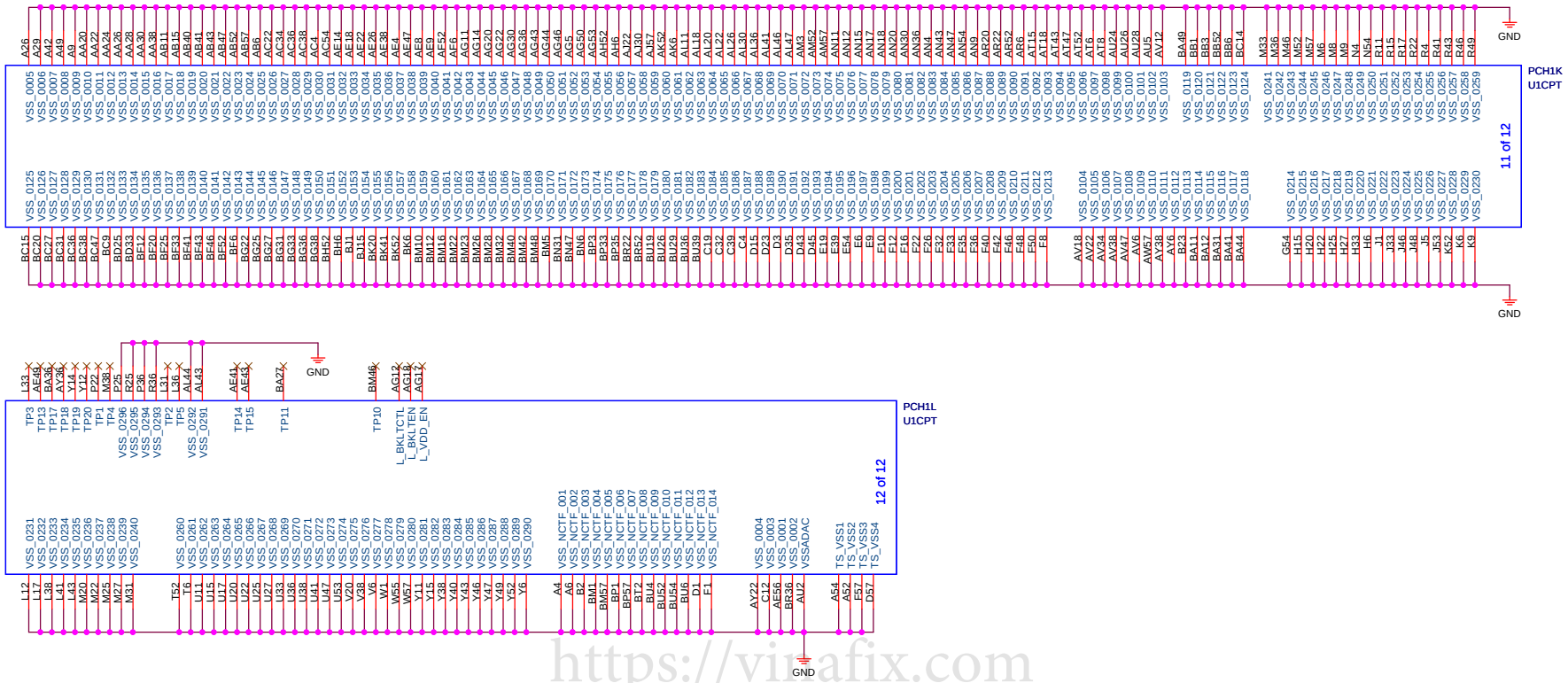




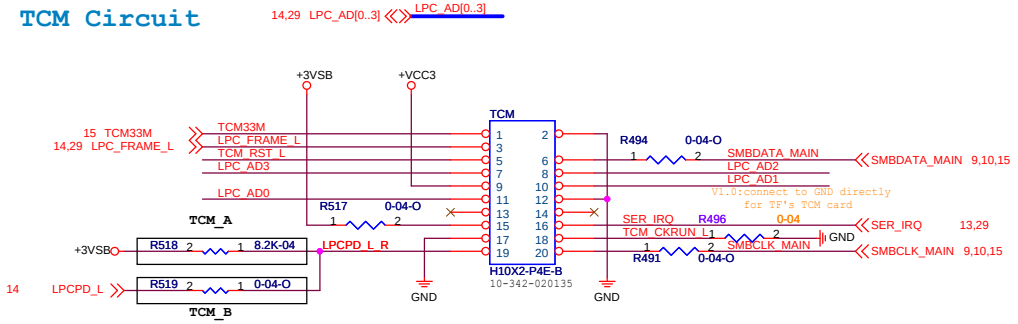
Elitegroup Computer Systems			
Title	PCH - DVI/HDMI/VGA		
Size: Custom	Document Number: H61H2-CM		Rev: V1.0
Date: Monday, December 20, 2010	Sheet 17 of 42		



Elitegroup Computer Systems				
Title	PCH - PWR			
Size: Custom	Document Number: H61H2-CM			Rev: V1.0
Date: Monday, December 20, 2010		Sheet 18 of 42		



TCM Circuit

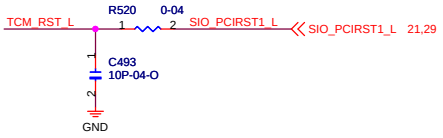


BOM Difference

	TongFang TCM	normal TCM
TCM_A	v	x
TCM_B	x	v

* V:stuff X:NC

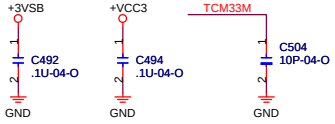
TF note: keep pin 13,14,6,15,20 no connect



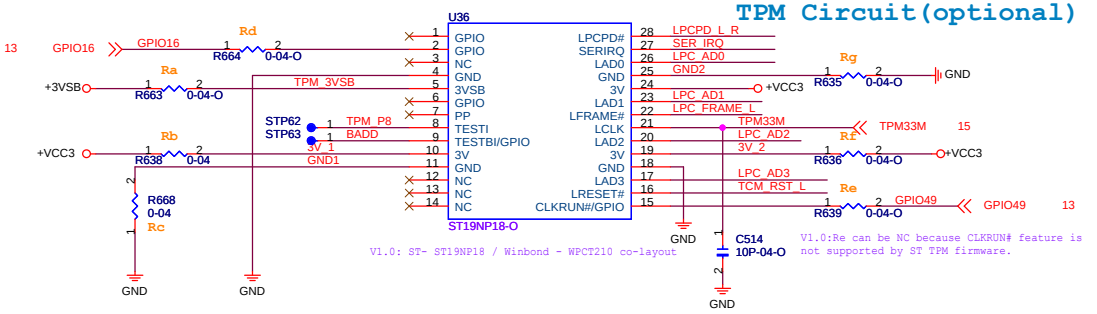
BOM Difference

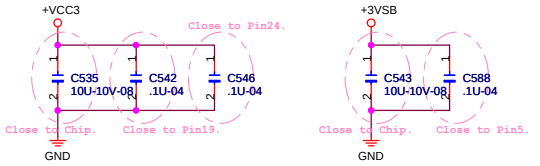
	china one	other customer
R496	0 OHM	check TCM Card spec

*



TPM Circuit(optional)





*

02-440-918264:
IC TPM.ST19NP18ER28PVLR..TSSOP 28P.3.3V.....LEAD-FREE(RoHS).ST

02-440-210900:
IC TPM.WPCT210CA0WX..TSSOP 28P.....HF.LEAD-FREE.NUVOTON

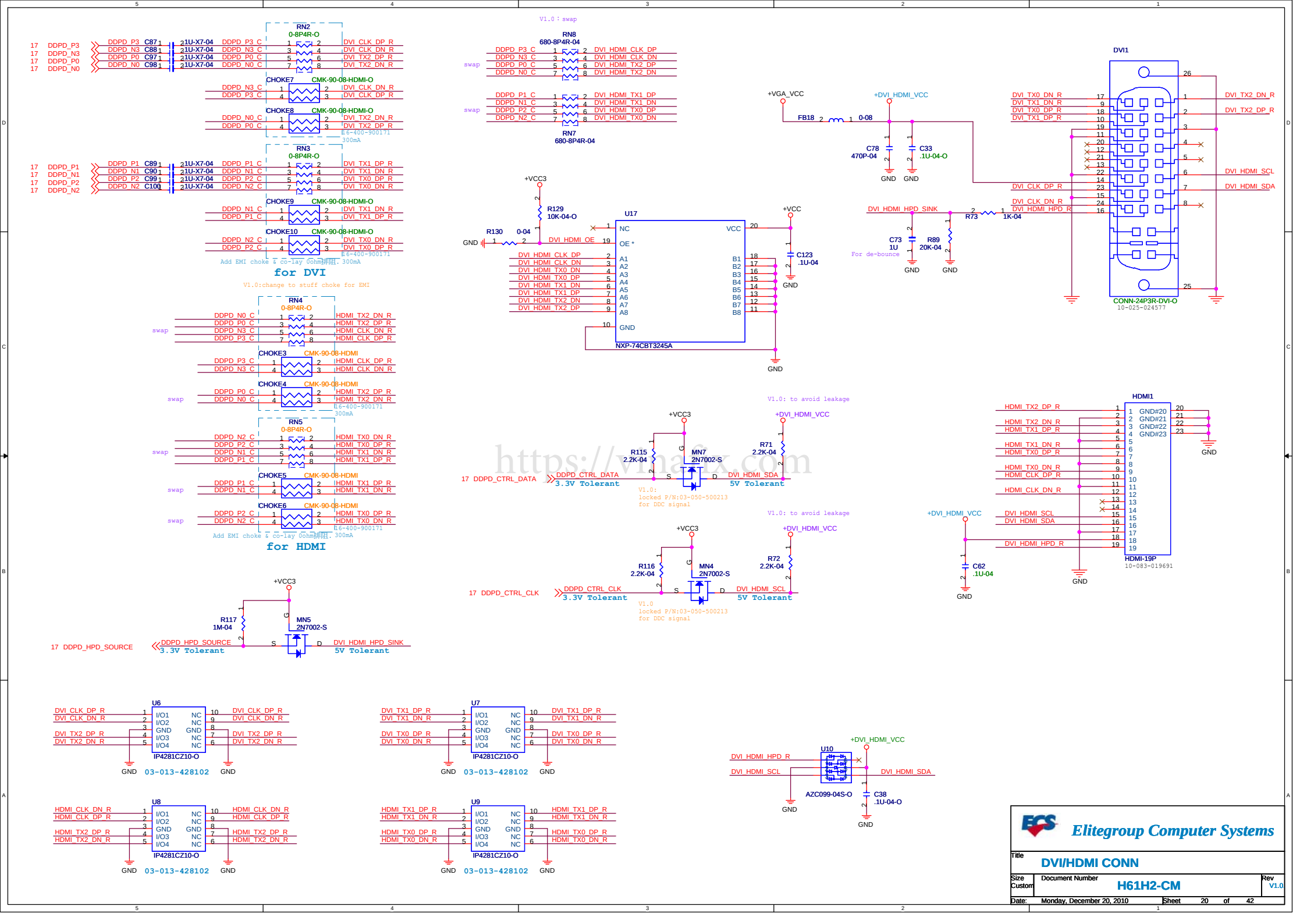
	Ra	Rb	Rc	Rd	Re	Rf	Rg
ST	X	V	V	X	X	X	X
Winbond	V	X	X	X	X	V	V

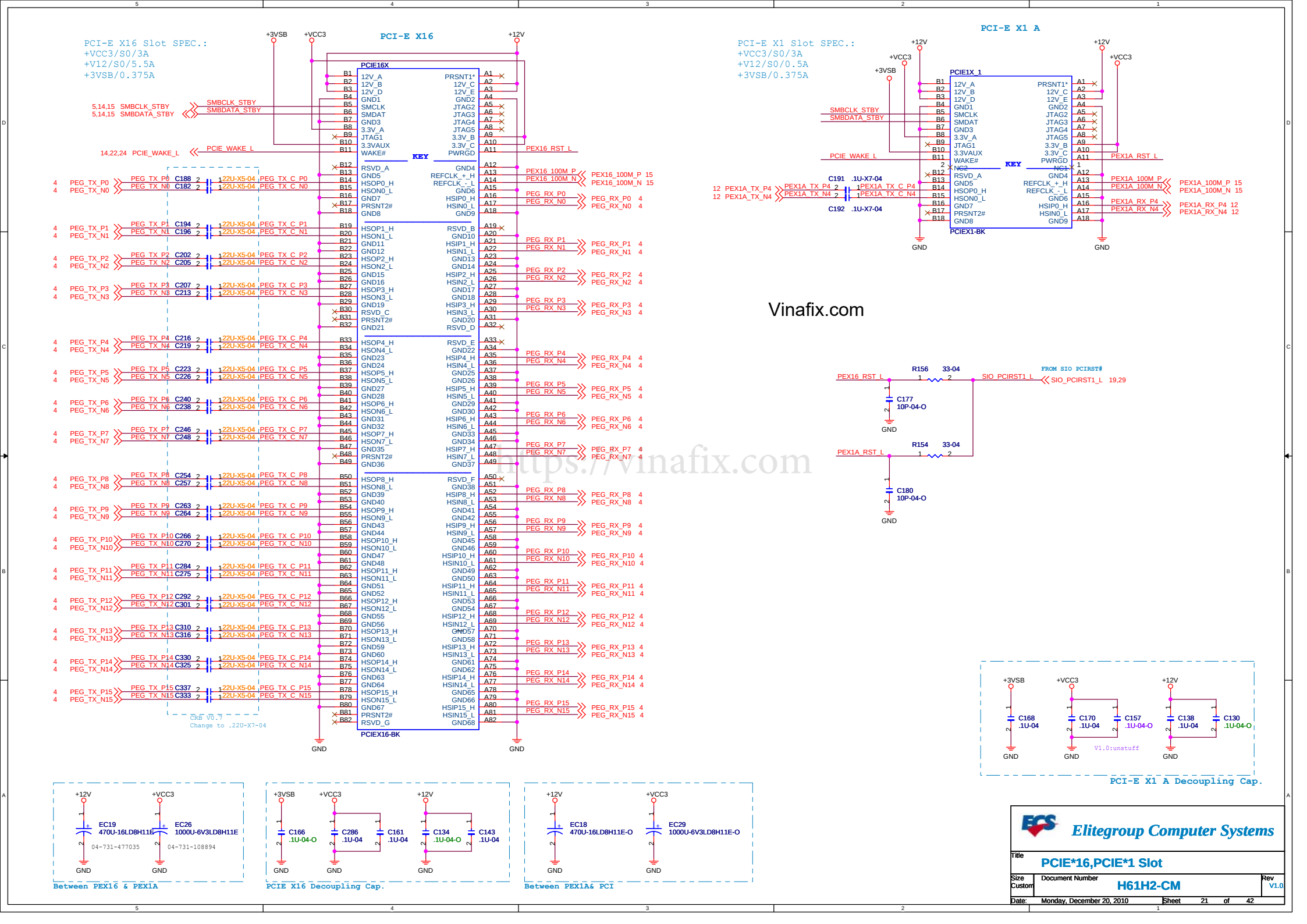
Elitegroup Computer Systems

Title: PCH - GND,TCM Header

Size: Custom | Document Number: H61H2-CM | Rev: V1.0

Date: Monday, December 20, 2010 | Sheet 19 of 42


RN2
0-8P4R-O
CHOKE7 CMK-90-08-HDMI-O
CHOKE8 CMK-90-08-HDMI-O
RN3
0-8P4R-O
CHOKE9 CMK-90-08-HDMI-O
CHOKE10 CMK-90-08-HDMI-O
for DVI
RN8
680-8P4R-04
RN7
680-8P4R-04
U17
NXP-74CBT3245A
DVI1
CONN-24P3R-DVI-O
RN4
0-8P4R-O
CHOKE3 CMK-90-08-HDMI
CHOKE4 CMK-90-08-HDMI
RN5
0-8P4R-O
CHOKE5 CMK-90-08-HDMI
CHOKE6 CMK-90-08-HDMI
for HDMI
HDMI1
HDMI-19P
MN5 2N7002-S
MN7 2N7002-S
MN4 2N7002-S
U6
U7
U8
U9
U10
IP4281CZ10-O
AZC099-04S-O
Elitegroup Computer Systems
DVI/HDMI CONN
H61H2-CM
Monday, December 20, 2010


PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A
PCI-E X16
PCIE16X
PCIEX16-BK
KEY
5,14,15 SMBCLK_STBY
5,14,15 SMBDATA_STBY
14,22,24 PCIE_WAKE_L
PEX16_RST_L
PEX16_100M_P
PEX16_100M_N
PEG_RX_P0
PEG_RX_N0
PEG_TX_P0
PEG_TX_N0
C188
C182
CRB V0.7
Change to .22U-X7-04
PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A
PCI-E X1 A
PCIE1X_1
PCIEX1-BK
PEX1A_RST_L
PEX1A_100M_P
PEX1A_100M_N
PEX1A_RX_P4
PEX1A_RX_N4
PEX1A_TX_P4
PEX1A_TX_N4
C191 .1U-X7-04
C192 .1U-X7-04
Vinafix.com
https://Vinafix.com
R156 33-04
R154 33-04
PEX16_RST_L
PEX1A_RST_L
SIO_PCIRST1_L
FROM SIO PCIRST#
SIO_PCIRST1_L 19,29
C177 10P-04-O
C180 10P-04-O
C168 .1U-04
C170 .1U-04
C157 .1U-04-O
C138 .1U-04
C130 .1U-04-O
V1.0:unstuff
PCI-E X1 A Decoupling Cap.
EC19 470U-16LD8H11E
EC26 1000U-6V3LD8H11E
04-731-477035
04-731-108894
Between PEX16 & PEX1A
C166 .1U-04-O
C286 .1U-04
C161 .1U-04
C134 .1U-04-O
C143 .1U-04
PCIE X16 Decoupling Cap.
EC18 470U-16LD8H11E-O
EC29 1000U-6V3LD8H11E-O
Between PEX1A& PCI
Elitegroup Computer Systems
Title
PCIE*16,PCIE*1 Slot
Size Custom
Document Number
H61H2-CM
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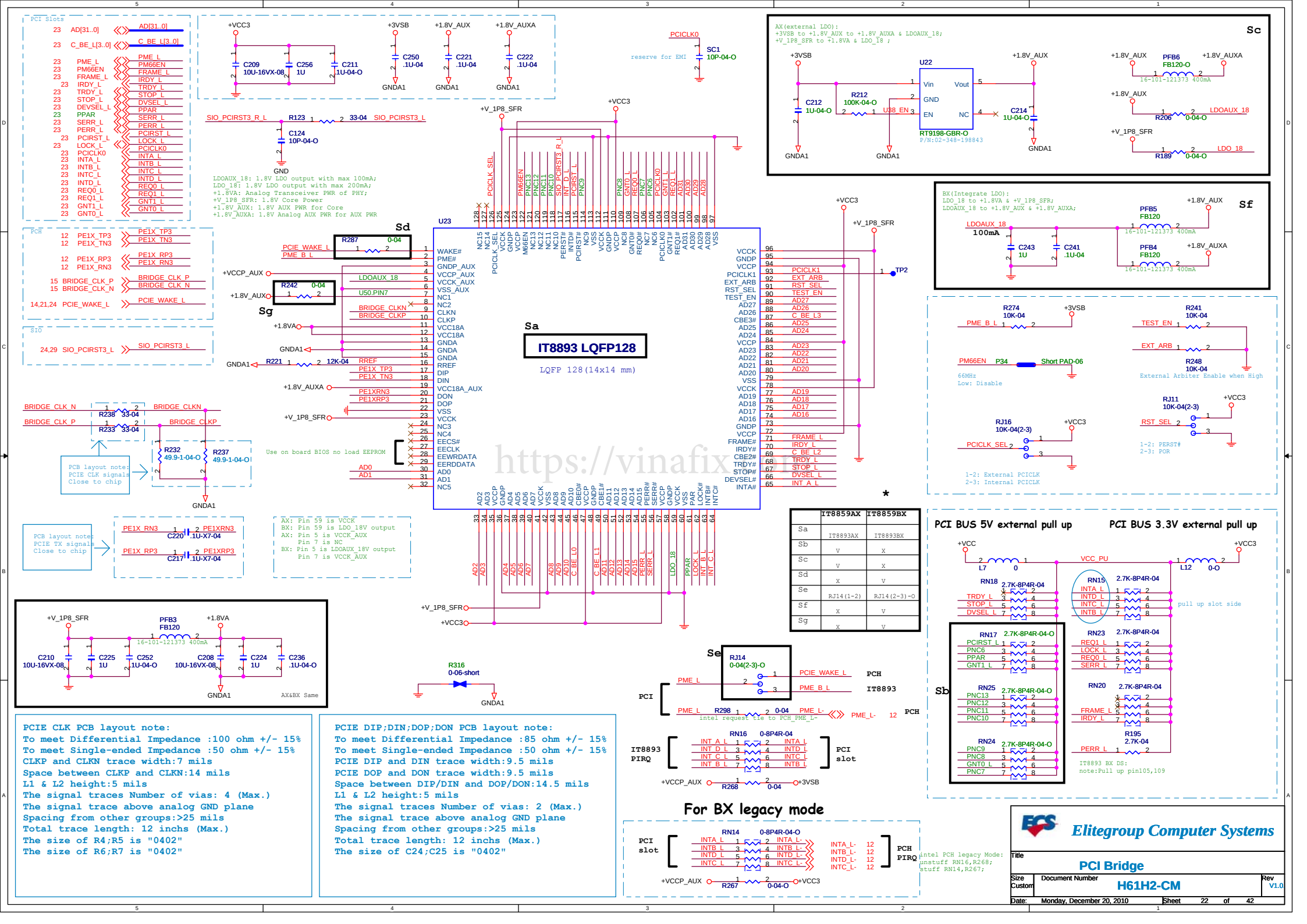
PCI Slots
AD[31..0]
C_BE_L[3..0]
PME_L
PM66EN
FRAME_L
IRDY_L
TRDY_L
STOP_L
DVSEL_L
PPAR
SERR_L
PERR_L
PCIRST_L
LOCK_L
PCICLK0
INTA_L
INTB_L
INTC_L
INTD_L
REQ0_L
REQ1_L
GNT1_L
GNT0_L
PCH
PE1X_TP3
PE1X_TN3
PE1X_RP3
PE1X_RN3
BRIDGE_CLK_P
BRIDGE_CLK_N
PCIE_WAKE_L
SIO
SIO_PCIRST3_L
+VCC3
+3VSB
+1.8V_AUX
+1.8V_AUXA
C209 10U-16VX-08
C256 1U
C211 .1U-04-O
C250 .1U-04
C221 .1U-04
C222 .1U-04
GNDA1
PCICLK0
reserve for EMI
SC1 10P-04-O
SIO_PCIRST3_R_L
R123 33-04
SIO_PCIRST3_L
C124 10P-04-O
GND
LDOAUX_18: 1.8V LDO output with max 100mA;
LDO_18: 1.8V LDO output with max 200mA;
+1.8VA: Analog Transceiver PWR of PHY;
+V_1P8_SFR: 1.8V Core Power
+1.8V_AUX: 1.8V AUX PWR for Core
+1.8V_AUXA: 1.8V Analog AUX PWR for AUX PWR
Sd
PCIE_WAKE_L
PME_B_L
R287 0-04
+VCCP_AUX
+1.8V_AUX
R242 0-04
LDOAUX_18
U50.PIN7
Sg
+1.8VA
GNDA1
R221 12K-04
RREF
BRIDGE_CLKN
BRIDGE_CLKP
PE1X_TP3
PE1X_TN3
+1.8V_AUXA
PE1XRN3
PE1XRP3
+V_1P8_SFR
Use on board BIOS no load EEPROM
AD0
AD1
U23
WAKE#
PME#
GNDP_AUX
VCCP_AUX
VCCK_AUX
VSS_AUX
NC1
NC2
CLKN
CLKP
VCC18A
VCC18A
GNDA
GNDA
GNDA
RREF
DIP
DIN
VCC18A_AUX
DON
DOP
VSS
VCCK
NC3
NC4
EECS#
EECLK
EEWRDATA
EERDDATA
AD0
AD1
NC5
Sa
IT8893 LQFP128
LQFP 128(14x14 mm)
PCICLK_SEL
PM66EN
SIO_PCIRST3_R_L
INT_D_L
PCIRST_L
PNC3
PNC8
REQ0_L
PNC7
PNC6
PCICLK0
GNT1_L
REQ1_L
AD31
AD30
AD29
AD28
VCCK
GNDP
VCCP
PCICLK1
EXT_ARB
RST_SEL
TEST_EN
AD27
AD26
CBE3#
AD25
AD24
AD23
AD22
AD21
AD20
FRAME#
IRDY#
CBE2#
TRDY#
STOP#
DEVSEL#
INTA#
TP2
AD19
AD18
AD17
AD16
FRAME_L
IRDY_L
C_BE_L2
TRDY_L
STOP_L
DVSEL_L
INT_A_L
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
C_BE_L0
AD11
AD12
AD13
AD14
AD15
PERR_L
SERR_L
LDO_18
PPAR
LOCK_L
INT_B_L
INT_C_L
BRIDGE_CLK_N
BRIDGE_CLK_P
R238 33-04
R233 33-04
BRIDGE_CLKN
BRIDGE_CLKP
R232 49.9-1-04-O
R237 49.9-1-04-O
PCB layout note:
PCIE CLK signals
Close to chip
PE1X_RN3
C220 .1U-X7-04
PE1XRN3
PE1X_RP3
C217 .1U-X7-04
PE1XRP3
AX: Pin 59 is VCCK
BX: Pin 59 is LDO_18V output
AX: Pin 5 is VCCK_AUX
Pin 7 is NC
BX: Pin 5 is LDOAUX_18V output
Pin 7 is VCCK_AUX
+V_1P8_SFR
PFB3 FB120
16-101-121373 400mA
+1.8VA
C210 10U-16VX-08
C225 1U
C252 .1U-04-O
C208 10U-16VX-08
C224 1U
C236 .1U-04-O
AX&BX Same
R316 0-06-short
Sc
AX(external LDO):
+3VSB to +1.8V_AUX to +1.8V_AUXA & LDOAUX_18;
+V_1P8_SFR to +1.8VA & LDO_18 ;
U22
Vin
Vout
GND
EN
NC
RT9198-GBR-O
P/N:02-348-198843
C212 1U-04-O
R212 100K-04-O
U38_EN
C214 1U-04-O
PFB6 FB120-O
16-101-121373 400mA
R206 0-04-O
LDOAUX_18
R189 0-04-O
LDO_18
Sf
BX(Integrate LDO):
LDO_18 to +1.8VA & +V_1P8_SFR;
LDOAUX_18 to +1.8V_AUX & +1.8V_AUXA;
LDOAUX_18
100mA
C243 1U
C241 .1U-04
PFB5 FB120
PFB4 FB120
R274 10K-04
PME_B_L
PM66EN
P34
Short PAD-06
66MHz
Low: Disable
R241 10K-04
TEST_EN
EXT_ARB
R248 10K-04
External Arbiter Enable when High
RJ11 10K-04(2-3)
RST_SEL
RJ16 10K-04(2-3)
PCICLK_SEL
1-2: PERST#
2-3: POR
1-2: External PCICLK
2-3: Internal PCICLK
IT8859AX
IT8859BX
Sa
Sb
Sc
Sd
Se
Sf
Sg
PCI BUS 5V external pull up
PCI BUS 3.3V external pull up
L7 0
VCC_PU
L12 0-O
RN18 2.7K-8P4R-04
TRDY_L
STOP_L
DVSEL_L
RN15 2.7K-8P4R-04
INTA_L
INTD_L
INTC_L
INTB_L
pull up slot side
RN17 2.7K-8P4R-O
PCIRST_L
PNC6
PPAR
GNT1_L
RN23 2.7K-8P4R-04
REQ1_L
LOCK_L
REQ0_L
SERR_L
RN25 2.7K-8P4R-O
PNC13
PNC12
PNC11
PNC10
RN20 2.7K-8P4R-04
FRAME_L
IRDY_L
RN24 2.7K-8P4R-O
PNC9
PNC8
GNT0_L
PNC7
R195 2.7K-04
PERR_L
IT8893 BX DS:
note:Pull up pin105,109
Se
RJ14 0-04(2-3)-O
PCIE_WAKE_L
PME_L
PME_B_L
PCH
IT8893
PCI
R298 0-04
PME_L-
intel request tie to PCH_PME_L-
RN16 0-8P4R-04
INT_A_L
INT_D_L
INT_C_L
INT_B_L
IT8893 PIRQ
PCI slot
R268 0-04
+3VSB
For BX legacy mode
RN14 0-8P4R-04-O
R267 0-04-O
PCH PIRQ
intel PCH legacy Mode:
unstuff RN16,R268;
stuff RN14,R267;
PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of R4;R5 is "0402"
The size of R6;R7 is "0402"
PCIE DIP;DIN;DOP;DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of C24;C25 is "0402"
Elitegroup Computer Systems
Title
PCI Bridge
Size Custom
Document Number
H61H2-CM
Rev V1.0
Date: Monday, December 20, 2010
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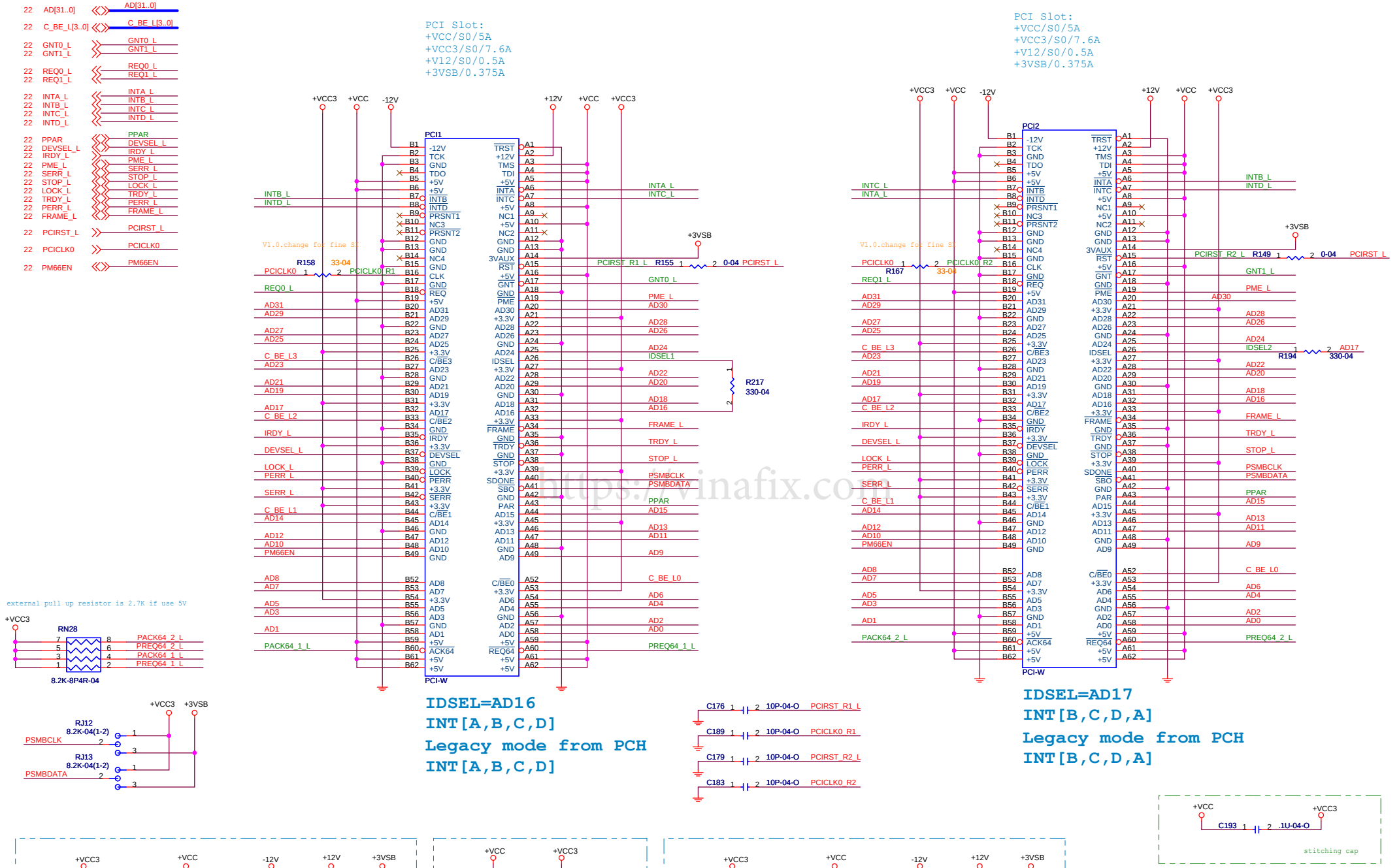
PCI Slot:
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A
PCI Slot:
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A
IDSEL=AD16
INT[A,B,C,D]
Legacy mode from PCH
INT[A,B,C,D]
IDSEL=AD17
INT[B,C,D,A]
Legacy mode from PCH
INT[B,C,D,A]
external pull up resistor is 2.7K if use 5V
8.2K-8P4R-04
PCI1 Decoupling Cap.
Between PCI1 & PCI2
PCI2 Decoupling Cap.
stitching cap
Elitegroup Computer Systems
PCI Slot
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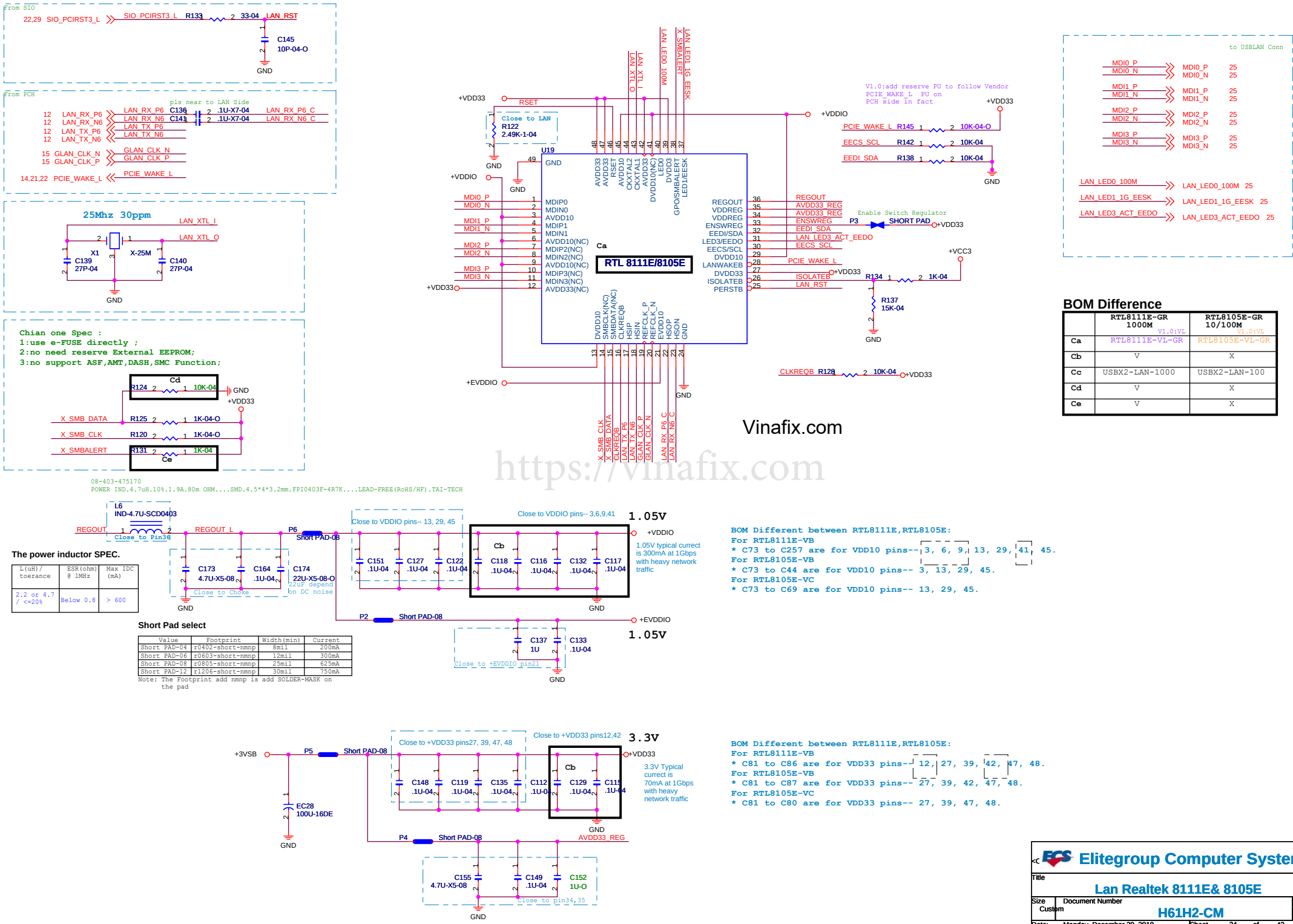

BOM Difference

	RTL8111E-GR 1000M V1.0:VL	RTL8105E-GR 10/100M V1.0:VL
Ca	RTL8111E-VL-GR	RTL8105E-VL-GR
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	V	X
Ce	V	X

Elitegroup Computer Systems

Title: Lan Realtek 8111E& 8105E

Size: Custom | Document Number: H61H2-CM | Rev: V1.0.

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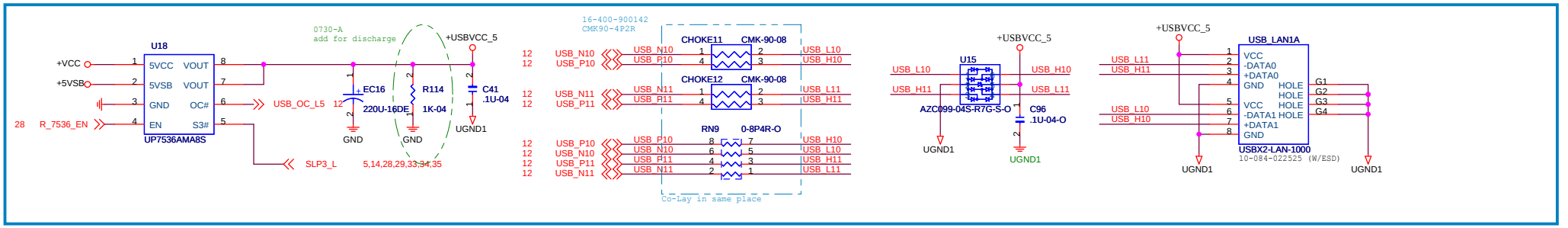
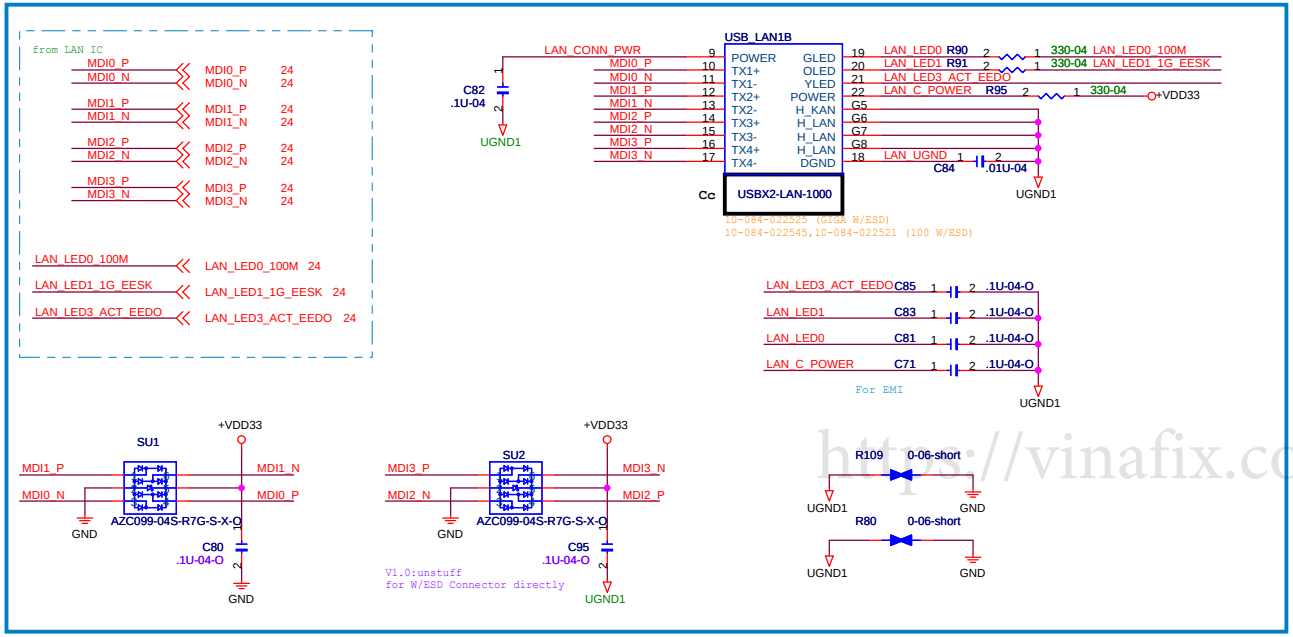
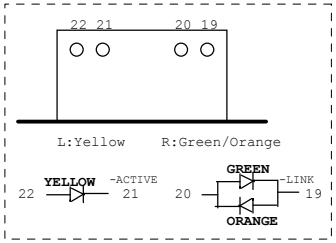




REAR SIDE 2 PORTS ON LANUSB CONN.



For China-one LED Light:

	Status	Yellow	Grn/Org
	No Link	Off	Off
	S3/S4/S5	Off	Off
	10M, inactive	Off	Off
	10M, active		Off
	100M, inactive	Off	
	100M, active		
	1G, inactive	Off	
	1G, active		
	Blinking		

REAR SIDE 2 PORTS ON LANUSB CONN.

RTL8111E-VB-GR_Datasheet_1.3

Table 12. Customized LEDs

	LINK			ACT/Full
Speed	Link 10M	Link 100M	Link 1000M	-
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
Not Defined	Bit 8	Bit 9	Bit 10	Bit 11
LED 3	Bit 12	Bit 13	Bit 14	Bit 15

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Selected Speed LINK+ACT

Note1: ACT means blinking TX and RX. LINK indicates Link 10M/100M/1000M.
Note2: There are four special modes:

Mode A: LED OFF Mode → Set all bits to 0

Mode B: Full Duplex LED Mode → Set LED 0=0, and either LED 1 or LED 3 >0
LED 0 = Full Duplex
LED 1 = Follow Customized LED rule
LED 3= Follow Customized LED rule

Mode C: Separated TX/RX Mode → Set LED 0=0, LED1 = 0, LED3 = 1
LED 0 = TX
LED 1 = RX
LED 3= LINK

Mode D: Separated Speed ACT Mode → Set LED 0=0, LED1 =1 , LED3 = 1
LED 0 = 10ACT
LED 1 = 100ACT
LED 3= 1000ACT

RTL8111E-VB-GR_Datasheet_1.3

Table 7. LEDs

Symbol	Type	Pin No	Description
LED0	O	40	
LED1	O	37	
LED3	O	31	

LEDS1-0	00	01	10	11
LED0	ACT_{ALL}	$Link_{ALL}$/ ACT_{ALL}	Link10/ ACT_{ALL}	LINK10/ ACT_{10}
LED1	LINK100	LINK100	LINK100	LINK100/ ACT_{100}
LED3	LINK1000	LINK1000	LINK1000	LINK1000 /ACT_{1000}

Note 1: During power down mode, the LED signals are logic high.
Note 2: LEDS1-0's initial value comes from the EEPROM. If there is no EEPROM, the default value of the (LEDS1, LEDS0)=(1, 1).

Customized LEDs

	RTL8111E(1G) LED TABLE
LEDS1~0	N/A (Coutomization)
LED0	LINK100
LED1	LINK1000
LED3	LINK(all) /ACT(all)

★ Active Low

Elitegroup Computer Systems

Title: USBLAN Connector

Size: Custom | Document Number: H61H2-CM | Rev: V1.0

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14 HDA_RST_L → HDA_RST_L
14 HDA_BITCLK → HDA_BITCLK
14 HDA_SYNC → HDA_SYNC
14 HDA_SDIN0 → HDA_SDIN0
14 HDA_SDOUT → HDA_SDOUT
27 FP_AUD_DETECT → FP_AUD_DETECT

Verfout bias for stereo microphone.

RJ2 4.7K-04(2-3)-O — PER_C / PORT-E_R
D1 BAT54A-S-O — LINE2_VREFO — PEVR / PEVL
RJ1 4.7K-04(2-3)-O — PEL_C / PORT-E_L
Richtek: stuff for F_Re_tasking Function

RJ4 4.7K-04(2-3) — PFR_C / PORT-F_R
D2 BAT54A-S — MIC2_VREFO — PFVR / PFVL
RJ3 4.7K-04(2-3) — PFL_C / PORT-F_L
Ct

Placement near to codec

Cx

C16 10U-X5-08-O — EC4 100U-16D6.3H5E — PDR_C — R8 75-04 — PORT-D_R — PORT-D_R 27
C17 10U-X5-08-O — EC3 100U-16D6.3H5E — PDL_C — R9 75-04 — PORT-D_L — PORT-D_L 27

MC1 10U-16VX-08-O — C26 .1U-04-O — AUGND
reserve cap for VIA

MIC1_VREFO_R — MIC1_VREFO_R 27
LINE2_VREFO
MIC2_VREFO
MIC1_VREFO_L — MIC1_VREFO_L 27

+LDOVDD
C22 10U-X5-08 — C19 .1U-04-O — near chip — X5R
+5VA — C23 10U-X5-08 — AUGND

Cs

CLOSE TO CODEC
AUGND — R68 20K-1-04 — AUDVREFP40
C63 100P-04-O
reserve cap for VIA

use 75 ohm for ESD,retasking 75,only output 75,only input 1K.

AUDIO1

PDR, PDL, NETB, VCAP, VREF_FILT, AVSS1, AVDD1

36	VrefOut-A	24	LINE1_R/PORT-C_R
35	AVDD2	23	LINE1_L/PORT-C_L
34	PORT-A_L/SURR_L	22	MIC1_R/PORT-B_R
33	VrefOut-H	21	MIC1_L/PORT-B_L
32	PORT-A_R/SURR_R	20	CD-R
31	AVSS3	19	CD-G
30	PORT-G_L/CEN_OUT	18	CD-L
29	PORT-G_R/LEF_OUT	17	MIC2_R/PORT-F_R
28	PORT-H_L/SIDESURR_L	16	MIC2_L/PORT-F_L
27	PORT-H_R/SIDESURR_R	15	LINE2_R/PORT-E_R
26	S/PDIF IN / EAPD	14	LINE2_L/PORT-E_L
25	S/PDIF-OUT	13	SENSE A

DVDD_CORE, XI / DVSS, XO / DVDD_IO, DVSS, SDO, BCLK, DVSS, SDI, DVDD_CORE, SYNC, RESET#, PC_BEEP

Ca

AUGND — C34 .1U-04 — +5VA — AUDVREFP40

PORT-A_L	R25 75-04-O	PAL_C	10U-25D4H5E-O	EC10	PAL
PORT-A_R	R23 75-04-O	PAR_C	10U-25D4H5E-O	EC9	PAR
PORT-G_L	R50 75-04-O (R47 75-04-O)	PGL_C	10U-25D4H5E-O	EC14	PGL
PORT-G_R	R49 75-04-O	PGR_C	10U-25D4H5E-O	EC13	PGR
PORT-H_L	R48 75-04-O	PHL_C	10U-25D4H7E-O	EC8	PHL
PORT-H_R		PHR_C	10U-25D4H7E-O	EC7	PHR

27 SPO → SPO

Cd

ALC662-VC-GRS
02-301-662691

Ci

EC5 10U-25D4H5E — C10 4.7U-X5-08-O — PCR
EC6 10U-25D4H5E — C11 4.7U-X5-08-O — PCL
EC1 10U-25D4H5E — C1 4.7U-X5-08-O — PBR
EC2 10U-25D4H5E — C2 4.7U-X5-08-O — PBL

Ce

PCR_C	R12 75-04	PORT-C_R — PORT-C_R 27
PCL_C	R13 75-04	PORT-C_L — PORT-C_L 27
PBR_C	R1 75-04	PORT-B_R — PORT-B_R 27
PBL_C	R2 75-04	PORT-B_L — PORT-B_L 27

Cq

C20 4.7U-X5-08 — PFR_C — R19 1K-04 — PORT-F_R — PORT-F_R 27
C21 4.7U-X5-08 — PFL_C — R20 1K-04 — PORT-F_L — PORT-F_L 27

Richtek: 100U+75ohm for Re_tasking Function; 4.7U+1K for no Re_tasking Function
VIA: 220U+16ohm for Re_tasking Function; 100U+16ohm for no Re_tasking Function

Cr

EC12 100U-25VD6H11E — PER_C — R65 75-04 — PORT-E_R — PORT-E_R 27
EC15 100U-25VD6H11E — PEL_C — R74 75-04 — PORT-E_L — PORT-E_L 27

VIA: 220U+16ohm for Re_tasking Function; 100U+16ohm for no Re_tasking Function

NETA

GPIO(front panel detection) select table

	ALC892	ALC888S-VC	ALC662-VC
PIN-2	GPIO0/SPDIF-OUT2	SPDIF-OUT2	GPIO0
PIN-3	REGREF	GPIO0	GPIO1
PIN-4	GPIO1	GPIO1	DVSS

+VCC3 — 38 / 23 mA — R302 0-04 — AUD_VCC
PCBEEP — TP1

HDA_RST_L_RC — R108 0-04 — HDA_RST_L
HDA_SYNC
HDA_SDIN0_R — R107 33-04 — HDA_SDIN0
HDA_BITCLK
HDA_SDOUT

C104 22U-X5-08
C109 .1U-04
AUD_P9

Ck

ONLY for ALC892
03-012-712517
D14 AZ5125-01H-O
16-101-121373 400mA
PFB2 FB120-O

Cl

ONLY for ALC662
R112 GND 0-04
R105 0-04
FP_AUD_DETECT

Cm

R106 0-04-O
C108 10U-X5-08-O
ONLY for ALC892

C110 22P-04-O
C111 .1U-04-O

+PS_5VSB

Cj

02-343-805180
IC REG.L78L05ACZ-AP..TO-92.5V..LEAD-FREE.ST
D15 BAT54C-S
5VA_1

Pd = 0.27 W

+12V — R146 0 — R_AUDIO_VIN
U20 APL78L05-ECS — 5VA_OUT
MN8 APM2306ACTRL-S
EC25 100U-16DE-O
ONLY for ALC662

Cn

R127 0 — +5VA
ONLY for ALC662

Co

R126 0-O — +LDOVDD
ONLY for ALC892

5V Max:38 mA

EC17 22U-25DE — change for layout
C128 .1U-04

C171 .1U-04

AUD_VCC — R277 0-04-O — AUD_P9
+3VSB — R292 0-04
to fix HDA_SDO strap issue;

Resistors Networks

Placement near to codec

NETA — C68 100P-04-O — reserve cap for VIA

R84	5.1K-1-04	SW_D	SW_D 27
R85	10K-1-04	SW_C	SW_C 27
R83	20K-1-04	SW_B	SW_B 27
R82	39.2K-1-04-O	SW_A	SW_A 27

Cb

NETB — C18 100P-04-O — reserve cap for VIA

R35	20K-1-04	F_R_A	F_R_A 27
R34	39.2K-1-04	F_L_A	F_L_A 27
R36	10K-1-04-O	SW_G	SW_G 27
R37	5.1K-1-04-O	SW_H	SW_H 27

Cc

Elitegroup Computer Systems

Title: Audio -ALC892 COLAY 662

Size: Custom | Document Number: H61H2-CM | Rev: V1.0

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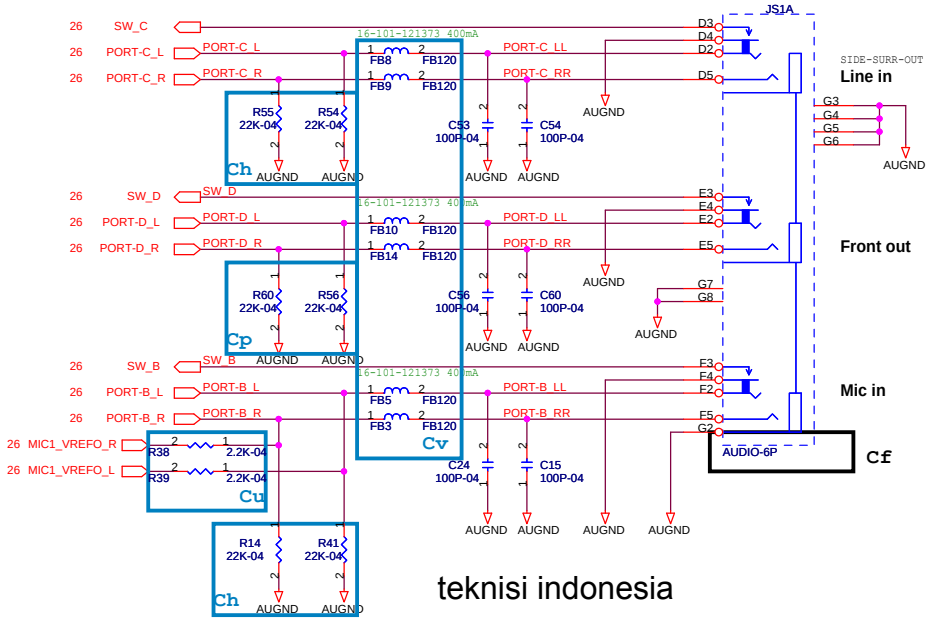

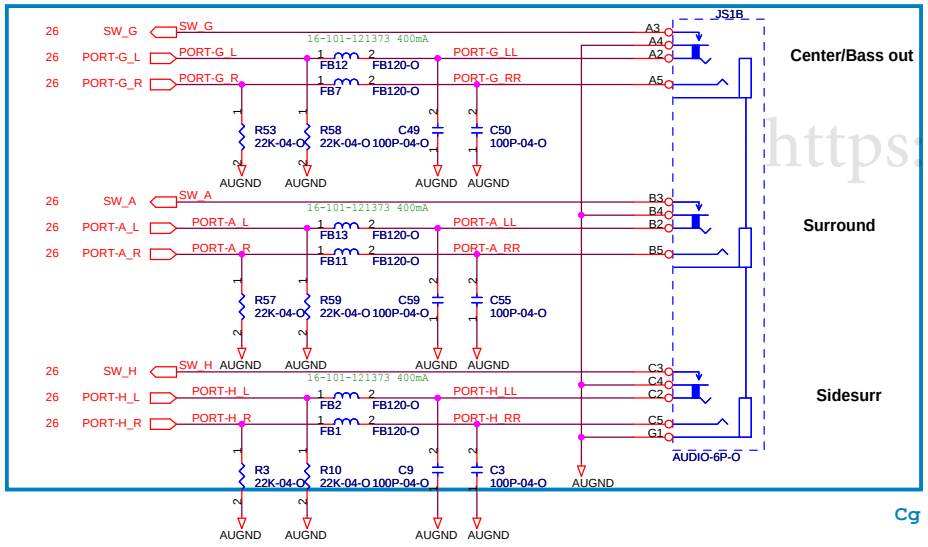

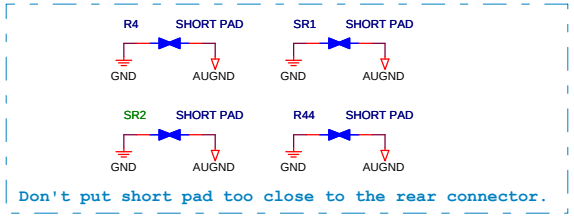

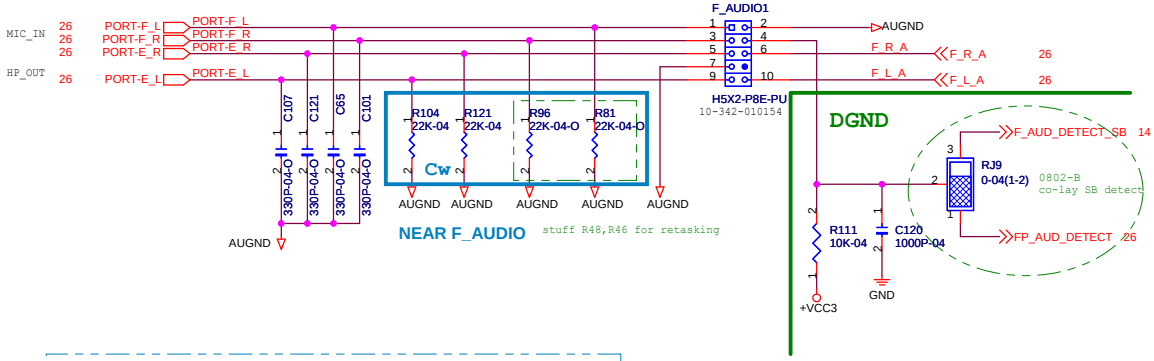

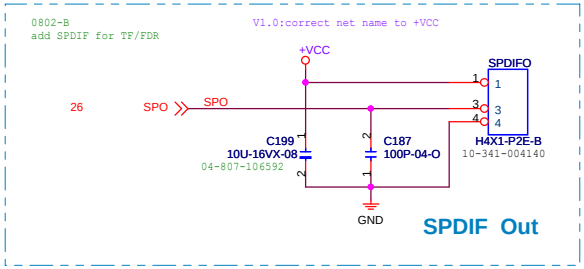

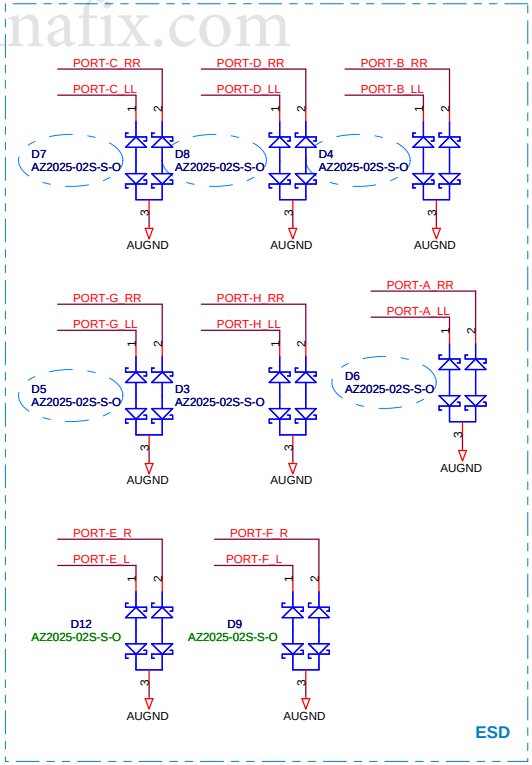

BOM Difference

	ALC892	ALC662	VT1705
Ca	V	X	X
Cb	V	X	X
Cc	V	X	X
Cd	ALC892-GR	ALC662-VC-GRS	VT1705
Ce	1K-04	75-04	0-04
Cf	AUDIO-26P	AUDIO-3P-HDA	AUDIO-3P-HDA
Cg	V	X	X
Ch	X	V	X
Ci	4.7U-X5-08	10U-25DE	10U-25DE
Cj	X	V	V
Ck	V	X	X
Cl	X	V	V
Cm	V	X	X
Cn	X	V	V
Co	V	X	X
Cp	V	V	X
Cq	4.7U+1K	4.7U+1K	10U+16ohm
Cr	75-04	75-04	16-04
Cs	20K-1-04	20K-1-04	5.1K-1-04
Ct	4.7K-04(2-3)	4.7K-04(2-3)	3.3K-04(1-2)
Cu	2.2K-04	2.2K-04	3.3K-04
Cv	FB120	FB120	FB60
Cw	22K-04(*2)	22K-04(*2)	X
Cx	100u+75	100u+75	10U+32ohm

*

Elitegroup Computer Systems

Title: Audio - CONN/HDR

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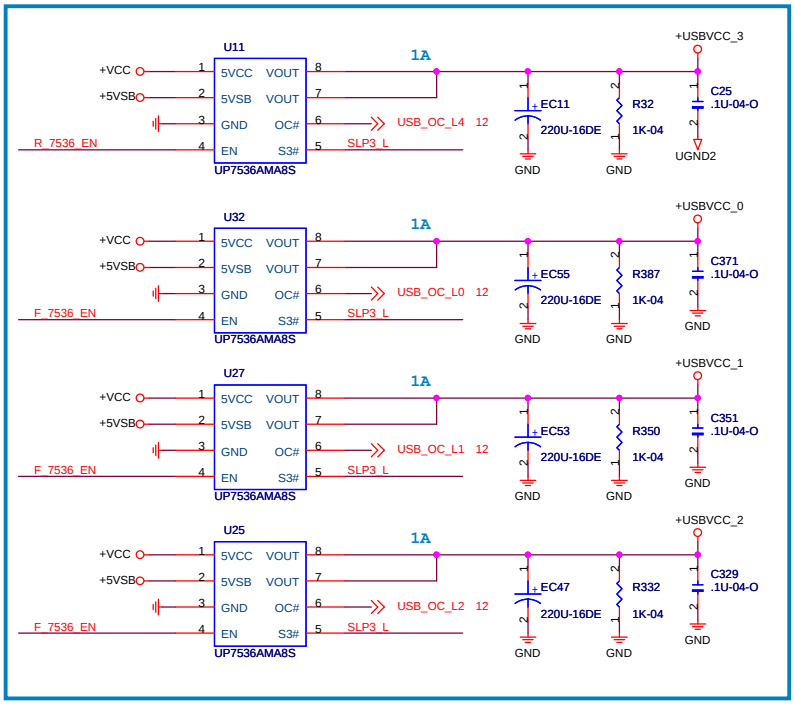
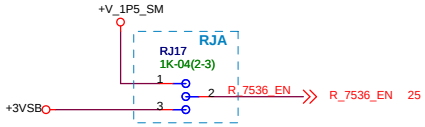
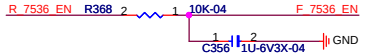


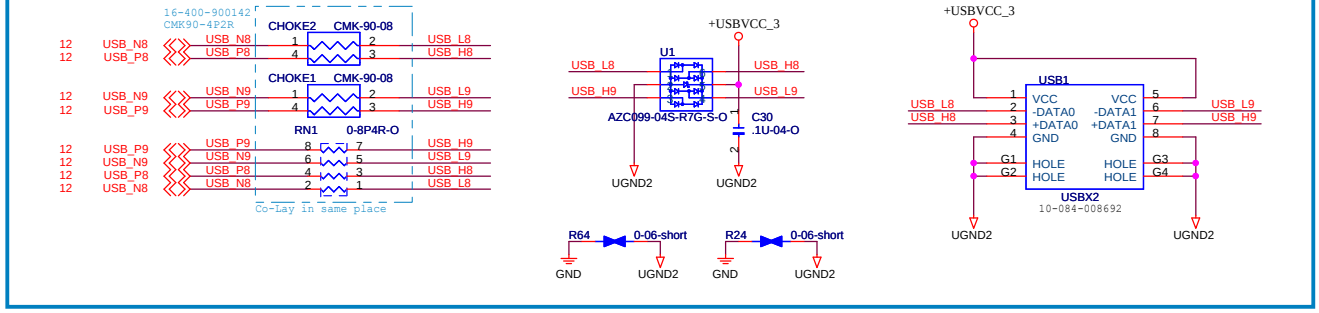
USB POWER CIRCUIT.

5,14,25,29,33,34,35 SLP3_L SLP3_L

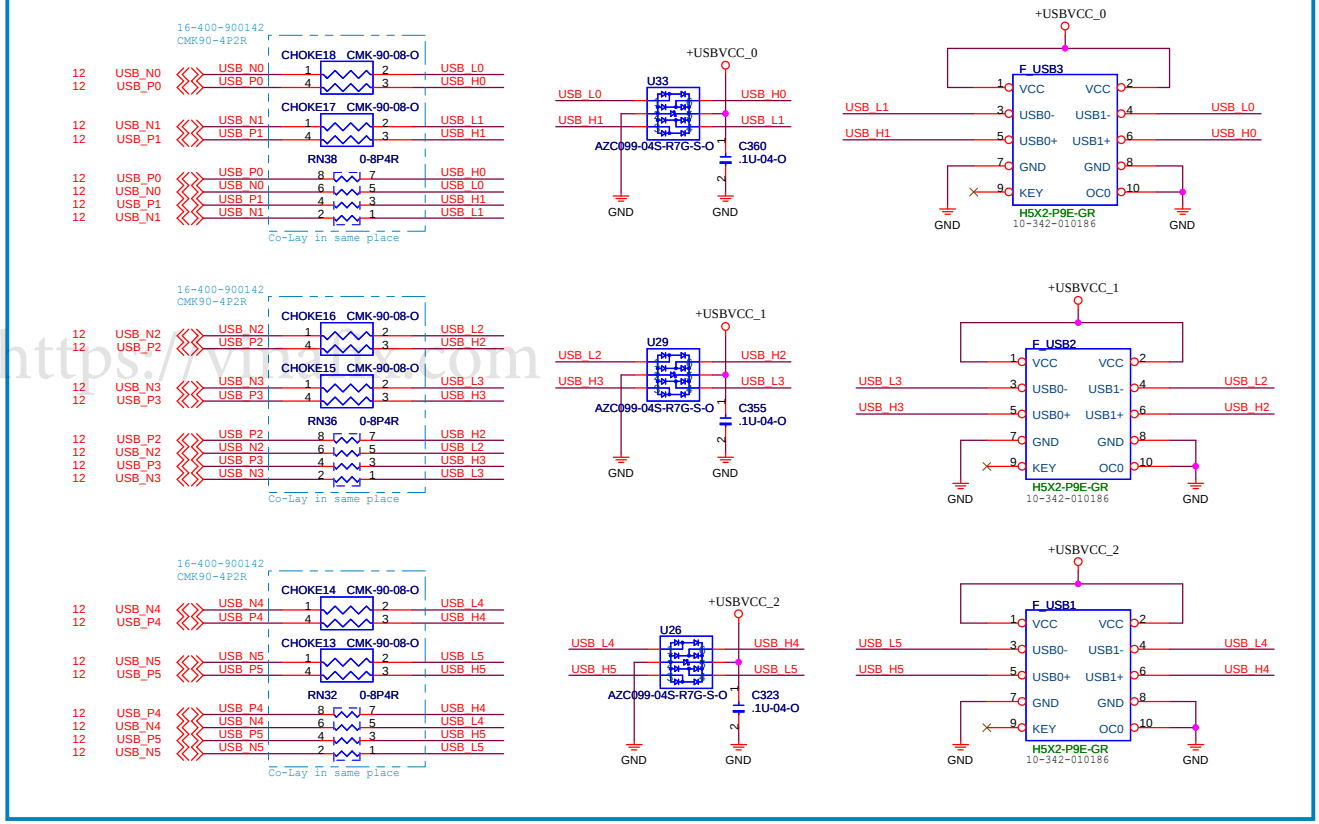




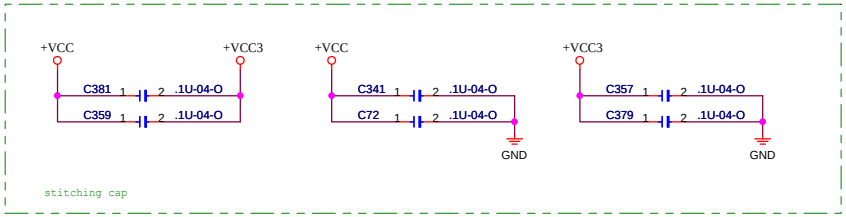
uP7536 Enable use	RJA	S4/S5 USB_5V_DUAL	Customer
VDIMM	0ohm (1-2)	0 Volt	FDR: may be reserved TF: W/USB_5V_DUAL S4/S5 W/USB_5V_DUAL
* +3VSB	1K (2-3)	5 Volt	



REAR SIDE 2 PORTS ON SINGLE USB CONN.



FRONT SIDE 6 PORTS on USB Header



Elitegroup Computer Systems

Title: USB - PWR/CONN/HDR

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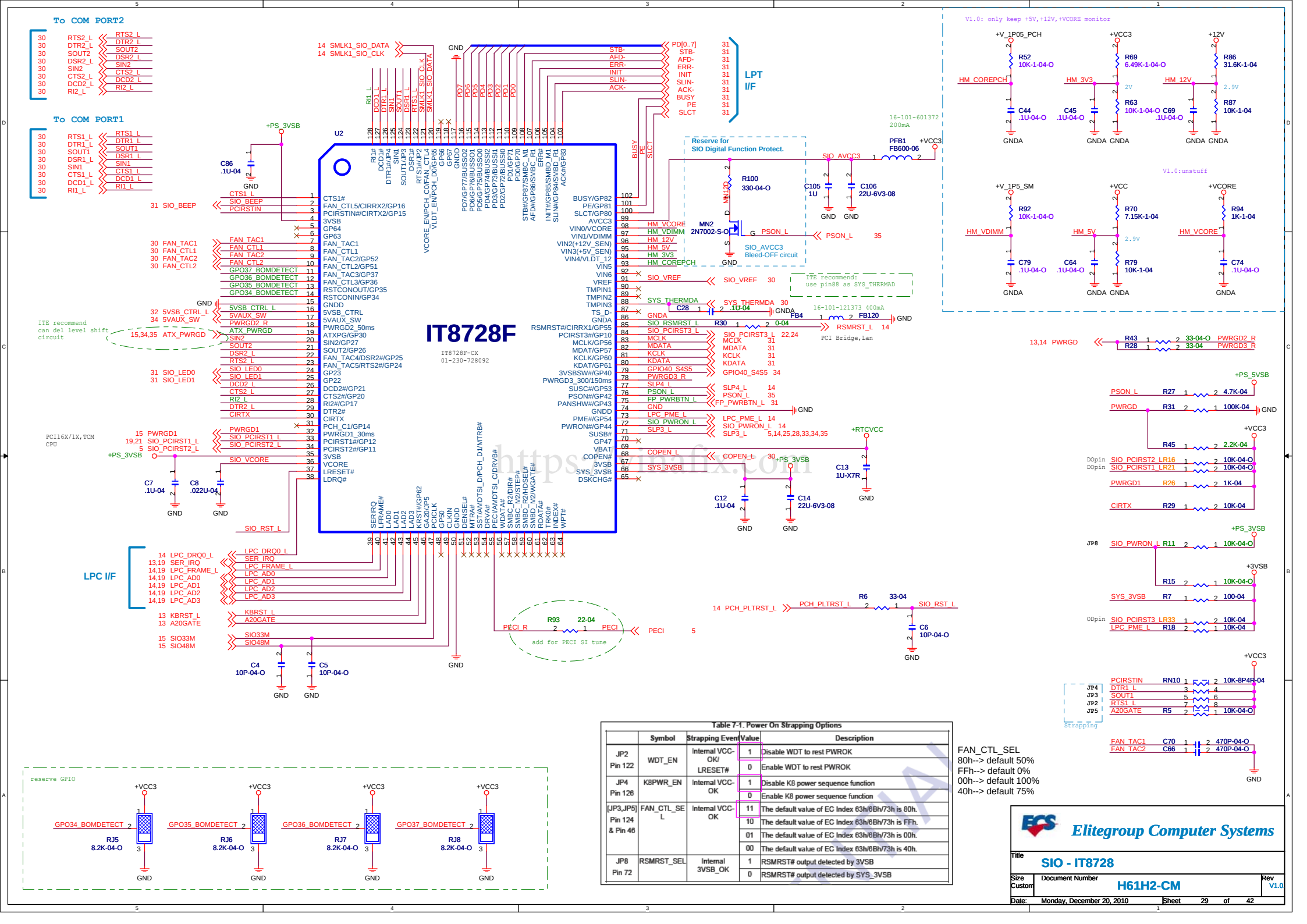
To COM PORT2
To COM PORT1
IT8728F
IT8728F-CX
01-230-728092
U2
LPT I/F
LPC I/F
Reserve for SIO Digital Function Protect.
SIO_AVCC3 Bleed-OFF circuit
ITE recommend: use pin88 as SYS_THERMAD
ITE recommend can del level shift circuit
PCI16X/1X,TCM CPU
add for PECI SI tune
reserve GPIO
V1.0: only keep +5V,+12V,+VCORE monitor
V1.0:unstuff
Strapping
FAN_CTL_SEL
80h--> default 50%
FFh--> default 0%
00h--> default 100%
40h--> default 75%
Table 7-1. Power On Strapping Options
Elitegroup Computer Systems
SIO - IT8728
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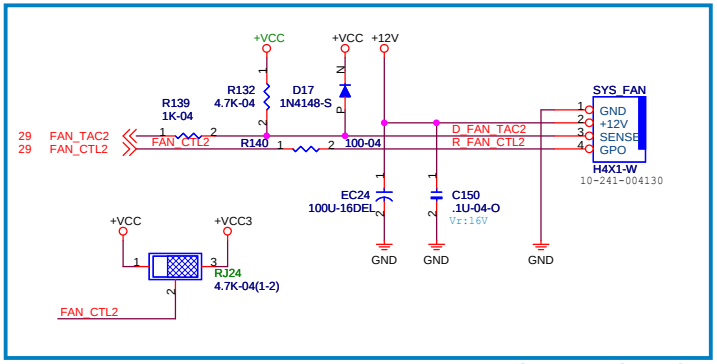
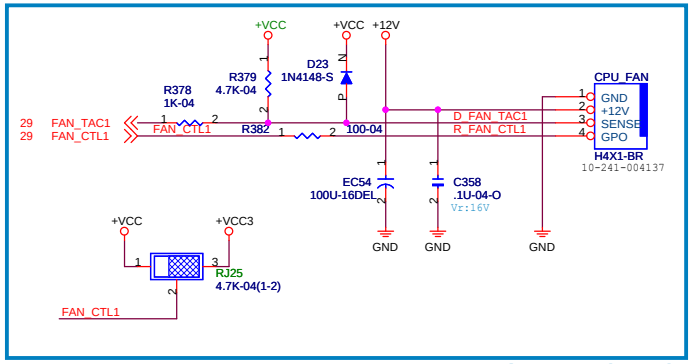
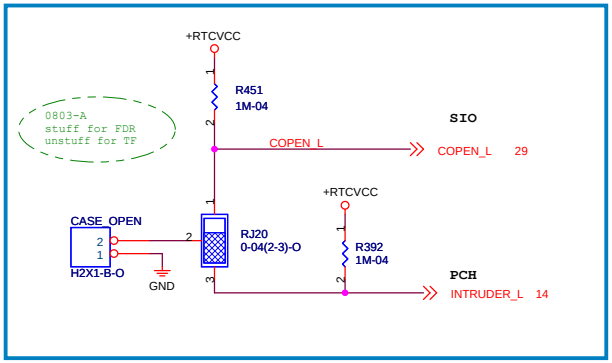


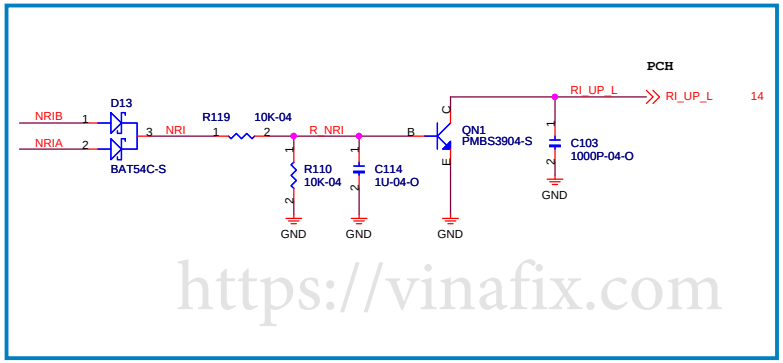
SYS FAN 4-PIN Circuit



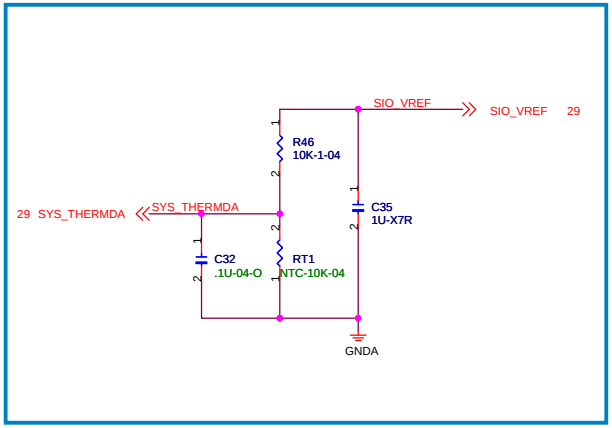
CPU FAN 4-PIN Circuit



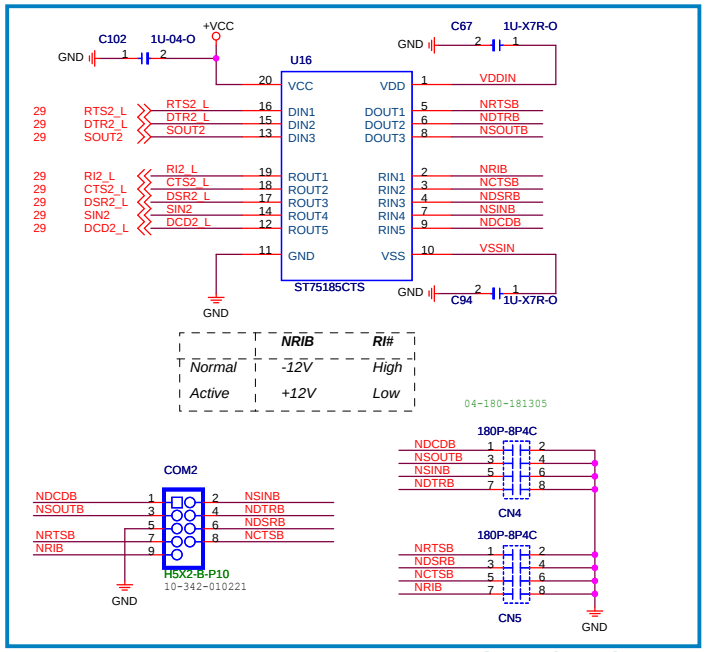
CASE Open Circuit



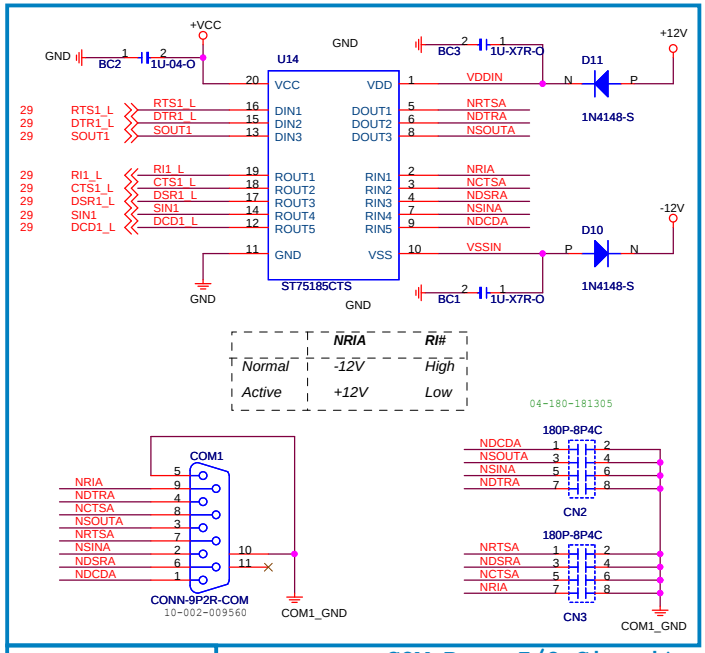
COM RI# Wake Up Circuit



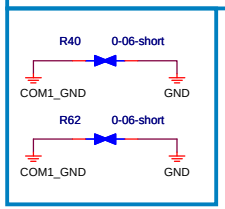
Thermal Sense



COM Header Circuit



COM Rear I/O Circuit



Elitegroup Computer Systems

Title: FAN, COM, CASE_OPEN, THERM

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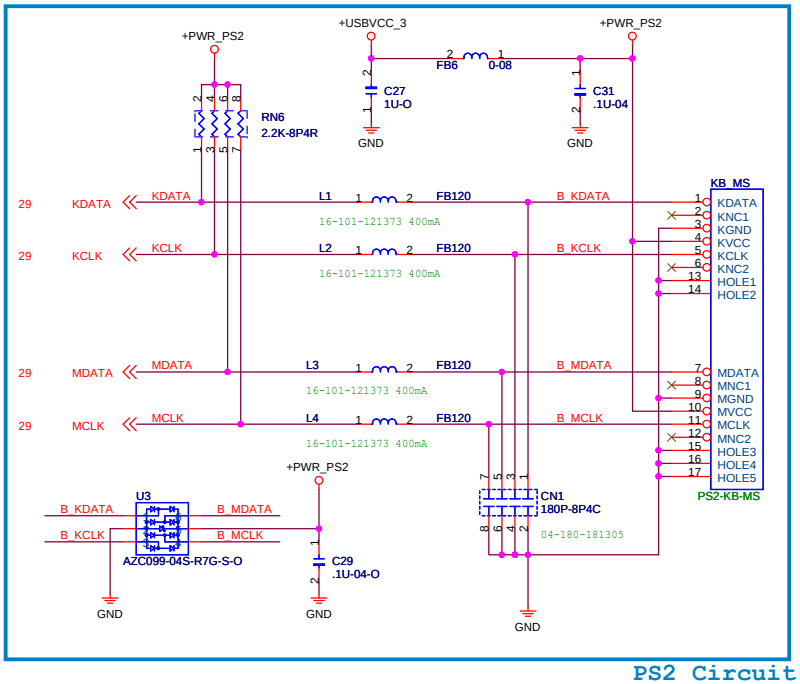
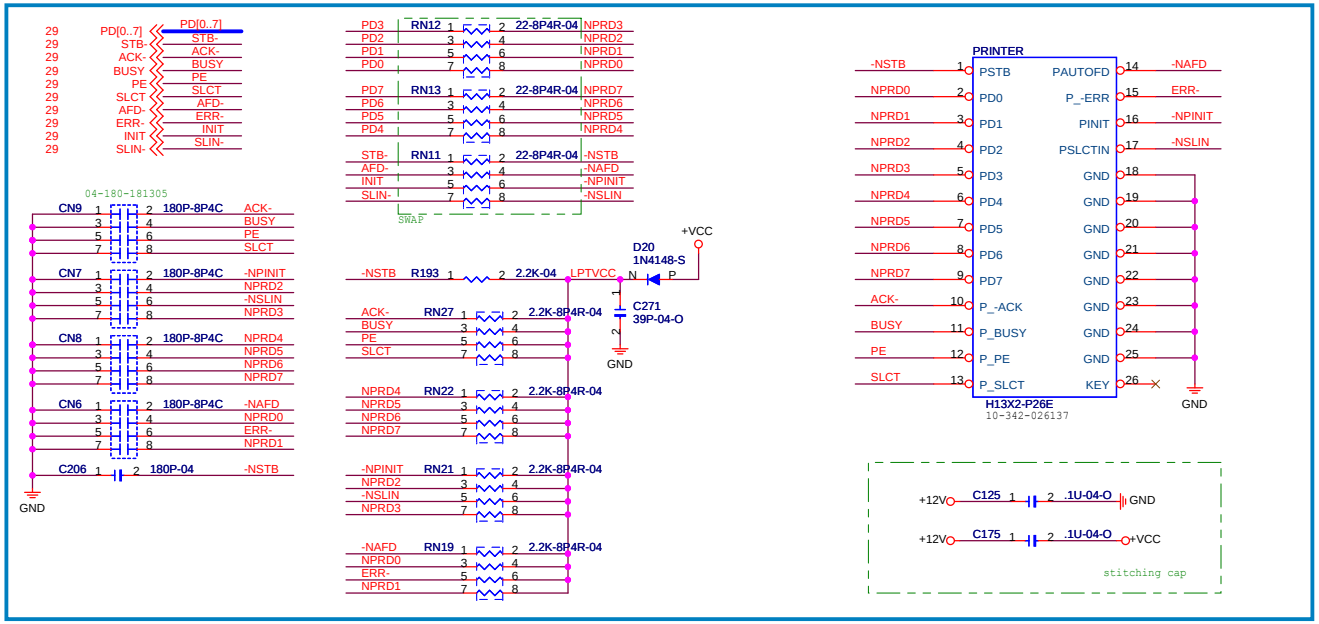
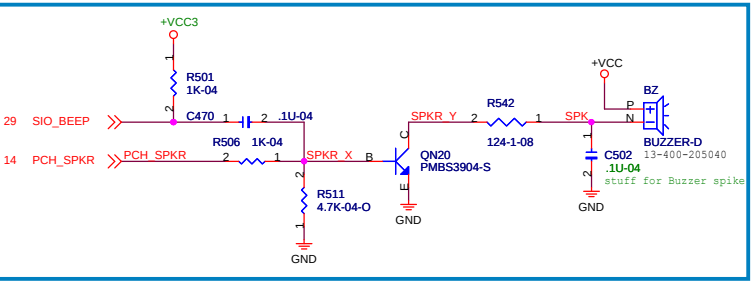


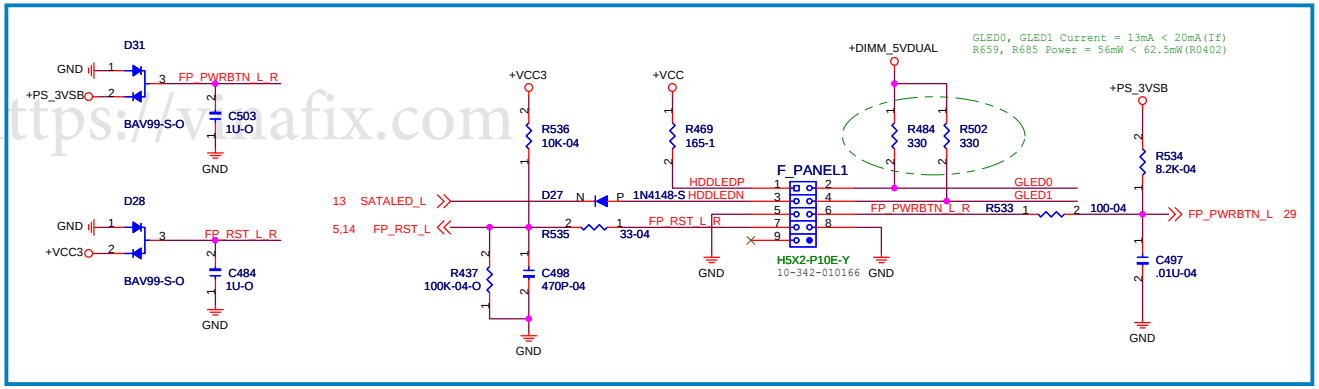
PS2 Circuit



LPT Header Circuit



Buzzer Circuit

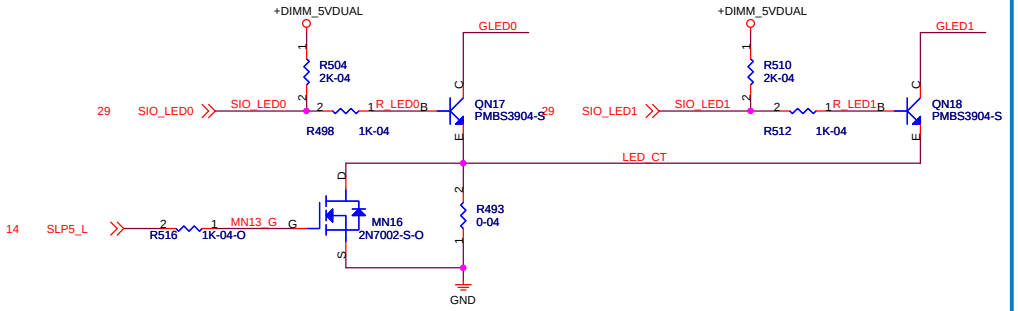


Front Panel Circuit

China-one PWR_LED SPEC

SYSTEM STATUS	SIGNAL-PWR_LED
NORMAL	STEADY_GREEN
S1	GREEN_BLINKING
S3,S4,S5	OFF

Intel GLED0 G GLED1



Front LED

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Elitegroup Computer Systems

Title	F_PANEL, BUZ, PS2, LPT	
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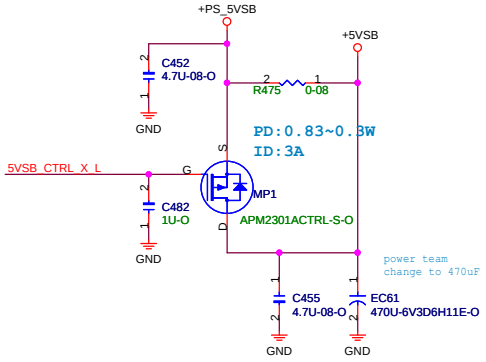
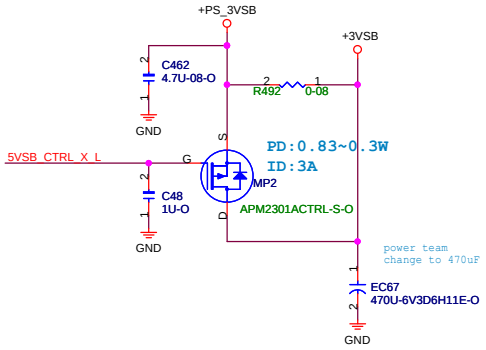
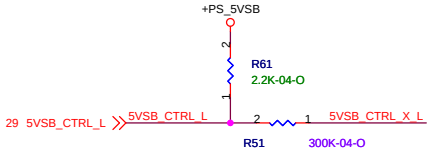
EuP Lot6 Power Saving Circuit







add R51 to Fix EUP enable STBY drop

V1.0:因1M會跟MOS內阻分壓導致5VSB_CTRL_X_L位準偏低造成漏電。

Layout Note:
Close to ATX 24P2R Connector.

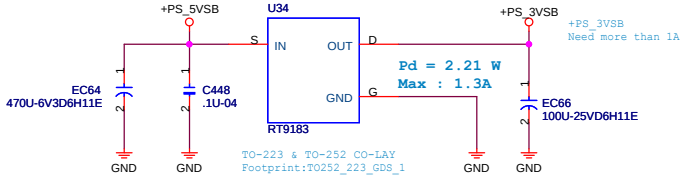
EuP Lot6 2013 0.5W:

PWR STATE	+5VSB Source
S0	+PS_5VSB
S3	+PS_5VSB
S4	OFF
S5	OFF

*** China one Enery Saving Spec**

Customer	S3	S5
TF	< 0.4A	< 0.18A
FDR	< 0.3A	< 0.15A

+3VSB Circuit



★ 02-347-183840: 0.74W
IC REG.RT9183-33GGF..SOT-223(F-TYPE).
3.3V.1.5A.....LEAD-FREE(RoHS/HF).RICHTEK
XX-XXX-XXXXXX: 1.333W
RT9183-33GLF TO-252

3VSB Non-EuP Lot6 Mode:

Power Name	Current
4 Slots	0.375 X4 = 1.5A
LAN	16m + 49m = 65mA
PCH	123mA
TPM(WPCT210)	50mA
EPW	16mA
SPI	mA
SIO	mA
Total Current	+ 1.754 A

Del PCH_MEPWROK Circuit

del 3VDual ,VCC3_EPW control

Elitegroup Computer Systems

Title	DC/DC 3VDUAL,EUP	
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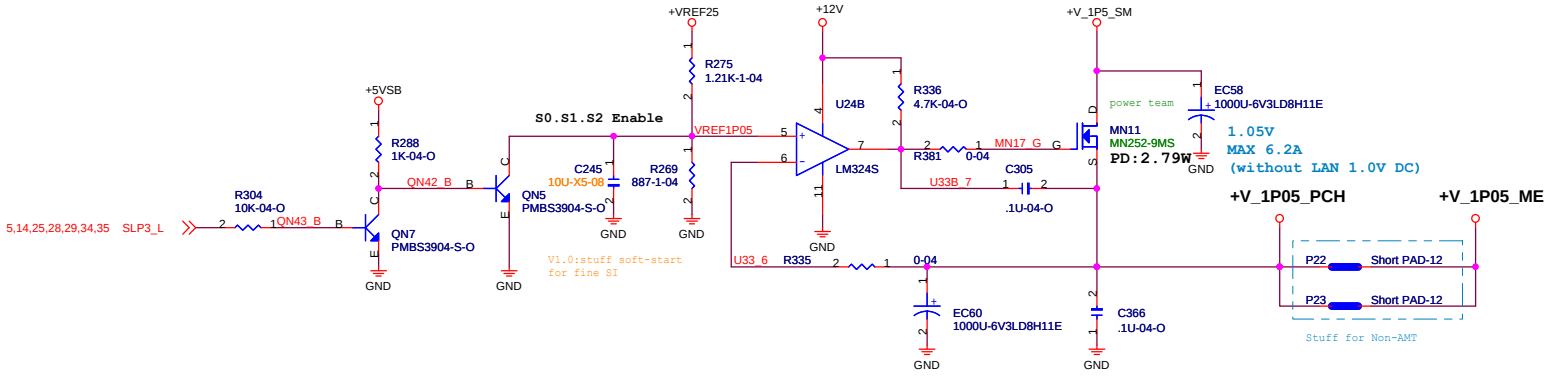
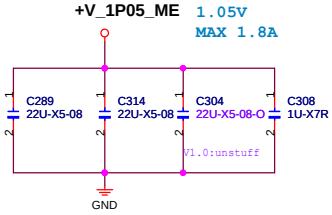
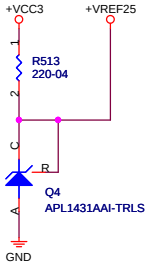
V1P05_PCH

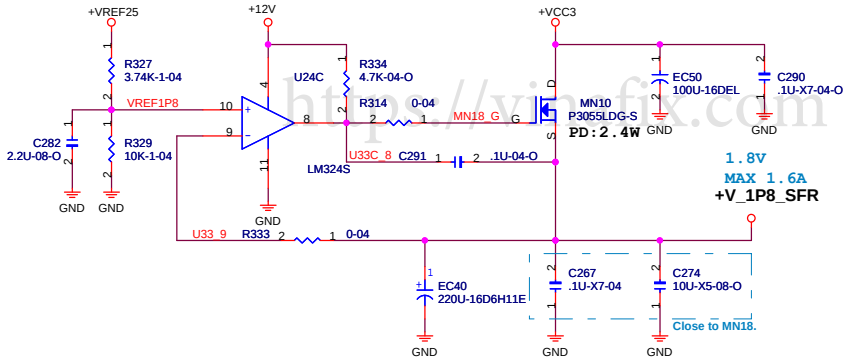


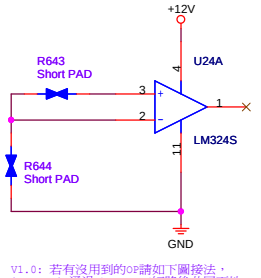


VREF25



V1P8_SFR(1.5A max)





del 1.05V ME power

V1P05_ME

Elitegroup Computer Systems

Title	DC/DC V1P05_PCH,ME/V1P8_SFR	
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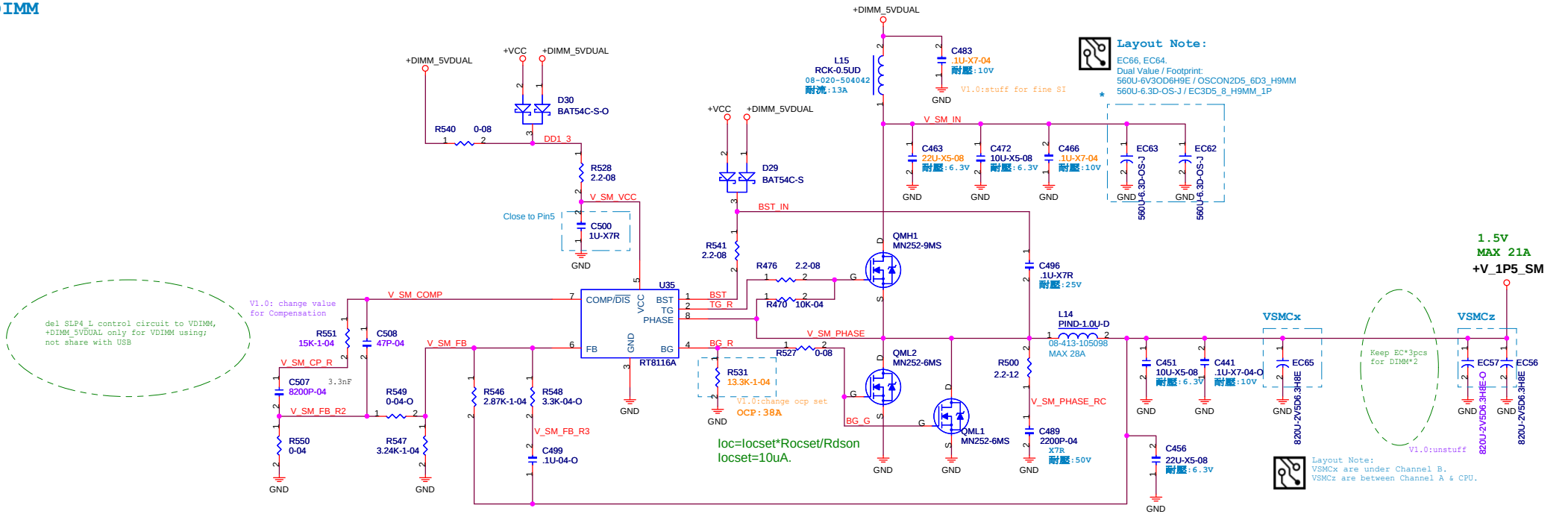
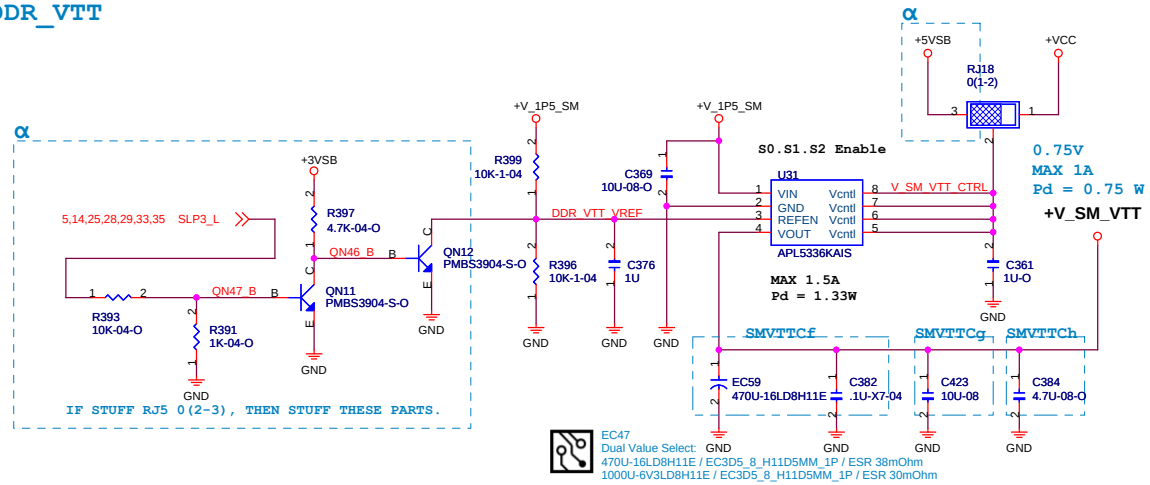
VDIMM

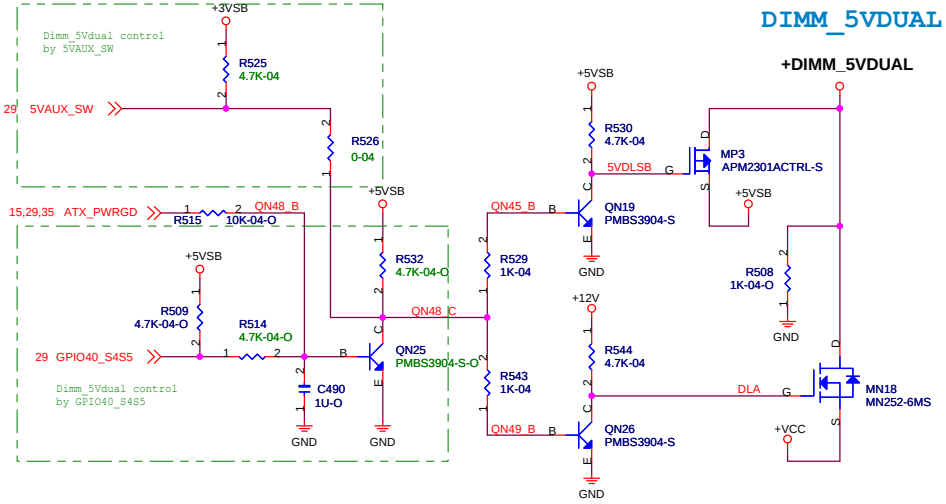


DDR_VTT



Layout Note:
SMVTTCf close to U39 Pin4.
SMVTTCg are between Channel A & B.
SMVTTCh are between Channel A & CPU.

DIMM_5VDUAL



*		S5	S0	S3
	5VAUX_SW	0	0	1
	GPIO40_S4S5	1	1	0
	+DIMM_5VDUAL	0	VCC	+5VSB

Elitegroup Computer Systems

Title: DC/DC VDIMM/DDR_VTT/5VDUAL

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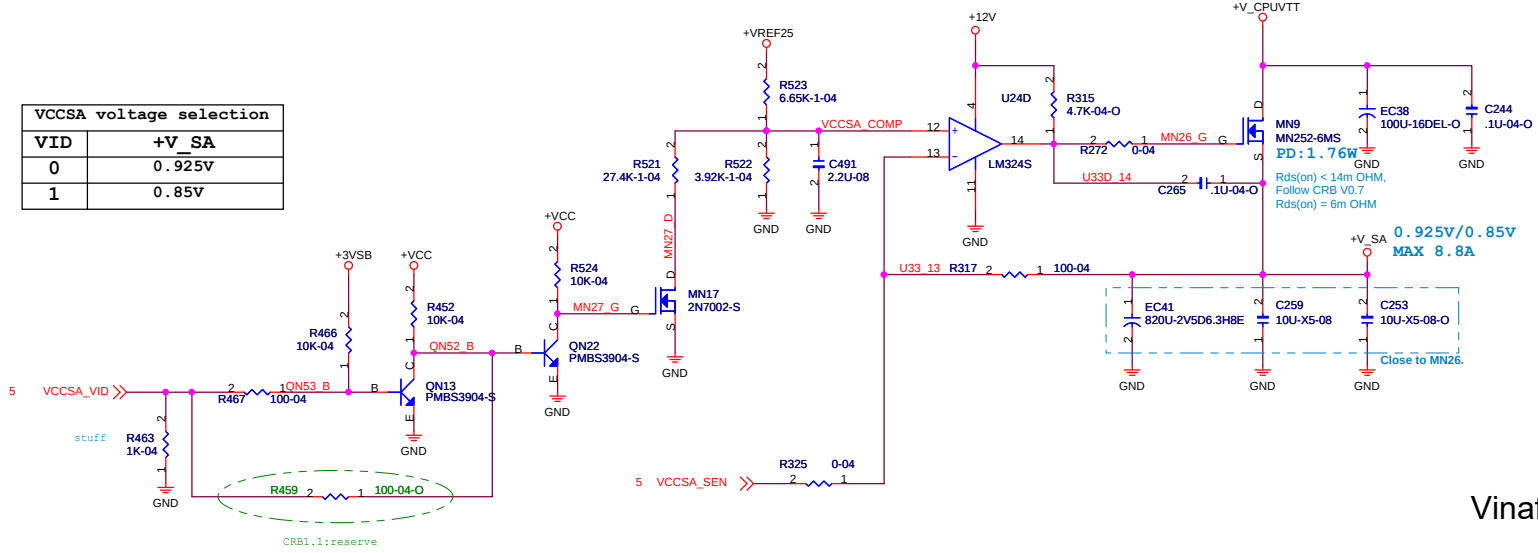
+V_SA

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

*



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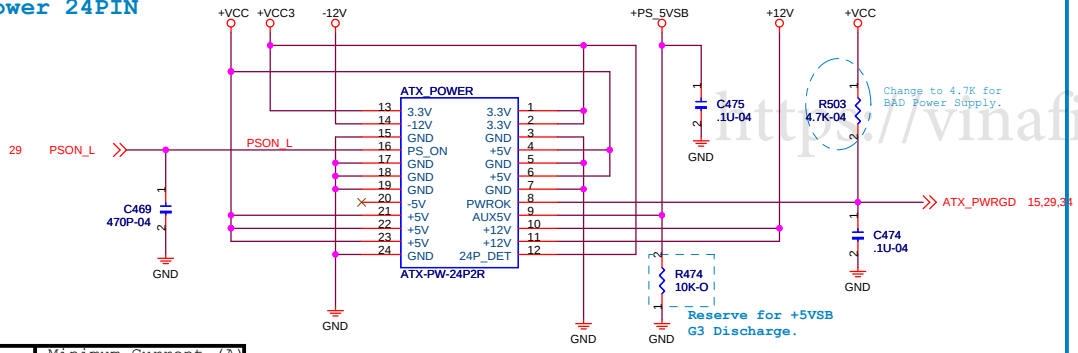
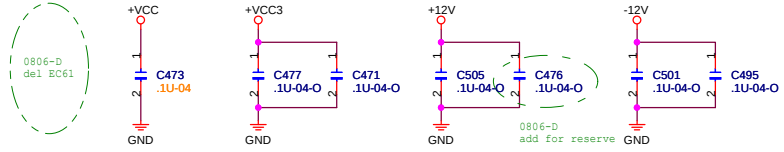
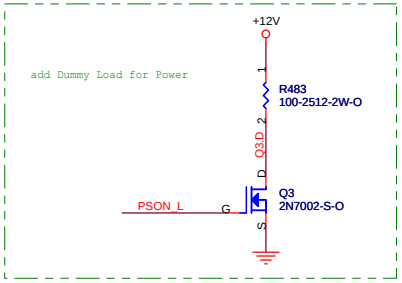
ATX Power 24PIN

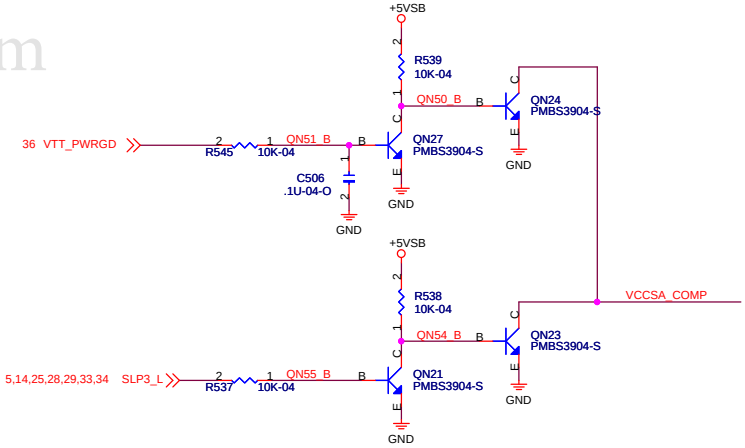


OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0





VCCSA Sequence



Elitegroup Computer Systems

Title: DC/DC VCCSA, ATXPWR

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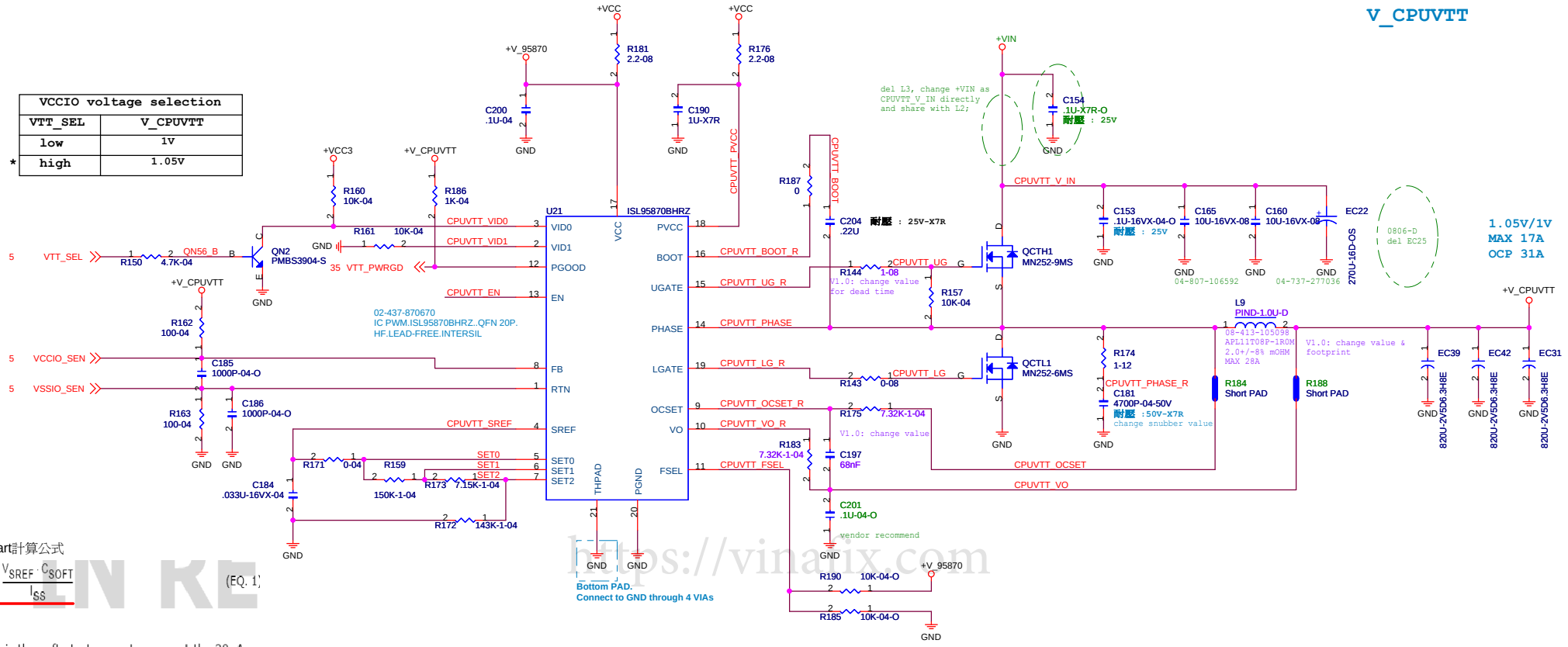
V_CPUVTT

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
* high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad \text{(EQ. 1)}$$

Where:

- I_{SS} is the soft-start current source at the 20µA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V_{SREF}	V_{OUT}
1	1	SW0	V_{SET1}	V_{OUT1}
1	0	SW1	V_{SET2}	V_{OUT2}
0	1	SW2	V_{SET3}	V_{OUT3}
0	0	SW3	V_{SET4}	V_{OUT4}

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad \text{(EQ. 21)}$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 22)}$$

The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 23)}$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \quad \text{(EQ. 24)}$$

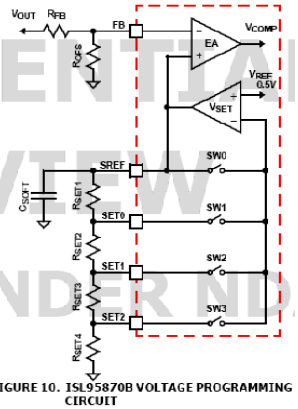
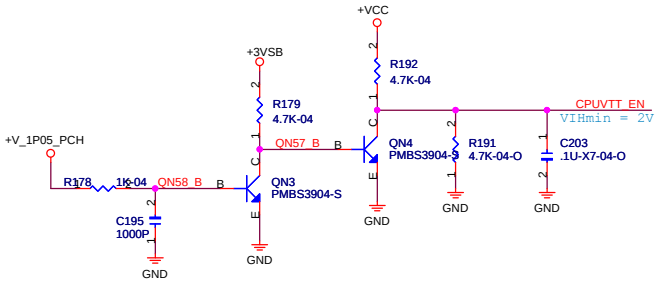


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT

Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC



Elitegroup Computer Systems

Title	DC/DC V_CPUVTT	
Size: Custom	Document Number: H61H2-CM	Rev: V1.0
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V1.0:change PWM IC

0608_DEL_SVID_DEBUG_PORT

02-437-364670
IC PWM ISL6364CRZ_QFN 48P.
HF LEAD-FREE INTERSIL

U37 ISL6364CRZ

In VR12 SPEC,
Serial VID includes IMON Data.

Bottom PAD.
Connect to GND through 8 VIAs

V1.0:change for IMON & IMOS
FS_DRP & FS_DRPS RSET
SICI

V1.0:change for FBS & HFCOMPS/DVCS COMPS

V1.0:change for R-C Mach Vcore & Vaxg RISEN CT

0623 ADD

Stuff for Disable PWM4.

Vendor:L/DCR=R*C , 0.3/0.65=0.1*R, R*1.25=5.76K

For VR_READY Power On Sequence

Elitegroup Computer Systems			
Title: DC/DC VCORE/VAXG1			
Size: Custom	Document Number: H61H2-CM		Rev: V1.0
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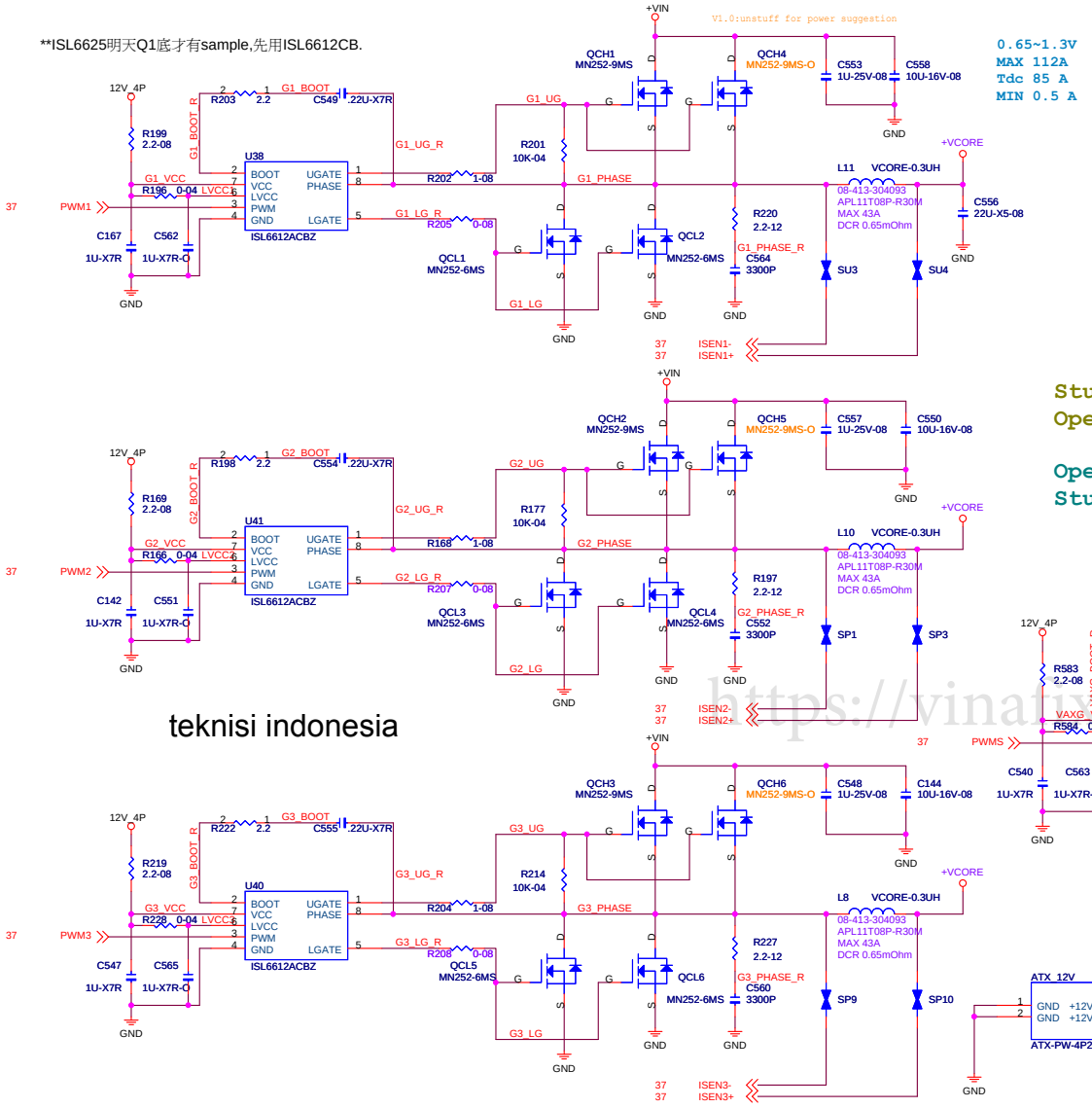
V1.0:change PWM IC

**ISL6625明天Q1底才有sample,先用ISL6612CB.



0.65~1.3V
MAX 112A
Tdc 85 A
MIN 0.5 A

Stuff for ISL6612,
Open for ISL6625.

Open for ISL6612,
Stuff for ISL6625.

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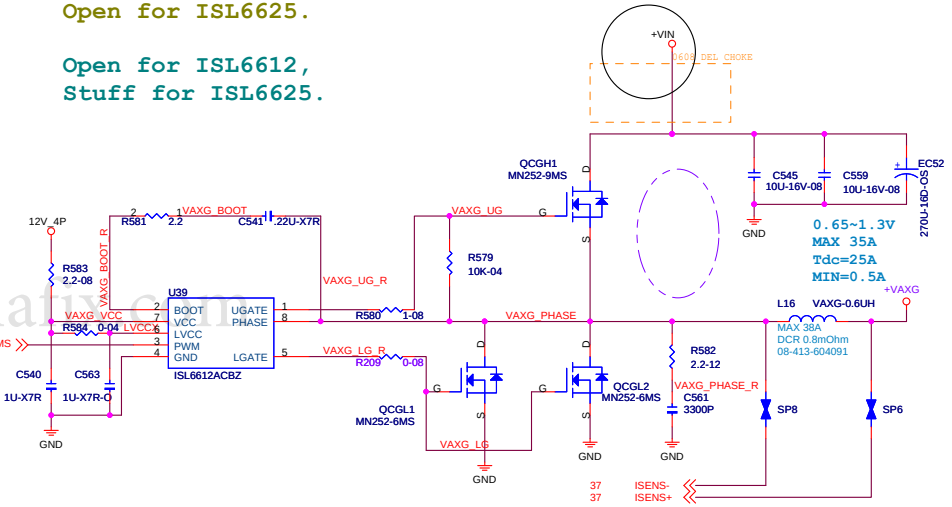

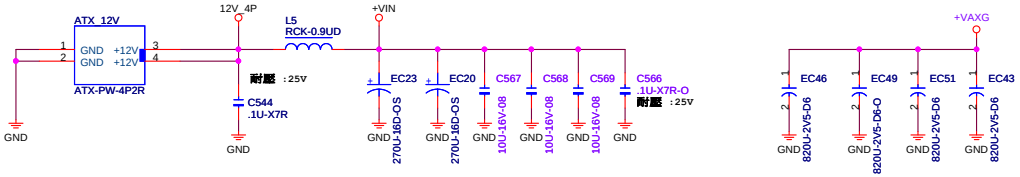

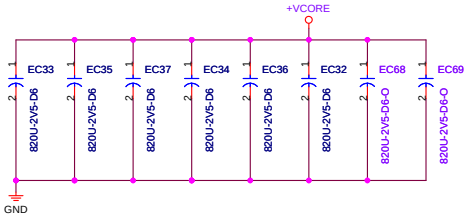

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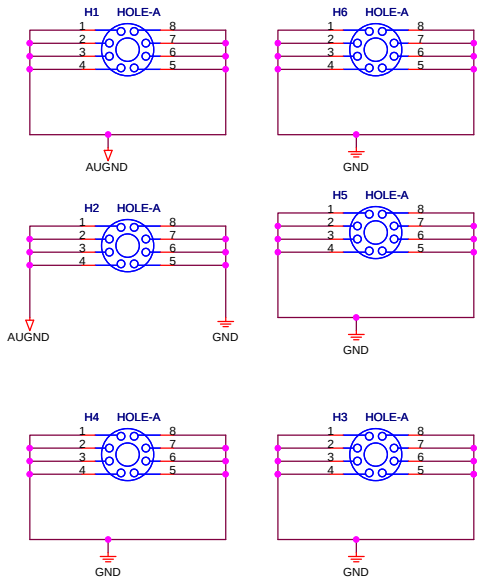
PCH Strap Pin

Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down，No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up，intend for Firmware Hub.
GNT[3]#/GPIO[55]	Disable Top-Block Swap	20K internal pull-up，“topblock swap” mode Disable
INTVRMEN	Enable Integrated 1.05V VRM	Need External Pull-up，Integrated 1.05V VRM Enable
GNT1# /GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up，The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	20K internal pull-up，The default flash selection is the SPI flash.All
HDA_SDO	Flash Descriptor Security Override/ ME	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
DF_TVS	Enable DMI termination voltage	This signal has a weak internal pull-down.
GPIO28	Eable On-Die PLL Voltage Regulator	The On-Die PLL voltage regulator is enabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Enable TLS Confidentiality	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

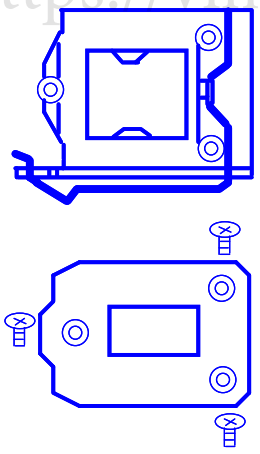
Table 7-1. Power On Strapping Options

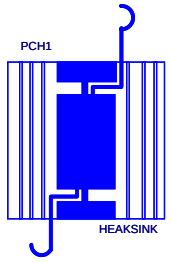
	Symbol	Strapping Event	Value	Description
JP2 Pin 122	Flashseg1_EN	Internal VCC-OK/ LRESET#	1	Disable
			0	Enable Flash I/F Address Segment FFF8_0000 ~ FFFF_FFFF & 000E_0000 ~ 000F_FFFF
JP4 Pin 126	K8PWR_EN	Internal VCC-OK	1	Disable K8 power sequence function
			0	Enable K8 power sequence function
[JP3,JP5] Pin 124 & Pin 46	FAN_CTL_SEL	Internal VCC-OK	11	The default value of EC Index 63h/6Bh/73h is 80h.
			10	The default value of EC Index 63h/6Bh/73h is FFh.
			01	The default value of EC Index 63h/6Bh/73h is 00h.
			00	The default value of EC Index 63h/6Bh/73h is 40h.

V1.0.:update hole,del pin9, and use pin1

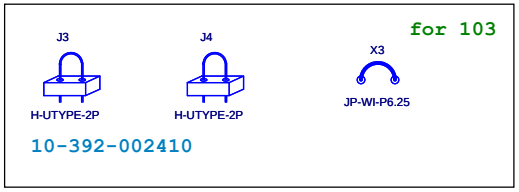


15-Y84-011090 PCB M/B.H61H2-CM.V1.0(.)....244*200*1.6mm.4L..LEAD-FREE.GREEN.OSP.....GE1





20-120-Y84000
20-120-Y84001



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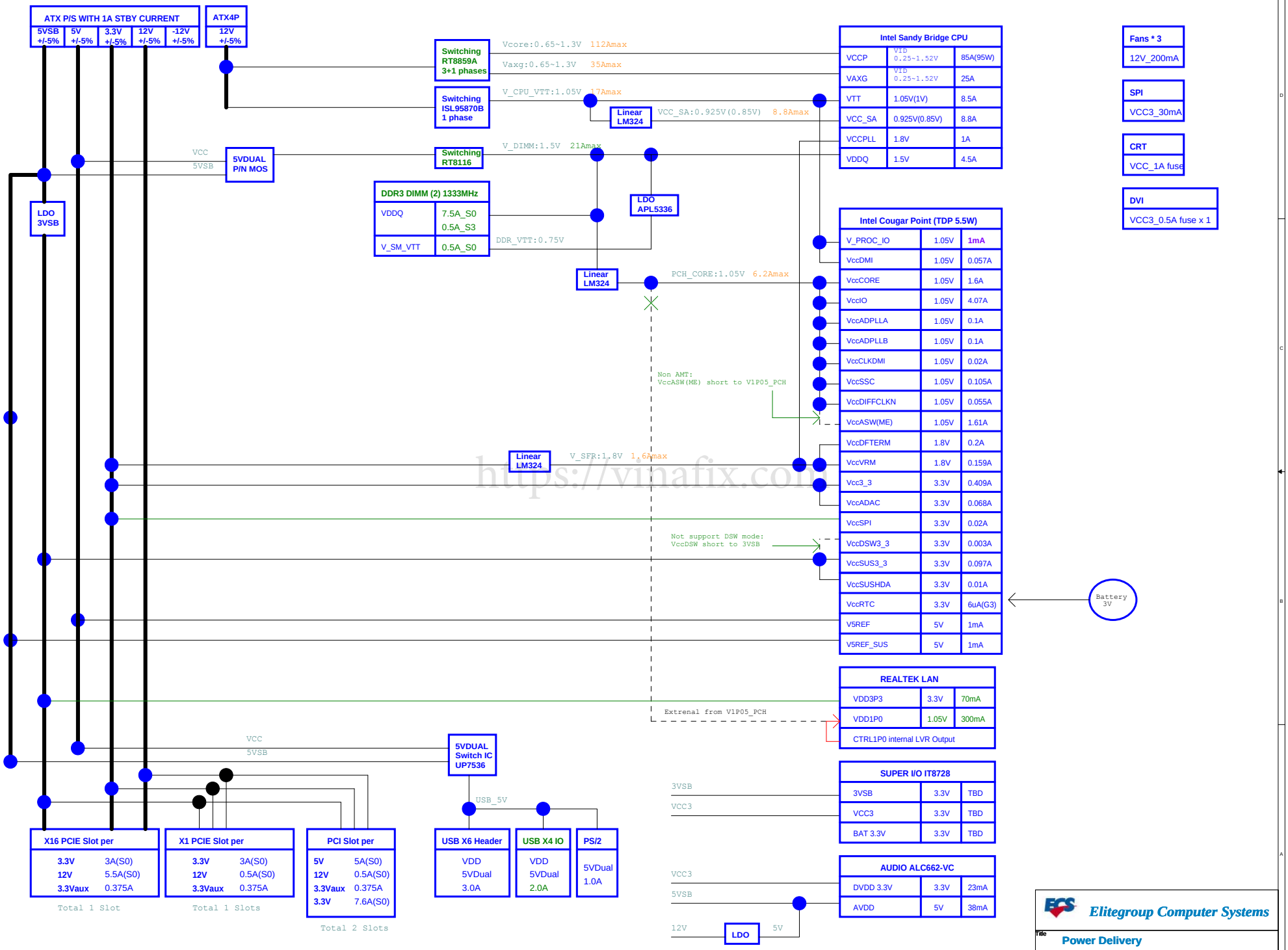
ATX P/S WITH 1A STBY CURRENT
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
-12V +/-5%
ATX4P
12V +/-5%
Switching RT8859A 3+1 phases
Vcore:0.65~1.3V 112Amax
Vaxg:0.65~1.3V 35Amax
Switching ISL95870B 1 phase
V_CPU_VTT:1.05V 17Amax
Linear LM324
VCC_SA:0.925V(0.85V) 8.8Amax
Intel Sandy Bridge CPU
VCCP VID 0.25~1.52V 85A(95W)
VAXG VID 0.25~1.52V 25A
VTT 1.05V(1V) 8.5A
VCC_SA 0.925V(0.85V) 8.8A
VCCPLL 1.8V 1A
VDDQ 1.5V 4.5A
Fans * 3
12V_200mA
SPI
VCC3_30mA
CRT
VCC_1A fuse
DVI
VCC3_0.5A fuse x 1
VCC
5VSB
5VDUAL P/N MOS
Switching RT8116
V_DIMM:1.5V 21Amax
DDR3 DIMM (2) 1333MHz
VDDQ 7.5A_S0 0.5A_S3
V_SM_VTT 0.5A_S0
LDO APL5336
DDR_VTT:0.75V
LDO 3VSB
Linear LM324
PCH_CORE:1.05V 6.2Amax
Intel Cougar Point (TDP 5.5W)
V_PROC_IO 1.05V 1mA
VccDMI 1.05V 0.057A
VccCORE 1.05V 1.6A
VccIO 1.05V 4.07A
VccADPLLA 1.05V 0.1A
VccADPLLB 1.05V 0.1A
VccCLKDMI 1.05V 0.02A
VccSSC 1.05V 0.105A
VccDIFFCLKN 1.05V 0.055A
VccASW(ME) 1.05V 1.61A
VccDFTERM 1.8V 0.2A
VccVRM 1.8V 0.159A
Vcc3_3 3.3V 0.409A
VccADAC 3.3V 0.068A
VccSPI 3.3V 0.02A
VccDSW3_3 3.3V 0.003A
VccSUS3_3 3.3V 0.097A
VccSUSHDA 3.3V 0.01A
VccRTC 3.3V 6uA(G3)
V5REF 5V 1mA
V5REF_SUS 5V 1mA
Non AMT:
VccASW(ME) short to V1P05_PCH
Linear LM324
V_SFR:1.8V 1.6Amax
Not support DSW mode:
VccDSW short to 3VSB
Battery 3V
REALTEK LAN
VDD3P3 3.3V 70mA
VDD1P0 1.05V 300mA
CTRL1P0 internal LVR Output
Extrenal from V1P05_PCH
VCC
5VSB
5VDUAL Switch IC UP7536
USB_5V
SUPER I/O IT8728
3VSB 3.3V TBD
VCC3 3.3V TBD
BAT 3.3V 3.3V TBD
X16 PCIE Slot per
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A
Total 1 Slot
X1 PCIE Slot per
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
Total 1 Slots
PCI Slot per
5V 5A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
3.3V 7.6A(S0)
Total 2 Slots
USB X6 Header
VDD 5VDual 3.0A
USB X4 IO
VDD 5VDual 2.0A
PS/2
5VDual 1.0A
AUDIO ALC662-VC
DVDD 3.3V 3.3V 23mA
AVDD 5V 38mA
VCC3
5VSB
12V
LDO
5V
https://vinafix.com
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Power Delivery
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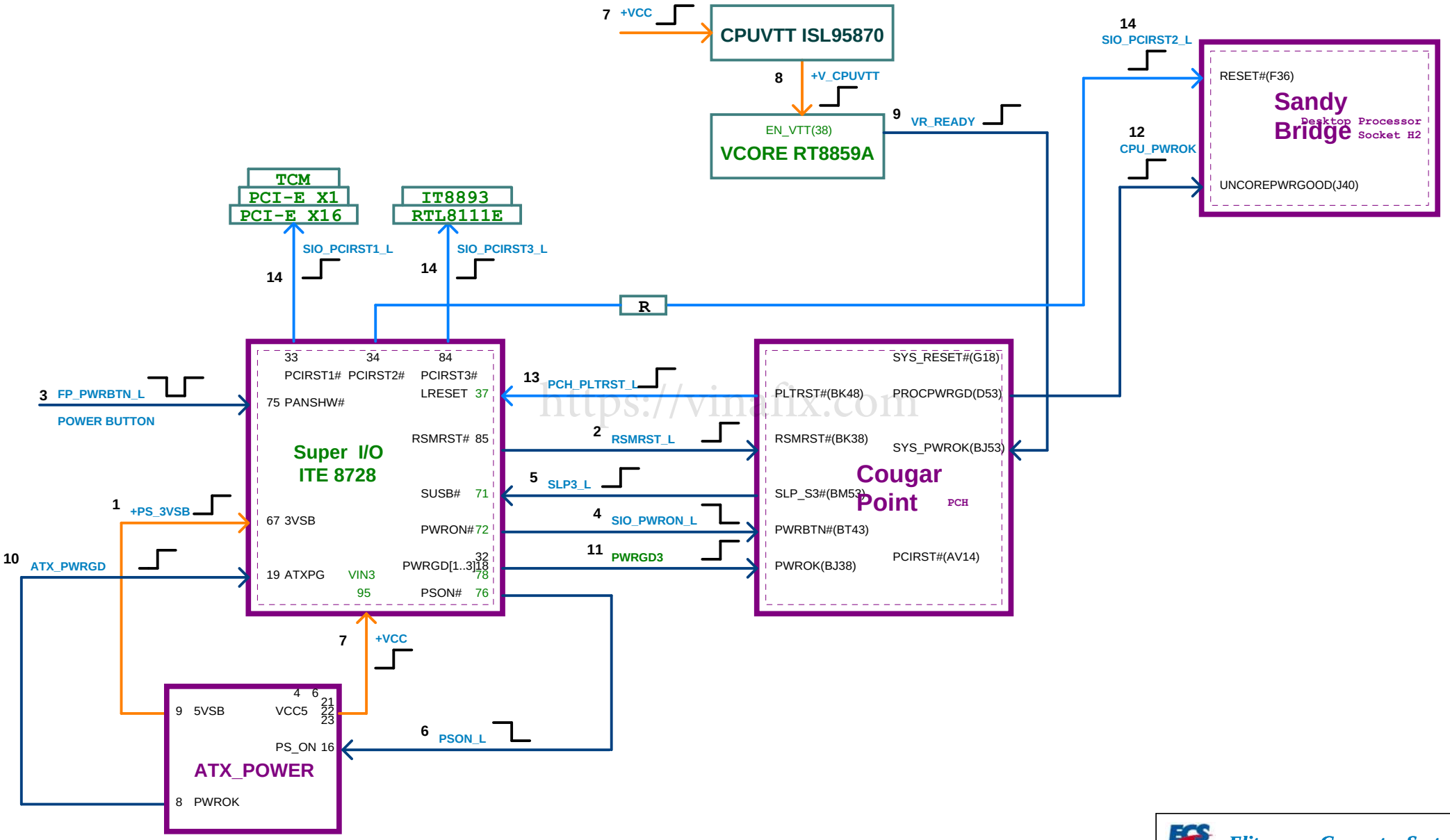

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Title	Power Sequence, Reset Diagram	
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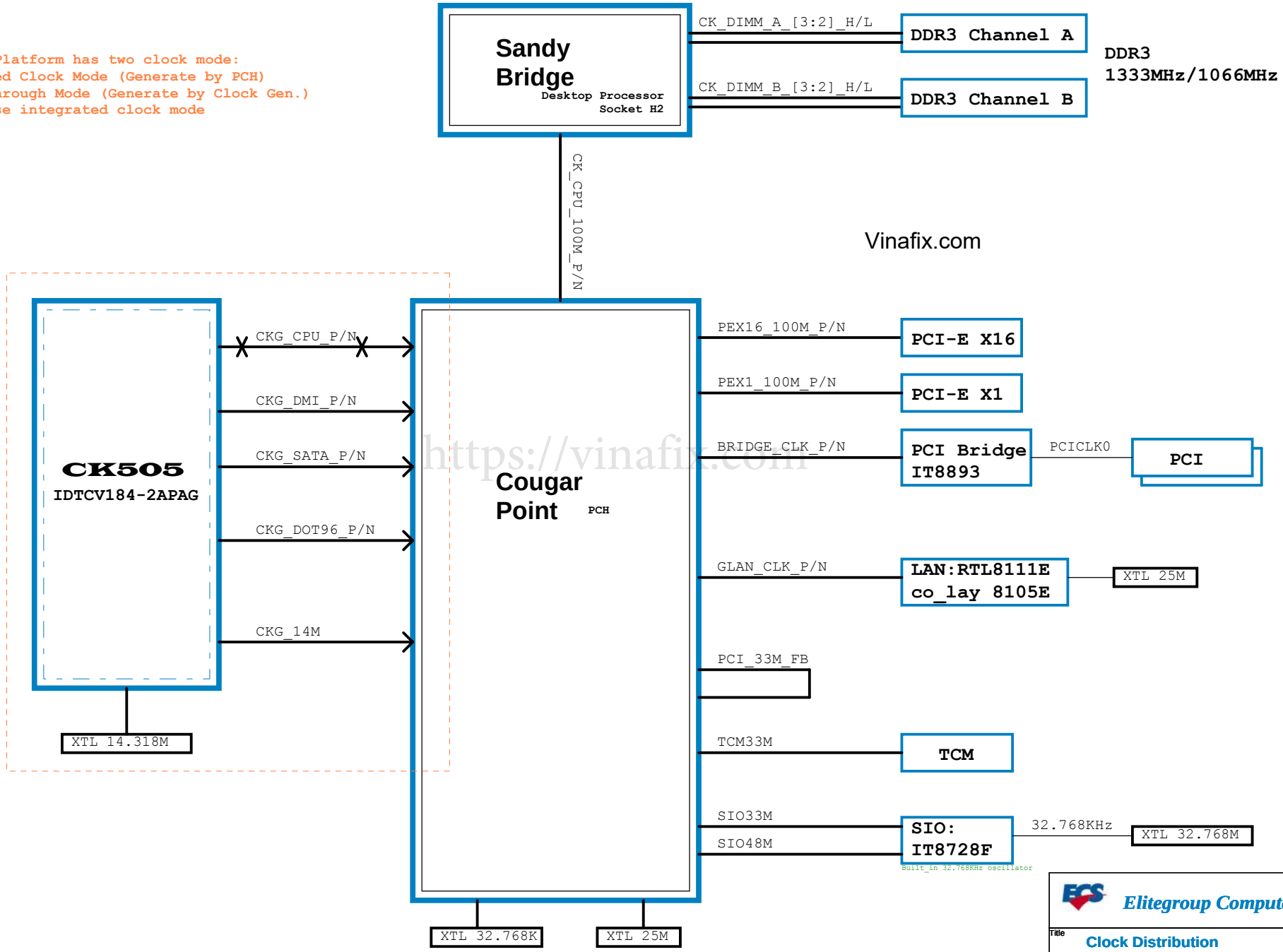
NOTE:

Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
H61H2-CM use integrated clock mode



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Title: Clock Distribution		
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