Cyborg-N/V/L 14/15_TGL-U & Watchmen 14N TGL-U Schematic

2020-08-20
REV : X01

DY : None Installed
UMA: Unified Memory Architecture
OPS: Optimal Playable Settings

CBG X01 N Compare

DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Cover Page***	
Size: A4	Document Number: **Cyborg TGL**	Rev: **SB**
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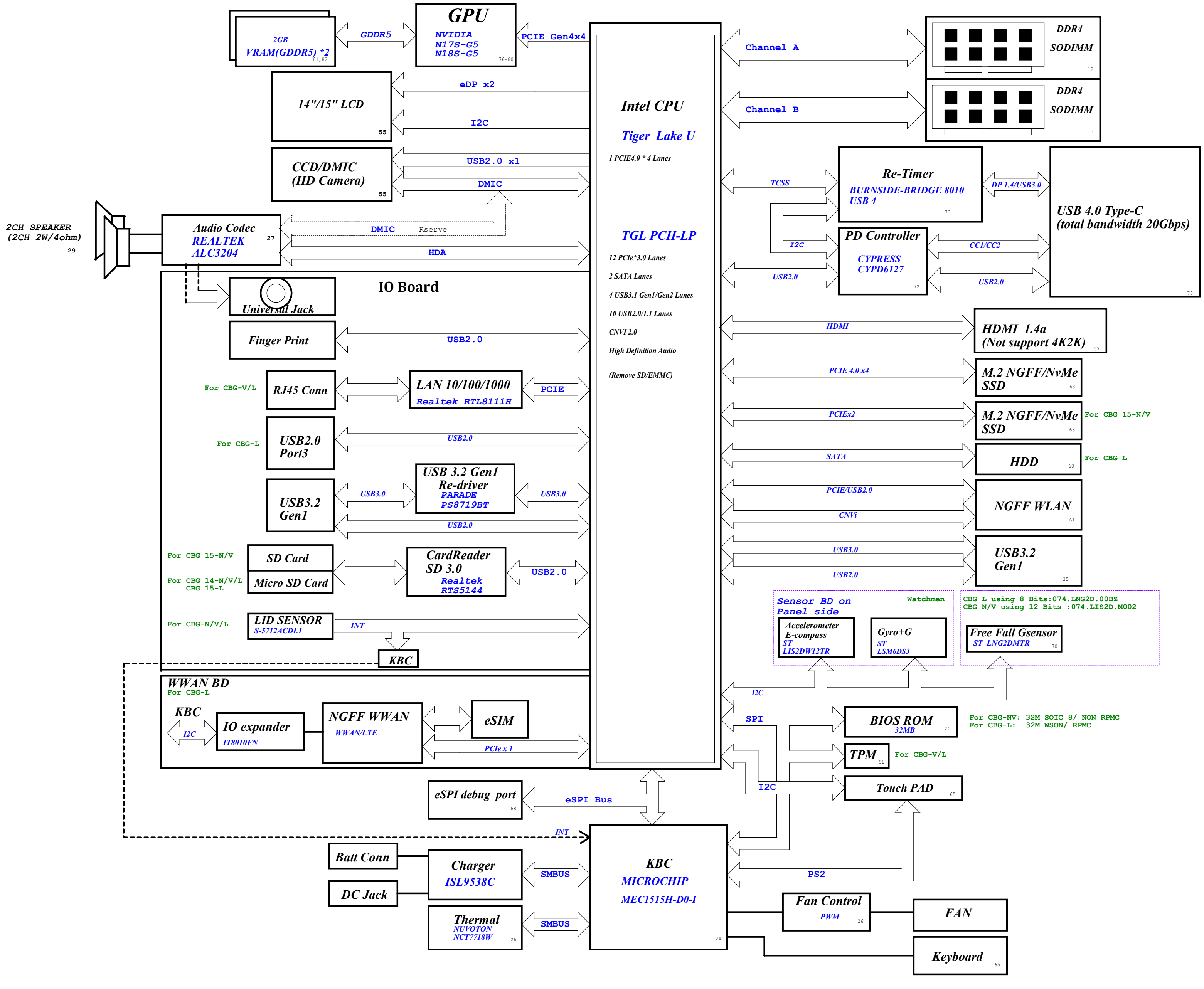
Cyborg N/V/L & Watchmen 14 TGL Block Diagram



CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Block Diagram	
Size: Custom	Document Number: Cyborg TGL	Rev: SB
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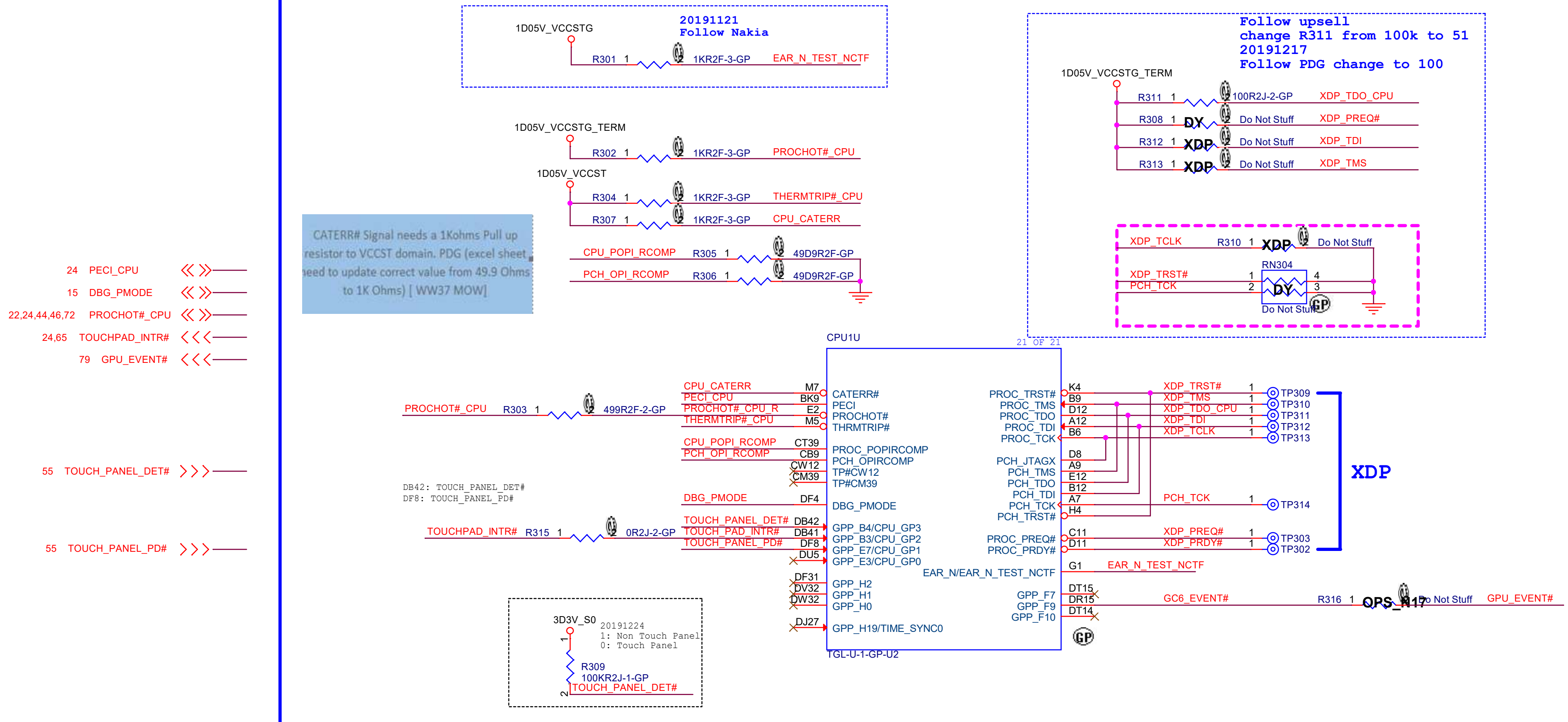

CBG X01 N Compare

Wistron Corporation
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Title	CPU (THML/JTAG)
Size	A3
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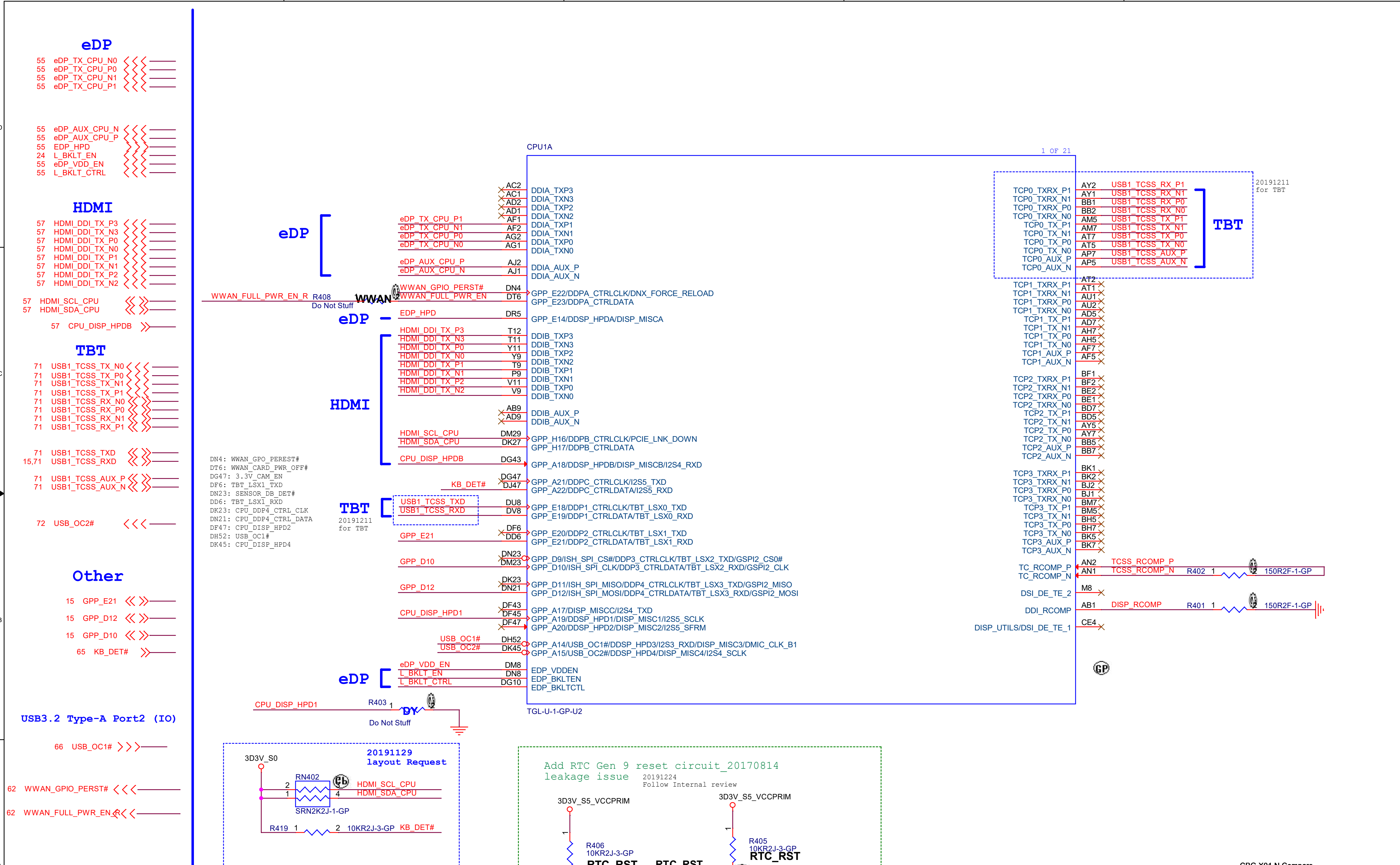

CBG X01 N Compare

Wistron Corporation
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Title: CPU (DDI/EDP/TBT/TPC/)

Size	Document Number	Rev
A3	Cyborg TGL	SB

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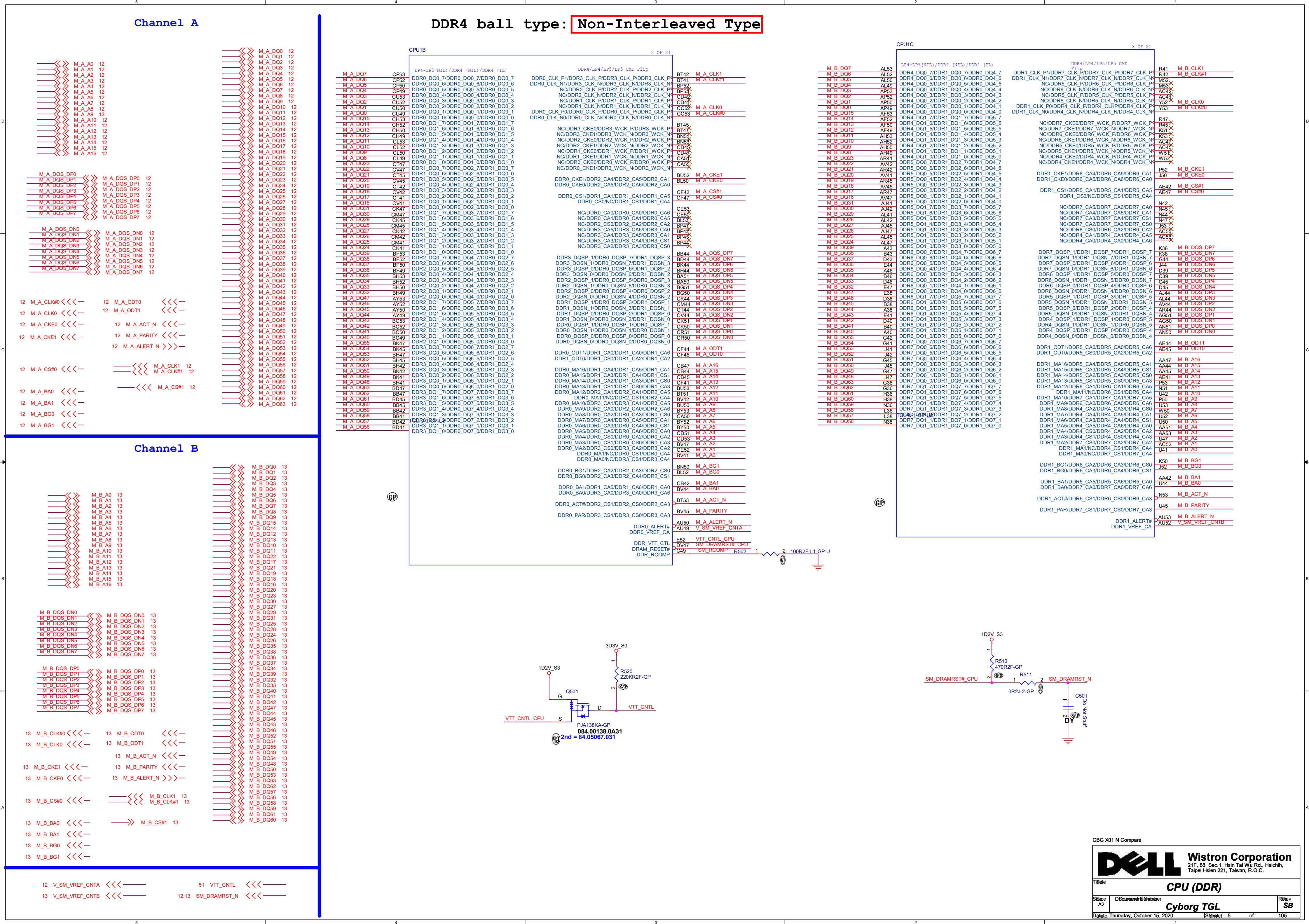

DDR4 ball type: Non-Interleaved Type
Channel A
Channel B
CPU1B
2 OF 21
LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)
DDR4/LP4/LP5/LP5 CMD Flip
CPU1C
3 OF 21
1D2V_S3
3D3V_S0
R520
220KR2F-GP
Q501
PJA138KA-GP
084.00138.0A31
2nd = 84.05067.031
VTT_CNTL_CPU
VTT_CNTL
R502
100R2F-L1-GP-U
R510
470R2F-GP
R511
0R2J-2-GP
SM_DRAMRST#_CPU
SM_DRAMRST_N
C501
Do Not Stuff
DY
12 V_SM_VREF_CNTA
13 V_SM_VREF_CNTB
51 VTT_CNTL
12,13 SM_DRAMRST_N
CBG X01 N Compare
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (DDR)
Size A2
Document Number
Cyborg TGL
Rev SB
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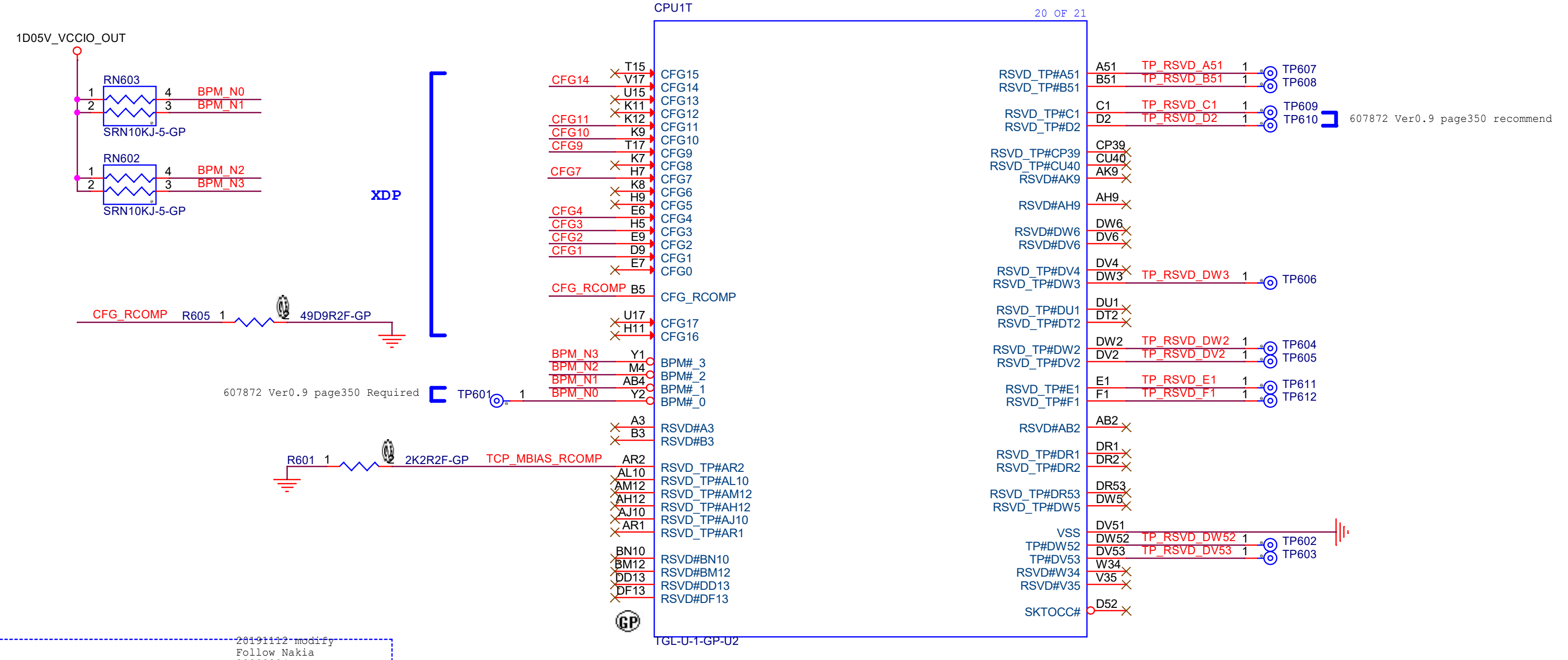

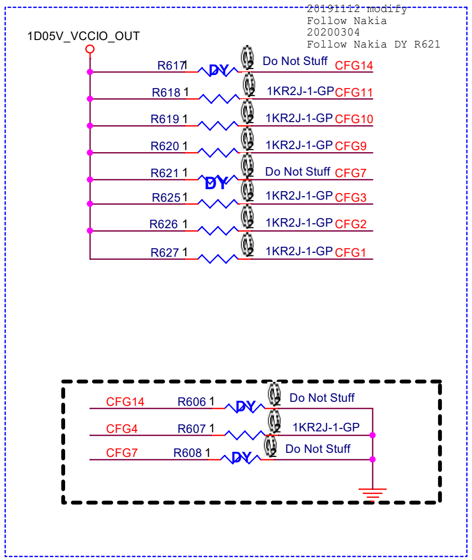

607872 Ver0.9 page350 Required

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull-up to VCCSTG	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

Bifurcation	Link Width	CFG Signals	Lanes			
	0:6:0	CFG [14]	0	1	2	3
1x4	x4	0	0	1	2	3
1x4 **Reversed**	x4	1	3	2	1	0

Notes:
1. PCIe* Port60 is a single x4 port without bifurcation capabilities, thus bifurcation pin straps are not applicable.

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Title	CPU (CFG/IST)	
Size A3	Document Number Cyborg TGL	Rev SB
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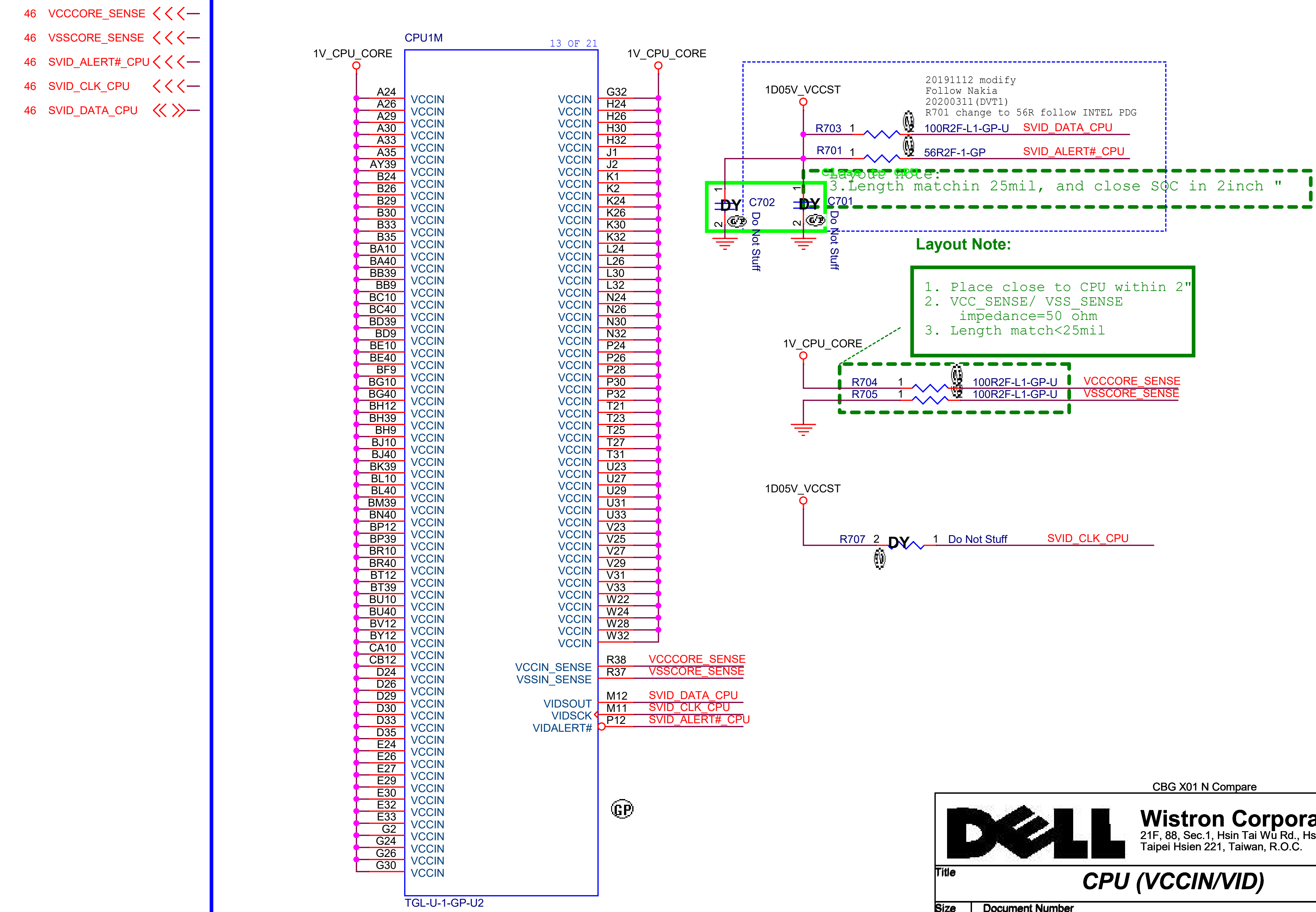

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Title	CPU (VCCIN/VID)	
Size A4	Document Number Cyborg TGL	Rev SB
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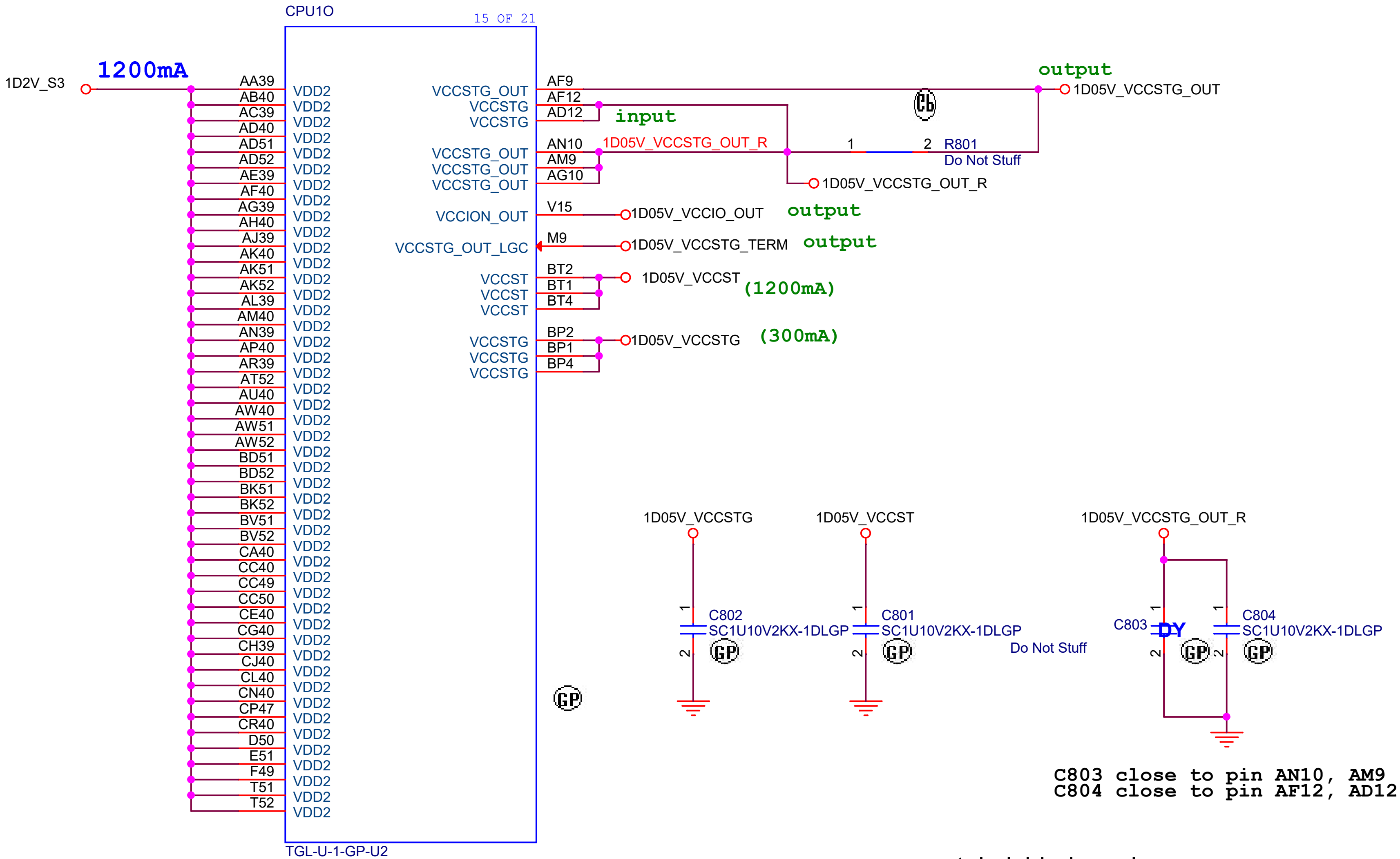
Main Func = CPU



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Lack of VCCPLL_OC / VCC1P8A / VCCPLL

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Title	CPU (VDDQ/VCC/VCCST/VCCSTG)	
Size A4	Document Number: Cyborg TGL	Rev SB
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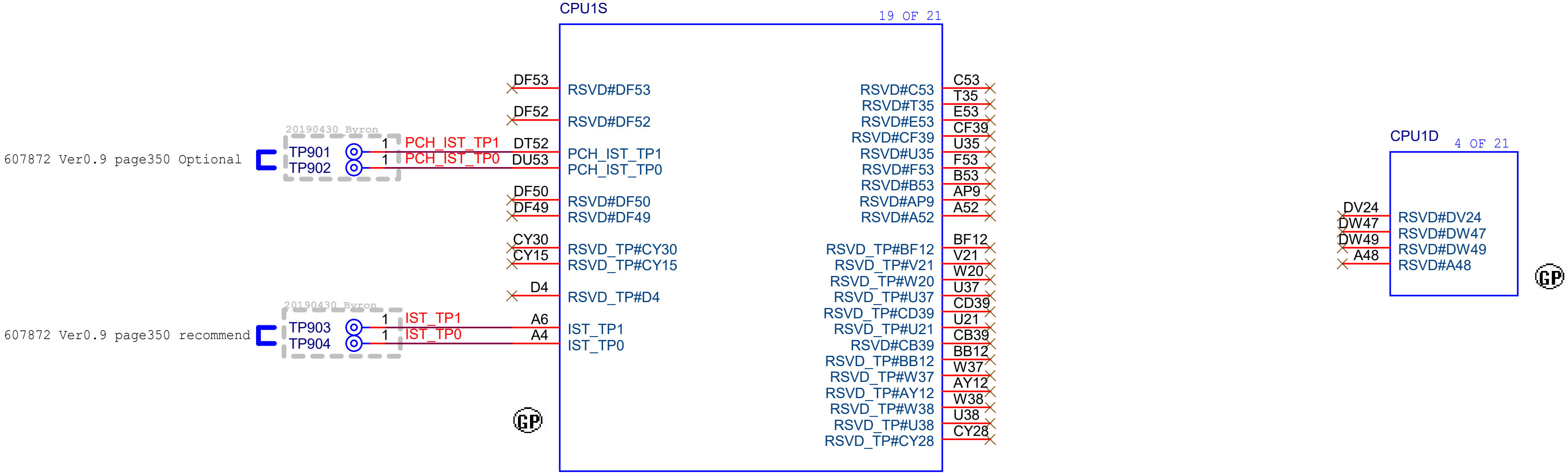

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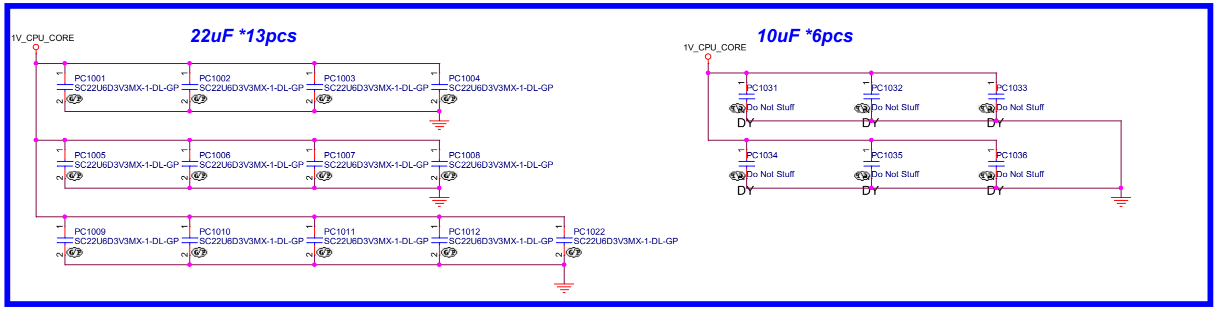
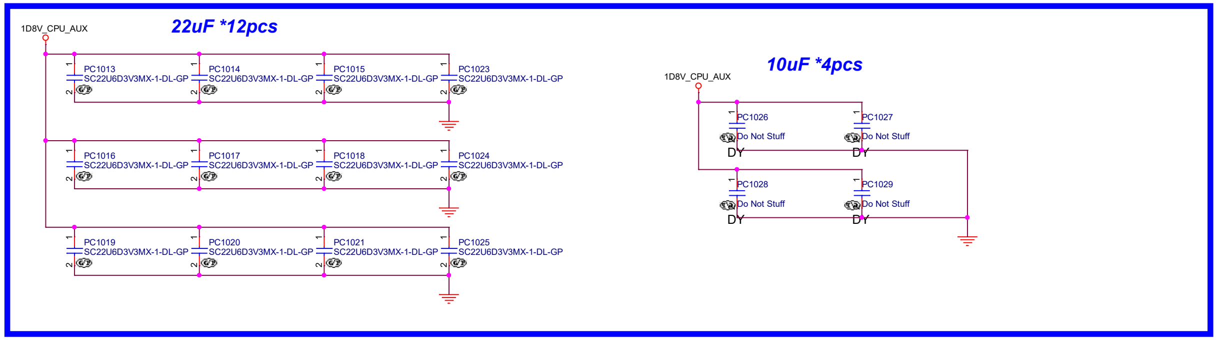
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (RSVD)	
Size A4	Document Number: Cyborg TGL	Rev SB
Date: Thursday, October 15, 2020	Sheet 9 of 105	

Main Func = CPU





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Title	CPU (CORE Power Cap1)	
Size: A2	Document Number: Cyborg TGL	Rev: SB
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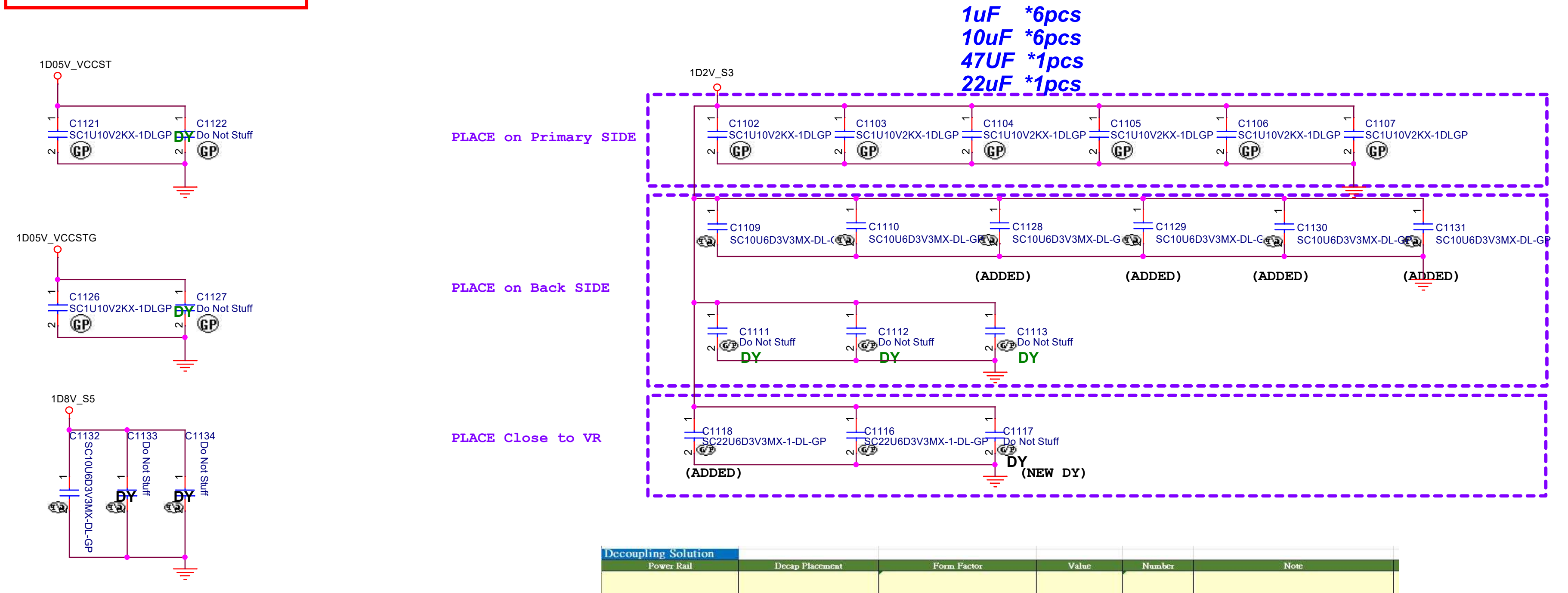
Main Func = CPU



11/5 Tery Don
add 1D8V_S5 decoupling cap. follow Shuri

Decoupling Solution

Power Rail	Decap Placement	Form Factor	Value	Number	Note
VCCDD2	Secondary Side	0402	10uF	8	Place on the back side of the SOC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	Primary Side	0603	47uF	2	Place them as close to the VR as possible. 2 caps should be stuffed.
		0402	1uF	8	Place on the primary side, as close as possible to the vias that connect to the outer row of SoC pins, use wide traces to connect the capacitor pins to the vias. Make sure to put atleast 1 via down near the outer Vdd2 BGA and 1 via down near the cap pad

CBG X01 N Compare

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Title	CPU (Power Cap2)	
Size A3	Document Number: Cyborg TGL	Rev SB
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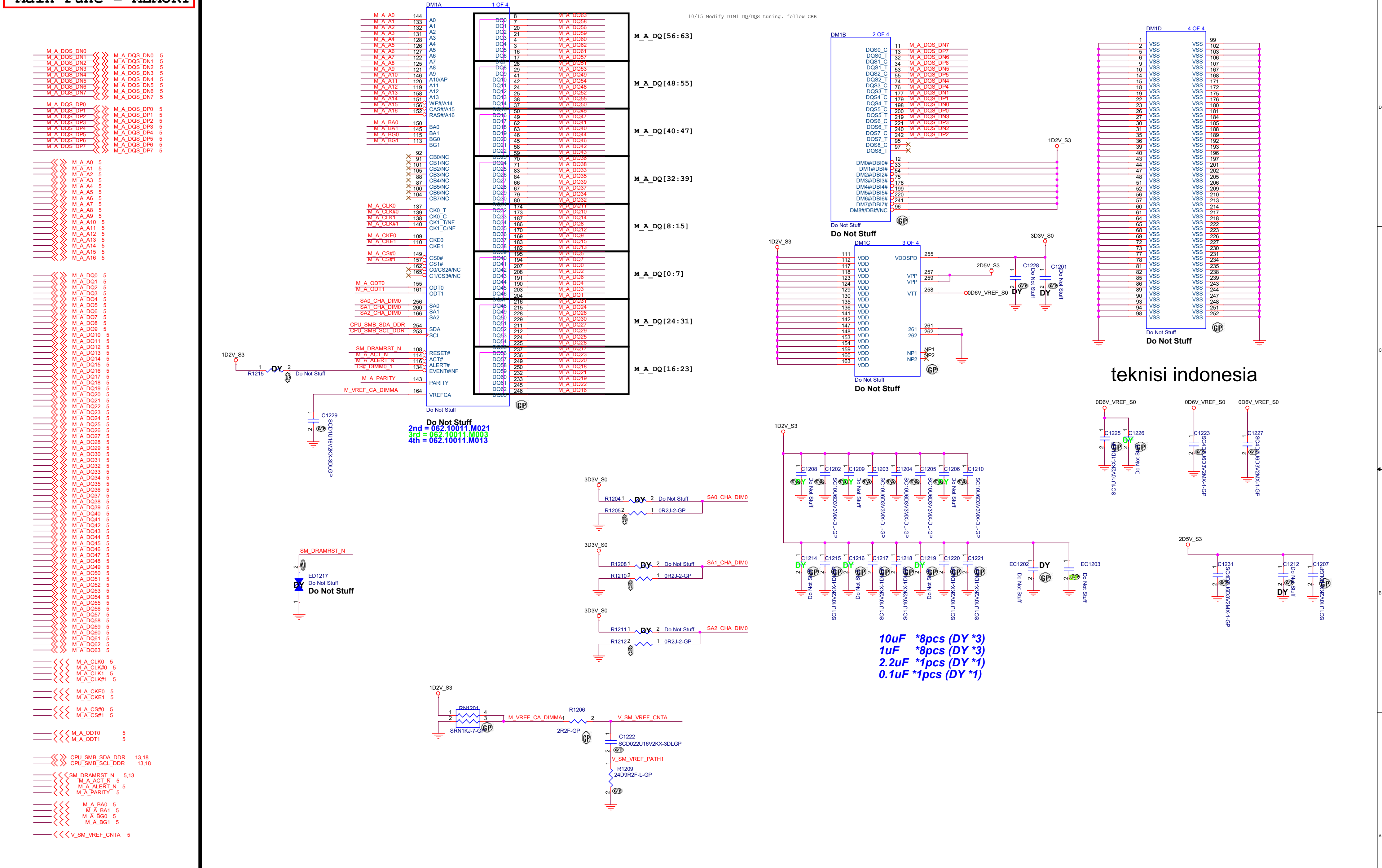
Main Func = MEMORY



CBG X01 N Compare

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Title	DDR3-SODIMM1	
Size A2	Document Number Cyborg TGL	Rev SB
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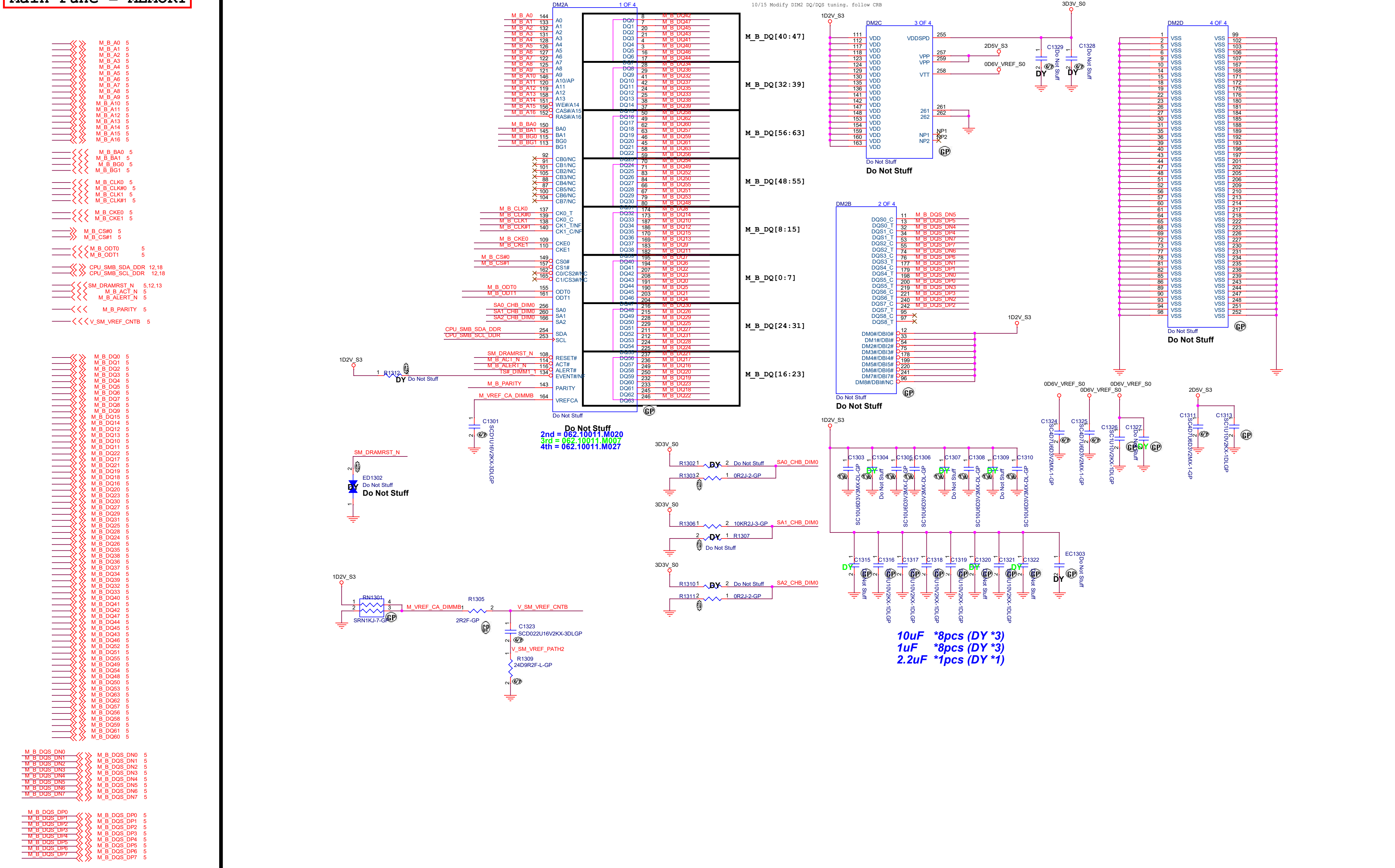
Main Func = MEMORY



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Title	DDR3-SODIMM1
Size	A2
Document Number	Cyborg TGL
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CBG X01 N Compare

DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	***DDR (RSVD) (DDR4-CHA1)***	
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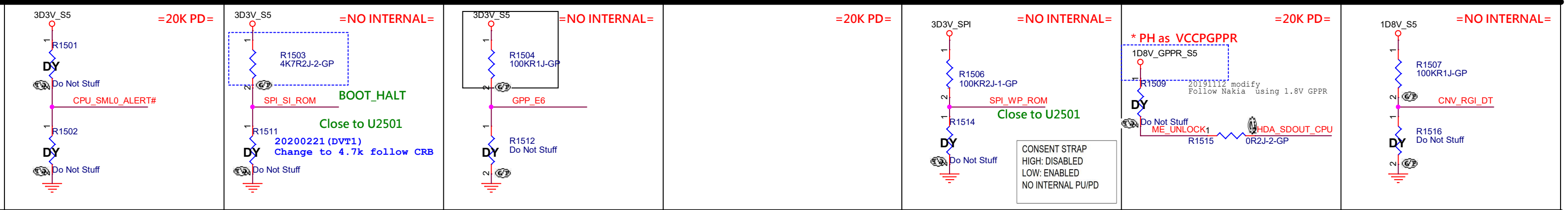
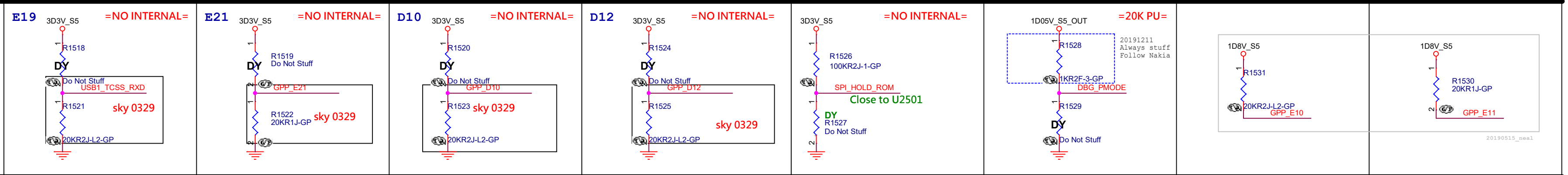
18,24,25,91	SPI_SI_ROM
18,24,25	SPI_WP_ROM
18,24,25	SPI_HOLD_ROM
21	CNV_RGI_DT
18	CPU_SML0_ALERT#
18	GPP_E6
19	HDA_SDOUT_CPU
4,71	USB1_TCSS_RXD
4	GPP_D10
3	DBG_PMODE
4	GPP_D12
4	GPP_E21
18	GPP_E10
18	GPP_E11

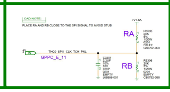
GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic	=20K PD=	=NO INTERNAL=	=NO INTERNAL=	=20K PD=	=NO INTERNAL=	=20K PD=	=NO INTERNAL=
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE



GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10	GPP_E11
Schematic	E19 =NO INTERNAL=	E21 =NO INTERNAL=	D10 =NO INTERNAL=	D12 =NO INTERNAL=	=NO INTERNAL=	=20K PU=		
High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)		
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED		



Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**A0**	**GPP_E10**	**GPP_E11**		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	 RA RB	 RA RB		

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Wistron Corporation
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Title: CPU (STRAP)

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Wistron Corporation
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Title: CPU (PCIE/SATA/USB)

Size: A2 | Document Number: Cyborg TGL | Rev: SB

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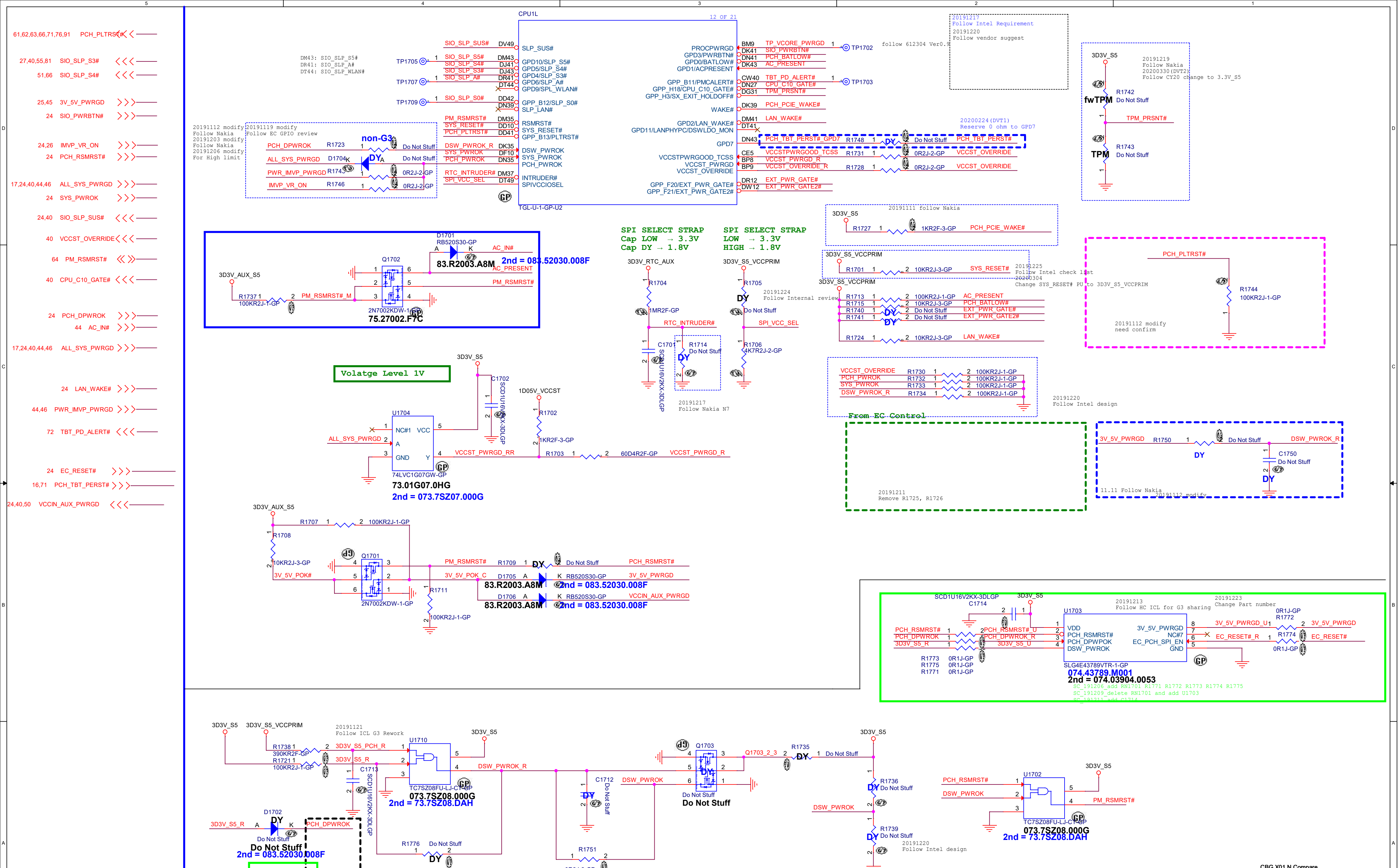

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)

Size: Custom | Document Number: Cyborg TGL | Rev: SB

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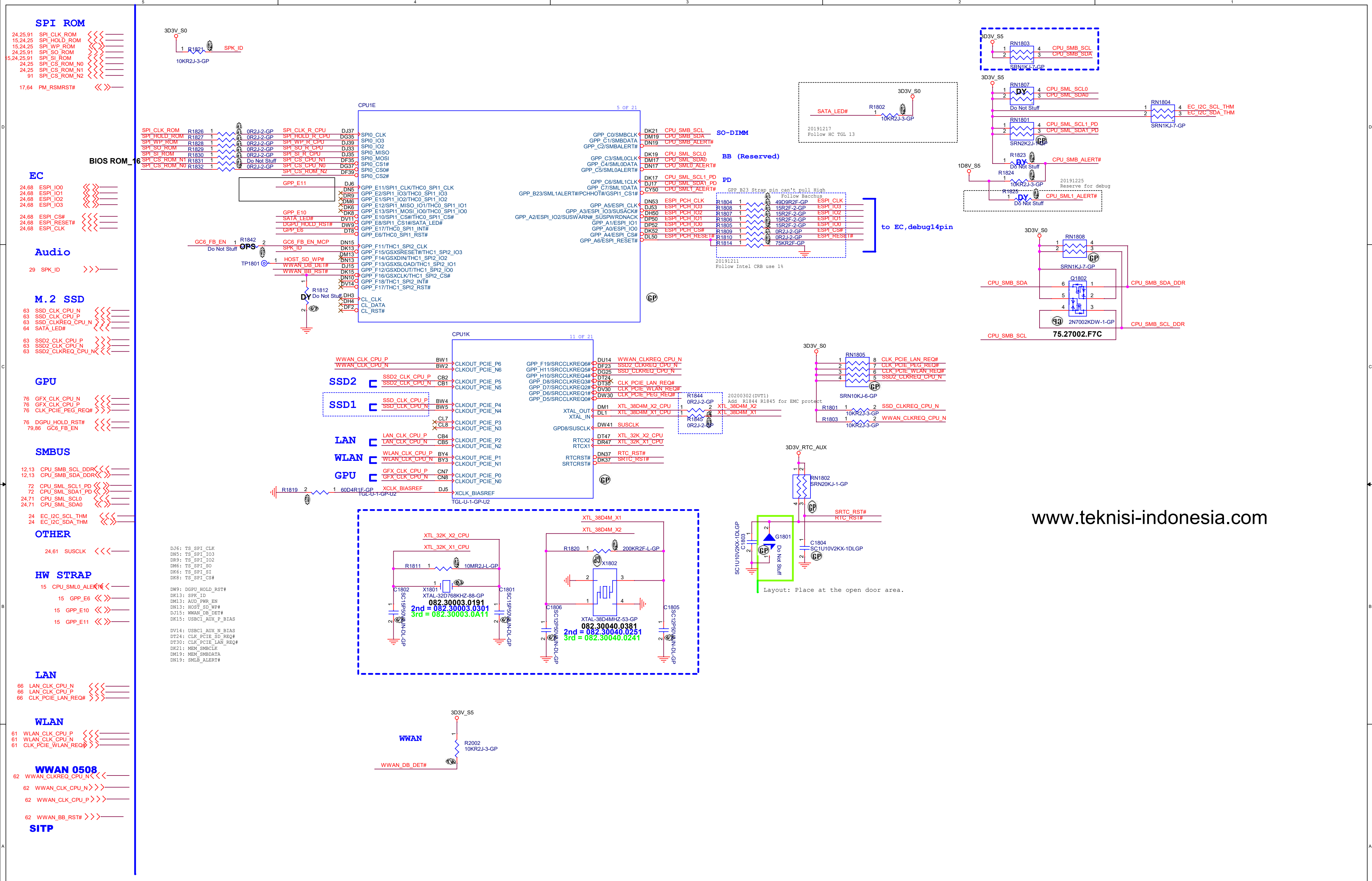

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/LPC/SMBS/XTAL/CLK)

Size: A2 | Document Number: Cyborg TGL | Rev: SB

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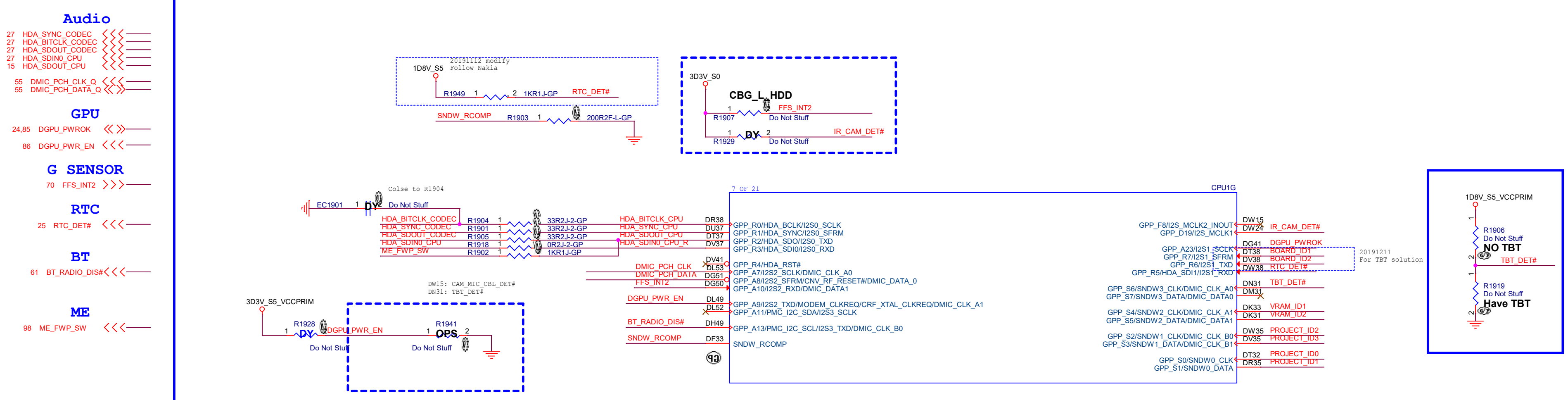
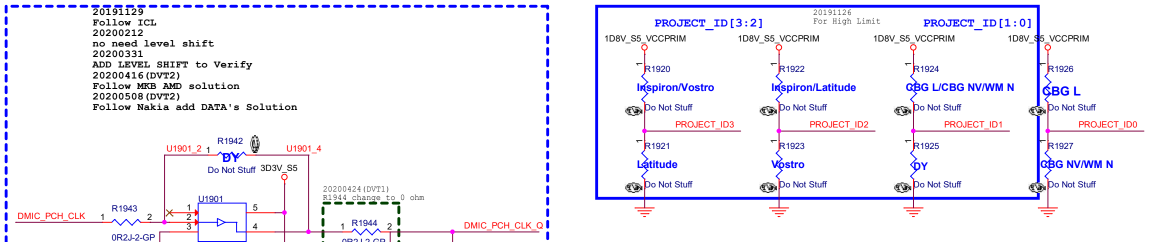
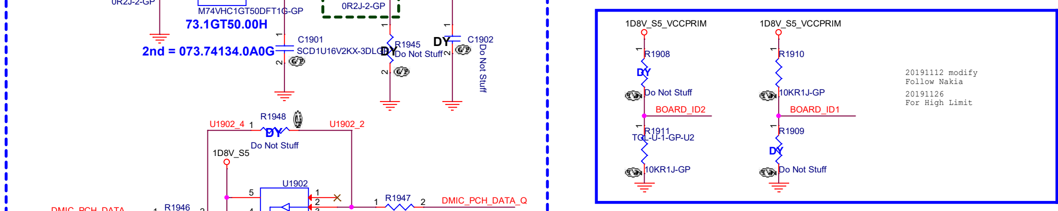
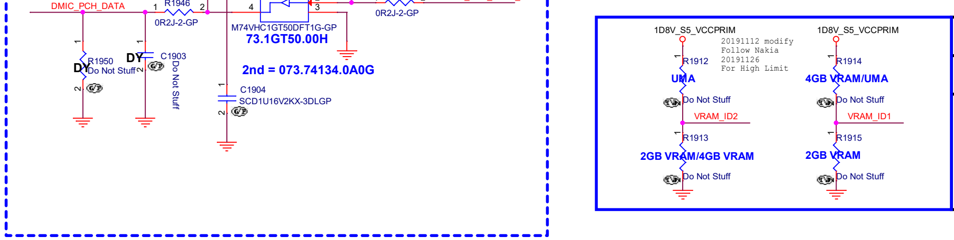








ID	Description	Setting	Mapping
TBT_DET#	TBT function detected	1	no TBT
		0	Have TBT

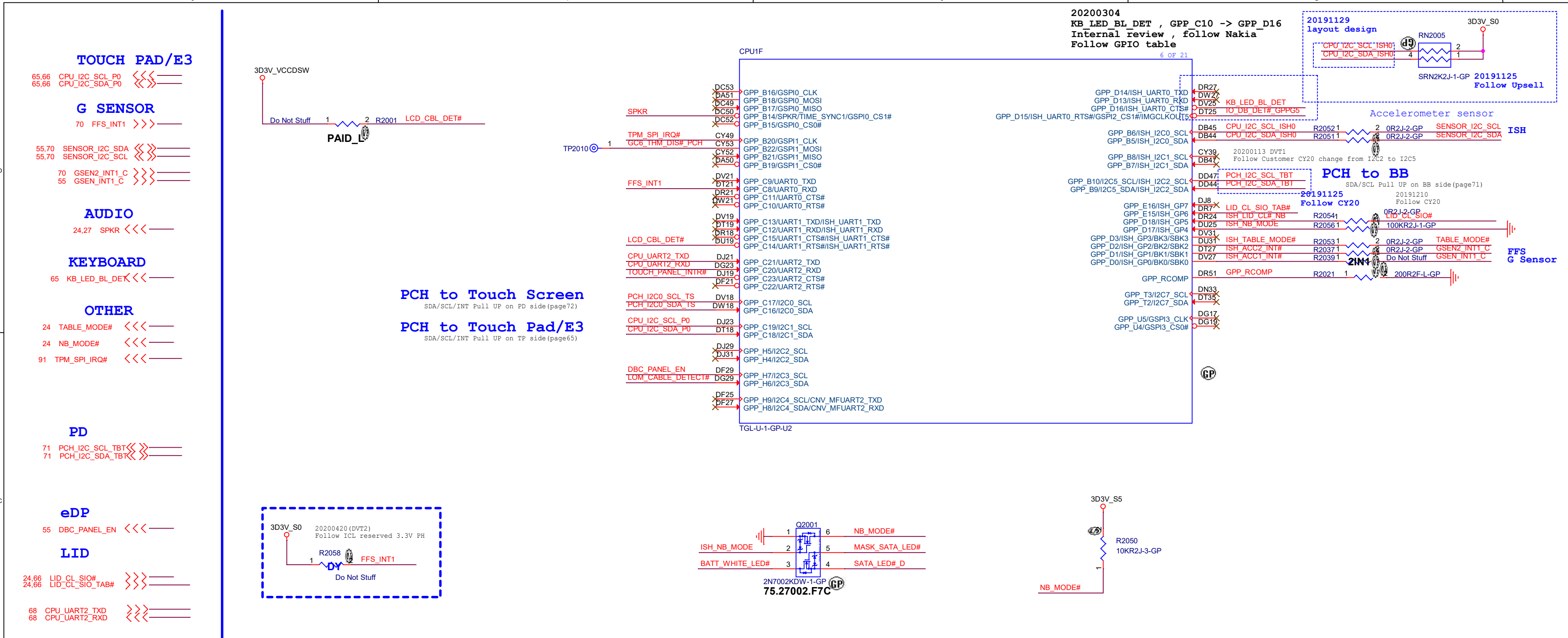
ID	Description	Setting	Mapping
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Series
		10	5000 Series
		01	7000 Series
		00	N/A

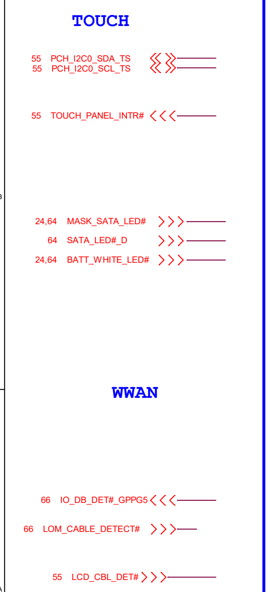
CY21 Board ID Mapping table

ID	Description	Setting	Mapping
Board ID[2:1]	Board SKU ID	11	ADL-P
		10	TGL-C
		01	TGL-U
		00	ICL-U

CY19 VRAM ID Mapping table

ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM





	NB_MODE	LID_CL_SIO_TAB#	
NB Mode	1	1	KB 可以動
Tablet Mode	don´t care	0	KB 鎖住
ClamShell Mode	0	1	KB 鎖住

DA51: NRB_BIT
DC49: VGA_DB_DET#
CY49: TPM_PIRQ#
CY53: GC6_THM_DIS#_PCH
CY52: PCH_3.3V_TS_EN
DA50: HDD_FALL_INT
DV21: SBIOS_TX
DR21: USBC0_AUX_N_BIAS
DW21: USBC0_AUX_P_BIAS
DV19: DGPU_MACO_EN
DT19: SIO_EXT_WAKE#
DR18: PCH_HDD_EN
DU19: LCD_CBL_DET#
DG23: cTPM_PRSNT#
DJ19: TOUCH_PANEL_INTR#
DF21: TOUCH_I2C_DET#
DV18: I2C0_SCL_TS
DW18: I2C0_SDA_TS
DF29: DBC_PANEL_EN
DG29: LOM_CABLE_DETECT#
DF25: CNV_COEX1
DF27: CNV_COEX2
DR27: STYLUS_PWR_OCP#
DW27: CAM_SHUTTER#
DT25: IO_DB_DET#
CY39: ISH_I2C1_ALS_SCL
DB47: ISH_I2C1_ALS_SDA
DD47: ISH_I2C2_SCL
DD44: ISH_I2C2_SDA
DJ8: ISH_P_SENSOR_INT#
DV31: ISH_ALS_INT#
DG17: ZPODD_PWR_EN#
DG19: ZPODD_DA#

CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)

Size: A2 | Document Number: Cyborg TGL | Rev: SB

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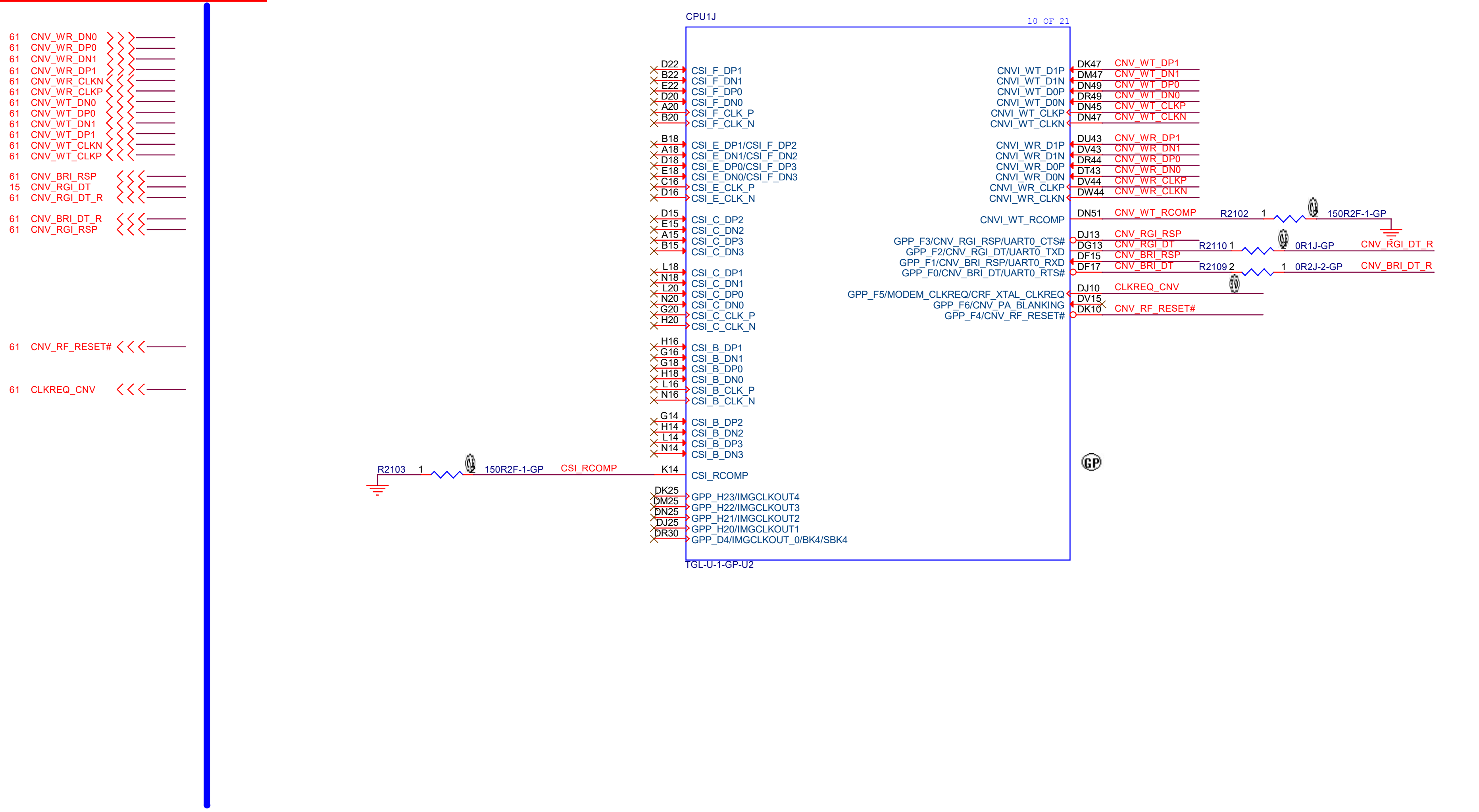
Main Func = PCH



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CBG X01 N Compare

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Title	CPU (CSI/EMMC/CNVi)
Size A3	Document Number: Cyborg TGL — Rev SB
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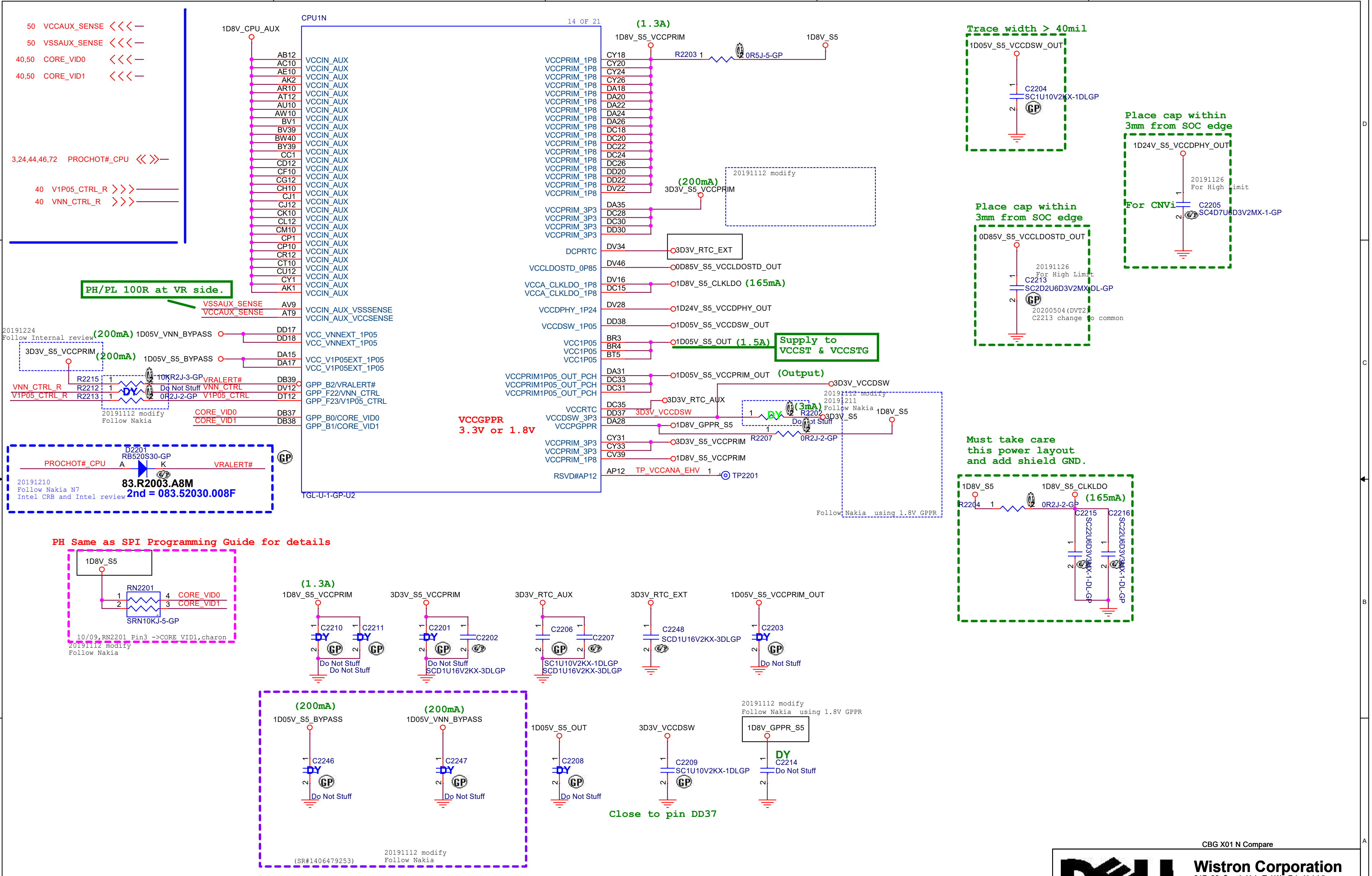

CBG X01 N Compare

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Title	CPU (PCH-LP PWR&Caps)	
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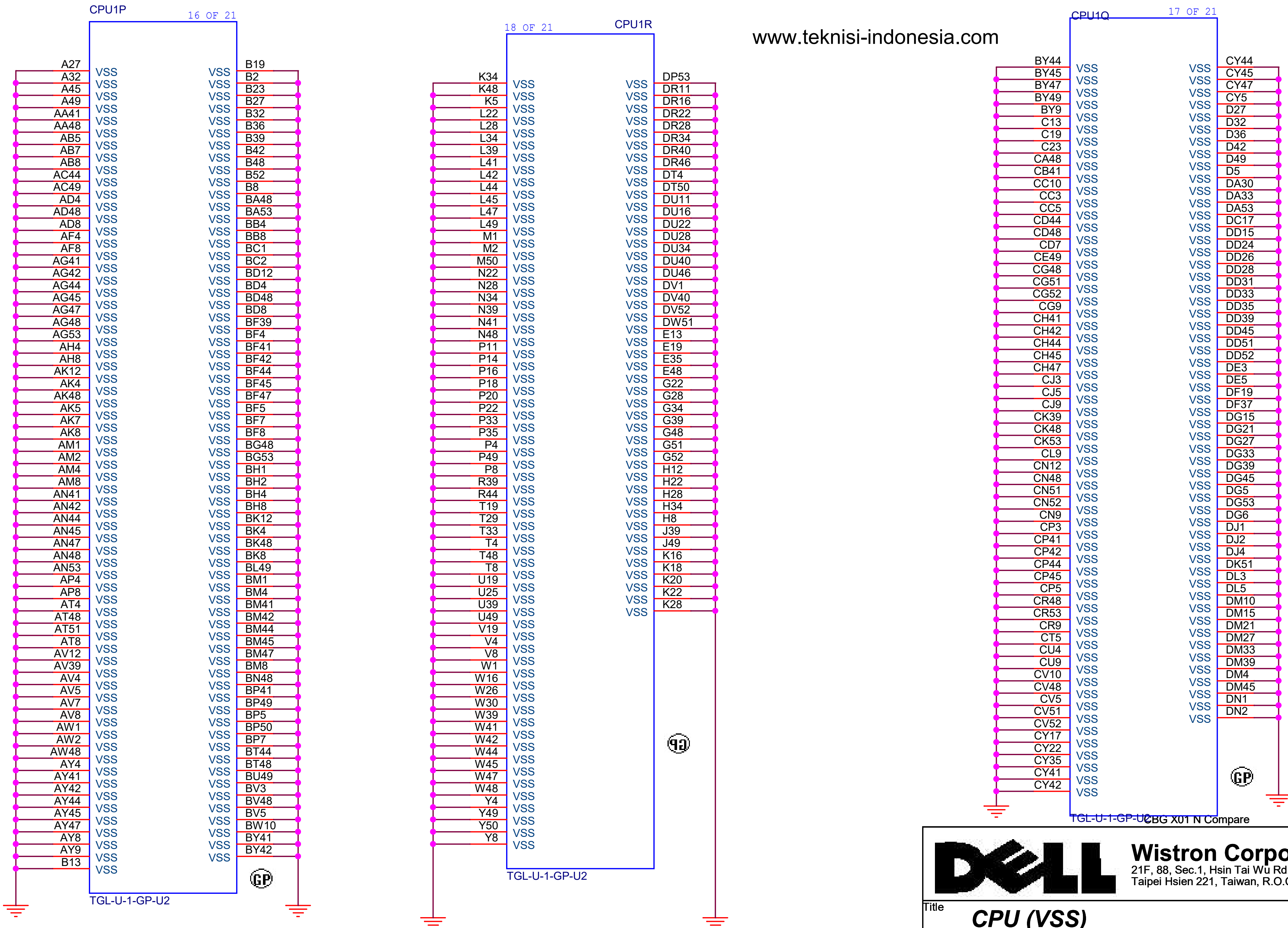

CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**CPU (VSS)**	
Size A4	Document Number **Cyborg TGL**	Rev **SB**
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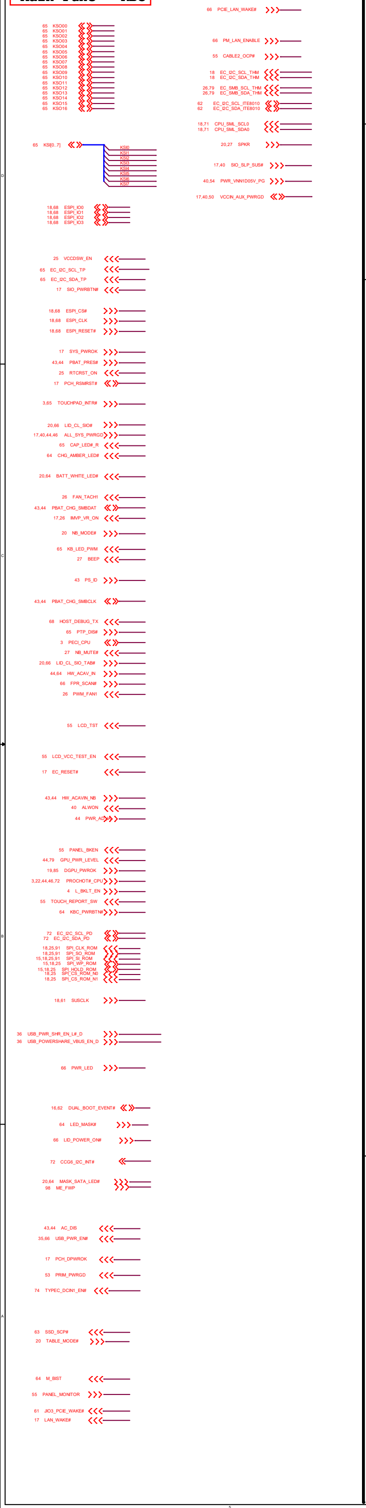
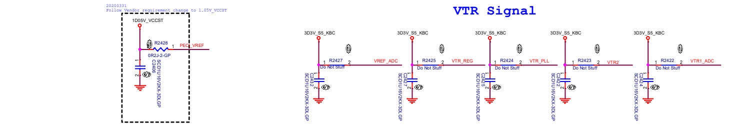
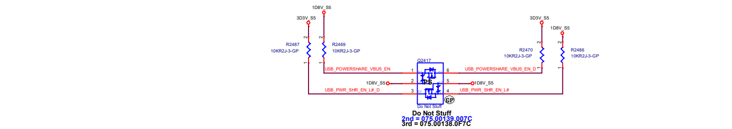
Main Func = KBC

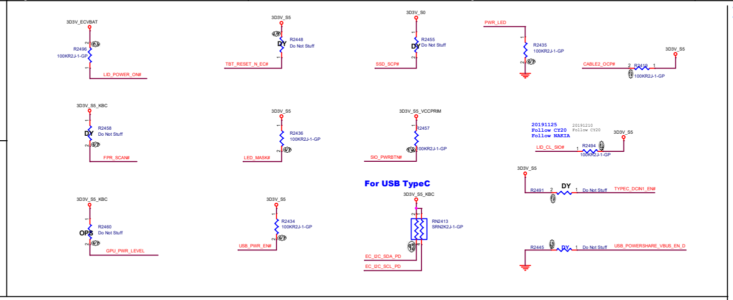


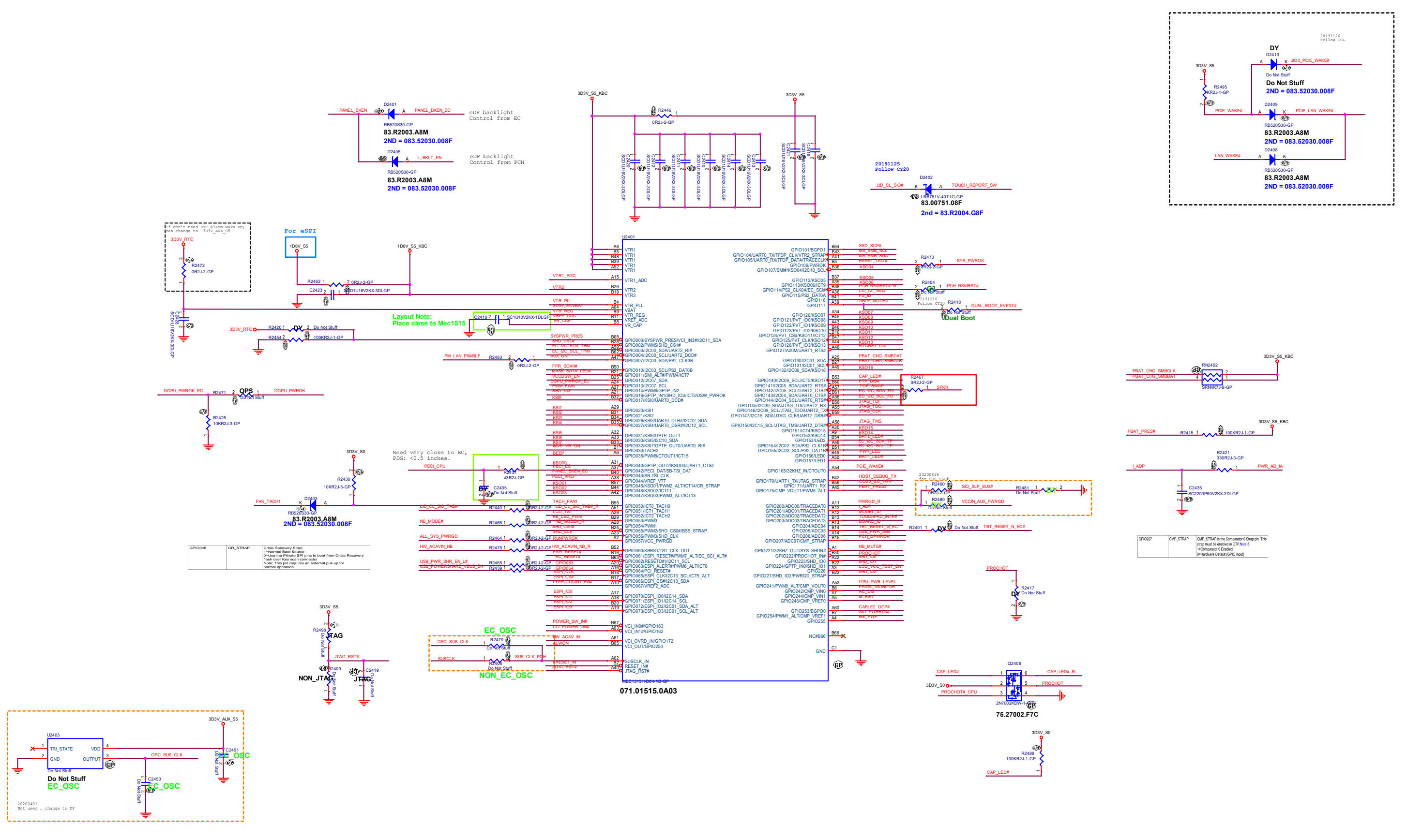
VTR Signal



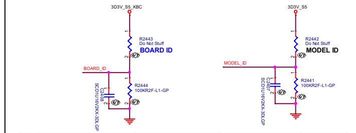
For USB Charge Level shift







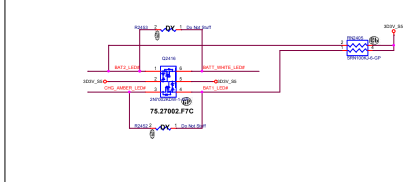
Board ID and Model ID



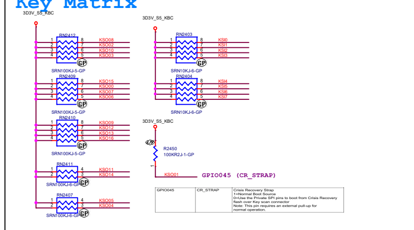
#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K 64.17825.6DL	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

#	MODEL ID (GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR (R2442)	VOLTAGE	
1	CBG-N-14&15 UMA	100k	10.0k	3	64.10025.6DL
2	CBG-V-14&15 UMA	100k	17.8k	2.801	64.17825.6DL
3	CBG-L-14&15 UMA	100k	27.0k	2.598	64.27025.6DL
4	WM-N-14 UMA	100k	37.4k	2.402	64.37425.6DL
5		100k	49.9k	2.201	
6	CBG-N-14&15 DIS	100k	64.9k	2.001	64.64925.6DL
7	CBG-V-14&15 DIS	100k	82.5k	1.808	64.82525.6DL
8	CBG-L-14&15 DIS	100k	107k	1.594	64.10735.6DL
9	WM-N-14 DIS	100k	154k	1.299	64.15435.6DL
10		100k	200k	1.1	

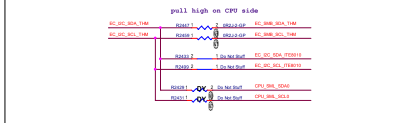
LED



Key Matrix



SMBUS Option



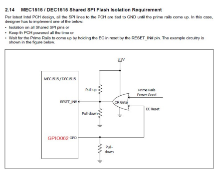


TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for BootNote 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/ICT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

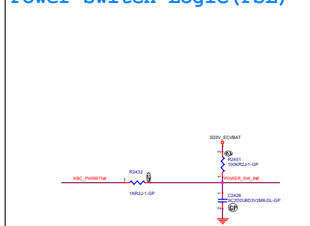
3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

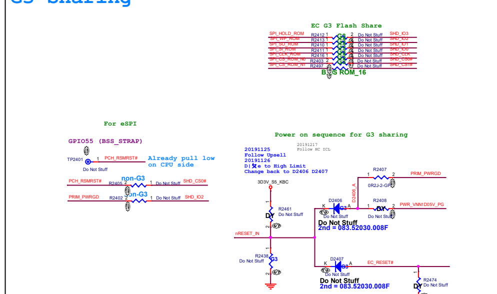
GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI CS0# is detected high while RSMRST# is low.

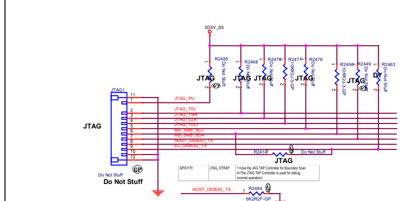
Power Switch Logic(PSL)



G3 Sharing



JTAG DEBUG CONN



GPIO170	JTAG_STRAP	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug (normal operation)

CBG X01 N Compare

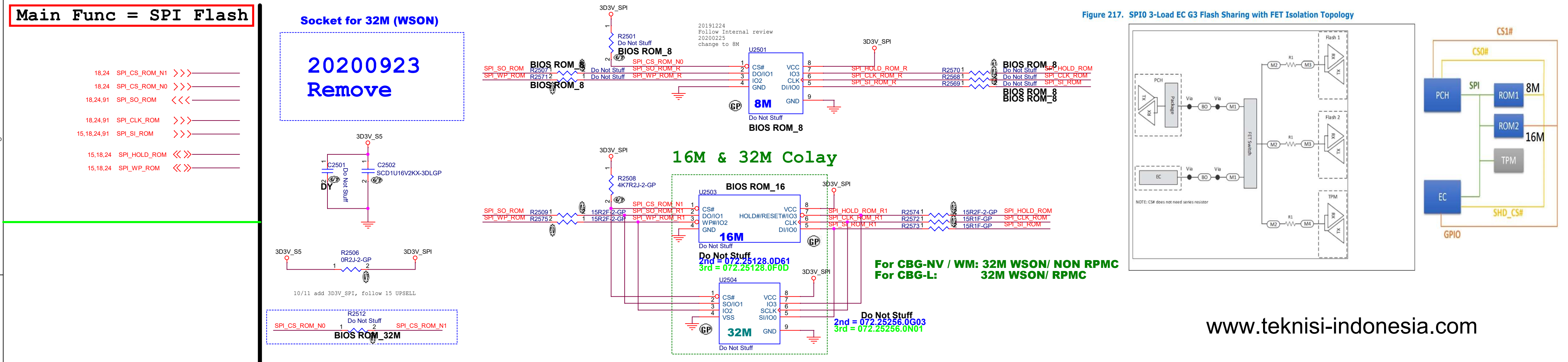
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE285PA0DX

Size: Custom | Document Number: Cyborg TGL | Rev: SB

Date: Thursday, October 15, 2020 | Sheet 24 of 105

Main Func = SPI Flash



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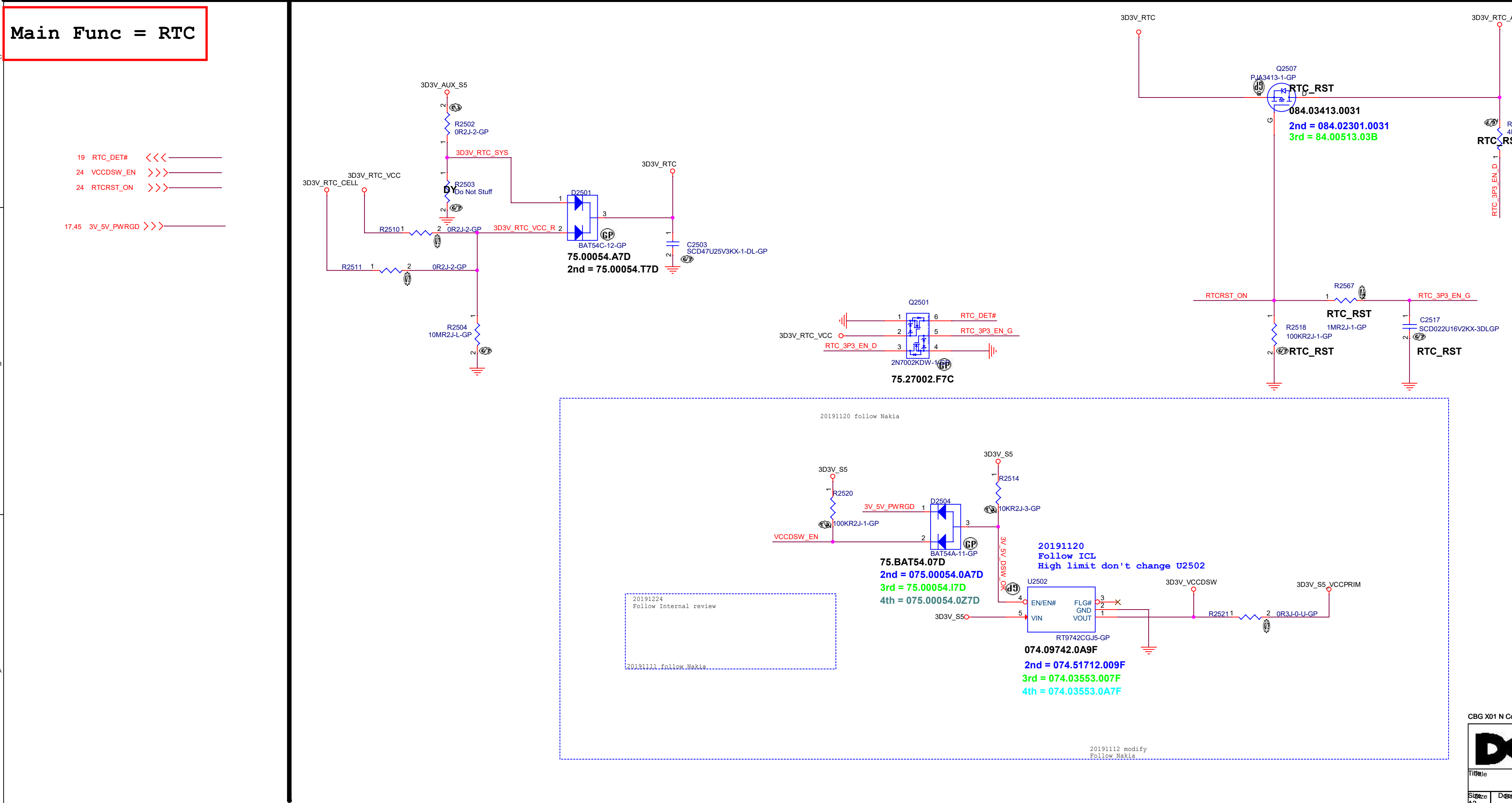
Main Func = RTC

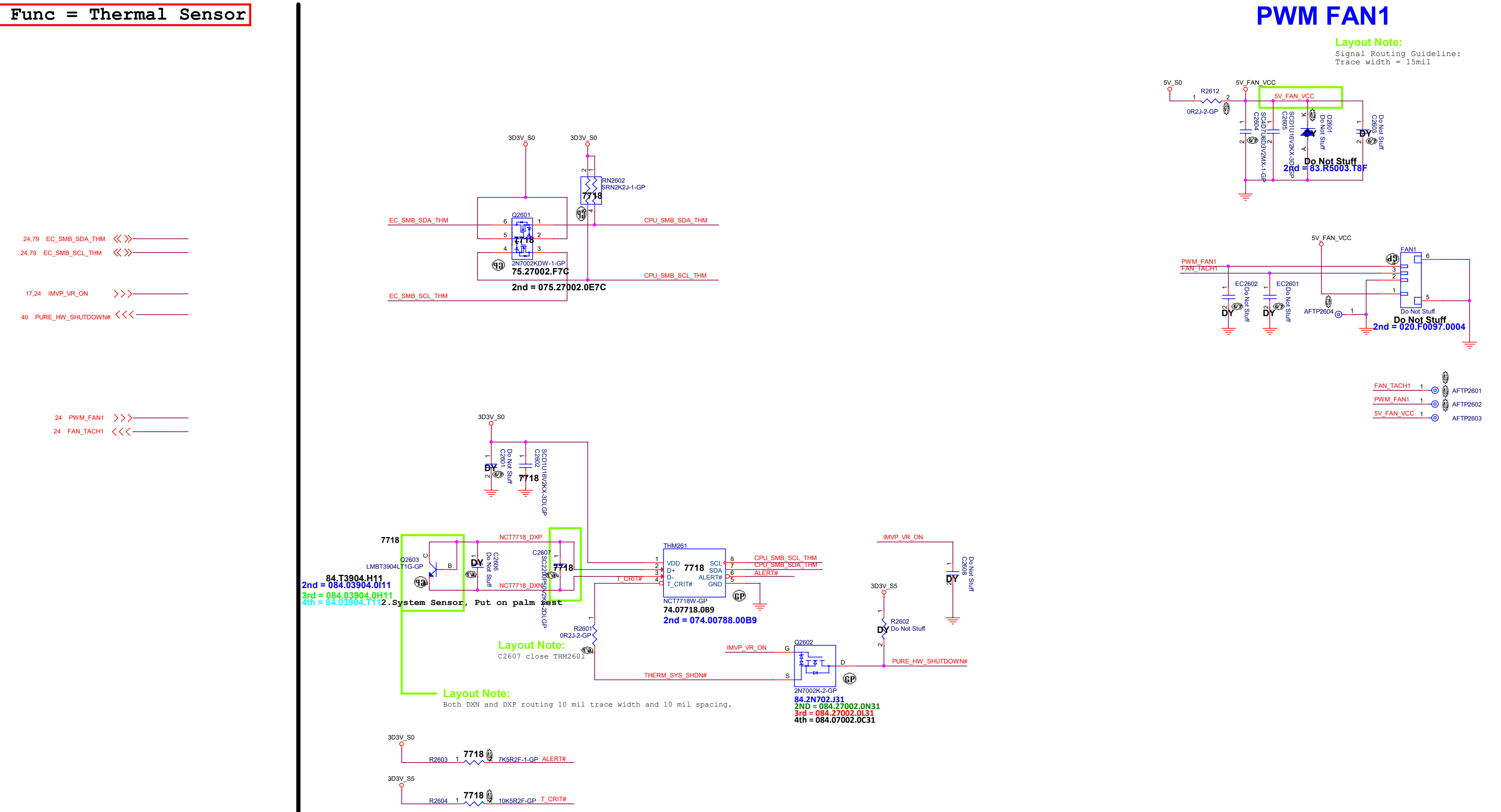


CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Flash	
Size A2	Document Number: Cyborg TGL	Rev SB
Date: Thursday, October 15, 2020	Sheet 25 of 105	

Main Func = Thermal Sensor



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

CBG X01 N Compare

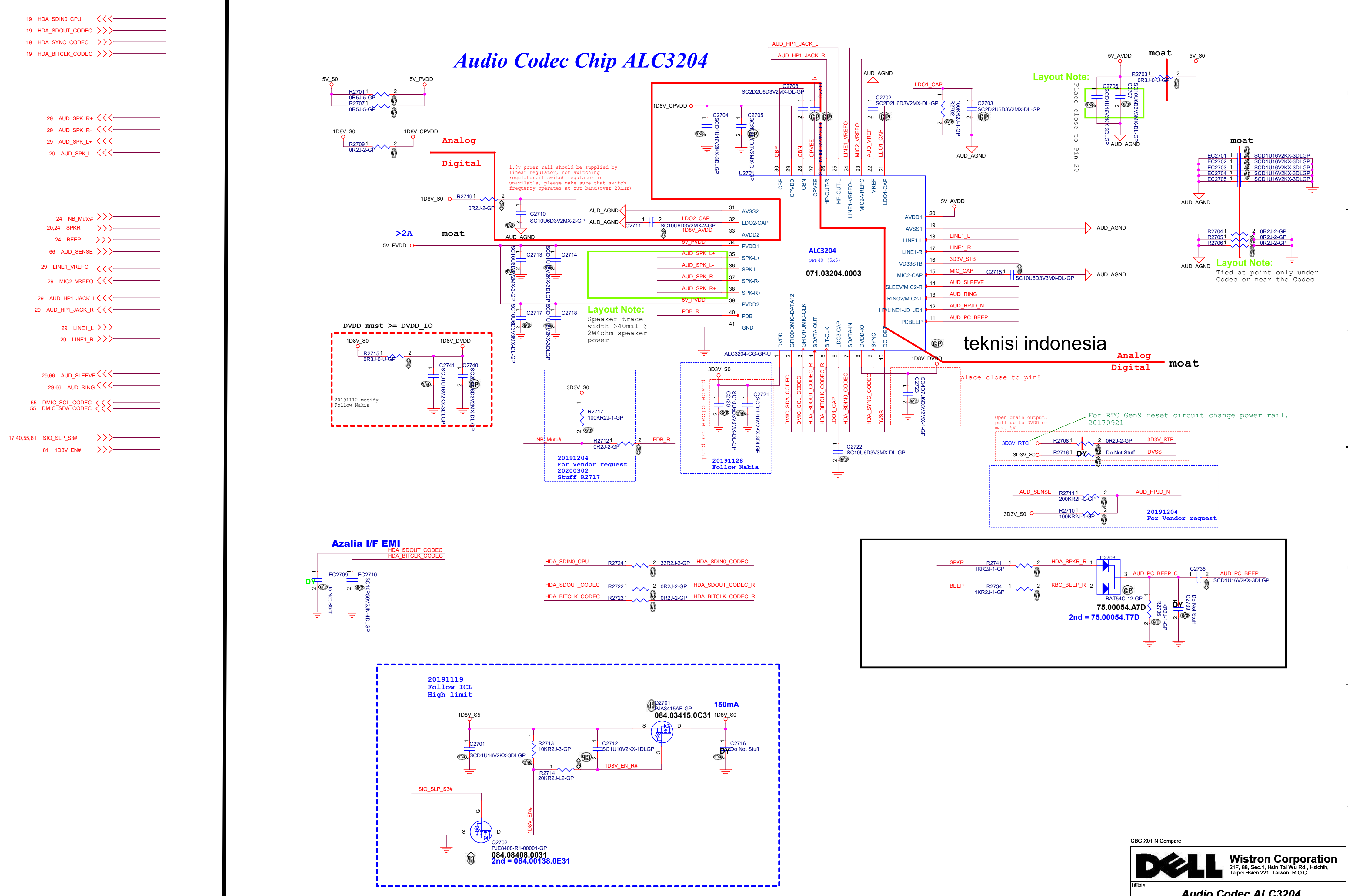
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: A2 | Document Number: Cyborg TGL | Rev: SB

Date: Thursday, October 15, 2020 | Sheet 26 of 105

Main Func = Audio



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3204

Size: A2 | Document Number: Cyborg TGL | Rev: SB

Date: Thursday, October 15, 2020 | Sheet 27 of 105

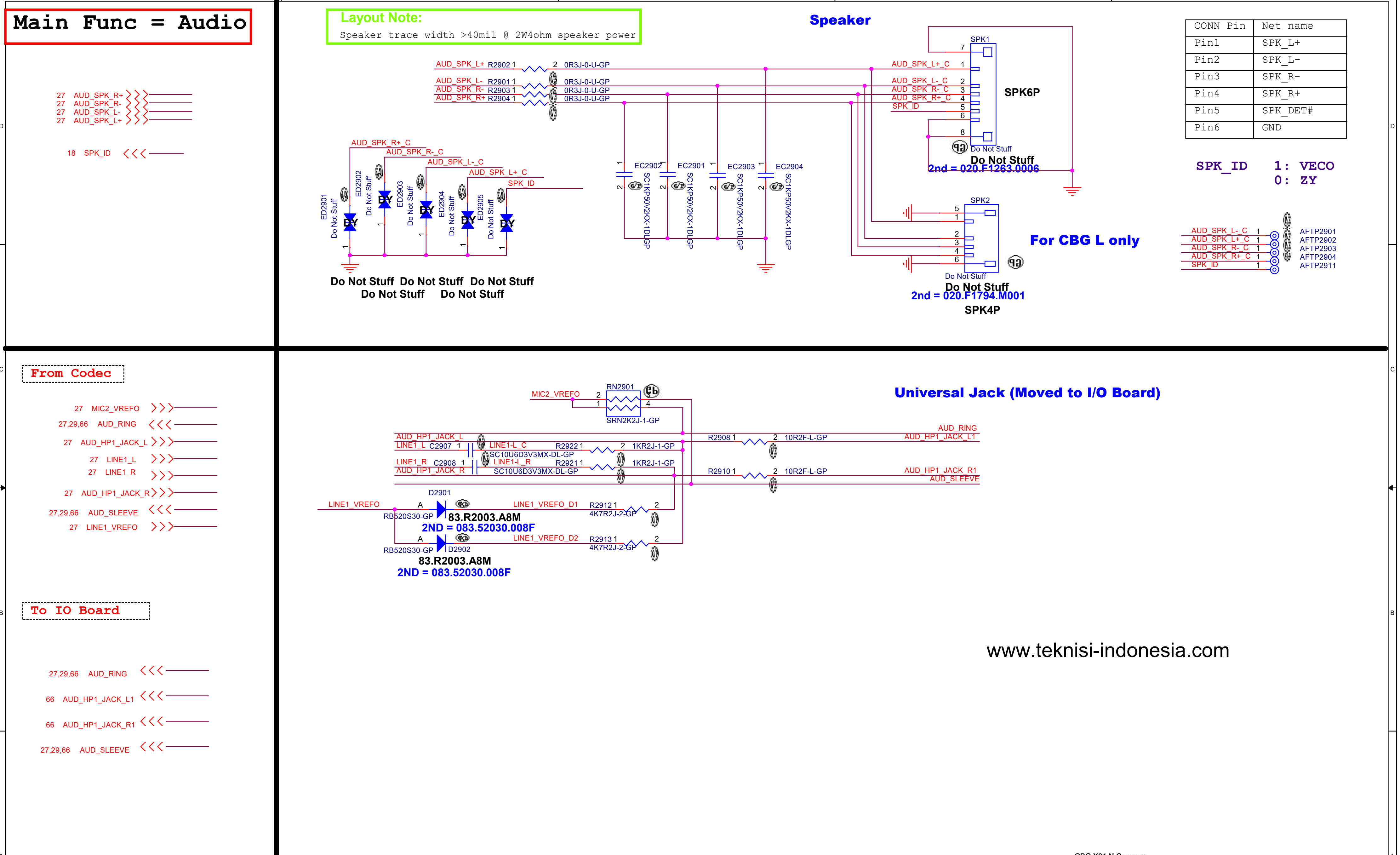
(Blanking)

CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)		
Size: A4	Document Number: Cyborg TGL	Rev: SB
Date: Thursday, October 15, 2020	Sheet 28 of 105	

Main Func = Audio



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO
Size: A3 Document Number: Cyborg TGL Rev: SB
Date: Thursday, October 15, 2020 Sheet 29 of 105

(Blanking)

Main Func = LAN

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
LAN RTL8106

Size: Custom
Document Number: Cyborg TGL
Rev: SB

Date: Thursday, October 15, 2020
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Main Func = LAN

CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	XFOM&RJ45		
Size A3	Document Number Cyborg TGL		Rev SB
Date: Thursday, October 15, 2020	Sheet 32	of	105

Main Func = Card Reader

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CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Card Reader-RTS5170*		
Size: A4	Document Number: *Cyborg TGL*	Rev: *SB*
Date: Thursday, October 15, 2020	Sheet 33 of 105	

Main Func = USB2.0

CBG X01 N Compare

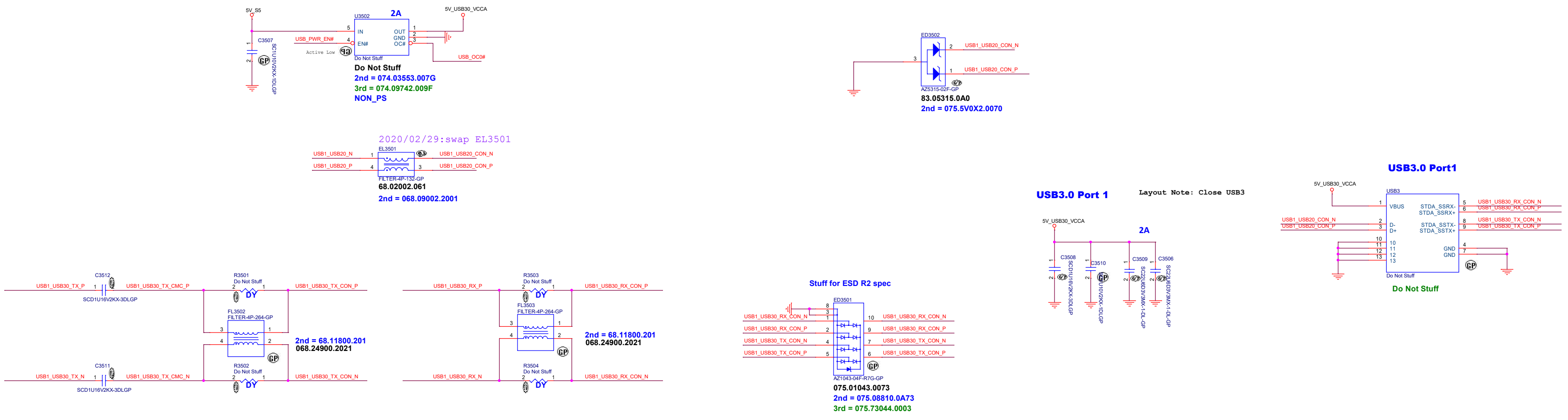
Main Func = USB3.0 Port1

24,66 USB_PWR_EN#

16,36 USB_OC0#

36 USB1_USB20_N
36 USB1_USB20_P

16 USB1_USB30_TX_N
16 USB1_USB30_TX_P
16 USB1_USB30_RX_N
16 USB1_USB30_RX_P



CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0 CONN
Size	A1
Document Number	Cyborg TGL
Rev	SB
Date:	Thursday, October 15, 2020
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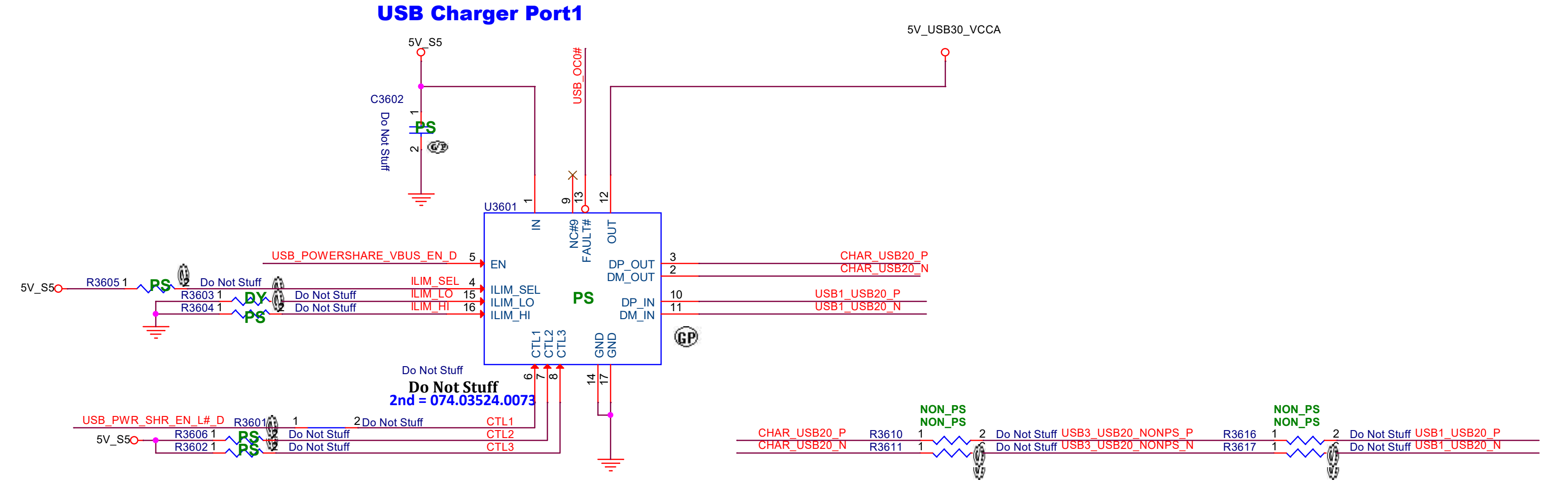
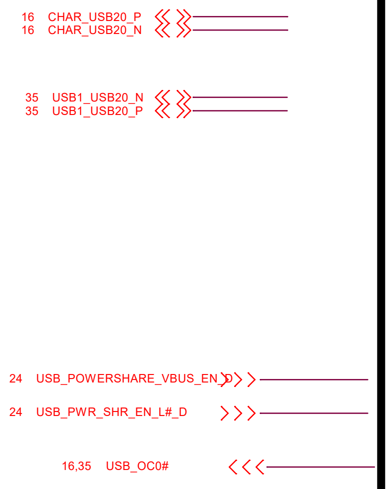
Main Func = USB Charger

For CBG L





Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Charger

Size: Custom | Document Number: Cyborg TGL | Rev: SB

Date: Thursday, October 15, 2020 | Sheet 36 of 106

(Blanking)

CBG X01 N Compare

DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**USB3.0 PORT**
Size A4	Document Number **Cyborg TGL** — Rev **SB**
Date: Thursday, October 15, 2020	Sheet 37 of 105

5 4 3 2 1

D C B A

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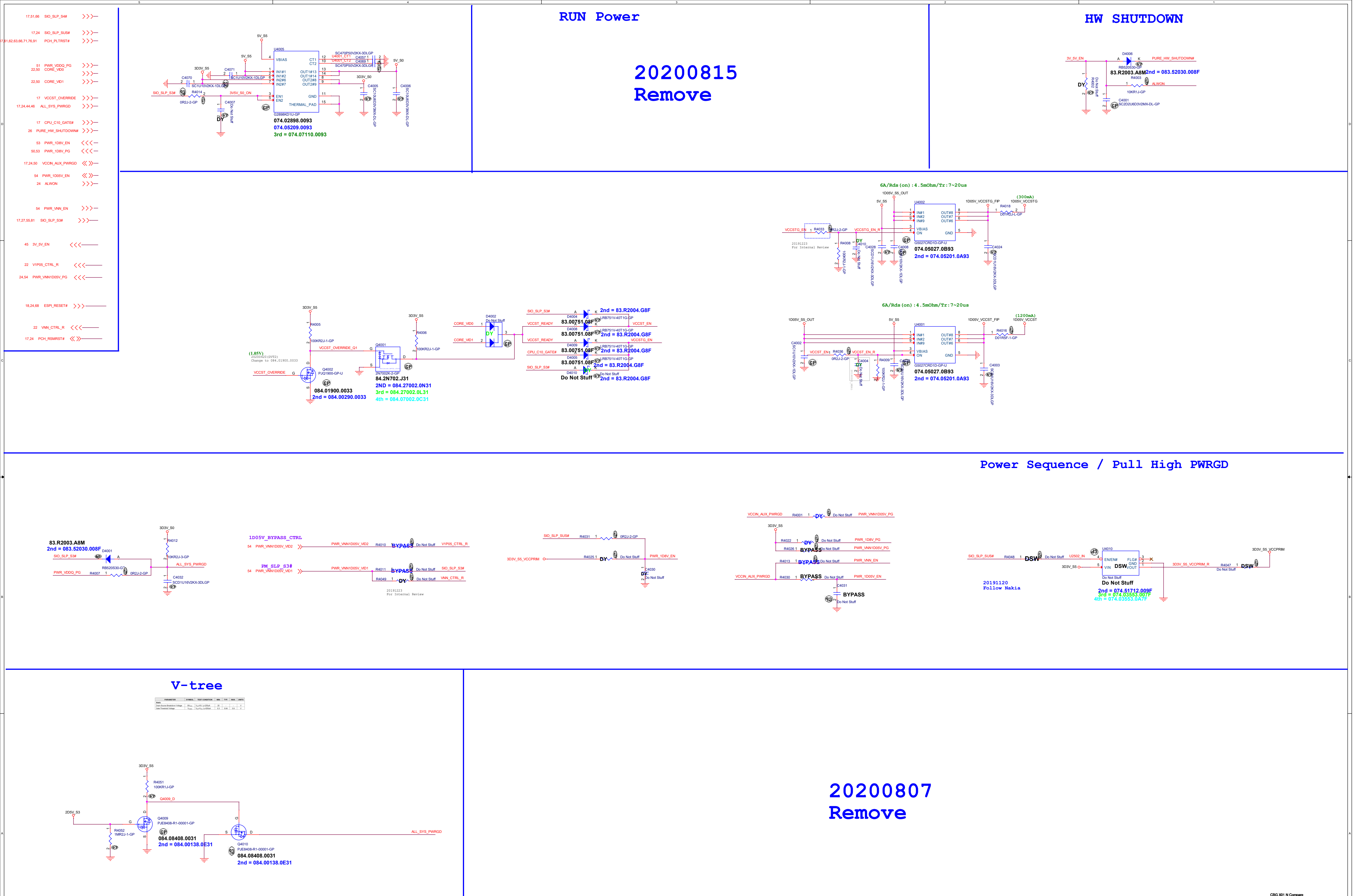
CBG X01 N Compare

CBG X01 N Compare			
DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***(RSVD)***			
Size: A4	Document Number: ***Cyborg TGL***		Rev: ***SB***
Date: Thursday, October 15, 2020	Sheet 39	of	105



CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (THML/JTAG)
Size	A1
Document Number	Cyborg TGL
Rev	SB
Date:	Thursday, October 15, 2020
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CBG X01 N Compare

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Connected_Standby(1/2)+DS3*		
Size: A4	Document Number: *Cyborg TGL*	Rev: *SB*
Date: Thursday, October 15, 2020	Sheet 41 of 105	

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CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Connected_Standby(2/2)*	
Size A4	Document Number **Cyborg TGL**	Rev **SB**
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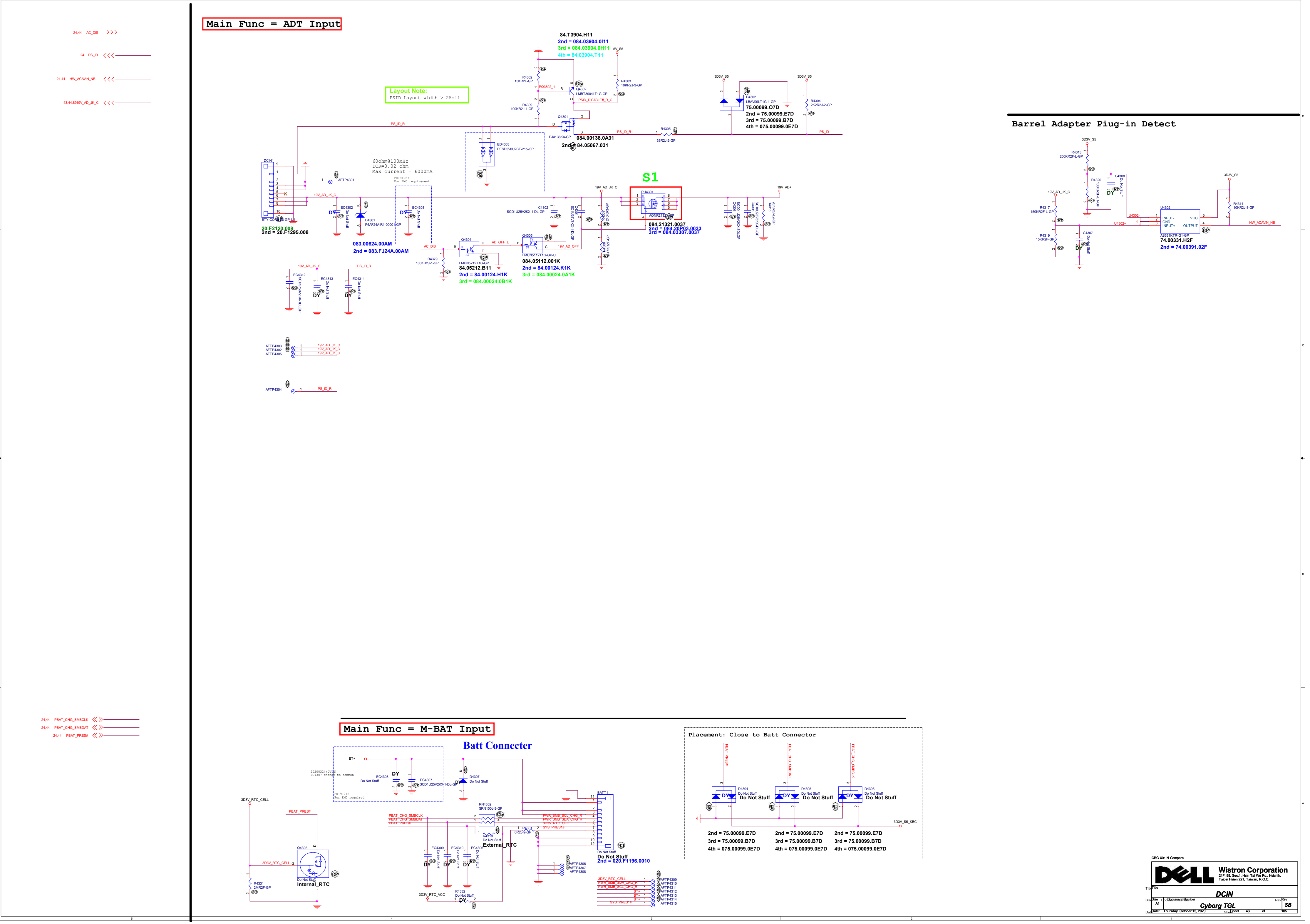

Main Func = ADT Input
Layout Note:
PSID Layout width > 25mil
84.T3904.H11
2nd = 084.03904.0I11
3rd = 084.03904.0H11
4th = 84.03904.T11
75.00099.O7D
2nd = 75.00099.E7D
3rd = 75.00099.B7D
4th = 075.00099.0E7D
084.00138.0A31
2nd = 84.05067.031
60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA
S1
084.21321.0037
2nd = 084.20P03.0033
3rd = 084.03307.0037
20.F2120.008
2nd = 20.F1295.008
083.00624.00AM
2nd = 083.FJ24A.00AM
84.05212.B11
2nd = 84.00124.H1K
3rd = 084.00024.0B1K
084.05112.001K
2nd = 84.00124.K1K
3rd = 084.00024.0A1K
Barrel Adapter Plug-in Detect
74.00331.H2F
2nd = 74.00391.02F
Main Func = M-BAT Input
Batt Connecter
Placement: Close to Batt Connector
External_RTC
Internal_RTC
Do Not Stuff
2nd = 020.F1196.0010
2nd = 75.00099.E7D
3rd = 75.00099.B7D
4th = 075.00099.0E7D
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DCIN
Cyborg TGL
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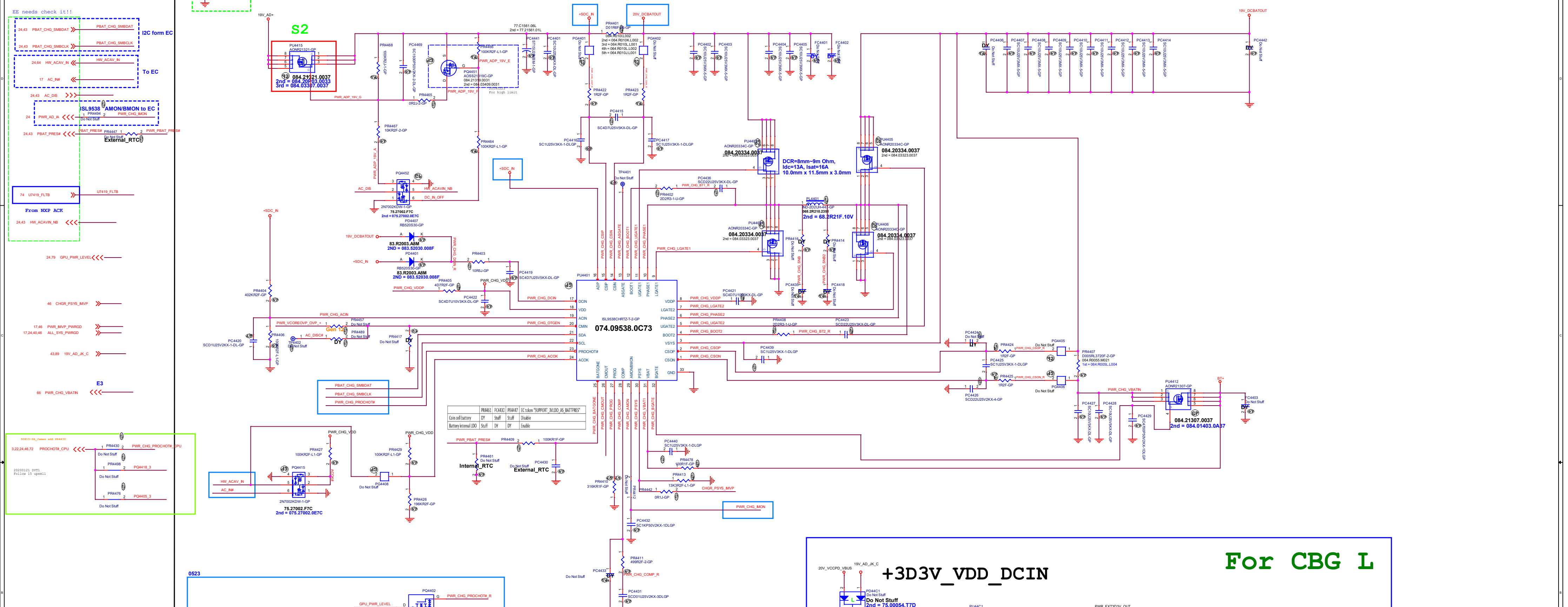
SB

Main Func = Charger

OFFPAGE

ISL9538C For Charger



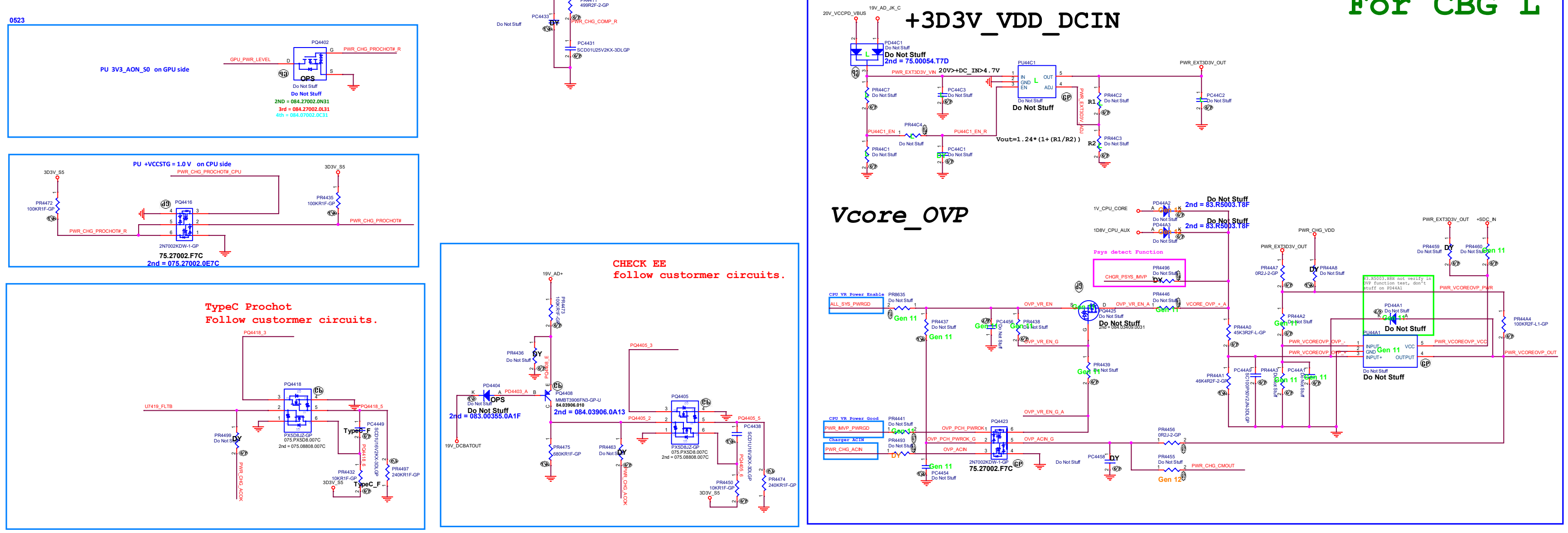
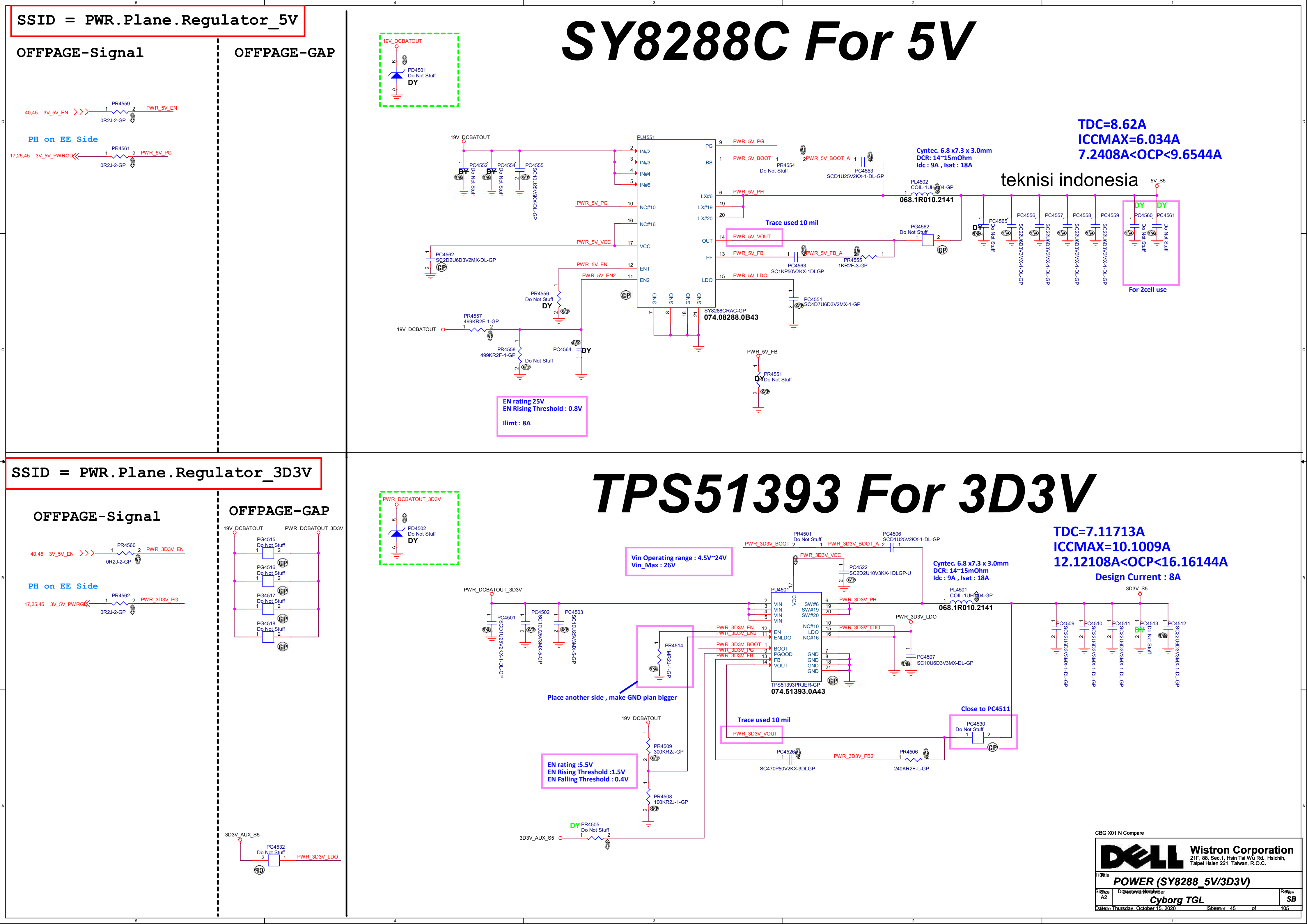


TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476

Location	Gen11	Gen12
PC44A1	Stuff	DY
PC4454	Stuff	DY
PC4456	Stuff	DY
PQ4425	Stuff	DY
PR4447	Stuff	DY
PR4437	Stuff	DY
PR4438	Stuff	DY
PR4439	Stuff	DY
PR4441	Stuff	DY
PR4446	Stuff	DY
PR44A2	Stuff	DY
PR44A3	Stuff	DY
PR4460	Stuff	DY
PR4491	Stuff	DY
PU44A1	Stuff	DY
PD44A1	Stuff	DY
PD44A2	DY	Stuff
PD44A3	DY	Stuff
PR4455	DY	Stuff
PR4457	DY	Stuff

CBG X01 N Compare



SSID = PWR.Plane.Regulator_5V
OFFPAGE-Signal
OFFPAGE-GAP
SY8288C For 5V
19V_DCBATOUT
PD4501
Do Not Stuff
DY
PR4559
40,45 3V_5V_EN
PWR_5V_EN
0R2J-2-GP
PH on EE Side
PR4561
17,25,45 3V_5V_PWRGD
PWR_5V_PG
PU4551
PWR_5V_BOOT
PR4554
Do Not Stuff
PWR_5V_BOOT_A
PC4553
SCD1U25V2KX-1-DL-GP
PC4552
PC4554
PC4555
SC10U25V5KX-DL-GP
PWR_5V_PH
PWR_5V_VCC
PC4562
SC2D2U6D3V2MX-DL-GP
PWR_5V_EN2
PR4556
PR4557
499KR2F-1-GP
PR4558
499KR2F-1-GP
PC4564
PWR_5V_VOUT
PWR_5V_FB
PWR_5V_FB_A
PC4563
SC1KP50V2KX-1DLGP
PR4555
1KR2F-3-GP
PWR_5V_LDO
PC4551
SC4D7U6D3V2MX-1-GP
SY8288CRAC-GP
074.08288.0B43
PR4551
Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A
PL4502
COIL-1UH-104-GP
068.1R010.2141
PG4562
Do Not Stuff
Trace used 10 mil
TDC=8.62A
ICCMAX=6.034A
7.2408A<OCP<9.6544A
teknisi indonesia
5V_S5
PC4565
PC4556
PC4557
PC4558
PC4559
PC4560
PC4561
SC22U6D3V3MX-1-DL-GP
For 2cell use
EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 8A
SSID = PWR.Plane.Regulator_3D3V
TPS51393 For 3D3V
PWR_DCBATOUT_3D3V
PD4502
PG4515
PG4516
PG4517
PG4518
PR4560
PWR_3D3V_EN
PR4562
PWR_3D3V_PG
Vin Operating range : 4.5V~24V
Vin_Max : 26V
PR4501
PWR_3D3V_BOOT
PWR_3D3V_BOOT_A
PC4506
SCD1U25V2KX-1-DL-GP
PWR_3D3V_VCC
PC4522
SC2D2U10V3KX-1DLGP-U
PU4501
PC4501
SCD1U25V2KX-1-DL-GP
PC4502
PC4503
SC10U25V3MX-5-GP
PR4514
1MR2J-1-GP
PWR_3D3V_EN2
PWR_3D3V_FB
PWR_3D3V_PH
PWR_3D3V_LDO
PC4507
SC10U6D3V3MX-DL-GP
TPS51393PRJER-GP
074.51393.0A43
Place another side , make GND plan bigger
Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A
PL4501
COIL-1UH-104-GP
068.1R010.2141
TDC=7.11713A
ICCMAX=10.1009A
12.12108A<OCP<16.16144A
Design Current : 8A
3D3V_S5
PC4509
PC4510
PC4511
PC4513
PC4512
SC22U6D3V3MX-1-DL-GP
Close to PC4511
PG4530
Trace used 10 mil
PWR_3D3V_VOUT
PC4526
SC470P50V2KX-3DLGP
PWR_3D3V_FB2
PR4506
240KR2F-L-GP
PR4509
300KR2J-1-GP
PR4508
100KR2J-1-GP
EN rating :5.5V
EN Rising Threshold :1.5V
EN Falling Threshold : 0.4V
PR4505
3D3V_AUX_S5
PG4532
CBG X01 N Compare
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
POWER (SY8288_5V/3D3V)
A2
Cyborg TGL
SB
Date: Thursday, October 15, 2020
Sheet 45 of 105

Main Func = CPU_CORE

OFFPAGE

SVID

- 7 SVID_CLK_CPU
- 7 SVID_DATA_CPU
- 7 SVID_ALERT#_CPU

PR4631 Do Not Stuff
3,22,24,44,72 PROCHOT#_CPU — PWR_VCORE_VRHOT_R

44 CHGR_PSYS_IMVP — CHGR_PSYS_IMVP

20191119
check with Nakia need change netname to PWR_VCORE_VR_READY or not

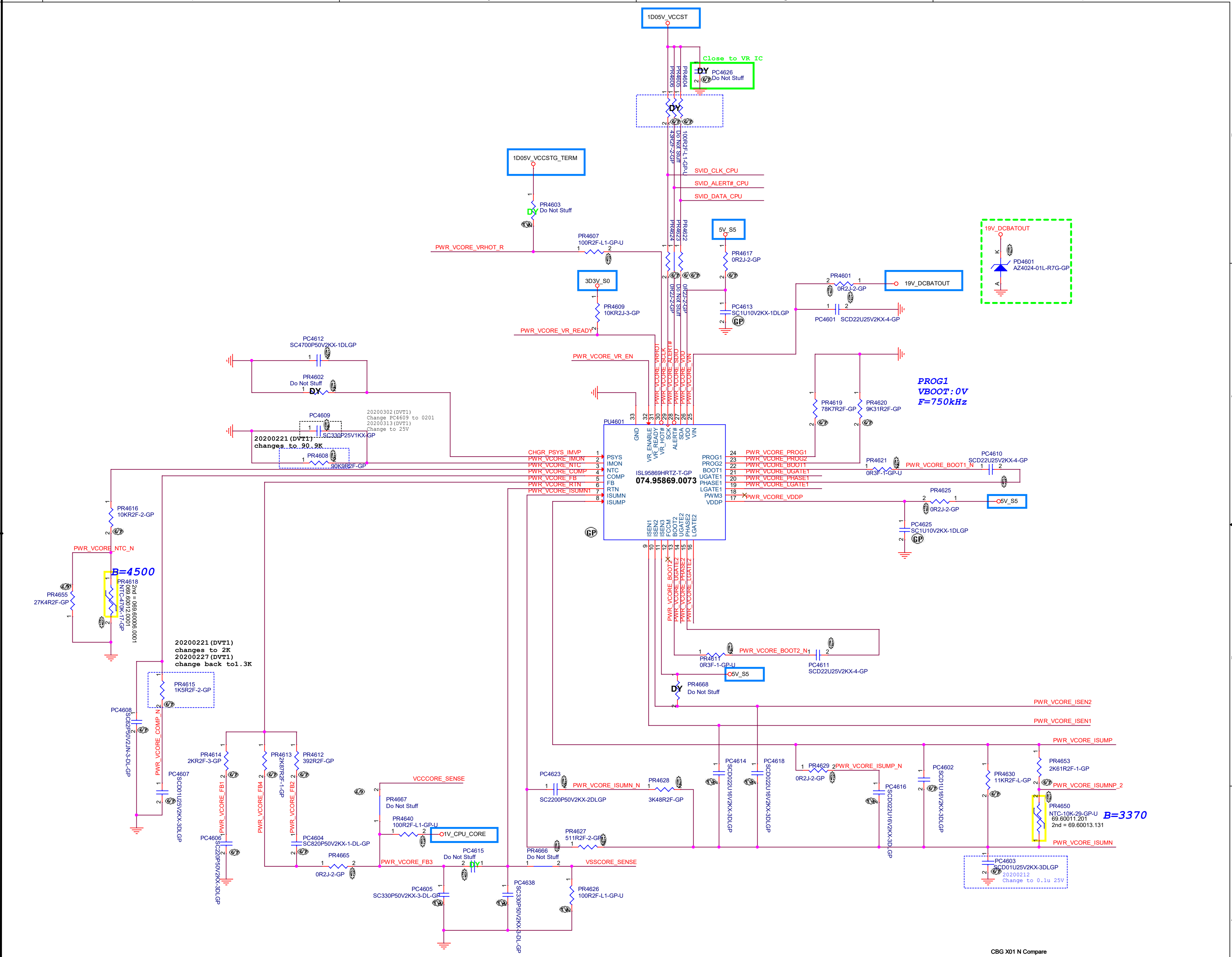
PR4636 Do Not Stuff
17,44 PWR_IMVP_PWRGD — PWR_VCORE_VR_READY

PR4635 Do Not Stuff
17,24,40,44 ALL_SYS_PWRGD — PWR_VCORE_VR_EN

VCORE SENSE

- 7 VSSCORE_SENSE — VSSCORE_SENSE
- 7 VCCCORE_SENSE — VCCCORE_SENSE

- 47 PWR_VCORE_UGATE1 — PWR_VCORE_UGATE1
- 47 PWR_VCORE_PHASE1 — PWR_VCORE_PHASE1
- 47 PWR_VCORE_LGATE1 — PWR_VCORE_LGATE1
- 47 PWR_VCORE_UGATE2 — PWR_VCORE_UGATE2
- 47 PWR_VCORE_PHASE2 — PWR_VCORE_PHASE2
- 47 PWR_VCORE_LGATE2 — PWR_VCORE_LGATE2
- 47 PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
- 47 PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
- 47 PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
- 47 PWR_VCORE_ISUMN — PWR_VCORE_ISUMN



CBG X01 N Compare

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Title	POWER (95869_CPUCORE(1/3))	
Size A2	Document Number: Cyborg TGL	Rev SB
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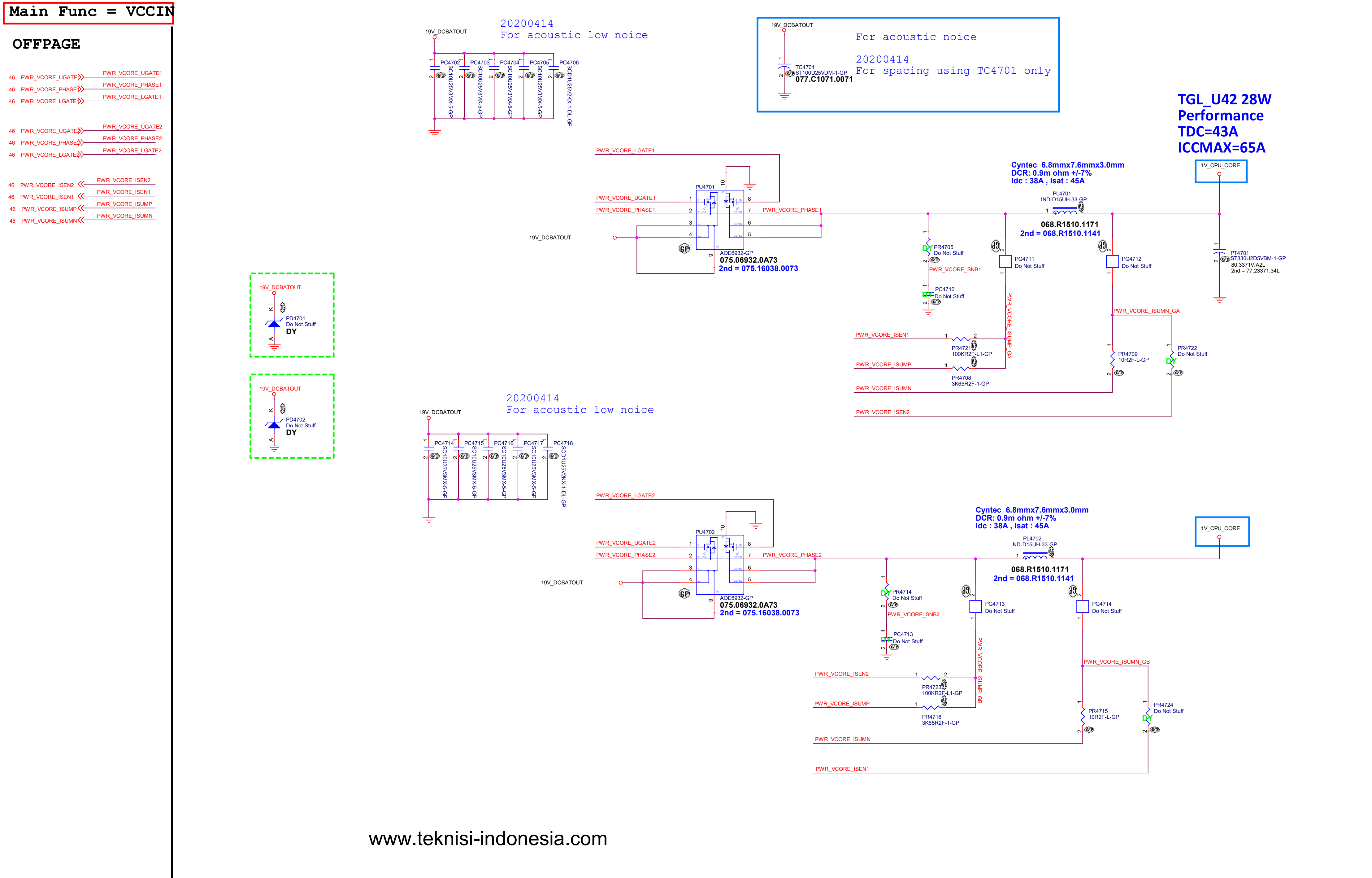

CBG X01 N Compare

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95829_CPUCORE(2/3))

Size: A2 | Document Number: Cyborg TGL | Rev: SB

Date: Thursday, October 15, 2020 | Sheet 47 of 105

Main Func = CPU_CORE

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Title *(RSVD)*		
Size **A**	Document Number *Cyborg TGL*	Rev *SB*
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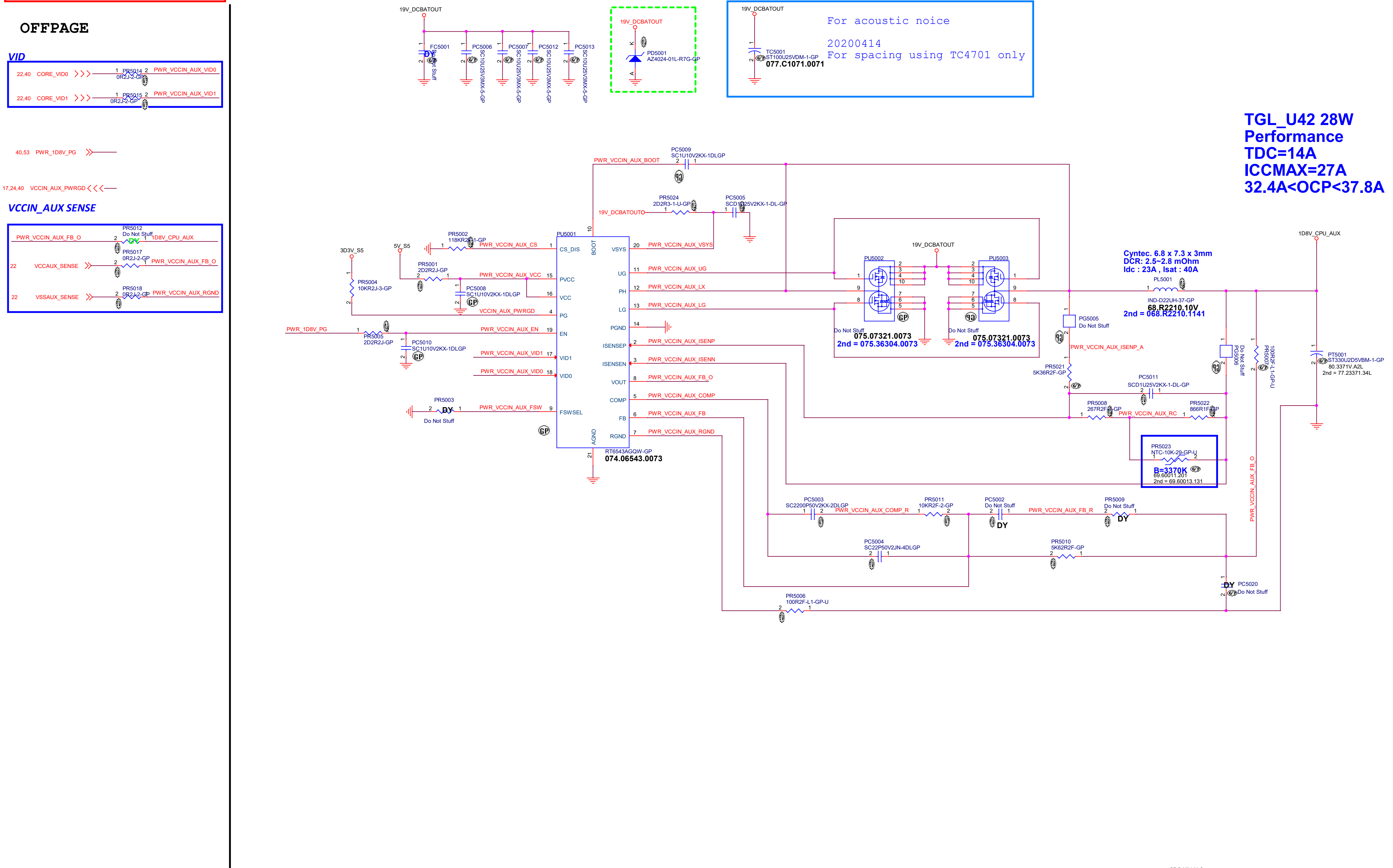
Main Func = VCCIN_AUX

OFFPAGE



CBG X01 N Compare

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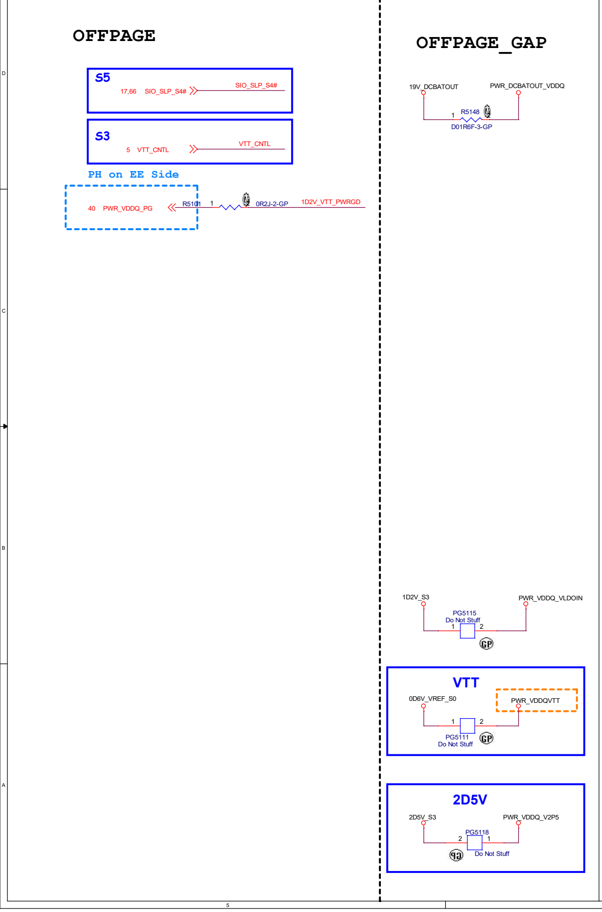
Title	RT6543A_VCCIN_AUX
Size A2	Document Number	Rev SB
Date: Thursday, October 15, 2020	Sheet 50 of 105



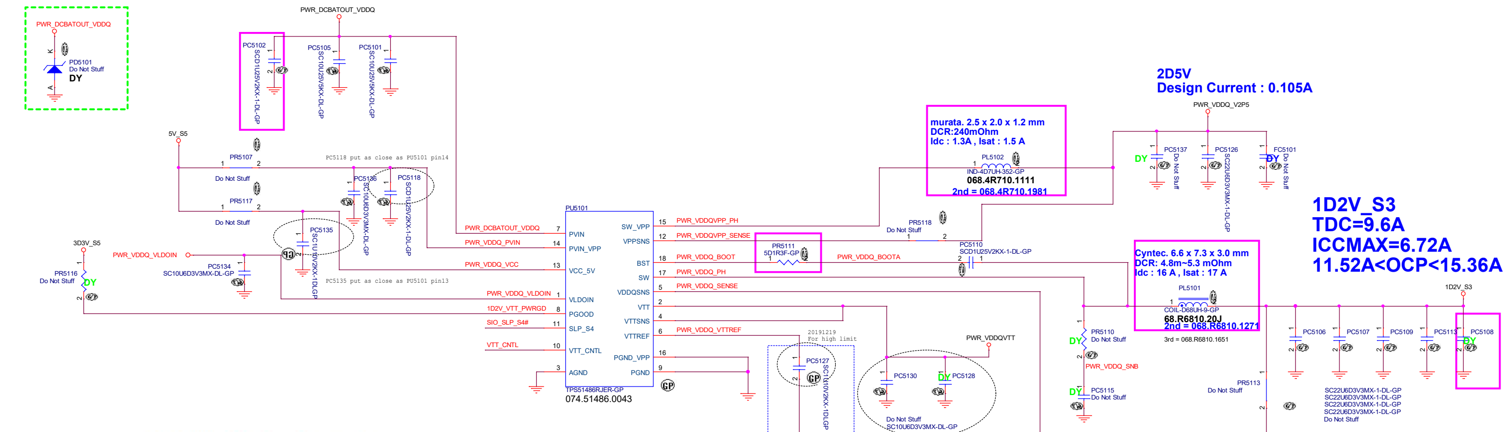


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

CBG X01 N Compare

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Title: 051_POWER (TPS51486R_VDDQ/VTT)

Size: Custom | Document Number: Cyborg TGL | Rev: SB

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SSID = PWR.Plane.Regulator_1D0V

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Title	POWER (AOZ2262Q_1D0V)	
Size A3	Document Number Cyborg TGL	Rev SB
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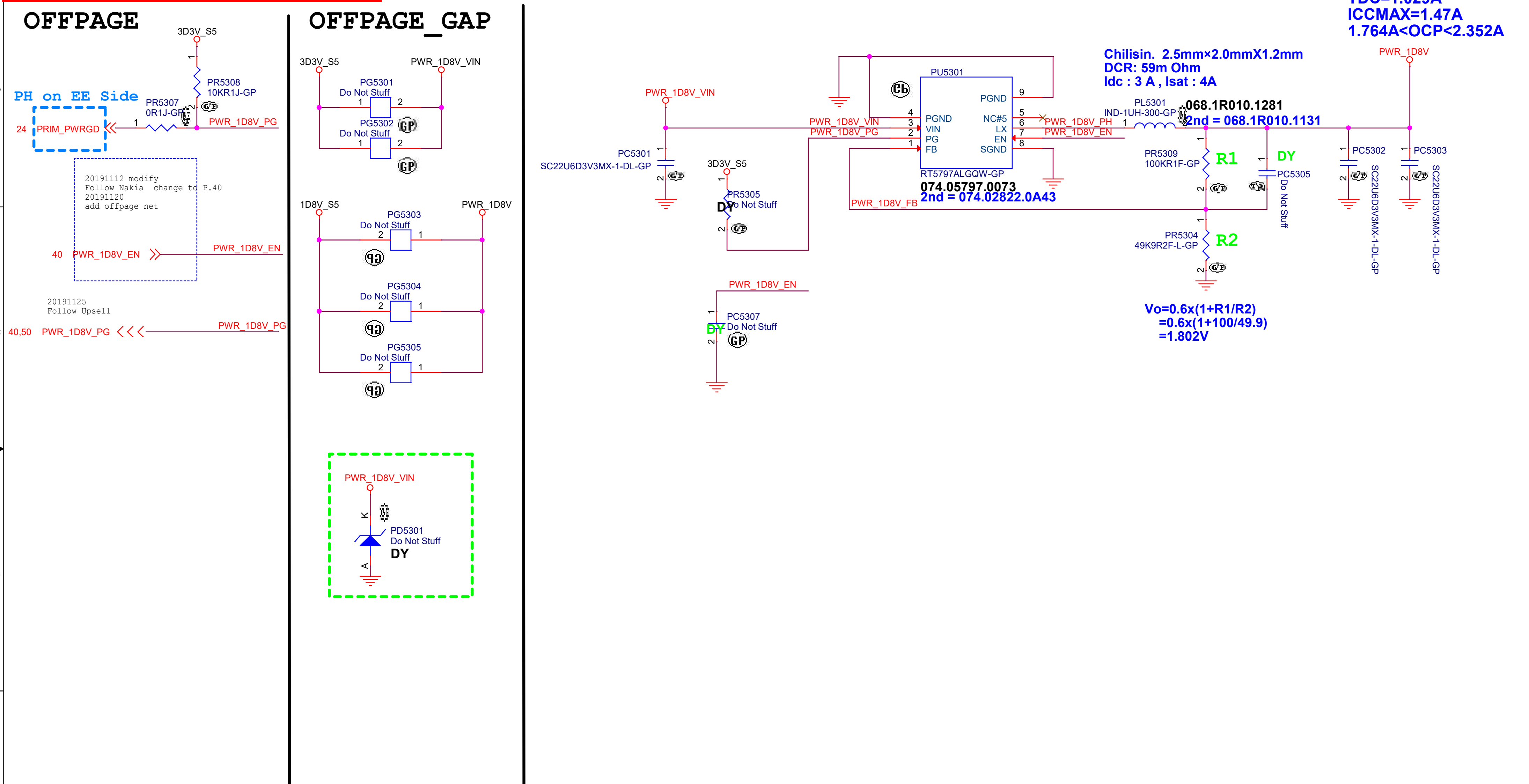
Main Func = 1D8V/1D2V



CBG X01 N Compare

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Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD&CAM&DMC&Touch	
Size B	Document Number Cyborg TGL	Rev SB
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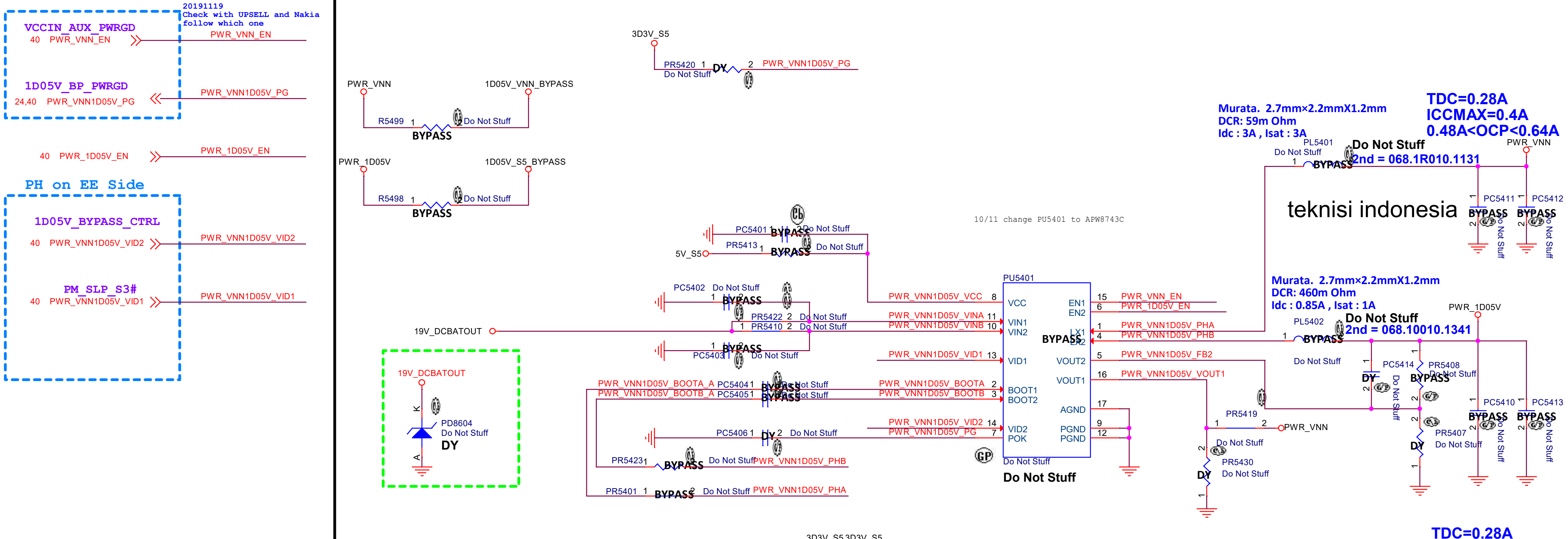
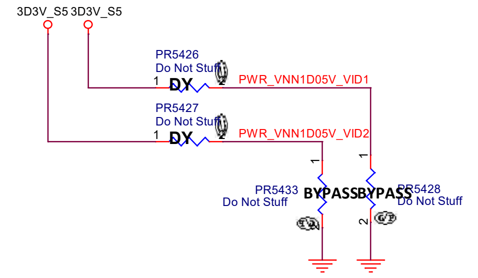
Main Func = 1D05V

OFFPAGE

OFFPAGE-GAP



TDC=0.28A
ICCMAX=0.4A
0.48A<OCP<0.64A



VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

CBG X01 N Compare

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Title: **POWER(APW8738A_VNN1D05)**

Size: A3 | Document Number: **Cyborg TGL** | Rev: SB

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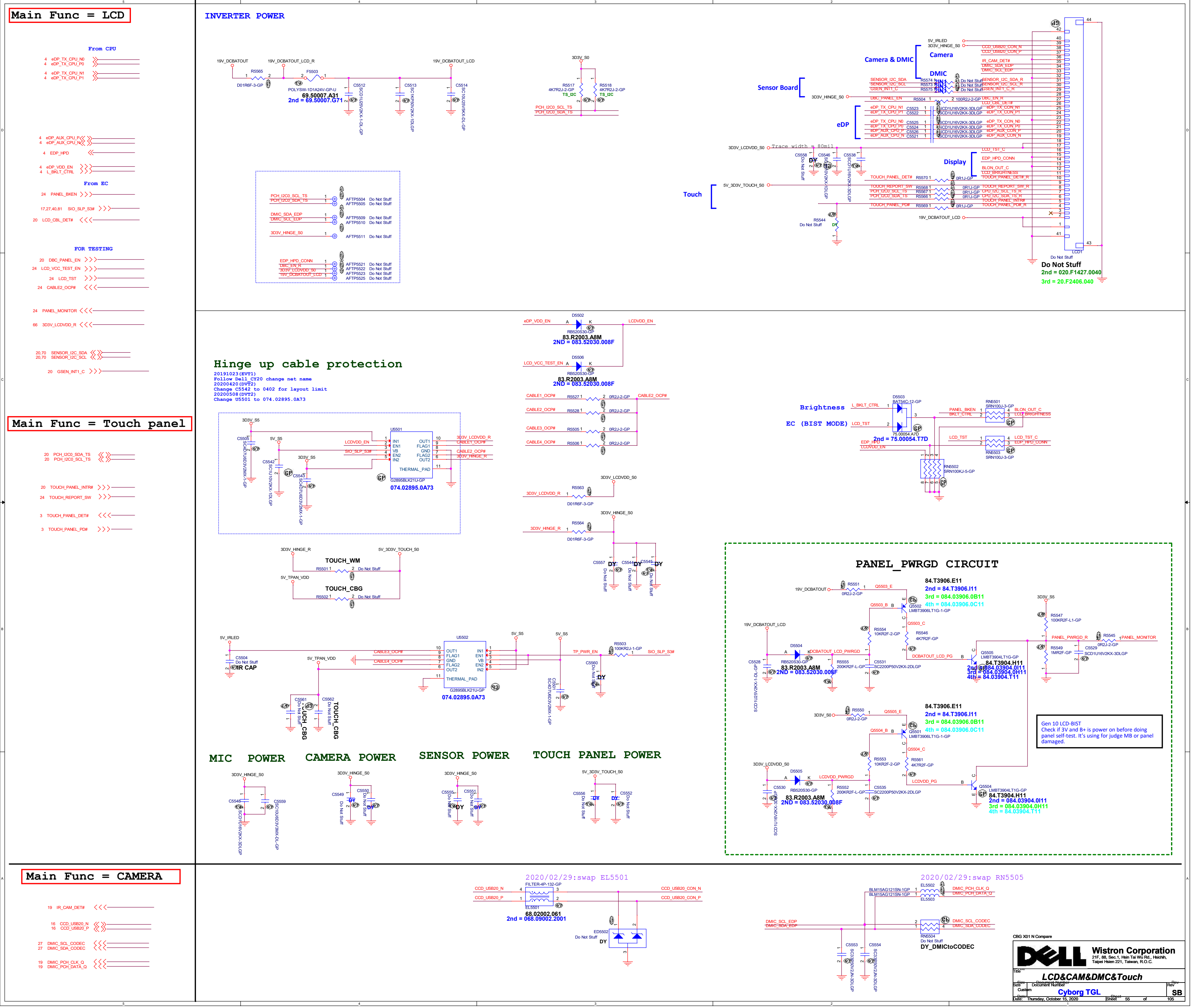
Main Func = LCD
From CPU
eDP_TX_CPU_N0
eDP_TX_CPU_P0
eDP_TX_CPU_N1
eDP_TX_CPU_P1
eDP_AUX_CPU_P
eDP_AUX_CPU_N
EDP_HPD
eDP_VDD_EN
L_BKLT_CTRL
From EC
PANEL_BKEN
SIO_SLP_S3#
LCD_CBL_DET#
FOR TESTING
DBC_PANEL_EN
LCD_VCC_TEST_EN
LCD_TST
CABLE2_OCP#
PANEL_MONITOR
3D3V_LCDVDD_R
SENSOR_I2C_SDA
SENSOR_I2C_SCL
GSEN_INT1_C
Main Func = Touch panel
PCH_I2C0_SDA_TS
PCH_I2C0_SCL_TS
TOUCH_PANEL_INTR#
TOUCH_REPORT_SW
TOUCH_PANEL_DET#
TOUCH_PANEL_PD#
Main Func = CAMERA
IR_CAM_DET#
CCD_USB20_N
CCD_USB20_P
DMIC_SCL_CODEC
DMIC_SDA_CODEC
DMIC_PCH_CLK_Q
DMIC_PCH_DATA_Q
INVERTER POWER
19V_DCBATOUT
19V_DCBATOUT_LCD_R
19V_DCBATOUT_LCD
69.50007.A31
2nd = 69.50007.G71
Camera & DMIC
Camera
DMIC
Sensor Board
eDP
Display
Touch
Trace width = 80mil
Do Not Stuff
2nd = 020.F1427.0040
3rd = 20.F2406.040
Hinge up cable protection
20191023(EVT1)
Follow Dell_CY20 change net name
20200420(DVT2)
Change C5542 to 0402 for layout limit
20200508(DVT2)
Change U5501 to 074.02895.0A73
074.02895.0A73
83.R2003.A8M
2ND = 083.52030.008F
Brightness
EC (BIST MODE)
2nd = 75.00054.T7D
TOUCH_WM
TOUCH_CBG
IR CAP
PANEL_PWRGD CIRCUIT
84.T3906.E11
2nd = 84.T3906.I11
3rd = 084.03906.0B11
4th = 084.03906.0C11
84.T3904.H11
2nd = 084.03904.0I11
3rd = 084.03904.0H11
4th = 84.03904.T11
Gen 10 LCD-BIST
Check if 3V and B+ is power on before doing panel self-test. It's using for judge MB or panel damaged.
MIC POWER
CAMERA POWER
SENSOR POWER
TOUCH PANEL POWER
2020/02/29:swap EL5501
68.02002.061
2nd = 068.09002.2001
2020/02/29:swap RN5505
DY_DMICtoCODEC
CBG X01 N Compare
Wistron Corporation
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Title
LCD&CAM&DMC&Touch
Size Custom
Document Number
Cyborg TGL
Rev SB
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Main Func = CRT

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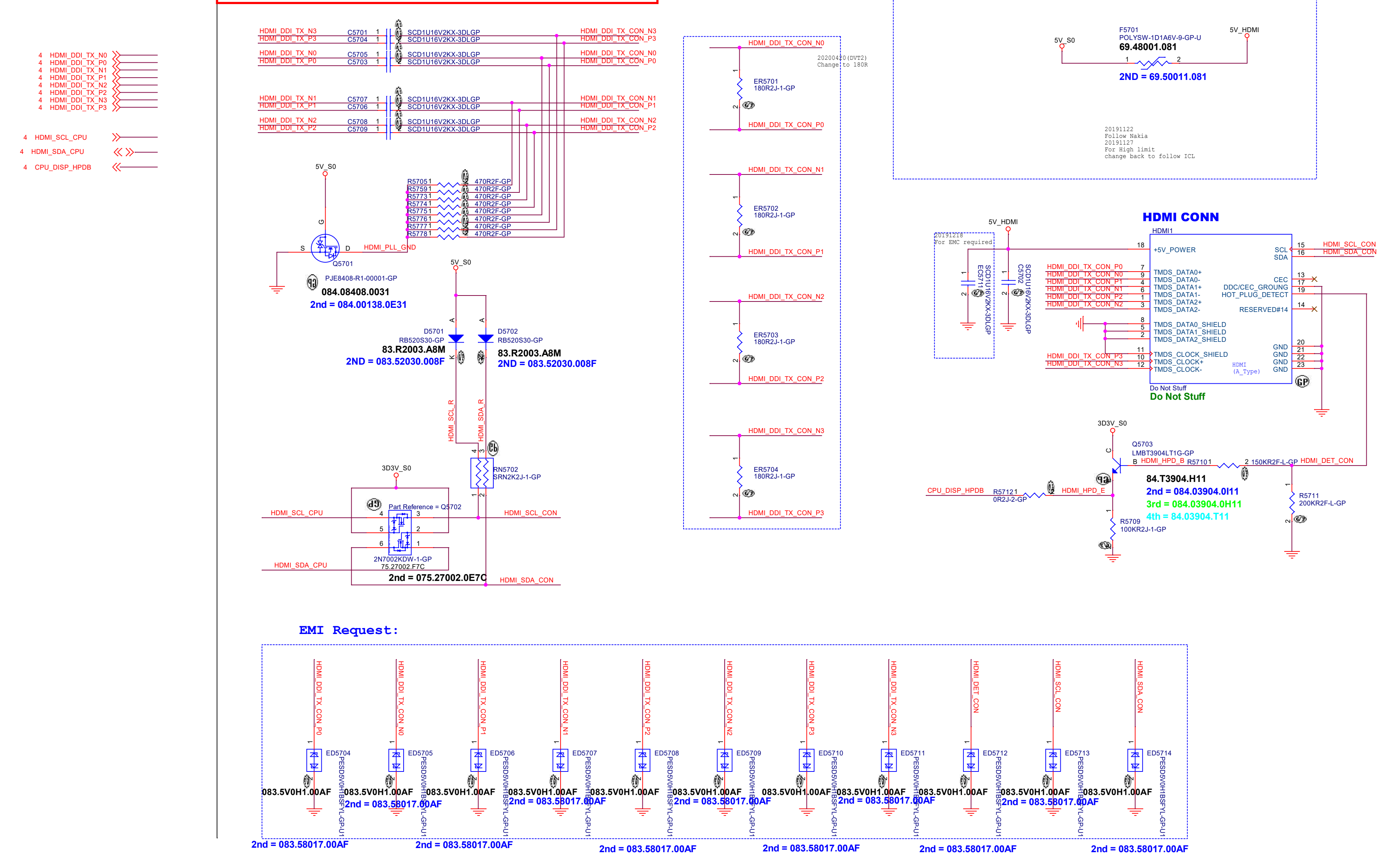
SSID = HDMI Level Shifter/Connector



CBG X01 N Compare

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Title	HDMI
Size: Custom	Document Number: Cyborg TGL
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(Blanking)

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Title		
(Reserved)		
Size: A4	Document Number: *Cyborg TGL*	Rev: *SB*
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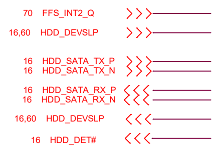
(Blanking)

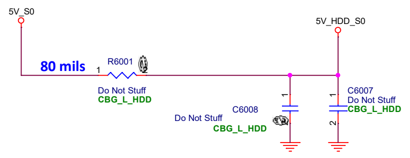
Main Func = HDD

HDD



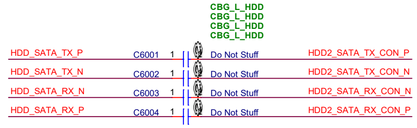
HDD POWER

For CBG L

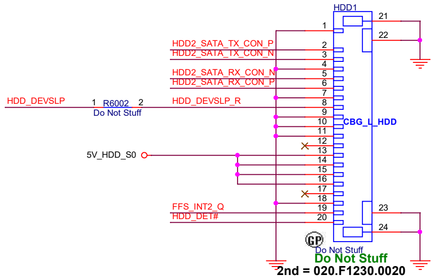


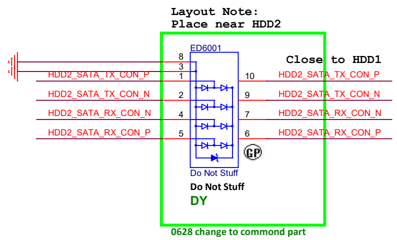
SATA RE-DRIVER

20201013
Remove



SATA HDD Connector





CBG X01 N Compare

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Title: **SATA IF_HDD/ODD**

Size: A2 | Document Number: **Cyborg TGL** | Rev: **SB**

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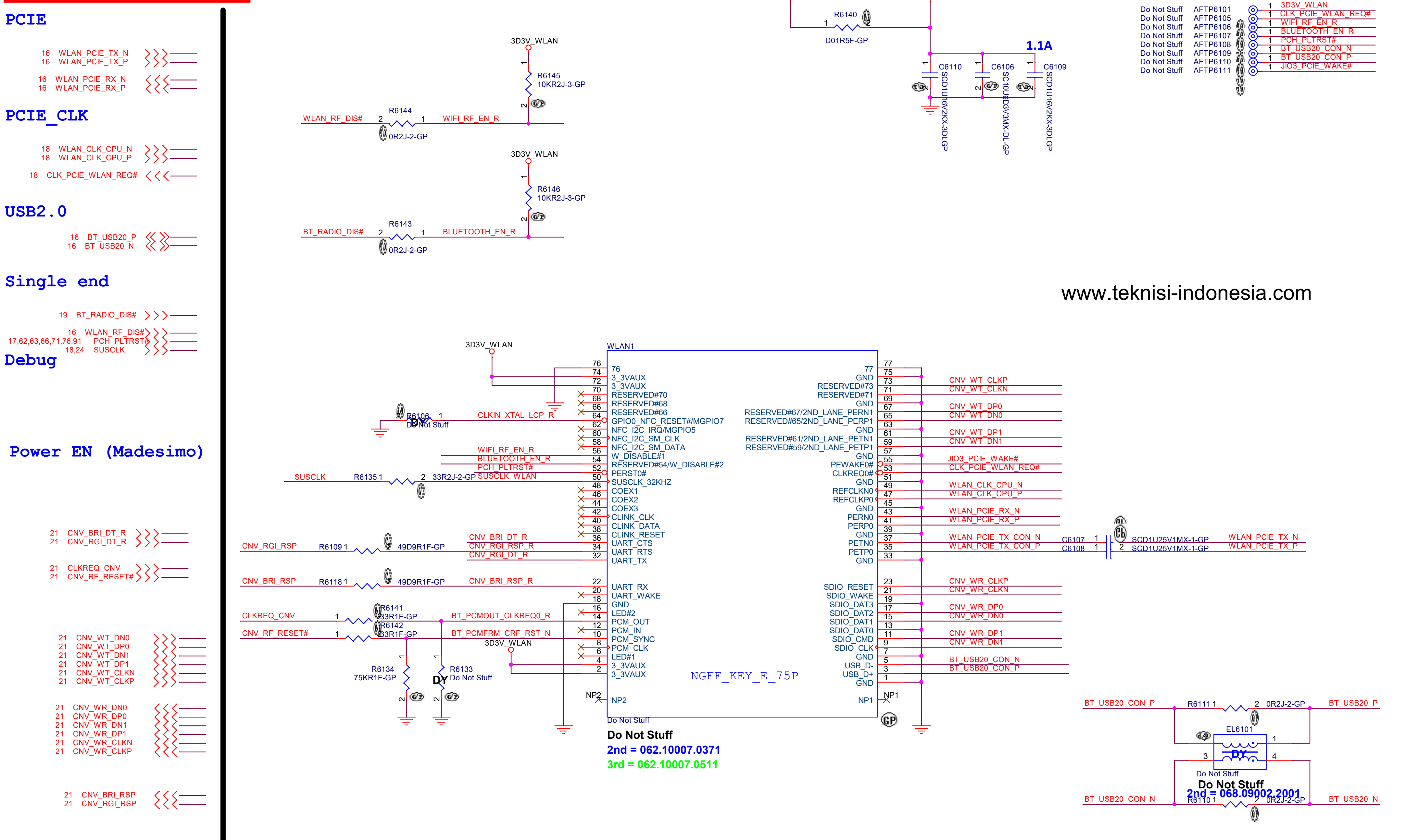
Main Func = WLAN



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CBG X01 N Compare

Wistron Corporation
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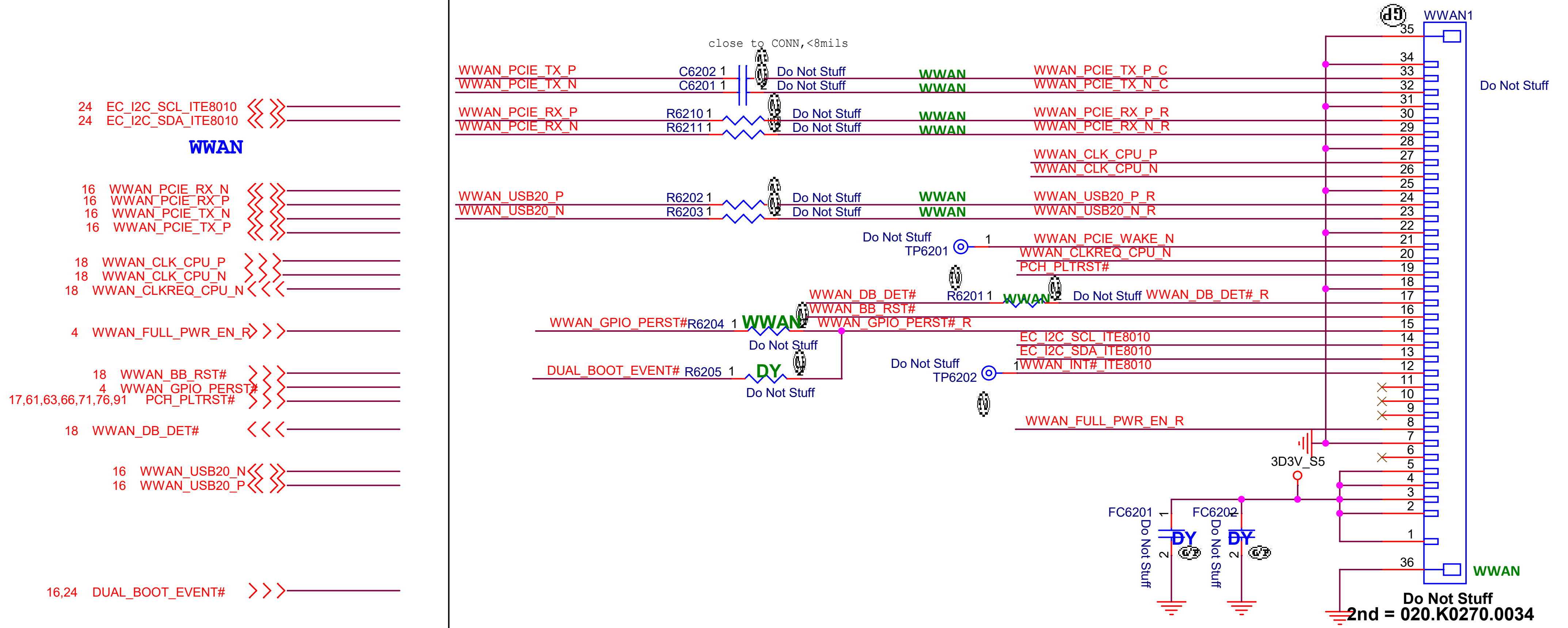
Title: NGFF_WLAN CONN

Size: A3 | Document Number: Cyborg TGL | Rev: SB

Date: Thursday, October 15, 2020 | Sheet 61 of 105

Main Func = WWAN

For CBG L



CBG X01 N Compare

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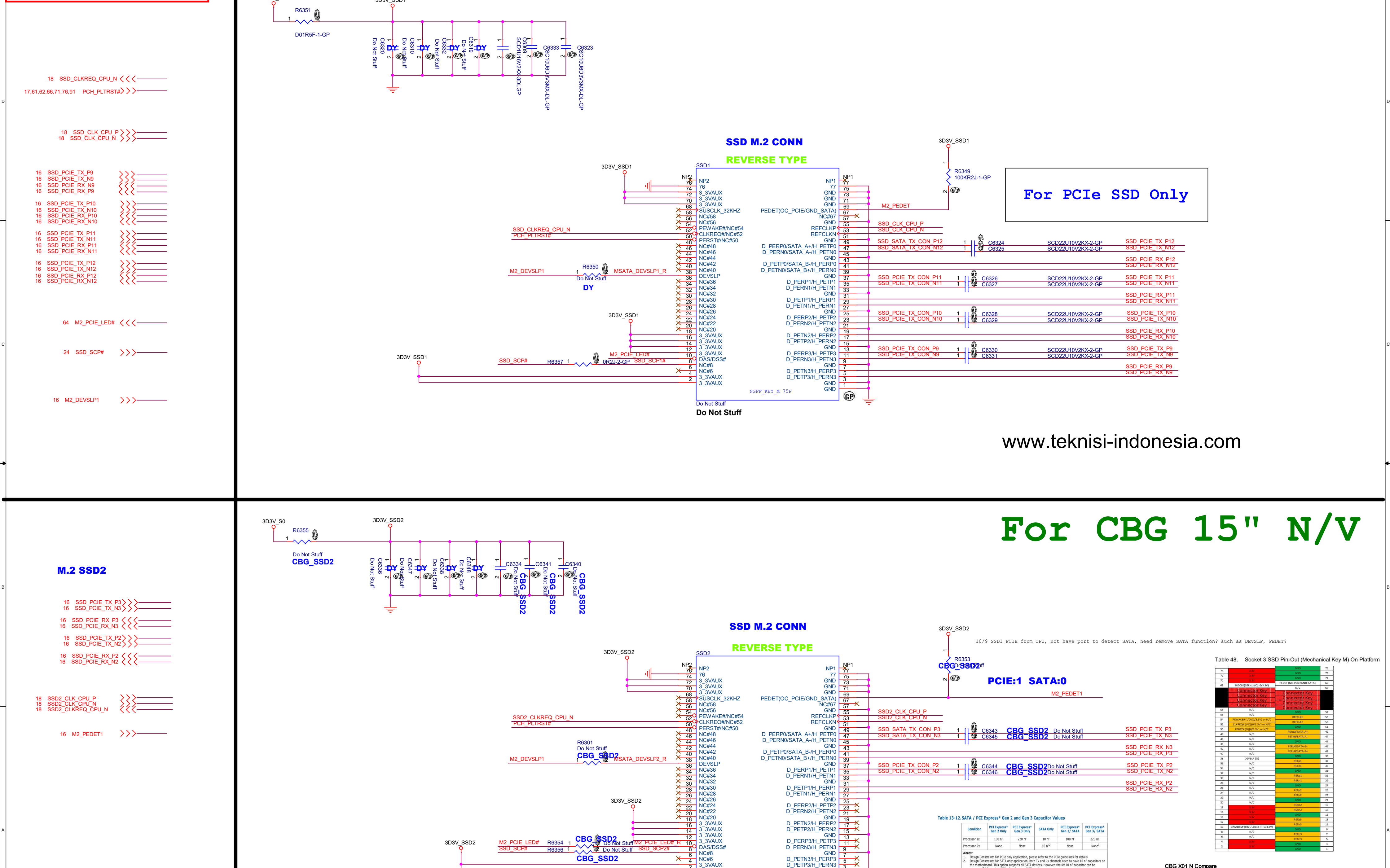
Title	WWAN	
Size A4	Document Number Cyborg TGL	Rev SB
Date: Thursday, October 15, 2020	Sheet 62 of 105	

Main Func = M.2 SSD



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Title	mSATA	
Size A2	Document Number: Cyborg TGL	Rev SB
Date: Thursday, October 15, 2020	Sheet 63 of 105	

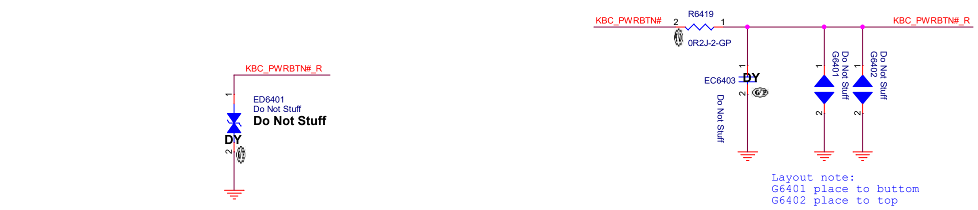
NONE FINGER PRINT 才會上件

Main Func = Power BTN

24 KBC_PWRBTN# <<<

66 KBC_PWRBTN#_R <<<

Power button



Main Func = Battery LED

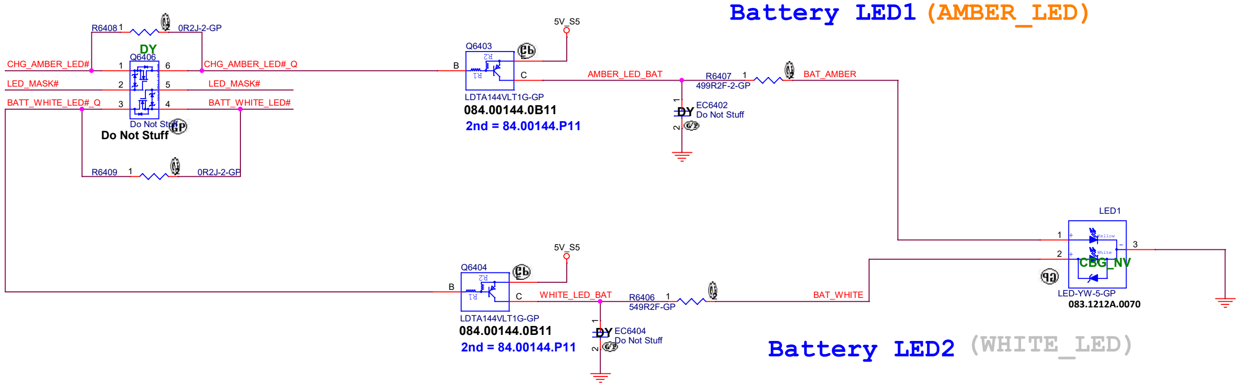
Low actived from KBC GPIO

24 LED_MASK# >>>

24 CHG_AMBER_LED# >>>

20,24 BATT_WHITE_LED# >>>

Battery LED1 (AMBER_LED)



Battery LED2 (WHITE_LED)

Main Func = HDD LED

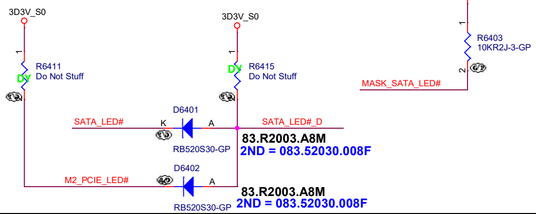
20,24 MASK_SATA_LED# >>>

18 SATA_LED# >>>

63 M2_PCIE_LED# <<<

20 SATA_LED#_D <<<

SATA HDD LED
LOW actived from PCH GPIO

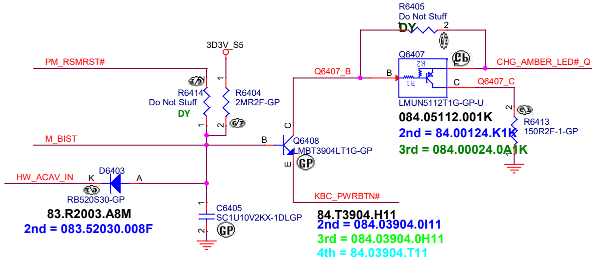


Main Func = M-BIST

17 PM_RSMRST# >>>

24 M_BIST >>>

24,44 HW_ACAV_IN >>>



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button.
There is a LED will light up to indicate the MB is damage by

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Title	LED Board&Power Button	
Size A2	Document Number Cyborg TGL	Rev SB
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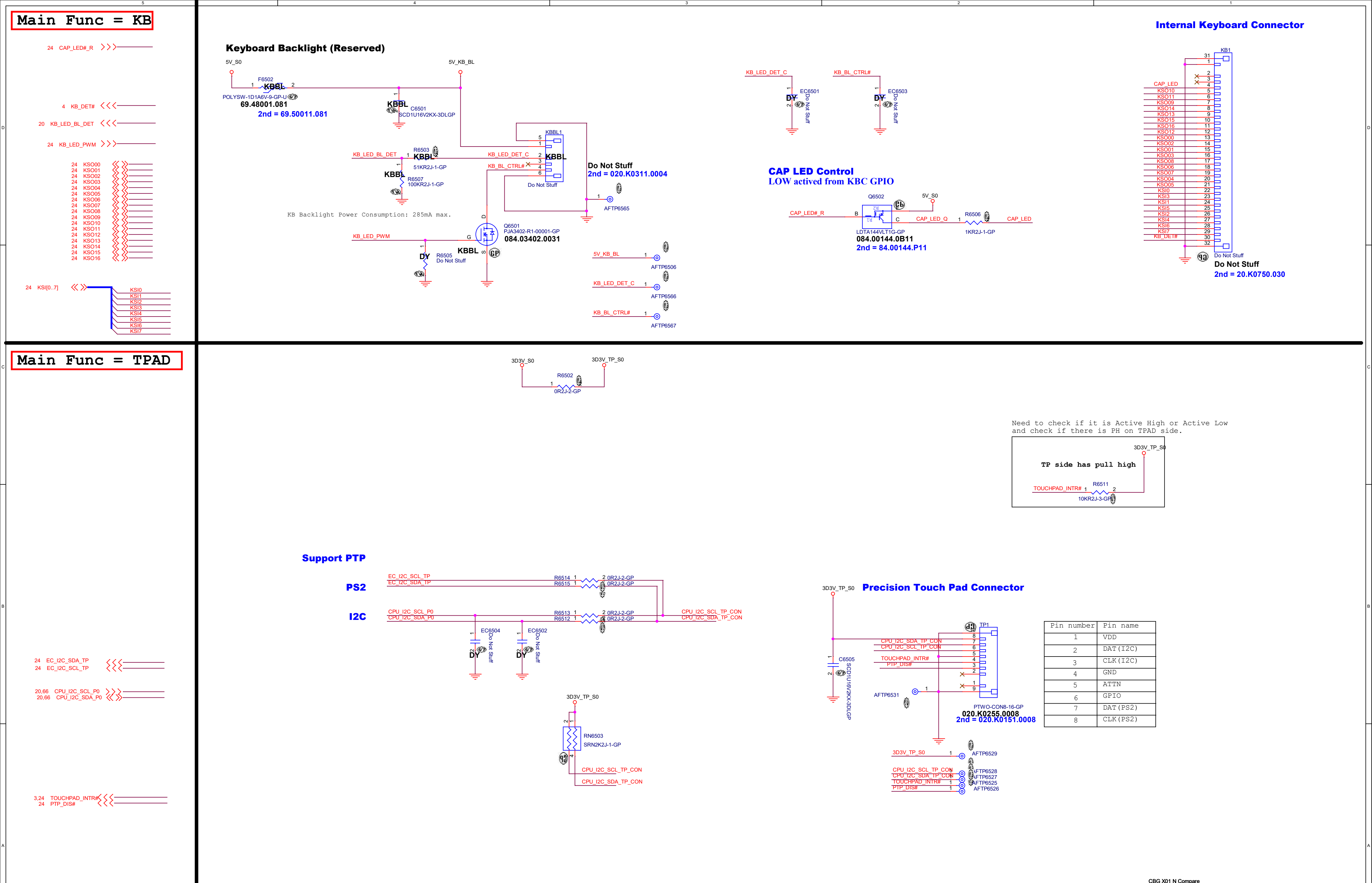

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

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Title: Key Board&Touch Pad

Size: A2 | Document Number: Cyborg TGL | Rev: SB

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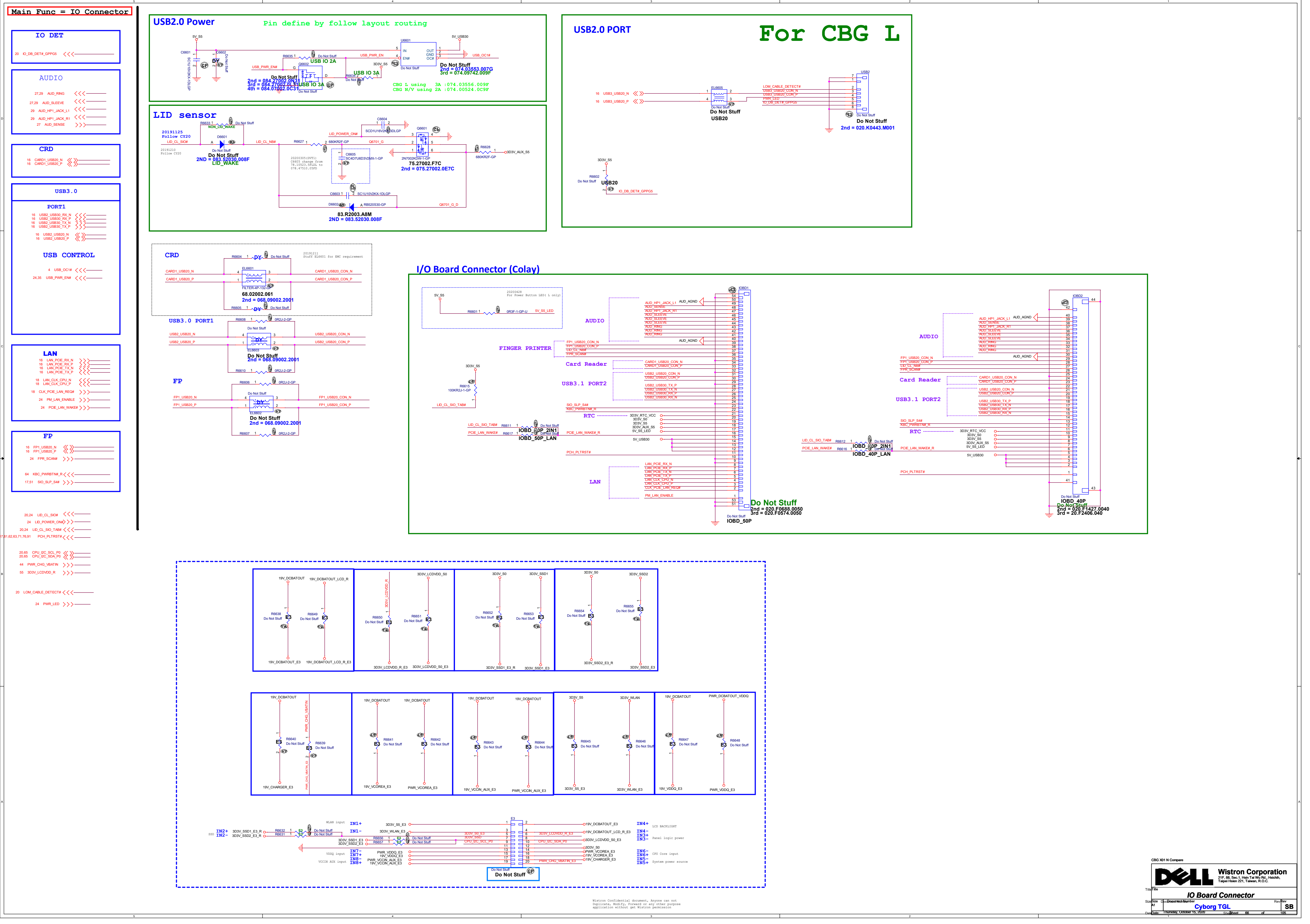

Main Func = IO Connector
IO DET
AUDIO
CRD
USB3.0
PORT1
USB CONTROL
LAN
FP
USB2.0 Power
Pin define by follow layout routing
USB IO 2A
USB IO 3A
CBG L using 3A :074.03556.009F
CBG N/V using 2A :074.00524.0C9F
LID sensor
USB2.0 PORT
For CBG L
CRD
USB3.0 PORT1
FP
I/O Board Connector (Colay)
AUDIO
FINGER PRINTER
Card Reader
USB3.1 PORT2
RTC
LAN
Do Not Stuff
IOBD_50P
IOBD_40P
IOBD_50P_LAN
IOBD_40P_LAN
IN1+
IN1-
IN2+
IN2-
IN3+
IN3-
IN4+
IN4-
IN5-
IN5+
IN6-
IN6+
IN7-
IN7+
IN8-
IN8+
LCD BACKLIGHT
Panel logic power
CPU Core input
System power source
WLAN input
VDDQ input
VCCIN AUX input
SSD
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
IO Board Connector
Cyborg TGL
SB
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Main Func = HALL SENSOR

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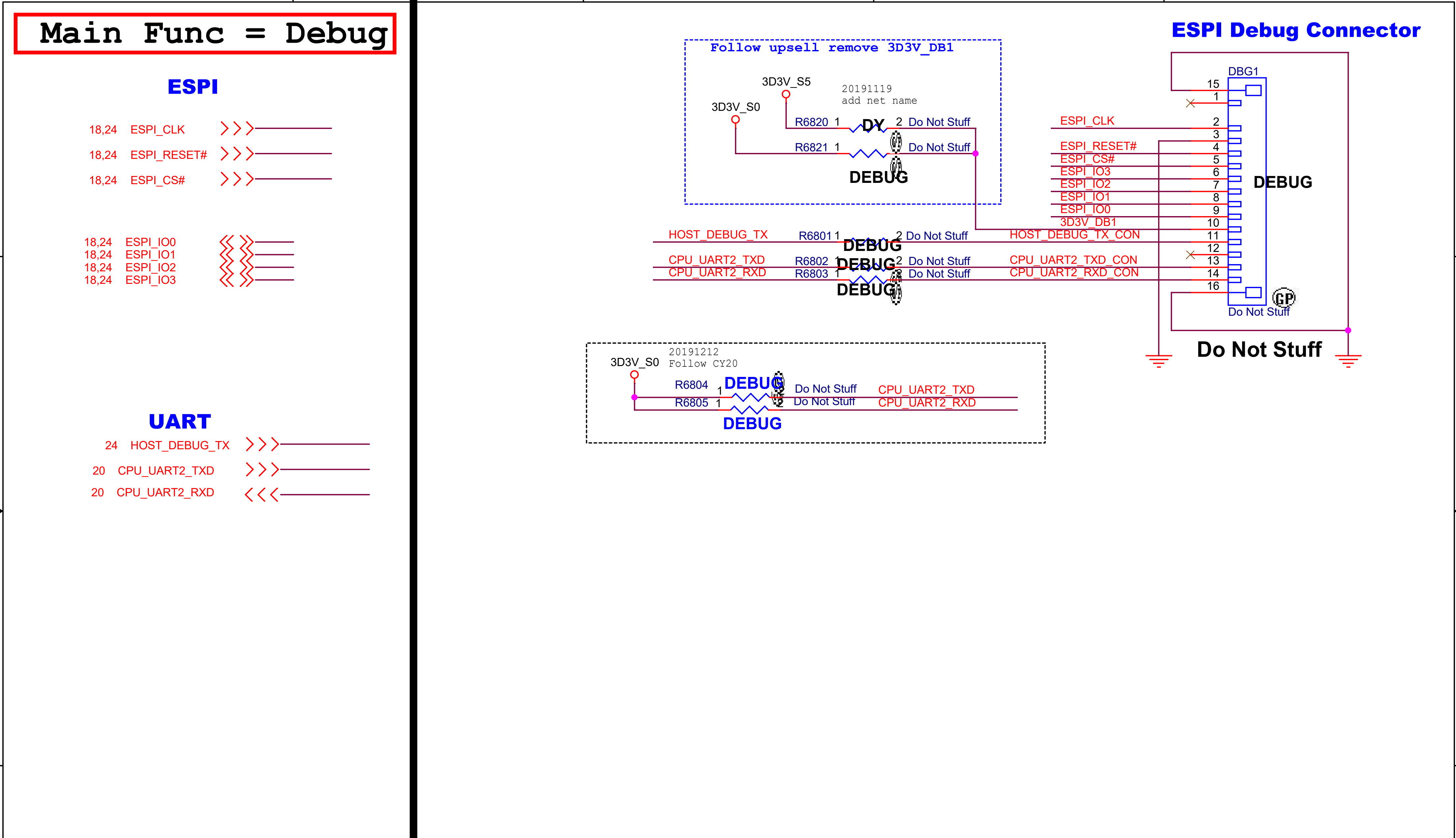

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Title	*Dubug connector*	
Size A4	Document Number *Cyborg TGL*	Rev *SB*
Date: Thursday, October 15, 2020	Sheet 68 of 105	

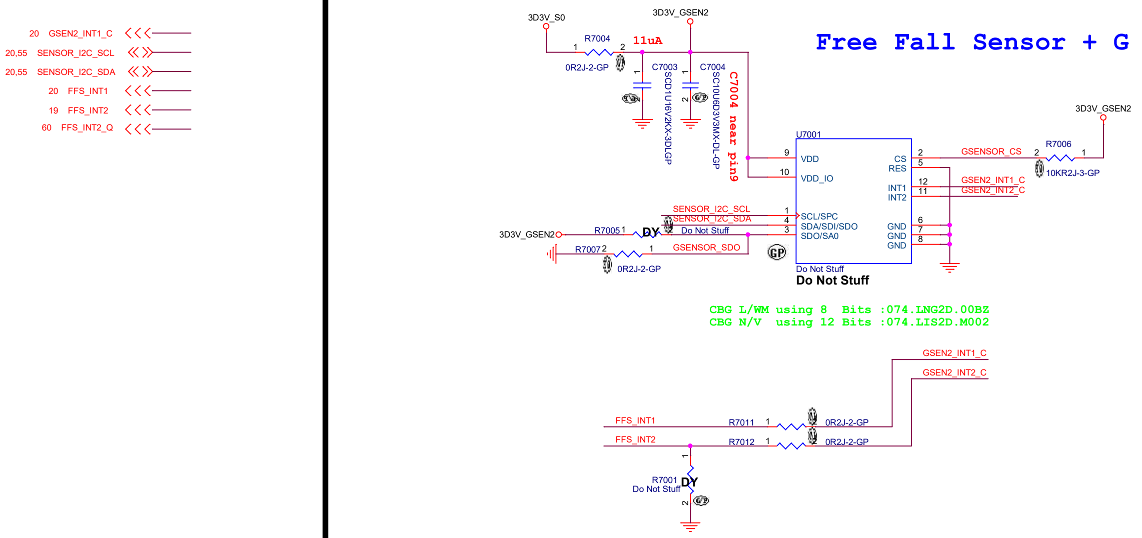
(Blanking)

SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

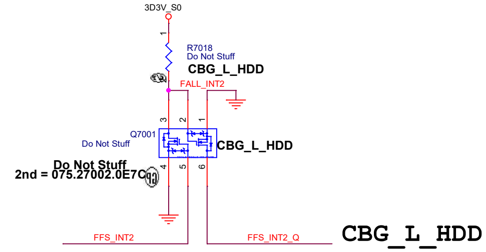
The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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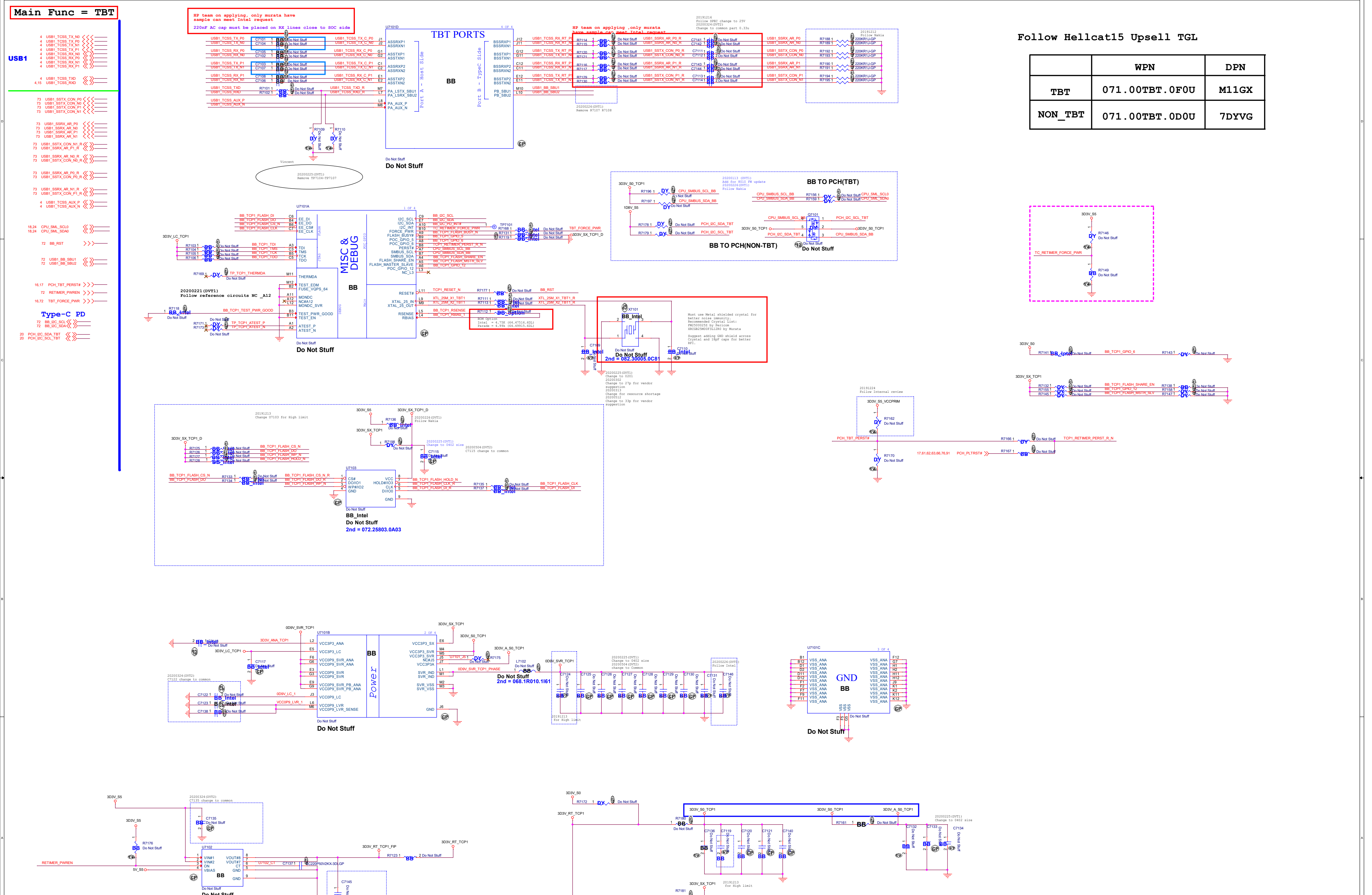
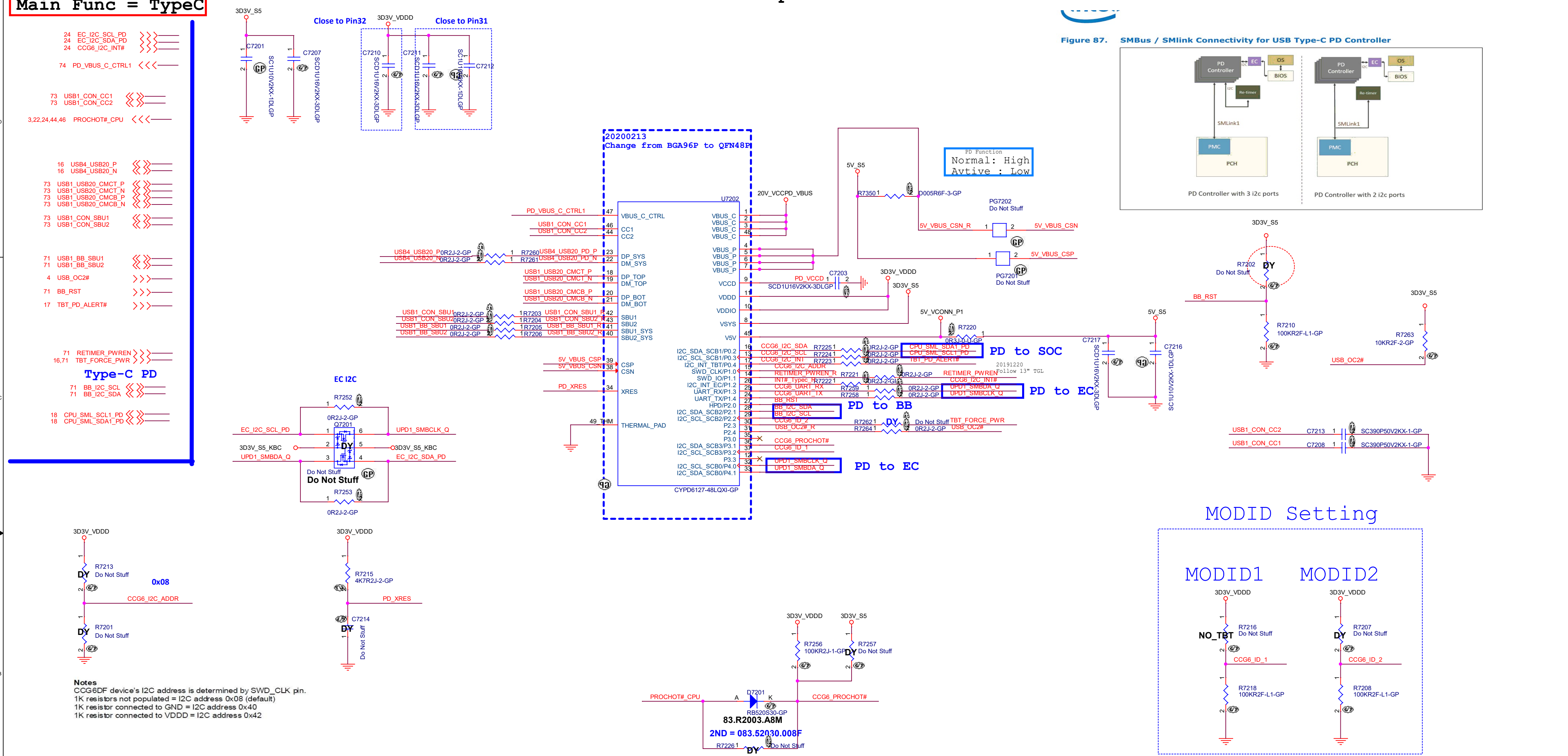
Title	Free Fall Sensor	
Size A2	Document Number Cyborg TGL	Rev SB
Date: Thursday, October 15, 2020	Sheet 70 of 105	



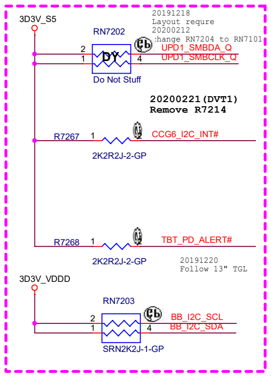
Follow Hellcat15 Upsell TGL

	WPN	DPN
TBT	071.00TBT.0F0U	M11GX
NON_TBT	071.00TBT.0D0U	7DYVG

Follow Hellcat15 Upsell TGL



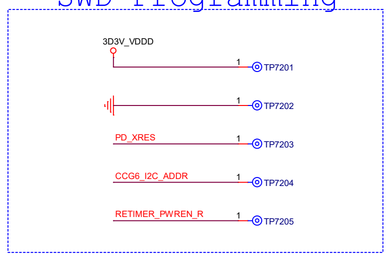
Notes
CCG6DF device's I2C address is determined by SWD_CLK pin.
1K resistors not populated = I2C address 0x08 (default)
1K resistor connected to GND = I2C address 0x40
1K resistor connected to VDDD = I2C address 0x42



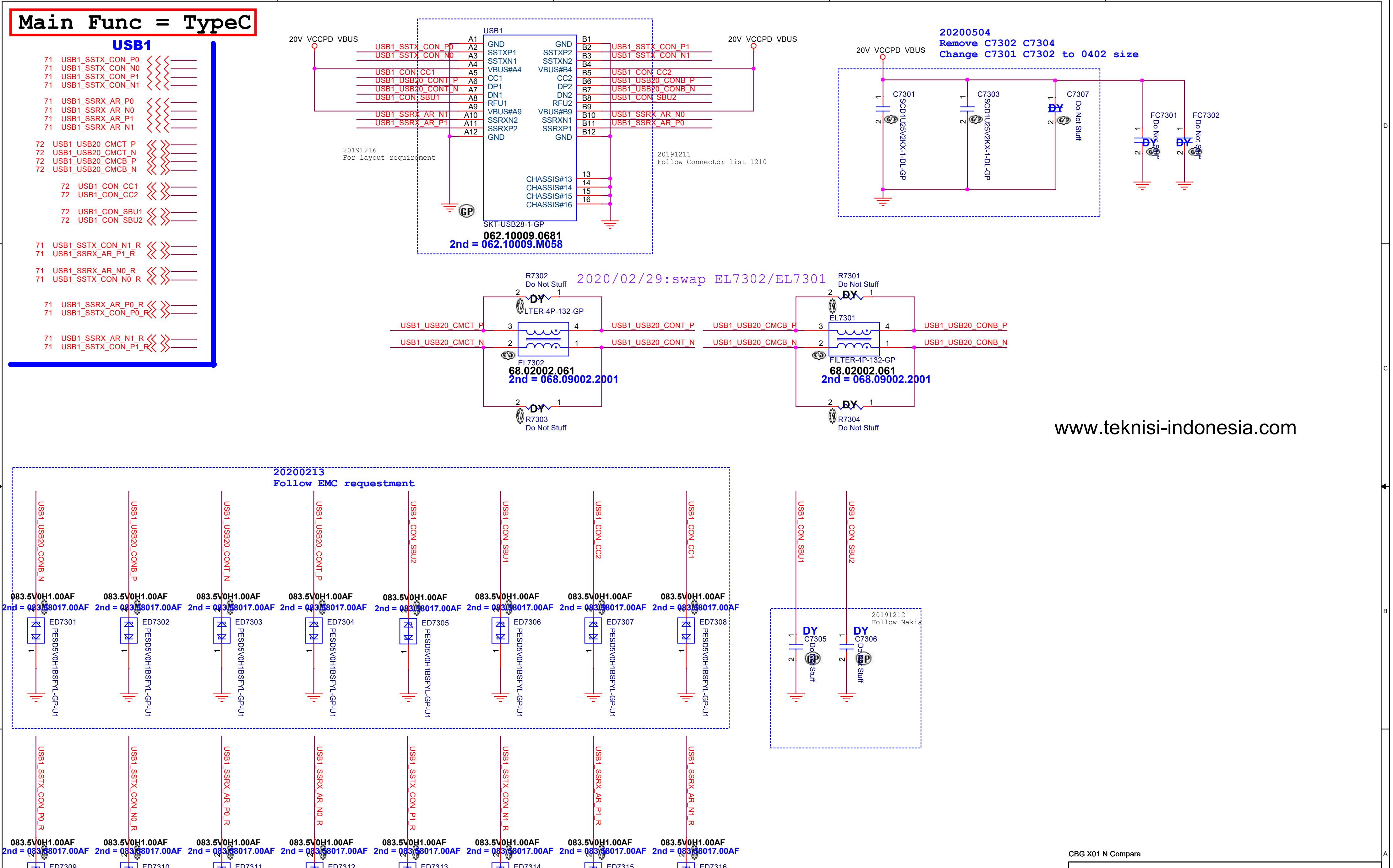
	Dell TGL Platform MOD_ID Options		
MUX	MOD_ID1	MOD_ID2	Description
BB8040R	L0	L0/Reserved	TBT Configuration w/BB Retimer
Two BB8040R	L1	L0	TBT Configuration w/BB Retimer - 2 retimers per port (Stradale)
BB8010R	L2	L0/Reserved	non-TBT Configuration w/BB Retimer
Maple Ridge	L4	L0	TBT Configuration w/Maple Ridge
TUSB546/1046	L6	L0	TUSB546 Equalizer config #1
TUSB546/1046	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved
PS8802	L6	L4 - L5	MFDP
PS8828	L7	L0 - L2	For Non-TBT (with USB4), PTP with BB 8010
PS8830	L7	L3 - L5	For TBT (with USB4), PTP with BB 8040

	CCG6_ID	R7216	R7218	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.10035.6DL (100K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

SWD Programming



CBG X01 N Compare



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Title	EXT IO (Thunderbolt(3/3)/Type C Conn)
Size	A3
Document Number	Cyborg TGL
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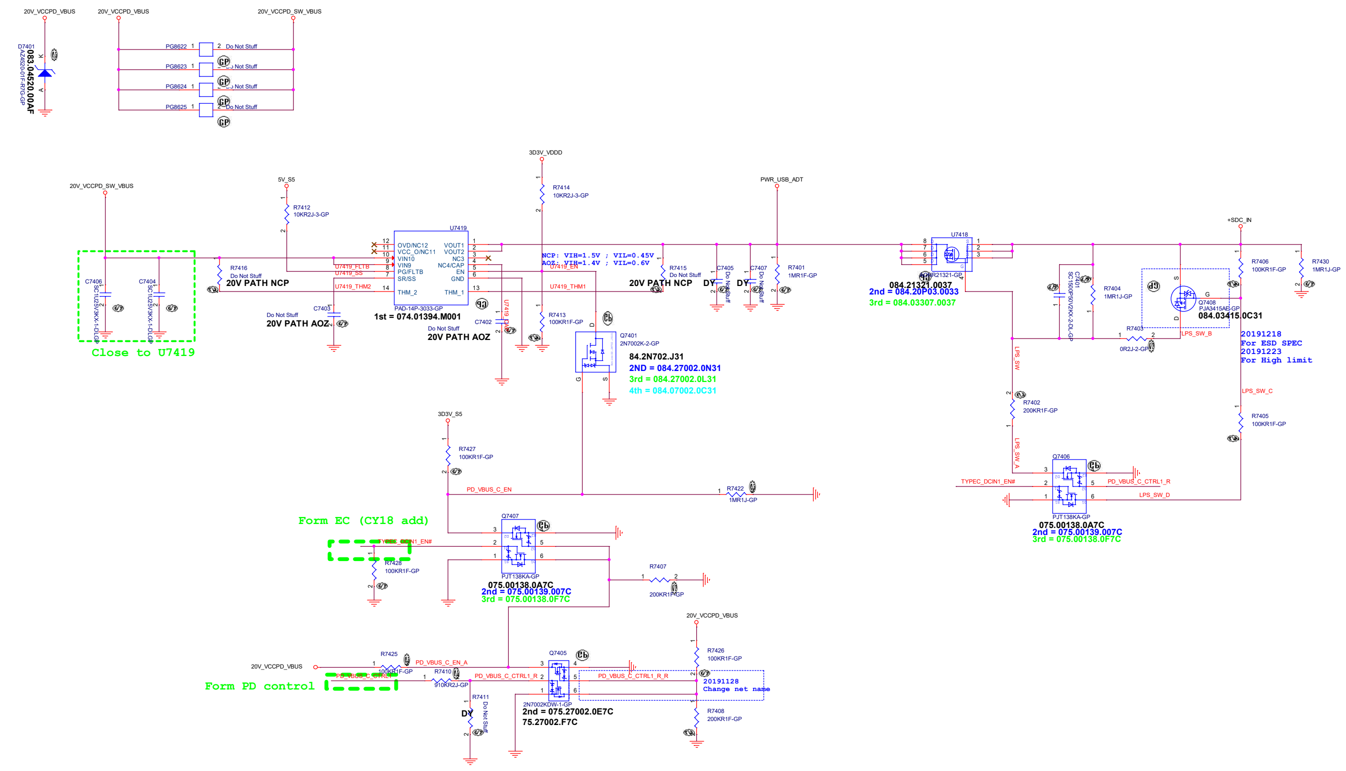
72 PD_VBUS_C_CTRL1
24 TYPEC_DCIN1_EN#
44 U7419_FLTB



CBG X01 N Compare

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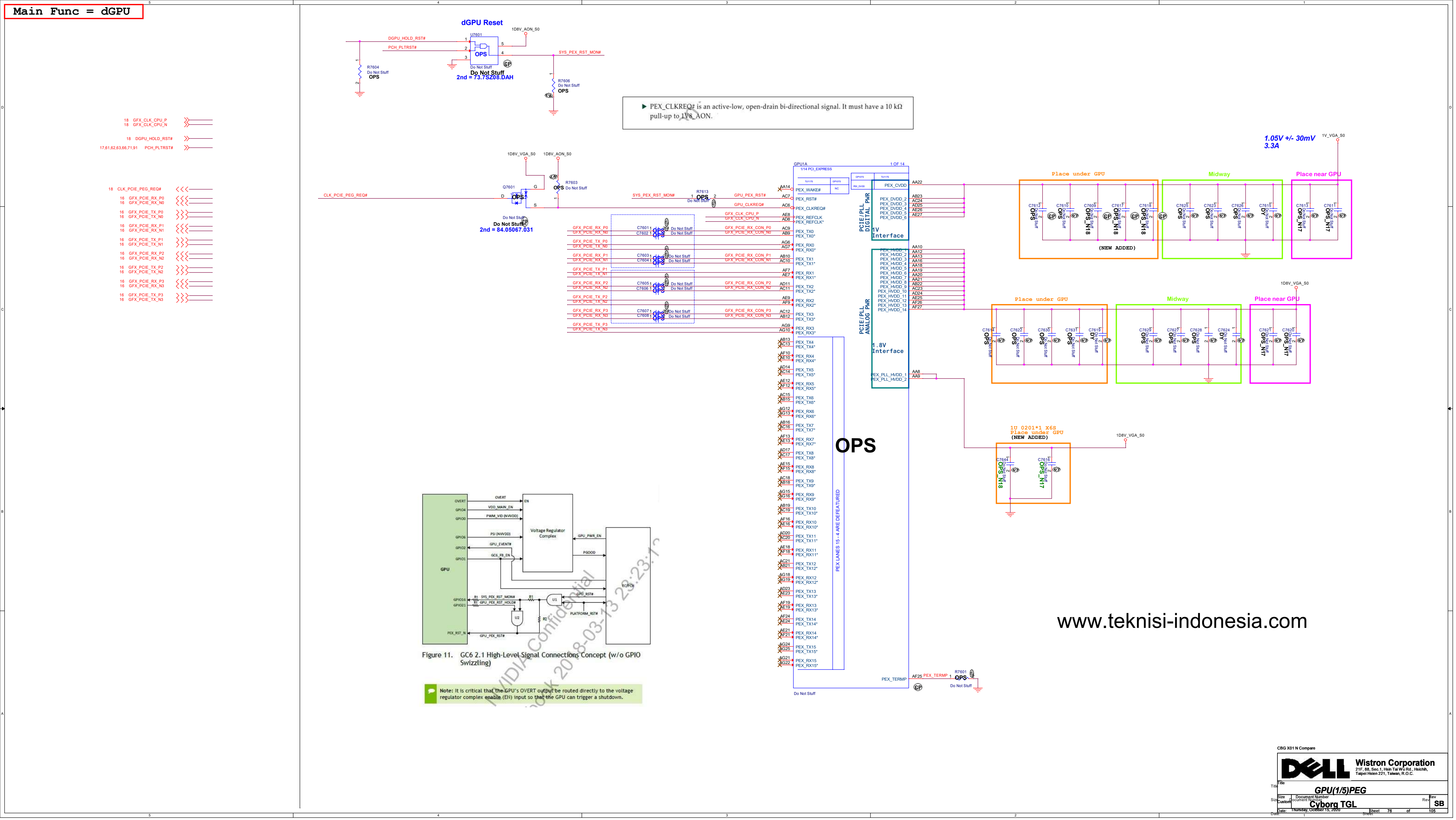
Title	GPU(2/5)DIGITALOUT
Size A1	Document Number Cyborg TGL	Rev SB
Date: Thursday, October 15, 2020	Sheet 74 of 105

(Blanking)



Main Func = dGPU
dGPU Reset
DGPU_HOLD_RST#
PCH_PLTRST#
SYS_PEX_RST_MON#
1D8V_AON_S0
U7601
OPS
Do Not Stuff
2nd = 73.7SZ08.DAH
R7604
R7606
PEX_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 kΩ pull-up to 1V8_AON.
GFX_CLK_CPU_P
GFX_CLK_CPU_N
CLK_PCIE_PEG_REQ#
1D8V_VGA_S0
Q7601
R7603
2nd = 84.05067.031
R7613
GPU_PEX_RST#
GPU_CLKREQ#
GPU1A
1/14 PCI_EXPRESS
1 OF 14
PCIE/PLL DIGITAL PWR
1V Interface
PCIE/PLL ANALOG PWR
1.8V Interface
PEX LANES 15 - 4 ARE DEFEATURED
OPS
PEX_TERMP
R7601
1.05V +/- 30mV
3.3A
1V_VGA_S0
Place under GPU
Midway
Place near GPU
(NEW ADDED)
1U 0201*1 X6S
Place under GPU
(NEW ADDED)
OVERT
VDD_MAIN_EN
PWM_VID (NVVDD)
PSI (NVVDD)
GPU_EVENT#
GC6_FB_EN
Voltage Regulator Complex
GPU_PWR_EN
PGOOD
GPU
PEX_RST_N
GPU_PEX_RST#
PLATFORM_RST#
Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)
Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.
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DELL
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GPU(1/5)PEG
Cyborg TGL
SB
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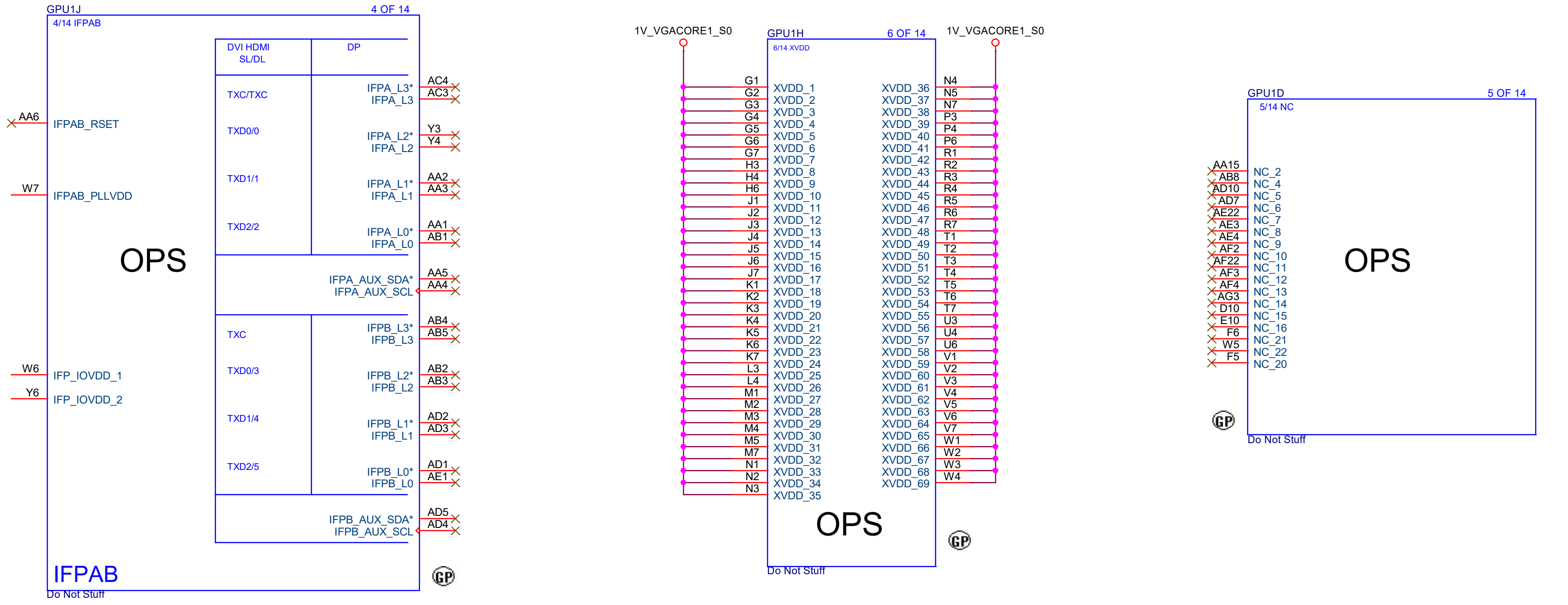
Main Func = dGPU



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Title	GPU(2/5)DIGITALOUT	
Size A3	Document Number Cyborg TGL	Rev SB
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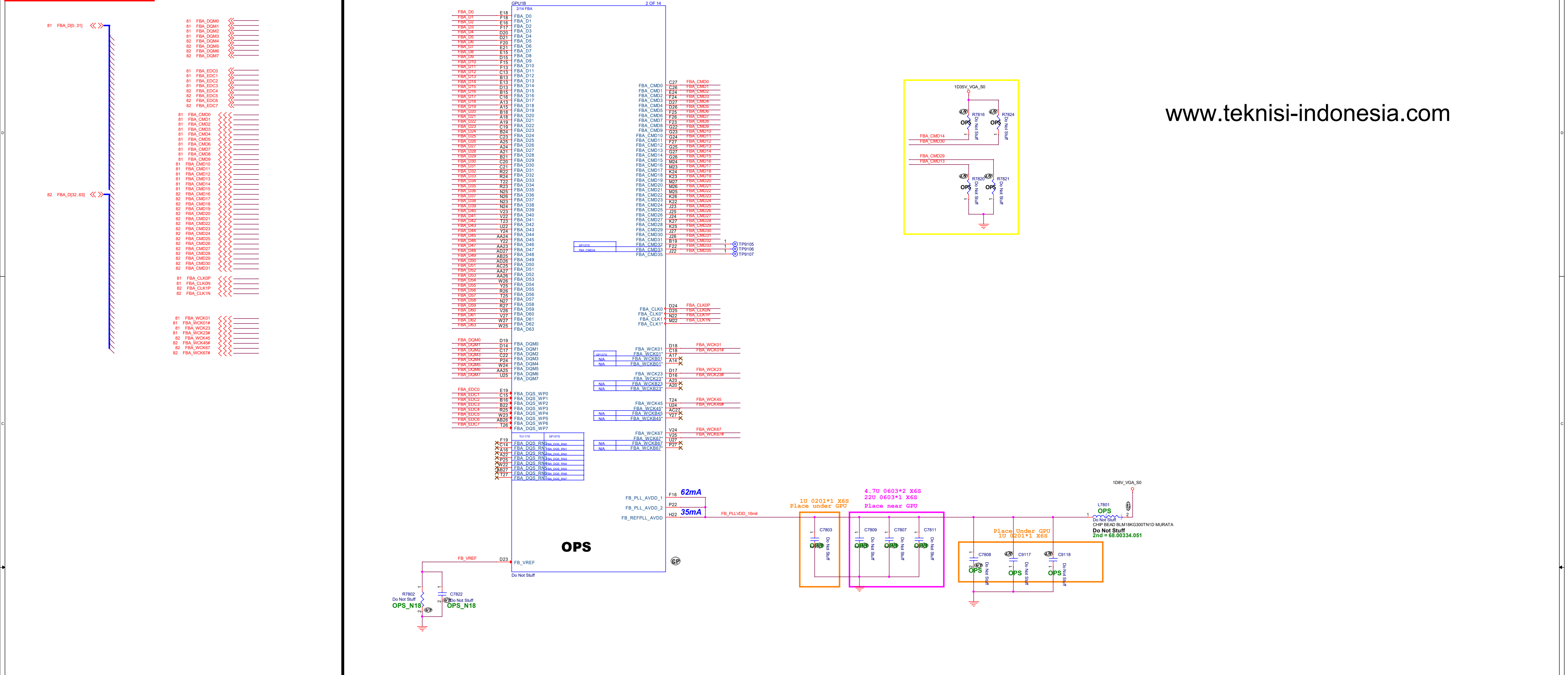
Main Func = dGPU



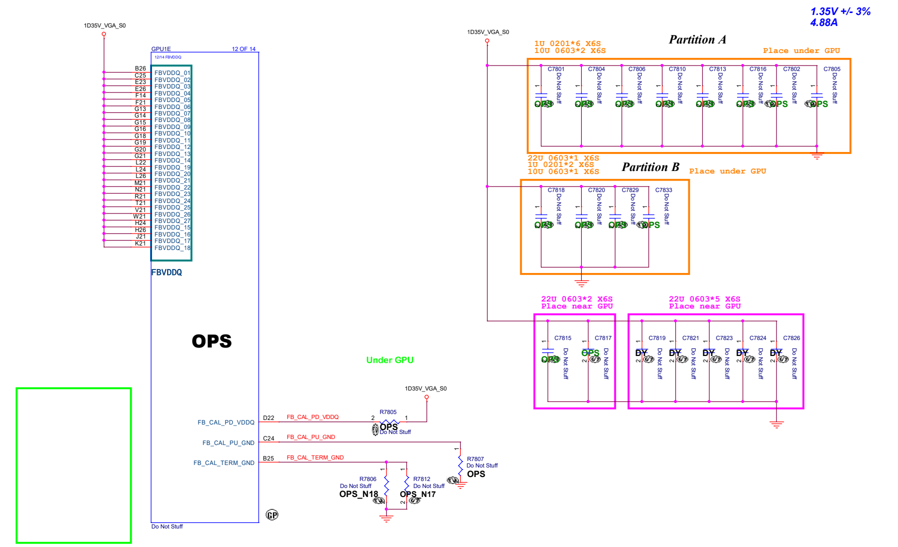


Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

CSG X01 N Compare

Wistron Corporation
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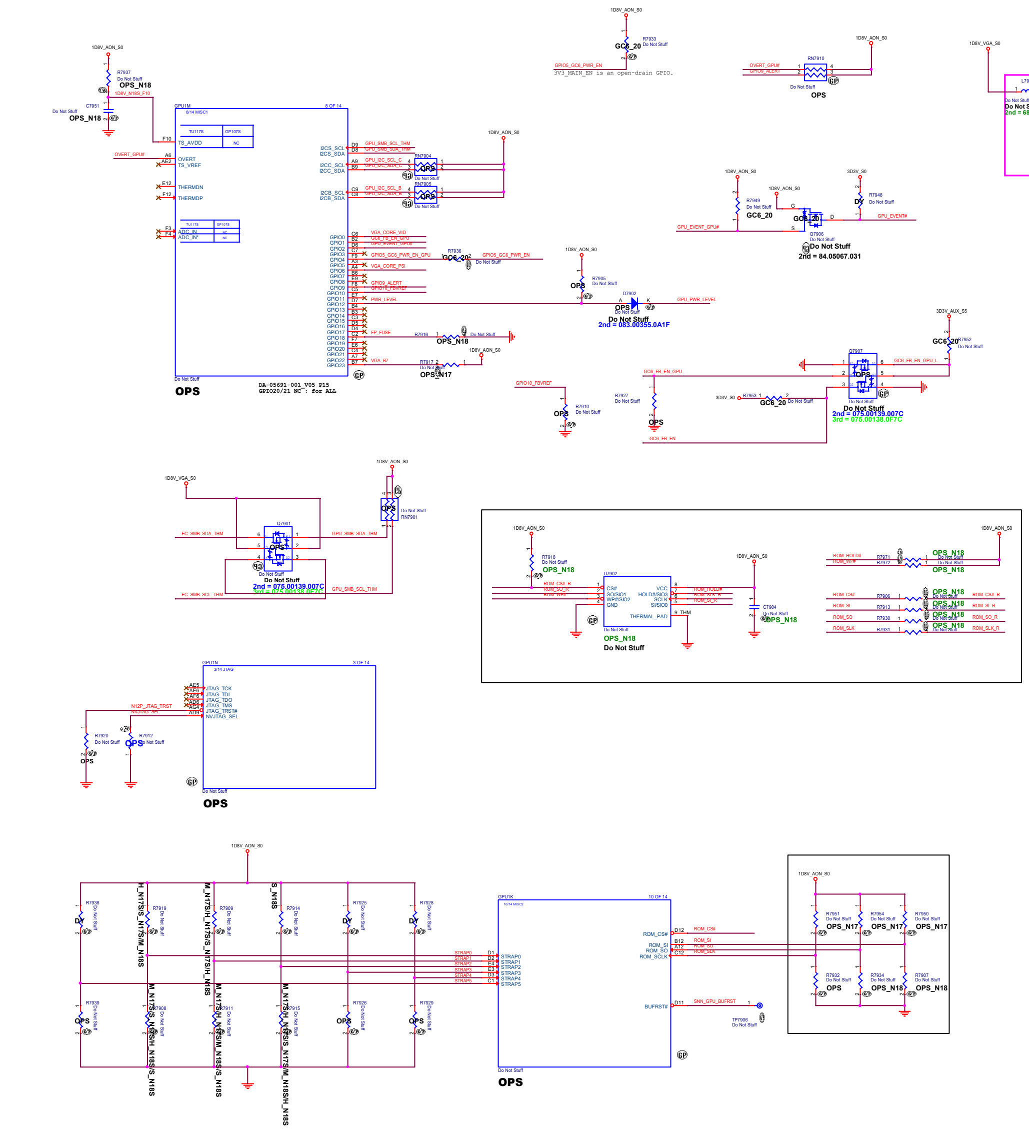
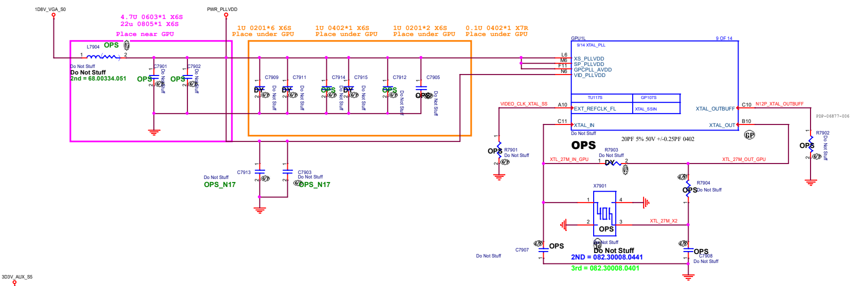
Title: GPU(3/5)VRAM/F
Size: Custom | Document Number: Cyborg TGL | Rev: SB
Date: Thursday, October 15, 2020 | Sheet 78 of 105

Main Func = dGPU





Ta Table 5.2 RAMCFG

S	Strap Pins see Note			RAMCFG Setting Number
	STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
	L	L	L	0 (0x0000)
	L	L	H	1 (0x0001)
	L	H	L	2 (0x0002)
	L	H	H	3 (0x0003)
	H	L	L	4 (0x0004)
	H	L	H	5 (0x0005)
	H	H	L	6 (0x0006)
	H	H	H	7 (0x0007)
	L	L	M	8 (0x0008)
	L	M	L	9 (0x0009)
	L	M	H	10 (0x000A)
	L	H	M	11 (0x000B)
	M	L	L	12 (0x000C)
	M	L	H	13 (0x000D)

Table 13. N18S-G5 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0x4	8 Gbps	N/A	Full	Production candidate

Notes:

1. For N18S-G5, the maximum allowable memory case temperature is 85 °C.

Table 4. N17S-G5/LP GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0xB	8 Gbps	N/A	Full	Production candidate

Notes:

1. For N17S-G5/LP, the maximum allowable memory case temperature is 85 °C.

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Strap Pin	N18/GB2E-64
ROM_SI	Pull low to enable FS_OVERT*
ROM_SO[1]	
ROM_CLK	
STRAP5	• SMB_ALT_ADDR
STRAP4	• DEVID_SEL
STRAP3	• PCIE_CFG • VGA_DEVICE
STRAP2	RAMCFG[4:0]
STRAP1	
STRAP0	

Note:

1 The ROM_SO pin should be pulled low using a 10 kΩ resistor for N18/GB2E-64 GPUs and using a 100 kΩ resistor for N17/GB2D-64/GB2C-64 GPUs.

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

CBG X01 N Compare

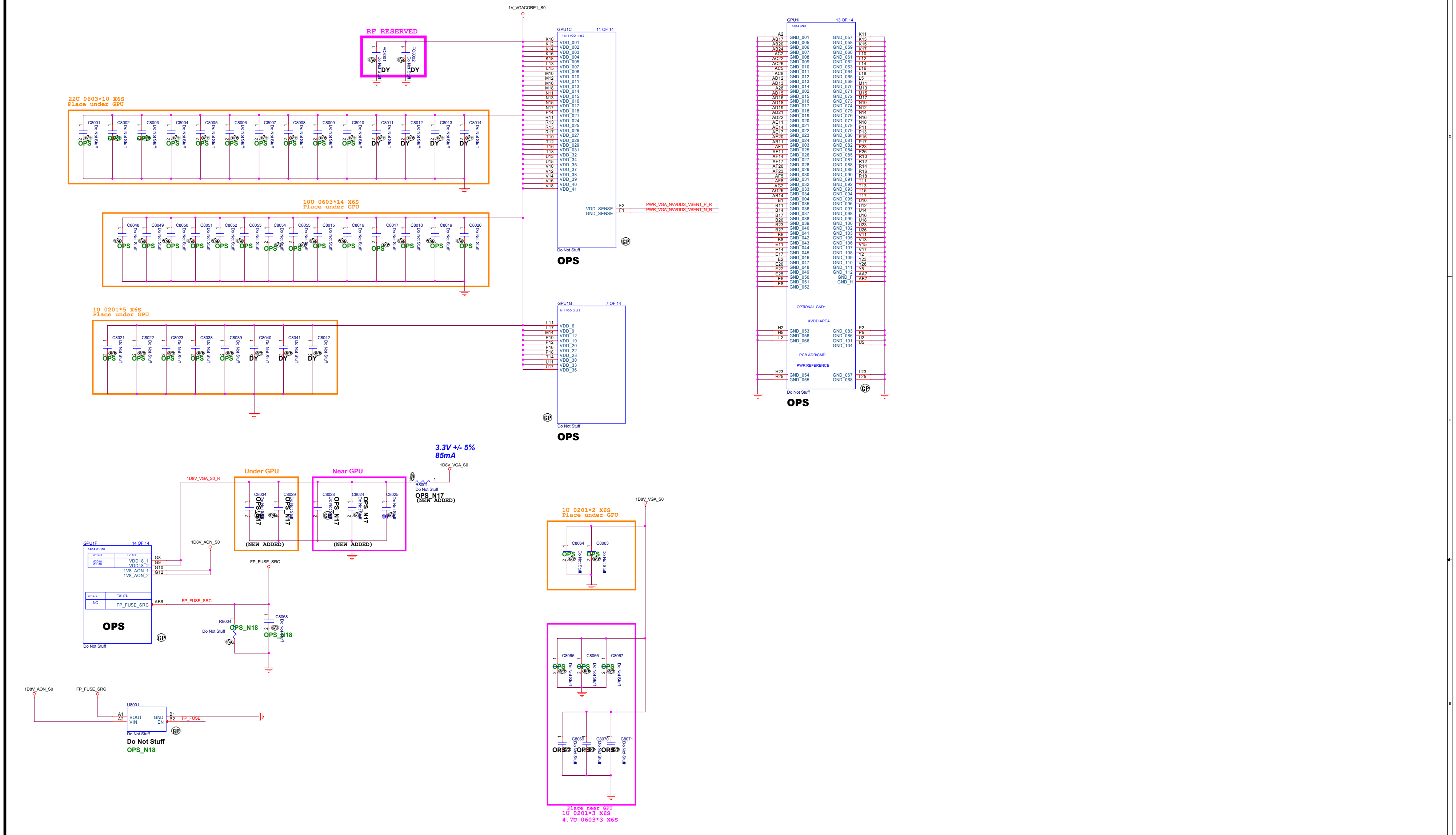
DELL Wistron Corporation

GPU(4/5)GPIO/STRAP

Cyborg TGL

SB

Main Func = dGPU



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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(5/5)PWR/GND

Size: A1 | Document Number: Cyborg TGL | Rev: SB

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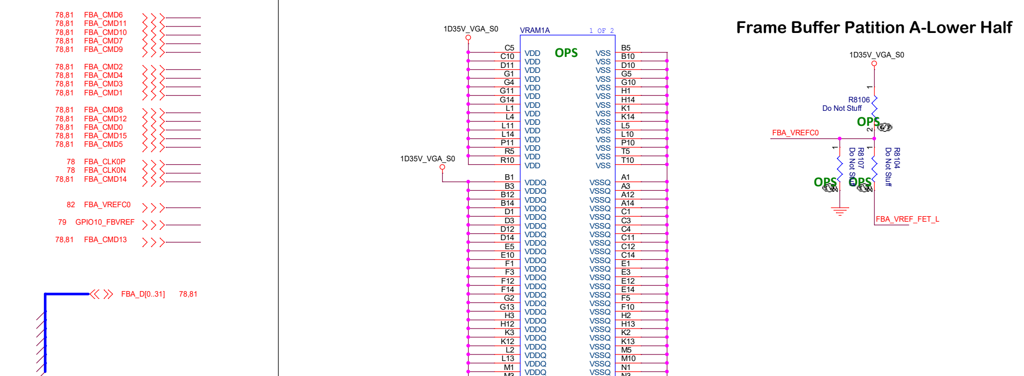
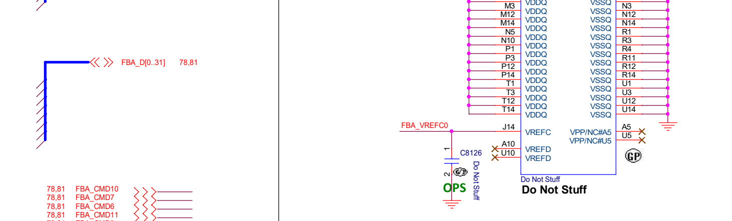
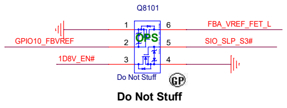
SSID = VRAM

Frame Buffer Patition A-Lower Half

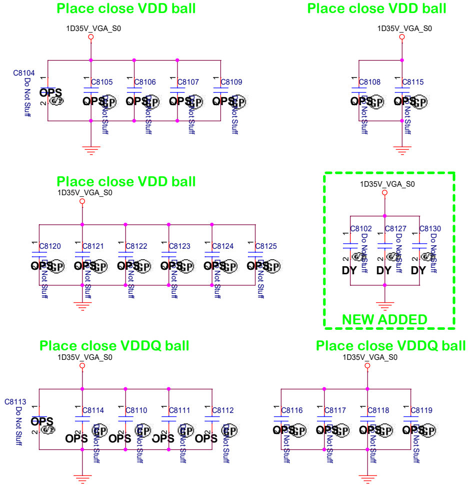




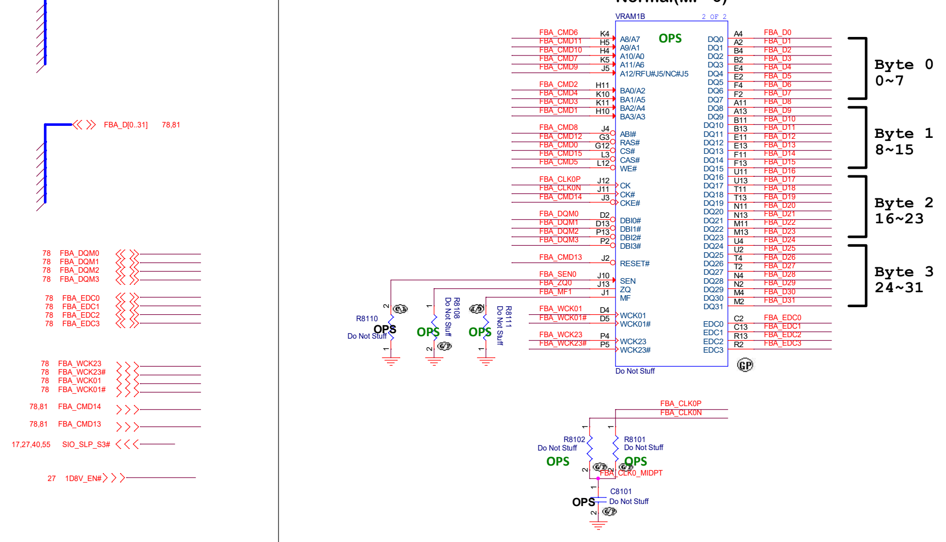


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



Normal(MF=0)



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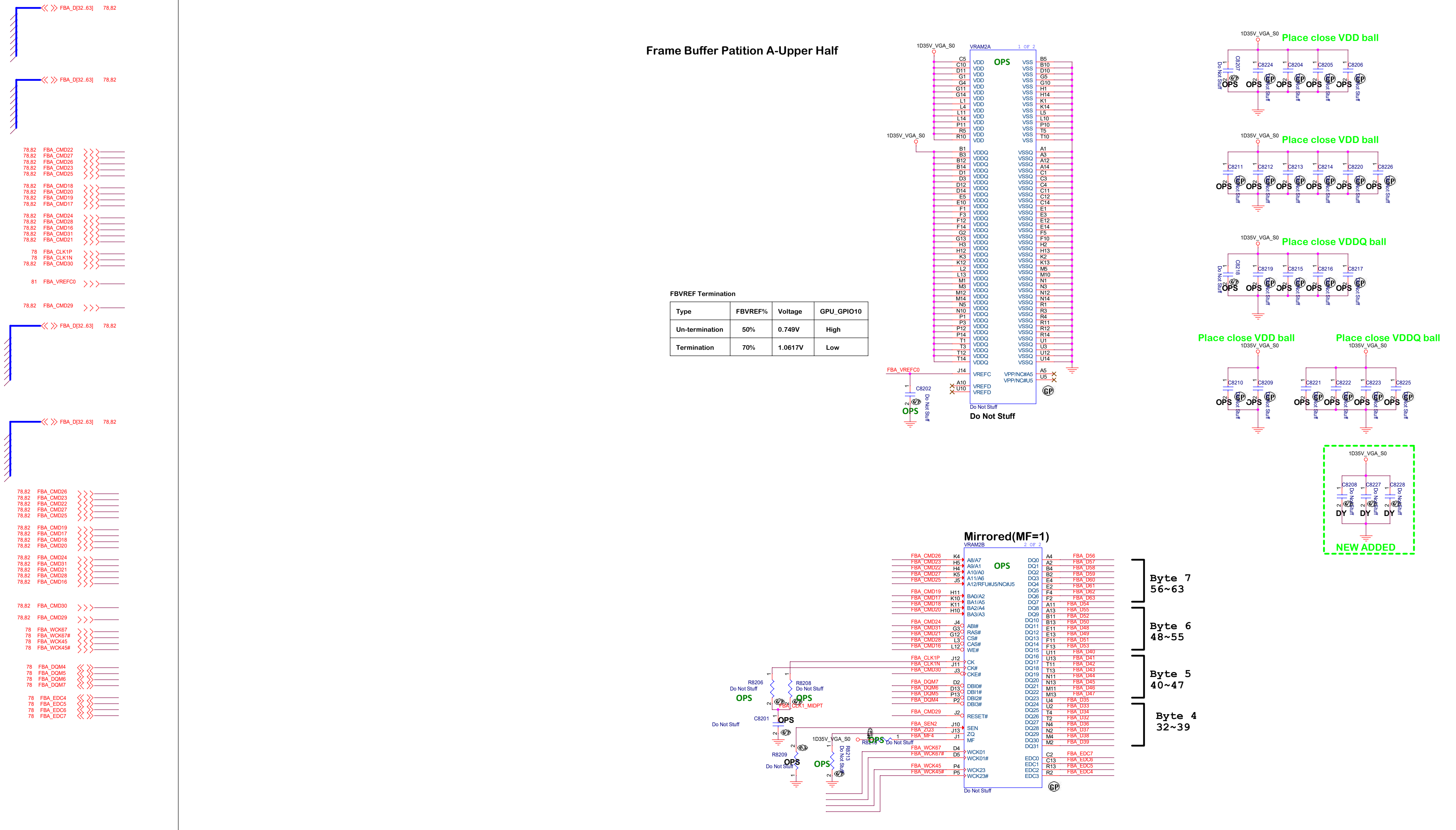
SSID = VRAM

Frame Buffer Patition A-Upper Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

CBG X01 N Compare

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Title	GPU-VRAM3,4 (2/4)		
Size: Custom	Document Number: Cyborg TGL		Rev: SB
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Title	GPU-VRAM5,6 (3/4)	
Size A3	Document Number Cyborg TGL	Rev SB
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Title	GPU-VRAM7,8 (4/4)	
Size A4	Document Number Cyborg TGL	Rev SB
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RT8816B For NVVDDS

VGA : N17S-G3/G5
EDP-Peak : 69.9A

VGA : N17S-G5/N18S-G5
EDP:32.6A
EDP-Peak : 78A
93.6A<OCP<109.2A

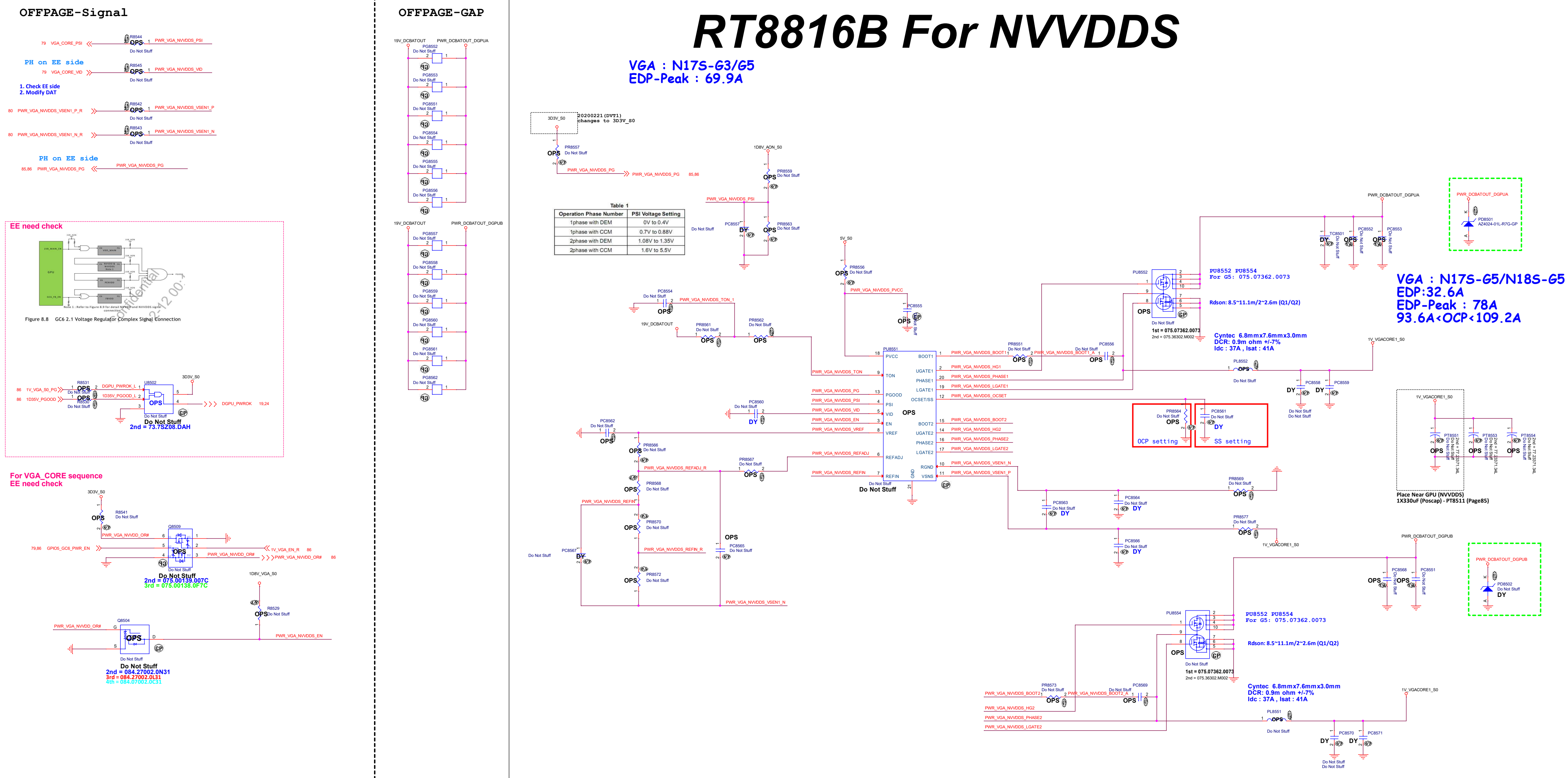
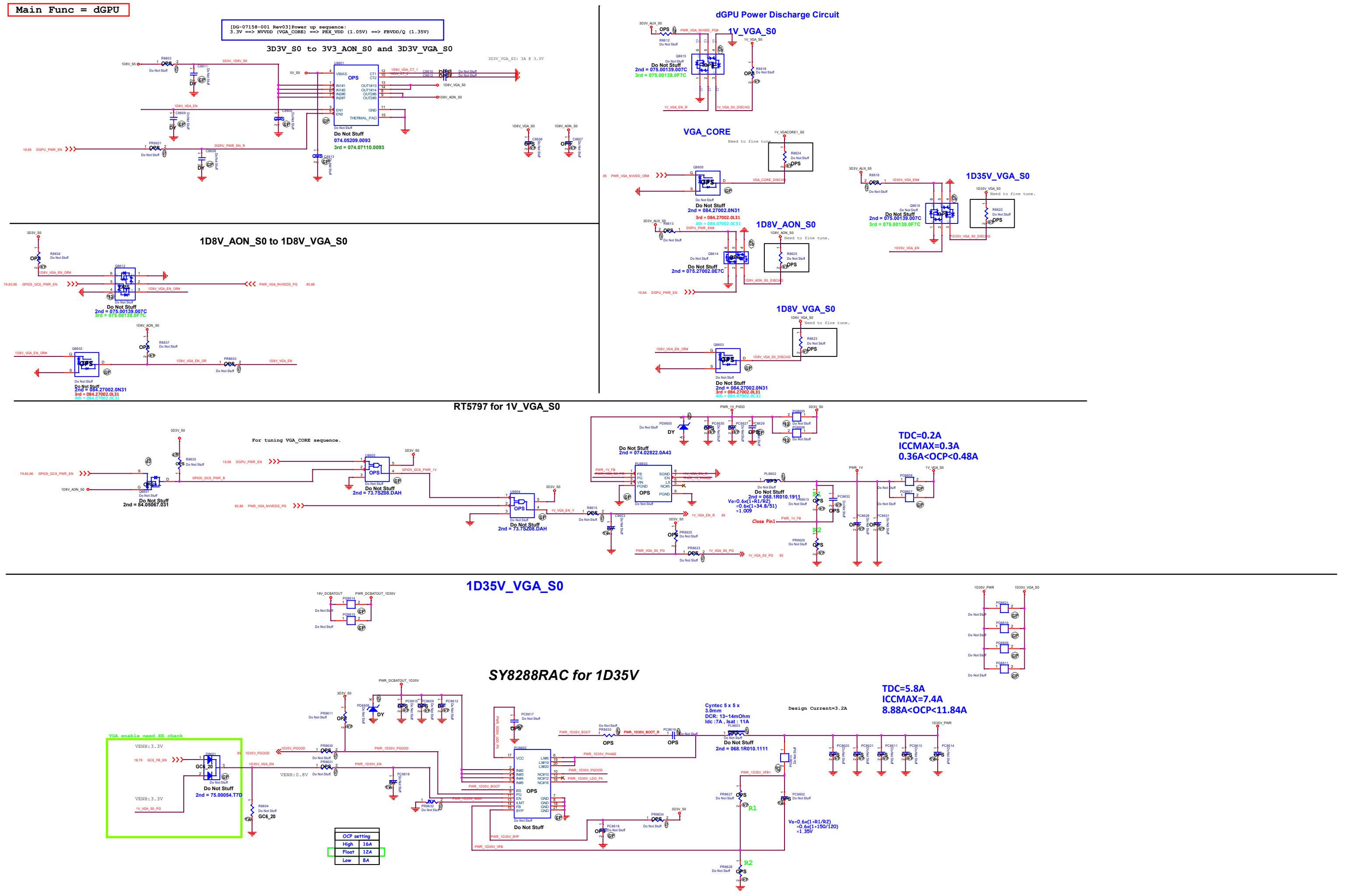


Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

Main Func = dGPU



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Title	DISCRETE VGA POWER
Size	A0
Document Number	Cyborg TGL
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Main Func = dGPU

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Title: Reserved		
Size: A3	Document Number: Cyborg TGL	Rev: SB
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Title: Reserved			
Size: A4	Document Number: Cyborg TGL		Rev: SB
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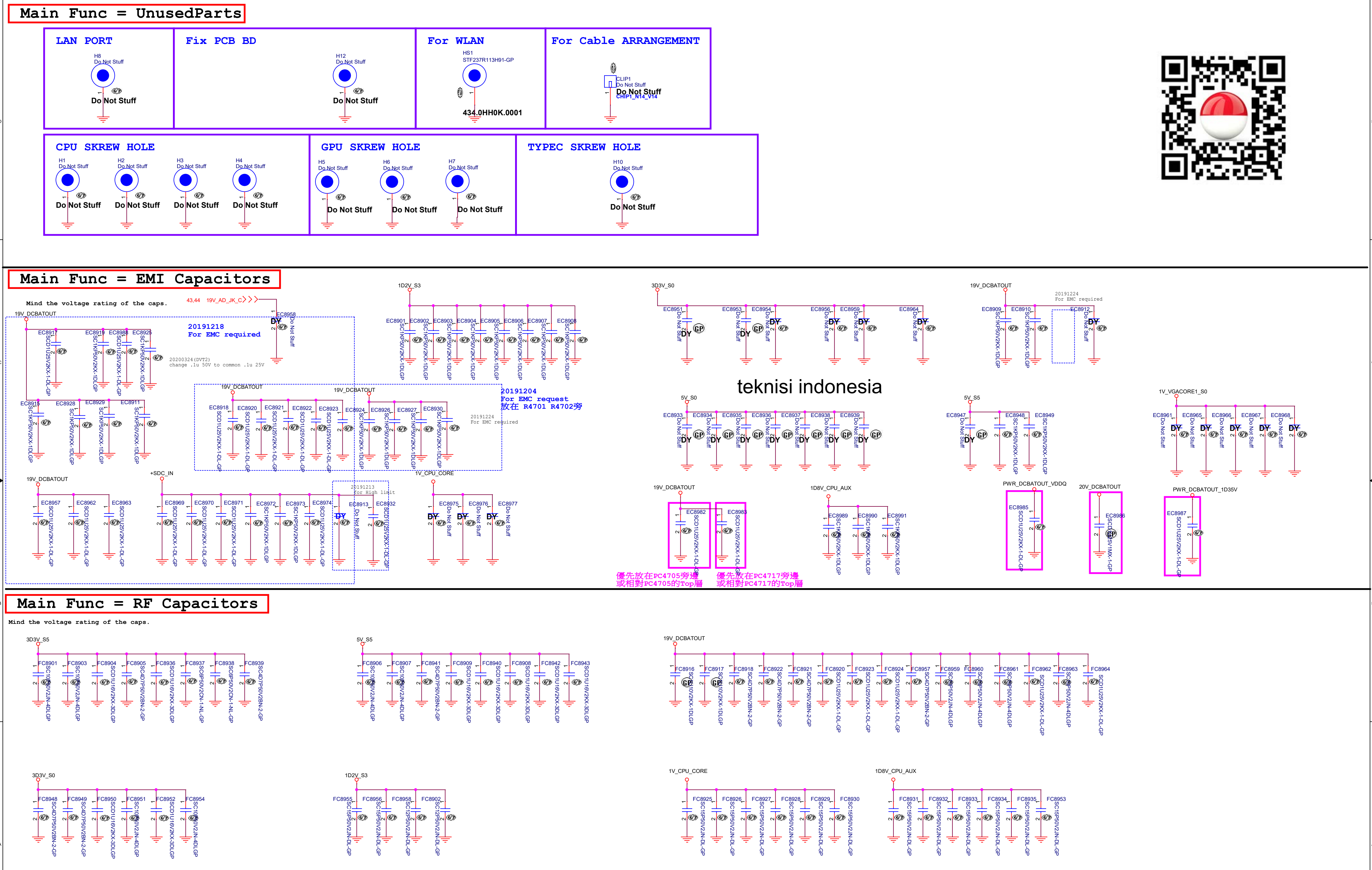

CBG X01 N Compare

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Taipei Hsien 221, Taiwan, R.O.C.

Title	UNUSED PARTS/EMI Capacitors	
Size A2	Document Number: Cyborg TGL	Rev SB
Date: Thursday, October 15, 2020	Sheet 89 of 105	

5 4 3 2 1

D

C

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B

A

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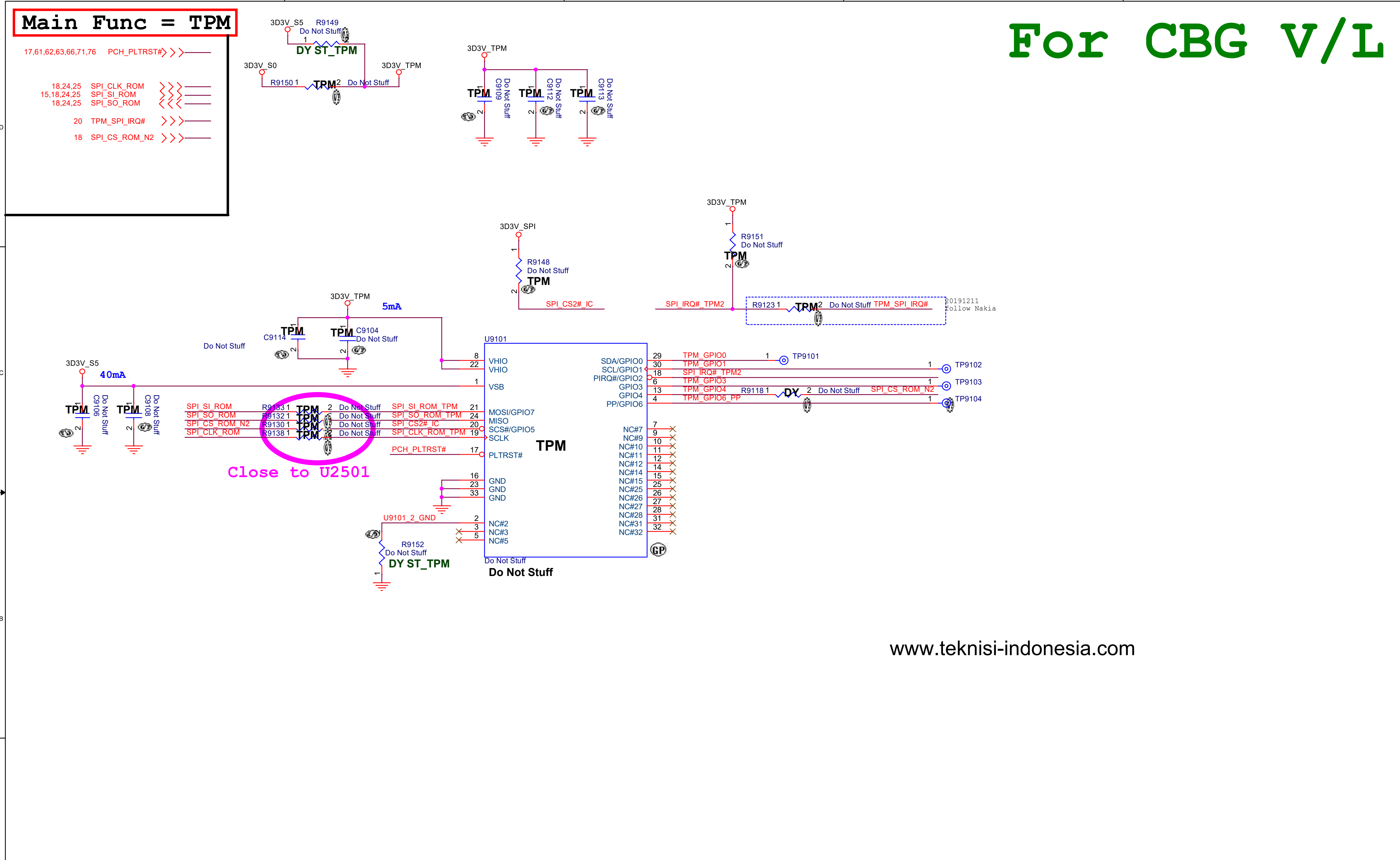
Title			
Reserved			
Size A4	Document Number ***Cyborg TGL***		Rev ***SB***
Date: Thursday, October 15, 2020		Sheet 90 of 105	

5 4 3 2 1



CBG X01 N Compare

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Title	INT IO (TPM)	
Size A3	Document Number: Cyborg TGL	Rev SB
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SSID = Finger Print

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Title	Finger Print	
Size: A4	Document Number: Cyborg TGL	Rev: SB
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Title: (Reserved)		
Size: A3	Document Number: Cyborg TGL	Rev: SB
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Title	(Reserved)	
Size: A3	Document Number: Cyborg TGL	Rev: SB
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Remove

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Title	SITP	
Size A3	Document Number Cyborg TGL	Rev SB
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Title: *LVDS_Switch*			
Size: A4	Document Number: Cyborg TGL		Rev: SB
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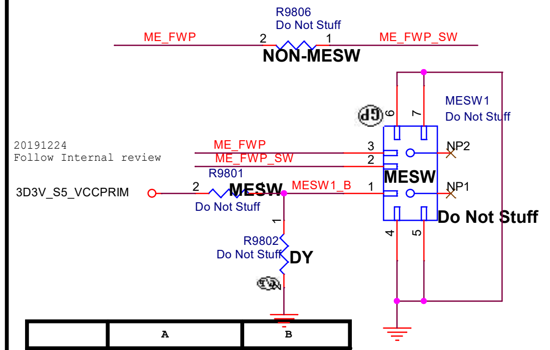
Main Func = Firmware SW

19 ME_FWP_SW

24 ME_FWP

Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

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Title: CRT_Switch

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CLK Block Diagram

TBD

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Title		
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Size: A3	Document Number: Cyborg TGL	Rev: SB
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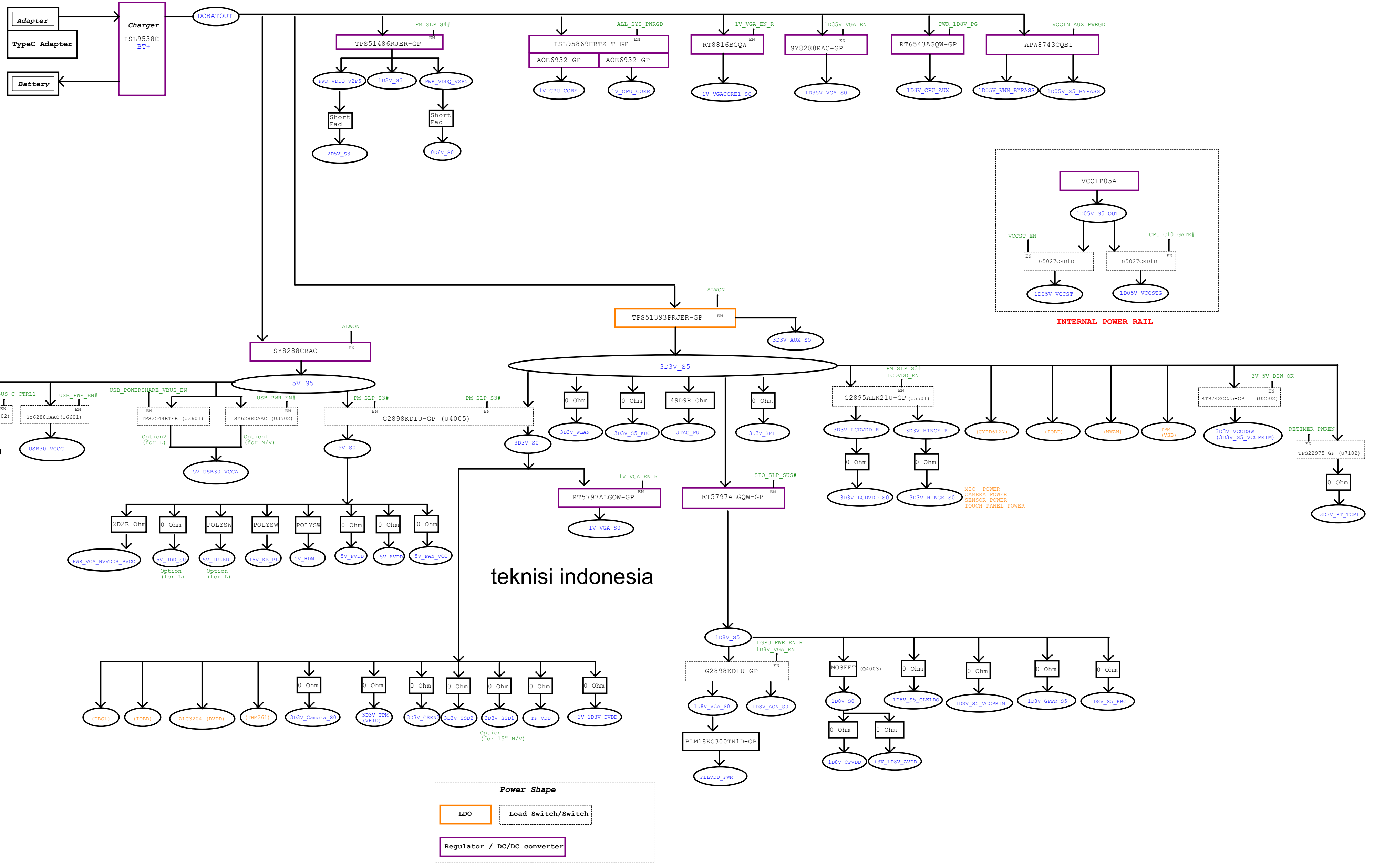
TBD



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Title: Power Block Diagram

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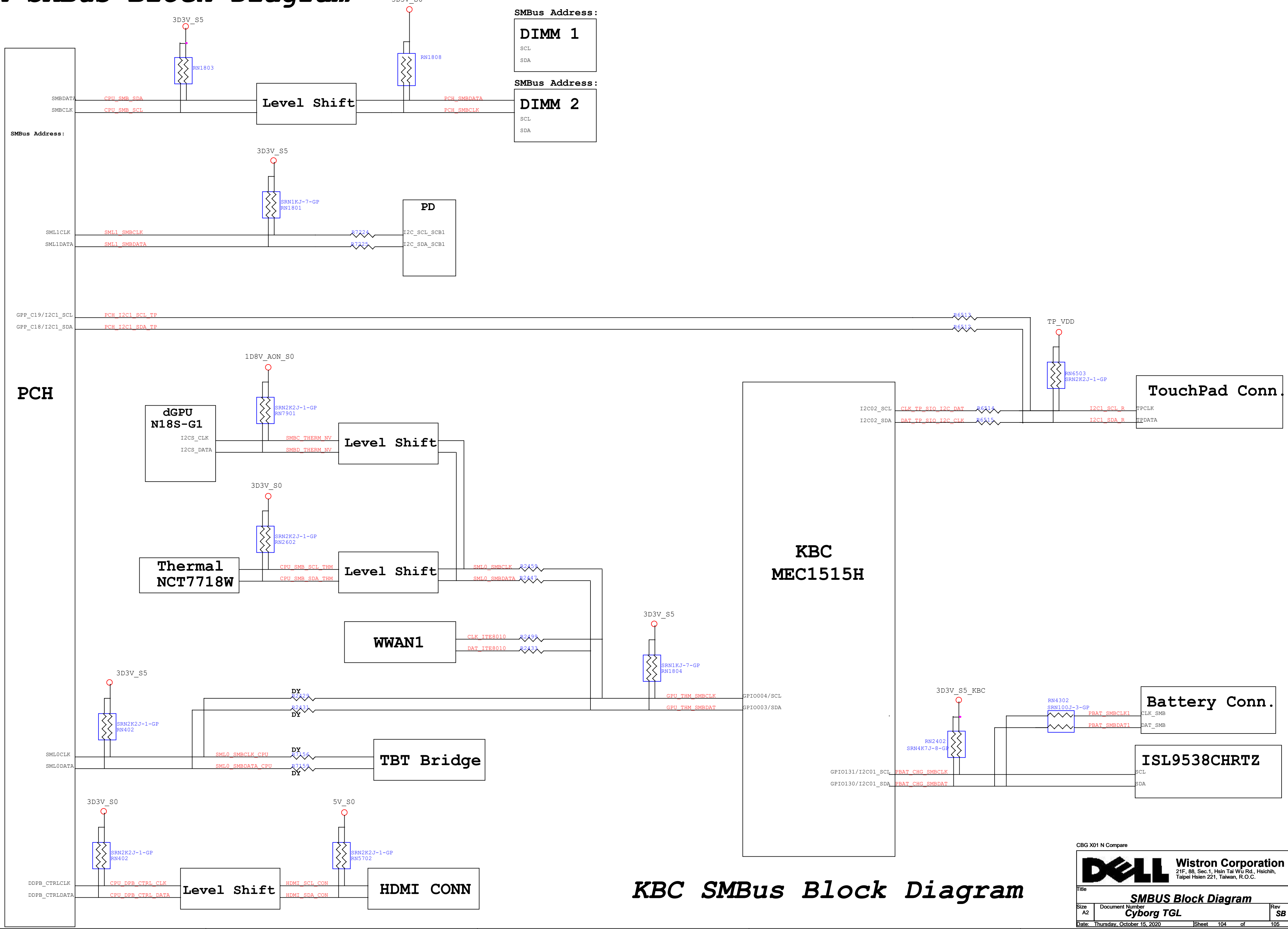
PCH SMBus Block Diagram



KBC SMBus Block Diagram

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Title		
SMBUS Block Diagram		
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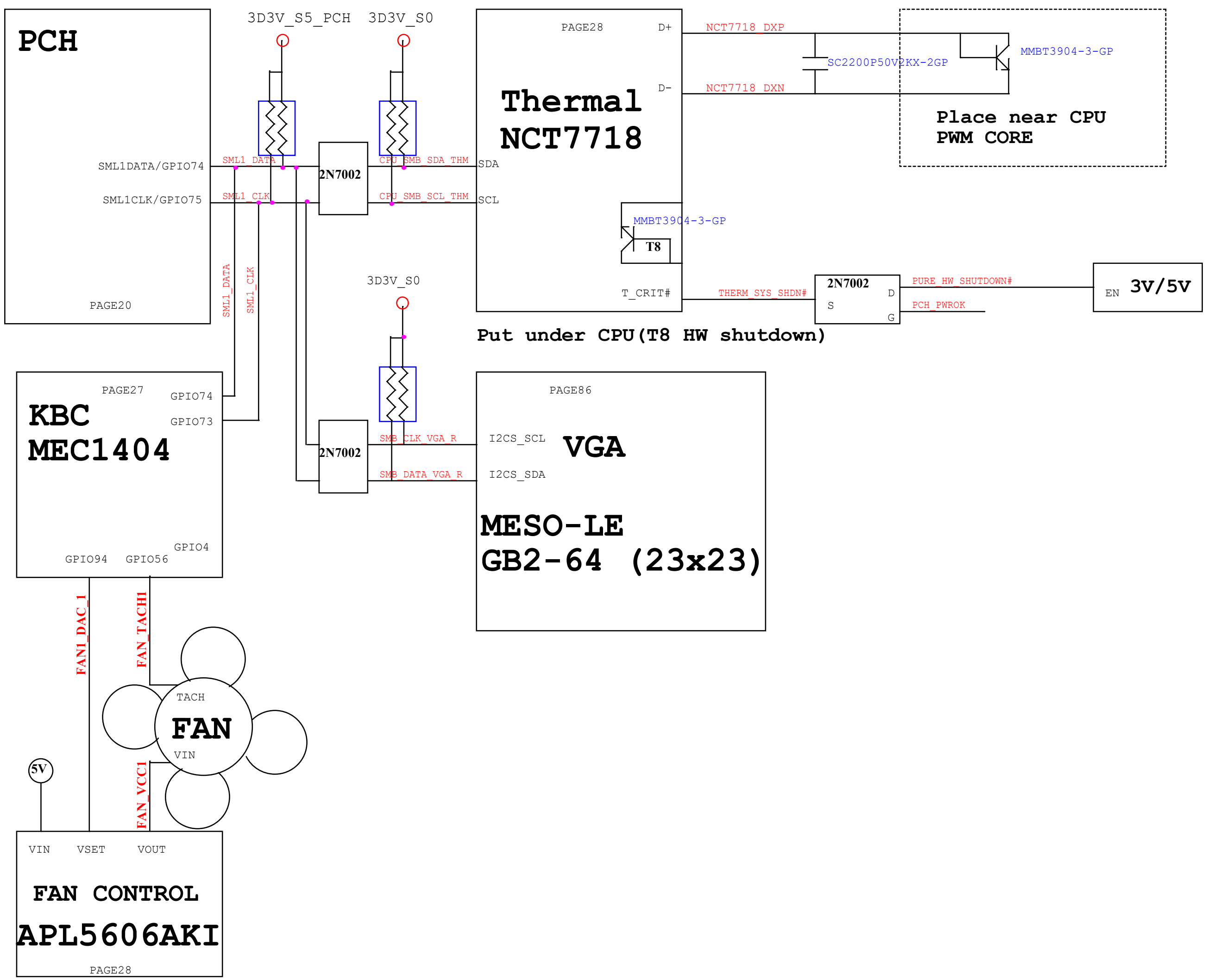
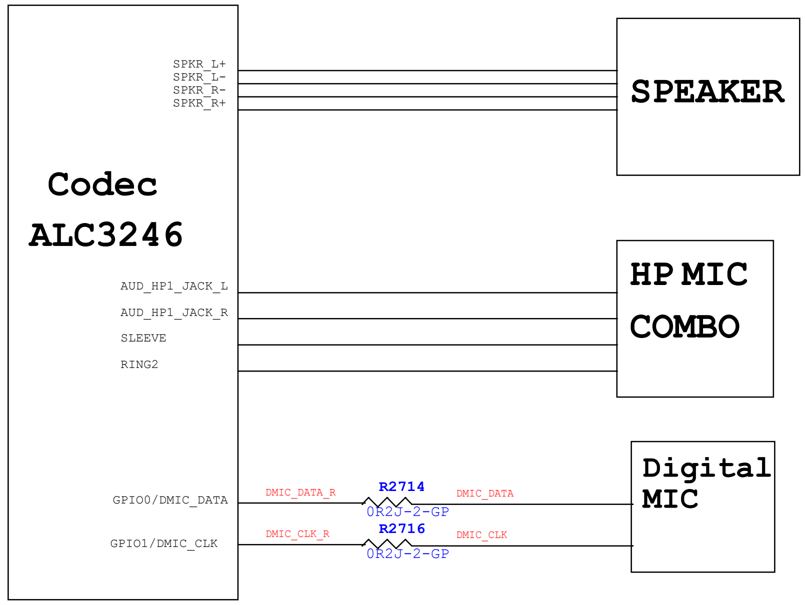
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
Size: Custom	Document Number: Cyborg TGL	Rev: SB
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