MS-7973

ATX:243*180

Ver: 10

Intel -SkyLake-S plamform

CPU:

LGA1151
*CPU POWER PAK *3 Phase*
*GT POWER PAK *2 Phase*

Onboard Chip:

HD Audio Codec: ALC892
SIO: NCT6793D
Flash ROM: SPI 64 MB
DP to VGA: ITE6515

Main Memory:

*DDR3L * 2 (Dual Channel)*

ACPI:

5VDAUL:uP7501
5VDIMM:uP7501
3VSB:GS7166+PN MOS
3VDSW:GS7166

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 3*

System Chipset:

PCH-H :H110

PWM:

VCORE - RT3606BC
DDR - RT8231AGQW
PCH(1.0V) - RT8125C
VCCSA - RT8125C
VCCIO - NB681(Converter)

LDO:

VCCSTPLL - GS7166

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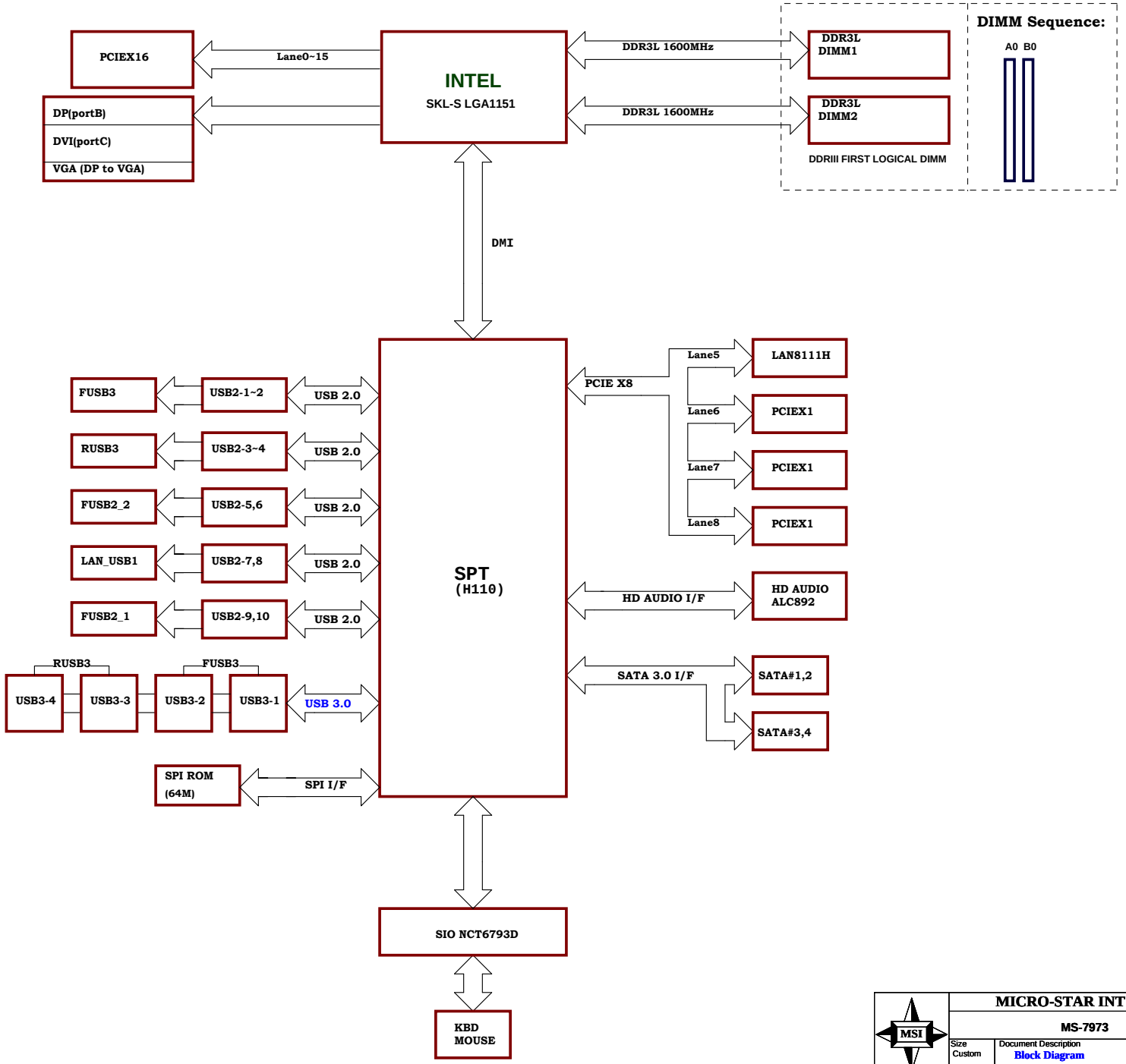
MS-7981 Block Diagram



Slot Sequence:

PCIE X16	(By CPU)
PCIE X1	(By PCH)
PCIE X1	(By PCH)
PCIE X1	(By PCH)

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Size: Custom | Document Description: Block Diagram | Rev: 11

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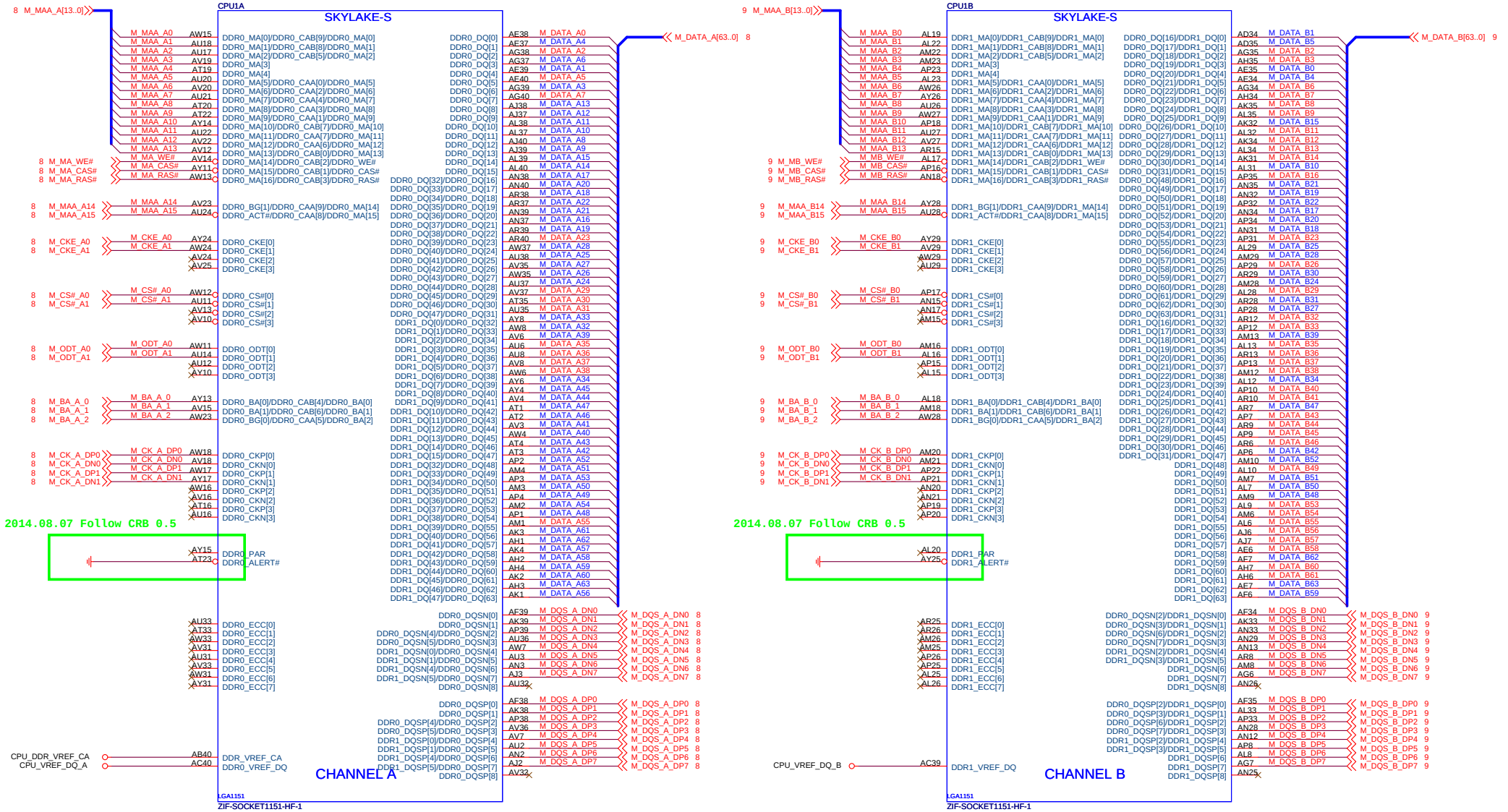

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Size	Document Description	Rev
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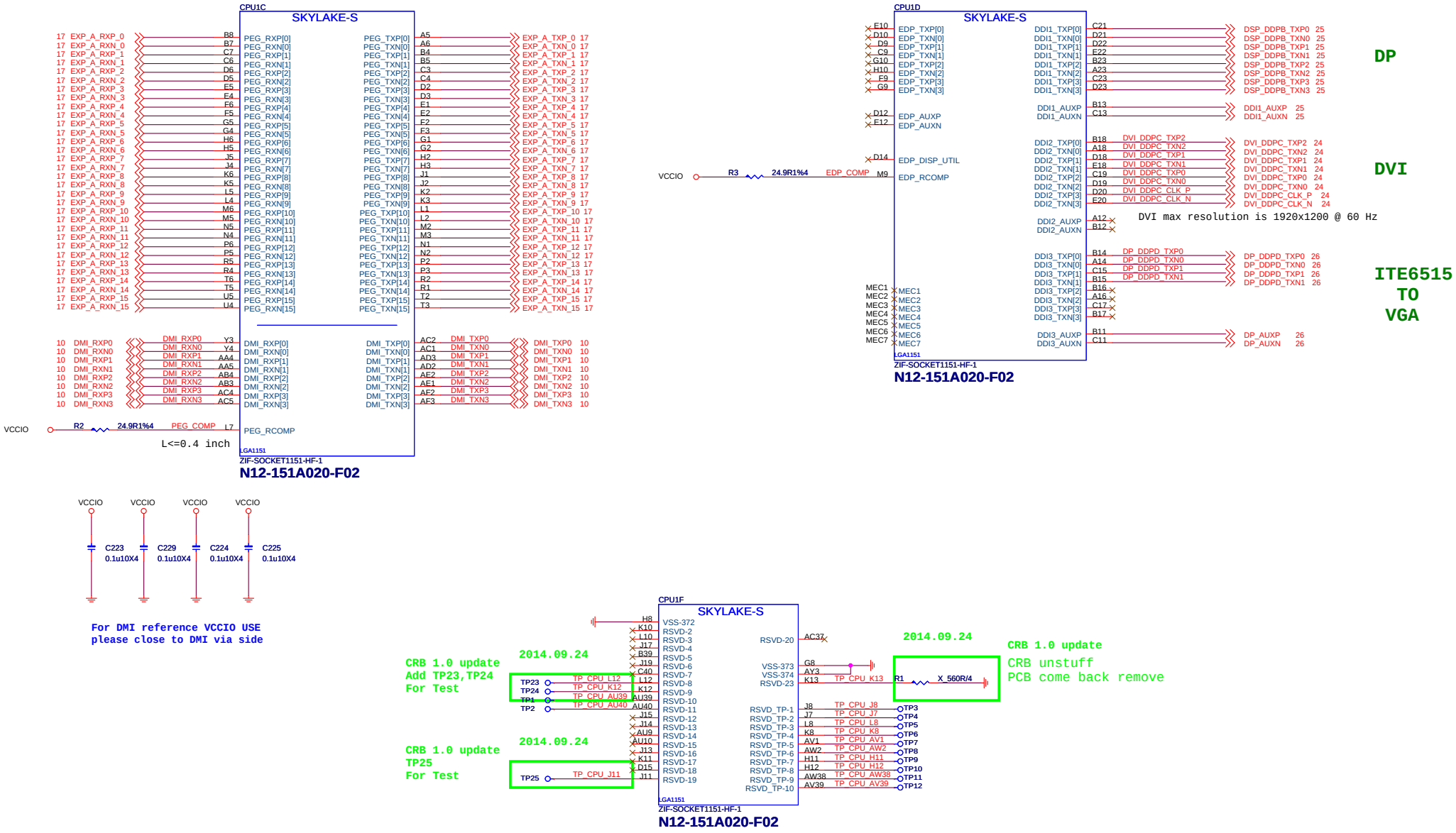

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Size	Document Description	Rev
Custom	CPU-PEG/Display	11

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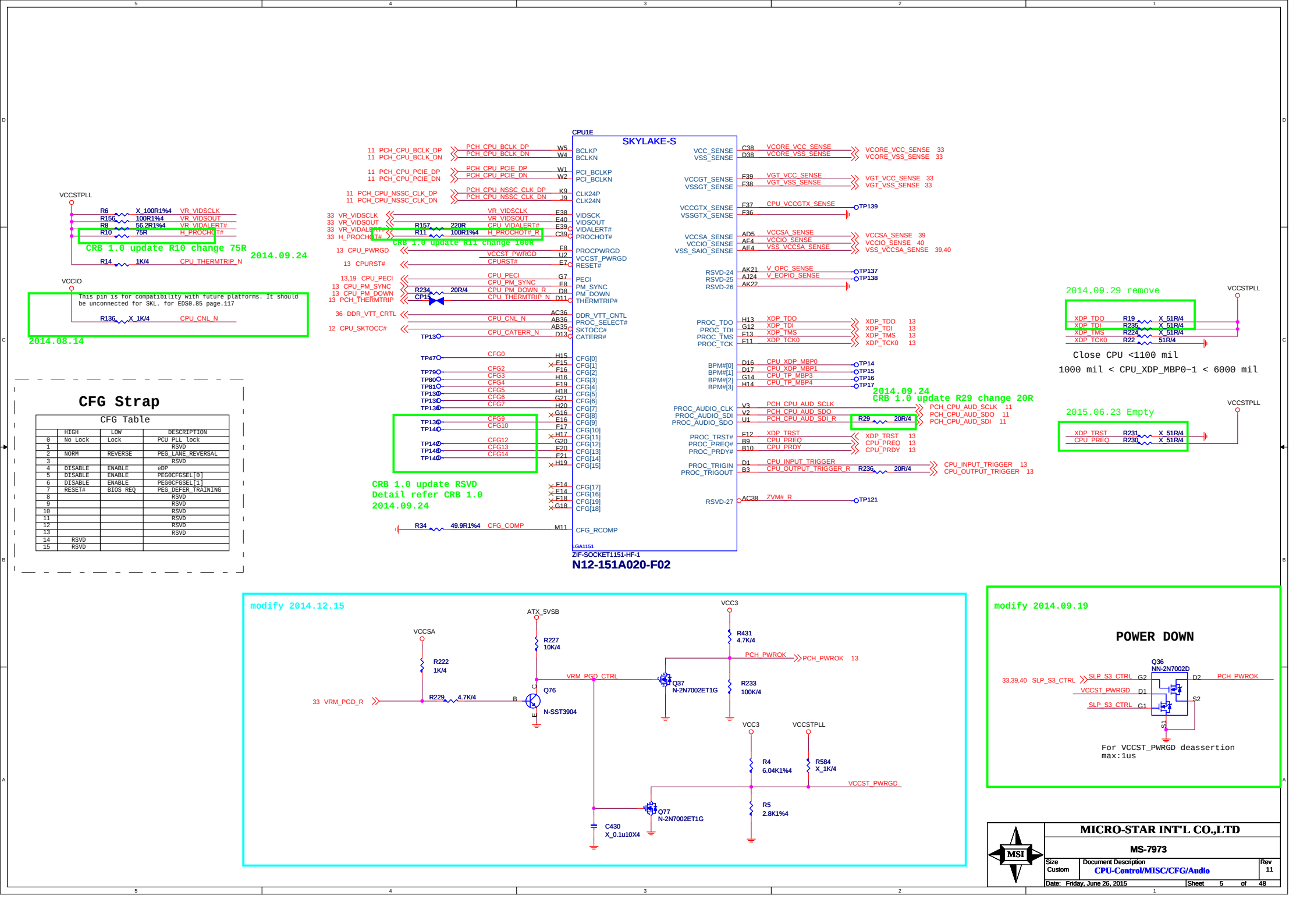
VCCSTPLL
R6 X_100R1%4 VR_VIDSCLK
R156 100R1%4 VR_VIDSOUT
R8 56.2R1%4 VR_VIDALERT#
R10 75R H_PROCHOT#
CRB 1.0 update R10 change 75R
2014.09.24
R14 1K/4 CPU_THERMTRIP_N
VCCIO
This pin is for compatibility with future platforms. It should be unconnected for SKL. for EDS0.85 page.117
R136 X_1K/4 CPU_CNL_N
2014.08.14
CPU1E
SKYLAKE-S
11 PCH_CPU_BCLK_DP
11 PCH_CPU_BCLK_DN
PCH_CPU_BCLK_DP W5 BCLKP
PCH_CPU_BCLK_DN W4 BCLKN
11 PCH_CPU_PCIE_DP
11 PCH_CPU_PCIE_DN
PCH_CPU_PCIE_DP W1 PCI_BCLKP
PCH_CPU_PCIE_DN W2 PCI_BCLKN
11 PCH_CPU_NSSC_CLK_DP
11 PCH_CPU_NSSC_CLK_DN
PCH_CPU_NSSC_CLK_DP K9 CLK24P
PCH_CPU_NSSC_CLK_DN J9 CLK24N
33 VR_VIDSCLK
33 VR_VIDSOUT
33 VR_VIDALERT#
33 H_PROCHOT#
R157 220R
R11 100R1%4
VR_VIDSCLK E38 VIDSCK
VR_VIDSOUT E40 VIDSOUT
CPU_VIDALERT# E39 VIDALERT#
H_PROCHOT#_R C39 PROCHOT#
CRB 1.0 update R11 change 100R
13 CPU_PWRGD
VCCST_PWRGD U2 PROCPWRGD
VCCST_PWRGD
13 CPURST#
CPURST# E7 RESET#
13,19 CPU_PECI
13 CPU_PM_SYNC
13 CPU_PM_DOWN
13 PCH_THERMTRIP
R234 20R/4
CP15
CPU_PECI G7 PECI
CPU_PM_SYNC F8 PM_SYNC
CPU_PM_DOWN_R D8 PM_DOWN
CPU_THERMTRIP_N D11 THERMTRIP#
36 DDR_VTT_CRTL
12 CPU_SKTOCC#
TP13
DDR_VTT_CRTL AC36
CPU_CNL_N AB36 PROC_SELECT#
AB35 SKTOCC#
CPU_CATERR_N D13 CATERR#
TP47
TP79
TP80
TP81
TP130
TP131
TP134
TP136
TP140
TP142
TP143
TP140
CFG0 H15 CFG[0]
E15 CFG[1]
CFG2 F16 CFG[2]
CFG3 H16 CFG[3]
CFG4 F19 CFG[4]
CFG5 H18 CFG[5]
CFG6 G21 CFG[6]
CFG7 H20 CFG[7]
G16 CFG[8]
CFG9 E16 CFG[9]
CFG10 F17 CFG[10]
H17 CFG[11]
CFG12 G20 CFG[12]
CFG13 F20 CFG[13]
CFG14 F21 CFG[14]
H19 CFG[15]
CRB 1.0 update RSVD
Detail refer CRB 1.0
2014.09.24
F14 CFG[17]
E14 CFG[16]
F18 CFG[19]
G18 CFG[18]
R34 49.9R1%4 CFG_COMP
M11 CFG_RCOMP
LGA1151
ZIF-SOCKET1151-HF-1
N12-151A020-F02
VCC_SENSE C38 VCORE_VCC_SENSE
VSS_SENSE D38 VCORE_VSS_SENSE
VCORE_VCC_SENSE 33
VCORE_VSS_SENSE 33
VCCGT_SENSE F39 VGT_VCC_SENSE
VSSGT_SENSE F38 VGT_VSS_SENSE
VGT_VCC_SENSE 33
VGT_VSS_SENSE 33
VCCGTX_SENSE F37 CPU_VCCGTX_SENSE
VSSGTX_SENSE F36
TP139
VCCSA_SENSE AD5 VCCSA_SENSE
VCCIO_SENSE AE4 VCCIO_SENSE
VSS_SAIO_SENSE AE4 VSS_VCCSA_SENSE
VCCSA_SENSE 39
VCCIO_SENSE 40
VSS_VCCSA_SENSE 39,40
RSVD-24 AK21 V_OPC_SENSE
RSVD-25 AJ24 V_EOPIO_SENSE
RSVD-26 AK22
TP137
TP138
PROC_TDO H13 XDP_TDO
PROC_TDI G12 XDP_TDI
PROC_TMS F13 XDP_TMS
PROC_TCK F11 XDP_TCK0
XDP_TDO 13
XDP_TDI 13
XDP_TMS 13
XDP_TCK0 13
BPM#[0] D16 CPU_XDP_MBP0
BPM#[1] D17 CPU_XDP_MBP1
BPM#[2] G14 CPU_TP_MBP3
BPM#[3] H14 CPU_TP_MBP4
TP14
TP15
TP16
TP17
2014.09.24
CRB 1.0 update R29 change 20R
PROC_AUDIO_CLK V3 PCH_CPU_AUD_SCLK
PROC_AUDIO_SDI V2 PCH_CPU_AUD_SDO
PROC_AUDIO_SDO U1 PCH_CPU_AUD_SDI_R
R29 20R/4
PCH_CPU_AUD_SCLK 11
PCH_CPU_AUD_SDO 11
PCH_CPU_AUD_SDI 11
PROC_TRST# F12 XDP_TRST
PROC_PREQ# B9 CPU_PREQ
PROC_PRDY# B10 CPU_PRDY
XDP_TRST 13
CPU_PREQ 13
CPU_PRDY 13
PROC_TRIGIN D1 CPU_INPUT_TRIGGER
PROC_TRIGOUT B3 CPU_OUTPUT_TRIGGER_R
R236 20R/4
CPU_INPUT_TRIGGER 13
CPU_OUTPUT_TRIGGER 13
RSVD-27 AC38 ZVM#_R
TP121
2014.09.29 remove
VCCSTPLL
XDP_TDO R19 X_51R/4
XDP_TDI R235 X_51R/4
XDP_TMS R224 X_51R/4
XDP_TCK0 R22 51R/4
Close CPU <1100 mil
1000 mil < CPU_XDP_MBP0~1 < 6000 mil
2015.06.23 Empty
VCCSTPLL
XDP_TRST R231 X_51R/4
CPU_PREQ R230 X_51R/4
CFG Strap
CFG Table
HIGH LOW DESCRIPTION
0 No Lock Lock PCU_PLL_lock
1 RSVD
2 NORM REVERSE PEG_LANE_REVERSAL
3 RSVD
4 DISABLE ENABLE eDP
5 DISABLE ENABLE PEG0CFGSEL[0]
6 DISABLE ENABLE PEG0CFGSEL[1]
7 RESET# BIOS_REQ PEG_DEFER_TRAINING
8 RSVD
9 RSVD
10 RSVD
11 RSVD
12 RSVD
13 RSVD
14 RSVD
15 RSVD
modify 2014.12.15
ATX_5VSB
VCCSA
VCC3
R227 10K/4
R222 1K/4
R431 4.7K/4
PCH_PWROK
PCH_PWROK 13
VRM_PGD_CTRL
Q37 N-2N7002ET1G
R233 100K/4
33 VRM_PGD_R
R229 4.7K/4
Q76 N-SST3904
VCC3
VCCSTPLL
R4 6.04K1%4
R584 X_1K/4
VCCST_PWRGD
R5 2.8K1%4
Q77 N-2N7002ET1G
C430 X_0.1u10X4
modify 2014.09.19
POWER DOWN
Q36 NN-2N7002D
33,39,40 SLP_S3_CTRL
SLP_S3_CTRL G2
VCCST_PWRGD D1
SLP_S3_CTRL G1
D2 PCH_PWROK
S2
S1
For VCCST_PWRGD deassertion
max:1us
MICRO-STAR INT'L CO.,LTD
MS-7973
Size Custom
Document Description
CPU-Control/MISC/CFG/Audio
Rev 11
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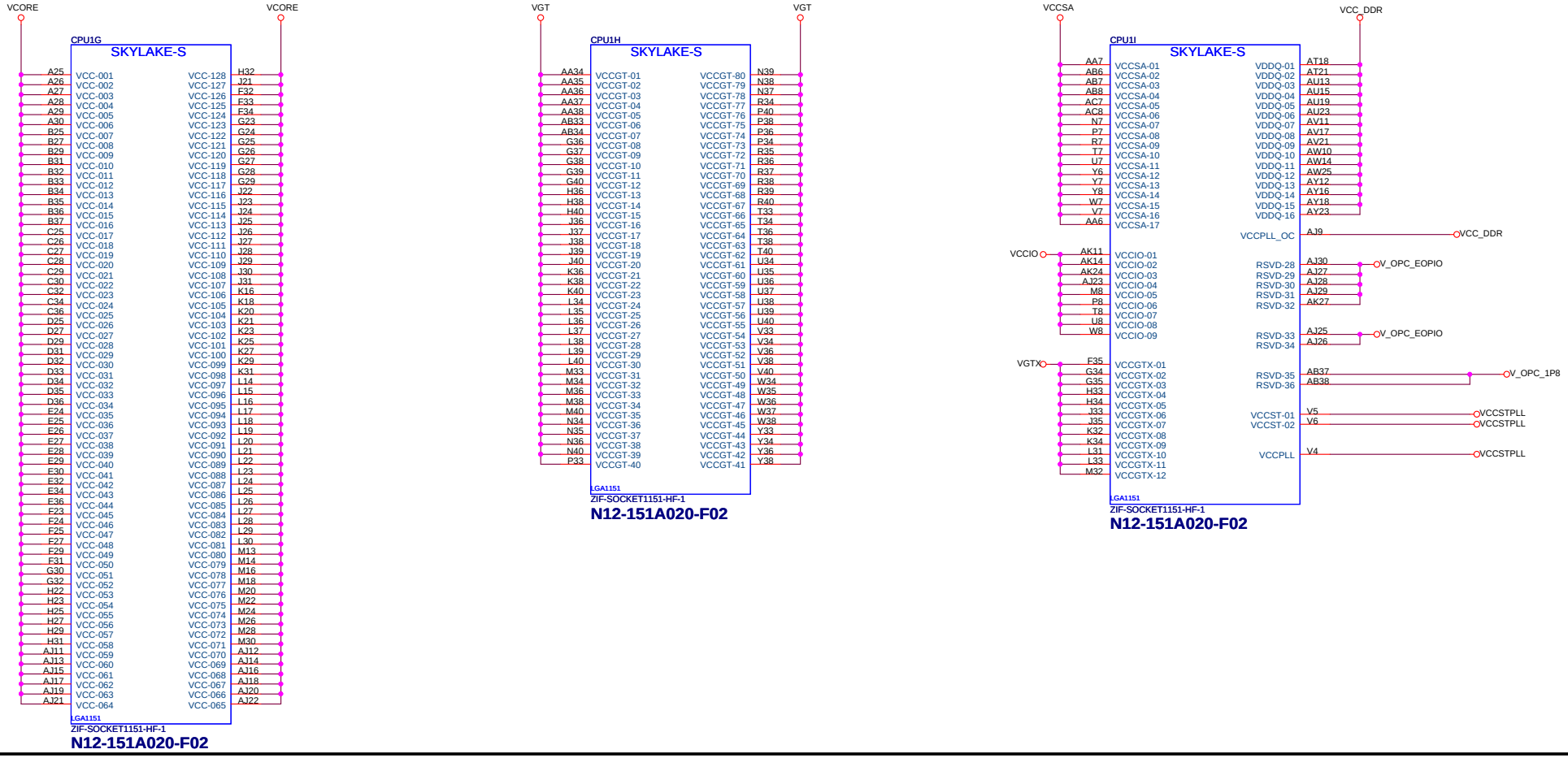
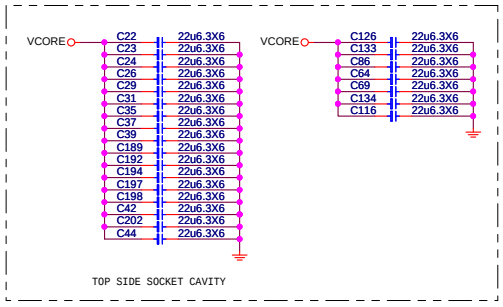
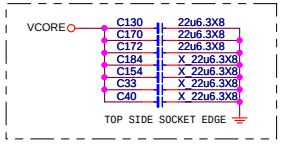
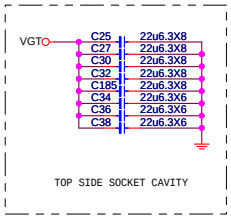


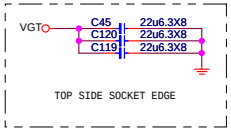
CAP

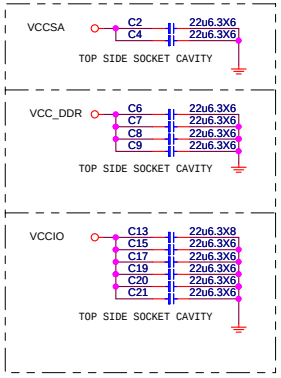


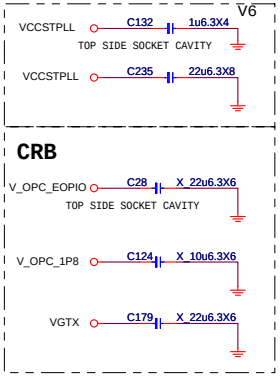


TBD









MICRO-STAR INT'L CO.,LTD

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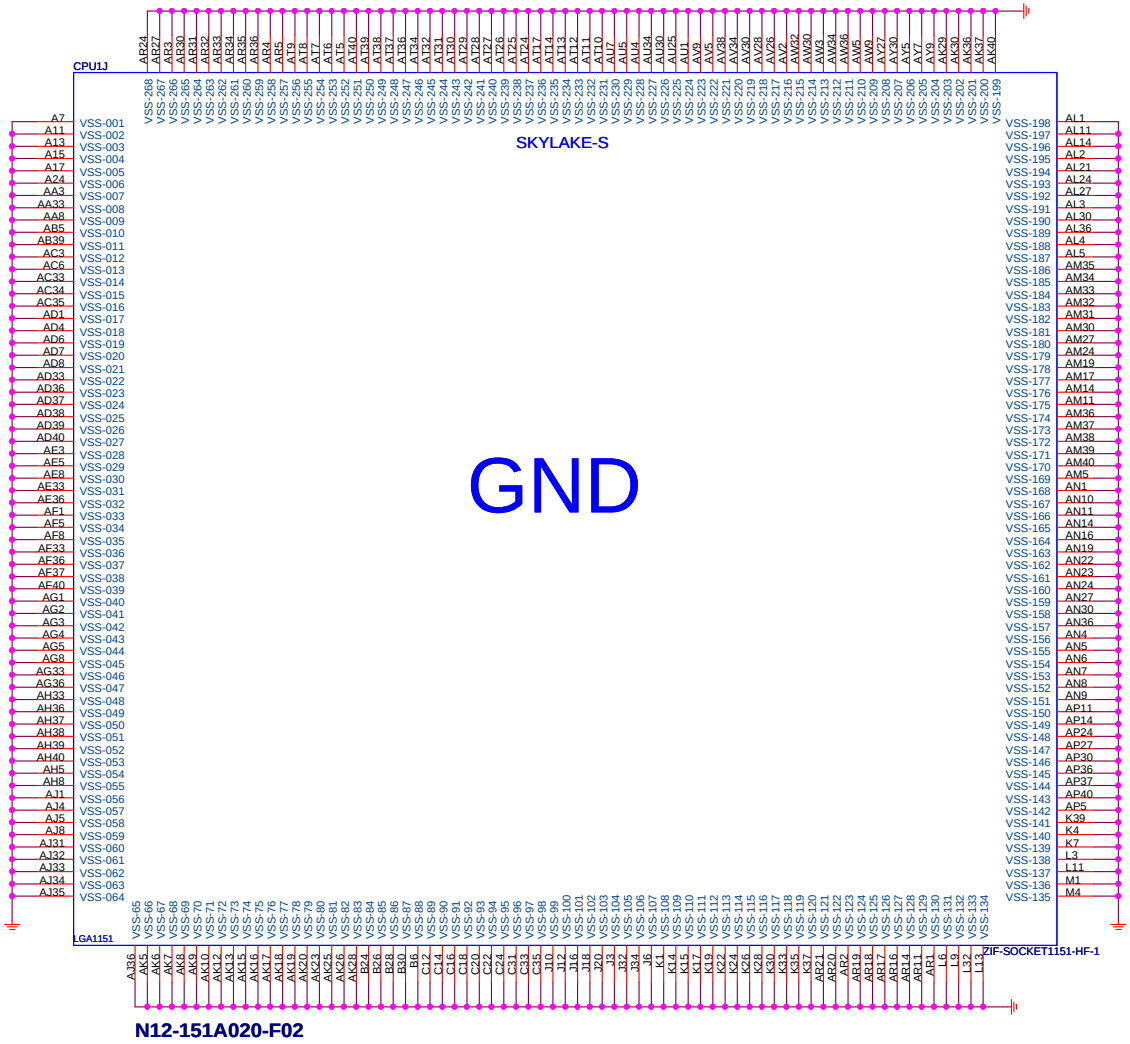
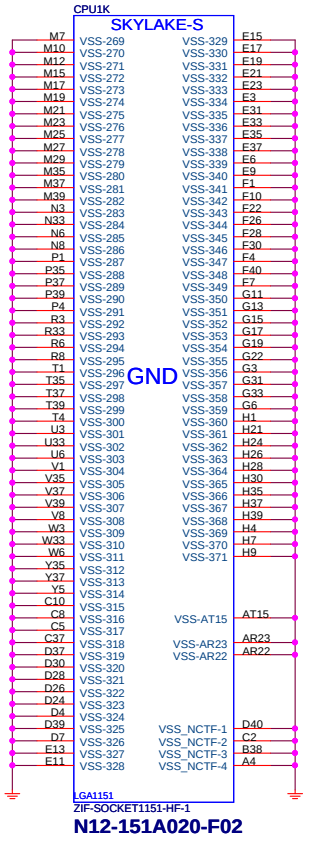
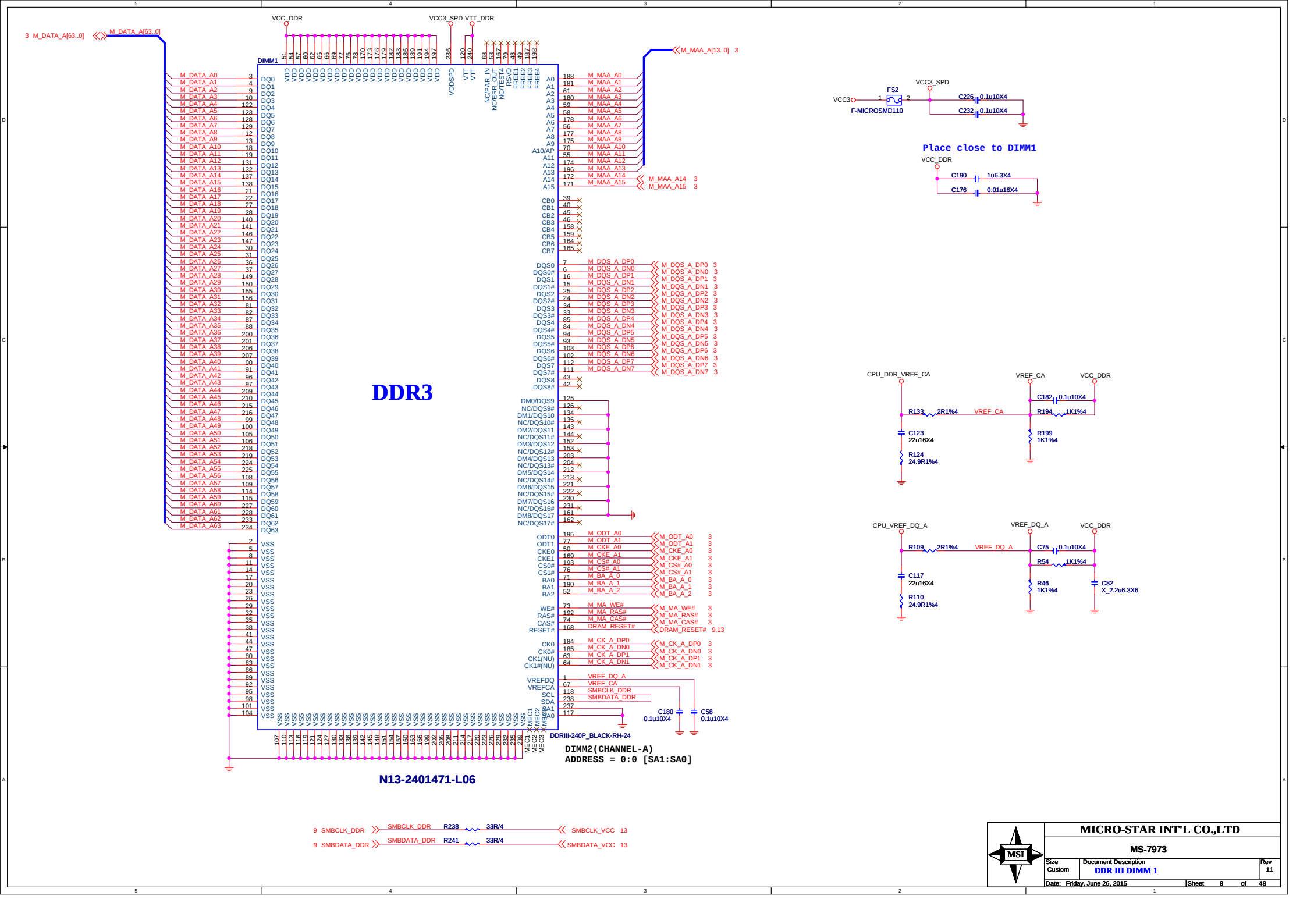




MICRO-STAR INT'L CO.,LTD			
MS-7973			
Size: Custom	Document Description: CPU-GND		Rev: 11
Date: Friday, June 26, 2015		Sheet 7 of 48	


DDR3
DIMM1
DDRIII-240P_BLACK-RH-24
DIMM2(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
N13-2401471-L06
Place close to DIMM1
MICRO-STAR INT'L CO.,LTD
MS-7973
DDR III DIMM 1
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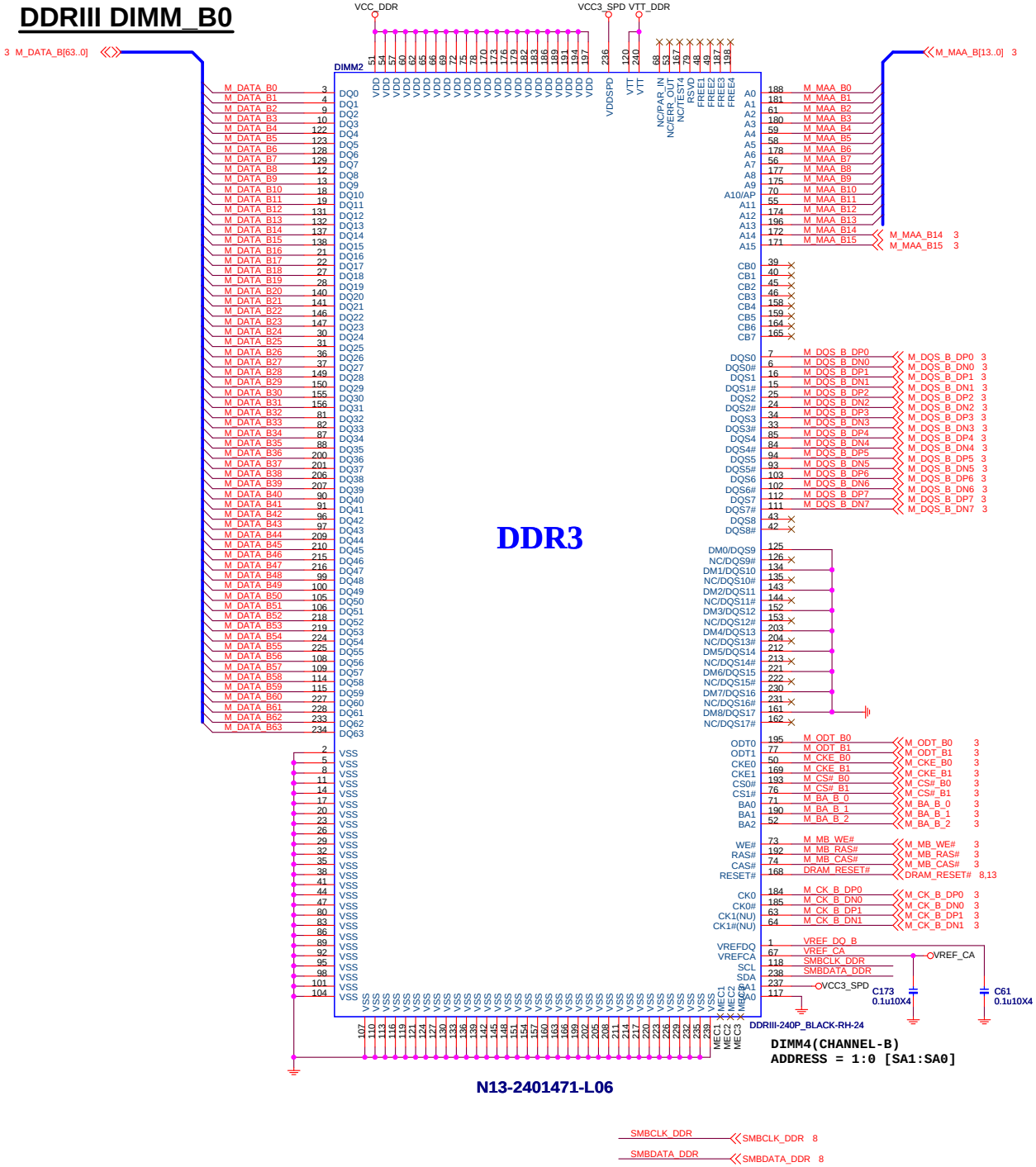
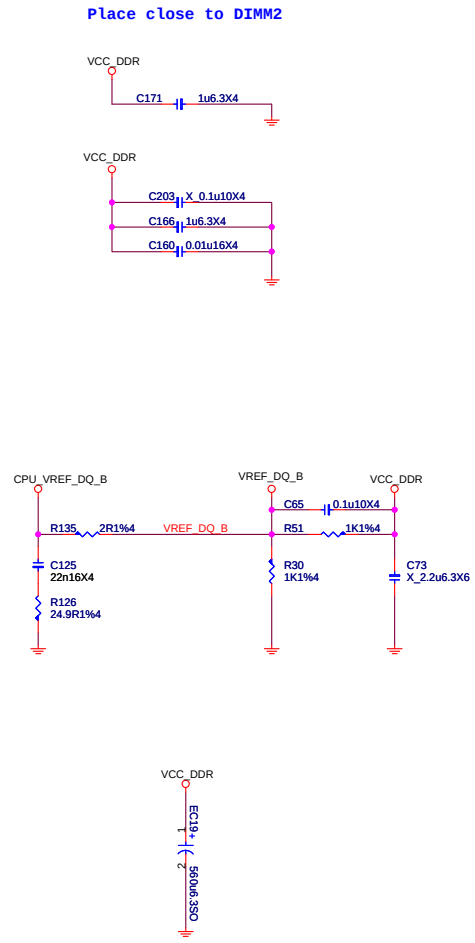
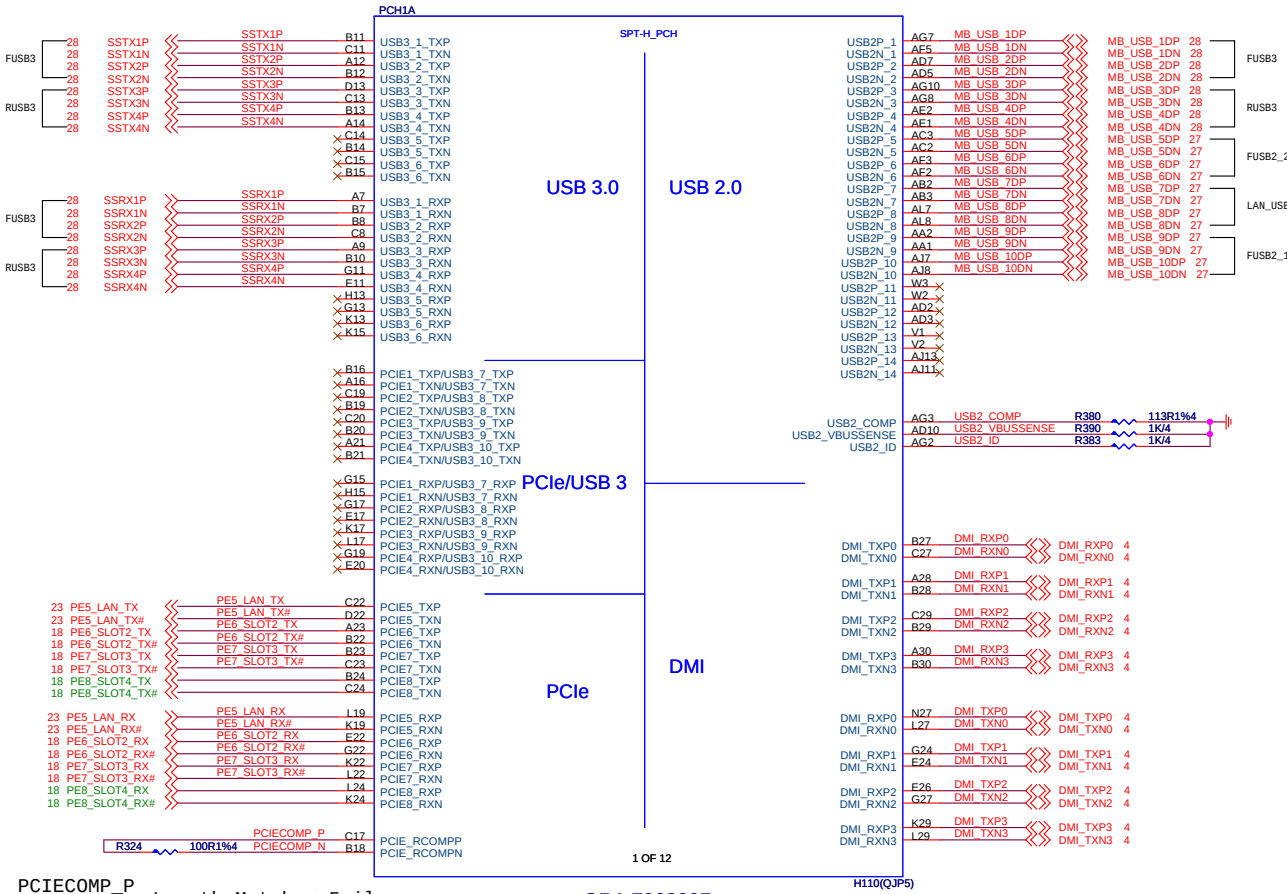
DDRIII DIMM_B0



DDRIII DIMM_B1

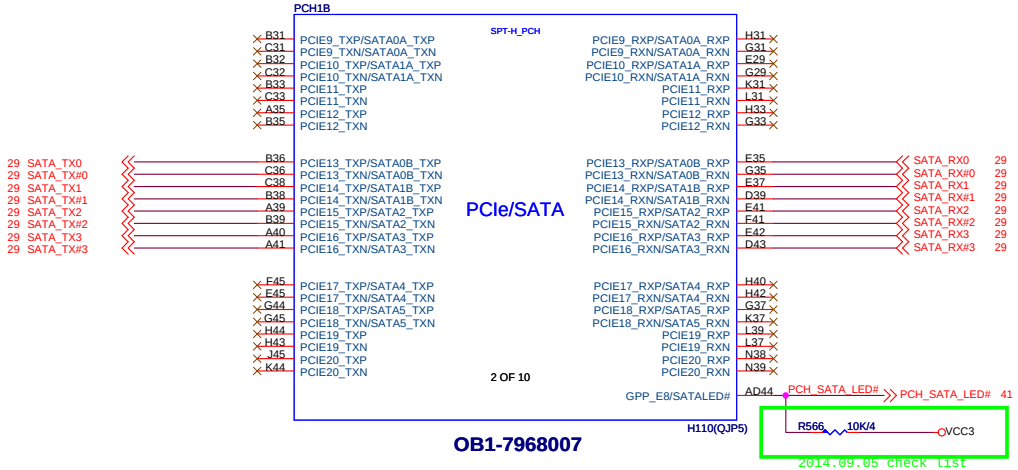


MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: DDR III DIMM 2	Rev: 11
Date: Friday, June 26, 2015	Sheet 9 of 48	



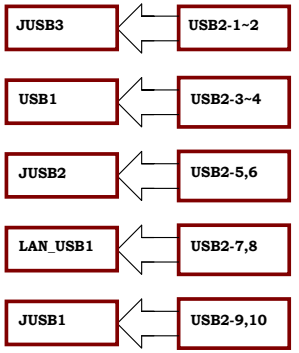
PCIECOMP_P
PCIECOMP_N Length Match < 5mil

OB1-7968007



OB1-7968007

2014.09.05 check list



USB2_COMP < 500 mil

	USB3[5-6]	USB3[7-8]
H110	X	X
B150	V	X
Q150	V	V
H170	V	X
Z170	V	X
Q170	V	X

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GPP_I[3:0] with SMI/NMI

EMI

AZ_BITCLK
CA23 X_10p50N4

PCH1D

21 AZ_BITCLK → AZ_BITCLK R449 33R/4 AZ_BITCLK_LR → BA9 HDA_BCLK
21 AZ_RST# → AZ_RST# R510 33R/4 AZ_RST#_R → BD8 HDA_RST#
21 AZ_SDIN0 → AZ_SDIN0 → BE7 HDA_SDI0
BC8 HDA_SDI1

16 AZ_SDOUT_R → AZ_SDOUT_R
21 AZ_SDOUT → AZ_SDOUT R489 33R/4 AZ_SDOUT_R → BB7 HDA_SDO
21 AZ_SYNC → AZ_SYNC R490 33R/4 AZ_SYNC_R → BD9 HDA_SYNC

5 PCH_CPU_AUD_SDO → R412 33R/4 PCH_CPU_AUD_SDO_R → AM1 DISPA_SDO
5 PCH_CPU_AUD_SDI → PCH_CPU_AUD_SDI → AN2 DISPA_SDI
5 PCH_CPU_AUD_SCLK → R419 33R/4 PCH_CPU_AUD_SCLK_R → AM2 DISPA_BCLK

AUDIO

AL42 GPP_D8/SSP0_SCLK
AN42 GPP_D7/SSP0_RXD
AM43 GPP_D6/SSP0_TXD
AJ33 GPP_D5/SSP0_SFRM

AH44 GPP_D20/DMIC_DATA0
AJ35 GPP_D19/DMIC_CLK0
AJ38 GPP_D18/DMIC_DATA1
AJ42 GPP_D17/DMIC_CLK1

4 OF 10

SPT-H_PCH

Port B
BA5 GPP_I5/DDPB_CTRLCLK → DSP_DDPB_CTRLCLK → DSP_DDPB_CTRLCLK 25
BC4 GPP_I6/DDPB_CTRLDATA → DSP_DDPB_CTRLDATA → DSP_DDPB_CTRLDATA 25
AW4 GPP_I0/DDPB_HPD0 → DSP_DDPB_HPD → DSP_DDPB_HPD 25

Port C
BB3 GPP_I7/DDPC_CTRLCLK → DVI_DDPC_CTRLCLK → DVI_DDPC_CTRLCLK 24
BD6 GPP_I8/DDPC_CTRLDATA → DVI_DDPC_CTRLDATA → DVI_DDPC_CTRLDATA 24
AY2 GPP_I1/DDPC_HPD1 → DVI_DDPC_HPD → DVI_DDPC_HPD 24

Port D
BE5 GPP_I9/DDPD_CTRLCLK → DP_DDPD_CTRLCLK
BE6 GPP_I10/DDPD_CTRLDATA → DP_DDPD_CTRLDATA
AV4 GPP_I2/DDPD_HPD2 → DP_HPD → DP_HPD 26
BA4 GPP_I3/DDPE_HPD3 → DDPE_HPD3 R428 10K/4

By Server CRB

eDP
W36 GPP_F21/EDP_BKLTCTL
W35 GPP_F20/EDP_BKLTEN
W42 GPP_F19/EDP_VDDEN
BD7 GPP_I4/EDP_HPD → EDP_HPD R476 100K/4

H110(QJP5)

VCC3
DSP_DDPB_CTRLCLK R414 2.2K/4
DSP_DDPB_CTRLDATA R422 2.2K/4
DVI_DDPC_CTRLCLK R410 2.2K/4
DVI_DDPC_CTRLDATA R415 2.2K/4
DP_DDPD_CTRLCLK R523 2.2K/4
DP_DDPD_CTRLDATA R492 2.2K/4

DDI interfaace Disable
no connect

Port B HDMI

Port C DVI,HDMI2.0 OR Others

Port D DisplayPort

OB1-7968007

EMI

CLK_BUFFER → CA25 X_10p50N4
CLK_SIO_PCI → CA26 X_10p50N4
CLK_SIO_24M → CA27 X_10p50N4
TPM_CLK → CA36 X_10p50N4

24M CLOCK BUFFER

3VSB
U19
CLK_SIO_24M R539 X_0R/4 CLK_BUFFER_OUT0
CLK_BUFFER R541 X_10K/4
CLK_IN OE CLK0 GND CLK3 CLK2 VDD CLK1
3VSB
R540 X_0R/4 CLK_BUFFER_OUT1
R520 X_0R/4 CLK_SIO_PCI
X_5V30014PGGI8_TSSOP8-HF

CO-LAY

CLK_BUFFER R516 X_22R/4
19 CLK_SIO_PCI → CLK_SIO_PCI R614 0R/4
19 CLK_SIO_24M → CLK_SIO_24M R613 22R/4 → CLK_PCH_LPC0 → BC17 GPP_A9/CLKOUT_LPC0/ESPI_CLK
41 TPM_CLK → R612 0R/4 → TPM_CLK_R → AV19 GPP_A10/CLKOUT_LPC1
TP18 CLKOUT_48M → AR17 GPP_A16/CLKOUT_48

PCH_CLK5_1P0 → R339 2.7K1%4 → XCLK_BIASREF → E1 XCLK_BIASREF

XCLK_BIASREF < 500 mil

PCH1C

SPT-H_PCH

CLKOUT_CPUBCLK_P G2 → PCH_CPU_BCLK_DP → PCH_CPU_BCLK_DP 5
CLKOUT_CPUBCLK_N H2 → PCH_CPU_BCLK_DN → PCH_CPU_BCLK_DN 5 100M

CLKOUT_CPUNSSC_P G1 → PCH_CPU_NSSC_CLK_DP → PCH_CPU_NSSC_CLK_DP 5
CLKOUT_CPUNSSC_N F1 → PCH_CPU_NSSC_CLK_DN → PCH_CPU_NSSC_CLK_DN 5 24M

CLKOUT_CPUPCIBCLK_P J2 → PCH_CPU_PCIE_DP → PCH_CPU_PCIE_DP 5
CLKOUT_CPUPCIBCLK_N J1 → PCH_CPU_PCIE_DN → PCH_CPU_PCIE_DN 5 100M

CLKOUT_ITPXDP_P L2
CLKOUT_ITPXDP_N L1

LAN
23 CLKREQ#4 →

CLKREQ#0 BC24 GPP_B5/SRCCLKREQ0#
CLKREQ#1 AW24 GPP_B6/SRCCLKREQ1#
CLKREQ#2 AT24 GPP_B7/SRCCLKREQ2#
CLKREQ#3 BD25 GPP_B8/SRCCLKREQ3#
CLKREQ#4 BB24 GPP_B9/SRCCLKREQ4#
CLKREQ#5 BE25 GPP_B10/SRCCLKREQ5#
CLKREQ#6 AT33 GPP_H0/SRCCLKREQ6#
CLKREQ#7 AR31 GPP_H1/SRCCLKREQ7#
CLKREQ#8 BD32 GPP_H2/SRCCLKREQ8#
CLKREQ#9 BC32 GPP_H3/SRCCLKREQ9#
CLKREQ#10 BB31 GPP_H4/SRCCLKREQ10#
CLKREQ#11 BC33 GPP_H5/SRCCLKREQ11#
CLKREQ#12 BA33 GPP_H6/SRCCLKREQ12#
CLKREQ#13 AW33 GPP_H7/SRCCLKREQ13#
CLKREQ#14 BB33 GPP_H8/SRCCLKREQ14#
CLKREQ#15 BD33 GPP_H9/SRCCLKREQ15#

Clock

CLKOUT_SRC_P0 N8 → CK_SLOT2_DP 18
CLKOUT_SRC_N0 N7 → CK_SLOT2_DN 18
CLKOUT_SRC_P1 L5 → CK_SLOT4_DP 18
CLKOUT_SRC_N1 L7 → CK_SLOT4_DN 18
CLKOUT_SRC_P2 F2
CLKOUT_SRC_N2 D3
CLKOUT_SRC_P3 G4 → CK_SLOT1_DP 17
CLKOUT_SRC_N3 E5 → CK_SLOT1_DN 17
CLKOUT_SRC_P4 E6 → CK_PE_LAN 23
CLKOUT_SRC_N4 D5 → CK_PE_LAN# 23
CLKOUT_SRC_P5 D7
CLKOUT_SRC_N5 D8
CLKOUT_SRC_P6 R7
CLKOUT_SRC_N6 R8
CLKOUT_SRC_P7 U7
CLKOUT_SRC_N7 U5
CLKOUT_SRC_P8 W11
CLKOUT_SRC_N8 W10
CLKOUT_SRC_P9 N2
CLKOUT_SRC_N9 N3
CLKOUT_SRC_P10 P2
CLKOUT_SRC_N10 P3
CLKOUT_SRC_P11 R4 → CK_SLOT3_DP 18
CLKOUT_SRC_N11 R3 → CK_SLOT3_DN 18
CLKOUT_SRC_P12 U3
CLKOUT_SRC_N12 U2
CLKOUT_SRC_P13 Y5
CLKOUT_SRC_N13 W7
CLKOUT_SRC_P14 R2
CLKOUT_SRC_N14 P1
CLKOUT_SRC_P15 R11
CLKOUT_SRC_N15 R13

XTAL_24M_PCH_IN A6 XTAL24_IN
XTAL_24M_PCH_OUT A5 XTAL24_OUT

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H110(QJP5)

OB1-7968007

VCC3
R527 10K/4 CLKREQ#0
R529 10K/4 CLKREQ#1
R531 10K/4 CLKREQ#2
R528 10K/4 CLKREQ#3
R501 10K/4 CLKREQ#4
R546 10K/4 CLKREQ#5
R479 10K/4 CLKREQ#6
R405 10K/4 CLKREQ#7
R465 10K/4 CLKREQ#8
R466 10K/4 CLKREQ#9
R481 10K/4 CLKREQ#10
R468 10K/4 CLKREQ#11
R478 10K/4 CLKREQ#12
R477 10K/4 CLKREQ#13
R469 10K/4 CLKREQ#14
R467 10K/4 CLKREQ#15

Conntact to SLOT Pin B12
for support L1 PM Substates
ME also can disable this funtion.

XTAL_24M_PCH_OUT
XTAL_24M_PCH_IN
R327 1M1%6
Y1
24MHZ20P
C332 22p50N4
C326 22p50N4

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W/ SMI/NMI Funtion

GPP_B[23,20,14]
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]

3VSB PWR_GPP_A CP13 BC42 C380 X_0.1u10X4

2014.10.16 PCH cOM BACK test

CRB R400 X_8.2K1%4 GPP_E3 R545 8.2K1%4 GPP_B4

GPP_B11 default GPO to LOW

If the interface is not used: the signals can be used as GPIO. If GPIO functionality is also not used, the signals can be left as no-connect.

ISH For U,Y only use

UART/GPIO no use can no connect

SML For sever only use

PCH1F

SPT-H_PCH

GPIO A: BA31 VCCPGPPA; BC19 GPP_A17/ISH_GP7; BB22 GPP_A18/ISH_GP0; BD21 GPP_A19/ISH_GP1; BD22 GPP_A20/ISH_GP2; BE21 GPP_A21/ISH_GP3; BD18 GPP_A22/ISH_GP4; BC22 GPP_A23/ISH_GP5

GROUP BCH PWR: BC42 VCCPGPPBCH_BC42; BD40 VCCPGPPBCH_BD40

GPIO B: BC23 GPP_B3/CPU_GP2; BD24 GPP_B4/CPU_GP3; AN24 GPP_B11; AR24 GPP_B15/GSPI0_CS#; AW27 GPP_B16/GSPI0_CLK; BD27 GPP_B17/GSPI0_MISO; BD28 GPP_B18/GSPI0_MOSI; BC27 GPP_B19/GSPI1_CS#; AV29 GPP_B20/GSPI1_CLK; AR29 GPP_B21/GSPI1_MISO; AT29 GPP_B22/GSPI1_MOSI

GPIO C: BA41 GPP_C8/UART0_RXD; AV44 GPP_C9/UART0_TXD; AV43 GPP_C10/UART0_RTS#; AU44 GPP_C11/UART0_CTS#; AU43 GPP_C12/UART1_RXD/ISH_UART1_RXD; AT43 GPP_C13/UART1_TXD/ISH_UART1_TXD; AT44 GPP_C14/UART1_RTS#/ISH_UART1_RTS#; AU41 GPP_C15/UART1_CTS#/ISH_UART1_CTS#; AT42 GPP_C16/I2C0_SDA; AR38 GPP_C17/I2C0_SCL; AR44 GPP_C18/I2C1_SDA; AR41 GPP_C19/I2C1_SCL; AR45 GPP_C20/UART2_RXD; AR39 GPP_C21/UART2_TXD; AN44 GPP_C22/UART2_RTS#; AN43 GPP_C23/UART2_CTS#

GPIO H: BD34 GPP_H10/SML2CLK; AW35 GPP_H11/SML2DATA; BD35 GPP_H12/SML2ALERT#; BC35 GPP_H13/SML3CLK; BA35 GPP_H14/SML3DATA; BB36 GPP_H15/SML3ALERT#; BD39 GPP_H16/SML4CLK; BE34 GPP_H17/SML4DATA; BC36 GPP_H18/SML4ALERT#; BB38 GPP_H19/ISH_I2C0_SDA; BC38 GPP_H20/ISH_I2C0_SCL; BE39 GPP_H21/ISH_I2C1_SDA; BD38 GPP_H22/ISH_I2C1_SCL; BD36 GPP_H23

GROUP CD PWR: BC44 VCCPGPPCD_BC44; BA45 VCCPGPPCD_BA45; BC45 VCCPGPPCD_BC45; BB45 VCCPGPPCD_BB45 → PWR_GPP_D

GPIO D: AM44 GPP_D4 / ISH_I2C2_SDA / I2C3_SDA; AL44 GPP_D9 → TP60; AL36 GPP_D10 → TP77; AL35 GPP_D11 → TP28; AJ39 GPP_D12 → TP29; AK45 GPP_D13/ISH_UART0_RXD; AK44 GPP_D14/ISH_UART0_TXD; AL43 GPP_D15/ISH_UART0_RTS#; AJ43 GPP_D16/ISH_UART0_CTS#; AJ44 GPP_D23 / ISH_I2C2_SCL / I2C3_SCL

GROUP EF PWR: AJ41 VCCPGPPEF_AJ41; AL41 VCCPGPPEF_AL41 → 3VSB

GPIO E: AF41 GPP_E3; AE44 GPP_E7 → TP40

GPIO F: AB33 GPP_F10 → TP43; AB35 PCH_RSVD; AA45 SV_ADVANCE; AA44 GFX_CRB_DETECT; Y44 CPU_SKTOCC#_R R373 X_0R/4 → CPU_SKTOCC# 5; W39 GPP_F22 → GPP_F22 17; V44 GPP_F23 → TP49

2014.08.14

GPIO G: AD41 VCCPGPPG → 3VSB; U43 GPP_G0/FAN_TACH_0; U42 GPP_G1/FAN_TACH_1; U41 GPP_G2/FAN_TACH_2; M44 GPP_G3/FAN_TACH_3; U36 GPP_G4/FAN_TACH_4; P44 GPP_G5/FAN_TACH_5; T45 GPP_G6/FAN_TACH_6; T44 GPP_G7/FAN_TACH_7; R44 GPP_G8/FAN_PWM_0; R43 USB_MODE → TP50; U39 GPP_G9/FAN_PWM_1; N42 GPP_G10/FAN_PWM_2; N43 GPP_G11 R553 X_0R/4 → ME_DIS# 13,16; R39 GPP_G11/FAN_PWM_3; R36 GPP_G12/GSXDOUT; R42 GPP_G13/GSXSLOAD; R41 GPP_G14/GSXDIN; R43 GPP_G15/GSXSRESET#; N44 GPP_G16/GSXCLK; R35 GPP_G17/ADR_COMPLETE; U35 TEST_SETUP_MENU; L44 GPP_G20; L43 GPP_G21; GPP_G22; GPP_G23

Remove

2014.08.14

GPIO DSW: BA24 VCCDSW_3P3_BA24 → 3VDSW; BD14 GPD7/RSVD → GPD7 → TP87

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H110(QJP5)

OB1-7968007

3VSB PWR_GPP_D CP16

3VSB AJ41 C367 X_0.1u10X4; 3VSB AD41 C356 X_0.1u10X4

GPP_F22 R392 10K/4 VCC3

TEST_SETUP_MENU R346 10K/4 VCC3; R355 X_10K/4 3VSB

PCH_RSVD R406 10K/4 VCC3; R417 X_10K/4 3VSB

GFX_CRB_DETECT R387 X_10K/4 VCC3; R378 10K/4; R376 X_10K/4 3VSB

SV_ADVANCE R398 20K/4 VCC3; R386 X_10K/4 3VSB

For BIOS BOM USE

3VSB R362 10K/4 GPP_G21 R365 X_10K/4; R344 10K/4 GPP_G22 R345 X_10K/4; R333 10K/4 GPP_G23 R338 X_10K/4

When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

PCH1E

SPT-H_PCH

C359 C357 C350 C355 C352 X_0.1u10X4 OC#0 OC#1 OC#2 OC#3 OC#4 27

3VSB R382 R370 R369 10K/4 OC#5 OC#6 OC#7

USB OC#: AD43 GPP_E9/USB2_OC0#; AD42 GPP_E10/USB2_OC1#; AD39 GPP_E11/USB2_OC2#; AC44 GPP_E12/USB2_OC3#; Y43 GPP_F15 / USB2_OC4#; Y41 GPP_F16 / USB2_OC5#; W44 GPP_F17 / USB2_OC6#; W43 GPP_F18 / USB2_OC7#

SATA DEVSLP: AG42 GPP_E4/DEVSLP0 → GPP_E4 → TP19; AG43 GPP_E5/DEVSLP1 → GPP_E5 → TP21; AE45 GPP_E6/DEVSLP2; AB41 GPP_F5/DEVSLP3; AB42 GPP_F6/DEVSLP4; AB43 GPP_F7/DEVSLP5; AB36 GPP_F8/DEVSLP6; AB39 GPP_F9/DEVSLP7

RSVD For B150 SATA/PCIE use

Remove

CLINK: AV2 CL_CLK; AV3 CL_DATA; AW2 CL_RST#

SATA Strap: AG36 GPP_E0/SATAXPCIE0/SATAGP0 → GPP_E0 → TP30; AG35 GPP_E1/SATAXPCIE1/SATAGP1 → GPP_E1 → TP27; AG39 GPP_E2/SATAXPCIE2/SATAGP2; AD35 GPP_F0/SATAXPCIE3/SATAGP3; AD31 GPP_F1/SATAXPCIE4/SATAGP4; AD38 GPP_F2/SATAXPCIE5/SATAGP5; AC43 GPP_F3/SATAXPCIE6/SATAGP6; AB44 GPP_F4/SATAXPCIE7/SATAGP7

RSVD For B150 SATA/PCIE use

2014.08.14

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H110(QJP5)

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If an AMT capable Intel WLAN device is not implemented then this signal can be left as NO CONNECT (NC).

MICRO-STAR INT'L CO.,LTD

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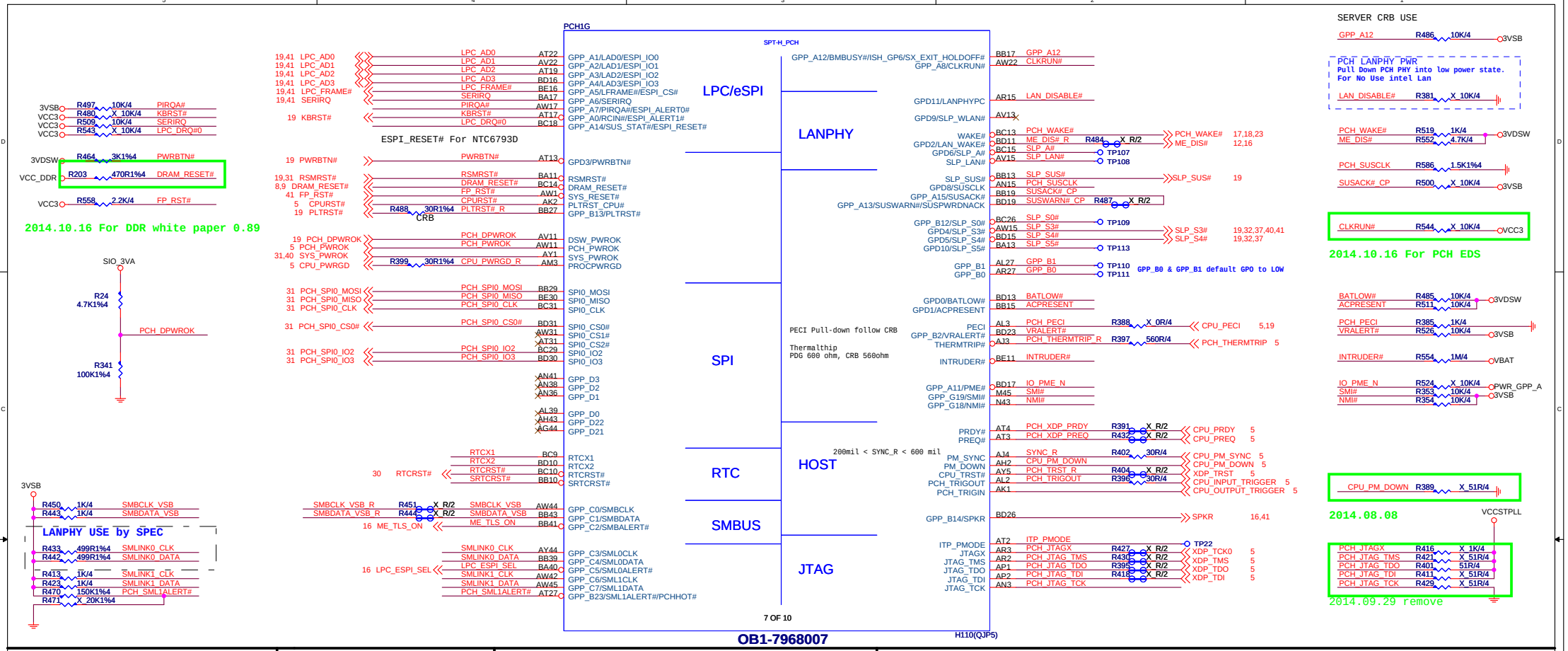
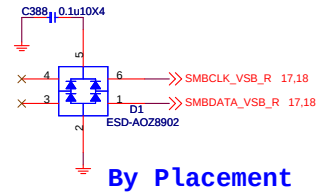


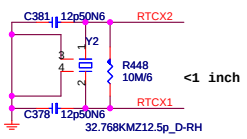
SMBUS ESD



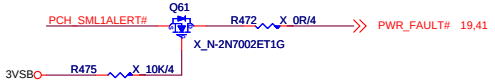
By Placement

RTC Block

Close to PCH



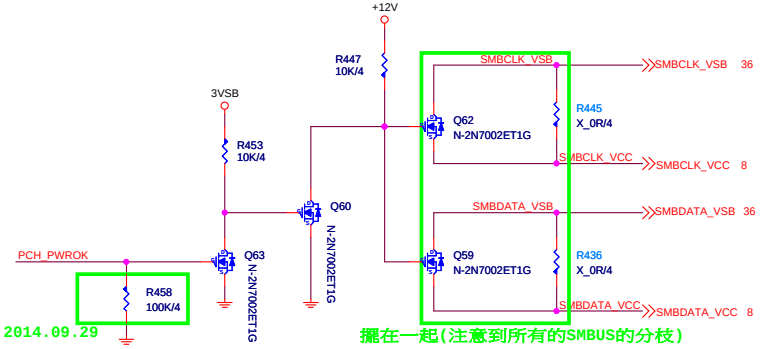
PCH Thermal Monitor



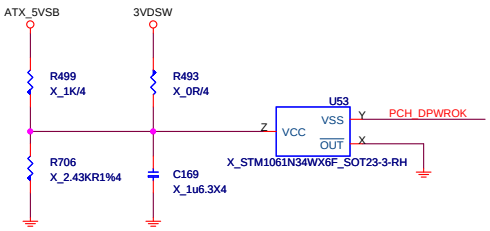
當溫度高於設定之後，此信號會被拉LOW。
PS:只能在S0下使用，S5 不會有功能

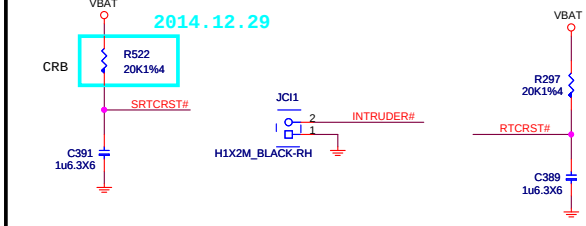
SMBUS隔離線路(PCH接出來是PULL HIGH 3VSB)
需要再S3/S5底下動作的接SMBCLK_VSB/SMBDATA_VSB
不需要的接SMBCLK_VCC/SMBDATA_VCC

基本上PCIE的SLOT要接3VSB的CPU的PWM IC/DDR要接VCC3的其他的請注意要怎麼接

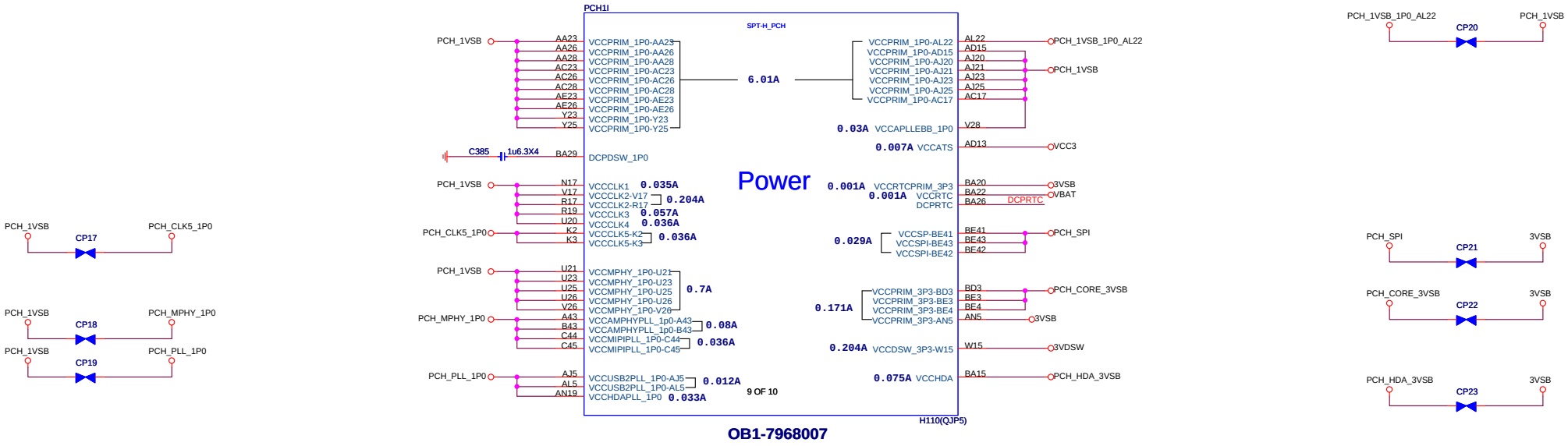


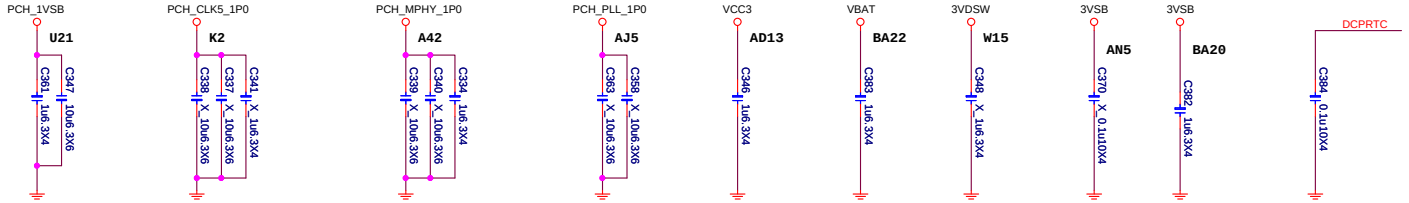
2015.6.11 channel reserve

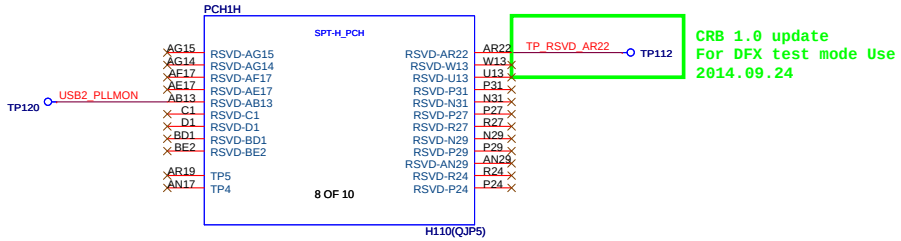




MICRO-STAR INT'L CO.,LTD	
MS-7973	
Size: Custom	Document Description: PCH-LPC/SPI/SMBUS/MISC
Rev: 11	
Date: Friday, June 26, 2015	Sheet 13 of 48







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MS-7973		
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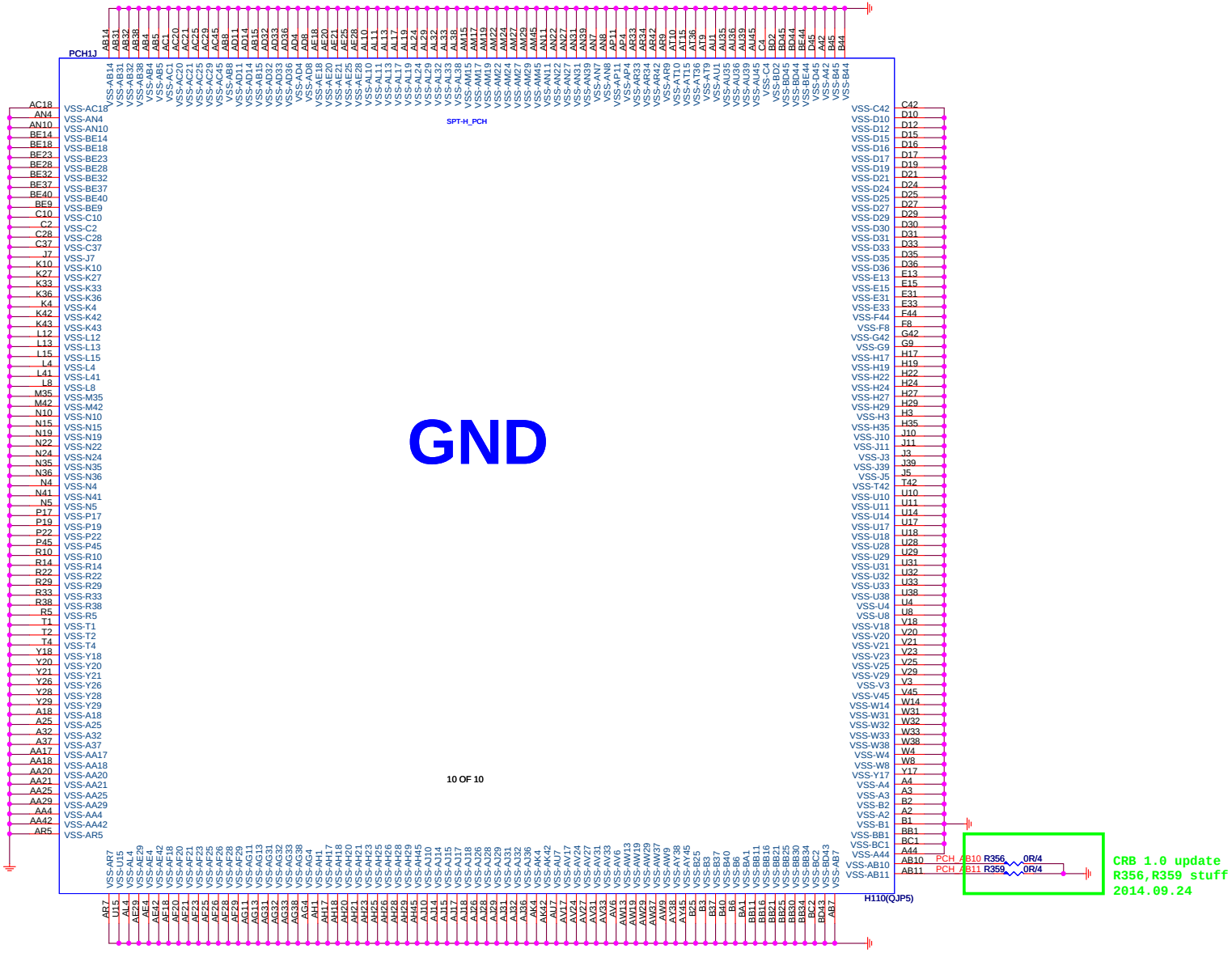

CRB 1.0 update
R356,R359 stuff
2014.09.24

OB1-7968007

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MS-7973			
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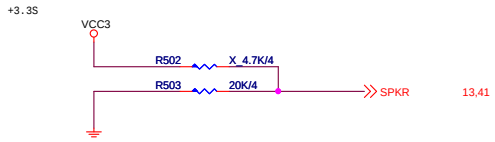
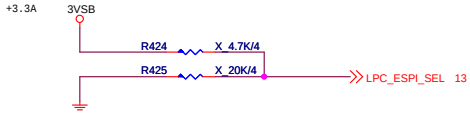
TOP Swap



Internal pull-down 20K is disabled after PLTRST#

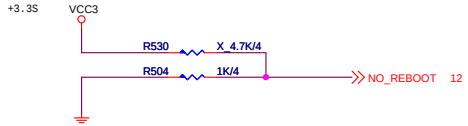
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

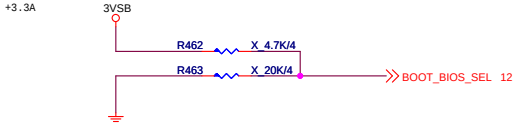
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

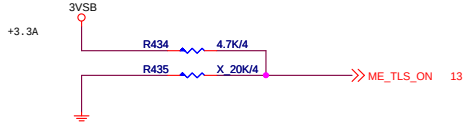
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

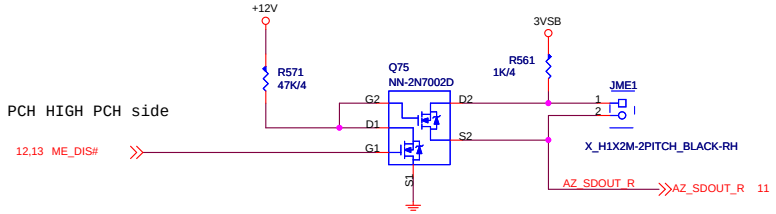
AMT and SBA with confidentiality



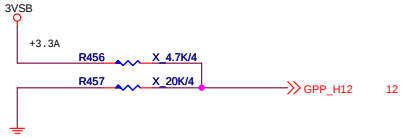
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

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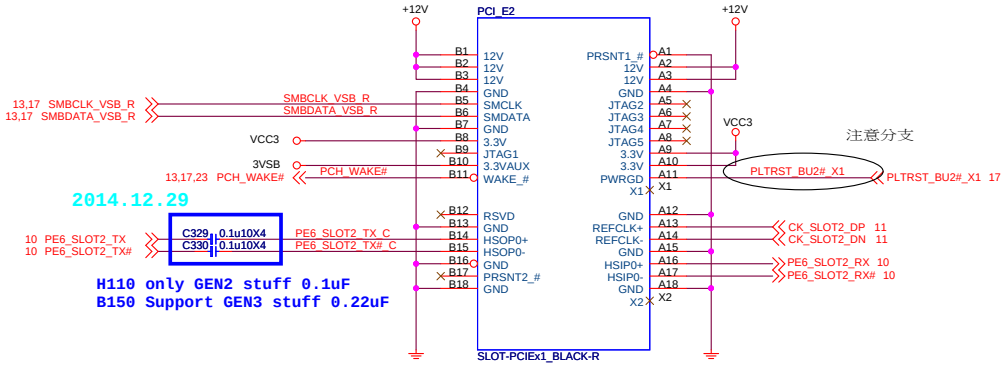
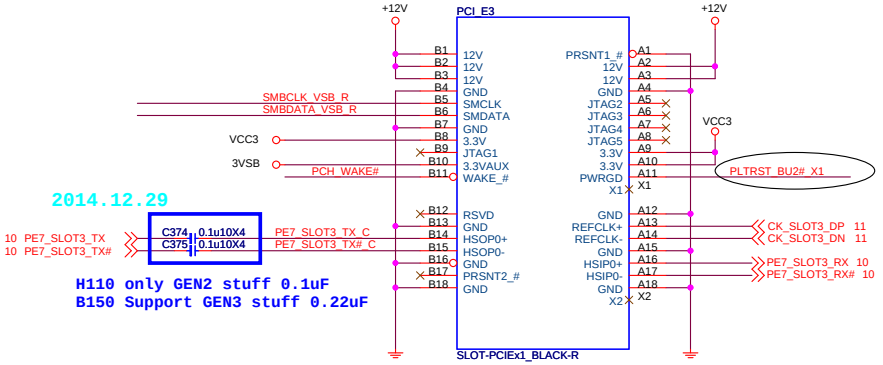
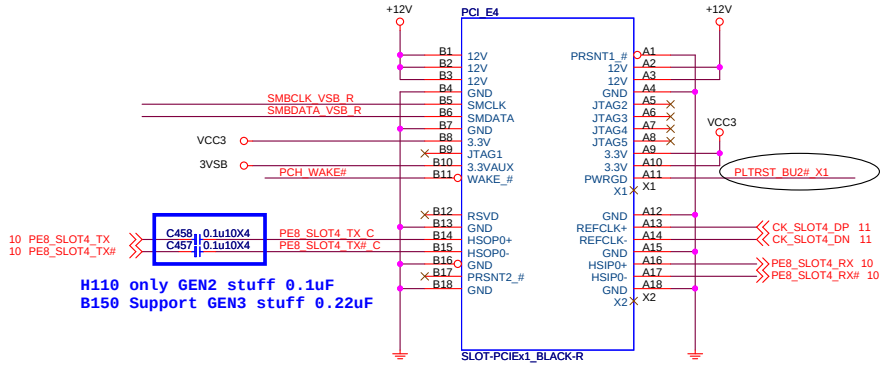


N11-0360381-L06



N11-0360381-L06



N11-0360381-L06

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Custom	PCIE SLOT-PCH(X1)	11

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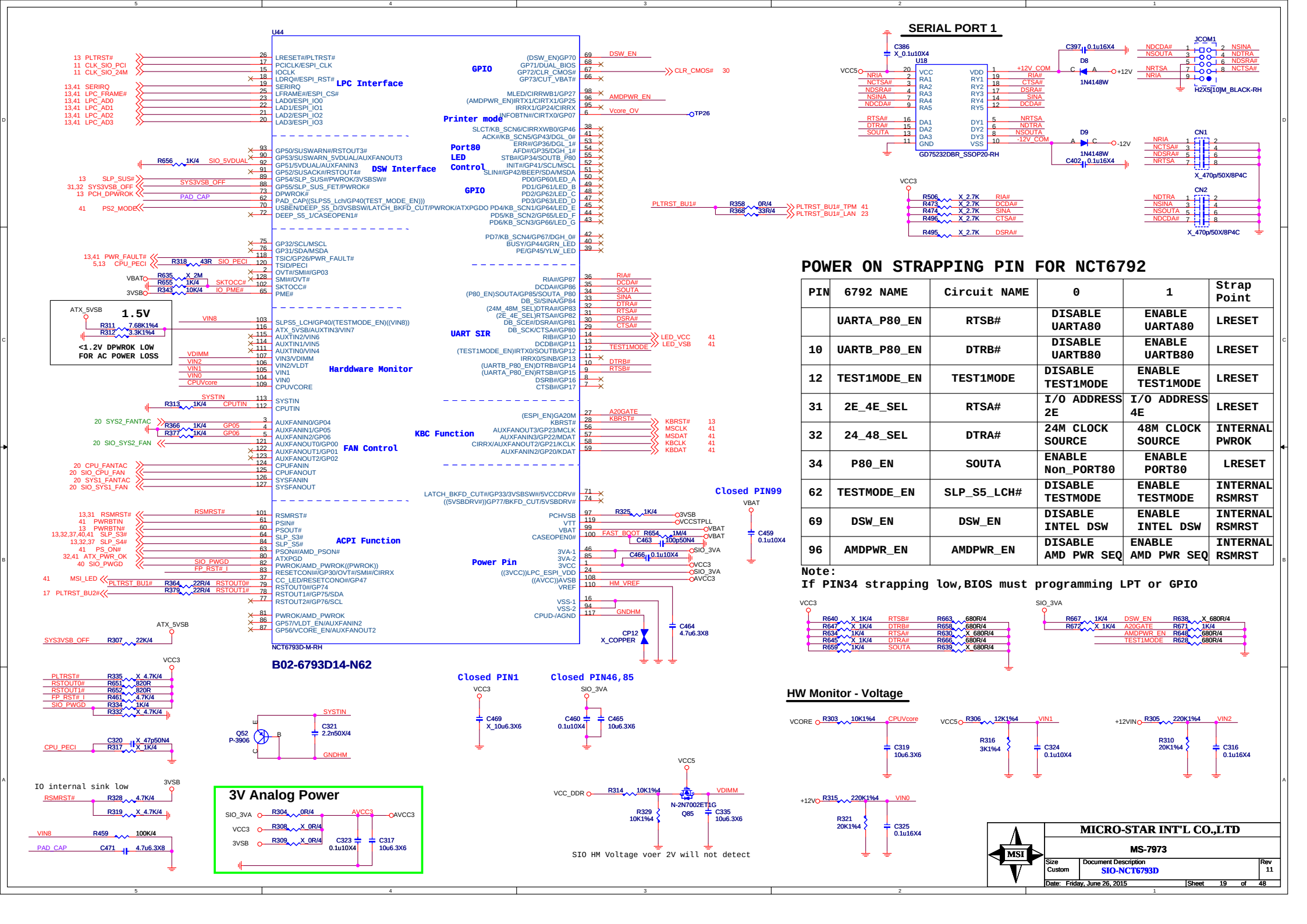

POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

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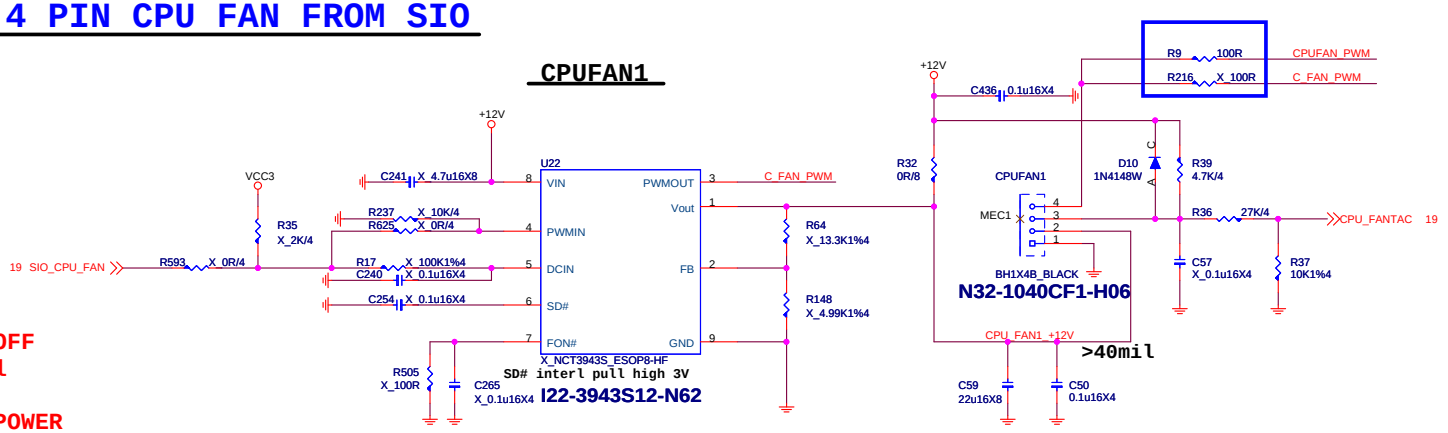
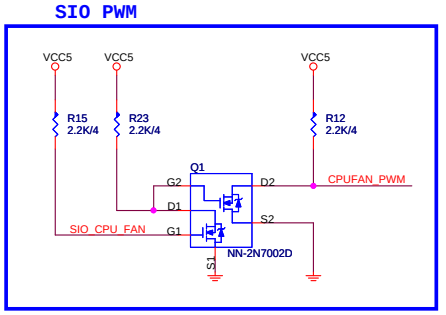
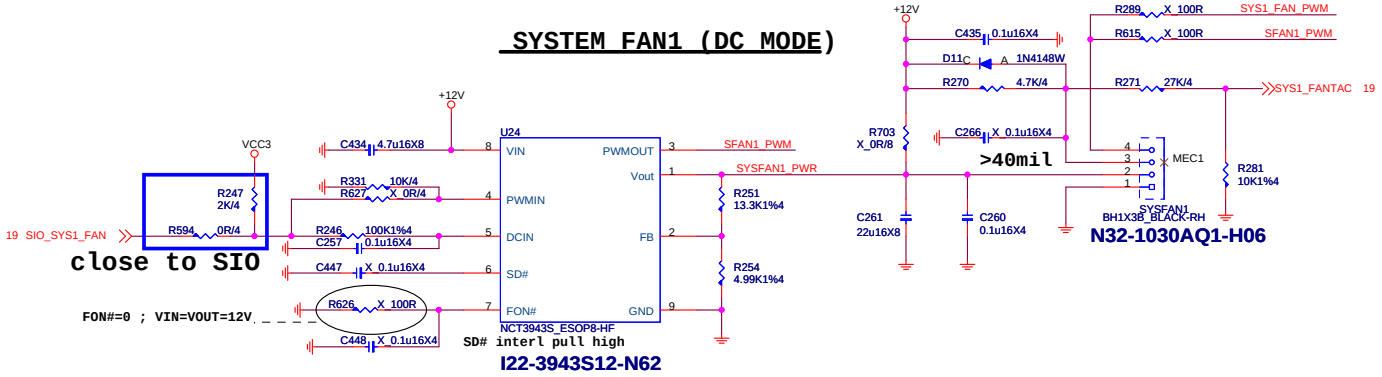
Type G : 4 PIN CPU FAN FROM SIO

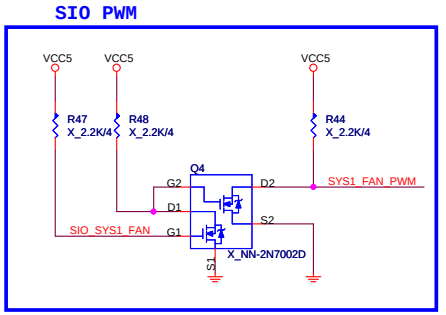


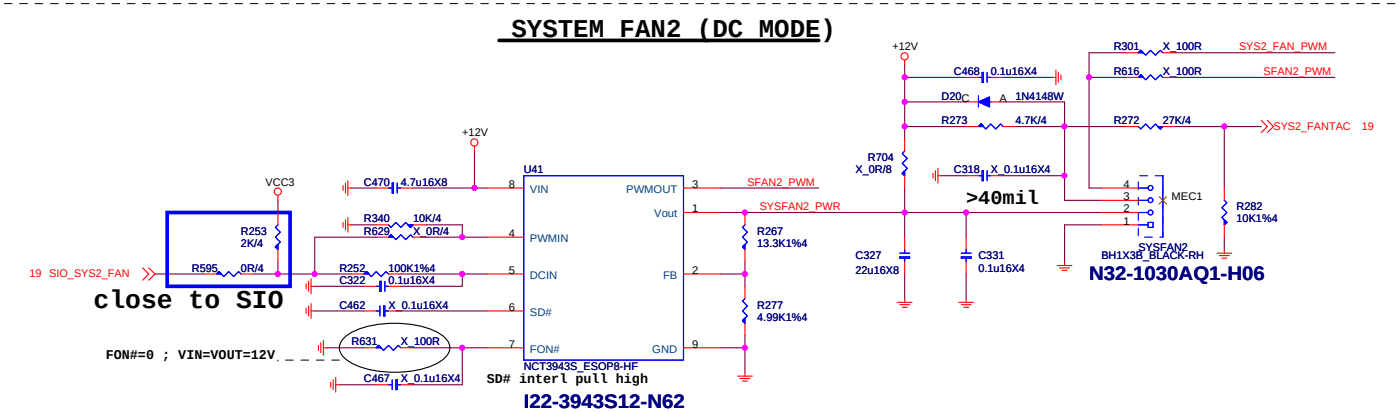


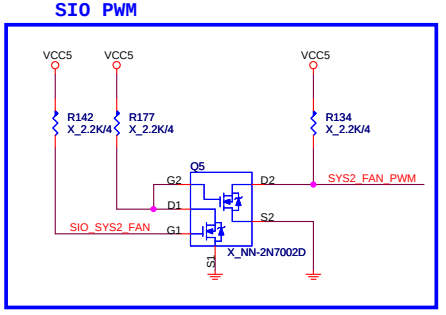
CPUFAN_PWR_OFF
GPIO Control
Deafult GPI
If USE CUT POWER
1.OPEN DRAIN LOW:SD# LOW Active，CPUFAN(PIN2)= 0V
2.OPEN DRAIN : SD# Internal Pull high，CPUFAN(PIN2)=12V

Type H : 4 PIN SYS FAN FROM SIO









MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	FAN CONTROLLOR	11

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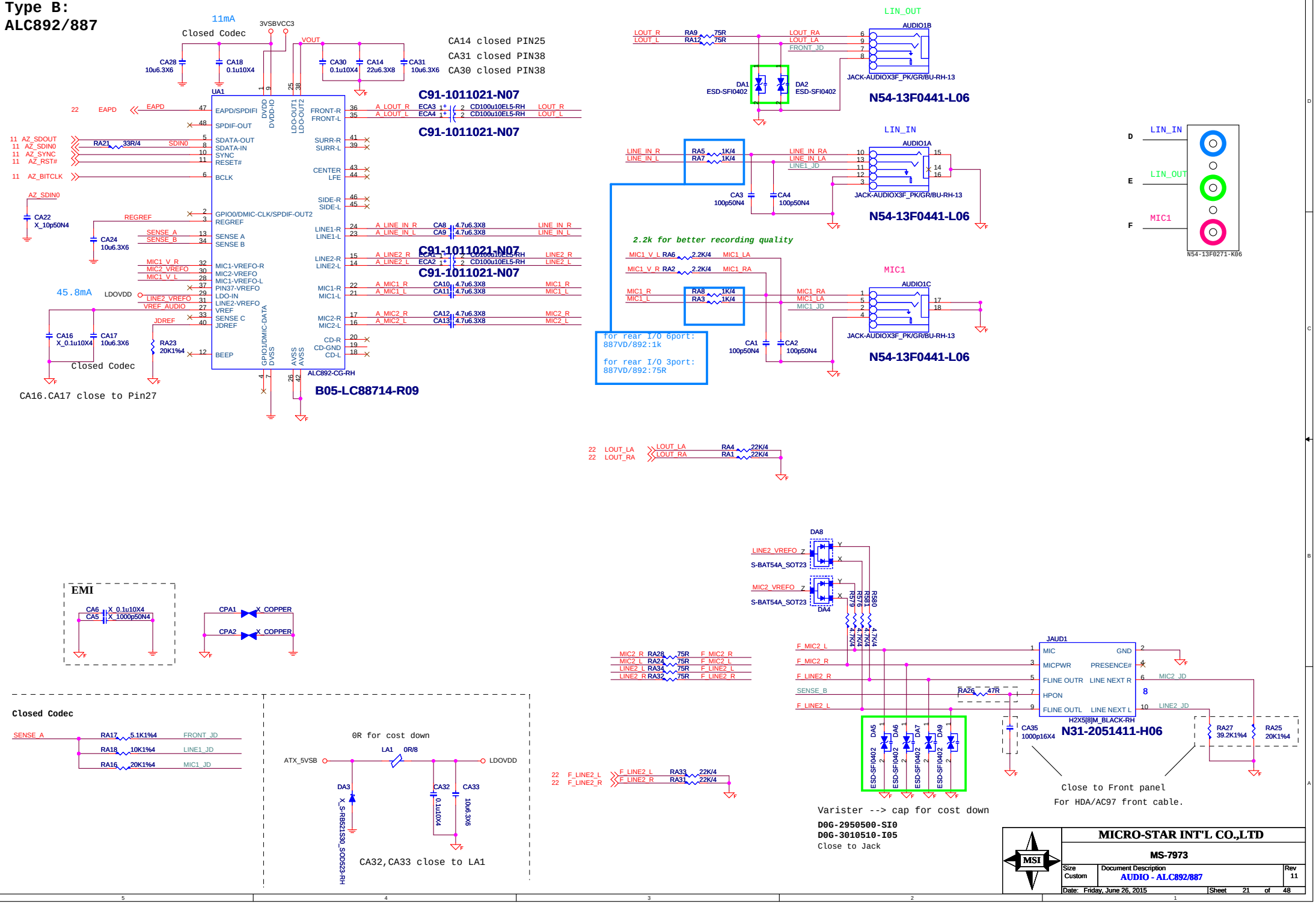
Type B: ALC892/887



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MS-7973	
Size: Custom	Document Description: AUDIO - ALC892/887
Rev: 11	
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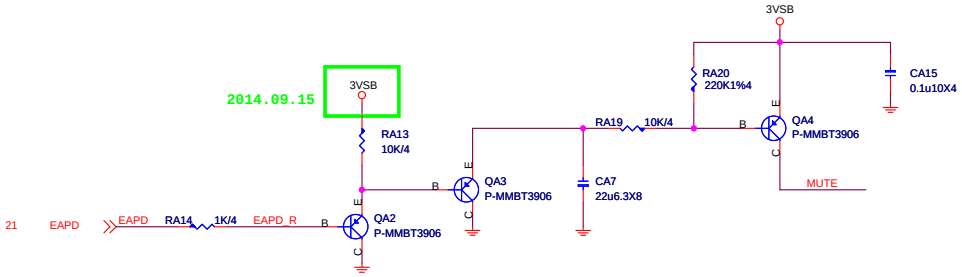
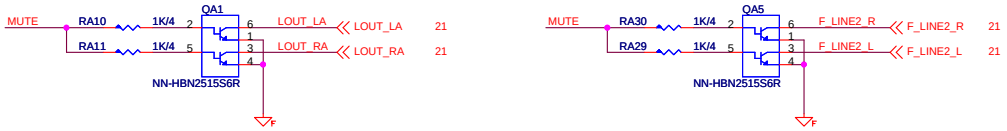
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

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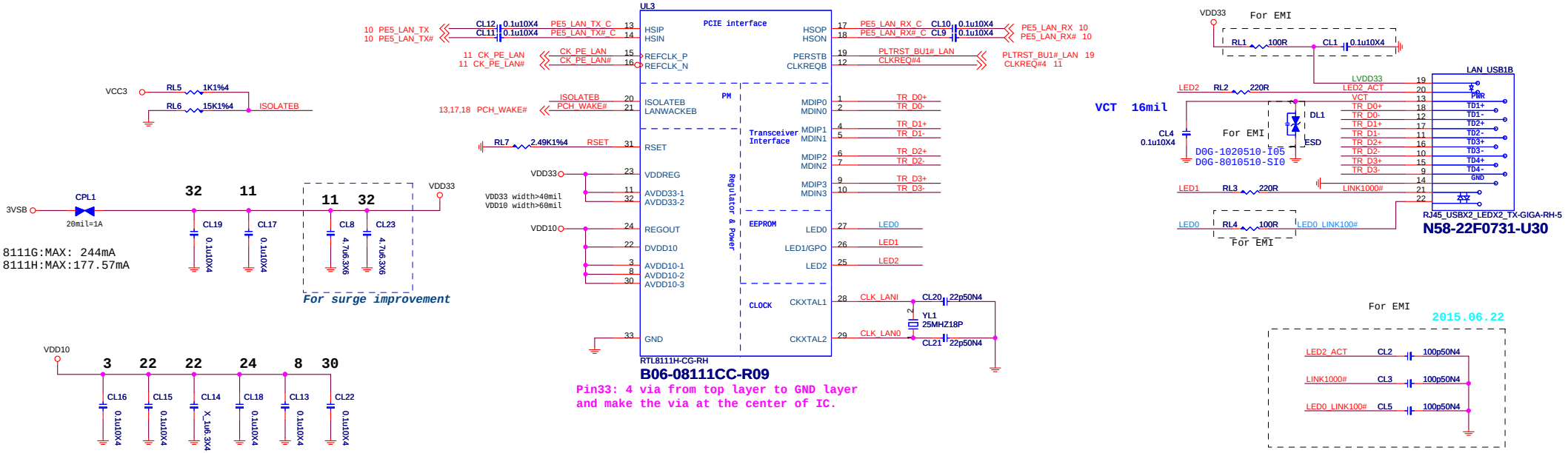
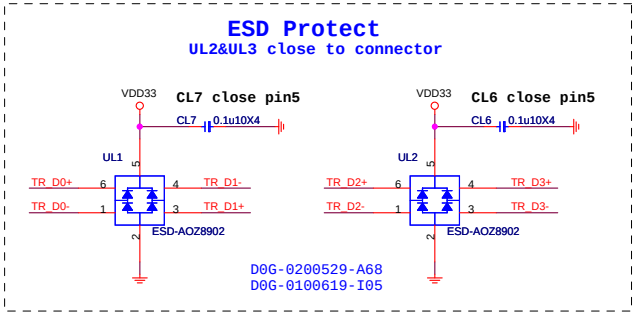
RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09



LAN Connector



8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

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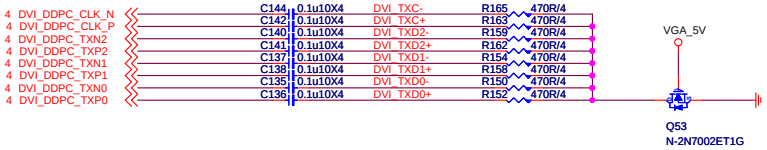
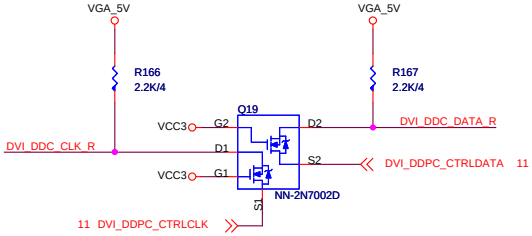
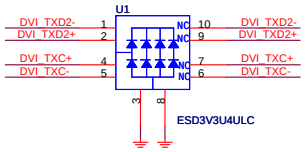
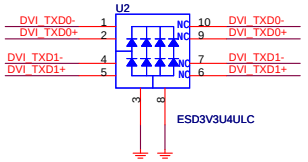
DVI level shifter

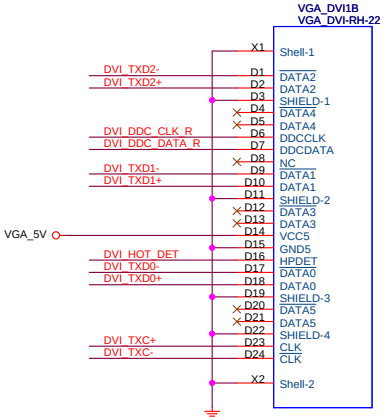
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)





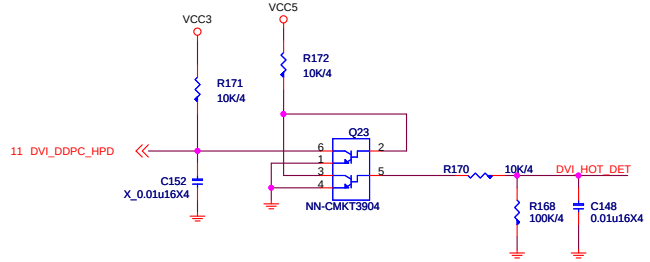




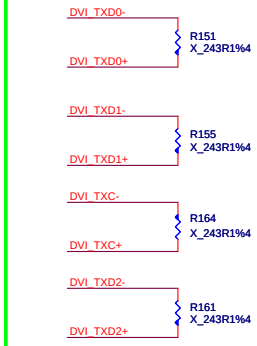


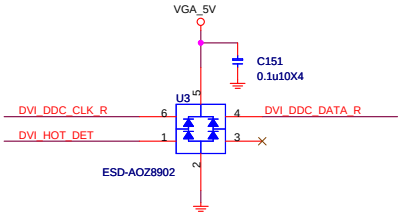
N58-39F0281-EB6

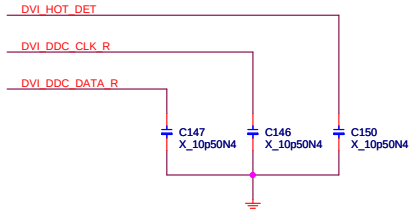
HPD



For EMI







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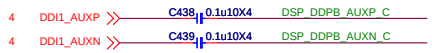
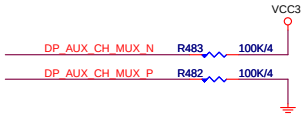
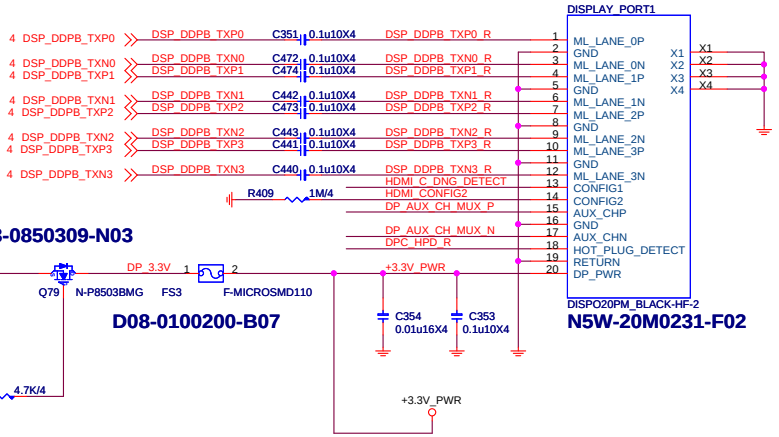
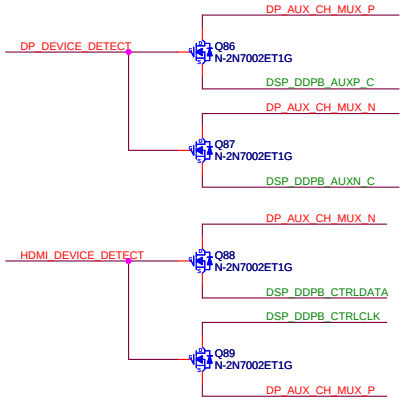
DISPLAY PORT



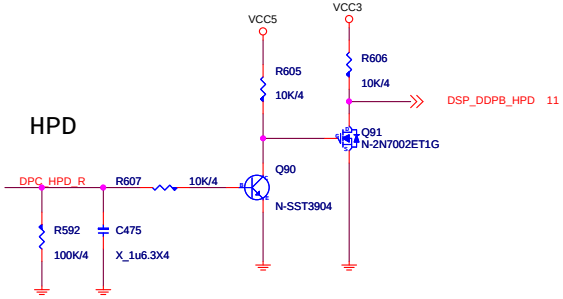


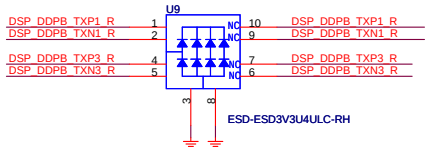


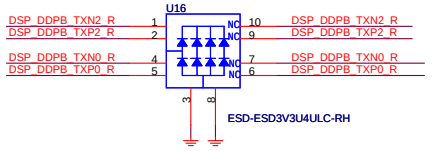
D03-7002E89-O05

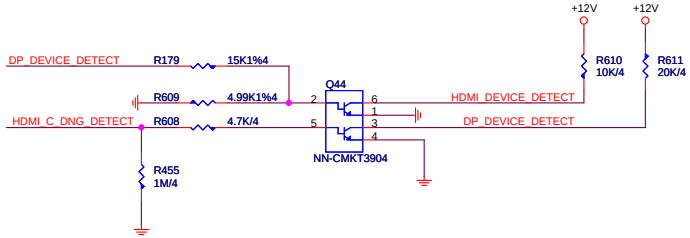


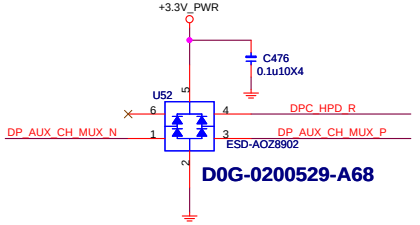
HPD











	DP	HDMI
HDMI_C_DNG_DETECT	L	H
DP_DEVICE_DETECT	H	L
HDMI_DEVICE_DETECT	L	H

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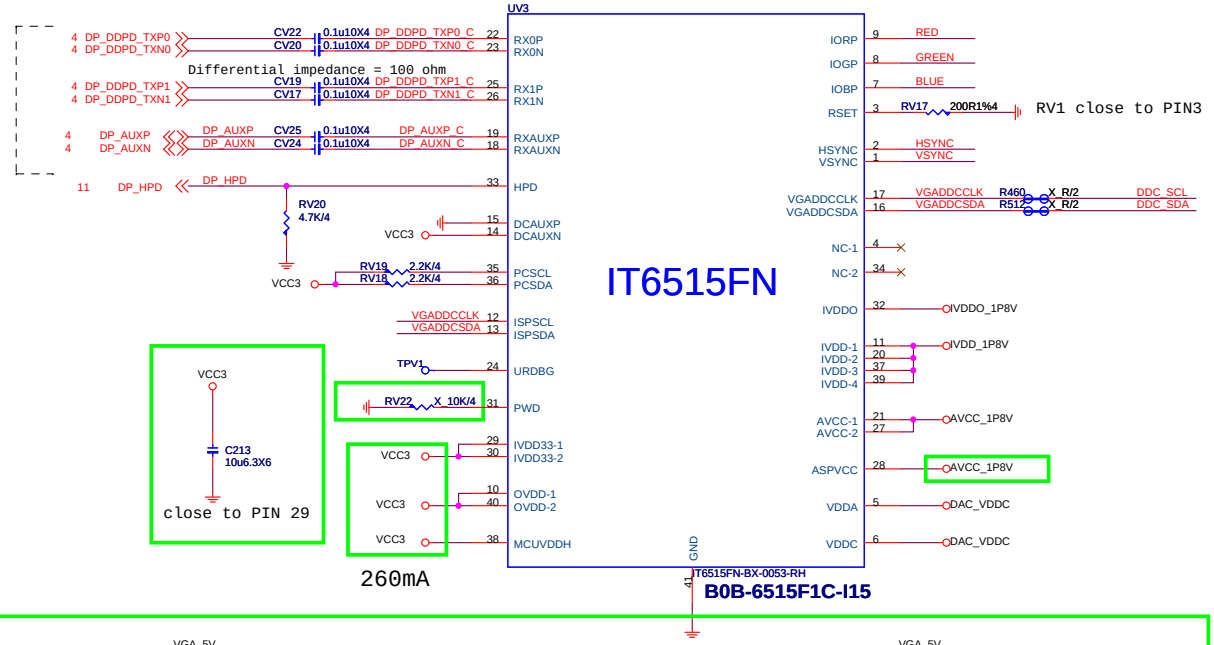
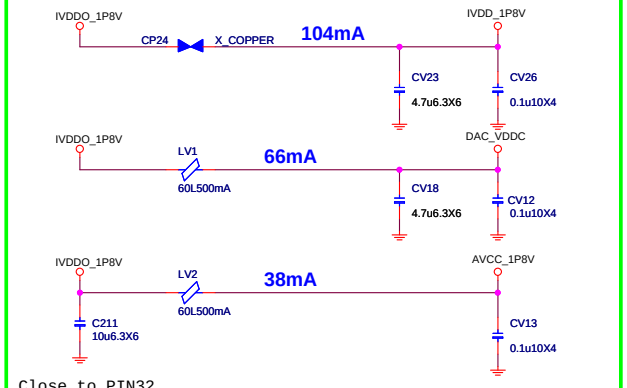
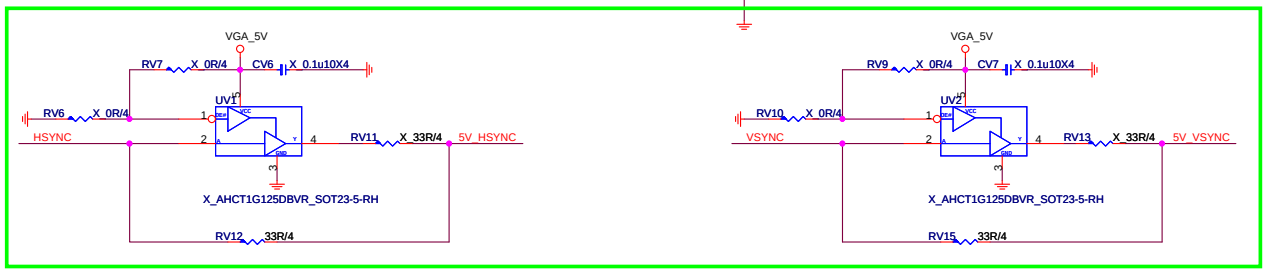
Note:

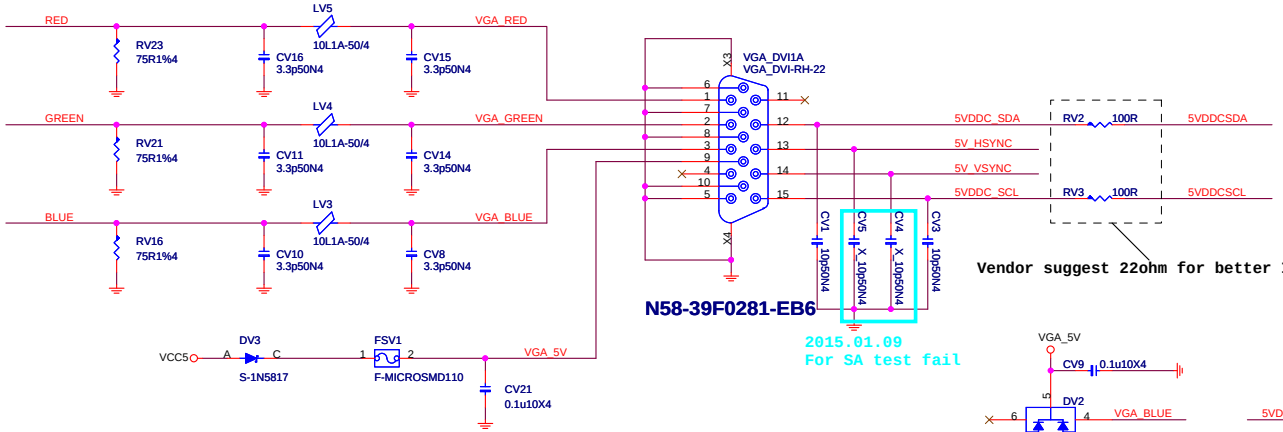
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



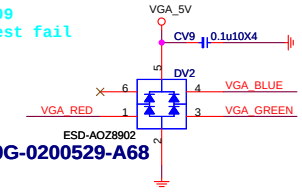
Remove

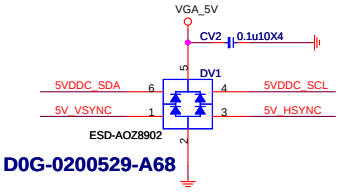


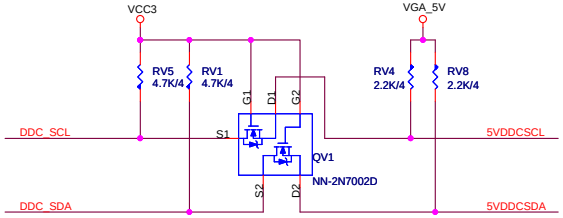




2015.01.09
For SA test fail







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	MS-7973	
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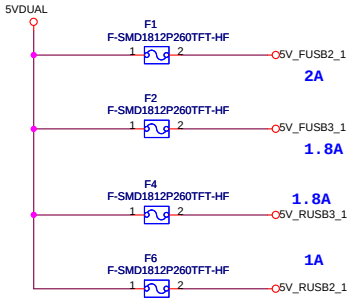
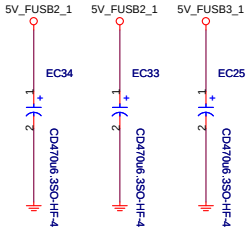
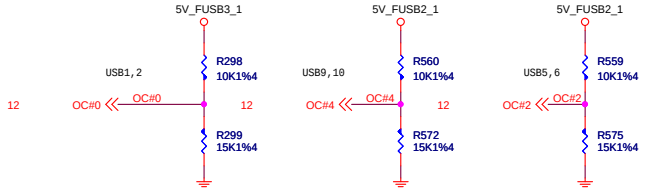
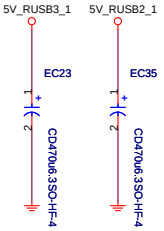
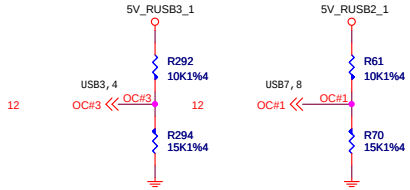
D08-0300700-P16 (Itrip=2.6A; 0.015ohm)



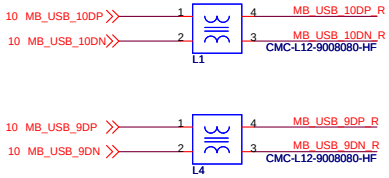


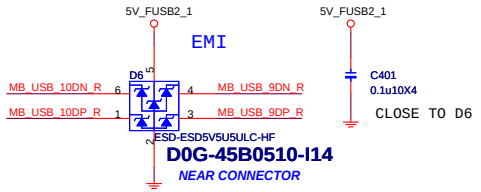






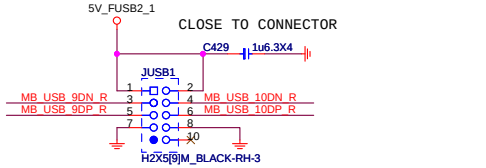
FRONT USB PORT 9,10





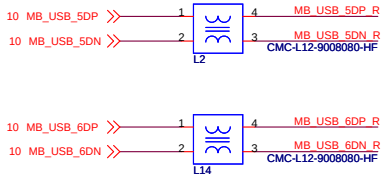
D0G-45B0510-I14

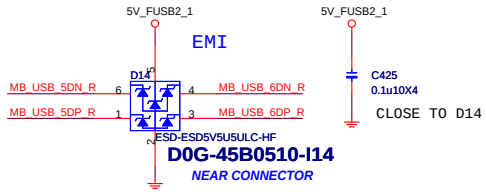
NEAR CONNECTOR



N31-2051BG1-H06

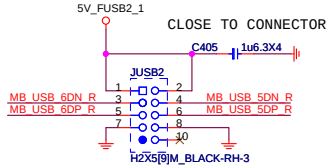
FRONT USB PORT 5,6





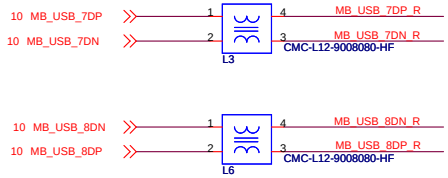
D0G-45B0510-I14

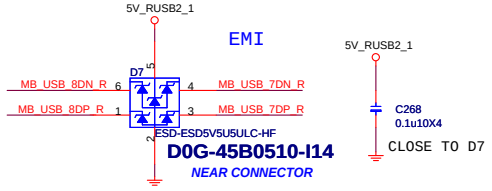
NEAR CONNECTOR



N31-2051BG1-H06

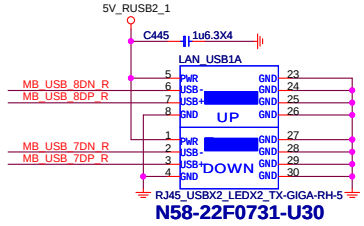
REAR USB PORT 7,8 (With LAN)





D0G-45B0510-I14

NEAR CONNECTOR



N58-22F0731-U30

MICRO-STAR INT'L CO.,LTD

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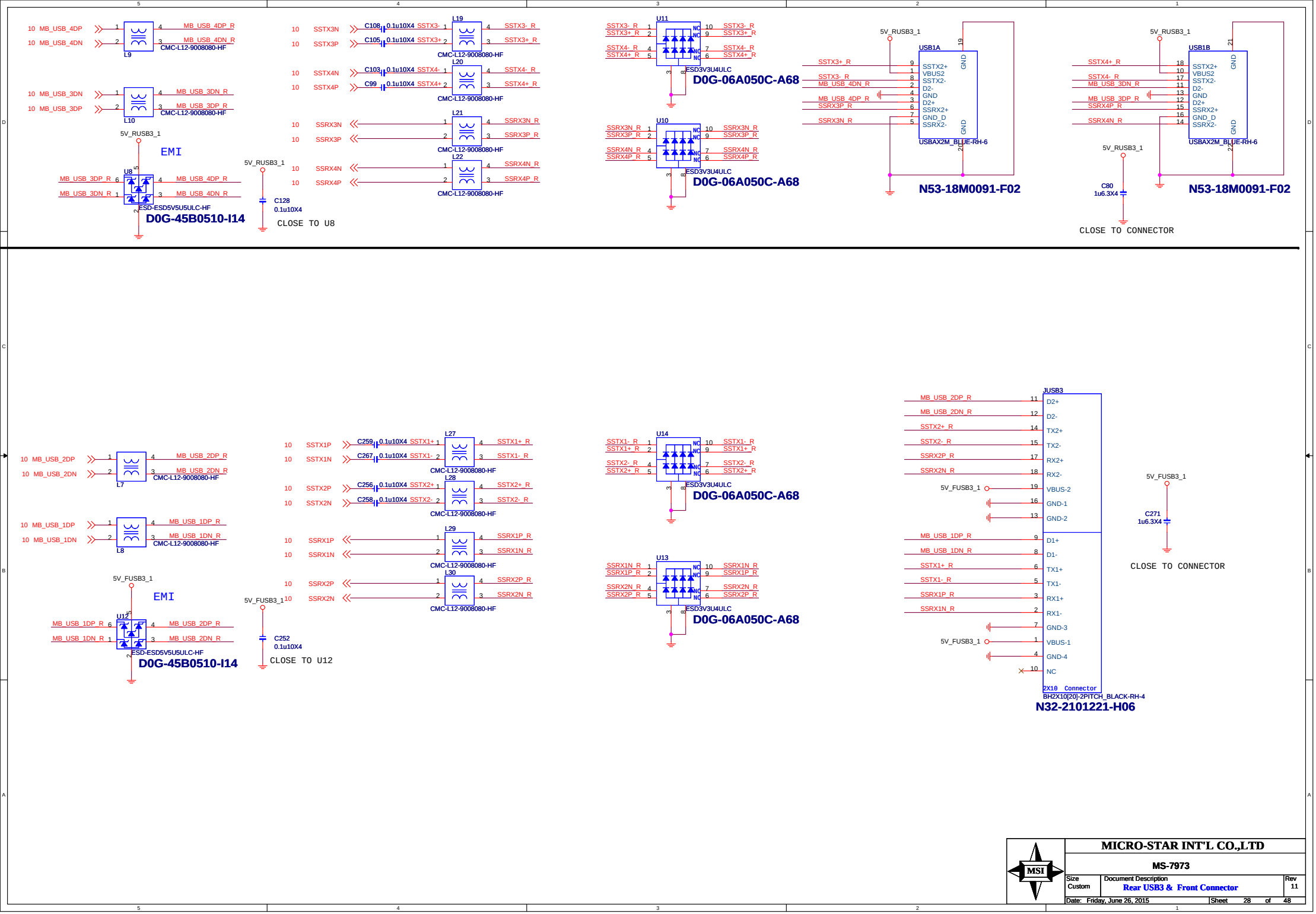
10 MB_USB_4DP
10 MB_USB_4DN
L9
MB_USB_4DP_R
MB_USB_4DN_R
CMC-L12-9008080-HF
10 MB_USB_3DN
10 MB_USB_3DP
L10
MB_USB_3DN_R
MB_USB_3DP_R
5V_RUSB3_1
EMI
U8
MB_USB_3DP_R
MB_USB_3DN_R
MB_USB_4DP_R
MB_USB_4DN_R
ESD-ESD5V5U5ULC-HF
D0G-45B0510-I14
C128
0.1u10X4
CLOSE TO U8
10 SSTX3N
10 SSTX3P
C108 0.1u10X4 SSTX3-
C105 0.1u10X4 SSTX3+
L19
SSTX3-_R
SSTX3+_R
10 SSTX4N
10 SSTX4P
C103 0.1u10X4 SSTX4-
C99 0.1u10X4 SSTX4+
L20
SSTX4-_R
SSTX4+_R
10 SSRX3N
10 SSRX3P
L21
SSRX3N_R
SSRX3P_R
10 SSRX4N
10 SSRX4P
L22
SSRX4N_R
SSRX4P_R
U11
SSTX3-_R
SSTX3+_R
SSTX4-_R
SSTX4+_R
ESD3V3U4ULC
D0G-06A050C-A68
U10
SSRX3N_R
SSRX3P_R
SSRX4N_R
SSRX4P_R
ESD3V3U4ULC
D0G-06A050C-A68
5V_RUSB3_1
USB1A
SSTX3+_R
SSTX3-_R
MB_USB_4DN_R
MB_USB_4DP_R
SSRX3P_R
SSRX3N_R
SSTX2+
VBUS2
SSTX2-
D2-
GND
D2+
SSRX2+
GND_D
SSRX2-
GND
USBAX2M_BLUE-RH-6
N53-18M0091-F02
5V_RUSB3_1
USB1B
SSTX4+_R
SSTX4-_R
MB_USB_3DN_R
MB_USB_3DP_R
SSRX4P_R
SSRX4N_R
USBAX2M_BLUE-RH-6
N53-18M0091-F02
5V_RUSB3_1
C80
1u6.3X4
CLOSE TO CONNECTOR
10 MB_USB_2DP
10 MB_USB_2DN
L7
MB_USB_2DP_R
MB_USB_2DN_R
CMC-L12-9008080-HF
10 MB_USB_1DP
10 MB_USB_1DN
L8
MB_USB_1DP_R
MB_USB_1DN_R
5V_FUSB3_1
EMI
U12
MB_USB_1DP_R
MB_USB_1DN_R
MB_USB_2DP_R
MB_USB_2DN_R
ESD-ESD5V5U5ULC-HF
D0G-45B0510-I14
C252
0.1u10X4
CLOSE TO U12
10 SSTX1P
10 SSTX1N
C259 0.1u10X4 SSTX1+
C267 0.1u10X4 SSTX1-
L27
SSTX1+_R
SSTX1-_R
10 SSTX2P
10 SSTX2N
C256 0.1u10X4 SSTX2+
C258 0.1u10X4 SSTX2-
L28
SSTX2+_R
SSTX2-_R
10 SSRX1P
10 SSRX1N
L29
SSRX1P_R
SSRX1N_R
10 SSRX2P
10 SSRX2N
L30
SSRX2P_R
SSRX2N_R
U14
SSTX1-_R
SSTX1+_R
SSTX2-_R
SSTX2+_R
ESD3V3U4ULC
D0G-06A050C-A68
U13
SSRX1N_R
SSRX1P_R
SSRX2N_R
SSRX2P_R
ESD3V3U4ULC
D0G-06A050C-A68
JUSB3
MB_USB_2DP_R
MB_USB_2DN_R
SSTX2+_R
SSTX2-_R
SSRX2P_R
SSRX2N_R
5V_FUSB3_1
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS-2
GND-1
GND-2
MB_USB_1DP_R
MB_USB_1DN_R
SSTX1+_R
SSTX1-_R
SSRX1P_R
SSRX1N_R
5V_FUSB3_1
D1+
D1-
TX1+
TX1-
RX1+
RX1-
GND-3
VBUS-1
GND-4
NC
2X10 Connector
BH2X10[20]-2PITCH_BLACK-RH-4
N32-2101221-H06
5V_FUSB3_1
C271
1u6.3X4
CLOSE TO CONNECTOR
MICRO-STAR INT'L CO.,LTD
MS-7973
Size
Custom
Document Description
Rear USB3 & Front Connector
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11
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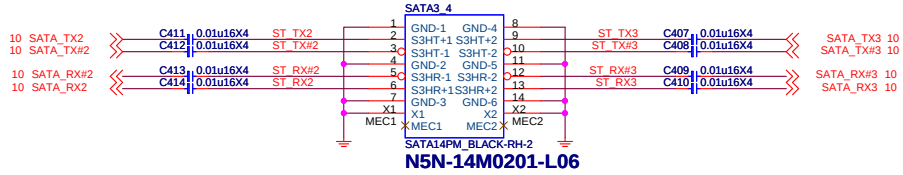
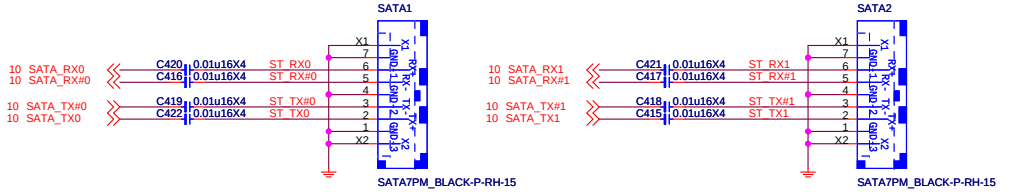


N5N-14M0201-L06



N5N-07M2441-L06

N5N-07M2441-L06

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7973	
Size: Custom	Document Description: SATA connector	Rev: 11
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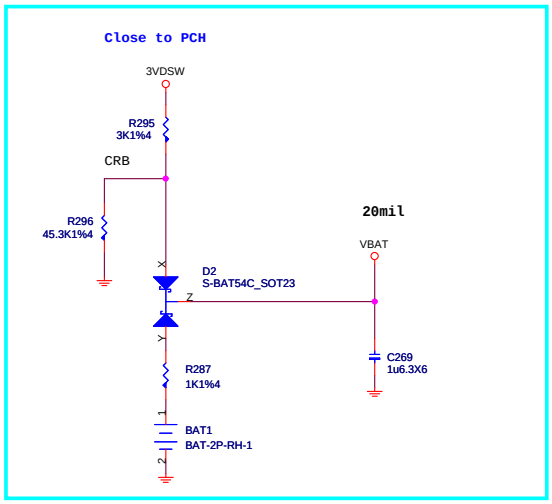
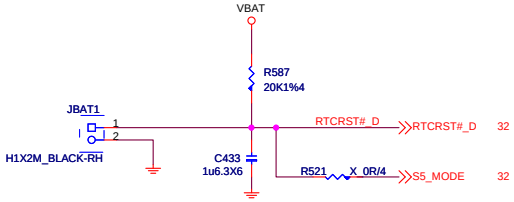
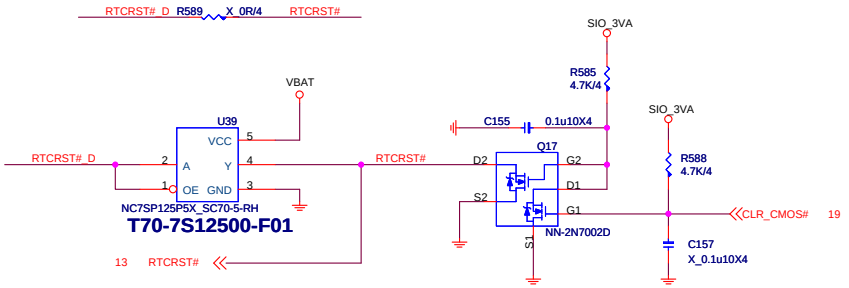
G3 Status

CUT_VBAT







tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

	R589	U39	R587	C433
USE U39 Auto CLR_CMOS	X	0	0	0
NOT USE U39 Auto CLR_CMOS	0	X	X	X

MICRO-STAR INT'L CO.,LTD

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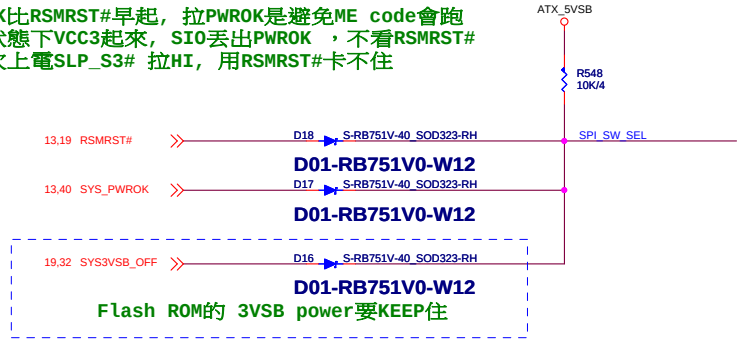
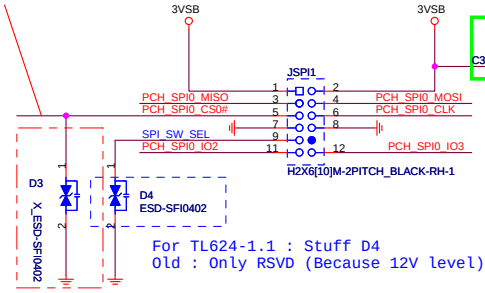
13 PCH_SPI0_MOSI — PCH_SPI0_MOSI
13 PCH_SPI0_MISO — PCH_SPI0_MISO
13 PCH_SPI0_CLK — PCH_SPI0_CLK
13 PCH_SPI0_CS0# — PCH_SPI0_CS0#
13 PCH_SPI0_IO2 — PCH_SPI0_IO2
13 PCH_SPI0_IO3 — PCH_SPI0_IO3

1.DPWROK比RSMRST#早起，拉PWROK是避免ME code會跑
2.開機狀態下VCC3起來，SIO丟出PWROK ，不看RSMRST#
3.第一次上電SLP_S3# 拉HI，用RSMRST#卡不住



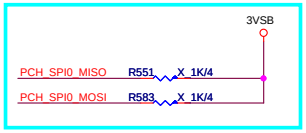
SPI CS# < 25pF
D0G-0402510-SI0



2014.08.25
Close to JSPI1
C399 0.1u10X4

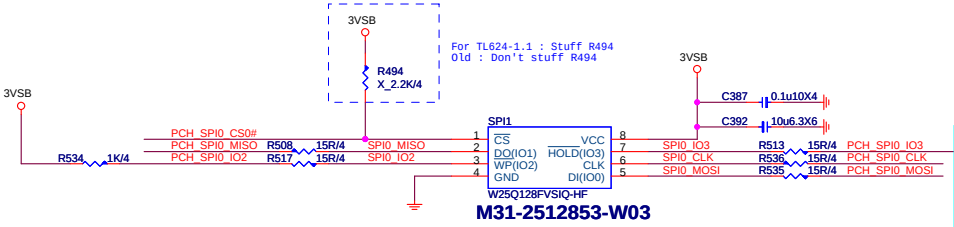
For TL624-1.1 : Stuff D4
Old : Only RSVD (Because 12V level)

2014.12.15



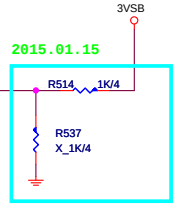
For TL624-1.1 : Stuff R493
Old : Don't stuff R493

For TL624-1.1 : Stuff R494
Old : Don't stuff R494



M31-2512853-W03

2015.01.15



2014.09.24 For intel MOW36 update

pull down resistor on SPI0_IO3 is needed for SKL S/H platforms with pre-ES1/ES1 samples.

20150115
update this issue for PRE-ES2/ES2 refer mail 20150115 From synge

* if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002
* if you support Standby power in S5 Status(Ex; PCH is B75 Chipset) , component Q14.G Pull-high to ATX_5VSB , Q14 must select "Vth" under 1V (Component Suggestion as below)

D03-0341409-A68 / D03-0230019-A30

MICRO-STAR INT'L CO.,LTD	
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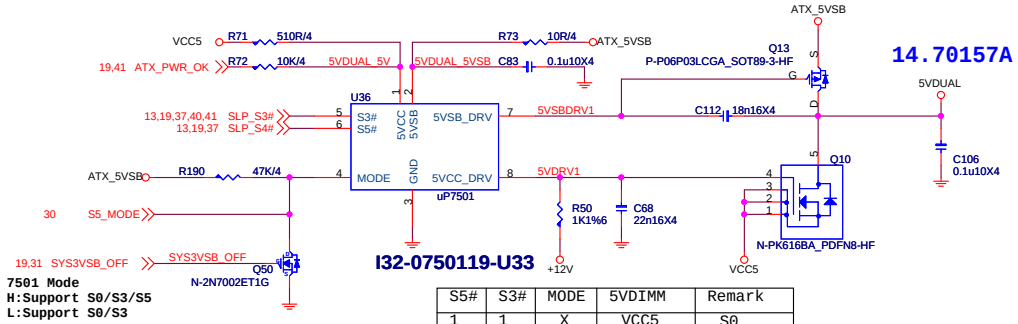
5VDUAL

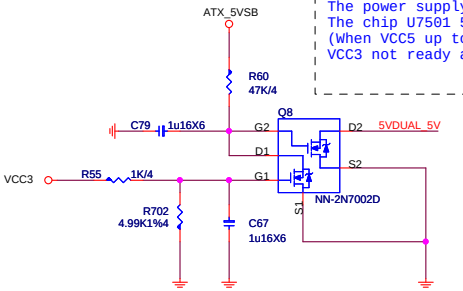


7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

S5#	S3#	MODE	5VDIMM	Remark
1	1	X	VCC5	S0
1	0	X	5VSB	S3
0	X	1	5VSB	S4/S5
0	X	0	Shutdown	S4/S5

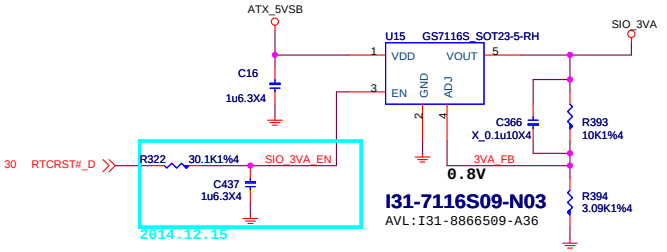
SYS3VSB_OFF (DSW POWER CONTROL)
default is set to 1 to cut off the standby power
DSW S5 (HIGH): USB no power
S5 (LOW): USB have power

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



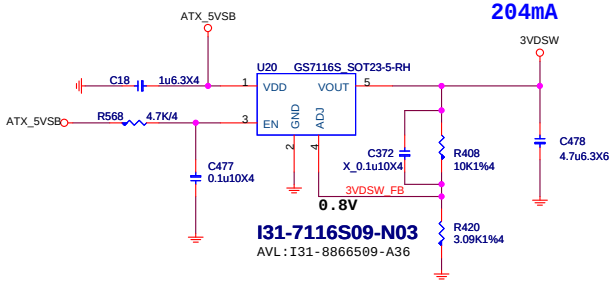
SIO_3VA

20mA



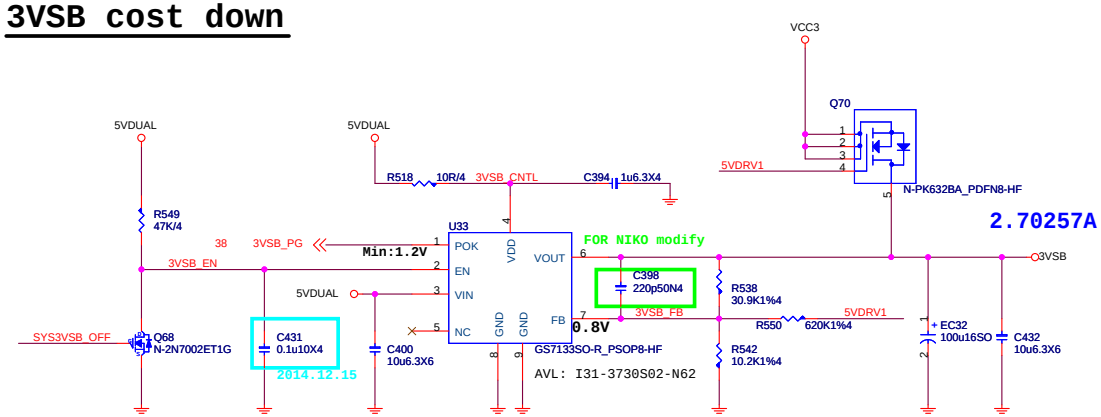
3VDSW

204mA



Vout=[1+(R1/R2)]*Vref
=[1+(10K/3.09K)]*0.8
=3.388997V

3VSB cost down



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ACPI CONTROLLER	11

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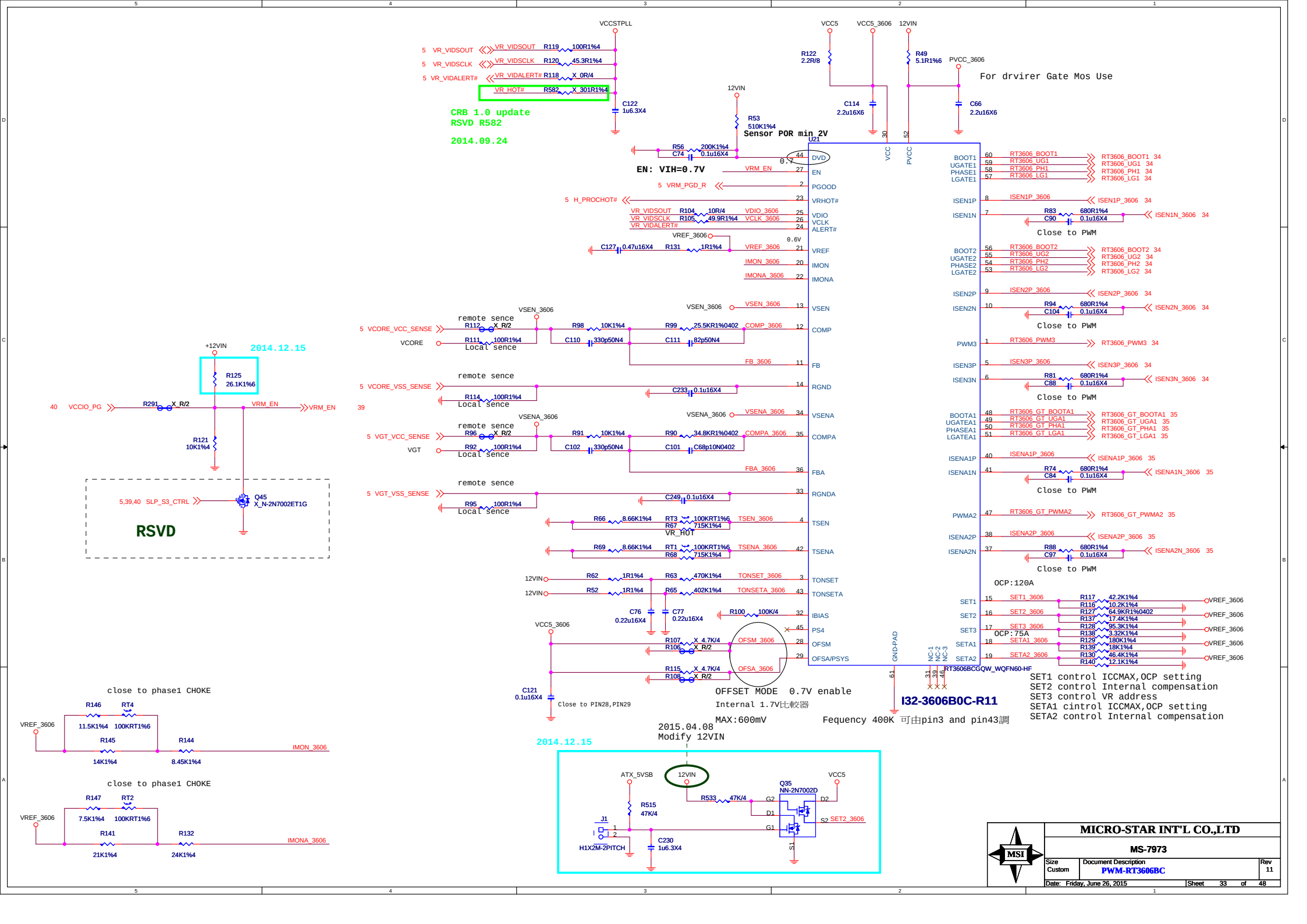

MICRO-STAR INT'L CO.,LTD	
MS-7973	
Size: Custom	Document Description: PWM-RT3606BC
Rev: 11	
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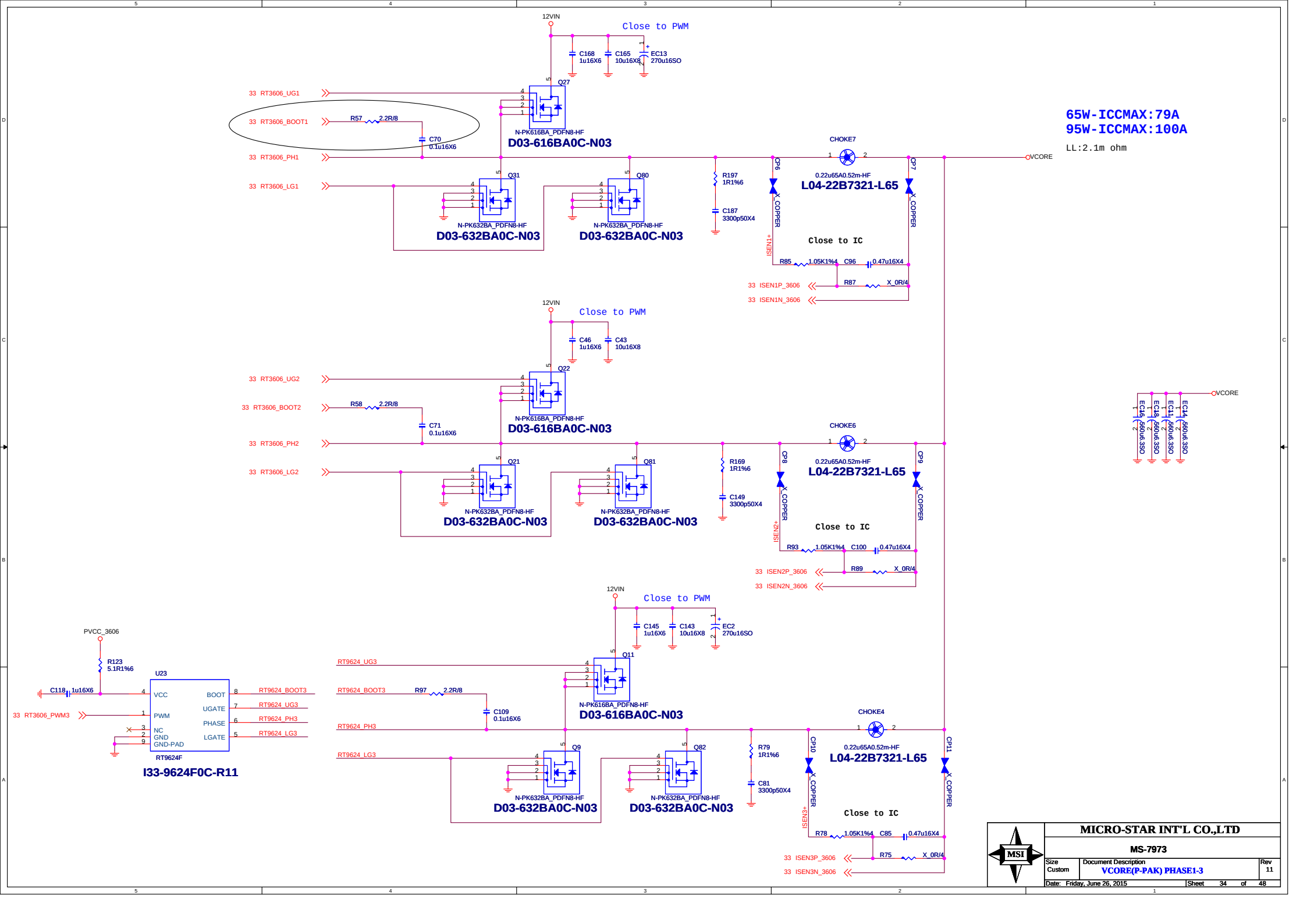
65W-ICCMAX:79A
95W-ICCMAX:100A
LL:2.1m ohm
12VIN
Close to PWM
C168 1u16X6
C165 10u16X8
EC13 270u16SO
Q27
33 RT3606_UG1
33 RT3606_BOOT1
R57 2.2R/8
C70 0.1u16X6
33 RT3606_PH1
33 RT3606_LG1
N-PK616BA_PDFN8-HF
D03-616BA0C-N03
Q31
Q80
N-PK632BA_PDFN8-HF
D03-632BA0C-N03
R197 1R1%6
C187 3300p50X4
CHOKE7
0.22u65A0.52m-HF
L04-22B7321-L65
CP6
CP7
X_COPPER
VCORE
ISEN1+
Close to IC
R85 1.05K1%4
C96 0.47u16X4
R87 X_0R/4
33 ISEN1P_3606
33 ISEN1N_3606
C46 1u16X6
C43 10u16X8
Q22
33 RT3606_UG2
33 RT3606_BOOT2
R58 2.2R/8
C71 0.1u16X6
33 RT3606_PH2
33 RT3606_LG2
Q21
Q81
R169 1R1%6
C149 3300p50X4
CHOKE6
CP8
CP9
ISEN2+
R93 1.05K1%4
C100 0.47u16X4
R89 X_0R/4
33 ISEN2P_3606
33 ISEN2N_3606
EC16 560u6.3SO
EC15 560u6.3SO
EC12 560u6.3SO
EC11 560u6.3SO
EC14 560u6.3SO
C145 1u16X6
C143 10u16X8
EC2 270u16SO
Q11
RT9624_UG3
RT9624_BOOT3
R97 2.2R/8
C109 0.1u16X6
RT9624_PH3
RT9624_LG3
Q9
Q82
R79 1R1%6
C81 3300p50X4
CHOKE4
CP10
CP11
ISEN3+
R78 1.05K1%4
C85 0.47u16X4
R75 X_0R/4
33 ISEN3P_3606
33 ISEN3N_3606
PVCC_3606
R123 5.1R1%6
C118 1u16X6
U23
VCC
PWM
NC
GND
GND-PAD
BOOT
UGATE
PHASE
LGATE
RT9624_BOOT3
RT9624_UG3
RT9624_PH3
RT9624_LG3
33 RT3606_PWM3
RT9624F
I33-9624F0C-R11
MICRO-STAR INT'L CO.,LTD
MS-7973
Size Custom
Document Description
VCORE(P-PAK) PHASE1-3
Rev 11
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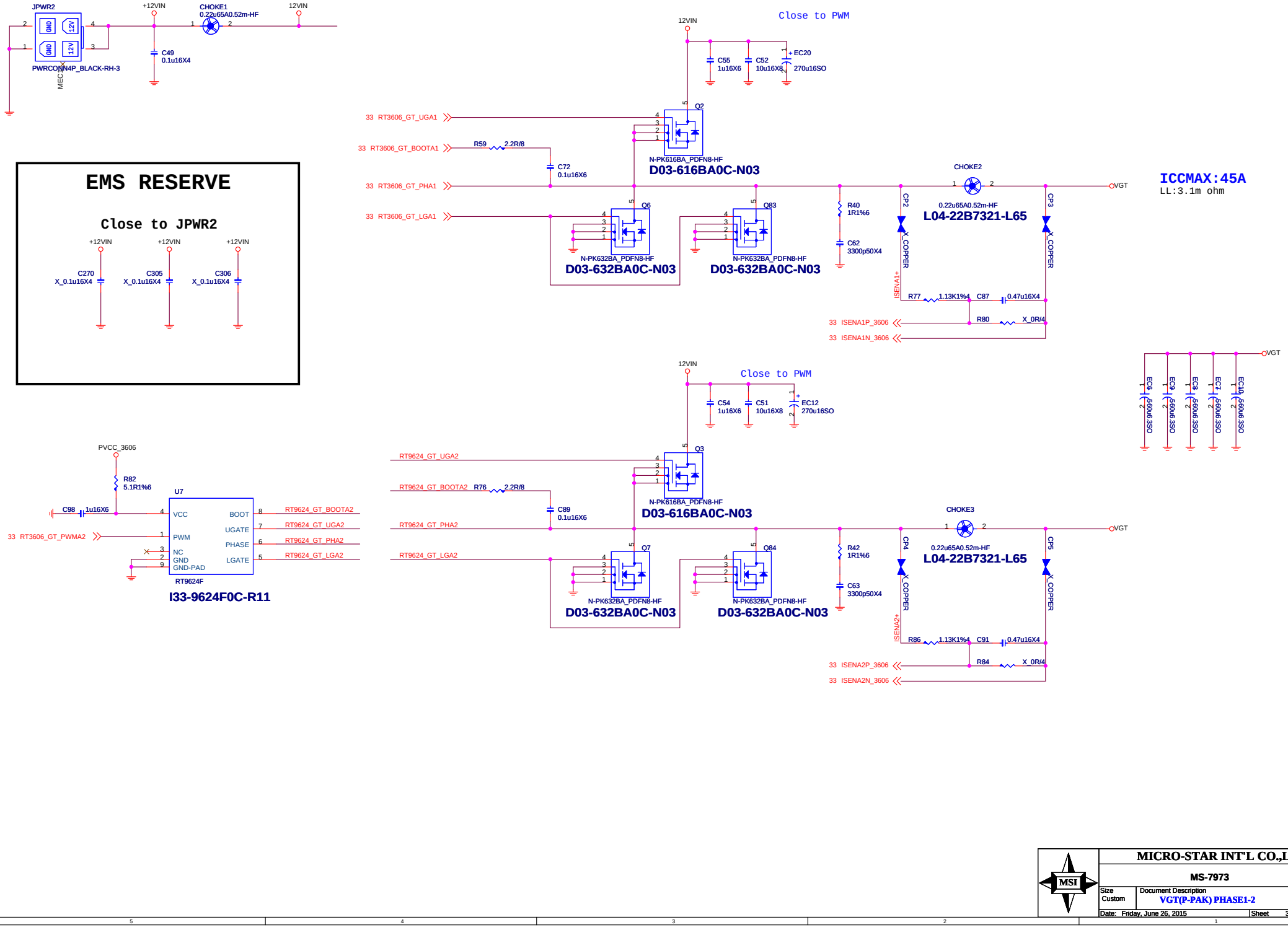

MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: VGT(P-PAK) PHASE1-2	Rev: 11
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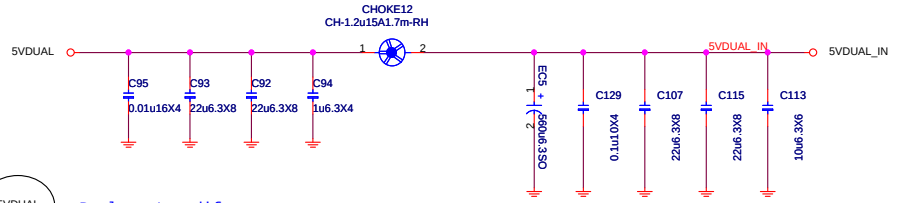
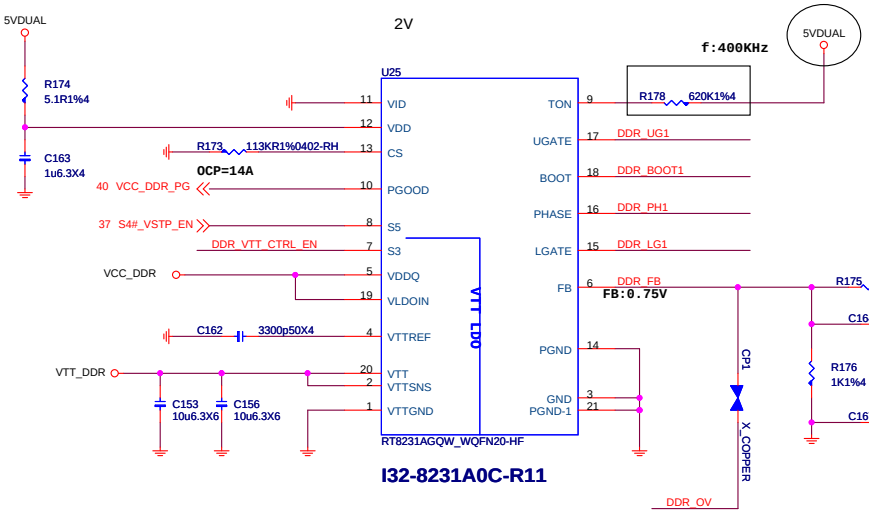
DDR Power:1.35V,9.357A

2.8A FOR CPU
6A FOR 2DIMM DDR3
0.557A FOR VTT_DDR

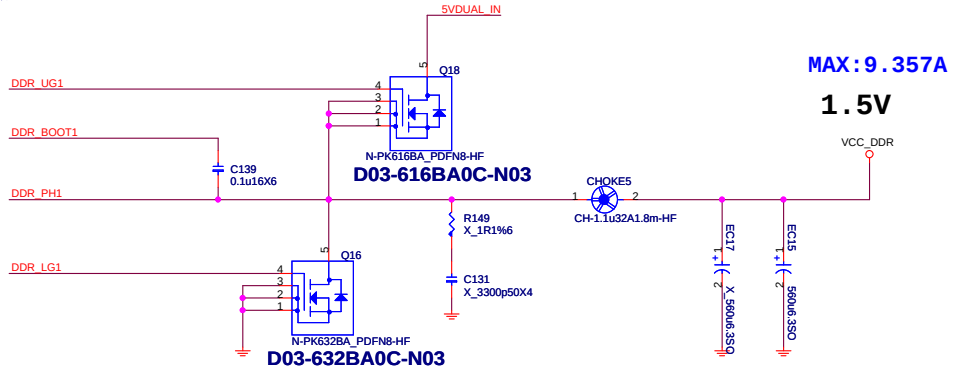
OCP =9.357A*1.5=14.0625A
Rlimit(R277)=OCP*Rdson(Low side)4.6mohm]/10uA
=14.0625*4.6mohm/10uA
=6.467Kohm

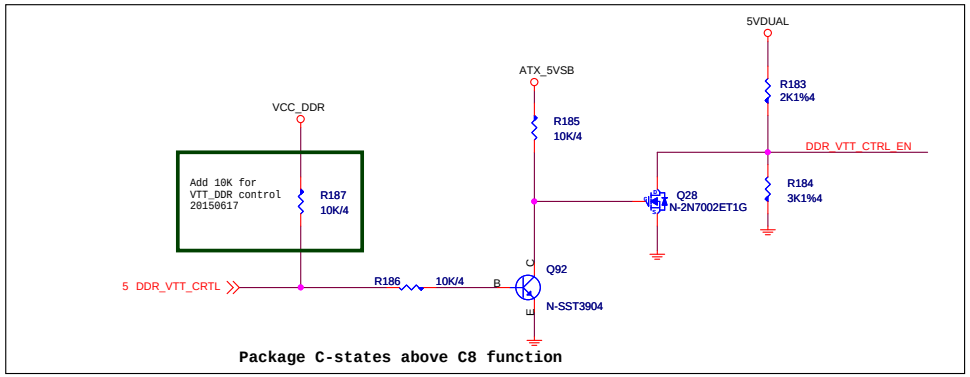
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 9.357 * 0.44
= 4.154A





I32-8231A0C-R11

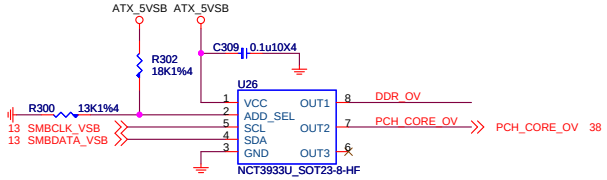




Package C-states above C8 function

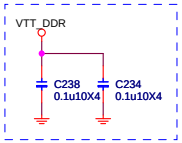
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



I34-3933U09-N62

0.1uFx1 per dimm



MICRO-STAR INT'L CO.,LTD		
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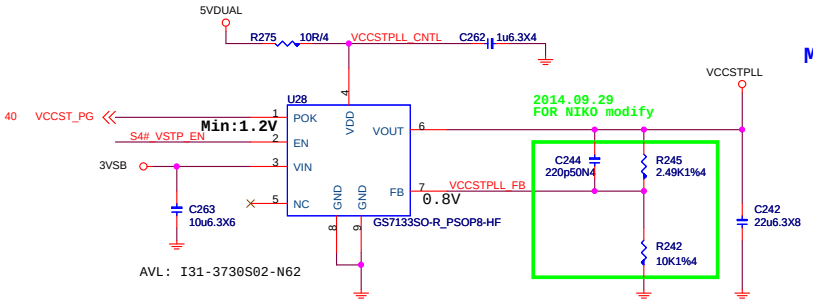
VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

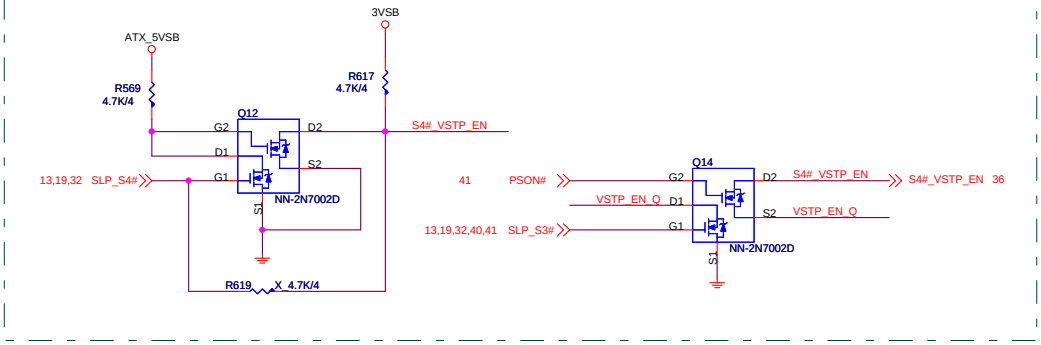


I31-7133S02-N03

VCCIO ramped and stable before
beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

20151623 Fix G3->S5 PWR auto enable



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Size: Custom	Document Description: CPU PWR_ST/PLL	Rev: 11
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PCH_1VSB

1.0V; 7.24A

OCP = 15.996A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 7.24 * 4.6mohm / 10uA
= 4.9956K

Rocs:7.87K,OCP:
D03-4C05N03-O05 : 15.74A
D03-632BA0C-N03 : 17.1A
use UBIQ MOS need Check

Rdson(low)4.5V
D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

2014.08.22 close to U34

PCH_1VSB_EN
R438 36K1%4
C379 33p50N4
C373 3300p50X4
For up1540

2015.01.22
for up1540:stuff R438->36K,
C379->NC,C373->3.3nF
for RT8125:R438.C379.C373->NC

2015.01.22
for up1540:R96->2.2R,C84->1uF
for RT8125:R96->10R,C84->1uF

5VDUAL
R403 2.2R/8
C362 1u6.3X6
R180 X_10K/4
POR:4.2V
EN:2.4V
32 3VSB_PG
R293 X_R/2
PCH_1VSB_EN

U34
UP1540QDDA_WDFN10-HF
I32-1540Q0C-U33
COMP/EN
POK
NC
OCS
VCC
GND
BOOT
PH
UG
LG
FB

PCH_BOOT
PCH_PHASE
PCH_UGATE
PCH_LGATE
C349 0.1u16X6

2014.12.25
for up1540:C364&R407 ->NC
C364 X_1000p16X4
R407 X_806R1%4
PCH_REFOUT
PCH_REFIN
R705 6.98KR1%0402-RH
R623 X_0R/4

2014.12.25
for up1540:R705 is OCP set min:5Kohm
stuff 7.87K OCP SET:15.74A
RT8125C stuff C1000P C11-1022032-W08

2014.12.25
for up1540:R623 ->NC

36 PCH_CORE_OV
PCH_CORE_OV
to sink/source over voltage IC.
pin10 sink/source current capability can't over 1mA
So max voltage can't over 1.8V.
from NCT3933

36 PCH_CORE_OV
2014.12.25
for up1540:stuff R622->0R
R622 0R/4

PCH_CORE_FB_R
C376 X_0.01u16X4
PCH_TYPE3
R437 X_0R/4
R441 1K1%4
R439 3.92K1%4

R374 X_6.8K1%4
2014.12.25
for up1540:R374->NC

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

5VDUAL_PCH_IN
CHOKE11 CH-1.2u15A1.7m-RH
5VDUAL
C333 0.1u16X4
C314 10u16X8
EC26 560u6.3SO
C307 X_0.1u10X4

R375 10K/4
Q57
N-PK616BA_PDFN8-HF
D03-616BA0C-N03
Q56
N-PK632BA_PDFN8-HF
D03-632BA0C-N03
R330 X_2.2R/8
C328 X_3300p50X4

確認 電流
CHOKE10 CH-1.2u15A1.7m-RH
PCH_1VSB
EC31 560u6.3SO
EC30 560u6.3SO
C369 22u6.3X8
C371 10u6.3X6
C388 10u6.3X6
C360 1u6.3X4

MAX:7.24A

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

CP14
PCH_1VSB
PLACE UNDER THE PCH

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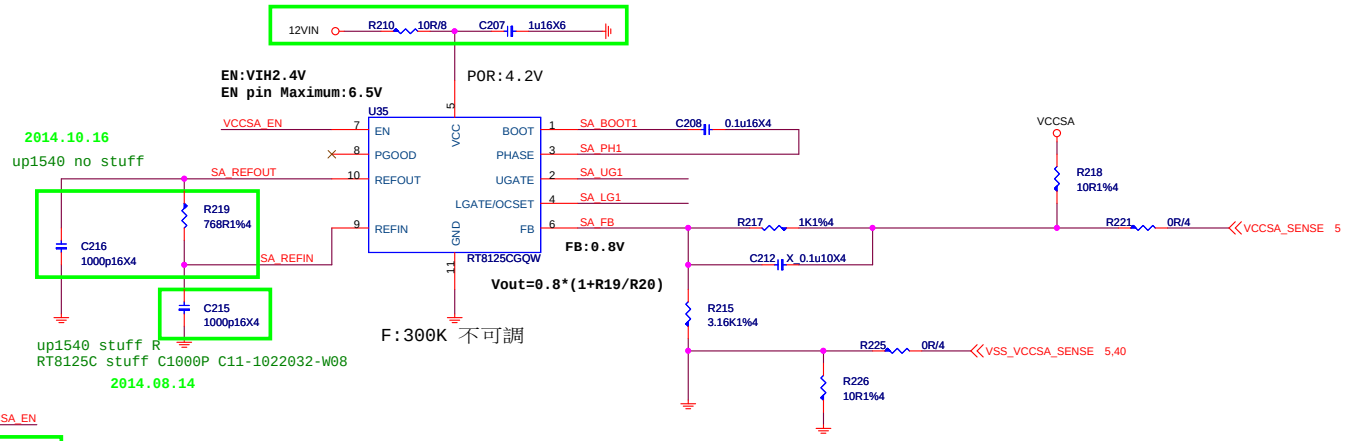
SA Power:1.05V,11.1A

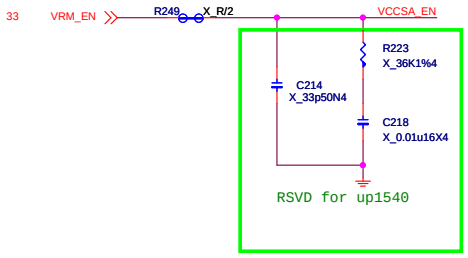
2015.01.22
for up1540:R96->2.2R,C84->1uF
for RT8125:R96->10R,C84->1uF

*OCP =11.1A*1.4=15.54A*
*Rocs(R15)=OCP*Rdson(Low side)3.3mohm]/10uA*
=15.54(3.3)mohm/10uA*
=5.2836Kohm

Rocs:5.2836K,OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

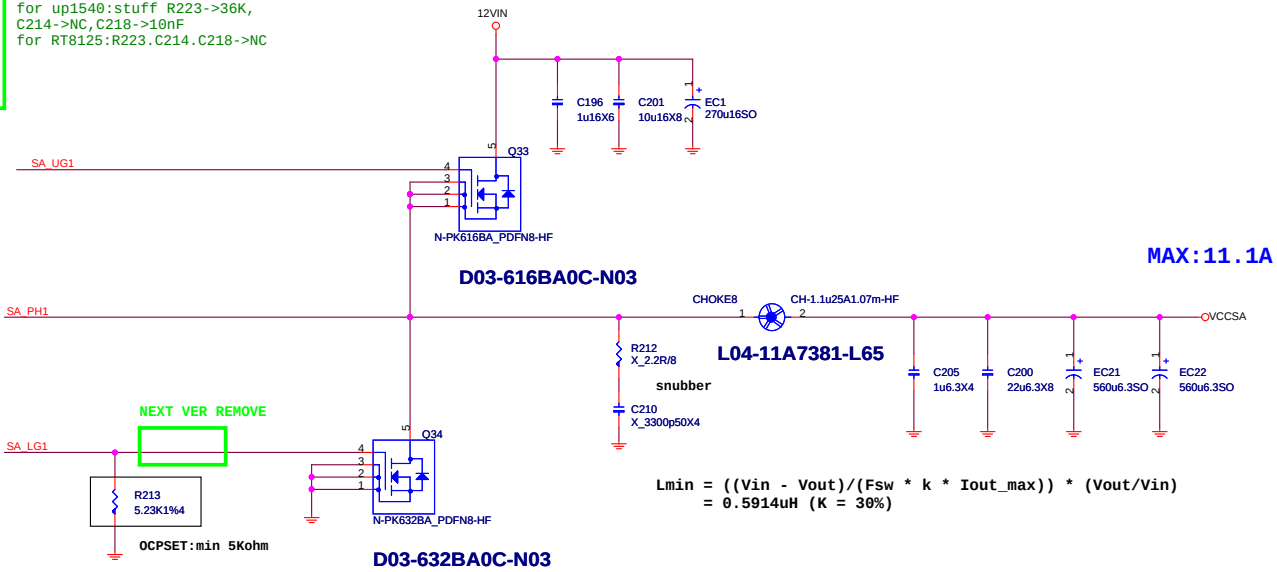




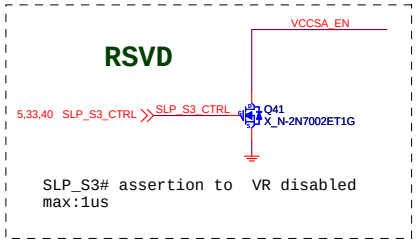
close to U35

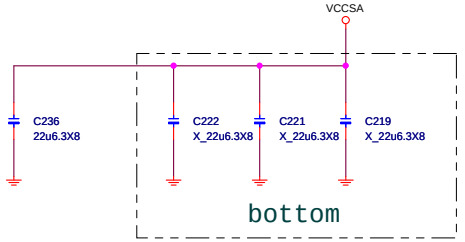
2015.01.22
for up1540:stuff R223->36K,
C214->NC,C218->10nF
for RT8125:R223.C214.C218->NC

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1* 0.2825
= 3.13575A



Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)





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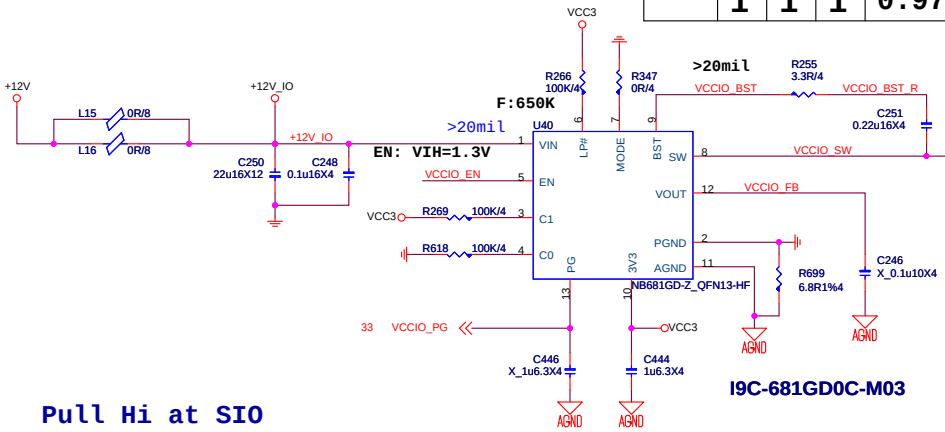
VCCIO

0.95V; 5.5A

IMAX 6A
ILIMIT=8.5~9A

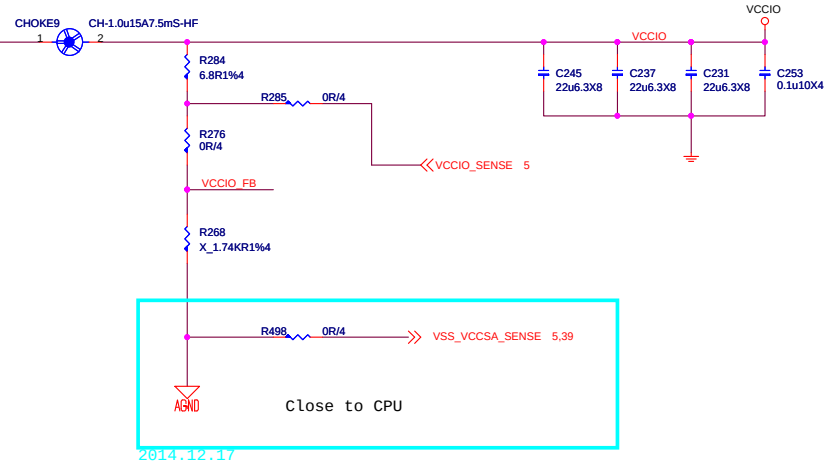
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975



I9C-681GD0C-M03

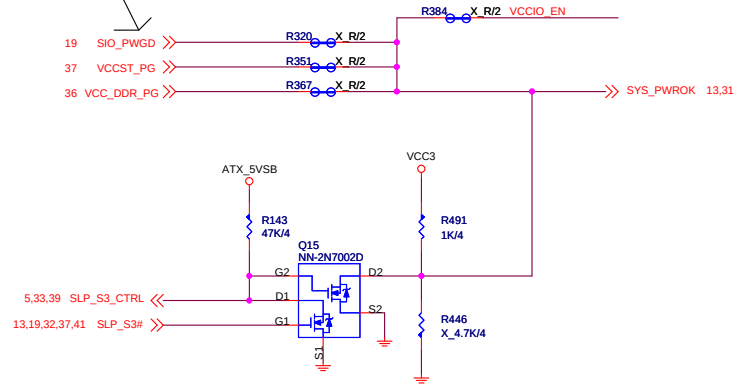
AVL:L04-0107800-M26 ; 6.86x6.47x3.0mm,22A,10mOhm
EM-10AM05V01---1UH/6*6

MAX:5.5A



2014.12.17

Pull Hi at SIO



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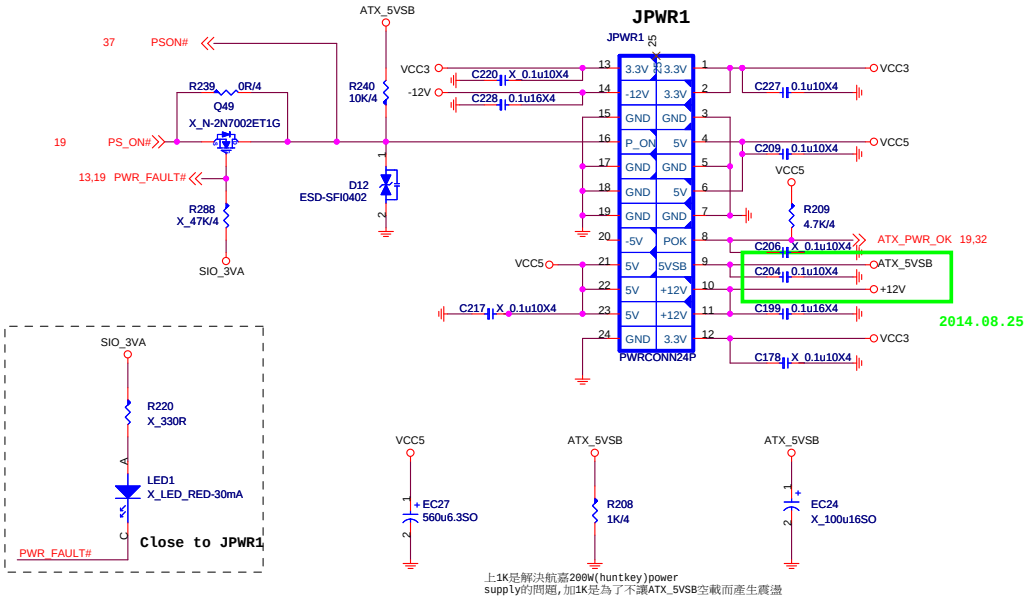
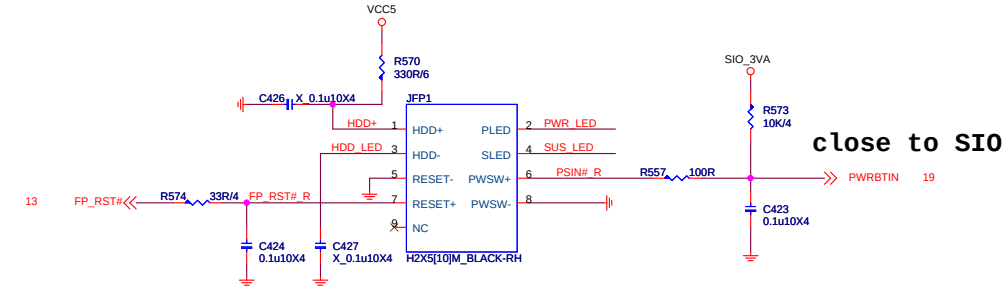
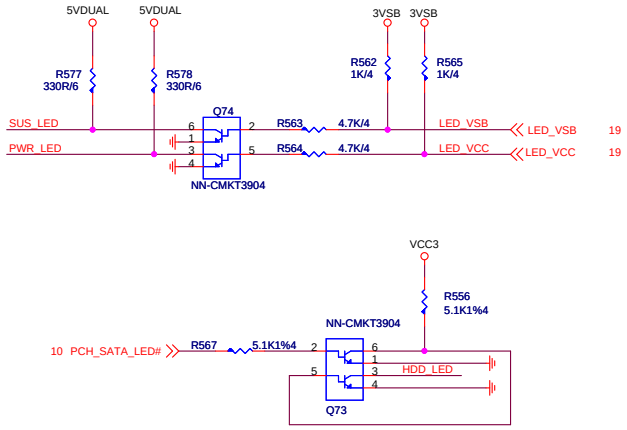
ATX POWER CONNECTOR



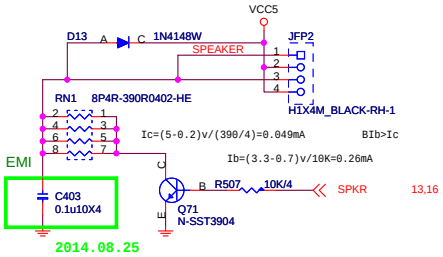
FRONT PANNEL



LED (for NV6793D)

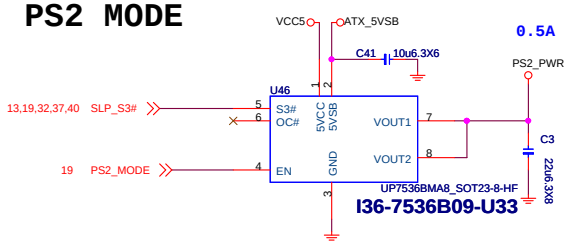


Speaker Pin Header

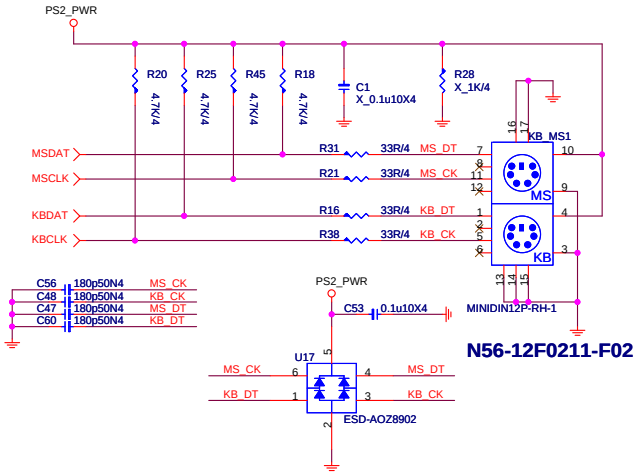


R=390 Ohm
I=(5-0.2)/R=0.0123 A
W=0.0123A x 5v=0.0615W(夠耐電阻)
R=1/16W=0.062W

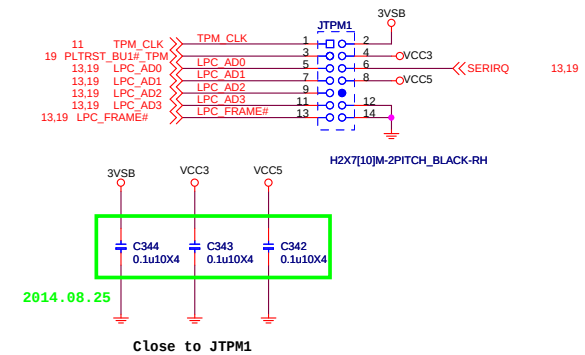
PS2 POWER



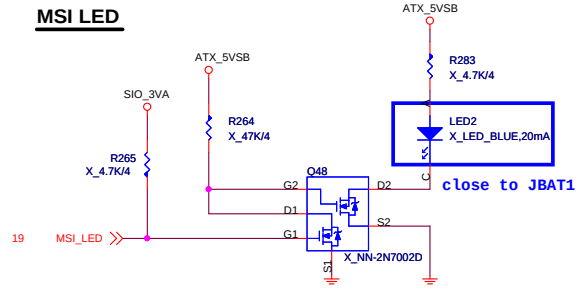
PS2 Connector



TPM



MSI LED



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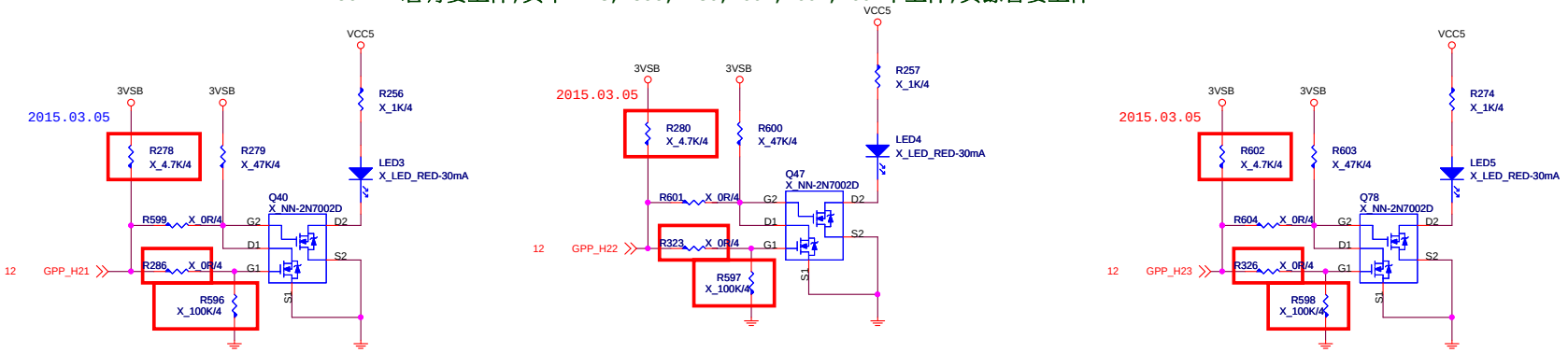
DEBUG LED

DEBUG LED若有要上件,其中R278,R599,R280,R601,R602,R604不上件,其餘皆要上件



GPIO / LED	GPP_H21	GPP_H21	GPP_H21
亮	GPI (default LOW)	GPI (default LOW)	GPI (default LOW)
滅	HIGH	HIGH	HIGH

關機斷電狀態下，3個LED先維持default全亮(Eup Enable 會全滅)，開機通電後，首先進行CPU check（請研究可否blink），check PASS後則CPU LED滅掉，接著依序進行Memory與VGA的check，LED的行為相同。因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

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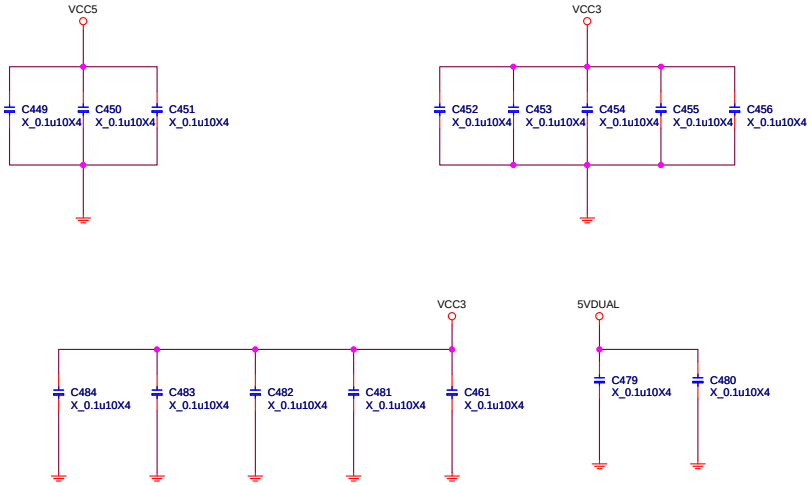
EMI CAP



MSI	MICRO-STAR INT'L CO.,LTD	
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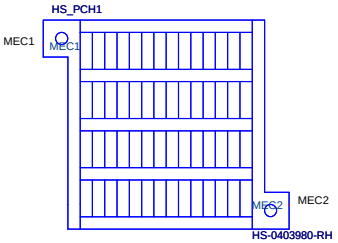
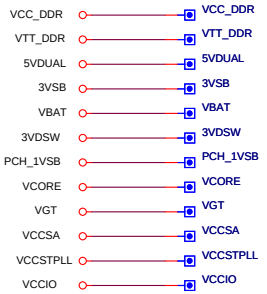
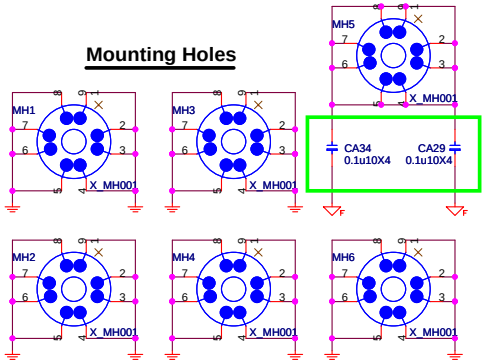


E31-0403980-K08



Mounting Holes

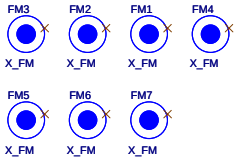


E21-7869020-F02

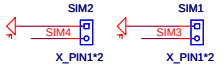
PK0-0797311-G37

PK0-0797310-G37,精成,23,寶安恩斯邁廠(MSIS)4,Coffee
PK0-0797310-E48,競華,23,寶安恩斯邁廠(MSIS)4,Coffee

Optical Fiducial Marks-120



Simulation



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