TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-Memory, CPU-PEG/Display	3,4
CPU-Control/MISC/CFG/Audio	5
CPU-Power,CPU-GND	6,7
DDRIII DIMM1&DDRIII DIMM1	8,9
PCH-USB/PCIE/DMI/SATA	10
PCH-Audio/Display/Clock	11
PCH-GPIO/USBOC#/SATASTRAP	12
PCH-LPC/SPI/SMBUS/MISC	13
PCH-Power,PCH-GND,PCH-Strap	14,15,16
PCIE SLOT-CPU(X16)	17
PCIE SLOT-PCH(X1)	18
SIO-NCT6793D/FAN CONTROLLOR	19,20
AUDIO - ALC892/887,AUDIO - depop circuit	21,22
LAN - RTL8111H	23
DVI/Display Port/VGA	24,25,26
USB2.0/USB3.0/SATA connector	27,28,29
CUT_VBAT circuit/BIOS ROM	30,31
ACPI CONTROLLER	32
PWM-RT3606BC/VCORE 3PHASE/VGT 2PHASE	33,34,35
DDR-RT8231AGQW	36
CPU PWR_ST/PLL	37
PCH Core power	38
VCCSA - POWER/VCCIO - POWER	39,40
ATX F_Panel/TPM/MSI_LED	41
DEBUG LED/EMI CAP/Manial Part	42,43,44
Power Map/Power Sequence/GPIO MAP	45,46,47
Revision History	48

MS-7973

ATX:243*180

Ver: 10

Intel -SkyLake-S plamform

CPU:

LGA1151
*CPU POWER PAK *3 Phase*
*GT POWER PAK *2 Phase*

Onboard Chip:

HD Audio Codec: ALC892
SIO: NCT6793D
Flash ROM: SPI 64 MB
DP to VGA: ITE6515

Main Memory:

*DDR3L * 2 (Dual Channel)*

ACPI:

5VDAUL:uP7501
5VDIMM:uP7501
3VSB:GS7166+PN MOS
3VDSW:GS7166

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X1) Slot * 3*

System Chipset:

PCH-H :H110

PWM:

VCORE - RT3606BC
DDR - RT8231AGQW
PCH(1.0V) - RT8125C
VCCSA - RT8125C
VCCIO - NB681(Converter)

LDO:

VCCSTPLL - GS7166

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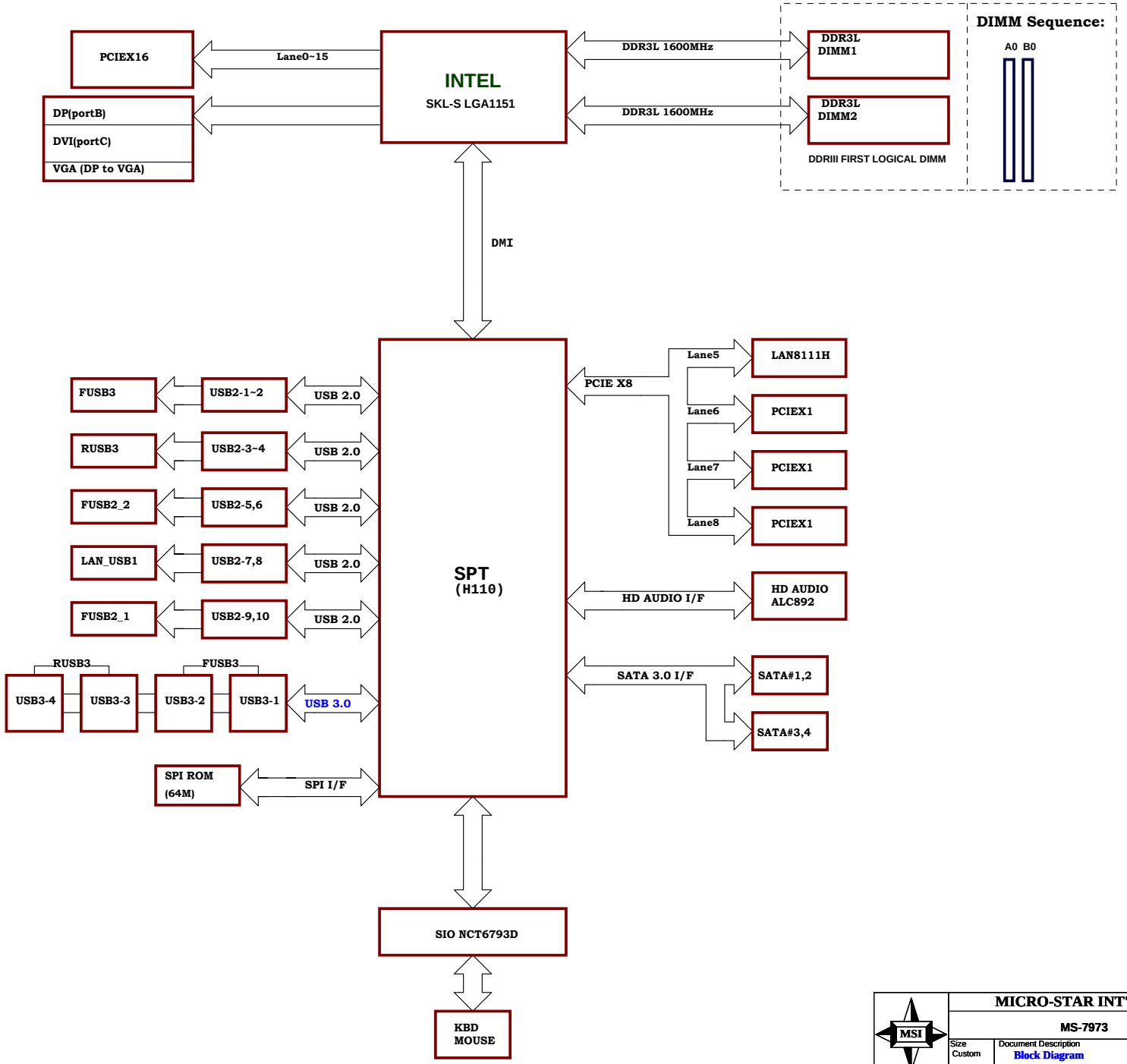
MS-7973

Size	Document Description	Rev
Custom	Cover Sheet	10

Date: Thursday, April 09, 2015 Sheet 1 of 48

MS-7981 Block Diagram



Slot Sequence:

PCIE X16	(By CPU)
PCIE X1	(By PCH)
PCIE X1	(By PCH)
PCIE X1	(By PCH)

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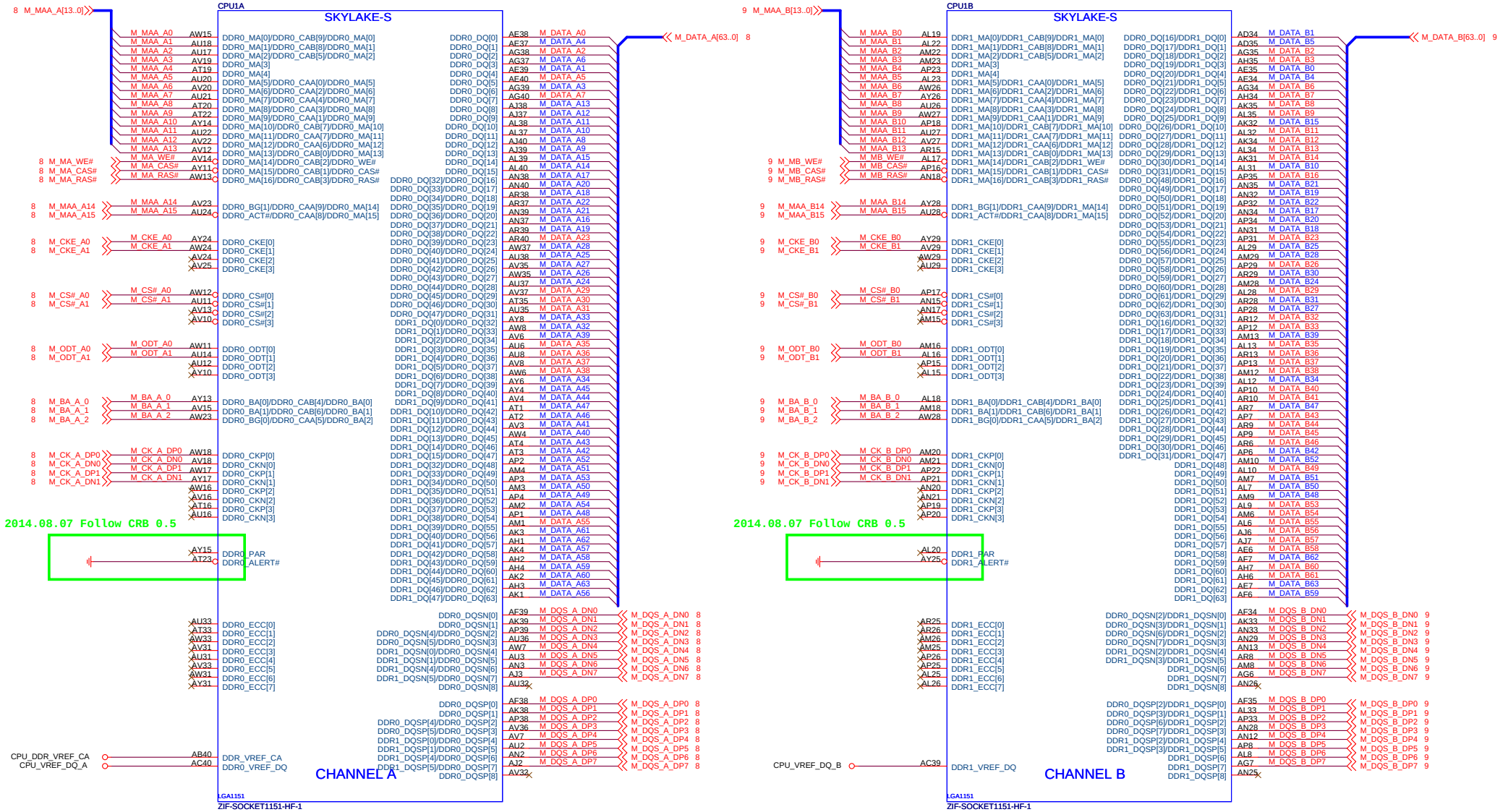
MS-7973

Size: Custom | Document Description: Block Diagram | Rev: 10

Date: Thursday, April 09, 2015 | Sheet 2 of 48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SKYLAKE-S
8 M_MAA_A[13..0]
M_MAA_A0 AW15
M_MAA_A1 AU18
M_MAA_A2 AU17
M_MAA_A3 AV19
M_MAA_A4 AT19
M_MAA_A5 AU20
M_MAA_A6 AV20
M_MAA_A7 AU21
M_MAA_A8 AT20
M_MAA_A9 AT22
M_MAA_A10 AY14
M_MAA_A11 AU22
M_MAA_A12 AV22
M_MAA_A13 AV12
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]
DDR0_MA[3]
DDR0_MA[4]
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]
DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]
8 M_MA_WE# M_MA_WE# AV14
8 M_MA_CAS# M_MA_CAS# AY11
8 M_MA_RAS# M_MA_RAS# AW13
DDR0_MA[14]/DDR0_CAB[2]/DDR0_WE#
DDR0_MA[15]/DDR0_CAB[1]/DDR0_CAS#
DDR0_MA[16]/DDR0_CAB[3]/DDR0_RAS#
8 M_MAA_A14 M_MAA_A14 AV23
8 M_MAA_A15 M_MAA_A15 AU24
DDR0_BG[1]/DDR0_CAA[9]/DDR0_MA[14]
DDR0_ACT#/DDR0_CAA[8]/DDR0_MA[15]
8 M_CKE_A0 M_CKE_A0 AY24
8 M_CKE_A1 M_CKE_A1 AW24
AV24
AV25
DDR0_CKE[0]
DDR0_CKE[1]
DDR0_CKE[2]
DDR0_CKE[3]
8 M_CS#_A0 M_CS#_A0 AW12
8 M_CS#_A1 M_CS#_A1 AU11
AV13
AV10
DDR0_CS#[0]
DDR0_CS#[1]
DDR0_CS#[2]
DDR0_CS#[3]
8 M_ODT_A0 M_ODT_A0 AW11
8 M_ODT_A1 M_ODT_A1 AU14
AU12
AY10
DDR0_ODT[0]
DDR0_ODT[1]
DDR0_ODT[2]
DDR0_ODT[3]
8 M_BA_A_0 M_BA_A_0 AY13
8 M_BA_A_1 M_BA_A_1 AV15
8 M_BA_A_2 M_BA_A_2 AW23
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]
DDR0_BG[0]/DDR0_CAA[5]/DDR0_BA[2]
8 M_CK_A_DP0 M_CK_A_DP0 AW18
8 M_CK_A_DN0 M_CK_A_DN0 AV18
8 M_CK_A_DP1 M_CK_A_DP1 AW17
8 M_CK_A_DN1 M_CK_A_DN1 AY17
AW16
AV16
AT16
AU16
DDR0_CKP[0]
DDR0_CKN[0]
DDR0_CKP[1]
DDR0_CKN[1]
DDR0_CKP[2]
DDR0_CKN[2]
DDR0_CKP[3]
DDR0_CKN[3]
2014.08.07 Follow CRB 0.5
AY15
AT23
DDR0_PAR
DDR0_ALERT#
AU33
AT33
AW33
AV31
AU31
AV33
AW31
AY31
DDR0_ECC[0]
DDR0_ECC[1]
DDR0_ECC[2]
DDR0_ECC[3]
DDR0_ECC[4]
DDR0_ECC[5]
DDR0_ECC[6]
DDR0_ECC[7]
CPU_DDR_VREF_CA AB40
CPU_VREF_DQ_A AC40
DDR_VREF_CA
DDR0_VREF_DQ
DDR0_DQ[0]
DDR0_DQ[1]
DDR0_DQ[2]
DDR0_DQ[3]
DDR0_DQ[4]
DDR0_DQ[5]
DDR0_DQ[6]
DDR0_DQ[7]
DDR0_DQ[8]
DDR0_DQ[9]
DDR0_DQ[10]
DDR0_DQ[11]
DDR0_DQ[12]
DDR0_DQ[13]
DDR0_DQ[14]
DDR0_DQ[15]
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DDR0_DQ[33]/DDR0_DQ[17]
DDR0_DQ[34]/DDR0_DQ[18]
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DDR0_DQ[36]/DDR0_DQ[20]
DDR0_DQ[37]/DDR0_DQ[21]
DDR0_DQ[38]/DDR0_DQ[22]
DDR0_DQ[39]/DDR0_DQ[23]
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DDR0_DQ[41]/DDR0_DQ[25]
DDR0_DQ[42]/DDR0_DQ[26]
DDR0_DQ[43]/DDR0_DQ[27]
DDR0_DQ[44]/DDR0_DQ[28]
DDR0_DQ[45]/DDR0_DQ[29]
DDR0_DQ[46]/DDR0_DQ[30]
DDR0_DQ[47]/DDR0_DQ[31]
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DDR1_DQ[1]/DDR0_DQ[33]
DDR1_DQ[2]/DDR0_DQ[34]
DDR1_DQ[3]/DDR0_DQ[35]
DDR1_DQ[4]/DDR0_DQ[36]
DDR1_DQ[5]/DDR0_DQ[37]
DDR1_DQ[6]/DDR0_DQ[38]
DDR1_DQ[7]/DDR0_DQ[39]
DDR1_DQ[8]/DDR0_DQ[40]
DDR1_DQ[9]/DDR0_DQ[41]
DDR1_DQ[10]/DDR0_DQ[42]
DDR1_DQ[11]/DDR0_DQ[43]
DDR1_DQ[12]/DDR0_DQ[44]
DDR1_DQ[13]/DDR0_DQ[45]
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DDR0_DQSN[2]
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DDR0_DQSP[7]
DDR0_DQSP[8]
AE38 M_DATA_A0
AE37 M_DATA_A4
AG38 M_DATA_A2
AG37 M_DATA_A6
AE39 M_DATA_A1
AE40 M_DATA_A5
AG39 M_DATA_A3
AG40 M_DATA_A7
AJ38 M_DATA_A13
AJ37 M_DATA_A12
AL38 M_DATA_A11
AL37 M_DATA_A10
AJ40 M_DATA_A8
AJ39 M_DATA_A9
AL39 M_DATA_A15
AL40 M_DATA_A14
AN38 M_DATA_A17
AN40 M_DATA_A20
AR38 M_DATA_A18
AR37 M_DATA_A22
AN39 M_DATA_A21
AN37 M_DATA_A16
AR39 M_DATA_A19
AR40 M_DATA_A23
AW37 M_DATA_A28
AU38 M_DATA_A25
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AW35 M_DATA_A26
AU37 M_DATA_A24
AV37 M_DATA_A29
AT35 M_DATA_A30
AU35 M_DATA_A31
AY8 M_DATA_A33
AW8 M_DATA_A32
AV6 M_DATA_A39
AU6 M_DATA_A35
AU8 M_DATA_A36
AV8 M_DATA_A37
AW6 M_DATA_A38
AY6 M_DATA_A34
AY4 M_DATA_A45
AV4 M_DATA_A44
AT1 M_DATA_A47
AT2 M_DATA_A46
AV3 M_DATA_A41
AW4 M_DATA_A40
AT4 M_DATA_A43
AT3 M_DATA_A42
AP2 M_DATA_A52
AM4 M_DATA_A51
AP3 M_DATA_A53
AM3 M_DATA_A50
AP4 M_DATA_A49
AM2 M_DATA_A54
AP1 M_DATA_A48
AM1 M_DATA_A55
AK3 M_DATA_A61
AH1 M_DATA_A62
AK4 M_DATA_A57
AH2 M_DATA_A58
AH4 M_DATA_A59
AK2 M_DATA_A60
AH3 M_DATA_A63
AK1 M_DATA_A56
AF39 M_DQS_A_DN0
AK39 M_DQS_A_DN1
AP39 M_DQS_A_DN2
AU36 M_DQS_A_DN3
AW7 M_DQS_A_DN4
AU3 M_DQS_A_DN5
AN3 M_DQS_A_DN6
AJ3 M_DQS_A_DN7
AU32
AF38 M_DQS_A_DP0
AK38 M_DQS_A_DP1
AP38 M_DQS_A_DP2
AV36 M_DQS_A_DP3
AV7 M_DQS_A_DP4
AU2 M_DQS_A_DP5
AN2 M_DQS_A_DP6
AJ2 M_DQS_A_DP7
AV32
M_DQS_A_DN0 8
M_DQS_A_DN1 8
M_DQS_A_DN2 8
M_DQS_A_DN3 8
M_DQS_A_DN4 8
M_DQS_A_DN5 8
M_DQS_A_DN6 8
M_DQS_A_DN7 8
M_DQS_A_DP0 8
M_DQS_A_DP1 8
M_DQS_A_DP2 8
M_DQS_A_DP3 8
M_DQS_A_DP4 8
M_DQS_A_DP5 8
M_DQS_A_DP6 8
M_DQS_A_DP7 8
M_DATA_A[63..0] 8
CHANNEL A
LGA1151
ZIF-SOCKET1151-HF-1
N12-151A020-F02
CPU1B
SKYLAKE-S
9 M_MAA_B[13..0]
M_MAA_B0 AL19
M_MAA_B1 AL22
M_MAA_B2 AM22
M_MAA_B3 AM23
M_MAA_B4 AP23
M_MAA_B5 AL23
M_MAA_B6 AW26
M_MAA_B7 AY26
M_MAA_B8 AU26
M_MAA_B9 AW27
M_MAA_B10 AP18
M_MAA_B11 AU27
M_MAA_B12 AV27
M_MAA_B13 AR15
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]
DDR1_MA[3]
DDR1_MA[4]
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
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DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
9 M_MB_WE# M_MB_WE# AL17
9 M_MB_CAS# M_MB_CAS# AP16
9 M_MB_RAS# M_MB_RAS# AN18
DDR1_MA[14]/DDR1_CAB[2]/DDR1_WE#
DDR1_MA[15]/DDR1_CAB[1]/DDR1_CAS#
DDR1_MA[16]/DDR1_CAB[3]/DDR1_RAS#
9 M_MAA_B14 M_MAA_B14 AY28
9 M_MAA_B15 M_MAA_B15 AU28
DDR1_BG[1]/DDR1_CAA[9]/DDR1_MA[14]
DDR1_ACT#/DDR1_CAA[8]/DDR1_MA[15]
9 M_CKE_B0 M_CKE_B0 AY29
9 M_CKE_B1 M_CKE_B1 AV29
AW29
AU29
DDR1_CKE[0]
DDR1_CKE[1]
DDR1_CKE[2]
DDR1_CKE[3]
9 M_CS#_B0 M_CS#_B0 AP17
9 M_CS#_B1 M_CS#_B1 AN15
AN17
AM15
DDR1_CS#[0]
DDR1_CS#[1]
DDR1_CS#[2]
DDR1_CS#[3]
9 M_ODT_B0 M_ODT_B0 AM16
9 M_ODT_B1 M_ODT_B1 AL16
AP15
AL15
DDR1_ODT[0]
DDR1_ODT[1]
DDR1_ODT[2]
DDR1_ODT[3]
9 M_BA_B_0 M_BA_B_0 AL18
9 M_BA_B_1 M_BA_B_1 AM18
9 M_BA_B_2 M_BA_B_2 AW28
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
DDR1_BG[0]/DDR1_CAA[5]/DDR1_BA[2]
9 M_CK_B_DP0 M_CK_B_DP0 AM20
9 M_CK_B_DN0 M_CK_B_DN0 AM21
9 M_CK_B_DP1 M_CK_B_DP1 AP22
9 M_CK_B_DN1 M_CK_B_DN1 AP21
AN20
AN21
AP19
AP20
DDR1_CKP[0]
DDR1_CKN[0]
DDR1_CKP[1]
DDR1_CKN[1]
DDR1_CKP[2]
DDR1_CKN[2]
DDR1_CKP[3]
DDR1_CKN[3]
2014.08.07 Follow CRB 0.5
AL20
AY25
DDR1_PAR
DDR1_ALERT#
AR25
AR26
AM26
AM25
AP26
AP25
AL25
AL26
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DDR1_ECC[6]
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DDR1_VREF_DQ
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DDR1_DQSN[6]
DDR1_DQSN[7]
DDR1_DQSN[8]
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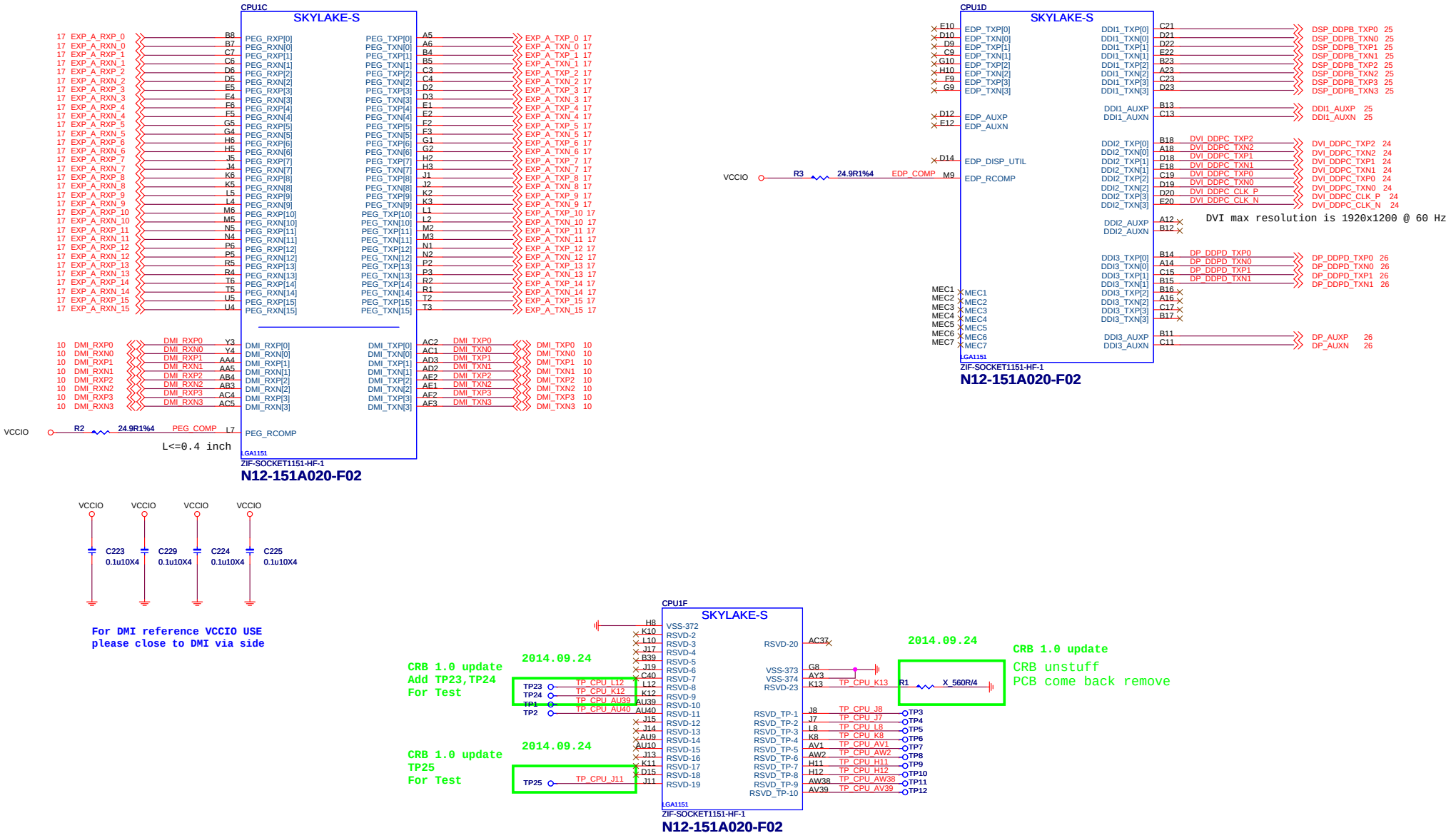
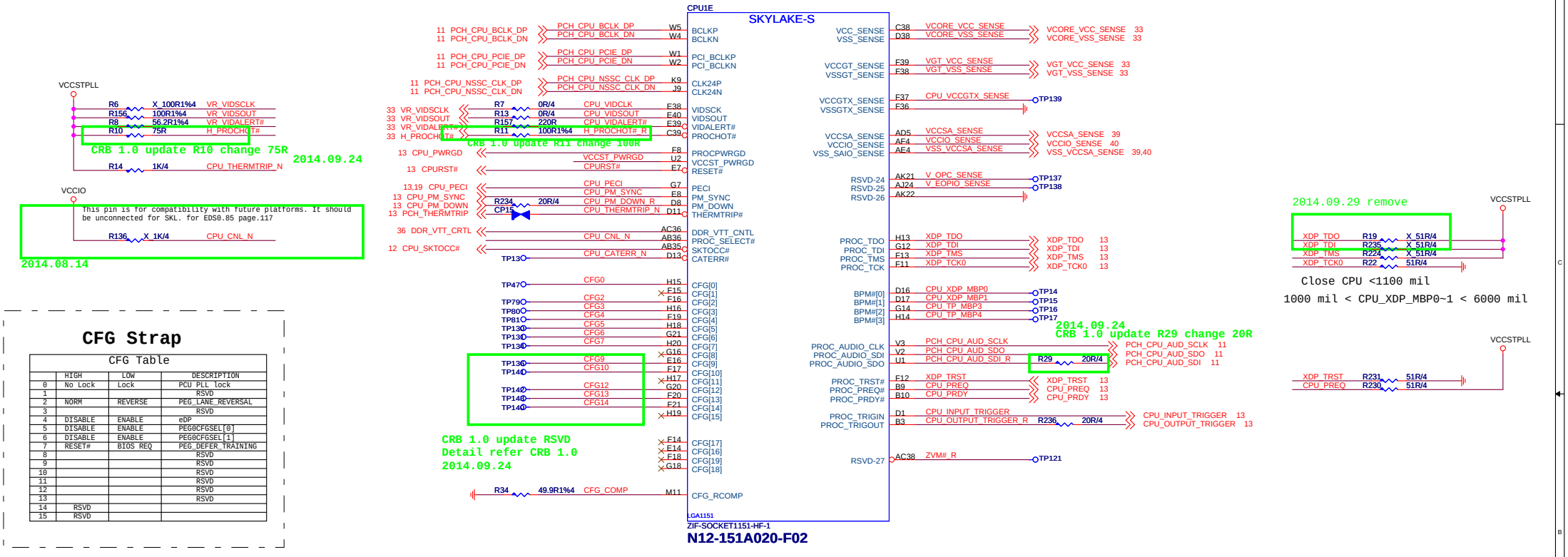
DDR0_DQSP[6]/DDR1_DQSP[2]
DDR0_DQSP[7]/DDR1_DQSP[3]
DDR1_DQSP[2]/DDR1_DQSP[4]
DDR1_DQSP[3]/DDR1_DQSP[5]
DDR1_DQSP[6]
DDR1_DQSP[7]
DDR1_DQSP[8]
AD34 M_DATA_B1
AD35 M_DATA_B5
AG35 M_DATA_B2
AH35 M_DATA_B3
AE35 M_DATA_B0
AE34 M_DATA_B4
AG34 M_DATA_B6
AH34 M_DATA_B7
AK35 M_DATA_B8
AL35 M_DATA_B9
AK32 M_DATA_B15
AL32 M_DATA_B11
AK34 M_DATA_B12
AL34 M_DATA_B13
AK31 M_DATA_B14
AL31 M_DATA_B10
AP35 M_DATA_B16
AN35 M_DATA_B21
AN32 M_DATA_B19
AP32 M_DATA_B22
AN34 M_DATA_B17
AP34 M_DATA_B20
AN31 M_DATA_B18
AP31 M_DATA_B23
AL29 M_DATA_B25
AM29 M_DATA_B28
AP29 M_DATA_B26
AR29 M_DATA_B30
AM28 M_DATA_B24
AL28 M_DATA_B29
AR28 M_DATA_B31
AP28 M_DATA_B27
AR12 M_DATA_B32
AP12 M_DATA_B33
AM13 M_DATA_B39
AL13 M_DATA_B35
AR13 M_DATA_B36
AP13 M_DATA_B37
AM12 M_DATA_B38
AL12 M_DATA_B34
AP10 M_DATA_B40
AR10 M_DATA_B41
AR7 M_DATA_B47
AP7 M_DATA_B43
AR9 M_DATA_B44
AP9 M_DATA_B45
AR6 M_DATA_B46
AP6 M_DATA_B42
AM10 M_DATA_B52
AL10 M_DATA_B49
AM7 M_DATA_B51
AL7 M_DATA_B50
AM9 M_DATA_B48
AL9 M_DATA_B53
AM6 M_DATA_B54
AL6 M_DATA_B55
AJ6 M_DATA_B56
AJ7 M_DATA_B57
AE6 M_DATA_B58
AE7 M_DATA_B62
AH7 M_DATA_B60
AH6 M_DATA_B61
AE7 M_DATA_B63
AF6 M_DATA_B59
AF34 M_DQS_B_DN0
AK33 M_DQS_B_DN1
AN33 M_DQS_B_DN2
AP29 M_DQS_B_DN3
AN13 M_DQS_B_DN4
AR8 M_DQS_B_DN5
AM8 M_DQS_B_DN6
AG6 M_DQS_B_DN7
AN26
AF35 M_DQS_B_DP0
AL33 M_DQS_B_DP1
AP33 M_DQS_B_DP2
AP28 M_DQS_B_DP3
AN12 M_DQS_B_DP4
AP8 M_DQS_B_DP5
AL8 M_DQS_B_DP6
AG7 M_DQS_B_DP7
AN25
M_DQS_B_DN0 9
M_DQS_B_DN1 9
M_DQS_B_DN2 9
M_DQS_B_DN3 9
M_DQS_B_DN4 9
M_DQS_B_DN5 9
M_DQS_B_DN6 9
M_DQS_B_DN7 9
M_DQS_B_DP0 9
M_DQS_B_DP1 9
M_DQS_B_DP2 9
M_DQS_B_DP3 9
M_DQS_B_DP4 9
M_DQS_B_DP5 9
M_DQS_B_DP6 9
M_DQS_B_DP7 9
M_DATA_B[63..0] 9
CHANNEL B
LGA1151
ZIF-SOCKET1151-HF-1
N12-151A020-F02
MICRO-STAR INT'L CO.,LTD
MS-7973
Size Custom
Document Description CPU-Memory
Rev 10
Date: Tuesday, April 21, 2015
Sheet 3 of 48



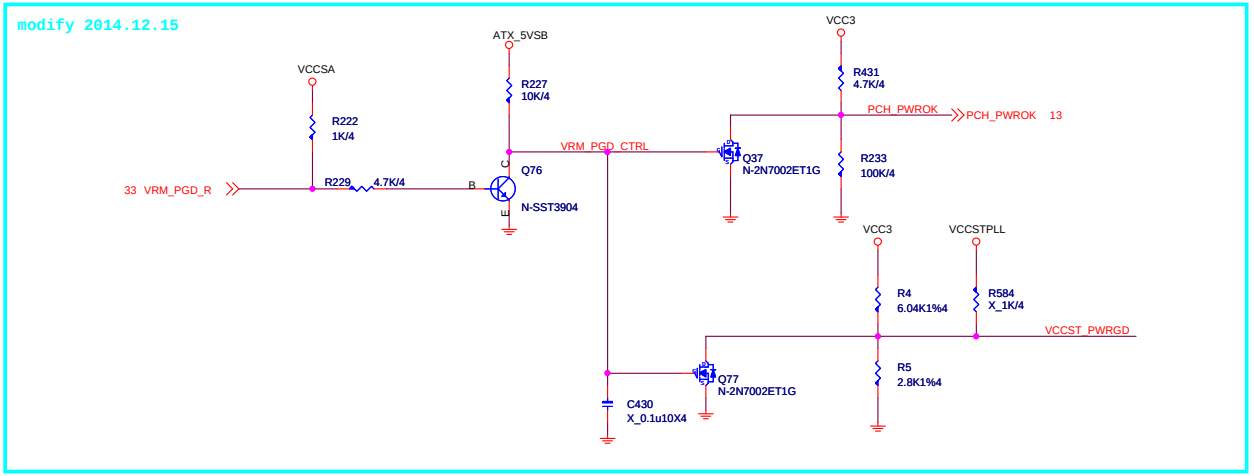
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7973	
Size: Custom	Document Description: CPU-PEG/Display	Rev: 10
Date: Tuesday, April 21, 2015	Sheet 4 of 48	

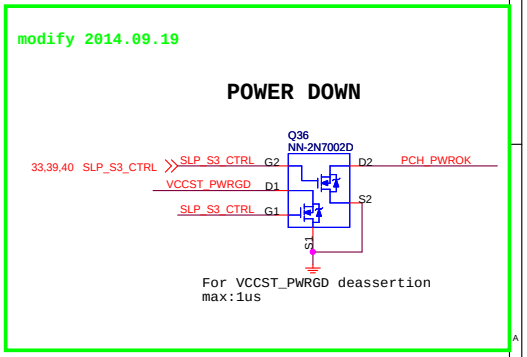


CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		



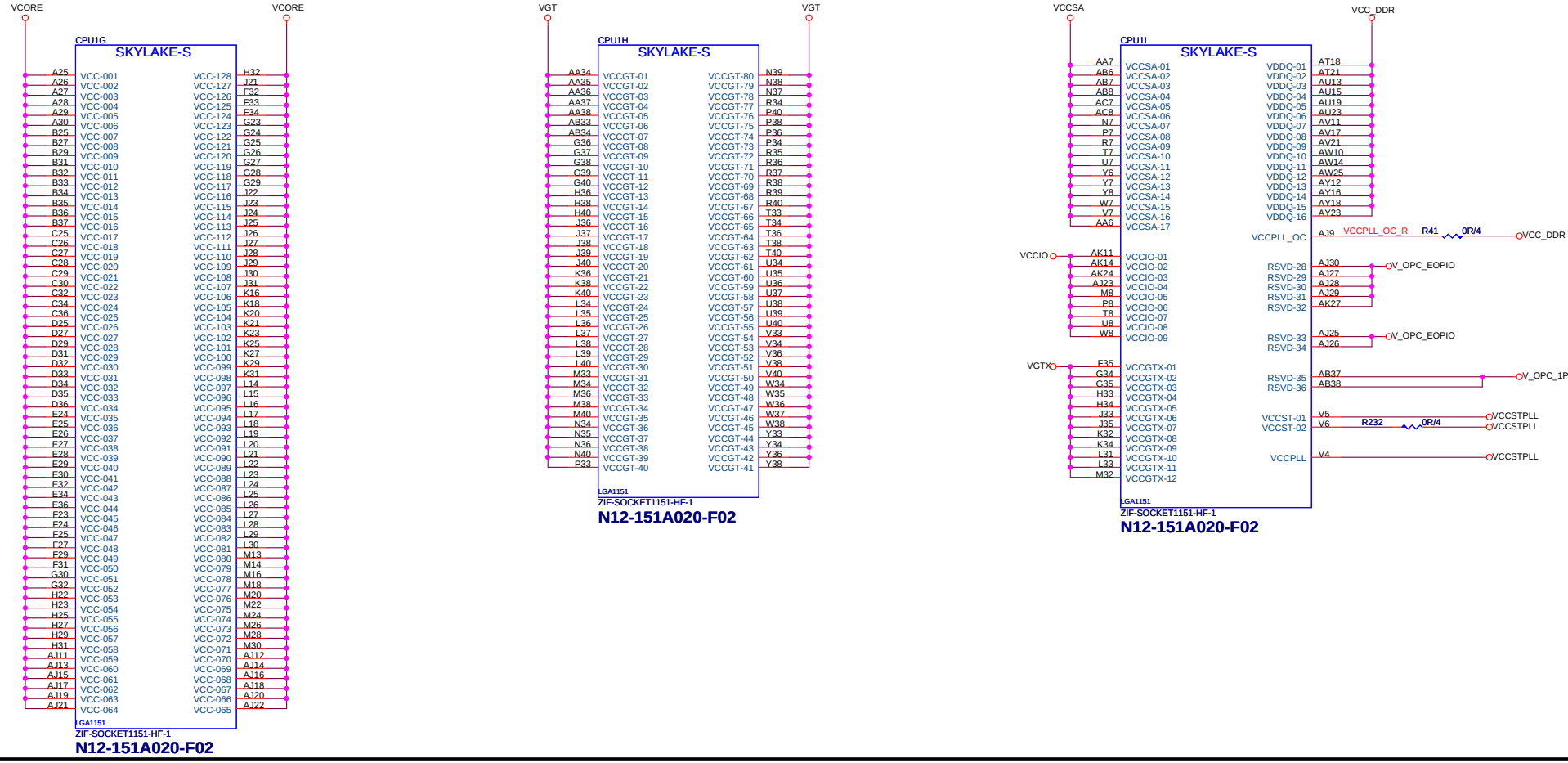


MICRO-STAR INT'L CO.,LTD

MS-7973

Size	Document Description	Rev
Custom	CPU-Control/MISC/CFG/Audio	10

Date: Tuesday, April 21, 2015 Sheet 5 of 48


VCORE
CPU1G
SKYLAKE-S
VCC-001 A25
VCC-002 A26
VCC-003 A27
VCC-004 A28
VCC-005 A29
VCC-006 A30
VCC-007 B25
VCC-008 B27
VCC-009 B29
VCC-010 B31
VCC-011 B32
VCC-012 B33
VCC-013 B34
VCC-014 B35
VCC-015 B36
VCC-016 B37
VCC-017 C25
VCC-018 C26
VCC-019 C27
VCC-020 C28
VCC-021 C29
VCC-022 C30
VCC-023 C32
VCC-024 C34
VCC-025 C36
VCC-026 D25
VCC-027 D27
VCC-028 D29
VCC-029 D31
VCC-030 D32
VCC-031 D33
VCC-032 D34
VCC-033 D35
VCC-034 D36
VCC-035 E24
VCC-036 E25
VCC-037 E26
VCC-038 E27
VCC-039 E28
VCC-040 E29
VCC-041 E30
VCC-042 E32
VCC-043 E34
VCC-044 E36
VCC-045 F23
VCC-046 F24
VCC-047 F25
VCC-048 F27
VCC-049 F29
VCC-050 F31
VCC-051 G30
VCC-052 G32
VCC-053 H22
VCC-054 H23
VCC-055 H25
VCC-056 H27
VCC-057 H29
VCC-058 H31
VCC-059 AJ11
VCC-060 AJ13
VCC-061 AJ15
VCC-062 AJ17
VCC-063 AJ19
VCC-064 AJ21
VCC-065 AJ22
VCC-066 AJ20
VCC-067 AJ18
VCC-068 AJ16
VCC-069 AJ14
VCC-070 AJ12
VCC-071 M30
VCC-072 M28
VCC-073 M26
VCC-074 M24
VCC-075 M22
VCC-076 M20
VCC-077 M18
VCC-078 M16
VCC-079 M14
VCC-080 M13
VCC-081 L30
VCC-082 L29
VCC-083 L28
VCC-084 L27
VCC-085 L26
VCC-086 L25
VCC-087 L24
VCC-088 L23
VCC-089 L22
VCC-090 L21
VCC-091 L20
VCC-092 L19
VCC-093 L18
VCC-094 L17
VCC-095 L16
VCC-096 L15
VCC-097 L14
VCC-098 K31
VCC-099 K29
VCC-100 K27
VCC-101 K25
VCC-102 K23
VCC-103 K21
VCC-104 K20
VCC-105 K18
VCC-106 K16
VCC-107 J31
VCC-108 J30
VCC-109 J29
VCC-110 J28
VCC-111 J27
VCC-112 J26
VCC-113 J25
VCC-114 J24
VCC-115 J23
VCC-116 J22
VCC-117 G29
VCC-118 G28
VCC-119 G27
VCC-120 G26
VCC-121 G25
VCC-122 G24
VCC-123 G23
VCC-124 F34
VCC-125 F33
VCC-126 F32
VCC-127 J21
VCC-128 H32
LGA1151
ZIF-SOCKET1151-HF-1
N12-151A020-F02
VGT
CPU1H
SKYLAKE-S
VCCGT-01 AA34
VCCGT-02 AA35
VCCGT-03 AA36
VCCGT-04 AA37
VCCGT-05 AA38
VCCGT-06 AB33
VCCGT-07 AB34
VCCGT-08 G36
VCCGT-09 G37
VCCGT-10 G38
VCCGT-11 G39
VCCGT-12 G40
VCCGT-13 H36
VCCGT-14 H38
VCCGT-15 H40
VCCGT-16 J36
VCCGT-17 J37
VCCGT-18 J38
VCCGT-19 J39
VCCGT-20 J40
VCCGT-21 K36
VCCGT-22 K38
VCCGT-23 K40
VCCGT-24 L34
VCCGT-25 L35
VCCGT-26 L36
VCCGT-27 L37
VCCGT-28 L38
VCCGT-29 L39
VCCGT-30 L40
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VCCGT-32 M34
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VCCGT-34 M38
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VCCGT-36 N34
VCCGT-37 N35
VCCGT-38 N36
VCCGT-39 N40
VCCGT-40 P33
VCCGT-41 Y38
VCCGT-42 Y36
VCCGT-43 Y34
VCCGT-44 Y33
VCCGT-45 W38
VCCGT-46 W37
VCCGT-47 W36
VCCGT-48 W35
VCCGT-49 W34
VCCGT-50 V40
VCCGT-51 V39
VCCGT-52 V36
VCCGT-53 V34
VCCGT-54 V33
VCCGT-55 U40
VCCGT-56 U39
VCCGT-57 U38
VCCGT-58 U37
VCCGT-59 U36
VCCGT-60 U35
VCCGT-61 U34
VCCGT-62 T40
VCCGT-63 T38
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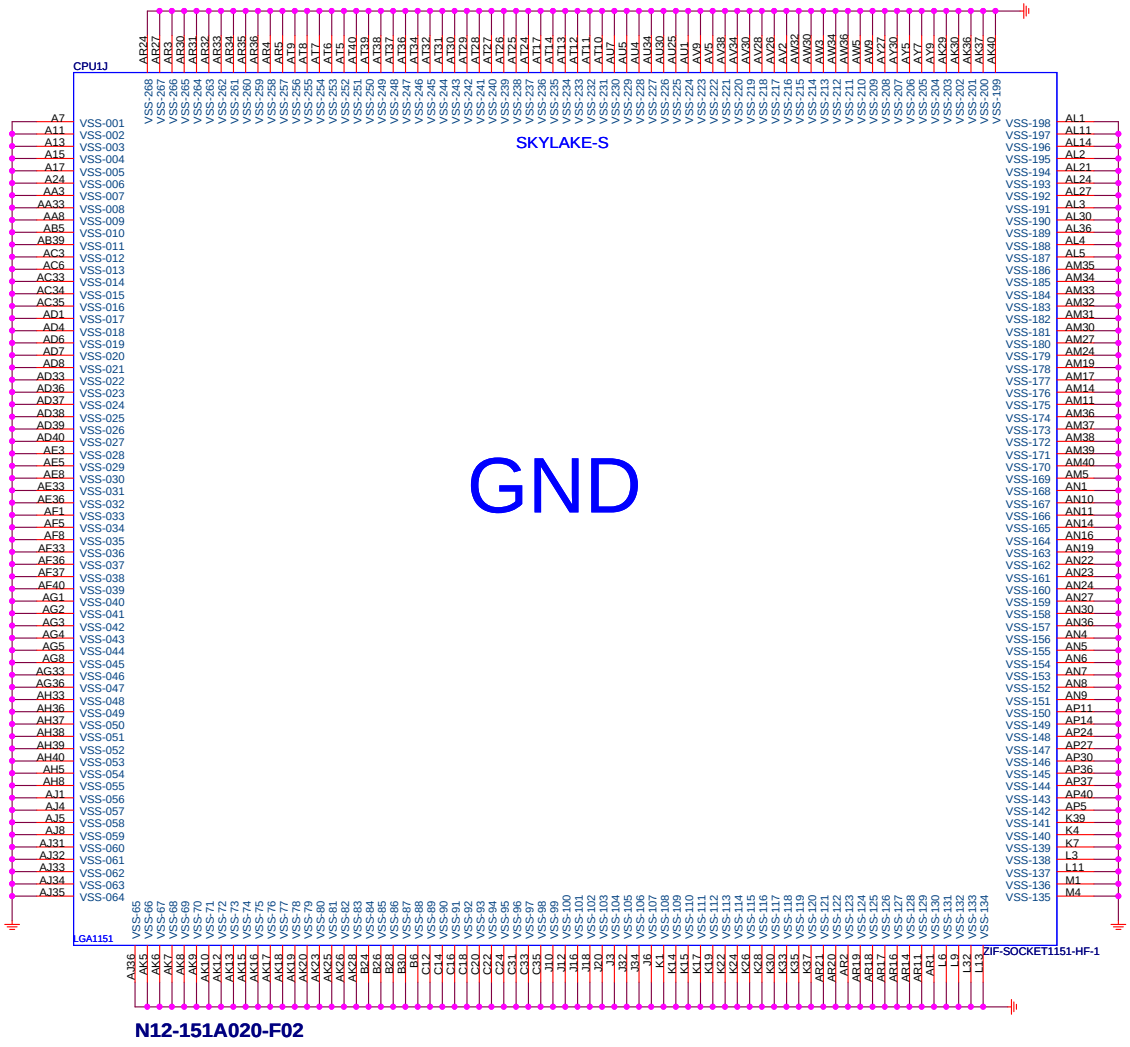
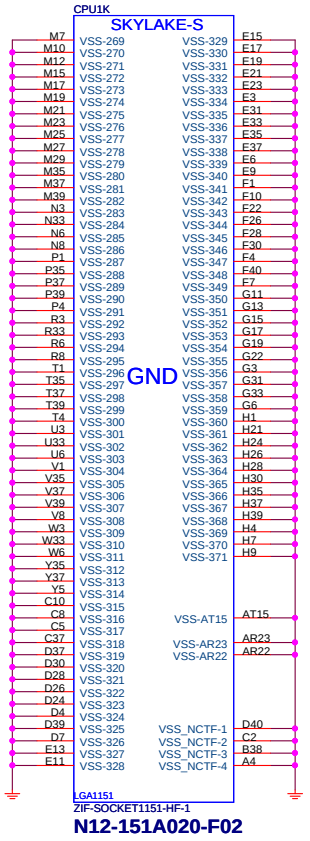
VCCGT-66 T33
VCCGT-67 R40
VCCGT-68 R39
VCCGT-69 R38
VCCGT-70 R37
VCCGT-71 R36
VCCGT-72 R35
VCCGT-73 P34
VCCGT-74 P36
VCCGT-75 P38
VCCGT-76 P40
VCCGT-77 R34
VCCGT-78 N37
VCCGT-79 N38
VCCGT-80 N39
LGA1151
ZIF-SOCKET1151-HF-1
N12-151A020-F02
VCCSA
VCC_DDR
CPU1I
SKYLAKE-S
VCCSA-01 AA7
VCCSA-02 AB6
VCCSA-03 AB7
VCCSA-04 AB8
VCCSA-05 AC7
VCCSA-06 AC8
VCCSA-07 N7
VCCSA-08 P7
VCCSA-09 R7
VCCSA-10 T7
VCCSA-11 U7
VCCSA-12 Y6
VCCSA-13 Y7
VCCSA-14 Y8
VCCSA-15 W7
VCCSA-16 V7
VCCSA-17 AA6
VDDQ-01 AT18
VDDQ-02 AT21
VDDQ-03 AU13
VDDQ-04 AU15
VDDQ-05 AU19
VDDQ-06 AU23
VDDQ-07 AV11
VDDQ-08 AV17
VDDQ-09 AV21
VDDQ-10 AW10
VDDQ-11 AW14
VDDQ-12 AW25
VDDQ-13 AY12
VDDQ-14 AY16
VDDQ-15 AY18
VDDQ-16 AY23
VCCPLL_OC AJ9
VCCPLL_OC_R
R41
0R/4
VCC_DDR
VCCIO
VCCIO-01 AK11
VCCIO-02 AK14
VCCIO-03 AK24
VCCIO-04 AJ23
VCCIO-05 M8
VCCIO-06 P8
VCCIO-07 T8
VCCIO-08 U8
VCCIO-09 W8
RSVD-28 AJ30
RSVD-29 AJ27
RSVD-30 AJ28
RSVD-31 AJ29
RSVD-32 AK27
V_OPC_EOPIO
RSVD-33 AJ25
RSVD-34 AJ26
V_OPC_EOPIO
VGTX
VCCGTX-01 F35
VCCGTX-02 G34
VCCGTX-03 G35
VCCGTX-04 H33
VCCGTX-05 H34
VCCGTX-06 J33
VCCGTX-07 J35
VCCGTX-08 K32
VCCGTX-09 K34
VCCGTX-10 L31
VCCGTX-11 L33
VCCGTX-12 M32
RSVD-35 AB37
RSVD-36 AB38
V_OPC_1P8
VCCST-01 V5
VCCST-02 V6
R232
0R/4
VCCSTPLL
VCCSTPLL
VCCPLL V4
VCCSTPLL
LGA1151
ZIF-SOCKET1151-HF-1
N12-151A020-F02
CAP
VCORE
C22 22u6.3X6
C23 22u6.3X6
C24 22u6.3X6
C26 22u6.3X6
C29 22u6.3X6
C31 22u6.3X6
C35 22u6.3X6
C37 22u6.3X6
C39 22u6.3X6
C189 22u6.3X6
C192 22u6.3X6
C194 22u6.3X6
C197 22u6.3X6
C198 22u6.3X6
C42 22u6.3X6
C202 22u6.3X6
C44 22u6.3X6
TOP SIDE SOCKET CAVITY
VCORE
C126 22u6.3X6
C133 22u6.3X6
C86 22u6.3X6
C64 22u6.3X6
C69 22u6.3X6
C134 22u6.3X6
C116 22u6.3X6
VCORE
C130 22u6.3X8
C170 22u6.3X8
C172 22u6.3X8
C184 X_22u6.3X8
C154 X_22u6.3X8
C33 X_22u6.3X8
C40 X_22u6.3X8
TOP SIDE SOCKET EDGE
TBD
VGT
C25 22u6.3X8
C27 22u6.3X8
C30 22u6.3X8
C32 22u6.3X8
C185 22u6.3X8
C34 22u6.3X6
C36 22u6.3X6
C38 22u6.3X6
TOP SIDE SOCKET CAVITY
VGT
C45 22u6.3X8
C120 22u6.3X8
C119 22u6.3X8
TOP SIDE SOCKET EDGE
VCCSA
C2 22u6.3X6
C4 22u6.3X6
TOP SIDE SOCKET CAVITY
VCC_DDR
C6 22u6.3X6
C7 22u6.3X6
C8 22u6.3X6
C9 22u6.3X6
TOP SIDE SOCKET CAVITY
VCCIO
C13 22u6.3X8
C15 22u6.3X6
C17 22u6.3X6
C19 22u6.3X6
C20 22u6.3X6
C21 22u6.3X6
TOP SIDE SOCKET CAVITY
V6
VCCSTPLL
C132 1u6.3X4
TOP SIDE SOCKET CAVITY
VCCSTPLL
C235 22u6.3X8
CRB
V_OPC_EOPIO
C28 X_22u6.3X6
TOP SIDE SOCKET CAVITY
V_OPC_1P8
C124 X_10u6.3X6
VGTX
C179 X_22u6.3X6
MICRO-STAR INT'L CO.,LTD
MS-7973
Size
Custom
Document Description
CPU-Power
Rev
10
Date: Thursday, May 07, 2015
Sheet 6 of 48





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MS-7973			
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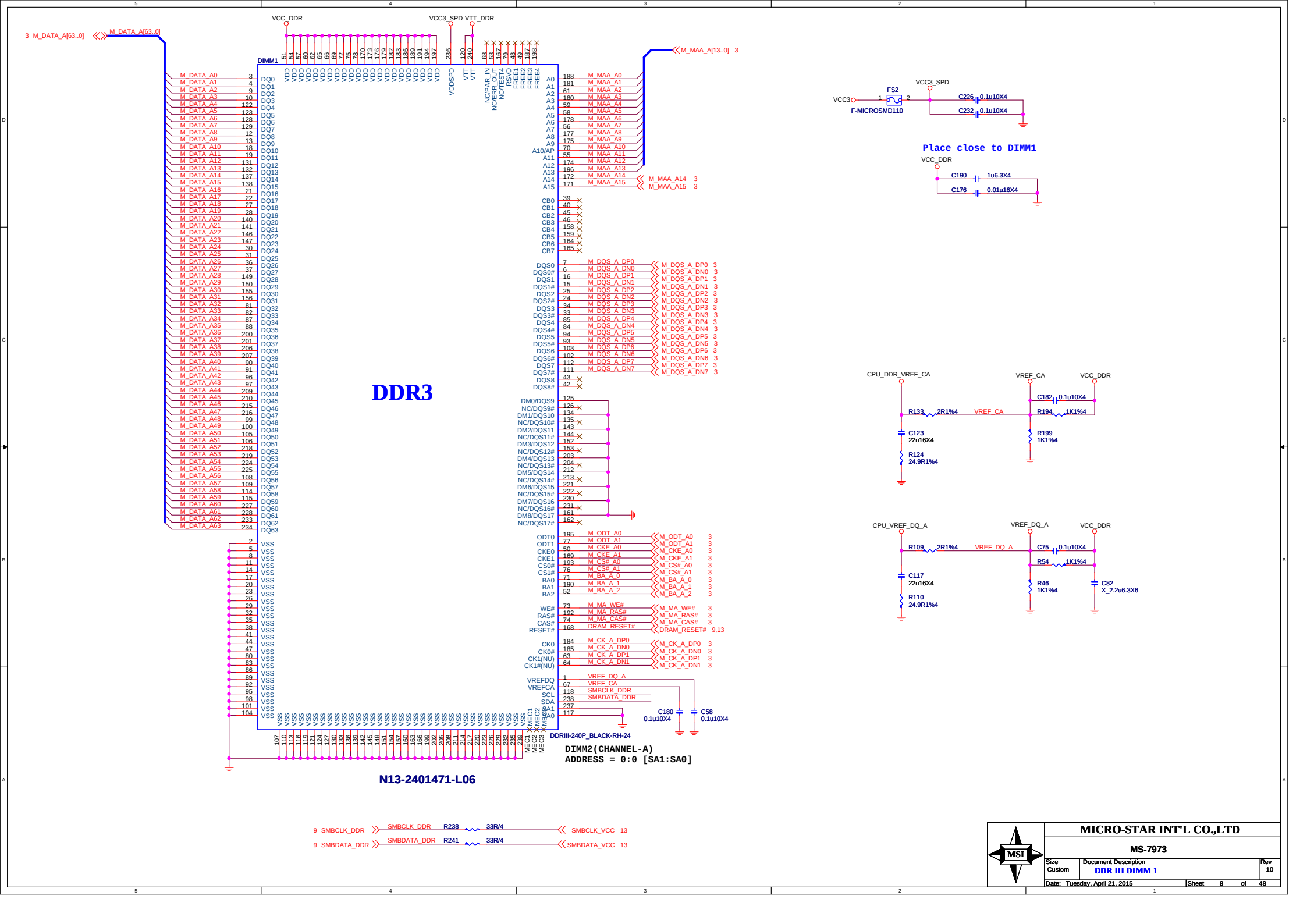
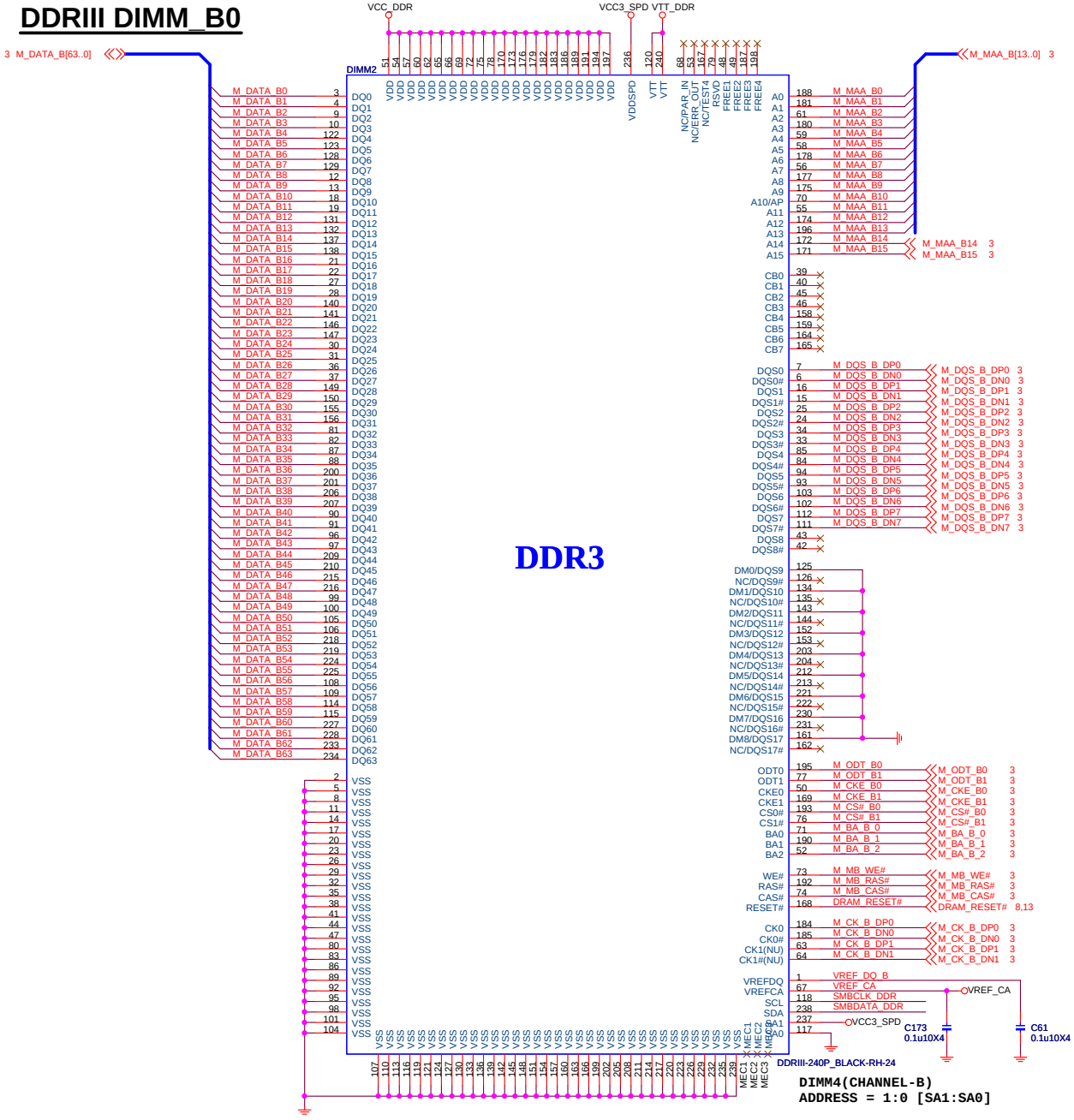
Date: Thursday, April 09, 2015		Sheet 7 of 48	

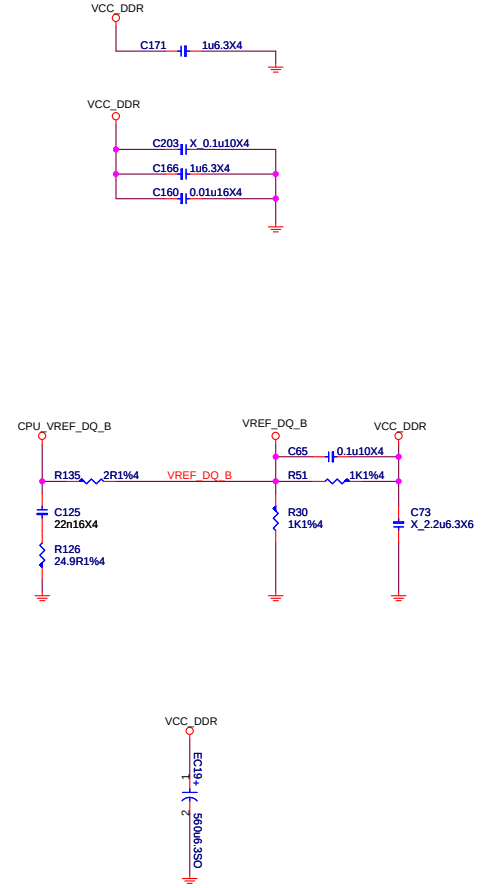

DDR3
DIMM1
DDRIII-240P_BLACK-RH-24
DIMM2(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
N13-2401471-L06
Place close to DIMM1
MICRO-STAR INT'L CO.,LTD
MS-7973
Size Custom
Document Description
DDR III DIMM 1
Rev 10
Date: Tuesday, April 21, 2015
Sheet 8 of 48

DDRIII DIMM_B0

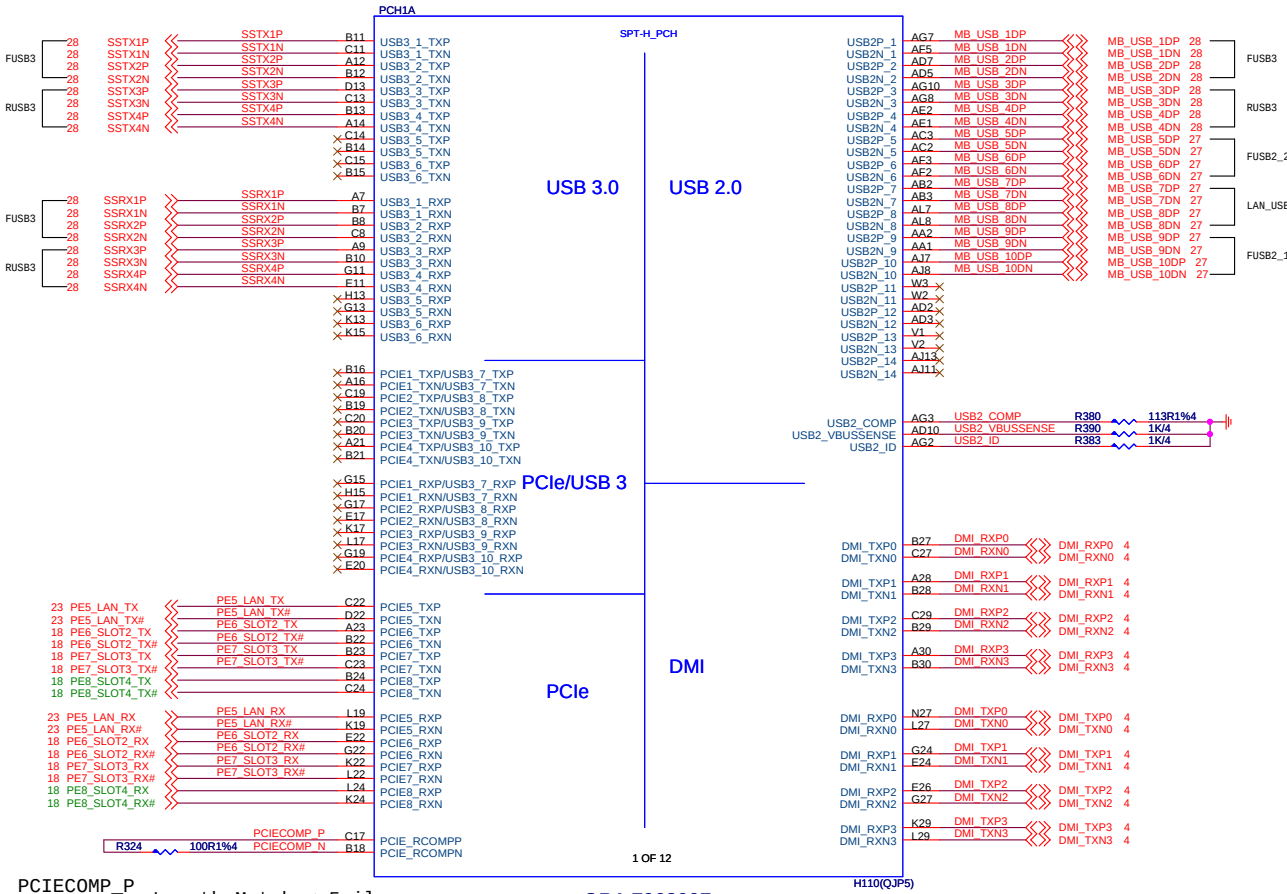


DDRIII DIMM_B1

Place close to DIMM2

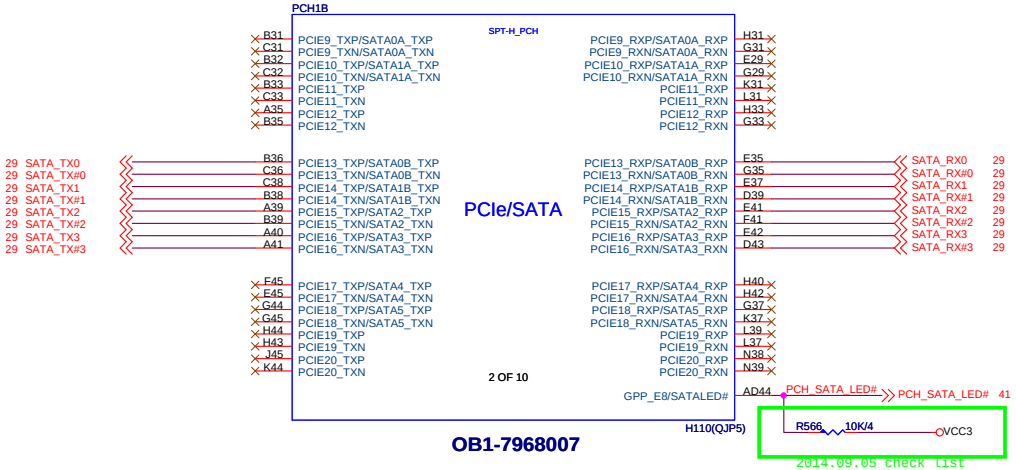


MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: DDR III DIMM 2	Rev: 10
Date: Tuesday, April 21, 2015	Sheet 9 of 48	



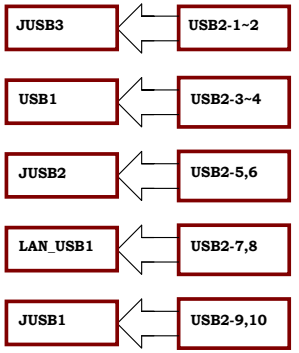
PCIECOMP_P
PCIECOMP_N Length Match < 5mil

OB1-7968007



OB1-7968007

2014.09.05 check list



USB2_COMP < 500 mil

	USB3[5-6]	USB3[7-8]
H110	X	X
B150	V	X
Q150	V	V
H170	V	X
Z170	V	X
Q170	V	X

MICRO-STAR INT'L CO.,LTD

MS-7973

Size	Document Description	Rev
Custom	PCH-USB/PCIE/DMI/SATA	10

Date: Thursday, April 23, 2015 Sheet 10 of 48

GPP_I[3:0] with SMI/NMI

EMI

AZ_BITCLK
CA23 X_10p50N4

PCH1D

21 AZ_BITCLK → AZ_BITCLK R449 33R/4 AZ_BITCLK_LR → BA9 HDA_BCLK
21 AZ_RST# → AZ_RST# R510 33R/4 AZ_RST#_R → BD8 HDA_RST#
21 AZ_SDIN0 → AZ_SDIN0 → BC8 HDA_SDI0
HDA_SDI1

16 AZ_SDOUT_R → AZ_SDOUT_R
21 AZ_SDOUT → AZ_SDOUT R489 33R/4 AZ_SDOUT_R → BB7 HDA_SDO
21 AZ_SYNC → AZ_SYNC R490 33R/4 AZ_SYNC_R → BD9 HDA_SYNC

5 PCH_CPU_AUD_SDO → R412 33R/4 PCH_CPU_AUD_SDO_R → AM1 DISPA_SDO
5 PCH_CPU_AUD_SDI → PCH_CPU_AUD_SDI → AN2 DISPA_SDI
5 PCH_CPU_AUD_SCLK → R419 33R/4 PCH_CPU_AUD_SCLK_R → AM2 DISPA_BCLK

AUDIO

AL42 GPP_D8/SSP0_SCLK
AN42 GPP_D7/SSP0_RXD
AM43 GPP_D6/SSP0_TXD
AJ33 GPP_D5/SSP0_SFRM

AH44 GPP_D20/DMIC_DATA0
AJ35 GPP_D19/DMIC_CLK0
AJ38 GPP_D18/DMIC_DATA1
AJ42 GPP_D17/DMIC_CLK1

4 OF 10

SPT-H_PCH

Port B
BA5 GPP_I5/DDPB_CTRLCLK → DSP_DDPB_CTRLCLK → DSP_DDPB_CTRLCLK 25
BC4 GPP_I6/DDPB_CTRLDATA → DSP_DDPB_CTRLDATA → DSP_DDPB_CTRLDATA 25
AW4 GPP_I0/DDPB_HPD0 → DSP_DDPB_HPD → DSP_DDPB_HPD 25

Port C
BB3 GPP_I7/DDPC_CTRLCLK → DVI_DDPC_CTRLCLK → DVI_DDPC_CTRLCLK 24
BD6 GPP_I8/DDPC_CTRLDATA → DVI_DDPC_CTRLDATA → DVI_DDPC_CTRLDATA 24
AY2 GPP_I1/DDPC_HPD1 → DVI_DDPC_HPD → DVI_DDPC_HPD 24

Port D
BE5 GPP_I9/DDPD_CTRLCLK → DP_DDPD_CTRLCLK
BE6 GPP_I10/DDPD_CTRLDATA → DP_DDPD_CTRLDATA
AV4 GPP_I2/DDPD_HPD2 → DP_HPD → DP_HPD 26

BA4 GPP_I3/DDPE_HPD3 → DDPE_HPD3 R428 10K/4
By Server CRB

eDP
W36 GPP_F21/EDP_BKLTCTL
W35 GPP_F20/EDP_BKLTEN
W42 GPP_F19/EDP_VDDEN
BD7 GPP_I4/EDP_HPD → EDP_HPD R476 100K/4

H110(QJP5)

VCC3
DSP_DDPB_CTRLCLK R414 2.2K/4
DSP_DDPB_CTRLDATA R422 2.2K/4
DVI_DDPC_CTRLCLK R410 2.2K/4
DVI_DDPC_CTRLDATA R415 2.2K/4
DP_DDPD_CTRLCLK R523 2.2K/4
DP_DDPD_CTRLDATA R492 2.2K/4

DDI interfaace Disable
no connect

Port B HDMI

Port C DVI,HDMI2.0 OR Others

Port D DisplayPort

OB1-7968007

24M CLOCK BUFFER

3VSB
U19
CLK_BUFFER R541 X_10K/4
CLK_SIO_24M R539 X_0R/4 CLK_BUFFER_OUT0
CLK_IN CLK3 OE CLK2 CLK0 VDD GND CLK1
3VSB
R540 X_0R/4 CLK_BUFFER_OUT1
R520 X_0R/4 CLK_SIO_PCI
X_5V30014PGGI8_TSSOP8-HF

CO-LAY

EMI
CLK_BUFFER CA25 X_10p50N4
CLK_SIO_PCI CA26 X_10p50N4
CLK_SIO_24M CA27 X_10p50N4
TPM_CLK CA36 X_10p50N4

CLK_BUFFER R516 X_22R/4

19 CLK_SIO_PCI → CLK_SIO_PCI R614 0R/4
19 CLK_SIO_24M → CLK_SIO_24M R613 22R/4 → CLK_PCH_LPC0 → BC17 GPP_A9/CLKOUT_LPC0/ESPI_CLK
41 TPM_CLK → R612 0R/4 → TPM_CLK_R → AV19 GPP_A10/CLKOUT_LPC1
TP18 CLKOUT_48M → AR17 GPP_A16/CLKOUT_48

PCH_CLK5_1P0 → R339 2.7K1%4 → XCLK_BIASREF → E1 XCLK_BIASREF

XCLK_BIASREF < 500 mil

PCH1C

SPT-H_PCH

CLKOUT_CPUBCLK_P G2 PCH_CPU_BCLK_DP → PCH_CPU_BCLK_DP 5
CLKOUT_CPUBCLK_N H2 PCH_CPU_BCLK_DN → PCH_CPU_BCLK_DN 5 100M
CLKOUT_CPUNSSC_P G1 PCH_CPU_NSSC_CLK_DP → PCH_CPU_NSSC_CLK_DP 5
CLKOUT_CPUNSSC_N F1 PCH_CPU_NSSC_CLK_DN → PCH_CPU_NSSC_CLK_DN 5 24M
CLKOUT_CPUPCIBCLK_P J2 PCH_CPU_PCIE_DP → PCH_CPU_PCIE_DP 5
CLKOUT_CPUPCIBCLK_N J1 PCH_CPU_PCIE_DN → PCH_CPU_PCIE_DN 5 100M
CLKOUT_ITPXDP_P L2
CLKOUT_ITPXDP_N L1

CLKREQ#0 BC24 GPP_B5/SRCCLKREQ0#
CLKREQ#1 AW24 GPP_B6/SRCCLKREQ1#
CLKREQ#2 AT24 GPP_B7/SRCCLKREQ2#
CLKREQ#3 BD25 GPP_B8/SRCCLKREQ3#
CLKREQ#4 BB24 GPP_B9/SRCCLKREQ4#
CLKREQ#5 BE25 GPP_B10/SRCCLKREQ5#
CLKREQ#6 AT33 GPP_H0/SRCCLKREQ6#
CLKREQ#7 AR31 GPP_H1/SRCCLKREQ7#
CLKREQ#8 BD32 GPP_H2/SRCCLKREQ8#
CLKREQ#9 BC32 GPP_H3/SRCCLKREQ9#
CLKREQ#10 BB31 GPP_H4/SRCCLKREQ10#
CLKREQ#11 BC33 GPP_H5/SRCCLKREQ11#
CLKREQ#12 BA33 GPP_H6/SRCCLKREQ12#
CLKREQ#13 AW33 GPP_H7/SRCCLKREQ13#
CLKREQ#14 BB33 GPP_H8/SRCCLKREQ14#
CLKREQ#15 BD33 GPP_H9/SRCCLKREQ15#

XTAL_24M_PCH_IN A6 XTAL24_IN
XTAL_24M_PCH_OUT A5 XTAL24_OUT

3 OF 10

CLKOUT_SRC_P0 N8 → CK_SLOT2_DP 18
CLKOUT_SRC_N0 N7 → CK_SLOT2_DN 18
CLKOUT_SRC_P1 L5 → CK_SLOT4_DP 18
CLKOUT_SRC_N1 L7 → CK_SLOT4_DN 18
CLKOUT_SRC_P2 F2
CLKOUT_SRC_N2 D3
CLKOUT_SRC_P3 G4 → CK_SLOT1_DP 17
CLKOUT_SRC_N3 E5 → CK_SLOT1_DN 17
CLKOUT_SRC_P4 E6 → CK_PE_LAN 23
CLKOUT_SRC_N4 D5 → CK_PE_LAN# 23
CLKOUT_SRC_P5 D7
CLKOUT_SRC_N5 D8
CLKOUT_SRC_P6 R7
CLKOUT_SRC_N6 R8
CLKOUT_SRC_P7 U7
CLKOUT_SRC_N7 U5
CLKOUT_SRC_P8 W11
CLKOUT_SRC_N8 W10
CLKOUT_SRC_P9 N2
CLKOUT_SRC_N9 N3
CLKOUT_SRC_P10 P2
CLKOUT_SRC_N10 P3
CLKOUT_SRC_P11 R4 → CK_SLOT3_DP 18
CLKOUT_SRC_N11 R3 → CK_SLOT3_DN 18
CLKOUT_SRC_P12 U3
CLKOUT_SRC_N12 U2
CLKOUT_SRC_P13 Y5
CLKOUT_SRC_N13 W7
CLKOUT_SRC_P14 R2
CLKOUT_SRC_N14 P1
CLKOUT_SRC_P15 R11
CLKOUT_SRC_N15 R13

Clock

H110(QJP5)

OB1-7968007

LAN
23 CLKREQ#4

VCC3
R527 10K/4 CLKREQ#0
R529 10K/4 CLKREQ#1
R531 10K/4 CLKREQ#2
R528 10K/4 CLKREQ#3
R501 10K/4 CLKREQ#4
R546 10K/4 CLKREQ#5
R479 10K/4 CLKREQ#6
R405 10K/4 CLKREQ#7
R465 10K/4 CLKREQ#8
R466 10K/4 CLKREQ#9
R481 10K/4 CLKREQ#10
R468 10K/4 CLKREQ#11
R478 10K/4 CLKREQ#12
R477 10K/4 CLKREQ#13
R469 10K/4 CLKREQ#14
R467 10K/4 CLKREQ#15

Conntact to SLOT Pin B12
for support L1 PM Substates
ME also can disable this funtion.

XTAL_24M_PCH_OUT
XTAL_24M_PCH_IN
R327 1M1%6
Y1
24MHZ20P
C332 22p50N4
C326 22p50N4

MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: PCH-Audio/Display/Clock	Rev: 10
Date: Monday, May 04, 2015	Sheet 11 of 48	

W/ SMI/NMI Funtion

GPP_B[23,20,14]
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]

3VSB PWR_GPP_A CP13 BC42 C380 X_0.1u10X4

2014.10.16 PCH cOM BACK test

CRB R400 X_8.2K1%4 GPP_E3 R545 8.2K1%4 GPP_B4

GPP_B11 default GPO to LOW

If the interface is not used: the signals can be used as GPIO. If GPIO functionality is also not used, the signals can be left as no-connect.

ISH For U,Y only use

UART/GPIO no use can no connect

SML For sever only use

PCH1F SPT-H_PCH

GROUP CD PWR GROUP BCH PWR GROUP EF PWR GPIO A GPIO B GPIO C GPIO D GPIO E GPIO F GPIO G GPIO H GPIO DSW

6 OF 10 H110(QJP5)

OB1-7968007

2014.08.14

Remove

3VSB AJ41 AD41 C367 X_0.1u10X4 C356 X_0.1u10X4

For BIOS BOM USE

When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

PCH1E SPT-H_PCH

USB OC# SATA DEVSLP CLINK SATA Strap

RSVD For B150 SATA/PCIE use

RSVD For B150 SATA/PCIE use

5 OF 10 H110(QJP5)

OB1-7968007

2014.08.14

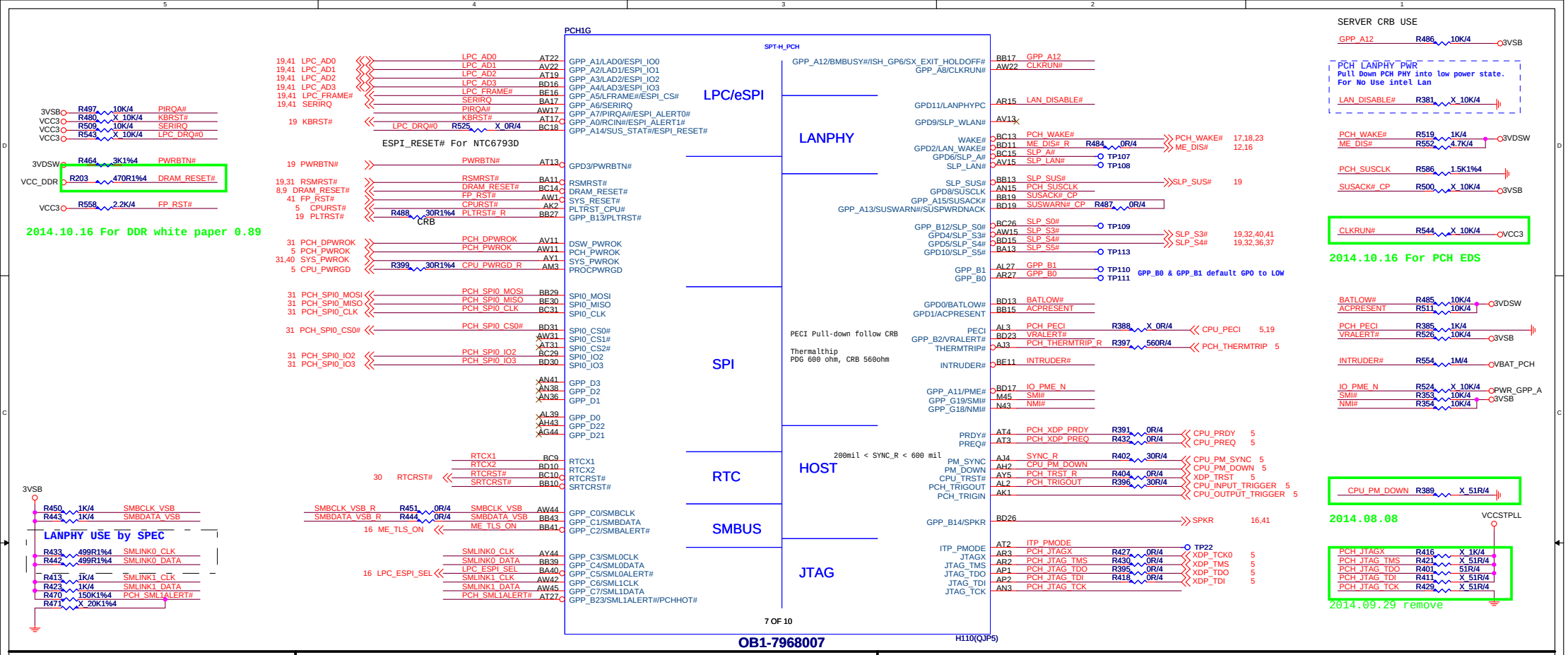
If an AMT capable Intel WLAN device is not implemented then this signal can be left as NO CONNECT (NC).

MICRO-STAR INT'L CO.,LTD

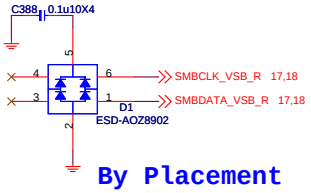
MS-7973

Size Custom | Document Description PCH-GPIO/USBOC#/SATASTRAP | Rev 10

Date: Thursday, April 23, 2015 | Sheet 12 of 48

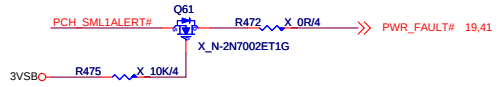


SMBUS ESD



By Placement

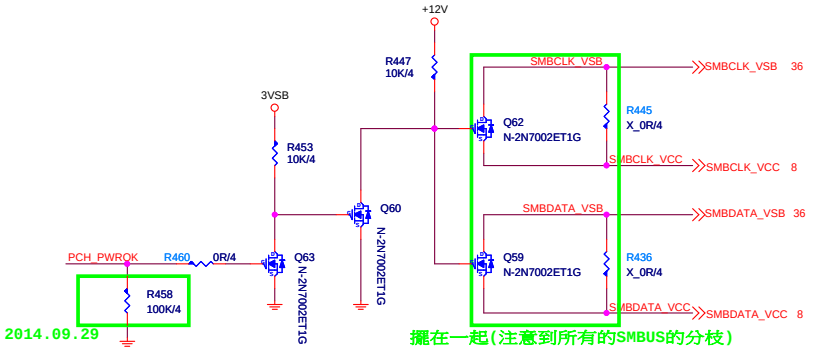
PCH Thermal Monitor



當溫度高於設定之後，此信號會被拉LOW。
PS:只能在S0下使用，S5 不會有功能

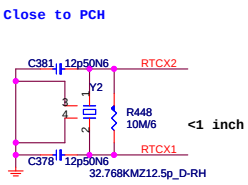
SMBUS隔離線路(PCH接出來是PULL HIGH 3VSB)
需要再S3/S5底下動作的接SMBCLK_VSB/SMBDATA_VSB
不需要的接SMBCLK_VCC/SMBDATA_VCC

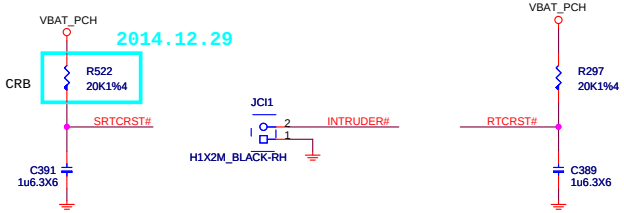
基本上PCIE的SLOT要接3VSB的CPU的PWM IC/DDR要接VCC3的其他的請注意要怎麼接



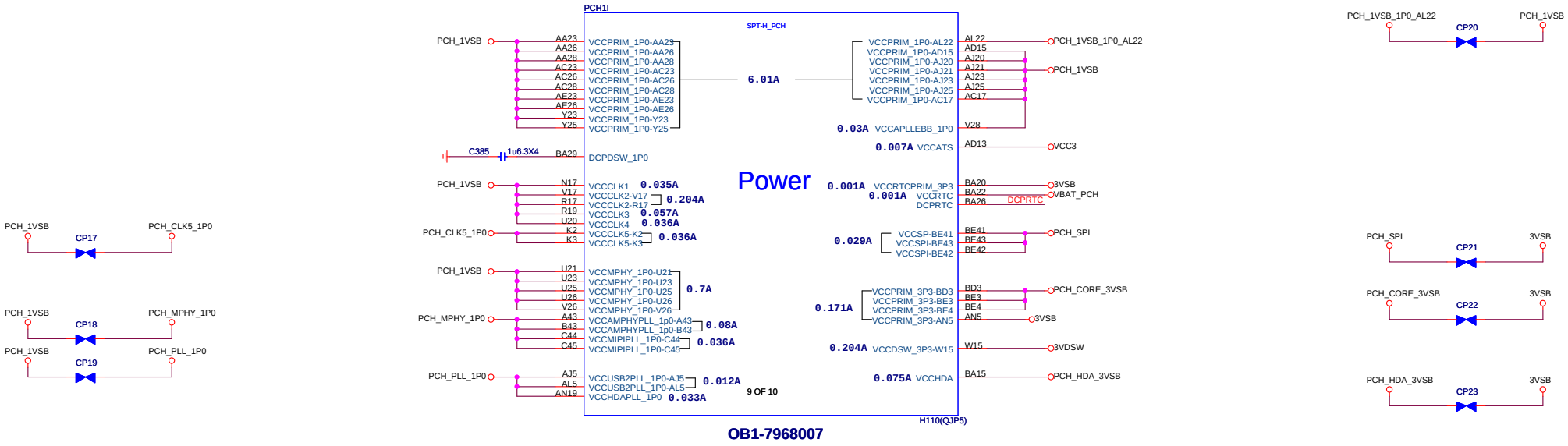
RTC Block

Close to PCH

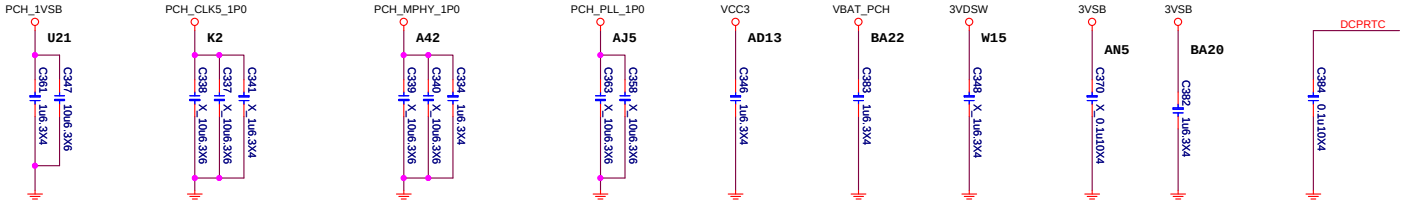


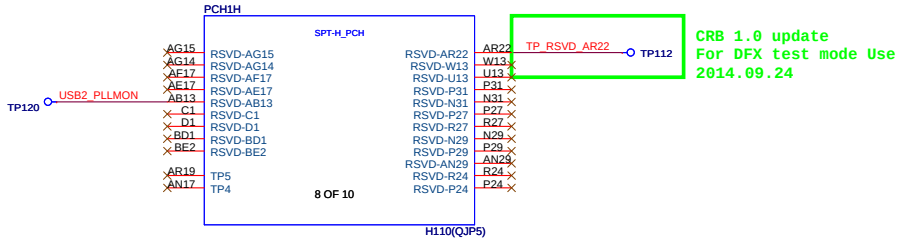


MICRO-STAR INT'L CO.,LTD	
MS-7973	
Size: Custom	Document Description: PCH-LPC/SPI/SMBUS/MISC
Rev: 10	
Date: Thursday, April 23, 2015	Sheet 13 of 48



OB1-7968007





OB1-7968007

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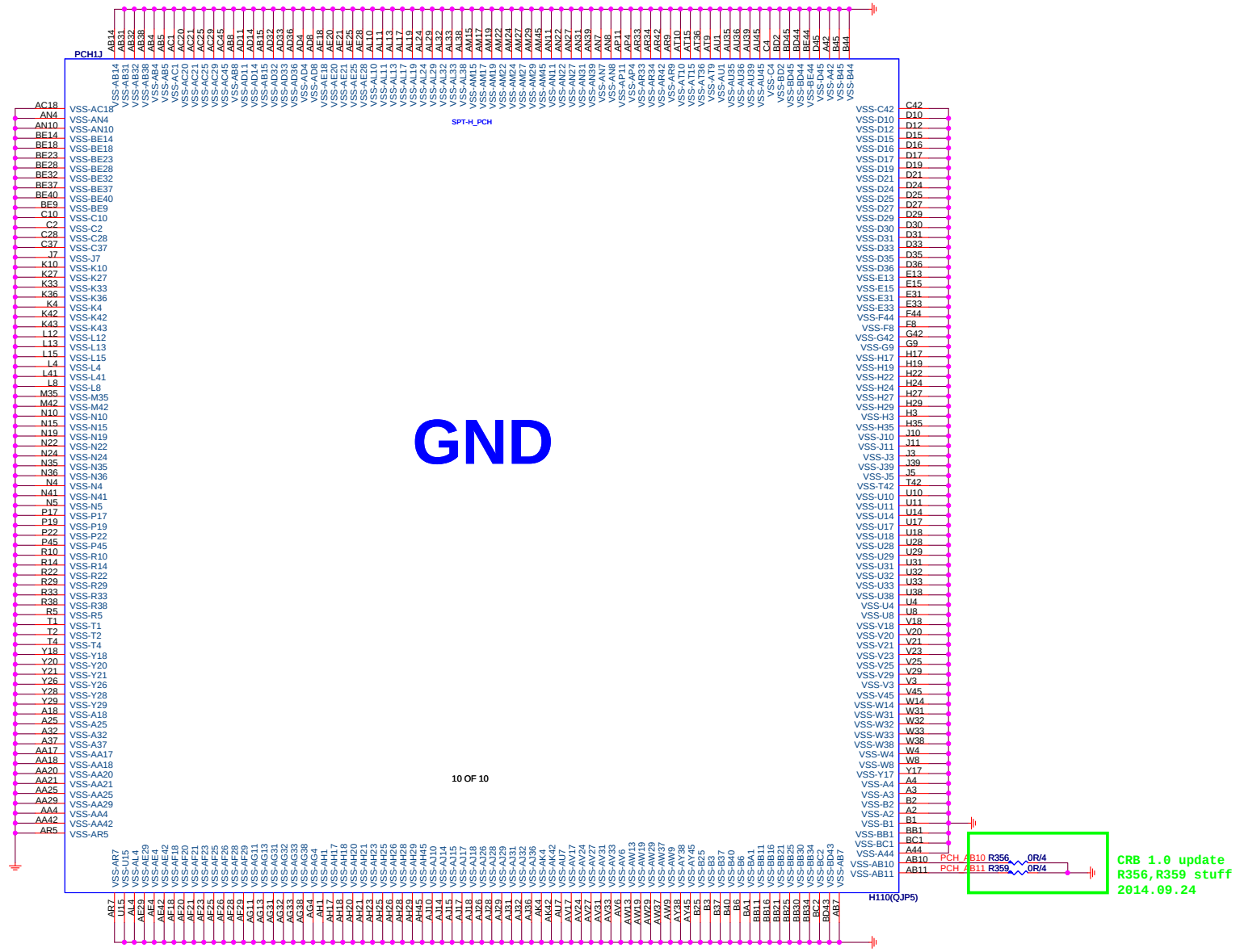
MS-7973		
Size: Custom	Document Description: PCH-Power	Rev: 10
Date: Thursday, May 07, 2015	Sheet 14 of 48	

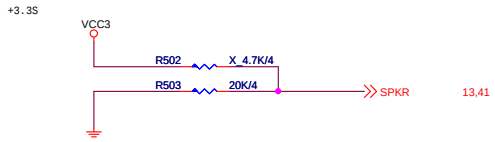


CRB 1.0 update
R356,R359 stuff
2014.09.24

OB1-7968007

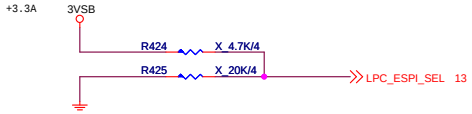
MICRO-STAR INT'L CO.,LTD			
MS-7973			
Size: Custom	Document Description: PCH-GND		Rev: 10
Date: Thursday, April 23, 2015		Sheet 15 of 48	

TOP Swap



Internal pull-down 20K is disabled after PLTRST#

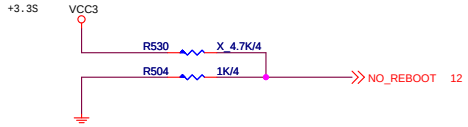
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

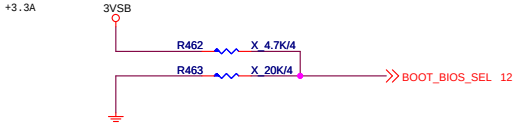
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

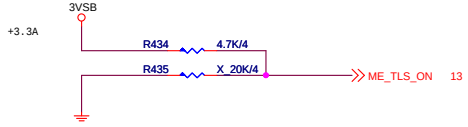
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

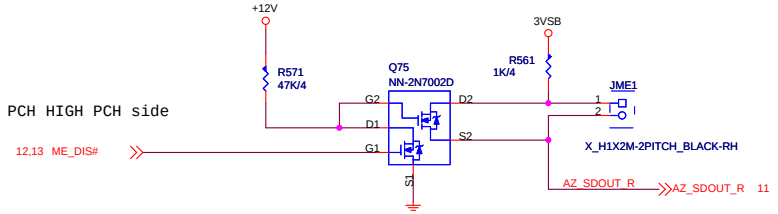
AMT and SBA with confidentiality



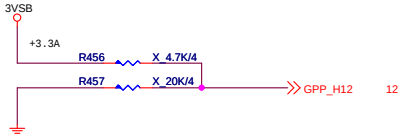
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE

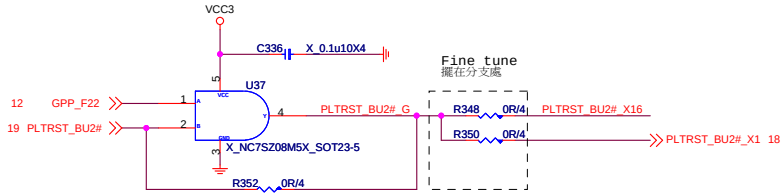


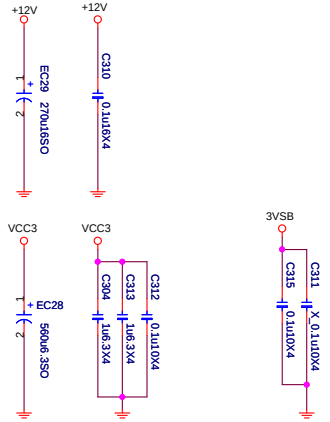
0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

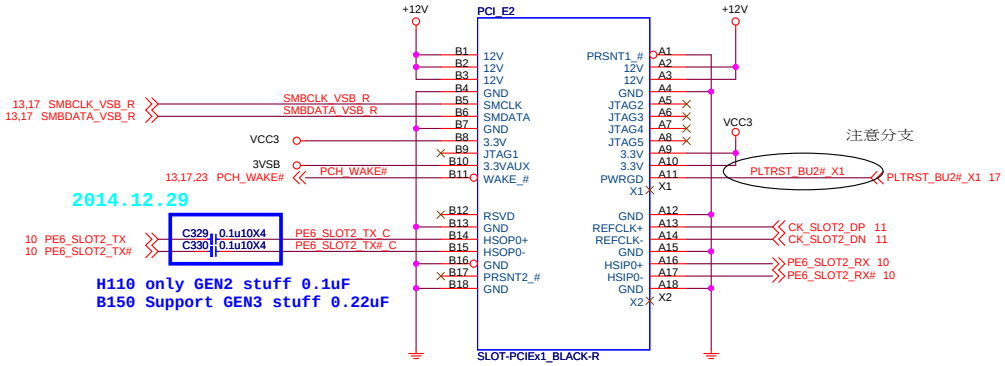
MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: PCH-Strap	Rev: 10
Date: Tuesday, April 21, 2015	Sheet 16 of 48	

N11-1641221-L06

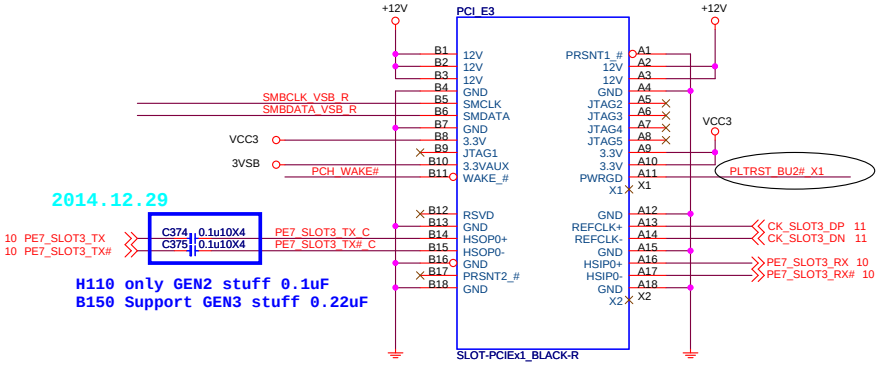




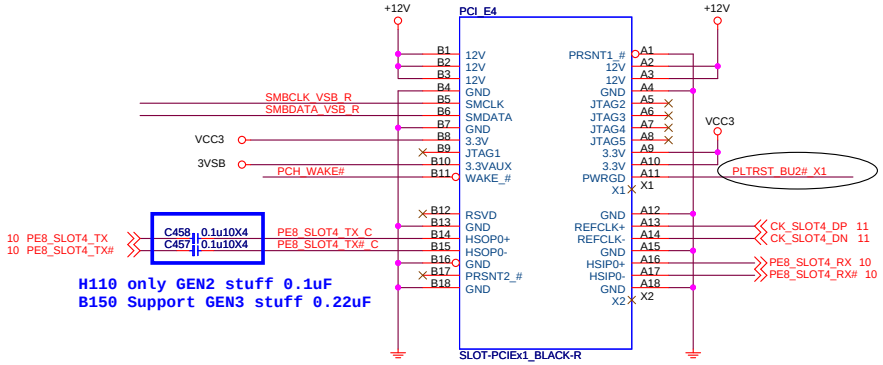
MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: PCIE SLOT-CPU(X16)	Rev: 10
Date: Tuesday, April 21, 2015	Sheet 17 of 48	



N11-0360381-L06



N11-0360381-L06



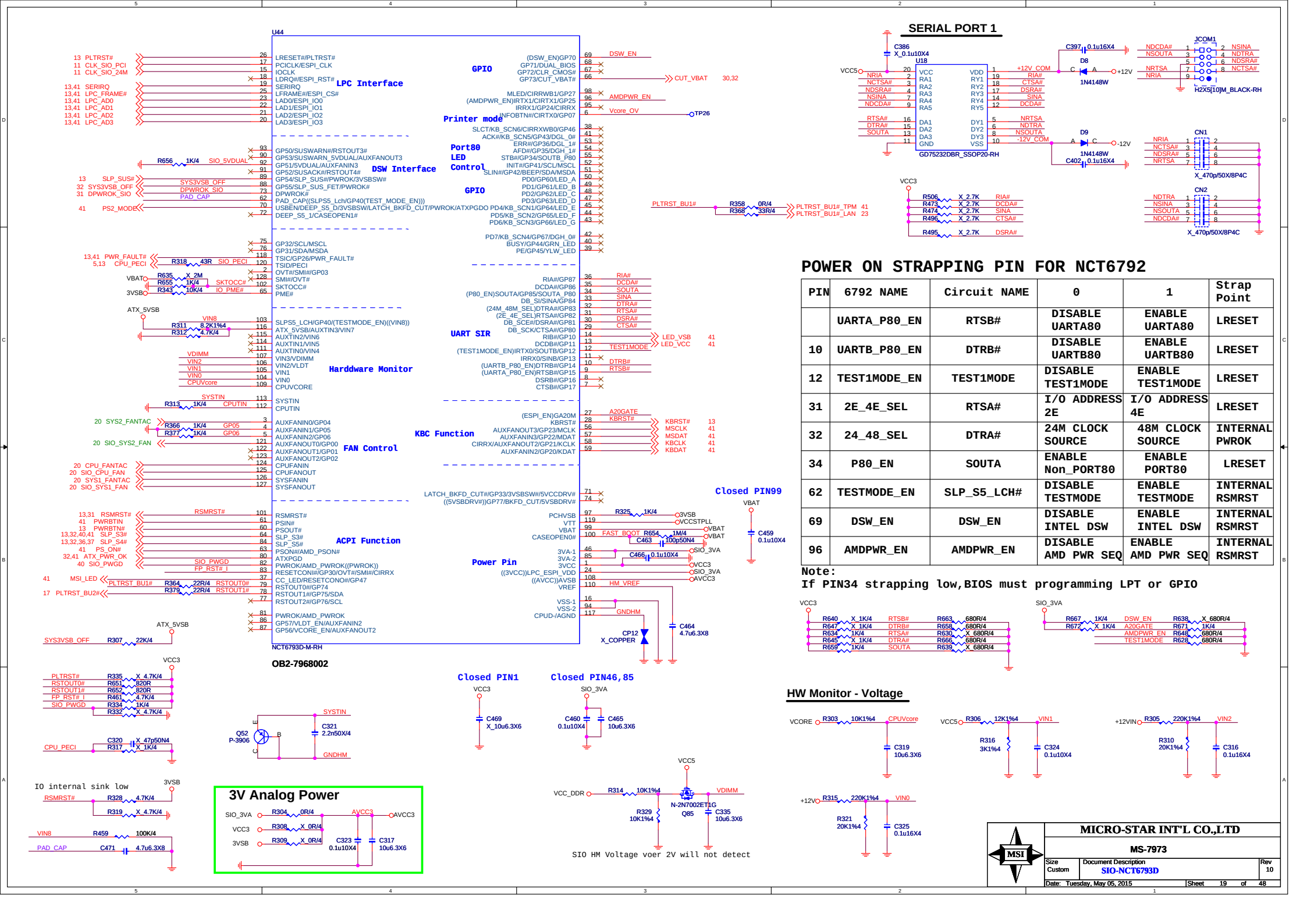
N11-0360381-L06

MICRO-STAR INT'L CO.,LTD

MS-7973

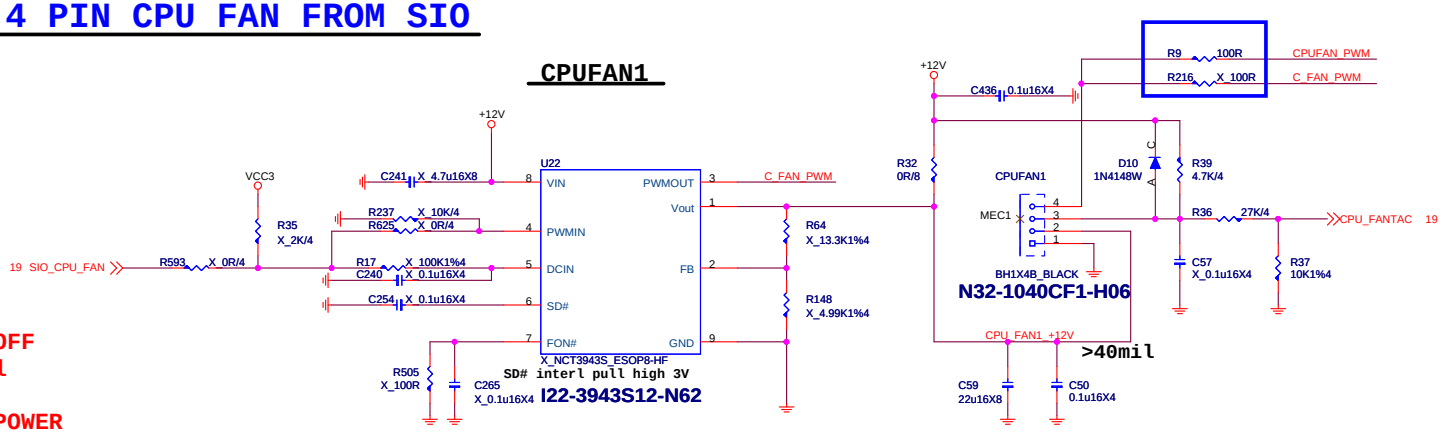
Size	Document Description	Rev
Custom	PCIE SLOT-PCH(X1)	10

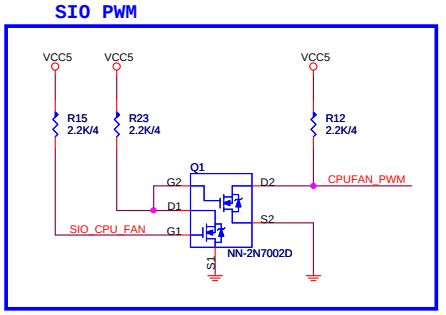
Date: Thursday, May 07, 2015 Sheet 18 of 48



PIN	6792 NAME	Circuit NAME	0	1	Strap Point
	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

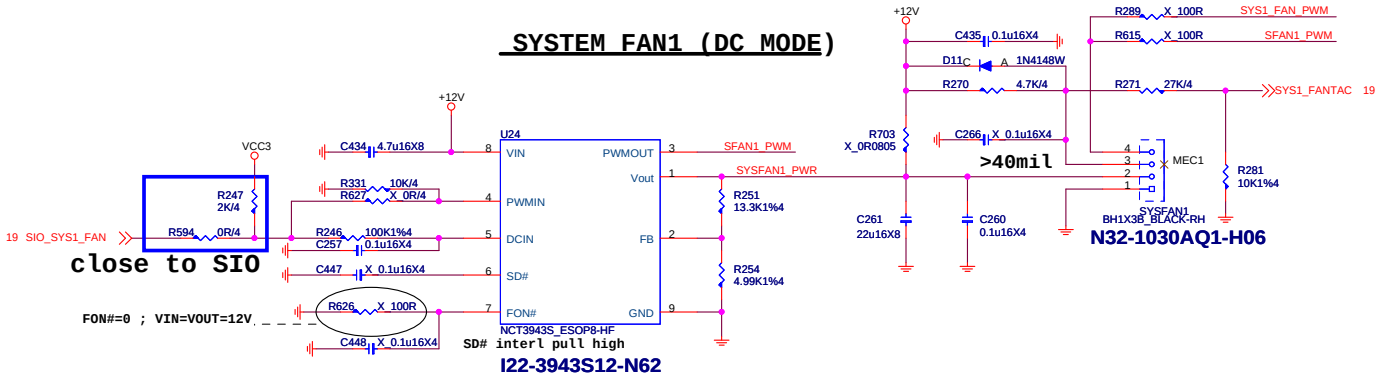
Type G : 4 PIN CPU FAN FROM SIO

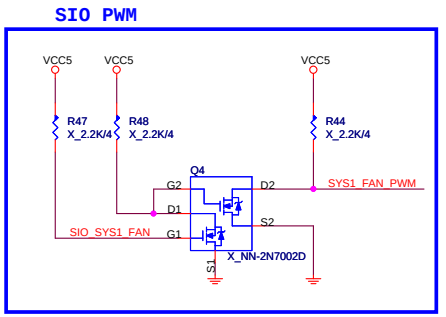


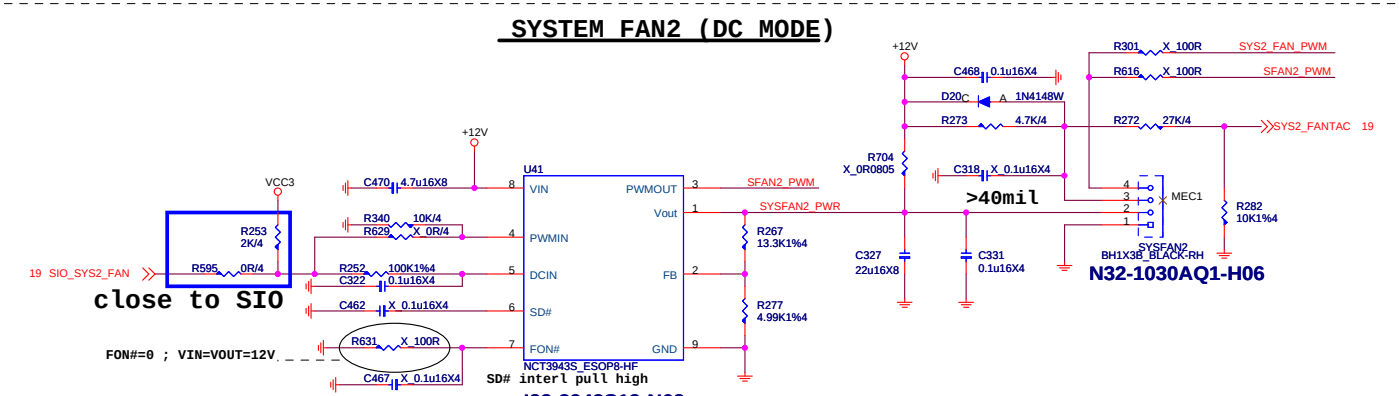


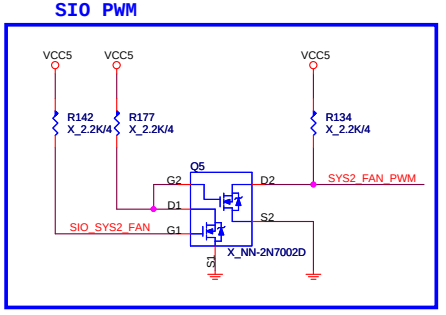
CPUFAN_PWR_OFF
GPIO Control
Deafult GPI
If USE CUT POWER
1.OPEN DRAIN LOW:SD# LOW Active，CPUFAN(PIN2)= 0V
2.OPEN DRAIN : SD# Internal Pull high，CPUFAN(PIN2)=12V

Type H : 4 PIN SYS FAN FROM SIO









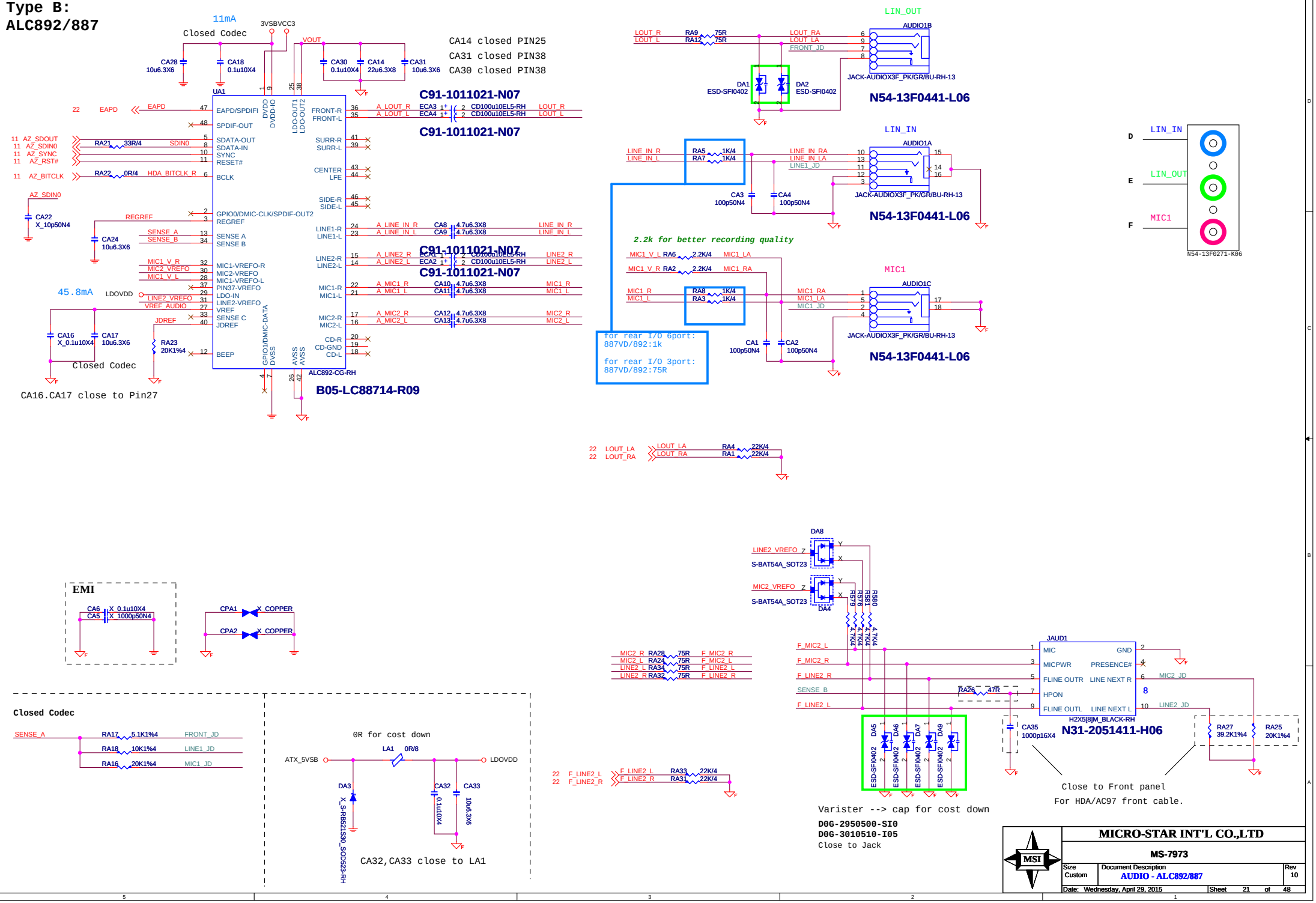
MICRO-STAR INT'L CO.,LTD

MS-7973

Size	Document Description	Rev
Custom	FAN CONTROLLOR	10

Date: Tuesday, May 05, 2015 Sheet 20 of 48

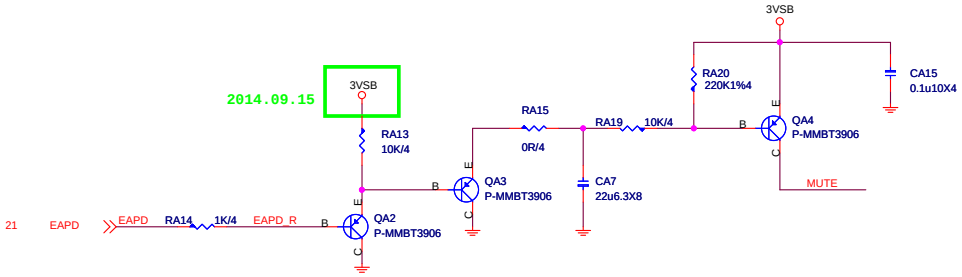
Type B: ALC892/887



MICRO-STAR INT'L CO.,LTD	
MS-7973	
Size: Custom	Document Description: AUDIO - ALC892/887
Rev: 10	
Date: Wednesday, April 29, 2015	Sheet 21 of 48

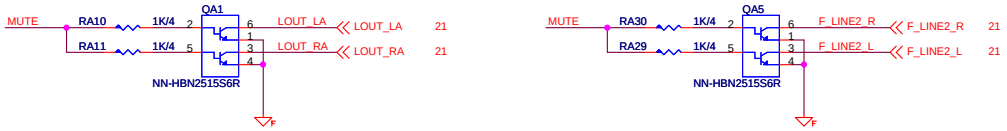
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



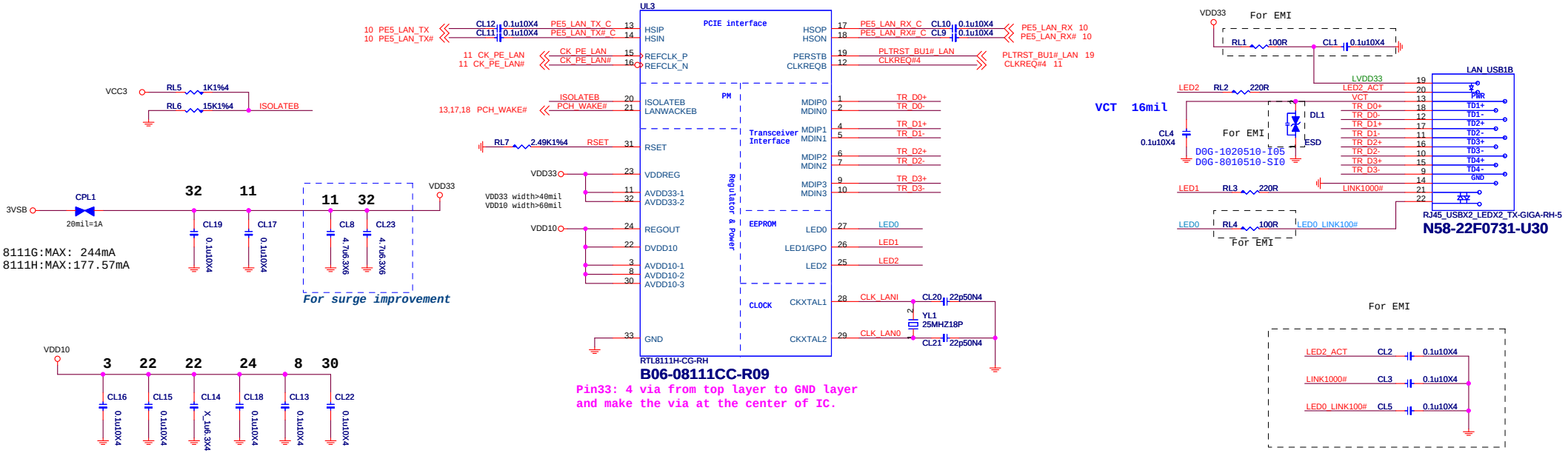
History:

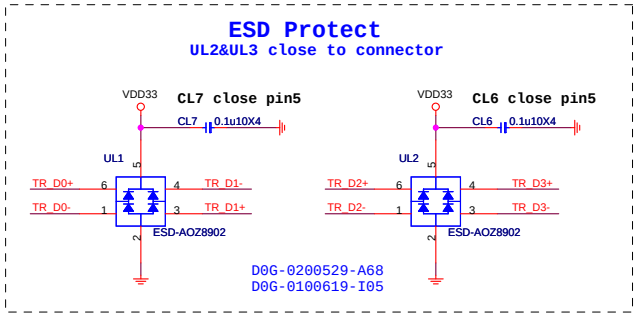
2014/02/13: stuff de-pop circuit of Line out & HP out.

MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: AUDIO - depop circuit	Rev: 10
Date: Tuesday, April 21, 2015	Sheet 22 of 48	

RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09





8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MICRO-STAR INT'L CO.,LTD

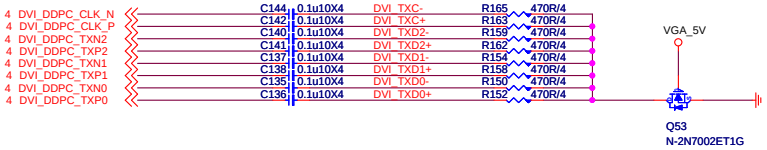
MS-7973

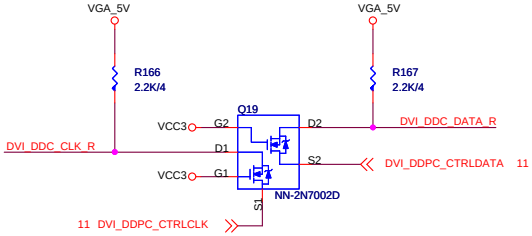
Size: Custom | Document Description: LAN - RTL8111H | Rev: 10

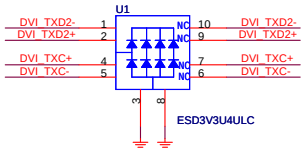
Date: Thursday, May 07, 2015 | Sheet 23 of 48

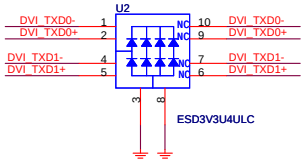
DVI level shifter

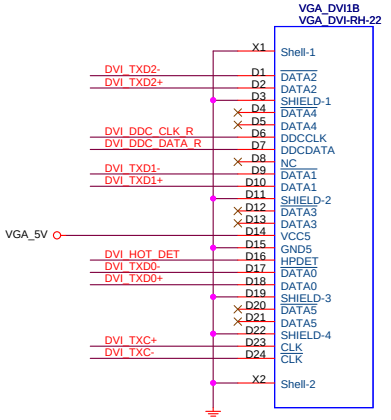
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



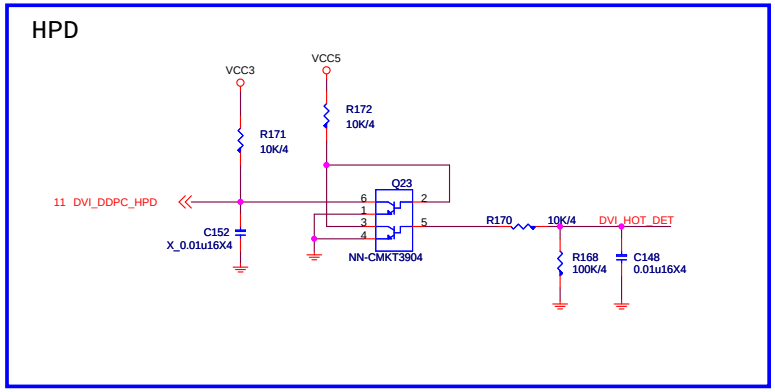


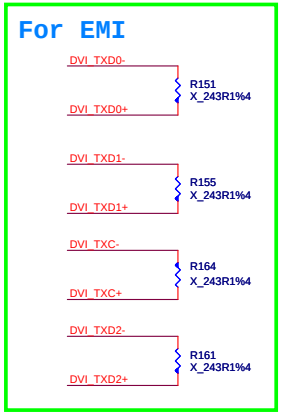


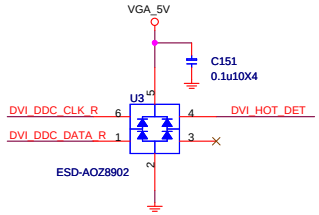


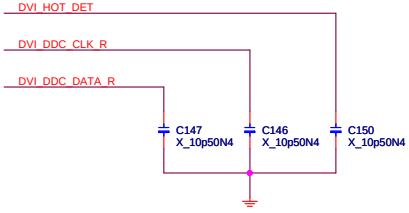


N58-39F0281-EB6



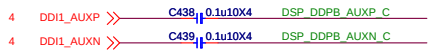


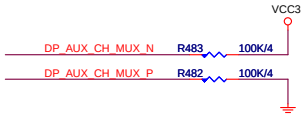


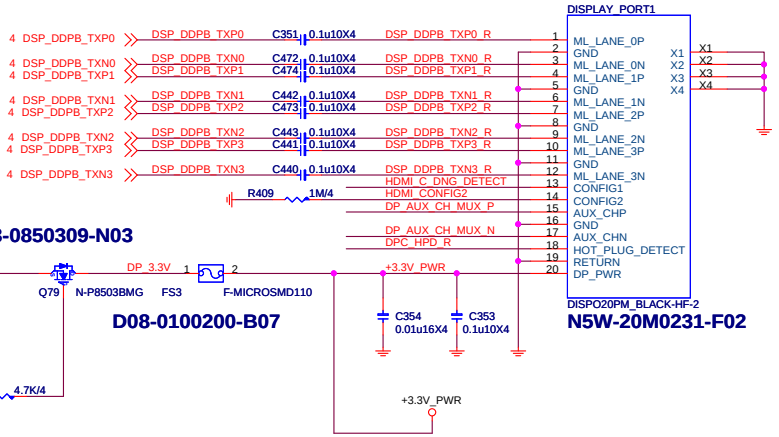


MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: DVI	Rev: 10
Date: Tuesday, April 21, 2015	Sheet 24 of 48	

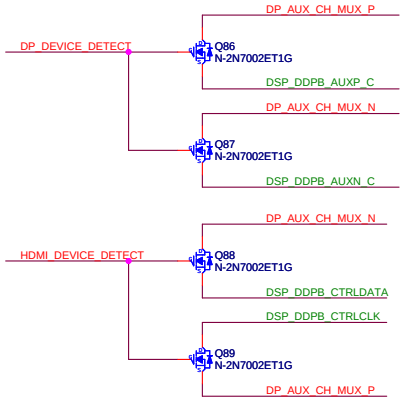
DISPLAY PORT





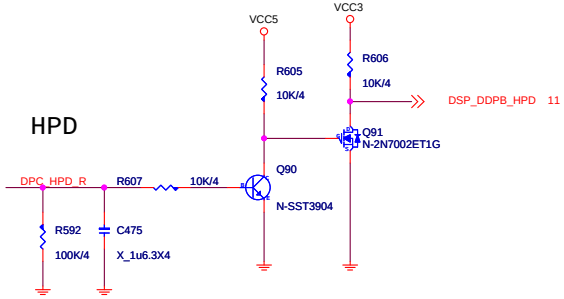


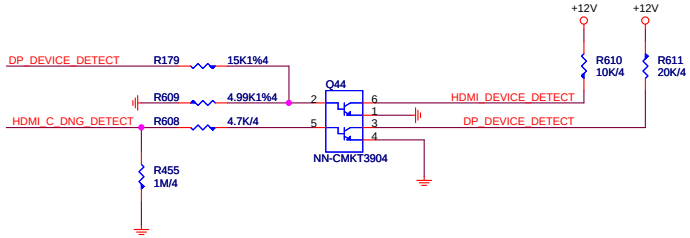
D03-7002E89-O05

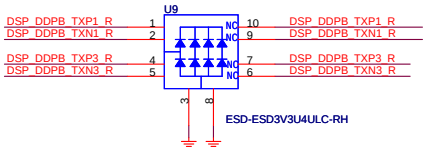


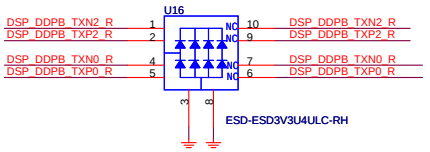
	DP	HDMI
HDMI_C_DNG_DETECT	L	H
DP_DEVICE_DETECT	H	L
HDMI_DEVICE_DETECT	L	H

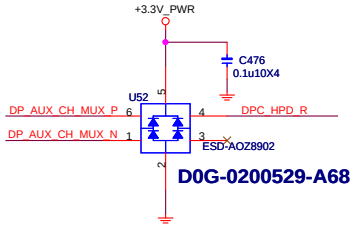
HPD







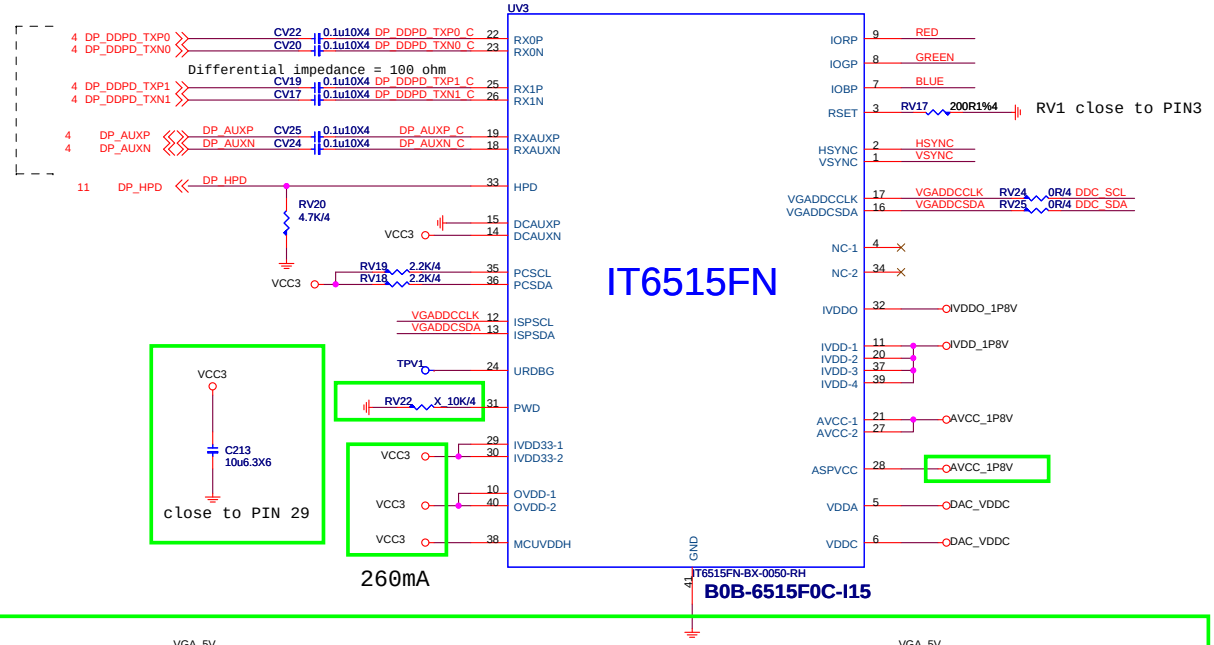




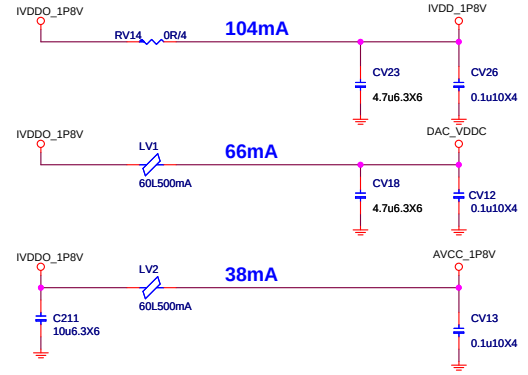
MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7973		
Size: Custom	Document Description: HDMI Connector		Rev: 10
Date: Thursday, May 07, 2015		Sheet 25 of 48	

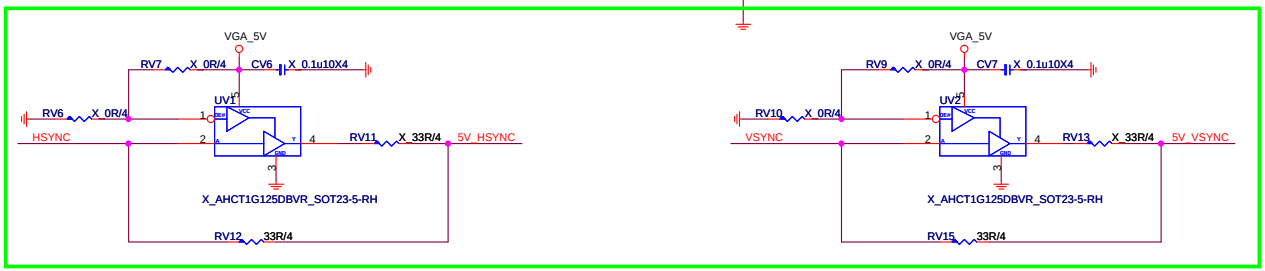
Note:

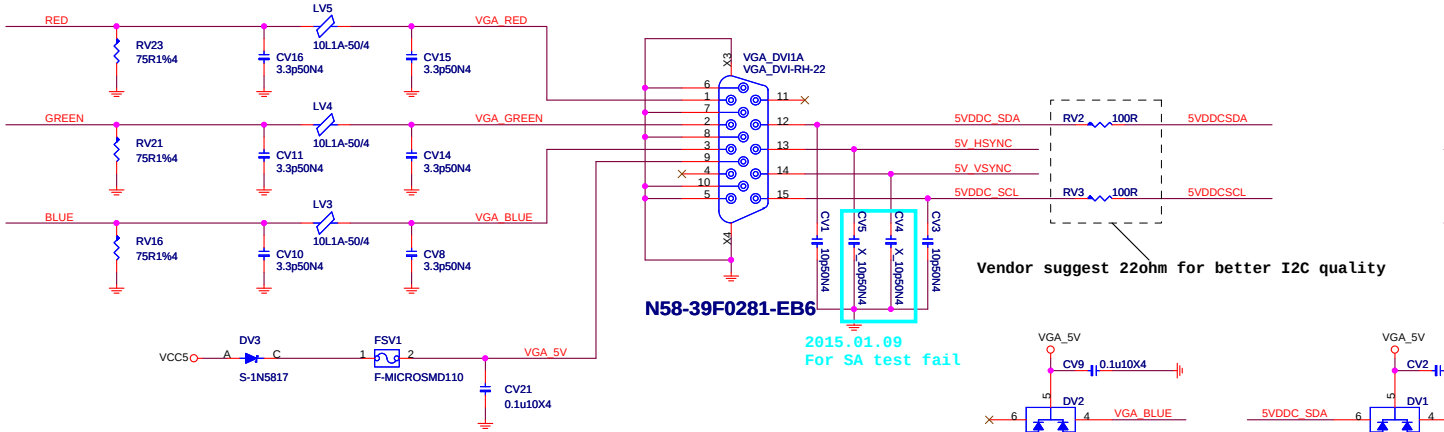
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

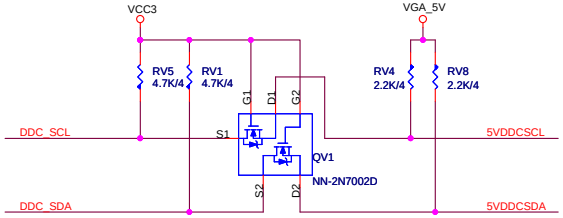


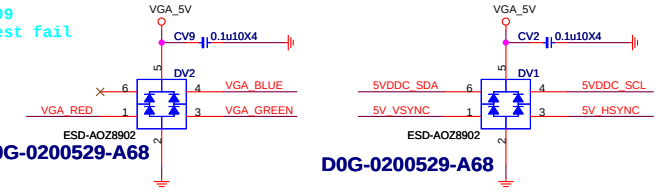
Remove





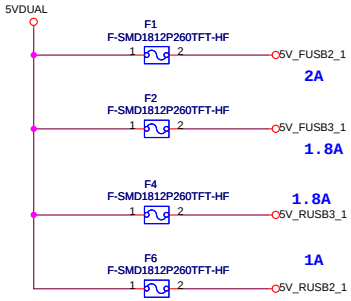


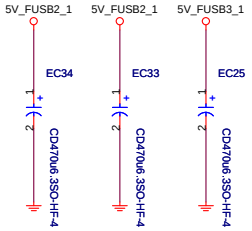


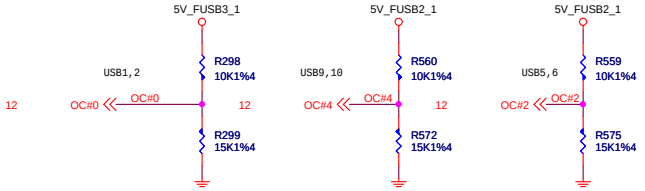


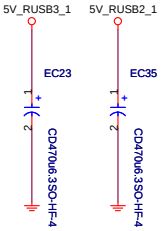
MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: VGA - ITE6515	Rev: 10
Date: Thursday, April 30, 2015	Sheet 26 of 48	

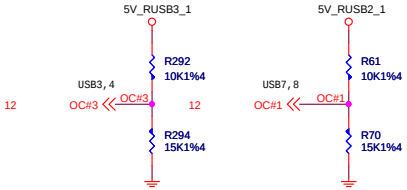
D08-0300700-P16 (Itrip=2.6A; 0.015ohm)



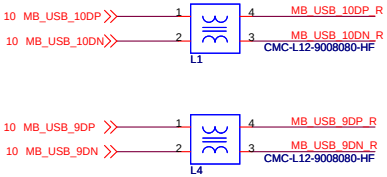


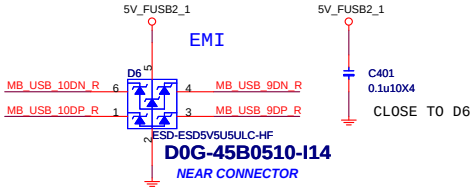






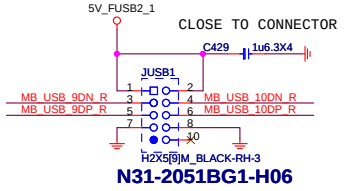
FRONT USB PORT 9,10





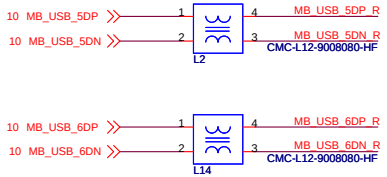
D0G-45B0510-I14

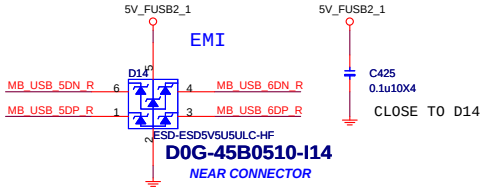
NEAR CONNECTOR



N31-2051BG1-H06

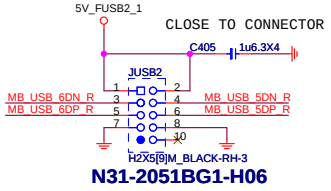
FRONT USB PORT 5,6





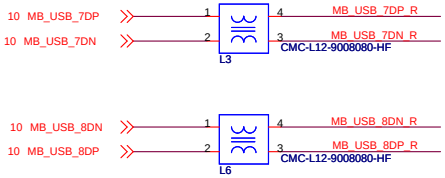
D0G-45B0510-I14

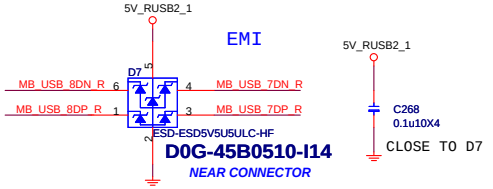
NEAR CONNECTOR



N31-2051BG1-H06

REAR USB PORT 7,8 (With LAN)





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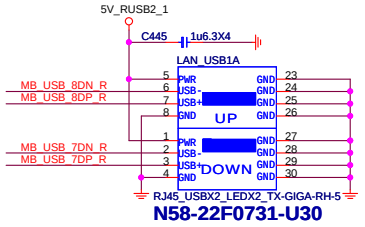
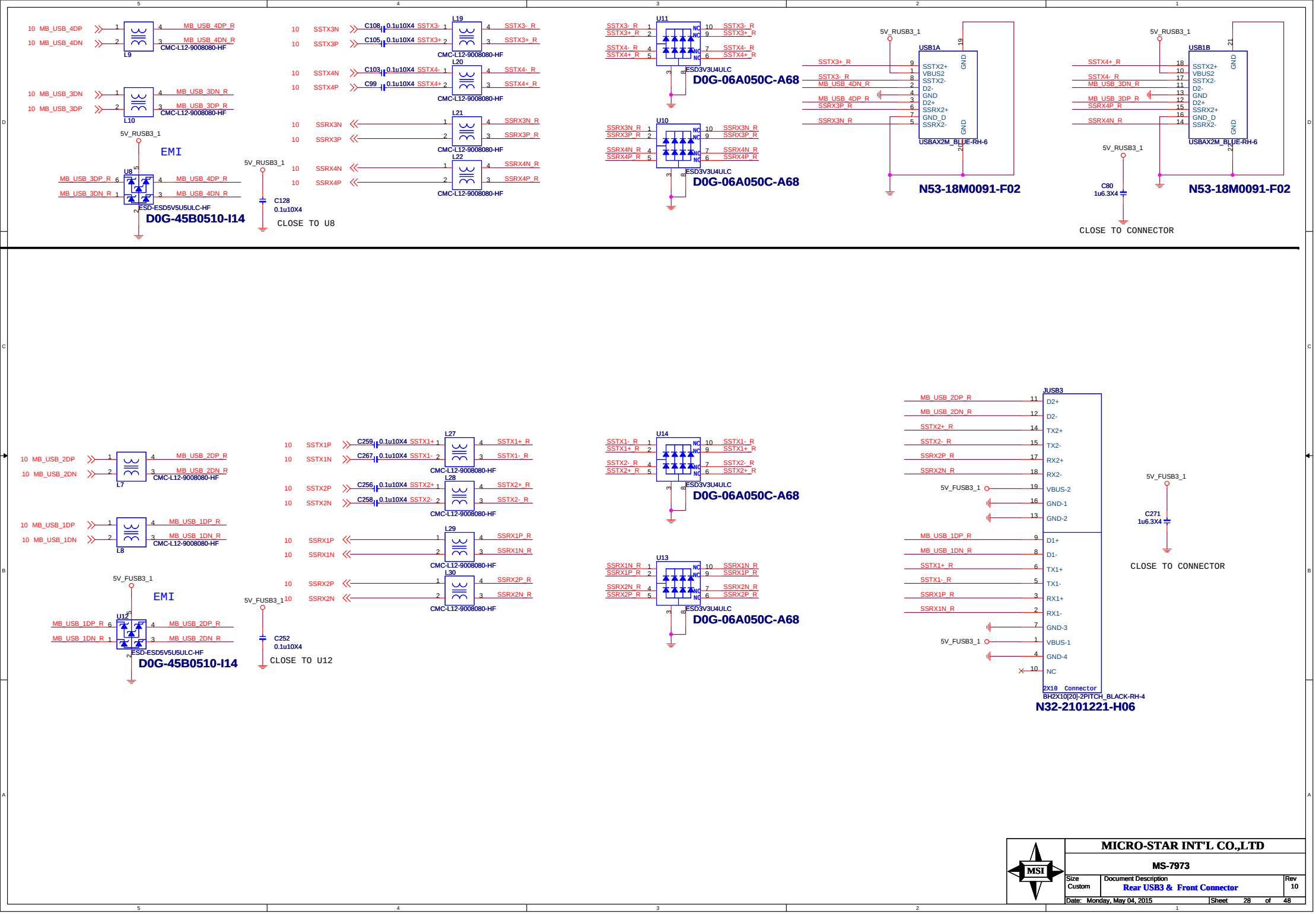
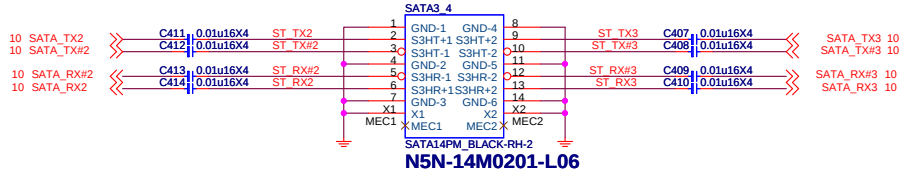
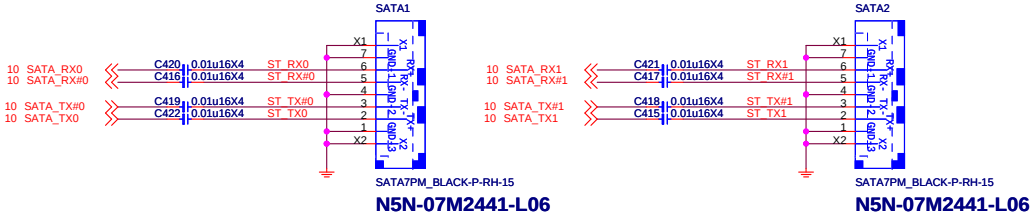


N58-22F0731-U30

MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: USB2.0 Connector	Rev: 10
Date: Monday, May 04, 2015	Sheet 27 of 48	

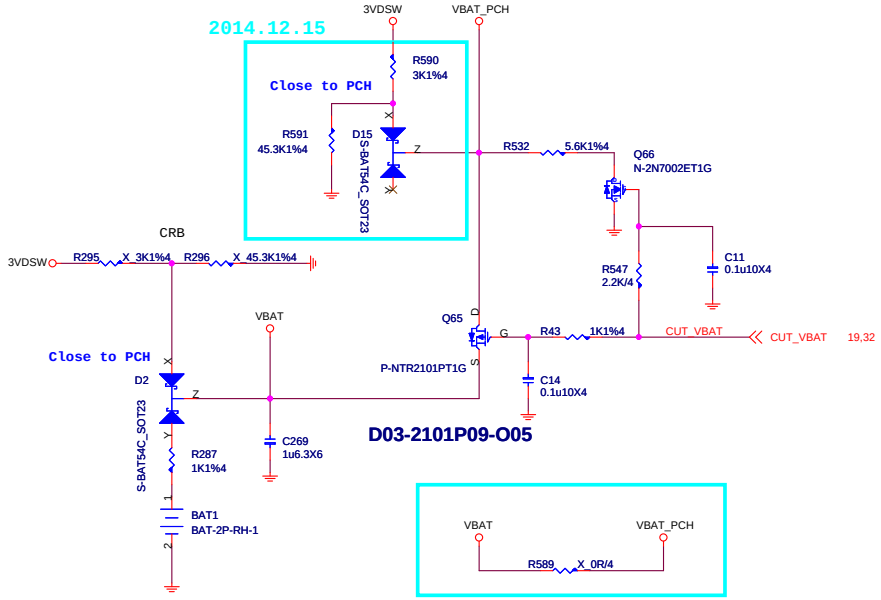

10 MB_USB_4DP
10 MB_USB_4DN
L9
MB_USB_4DP_R
MB_USB_4DN_R
CMC-L12-9008080-HF
10 MB_USB_3DN
10 MB_USB_3DP
L10
MB_USB_3DN_R
MB_USB_3DP_R
5V_RUSB3_1
EMI
U8
MB_USB_3DP_R
MB_USB_3DN_R
MB_USB_4DP_R
MB_USB_4DN_R
ESD-ESD5V5U5ULC-HF
D0G-45B0510-I14
C128
0.1u10X4
CLOSE TO U8
10 SSTX3N
10 SSTX3P
C108 0.1u10X4 SSTX3-
C105 0.1u10X4 SSTX3+
L19
SSTX3-_R
SSTX3+_R
10 SSTX4N
10 SSTX4P
C103 0.1u10X4 SSTX4-
C99 0.1u10X4 SSTX4+
L20
SSTX4-_R
SSTX4+_R
10 SSRX3N
10 SSRX3P
L21
SSRX3N_R
SSRX3P_R
10 SSRX4N
10 SSRX4P
L22
SSRX4N_R
SSRX4P_R
U11
SSTX3-_R
SSTX3+_R
SSTX4-_R
SSTX4+_R
ESD3V3U4ULC
D0G-06A050C-A68
U10
SSRX3N_R
SSRX3P_R
SSRX4N_R
SSRX4P_R
ESD3V3U4ULC
D0G-06A050C-A68
5V_RUSB3_1
USB1A
SSTX3+_R
SSTX3-_R
MB_USB_4DN_R
MB_USB_4DP_R
SSRX3P_R
SSRX3N_R
SSTX2+
VBUS2
SSTX2-
D2-
GND
D2+
SSRX2+
GND_D
SSRX2-
GND
USBAX2M_BLUE-RH-6
N53-18M0091-F02
5V_RUSB3_1
USB1B
SSTX4+_R
SSTX4-_R
MB_USB_3DN_R
MB_USB_3DP_R
SSRX4P_R
SSRX4N_R
SSTX2+
VBUS2
SSTX2-
D2-
GND
D2+
SSRX2+
GND_D
SSRX2-
GND
USBAX2M_BLUE-RH-6
N53-18M0091-F02
5V_RUSB3_1
C80
1u6.3X4
CLOSE TO CONNECTOR
10 MB_USB_2DP
10 MB_USB_2DN
L7
MB_USB_2DP_R
MB_USB_2DN_R
CMC-L12-9008080-HF
10 MB_USB_1DP
10 MB_USB_1DN
L8
MB_USB_1DP_R
MB_USB_1DN_R
5V_FUSB3_1
EMI
U12
MB_USB_1DP_R
MB_USB_1DN_R
MB_USB_2DP_R
MB_USB_2DN_R
ESD-ESD5V5U5ULC-HF
D0G-45B0510-I14
C252
0.1u10X4
CLOSE TO U12
10 SSTX1P
10 SSTX1N
C259 0.1u10X4 SSTX1+
C267 0.1u10X4 SSTX1-
L27
SSTX1+_R
SSTX1-_R
10 SSTX2P
10 SSTX2N
C256 0.1u10X4 SSTX2+
C258 0.1u10X4 SSTX2-
L28
SSTX2+_R
SSTX2-_R
10 SSRX1P
10 SSRX1N
L29
SSRX1P_R
SSRX1N_R
10 SSRX2P
10 SSRX2N
L30
SSRX2P_R
SSRX2N_R
U14
SSTX1-_R
SSTX1+_R
SSTX2-_R
SSTX2+_R
ESD3V3U4ULC
D0G-06A050C-A68
U13
SSRX1N_R
SSRX1P_R
SSRX2N_R
SSRX2P_R
ESD3V3U4ULC
D0G-06A050C-A68
JUSB3
MB_USB_2DP_R
MB_USB_2DN_R
SSTX2+_R
SSTX2-_R
SSRX2P_R
SSRX2N_R
5V_FUSB3_1
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS-2
GND-1
GND-2
MB_USB_1DP_R
MB_USB_1DN_R
SSTX1+_R
SSTX1-_R
SSRX1P_R
SSRX1N_R
5V_FUSB3_1
D1+
D1-
TX1+
TX1-
RX1+
RX1-
GND-3
VBUS-1
GND-4
NC
2X10 Connector
BH2X10[20]-2PITCH_BLACK-RH-4
N32-2101221-H06
5V_FUSB3_1
C271
1u6.3X4
CLOSE TO CONNECTOR
MICRO-STAR INT'L CO.,LTD
MS-7973
Size
Custom
Document Description
Rear USB3 & Front Connector
Rev
10
Date: Monday, May 04, 2015
Sheet 28 of 48



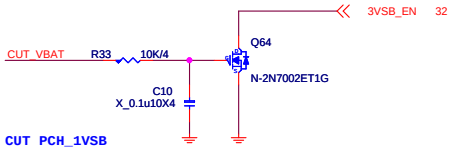


MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: SATA connector	Rev: 10
Date: Tuesday, April 28, 2015	Sheet 29 of 48	

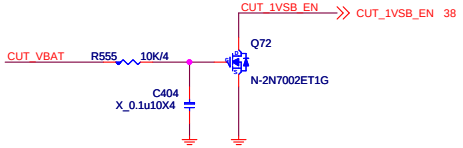
CUT_VBAT



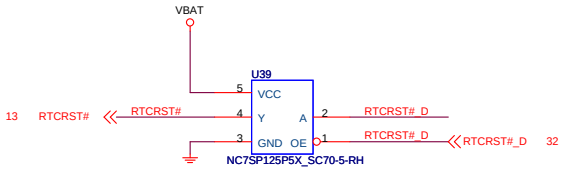
CUT 3VSB

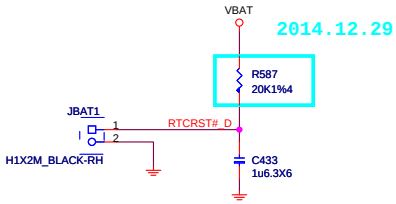


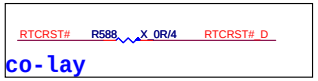
CUT PCH_1VSB



tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z







MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: CUT_VABT circuit	Rev: 10
Date: Tuesday, April 21, 2015	Sheet 30 of 48	

13 PCH_SPI0_MOSI — PCH_SPI0_MOSI
13 PCH_SPI0_MISO — PCH_SPI0_MISO
13 PCH_SPI0_CLK — PCH_SPI0_CLK
13 PCH_SPI0_CS0# — PCH_SPI0_CS0#
13 PCH_SPI0_IO2 — PCH_SPI0_IO2
13 PCH_SPI0_IO3 — PCH_SPI0_IO3

SPI CS# < 25pF
D0G-0402510-SI0

2014.08.25
Close to JSPI1

3VSB
C399 0.1u10X4
JSPI1
PCH_SPI0_MISO
PCH_SPI0_CS0#
SPI_SW_SEL
PCH_SPI0_IO2
PCH_SPI0_MOSI
PCH_SPI0_CLK
PCH_SPI0_IO3
H2X6[10]M-2PITCH_BLACK-RH-1

ATX_5VSB
R548 10K/4
SPI_SW_SEL
R585 X_1K/4
Q67 X_N-AO3414
R493 0R/4

D3 X_ESD-SFI0402
D4 ESD-SFI0402

For TL624-1.1 : Stuff D4
Old : Only RSVD (Because 12V level)

13,19 RSMRST# — D18 S-RB751V-40_SOD323-RH
13,40 SYS_PWROK — D17 S-RB751V-40_SOD323-RH
PCH_DPWROK — D16 X_S-RB751V-40_SOD323-RH
D01-RB751V0-W12
D01-RB751V0-W12
D01-RB751V0-W12

For TL624-1.1 : Stuff R493
Old : Don't stuff R493

2014.12.15
3VSB
PCH_SPI0_MISO R551 X_1K/4
PCH_SPI0_MOSI R583 X_1K/4

3VSB
R494 X_2.2K/4
For TL624-1.1 : Stuff R494
Old : Don't stuff R494

3VSB
C387 0.1u10X4
C392 10u6.3X6

2015.01.15
3VSB
R514 1K/4
R537 X_1K/4

SPI1
CS — VCC
DO(IO1) — HOLD(IO3)
WP(IO2) — CLK
GND — DI(IO0)
KH25L6473EM2I-10G-HF
M31-25L6462-K95

SPI0_CS0#
PCH_SPI0_MISO R508 15R/4 SPI0_MISO
PCH_SPI0_IO2 R517 15R/4 SPI0_IO2
R534 1K/4
SPI0_IO3 R513 15R/4 PCH_SPI0_IO3
SPI0_CLK R536 15R/4 PCH_SPI0_CLK
SPI0_MOSI R535 15R/4 PCH_SPI0_MOSI

2014.09.24 For intel MOW36 update
pull down resistor on SPI0_IO3 is needed for SKL S/H platforms with pre-ES1/ES1 samples.

20150115
update this issue for PRE-ES2/ES2 refer mail 20150115 From synge

For TL624-1.1 (SKYLAKE)
In skylake,PCH core is powered by VSB which need sink RSMRST# to low by SPI_SW_SEL.

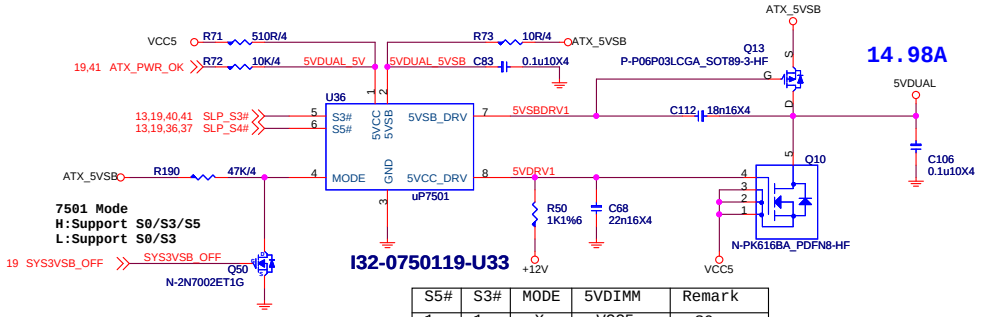
* if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002
* if you support Standby power in S5 Status(Ex; PCH is B75 Chipset) , component Q14.G Pull-high to ATX_5VSB , Q14 must select "Vth" under 1V (Component Suggestion as below)

D03-0341409-A68 / D03-0230019-A30

SIO_3VA
R24 4.7K1%4
R341 100K1%4
3VDSW
R336 X_4.7K1%4
R349 X_100K1%4
19 DPWROK_SIO — R342 0R/4 — PCH_DPWROK — PCH_DPWROK 13

MICRO-STAR INT'L CO.,LTD
MS-7973
Size: Custom
Document Description: BIOS ROM
Rev: 10
Date: Tuesday, April 21, 2015
Sheet 31 of 48

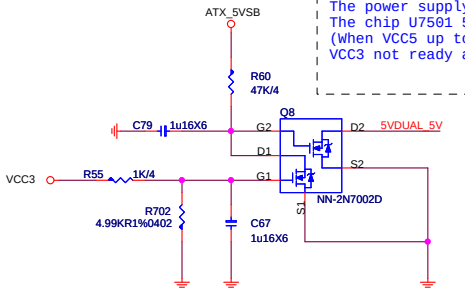
5VDUAL



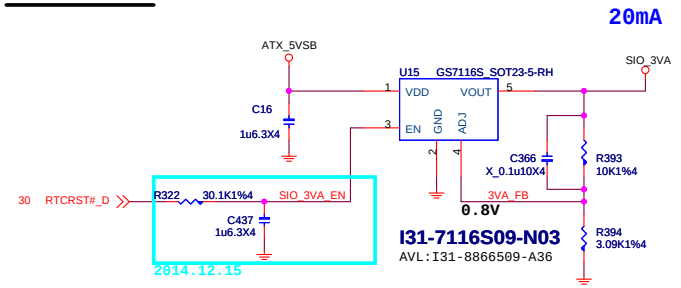
S5#	S3#	MODE	5VDIMM	Remark
1	1	X	VCC5	S0
1	0	X	5VSB	S3
0	X	1	5VSB	S4/S5
0	X	0	Shutdown	S4/S5

SYS3VSB_OFF (DSW POWER CONTROL)
default is set to 1 to cut off the standby power
DSW S5 (HIGH): USB no power
S5 (LOW): USB have power

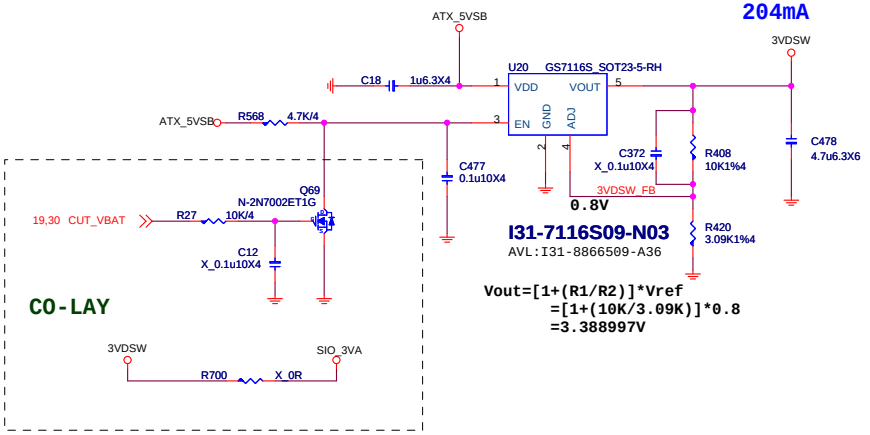
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



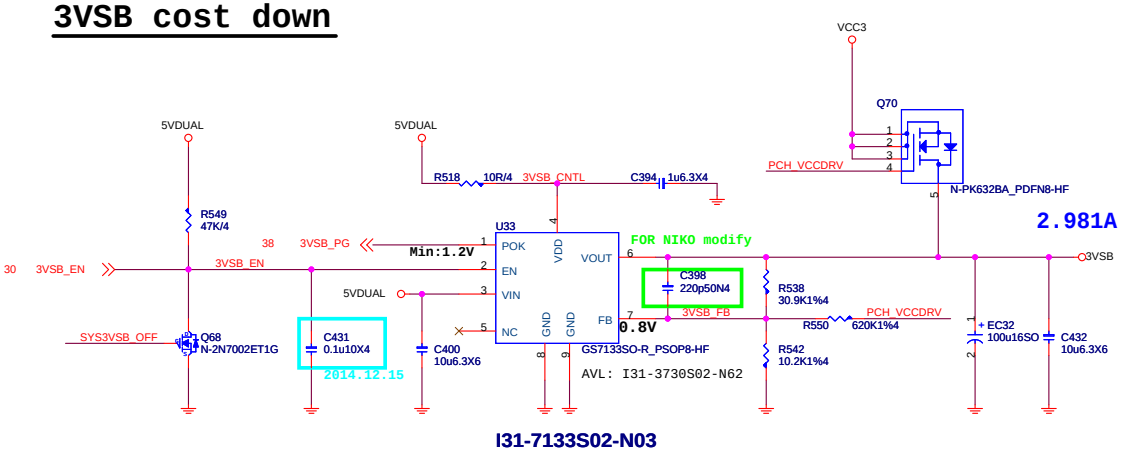
SIO_3VA



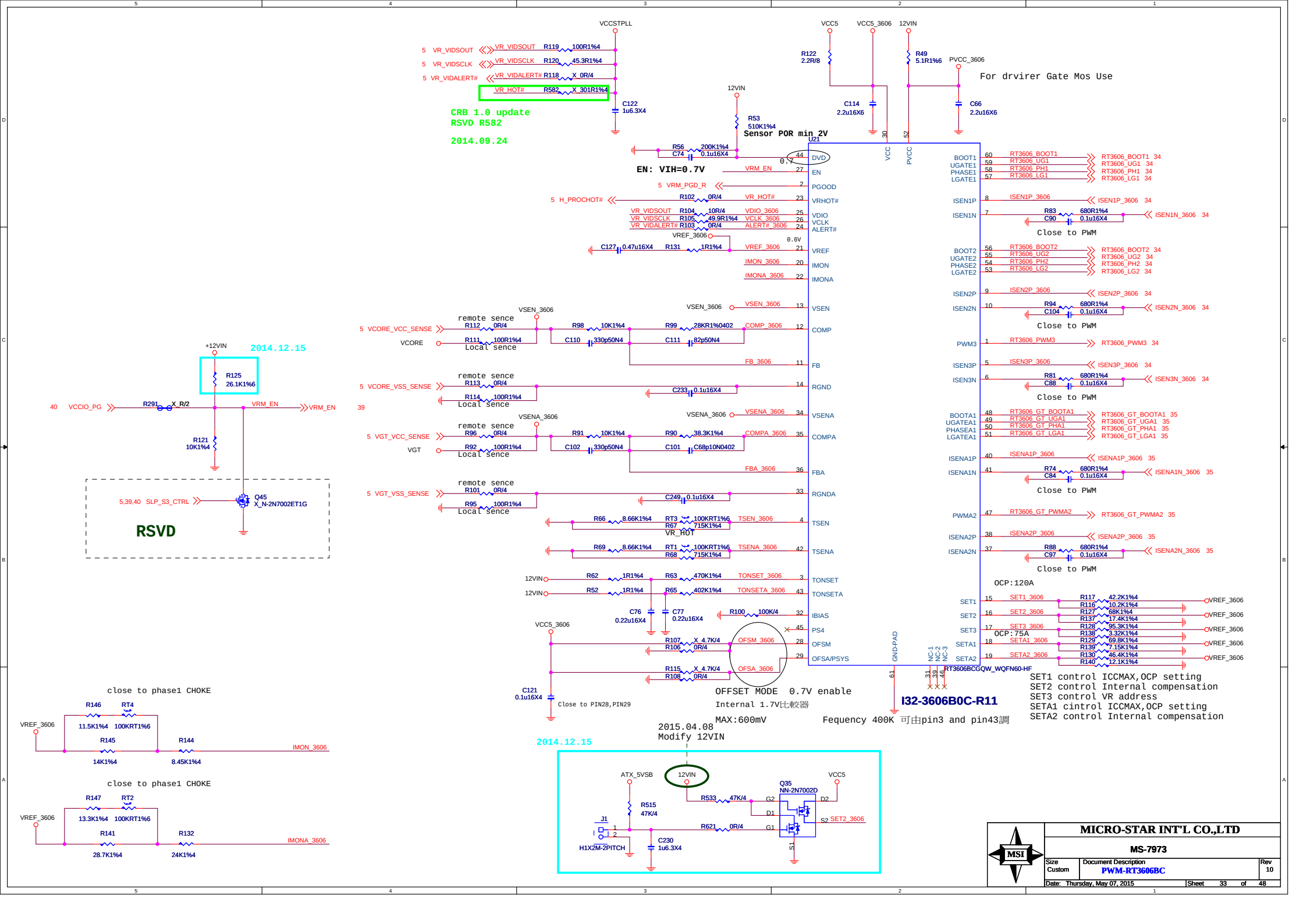
3VDSW

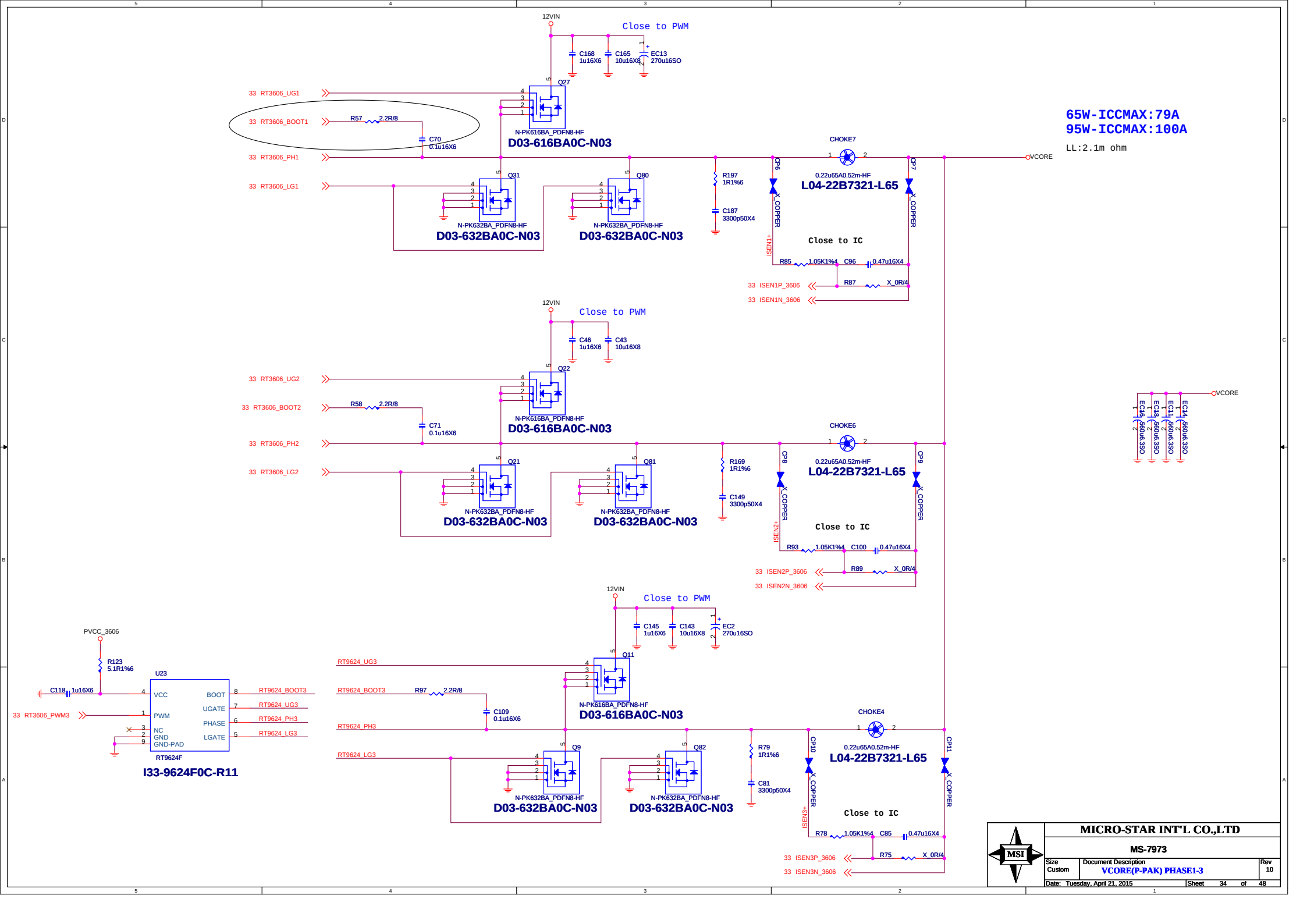


3VSB cost down



MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: ACPI CONTROLLER	Rev: 10
Date: Thursday, May 07, 2015	Sheet 32 of 48	


VCCSTPLL
VR_VIDSOUT R119 100R1%4
VR_VIDSCLK R120 45.3R1%4
VR_VIDALERT# R118 X_0R/4
VR_HOT# R582 X_301R1%4
C122 1u6.3X4
CRB 1.0 update
RSVD R582
2014.09.24
12VIN
R53 510K1%4
Sensor POR min_2V
VCC5
VCC5_3606
12VIN
R122 2.2R/8
C114 2.2u16X6
R49 5.1R1%6
PVCC_3606
C66 2.2u16X6
For drvirer Gate Mos Use
U21
R56 200K1%4
C74 0.1u16X4
EN: VIH=0.7V
VRM_EN
VR_HOT#
VDIO_3606
VCLK_3606
ALERT#_3606
VREF_3606
C127 0.47u16X4
R131 1R1%4
IMON_3606
IMONA_3606
DVD
EN
PGOOD
VRHOT#
VDIO
VCLK
ALERT#
VREF
IMON
IMONA
VSEN_3606
R112 0R/4
R111 100R1%4
Local sence
R98 10K1%4
C110 330p50N4
R99 28KR1%0402
C111 82p50N4
COMP_3606
FB_3606
VSEN
COMP
FB
remote sence
R113 0R/4
R114 100R1%4
C233 0.1u16X4
RGND
VSENA_3606
R96 0R/4
R92 100R1%4
R91 10K1%4
C102 330p50N4
R90 38.3K1%4
C101 C68p10N0402
COMPA_3606
FBA_3606
VSENA
COMPA
FBA
R101 0R/4
R95 100R1%4
C249 0.1u16X4
RGNDA
R66 8.66K1%4
R67 715K1%4
RT3 100KRT1%6
TSEN_3606
R69 8.66K1%4
R68 715K1%4
RT1 100KRT1%6
TSENA_3606
TSEN
TSENA
R62 1R1%4
R63 470K1%4
TONSET_3606
R52 1R1%4
R65 402K1%4
TONSETA_3606
TONSET
TONSETA
C76 0.22u16X4
C77 0.22u16X4
R100 100K/4
IBIAS
PS4
R107 X_4.7K/4
R106 0R/4
OFSM_3606
OFSM
R115 X_4.7K/4
R108 0R/4
OFSA_3606
OFSA/PSYS
C121 0.1u16X4
Close to PIN28,PIN29
OFFSET MODE 0.7V enable
Internal 1.7V比較器
MAX:600mV
Fequency 400K 可由pin3 and pin43調
I32-3606B0C-R11
RT3606BCGQW_WQFN60-HF
GND-PAD
BOOT1 RT3606_BOOT1
UGATE1 RT3606_UG1
PHASE1 RT3606_PH1
LGATE1 RT3606_LG1
ISEN1P ISEN1P_3606
ISEN1N R83 680R1%4 C90 0.1u16X4 ISEN1N_3606
Close to PWM
BOOT2 RT3606_BOOT2
UGATE2 RT3606_UG2
PHASE2 RT3606_PH2
LGATE2 RT3606_LG2
ISEN2P ISEN2P_3606
ISEN2N R94 680R1%4 C104 0.1u16X4 ISEN2N_3606
PWM3 RT3606_PWM3
ISEN3P ISEN3P_3606
ISEN3N R81 680R1%4 C88 0.1u16X4 ISEN3N_3606
BOOTA1 RT3606_GT_BOOTA1
UGATEA1 RT3606_GT_UGA1
PHASEA1 RT3606_GT_PHA1
LGATEA1 RT3606_GT_LGA1
ISENA1P ISENA1P_3606
ISENA1N R74 680R1%4 C84 0.1u16X4 ISENA1N_3606
PWMA2 RT3606_GT_PWMA2
ISENA2P ISENA2P_3606
ISENA2N R88 680R1%4 C97 0.1u16X4 ISENA2N_3606
OCP:120A
OCP:75A
SET1 SET1_3606 R117 42.2K1%4 R116 10.2K1%4 VREF_3606
SET2 SET2_3606 R127 68K1%4 R137 17.4K1%4 VREF_3606
SET3 SET3_3606 R128 95.3K1%4 R138 3.32K1%4 VREF_3606
SETA1 SETA1_3606 R129 69.8K1%4 R139 7.15K1%4 VREF_3606
SETA2 SETA2_3606 R130 46.4K1%4 R140 12.1K1%4 VREF_3606
SET1 control ICCMAX,OCP setting
SET2 control Internal compensation
SET3 control VR address
SETA1 cintrol ICCMAX,OCP setting
SETA2 control Internal compensation
+12VIN
2014.12.15
R125 26.1K1%6
40 VCCIO_PG
R291 X_R/2
VRM_EN
39
R121 10K1%4
5,39,40 SLP_S3_CTRL
Q45 X_N-2N7002ET1G
RSVD
close to phase1 CHOKE
VREF_3606
R146 11.5K1%4
RT4 100KRT1%6
R145 14K1%4
R144 8.45K1%4
IMON_3606
close to phase1 CHOKE
VREF_3606
R147 13.3K1%4
RT2 100KRT1%6
R141 28.7K1%4
R132 24K1%4
IMONA_3606
2015.04.08
Modify 12VIN
2014.12.15
ATX_5VSB
12VIN
VCC5
R515 47K/4
R533 47K/4
Q35 NN-2N7002D
J1
H1X2M-2PITCH
C230 1u6.3X4
R621 0R/4
SET2_3606
MICRO-STAR INT'L CO.,LTD
MS-7973
Size Custom
Document Description PWM-RT3606BC
Rev 10
Date: Thursday, May 07, 2015
Sheet 33 of 48


65W-ICCMAX:79A
95W-ICCMAX:100A
LL:2.1m ohm
12VIN
Close to PWM
C168 1u16X6
C165 10u16X8
EC13 270u16SO
Q27
33 RT3606_UG1
33 RT3606_BOOT1
R57 2.2R/8
C70 0.1u16X6
33 RT3606_PH1
33 RT3606_LG1
N-PK616BA_PDFN8-HF
D03-616BA0C-N03
Q31
Q80
N-PK632BA_PDFN8-HF
D03-632BA0C-N03
R197 1R1%6
C187 3300p50X4
CHOKE7
0.22u65A0.52m-HF
L04-22B7321-L65
CP6
CP7
X_COPPER
VCORE
ISEN1+
Close to IC
R85 1.05K1%4
C96 0.47u16X4
R87 X_0R/4
33 ISEN1P_3606
33 ISEN1N_3606
C46 1u16X6
C43 10u16X8
Q22
33 RT3606_UG2
33 RT3606_BOOT2
R58 2.2R/8
C71 0.1u16X6
33 RT3606_PH2
33 RT3606_LG2
Q21
Q81
R169 1R1%6
C149 3300p50X4
CHOKE6
CP8
CP9
ISEN2+
R93 1.05K1%4
C100 0.47u16X4
R89 X_0R/4
33 ISEN2P_3606
33 ISEN2N_3606
EC16 560u6.3SO
EC15 560u6.3SO
EC12 560u6.3SO
EC11 560u6.3SO
EC14 560u6.3SO
C145 1u16X6
C143 10u16X8
EC2 270u16SO
Q11
RT9624_UG3
RT9624_BOOT3
R97 2.2R/8
C109 0.1u16X6
RT9624_PH3
RT9624_LG3
Q9
Q82
R79 1R1%6
C81 3300p50X4
CHOKE4
CP10
CP11
ISEN3+
R78 1.05K1%4
C85 0.47u16X4
R75 X_0R/4
33 ISEN3P_3606
33 ISEN3N_3606
PVCC_3606
R123 5.1R1%6
C118 1u16X6
U23
VCC
PWM
NC
GND
GND-PAD
BOOT
UGATE
PHASE
LGATE
RT9624_BOOT3
RT9624_UG3
RT9624_PH3
RT9624_LG3
33 RT3606_PWM3
RT9624F
I33-9624F0C-R11
MICRO-STAR INT'L CO.,LTD
MS-7973
Size Custom
Document Description
VCORE(P-PAK) PHASE1-3
Rev 10
Date: Tuesday, April 21, 2015
Sheet 34 of 48

JPWR2
PWRCON4P_BLACK-RH-3
MECX
+12VIN
CHOKE1
0.22u65A0.52m-HF
12VIN
C49
0.1u16X4

EMS RESERVE

Close to JPWR2

+12VIN
C270
X_0.1u16X4
+12VIN
C305
X_0.1u16X4
+12VIN
C306
X_0.1u16X4

Close to PWM

12VIN
C55
1u16X6
C52
10u16X8
EC20
270u16SO

33 RT3606_GT_UGA1
33 RT3606_GT_BOOTA1
R59 2.2R/8
C72
0.1u16X6
33 RT3606_GT_PHA1
33 RT3606_GT_LGA1

Q2
N-PK616BA_PDFN8-HF
D03-616BA0C-N03

Q6
N-PK632BA_PDFN8-HF
D03-632BA0C-N03

Q83
N-PK632BA_PDFN8-HF
D03-632BA0C-N03

R40
1R1%6
C62
3300p50X4

CHOKE2
0.22u65A0.52m-HF
L04-22B7321-L65

CP2
X_COPPER
CP3
X_COPPER
ISENA1+

R77 1.05K1%4
C87 0.47u16X4
R80 X_0R/4

33 ISENA1P_3606
33 ISENA1N_3606

VGT

ICCMAX:45A
LL:3.1m ohm

EC9 560u6.3SO
EC9 560u6.3SO
EC8 560u6.3SO
EC7 560u6.3SO
EC10 560u6.3SO

PVCC_3606
R82
5.1R1%6
C98 1u16X6

U7
VCC
PWM
NC
GND
GND-PAD
BOOT
UGATE
PHASE
LGATE
RT9624F

33 RT3606_GT_PWMA2

RT9624_GT_BOOTA2
RT9624_GT_UGA2
RT9624_GT_PHA2
RT9624_GT_LGA2

I33-9624F0C-R11

Close to PWM

12VIN
C54
1u16X6
C51
10u16X8
EC12
270u16SO

RT9624_GT_UGA2
RT9624_GT_BOOTA2
R76 2.2R/8
C89
0.1u16X6
RT9624_GT_PHA2
RT9624_GT_LGA2

Q3
N-PK616BA_PDFN8-HF
D03-616BA0C-N03

Q7
N-PK632BA_PDFN8-HF
D03-632BA0C-N03

Q84
N-PK632BA_PDFN8-HF
D03-632BA0C-N03

R42
1R1%6
C63
3300p50X4

CHOKE3
0.22u65A0.52m-HF
L04-22B7321-L65

CP4
X_COPPER
CP5
X_COPPER
ISENA2+

R86 1.05K1%4
C91 0.47u16X4
R84 X_0R/4

33 ISENA2P_3606
33 ISENA2N_3606

VGT

MICRO-STAR INT'L CO.,LTD

MS-7973

Size	Document Description	Rev
Custom	VGT(P-PAK) PHASE1-2	10

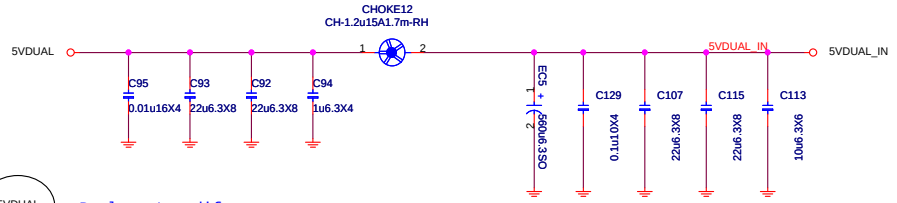
Date: Tuesday, April 28, 2015 Sheet 35 of 48

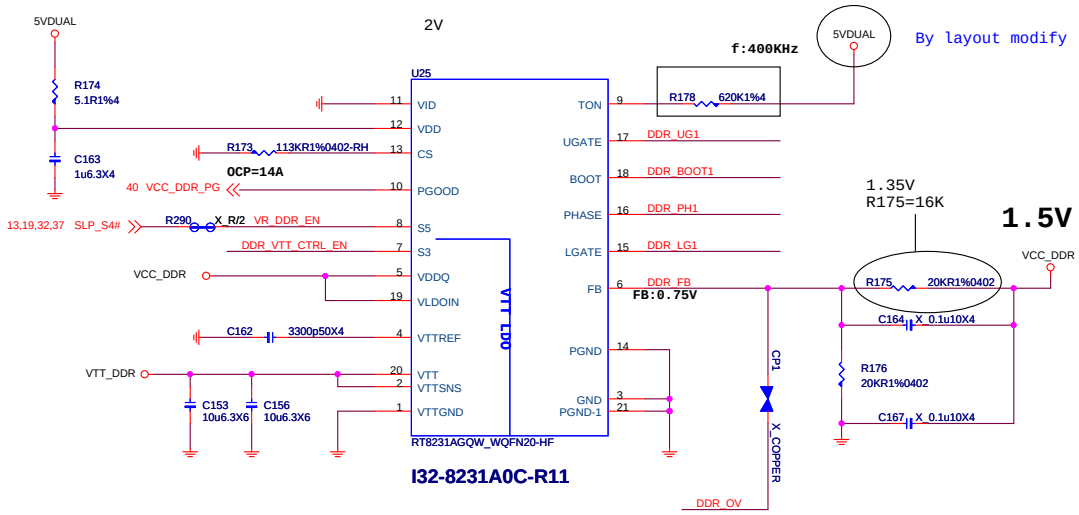
DDR Power:1.35V,9.357A

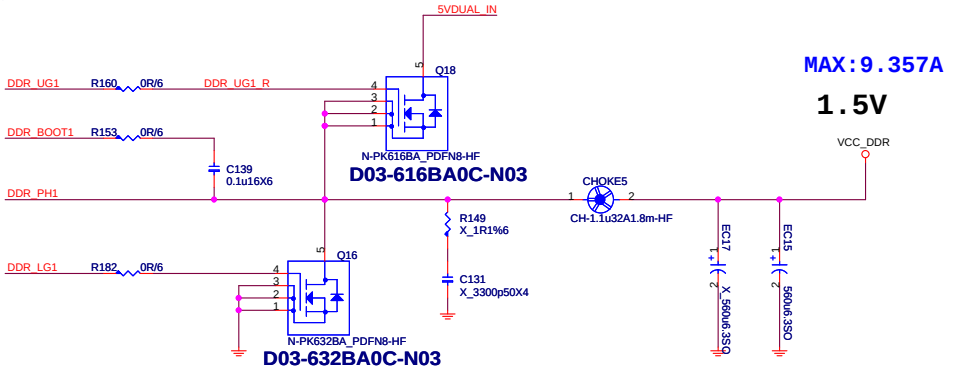
2.8A FOR CPU
6A FOR 2DIMM DDR3
0.557A FOR VTT_DDR

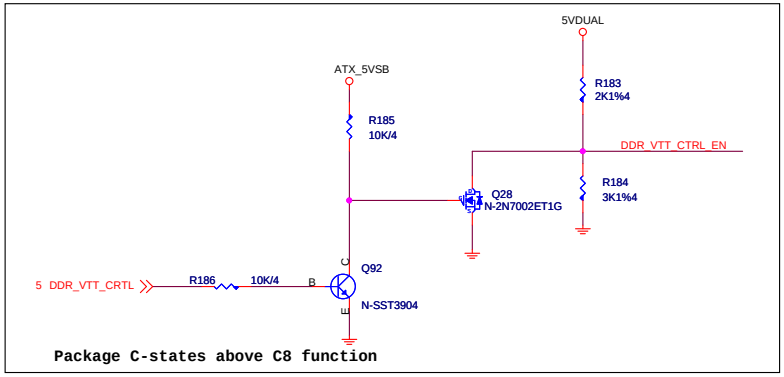
OCP =9.357A*1.5=14.0625A
Rlimit(R277)=OCP*Rdson(Low side)4.6mohm]/10uA
=14.0625*4.6mohm/10uA
=6.467Kohm

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
     = 9.357 * 0.44
     = 4.154A
```



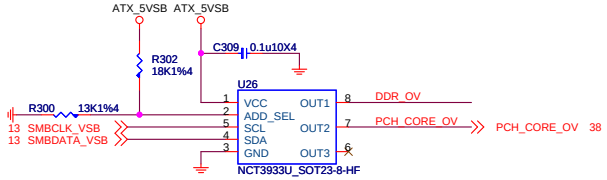


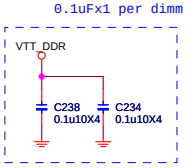




UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



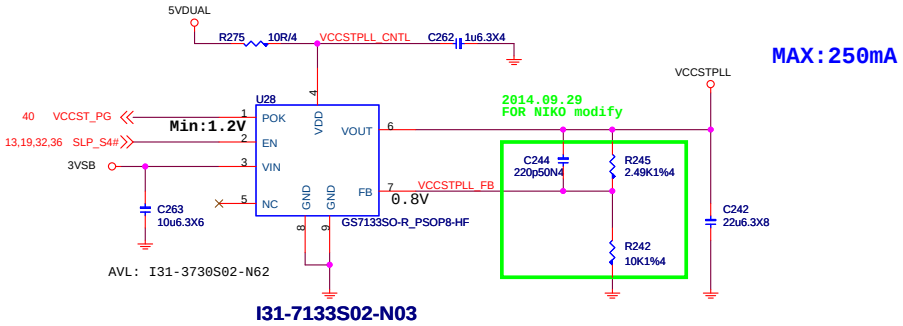


MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: DDR-RT8231AGQW	Rev: 10
Date: Friday, May 08, 2015	Sheet 36 of 48	

VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge



VCCIO ramped and stable before
beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: CPU PWR_ST/PLL	Rev: 10
Date: Thursday, May 07, 2015	Sheet 37 of 48	

PCH_1VSB

1.0V; 7.24A

OCP = 15.996A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 7.24 * 4.6mohm / 10uA
= 4.9956K

Rocs:7.87K,OCP:
D03-4C05N03-O05 : 15.74A
D03-632BA0C-N03 : 17.1A
use UBIQ MOS need Check

Rdson(low)4.5V
D03-4C05N03-O05 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

2014.08.22 close to U34

PCH_1VSB_EN
R438 X_36K1%4
C379 X_33p50N4
C373 X_3300p50X4
RSVD for up1540

2015.01.22
for up1540:stuff R438->36K,
C379->NC,C373->3.3nF
for RT8125:R438.C379.C373->NC

2015.01.22
for up1540:R96->2.2R,C84->1uF
for RT8125:R96->10R,C84->1uF

5VDUAL
R403 10R/8
C362 1u6.3X6
R180 X_10K/4 POR:4.2V
EN:2.4V

U34
RT8125CGQW
EN, PGOOD, REFOUT, REFIN, VCC, GND, BOOT, PHASE, UGATE, LGATE/OCSET, FB

PCH_BOOT R372 0R/6 PCH_R_BOOT C349 0.1u16X6
PCH_PHASE
PCH_UGATE R371 0R/6 PCH_R_UGATE
PCH_LGATE
PCH_REFOUT
PCH_REFIN

2014.12.25
for up1540:C364&R407 ->NC
C364 1000p16X4
R407 806R1%4
C365 1000p16X4
R623 0R/4
I32-8125C0C-R11

2014.12.25
for up1540:C365 is OCP set min:5Kohm
stuff 7.87K OCP SET:15.74A
RT8125C stuff C1000P C11-1022032-W08

2014.12.25
for up1540:R623 ->NC

R374 6.8K1%4
2014.12.25
for up1540:R374->NC

R375 10K/4

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

5VDUAL_PCH_IN
CHOKE11 CH-1.2u15A1.7m-RH
C333 0.1u16X4
C314 10u16X8
EC26 560u6.3SO
C307 X_0.1u10X4

Q57 N-PK616BA_PDFN8-HF
D03-616BA0C-N03
Q56 N-PK632BA_PDFN8-HF
D03-632BA0C-N03

確認 電流
CHOKE10 CH-1.2u15A1.7m-RH
R330 X_2.2R/8
C328 X_3300p50X4

MAX:7.24A

PCH_1VSB
EC31 560u6.3SO
EC30 560u6.3SO
C369 22u6.3X8
C371 10u6.3X6
C368 10u6.3X6
C360 1u6.3X4

to sink/source over voltage IC.
pin10 sink/source current capability can't over 1mA
So max voltage can't over 1.8V.
from NCT3933

36 PCH_CORE_OV
PCH_CORE_OV
36 PCH_CORE_OV

R622 X_0R/4

2014.12.25
for up1540:stuff R622->0R

PCH_CORE_FB_R
C376 X_0.01u16X4
PCH_TYPE3
R437 X_0R/4
R441 1K1%4
R439 3.92K1%4

CP14
PCH_1VSB
PLACE UNDER THE PCH

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

30 CUT_1VSB_EN
R440 0R/4
PCH_1VSB_EN

32 3VSB_PG
R293 X_R/2

MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: PCH Core power	Rev: 10
Date: Tuesday, April 21, 2015	Sheet 38 of 48	

SA Power:1.05V,11.1A

*OCP =11.1A*1.4=15.54A*
*Rocs(R15)=OCP*Rdson(Low side)3.3mohm]/10uA*
=15.54(3.3)mohm/10uA*
=5.2836Kohm

Rocs:5.2836K,OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

2015.01.22
for up1540:R96->2.2R,C84->1uF
for RT8125:R96->10R,C84->1uF

12VIN R210 10R/8 C207 1u16X6

EN:VIH2.4V
EN pin Maximum:6.5V

POR:4.2V

2014.10.16
up1540 no stuff

U35 RT8125CGQW
VCCSA_EN → EN
PGOOD
SA_REFOUT → REFOUT
SA_REFIN → REFIN
VCC
GND
BOOT → SA_BOOT1 R211 0R/6 SA_BOOT1_R C208 0.1u16X4
PHASE → SA_PH1
UGATE → SA_UG1
LGATE/OCSET → SA_LG1
FB → SA_FB

R219 768R1%4
C216 1000p16X4
C215 1000p16X4

FB:0.8V

Vout=0.8*(1+R19/R20)

F:300K 不可調

up1540 stuff R
RT8125C stuff C1000P C11-1022032-W08
2014.08.14

VCCSA
R218 10R1%4
R217 1K1%4
C212 X_0.1u10X4
R221 0R/4 VCCSA_SENSE 5
R215 3.16K1%4
R225 0R/4 VSS_VCCSA_SENSE 5,40
R226 10R1%4

R249 0R/4 VCCSA_EN
R223 X_36K1%4
C214 X_33p50N4
C218 X_0.01u16X4
ATX_5VSB
R248 X_47K/4
Q42 X_N-2N7002ET1G
33 VRM_EN
Q43 X_N-2N7002ET1G
C239 X_0.1u10X4

RSVD for up1540

2015.01.22
for up1540:stuff R223->36K,
C214->NC,C218->10nF
for RT8125:R223.C214.C218->NC

close to U35

RSVD
VCCSA_EN
5,33,40 SLP_S3_CTRL → SLP_S3_CTRL Q41 X_N-2N7002ET1G

SLP_S3# assertion to VR disabled
max:1us

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1* 0.2825
= 3.13575A

12VIN
C196 1u16X6
C201 10u16X8
EC1 270u16SO
SA_UG1 R207 0R/6 SA_UG1_R
Q33 N-PK616BA_PDFN8-HF

D03-616BA0C-N03

MAX:11.1A

SA_PH1
CHOKE8 CH-1.1u25A1.07m-HF
VCCSA
R212 X_2.2R/8
C210 X_3300p50X4
snubber
L04-11A7381-L65
C205 1u6.3X4
C200 22u6.3X8
EC21 560u6.3SO
EC22 560u6.3SO

NEXT VER REMOVE
SA_LG1
Q34 N-PK632BA_PDFN8-HF
R213 5.23K1%4
OCPSET:min 5Kohm

D03-632BA0C-N03

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)

VCCSA
C236 22u6.3X8
C222 X_22u6.3X8
C221 X_22u6.3X8
C219 X_22u6.3X8

MICRO-STAR INT'L CO.,LTD

MS-7973

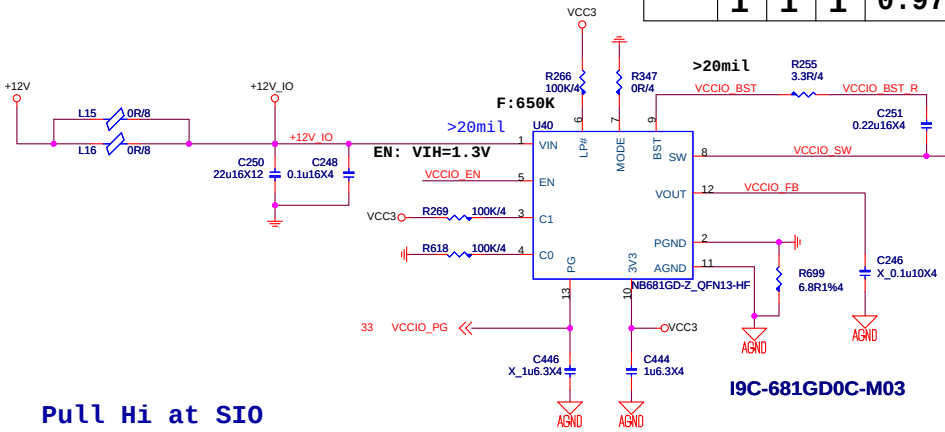
Size	Document Description	Rev
Custom	VCCSA - POWER RT8125C	10
Date: Tuesday, May 05, 2015	Sheet 39 of 48	

VCCIO

0.95V; 5.5A

IMAX 6A
ILIMIT=8.5~9A

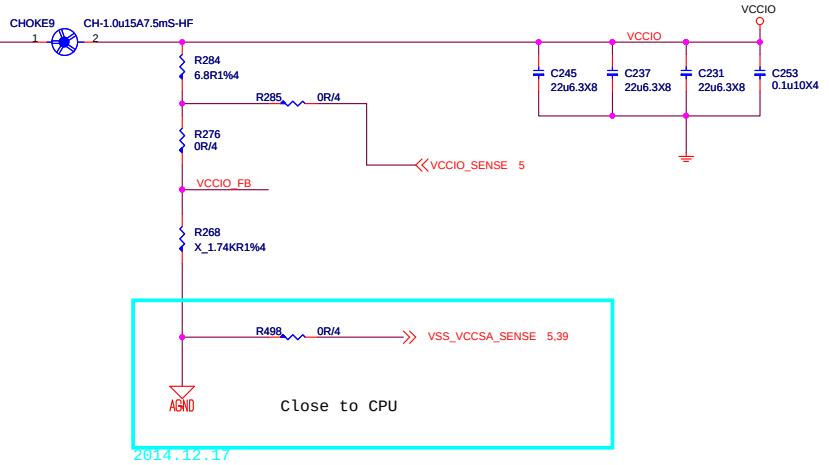
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975



I9C-681GD0C-M03

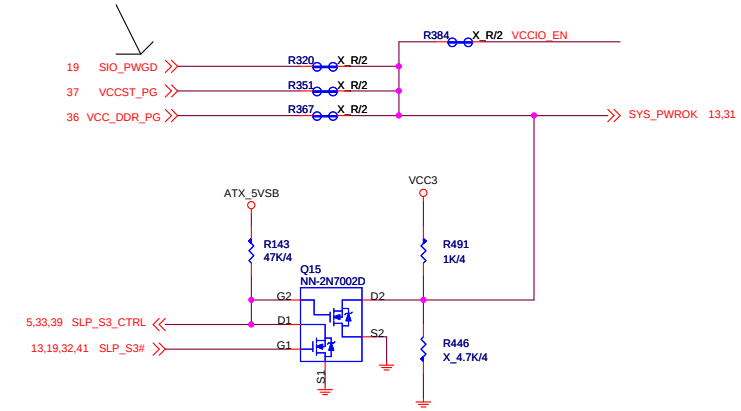
AVL:L04-0107800-M26 ; 6.86x6.47x3.0mm,22A,10mOhm
EM-10AM05V01---1UH/6*6

MAX:5.5A



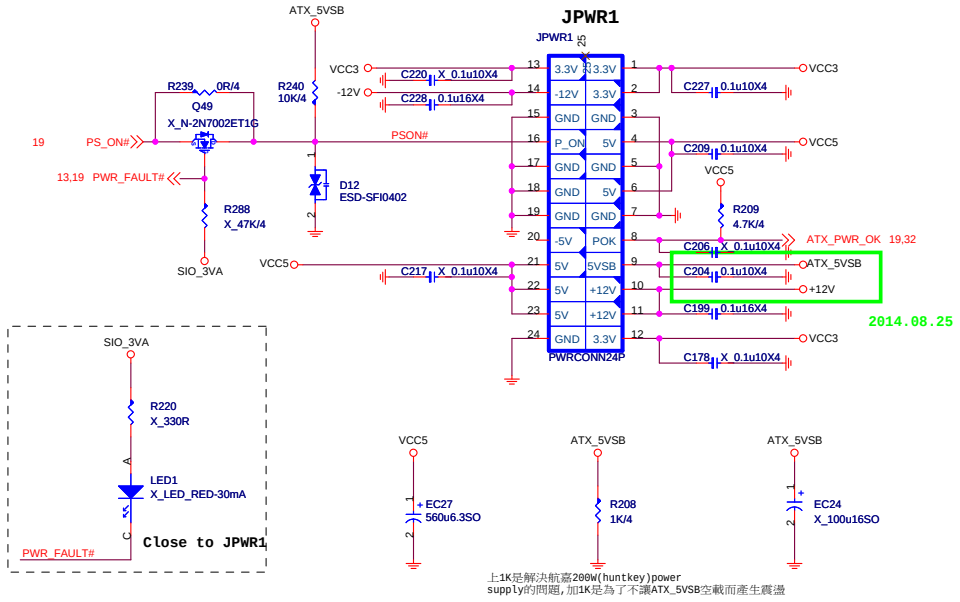
2014.12.17

Pull Hi at SIO

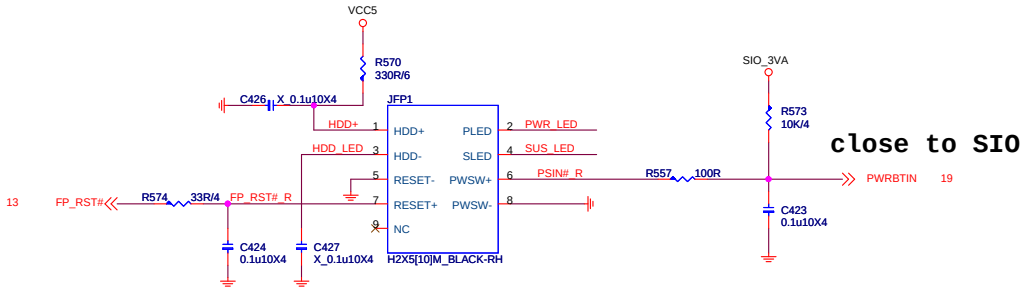


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7973	
Size: Custom	Document Description: VCCIO - POWER NB671	Rev: 10
Date: Tuesday, April 21, 2015	Sheet 40 of 48	

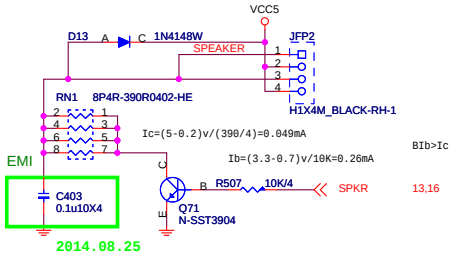
ATX POWER CONNECTOR



FRONT PANNEL

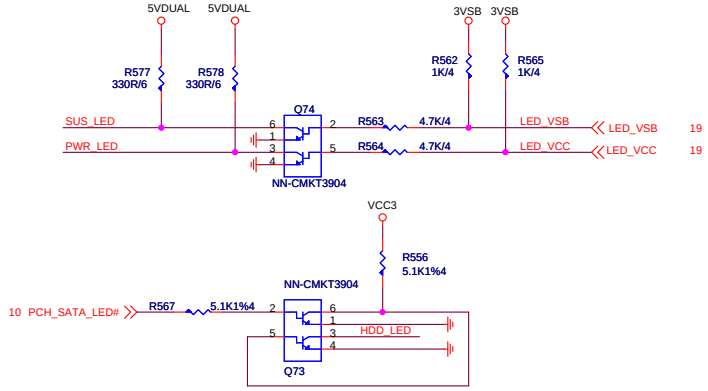


Speaker Pin Header



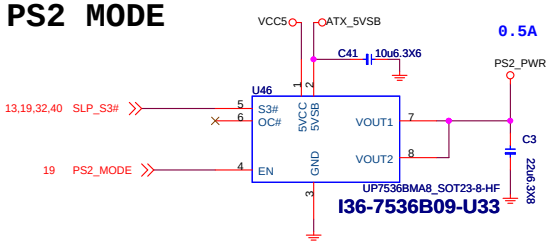
R=390 Ohm
I=(5−0.2)/R=0.0123 A
W=0.0123A x 5v=0.0615W(夠耐電阻)
R=1/16W=0.062W

LED (for NV6793D)

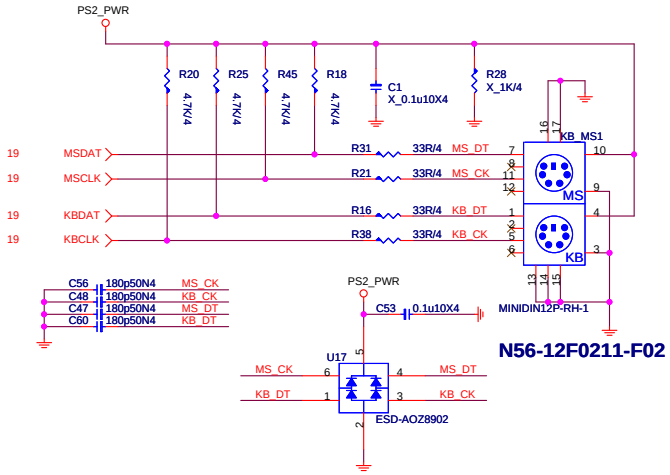


PS2 POWER

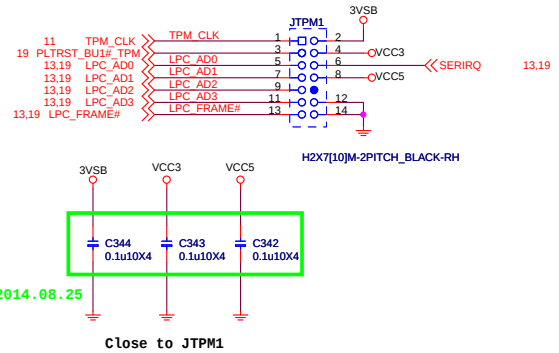
PS2 MODE



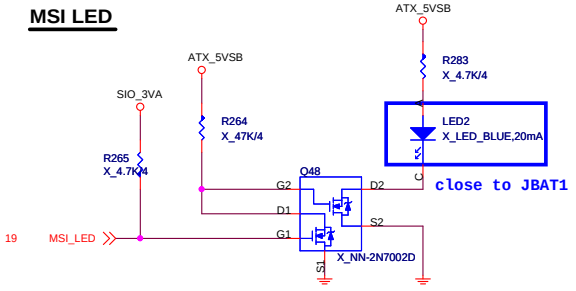
PS2 Connector



TPM



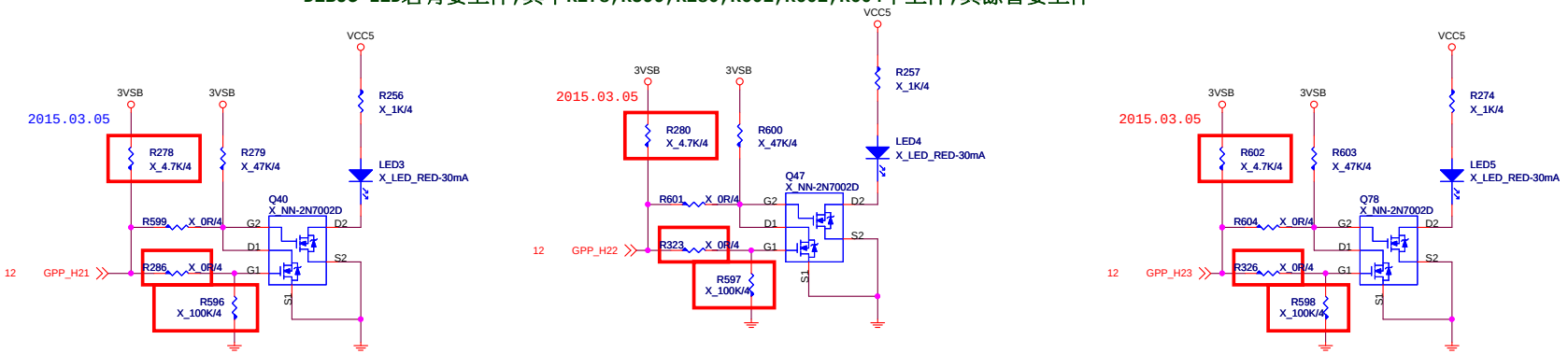
MSI LED



MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: ATX F_Panel/TPM/MSI_LED	Rev: 10
Date: Wednesday, April 29, 2015	Sheet 41 of 48	

DEBUG LED

DEBUG LED若有要上件,其中R278,R599,R280,R601,R602,R604不上件,其餘皆要上件

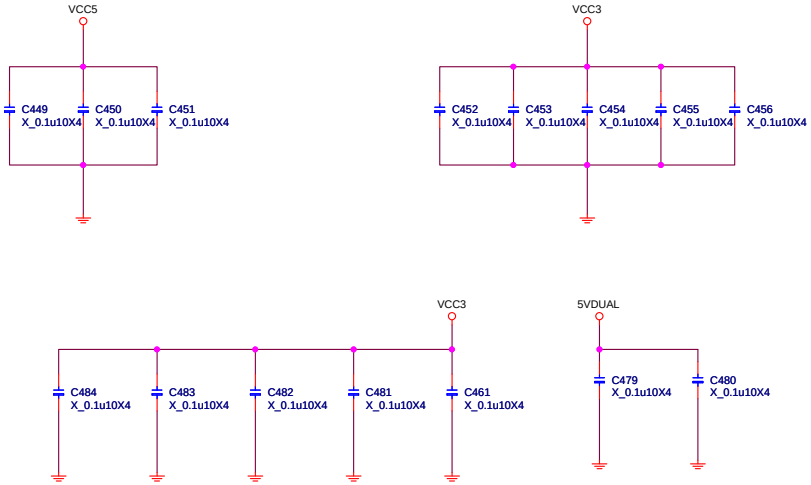


GPIO / LED	GPP_H21	GPP_H21	GPP_H21
亮	GPI (default LOW)	GPI (default LOW)	GPI (default LOW)
滅	HIGH	HIGH	HIGH

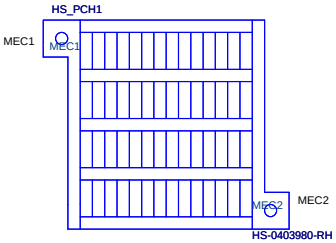
關機斷電狀態下，3個LED先維持default全亮(Eup Enable 會全滅)，開機通電後，首先進行CPU check（請研究可否blink），check PASS後則CPU LED滅掉，接著依序進行Memory與VGA的check，LED的行為相同。因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

MICRO-STAR INT'L CO.,LTD	
MS-7973	
Size: Custom	Document Description: ATX F_Panel/TPM/MSI_LED
Rev: 10	
Date: Friday, April 24, 2015	Sheet 42 of 48

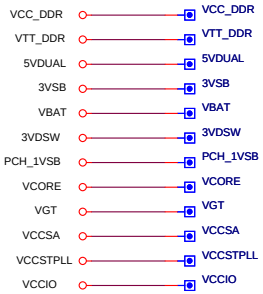
EMI CAP



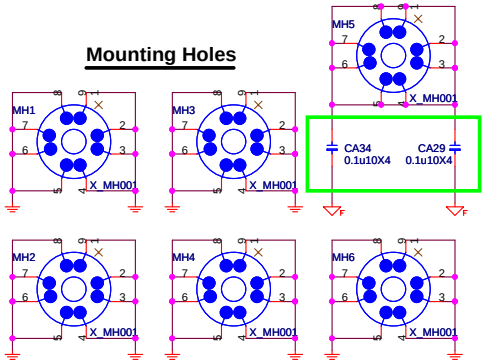
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7973	
Size: Custom	Document Description: EMI	Rev: 10
Date: Monday, May 04, 2015	Sheet 43 of 48	



E31-0403980-K08



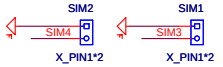
Mounting Holes



PK0-0798120-G37,精成,23,寶安恩斯邁廠(MSIS)4,Coffee
PK0-0798120-E48,競華,23,寶安恩斯邁廠(MSIS)4,Coffee

Optical Fiducial Marks-120

Simulation



MICRO-STAR INT'L CO.,LTD		
MS-7973		
Size: Custom	Document Description: Manual Parts	Rev: 10
Date: Tuesday, April 14, 2015	Sheet 44 of 48	