LCFC Confidential

TGL-U LCFC T/S Schematics Document

Tiger / Serval M/B SCHEMATICS

Intel TigerLake Processy with LPDDR4X

REV:0.03

Title	<Title>	
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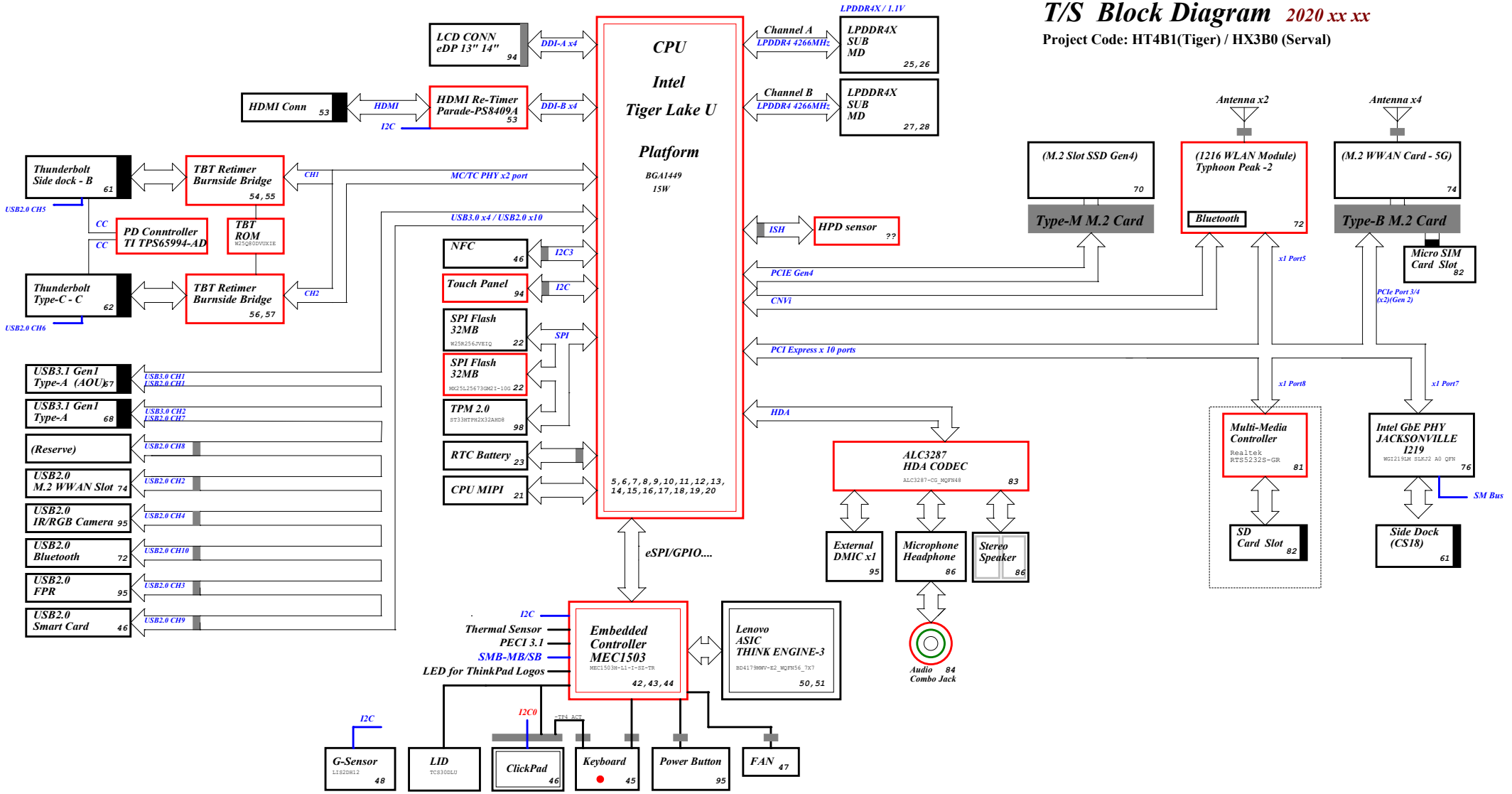
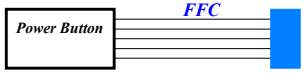
T/S Block Diagram 2020 xx xx

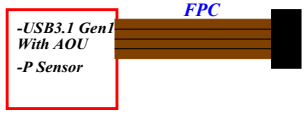
Project Code: HT4B1(Tiger) / HX3B0 (Serval)



Common Sub-Board



T14s Sub-Board



Sub Board

Different with CS20

External Connector/Socket

Internal Connector/Socket

Internal Switch

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EC HISTORY

VER.0.01 2020/02/05 TG1_EVT_EC001_Logic_Page v4

607872_TGL_UP3_UP4_PltDoc_Rev1p5

10.12.4 Power States

Table 237. System with M3 State Supported

Rails	SKUs	S0/M0[3]	C10[2]	S0ix/M-off[4]	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3[1]
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	OFF	No Power
VCC_VNNEXT_1P05	All	ON	ON	ON	ON	ON	OFF	No Power
VCC_V1P05EXT_1P05	All	ON	ON	ON	ON	ON	OFF	No Power
V3.3M[5]	All	ON	ON	OFF	ON[10]	OFF	OFF	No Power
V1.8M[5]	All	ON	ON	OFF	ON[10]	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST	All	ON	ON	ON	OFF[6]	OFF[6]	OFF	No Power
VCCSTG	All	ON	OFF [2]	OFF	OFF	OFF	OFF	No Power
VCC1P8A[15]	H	ON	OFF	OFF	OFF	OFF	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON[11]	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON[11]	OFF[14]	OFF[14]	OFF	No Power

continued...

Notes:
1. The state of the system without RTC well powered can also be considered G3.
2. VCCSTG can be turned off when the processor is in C10
3. S0/M0 state includes all Package C-states from C0-C10
4. Assume SLP_S0# and CPU_C10_GATE# have asserted from the PCH
5. V3.3M and V1.8M are platform rails used by external devices which ME operates during Sx/M3 states. These rails are not use directly by the CPU/PCH, and are not present on non-M3 supported systems
6. VCCST and VCCSTG can remain powered during S4 and S5 power states for board cost optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Platform Debug and Test Hooks chapter for more details.
7. NA
8. NA
9. VCCSTG is allowed to be ramped to 0V during S0 only when CPU_C10_GATE# is asserted. Specific exit latency targets are required when this feature is implemented. If VCCSTG power gating is not supported on the platform (shared with VCCST), VCCSTG is allowed to stay ON during S0ix states. Note that merging power rails may reduce power optimization opportunities on the platform.
10. For no M3 support on external devices, V3.3M/V1.8M will be OFF in Sx/M3
11. This supply is expected to be 0V during states where SLP_S0# is asserted. It may be left on during this condition, but the SoC will not achieve it is lowest power consumption. Specific power up latencies apply when exiting this state. Applicable to form factors with battery only (ie. AIO)Optional depending platform design; ON if AC is present

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T/S SIT Planar Logic Schematics

T/S
VER 1.00
Sep/06/2020

BASE LOGIC : T14s GEN2_FVT_0803_V20_final_BOM

Lenovo

Project Name : T14s Gen2	Title : TITLE PAGE
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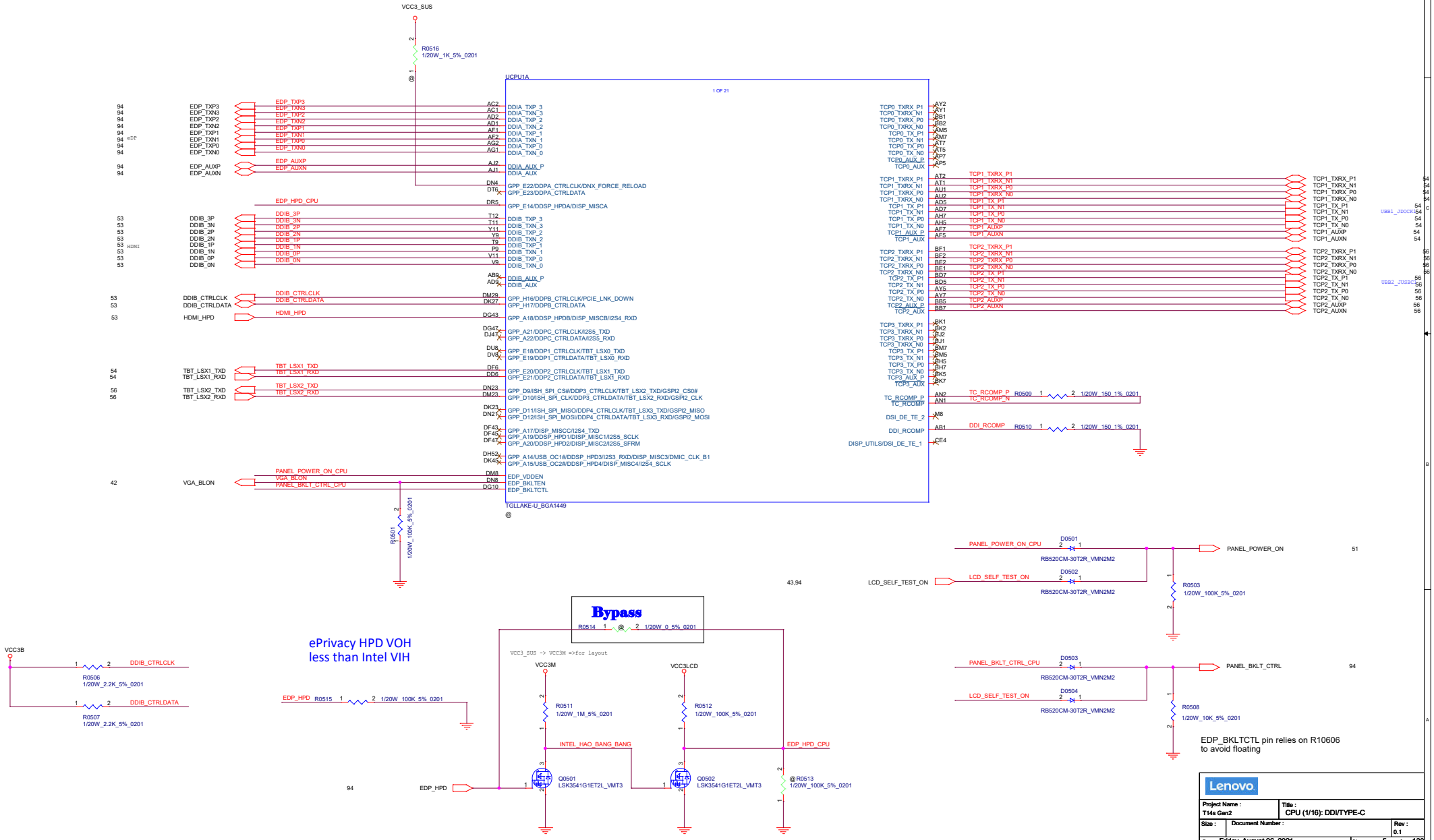
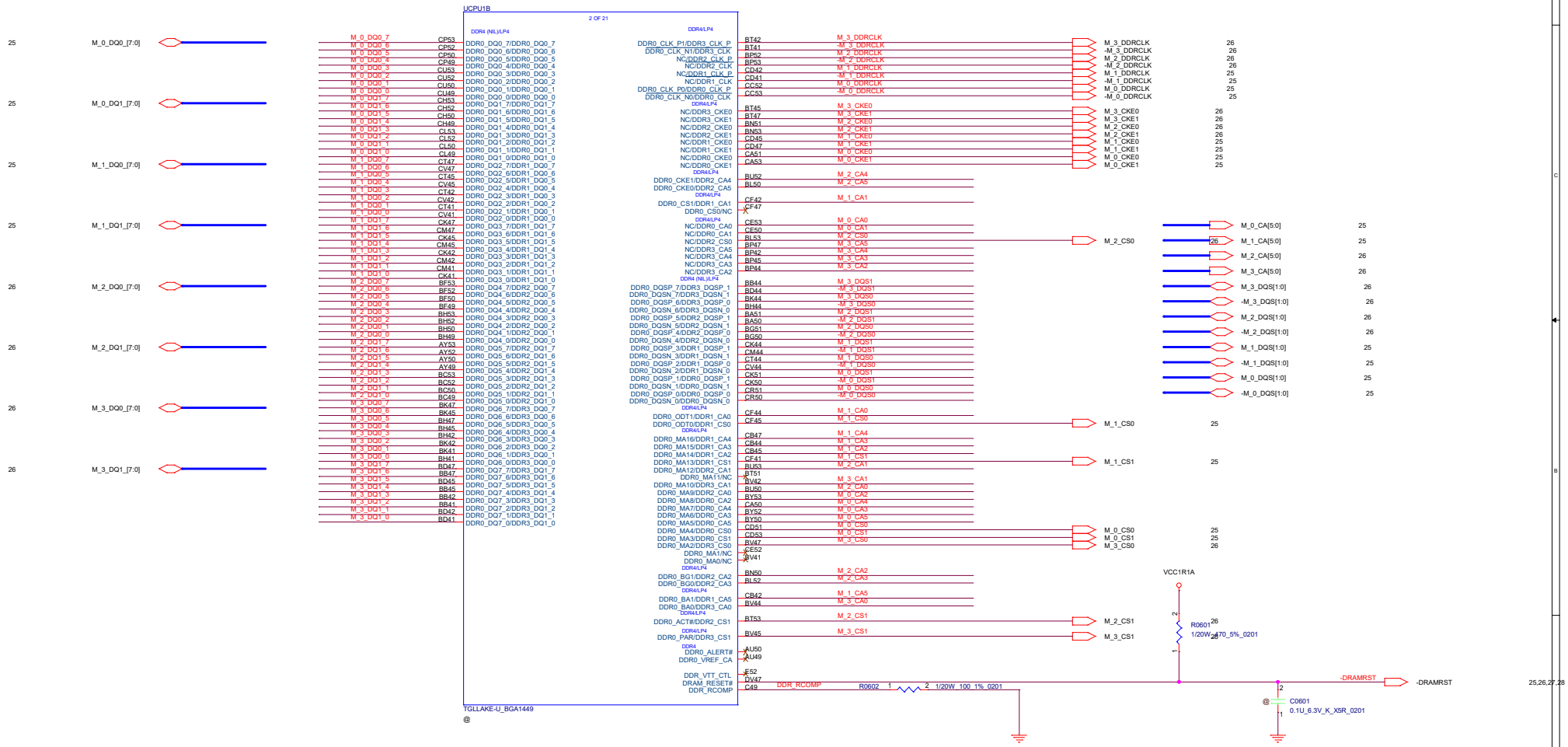
TABLE : Functional Strap

GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD (DDP1 I2C / TBT_LSX0 Pin VCC Configuration)	
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD (DDP2 I2C / TBT_LSX1 Pin VCC Configuration)	
GPP_D10/DDP3_CTRLDATA/TBT_LSX2_RXD (DDP3 I2C / TBT_LSX2 Pin VCC Configuration)	
GPP_D12/DDP4_CTRLDATA/TBT_LSX3_RXD (DDP4 I2C / TBT_LSX3 Pin VCC Configuration)	
HIGH	3.3V for HDMI Display I2C (External Pull-Up Resistor Required)
LOW	1.8V for Thunderbolt LSX (Default)





Project Name : T14s Gen2	Title : CPU (2/16): DDR (1/2)
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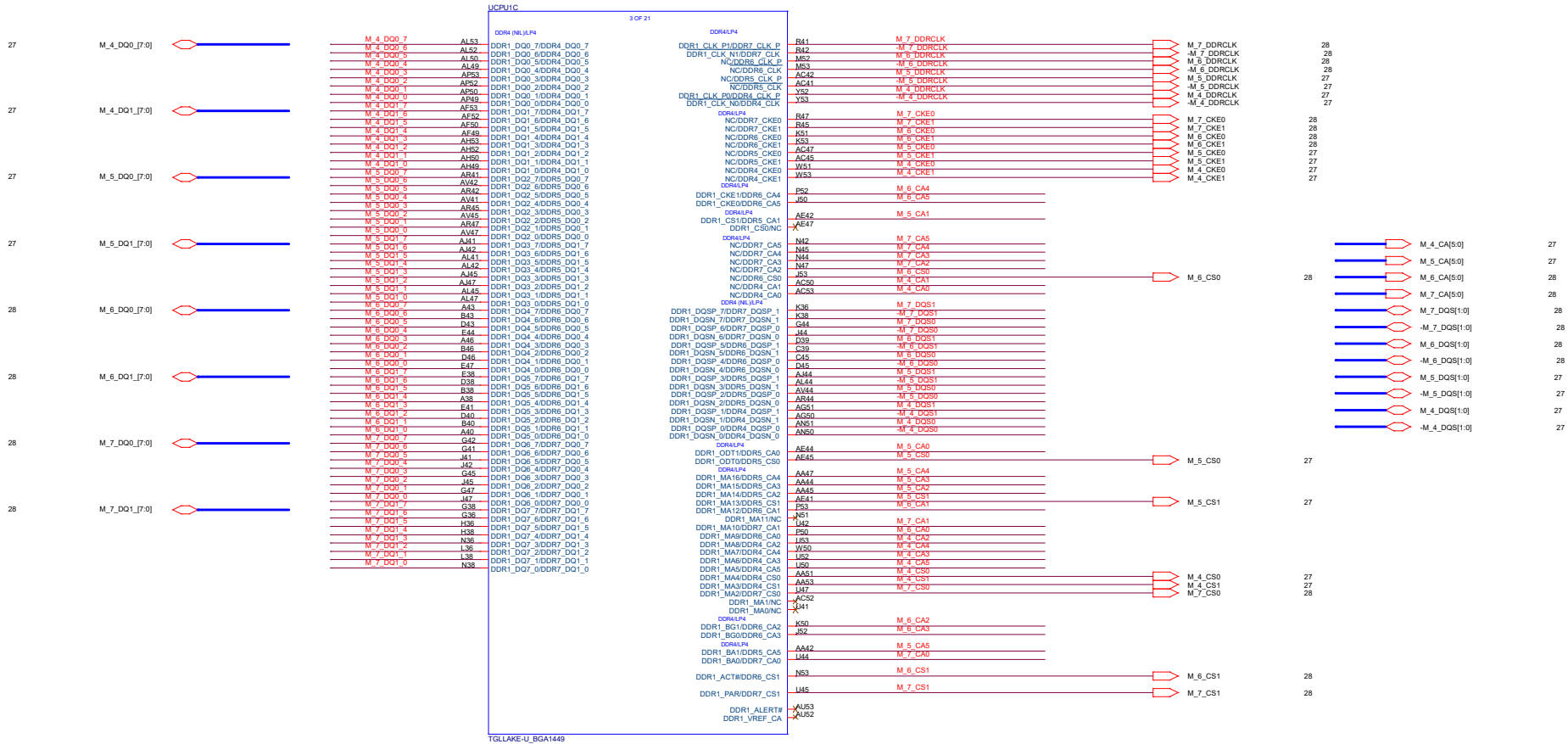

Project Name : T14s Gen2	Title : CPU (3/16): DDR (2/2)
Size : C	Document Number :
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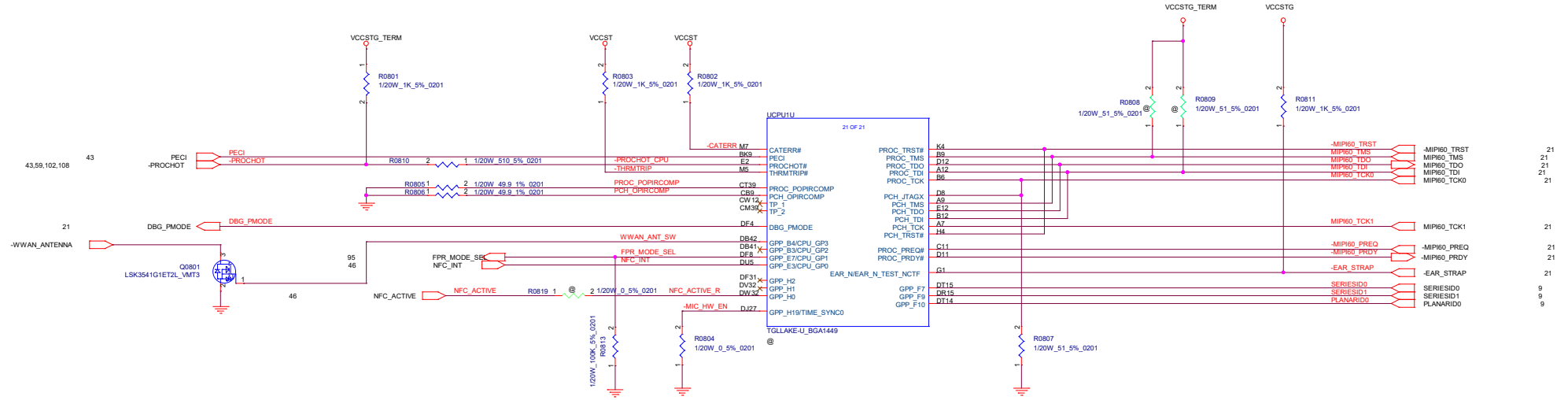

TABLE : Functional Strap

GPP_C5/SML0ALERT# (Boot Strap Bit 0)	
GPP_H0 (Boot Strap Bit 1)	
GPP_H1 (Boot Strap Bit 2)	
GPP_H2 (Boot Strap Bit 3)	
0000b	Master Attached Flash Configuration (Default)

TABLE : Functional Strap

GPP_F7 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

TABLE : Functional Strap

GPP_F10 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

TABLE : Functional Strap

DBG_PMODE (DFx Test Mode)	
HIGH	DFx Test Mode Disabled (default)
LOW	DFx Test Mode Enabled

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Project Name : T14s Gen2	Title : CPU (4/16): MISC/JTAG	
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TABLE : Functional Strap

SPI0_MOSI (Boot Halt)	
HIGH	Disabled
LOW	Enabled

← LOGIC

TABLE : Functional Strap

SPI0_IO2 (Consent Strap)	
HIGH	Disabled
LOW	Enabled

← LOGIC

TABLE : Functional Strap

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled
LOW	Enabled

← LOGIC

TABLE : Functional Strap

GPP_E6 (JTAG ODT Disable)	
HIGH	JTAG ODT Enabled
LOW	JTAG ODT Disabled

← LOGIC

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

← LOGIC

TABLE : Functional Strap

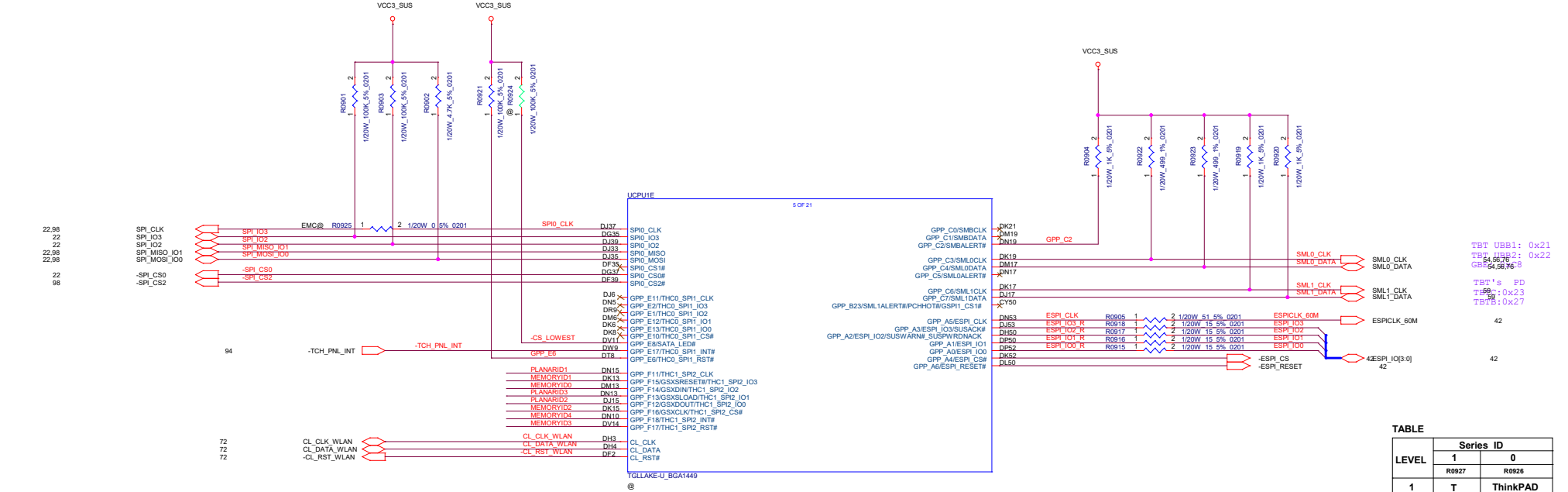
GPP_C5/SML0ALERT# (Boot Strap Bit 0)
GPP_H0 (Boot Strap Bit 1)
GPP_H1 (Boot Strap Bit 2)
GPP_H2 (Boot Strap Bit 3)

0000b	Master Attached Flash Configuration (Default)

TABLE : Functional Strap

GPP_B23/SML1ALERT#/PCHHOT# (CPUNSSC Clock Frequency)	
HIGH	19.2MHz Clock (Derived from 38.4MHz Crystal)
LOW	38.4MHz Clock (Direct from Crystal) (Default)

← LOGIC



TABLE

LEVEL	MEMORY ID				
	4	3	2	1	0
	R0910	R0911	R0912	R0913	R0914
1	NA	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM	ASM

TABLE:

MEMORYID[4:0]	U2501,U2601,U2701,U2801				Total Memory	LCFC PN
	Supplier	Supplier's P/N	Capacity			
00h (00000b)	SK hynix	H9HCNNNBKMMLXR-NEE	16Gb	DDP	8GB	SA0000AMA10
01h (00001b)		H9HCNNNCPMMLXR-NEE	32Gb	QDP	16GB	SA0000AMB10
02h (00010b)		H9HCNNNFAMMLXR-NEE	64Gb	ODP	32GB	SA0000AXB00
03h (00011b)	Samsung	K4U6E3S4AA-MGCR	16Gb	SDP	8GB	SA0000AMP10
04h (00100b)		K4UBE3D4AA-MGCR	32Gb	DDP	16GB	SA0000AMQ10
05h (00101b)		K4UCE3Q4AA-MGCR	64Gb	QDP	32GB	SA0000AMR10
06h (00110b)	Micron	MT53E512M32D2NP-046 WT:E	16Gb	DDP	8GB	SA00009ET00
07h (00111b)		MT53E1G32D2NP-046 WT:A	32Gb	DDP	16GB	SA0000AN910
08h (01000b)		MT53E2G32D4NQ-046 WT:A	64Gb	QDP	32GB	SA0000ANA10

Samsung found some problem by internal evaluation on EVT

TABLE

LEVEL	Series ID	
	1	0
	R0927	R0926
1	T	ThinkPAD
0	Ts/X	NEC

TABLE

LEVEL	PLANAR ID			
	3	2	1	0
	R0906	R0907	R0908	R0909
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

LEVEL	PLANARID[3:0]
EVT	0000b
FVT	0001b
SIT	0100b
SVT	1111b

Lenovo

Project Name : T14s Gen2	Title : CPU (5/16): ESPI/SPI/SMBUS/C-LINK	
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TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" mode
LOW	Disable "Top Swap" mode (Default)

← LOGIC

ISH I2C0: 1.8V

ISH I2C1: 3.3V

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

← LOGIC

VCC3_SUS VCC3B VCC1R8_SUS VCC3M

R1001 R1002 R1003 @ R1004 @ R1005 1/20W_1K_5%_0201 1/20W_10K_5%_0201 1/20W_51K_5%_0201

R1008 R1009 1/20W_4.7K_5%_0201

R408 R409 1/20W_1K_5%_0201

R1012 R1016 R1018 R1017 1/20W_10K_5%_0201

TOP_SWAP_EN R1014 1 2 0_0201_SP

LCD size control
Low:14" JAZZ
High:13" SIDESWIPE

-WWAN_PERST
PCH_SPKR
Size CTL
-IR_CAM_DTCT
-WWAN_PEWAKE
-PAD_INT
-FULL_CARD_POWER_OFF
-WWAN_RESET
SMARTCARD_ON
-TPM_IRQ
LPSS_UART2_TXD
LPSS_UART2_RXD
LPSS_I2C0_SCL_PAD
LPSS_I2C0_SDA_PAD
LPSS_I2C1_SCL_PNL
LPSS_I2C1_SDA_PNL
I2C_CLK_E3
I2C_DATA_E3
LPSS_I2C3_SCL_NFC
LPSS_I2C3_SDA_NFC

UCPU1F
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TGLLAKE-U_BGA1449

GPP_B16/GSPI0_CLK
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
GPP_B15/GSPI0_CS0#
GPP_B20/GSPI1_CLK
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B19/GSPI1_CS0#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_H5/I2C2_SCL
GPP_H4/I2C2_SDA
GPP_H7/I2C3_SCL
GPP_H6/I2C3_SDA
GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5
GPP_B6/ISH_I2C0_SCL
GPP_B5/ISH_I2C0_SDA
GPP_B8/ISH_I2C1_SCL
GPP_B7/ISH_I2C1_SDA
GPP_B10/I2C5_SCL/ISH_I2C2_SCL
GPP_B9/I2C5_SDA/ISH_I2C2_SDA
GPP_E16/ISH_GP7
GPP_E15/ISH_GP6
GPP_D18/ISH_GP5
GPP_D17/ISH_GP4
GPP_D3/ISH_GP3/BK3/SBK3
GPP_D2/ISH_GP2/BK2/SBK2
GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0
GPP_RCOMP
GPP_T3
GPP_T2
GPP_U5
GPP_U4

TOUCHPANEL_ON_U
-TCH_PNL_RST_U
-HPD_DTCT
-LID_CLOSE
-ISH_ACCEL_INT
-ISH_HPD_INT

R1013 1/20W_200_1%_0201
R1015 1/20W_100K_5%_0201
R1019 1/20W_0_5%_0201
D1001 RB521CM-30T2R_VMN2M-2
R1021 R1020 1/20W_0_5%_02011

EPRIVACY_ON
TOUCHPANEL_ON
-SSD_PERST_R
-WWAN_DISABLE
ISH_I2C0_SCL
ISH_I2C0_SDA

TP1001 TP1002 TP1003 Test_Point_16MIL

U0501
SN74LVC1G17DRLR_SOT-5
-SSD_PERST_R
-SSD_PERST

LPSS Port Assignment	
I2C0	Touch Pad
I2C1	Touch Panel
I2C2	(Smart Light) PAC1934
I2C3	NFC
I2C4	(MIPI CSI Camera)
I2C5	(E3)
UART0	
UART1	
UART2	Debug Port
GSPI0	
GSPI1	(Fingerprint Reader)
GSPI2	

ISH I2C Port Assigment	
ISH_I2C0	HPD Sensor (JCAM side)
ISH_I2C1	EC
ISH_I2C2	

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Project Name : T14s Gen2	Title : CPU (6/16): LPSS/ISH	
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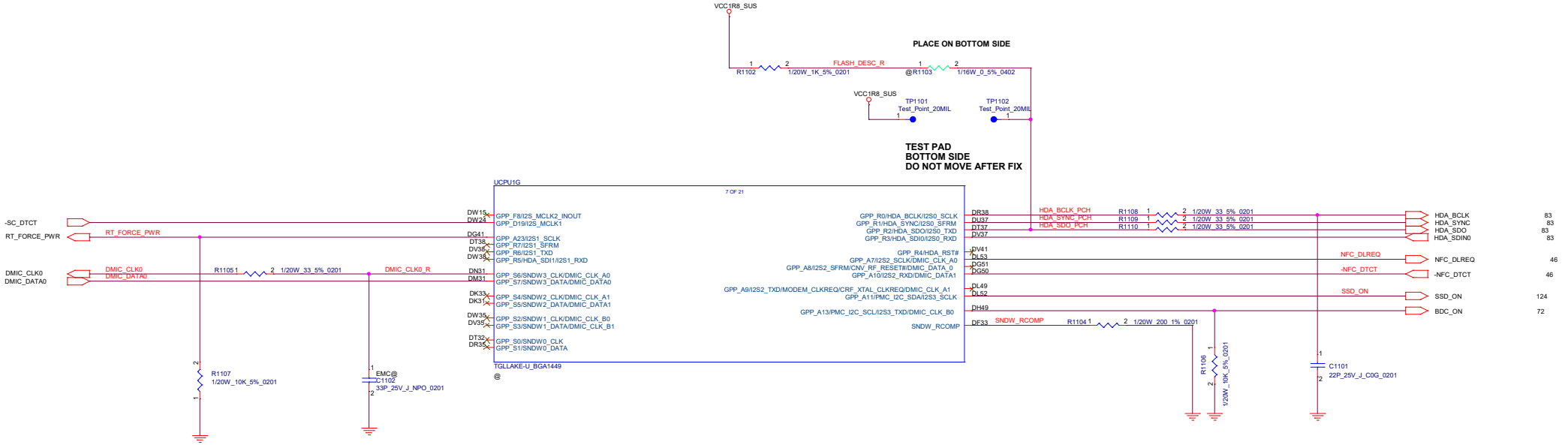
TABLE : Functional Strap

GPP_R2/HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)



Project Name : T14s Gen2	Title : CPU (7/16): AUDIO
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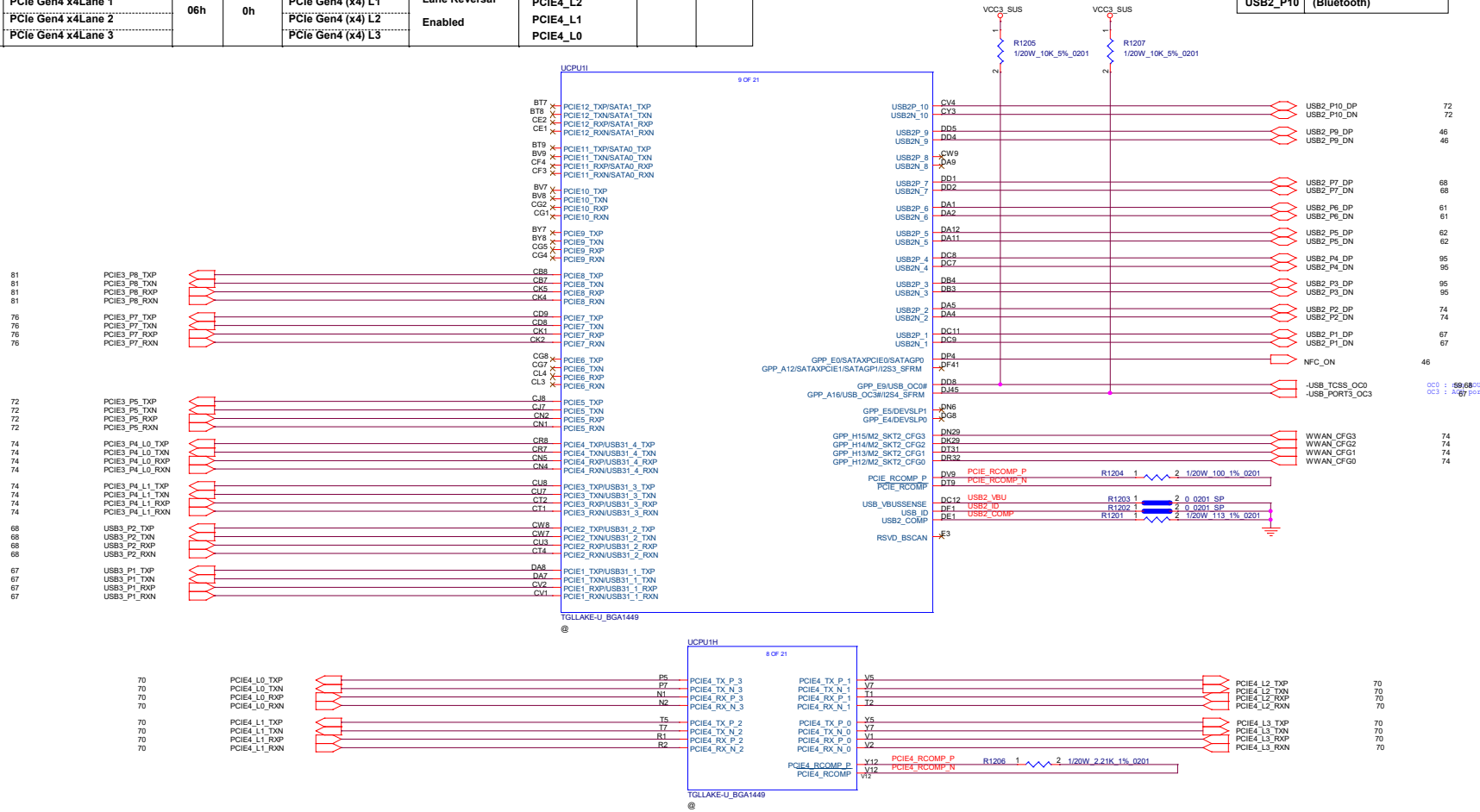
Flexible I/O Configuration								
HSIO Port	High Speed Signals	PCI Device	PCI Function	HSIO Configuration	Descriptor for PCIe	Net Name	PCI Device	PCI Function
PCH L0	USB 3.1 #1 / PCIe Gen3 #1	1Ch	0h	USB 3.1 #1	1x2, 2x1 Lane Reversal Enabled	USB3_P1		
PCH L1	USB 3.1 #2 / PCIe Gen3 #2		1h	USB 3.1 #2		USB3_P2		
PCH L2	USB 3.1 #3 / PCIe Gen3 #3		2h	PCIe Gen3 #3		PCIE3_P4_L1		
PCH L3	USB 3.1 #4 / PCIe Gen3 #4		3h	PCIe Gen3 #4		PCIE3_P4_L0		
PCH L4	PCIe Gen3 #5	1Ch	4h	PCIe Gen3 #5	4x1 Lane Reversal Disabled	PCIE3_P5		
PCH L5	PCIe Gen3 #6		5h	PCIe Gen3 #6		N/A		
PCH L6	PCIe Gen3 #7 (GbE)		6h	PCIe Gen3 #7 (GbE)		PCIE3_P7		
PCH L7	PCIe Gen3 #8 (GbE)		7h	PCIe Gen3 #8		PCIE3_P8		
PCH L8	PCIe Gen3 #9 (GbE)	1Dh	0h	PCIe Gen3 #9 (x4)	1x4 Lane Reversal Disabled	N/A		
PCH L9	PCIe Gen3 #10		1h	PCIe Gen3 #10 (x4)		N/A		
PCH L10	PCIe Gen3 #11 / SATA #0		2h	PCIe Gen3 #11 (x4)		N/A		
PCH L11	PCIe Gen3 #12 / SATA #1		3h	PCIe Gen3 #12 (x4)		N/A		
CPU L0	PCIe Gen4 x4Lane 0	06h	0h	PCIe Gen4 (x4) L0	1x4 Lane Reversal Enabled	PCIE4_L3		
CPU L1	PCIe Gen4 x4Lane 1			PCIe Gen4 (x4) L1		PCIE4_L2		
CPU L2	PCIe Gen4 x4Lane 2			PCIe Gen4 (x4) L2		PCIE4_L1		
CPU L3	PCIe Gen4 x4Lane 3			PCIe Gen4 (x4) L3		PCIE4_L0		

PCIe Port Assignment	
PCIE3_P1	(USB3_P1)
PCIE3_P2	(USB3_P2)
PCIE3_P3	WWAN Lane 1
PCIE3_P4	WWAN Lane 0
PCIE3_P5	(WLAN)
PCIE3_P6	(Reserved)
PCIE3_P7	GbE PHY
PCIE3_P8	(SD Card)
PCIE3_P9 (x4)	(dGPU)
PCIE4 (x4)	NVMe SSD

SATA Port Assignment	
SATA_P0	(PCIE3_P11)
SATA_P1	(PCIE3_P12)

USB 3.1 Port Assignment	
USB3_P1	(Type-A Port) (AOU)
USB3_P2	Type-A Port
USB3_P3	(PCIE3_P3)
USB3_P4	(PCIE3_P4)

USB 2.0 Port Assignment	
USB2_P1	(Type-A Port) (AOU)
USB2_P2	WWAN
USB2_P3	Fingerprint Reader
USB2_P4	RGB / IR Hybrid Camera
USB2_P5	Type-C Port B
USB2_P6	Type-C Port C
USB2_P7	Type-A Port
USB2_P8	(Reserve)
USB2_P9	(Smart Card Reader)
USB2_P10	(Bluetooth)



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Project Name : T14s Gen2	Title : CPU (8/16): PCIE/USB/SATA	
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GPP_A11	SSD_ON
GPP_H23	TOUCHPANEL_ON(Reserve)
GPP_D13	TOUCHPANEL_ON

VCC3_TOUCHPANEL_ON is connected to both TOUCHPANEL_ON and B_ON via diode.
So, We assume that VCC3_TOUCHPANEL_ON is asserted To "High" by B_ON like attached waveform of VCC3_SSD
But GPP_H23 is set to low state after reset as PCH GPIO table. Then, VCC3_TOUCHPANEL_ON is not aligned with B_ON like attached waveform.
So we have changed GPIO assignment to GPP_D13 to align power on sequence With B_ON.

GPIO	Power Well	Voltage Tolerance	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Pin State During Reset	Pin State Immediately After Reset
GPP_A11	VCCPRIM_1P8 or VCCPRIM_3P3	1.8 V or 3.3 V	GP-In			no	no	yes(1)	Z	Z
GPP_D13	VCCPRIM_1P8 or VCCPRIM_3P3	1.8 V or 3.3 V	GP-In			no	no	yes(1)	Z	Z
GPP_H23	VCCPRIM_1P8 or VCCPRIM_3P3	1.8 V or 3.3 V	GP-Out			no	no	no	Z	L

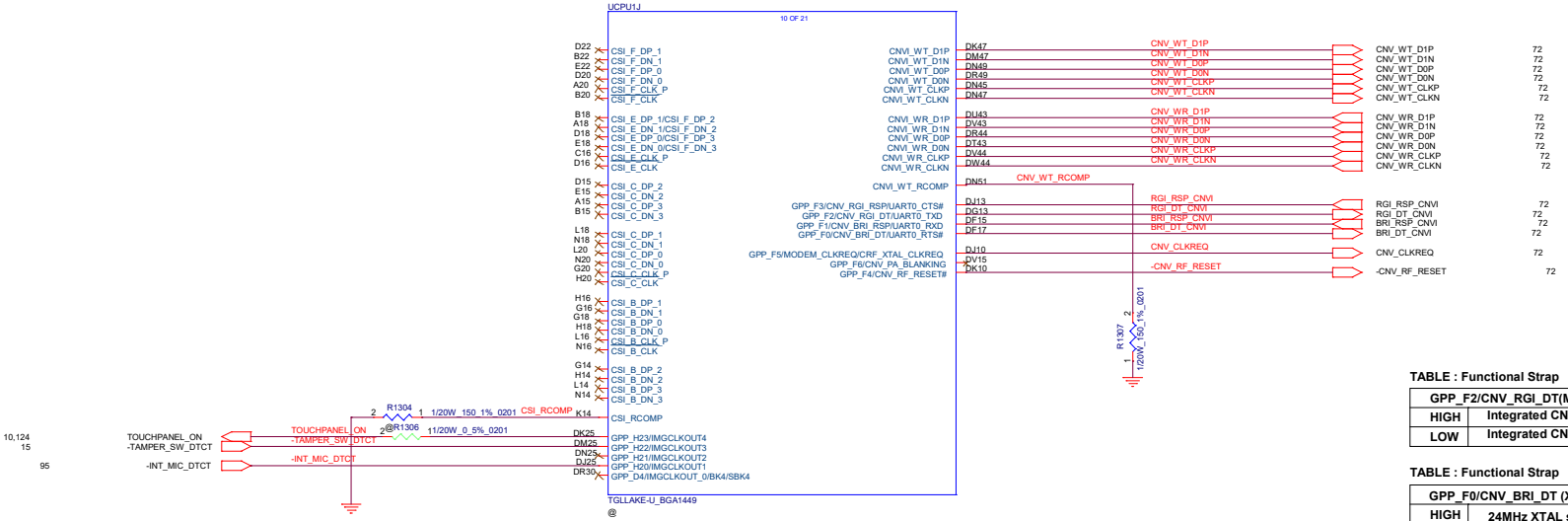

TABLE : Functional Strap

GPP_F2/CNV_RGI_DT(M.2 CNVi Mode Select)	
HIGH	Integrated CNVi Disabled
LOW	Integrated CNVi Enabled

TABLE : Functional Strap

GPP_F0/CNV_BRI_DT (XTAL Frequency Selection)	
HIGH	24MHz XTAL selected
LOW	38.4MHz XTAL frequency selected (Default) ← LOGIC

[Issue Symptom]
All PCIe device can't recognize

[Root cause]
GPP_F0 strap not correct setting.

[Solution]
GPIO need to set up "native" and can't have PU resistance.

CNVi_WT_RCOMP

Interface	Pin Name	Board Rterm (Ohm)	Board DC resistance (ohms)	Main route trace spacing requirement (um)	Notes
CNVi	CNVi_WT_RCOMP	150Ω ±1% to GND	<0.5	200	This RCOMP can be left unconnected if not used.

Lenovo

Project Name : T14s Gen2	Title : CPU (9/16): CSI-2/CNVI
Size : C	Document Number :
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PCIECLK and CLKREQ# Port Assignment		
Port 0	PCIe Gen4 (x4)	NVMe SSD
Port 1	PCIe Gen3 P5	(M.2 WLAN)
Port 2	PCIe Gen3 P1	M.2 WWAN
Port 3	PCIe Gen3 P9 (x4)	(dGPU)
Port 4	PCIe Gen3 P7	GbE PHY
Port 5	PCIe Gen3 P8	(SD Card)
Port 6	PCIe Gen3 P6	(Reserved)

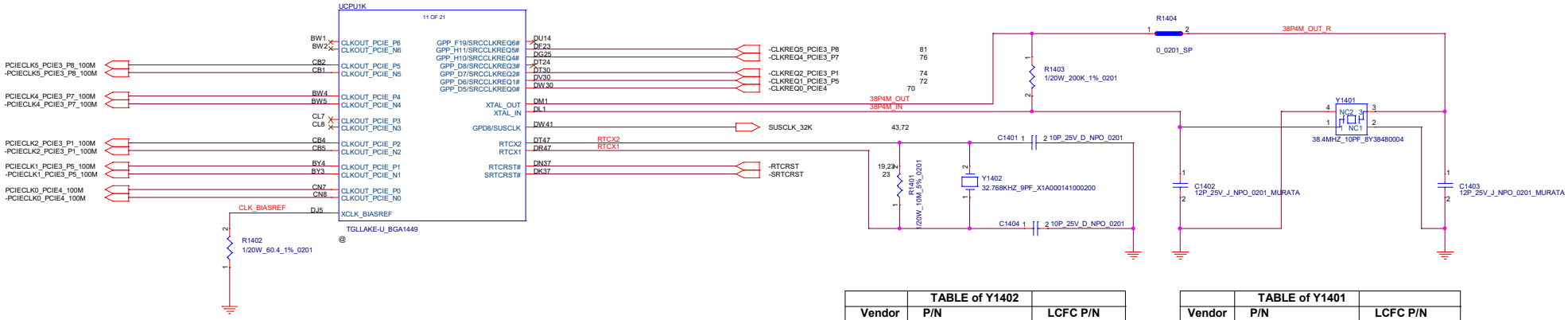

TABLE of Y1402		
Vendor	P/N	LCFC P/N
EPSON	X1A000141000201	SJ10000IX00
TXC	9H03280012	SJ10000J900
KDS	1TJF090DJ1A000B	SJ100069400

TABLE of Y1401		
Vendor	P/N	LCFC P/N
TXC	8Y38480004	SJ10000SN00

Project Name : T14s Gen2	Title : CPU (10/16): CLOCK SUGNALS	
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TABLE : U0501,U1501

TI	SN74LVC1G17DRLR	SA00005MG00
TOSHIBA	TC7SZ17FE	SA00008EZ00
ONSemi	NL17SZ17XV5T2G	SA00005OU00

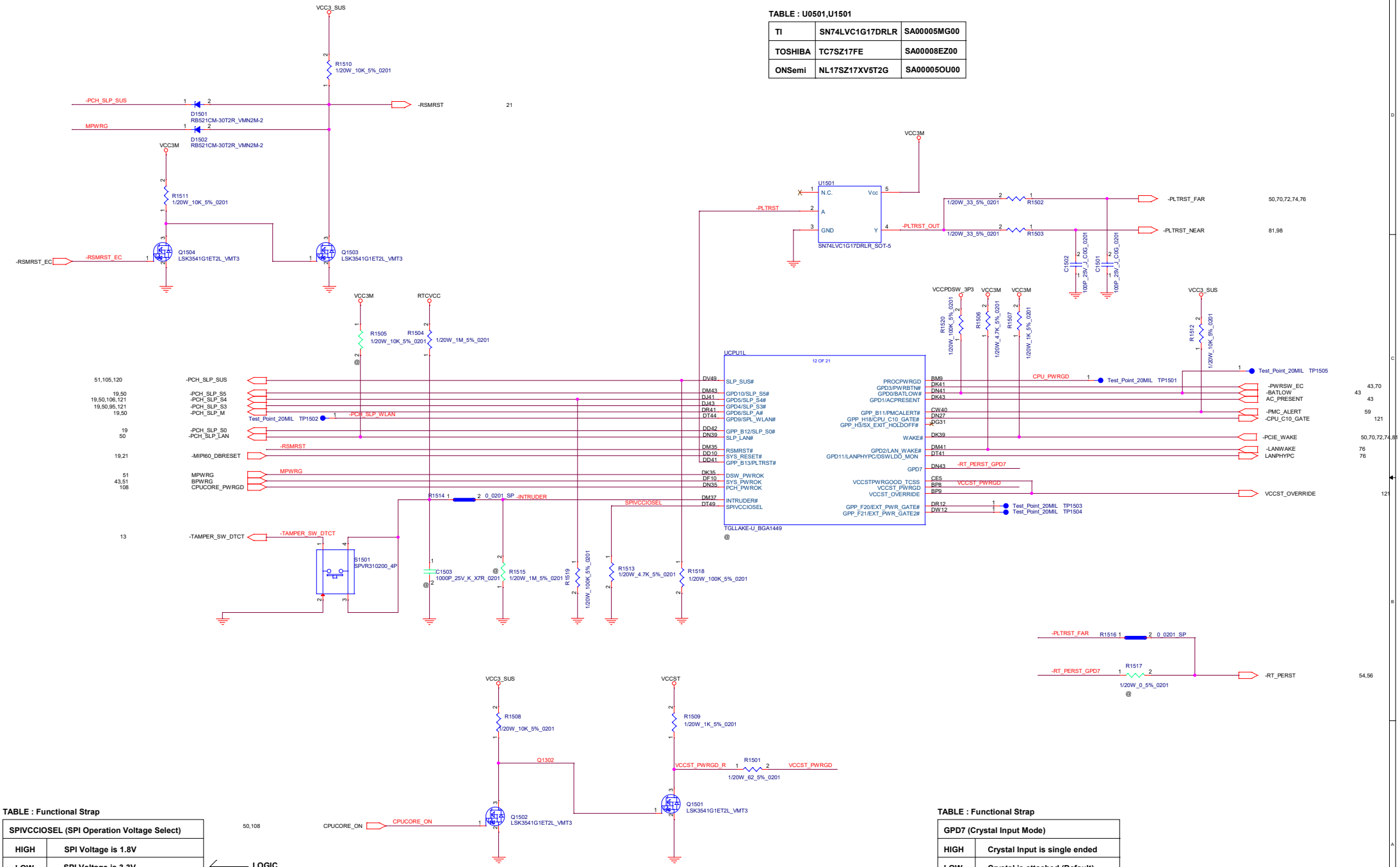

TABLE : Functional Strap

SPIVCCIOSEL (SPI Operation Voltage Select)	
HIGH	SPI Voltage is 1.8V
LOW	SPI Voltage is 3.3V

LOGIC

TABLE : Functional Strap

GPD7 (Crystal Input Mode)	
HIGH	Crystal Input is single ended
LOW	Crystal is attached (Default)

Project Name : T14s Gen2	Title : CPU (11/16): SYSTEM PM
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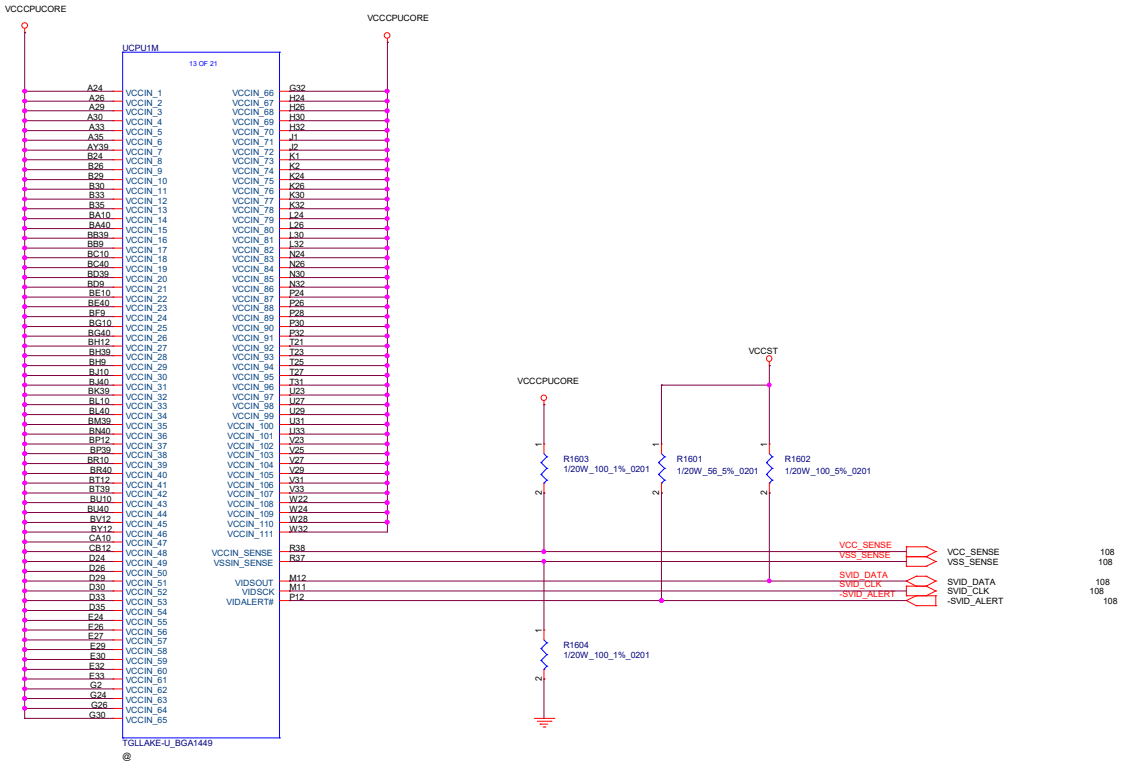
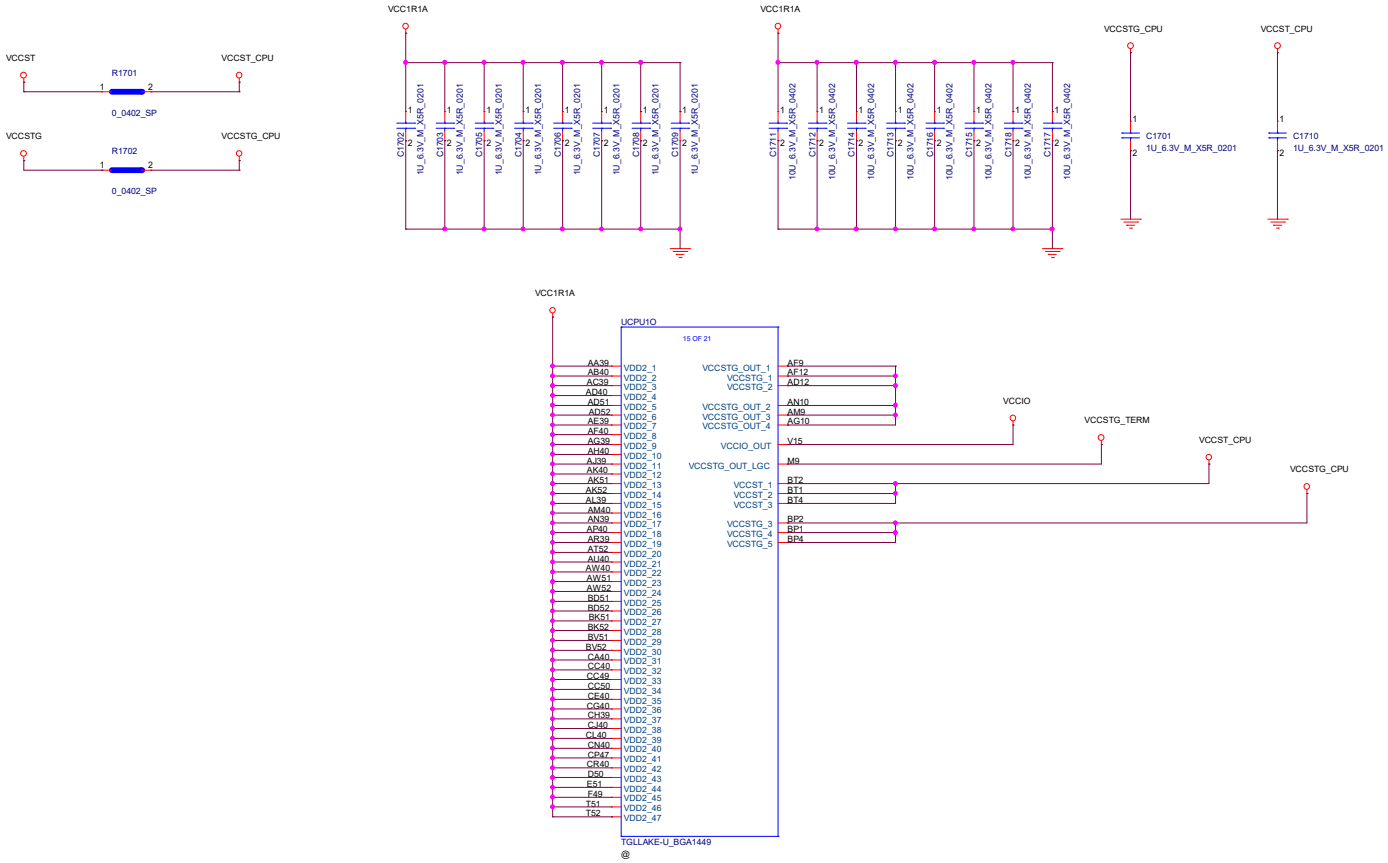


Project Name : T14s Gen2	Title : CPU (12/16): CPU POWER (1/2)	
Size :	Document Number :	Rev : 0.1
Date: Friday, August 06, 2021	Sheet : 16 of 130	



Lenovo

Project Name : T14s Gen2	Title : CPU (13/16): CPU POWER (2/2)
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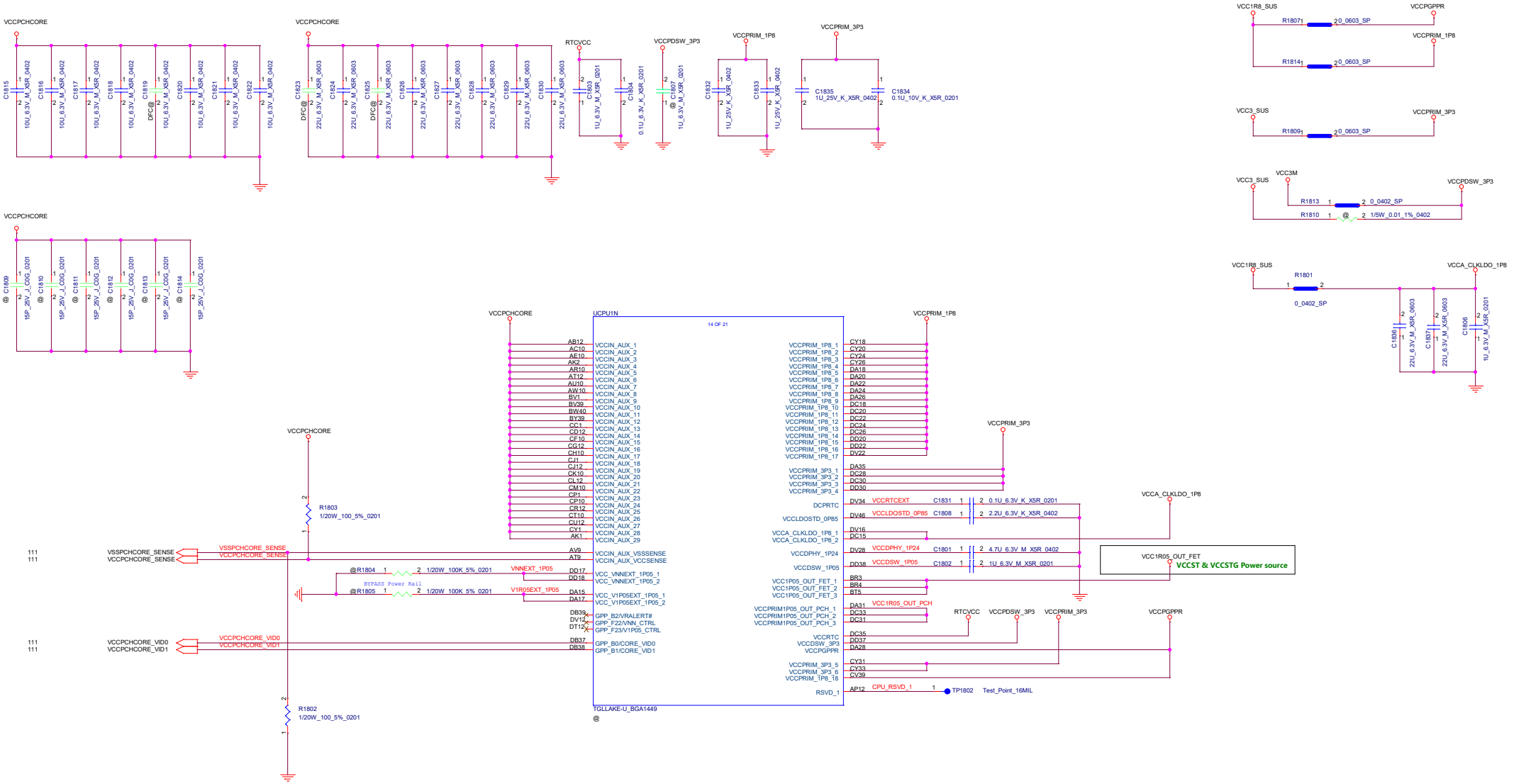

Project Name : T14s Gen2	Title : CPU (14/16): PCH POWER	
Size : C	Document Number :	Rev : 0.1
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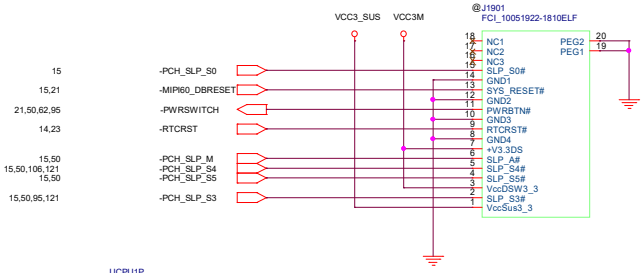
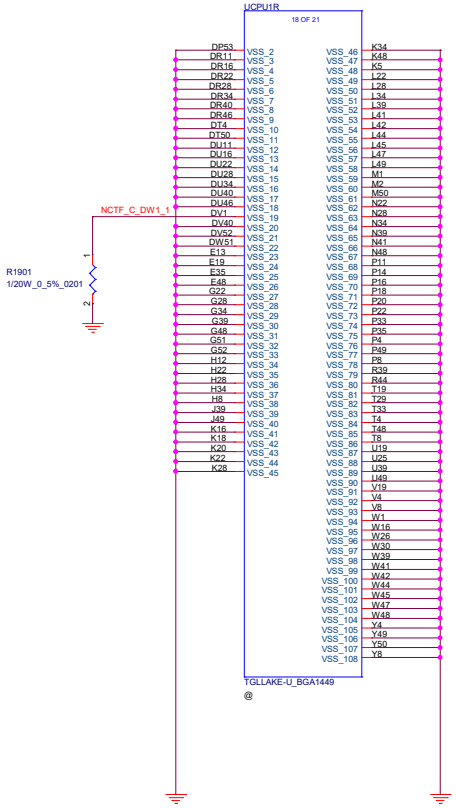
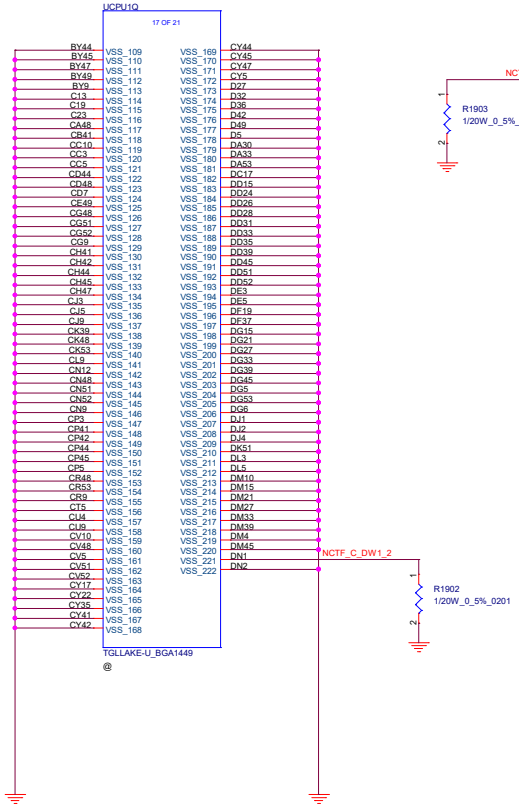
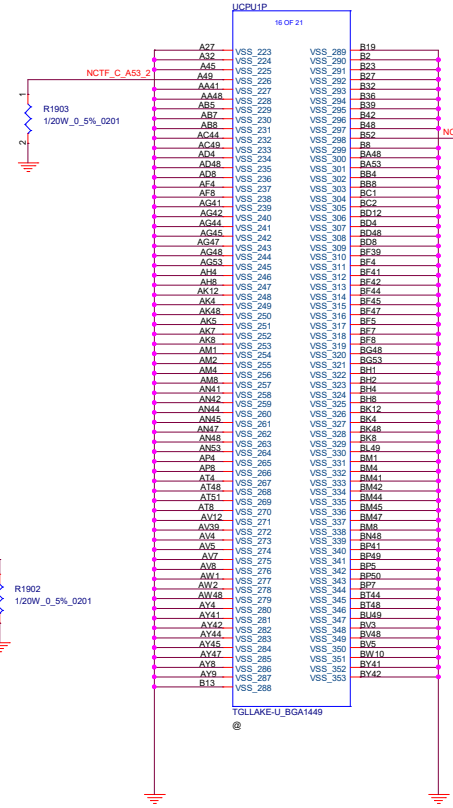
APS/PETS Interface









Lenovo

Project Name : T14s Gen2	Title : CPU (15/16): GND
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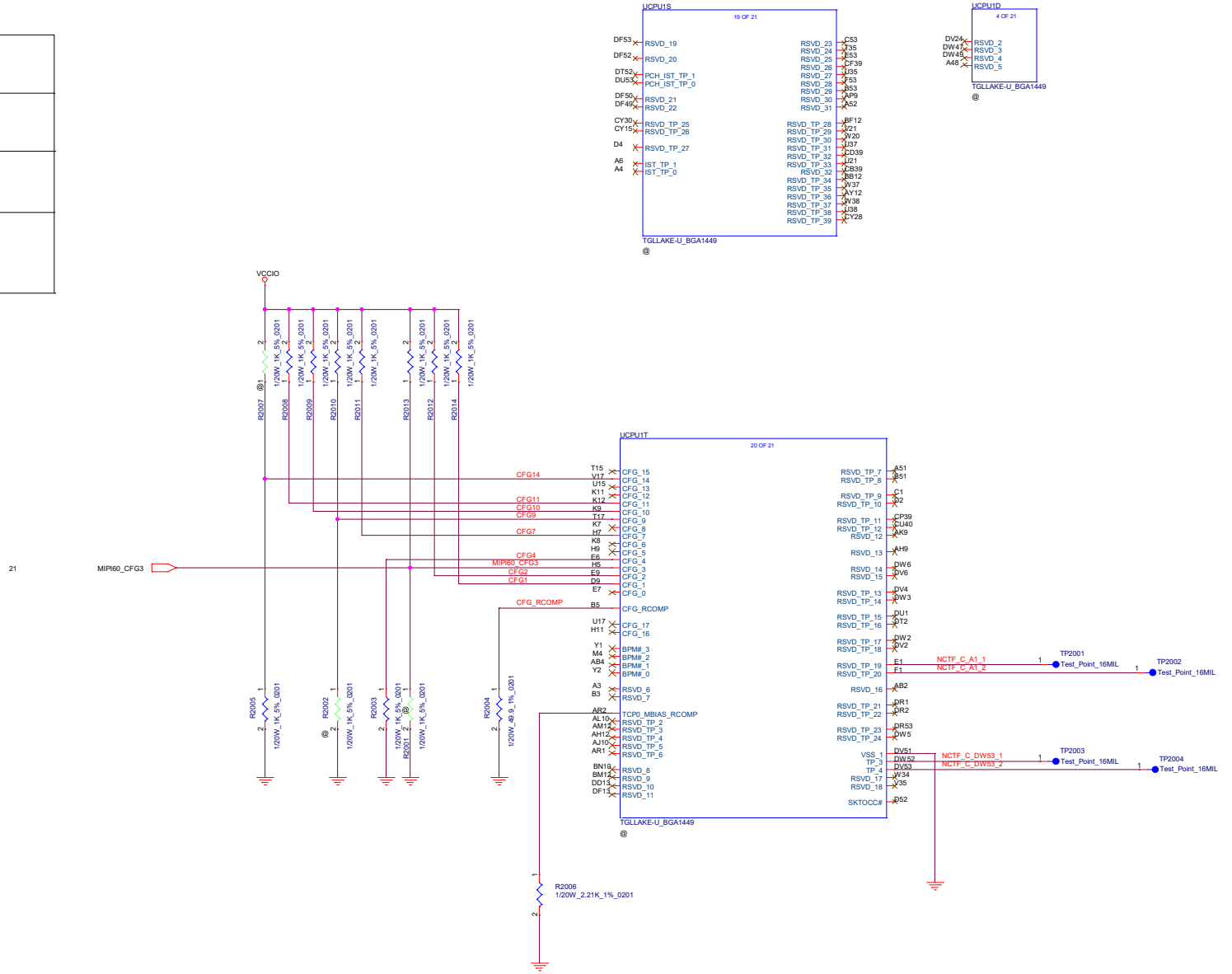
TABLE

CFG3: MSR Privacy Bit Feature **1: MSR (C80h) bit[0] setting** **0: MSR (C80h) bit[0] overridden**
CFG4: eDP Enable **1:Disabled** **0:Enabled**
CFG9: SVID Bus Communication **1:Enabled** **0:Disabled**
CFG14: PEG60 Lane Reversal **1:Normal** **0:Reversed**



Lenovo				
Project Name : T14s Gen2		Title : CPU (16/16): CFG/RESERVED		
Size :	Document Number :		Rev : 0.1	
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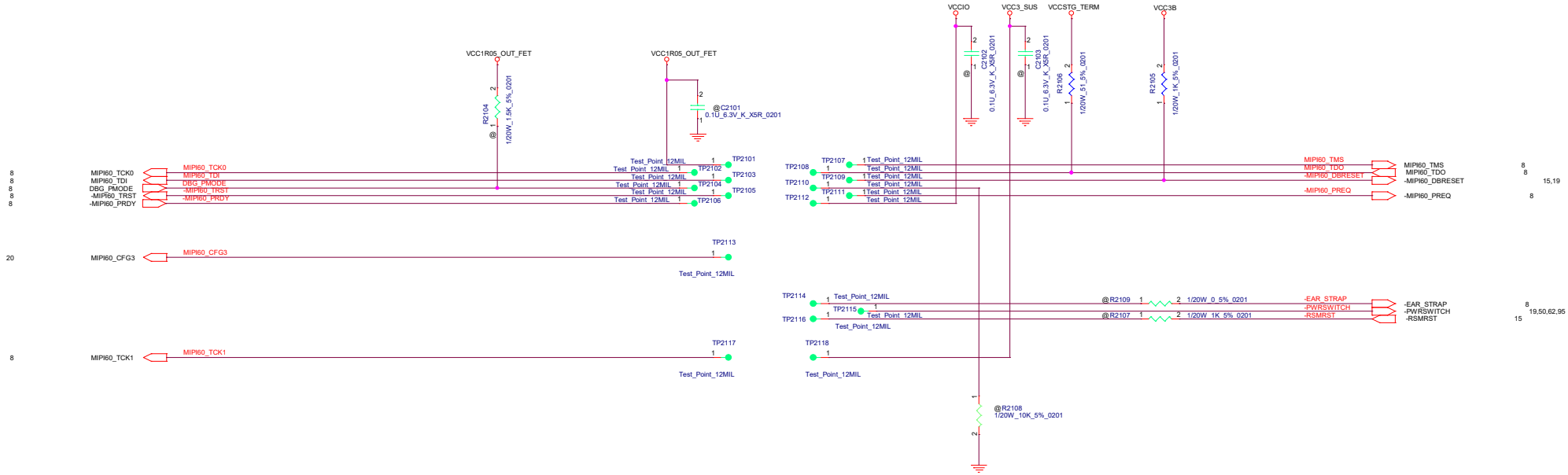

TABLE

Logic	Ref Des	MIPI60	DCI 2.0
Page8	R0808	ASM	NO_ASM
	R0809	ASM	NO_ASM
Page 20	R2001	ASM	NO_ASM
Page 22	J8	ASM	NO_ASM
	C2101	ASM	NO_ASM
	C2102	ASM	NO_ASM
	C2103	ASM	NO_ASM
	R2108	ASM	NO_ASM
	R2106	ASM	ASM
	R2105	ASM	ASM
	R2104	ASM	NO_ASM
	R2107	ASM	NO_ASM
	R2109	ASM	NO_ASM

LOGIC

Lenovo

Project Name : T14s Gen2	Title : MIPI60 DEBUG PORT
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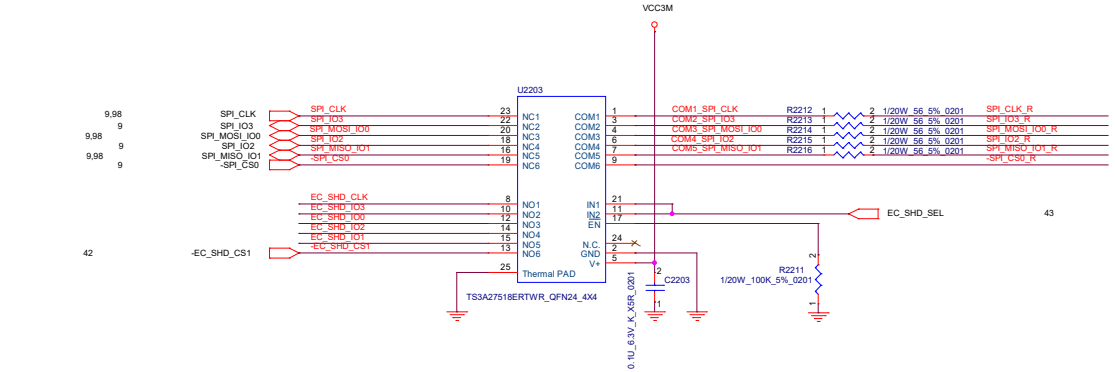
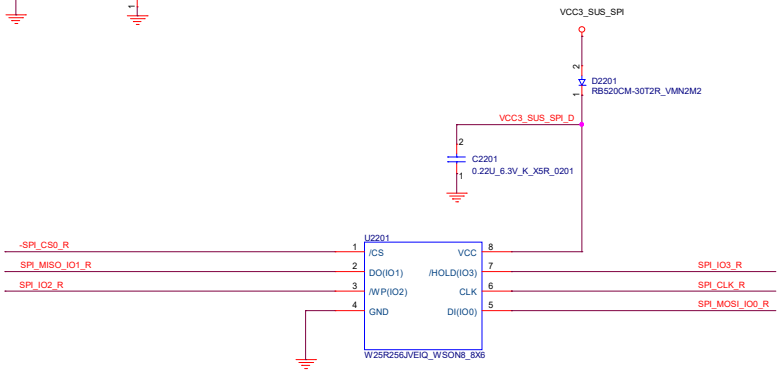




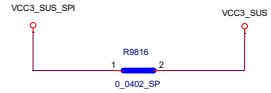


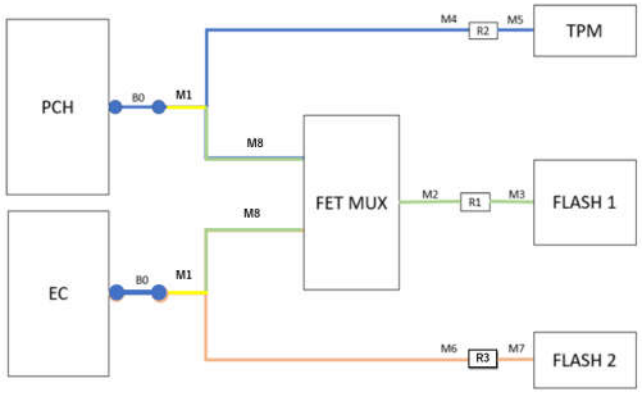
TABLE:U2201

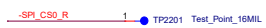
32MB (256Mb) 8x6mm WSON8		DUAL/QUAD SPI & RPMC
Winbond	W25R256JVEIQ	SA0000A1Q00
GigaDevice	GD25R256DYIGR	SA0000A1S00
Macronix	MX77L25650FZ4I42	SA0000A1R00

SIT-R changed as below
TABLE:U2201

32MB (256Mb) 8x6mm WSON8		DUAL/QUAD SPI & RPMC
Winbond	W25R256JVEIN	SA0000BND00
GigaDevice	GD25R256DYIGR	SA0000A1S00
Macronix	MX77L25650FZ4I42	SA0000A1R00

Delete in SOVP





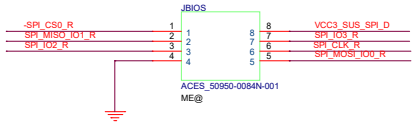


TABLE:JBIOS

WSON8 SPI FLASH SOCKET	
ACES	50950-0084N-001

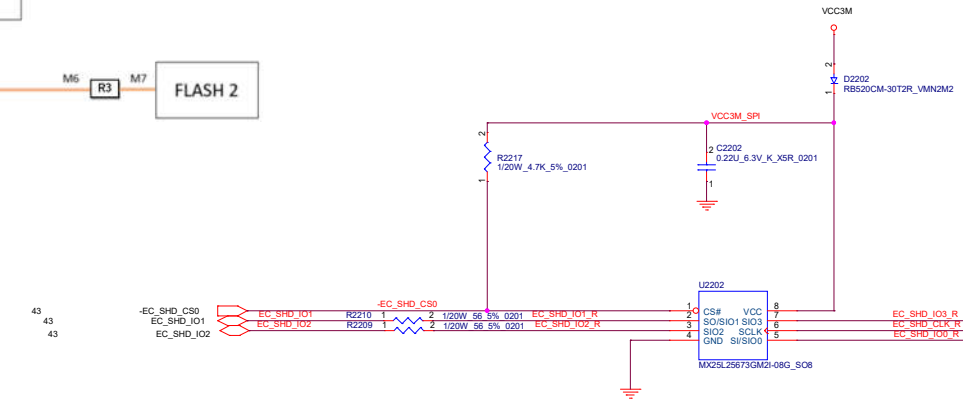


TABLE: U2202

32MB (256Mb) 200MIL SOIC8		
MACRONIX	MX25L25673GM2I-08G	SA00008J400
32MB (256Mb) 8x6mm WSON8		
WINBOND GIGADEVICE	W25Q256JVEIQ GD25B256DYIGR	SA00008WZ00 SA00009R800

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Project Name : T14s Gen2	Title : SPI FLASH
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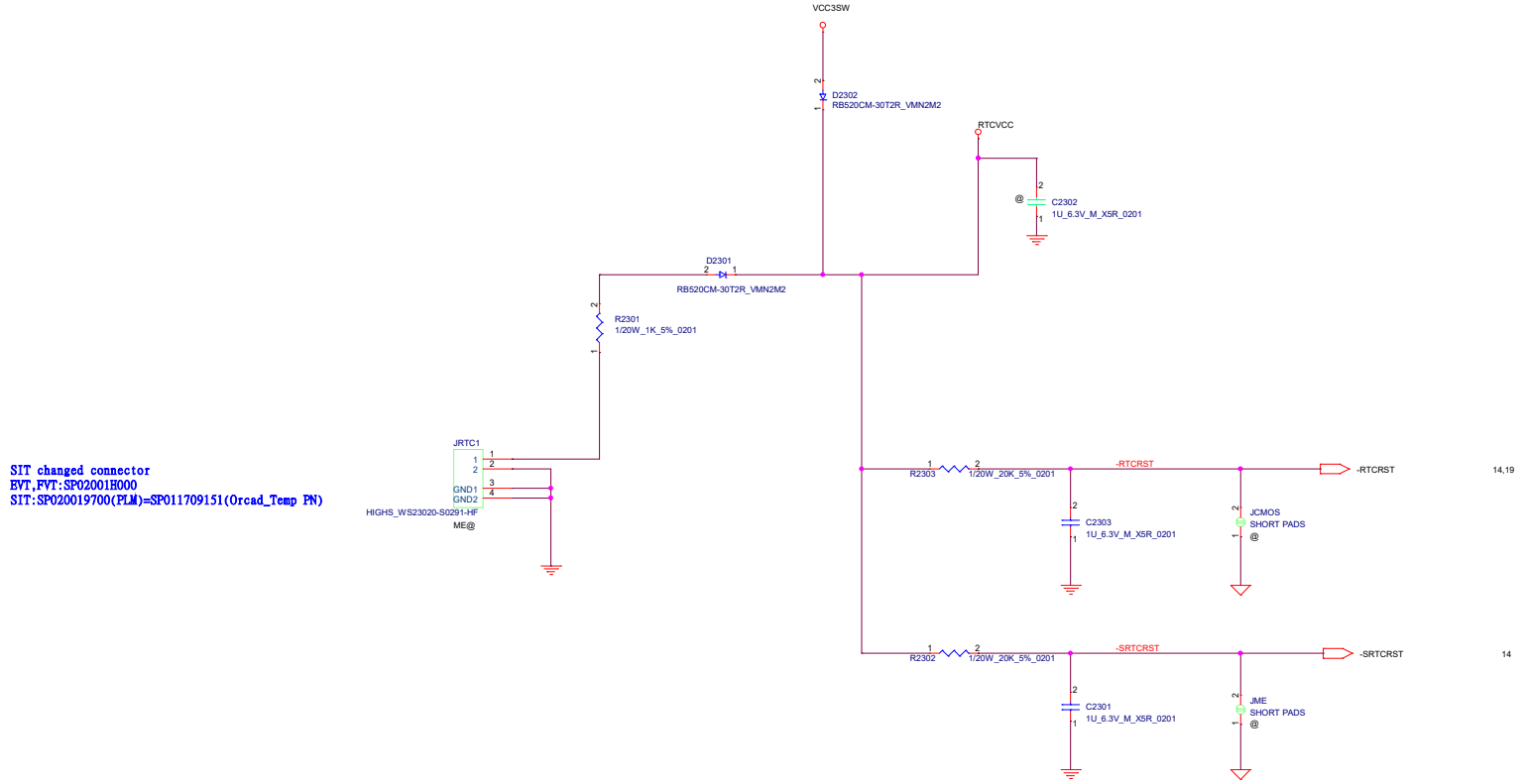

SIT changed connector
EVT,FVT:SP02001H000
SIT:SP020019700(PLM)=SP011709151(Orcad_Temp PN)

Project Name : T14s Gen2		Title : RTC BATTERY	
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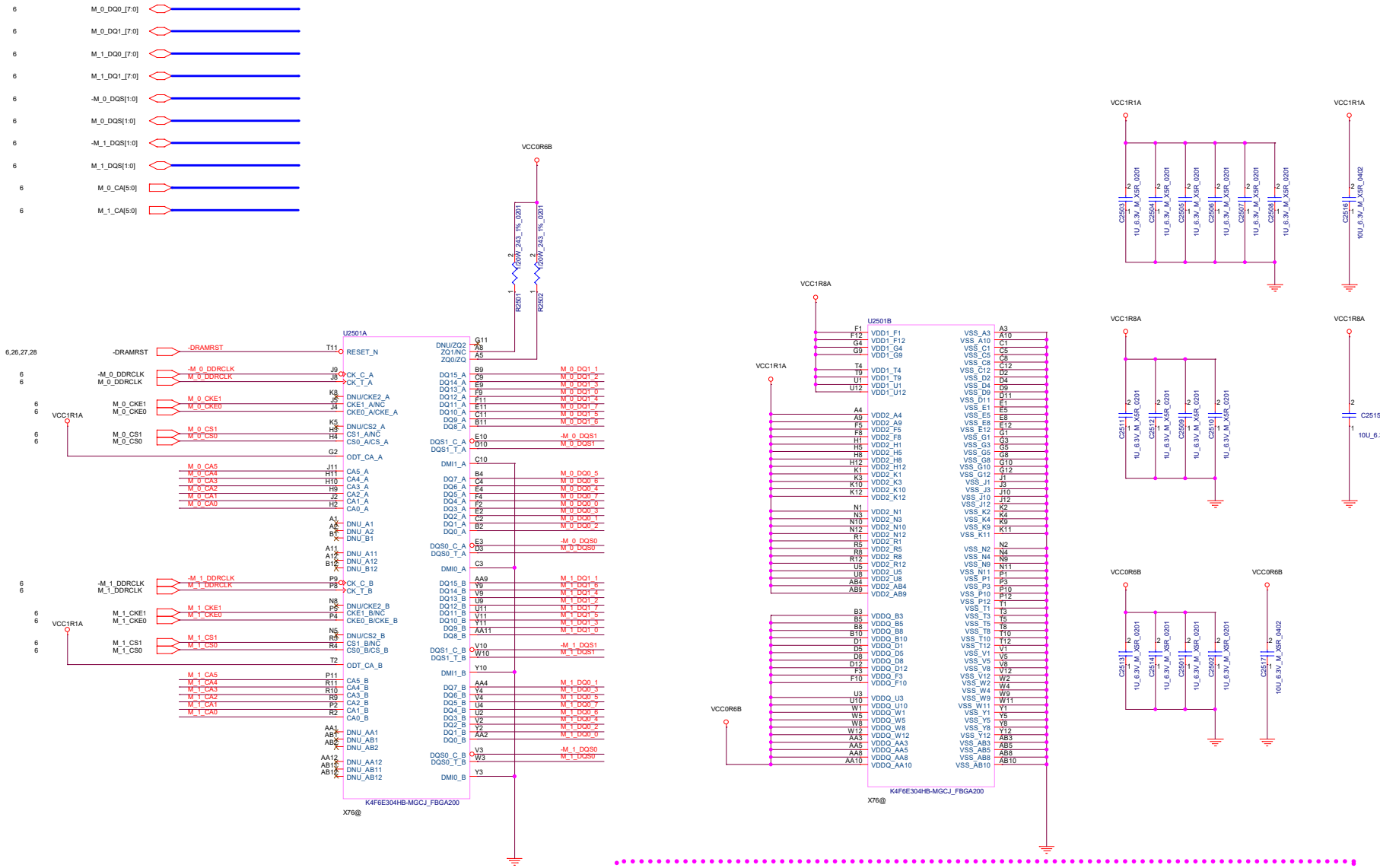

TABLE : LPDDR4x Source

Supplier	Capacity	Supplier's P/N	Package Size?		Die?	Device Configuration?	Memory
SK Hynix	16Gb	H9HCNNNBKMMLXR-NEE	10.0 x 15 .0 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	H9HCNNNCPMMLXR-NEE	10.0 x 15 .0 mm	QDP	8Gb (512Mx16x1Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	H9HCNNNFAMMLXR-NEE	10.0 x 15 .0 mm	ODP	8Gb (1Gx8x1Ch)	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	16Gb	K4U6E3S4AA-MGCR	10.0 x 15 .0 mm	SDP	16Gb (512Mx16x2Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	K4UBE3D4AA-MGCR	10.0 x 15 .0 mm	DDP	16Gb (512Mx16x2Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	K4UCE3Q4AA-MGCR	10.0 x 15 .0 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gb	MT53E512M32D2NP-046 WT:E	10.0 x 14 .5 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	MT53E1G32D2NP-046 WT:A	10.0 x 14 .5 mm	DDP	16Gb (T.B.D)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	MT53E2G32D4NQ-046 WT:A	10.0 x 14 .5 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB

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Project Name : T14s Gen2	Title : LPDDR4X CHANNEL 0&1
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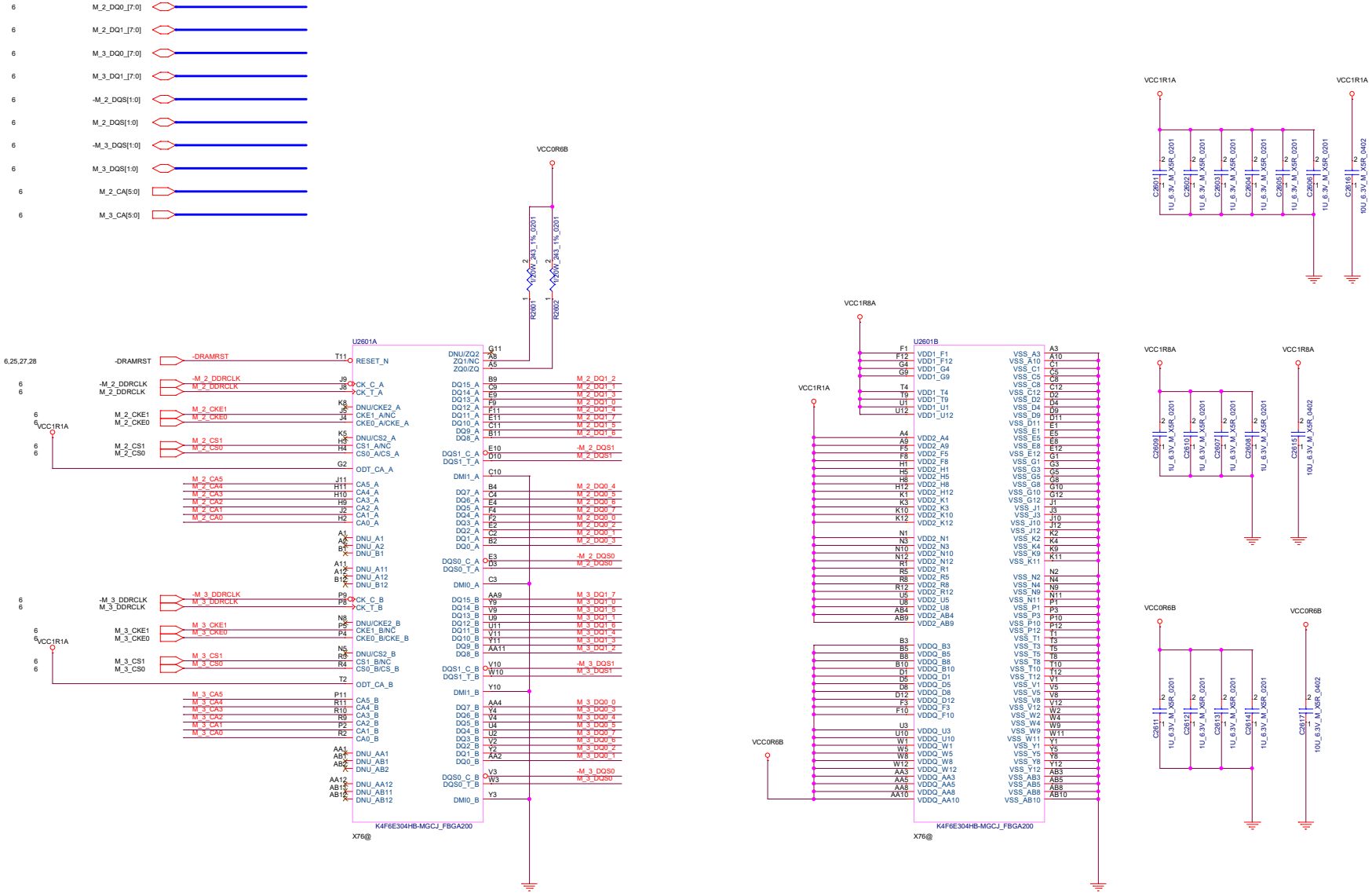

TABLE : LPDDR4x Source

Supplier	Capacity	Supplier's P/N	Package Size?		Die?	Device Configuration?	Memory
SK Hynix	16Gb	H9HCNNNBKMMLXR-NEE	10.0 x 15 .0 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	H9HCNNNCPMMLXR-NEE	10.0 x 15 .0 mm	QDP	8Gb (512Mx16x1Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	H9HCNNNFAMMLXR-NEE	10.0 x 15 .0 mm	ODP	8Gb (1Gx8x1Ch)	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	16Gb	K4U6E3S4AA-MGCR	10.0 x 15 .0 mm	SDP	16Gb (512Mx16x2Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	K4UBE3D4AA-MGCR	10.0 x 15 .0 mm	DDP	16Gb (512Mx16x2Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	K4UCE3Q4AA-MGCR	10.0 x 15 .0 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gb	MT53E512M32D2NP-046 WT:E	10.0 x 14 .5 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	MT53E1G32D2NP-046 WT:A	10.0 x 14 .5 mm	DDP	16Gb (T.B.D)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	MT53E2G32D4NQ-046 WT:A	10.0 x 14 .5 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB

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Project Name : T14s Gen2	Title : LPDDR4X CHANNEL 2&3
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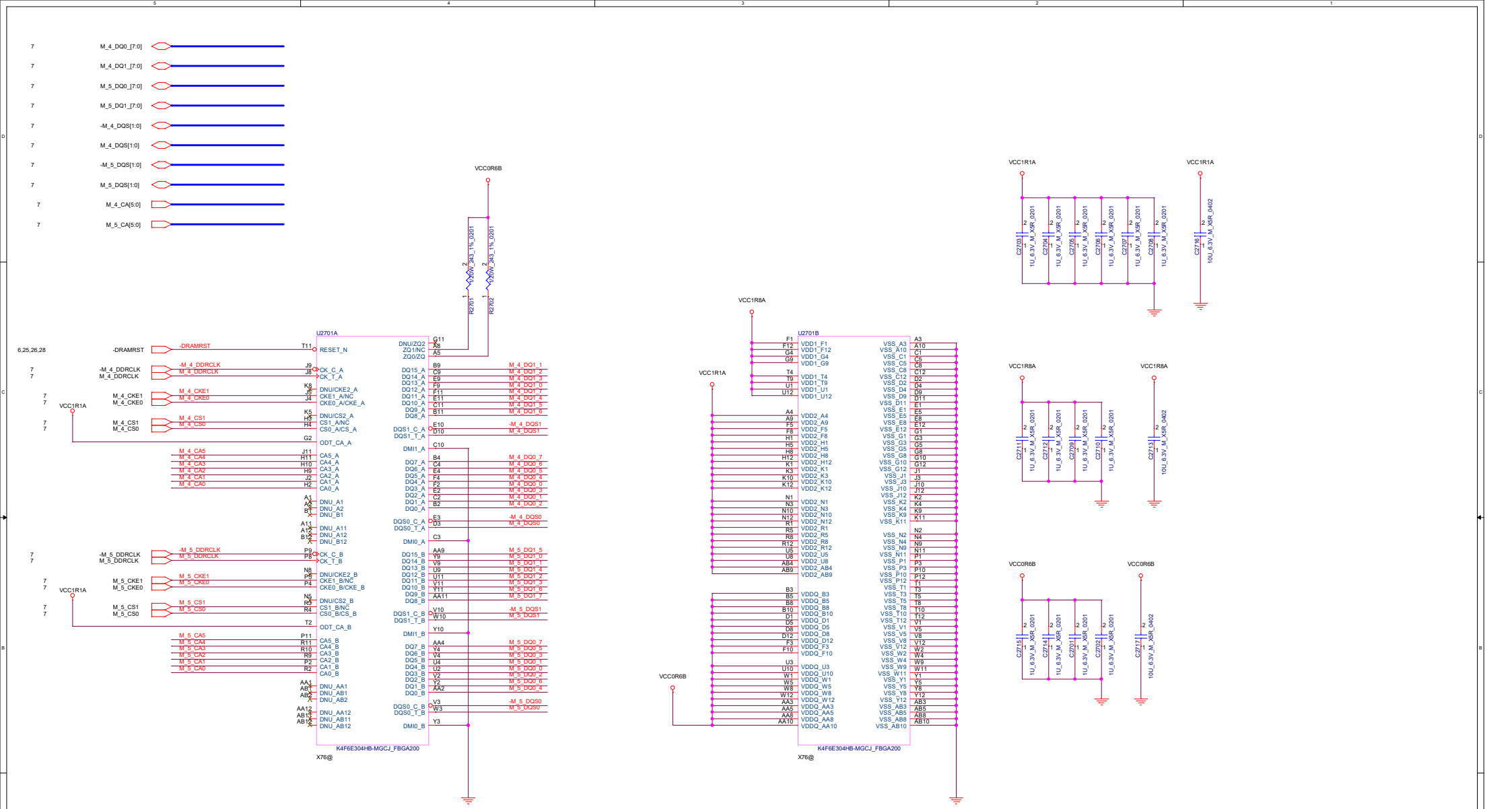

TABLE : LPDDR4x Source

Supplier	Capacity	Supplier's P/N	Package Size?		Die?	Device Configuration?	Memory
SK Hynix	16Gb	H9HCNNNBKMMLXR-NEE	10.0 x 15 .0 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	H9HCNNNCPMMLXR-NEE	10.0 x 15 .0 mm	QDP	8Gb (512Mx16x1Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	H9HCNNNFAMMLXR-NEE	10.0 x 15 .0 mm	ODP	8Gb (1Gx8x1Ch)	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	16Gb	K4U6E3S4AA-MGCR	10.0 x 15 .0 mm	SDP	16Gb (512Mx16x2Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	K4UBE3D4AA-MGCR	10.0 x 15 .0 mm	DDP	16Gb (512Mx16x2Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	K4UCE3Q4AA-MGCR	10.0 x 15 .0 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gb	MT53E512M32D2NP-046 WT:E	10.0 x 14 .5 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	MT53E1G32D2NP-046 WT:A	10.0 x 14 .5 mm	DDP	16Gb (T.B.D)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	MT53E2G32D4NQ-046 WT:A	10.0 x 14 .5 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB

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Project Name : T14s Gen2	Title : LPDDR4X CHANNEL 4&5
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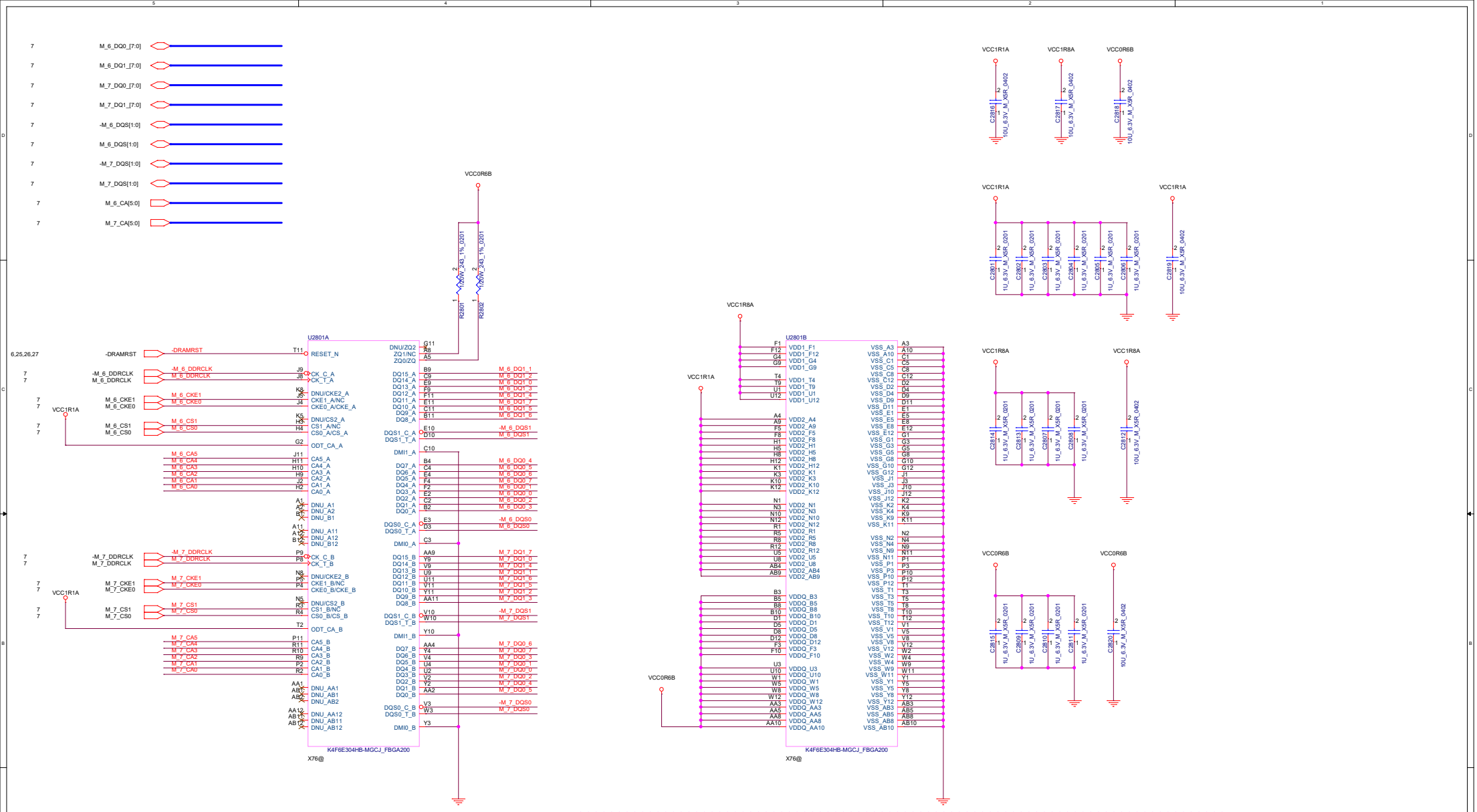

TABLE : LPDDR4x Source

Supplier	Capacity	Supplier's P/N	Package Size?		Die?	Device Configuration?	Memory
SK Hynix	16Gb	H9HCNNNBKMMLXR-NEE	10.0 x 15 .0 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	H9HCNNNCPMMLXR-NEE	10.0 x 15 .0 mm	QDP	8Gb (512Mx16x1Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	H9HCNNNFAMMLXR-NEE	10.0 x 15 .0 mm	ODP	8Gb (1Gx8x1Ch)	2 Rank x (1Gx16) x 2 Ch	32GB
Samsung	16Gb	K4U6E3S4AA-MGCR	10.0 x 15 .0 mm	SDP	16Gb (512Mx16x2Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	K4UBE3D4AA-MGCR	10.0 x 15 .0 mm	DDP	16Gb (512Mx16x2Ch)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	K4UCE3Q4AA-MGCR	10.0 x 15 .0 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB
Micron	16Gb	MT53E512M32D2NP-046 WT:E	10.0 x 14 .5 mm	DDP	8Gb (512Mx16x1Ch)	1 Rank x (512Mx16) x 2 Ch	8GB
	32Gb	MT53E1G32D2NP-046 WT:A	10.0 x 14 .5 mm	DDP	16Gb (T.B.D)	2 Rank x (512Mx16) x 2 Ch	16GB
	64Gb	MT53E2G32D4NQ-046 WT:A	10.0 x 14 .5 mm	QDP	16Gb (T.B.D)	2 Rank x (1Gx16) x 2 Ch	32GB

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Project Name : T14s Gen2	Title : LPDDR4X CHANNEL 6&7
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Project Name : T14s Gen2	Title : PWR SW/PEN CHARGER INTERFACE
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Project Name : T14s Gen2	Title : HDMI CONNECTOR
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Project Name : T14s Gen2	Title : THUNDERBOLT RETIMER B (1/2)	
Size : C	Document Number :	Rev : 0.1
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Project Name : T14s Gen2	Title : THUNDERBOLT RETIMER B (2/2)	
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Project Name : T14s Gen2	Title : THUNDERBOLT RETIMER C (1/2)
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Project Name : T14s Gen2	Title : THUNDERBOLT RETIMER C (2/2)	
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Project Name : T14s Gen2	Title : USB PD CONTROLLER
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Project Name : T14s Gen2	Title : THUNDERBOLT CONNECTOR	
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Project Name : T14s Gen2	Title : USB TYPE-A CONNECTOR
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Title	<Title>		
Size: Custom	Document Number: T14s Gen2		Rev: 0.1
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Title	<Title>		
Size	Document Number		Rev
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Project Name : T14s Gen2	Title : BLANK
Size : C	Document Number :
Rev : 0.1	
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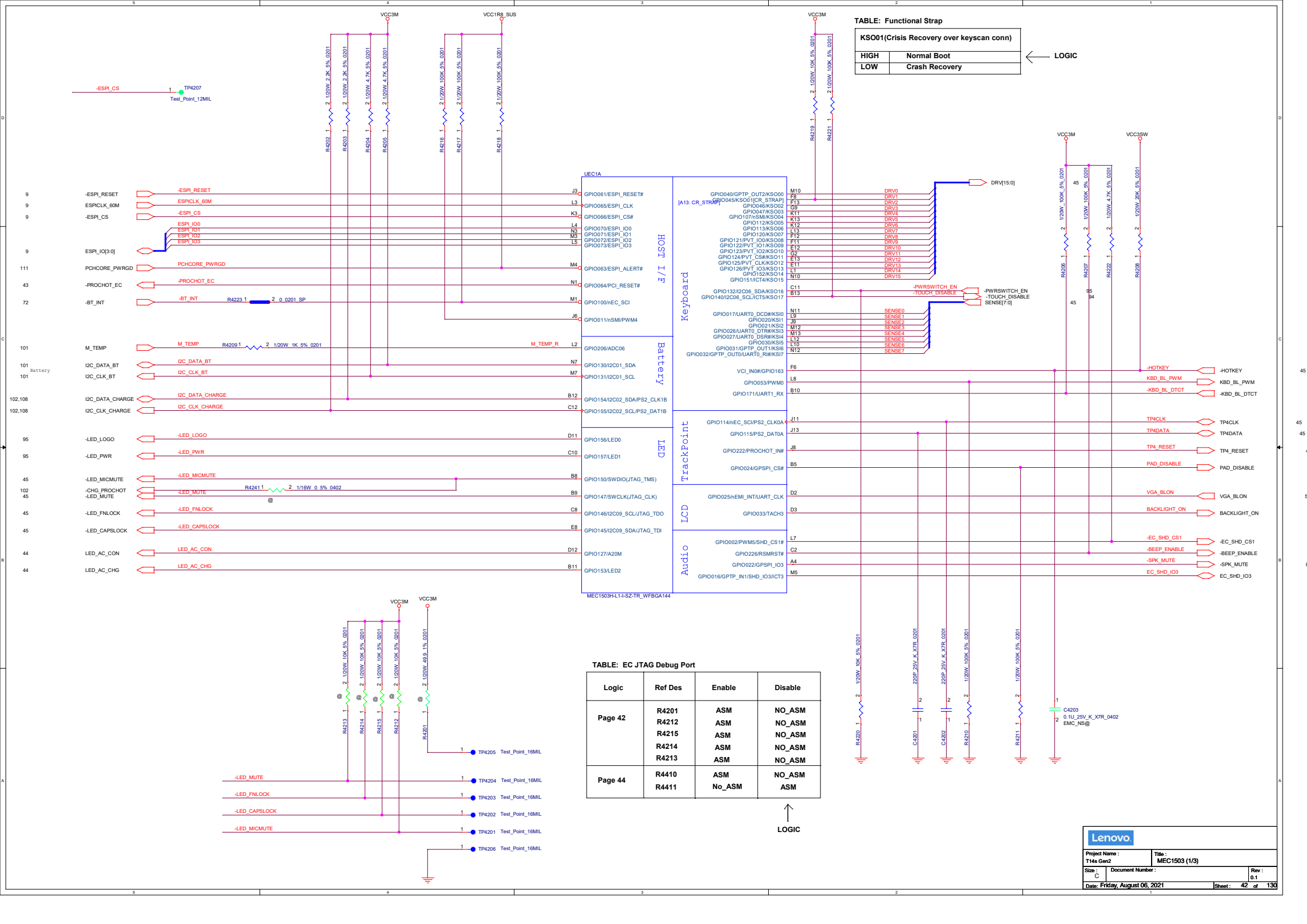
TABLE: Functional Strap
KSO01(Crisis Recovery over keyscan conn)
HIGH Normal Boot
LOW Crash Recovery
LOGIC
UEC1A
HOST I/F
Keyboard
Battery
LED
TrackPoint
LCD
Audio
MEC1503H-L1-I-SZ-TR_WFBGA144
TABLE: EC JTAG Debug Port
Logic
Ref Des
Enable
Disable
Page 42
R4201 R4212 R4215 R4214 R4213
ASM ASM ASM ASM ASM
NO_ASM NO_ASM NO_ASM NO_ASM NO_ASM
Page 44
R4410 R4411
ASM No_ASM
NO_ASM ASM
LOGIC
Lenovo
Project Name : T14s Gen2
Title : MEC1503 (1/3)
Size : C
Document Number :
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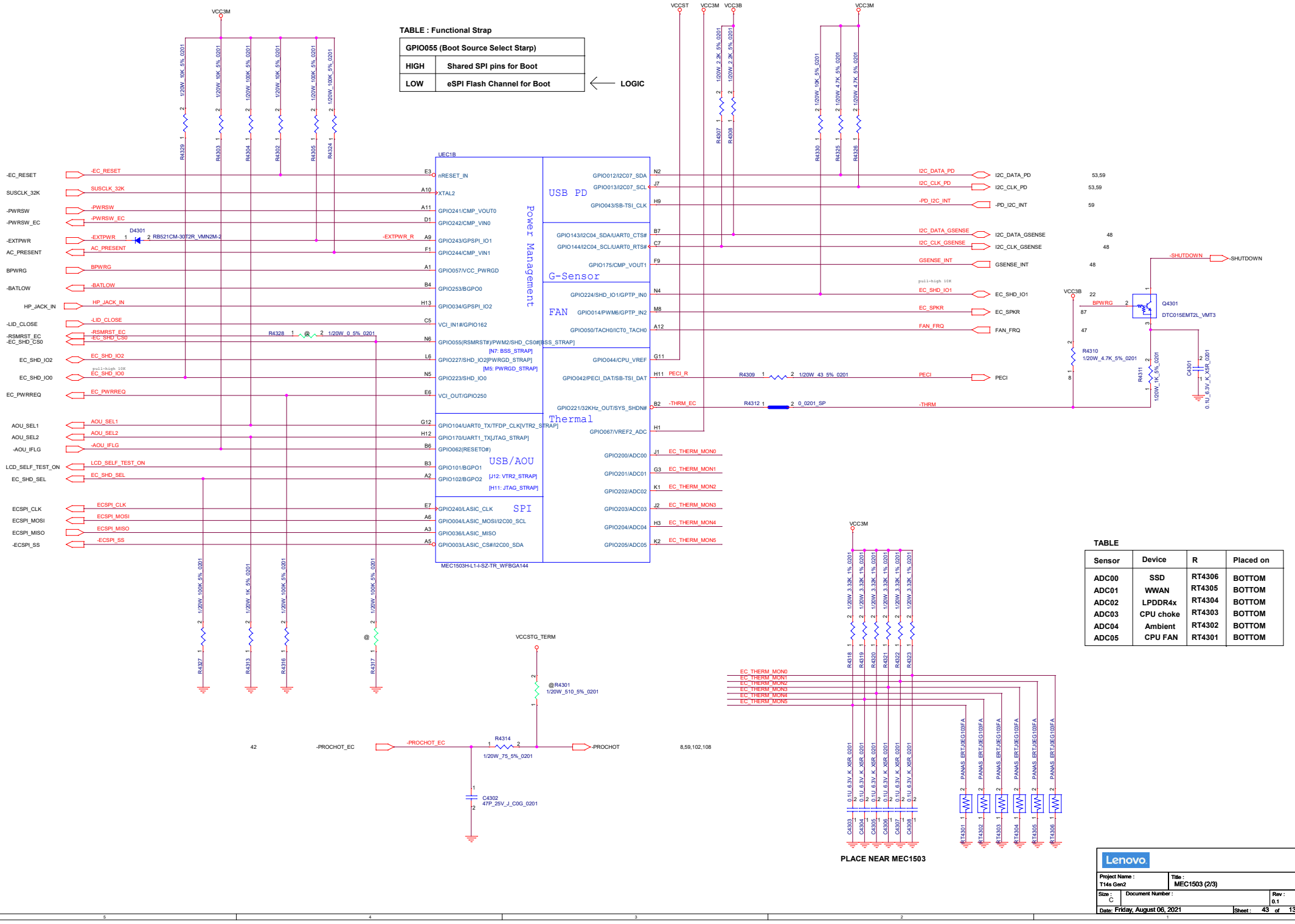

TABLE

Sensor	Device	R	Placed on
ADC00	SSD	RT4306	BOTTOM
ADC01	WWAN	RT4305	BOTTOM
ADC02	LPDDR4x	RT4304	BOTTOM
ADC03	CPU choke	RT4303	BOTTOM
ADC04	Ambient	RT4302	BOTTOM
ADC05	CPU FAN	RT4301	BOTTOM

Project Name : T14s Gen2	Title : MEC1503 (2/3)
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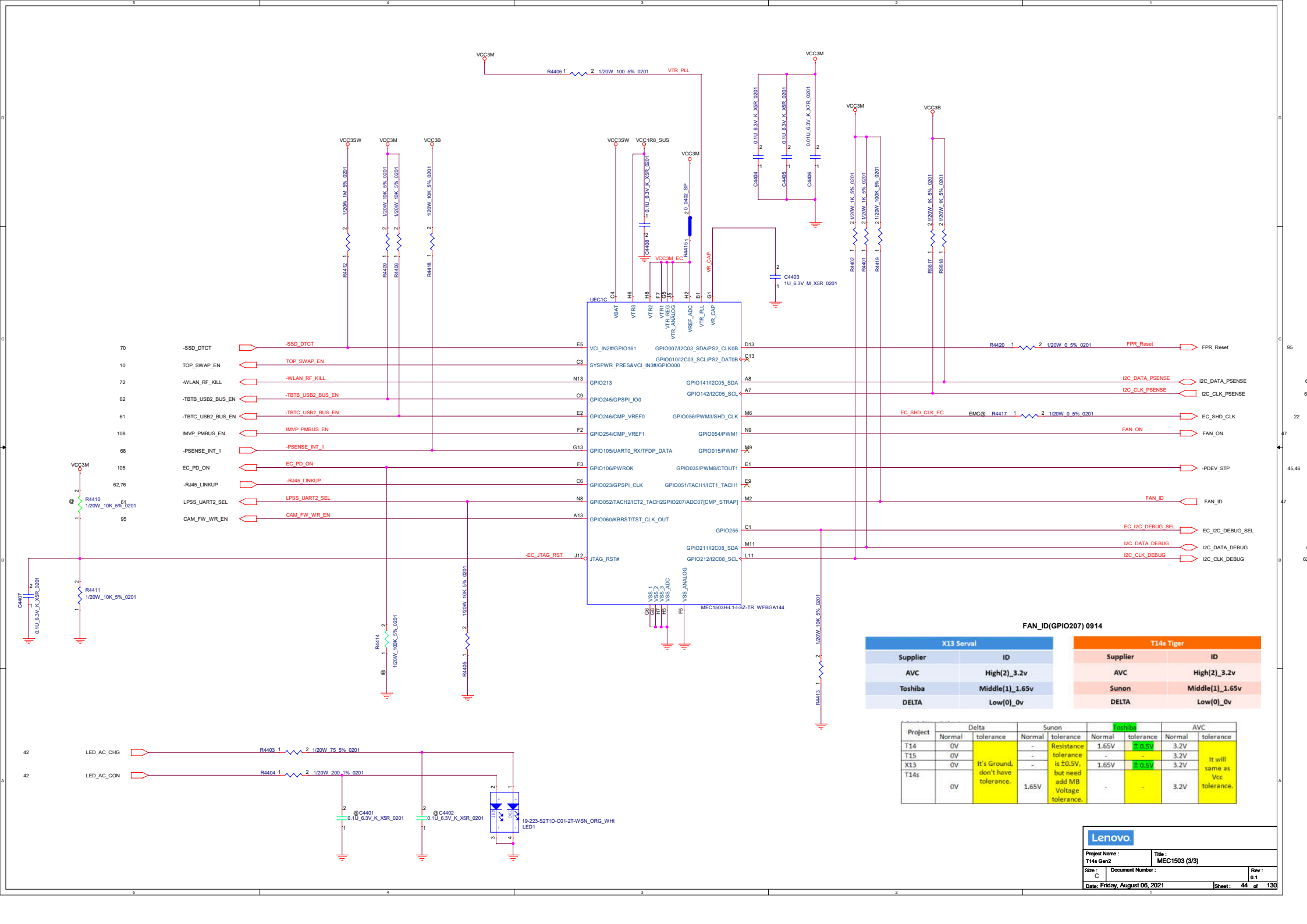

FAN_ID(GPIO207) 0914

X13 Serval	
Supplier	ID
AVC	High(2)_3.2v
Toshiba	Middle(1)_1.65v
DELTA	Low(0)_0v

T14s Tiger	
Supplier	ID
AVC	High(2)_3.2v
Sunon	Middle(1)_1.65v
DELTA	Low(0)_0v

Project	Delta		Sunon		Toshiba		AVC	
	Normal	tolerance	Normal	tolerance	Normal	tolerance	Normal	tolerance
T14	0V	It's Ground, don't have tolerance.	-	Resistance tolerance is ±0.5V, but need add MB Voltage tolerance.	1.65V	± 0.5V	3.2V	It will same as Vcc tolerance.
T15	0V		-		-	-	3.2V	
X13	0V		-		1.65V	± 0.5V	3.2V	
T14s	0V		1.65V		-	-	3.2V	

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Project Name : T14s Gen2	Title : MEC1503 (3/3)
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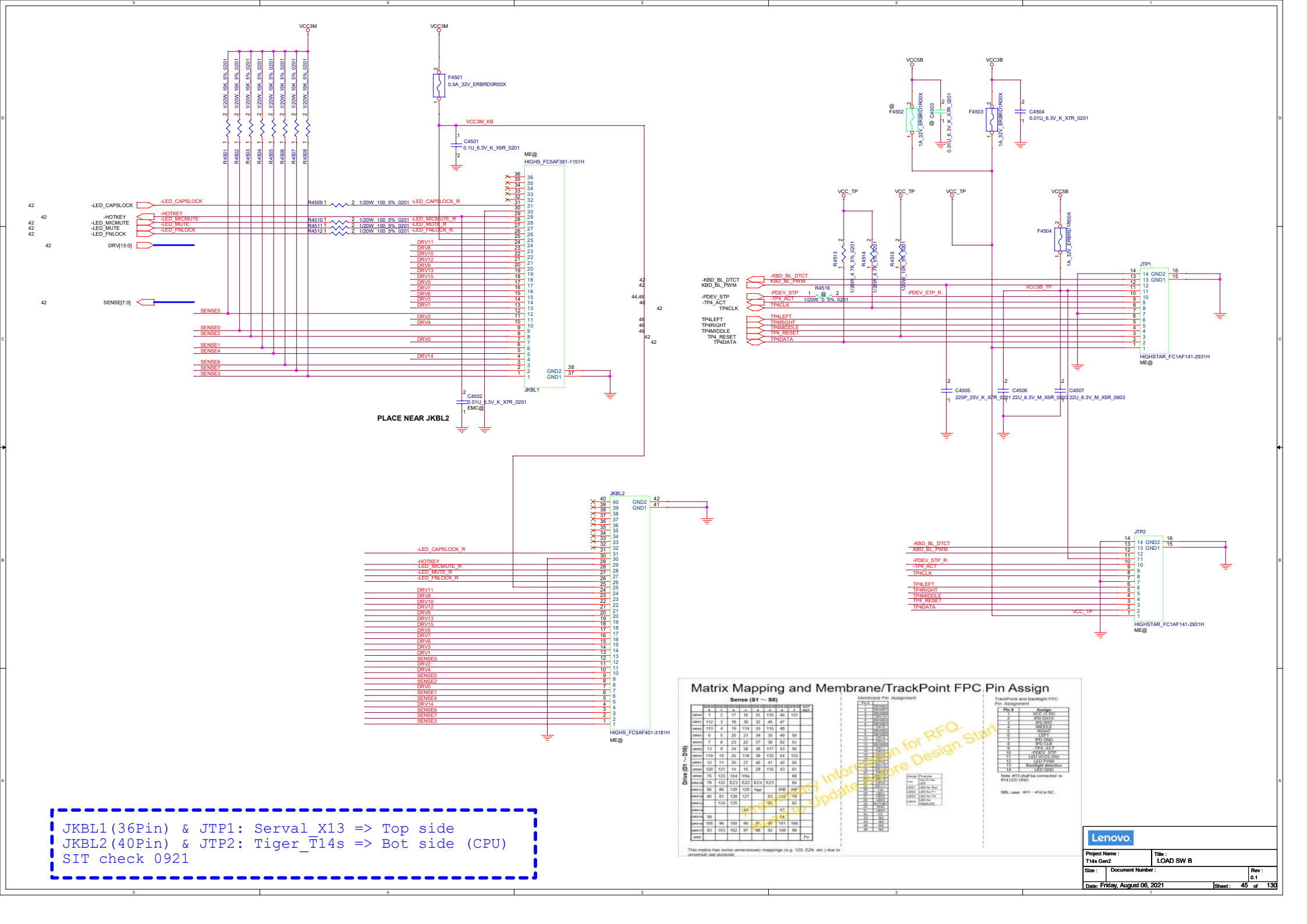

JKBL1(36Pin) & JTP1: Serval_X13 => Top side
JKBL2(40Pin) & JTP2: Tiger_T14s => Bot side (CPU)
SIT check 0921

Project Name : T14s Gen2	Title : LOAD SW B
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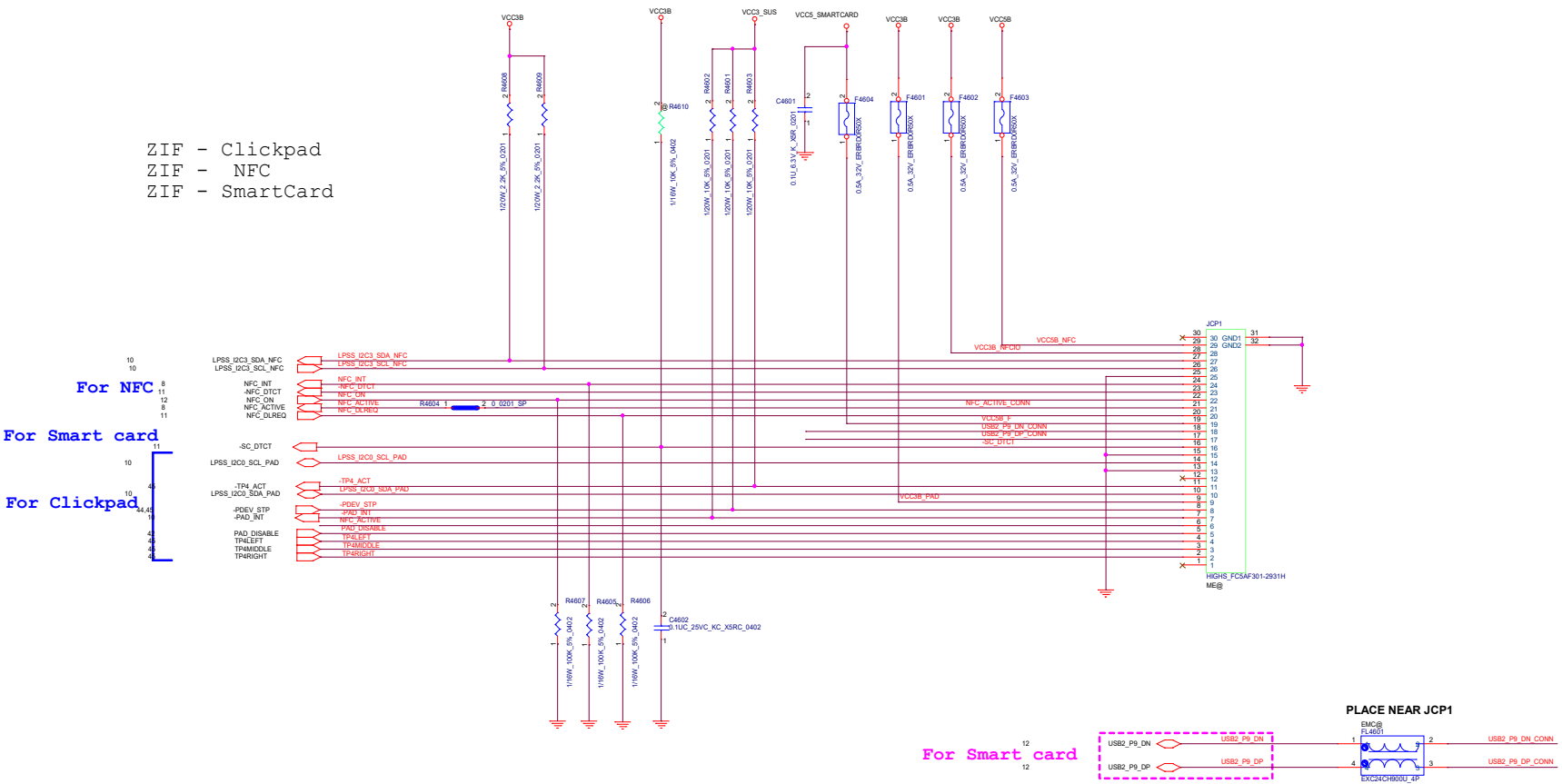
ZIF - Clickpad
ZIF - NFC
ZIF - SmartCard



For NFC 05/09 OK

Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C _SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

For Clickpad 05/09 OK

Original pin assign

Name	Pin#	Type	Function
GND	1	Power	Signal Ground
I2C_CLK	2	IN/OUT	I2C Clock to System I2C I/F on CPU/PCH
IPD_GND	3	IN	TrackPoint ground
NC	4		
-TP4_ACT	5	IN	TrackPoint Activity status. Please refer to "4.2.8"
I2C_DAT	6	IN/OUT	I2C Data to System I2C I/F on CPU/PCH
VDD	7	Power	Supply power from system. Power is not supplied when system is in S3, S4, S5 and G5 state. (Refer to electrical requirement)
- PDEV_STP	8	IN	This signal is used to disable to report button status and finger status to system when system LCD lid is closed or is in Tent /Stand /Tablet modes (Yoga case). Please refer to "4.2.5-PDEV_STP"
-I2C_INT	9	OUT	Interrupt for I2C communication
NFC_Active	10	IN	This signal should use if NFC Antenna is implemented under touch pad PCBA. This signal should be NC or not be used in touch pad PCBA if NFC antenna is not implemented under touch pad PCBA. Please refer to "4.2.6 NFC_Active"
PAD_DISABLE	11	IN	This signal is used to disable touch pad. Please refer to "4.2.4 PAD_DISABLE".
TP4LEFT	12	IN	TrackPoint button signal
TP4MIDDLE	13	IN	TrackPoint button signal
TP4RIGHT	14	IN	TrackPoint button signal

For Smart card 05/09 OK

PIN ASSIGNMENT	
PIN #	DESCRIPTION
#1	VCC +5V
#2	USB D–
#3	USB D+
#4	GND
#5	NC
#6	GND

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Project Name : T14s Gen2	Title : TOUCH PAD/Smart card/NFC
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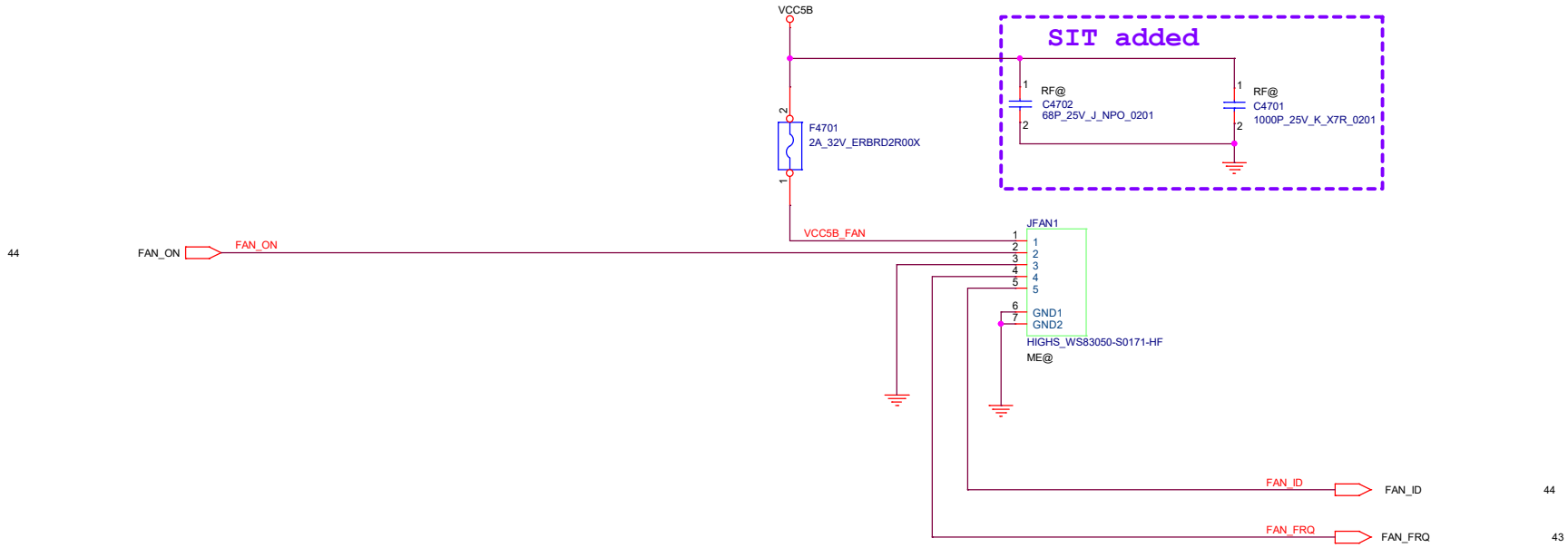

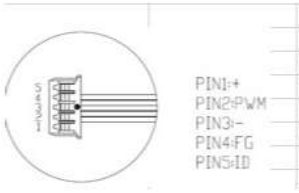

Pin No.	Signal	Note	Color
1	VCC	+5V	Black
2	PWM	PWM	Black
3	GND	–	Black
4	FG	2 Pulses	Black
5	ID	Fan ID	Black
--	–		

Security Classification	LC Future Center Secret Data		
Issued Date	2018/01/12	Deciphered Date	2018/01/12

Title: ***FAN CONNECTOR***

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TABLE : U4801

P/N	ADDR_SEL	Address
LIS2DWLTR	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX022-1020	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)
BMA280	H L	32h (W) & 33h (R) 30h (W) & 31h (R)

ST and Bosch I2C address is same but can be identified by Chip_ID

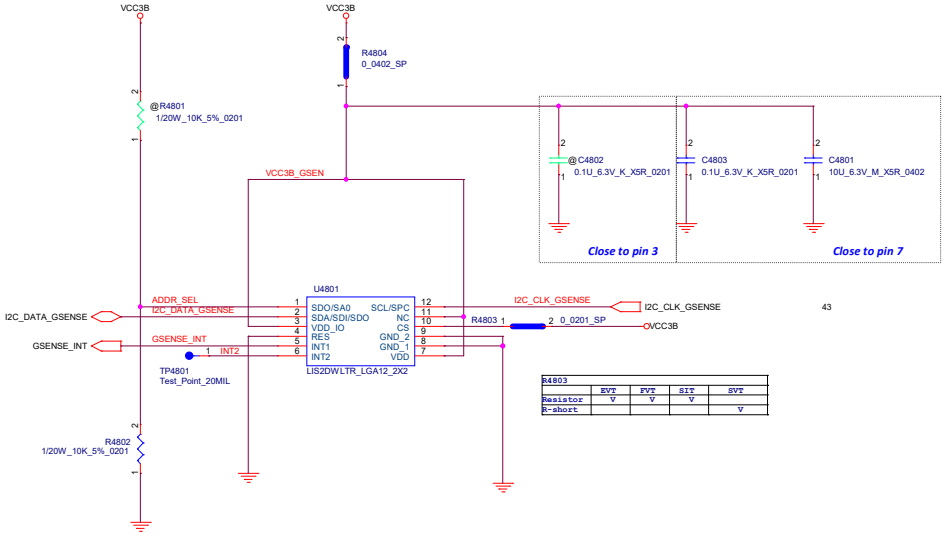
TABLE of G-Sensor (U4801)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00
BOSCH	BMA280	SA0000A1600

Table 2. Pin description

Pin#	Name	Function
1	SDO SA0	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)
2	SDA SDI SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
3	Vdd_IO	Power supply for I/O pins
4	RES	Connect to GND
5	INT1	Interrupt pin 1
6	INT2	Interrupt pin 2
7	Vdd	Power supply
8	GND	0 V supply
9	GND	0 V supply
10	CS	SPI enable I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
11	NC	Internally not connected. Can be tied to VDD, VDDIO, or GND.
12	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)

TABLE : G-Sensor Power

HDD Support	VCC3M
SSD Only	VCC3B



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Project Name : T14s Gen2	Title : APS G-SENSOR
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Project Name : T14s Gen2	Title : dGPU	
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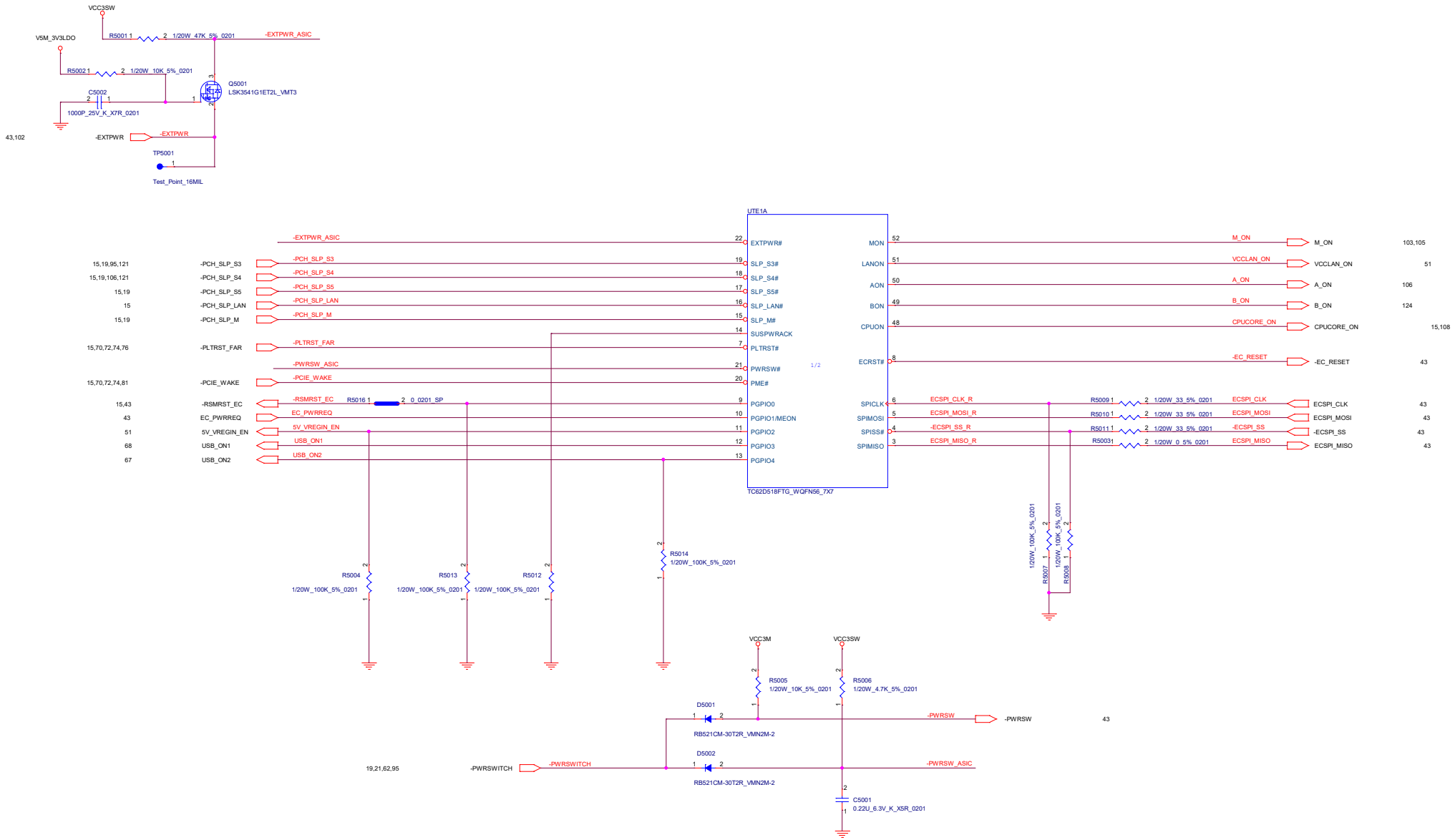

Project Name : T14s Gen2		Title : THINK ENGINE 3 (1/2)	
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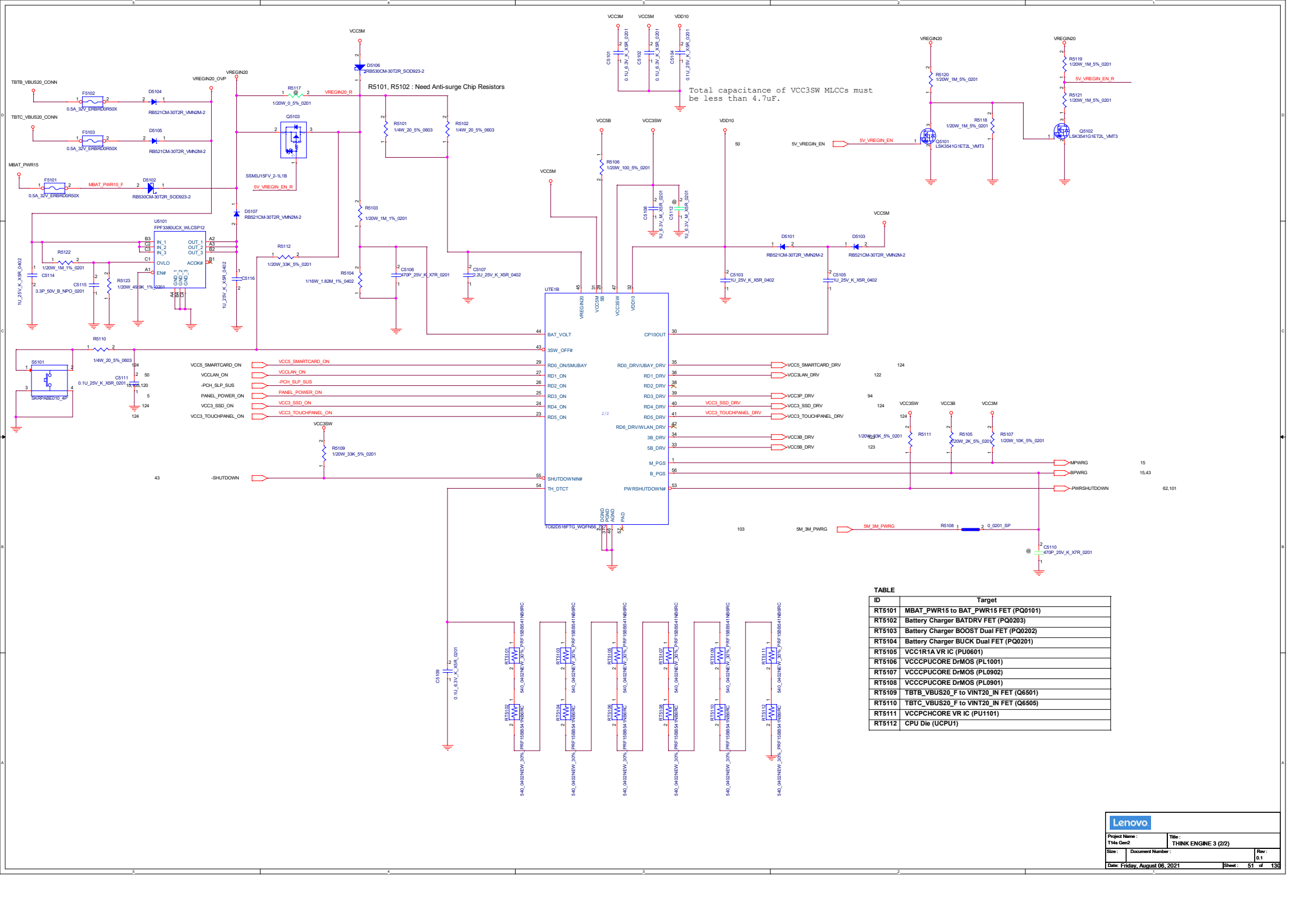

TABLE

ID	Target
RT5101	MBAT_PWR15 to BAT_PWR15 FET (PQ0101)
RT5102	Battery Charger BATDRV FET (PQ0203)
RT5103	Battery Charger BOOST Dual FET (PQ0202)
RT5104	Battery Charger BUCK Dual FET (PQ0201)
RT5105	VCC1R1A VR IC (PU0601)
RT5106	VCCCPUCORE DrMOS (PL1001)
RT5107	VCCCPUCORE DrMOS (PL0902)
RT5108	VCCCPUCORE DrMOS (PL0901)
RT5109	TBTB_VBUS20_F to VINT20_IN FET (Q6501)
RT5110	TBTC_VBUS20_F to VINT20_IN FET (Q6505)
RT5111	VCCPCHCORE VR IC (PU1101)
RT5112	CPU Die (UCPU1)

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Project Name : T14s Gen2	Title : THINK ENGINE 3 (2/2)
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Project Name : T14s Gen2	Title : dGPU	
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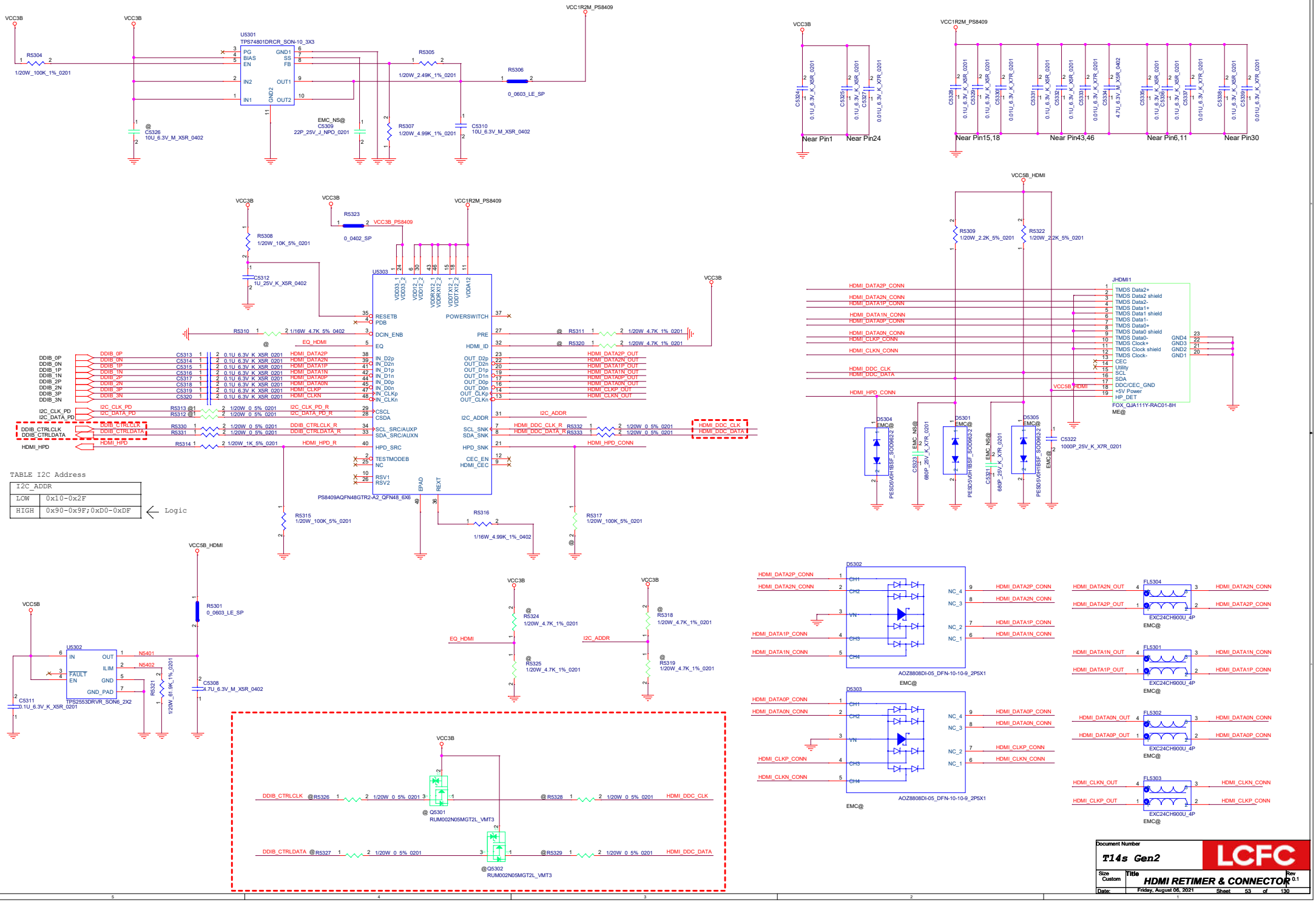
VCC3B
VCC1R2M_PS8409
U5301
TPS74801DRCR_SON-10_3X3
R5304
1/20W_100K_1%_0201
R5305
1/20W_2.49K_1%_0201
R5306
0_0603_LE_SP
C5326
10U_6.3V_M_X5R_0402
EMC_NS@
C5309
22P_25V_J_NPO_0201
R5307
1/20W_4.99K_1%_0201
C5310
10U_6.3V_M_X5R_0402
C5324
C5325
C5327
0.1U_6.3V_K_X5R_0201
0.01U_6.3V_K_X7R_0201
Near Pin1
Near Pin24
C5328
C5329
C5330
C5331
C5332
C5333
C5334
C5335
C5336
C5337
C5338
C5339
4.7U_6.3V_M_X5R_0402
Near Pin15,18
Near Pin43,46
Near Pin6,11
Near Pin30
R5308
1/20W_10K_5%_0201
C5312
1U_25V_K_X5R_0402
R5323
0_0402_SP
VCC3B_PS8409
U5303
VDD33_1
VDD33_2
VDD12_1
VDD12_2
VDDRX12_1
VDDRX12_2
VDDTX12_1
VDDTX12_2
VDDA12
RESETB
PDB
DCIN_ENB
EQ
PRE
HDMI_ID
POWERSWITCH
IN_D2p
IN_D2n
IN_D1p
IN_D1n
IN_D0p
IN_D0n
IN_CLKp
IN_CLKn
OUT_D2p
OUT_D2n
OUT_D1p
OUT_D1n
OUT_D0p
OUT_D0n
OUT_CLKp
OUT_CLKn
CSCL
CSDA
SCL_SRC/AUXP
SDA_SRC/AUXN
HPD_SRC
TESTMODEB
NC
RSV1
RSV2
SCL_SNK
SDA_SNK
HPD_SNK
CEC_EN
HDMI_CEC
I2C_ADDR
EPAD
REXT
PS8409AQFN48GTR2-A2_QFN48_6X6
R5310
1/16W_4.7K_5%_0402
R5311
R5320
1/20W_4.7K_1%_0201
EQ_HDMI
DDIB_0P
DDIB_0N
DDIB_1P
DDIB_1N
DDIB_2P
DDIB_2N
DDIB_3P
DDIB_3N
C5313
C5314
C5315
C5316
C5317
C5318
C5319
C5320
0.1U_6.3V_K_X5R_0201
HDMI_DATA2P
HDMI_DATA2N
HDMI_DATA1P
HDMI_DATA1N
HDMI_DATA0P
HDMI_DATA0N
HDMI_CLKP
HDMI_CLKN
HDMI_DATA2P_OUT
HDMI_DATA2N_OUT
HDMI_DATA1P_OUT
HDMI_DATA1N_OUT
HDMI_DATA0P_OUT
HDMI_DATA0N_OUT
HDMI_CLKP_OUT
HDMI_CLKN_OUT
I2C_CLK_PD
I2C_DATA_PD
R5313
R5312
1/20W_0_5%_0201
I2C_CLK_PD_R
I2C_DATA_PD_R
DDIB_CTRLCLK
DDIB_CTRLDATA
R5330
R5331
DDIB_CTRLCLK_R
DDIB_CTRLDATA_R
HDMI_HPD
R5314
1/20W_1K_5%_0201
HDMI_HPD_R
HDMI_HPD_CONN
HDMI_DDC_CLK_R
HDMI_DDC_DATA_R
R5332
R5333
HDMI_DDC_CLK
HDMI_DDC_DATA
R5315
1/20W_100K_5%_0201
R5316
1/16W_4.99K_1%_0402
R5317
1/20W_100K_5%_0201
TABLE I2C Address
I2C_ADDR
LOW
0x10-0x2F
HIGH
0x90-0x9F;0xD0-0xDF
Logic
VCC5B_HDMI
JHDMI1
TMDS Data2+
TMDS Data2 shield
TMDS Data2-
TMDS Data1+
TMDS Data1 shield
TMDS Data1-
TMDS Data0+
TMDS Data0 shield
TMDS Data0-
TMDS Clock+
TMDS Clock shield
TMDS Clock-
CEC
Utility
SCL
SDA
DDC/CEC_GND
+5V Power
HP_DET
GND4
GND3
GND2
GND1
FOX_QJA111Y-RAC01-8H
ME@
R5309
1/20W_2.2K_5%_0201
R5322
1/20W_2.2K_5%_0201
D5304
D5301
D5305
PESD5V0H1BSF_SOD962
EMC@
EMC_NS@
C5322
1000P_25V_K_X7R_0201
C5323
C5321
680P_25V_K_X7R_0201
VCC5B
U5302
TPS2553DRVR_SON6_2X2
R5301
0_0603_LE_SP
C5308
4.7U_6.3V_M_X5R_0402
C5311
R5321
1/20W_61.9K_1%_0201
R5324
R5325
R5318
R5319
1/20W_4.7K_1%_0201
D5302
D5303
AOZ8808DI-05_DFN-10-10-9_2P5X1
FL5304
FL5301
FL5302
FL5303
EXC24CH900U_4P
DDIB_CTRLCLK
DDIB_CTRLDATA
R5326
R5327
R5328
R5329
1/20W_0_5%_0201
Q5301
RUM002N05MGT2L_VMT3
Q5302
Document Number
T14s Gen2
LCFC
Size
Custom
Title
HDMI RETIMER & CONNECTOR
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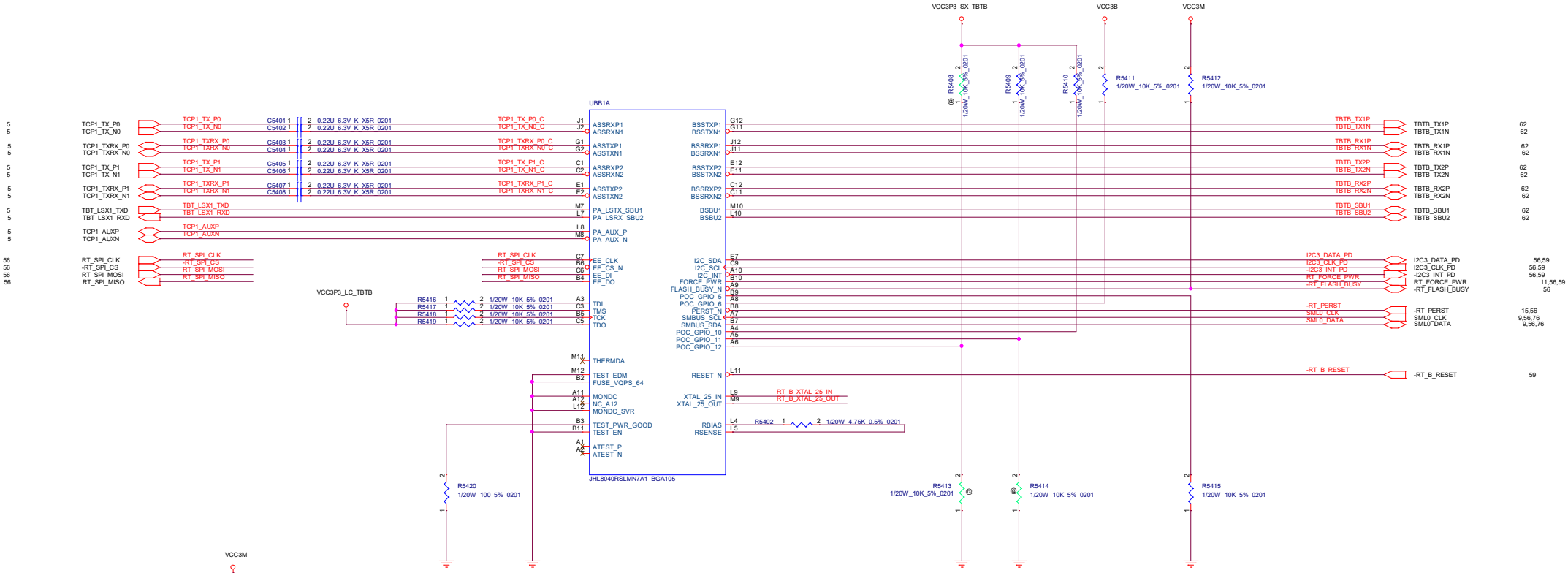

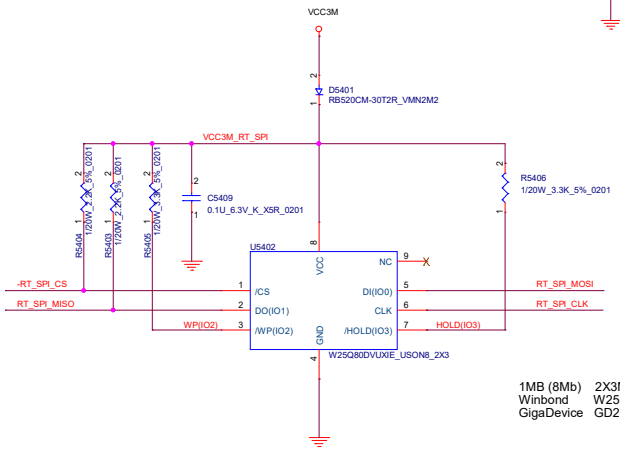

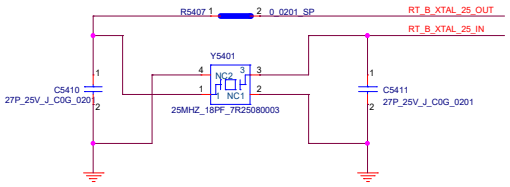

25MHz 18pF 30ppm 2016
TXC 7R25080003
EPSON Q22FA1280056000
KDS 1ZZHAE25000CC0F

1MB (8Mb) 2X3MM USON8
Winbond W25Q80DVUXIE SA00007AF00
GigaDevice GD25Q80CEIG SA00009ZX00

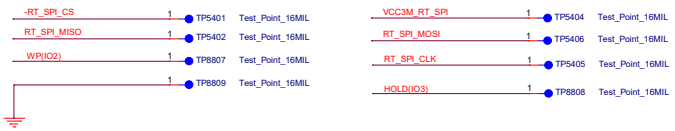

TABLE : Functional Strap

POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

← LOGIC

TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

← LOGIC

1.TypeC port => AUX p/n, HPD
JUSBC1 ->TCP2_AUXP/TCP2_AUXN/TBTC_SBU1/TBTC_SBU2
JDOCK1 ->TCP1_AUXP/TCP1_AUXN/TBTB_SBU1/TBTB_SBU2

2.EC to PD => I2C CLK/DATA/INT
I2C_DATA_PD/I2C_CLK_PD/-PD_I2C_INT

3.PCH(PMC(TBT)) to PD => I2C CLK/DATA/INT
SML1_CLK/SML1_DATA/-PMC_ALERT

4.PD to BB => I2C CLK/DATA
I2C3_CLK_PD/I2C3_DATA_PD/-I2C3_INT_PD

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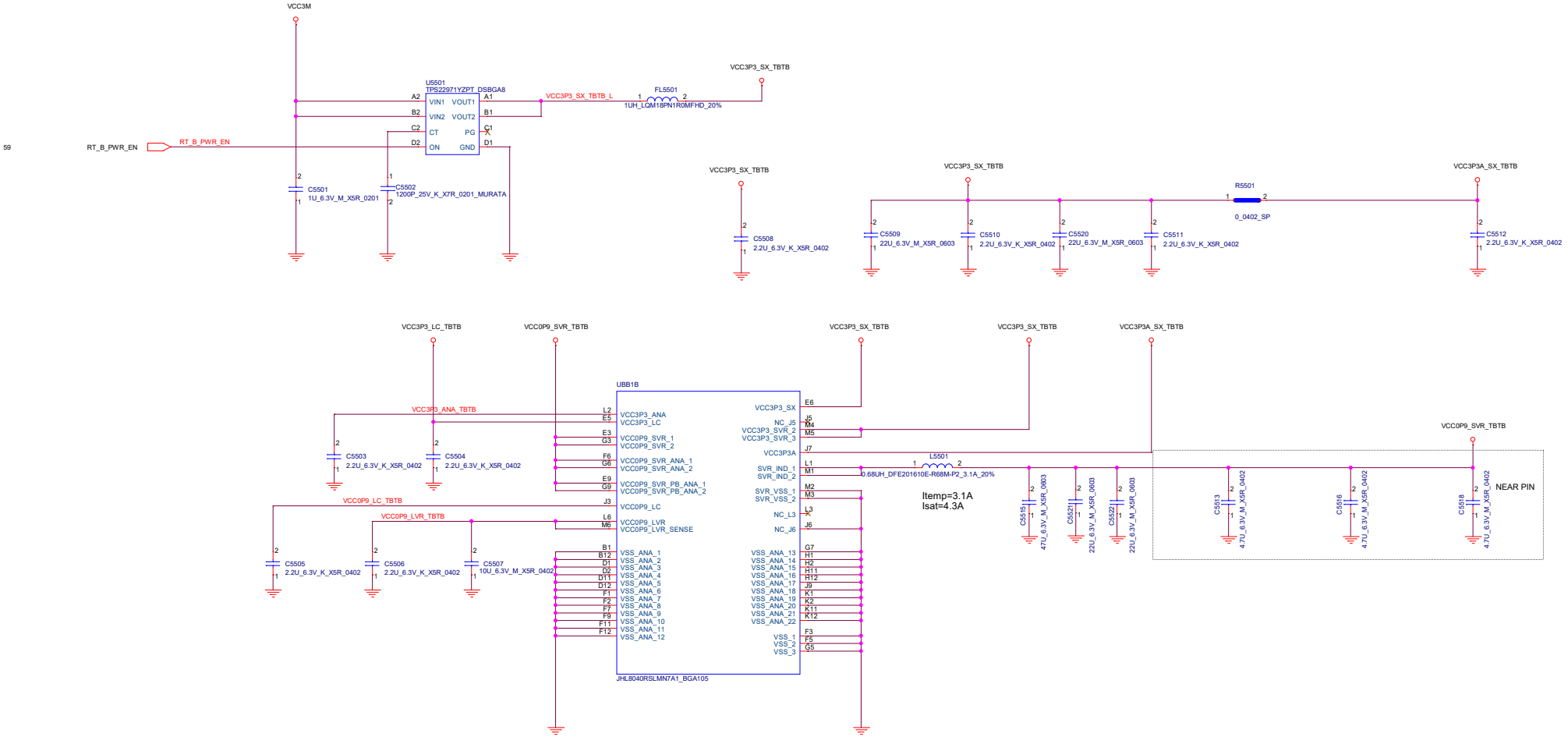

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Project Name : T14s Gen2	Title : THUNDERBOLT RETIMER B (2/2)
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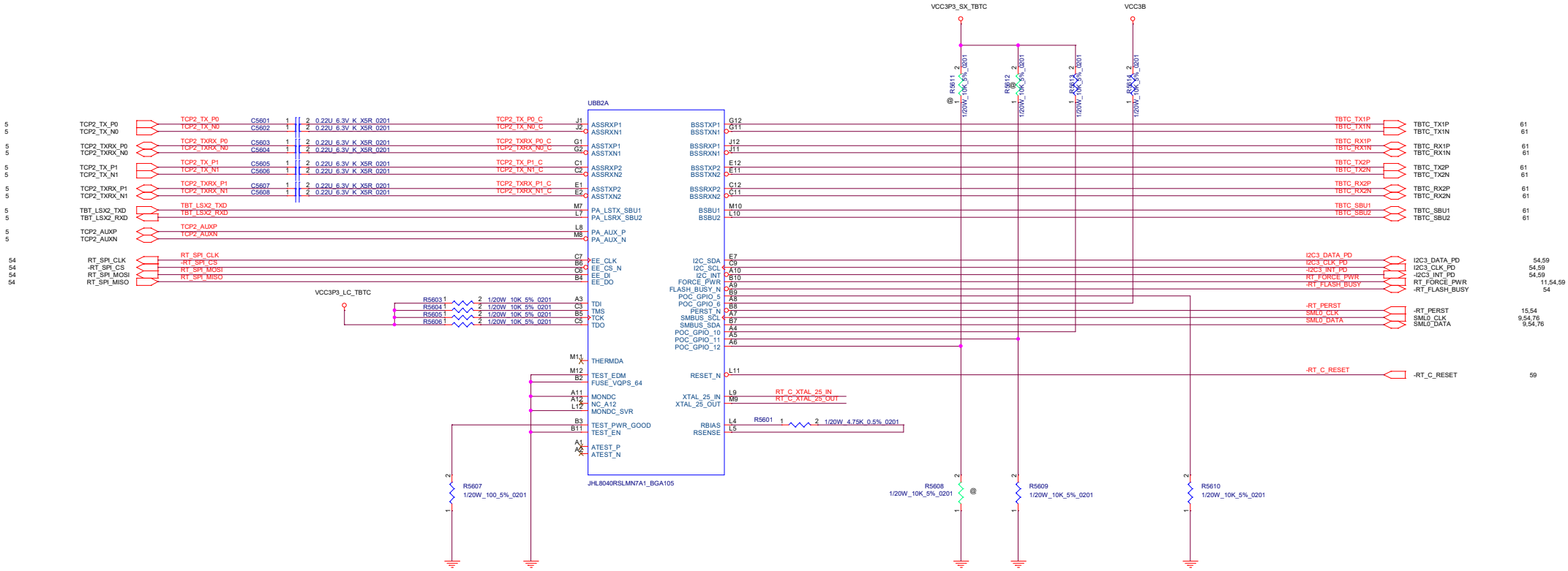

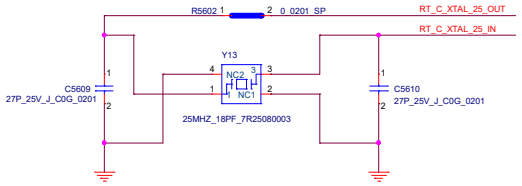

25MHz 18pF 30ppm 2016
TXC 7R25080003
EPSON Q22FA1280056000
KDS 1ZZHAE25000CC0F

TABLE : Functional Strap

POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

← LOGIC

TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

← LOGIC

Table 8. Miscellaneous Signal and Pin Information

Signal	Pin Number	Type	Power domain	Internal PU / PD	Fail-Safe	Description
I2C_SCL	C9	I/O	POC		Yes	I2C bus clock line
I2C_SDA	E7	I/O	POC		Yes	I2C bus data line
I2C_INT	A10	OD	POC		Yes	I2C bus interrupt
FORCE_PWR	B10	I/O	POC		Yes	GPIO Debug
FLASH_BUSY_N	A9	I/O	POC		Yes	GPIO Flash sharing control
POC_GPIO_5	B9	I/O	POC		Yes	GPIO
POC_GPIO_6	A8	I/O	POC		Yes	GPIO (should be connected to system S0 rail)
PERST_N	B8	I/O	POC		Yes	System PERST
SMBUS_SCL	A7	I/O	POC		Yes	SMBus clock
SMBUS_SDA	B7	I/O	POC		Yes	SMBus data
POC_GPIO_10	A4	I/O	POC	PU	Yes	GPIO (Used as Flash share strap)
POC_GPIO_11	A5	I/O	POC	PU	Yes	GPIO (Master-1/Slave-0 strap in Flash share mode)
POC_GPIO_12	A6	I/O	POC	PU	Yes	GPIO
RESET_N	L11	I/O	POC			Main power reset signal
RBIAS	L4	A-in				External resistor for current biasing Resistor value 4.75KOhm +/- 0.5%
RSENSE	L5	A-in				Shares same external resistor as RBIAS
TEST_EDM	M12	In			Yes	Testability signal, connect to GND
THERMDA	M11	A-out	LC			Thermal Diode pin (anode)
NC_L3	L3					

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Project Name : T14s Gen2	Title : THUNDERBOLT RETIMER C (1/2)
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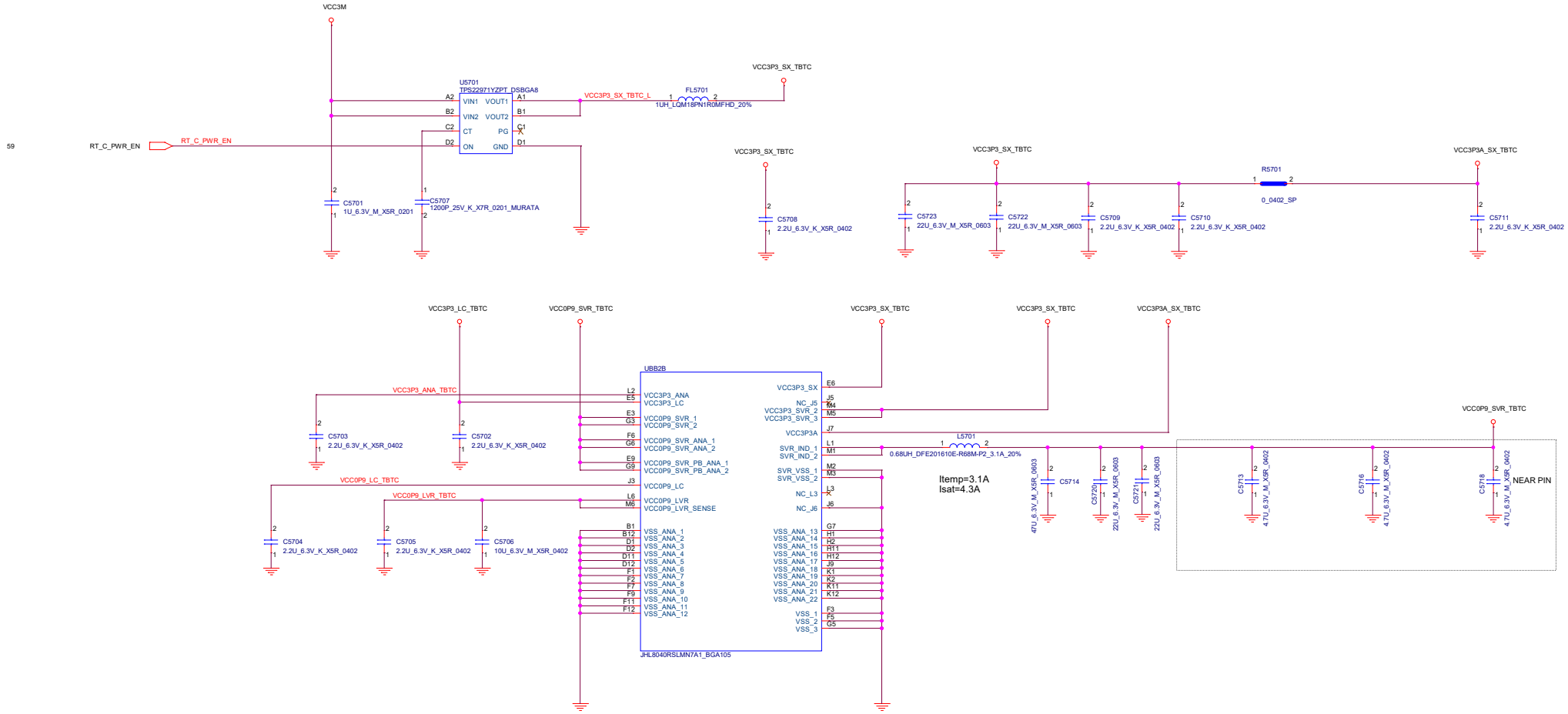

Project Name : T14s Gen2	Title : THUNDERBOLT RETIMER C (2/2)
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Lenovo

Project Name : T14s Gen2	Title : DDR VR
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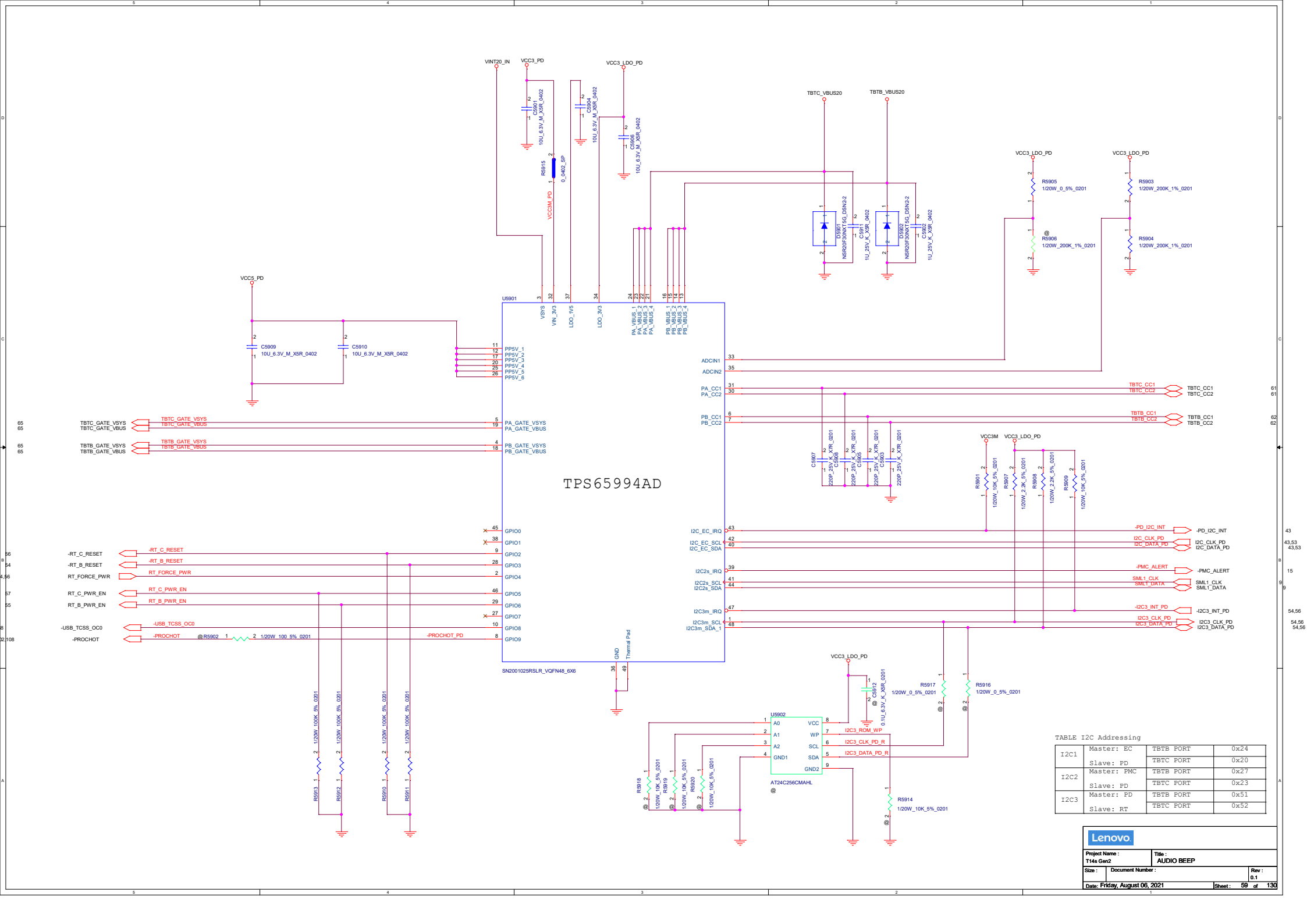

TABLE I2C Addressing

I2C1	Master: EC	TBTB PORT	0x24
	Slave: PD	TBTC PORT	0x20
I2C2	Master: PMC	TBTB PORT	0x27
	Slave: PD	TBTC PORT	0x23
I2C3	Master: PD	TBTB PORT	0x51
	Slave: RT	TBTC PORT	0x52

Project Name : T14s Gen2		Title : AUDIO BEEP	
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Title	<Title>		
Size	Document Number		Rev
Custom	T14s Gen2		0.1
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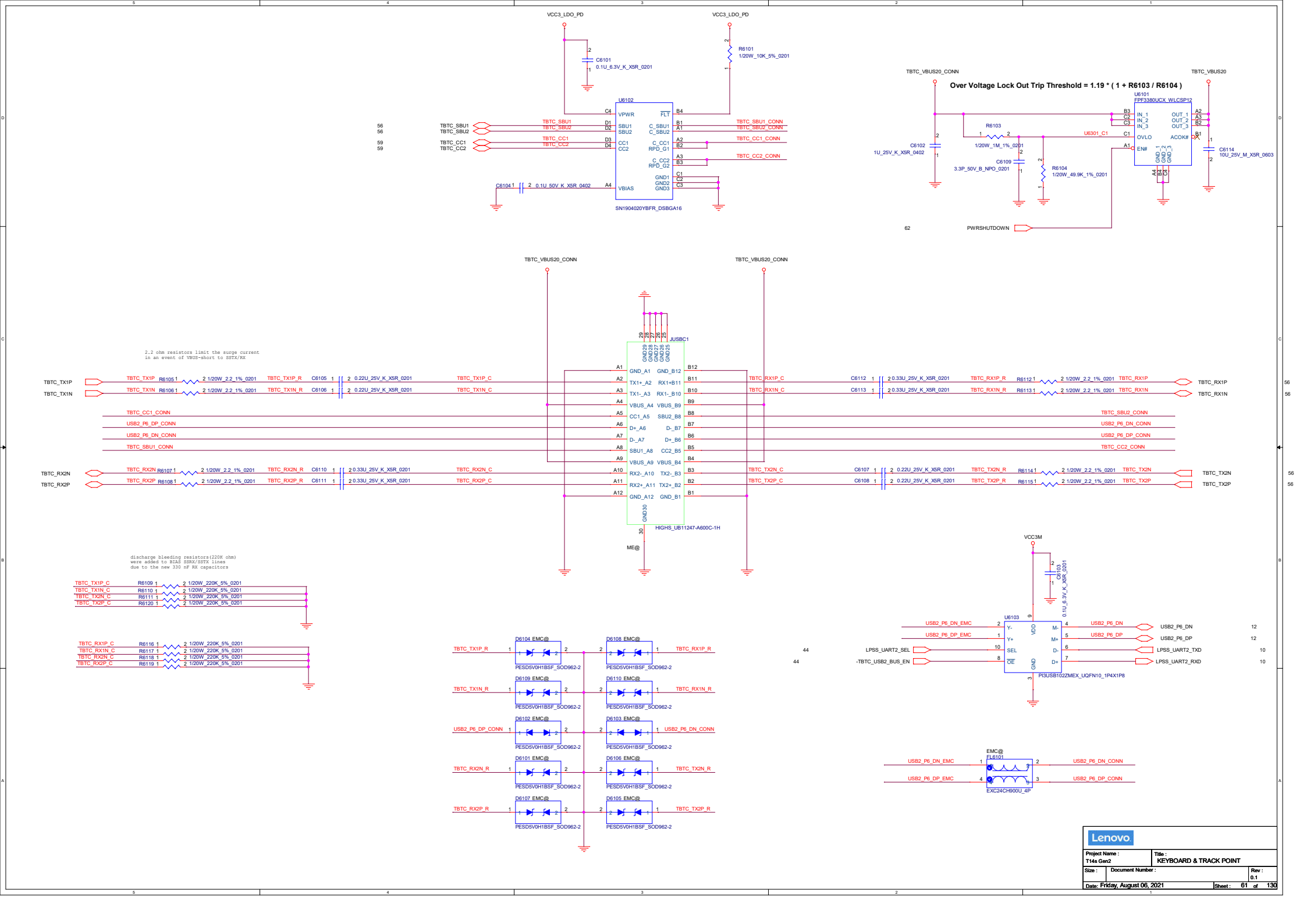
VCC3_LDO_PD
C6101
0.1U_6.3V_K_X5R_0201
R6101
1/20W_10K_5%_0201
U6102
VPWR
FLT
SBU1
SBU2
C_SBU1
C_SBU2
CC1
CC2
C_CC1
RPD_G1
C_CC2
RPD_G2
GND1
GND2
GND3
VBIAS
TBTC_SBU1
TBTC_SBU2
TBTC_SBU1_CONN
TBTC_SBU2_CONN
TBTC_CC1
TBTC_CC2
TBTC_CC1_CONN
TBTC_CC2_CONN
C6104 0.1U_50V_K_X5R_0402
SN1904020YBFR_DSBGA16
TBTC_VBUS20_CONN
TBTC_VBUS20
Over Voltage Lock Out Trip Threshold = 1.19 * (1 + R6103 / R6104)
U6101
FPF3380UCX_WLCSP12
IN_1
IN_2
IN_3
OUT_1
OUT_2
OUT_3
OVLO
ACOK#
EN#
U6301_C1
R6103
1/20W_1M_1%_0201
C6102
1U_25V_K_X5R_0402
C6109
3.3P_50V_B_NPO_0201
R6104
1/20W_49.9K_1%_0201
C6114
10U_25V_M_X5R_0603
62
PWRSHUTDOWN
2.2 ohm resistors limit the surge current
in an event of VBUS-short to SSTX/RX
JUSBC1
GND_A1
GND_B12
TX1+_A2
RX1+B11
TX1-_A3
RX1-_B10
VBUS_A4
VBUS_B9
CC1_A5
SBU2_B8
D+_A6
D-_B7
D-_A7
D+_B6
SBU1_A8
CC2_B5
VBUS_A9
VBUS_B4
RX2-_A10
TX2-_B3
RX2+_A11
TX2+_B2
GND_A12
GND_B1
GND30
HIGHS_UB11247-A600C-1H
ME@
TBTC_TX1P
TBTC_TX1N
TBTC_RX2N
TBTC_RX2P
R6105 2.2_1/20W_2.2_1%_0201
R6106 2.2_1/20W_2.2_1%_0201
R6107 2.2_1/20W_2.2_1%_0201
R6108 2.2_1/20W_2.2_1%_0201
C6105 0.22U_25V_K_X5R_0201
C6106 0.22U_25V_K_X5R_0201
C6110 0.33U_25V_K_X5R_0201
C6111 0.33U_25V_K_X5R_0201
TBTC_TX1P_C
TBTC_TX1N_C
TBTC_RX2N_C
TBTC_RX2P_C
C6112 0.33U_25V_K_X5R_0201
C6113 0.33U_25V_K_X5R_0201
C6107 0.22U_25V_K_X5R_0201
C6108 0.22U_25V_K_X5R_0201
R6112 2.2_1/20W_2.2_1%_0201
R6113 2.2_1/20W_2.2_1%_0201
R6114 2.2_1/20W_2.2_1%_0201
R6115 2.2_1/20W_2.2_1%_0201
TBTC_RX1P
TBTC_RX1N
TBTC_TX2N
TBTC_TX2P
TBTC_CC1_CONN
USB2_P6_DP_CONN
USB2_P6_DN_CONN
TBTC_SBU1_CONN
TBTC_SBU2_CONN
USB2_P6_DN_CONN
USB2_P6_DP_CONN
TBTC_CC2_CONN
discharge bleeding resistors(220K ohm)
were added to BIAS SSRX/SSTX lines
due to the new 330 nF RX capacitors
R6109 1/20W_220K_5%_0201
R6110 1/20W_220K_5%_0201
R6111 1/20W_220K_5%_0201
R6120 1/20W_220K_5%_0201
R6116 1/20W_220K_5%_0201
R6117 1/20W_220K_5%_0201
R6118 1/20W_220K_5%_0201
R6119 1/20W_220K_5%_0201
D6104_EMC@
D6108_EMC@
D6109_EMC@
D6110_EMC@
D6102_EMC@
D6103_EMC@
D6101_EMC@
D6106_EMC@
D6107_EMC@
D6105_EMC@
PESD5V0H1BSF_SOD962-2
VCC3M
C6103 0.1U_6.3V_K_X5R_0201
U6103
USB2_P6_DN_EMC
USB2_P6_DP_EMC
LPSS_UART2_SEL
-TBTC_USB2_BUS_EN
USB2_P6_DN
USB2_P6_DP
LPSS_UART2_TXD
LPSS_UART2_RXD
PI3USB102ZMEX_UQFN10_1P4X1P8
EMC@
FL6101
EXC24CH900U_4P
Lenovo
Project Name : T14s Gen2
Title : KEYBOARD & TRACK POINT
Size :
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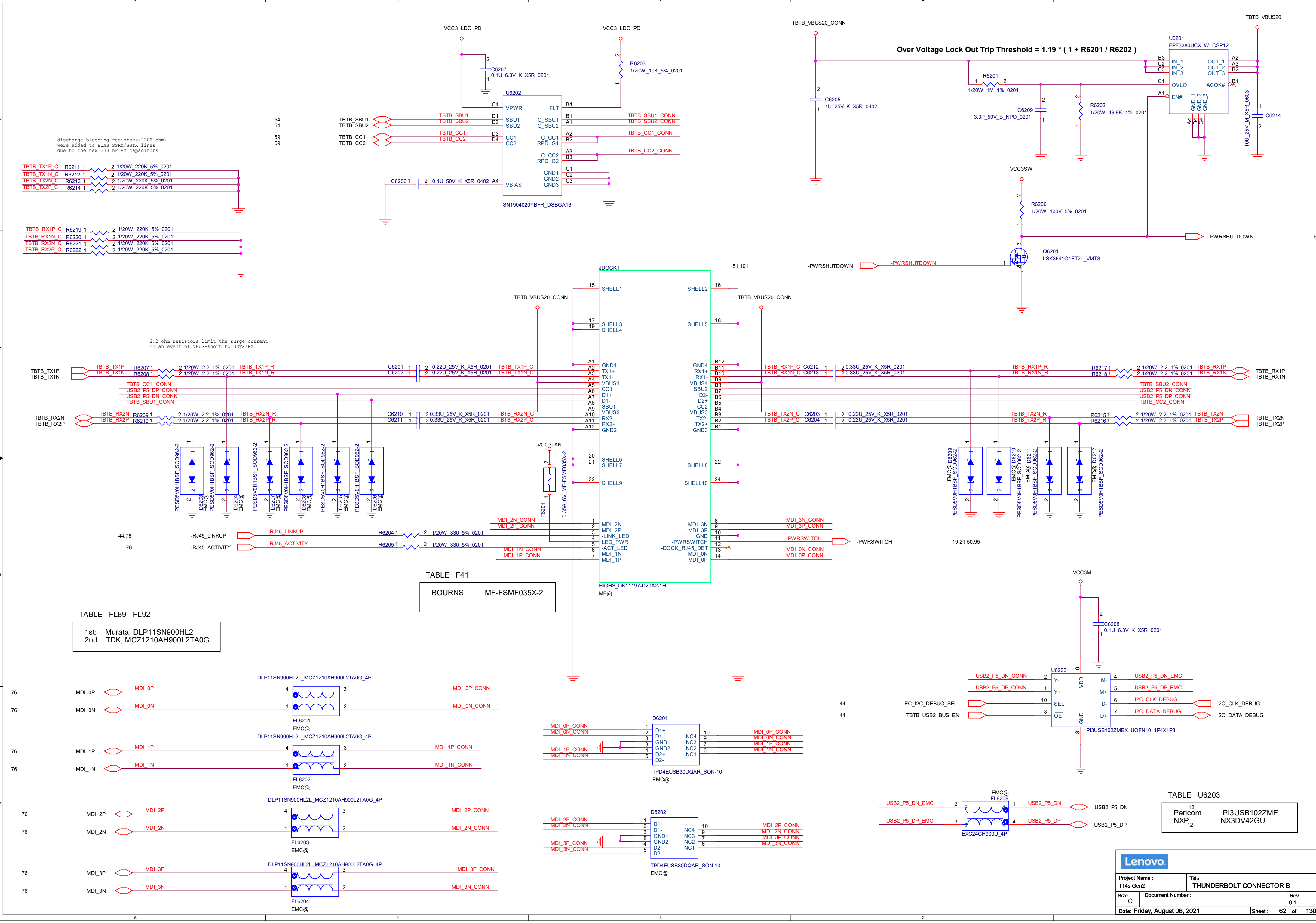
Over Voltage Lock Out Trip Threshold = 1.19 * (1 + R6201 / R6202)
TBTB_VBUS20_CONN
TBTB_VBUS20
U6201
FPF3380UCX_WLCSP12
IN_1
IN_2
IN_3
OVLO
EN#
OUT_1
OUT_2
OUT_3
ACOK#
R6201
1/20W_1M_1%_0201
R6202
1/20W_49.9K_1%_0201
C6205
1U_25V_K_X5R_0402
C6209
3.3P_50V_B_NPO_0201
C6214
10U_25V_M_X5R_0603
VCC3SW
R6206
1/20W_100K_5%_0201
Q6201
LSK3541G1ET2L_VMT3
PWRSHUTDOWN
-PWRSHUTDOWN
VCC3_LDO_PD
C6207
0.1U_6.3V_K_X5R_0201
R6203
1/20W_10K_5%_0201
U6202
SN1904020YBFR_DSBGA16
VPWR
FLT
SBU1
SBU2
C_SBU1
C_SBU2
CC1
CC2
C_CC1
RPD_G1
C_CC2
RPD_G2
GND1
GND2
GND3
VBIAS
C6206
0.1U_50V_K_X5R_0402
TBTB_SBU1
TBTB_SBU2
TBTB_CC1
TBTB_CC2
TBTB_SBU1_CONN
TBTB_SBU2_CONN
TBTB_CC1_CONN
TBTB_CC2_CONN
discharge bleeding resistors(220K ohm)
were added to BIAS SSRX/SSTX lines
due to the new 330 nF RX capacitors
TBTB_TX1P_C R6211 1/20W_220K_5%_0201
TBTB_TX1N_C R6212 1/20W_220K_5%_0201
TBTB_TX2N_C R6213 1/20W_220K_5%_0201
TBTB_TX2P_C R6214 1/20W_220K_5%_0201
TBTB_RX1P_C R6219 1/20W_220K_5%_0201
TBTB_RX1N_C R6220 1/20W_220K_5%_0201
TBTB_RX2N_C R6221 1/20W_220K_5%_0201
TBTB_RX2P_C R6222 1/20W_220K_5%_0201
2.2 ohm resistors limit the surge current
in an event of VBUS-short to SSTX/RX
JDOCK1
HIGHS_DK11197-D20A2-1H
ME@
SHELL1
SHELL2
SHELL3
SHELL4
SHELL5
SHELL6
SHELL7
SHELL8
SHELL9
SHELL10
GND1
TX1+
TX1-
VBUS1
CC1
D1+
D1-
SBU1
VBUS2
RX2-
RX2+
GND2
GND4
RX1+
RX1-
VBUS4
SBU2
D2-
D2+
CC2
VBUS3
TX2-
TX2+
GND3
MDI_2N
MDI_2P
-LINK_LED
LED_PWR
-ACT_LED
MDI_1N
MDI_1P
MDI_3N
MDI_3P
GND
-PWRSWITCH
-DOCK_RJ45_DET
MDI_0N
MDI_0P
TBTB_TX1P
TBTB_TX1N
TBTB_RX2N
TBTB_RX2P
TBTB_RX1P
TBTB_RX1N
TBTB_TX2N
TBTB_TX2P
R6207 1/20W_2.2_1%_0201
R6208 1/20W_2.2_1%_0201
R6209 1/20W_2.2_1%_0201
R6210 1/20W_2.2_1%_0201
R6217 1/20W_2.2_1%_0201
R6218 1/20W_2.2_1%_0201
R6215 1/20W_2.2_1%_0201
R6216 1/20W_2.2_1%_0201
C6201 0.22U_25V_K_X5R_0201
C6202 0.22U_25V_K_X5R_0201
C6210 0.33U_25V_K_X5R_0201
C6211 0.33U_25V_K_X5R_0201
C6212 0.33U_25V_K_X5R_0201
C6213 0.33U_25V_K_X5R_0201
C6203 0.22U_25V_K_X5R_0201
C6204 0.22U_25V_K_X5R_0201
USB2_P5_DP_CONN
USB2_P5_DN_CONN
PESD5V0H1BSF_SOD962-2
EMC@
VCC3LAN
F6201
0.35A_6V_MF-FSMF035X-2
-RJ45_LINKUP
-RJ45_ACTIVITY
R6204 1/20W_330_5%_0201
R6205 1/20W_330_5%_0201
-PWRSWITCH
VCC3M
C6208
0.1U_6.3V_K_X5R_0201
U6203
PI3USB102ZMEX_UQFN10_1P4X1P8
EC_I2C_DEBUG_SEL
-TBTB_USB2_BUS_EN
USB2_P5_DN_EMC
USB2_P5_DP_EMC
I2C_CLK_DEBUG
I2C_DATA_DEBUG
FL6205
EXC24CH900U_4P
USB2_P5_DN
USB2_P5_DP
DLP11SN900HL2L_MCZ1210AH900L2TA0G_4P
FL6201
FL6202
FL6203
FL6204
MDI_0P
MDI_0N
MDI_1P
MDI_1N
MDI_2P
MDI_2N
MDI_3P
MDI_3N
MDI_0P_CONN
MDI_0N_CONN
MDI_1P_CONN
MDI_1N_CONN
MDI_2P_CONN
MDI_2N_CONN
MDI_3P_CONN
MDI_3N_CONN
D6201
D6202
TPD4EUSB30DQAR_SON-10

TABLE F41

BOURNS	MF-FSMF035X-2

TABLE FL89 - FL92

1st:	Murata, DLP11SN900HL2
2nd:	TDK, MCZ1210AH900L2TA0G

TABLE U6203

Pericom	PI3USB102ZME
NXP	NX3DV42GU

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Project Name : T14s Gen2	Title : THUNDERBOLT CONNECTOR B
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Project Name : T14s Gen2	Title : RJ45 Connector
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Project Name : T14s Gen2	Title : TOUCH PAD/NFC/FPR	
Size : C	Document Number :	Rev : 0.1
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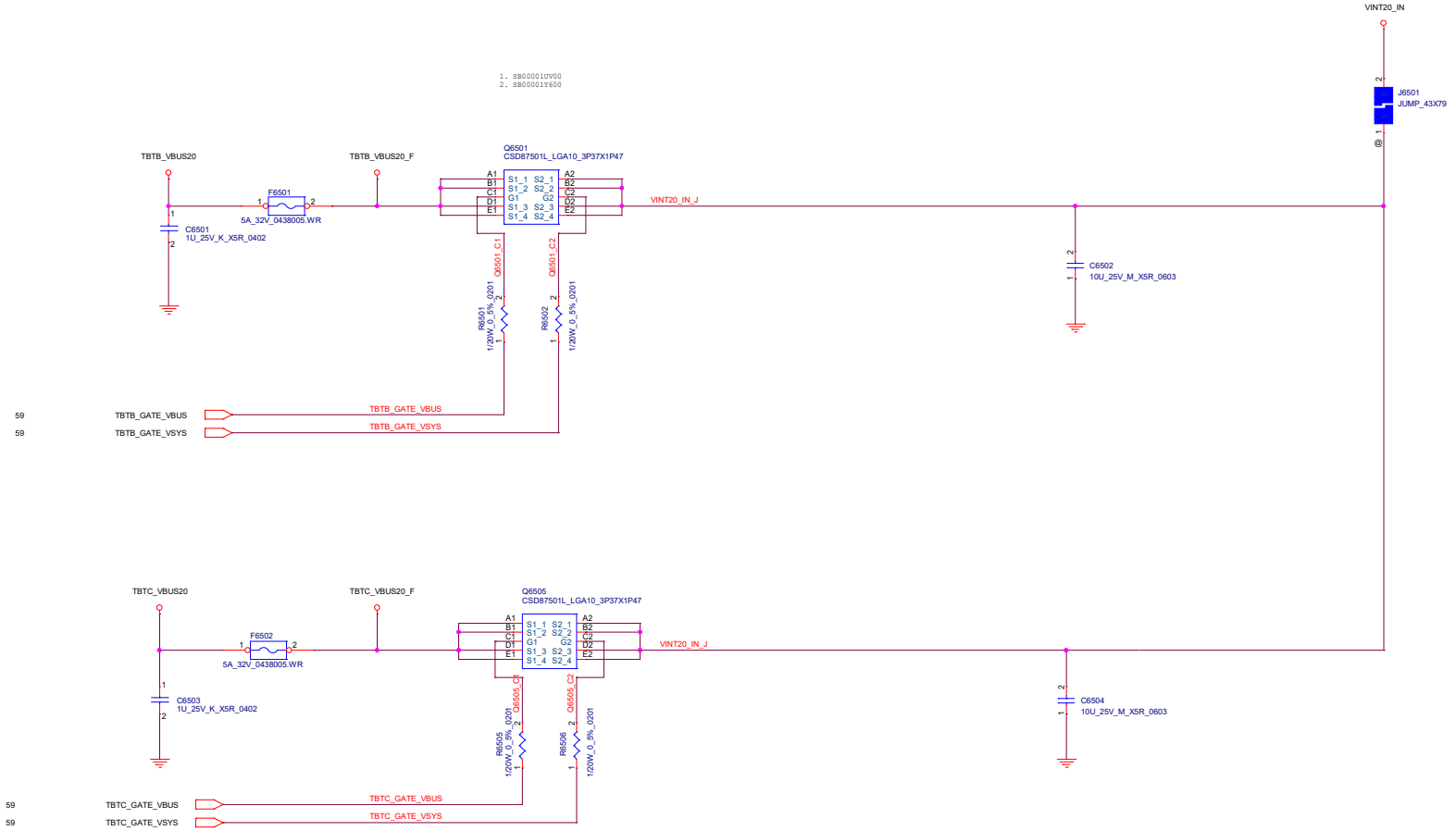

Document Number	T14s Gen2	LCFC
Size: Custom	Title: TYPEC_DCIN	Rev: 0.1
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Project Name : T14s Gen2	Title : FAN CONNECTOR
Size : C	Document Number :
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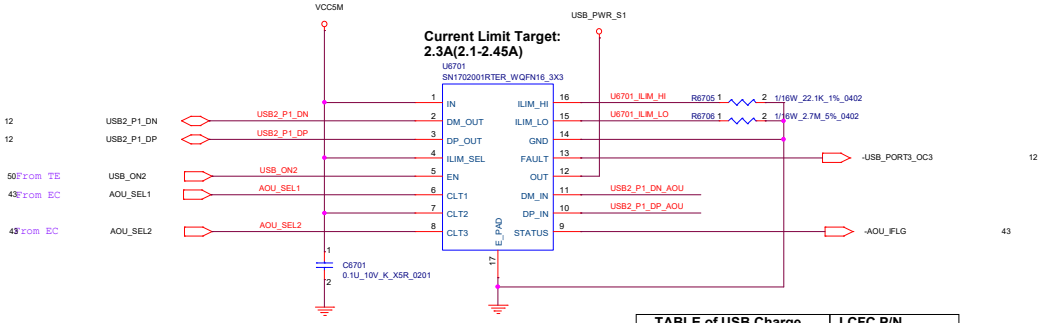
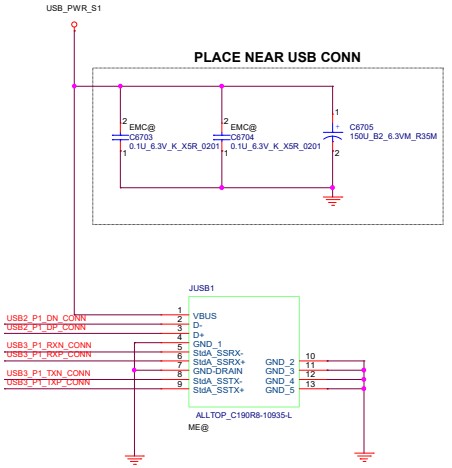
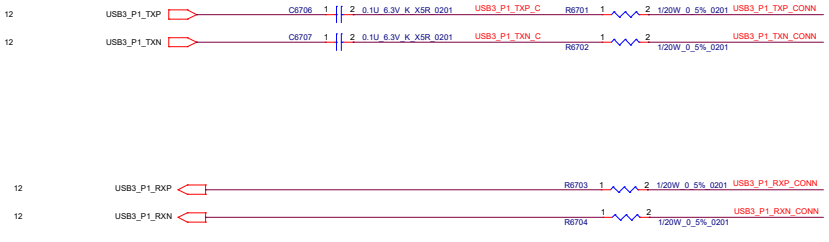
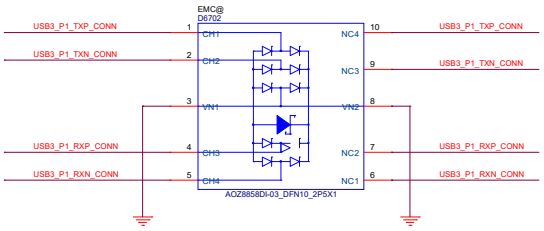
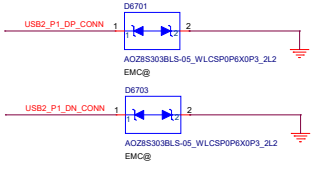


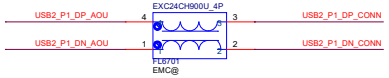
TABLE of USB Charge		LCFC P/N
TI	SN1702001RTER	SA00008HF00











Security Classification	LC Future Center Secret Data		
Issued Date	2019/01/12	Deciphered Date	2019/04/12

Title	USB TYPE-A CONNECTOR		
Size	Document Number		Rev
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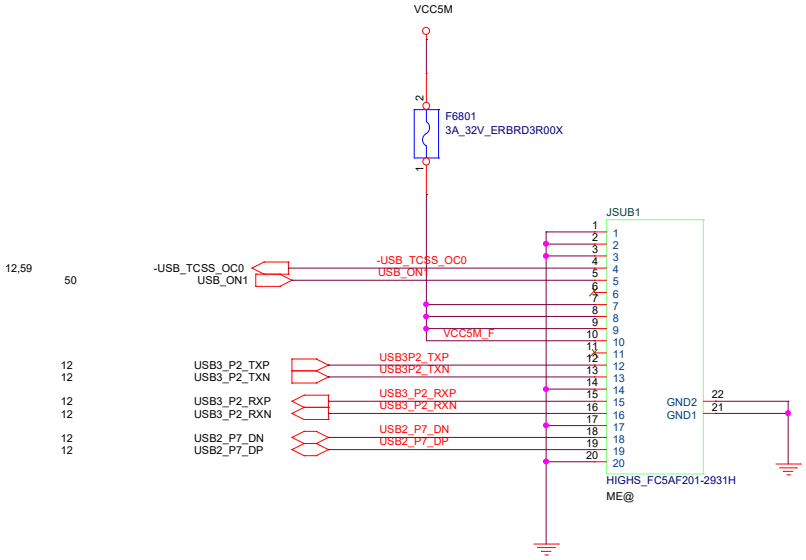

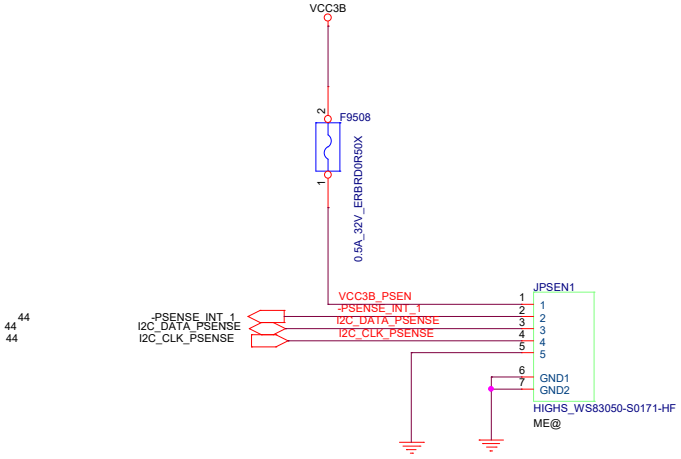

Pin assignment for P-sensor IC

Pin Number	
1	VCC3B 3.3V (VDDHI)
2	PSENSE_INT (GPIO0/RDY)
3	I2C_CLK_PSENSE (SCL)
4	I2C_DATA_PSENSE (SDA)
5	GND (VSS)

Security Classification	LC Future Center Secret Data		
Issued Date	2019/01/12	Deciphered Date	2019/04/12

Title: **USB TYPE-A CONNECTOR**

Size	Document Number	Rev
Custom	T14s Gen2	0.1

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Project Name : T14s Gen2	Title : LAN Switch
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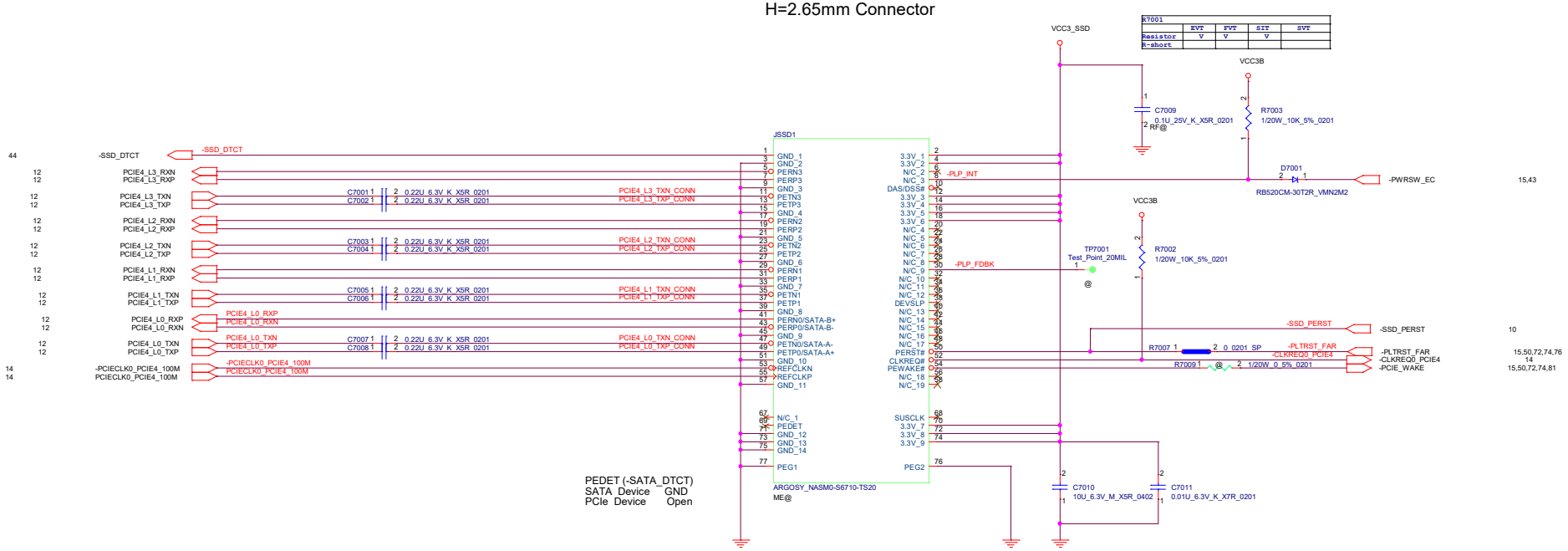
M.2 Socket 3 (Key-M) for 2280 S3 SSD

H=2.65mm Connector



Security Classification	LC Future Center Secret Data		
Issued Date	2018/01/12	Deciphered Date	2018/01/12

Title: M.2 SOCKET 3 MODULE I/F

Size: Custom	Document Number: C	T14s Gen2	Rev: 0.1
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Project Name : T14s Gen2	Title : SMBus Switch	
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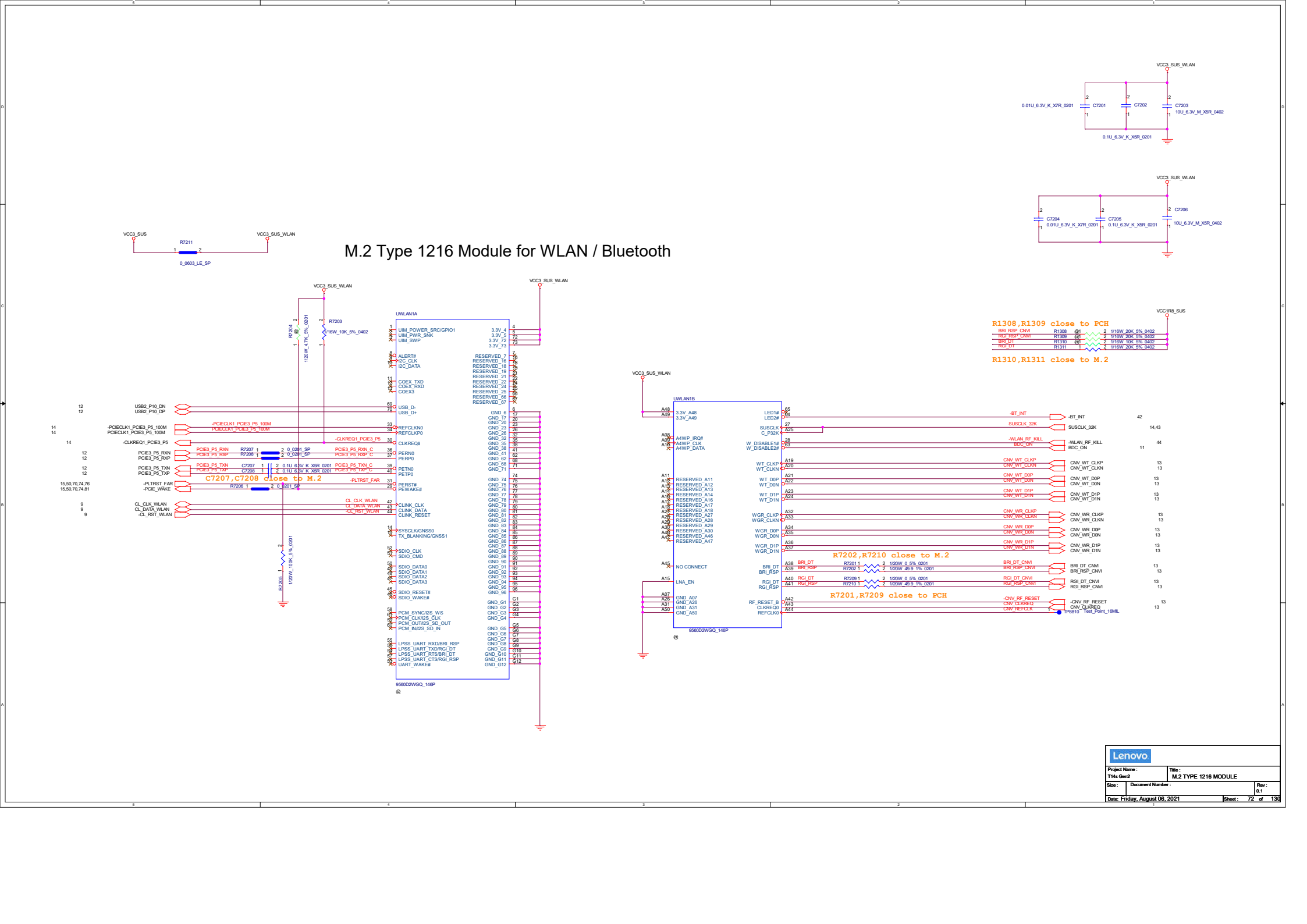
M.2 Type 1216 Module for WLAN / Bluetooth



Project Name : T14s Gen2	Title : M.2 TYPE 1216 MODULE
Size :	Document Number : Rev : 0.1
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Project Name : T14s Gen2	Title : dGPU
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M.2 Socket 2 (Key-B) for 3042 S3 WWAN

H=2.00mm Connector

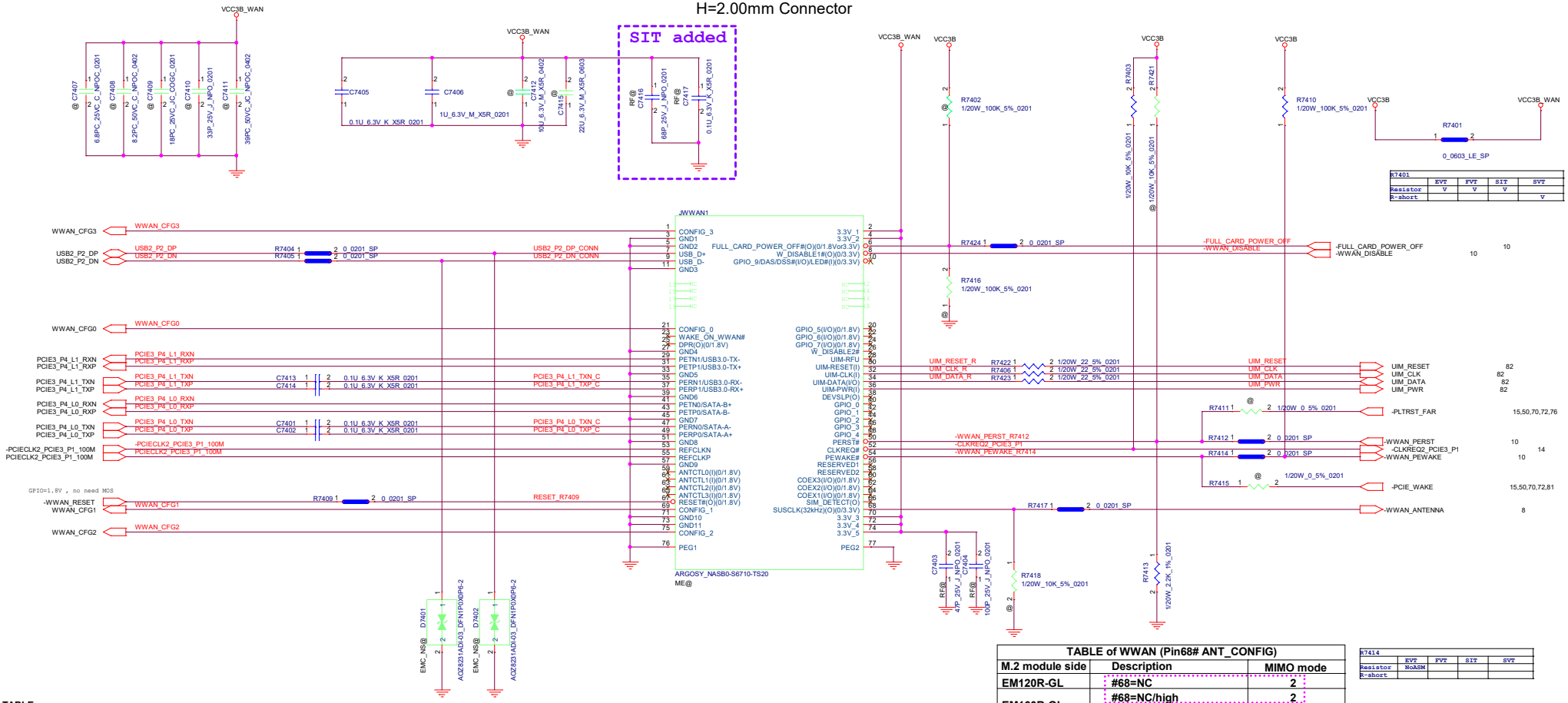

TABLE:

State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration	Module
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)			
0	GND	GND	GND	GND	SSD - SATA	N/A	
1	GND	GND	GND	NC	SSD - PCIe	N/A	
2	GND	GND	NC	GND	WWAN - PCIe	0	
3	GND	GND	NC	NC	WWAN - PCIe	1	
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0	
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1	
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2	EM120R-GL
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3	
8	NC	GND	GND	GND	WWAN - SSIC	0	EM05-CE
9	NC	GND	GND	NC	WWAN - SSIC	1	
10	NC	GND	NC	GND	WWAN - SSIC	2	
11	NC	GND	NC	NC	WWAN - SSIC	3	
12	NC	NC	GND	GND	WWAN - PCIe	2	SDX55
13	NC	NC	GND	NC	WWAN - PCIe	3	
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined	EM160R-GL
15	NC	NC	NC	NC	No Module Present	N/A	

TABLE of WWAN (Pin68# ANT_CONFIG)		
M.2 module side	Description	MIMO mode
EM120R-GL	#68=NC	2
	#68=NC/high	2
EM160R-GL	#68=low level	4

EM160R-GL

Table 26: List of EM160R-GL Configuration Pins

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	Vender defined	N/A

EM120R-GL

Table 28: List of EM120R-GL Configuration Pins

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
GND	GND	NC	NC	Vender defined	N/A

EM05-CE

Table 18: List of Configuration Pins

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
NC	GND	GND	GND	WWAN-SSIC	0

SDX55

1.5.1 Configuration Pins

The M.2 module provides 4 configuration pins. T99W175 is configured as WWAN-PCIe- 2, refer to PCIe M.2_Rev 1.2

Item	Module configuration decodes				Module type	Port configuration
Config	Config_0	Config_1	Config_2	Config_3		
Pin No.	21	69	75	1	WWAN-PCIe	2
State	NC	GND	GND	NC		

Security Classification	LC Future Center Secret Data		
Issued Date	2018/01/12	Deciphered Date	2018/01/12

Title			
M.2 SOCKET 2 MODULE I/F			
Size: Custom	Document Number: C T14s Gen2		Rev: 0.1
Date: Friday, August 06, 2021	Sheet 74 of 130		

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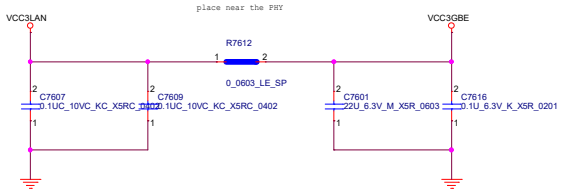
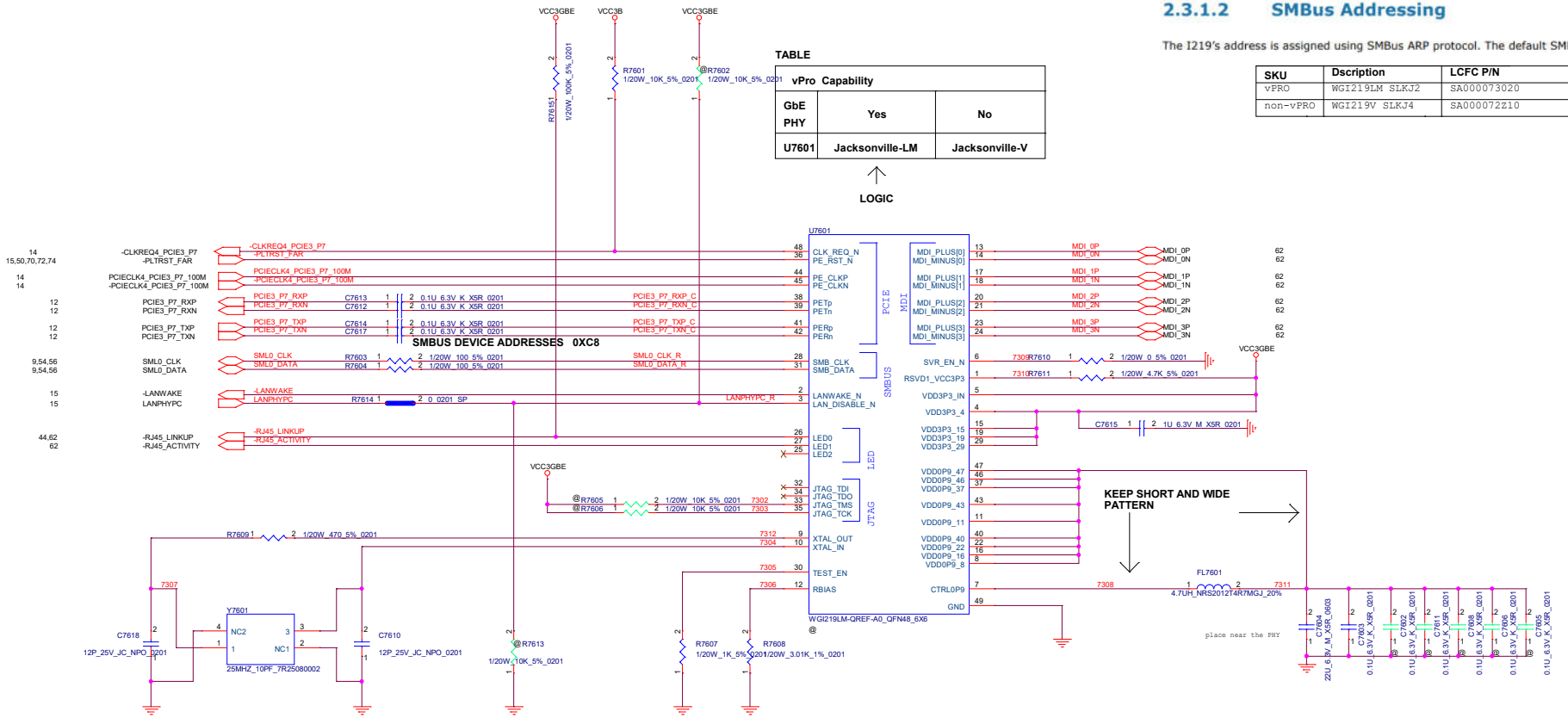
Project Name : T14s Gen2	Title : dGPU	
Size : C	Document Number :	Rev : 0.1
Date: Friday, August 06, 2021	Sheet : 75 of 130	





2.3.1.2 SMBus Addressing

The I219's address is assigned using SMBus ARP protocol. The default SMBus address is 0xC8.

SKU	Dscription	LCFC P/N
vPRO	WGI219LM SLKJ2	SA000073020
non-vPRO	WGI219V SLKJ4	SA000072Z10

Y7601 CRYSTAL - 25MHz 10pF 30ppm 2016		
Vendor	P/N	LCFC P/N
TXC	7R25080002	SJ10000PP00
KDS	1ZZHAE25000CC0B	SJ10000MN00
Epson	Q22FA1280055900	SJ10000PU00

Security Classification	LC Future Center Secret Data		
Issued Date	2018/01/12	Deciphered Date	2018/01/12

Title	GBE JACKSONVILLE		
Size	Document Number		Rev
Custom	C	T14s Gen2	0.1
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Size	Document Number		Rev
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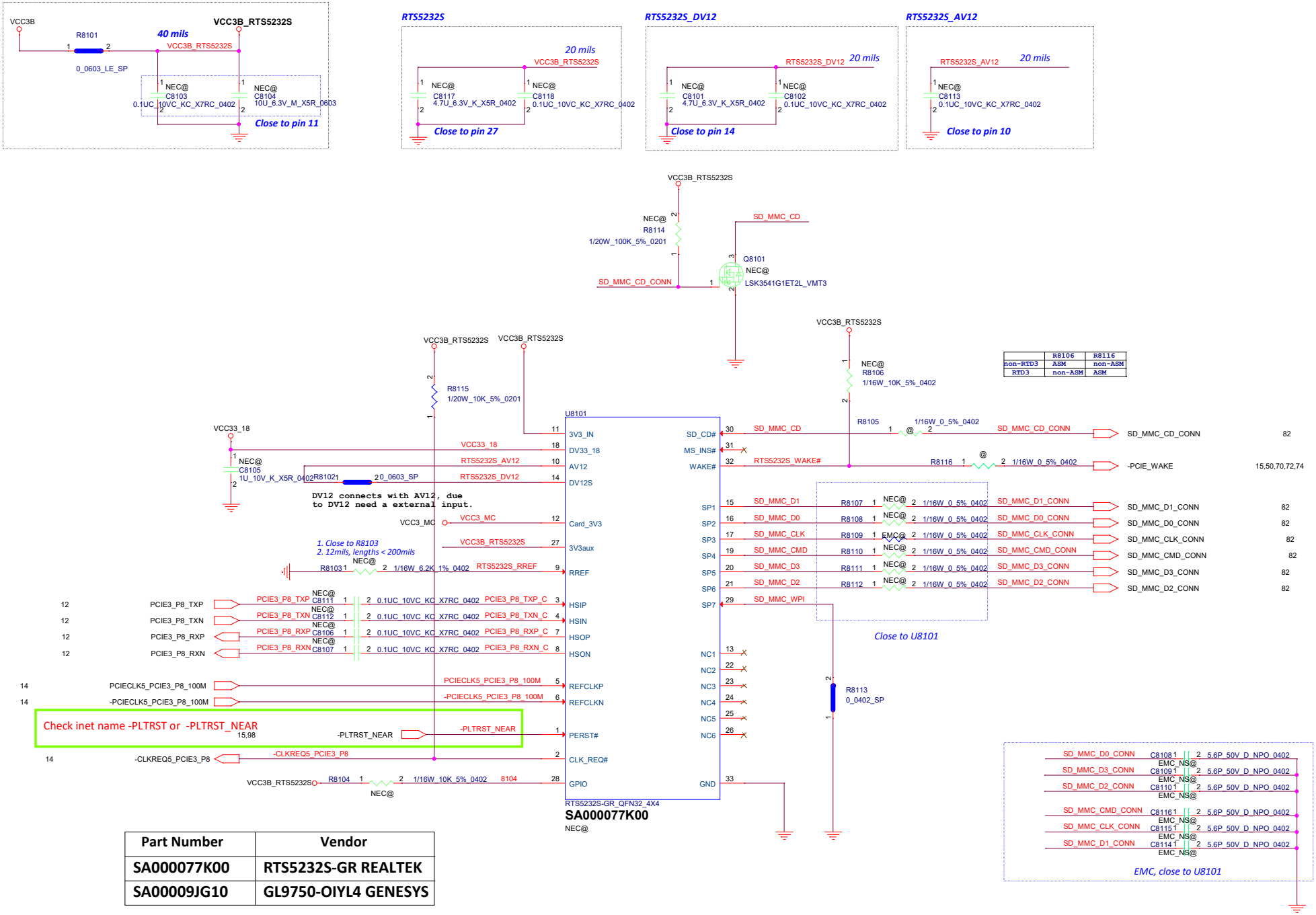


non-RTD3	R8106 ASM	R8116 non-ASM
RTD3	non-ASM	ASM

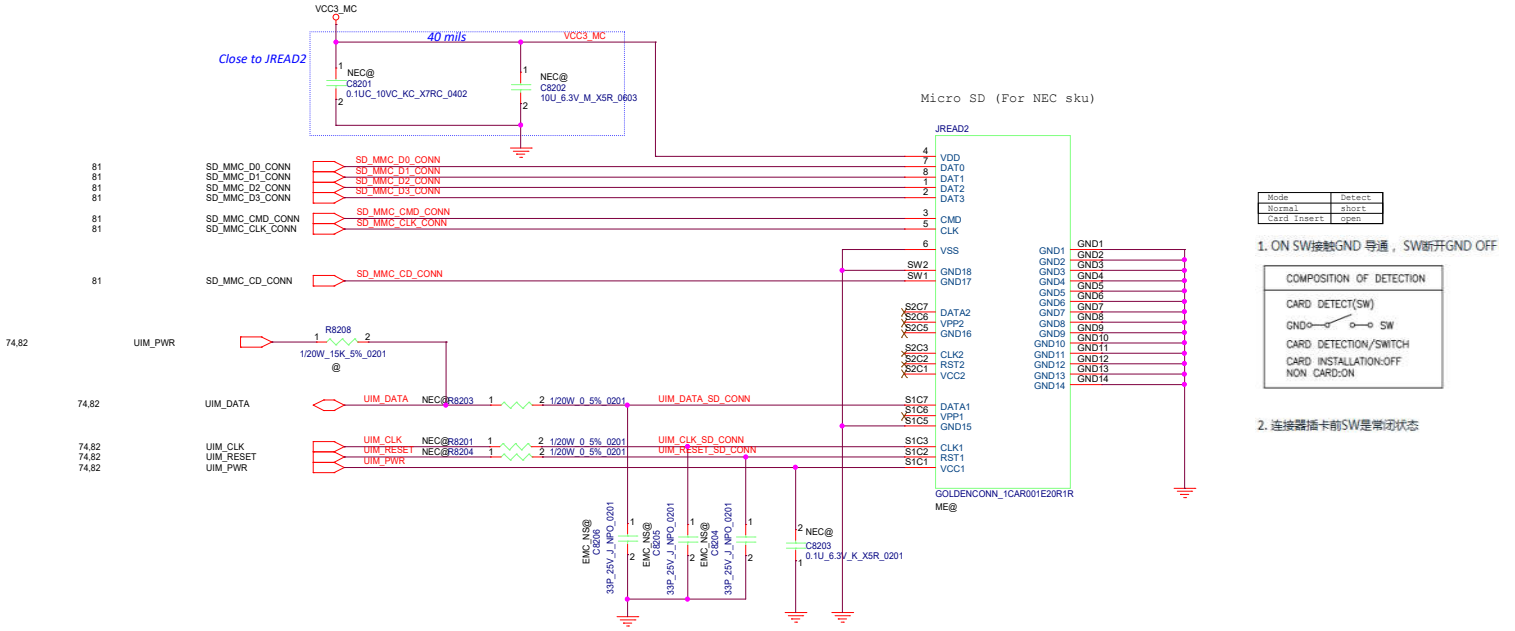
Part Number	Vendor
SA000077K00	RTS5232S-GR REALTEK
SA00009JG10	GL9750-OIYL4 GENESYS

Security Classification	LC Future Center Secret Data		
Issued Date	2019/01/12	Deciphered Date	2019/04/12

Title: MEDIA CARD CONTROLLER

Size	Document Number	Rev
Custom	T14s Gen2	0.1

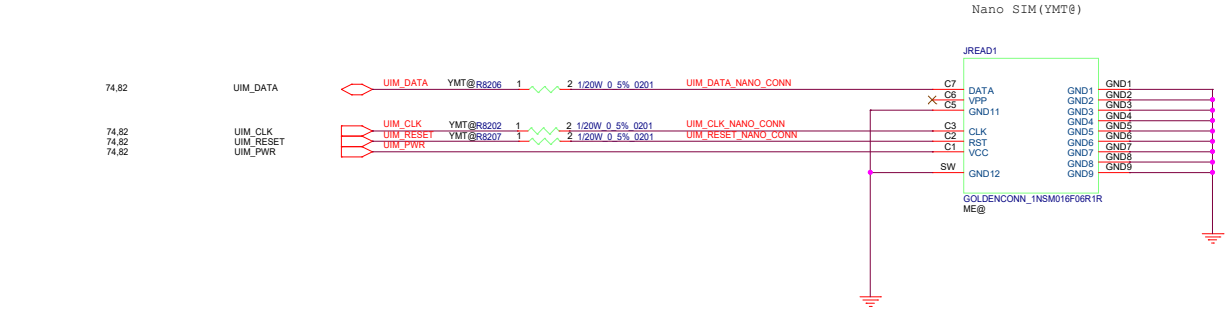
Date: Friday, August 06, 2021 Sheet 81 of 130



Mode	Detect
Normal	short
Card Insert	open

1. ON SW接触GND 导通， SW断开GND OFF

2. 连接器插卡前SW是常闭状态

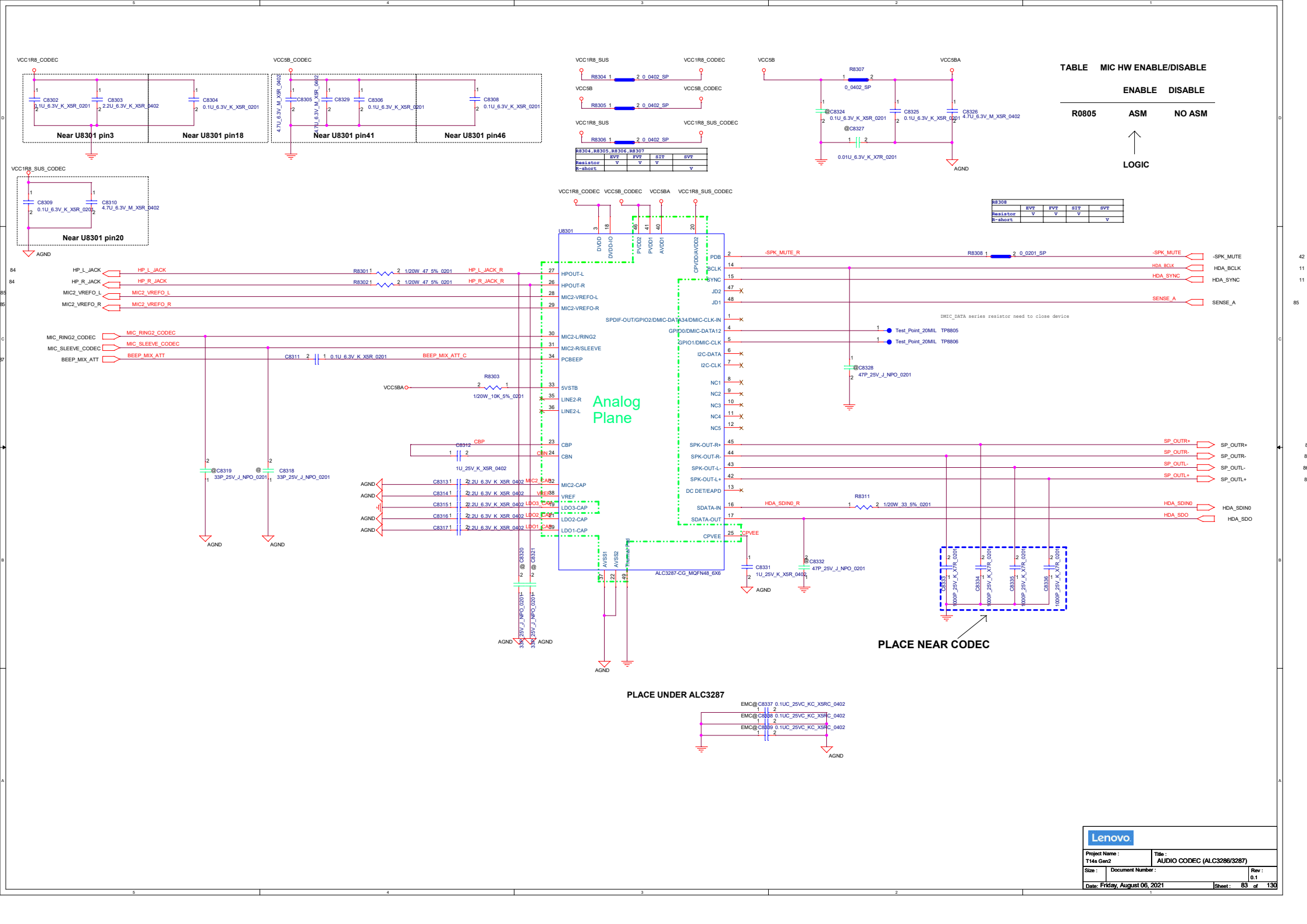


Security Classification	LC Future Center Secret Data		
Issued Date	2019/01/12	Deciphered Date	2019/04/12

Title: MEDIA CARD CONTROLLER

Size	Document Number	Rev
C	T14s Gen2	0.1

Date: Friday, August 06, 2021 Sheet 82 of 130



Project Name :	T14s Gen2
Title :	AUDIO CODEC (ALC3286/3287)
Size :	
Document Number :	
Rev :	0.1
Date:	Friday, August 06, 2021
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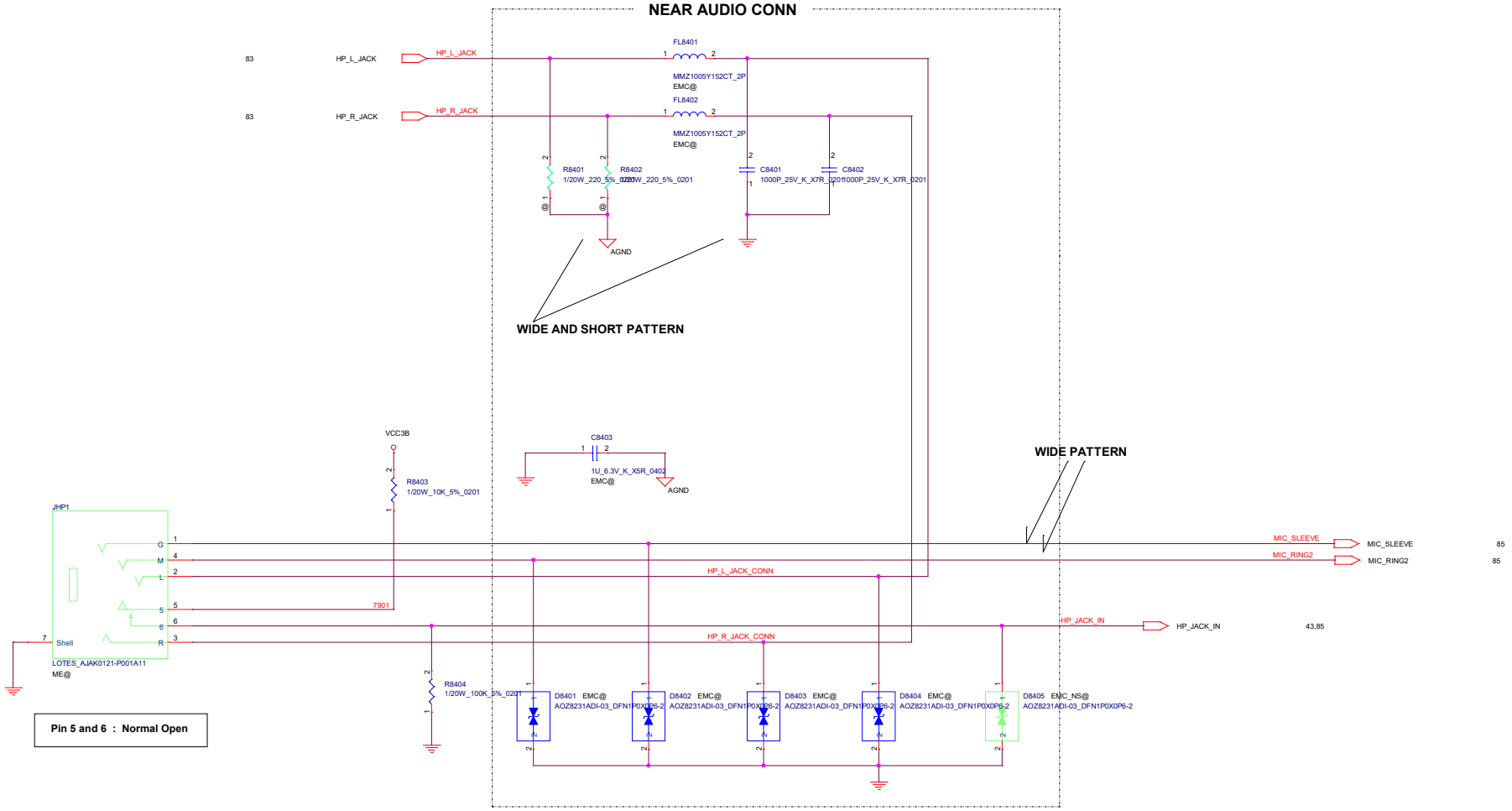
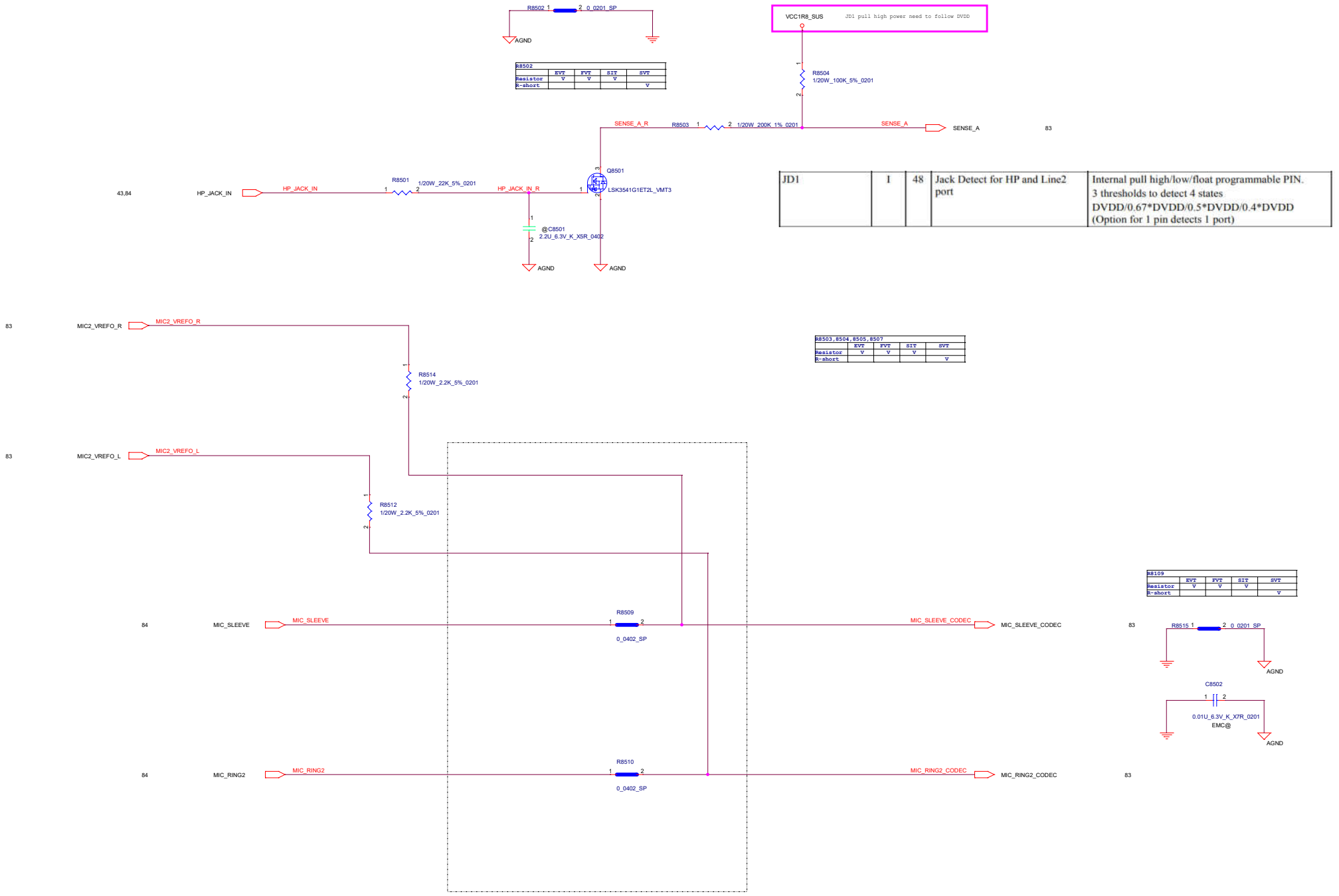
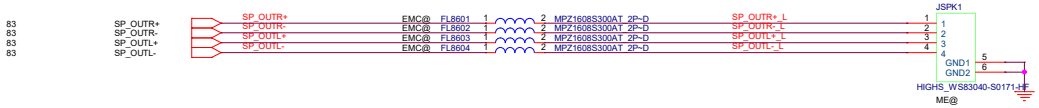


Project Name : T14s Gen2		Title : AUDIO CONNECTOR	
Size : C	Document Number :		Rev : 0.1
Date: Friday, August 06, 2021		Sheet : 84 of 130	



Lenovo

Project Name : T14s Gen2	Title : AUDIO JACK SENSE_MIC_I/F
Size : C	Document Number :
Rev : 0.1	
Date: Friday, August 06, 2021	Sheet : 85 of 130



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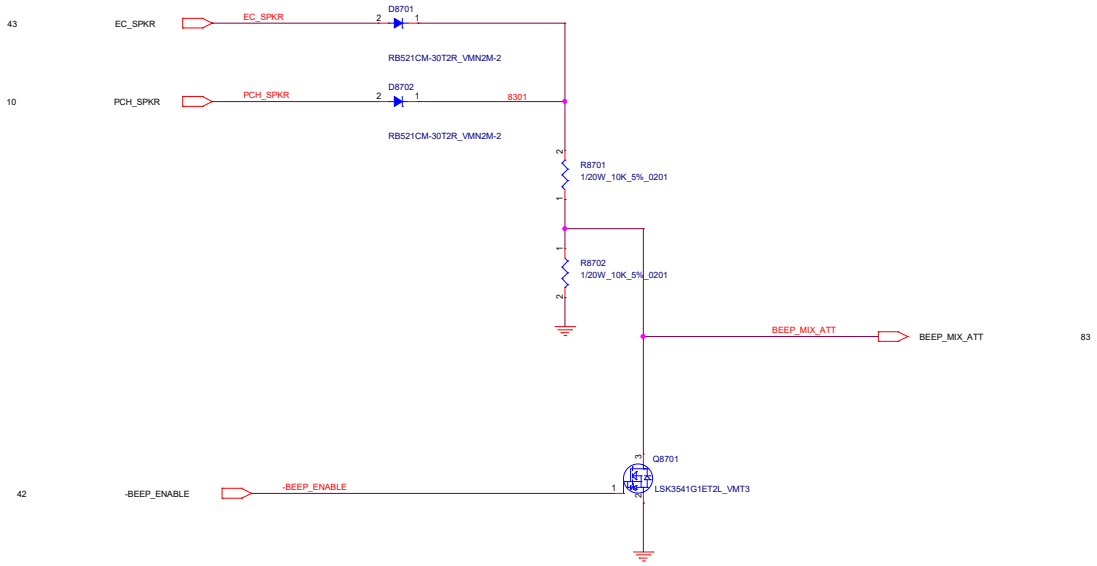
Size : C	Document Number :		Rev : 0.1
Date: Friday, August 06, 2021		Sheet : 86 of 130	



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Size : C	Document Number :		Rev : 0.1
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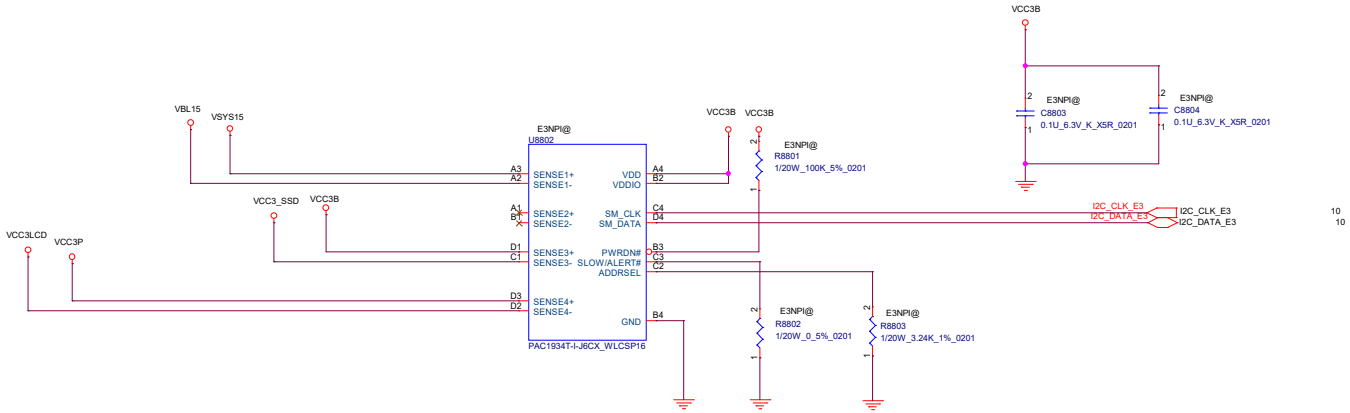
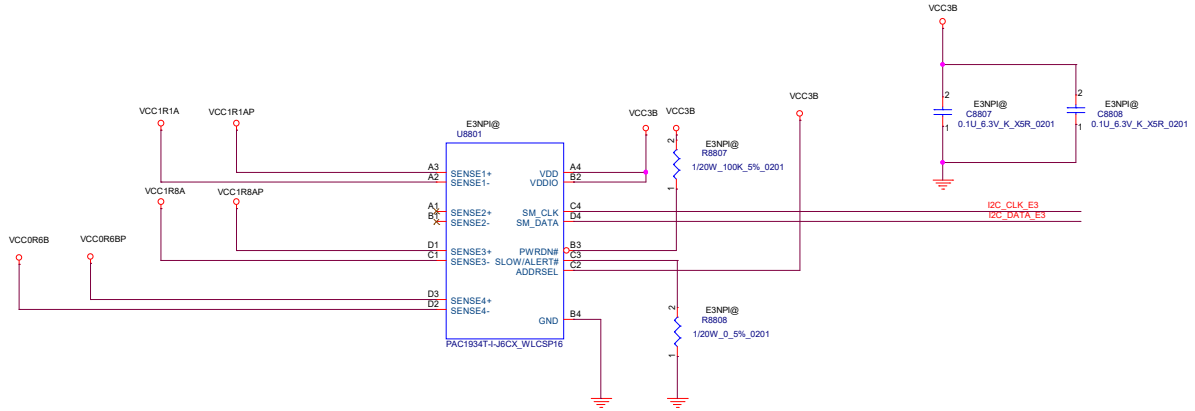


For LCD & Storage I2C Address:0010_101(ADDRSEL=3,240)



For DDR I2C Address:0011_111(ADDRSEL=Tied to VDD)

I2C Address:0011_010(ADDRSEL=34,000)

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Title		
SCR&FPR&NEC LED		
Size: C	Document Number: T14s Gen2	Rev: 0.1
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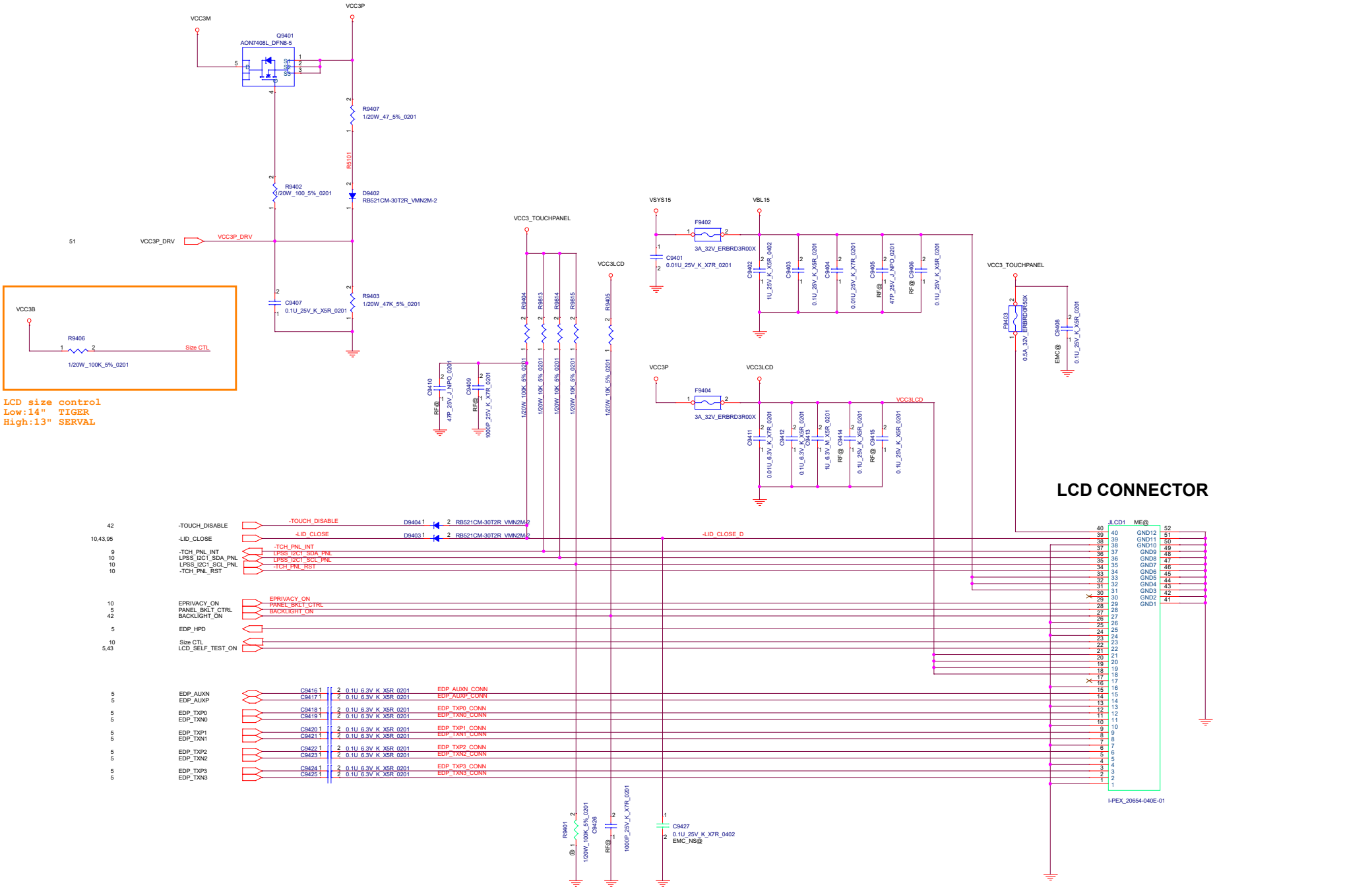

Security Classification	LC Future Center Secret Data		
Issued Date	2018/01/12	Deciphered Date	2018/01/12

Title	LCD INTERFACE		
Size	Document Number		Rev
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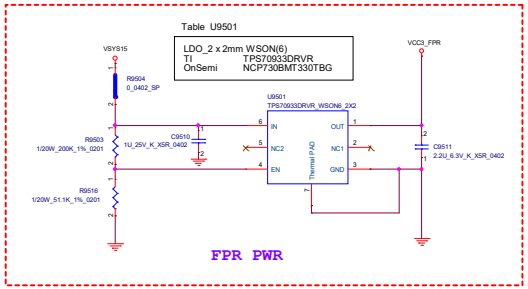
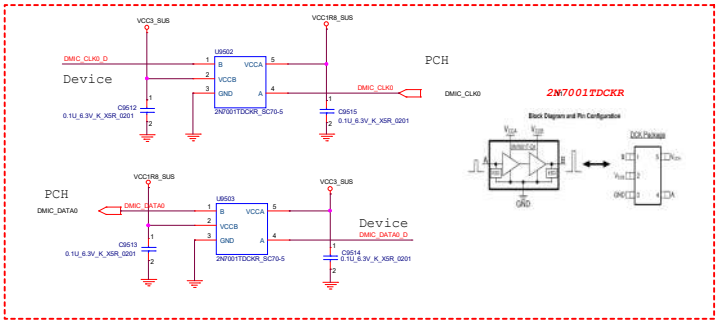
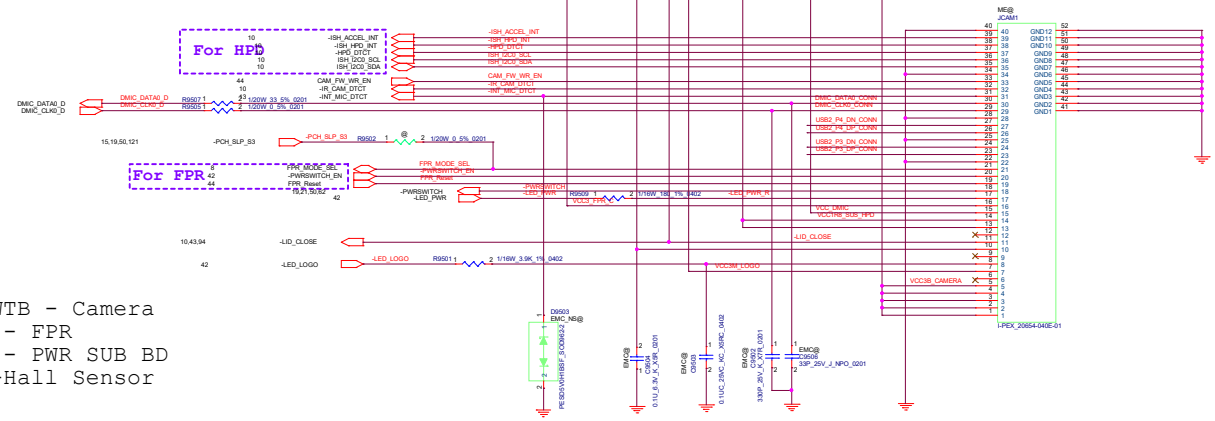
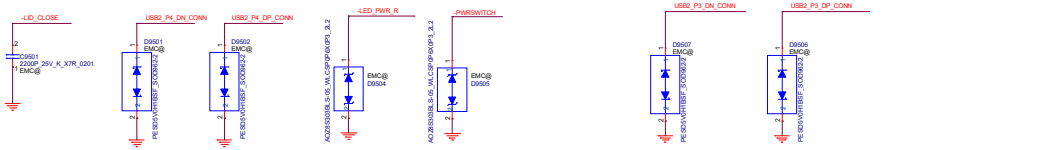
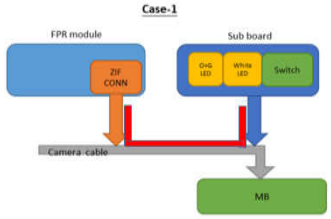






WTB - Camera
- FPR
- PWR SUB BD
-Hall Sensor





For HPD

for HPD SIG	
PIN	SIGNAL_NAME
	SIG 5PIN
1	GND
2	ISH_I2C0_SCL
3	ISH_I2C0_SDA
4	VCC1R8_SUS_HPD
5	-ISH_HPD_INT

For Hybrid & RGB

Pin assignment

No.		No.	
17	IR VCC	18	IR VCC
1	MIC DET	16	MIC VCC
2	WP	15	MIC CLK
3	NC	14	MIC DATA
4	NC	13	NC
5	CAM 3V3	12	CAM 3V3
6	Reverse	11	D
7	MIC GND	10	D-
8	DGND	9	DGND
19	IR GND	20	IR GND

For FPR

GPIO	State	
GPIO_AL0 -PWRSWITCH_EN	High	Disable Power Button
	Low	Enable Power Button
DELINK FPR_MODE_SEL	High	S0
	Low	S0/3/53/54/55
FPS_RESET_N Keep high	High	Normal
	Low	Reset

GPIO	Input/Output	S0	S0/3	S3	S4	S5
GPIO_AL0	Output	1. Enrollment/Authentication: High 2. Other: Low	Low	Low	Low	Low
DELINK	Input	High	Low	Low	Low	Low

Security Classification	LC Future Center Secret Data		
Issued Date	2018/01/12	Deciphered Date	2018/01/12

Title	LID/CAMERA/MIC/TOUCH INTERFACE		
Size: Custom	Document Number: T14s Gen2		Rev: 0.1
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Title	<Title>	
Size A	Document Number T14s Gen2	Rev 0.1
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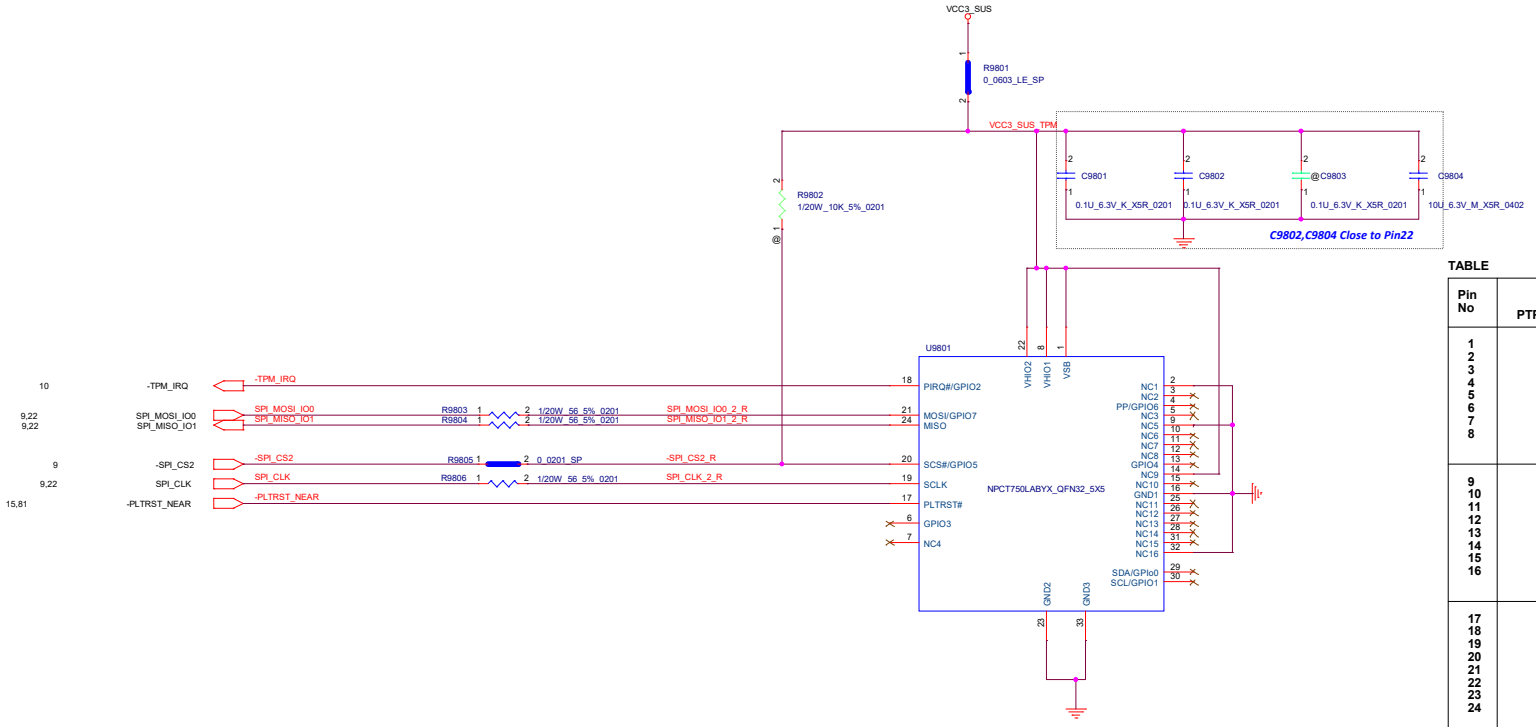
Date: Friday, August 06, 2021	Sheet 97 of 130	



TABLE

Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LABYX	ST Micro ST33HTPH2X32AHD4
1	VDD	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	GPIO	GPIO/PP	PP
5	NC	NC	NC
6	GPIO	GPIO3	NC
7	GPIO	NC	GPIO
8	VDD	VHIO	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC

	TABLE of TPM (U9801)		
	Vendor	P/N	LCFC P/N
Pre FVT	ST Micro	ST33HTPH2X32AHD4	SA0000AB710
	Nuvoton	NPCT750LABYX QFN	SA00008KS20
FVT and after	ST Micro	ST33HTPH2X32AHD8	SA0000AB720
	Nuvoton	NPCT750LADYX QFN	SA00008KS30

Title: *DISCRETE TPM 2.0*

Size: Custom | Document Number: C | *T14s Gen2* | Rev: 0.1

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@H6
HOLEA
PAD_C6P0D2P3

@H19
HOLEA
PAD_C6P0D2P3

@H9
HOLEA
PAD_D2P3X3P8

@H11
HOLEA
PAD_D2P3X3P8

@H1
HOLEA
PAD_C3P0D3P0N

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

H14 HOLEA PAD_C6P8 @

H15 HOLEA PAD_C6P8 @

H16 HOLEA PAD_C6P8 @

H17 HOLEA PAD_C6P8 @

@HICT1
HOLEA
PAD_C2P5D2P5N

@HICT2
HOLEA
PAD_C2P5D2P5N

@HICT3
HOLEA
PAD_C2P5D2P5N

@H3
HOLEA
PAD_C5P0D2P3

@H10
HOLEA
PAD_C7P0D3P3

@H8
HOLEA
PAD_C7P0D3P3

@H12
HOLEA
PAD_C8P0D5P4

@H5
HOLEA
PAD_C8P0D2P8

@H4
HOLEA
PAD_C2P0D2P0N

@H2
HOLEA
PAD_C5P0D3P0

@H13
HOLEA
PAD_C5P0D3P8

@H7
HOLEA
PAD_C5P0D3P4

@H18
HOLEA
PAD_O0P8X2P5D0P8X2P5N

@H20
HOLEA
PAD_C1P2D1P2N

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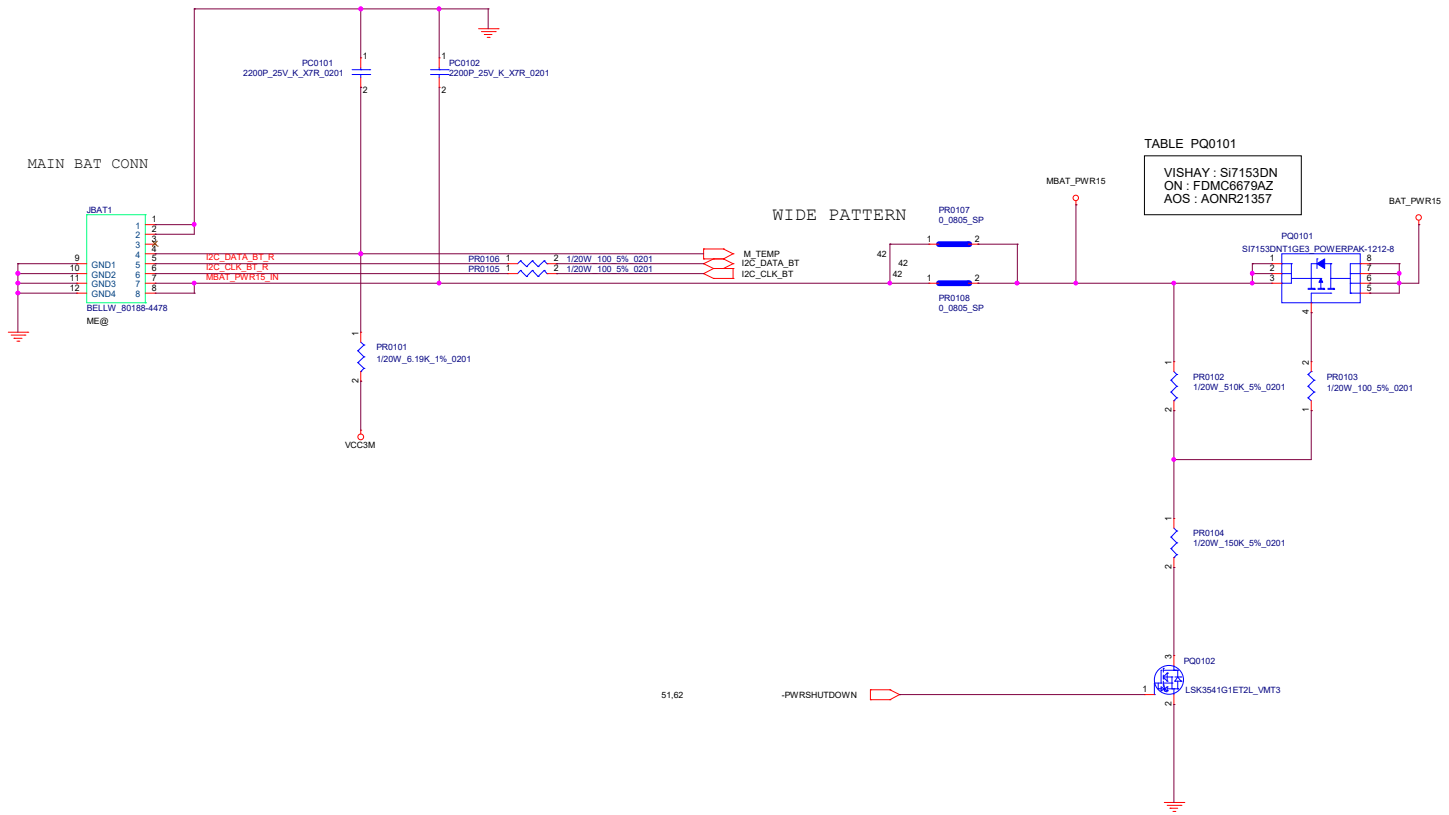
Date: Friday, August 06, 2021	Sheet 100 of 130		



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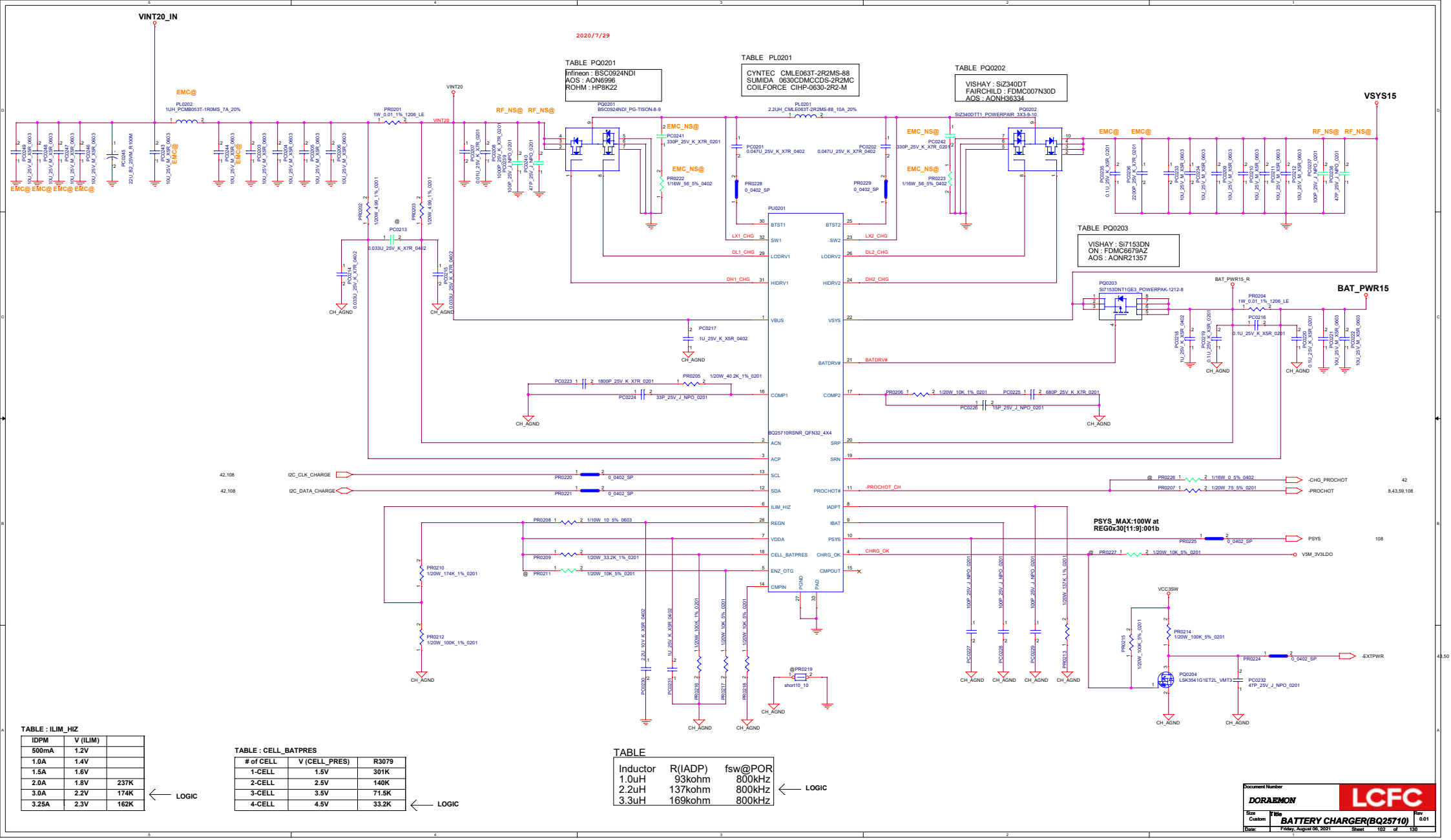
Size: Custom	Title: Battery Conn	Rev: 0.01
Date: Friday, August 06, 2021	Sheet 101 of 130	


VINT20_IN
2020/7/29
TABLE PQ0201
Infineon : BSC0924NDI
AOS : AON6996
ROHM : HP8K22
TABLE PL0201
CYNTEC CMLE063T-2R2MS-88
SUMIDA 0630CDMCCDS-2R2MC
COILFORCE CIHP-0630-2R2-M
TABLE PQ0202
VISHAY : SiZ340DT
FAIRCHILD : FDMC007N30D
AOS : AONH36334
TABLE PQ0203
VISHAY : Si7153DN
ON : FDMC6679AZ
AOS : AONR21357
VSYS15
BAT_PWR15
BQ25710RSNR_QFN32_4X4
PSYS_MAX:100W at
REG0x30[11:9]:001b
TABLE : ILIM_HIZ
IDPM V (ILIM)
500mA 1.2V
1.0A 1.4V
1.5A 1.6V
2.0A 1.8V 237K
3.0A 2.2V 174K
3.25A 2.3V 162K
LOGIC
TABLE : CELL_BATPRES
# of CELL V (CELL_PRES) R3079
1-CELL 1.5V 301K
2-CELL 2.5V 140K
3-CELL 3.5V 71.5K
4-CELL 4.5V 33.2K
LOGIC
TABLE
Inductor R(IADP) fsw@POR
1.0uH 93kohm 800kHz
2.2uH 137kohm 800kHz
3.3uH 169kohm 800kHz
LOGIC
DORAEMON
LCFC
BATTERY CHARGER(BQ25710)
Friday, August 06, 2021
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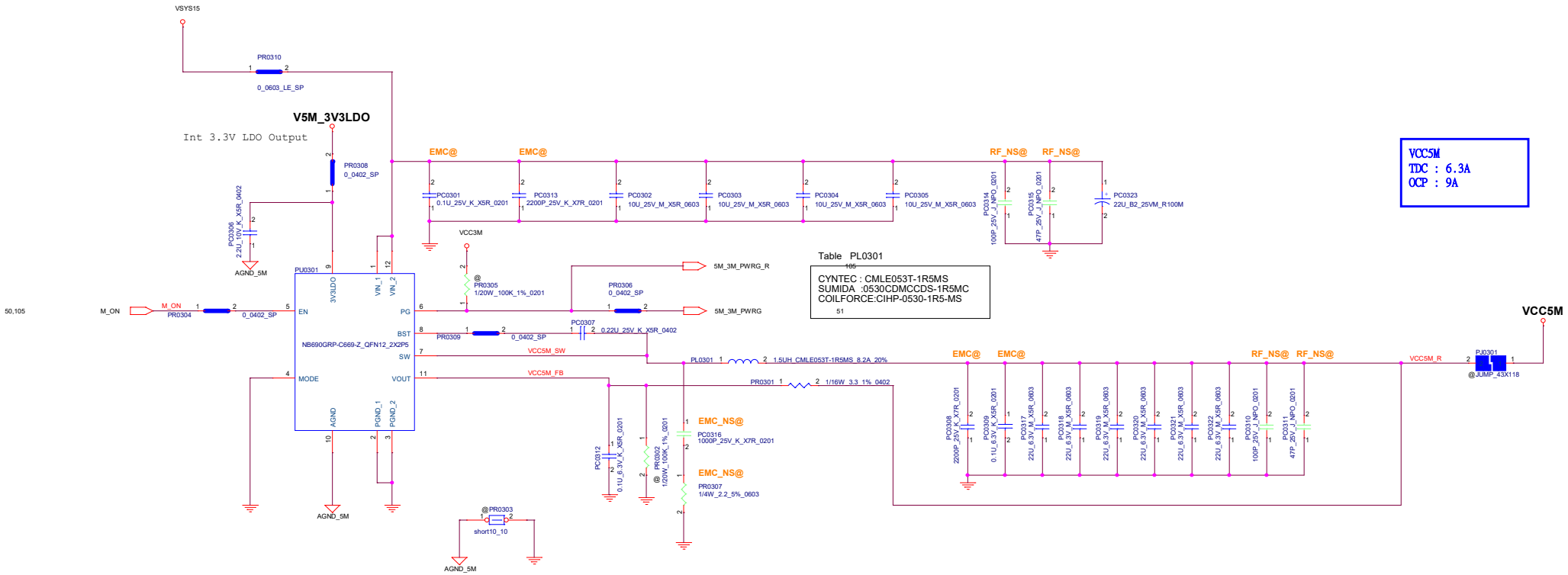

TABLE: NB690 Mode Control

RMode	MODE	VOUT	3V3LDO
0	Ceramic Cout	5.1V	3.3V
60K	POSCAP Cout	5.1V	3.3V
120K	Ceramic Cout	5V	3.3V
180K	POSCAP Cout	5V	3.3V
Floating	X	3.3V	3.3V

LOGIC

Document Number: DORAEMON			LCFC
Size: Custom	Title: DC/DC VCC5M (NB690)		Rev: 0.01
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TABLE : NB693 Mode Control

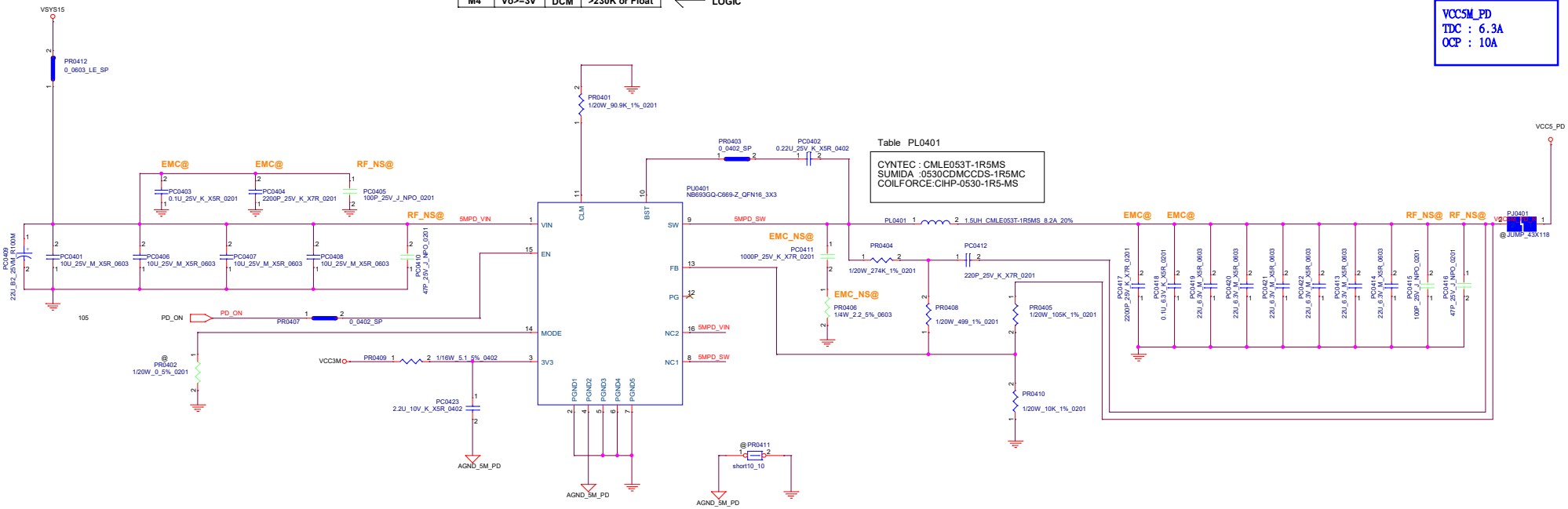
Mode	VOUT		RMode
M1	Vo<3V	DCM	0
M2	Vo<3V	CCM	90K
M3	Vo>=3V	CCM	150K
M4	Vo>=3V	DCM	>230K or Float

← LOGIC

VCC5M_PD
TDC : 6.3A
OCP : 10A

Table PL0401

CYNTEC : CMLE053T-1R5MS
SUMIDA :0530CDMCCDS-1R5MC
COILFORCE:CIHP-0530-1R5-MS



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Size: Custom	Title: DC/DC VCC5M_PD (NB693GQ)		Rev: 0.01
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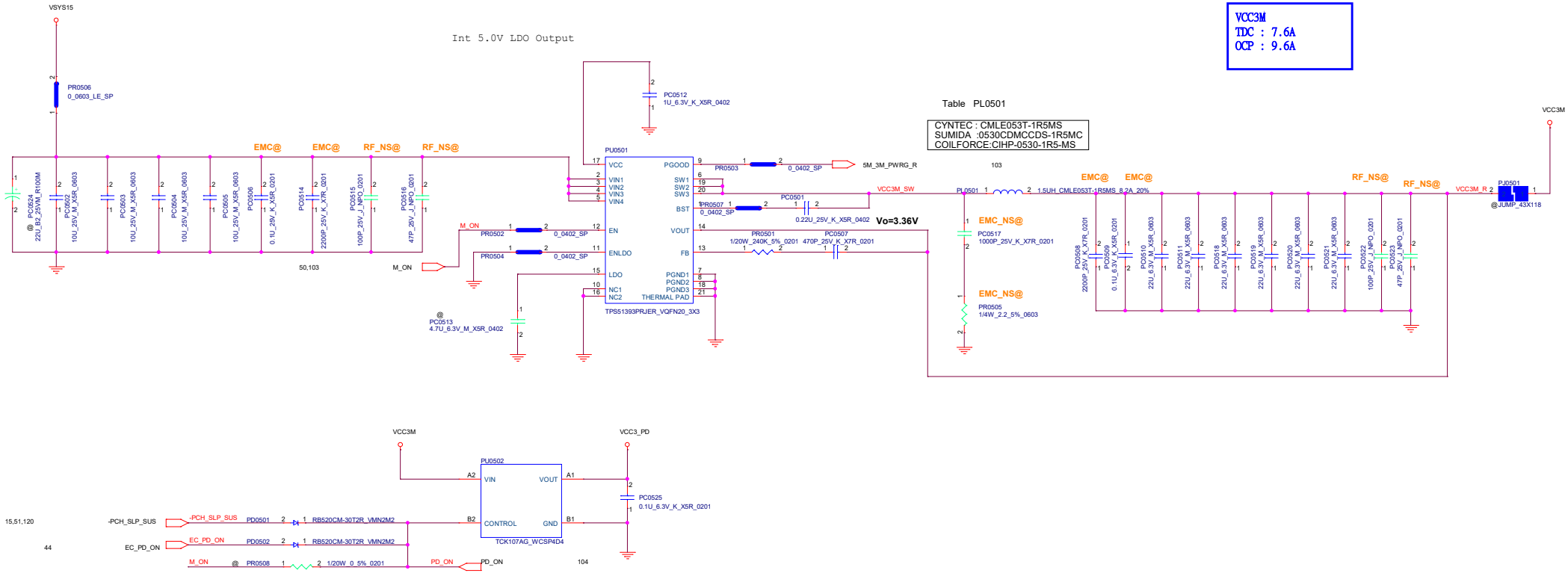

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Size: Custom	Title: DC/DC VCC3M (TPS51393P)		Rev: 0.01
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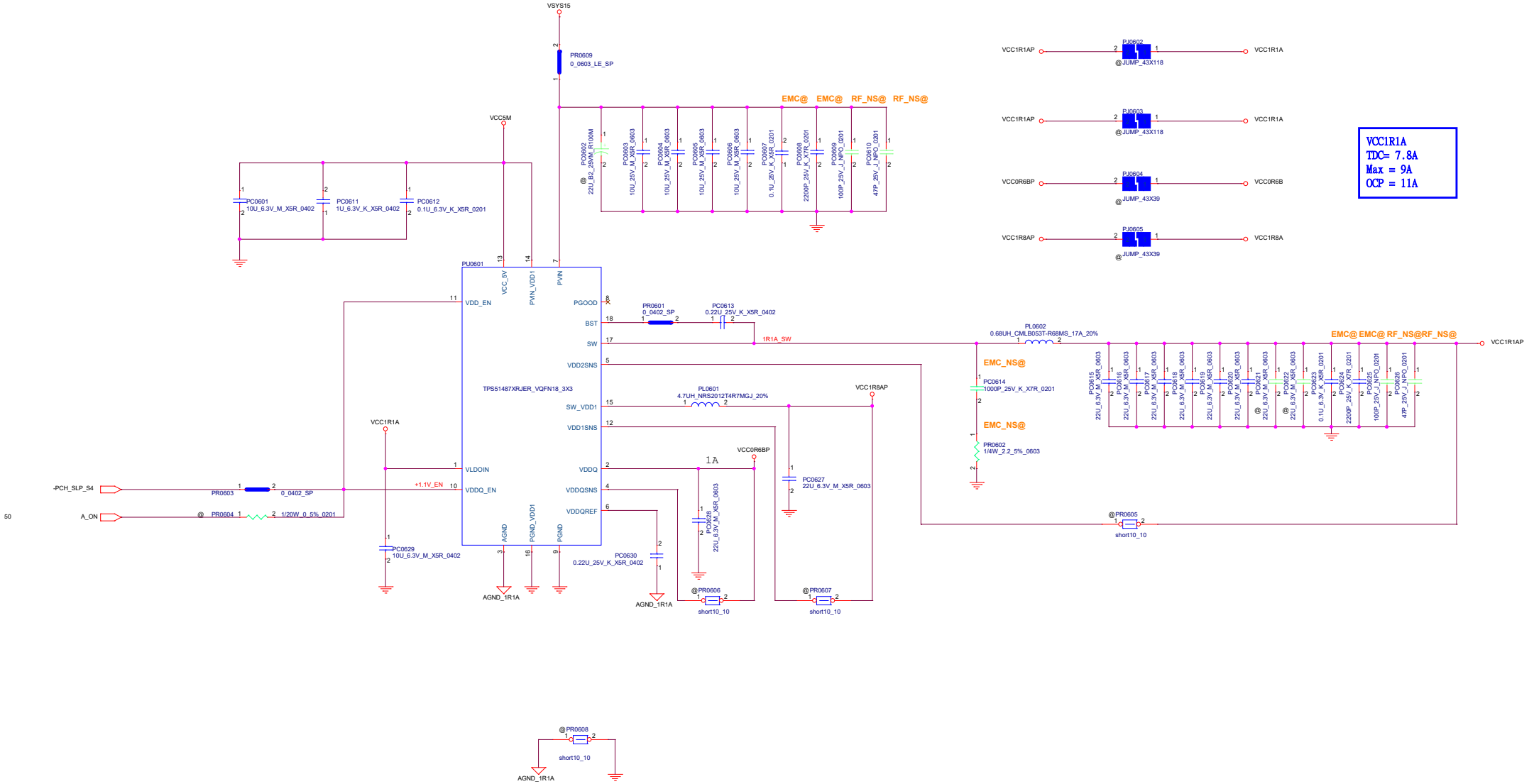

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Size: Custom	Title: DC/DC VCC1R2A/2R5A(NB687)		Rev: 0.01
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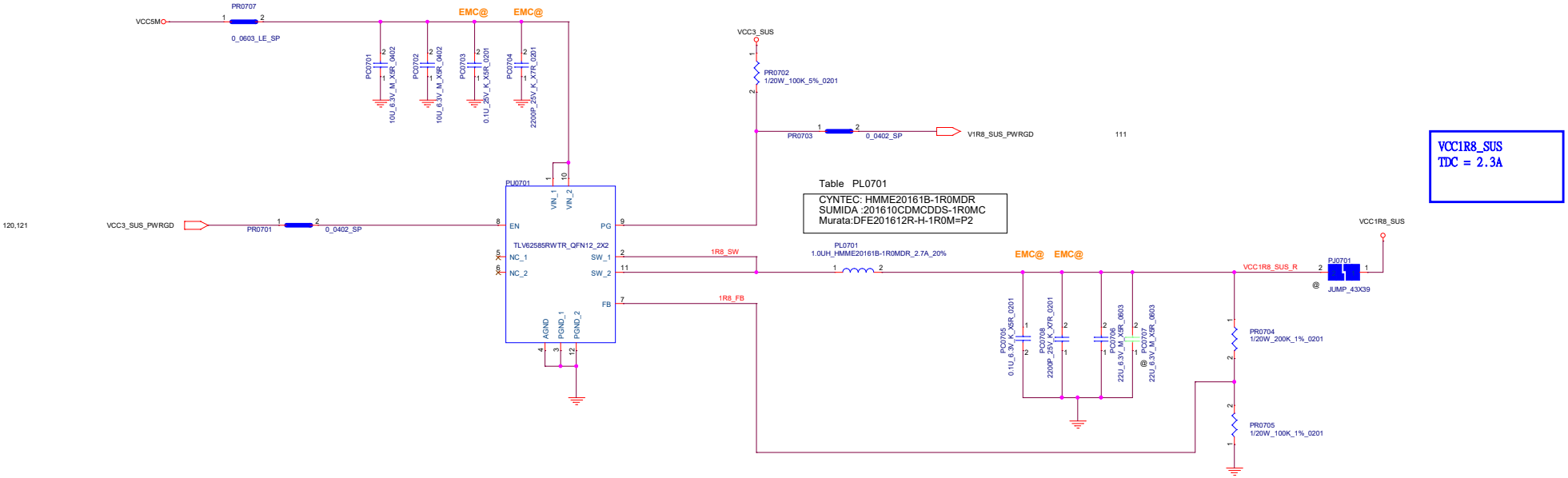

Table PL0701

CYNTEC: HMME20161B-1R0MDR
SUMIDA :201610CDMCDDS-1R0MC
Murata:DFE201612R-H-1R0M=P2

VCC1R8_SUS
TDC = 2.3A

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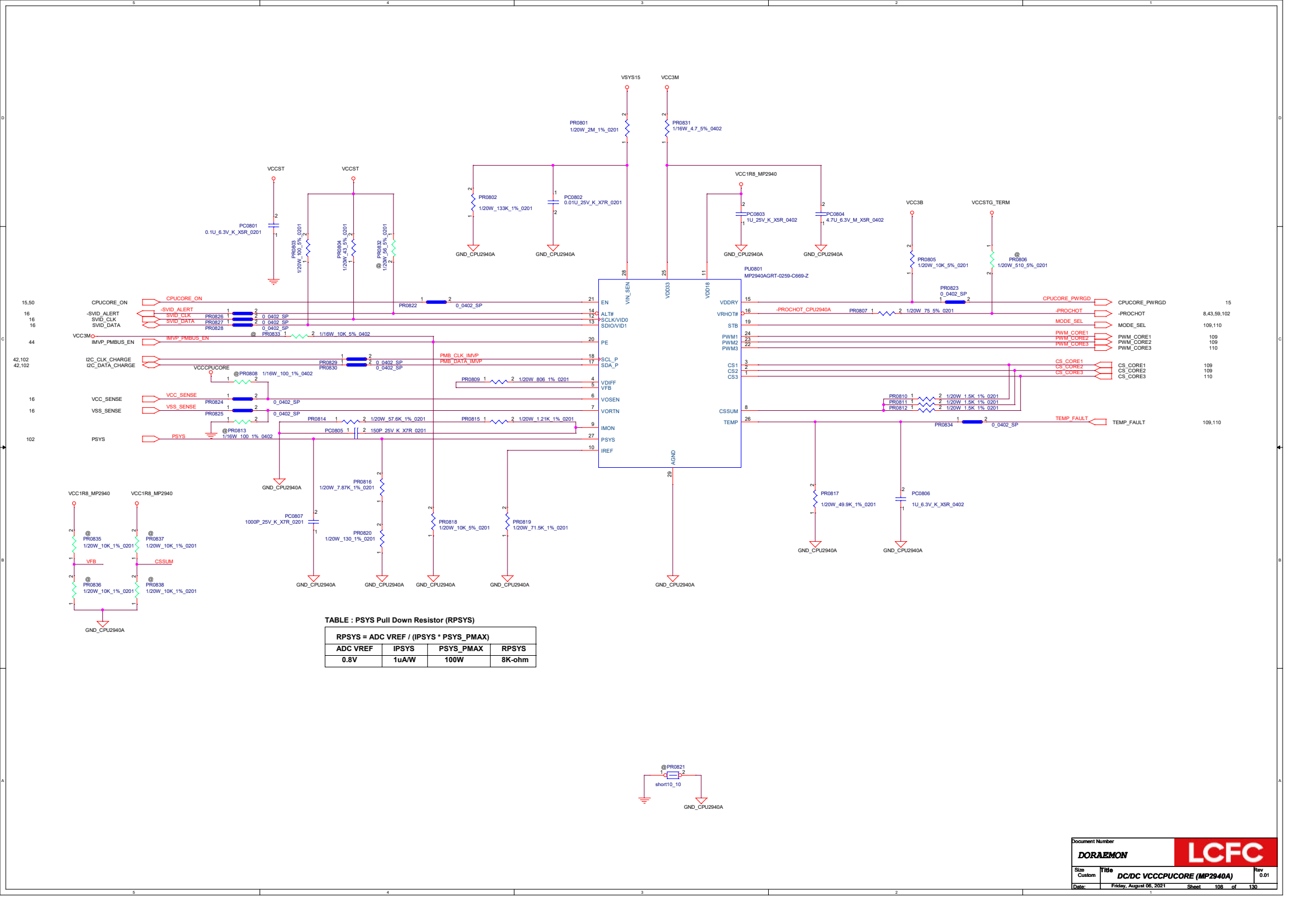

TABLE : PSYS Pull Down Resistor (RPSYS)

RPSYS = ADC VREF / (IPSYS * PSYS_PMAX)			
ADC VREF	**IPSYS**	**PSYS_PMAX**	**RPSYS**
0.8V	**1uA/W**	**100W**	**8K-ohm**

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Table PC0908,PC0909,PC0910

Panasonic:	25TQC68MYF
KEMET:	T521D686M025ATE070

VCCCPUCORE
UP3 4+2 28W(P)
TDC= 43A
IccMax= 65A

TABLE PL0901

SUMIDA	0624CDMCCDS_R22MC
CYNTEC	CMLS062D-R22MS-88

TABLE :

SYNC (MODE_SEL)

High	Normal Operation
H.Z.	Standby Mode
Low	Diode Emulation Mode

Table for PC0922, PC0923

Panasonic	ETPE330MA9L
NEC_TOKIN	TEPSGB20E337M9
KEMET	T520B337M2R5ATE009

TABLE PL0902

SUMIDA	0624CDMCCDS_R22MC
CYNTEC	CMLS062D-R22MS-88

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Size: Custom	Title: DC/DC VCCCPUCORE (MP86941 X 2)	Rev: 0.01
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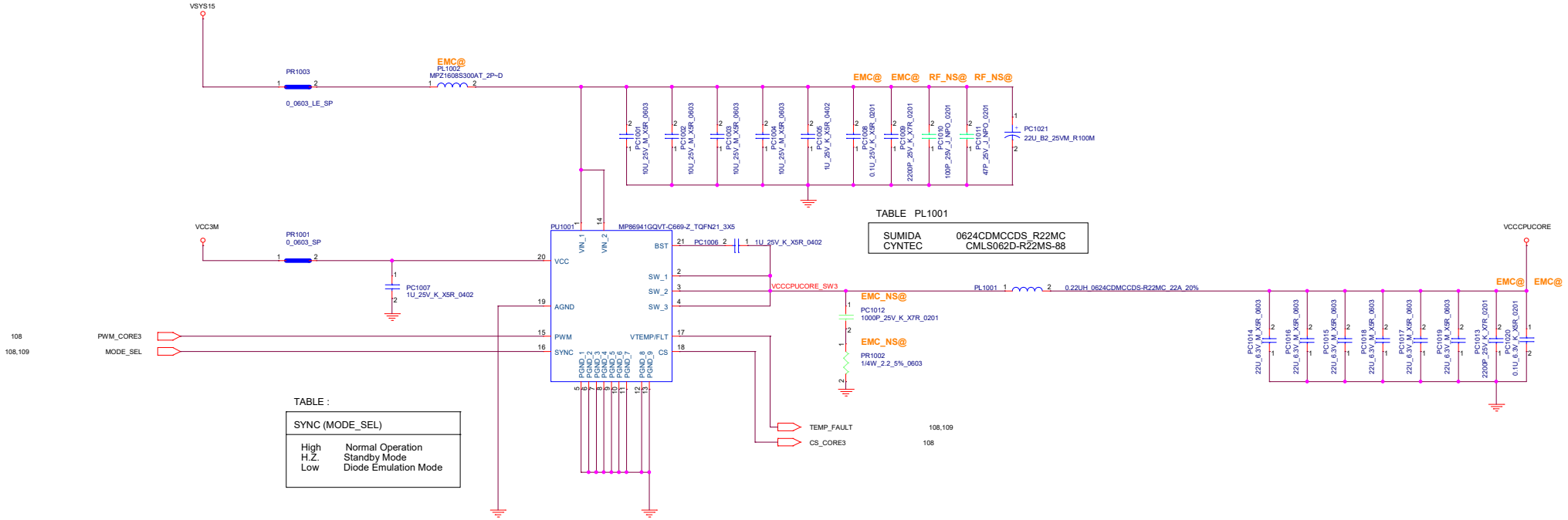

TABLE PL1001

SUMIDA	0624CDMCCDS_R22MC
CYNTEC	CMLS062D-R22MS-88

TABLE :

SYNC (MODE_SEL)	
High	Normal Operation
H.Z.	Standby Mode
Low	Diode Emulation Mode

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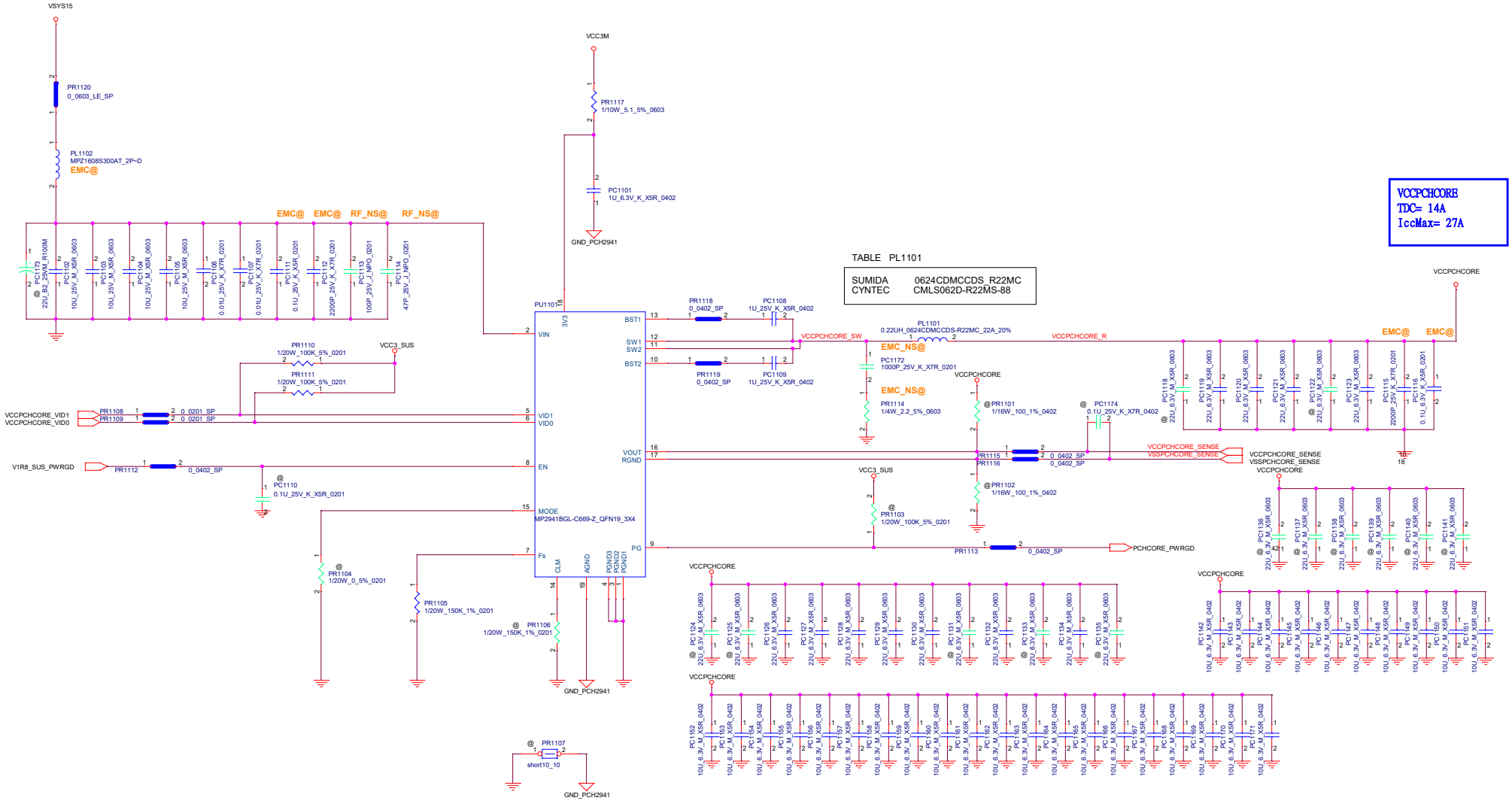

VCCPCHCORE
TDC= 14A
IccMax= 27A

TABLE PL1101

SUMIDA	0624CDMCCDS_R22MC
CYNTEC	CMLS062D-R22MS-88

TABLE:MODE

State	Interleaving	VID Down option	Resistor to GND
M1	No	Slew down	0
M2	Yes	Slew down	90K
M3	Yes	Decay	150K
M4	No	Decay	>230K or float

TABLE:FS

State	Fs(kHz)	Resistor to GND
M1	500	0
M2	700	90K
M3	1000	150K
M4	1200	>230K or float

MODE:CLM

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90K
M3	13A	150K
M4	17A	>230K or float

TABLE : MP2941 VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

TABLE : MP2941 R0 vs R1 (or later)

Item	R0	R1
VOUT	1.8V fixed	Defined by VCCPCHCORE VID1/VID0
RMode	0 ohm	Float
RFS	Float	Float or 150K
1Kohm bleeder	Necessary	Not necessary

TABLE for PC1117

Panasonic	ETPE330MA9L
NEC_TOKIN	TEPSGB20E337M9
KEMET	i@T520B337M2R5ATE009

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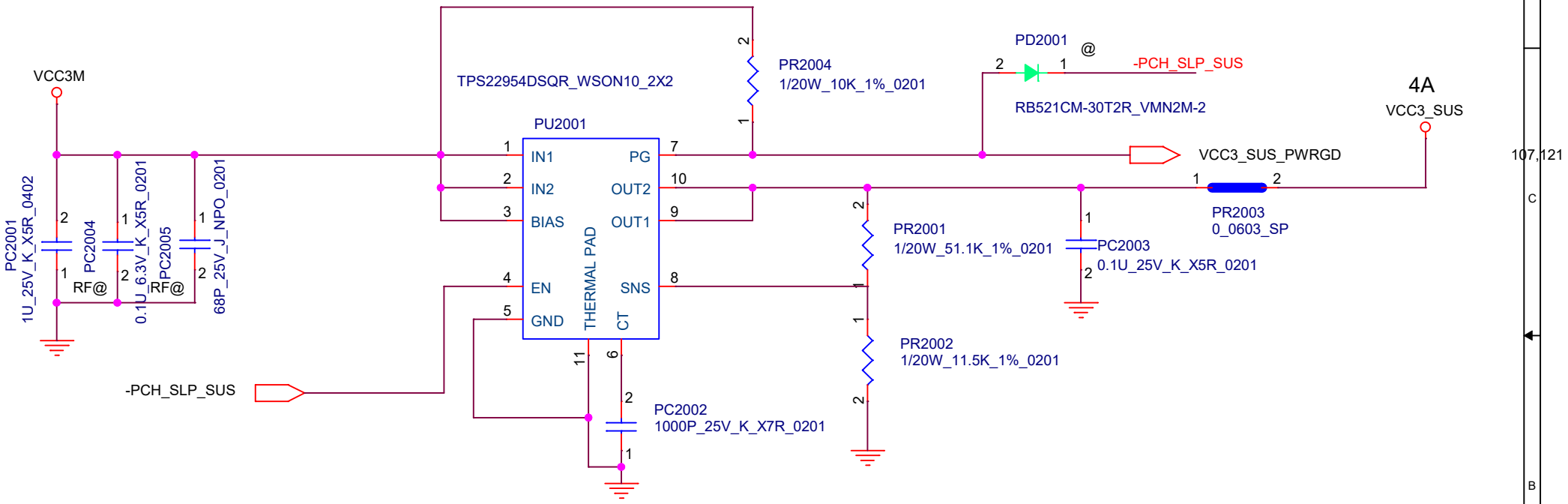

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Project Name : CS21 X1 HDI	Title : LOAD SW VCC3_SUS	
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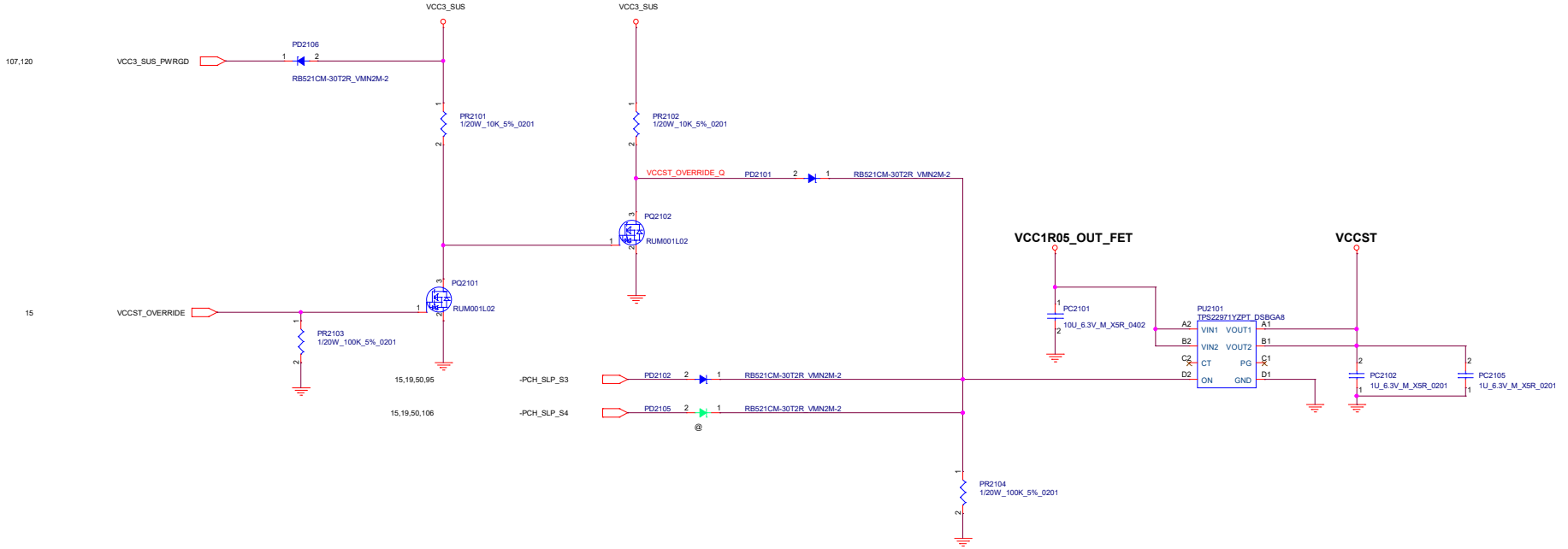

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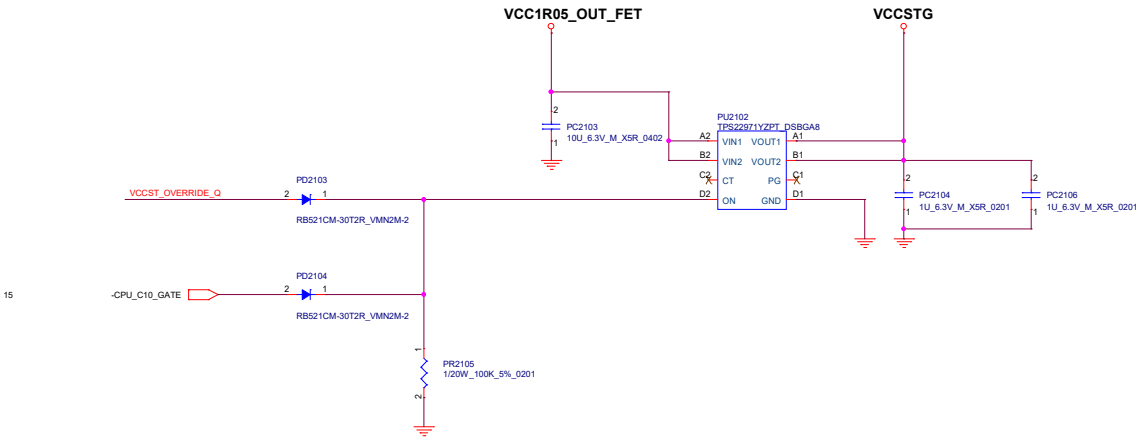

Lenovo			
Project Name : CS21 X1 HDI		Title : LOAD SW VCCST & VCCSTG	
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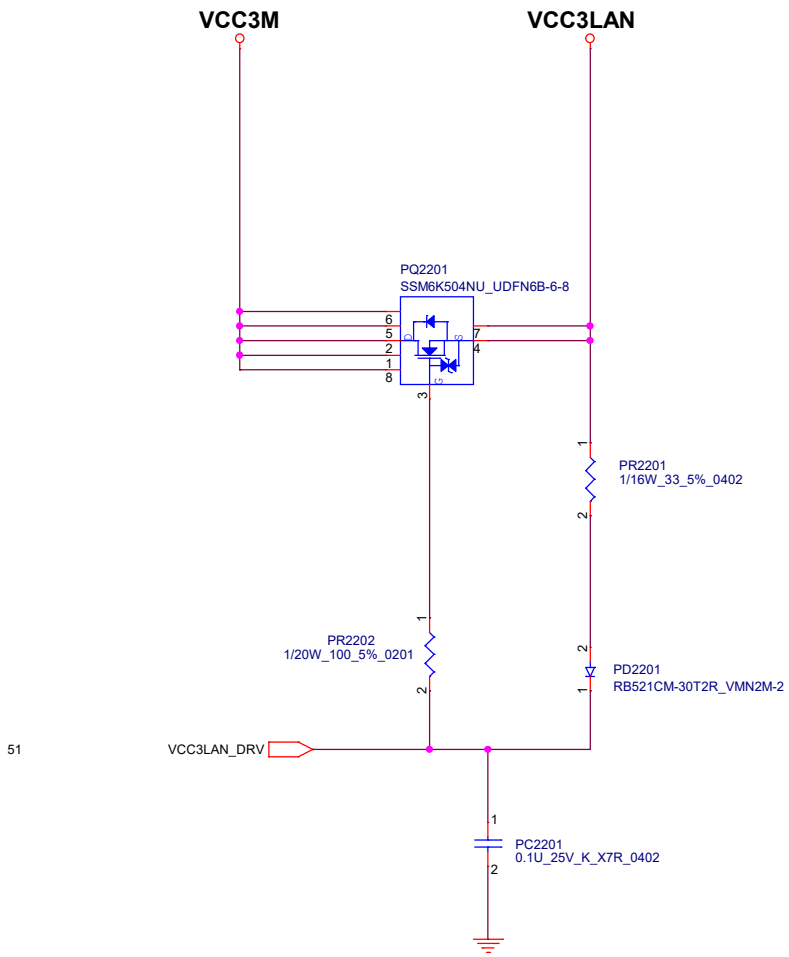

Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	

Title	LOAD SW LAN	
Size: B	Document Number: Drift/Ironhide_CML	Rev: 1.0
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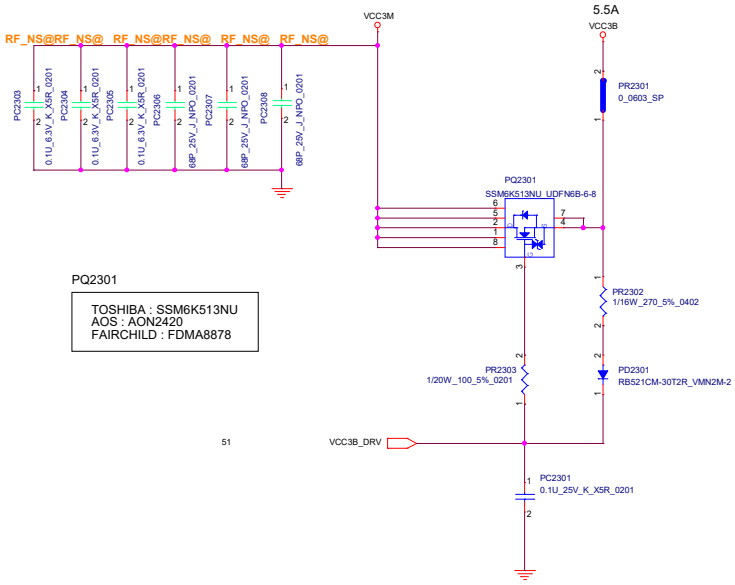
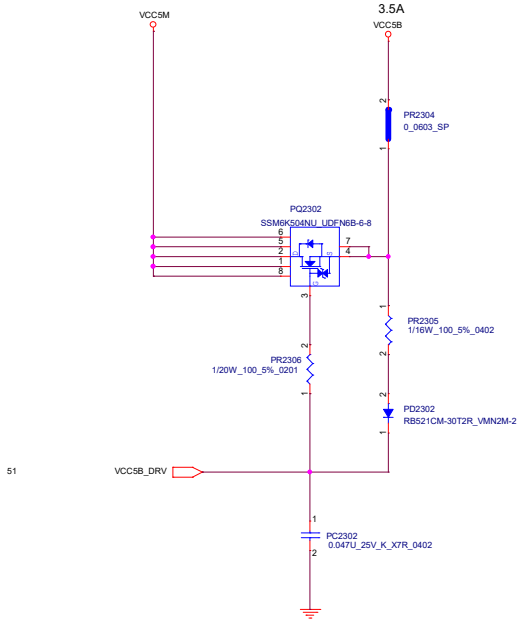


PQ2301

TOSHIBA : SSM6K513NU
AOS : AON2420
FAIRCHILD : FDMA8878



PQ2302

TOSHIBA : SSM6K504NU
ROHM : RF4E080BNTR
AOS : AON2420

Project Name : CS21 X1 HDI	Title : LOAD SW B	
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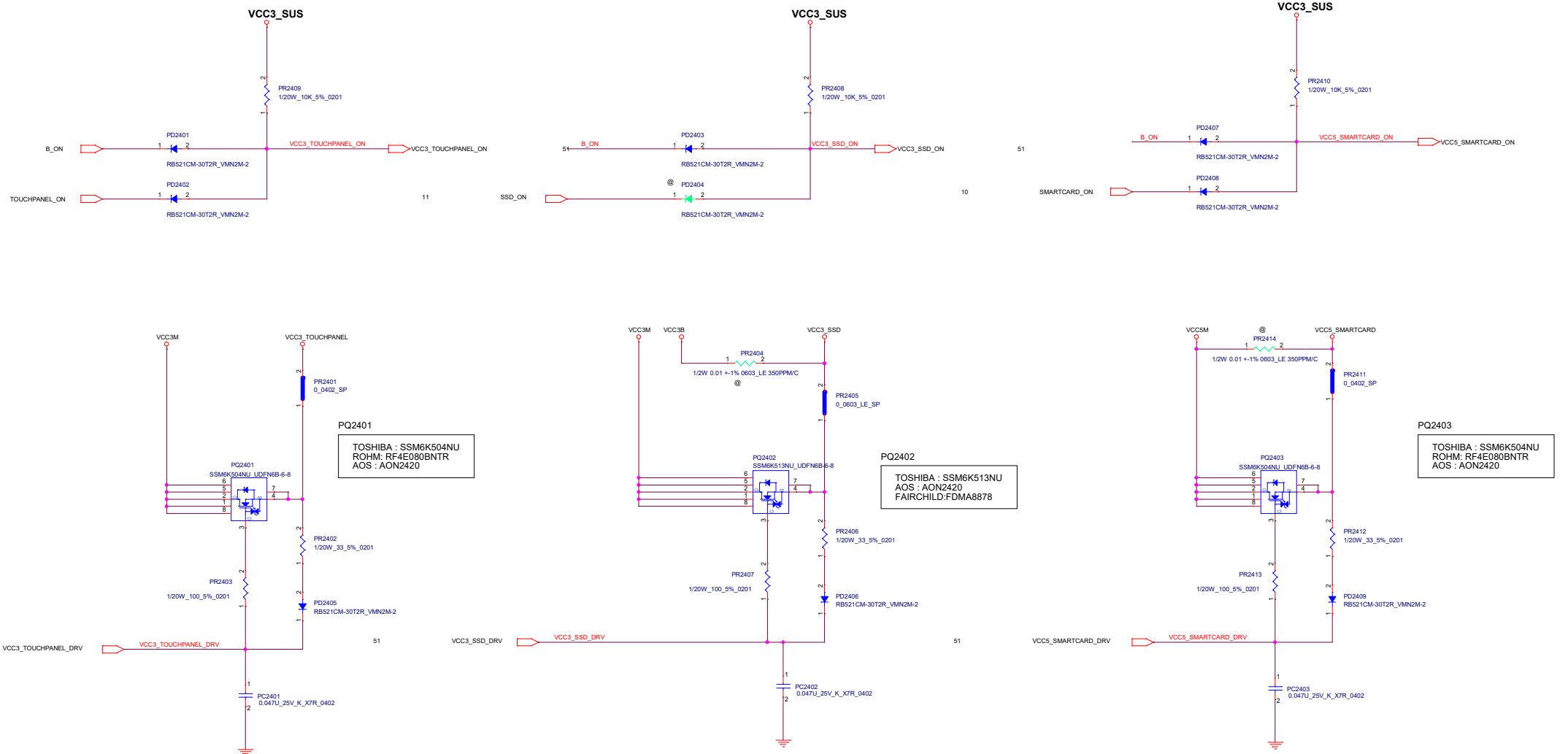

Project Name : CS21 X1 HDI		Title : LOAD SW TOUCH PANEL & SSD	
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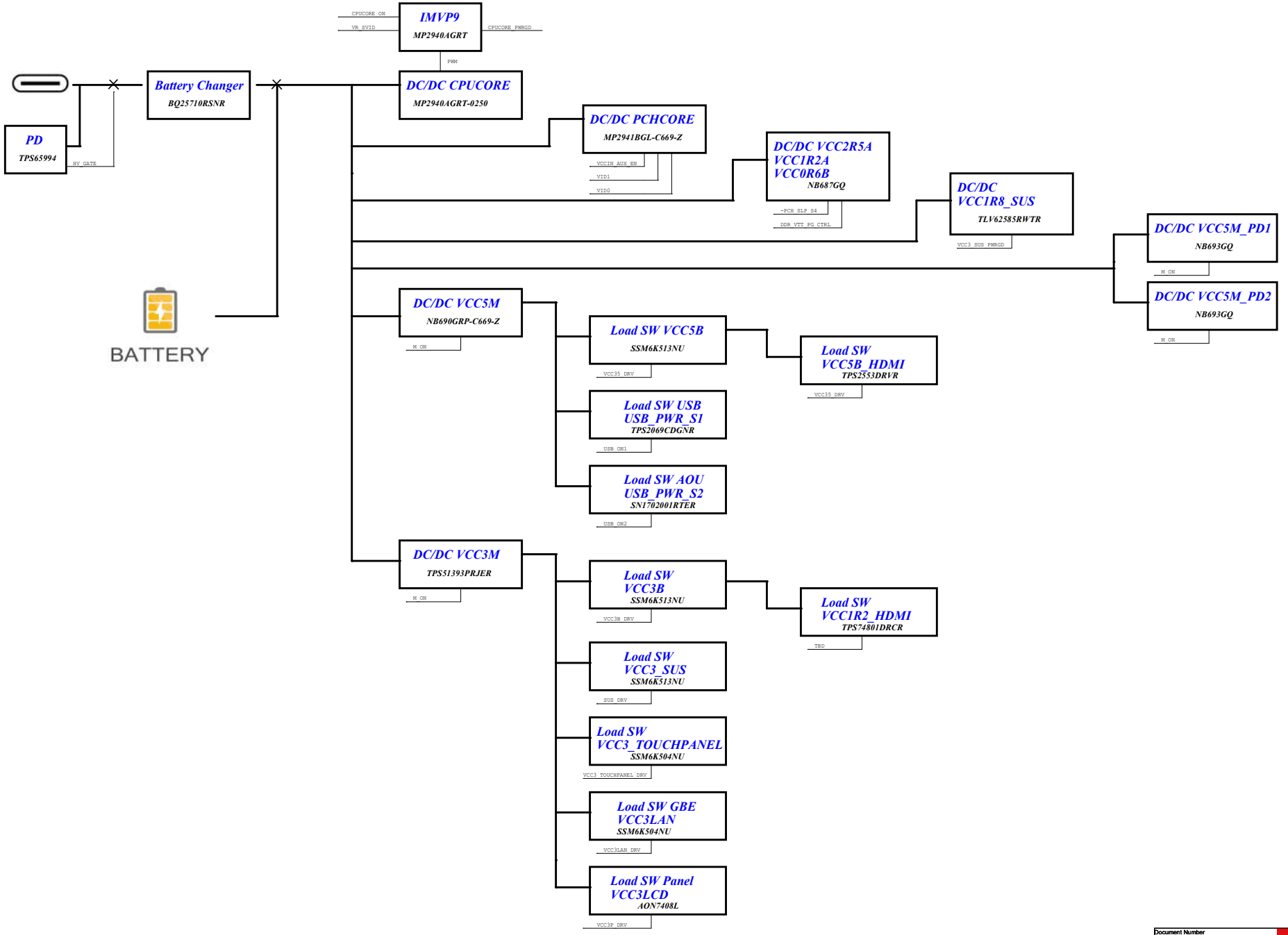

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Size: Custom	Title: System Power Tree	Rev: 0.01
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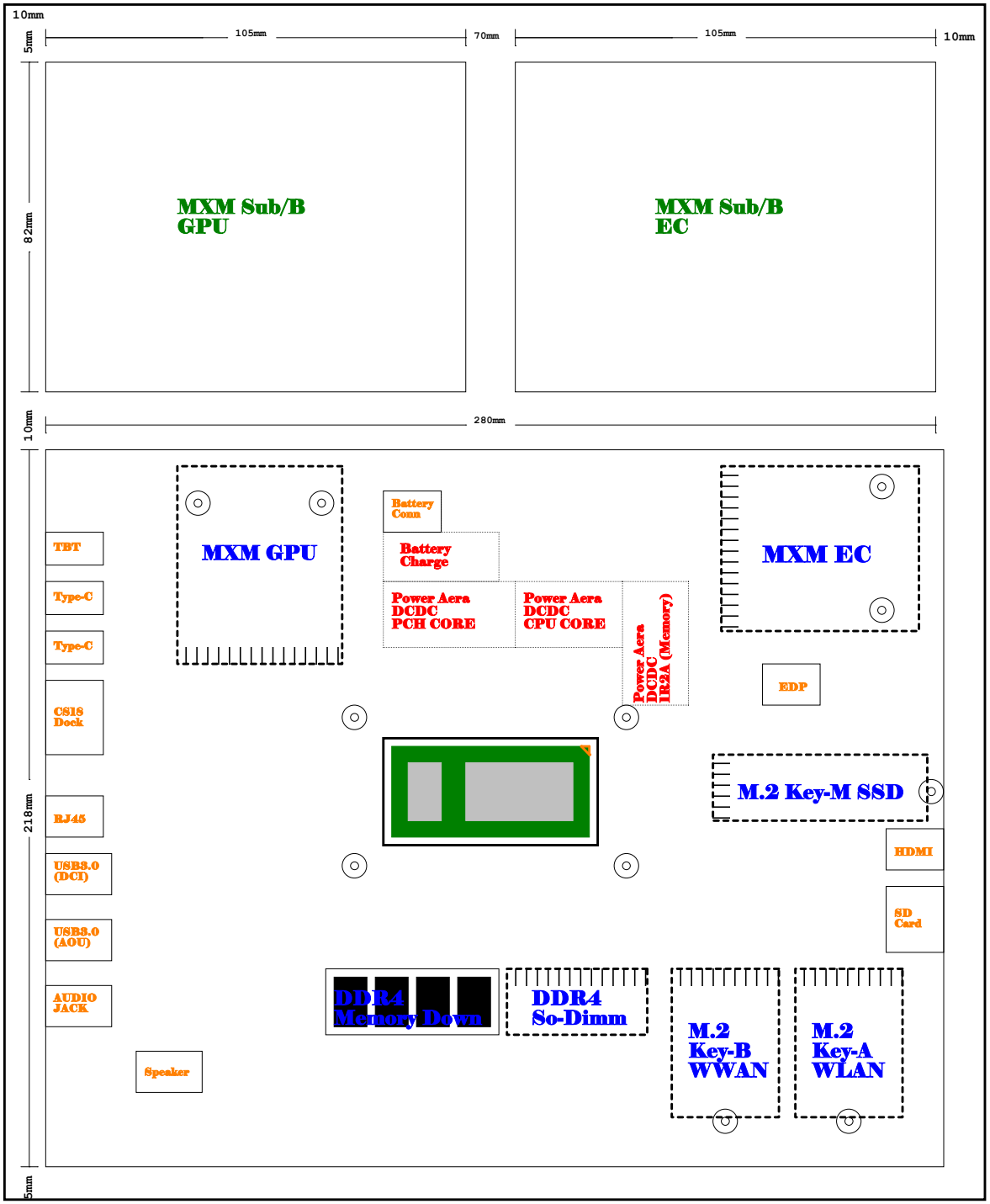

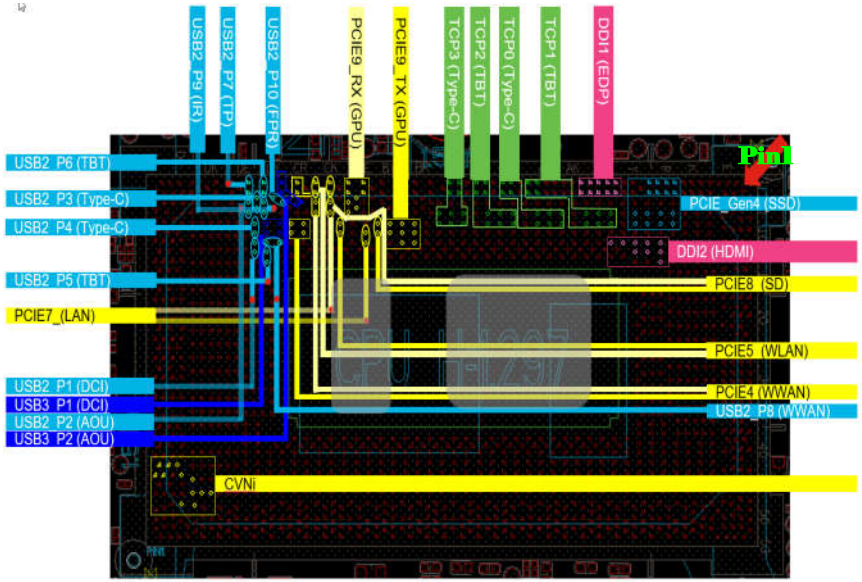

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