GA-M61PME-S2

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27	FRONT PANEL POWER SEQUENCE
28	ATX POWER, VCC12_DUAL, VDDA25
29	PWM ISL6312

Revision: 2.02

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M61PME-S2 | Rev: 2.02

Date: Thursday, January 24, 2008 | Sheet 1 of 29

Model Name:GA-M61PME-S2 Rev.2.02

Component value change history

P-Code: U96133-0

Date	Change Item		Reason
2007.12.12	1.0A E_BOM issue	PCB:1.0	New BOM release Change MCP61S to A3
2007.12.12	2.0B P_BOM issue	PCB:2.02	Change IDE Boxheader to white Change 22uf Cap to 0805 Change CAP to 50V (WC18)
2008.01.24	2.0B MP_BOM issue	PCB:2.02	Add PCB second source 鼎富&全成信

Circuit or PCB layout change for next version

Date	Change Item	Reason
2007.12.12	1.0 Gerber Out	Modify from M61SME-S2L 2.02. Can share PCB with M61SME-S2L 2.02
2007.12.27	2.02 Gerber Out	Modify from CBC47 & CBC48 22uF 1206 change to 0805

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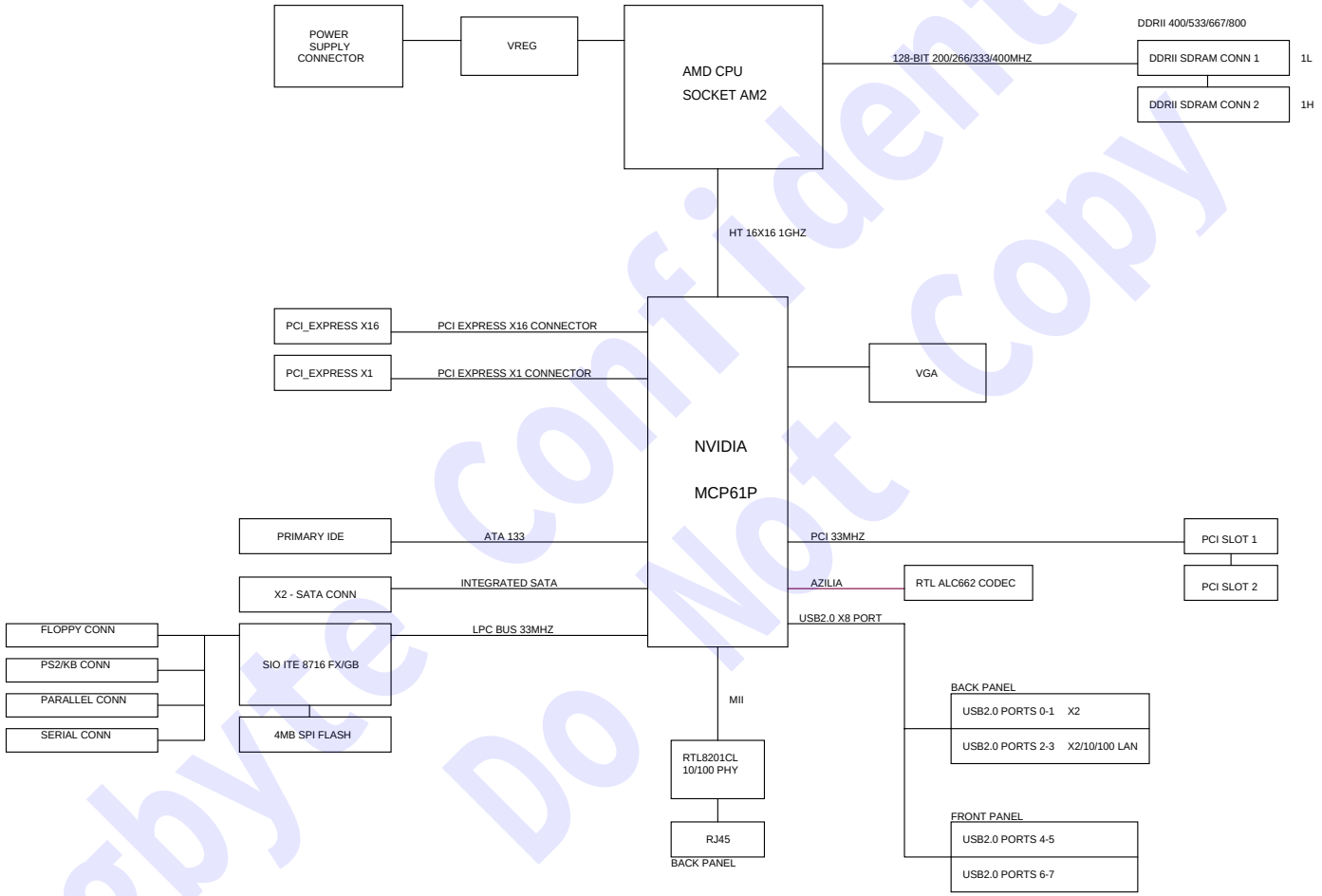
Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-M61PME-S2 | Rev: 2.02

Date: Tuesday, February 12, 2008 | Sheet 2 of 29

BLOCK DIAGRAM



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Title: BLOCK DIAGRAM

Size: Custom | Document Number: GA-M61PME-S2 | Rev: 2.02

Date: Thursday, January 24, 2008 | Sheet 3 of 29

L0_CADIN_L[0..15] L0_CADIN_L[0..15] <11>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <11>
L0_CLKIN_L[0..1] L0_CLKIN_L[0..1] <11>
L0_CLKIN_H[0..1] L0_CLKIN_H[0..1] <11>
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <11>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <11>
L0_CLKOUT_L[0..1] L0_CLKOUT_L[0..1] <11>
L0_CLKOUT_H[0..1] L0_CLKOUT_H[0..1] <11>

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1
L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1
L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0
L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0
				Y6	1 TP78
				W6	1 TP79
L0_CTLIN_H0	U1	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	W2	L0_CTLOUT_H0 <11>
L0_CTLIN_L0	V1	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W3	L0_CTLOUT_L0 <11>
		L0_CTLIN_H(0)	L0_CTLOUT_H(0)		
		L0_CTLIN_L(0)	L0_CTLOUT_L(0)		
L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15
L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15
L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14
L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14
L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13
L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13
L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12
L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12
L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11
L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11
L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10
L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10
L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9
L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9
L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8
L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8
L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7
L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7
L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6
L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6
L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5
L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5
L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4
L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4
L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3
L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3
L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2
L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2
L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1
L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1
L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0
L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0

VCC12_HT R3 49.9/4/1 V4
GND R4 49.9/4/1 V5

SOCKET_M2

M2/[12KRC-04K807-22R_12KRC-04K807-23R]

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Title: CPU HYPER TRANSPORT

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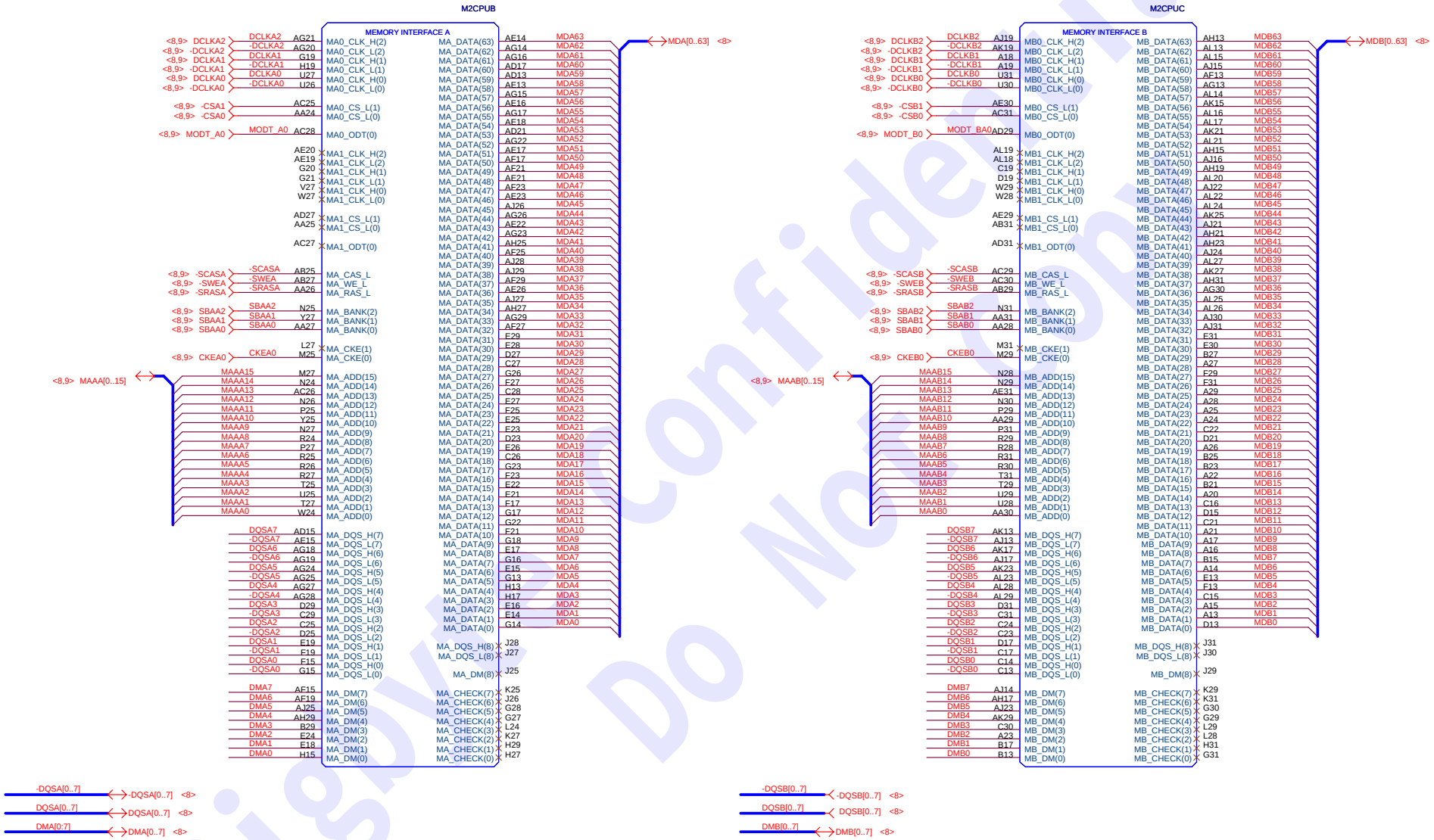

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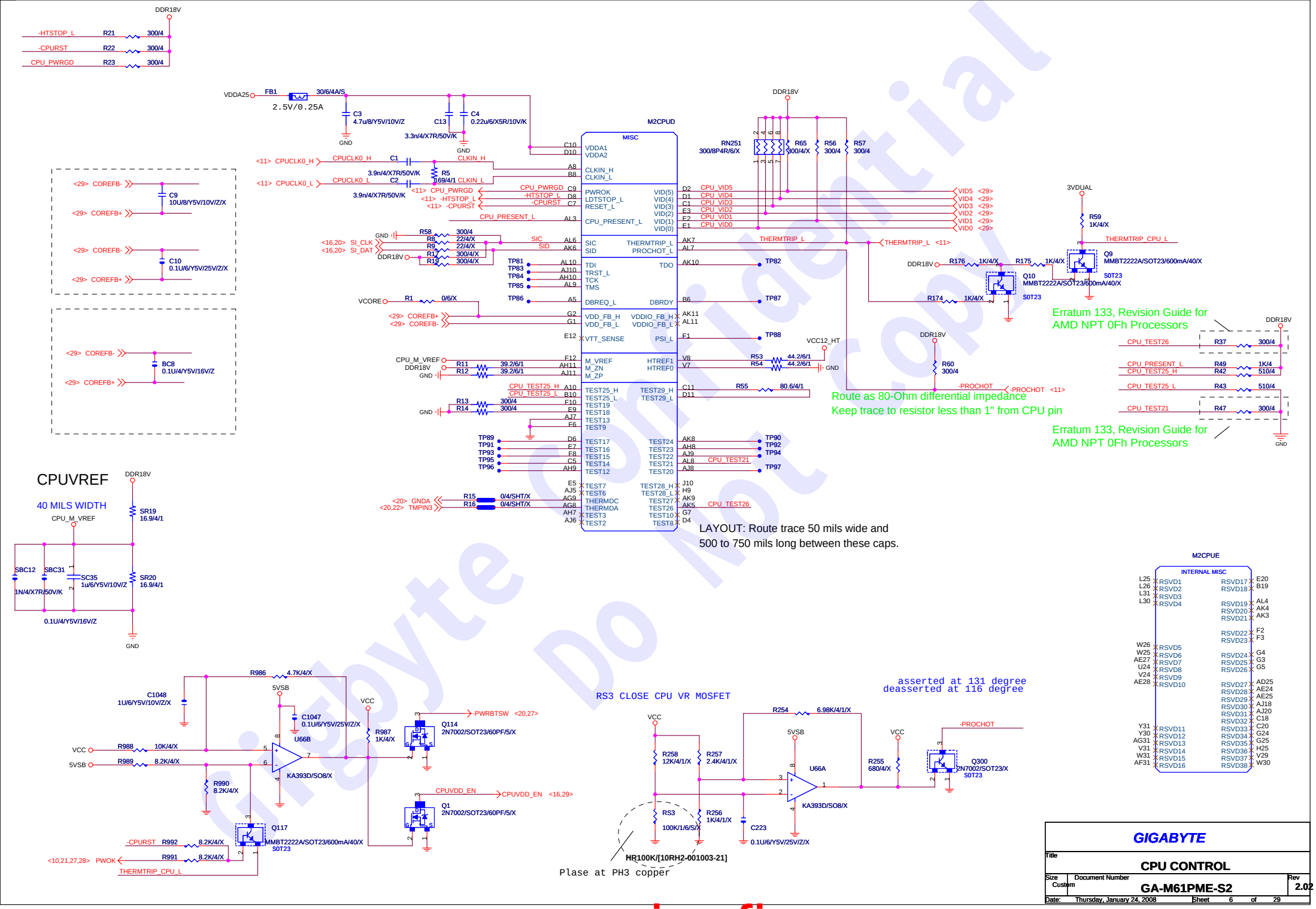
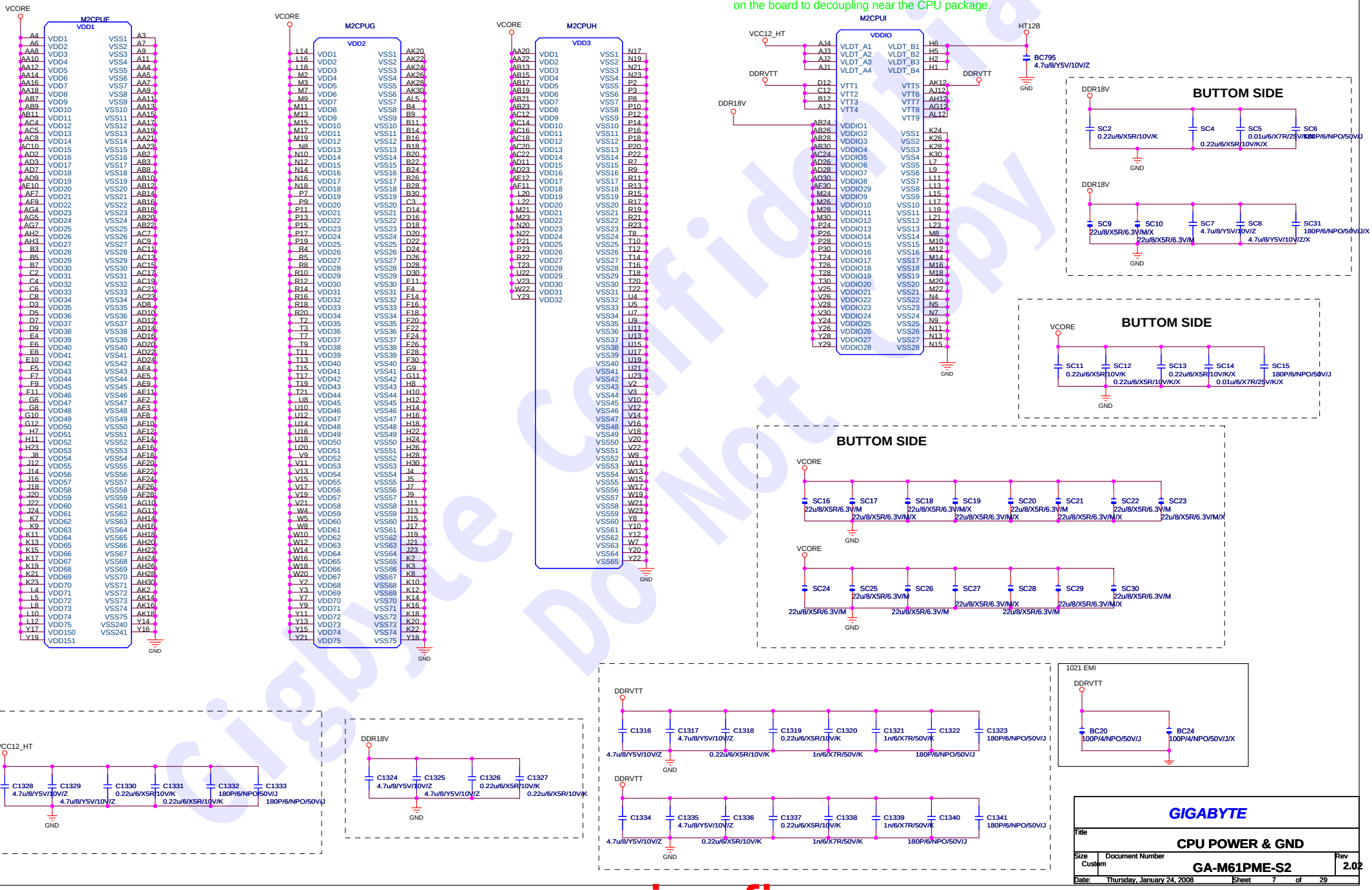
Title	CPU DDRII MEMORY	
Size: Custom	Document Number: GA-M61PME-S2	Rev: 2.02
Date: Thursday, January 24, 2008	Sheet 5 of 29	



VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



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Title	CPU POWER & GND	
Size: Custom	Document Number: GA-M61PME-S2	Rev: 2.02
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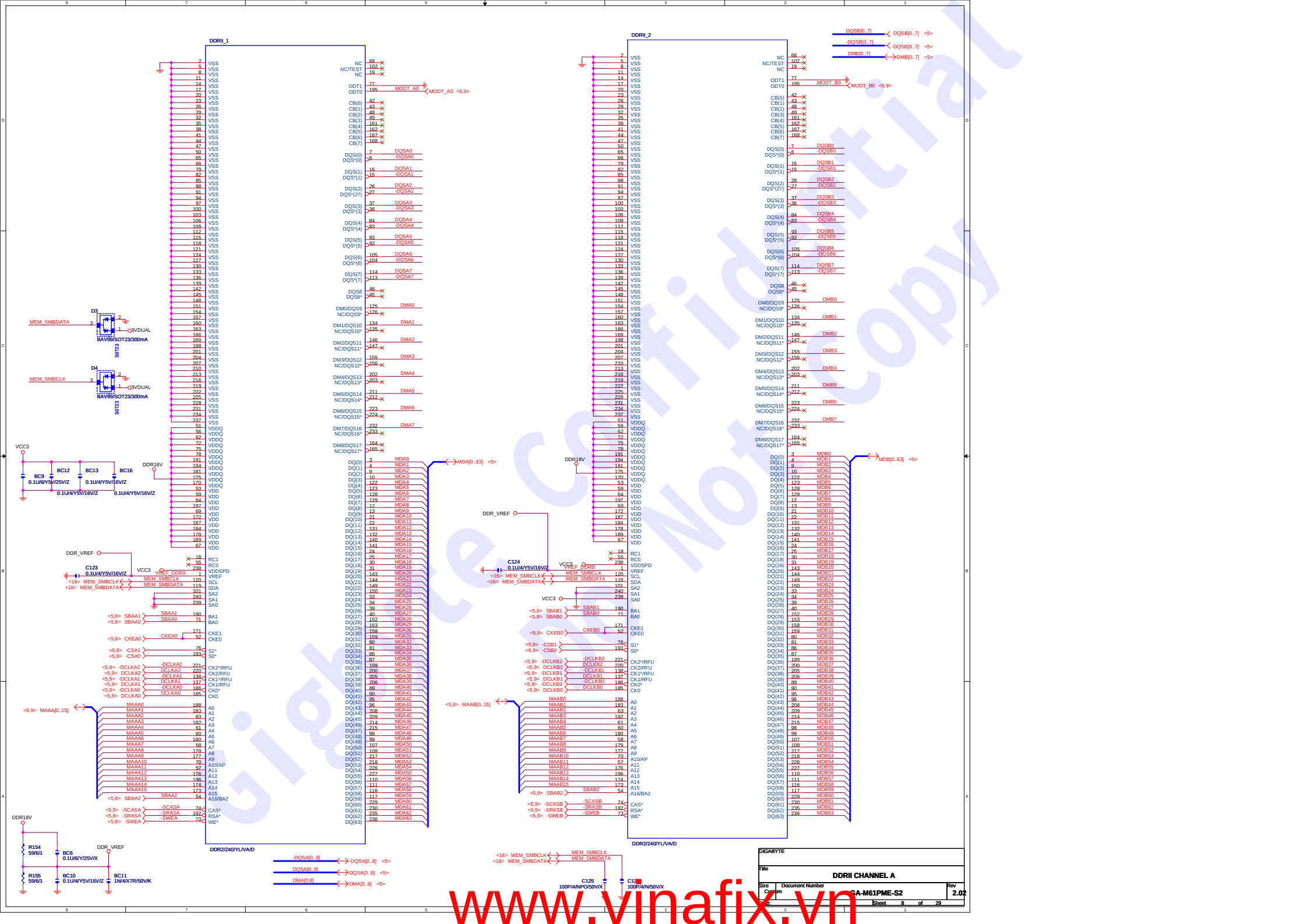

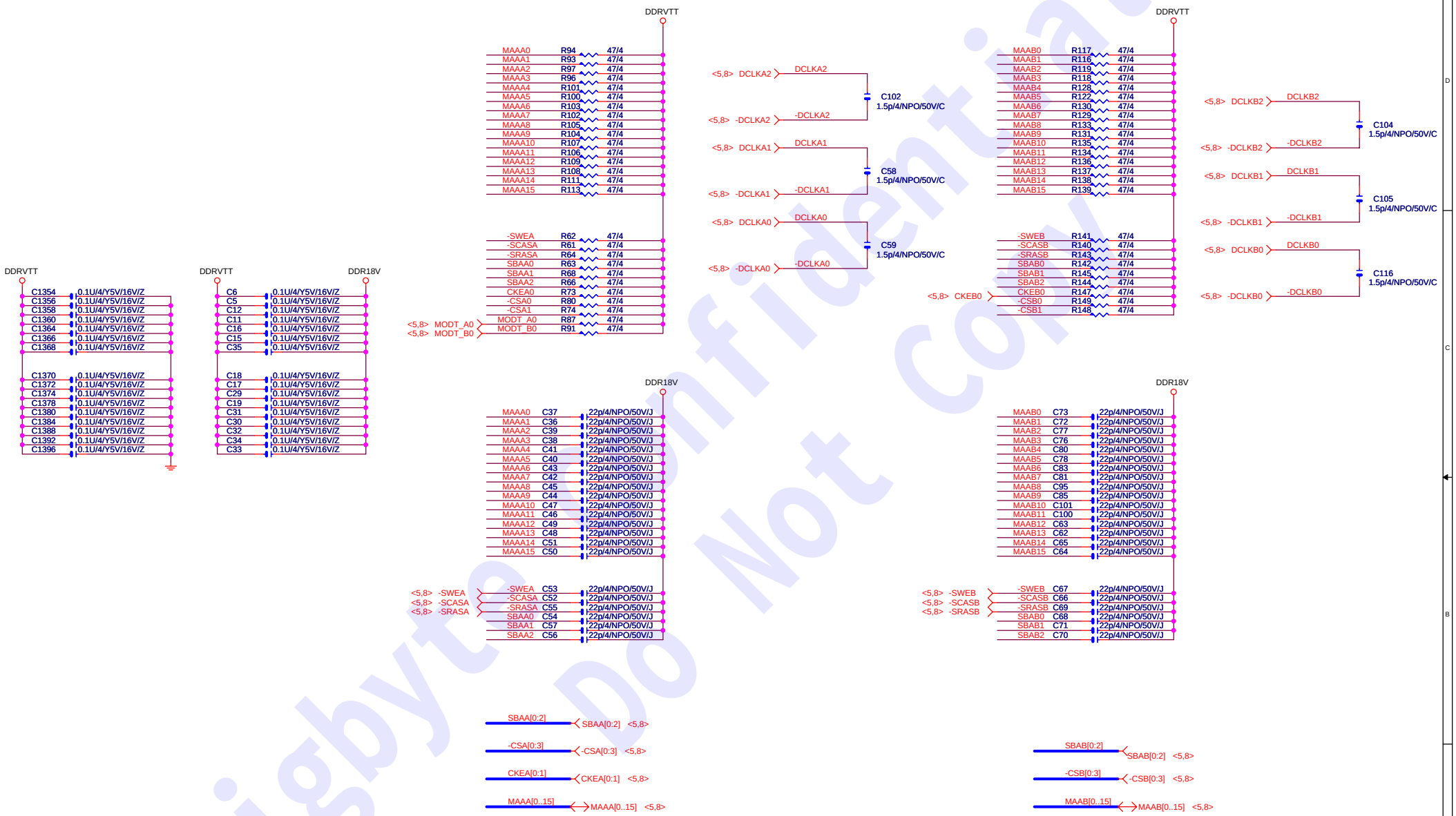

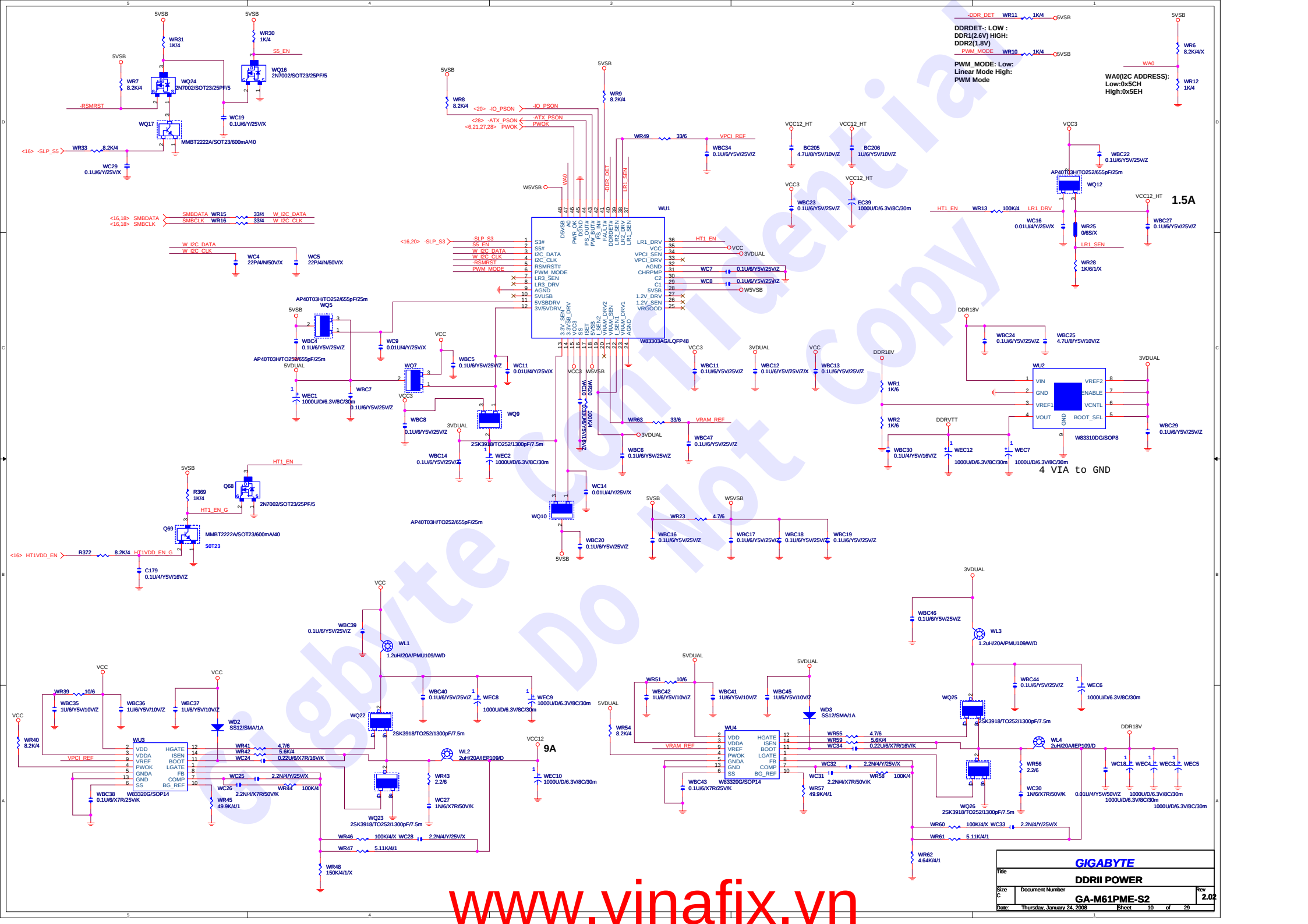
DDRDET-: LOW :
DDR1(2.6V) HIGH:
DDR2(1.8V)
PWM_MODE: Low:
Linear Mode High:
PWM Mode
WA0(I2C ADDRESS):
Low:0x5CH
High:0x5EH
1.5A
4 VIA to GND
W83303AG/LQFP48
W83310DG/SOP8
W83320G/SOP14
GIGABYTE
DDRII POWER
GA-M61PME-S2
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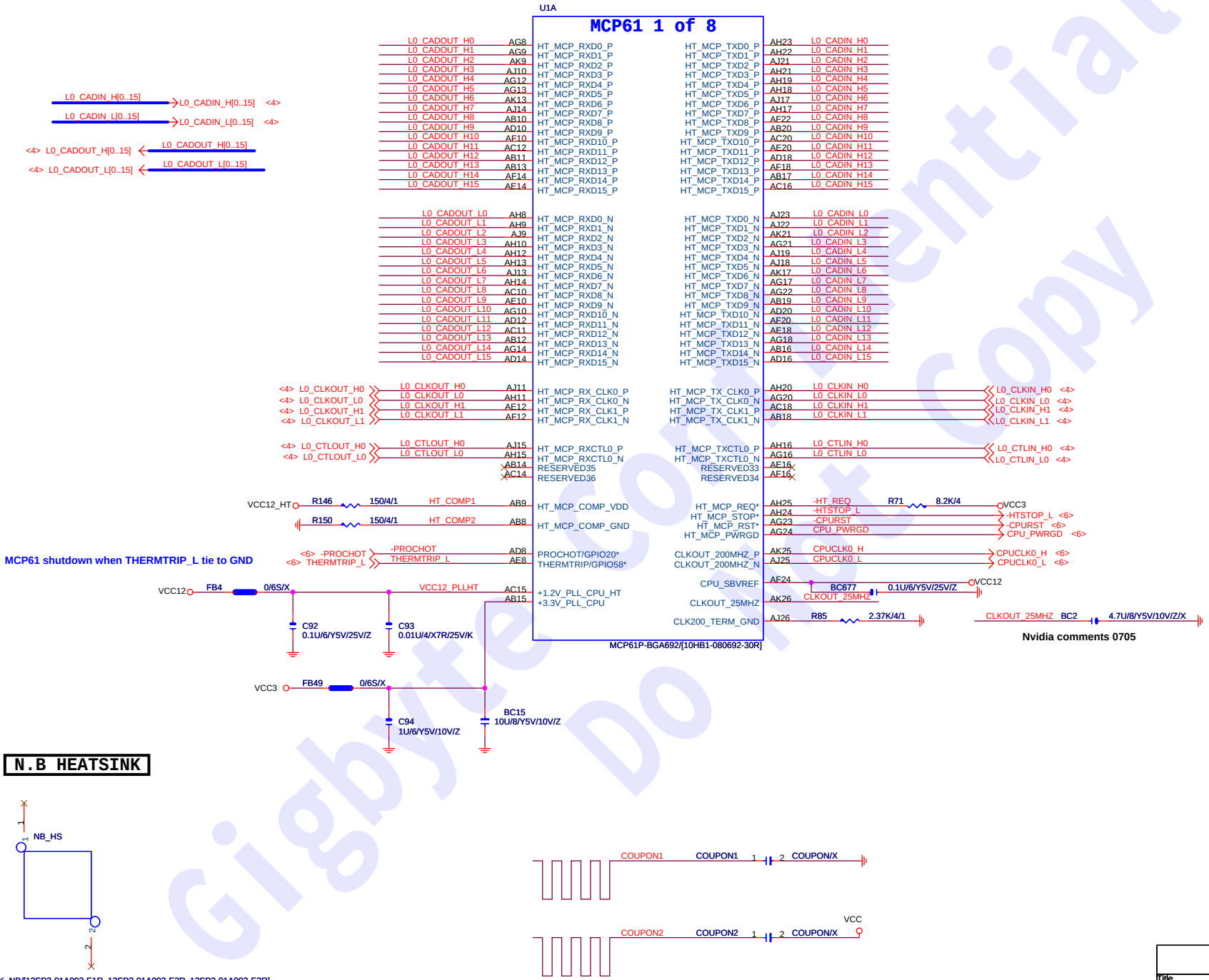

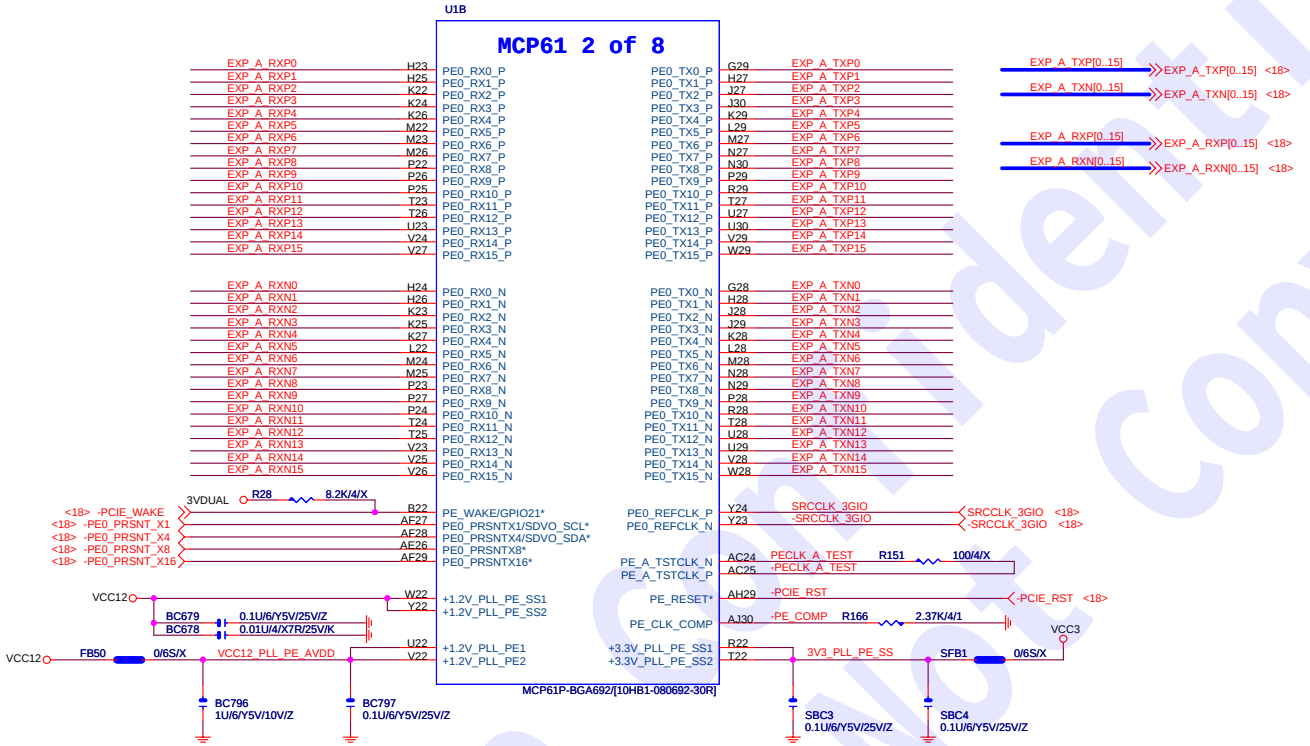

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Title: MCP61-PCI EXPRESS

Size: Custom | Document Number: GA-M61PME-S2 | Rev: 2.02

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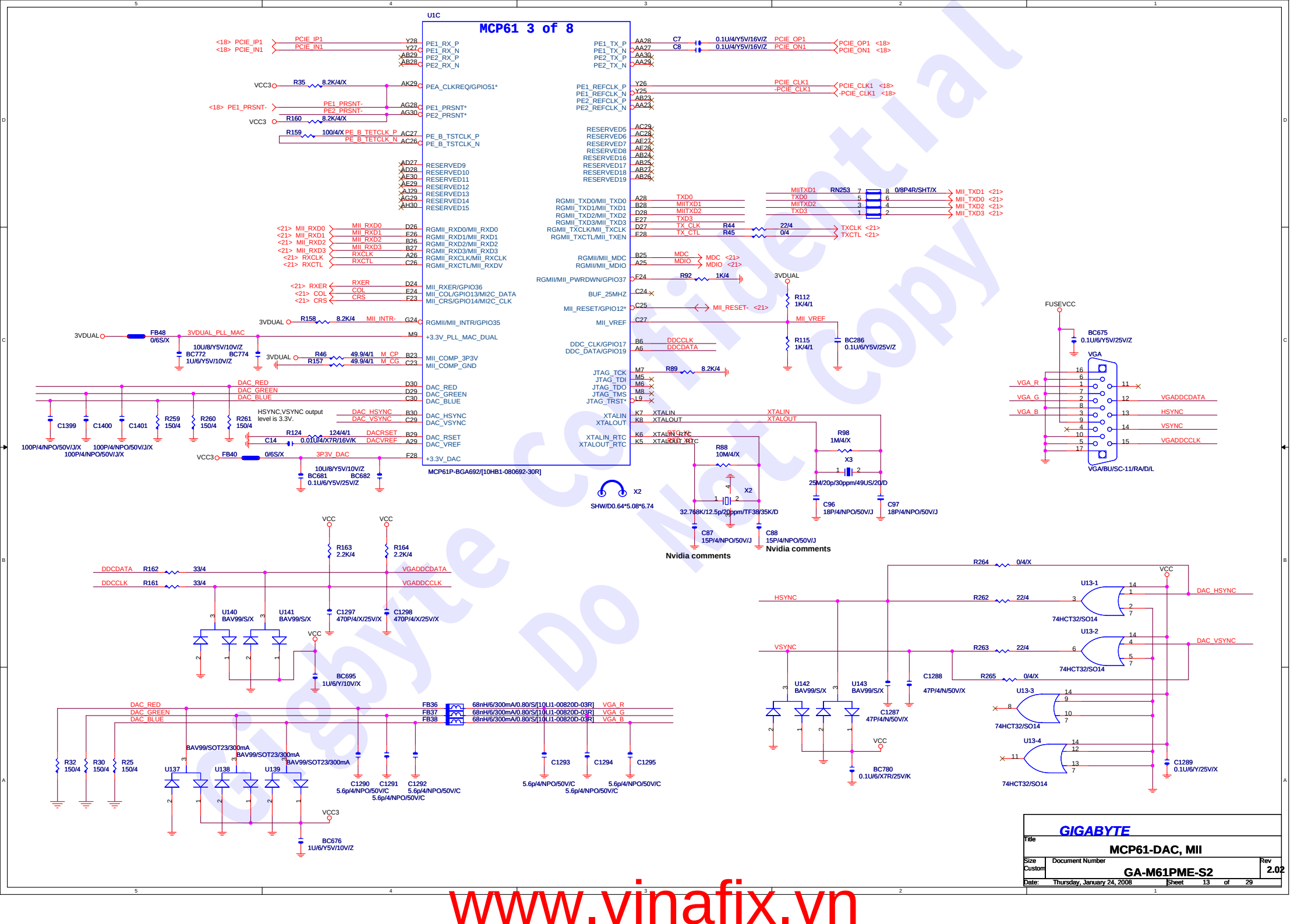

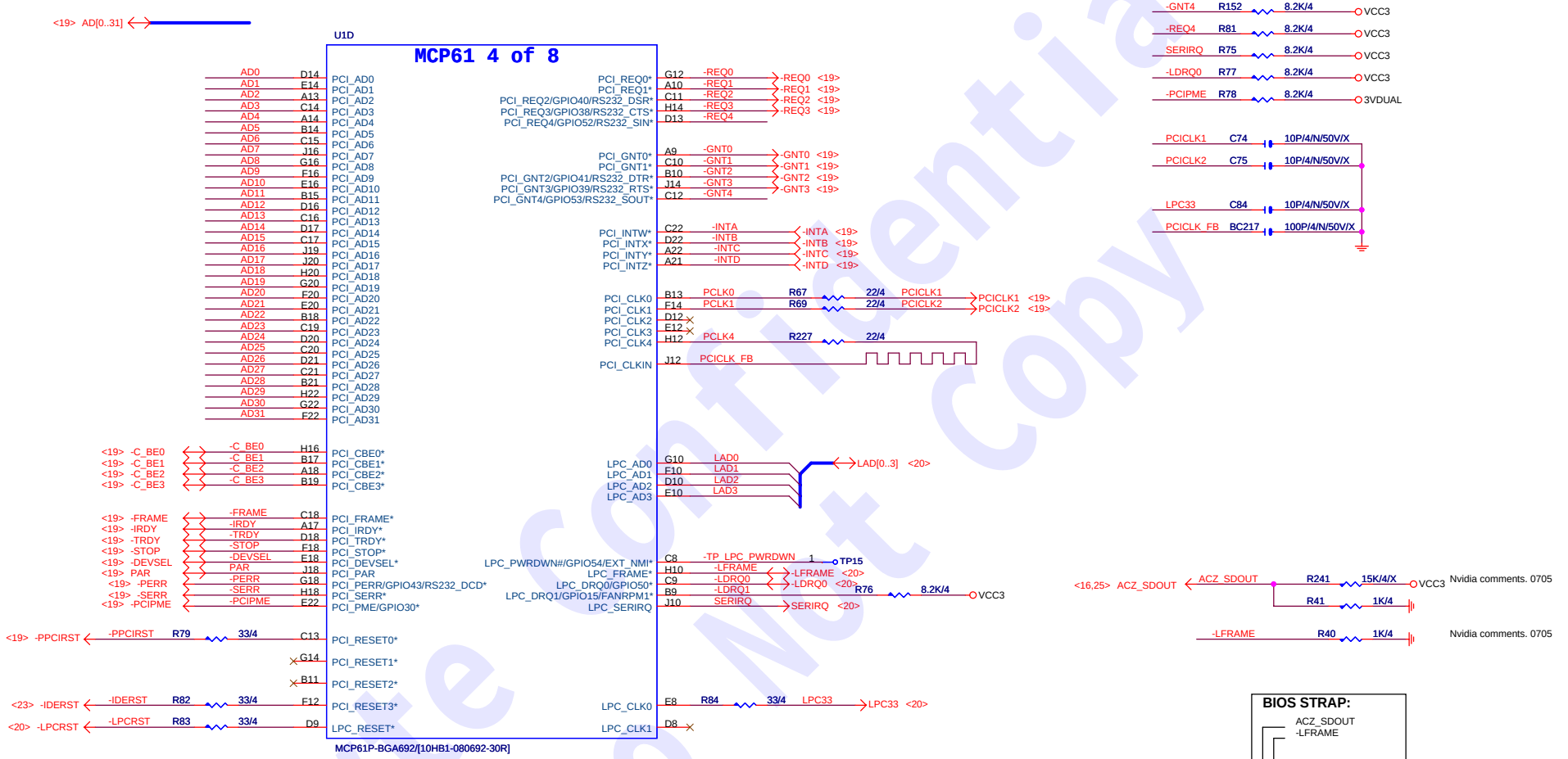

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Title: MCP61-PCI BUS

Size: Custom | Document Number: GA-M61PME-S2 | Rev: 2.02

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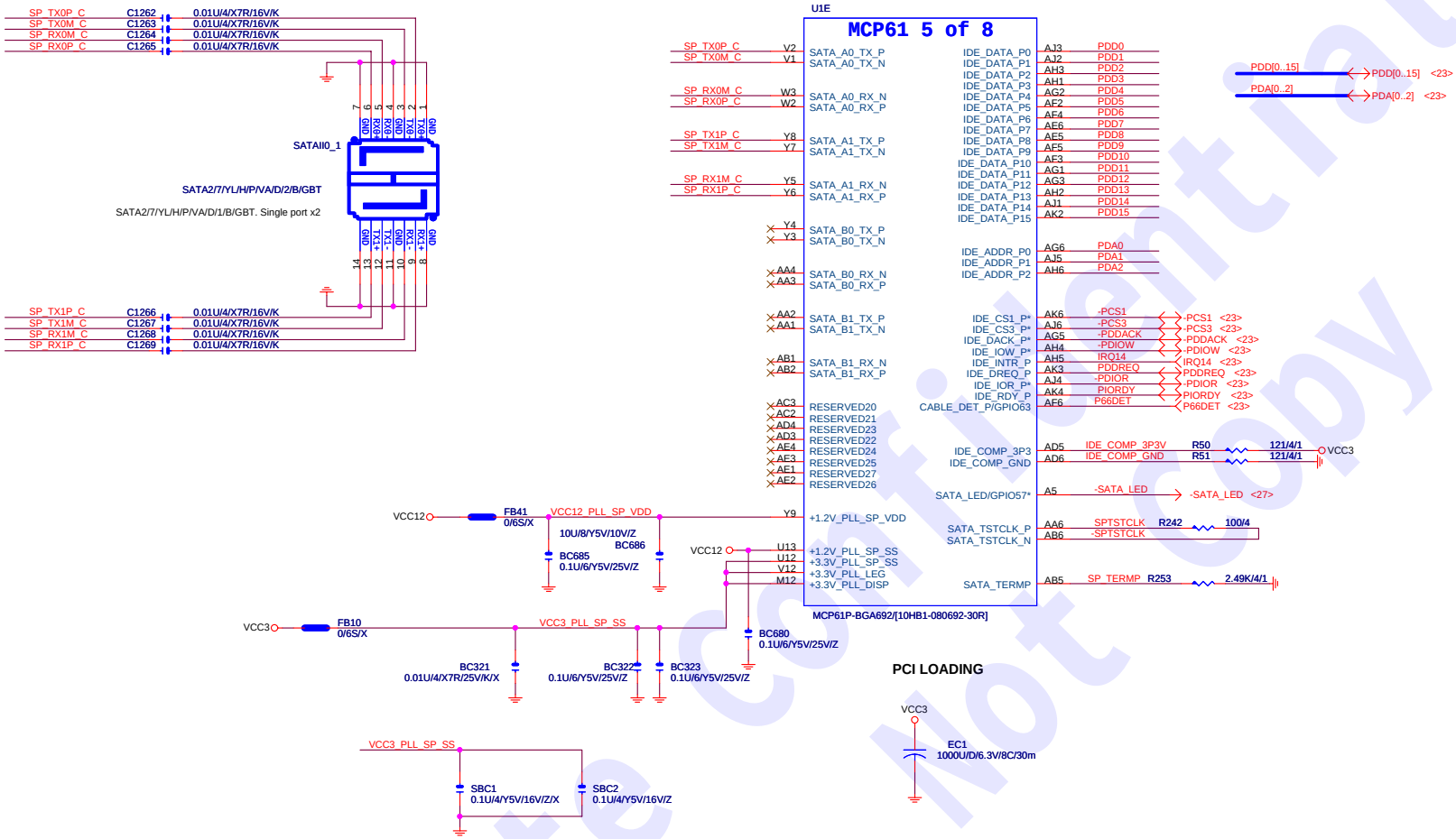

GIGABYTE		
Title	MCP61-SATA/IDE	
Size: Custom	Document Number: GA-M61PME-S2	Rev: 2.02
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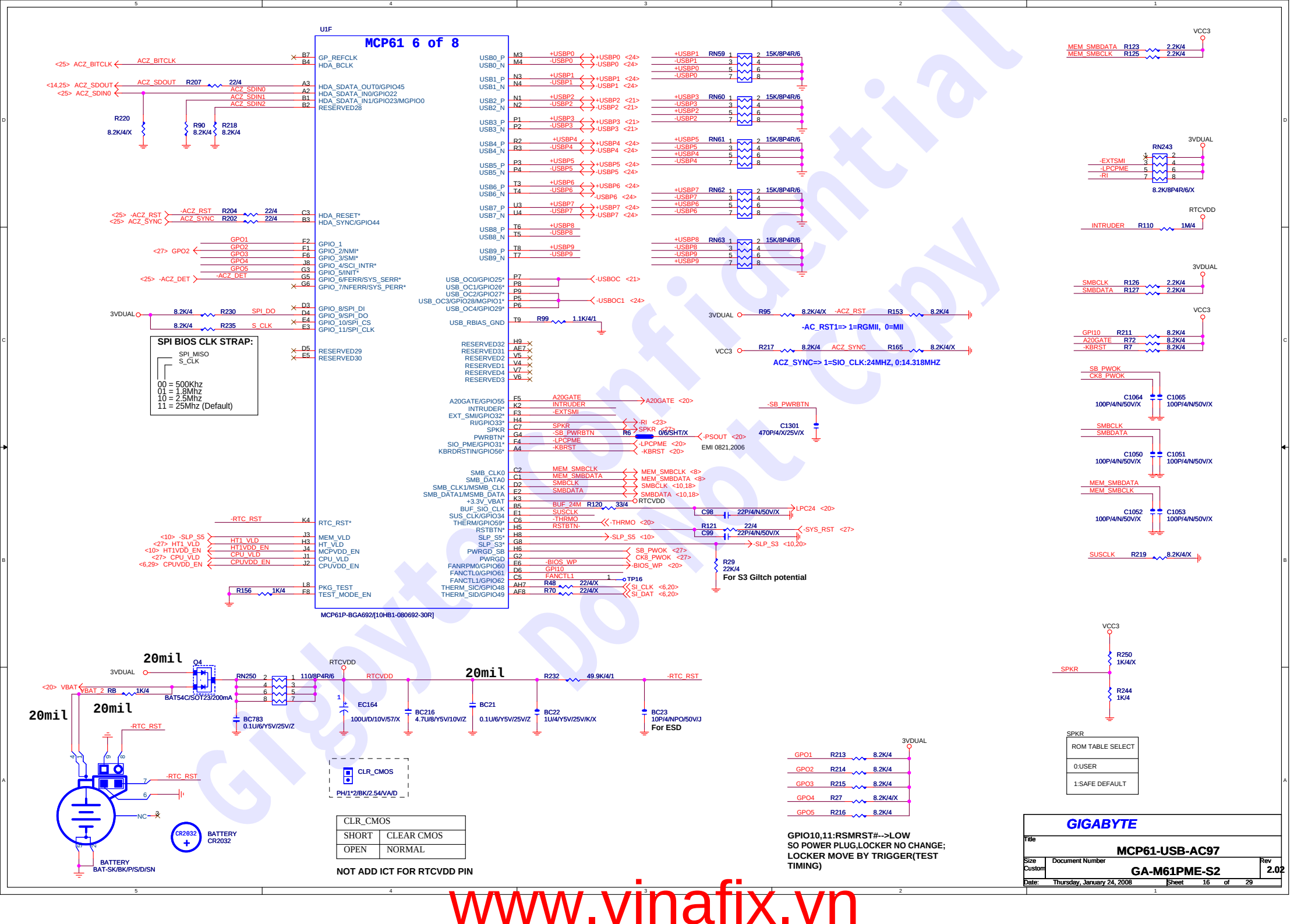
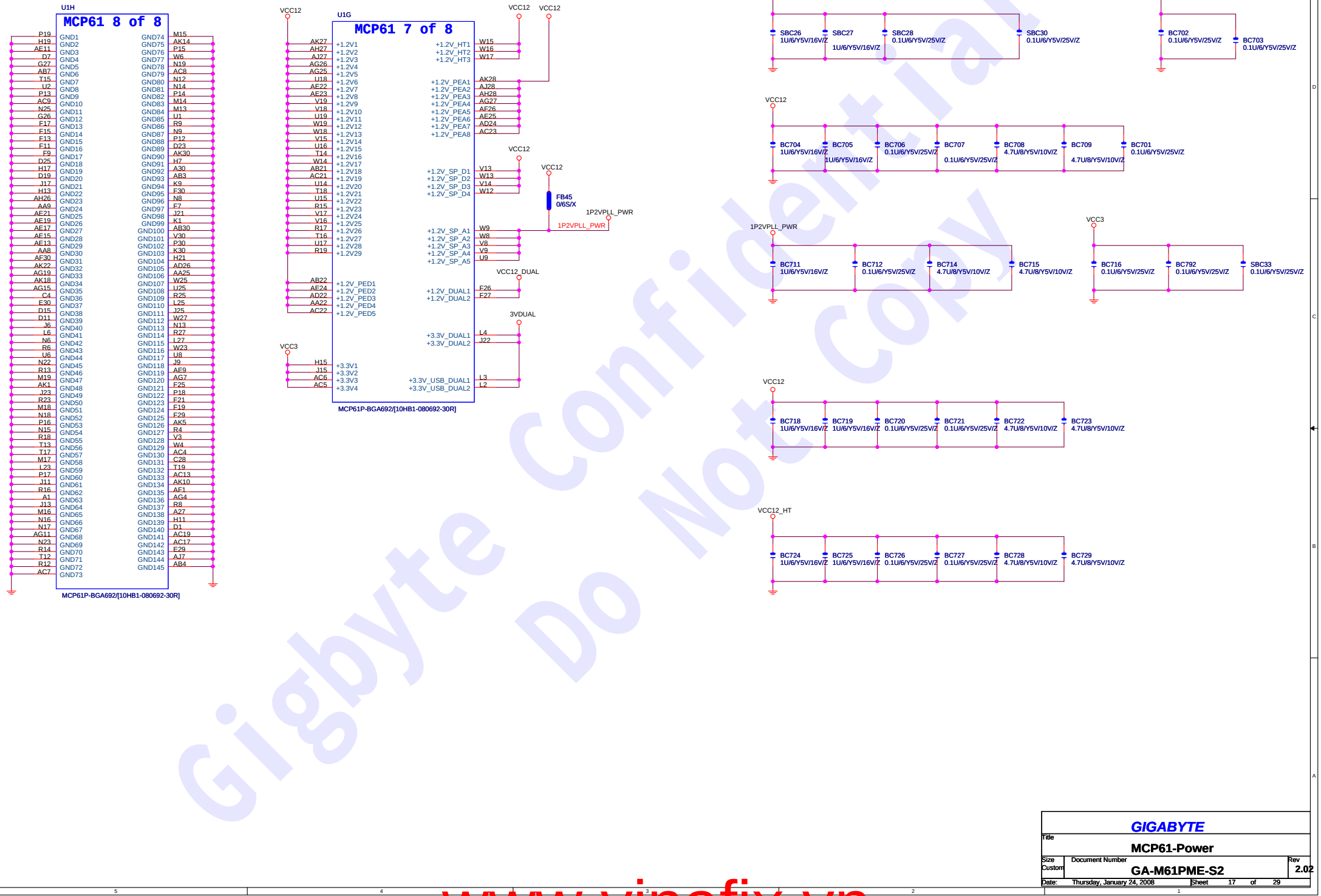


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

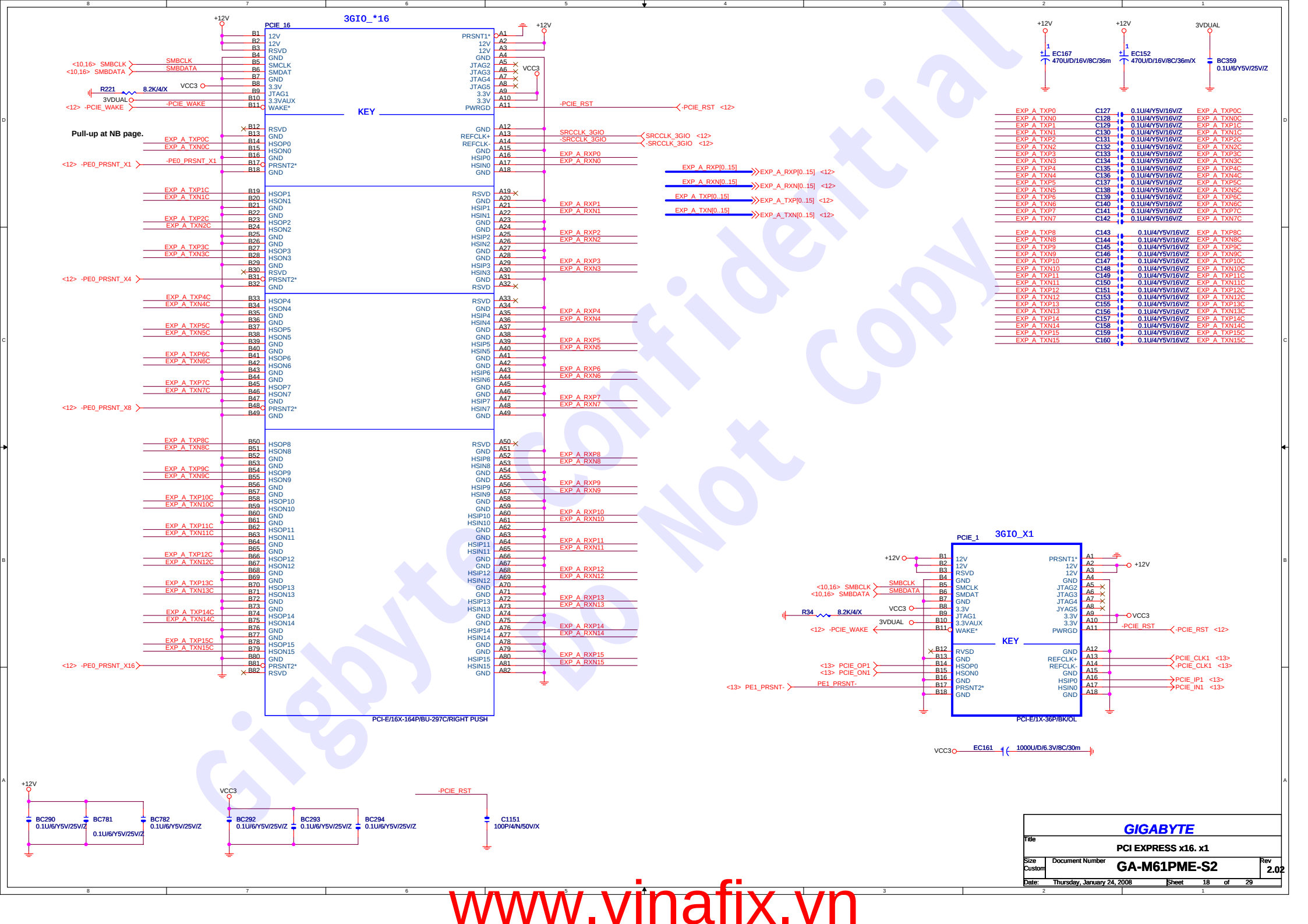


GIGABYTE

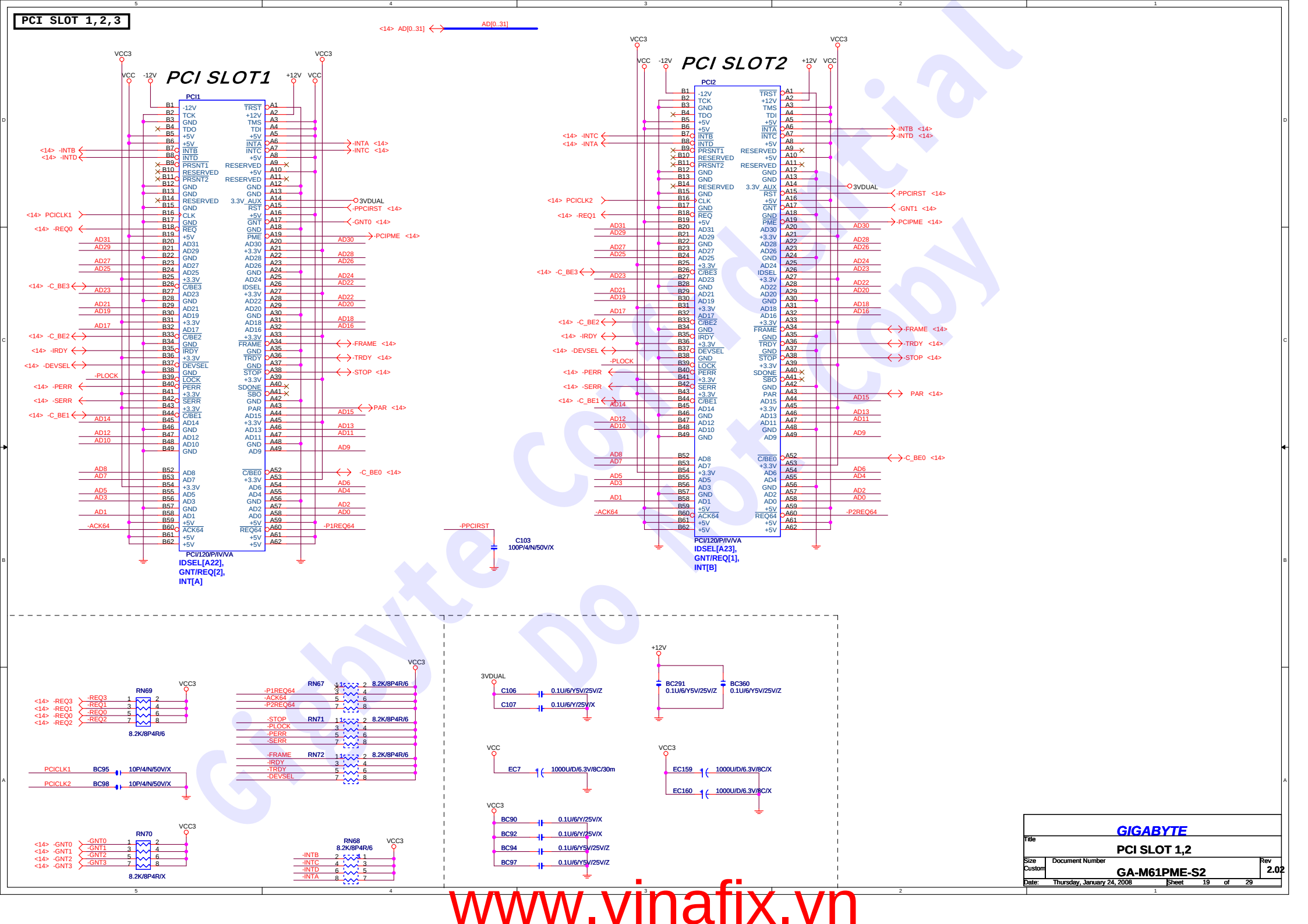
Title: MCP61-Power

Size: Custom | Document Number: GA-M61PME-S2 | Rev: 2.02

Date: Thursday, January 24, 2008 | Sheet 17 of 29



PCI SLOT 1,2,3



GIGABYTE		
Title	PCI SLOT 1,2	
Size: Custom	Document Number: GA-M61PME-S2	Rev: 2.02
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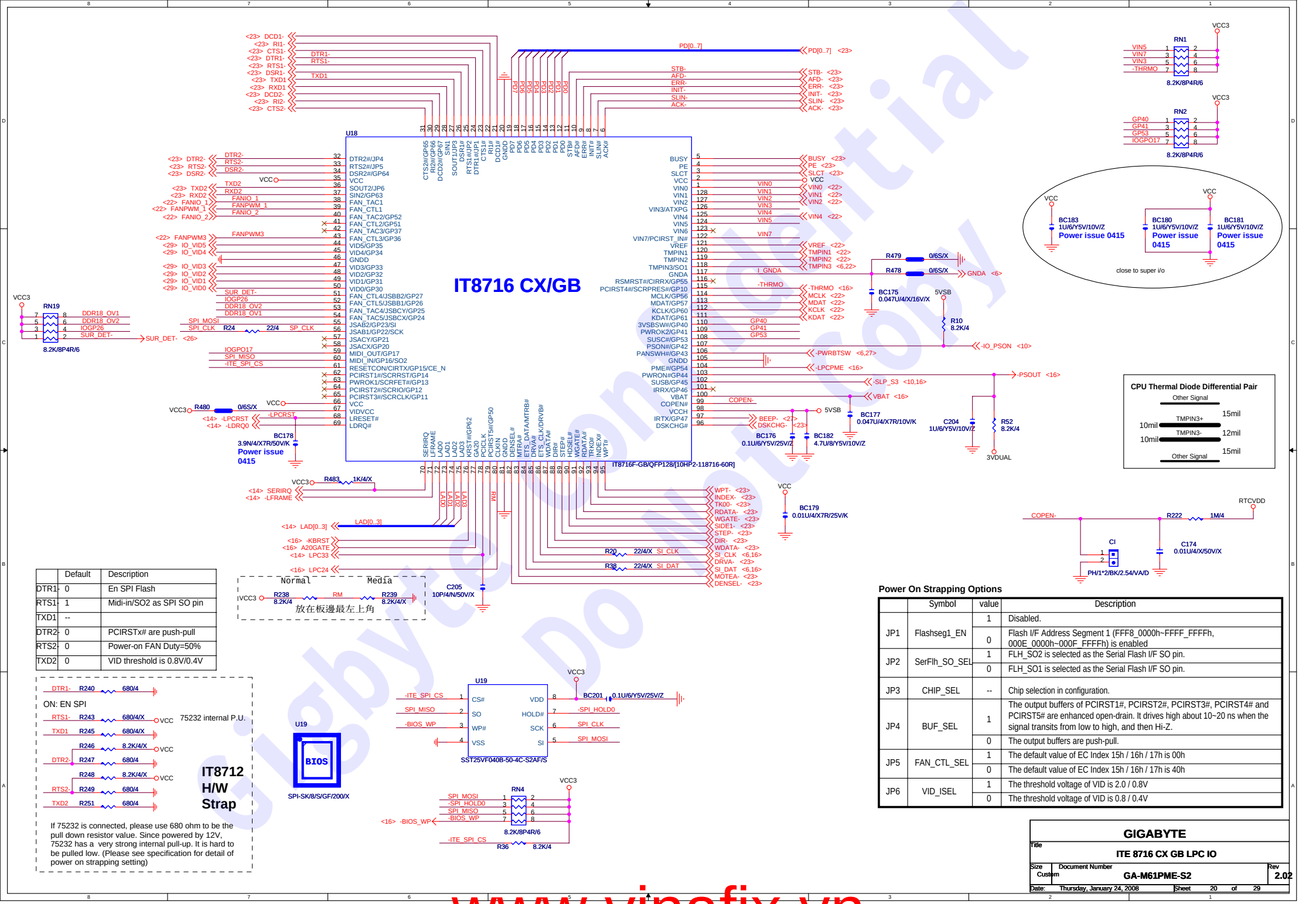

	Default	Description
DTR1-	0	En SPI Flash
RTS1-	1	Midi-in/SO2 as SPI SO pin
TXD1	--	
DTR2-	0	PCIRSTx# are push-pull
RTS2-	0	Power-on FAN Duty=50%
TXD2	0	VID threshold is 0.8V/0.4V

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

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Title: ITE 8716 CX GB LPC IO

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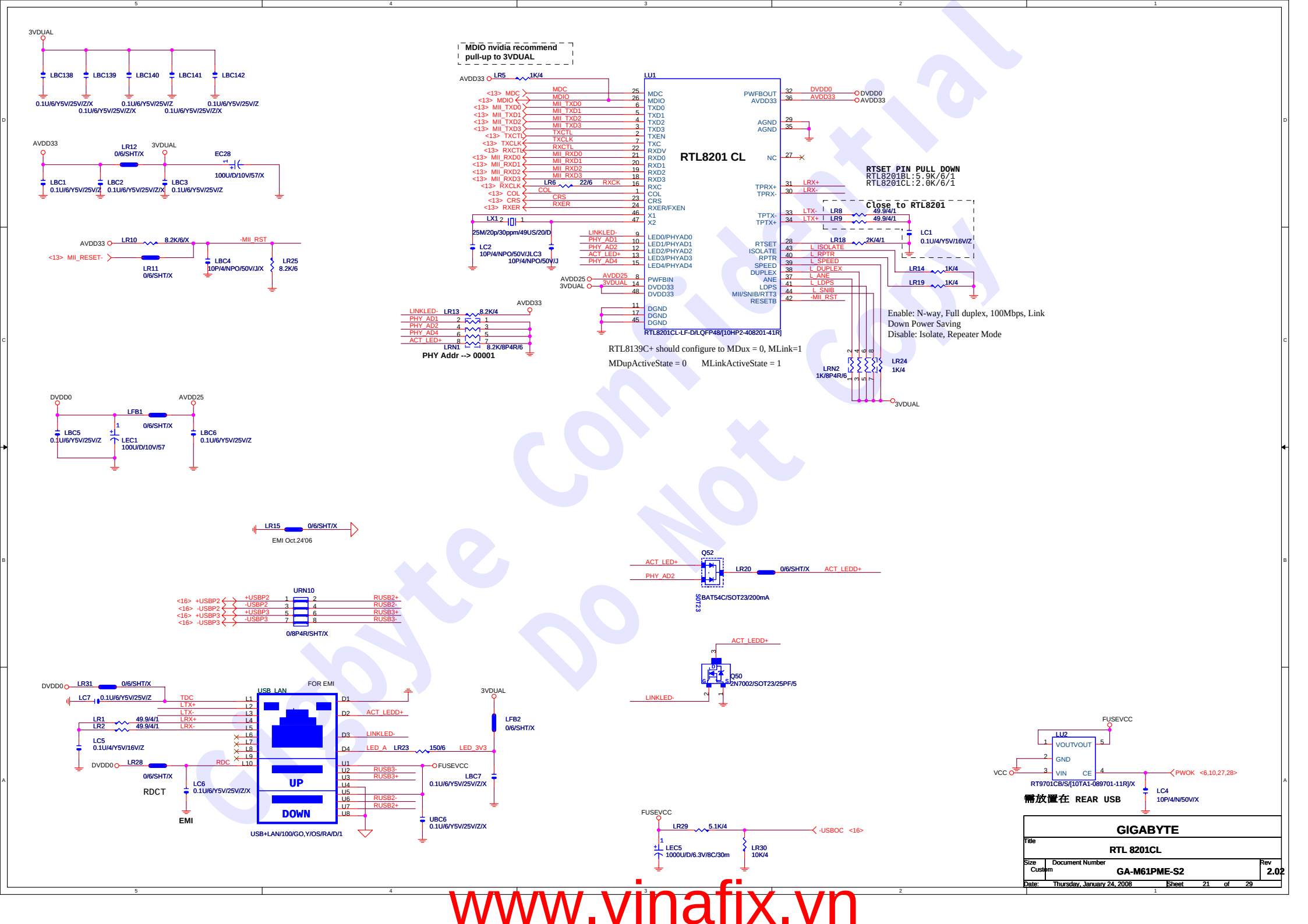
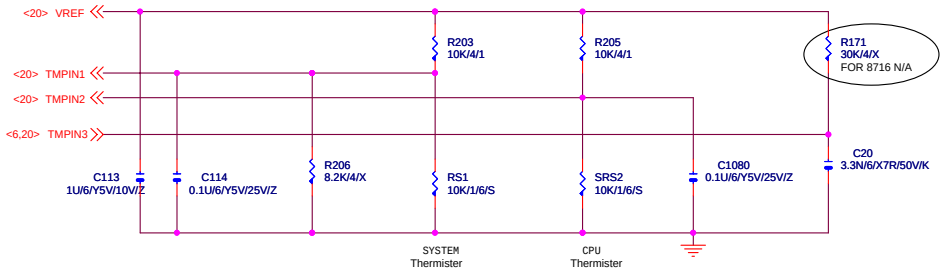
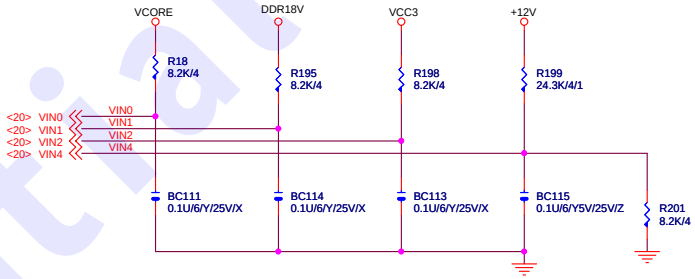
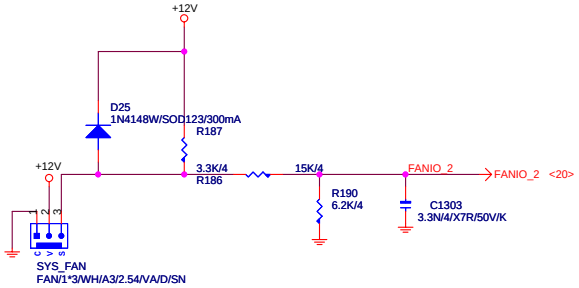


Hardware Monitor circuits

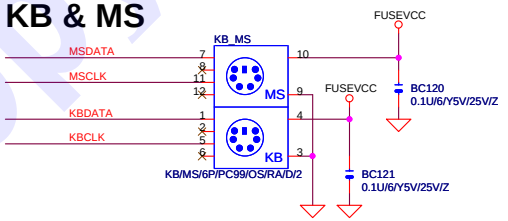


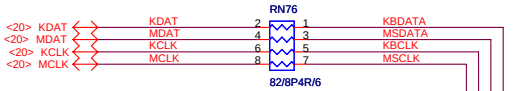


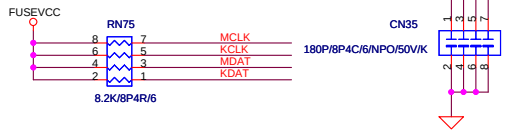
SYSTEM FAN



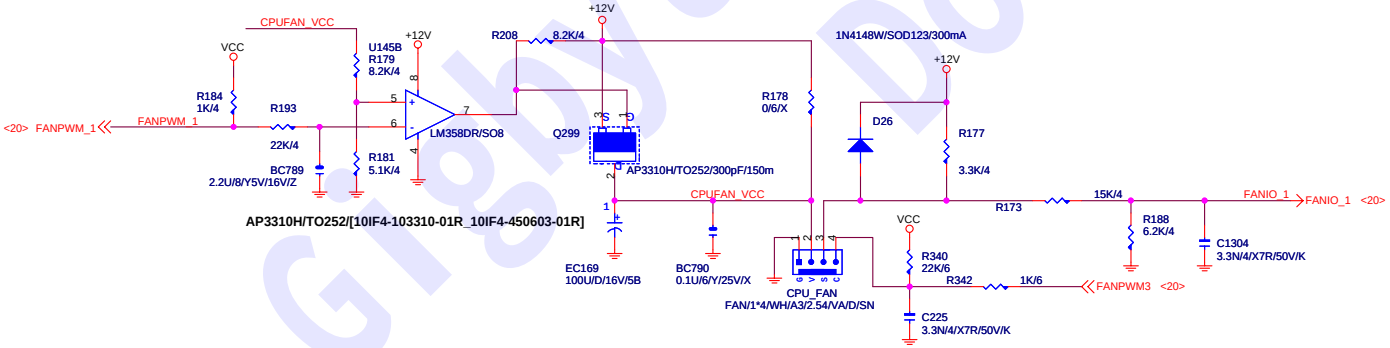
KB & MS







CPU FAN



GIGABYTE		
Title: FAN/HWMO KB/MS		
Size: Custom	Document Number: GA-M61PME-S2	Rev: 2.02
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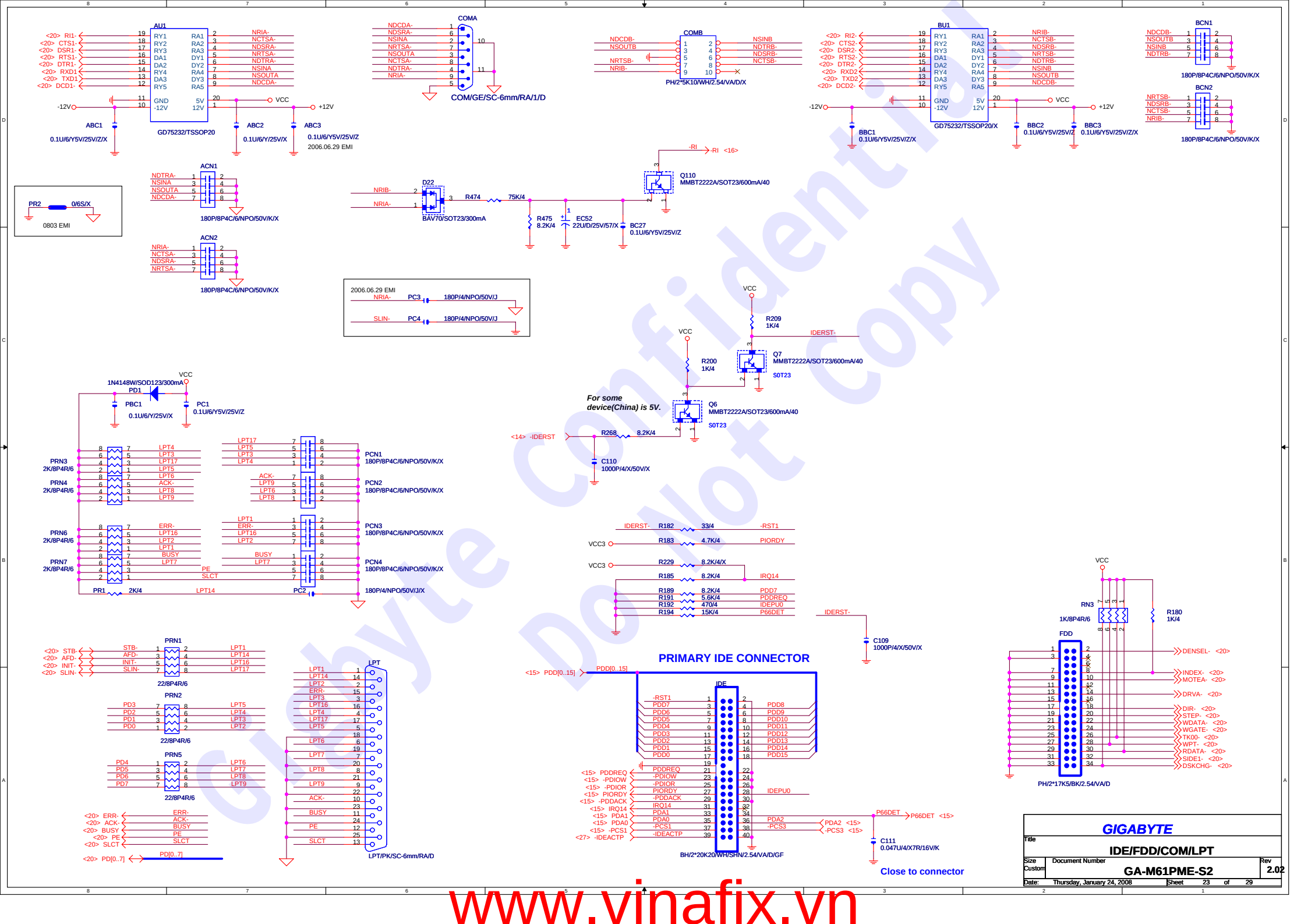
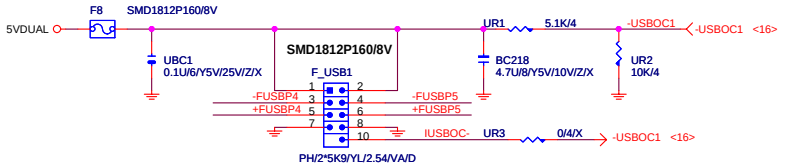
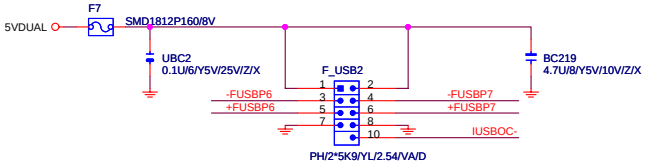


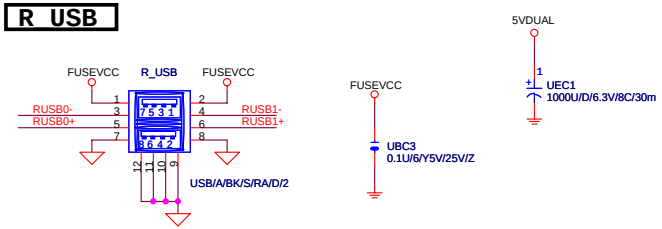
F_USB1

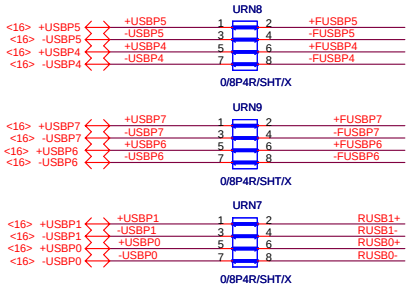


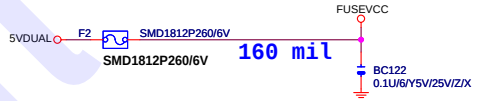
F_USB2

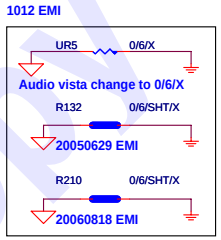


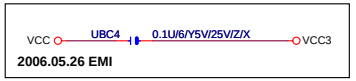
R_USB











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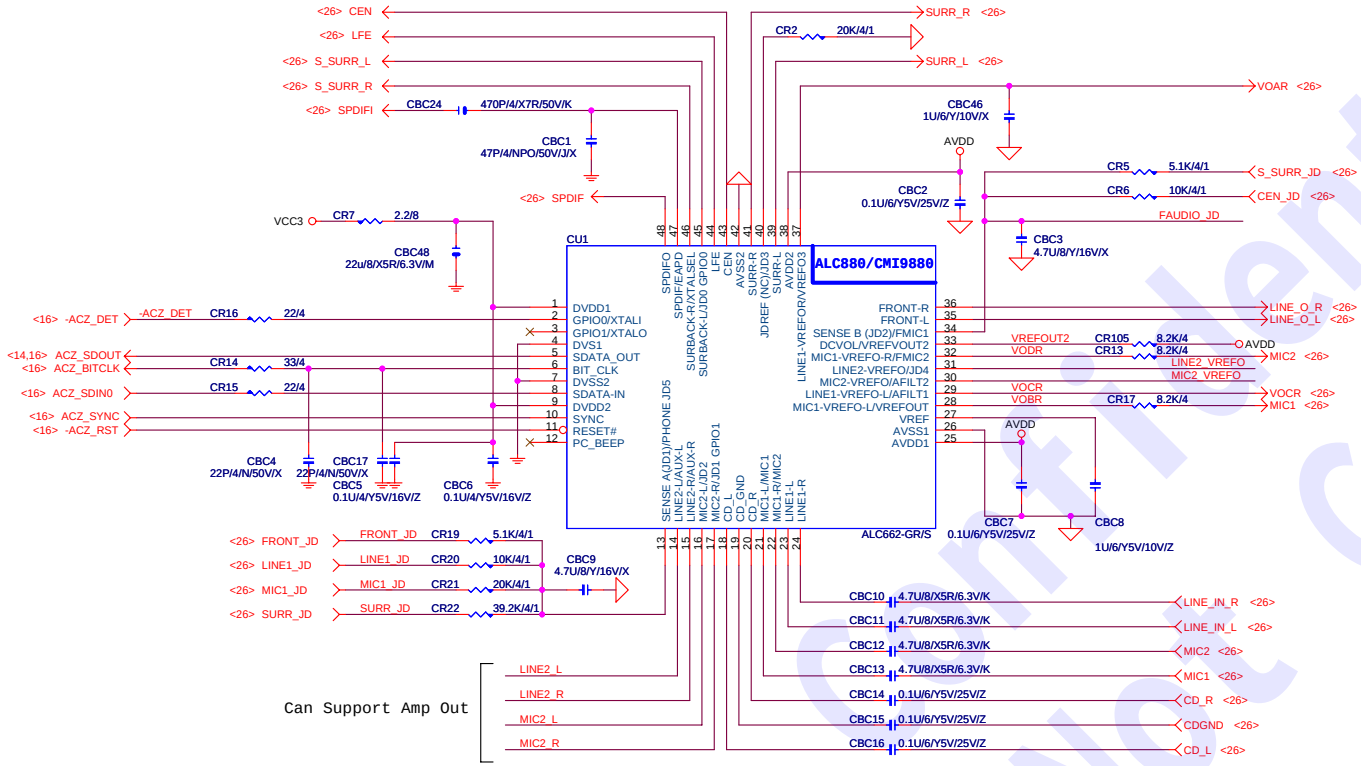
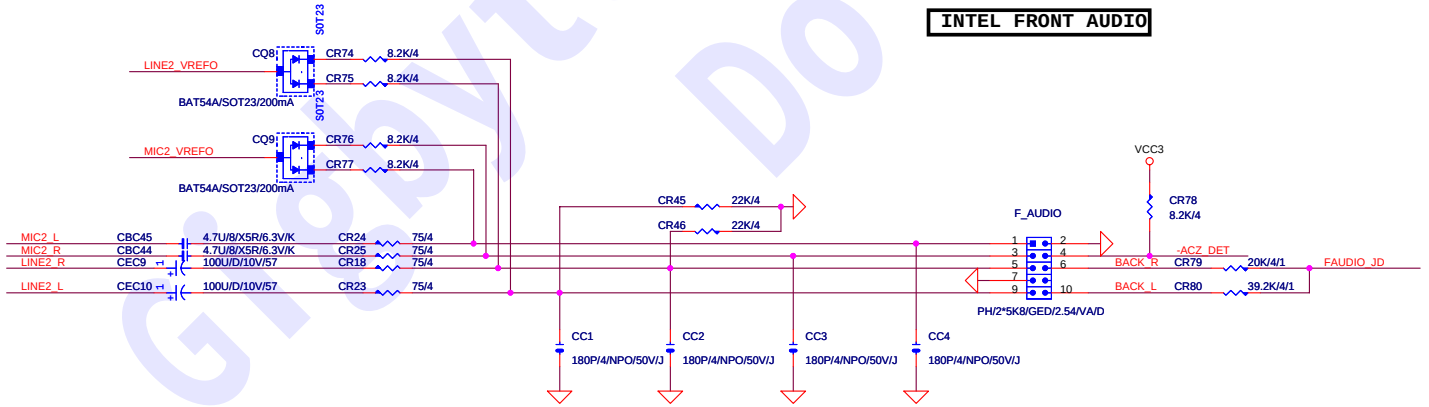


INTEL FRONT AUDIO



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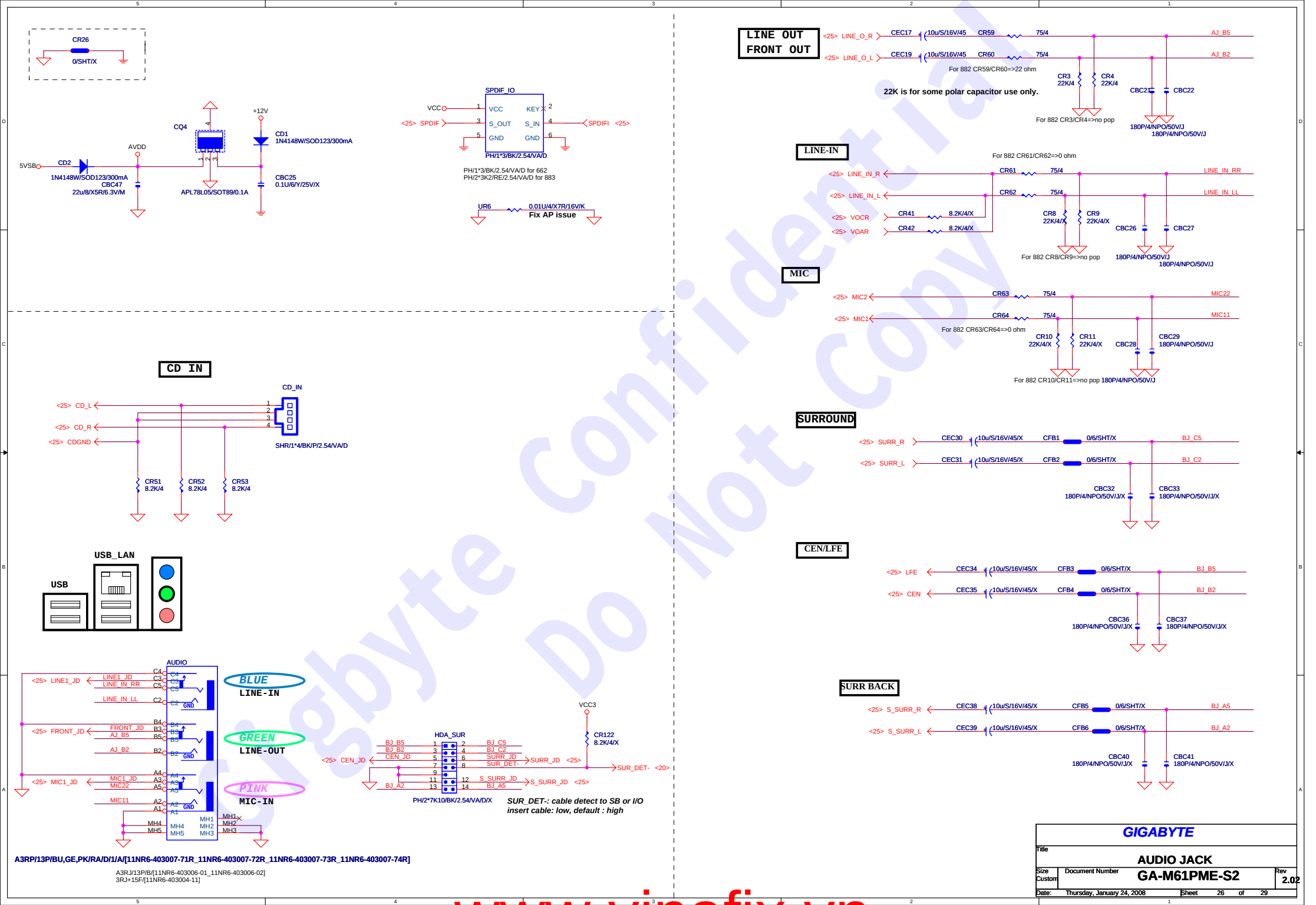

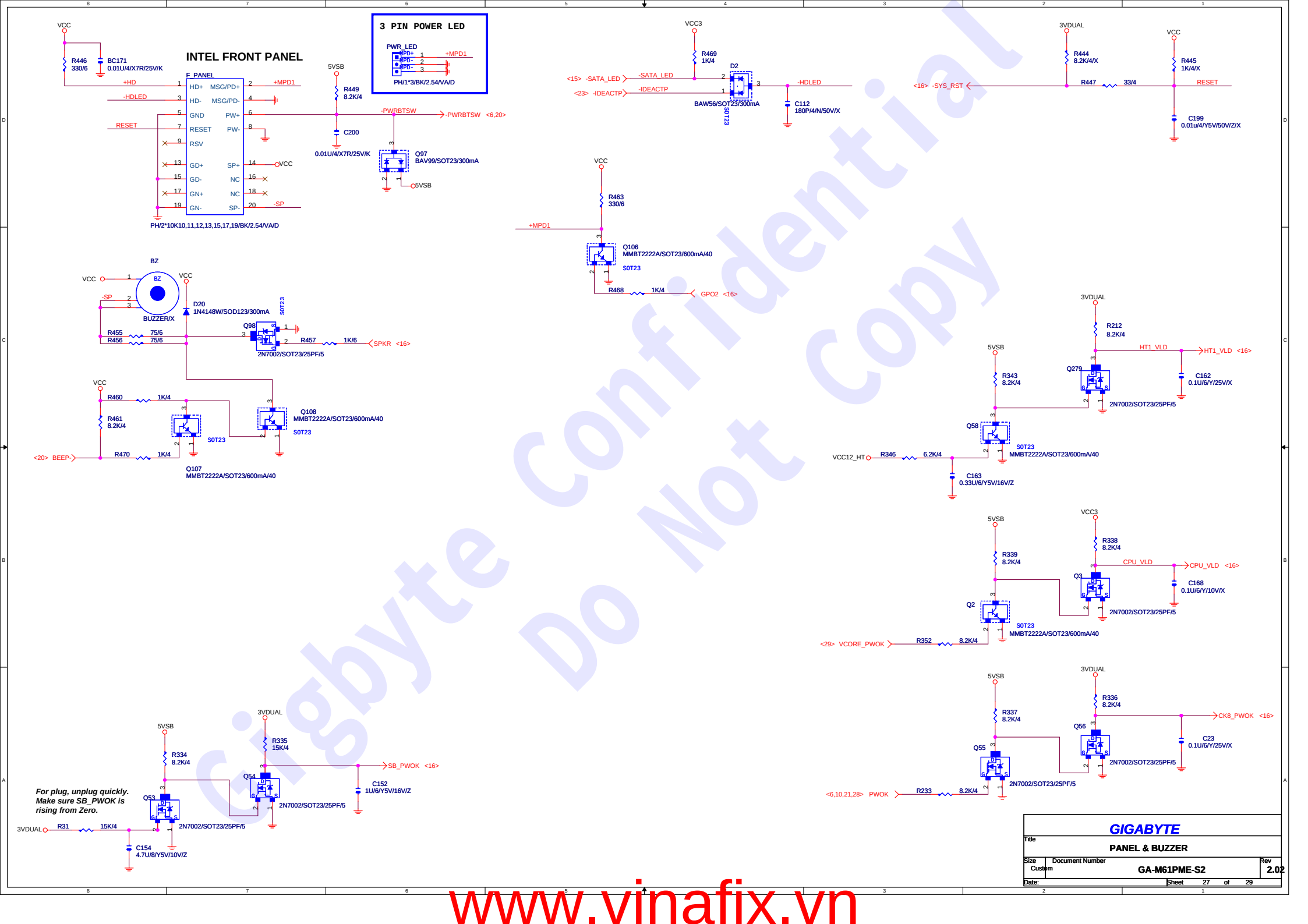
INTEL FRONT PANEL
F_PANEL
PH/2*10K10,11,12,13,15,17,19/BK/2.54/VA/D
3 PIN POWER LED
PWR_LED
PH/1*3/BK/2.54/VA/D
BUZZER/X
2N7002/SOT23/25PF/5
MMBT2222A/SOT23/600mA/40
BAW56/SOT23/300mA
BAV99/SOT23/300mA
For plug, unplug quickly. Make sure SB_PWOK is rising from Zero.
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PANEL & BUZZER
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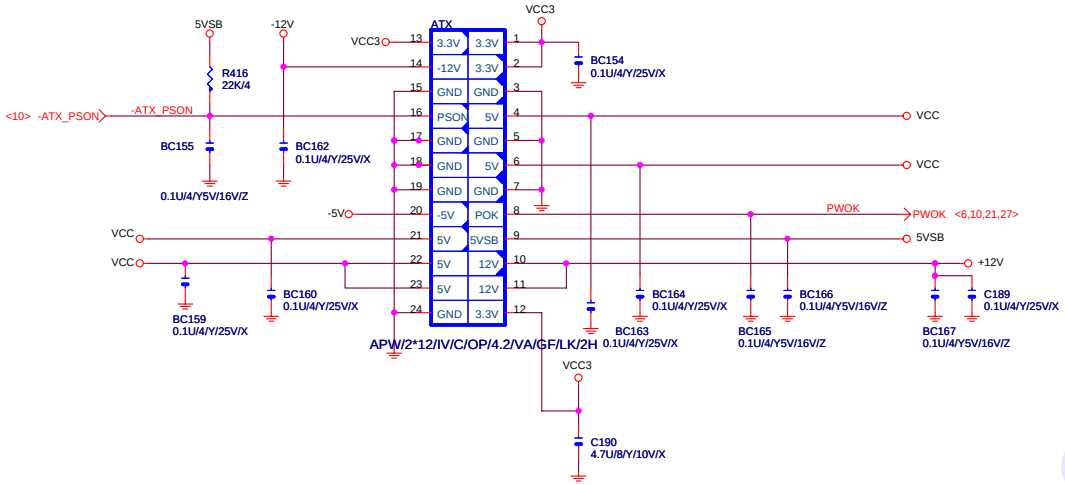

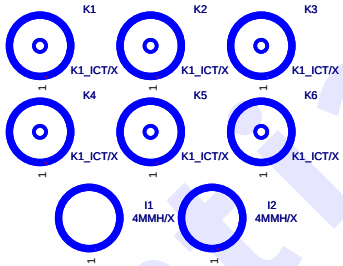

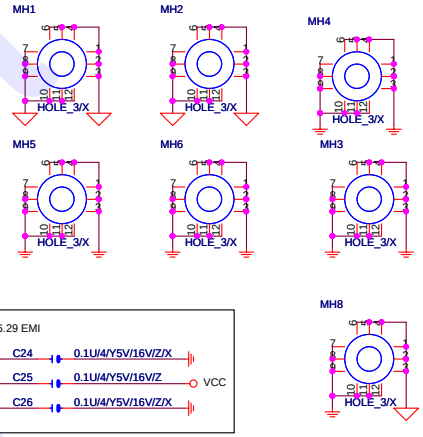

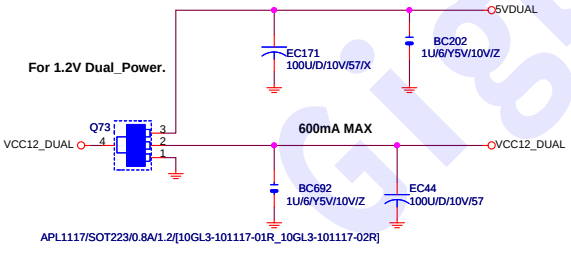

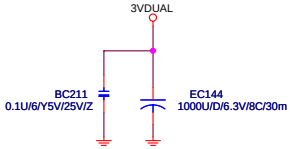

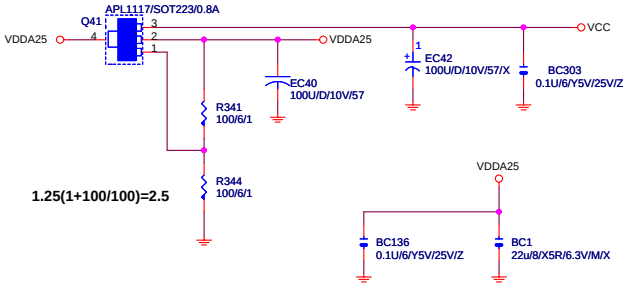

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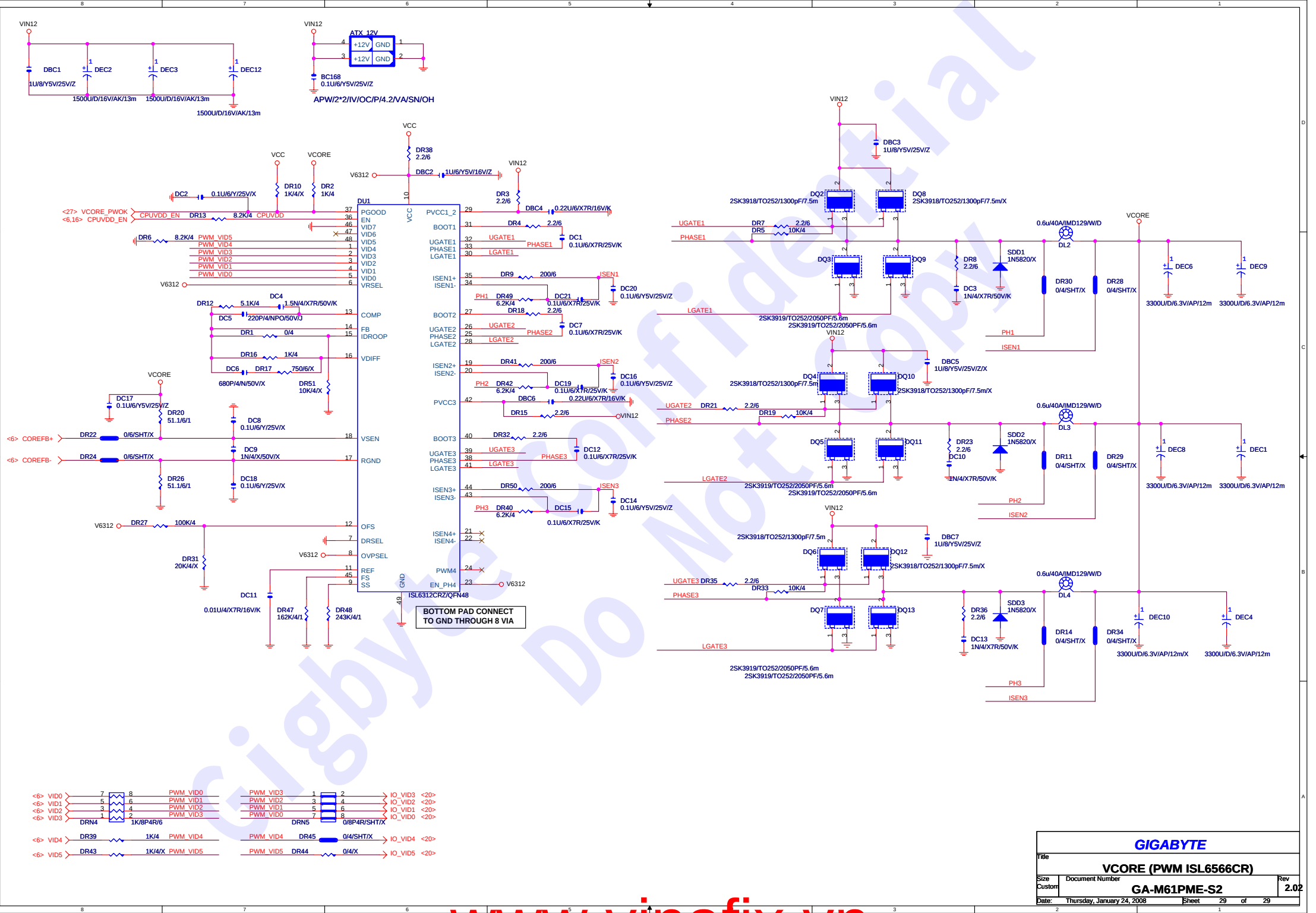

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