Table of Contents

CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

<Core Design>

Title:	Table of Contents	
Engineer:	*Surface*	
Size: A3	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 1 of 76	

Schematics Change History

Rev.	Date	Comments
0p9	28 Oct 2014	1. Starting with G_EV1_1021-1630.DSN 2. Added SL schematic from page 72 ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 3. Added External USB3 schematic from ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 4. Added external DP ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 5. Added IR_CAMERA from Front Camera...put in page 49 6. Removed page 73 PCIe GPU 7. Added Blade from T 8. Removed P72 T2B Pwr Transistors
0p10	3 Nov 2014	1. Changing to NVDC 2. Replaced GTX with GT, kept bypass caps 3. Replaced Charger with BQ24770
0p11	3 Nov 2014	1. Replace SKL-U with SKL-Y
0p12	11 Nov 2014	1. Model DDR connection from Intel SDS
0p13	18 Nov 2014	1. Added FUB information to all components 2. Changed Decretes.. sizing caps
0p14	20 Nov 2014	1. Added +5VA_SHA 2. Added T Cost Down/XCN's 3. Added SL +5V load Switch & Caps 4. Added Blade +5V load Switch & Caps
0p15	26 Nov 2014	1. Removed Boost 2. Re-adjusted usb ports on CPU 3. Removed Audio DSP
0p16	03 Dec 2014	1. changed +1VSB regulator 2. changed IR Camera/added diode 3. added power numbers from 0.91 PDG, Oct14 4. changed BLADE connector 5. cpu decoupling caps changed 6. changed +5V/+3V inductors (place holder)
0p17	05 Dec 2014	1. swapped M_A_CAA with MA_CAB on U1601/U1602 2. added two SAR chips, P32 3. remove tp's from csi lines on (p23) 4. change from 10 ceramic to 3 tantalum-poly on usb3 typeA (p45) 5. remove the RSENSE from output of +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) 6. change RSENSE input to 0402 from 0603 for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) input regulator 7. change inductor for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58) to HMLE20161B-1R0MDR-01 8. change RSENSE input to 0402 from 0603 for +5V_TS,+5V_SDXC,+5V_AUDIO,+5V, +5V_FAN(p64) 9. change RSENSE input to 0402 from 0603 for +3P3V_PANEL,+3P3V,+3P3V_SENSOR,+1P8V_DMIC (p65) 10. Replacing the SL connector with X908351-001 11. Replace PL5901 and PL5902 with CMLE042T-2R2MS-01 12. Replace 0402 1uf 6.3V with 0201 1uF 6.3V X5R 13. Replace L7201 with TOKO #A919CY-100M 14. Added VSYS -> BLADE FANG supply (p73)
0p18	09 Dec 2014	1. Reduced sizes of parts for Cameras (Resistors/Caps/Regulators)
0p19	12 Dec 2014	1. All 47uF caps become 0805/1mmZ 2. All 10uF caps become 0402...4V/6.3V
0p20	15 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x4 2. Shui Changes 3. more Shui Changes
0p21	16 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x5 2. changes from EV_schematic_issue_check_1216_JDM1.xlsx 3. changed name of +6_12 to +V_ALWAYS_ON 4. Removed 2 Mikes & Front Mike & added FPC conn 5. Added 2nd BLADE connector
0p22	17 Dec 2014	1. Replaced SD connector with AY531465T 2. changes from EV_schematic_issue_check_viola_1217_JDM1.xlsx
0p23 - current		1. See apexUfixes_revXpXX.xlsx

CAD Note:

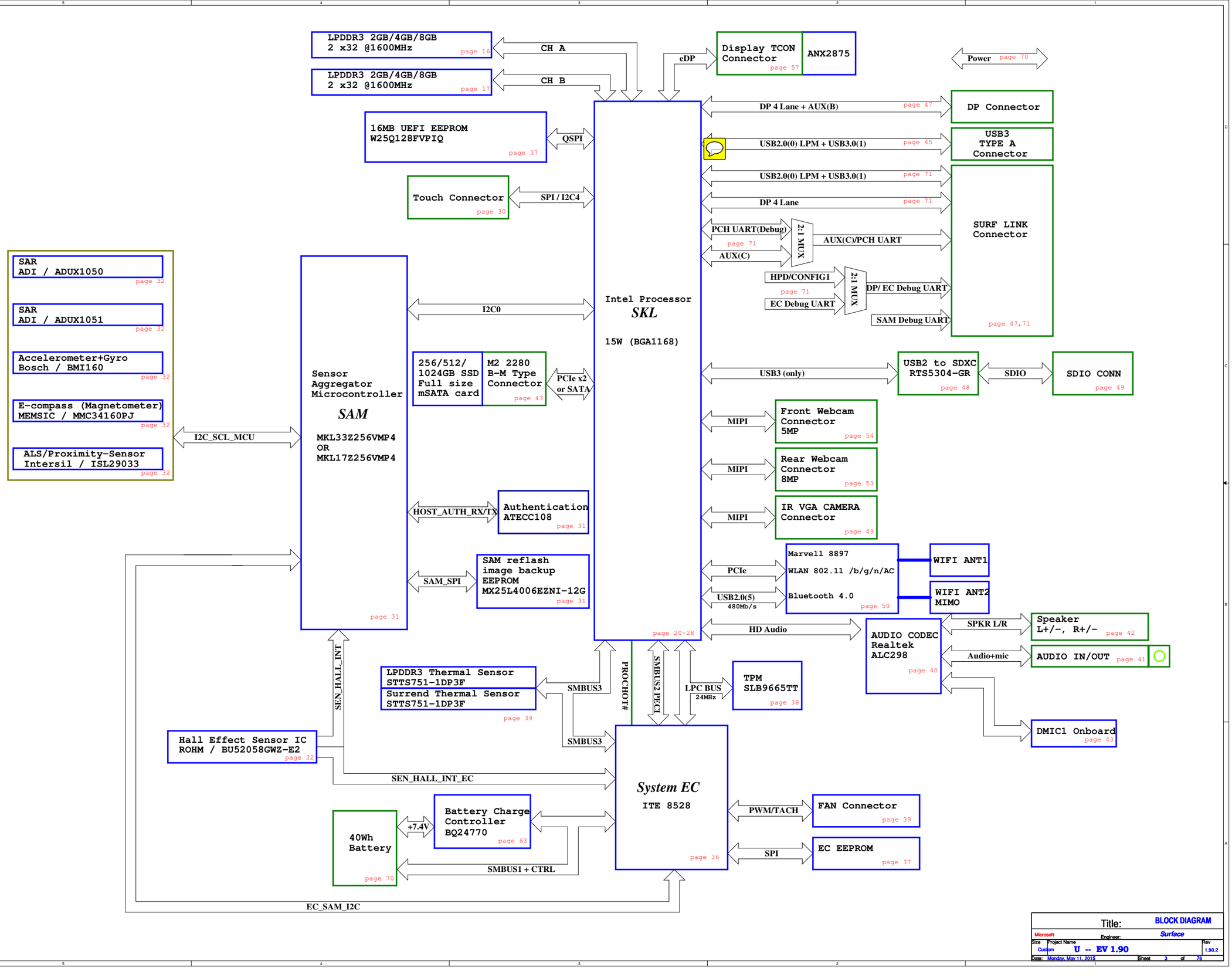
Default component footprint is SMD 0201, X5R, 1% resistors

S = Short after design fixed

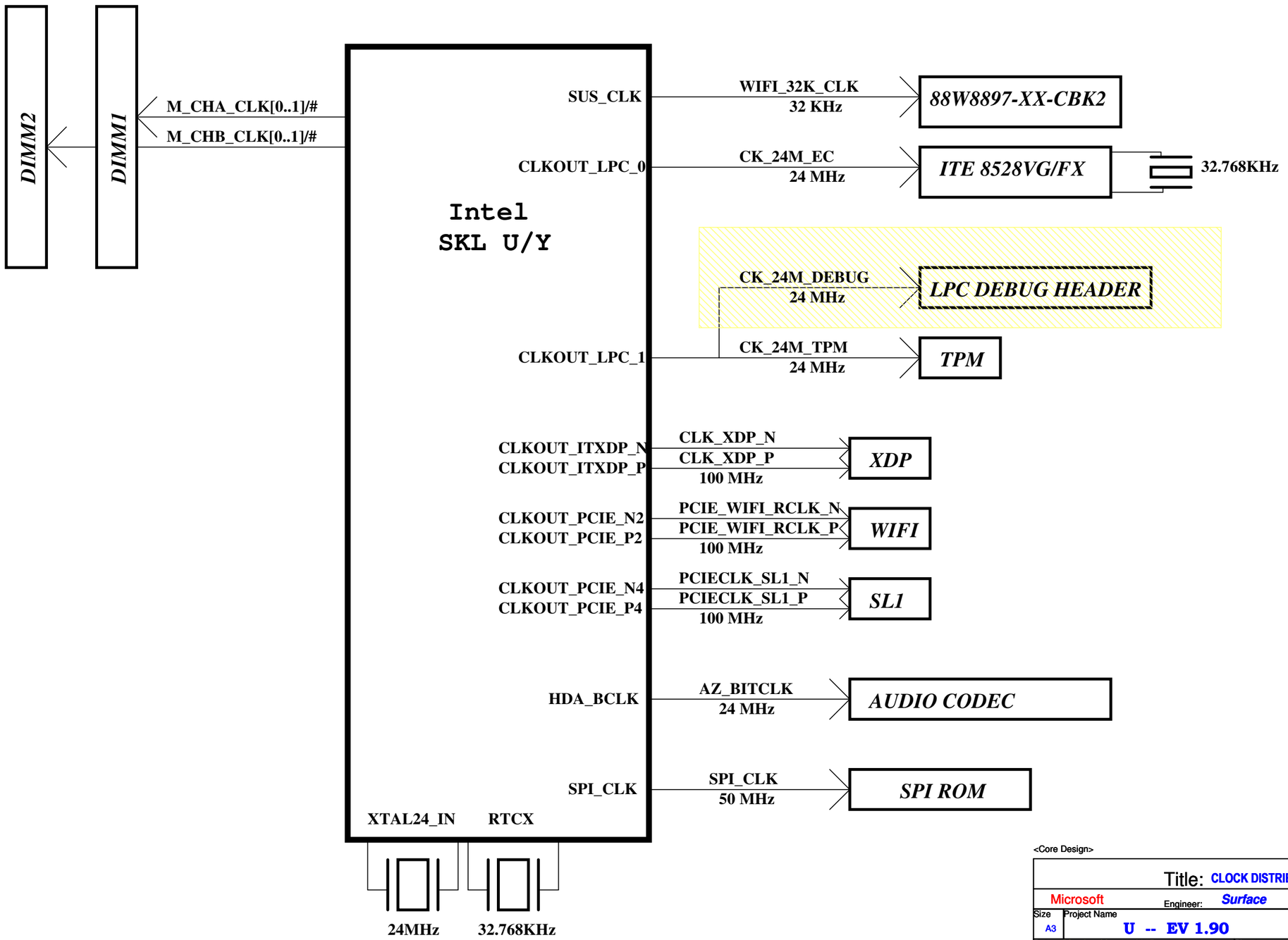
Property: BUILD-OPT

DNP = Not Installed Part.

Title:	CHANGE HISTORY-1		
Engineer:	*Surface*		
Size: A3	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 2 of 76	


LPDDR3 2GB/4GB/8GB
2 x32 @1600MHz
page 16
CH A
LPDDR3 2GB/4GB/8GB
2 x32 @1600MHz
page 17
CH B
eDP
Display TCON Connector
page 57
ANX2875
Power
page 70
16MB UEFI EEPROM
W25Q128FVPIQ
page 37
QSPI
DP 4 Lane + AUX(B)
page 47
DP Connector
USB2.0(0) LPM + USB3.0(1)
page 45
USB3 TYPE A Connector
Touch Connector
page 30
SPI / I2C4
USB2.0(0) LPM + USB3.0(1)
page 71
DP 4 Lane
page 71
SURF LINK Connector
page 47,71
PCH UART(Debug)
page 71
AUX(C)
2:1 MUX
AUX(C)/PCH UART
HPD/CONFIG1
page 71
EC Debug UART
2:1 MUX
DP/ EC Debug UART
SAM Debug UART
SAR
ADI / ADUX1050
page 32
SAR
ADI / ADUX1051
page 32
Accelerometer+Gyro
Bosch / BMI160
page 32
E-compass (Magnetometer)
MEMSIC / MMC34160PJ
page 32
ALS/Proximity-Sensor
Intersil / ISL29033
page 32
I2C_SCL_MCU
Sensor Aggregator Microcontroller
SAM
MKL33Z256VMP4
OR
MKL17Z256VMP4
page 31
I2C0
Intel Processor
SKL
15W (BGA1168)
page 20~28
256/512/ 1024GB SSD Full size mSATA card
M2 2280 B-M Type Connector
page 43
PCIe x2 or SATA
USB3 (only)
USB2 to SDXC RTS5304-GR
page 48
SDIO
SDIO CONN
page 49
MIPI
Front Webcam Connector 5MP
page 54
MIPI
Rear Webcam Connector 8MP
page 53
MIPI
IR VGA CAMERA Connector
page 49
HOST_AUTH_RX/TX
Authentication ATECC108
page 31
SAM_SPI
SAM reflash image backup EEPROM MX25L4006EZNI-12G
page 31
Marvell 8897
WLAN 802.11 /b/g/n/AC
Bluetooth 4.0
page 50
PCIe
USB2.0(5)
480Mb/s
WIFI ANT1
WIFI ANT2 MIMO
HD Audio
AUDIO CODEC Realtek ALC298
page 40
SPKR L/R
Speaker L+/-, R+/-
page 42
Audio+mic
AUDIO IN/OUT
page 41
SEN_HALL_INT
LPDDR3 Thermal Sensor
STTS751-1DP3F
Surrend Thermal Sensor
STTS751-1DP3F
page 39
SMBUS3
PROCHOT#
SMBUS2 PECI
LPC BUS
24MHz
TPM
SLB9665TT
page 38
DMIC1 Onboard
page 43
Hall Effect Sensor IC
ROHM / BU52058GWZ-E2
page 32
SEN_HALL_INT_EC
System EC
ITE 8528
page 36
PWM/TACH
FAN Connector
page 39
SPI
EC EEPROM
page 37
40Wh Battery
page 70
+7.4V
Battery Charge Controller
BQ24770
page 63
SMBUS1 + CTRL
EC_SAM_I2C
Title:
BLOCK DIAGRAM
Microsoft
Engineer:
Surface
Size
Project Name
Rev
Custom
U -- EV 1.90
1.90.2
Date: Monday, May 11, 2015
Sheet 3 of 76

HSW Buffer Through Mode for Pre-Silicon



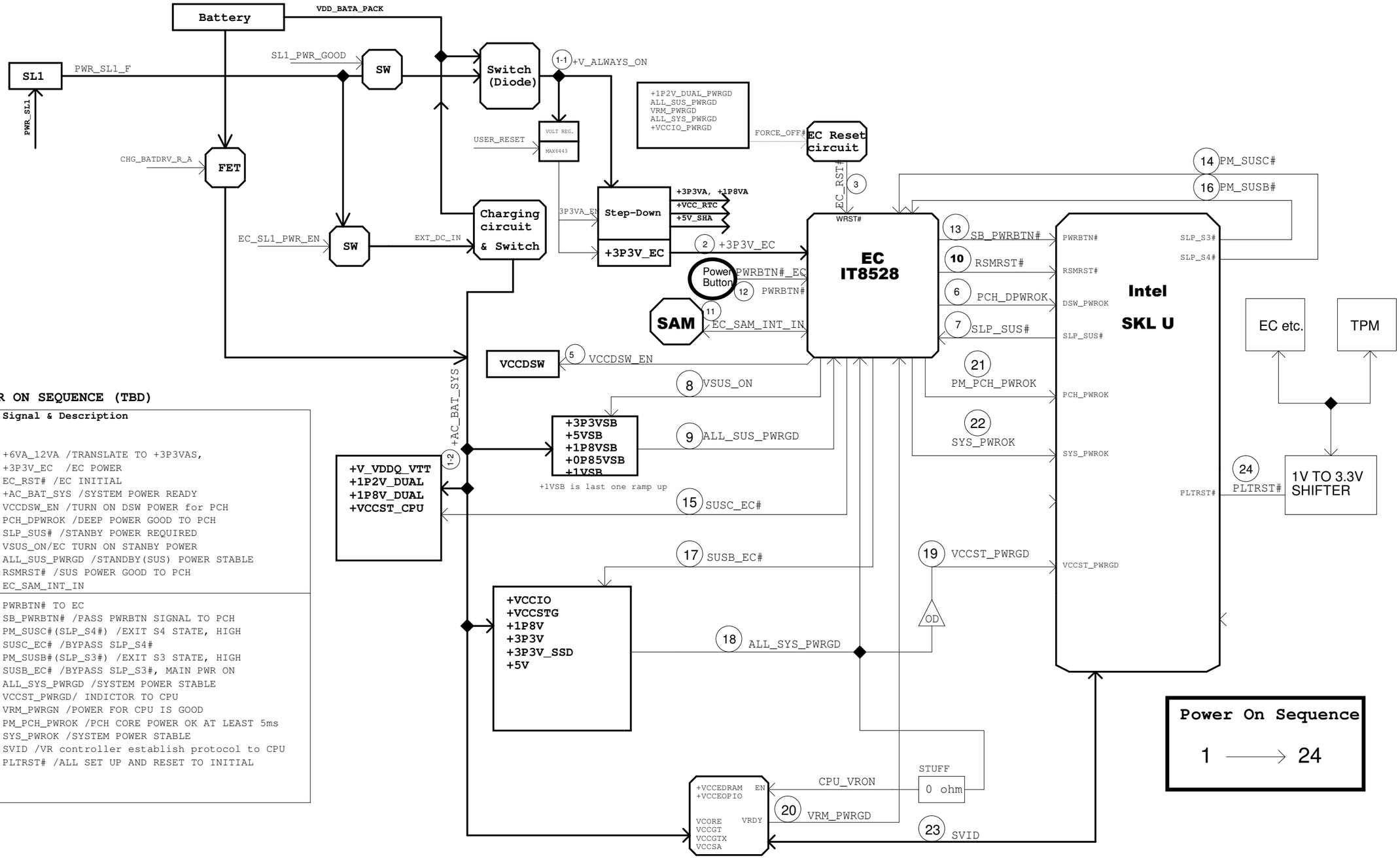
<Core Design>

Title: CLOCK DISTRIBUTION(TBD)

Microsoft Engineer: Surface

Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 4 of 76

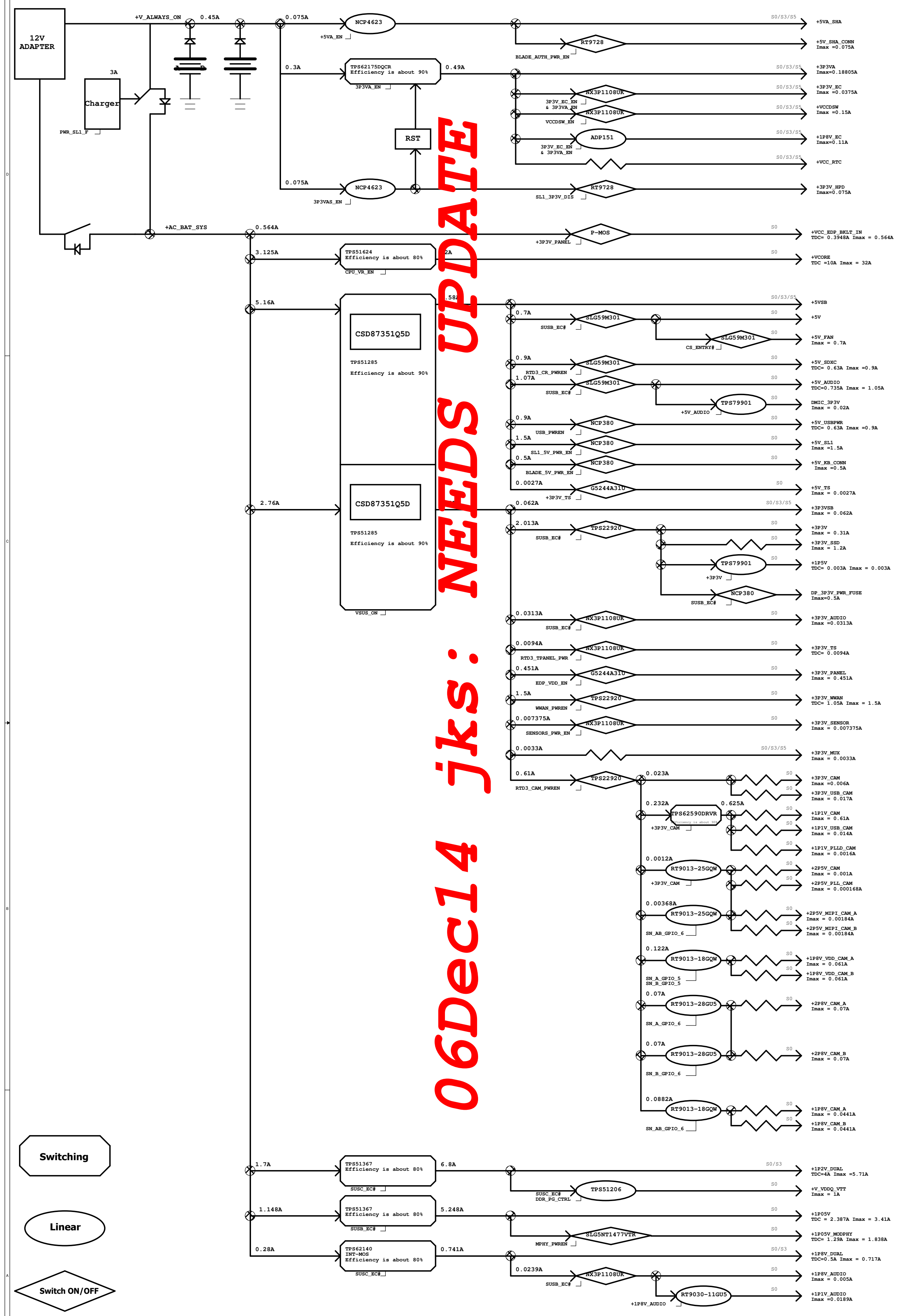


POWER ON SEQUENCE (TBD)

STEP	Signal & Description
1	+6VA_12VA /TRANSLATE TO +3P3VAS,
2	+3P3V_EC /EC POWER
3	EC_RST# /EC INITIAL
4.	+AC_BAT_SYS /SYSTEM POWER READY
5.	VCCDSW_EN /TURN ON DSW POWER for PCH
6.	PCH_DPWROK /DEEP POWER GOOD TO PCH
7.	SLP_SUS# /STANBY POWER REQUIRED
8.	VSUS_ON/EC TURN ON STANBY POWER
9.	ALL_SUS_PWRGD /STANDBY(SUS) POWER STABLE
10.	RSMRST# /SUS POWER GOOD TO PCH
11.	EC_SAM_INT_IN
12	PWRBTN# TO EC
13.	SB_PWRBTN# /PASS PWRBTN SIGNAL TO PCH
14.	PM_SUSC#(SLP_S4#) /EXIT S4 STATE, HIGH
15.	SUSC_EC# /BYPASS SLP_S4#
16.	PM_SUSB#(SLP_S3#) /EXIT S3 STATE, HIGH
17.	SUSB_EC# /BYPASS SLP_S3#, MAIN PWR ON
18.	ALL_SYS_PWRGD /SYSTEM POWER STABLE
19.	VCCST_PWRGD/ INDICTOR TO CPU
20.	VRM_PWRGN /POWER FOR CPU IS GOOD
21.	PM_PCH_PWROK /PCH CORE POWER OK AT LEAST 5ms
22.	SYS_PWROK /SYSTEM POWER STABLE
23.	SVID /VR controller establish protocol to CPU
24.	PLTRST# /ALL SET UP AND RESET TO INITIAL

<Core Design>

Title:	SIGNAL&RESET MAP	
Microsoft	Engineer:	Surface
Size: A2	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 5 of 76	



<Core Design>	
Title:	POWER FLOW
Microsoft	Engineer: Surface
Size: Custom	Project Name: U -- EV 1.90
Rev	1.90.2
Date: Monday, May 11, 2015	Sheet 6 of 76

CPU Haswell ULT

+VCORE	-> 32A
+1P05V	-> 0.6A
+DDR_V (+1P2V_DUAL)	-> 2.5A
+1P05V	-> 2.81A
+1P05V_MODPHY	-> 1.838A
+1P5V	-> 0.003A
+3P3V	-> 0.200A
+3P3VSB	-> 0.062A
+3P3VA	-> 0.099A

LPDDR3

+1P8V_DUAL	-> 0.717A
+1P2V_DUAL	-> 3.210A
+VTT_DDQ_VTT(0.6V)	-> 1A

mSATA(SSD)

+3P3V	-> 1.2A

EC

+3P3V_EC	-> 0.012A

EC ROM

+3P3V_EC	-> 0.005A
+3P3VA	-> 0.00025A

Temp sensor(STTS751)

+3P3V_EC	-> 0.00025A

Camera

+1P1V_CAM	-> 0.609A
+1P1V_PLLD_CAM	-> 0.0016A
+1P1V_USB_CAM	-> 0.0137A
+1P8V_CAM	-> 0.0882A
+1P8V_VDD_CAM	-> 0.122A
+2P5V_CAM	-> 0.001A
+2P5V_PLL_CAM	-> 0.000168A
+2P5V_MIPI_CAM	-> 0.00368A
+2P8V_CAM	-> 0.14A
+3P3V_CAM	-> 0.006A
+3P3V_USB_CAM	-> 0.0169A

TPM(Infineon SLB9665 ESS2)

+3P3V_TPM (+3P3V)	-> 0.1A

SDXC

+5V_SDXC	-> 0.9A

WiFi&BT

+3P3V_WWAN	-> 1.5A

DMIC

DMIC_+3P3V/+3P3V_AUDIO	-> 0.02A

FAN

+5V_FAN	-> 0.7A

UEFI_SPI_BIOS_ROM

+3P3V	-> 0.04A

Panel

VCC_EDP_BKLT_IN	-> 0.564A
+3P3V_PANEL	-> 0.2A

Authentication IC (ECC108)

+3P3VA	-> 0.005A

Touch Interface

+3P3V_TS	-> 0.0094A
+5V_TS	-> 0.0027A

ALC3264 CODEC

+3P3V_AUDIO	-> 0.005A
+5V_AUDIO	-> 1.05A
+1P8V_AUDIO	-> 0.005A

DSP (ES320)

+3P3V_AUDIO	-> 0.0063A
+1P1V_AUDIO	-> 0.0189A

Sensor uC(ATUC256L3U-Z3UR)

+3P3VA	-> 0.061A

SL1

+3P3V_HPD	->0.075A
+5V_SL1	-> 1.5A

BLADE

+5V_KB_CONN	-> 0.5A

Hall effect sensor(BU52058GWZ-E2)

+3P3VA	->0.0028A

Compass(MMC3416XMA)

+3P3V_SENSOR	->0.0012A

Acceleromte&Gyro(LSM330TR)

+3P3V_SENSOR	-> 0.0061A

ALS(ISL29033IROZ-T7) FPC CON

+3P3V_SENSOR	-> 0.000075A

MUX

+3P3V_MUX	-> 0.033A

mini DP

+3P3V	-> 0.5A

USB 3.0 connector

+5VUSBPWR	-> 0.9A

Transceiver SN74AVCT245

+1P8V_EC	-> 0.11A

Battery Charger BQ24735

+V_ALWAYS_ON	-> 0.003A

06Dec14 jks: NEEDS UPDATE

<Core Design>

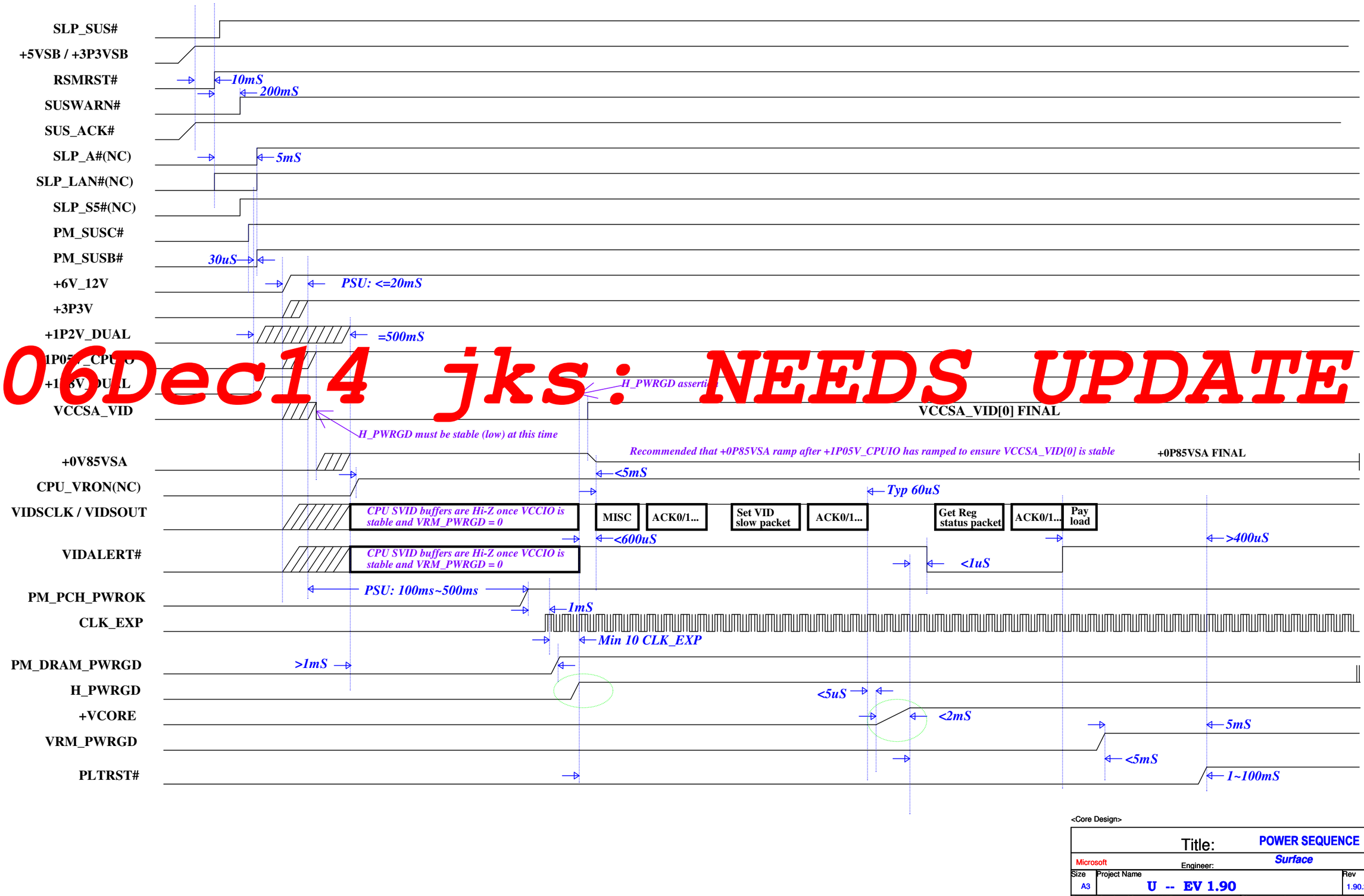
Title: POWER DISTRIBUTION

Microsoft Engineer: Surface

Size: Custom | Project Name: U -- EV 1.90 | Rev: 1.90.2

Date: Monday, May 11, 2015 | Sheet 7 of 76

S5 to S0 Power Sequence



06Dec14 jks: NEEDS UPDATE

<Core Design>

Title:	POWER SEQUENCE	
Microsoft	Engineer:	Surface
Size: A3	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 8 of 76	

I2C & SMBUS Map

SML1_PCH_DATA
SML1_PCH_CLK

Q3501
Q3504

PCH
U1001

S
M
M 0x4D

PCH_I2C1_SDA_3V3
PCH_I2C1_SCL_3V3

R3001
R3003

TS_A_I2C_SDA_CON
TS_A_I2C_SCL_CON

Touch Connector
CON3001 0x60

Surrend
TEMP Sensor
U3901 0x4B

Skin
TEMP Sensor
U3902 0x3B

Skin
TEMP Sensor
U3903 0x3A

Skin
TEMP Sensor
U3904 0x4A

SML3_EC_DATA
SML3_EC_CLK

SH_I2C_SDA
SH_I2C_SCL

Debug Connector
CON3302

U3501

SML0_EC_DATA
SML0_EC_CLK

M
S
EC
U3601
M 0x4E

S
M
SAM
U3105
0x28

I2C_SDA_MCU_R
I2C_SCL_MCU_R

R3122
R3124

I2C_SDA_MCU
I2C_SCL_MCU

TEMP Sensor
U3211 0x3A

R3229
R3230

R3266
R3267

R3210
R3211

SML1_EC_DATA
SML1_EC_CLK

CHG_SDA_A
CHG_SCL_A

Charger
U6301
0x12

PR6309
PR6310
0 ohm

ADUX1050
U3206 0x2D

ADUX6

R3285
R3287

R3212
R3213

MAG2_X_SDA
MAG2_X_SCL

Accel & Gyro
U3202 0x68

R7032/L7005
R7033/L7006

MAG2_SCL_3V3
MAG2_SDA_3V3

Magnetometer
U3203 0x30

EC_SMCLK_BAT
EC_SMDATA_BAT

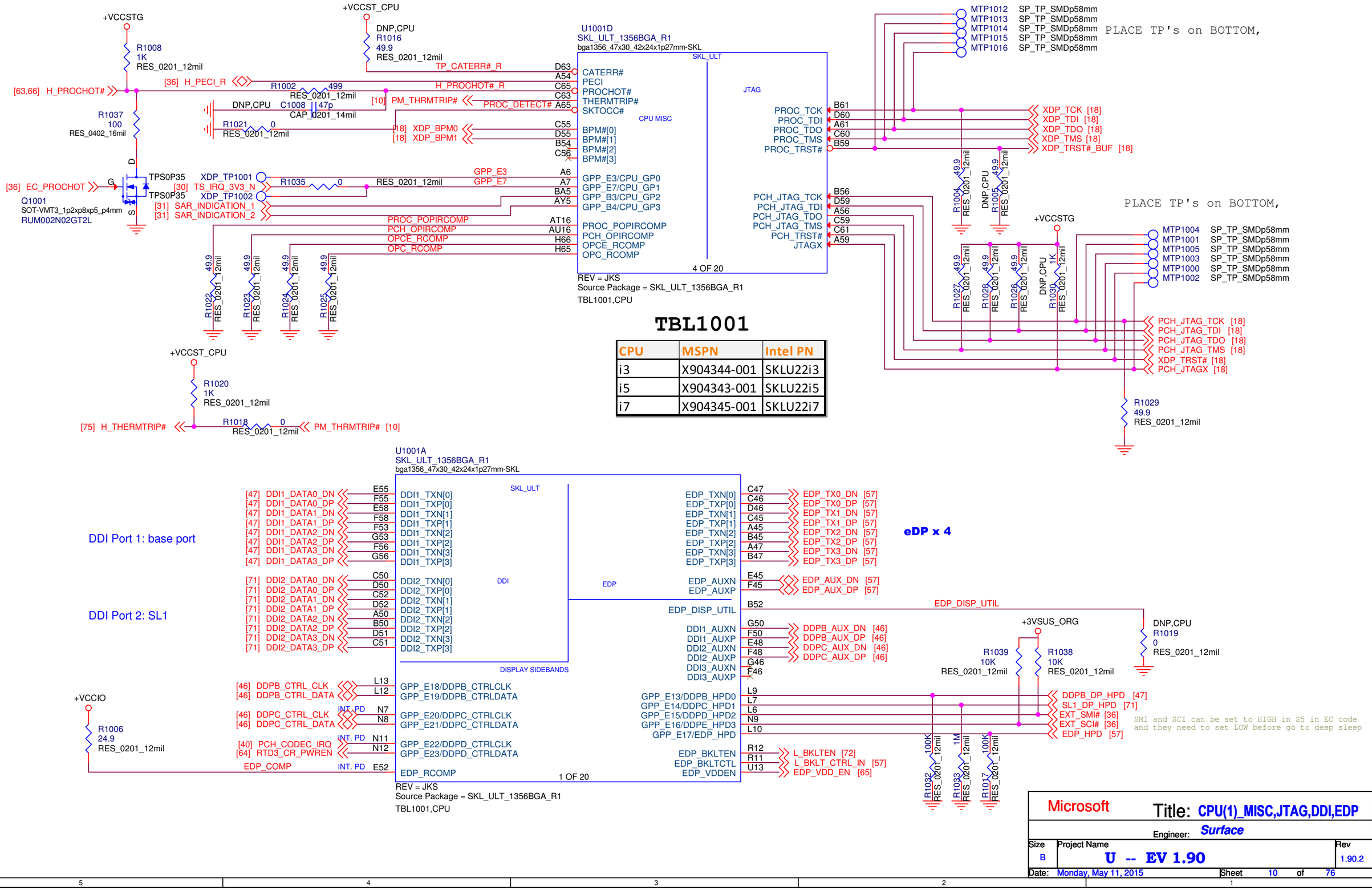
Battery
Connector
CON7001 0x16

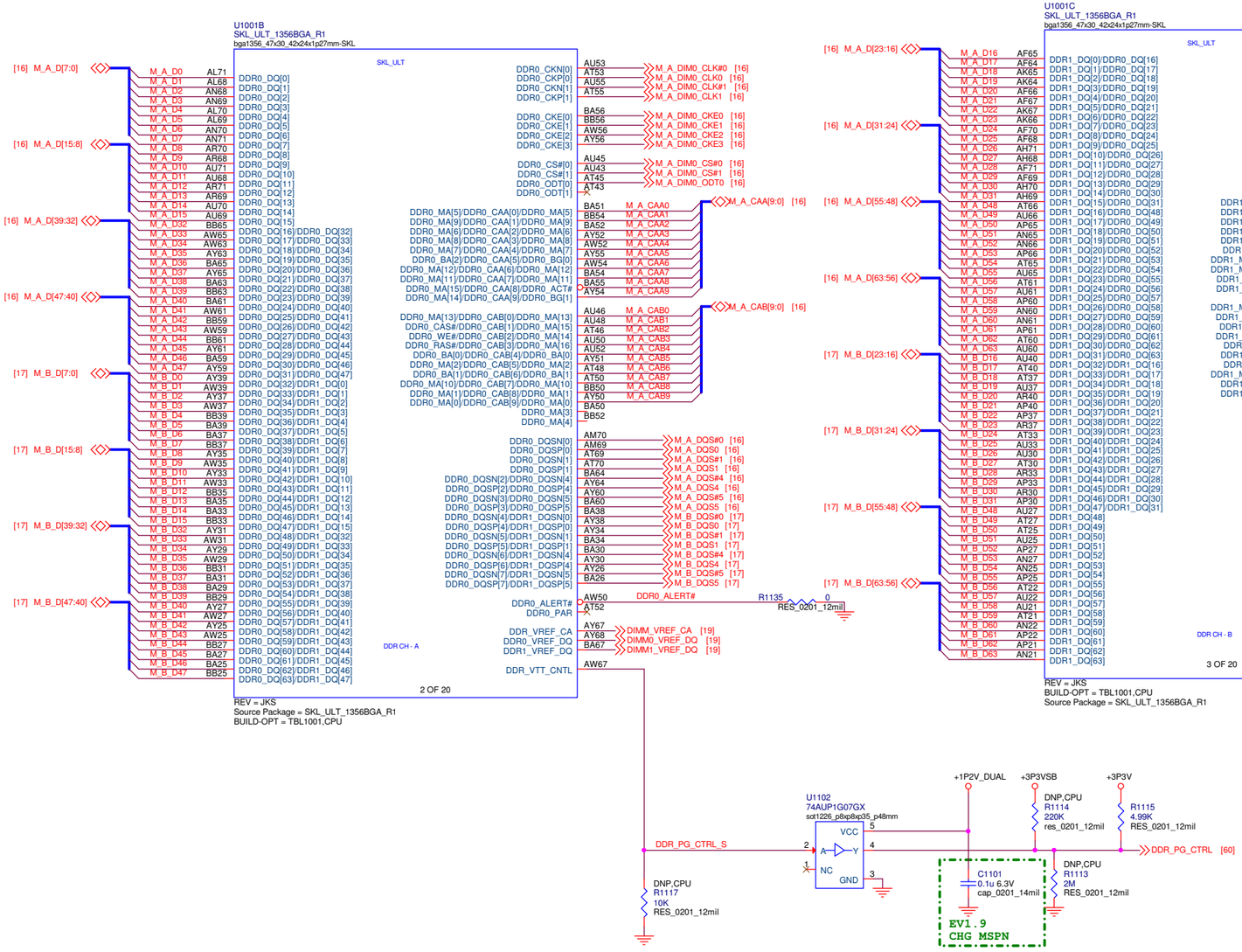
ADUX1050
U3207 0x2C

ADUX7

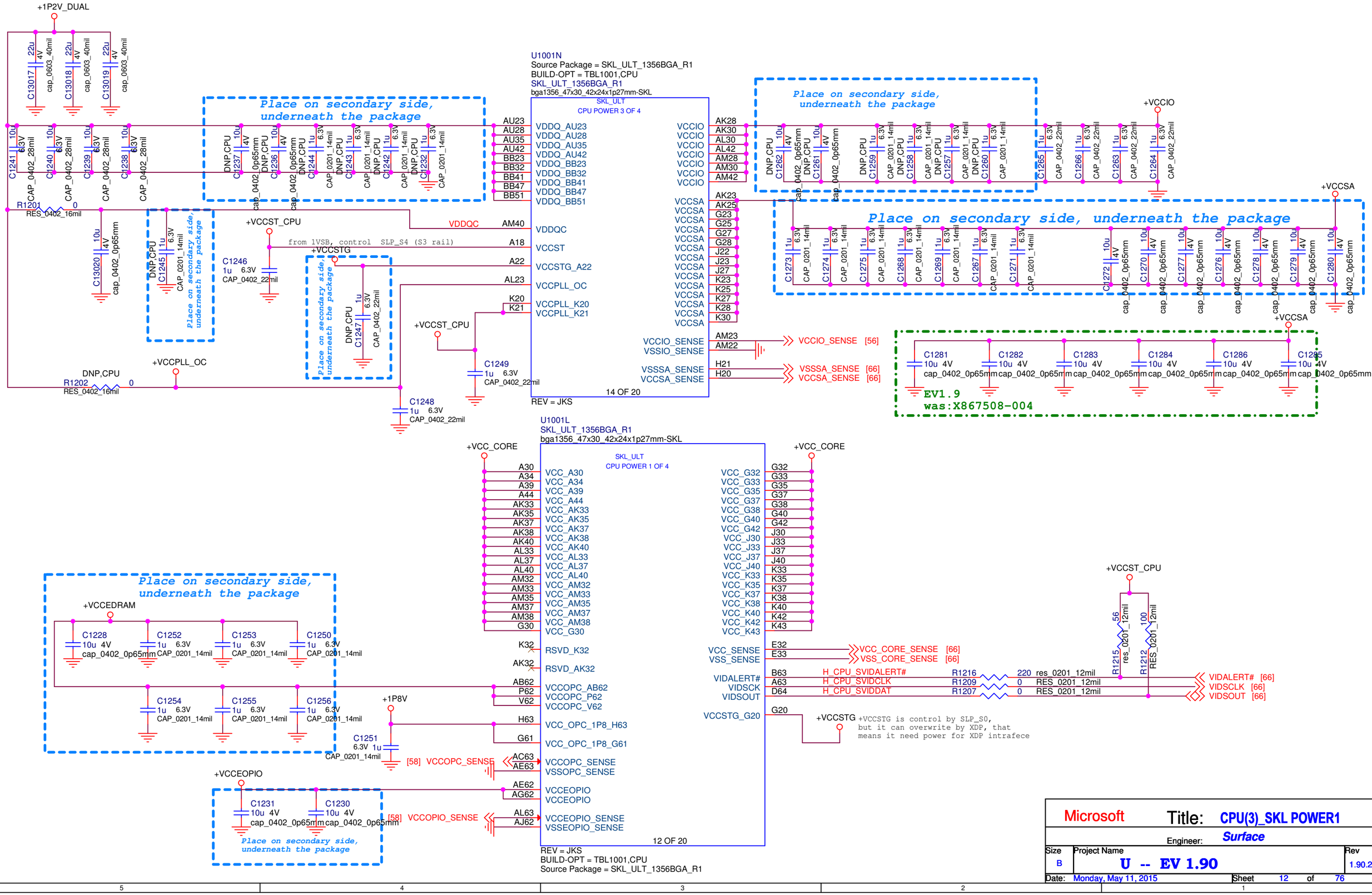
R3286
R3288

Title: 09. I2C MAP
Engineer: Surface
Size: A3
Project Name: U -- EV 1.90
Rev: 1.90.2
Date: Monday, May 11, 2015
Sheet 9 of 76


+VCCSTG
R1008
1K
RES_0201_12mil
[63,66] H_PROCHOT#
R1037
100
RES_0402_16mil
[36] EC_PROCHOT
Q1001
SOT-VMT3_1p2xp8xp5_p4mm
RUM002N02GT2L
TPS0P35
TPS0P35
+VCCST_CPU
DNP,CPU
R1016
49.9
RES_0201_12mil
[36] H_PECI_R
R1002
499
RES_0201_12mil
H_PROCHOT#_R
DNP,CPU C1008 47p
CAP_0201_14mil
[10] PM_THRMTRIP#
R1021 0
RES_0201_12mil
TP_CATERR#_R
PROC_DETECT#
[18] XDP_BPM0
[18] XDP_BPM1
XDP_TP1001
[30] TS_IRQ_3V3_N
R1035 0
RES_0201_12mil
XDP_TP1002
[31] SAR_INDICATION_1
[31] SAR_INDICATION_2
GPP_E3
GPP_E7
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
R1022 49.9 RES_0201_12mil
R1023 49.9 RES_0201_12mil
R1024 49.9 RES_0201_12mil
R1025 49.9 RES_0201_12mil
U1001D
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
CPU MISC
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
JTAG
PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#
PCH_JTAG_TCK
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_TRST#
JTAGX
4 OF 20
REV = JKS
Source Package = SKL_ULT_1356BGA_R1
TBL1001,CPU
MTP1012 SP_TP_SMDp58mm
MTP1013 SP_TP_SMDp58mm
MTP1014 SP_TP_SMDp58mm
MTP1015 SP_TP_SMDp58mm
MTP1016 SP_TP_SMDp58mm
PLACE TP's on BOTTOM,
XDP_TCK [18]
XDP_TDI [18]
XDP_TDO [18]
XDP_TMS [18]
XDP_TRST#_BUF [18]
R1004 49.9 RES_0201_12mil
DNP,CPU R1005 49.9 RES_0201_12mil
PLACE TP's on BOTTOM,
+VCCSTG
R1027 49.9 RES_0201_12mil
R1028 49.9 RES_0201_12mil
R1026 49.9 RES_0201_12mil
DNP,CPU R1030 1K RES_0201_12mil
MTP1004 SP_TP_SMDp58mm
MTP1001 SP_TP_SMDp58mm
MTP1005 SP_TP_SMDp58mm
MTP1003 SP_TP_SMDp58mm
MTP1000 SP_TP_SMDp58mm
MTP1002 SP_TP_SMDp58mm
PCH_JTAG_TCK [18]
PCH_JTAG_TDI [18]
PCH_JTAG_TDO [18]
PCH_JTAG_TMS [18]
XDP_TRST# [18]
PCH_JTAGX [18]
R1029
49.9
RES_0201_12mil
TBL1001
CPU | MSPN | Intel PN
i3 | X904344-001 | SKLU22i3
i5 | X904343-001 | SKLU22i5
i7 | X904345-001 | SKLU22i7
+VCCST_CPU
R1020
1K
RES_0201_12mil
[75] H_THERMTRIP#
R1018 0
RES_0201_12mil
PM_THRMTRIP# [10]
U1001A
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
DDI
EDP
DISPLAY SIDEBANDS
DDI Port 1: base port
DDI Port 2: SL1
[47] DDI1_DATA0_DN
[47] DDI1_DATA0_DP
[47] DDI1_DATA1_DN
[47] DDI1_DATA1_DP
[47] DDI1_DATA2_DN
[47] DDI1_DATA2_DP
[47] DDI1_DATA3_DN
[47] DDI1_DATA3_DP
[71] DDI2_DATA0_DN
[71] DDI2_DATA0_DP
[71] DDI2_DATA1_DN
[71] DDI2_DATA1_DP
[71] DDI2_DATA2_DN
[71] DDI2_DATA2_DP
[71] DDI2_DATA3_DN
[71] DDI2_DATA3_DP
[46] DDPB_CTRL_CLK
[46] DDPB_CTRL_DATA
[46] DDPC_CTRL_CLK
[46] DDPC_CTRL_DATA
[40] PCH_CODEC_IRQ
[64] RTD3_CR_PWREN
EDP_COMP
+VCCIO
R1006
24.9
RES_0201_12mil
GPP_E18/DDPB_CTRLCLK
GPP_E19/DDPB_CTRLDATA
GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA
GPP_E22/DDPD_CTRLCLK
GPP_E23/DDPD_CTRLDATA
EDP_RCOMP
1 OF 20
REV = JKS
Source Package = SKL_ULT_1356BGA_R1
TBL1001,CPU
eDP x 4
EDP_TX0_DN [57]
EDP_TX0_DP [57]
EDP_TX1_DN [57]
EDP_TX1_DP [57]
EDP_TX2_DN [57]
EDP_TX2_DP [57]
EDP_TX3_DN [57]
EDP_TX3_DP [57]
EDP_AUX_DN [57]
EDP_AUX_DP [57]
EDP_DISP_UTIL
DDPB_AUX_DN [46]
DDPB_AUX_DP [46]
DDPC_AUX_DN [46]
DDPC_AUX_DP [46]
+3VSUS_ORG
R1039 10K RES_0201_12mil
R1038 10K RES_0201_12mil
DNP,CPU R1019 0 RES_0201_12mil
DDPB_DP_HPD [47]
SL1_DP_HPD [71]
EXT_SMI# [36]
EXT_SCI# [36]
EDP_HPD [57]
SMI and SCI can be set to HIGH in S5 in EC code
and they need to set LOW before go to deep sleep
L_BKLTEN [72]
L_BKLT_CTRL_IN [57]
EDP_VDD_EN [65]
R1032 100K RES_0201_12mil
R1033 1M RES_0201_12mil
R1017 100K RES_0201_12mil
Microsoft
Title: CPU(1)_MISC,JTAG,DDI,EDP
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 10 of 76



Microsoft	Title: CPU(2)_LPDDR3
	Engineer: Surface
Size: C	Project Name: U -- EV 1.90
Rev: 1.90.2	
Date: Monday, May 11, 2015	Sheet 11 of 76


+1P2V_DUAL
C13017 22u 4V cap_0603_40mil
C13018 22u 4V cap_0603_40mil
C13019 22u 4V cap_0603_40mil
U1001N
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
CPU POWER 3 OF 4
VDDQ_AU23
VDDQ_AU28
VDDQ_AU35
VDDQ_AU42
VDDQ_BB23
VDDQ_BB32
VDDQ_BB41
VDDQ_BB47
VDDQ_BB51
VDDQC
VCCST
VCCSTG_A22
VCCPLL_OC
VCCPLL_K20
VCCPLL_K21
VCCIO
VCCSA
VCCIO_SENSE
VSSIO_SENSE
VSSSA_SENSE
VCCSA_SENSE
14 OF 20
REV = JKS
Place on secondary side, underneath the package
+VCCIO
+VCCSA
+VCCST_CPU
+VCCPLL_OC
DNP,CPU
R1201 0 RES_0402_16mil
R1202 0 RES_0402_16mil
from lVSB, control SLP_S4 (S3 rail)
+VCCSTG
VCCIO_SENSE [56]
VSSSA_SENSE [66]
VCCSA_SENSE [66]
EV1.9
was:X867508-004
U1001L
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
CPU POWER 1 OF 4
VCC_A30
VCC_A34
VCC_A39
VCC_A44
VCC_AK33
VCC_AK35
VCC_AK37
VCC_AK38
VCC_AK40
VCC_AL33
VCC_AL37
VCC_AL40
VCC_AM32
VCC_AM33
VCC_AM35
VCC_AM37
VCC_AM38
VCC_G30
RSVD_K32
RSVD_AK32
VCCOPC_AB62
VCCOPC_P62
VCCOPC_V62
VCC_OPC_1P8_H63
VCC_OPC_1P8_G61
VCCOPC_SENSE
VSSOPC_SENSE
VCCEOPIO
VCCEOPIO_SENSE
VSSEOPIO_SENSE
VCC_G32
VCC_G33
VCC_G35
VCC_G37
VCC_G38
VCC_G40
VCC_G42
VCC_J30
VCC_J33
VCC_J37
VCC_J40
VCC_K33
VCC_K35
VCC_K37
VCC_K38
VCC_K40
VCC_K42
VCC_K43
VCC_SENSE
VSS_SENSE
VIDALERT#
VIDSCK
VIDSOUT
VCCSTG_G20
12 OF 20
REV = JKS
BUILD-OPT = TBL1001,CPU
Source Package = SKL_ULT_1356BGA_R1
+VCC_CORE
+VCCEDRAM
+VCCEOPIO
+1P8V
VCC_CORE_SENSE [66]
VSS_CORE_SENSE [66]
VCCOPC_SENSE [58]
VCCOPIO_SENSE [58]
H_CPU_SVIDALERT#
H_CPU_SVIDCLK
H_CPU_SVIDDAT
VIDALERT# [66]
VIDSCLK [66]
VIDSOUT [66]
+VCCSTG +VCCSTG is control by SLP_S0, but it can overwrite by XDP, that means it need power for XDP intrafece
Microsoft
Title: CPU(3)_SKL POWER1
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 12 of 76

U1001M
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
CPU POWER 2 OF 4

+VCCGT

VCCGT: A48, A53, A58, A62, A66, AA63, AA64, AA66, AA67, AA69, AA70, AA71, AC64, AC65, AC66, AC67, AC68, AC69, AC70, AC71, J43, J45, J46, J48, J50, J52, J53, J55, J56, J58, J60, K48, K50, K52, K53, K55, K56, K58, K60, L62, L63, L64, L65, L66, L67, L68, L69, L70, L71, M62, N63, N64, N66, N67, N69, N70, N71, R63, R64, R65, R66, R67, R68, R69, R70, R71, T62, U65, U68, U71, W63, W64, W65, W66, W67, W68, W69, W70, W71, Y62

+VCCGT

VCCGTX_AK42: AK42, AK43, AK45, AK46, AK48, AK50, AK52, AK53, AK55, AK56, AK58, AK60, AK70, AL43, AL46, AL50, AL53, AL56, AL60, AM48, AM50, AM52, AM53, AM56, AM58, AU58, AU63, BB57, BB66, AK62, AL61

[66] VCCGT_SENSE — J70 VCCGT_SENSE
[66] VSSGT_SENSE — J69 VSSGT_SENSE
VCCGTX_SENSE
VSSGTX_SENSE

13 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

+VCC_CORE

Place on secondary side, underneath the package

C1315 C1314 C1317 C1316 C1310 C1311 C1312 C1313 C1318
10u 4V cap_0402_0p65mm

C13179 C13182 C13180 C13184 C13178 C13183 C13181 C13185 C13186
10u 4V cap_0402_0p65mm

C13188 C13191 C13189 C13193 C13187 C13192 C13190 C13194 C13195
10u 4V cap_0402_0p65mm

C1328 C1327 C1326 C1325 C1324 C1331 C1329
10u 4V cap_0402_0p65mm

EV1.9
was:X867508-004

C1334 C1335 C1332 C1333 C1323 C1330 C1301 C1300
1u 6.3V CAP_0201_14mil

C1306 C1307 C1304 C1305 C1302 C1303 C1309
1u 6.3V CAP_0201_14mil

C13108 C1322 C13104 C13103 C13106 C13105 C13107
1u 6.3V CAP_0201_14mil

C13115 C13109 C13111 C13110 C13113 C13112 C13114
1u 6.3V CAP_0201_14mil

C13121 C13116 C13119 C13117 C13120 C13118
1u 6.3V CAP_0201_14mil

THIS IS PLACE ON VCCGTX pins (they are connected to +VCCGT)
Place on secondary side, underneath the package
only for 23e

+VCCGT

U23E,CPU C1390 C1391 C1389 C1393 C1392 C1394 C1395 C1396
10u 4V cap_0402_0p65mm

EV1.9
was:X867508-004

only for 23e

U23E,CPU C13101 C1376 C1397 C1398 C1399 C1308 C13100 C13102
22u 4V cap_0603_40mil

+VCCGT

Place on secondary side, underneath the package

C1355 C1353 C1352 C1351 C1350 C1358 C1354 C1368 C1369 C1370 C13122 C13123
10u 4V cap_0402_0p65mm

EV1.9
was:X867508-004

C1361 C1360 C1357 C1359 C1349 C1356 C13196
1u 6.3V CAP_0201_14mil

C1366 C1367 C1364 C1365 C1363 C1362 C13197
1u 6.3V CAP_0201_14mil

DNP_CPU C13124 C13125 C13126 C13127 C13128 C13129 C13130 C13131 C13132 C13133 C13134 C13135 C13136 C13137 C13138 C13139 C13140 C13141 C13142 C13143
10u 4V cap_0402_0p65mm

EV1.9
was:X867508-003

Place on secondary side, underneath the package

DNP_CPU C13144 C13145 C13146 C13147 C13148 C13149 C13177 C13151 C13152 C13153 C13154 C13155 C13156 C13157 C13158 C13159 C13160 C13161 C13162 C13163
1u 6.3V CAP_0201_14mil

C1371 C1373 C1372 C1374 C1375
47u 6.3V cap_0805_36mil

C1382 C1381 C1384 C1383 C1377 C1378 C1379
22u 6.3V cap_0603_38mil

EV19
WAS: 0402

C13165 C13166 C13164
47u 6.3V cap_0805_36mil

C1380 C1385 C1386 C1387 C1388
22u 6.3V cap_0603_38mil

EV19
WAS: 0402

DNP_CPU C13167 C13168 C13169 C13170 C13171 C13172 C13173 C13174 C13175 C13176
10u 4V cap_0402_0p65mm

EV1.9
was:X867508-002

+VCC_CORE

C1338 C1337 C1336 C1320 C1321 C1319 C1339 C1340
10u 4V cap_0402_0p65mm

EV1.9
was:X867508-001

C1341 C1342 C1343 C1344 C1345 C1346 C1347 C1348
47u 6.3V cap_0603_40mil

EV1.9 was:0805

Microsoft

Title: CPU(4)_SKL_POWER2

Engineer: Surface

Size	Project Name	Rev
C	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 13 of 76

U1001P
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
GND 1 OF 3

A5	VSS	VSS	AL65
A67	VSS	VSS	AL66
A70	VSS	VSS	AM13
AA2	VSS	VSS	AM21
AA4	VSS	VSS	AM25
AA65	VSS	VSS	AM27
AA68	VSS	VSS	AM43
AB15	VSS	VSS	AM45
AB16	VSS	VSS	AM46
AB18	VSS	VSS	AM55
AB21	VSS	VSS	AM60
AB8	VSS	VSS	AM61
AD13	VSS	VSS	AM68
AD16	VSS	VSS	AM71
AD19	VSS	VSS	AM8
AD20	VSS	VSS	AN20
AD21	VSS	VSS	AN23
AD62	VSS	VSS	AN28
AD8	VSS	VSS	AN30
AE64	VSS	VSS	AN32
AE65	VSS	VSS	AN33
AE66	VSS	VSS	AN35
AE67	VSS	VSS	AN37
AE68	VSS	VSS	AN38
AE69	VSS	VSS	AN40
AF1	VSS	VSS	AN42
AF10	VSS	VSS	AN58
AF15	VSS	VSS	AN63
AF17	VSS	VSS	AP10
AF2	VSS	VSS	AP18
AF4	VSS	VSS	AP20
AF63	VSS	VSS	AP23
AG16	VSS	VSS	AP28
AG17	VSS	VSS	AP32
AG18	VSS	VSS	AP35
AG19	VSS	VSS	AP38
AG20	VSS	VSS	AP42
AG21	VSS	VSS	AP58
AG71	VSS	VSS	AP63
AH13	VSS	VSS	AP68
AH6	VSS	VSS	AP70
AH63	VSS	VSS	AR11
AH64	VSS	VSS	AR15
AH67	VSS	VSS	AR16
AJ15	VSS	VSS	AR20
AJ18	VSS	VSS	AR23
AJ20	VSS	VSS	AR28
AJ4	VSS	VSS	AR35
AK11	VSS	VSS	AR42
AK16	VSS	VSS	AR43
AK18	VSS	VSS	AR45
AK21	VSS	VSS	AR46
AK22	VSS	VSS	AR48
AK27	VSS	VSS	AR5
AK63	VSS	VSS	AR50
AK68	VSS	VSS	AR52
AK69	VSS	VSS	AR53
AK8	VSS	VSS	AR55
AL2	VSS	VSS	AR58
AL28	VSS	VSS	AR63
AL32	VSS	VSS	AR8
AL35	VSS	VSS	AT2
AL38	VSS	VSS	AT20
AL4	VSS	VSS	AT23
AL45	VSS	VSS	AT28
AL48	VSS	VSS	AT35
AL52	VSS	VSS	AT4
AL55	VSS	VSS	AT42
AL58	VSS	VSS	AT56
AL64	VSS	VSS	AT58

16 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

U1001Q
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
GND 2 OF 3

AT63	VSS	VSS	BA49
AT68	VSS	VSS	BA53
AT71	VSS	VSS	BA57
AU10	VSS	VSS	BA6
AU15	VSS	VSS	BA62
AU20	VSS	VSS	BA66
AU32	VSS	VSS	BA71
AU38	VSS	VSS	BB18
AV1	VSS	VSS	BB26
AV68	VSS	VSS	BB30
AV69	VSS	VSS	BB34
AV70	VSS	VSS	BB38
AV71	VSS	VSS	BB43
AW10	VSS	VSS	BB55
AW12	VSS	VSS	BB6
AW14	VSS	VSS	BB60
AW16	VSS	VSS	BB64
AW18	VSS	VSS	BB67
AW21	VSS	VSS	BB70
AW23	VSS	VSS	C1
AW26	VSS	VSS	C25
AW28	VSS	VSS	C5
AW30	VSS	VSS	D10
AW32	VSS	VSS	D11
AW34	VSS	VSS	D14
AW36	VSS	VSS	D18
AW38	VSS	VSS	D22
AW41	VSS	VSS	D25
AW43	VSS	VSS	D26
AW45	VSS	VSS	D30
AW47	VSS	VSS	D34
AW49	VSS	VSS	D39
AW51	VSS	VSS	D44
AW53	VSS	VSS	D45
AW55	VSS	VSS	D47
AW57	VSS	VSS	D48
AW6	VSS	VSS	D53
AW60	VSS	VSS	D58
AW62	VSS	VSS	D6
AW64	VSS	VSS	D62
AW66	VSS	VSS	D66
AW8	VSS	VSS	D69
AY66	VSS	VSS	E11
B10	VSS	VSS	E15
B14	VSS	VSS	E18
B18	VSS	VSS	E21
B22	VSS	VSS	E46
B30	VSS	VSS	E50
B34	VSS	VSS	E53
B39	VSS	VSS	E56
B44	VSS	VSS	E6
B48	VSS	VSS	E65
B53	VSS	VSS	E71
B58	VSS	VSS	F1
B62	VSS	VSS	F13
B66	VSS	VSS	F2
B71	VSS	VSS	F22
BA1	VSS	VSS	F23
BA10	VSS	VSS	F27
BA14	VSS	VSS	F28
BA18	VSS	VSS	F32
BA2	VSS	VSS	F33
BA23	VSS	VSS	F35
BA28	VSS	VSS	F37
BA32	VSS	VSS	F38
BA36	VSS	VSS	F4
F68	VSS	VSS	F40
BA45	VSS	VSS	F42
	VSS	VSS	BA41

17 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

U1001R
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
GND 3 OF 3

F8	VSS	VSS	L18
G10	VSS	VSS	L2
G22	VSS	VSS	L20
G43	VSS	VSS	L4
G45	VSS	VSS	L8
G48	VSS	VSS	N10
G5	VSS	VSS	N13
G52	VSS	VSS	N19
G55	VSS	VSS	N21
G58	VSS	VSS	N6
G6	VSS	VSS	N65
G60	VSS	VSS	N68
G63	VSS	VSS	P17
G66	VSS	VSS	P19
H15	VSS	VSS	P20
H18	VSS	VSS	P21
H71	VSS	VSS	R13
J11	VSS	VSS	R6
J13	VSS	VSS	T15
J25	VSS	VSS	T17
J28	VSS	VSS	T18
J32	VSS	VSS	T2
J35	VSS	VSS	T21
J38	VSS	VSS	T4
J42	VSS	VSS	U10
J8	VSS	VSS	U63
K16	VSS	VSS	U64
K18	VSS	VSS	U66
K22	VSS	VSS	U67
K61	VSS	VSS	U69
K63	VSS	VSS	U70
K64	VSS	VSS	V16
K65	VSS	VSS	V17
K66	VSS	VSS	V18
K67	VSS	VSS	W13
K68	VSS	VSS	W6
K70	VSS	VSS	W9
K71	VSS	VSS	Y17
L11	VSS	VSS	Y19
L16	VSS	VSS	Y20
L17	VSS	VSS	Y21
	VSS	VSS	

18 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

Microsoft

Title: CPU(5)_GND

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 14 of 76

CFG4	
0 **Default**	enable eDP
1	Disable eDP

TP1516

[18] CFG0
[18] CFG1
[18] CFG2
[18] CFG3
[18] CFG4
[18] CFG5
[18] CFG6
[18] CFG7
[18] CFG8
[18] CFG9
[18] CFG10
[18] CFG11
[18] CFG12
[18] CFG13
[18] CFG14
[18] CFG15
[18] CFG16
[18] CFG17
[18] CFG18
[18] CFG19

R1501
1K
RES_0201_12mil

R1507 49.9 RES_0201_12mil CFG_RCOMP

[18] ITP_PMODE

U1001S
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
RESERVED SIGNALS-1

E68	CFG[0]	
B67	CFG[1]	
D65	CFG[2]	
D67	CFG[3]	
E70	CFG[4]	
C68	CFG[5]	
D68	CFG[6]	
C67	CFG[7]	
F71	CFG[8]	
G69	CFG[9]	
F70	CFG[10]	
G68	CFG[11]	
H70	CFG[12]	
G71	CFG[13]	
H69	CFG[14]	
G70	CFG[15]	
E63	CFG[16]	
F63	CFG[17]	
E66	CFG[18]	
F66	CFG[19]	
E60	CFG_RCOMP	
E8	ITP_PMODE	
AY2	RSVD_AY2	
AY1	RSVD_AY1	
D1	RSVD_D1	
D3	RSVD_D3	
K46	RSVD_K46	
K45	RSVD_K45	
AL25	RSVD_AL25	
AL27	RSVD_AL27	
C71	RSVD_C71	
B70	RSVD_B70	
F60	RSVD_F60	
A52	RSVD_A52	
BA70	RSVD_TP_BA70	
BA68	RSVD_TP_BA68	
J71	RSVD_J71	
J68	RSVD_J68	
F65	VSS_F65	
G65	VSS_G65	
F61	RSVD_F61	
E61	RSVD_E61	

RSVD_TP_BB68	BB68	
RSVD_TP_BB69	BB69	
RSVD_TP_AK13	AK13	RSVD_TP_AK13 → TP1503 SP_TP_SMDp58mm
RSVD_TP_AK12	AK12	RSVD_TP_AK12 → TP1502 SP_TP_SMDp58mm
RSVD_BB2	BB2	
RSVD_BA3	BA3	
TP5	AU5	
TP6	AT5	
RSVD_D5	D5	
RSVD_D4	D4	
RSVD_B2	B2	
RSVD_C2	C2	
RSVD_B3	B3	
RSVD_A3	A3	
RSVD_AW1	AW1	
RSVD_E1	E1	
RSVD_E2	E2	
RSVD_BA4	BA4	
RSVD_BB4	BB4	
RSVD_A4	A4	
RSVD_C4	C4	
TP4	BB5	
RSVD_A69	A69	
RSVD_B69	B69	
RSVD_AY3	AY3	RSVD_AY3 R1502 0 RES_0201_12mil DNP,CPU
RSVD_D71	D71	
RSVD_C70	C70	
RSVD_C54	C54	
RSVD_D54	D54	
TP1	AY4	
TP2	BB3	
VSS_AY71	AY71	
ZVM#	AR56	ZVM# [58]
RSVD_TP_AW71	AW71	
RSVD_TP_AW70	AW70	
MSM#	AP56	MSM# [58]
PROC_SELECT#	C64	PROC_SELECT#

19 OF 20

REV = JKS
TBL1001,CPU
Source Package = SKL_ULT_1356BGA_R1

MFang 8Jan15: [Intel] used in the HVM testing should be left not connected.

ZVM# and MSM# may need to control the VCCOPC and VCCEOPIO

+VCCST_CPU
R1540 100K RES_0201_12mil
DNP,CPU

100k ohm resistor only needed for Cannonlake

U1001T
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT
SPARE

AW69	RSVD_AW69	RSVD_F6	F6
AW68	RSVD_AW68	RSVD_E3	E3
AU56	RSVD_AU56	RSVD_C11	C11
AW48	RSVD_AW48	RSVD_B11	B11
C7	RSVD_C7	RSVD_A11	A11
U12	RSVD_U12	RSVD_D12	D12
U11	RSVD_U11	RSVD_C12	C12
H11	RSVD_H11	RSVD_F52	F52

20 OF 20

REV = JKS
TBL1001,CPU
Source Package = SKL_ULT_1356BGA_R1

+1P8VSUS_ORG

DNP,CPU
C1501
1u
CAP_0402_22mil
6.3V

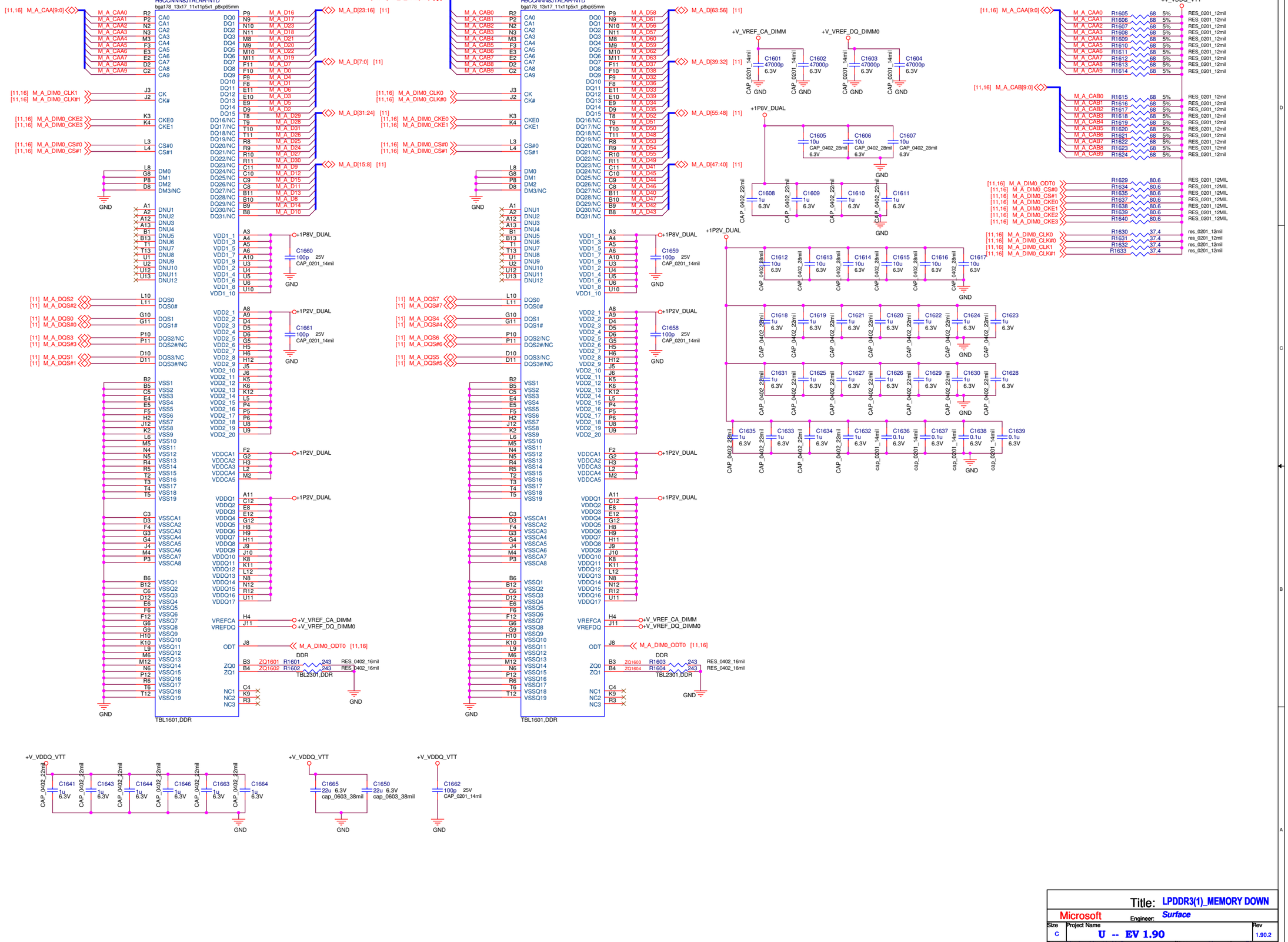
Microsoft

Title: CPU(6)_CFG_RESERVED

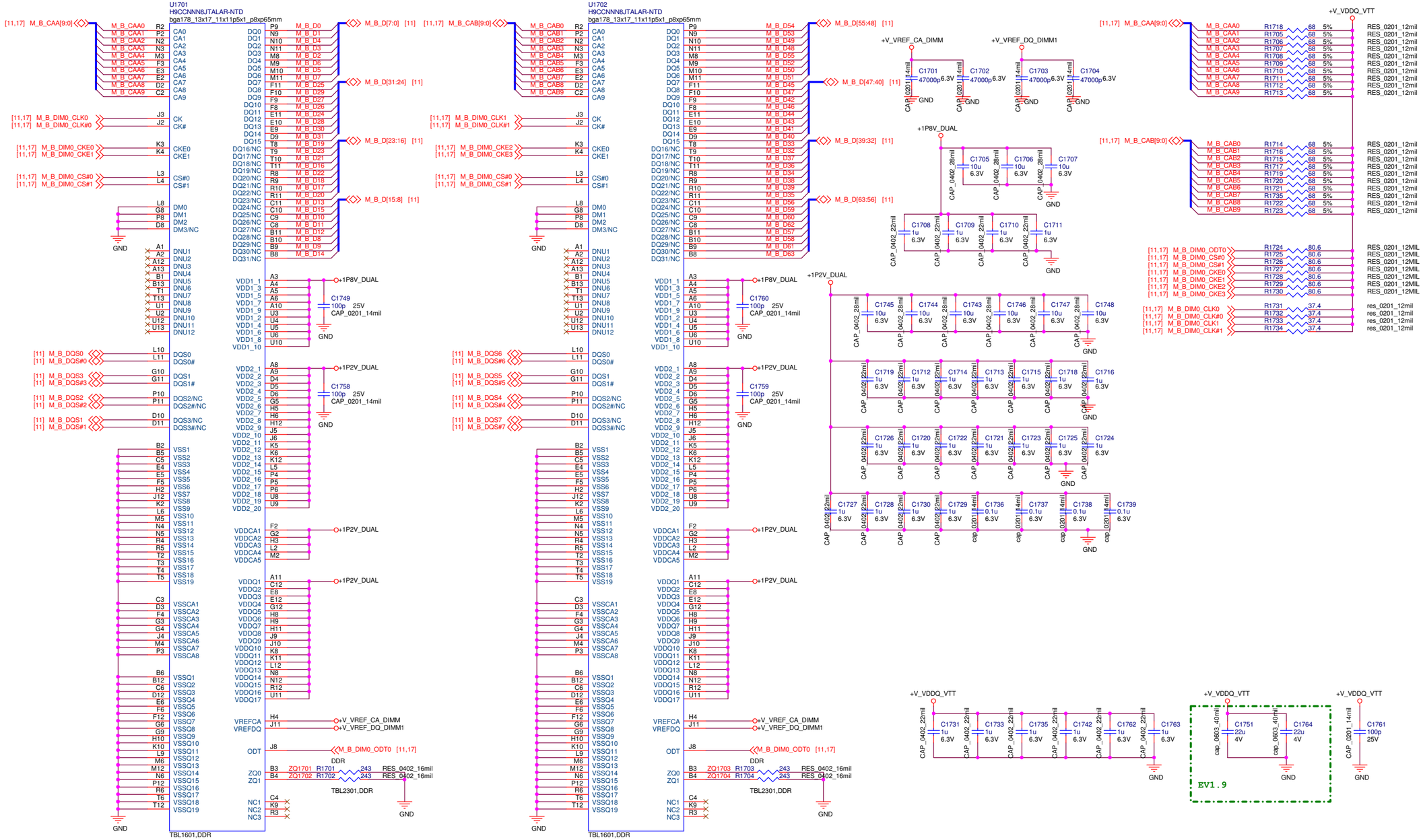
Engineer: *Surface*

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 15 of 76



Title:	LPDDR3(1)_MEMORY DOWN		
Microsoft	Engineer: Surface		
Size: C	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 16 of 76		



Title:	LPDDR3(2)_MEMORY DOWN		
Microsoft	Engineer: Surface		
Size: C	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 17 of 76	

PRIMARY XDP connector

[15,18] CFG3
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<3>
DB,XDP R1841 1K RES_0201_12mil
DB,XDP R1840 0 RES_0201_12mil
+1VSB_XDP
DNP,XDP R1803 49.9 RES_0201_12mil
XDP_PIN1
+1VSB
DB,XDP R1838 0 RES_0201_12mil
+1VSB_XDP
DB,XDP J1801 X869110-001
B2B 60P
conn_b2b-r_60_4mtg_14p2x2p54xp88_p4mm
RECEPTACLE

[24] XDP_PREQ#
[24] XDP_PRDY#
[15,18] CFG0
[15] CFG1
[15] CFG2
[15,18] CFG3
[10] XDP_BPM0
[10] XDP_BPM1
[15] CFG4
[15] CFG5
[15] CFG6
[15] CFG7
CFG17 [15]
CFG16 [15]
CFG8 [15]
CFG9 [15]
CFG10 [15]
CFG11 [15]
CFG19 [15]
CFG18 [15]
CFG12 [15]
CFG13 [15]
CFG14 [15]
CFG15 [15]

+1VSB_XDP
DNP,XDP C1803 1u 6.3V CAP_0201_14mil
GND
+3P3VSB
DB,XDP R1826 1.5K RES_0201_12mil

[22,36] RSMRST#
[22] PCH_PWRBTN#
[30,32,33] PWR_SW_N
R1842 DB,XDP 1K RES_0201_12mil
R1807 DB,XDP 0 RES_0201_12mil
R1804 DNP,XDP 0 RES_0201_12mil
PM_RSMRST_PWRGD_XDP
PM_PWRBTN#_XDP

[21] SPI0_MOSI_XDP
R1846 DB,XDP 0 RES_0201_12mil
[15,18] CFG0
R1843 DNP,XDP 0 XDP_CFG0
XDP_MOSI_R
RES_0201_12mil

DB,XDP PC1804 0.1u 6.3V cap_0201_14mil
DB,XDP PC1805 0.1u 6.3V cap_0201_14mil
GND

[21] SMBDATA
[21] SMBCLK
XDP_TCK1
[10] PCH_JTAG_TCK
[10] XDP_TCK
R1821 DB,XDP 0 RES_0201_12mil
R1853 DNP,XDP 0 RES_0201_12mil
[10] PCH_JTAGX
R1811 DB,XDP 0 RES_0201_12mil

CLK_XDP_R_DP
CLK_XDP_R_DN
XDP_RST#_R
XDP_DBRESET#_R
XDP_TDO_BUF
XDP_TDI_R
XDP_PIN60
MTG1 MTG2 MTG3 MTG4
[21] XDP_SPI0_IO2
R1845 DB,XDP 0 RES_0201_12mil
R1854 DNP,XDP 0 RES_0201_12mil

+1VSB_XDP
DB,XDP R1844 1K RES_0201_12mil
+3P3V
DB,XDP R1823 1K RES_0201_12mil

+VCCSTG
DNP,XDP R1825 49.9 RES_0201_12mil
Place R1825 within 1100mil from CPU

R1805 DB,XDP 0 RES_0201_12mil
R1806 DB,XDP 0 RES_0201_12mil
R1837 DB,XDP 0 RES_0201_12mil
R1808 DNP,XDP 1K RES_0201_12mil
R1810 DB,XDP 0 RES_0201_12mil
R1809 DB,XDP 0 RES_0201_12mil
R1849 DB,XDP 0 RES_0201_12mil
R1851 DB,XDP 0 RES_0201_12mil

CLK_XDP_DP [20]
CLK_XDP_DN [20]
ITP_PMODE [15]
PLT_RST#_BUF [22,36,38,43,75]
PCH_SYS_RST# [22]
XDP_TRST#_BUF [10]
XDP_TDO [10]
XDP_TRST# [10]
XDP_TDI [10]
XDP_TMS [10]

DB,XDP C1801 0.01u 10V CAP_0201_14mil
GND
DNP,XDP R1852 0 RES_0201_12mil

R1822 DB,XDP 0 RES_0201_12mil
R1848 DB,XDP 0 RES_0201_12mil
R1847 DB,XDP 0 RES_0201_12mil

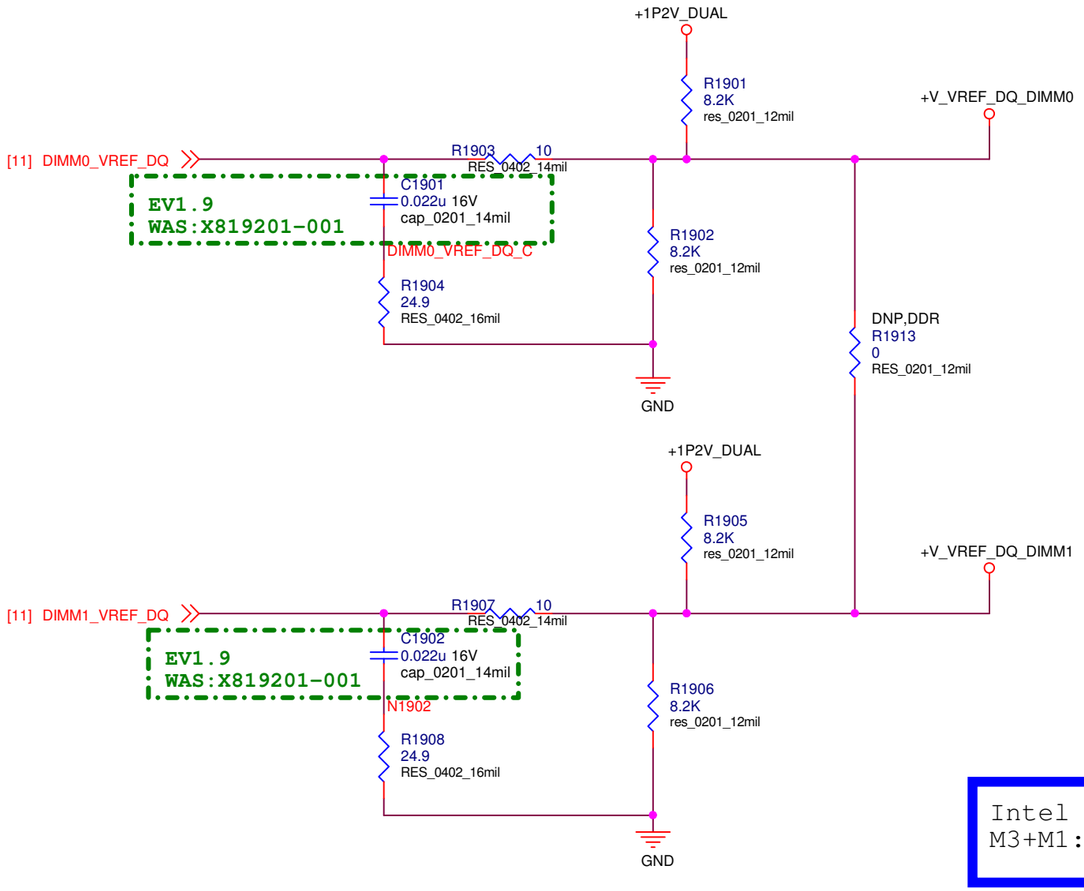
PCH_JTAG_TDI [10]
PCH_JTAG_TMS [10]
PCH_JTAG_TDO [10]

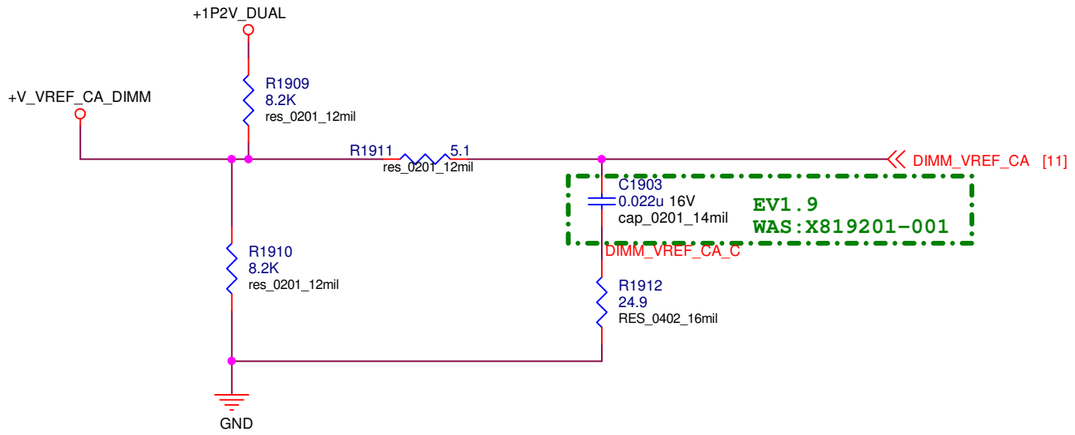
For the signals only go to XDP, the 0R should be close to XDP connector.
For the signals to both XDP and target circuit, the option resistor locaction should follow the target signal routing.

Title: XDP			
Microsoft	Engineer: Surface		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 18 of 76		

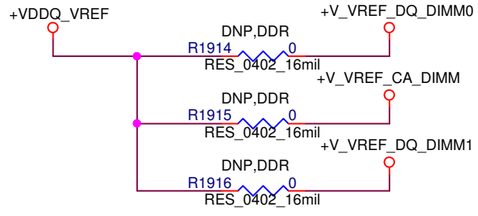
LPDDR3 Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

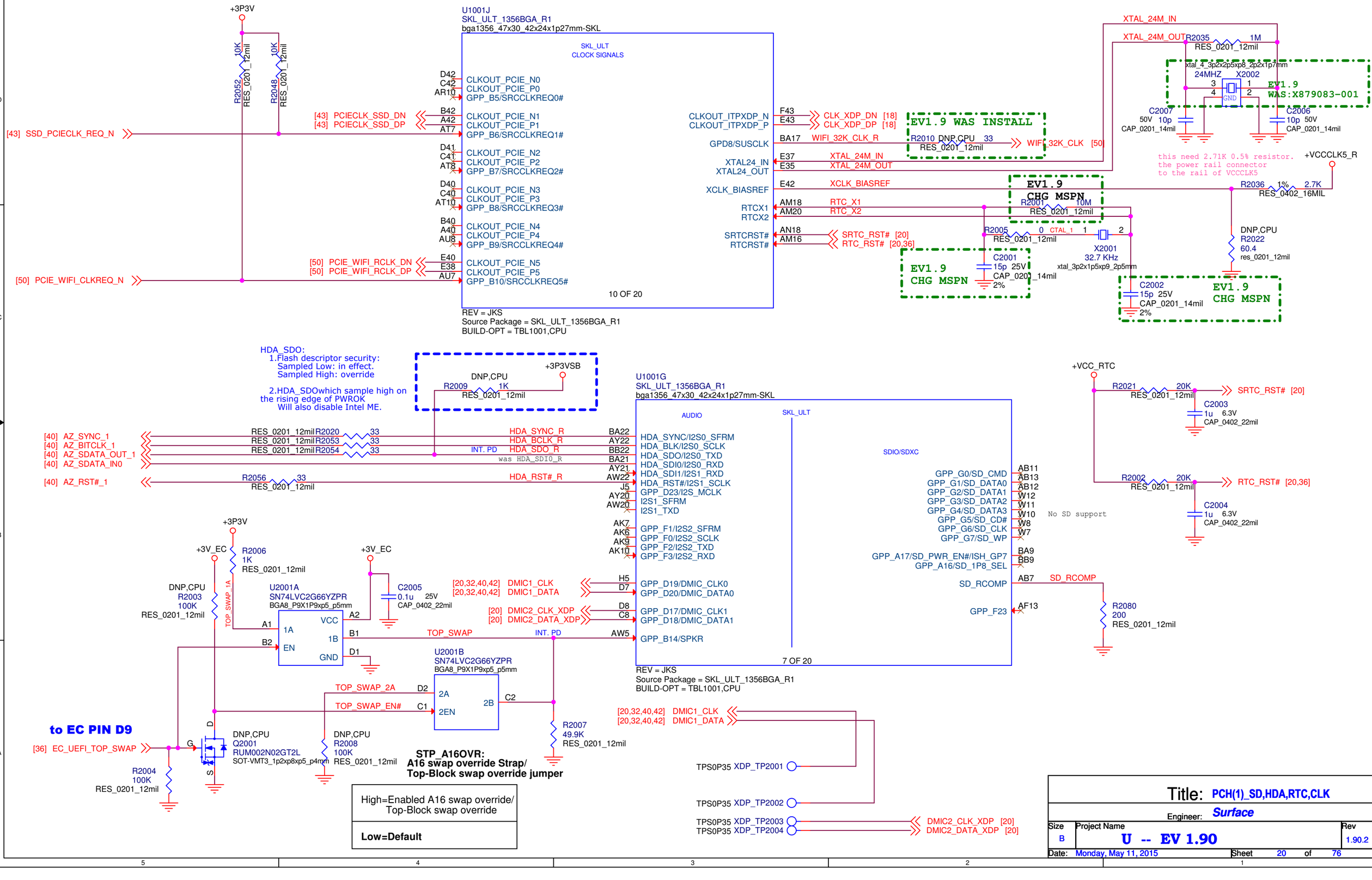




Intel 0203
M3+M1: Default Recommendation



Title:	LPDDR3(3)_CA/DQ Voltage		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 19 of 76		


+3P3V
R2052 10K RES_0201_12mil
R2048 10K RES_0201_12mil
[43] SSD_PCIECLK_REQ_N
[50] PCIE_WIFI_CLKREQ_N
U1001J
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
SKL_ULT
CLOCK SIGNALS
D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#
[43] PCIECLK_SSD_DN B42 CLKOUT_PCIE_N1
[43] PCIECLK_SSD_DP A42 CLKOUT_PCIE_P1
AT7 GPP_B6/SRCCLKREQ1#
D41 CLKOUT_PCIE_N2
C41 CLKOUT_PCIE_P2
AT8 GPP_B7/SRCCLKREQ2#
D40 CLKOUT_PCIE_N3
C40 CLKOUT_PCIE_P3
AT10 GPP_B8/SRCCLKREQ3#
B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
AU8 GPP_B9/SRCCLKREQ4#
[50] PCIE_WIFI_RCLK_DN E40 CLKOUT_PCIE_N5
[50] PCIE_WIFI_RCLK_DP E38 CLKOUT_PCIE_P5
AU7 GPP_B10/SRCCLKREQ5#
10 OF 20
REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU
CLKOUT_ITPXDP_N F43 CLK_XDP_DN [18]
CLKOUT_ITPXDP_P E43 CLK_XDP_DP [18]
GPD8/SUSCLK BA17 WIFI_32K_CLK_R
XTAL24_IN E37 XTAL_24M_IN
XTAL24_OUT E35 XTAL_24M_OUT
XCLK_BIASREF E42 XCLK_BIASREF
RTCX1 AM18 RTC_X1
RTCX2 AM20 RTC_X2
SRTCRST# AN18 SRTC_RST# [20]
RTCRST# AM16 RTC_RST# [20,36]
EV1.9 WAS INSTALL
R2010 DNP,CPU 33 RES_0201_12mil
WIFI_32K_CLK [50]
XTAL_24M_IN
XTAL_24M_OUT
R2035 1M RES_0201_12mil
xtal_4_3p2x2p5xp8_2p2x1p7mm
24MHZ X2002
EV1.9 WAS:X879083-001
C2007 50V 10p CAP_0201_14mil
C2006 10p 50V CAP_0201_14mil
this need 2.71K 0.5% resistor.
the power rail connector
to the rail of VCCCLK5
+VCCCLK5_R
R2036 1% 2.7K RES_0402_16MIL
EV1.9 CHG MSPN
R2001 10M RES_0201_12mil
R2005 0 CTAL_1 RES_0201_12mil
X2001 32.7 KHz xtal_3p2x1p5xp9_2p5mm
C2001 15p 25V CAP_0201_14mil 2%
C2002 15p 25V CAP_0201_14mil 2%
DNP,CPU R2022 60.4 res_0201_12mil
EV1.9 CHG MSPN
EV1.9 CHG MSPN
HDA_SDO:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.HDA_SDOwhich sample high on the rising edge of PWROK
Will also disable Intel ME.
+3P3VSB
DNP,CPU R2009 1K RES_0201_12mil
U1001G
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL
AUDIO
SKL_ULT
[40] AZ_SYNC_1 RES_0201_12mil R2020 33 HDA_SYNC_R BA22 HDA_SYNC/I2S0_SFRM
[40] AZ_BITCLK_1 RES_0201_12mil R2053 33 HDA_BCLK_R AY22 HDA_BLK/I2S0_SCLK
[40] AZ_SDATA_OUT_1 RES_0201_12mil R2054 33 INT. PD HDA_SDO_R BB22 HDA_SDO/I2S0_TXD
[40] AZ_SDATA_IN0 was HDA_SDI0_R BA21 HDA_SDI0/I2S0_RXD
AY21 HDA_SDI1/I2S1_RXD
[40] AZ_RST#_1 R2056 33 RES_0201_12mil HDA_RST#_R AW22 HDA_RST#/I2S1_SCLK
J5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD
AK7 GPP_F1/I2S2_SFRM
AK6 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD
H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0
D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1
AW5 GPP_B14/SPKR
7 OF 20
REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU
SDIO/SDXC
GPP_G0/SD_CMD AB11
GPP_G1/SD_DATA0 AB13
GPP_G2/SD_DATA1 AB12
GPP_G3/SD_DATA2 W12
GPP_G4/SD_DATA3 W11
GPP_G5/SD_CD# W10
GPP_G6/SD_CLK W8
GPP_G7/SD_WP W7
No SD support
GPP_A17/SD_PWR_EN#/ISH_GP7 BA9
GPP_A16/SD_1P8_SEL BB9
SD_RCOMP AB7
GPP_F23 AF13
SD_RCOMP
R2080 200 RES_0201_12mil
+VCC_RTC
R2021 20K RES_0201_12mil
SRTC_RST# [20]
C2003 1u 6.3V CAP_0402_22mil
R2002 20K RES_0201_12mil
RTC_RST# [20,36]
C2004 1u 6.3V CAP_0402_22mil
+3P3V
+3V_EC
R2006 1K RES_0201_12mil
DNP,CPU R2003 100K RES_0201_12mil
TOP_SWAP_1A
U2001A
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm
A1 1A
B2 EN
VCC A2
1B B1
GND D1
C2005 0.1u 25V CAP_0402_22mil
TOP_SWAP
INT. PD
U2001B
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm
TOP_SWAP_2A D2 2A
TOP_SWAP_EN# C1 2EN
2B C2
R2007 49.9K RES_0201_12mil
[20,32,40,42] DMIC1_CLK
[20,32,40,42] DMIC1_DATA
[20] DMIC2_CLK_XDP
[20] DMIC2_DATA_XDP
to EC PIN D9
[36] EC_UEFI_TOP_SWAP
DNP,CPU Q2001 RUM002N02GT2L SOT-VMT3_1p2xp8xp5_p4mm
R2004 100K RES_0201_12mil
DNP,CPU R2008 100K RES_0201_12mil
STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper
High=Enabled A16 swap override/ Top-Block swap override
Low=Default
TPS0P35 XDP_TP2001
TPS0P35 XDP_TP2002
TPS0P35 XDP_TP2003
TPS0P35 XDP_TP2004
DMIC2_CLK_XDP [20]
DMIC2_DATA_XDP [20]
Title: PCH(1)_SD,HDA,RTC,CLK
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 20 of 76

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

[18] XDP_SPI0_IO2
[18] SPI0_MOSI_XDP

R2133 1K RES_0201_12mil
R2134 1K RES_0201_12mil

Close to PCH

[37] SPI_CLK — R2136 15 — SPI_CLK_R — AV2
[37] SPI_SO — R2135 15 — SPI_SO_R — AW3
[37] SPI_SI — R2139 15 — SPI_SI_R — AV3
[37] SPI_WP_IO2 — R2137 15 — SPI_WP_IO2_R — AW2
[37] SPI_HOLD#_IO3 — R2138 15 RES_0201_12mil — SPI_HOLD#_IO3_R — AU4
[37] SPI_CS#0 — R2141 15 RES_0201_12mil — SPI_CS#0_R — AU3

EV1.9 ADD

[30] TS_SPI_CLK — R2109 15 RES_0201_12mil — TS_SPI_CLK_R — M2
[30] TS_SPI_MISO — R2105 15 RES_0201_12mil — TS_SPI_MISO_R — M3
[30] TS_SPI_MOSI — R2101 15 RES_0201_12mil — TS_SPI_MOSI_R — J4
[25,53,54] CAM_F_PWR_DN_N — R2111 DNP,CPU 330 res_0201_12mil — GPP_D21_R — V1
[25,53,54] CAM_R_PWR_DN_N — R2108 DNP,CPU 330 res_0201_12mil — GPP_D22_R — V2
[30] TS_SPI_CS_N — R2112 15 RES_0201_12mil — TS_SPI_CS_N_R — M1

[36] RC_IN# — AW13
DNP,CPU C2105 100p CAP_0201_14mil

AY11
+3P3V — R2132 8.2K res_0201_12mil
[36,38] PCH_SERIRQ — Serial Interrupt Request

U1001E
SKL_ULT_1356BGA_R1
PCB Footprint = bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT

SPI - FLASH
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#

SPI - TOUCH
GPP_D1/SPI1_CLK
GPP_D2/SPI1_MISO
GPP_D3/SPI1_MOSI
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS#

C LINK
G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

GPP_A0/RCIN#
GPP_A6/SERIRQ

5 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

SMBUS, SMLINK
1
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#

LPC
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#

+3P3VSB

R2102 1K RES 0201 12mil
R2103 1K RES 0201 12mil
R2107 1K RES 0201 12mil
R2110 1K RES 0201 12mil
R2104 1K RES 0201 12mil
R2106 1K RES 0201 12mil

R7
R8
R10 INT. PD — SMBALERT# — TP2101 — SP_TP_SMDp58mm
R9 — SML0CLK
W2 — SML0DAT
W1 INT. PD — was SMB0ALERT#
W3
V3
AM7 INT. PD — SMB1ALERT#

SMBCLK [18]
SMBDATA [18]
SD_CD#_PCH [48]
SML1_PCH_CLK [35]
SML1_PCH_DATA [35]

R2140 150K RES_0201_12mil — +3P3VSB

AY13 — LAD0 [36,38]
BA13 — LAD1 [36,38]
BB13 — LAD2 [36,38]
AY12 — LAD3 [36,38]
BA12
BA11 — SUS_STAT#_R — TP2128 — SP_TP_SMDp58mm — LFRAME# [36,38]

EV1.9
WAS 0402

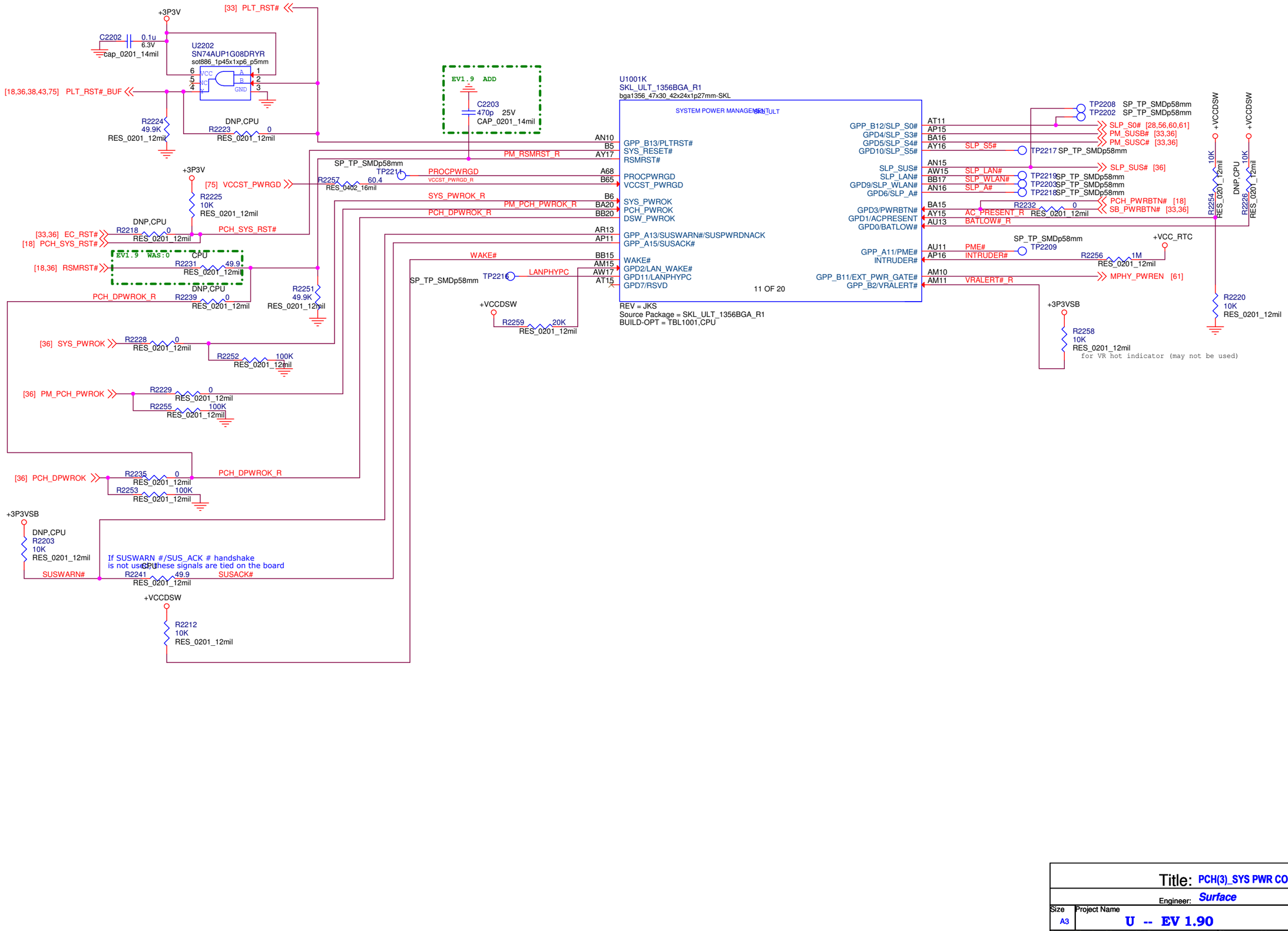
AW9 — CK_24M_EC_R — RES_0201_12mil — R2123 22 5% — CK_24M_EC [36]
AY9 — CK_24M_TPM_R — RES_0201_12mil — R2129 22 5% — CK_24M_TPM [38]
AW11

DNP,CPU C2103 10p 50V CAP_0201_14mil
DNP,CPU C2104 10p 50V CAP_0201_14mil

+3P3V — R2131 8.2K res_0201_12mil — PM_CLKRUN# [36,38]

GPP_C2/SMBALERT#	
0 **Default**	Disable ME crypto TLS
1	Enable ME crypto TLS

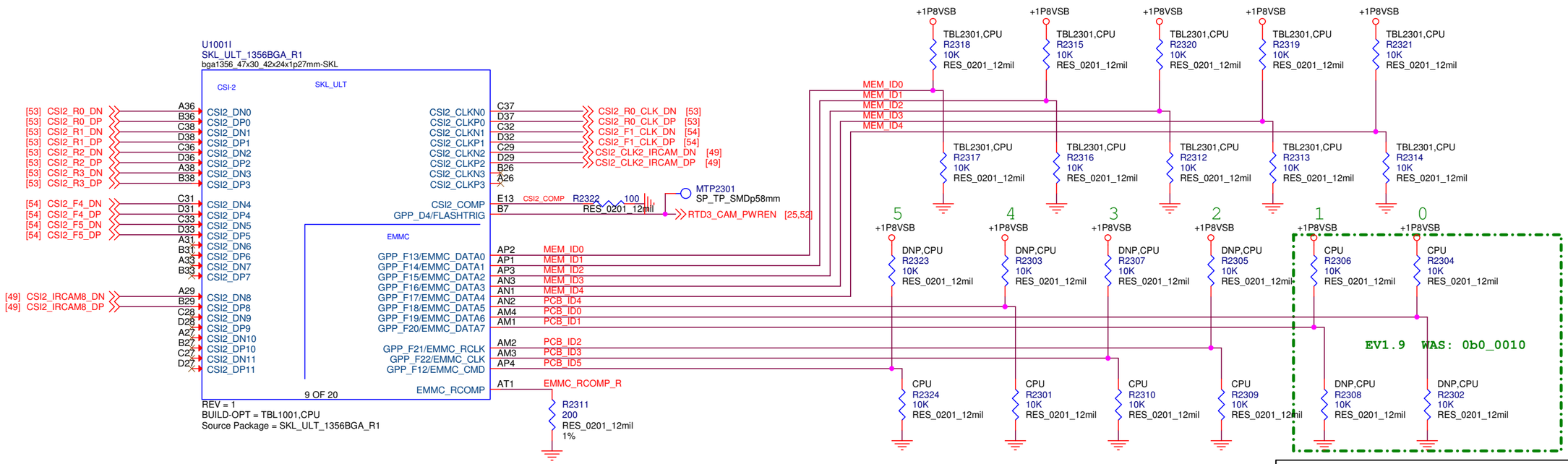
Title: PCH(2)_CLK,SMB,LPC,SPI
Engineer: Surface
Size: B | Project Name: U -- EV 1.90 | Rev: 1.90.2
Date: Monday, May 11, 2015 | Sheet 21 of 76



Title: PCH(3)_SYS PWR CONTR		
Engineer: Surface		
Size: A3	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 22 of 76	

Rev 4	EC Processor ID		PCH Processor ID	TPM			EC Board Rev	PCH Board ID[3:0]				DRAM Manufacturer		RAM Speed	RAM Size & Calibration		
Signal	EC_ID1	ED_ID0	PCB_ID5	PCB_ID4			R3619	PCB_ID3	PCB_ID2	PCB_ID1	PCB_ID0	MEM_ID1	MEM_ID0	MEM_ID4	MEM_ID3	MEM_ID2	ZQ1
	1 = R3642 0 = R3643	1 = R3640 0 = R3641	1 = R2323 0 = R2324	1 = R2303 0 = R2301	R3813 R3815 R3816	R3814		1 = R2307 0 = R2310	1 = R2305 0 = R2309	1 = R2306 0 = R2308	1 = R2304 0 = R2302	1 = R2315 0 = R2316	1 = R2318 0 = R2317	1 = R2321 0 = R2314	1 = R2319 0 = R2313	1 = R2320 0 = R2312	R1602 R1604 R1702 R1704
	U22 = 0 U23E = 1 Y = 0 S = 1	**U22 = 0 U23E=0 Y = 1 S = 1**	U = 0 Y = 1	Infineon = 0 Nation Z = 1	Infineon = DNP NationZ = POP	Infineon = POP NationZ =DNP						**Hynix = 0 Samsung = 0**	**Hynix = 0 Samsung = 1**	1600 LPDDR3 = 0 1866 LPDDR3 = 1	4GB = 0 8GB = 0 16GB = 1	4 GB = 0 8 GB = 1 16 GB = 0	4GB = DNP 8GB = POP 16GB = POP
EV 0.9							80.6 Ω	0	0	0	0						
EV 1.0							169 Ω	0	0	0	1						
EV 1.5							698 Ω	0	0	1	0						
EV 1.9							909 Ω	0	0	1	1						

TBL2301



Title: PCH(4)_CCI, HWID

Engineer: Surface

Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 23 of 76

U1001H
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT

PCIE/USB3/SATA

H13 PCIE1_RXN/USB3_5_RXN
G13 PCIE1_RXP/USB3_5_RXP
B17 PCIE1_TXN/USB3_5_TXN
A17 PCIE1_TXP/USB3_5_TXP

G11 PCIE2_RXN/USB3_6_RXN
F11 PCIE2_RXP/USB3_6_RXP
D16 PCIE2_TXN/USB3_6_TXN
C16 PCIE2_TXP/USB3_6_TXP

H16 PCIE3_RXN
G16 PCIE3_RXP
D17 PCIE3_TXN
C17 PCIE3_TXP

G15 PCIE4_RXN
F15 PCIE4_RXP
B19 PCIE4_TXN
A19 PCIE4_TXP

F16 PCIE5_RXN
E16 PCIE5_RXP
C19 PCIE5_TXN
D19 PCIE5_TXP

G18 PCIE6_RXN
F18 PCIE6_RXP
D20 PCIE6_TXN
C20 PCIE6_TXP

[43] PCIE_SSD_RX7_DN
[43] PCIE_SSD_RX7_DP
[43] PCIE_SSD_TX7_DN
[43] PCIE_SSD_TX7_DP
F20 PCIE7_RXN/SATA0_RXN
E20 PCIE7_RXP/SATA0_RXP
B21 PCIE7_TXN/SATA0_TXN
A21 PCIE7_TXP/SATA0_TXP

[43] PCIE_SSD_RX8_DN
[43] PCIE_SSD_RX8_DP
[43] PCIE_SSD_TX8_DN
[43] PCIE_SSD_TX8_DP
G21 PCIE8_RXN/SATA1A_RXN
F21 PCIE8_RXP/SATA1A_RXP
D21 PCIE8_TXN/SATA1A_TXN
C21 PCIE8_TXP/SATA1A_TXP

PCIE WIFI
[50] PCIE_WIFI_RX9_DN
[50] PCIE_WIFI_RX9_DP
[50] PCIE_WIFI_TX9_DN
[50] PCIE_WIFI_TX9_DP
E22 PCIE9_RXN
E23 PCIE9_RXP
B23 PCIE9_TXN
A23 PCIE9_TXP

F25 PCIE10_RXN
E25 PCIE10_RXP
D23 PCIE10_TXN
C23 PCIE10_TXP

SP_TP_SMDp58mm TP2417
SP_TP_SMDp58mm TP2418
PCIE_RCOMPN
R2401 100 PCIE_RCOMPP
RES_0201_12mil
F5 PCIE_RCOMPN
E5 PCIE_RCOMPP

[18] XDP_PRDY#
[18] XDP_PREQ#
D56 PROC_PRDY#
D61 PROC_PREQ#
TP2419 PIRQA# BB11 GPP_A7/PIRQA#
SP_TP_SMDp58mm

E28 PCIE11_RXN/SATA1B_RXN
E27 PCIE11_RXP/SATA1B_RXP
D24 PCIE11_TXN/SATA1B_TXN
C24 PCIE11_TXP/SATA1B_TXP
E30 PCIE12_RXN/SATA2_RXN
F30 PCIE12_RXP/SATA2_RXP
A25 PCIE12_TXN/SATA2_TXN
B25 PCIE12_TXP/SATA2_TXP

SSIC / USB3

H8 USB3_1_RXN
G8 USB3_1_RXP
C13 USB3_1_TXN
D13 USB3_1_TXP
USB3_CONN_RX_DN [45]
USB3_CONN_RX_DP [45]
USB3_CONN_TX_DN [45]
USB3_CONN_TX_DP [45]
USB Type A

J6 USB3_2_RXN/SSIC_1_RXN
H6 USB3_2_RXP/SSIC_1_RXP
B13 USB3_2_TXN/SSIC_1_TXN
A13 USB3_2_TXP/SSIC_1_TXP
USB3_SL1_RX_DN [71]
USB3_SL1_RX_DP [71]
USB3_SL1_TX_DN [71]
USB3_SL1_TX_DP [71]
USB SL1

J10 USB3_3_RXN/SSIC_2_RXN
H10 USB3_3_RXP/SSIC_2_RXP
B15 USB3_3_TXN/SSIC_2_TXN
A15 USB3_3_TXP/SSIC_2_TXP

E10 USB3_4_RXN
F10 USB3_4_RXP
C15 USB3_4_TXN
D15 USB3_4_TXP
USB3_SDXC_RX_DN [48]
USB3_SDXC_RX_DP [48]
USB3_SDXC_TX_DN [48]
USB3_SDXC_TX_DP [48]
USB3.0 SDXC

USB2

AB9 USB2N_1
AB10 USB2P_1
USB2_CONN_DN [45]
USB2_CONN_DP [45]
USB Type A

AD6 USB2N_2
AD7 USB2P_2
USB2_SL1_DN [71]
USB2_SL1_DP [71]
USB SL2

AH3 USB2N_3
AJ3 USB2P_3

AD9 USB2N_4
AD10 USB2P_4

AJ1 USB2N_5
AJ2 USB2P_5
USB2_BT_DN [50]
USB2_BT_DP [50]
BT

AF6 USB2N_6
AF7 USB2P_6

AH1 USB2N_7
AH2 USB2P_7
USB2_BLADE_DN [74]
USB2_BLADE_DP [74]
BLADE

AF8 USB2N_8
AF9 USB2P_8

AG1 USB2N_9
AG2 USB2P_9

AH7 USB2N_10
AH8 USB2P_10

AB6 USB2_COMP
AG3 USB2_ID
AG4 USB2_VBUSSENSE
USB2_COMP R2402 113 res_0201_12mil
GND

A9 GPP_E9/USB2_OC0#
C9 GPP_E10/USB2_OC1#
D9 GPP_E11/USB2_OC2#
B9 GPP_E12/USB2_OC3#
GPP_E10
GPP_E11
GPP_E12

J1 GPP_E4/DEVSLP0
J2 GPP_E5/DEVSLP1
J3 GPP_E6/DEVSLP2
GPP_E4
GPP_E5
GPP_E6

H2 GPP_E0/SATAXPCIE0/SATAGP0
H3 GPP_E1/SATAXPCIE1/SATAGP1
G4 GPP_E2/SATAXPCIE2/SATAGP2
GPP_E0
GPP_E1
GPP_E2

H1 GPP_E8/SATALED#
GPP_E8

+3VSUS_ORG
R2417 10K RES_0201_12mil DNP,CPU
R2418 10K RES_0201_12mil DNP,CPU
R2420 10K RES_0201_12mil DNP,CPU
R2419 10K RES_0201_12mil CPU
USB_CONN_OC# [45]

XDP_TP2400 TPS0P35
XDP_TP2401 TPS0P35
XDP_TP2402 TPS0P35
XDP_TP2403 TPS0P35
XDP_TP2404 TPS0P35
XDP_TP2405 TPS0P35
XDP_TP2406 TPS0P35
XDP_TP2407 TPS0P35
XDP_TP2408 TPS0P35
XDP_TP2409 TPS0P35
XDP_TP2410 TPS0P35

R2403 0 RES_0201_12mil DEVSLP_SSD [43]
R2409 0 RES_0201_12mil SSD_SATA_PCIE_DET_N [43]

8 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

Title: PCH(5)_PCIE,USB
Engineer: Surface
Size A3 | Project Name U -- EV 1.90 | Rev 1.90.2
Date: Monday, May 11, 2015 | Sheet 24 of 76

No reboot strap
Low: Disable (Default)
High:Enable

U1001F
SKL_ULT_1356BGA_R1
bga1356_47x30_42x24x1p27mm-SKL

SKL_ULT

LPSS

ISH

+3P3V
DNP,CPU R2543 1K RES_0201_12mil
SKL_NO_REBOOT
INT. PD

GPP_B15/GSPI0_CS# AN8
GPP_B16/GSPI0_CLK AP7
GPP_B17/GSPI0_MISO AP8
GPP_B18/GSPI0_MOSI AR7
GPP_B19/GSPI1_CS# AM5
GPP_B20/GSPI1_CLK AN7
GPP_B21/GSPI1_MISO AP5
GPP_B22/GSPI1_MOSI AN5

[31] PCH_SAM_INT
[25] BBS_BIT0
INT. PD

GPP_C8/UART0_RXD AB1
GPP_C9/UART0_TXD AB2
GPP_C10/UART0_RTS# W4
GPP_C11/UART0_CTS# AB3
GPP_C20/UART2_RXD AD1
GPP_C21/UART2_TXD AD2
GPP_C22/UART2_RTS# AD3
GPP_C23/UART2_CTS# AD4

[33,71] PCH_UART0_RXD
[33,71] PCH_UART0_TXD
[31,33] SWD_CLK
[31,33] SWD_DIO
DNP,CPU R2525 0 SWD_CLK_R
DNP,CPU R2526 0 SWD_DIO_R
RES_0201_12mil
RES_0201_12mil
EV19
WAS: INSTALL
[25,62,64] RTD3_AUD_PWR
[25,31] LID_CLOSED

+3P3V
RES_0201_12mil 499 R2589
RES_0201_12mil 499 R2590

TO SAM
[31,33] SH_I2C_SDA
[31,33] SH_I2C_SCL
GPP_C16/I2C0_SDA U7
GPP_C17/I2C0_SCL U6

[28] PMI_I2C_SDA
[28] PMI_I2C_SCL
GPP_C18/I2C1_SDA U8
GPP_C19/I2C1_SCL U9

[54] I2C_SDA_FCAM
[54] I2C_SCL_FCAM
R2522 0 RES_0201_12mil I2C_SDA_FCAM_R
R2523 0 RES_0201_12mil I2C_SCL_FCAM_R
GPP_F4/I2C2_SDA AH9
GPP_F5/I2C2_SCL AH10

[53] I2C_SDA_RCAM
[53] I2C_SCL_RCAM
R2520 0 RES_0201_12mil I2C_SDA_REAR_IR_CAM
R2521 0 RES_0201_12mil I2C_SCL_REAR_IR_CAM
GPP_F6/I2C3_SDA AH11
GPP_F7/I2C3_SCL AH12

[49] I2C_SDA_IRCAM
[49] I2C_SCL_IRCAM
0 R2527 RES_0201_12mil
0 R2528 RES_0201_12mil
GPP_F8/I2C4_SDA AF11
GPP_F9/I2C4_SCL AF12

I2C PU can be placed anywhere along the net

4.99K RES_0201_12mil R2504
4.99K RES_0201_12mil R2506
4.99K RES_0201_12mil R2507
4.99K RES_0201_12mil R2508

+1P8V_CAM_F
+1P8V_CAM_R

6 OF 20

REV = JKS
Source Package = SKL_ULT_1356BGA_R1
BUILD-OPT = TBL1001,CPU

GPP_D9 P2
GPP_D10 P3
GPP_D11 P4
GPP_D12 P1
TPANEL_RST#_R
RES_0201_12mil R2511 0
TPANEL_RST# [25,30]
RTD3_TPANEL_PWR [25,62,64]
CAM_R_XO_EN [25,53]
CAM_F_XO_EN [25,54]

GPP_D5/ISH_I2C0_SDA
GPP_D6/ISH_I2C0_SCL
res_0201_12mil MTP2531
M4 CAM_F_PWR_DN_N_R R2512 330
N3 CAM_R_PWR_DN_N_R R2513 CPU 330
res_0201_12mil MTP2530
CAM_F_PWR_DN_N [21,53,54]
CAM_R_PWR_DN_N [21,53,54]

GPP_D7/ISH_I2C1_SDA N1
GPP_D8/ISH_I2C1_SCL N2
CAM_IR_PWR_DN_N_R R2509 1K RES_0201_12mil
CAM_IRCAM_XO_EN [49]
CAM_IR_PWR_DN_N [49]
MTP2501 SP_TP_SMDp58mm

GPP_F10/I2C5_SDA/ISH_I2C2_SDA AD11
GPP_F11/I2C5_SCL/ISH_I2C2_SCL AD12
FLASH_PROTECT_N_R R2598 0 RES_0201_12mil
FLASH_PROTECT_N [30]

GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA U1
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL U2
GPP_D15/ISH_UART0_RTS# U3
GPP_D16/ISH_UART0_CTS#/SML0BALERT# U4
TS_BRD_REV[0] [25,30]
TS_BRD_REV[1] [25,30]
TCON_BRD_REV [25,57]
TCON_VENDOR_ID [25,57]

GPP_C12/UART1_RXD/ISH_UART1_RXD AC1
GPP_C13/UART1_TXD/ISH_UART1_TXD AC2
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AC3
GPP_C15/UART1_CTS#/ISH_UART1_CTS# AB4
was PCIE_GPU_PERST#
SL1_CONN [25,31]
SH_INT [25,31,33]
PCIE_WIFI_WAKE_N [25,50]
TP2514 SP_TP_SMDp58mm

GPP_A18/ISH_GP0 AY8
GPP_A19/ISH_GP1 BA8
GPP_A20/ISH_GP2 BB7
GPP_A21/ISH_GP3 BA7
GPP_A22/ISH_GP4 AY7
GPP_A23/ISH_GP5 AW7
GPP_A12/BM_BUSY#/ISH_GP6 AP13
PCIE_SSD_PERST#_R R2599 0 RES_0201_12mil
WLAN_PWD_N [25,50]
DISPLAY_OFF# [25,36,64]
PCIE_WIFI_DISABLE_N [25,50]
PCIE_WIFI_PERST_N [25,50]
WWAN_PWREN [25,65]
PCIE_SSD_PERST# [43]

TP2513 SP_TP_SMDp58mm
TP2521 SP_TP_SMDp58mm
TP2515 SP_TP_SMDp58mm
TP2516 SP_TP_SMDp58mm

EV1.9 SWAP
PCIE_WIFI_WAKE_N
and
DISPLAY_OFF#

[30] PCH_I2C1_SDA_TS
[30] PCH_I2C1_SCL_TS
+3VSUS_ORG

R2532 DNP,CPU 10K RES_0201_12mil
R2567 DNP,CPU 49.9K RES_0201_12mil PCIE_WIFI_DISABLE_N [25,50]
R2531 DNP,CPU 10K RES_0201_12mil
R2573 DNP,CPU 49.9K RES_0201_12mil PCIE_WIFI_PERST_N [25,50]
R2591 DNP,CPU 10K RES_0201_12mil SH_INT [25,31,33]
R2530 49.9K RES_0201_12mil
R2552 DNP,CPU 10K RES_0201_12mil RTD3_CAM_PWREN [23,52]
R2592 49.9K RES_0201_12mil
R2577 CPU 10K RES_0201_12mil PCIE_WIFI_WAKE_N [25,50]
R2535 DNP,CPU 49.9K RES_0201_12mil

RES_0201_12mil 1.21K R2586
RES_0201_12mil 1.21K R2587
+1P8V_TS

+1P8V
RES_0201_12mil R2560 49.9K TCON_BRD_REV [25,57]
RES_0201_12mil R2561 49.9K TCON_VENDOR_ID [25,57]
RES_0201_12mil R2562 49.9K TS_BRD_REV[0] [25,30]
RES_0201_12mil R2563 49.9K TS_BRD_REV[1] [25,30]

R2539 DNP,CPU 49.9K RES_0201_12mil DISPLAY_OFF# [25,36,64]
R2572 49.9K RES_0201_12mil WWAN_PWREN [25,65]
R2595 49.9K RES_0201_12mil RTD3_AUD_PWR [25,62,64]
R2559 49.9K RES_0201_12mil RTD3_TPANEL_PWR [25,62,64]
R2596 10K RES_0201_12mil TPANEL_RST# [25,30]
R2578 49.9K RES_0201_12mil LID_CLOSED [25,31]
R2502 49.9K RES_0201_12mil CAM_R_XO_EN [25,53]
R2503 49.9K RES_0201_12mil CAM_F_XO_EN [25,54]
R2548 49.9K RES_0201_12mil WLAN_PWD_N [25,50]
R2514 49.9K RES_0201_12mil SL1_CONN [25,31]

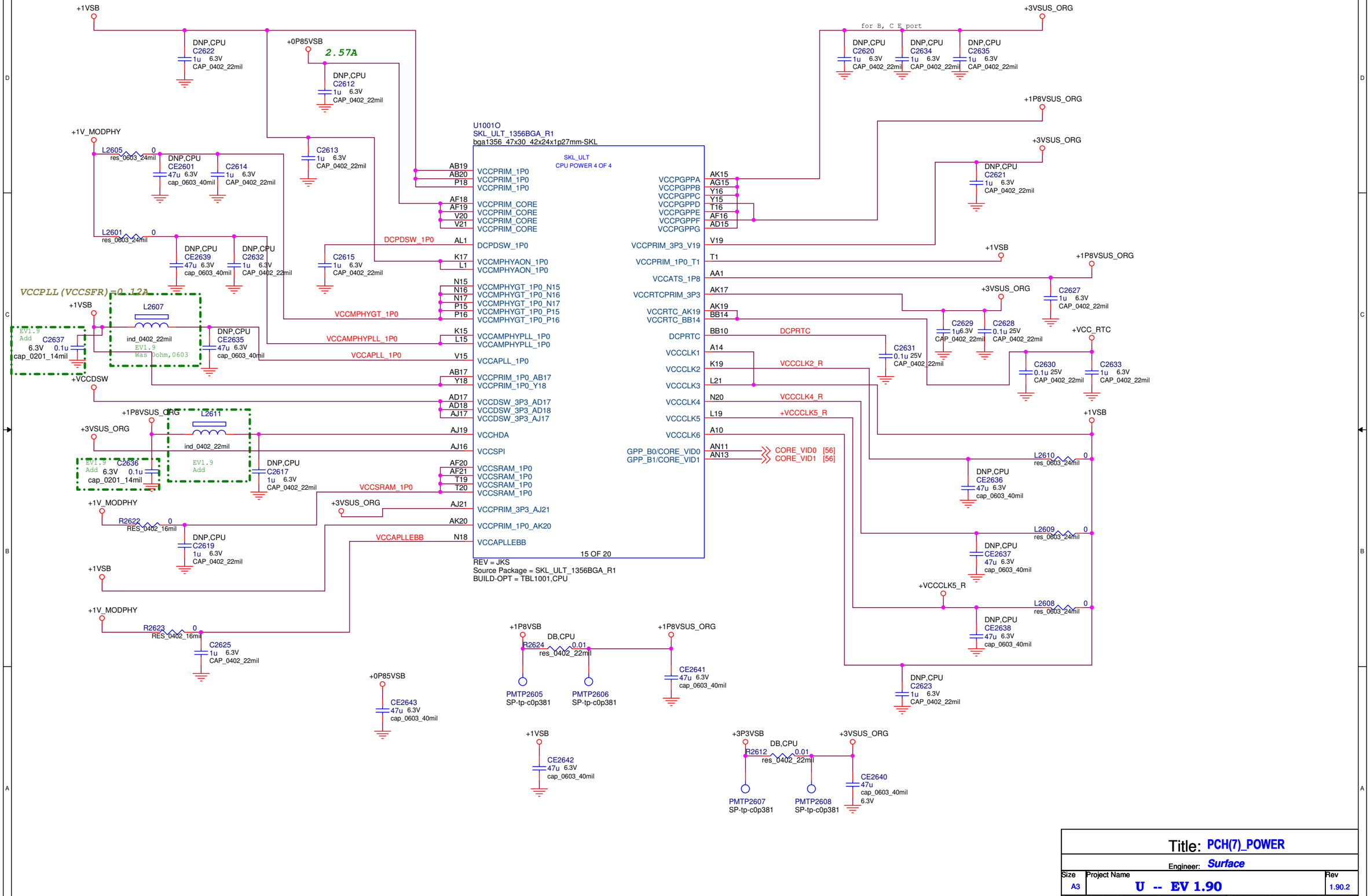
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

Boot BIOS Strap	
BBS_BIT0	Boot BIOS Location
1	LPC
0	SPI **(PCH)**

Sampled on rising edge of PWROK.

[25] BBS_BIT0
+3P3V
RES_0201_12mil R2501 DNP,CPU 10K
R2574 DNP,CPU 49.9K RES_0201_12mil

Title:	PCH(6)_CPU,GPIO,MISC		
Engineer:	*Surface*		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 25 of 76	



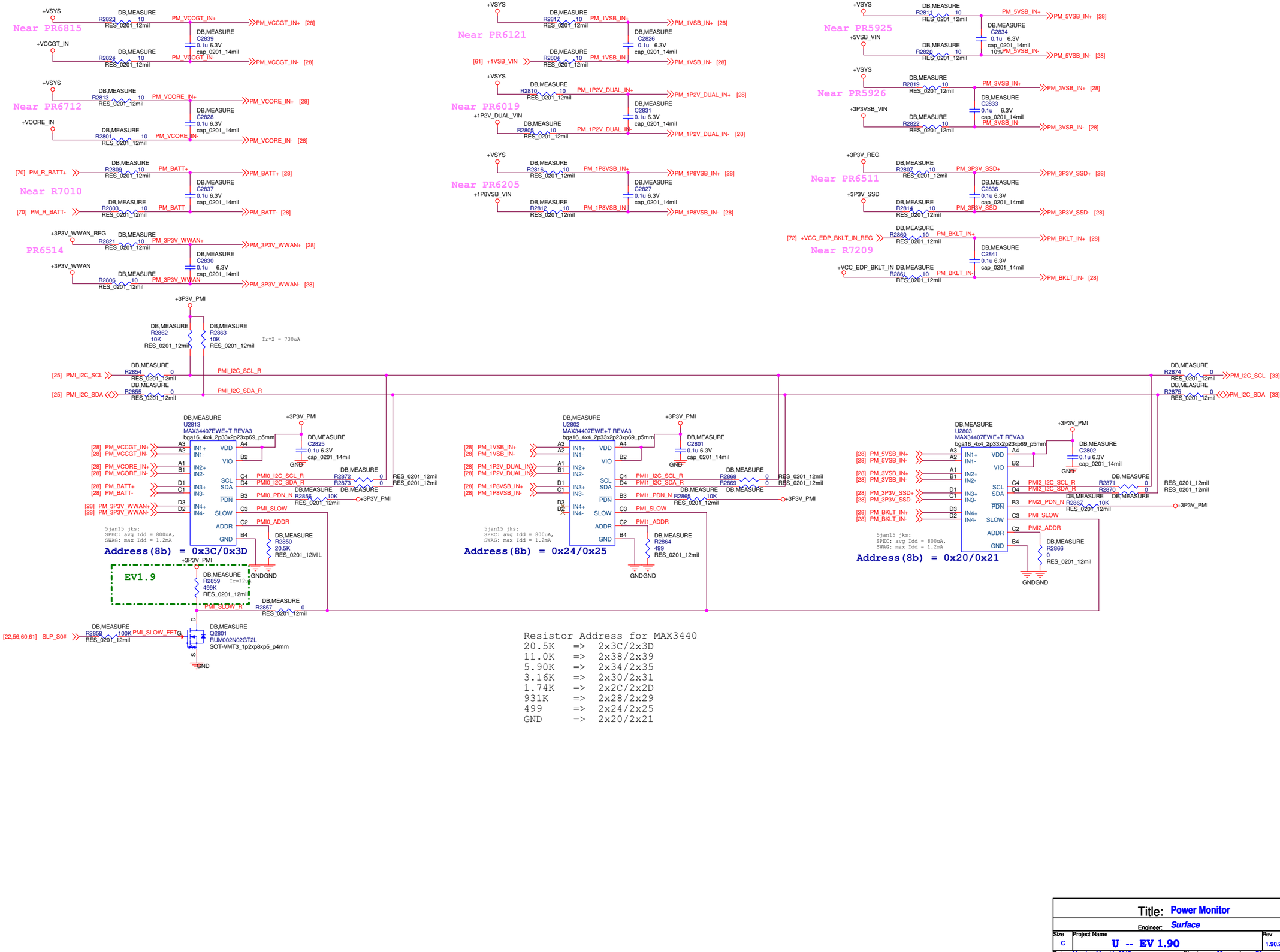
Title: PCH(7)_POWER

Engineer: Surface

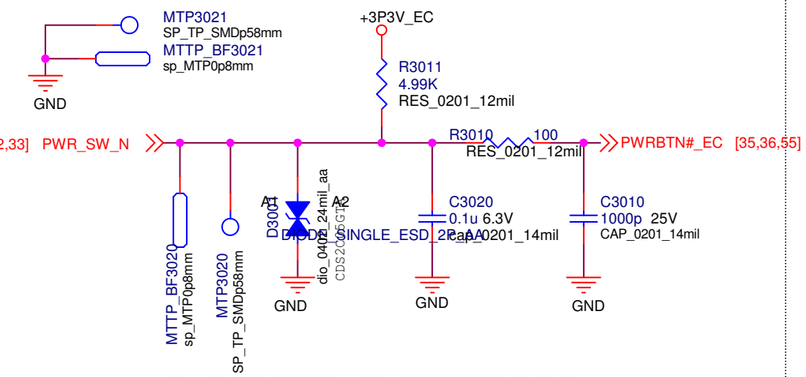
Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 26 of 76

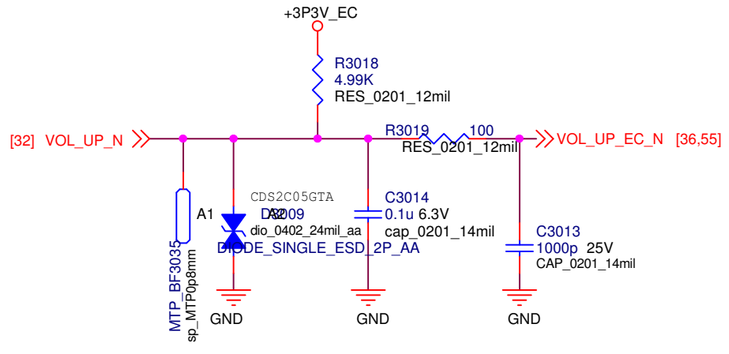
Title:	PCH(8)_empty
Engineer:	Surface
Size: B	Project Name: U -- EV 1.90
Rev:	1.90.2
Date:	Monday, May 11, 2015
Sheet	27 of 76


Near PR6815
Near PR6712
Near R7010
PR6514
Near PR6121
Near PR6019
Near PR6205
Near PR5925
Near PR5926
Near PR6511
Near R7209
EV1.9
Address(8b) = 0x3C/0x3D
Address(8b) = 0x24/0x25
Address(8b) = 0x20/0x21
Resistor Address for MAX3440
20.5K => 2x3C/2x3D
11.0K => 2x38/2x39
5.90K => 2x34/2x35
3.16K => 2x30/2x31
1.74K => 2x2C/2x2D
931K => 2x28/2x29
499 => 2x24/2x25
GND => 2x20/2x21
Title: Power Monitor
Engineer: Surface
Size C
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 28 of 76

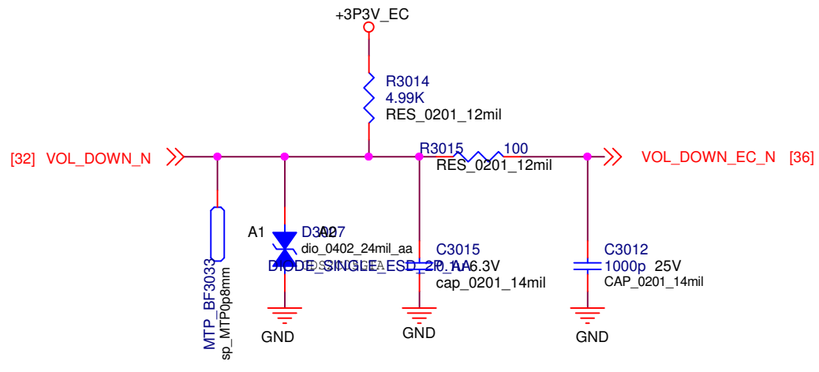
Title:	**EMPTY**
Engineer:	***Surface***
Size: B	Project Name: **U -- EV 1.90**
Rev:	1.90.2
Date:	Monday, May 11, 2015
Sheet	29 of 76



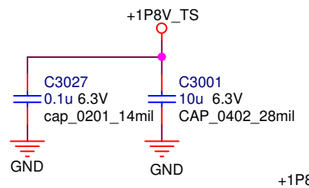
POWER BUTTON

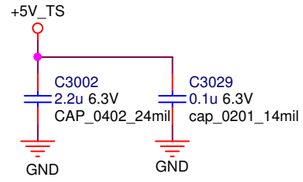


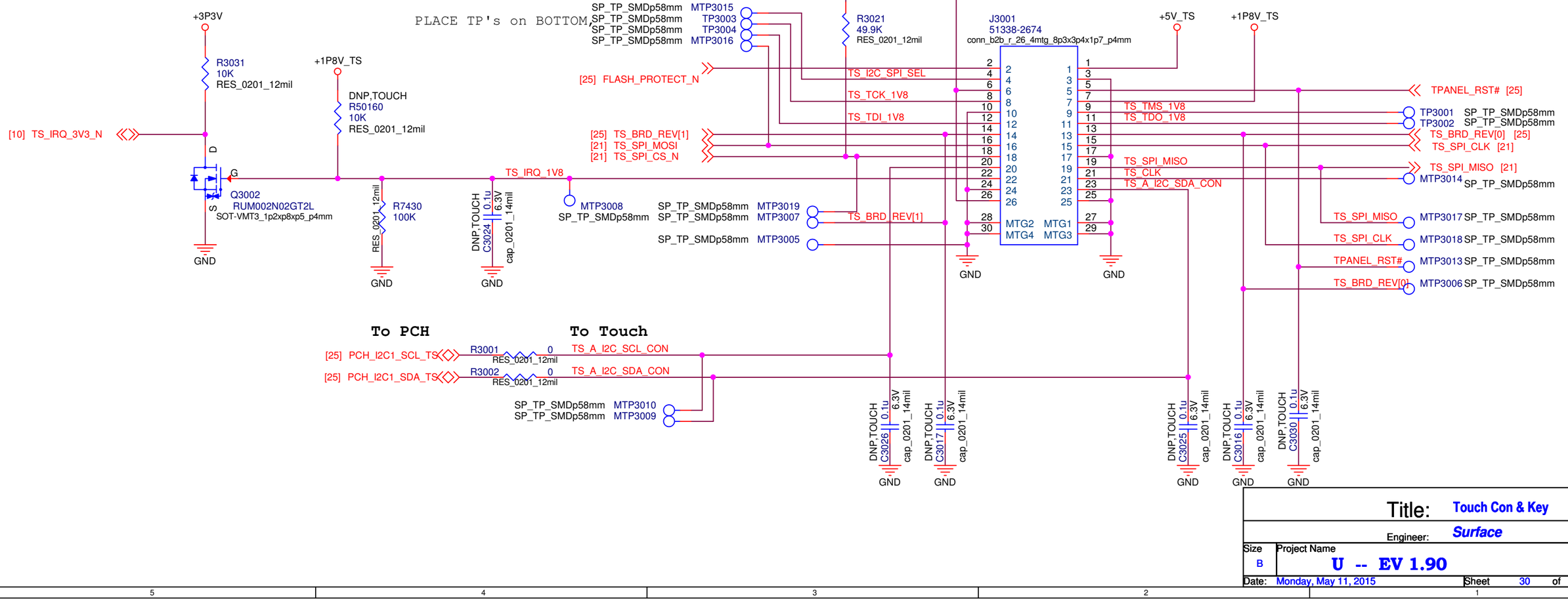
VOL_UP BUTTON



VOL_DOWN BUTTON







Title:	Touch Con & Key	
Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 30 of 76	

SENSOR MCU

Authentication

Address 0x28

+3P3VA
L3101 30 OHMS
IND_0603_38mil
1A
+1P8VA
Idda_adc<=1.7mA
R3172 0 RES_0402_16mil
VREFH
C3114 2.2u 6.3V CAP_0402_24mil
C3105 0.1u 6.3V cap_0201_14mil
GND
+3P3VA_F
C3110 10u 6.3V CAP_0402_28mil
C3107 0.1u 6.3V cap_0201_14mil
C3108 0.1u 6.3V cap_0201_14mil
C3109 0.1u 6.3V cap_0201_14mil
C3106 0.1u 6.3V cap_0201_14mil
GND
D3101 RB520CS3002L dio_sod882_1x6x6p5_p7mm 30V 200mA
+3P3VA
DNP,SENSOR
R3160 150K RES_0201_12mil
BLADE_AUTH_DATA [31,74]

U3105
MKL17Z256VMP4
bga64_8x8_5x5x1p23_p5mm

G4 VREFH
G3 VREFL
GND

VDD1 G7
VDD2 E4
VDDA F4

+3P3VA
R3104 4.99K RES_0201_12mil
HOST_AUTH_TXRX_R R3105 100 RES_0201_12mil
One Wire UART

[31] SAM_SPI_NPCS[0] → C3 PTD0
[70] SL1_ADC_RD_EN → A4 PTD1
[32] ALS_IRQ_N → C2 PTD2
HOST_AUTH_TXRX → B3 PTD3

U3102
ATECC108A-MAHUT-T
son9_3x2xp6_p5mm-2
8 VCC NC1
5 SDA NC2
6 SCL NC3
4 GND NC7
9
X906888-001
+3P3VA
C3130 0.1u 6.3V cap_0201_14mil
C3131 1u 6.3V CAP_0201_14mil
GND

SP_TP_SMDp58mm TP3146
R3179 100 RES_0201_12mil BLADE_DET_N
[31,74] BLADE_AUTH_DATA → A3 PTD4/LLWU_P14
[71] EC_PCH_DBG_EN → C1 PTD5
[74] BLADE_UART_RX → B2 PTD6/LLWU_P15
[74] BLADE_UART_TX → A2 PTD7

+3P3VA
R3103 200K RES_0201_12mil
[25,33] SH_INT
[25] SL1_CONN
SP_TP_SMDp58mm TP3126 → A1 PTE0 / B1 PTE1

SP_TP_SMDp58mm TP3116
[70] SL1_ADC → E1 PTE16
[31,33] SAM_SPI_SPCK → D1 PTE17
[31,33] SAM_SPI_MOSI → E2 PTE18
[31,33] SAM_SPI_MISO → D2 PTE19
R3143 33 SEN_MCU_UART_TXD_R → G1 PTE20
RES_0402_16mil
[33,71] SEN_MCU_UART_TXD
R3144 33 SEN_MCU_UART_RXD_R → F1 PTE21
RES_0402_16mil
[33,71] SEN_MCU_UART_RXD
[35] EC_SAM_I2C_SDA → G2 PTE22
[35] EC_SAM_I2C_SCL → F2 PTE23
SP_TP_SMDp58mm TP3152
SP_TP_SMDp58mm TP3153

+3P3VA
R3152 1K RES_0201_12mil
R3151 1K RES_0201_12mil
R3122 0 RES_0201_12mil
R3124 0 RES_0201_12mil
[31,32,33] I2C_SCL_MCU
[31,32,33] I2C_SDA_MCU
I2C_SCL_MCU_R → H4 PTE24
I2C_SDA_MCU_R → H5 PTE25

[31,32,33] I2C_SCL_MCU
[31,32,33] I2C_SDA_MCU
MTP3104 SP_TP_SMDp58mm
MTP3103 SP_TP_SMDp58mm

SP_TP_SMDp58mm TP3150
SP_TP_SMDp58mm TP3122
[73] BLADE_AUTH_PWR_EN → H1 PTE29
[70] SL1_UART_RX_SEL_N → H2 PTE30
H3 PTE31

[33,36] SAM_EC_INT
R3176 100K RES_0201_12mil
GND
SP_TP_SMDp58mm TP3139 → C5 NC

C4 VSS1
H7 VSS2
E3 VSS3
F3 VSSA
GND

SP_TP_SMDp58mm TP3144
MTP_BF3145 sp_MTP0p8mm
R3181 10K RES_0201_12mil
+3P3VA

PTA0 D3
PTA1 D4 BLADE_AUTH_RX — R3177 100 RES_0201_12mil → SWD_CLK [25,33]
PTA2 E5 BLADE_AUTH_TX — R3178 100 RES_0201_12mil

MTP_BF3154 sp_MTP0p8mm
PTA3 D5
PTA4 G5 SAM_BOOT_TRAP → SWD_DIO [25,33]
PTA5 F5 → LID_CLOSED [25]

RES_0201_12mil
R3182 1K
TP3137 SP_TP_SMDp58mm
PTA12 H6 → SL1_3P3V_DIS [72]
PTA13 G6 → SAR_CONV [32]
MTP3162 SP_TP_SMDp58mm

PTA18 H8
PTA19 G8 → SAM_X2_OUT
PTA20 F8

SAM_X2_IN R3171 10M RES_0201_12mil
R3112 0 RES_0402_16mil SAM_CTAL_1
32.7 KHz
xtal_3p2x1p5xp9_2p5mm
X3101
C3113 18p 25V CAP_0201_14mil
C3112 25V 18p CAP_0201_14mil
GND

+3P3VA
R3117 10K RES_0201_12mil
MTP_BF3102 sp_MTP0p8mm
SEN_MCU_NRST [33]
DNP,SENSOR
C3132 100p 25V CAP_0201_14mil
GND

TP3121 SP_TP_SMDp58mm
SP_TP_SMDp58mm MTP3149
R3173 100K RES_0201_12mil
GND
PTB0/LLWU_P5 F7 → PCH_SAM_INT [25]
PTB1 F6 → SENSORS_PWR_EN [65]
PTB2 E7 BLADE_UART_USB_N_R — R3180 1K RES_0201_12mil → BLADE_UART_USB_N [74]
PTB3 E8 → DBG_LED0 [33]
TP3101 SP_TP_SMDp58mm

TP3163 SP_TP_SMDp58mm
TP3120 SP_TP_SMDp58mm
PTB16 E6 SL1_UART_TX_SEL_R — R3113 0 RES_0201_12mil → SL1_UART_TX_SEL_N [70]
PTB17 D7 BLADE_+5V_KB_CONN_EN_R — R3183 0 RES_0201_12mil → BLADE_+5V_KB_CONN_EN [64]
PTB18 D6 SAR_INDICATION_2_R — R3107 0 RES_0201_12mil → SAR_INDICATION_2 [10]
PTB19 C7 was HINGER1_POS_A → SL1_5V_OC# [64]

TP3155 SP_TP_SMDp58mm
PTC0 D8 → SL1_5V_PWR_EN [64,70]
PTC1/LLWU_P6/RTC_CLKIN C6 → SH_I2C_SCL [25,33]
PTC2 B7 → SH_I2C_SDA [25,33]

PTC3/LLWU_P7 C8 SL1_UART_RX_R — R3115 100 RES_0201_12mil → SL1_UART_RX [33,70]
PTC4/LLWU_P8 B8 SL1_UART_TX_R — R3114 100 RES_0201_12mil → SL1_UART_TX [33,70]
PTC5/LLWU_P9 A8 SEN_HALL_INT_S_R — R3111 0 RES_0201_12mil → SEN_HALL_INT [32]
PTC6/LLWU_P10 A7 → EC_SAM_INT [33,36]
MTP3118 SP_TP_SMDp58mm

SP_TP_SMDp58mm TP3164
PTC9 B5 SAR_INDICATION_1_R — R3106 0 RES_0201_12mil → SAR_INDICATION_1 [10]
PTC8 A6 was HGR2_PWR_EN → TP3160 SP_TP_SMDp58mm
PTC7 B6 → SL1_BUF_EN [47,71]
TP3136 SP_TP_SMDp58mm

PTC10 B4 was HINGER2_POS_B → I2C_ADUX_MUX [32]
PTC11 A5 → AGYRO_INT1 [32]
TP3159 SP_TP_SMDp58mm

+3P3VA
R3102 0 RES_0402_16mil
R3125 10K RES_0201_12mil
C3119 0.1u 6.3V cap_0201_14mil
GND

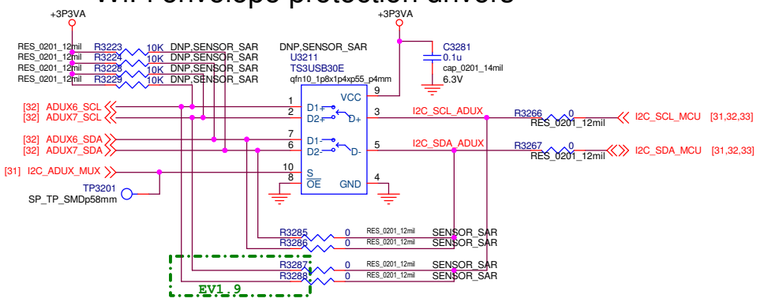
+3P3VA
R3127 10K RES_0201_12mil
R3126 10K RES_0201_12mil
[31] SAM_SPI_NPCS[0]
[31,33] SAM_SPI_MISO
FLASH_WP_N

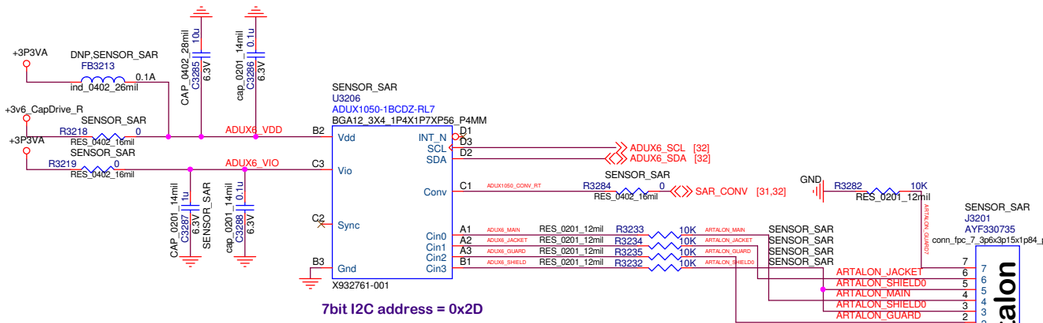
U3104
W25X40CLUXIG
son9_2x3xp6_p5mm
1 /CS
2 DO(IO1)
3 /WP
4 GND
9 GND_PAD
8 VCC
7 /HOLD
6 CLK
5 DI(IO0)
MSPN = X893206-001
GND

SAM_SPI_NPCS[0]
SAM_SPI_MISO
FLASH_WP_N
SAM_FLASH_VCC
SAM_HOLD#
SAM_SPI_SPCK
SAM_SPI_MOSI
SAM_SPI_SPCK [31,33]
SAM_SPI_MOSI [31,33]
SAM_HOLD# TP3130 SP_TP_SMDp58mm
TP3133 SP_TP_SMDp58mm
SAM_SPI_NPCS[0] TP3127 SP_TP_SMDp58mm
FLASH_WP_N TP3129 SP_TP_SMDp58mm

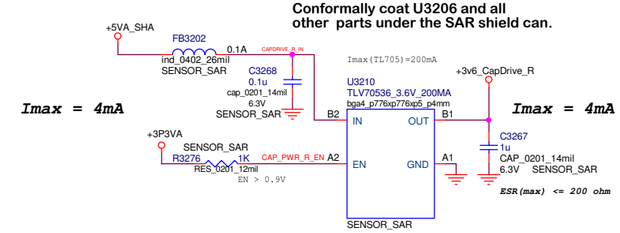
Title:	Sensor-uC	
Engineer:	Surface	
Size: B	Project Name	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 31 of 76	

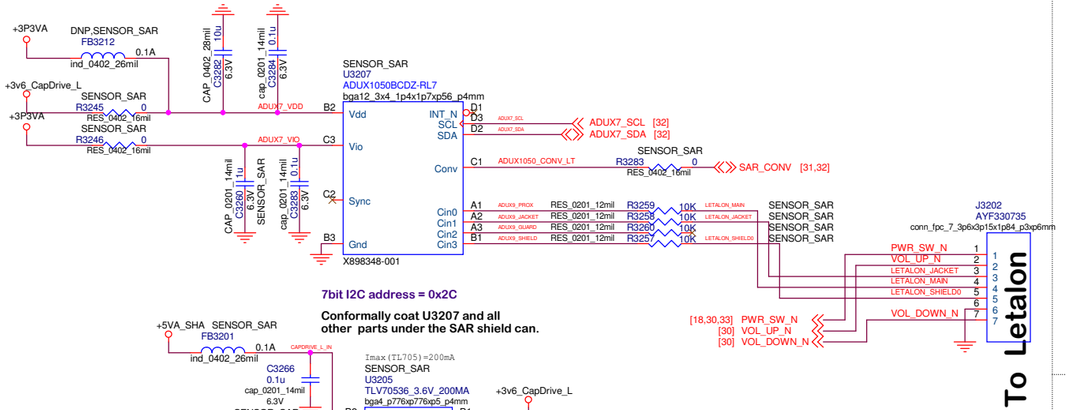
WiFi envelope protection drivers



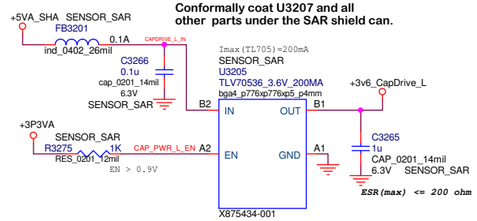


Conformally coat U3206 and all other parts under the SAR shield can.

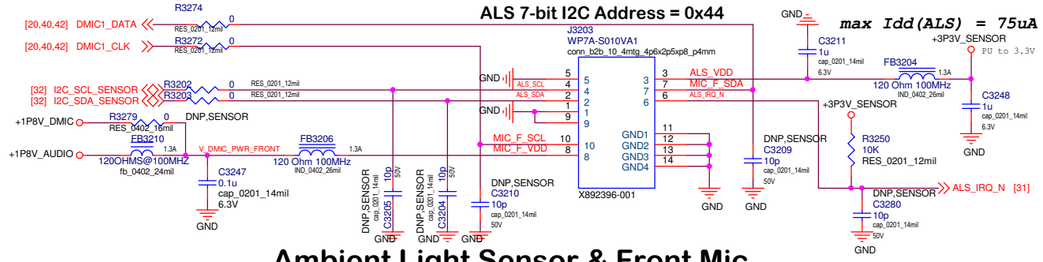




Conformally coat U3207 and all other parts under the SAR shield can.

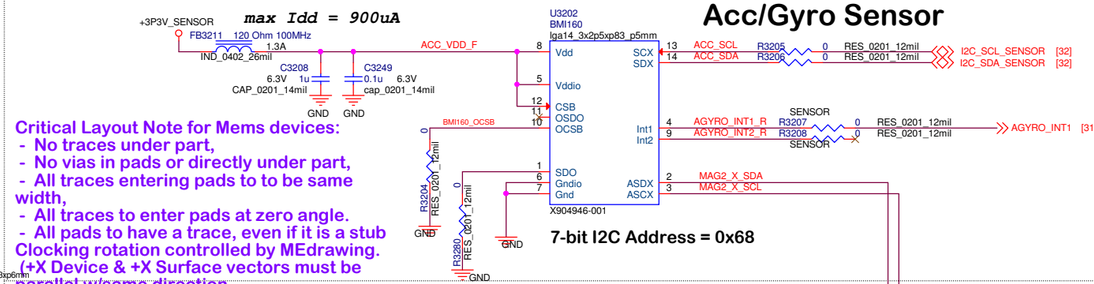


ALS 7-bit I2C Address = 0x44



Ambient Light Sensor & Front Mic

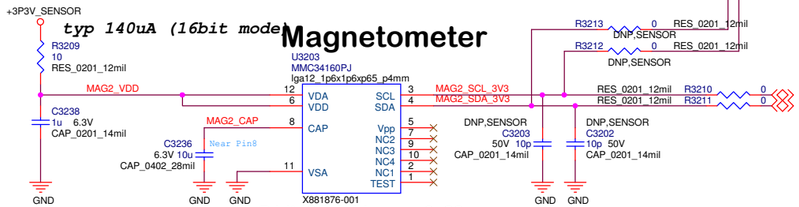
Acc/Gyro Sensor



Critical Layout Note for Mems devices:
- No traces under part,
- No vias in pads or directly under part,
- All traces entering pads to to be same width,
- All traces to enter pads at zero angle.
- All pads to have a trace, even if it is a stub

Clocking rotation controlled by MEdrawing. (+X Device & +X Surface vectors must be parallel w/same direction

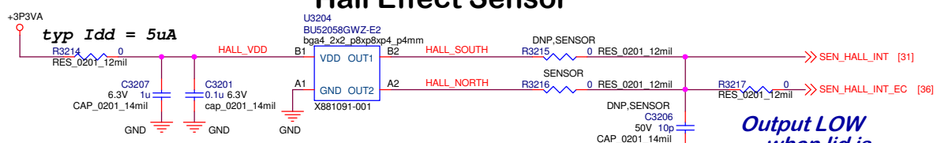
Magnetometer



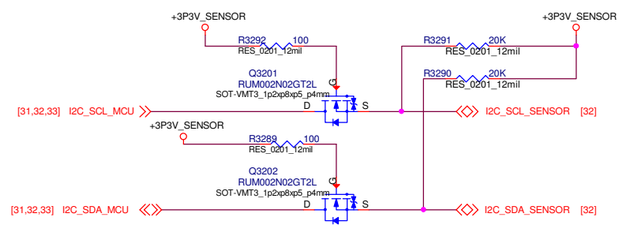
Critical Layout Note:
Extremely sensitive to ferrous materials:
Local ferrite bead to be >8mm remote
No traces carrying >8mA within 10mm ... on any layer.
Clocking rotation controlled by MEdrawing.

This change, putting the MAG behind the AGyro allows us to take advantage of the time-stamped FIFO in the AGyro to reduce power consumption and address load on the I2C bus -- in addition to improving jitter filtering in post processing. Eventually this will enable IR range camera frame syncing.

Hall Effect Sensor



Critical Layout Note:
Sensitive to ferrous materials
Do not mount under a steel shield can
If mounted on Glass side of board,
Trigger may occur
as early as 30Gauss North B-field
or as late as 50Gauss North B-field
Be careful not to mount within 15mm of speaker autofocus camera or other magnet.
X-Y location controlled by MEdrawing.



Title:	On Board-Sensors		
Engineer:	Surface		
Size: C	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 32 of 76	

DB,CONN
J3302
B2B 60P
X869110-001
conn_b2b-r_60_4mtg_14p2x2p54xp88_p4mm
RECEPTACLE

DEBUG CONN

[31,70] SL1_UART_RX
[31] SAM_SPI_MISO
[31] SAM_SPI_MOSI
[37] SPI1_CS#_DBG
[37] SPI1_CLK_DBG
[25,71] PCH_UART0_RXD
[37] SPI1_EXT
[35,36,63,70] SML1_EC_DATA
[35,36,63,70] SML1_EC_CLK
[37] SPI1_SO_DBG
[22,36] SB_PWRBTN#
[36] EC_GPC0
[35,36,39] SML3_EC_CLK
[35,36,39] SML3_EC_DATA
[25,31] SWD_CLK
[35,36] SML0_EC_DATA
[35,36] SML0_EC_CLK
[25,71] PCH_UART0_TXD
[31] SEN_MCU_NRST
[36,70] EC_SL1_PWR_EN
[36,73] EC_BLADE_PWR_EN
+5V_KB_CONN

SL1_UART_TX [31,70]
OT_RX_SEN_MCU_DEBUG [74]
PWR_SW_N [18,30,32]
EC_RST# [22,36]
SEN_MCU_UART_TXD [31,71]
SEN_MCU_UART_RXD [31,71]
OT_TX_SEN_MCU_DEBUG [74]
SPI1_SI_DBG [37]
PM_SUSC# [22,36]
SAM_EC_INT [31,36]
OT_SHA_DATA_TX [74]
EC_DBG_RxD [36,71]
EC_DBG_TxD [36,71]
SH_INT [25,31]
EC_SAM_INT [31,36]
OT_SHA_PWR_RX [74]
PM_SUSB# [22,36]
SAM_SPI_SPCK [31]
PLT_RST# [22]
SWD_DIO [25,31]
SH_I2C_SCL [25,31]
SH_I2C_SDA [25,31]
I2C_SCL_MCU [31,32]
I2C_SDA_MCU [31,32]

MTG1 MTG2 MTG3 MTG4

+3P3VA
DB,CONN
C3306
6.3V 0.1u
cap_0201_14mil
GND

+3P3V_EC
DB,CONN
C3307
0.1u 6.3V
cap_0201_14mil
GND

+3P3V_WWAN
DB,CONN
C3360
0.1u 6.3V
cap_0201_14mil
GND

EV1.9
new
+3P3V_PMI

DB,CONN
J3303
AYF532665
conn_fpc_26_4mtg_16x3p7x1p76_p5mm

Keyboard Connector(debug)
Power Monitor Conn.

MTG[2]
MTG[1]
NC28
NC27

[36] KSO0
[36] KSO1
[36] KSO2
[36] KSO3
[36] KSO4
[36] KSO5
[36] KSO6
[36] KSO7
[36] KSO8
[36] KSO9
[36] KSO10
[50] WIFI_TCK
[28] PM_I2C_SDA
[28] PM_I2C_SCL
[50] WIFI_TDI
[50] WIFI_TDO
[50] WIFI_TMS
[36] KSI0
[36] KSI1
[36] KSI2
[36] KSI3
[36] KSI4
[36] KSI5

GND GND

+3P3VA
EV1.9
DB,CONN
R3303
499
RES_0201_12mil
LED_G_A
DB,CONN
LED3303
Green
LED_0402_10mil
LED_G_K
DB,CONN
Q3303
RUM002N02GT2L
SOT-VMT3_1p2xp8xp5_p4mm
DBG_LED0 [31]
GND

[DBG_LED0]
Toggled whenever
SAM¡¦s software scheduler
is running

TOP

[EC DBG_LED]

+3P3V_EC
DB,CONN
R3301
1K
RES_0201_12mil
LED_R_A
DB,CONN
Red
led_2x1p2x1mm
LED3301
LED_R_K
DB,CONN
Q3301
RUM002N02GT2L
SOT-VMT3_1p2xp8xp5_p4mm
EC_HRTBT [36]
GND

[EC DBG_LED]

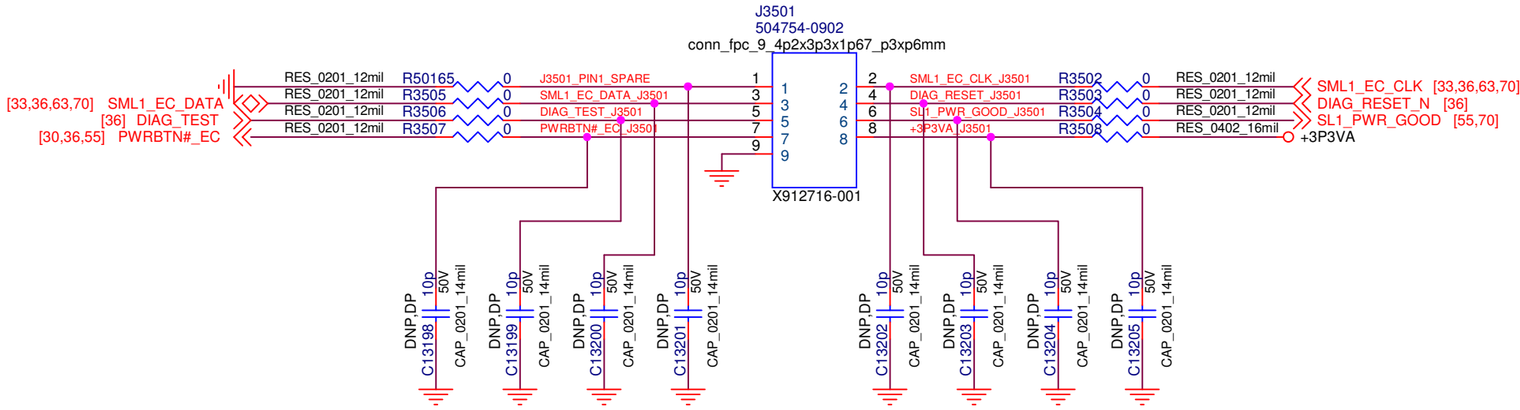
+3P3V_EC
DB,CONN
R3302
1K
RES_0201_12mil
LED_O_A
DB,CONN
Orange
led_0805_32mil
LED3302
LED_O_K
DB,CONN
Q3302
RUM002N02GT2L
SOT-VMT3_1p2xp8xp5_p4mm
EC_CODE [36]
GND

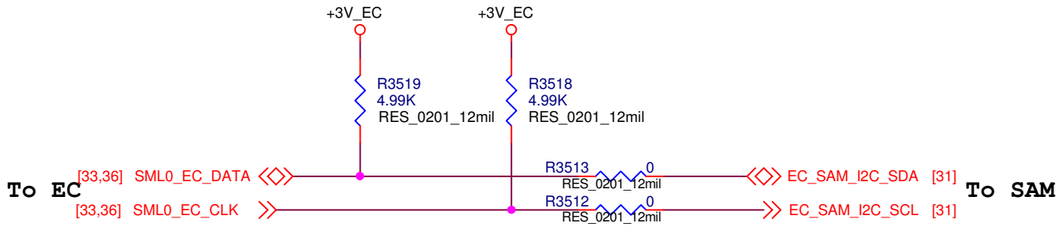
<Core Design>

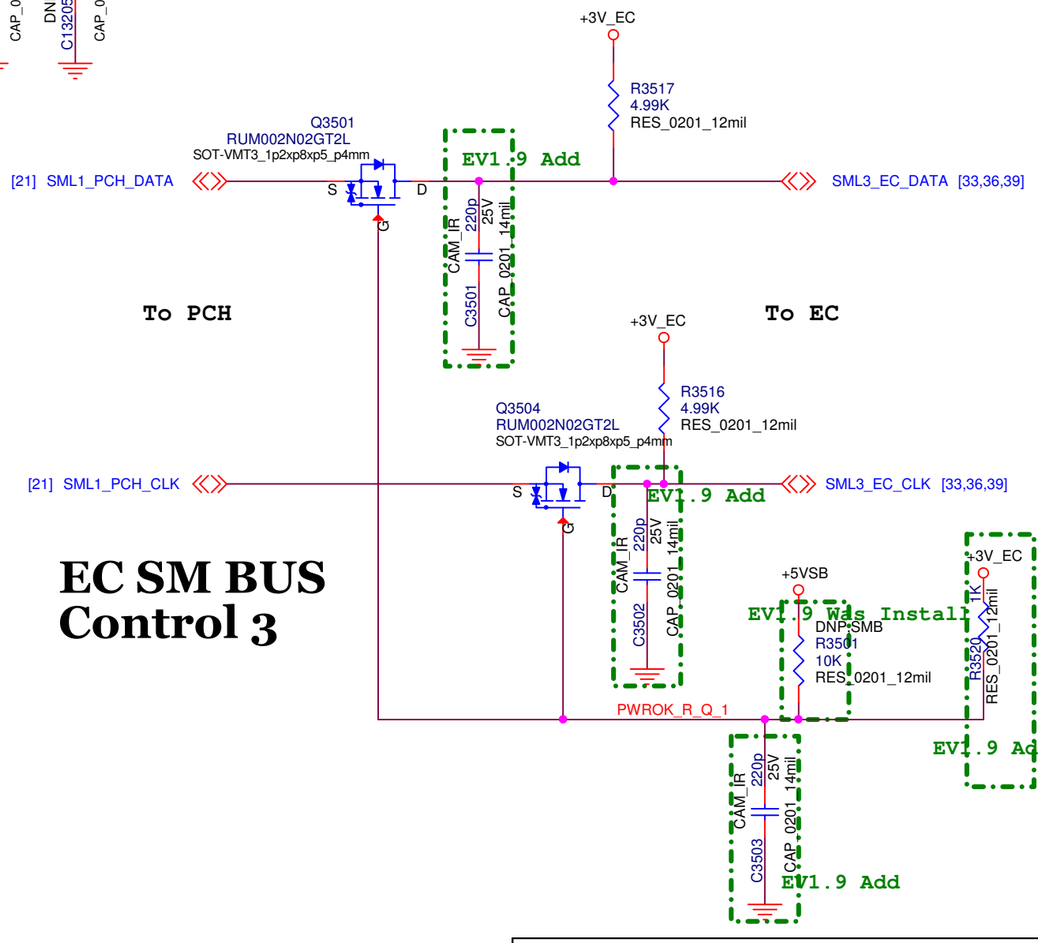
Title: Debug Conn / LPC
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 33 of 76

Title:	Empty			
Microsoft	Engineer:	Surface		
Size: A	Project Name: U -- EV 1.90			Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 34 of 76		

DIAGNOSTIC CONNECTOR







EC SM BUS Control 3

Title:	SM BUS/DIAG CONN		
Microsoft	Engineer: Surface		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 35 of 76		

Q3101
RUM002N02GT2L
SOT-VMT3_1p2x2p8xp5_p4mm

[36] RTCRST_CTRL
R3169 0 RES_0201_12mil
RTCRST_CTRL_R
R3167 100K RES_0201_12mil
RTC_RST# [20]
GND

+3V_EC
R3607 0 res_0603_24mil
+3V_EC_VBAT
DNP,EC R3618 res_0603_24mil
C3604 0.1u 6.3V cap_0201_14mil

+3P3V_EC
+3V_EC
R3606 0 res_0603_24mil
DNP,EC C3601 10u 6.3V CAP_0402_28mil
C3611 0.1u 6.3V cap_0201_14mil
C3609 0.1u 6.3V cap_0201_14mil
C3606 0.1u 6.3V cap_0201_14mil
C3607 0.1u 6.3V cap_0201_14mil
C3608 0.1u 6.3V cap_0201_14mil
C3602 10u 6.3V CAP_0402_28mil
C3610 0.1u 6.3V cap_0201_14mil
C3603 0.1u 6.3V cap_0201_14mil

U3601
IT8528VG/FX
bga128_13x13_7x7xp97_p5mm

J4 VBAT
K4 VSTBY4
K10 VSTBY5
E4 VSTBY(PLL)
D5 VSTBY3
D4 VSTBY2
D10 VSTBY1
E9 AVCC
J5 VCC

+3P3V
R3608 0 EC_VCC res_0603_24mil
C3612 0.1u 6.3V cap_0201_14mil

TP3605 SP_TP_SMDp58mm
TP3601 SP_TP_SMDp58mm
TP3602 SP_TP_SMDp58mm
TP3603 SP_TP_SMDp58mm
TP3604 SP_TP_SMDp58mm

[21,38] LAD0 — Func1 K1 LAD0/GPM0
[21,38] LAD1 — Func1 J2 LAD1/GPM1
[21,38] LAD2 — Func1 J1 LAD2/GPM2
[21,38] LAD3 — Func1 H2 LAD3/GPM3
[21] CK_24M_EC — Func1 K2 LPCCLK/GPM4
[21,38] LFRAME# — Func1 H1 LFRAME#/GPM5
[18,22,38,43,75] PLT_RST#_BUF — Func1 PU M4 LPCRST#/GPD2
[21,38] PCH_SERIRQ — (OD) Func1 G2 SERIRQ/GPM6
[10] EXT_SMI# — R3628 0 RES_0201_12mil — EXT_SMI#_R — (OD) GPI PU L2 ECSMI#/GPD4
[10] EXT_SCI# — R3629 0 RES_0201_12mil — EXT_SCI#_R — (OD) GPI PU N4 ECSCI#/GPD3
[25,64] DISPLAY_OFF# — R3602 0 RES_0201_12mil — CS_ENTRY#_R — GPO,L F1 GA20/GPB5
[21] RC_IN# — R3603 0 RES_0201_12mil — EC_GPB6 — GPO,L H4 KBRST#/GPB6
L1 WRST#

+3P3VO R3601 10K RES_0201_12mil
[22,33] EC_RST#

+3V_EC — R3627 100K RES_0201_12mil — D3601 RB520CS30202L dio_sod882_1xp6xp5_p7mm 30V 200mA
+3V_EC — K — A
[75] FORCE_OFF# — D3602 RB520CS3002L dio_sod882_1xp6xp5_p7mm 30V 200mA
C3605 1u 6.3V CAP_0201_14mil
GND

DNP,EC SC3603 100p 25V CAP_0201_14mil
DNP,EC SC3601 100p 25V CAP_0201_14mil
DNP,EC SC3602 100p 25V CAP_0201_14mil

[33] KSI0 — J12 KSI0/STB#
[33] KSI1 — J13 KSI1/AFD#
[33] KSI2 — J9 KSI2/INIT#
[33] KSI3 — H12 KSI3/SLIN#
[33] KSI4 — H9 KSI4
[33] KSI5 — H10 KSI5
H13 KSI6
G9 KSI7
[33] KSO0 — M8 KSO0/PD0
[33] KSO1 — J7 KSO1/PD1
[33] KSO2 — N9 KSO2/PD2
[33] KSO3 — M9 KSO3/PD3
[33] KSO4 — K8 KSO4/PD4
[33] KSO5 — J8 KSO5/PD5
[33] KSO6 — N10 KSO6/PD6
[33] KSO7 — M10 KSO7/PD7
[33] KSO8 — N11 KSO8/ACK#
[33] KSO9 — K9 KSO9/BUSY
[33] KSO10 — N12 KSO10/PE
N13 KSO11/ERR#
M13 KSO12/SLCT
L12 KSO13
L13 KSO14
K12 KSO15

NOTE: 40K <= PD(75K) <= 190K
GND R3635 100K RES_0201_12mil

[33] EC_GPC0 — GPI PD D1 CRX0/GPC0
[33] EC_CODE — GPI PD D2 CTX0/TMA0/GPB2

[36] BRD_ID_EN — GPI PU A11 PS2CLK0/TMB0/CEC/GPF0
GPI PU B11 PS2DAT0/TMB1/GPF1
CHARGER [63] EC_CHG_ACOK — GPI PU A10 PS2CLK1/DTR0#/GPF2
[63,70] EC_BATA_DET_N — GPI PU B10 PS2DAT1/RTS0#/GPF3
[20] EC_UEFI_TOP_SWAP — GPI PU D9 PS2CLK2/GPF4
B9 PS2DAT2/GPF5

[12/4] Remove TS_BRD_REV[0]

SAM [33,35] SML0_EC_CLK — (OD) GPI B4 SMCLK0/GPB3
[33,35] SML0_EC_DATA — (OD) GPI A2 SMDAT0/GPB4
CHARGER [33,35,63,70] SML1_EC_CLK — (OD) GPI B3 SMCLK1/GPC1
[33,35,63,70] SML1_EC_DATA — (OD) GPI B2 SMDAT1/GPC2
[10] H_PECI_R — R3626 43 RES_0402_16mil — H_PECI_EC — GPI PU C1 SMCLK2/PECI/GPF6
SMDAT2/PECIRQT#/GPF7

SAM [22,33] SB_PWRBTN# — GPI C12 DAC5/RIG0#/GPJ5
[31,33] SAM_EC_INT — GPI B13 DAC4/DCD0#/GPJ4
[31,33] EC_SAM_INT — GPI C13 DAC3/TACH1B/GPJ3
[12/4] Remove TCON_BRD_REV[0] — D12 DAC2/TACH0B/GPJ2
D13 HDIO3/GPJ1
[30,55] VOL_UP_EC_N — GPI E12 TACH2/HDIO2/GPJ0
GPI

DNP,EC R3630 100K RES_0201_12mil
GND
F2 CK32K/GPJ6
[12/4] Remove TCON_BRD_REV[1] — G1 CK32KE/GPJ7

[37] SCE#_EC — R3612 0 RES_0201_12mil — SCE#_EC_R — A7 FSCE#
[37] SCK_EC — R3611 0 RES_0201_12mil — SCK_EC_R — B5 FSCK
[37] SI_EC — R3610 0 RES_0201_12mil — SI_EC_R — B6 FMOSI
[37] SO_EC — R3609 0 RES_0201_12mil — SO_EC_R — A6 FMISO

7-bit I2C Address = 0x4E

Input Only

ADC0/GPI0 G10 GPI
ADC1/GPI1 G13 GPI
ADC2/GPI2 G12 GPI
ADC3/GPI3 F9 GPI
ADC4/GPI4 F13 GPI
ADC5/DCD1#/GPI5 F10 GPI (ADC)
ADC6/DSR1#/GPI6 F12 GPI
ADC7/CTS1#/GPI7 E13 GPI

+3P3V_EC
R3605 2.32K res_0201_12mil
EC_GPI0
EV1.9 was 698
TBL2301,EC R3619 909 RES_0402_16mil X807179-001
BRD_ID_EN_D
Q3601 RUM002N02GT2L SOT-VMT3_1p2x2p8xp5_p4mm
BRD_ID_EN [36]
GND

TP3612 SP_TP_SMDp58mm
TP3608 SP_TP_SMDp58mm
ALL_SUS_PWRGD [61,75] Check CRB time
ALL_SYS_PWRGD [58,66,75]
VRM_PWRGD [58,66,75]
VCCDSW_EN [55,76]
EC_ADP_IOUT [63]
EC_BAT_IOUT [63]
SLP_SUS# [22]
Charger

PWM0/GPA0 M5 PU GPI (GPO) jks 10nov: was EC_CTL
PWM1/GPA1 N5 PU GPI (GPO) — EC_MAG_DET [70]
PWM2/GPA2 M6 PU GPI (GPO)
PWM3/GPA3 N6 PU GPI (GPO)
PWM4/GPA4 K6 PU GPI (GPO) — EC_HRTBT [33]
PWM5/GPA5 J6 PU GPI — VOL_DOWN_EC_N [30]
PWM6/SSCK/GPA6 M7 PU GPI — CPUFAN1_PWM [39]
PWM7/RIG1#/GPA7 K7 PU GPI — DIAG_RESET_N [35]

DNP,EC C3615 0.1u 6.3V cap_0201_14mil
DNP,EC C3616 0.1u 6.3V cap_0201_14mil
DNP,EC C3617 0.1u 6.3V cap_0201_14mil
C3623 0.1u 6.3V cap_0201_14mil
C3620 0.1u 6.3V cap_0201_14mil
EC C3619 470p25V CAP_0201_14mil
EV1.9 install
GND

Debug UART to BLADE
RXD/SIN0/GPB0 A4 PU GPI — EC_DBG_RxD [33,71]
TXD/SOUT0/GPB1 A3 PU GPI — EC_DBG_TxD [33,71]
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7 A1 PD GPI (GPO) — RSMRST# [18,22]

PM_SUSC# [22,33]
EC C3622 470p 25V CAP_0201_14mil
EV1.9 install
GND

KSO16/SMOSI/GPC3 K13 PD GPI — DIAG_TEST [35]
TMRI0/GPC4 C2 PD GPI — EC_EXT_DC_OK [70]
KSO17/SMISO/GPC5 J10 PD GPI
TMRI1/GPC6 E1 PD GPI (GPO) — PM_PCH_PWROK [22]
PWUREQ#/BBO/SMCLK2ALT/GPC7 M2 PU GPI (GPO) — SYS_PWROK [22]

N1
RI1#/GPD0 N3 PU GPI
RI2#/GPD1 N7 PU GPI — EC_ID0
GINT/CTS0#/GPD5 M11 PD GPI — CPUFAN1_TACH [39]
TACH0A/GPD6 M12 — EC_ID1
TACH1A/TMA1/GPD7
[12/4] Remove TS_BRD_REV[1]
TP3611 SP_TP_SMDp58mm
TP3607 SP_TP_SMDp58mm

DNP,TBL2301,EC R3640 10K RES_0201_12mil
TBL2301,EC R3641 10K RES_0201_12mil
DNP,TBL2301,EC R3642 10K RES_0201_12mil
TBL2301,EC R3643 10K RES_0201_12mil
+3V_EC
GND
to configure EC_ID[1:0], see TBL2301

L80HLAT/BAO/GPE0 N2 PD GPI (GPO)
EGAD/GPE1 A13 PD GPI (GPO)
EGCS#/GPE2 A12 PD GPI (GPO)
EGCLK/GPE3 B12 PD GPI (GPO) — VSUS_ON [56,59,61,62]
PWRSW/GPE4 E2 PU GPI — MCU_PWRBTN#_R R3634 0 RES_0201_12mil — SEN_HALL_INT_EC [32] — PWRBTN# [30,35,55]
RTS1#/GPE5 N8 PD GPI (GPO)
LPCPD#/GPE6 M1 PD GPI (GPO) — PCH_DPWROK [22]
L80LLAT/GPE7 M3 PU GPI — EC_EXT_DCIN_EN [70]
Charger

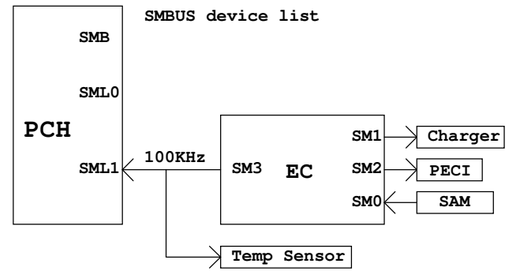
SUSC_EC# [45,60,61,62]
SUSB_EC# AND [36]
TP3610 SP_TP_SMDp58mm
EV1.9
R3639 100K RES_0201_12mil
R3638 100K RES_0201_12mil
GND

SSCE1#/FSCE1#/GPG0 E6 GPO,H
FDIO2/DTR1#/SBUSY/GPG1/ID7 A5 PD GPO(GPI)
SSCE#/GPG2 E7 GPI (GPO) — EC_PROCHOT [10]
FDIO3/DSR0#/GPG6 D6 GPI
PM_SUSB# [22,33,36]
EC SC3605 470p 25V CAP_0201_14mil
GND
EV1.9 WAS:DNP

CLKRUN#/GPH0/ID0 D8 PD GPI (OD) — PM_CLKRUN# [21,38]
CRX1/SIN1/SMCLK3/GPH1/ID1 E8 PD GPI (OD) — SML9_EC_CLK [33,35,39]
CTX1/SOUT1/SMDAT3/GPH2/ID2 D7 PD GPI (OD) — SML9_EC_DATA [33,35,39]
HSCE#/GPH3/ID3 A9 PD GPI — RTCRST_CTRL [36]
HSCK/GPH4/ID4 B8 PD GPI — EC_BLADE_5VLDSW_EN [73]
HMISO/GPH5/ID5 A8 PD GPI (GPO) — EC_BLADE_PWR_EN [33,73]
HMOSI/GPH6/ID6 B7 PD GPI (GPO) — EC_SL1_PWR_EN [33,70]
TEMP SENSOR

PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPG0, GPG2 AND GPG6 (Reserved hardware strapping).

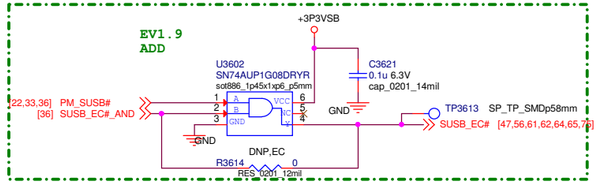
SMBUS device list



VSS2 F4
VCORE K5
VSS3 F5
VSS1 E5
VSS4 G4
VSS6 H5
VSS5 G5
AVSS E10
GND GND

EC_VCORE
C3613 0.1u 6.3V cap_0201_14mil
DNP,EC C3614 1u 6.3V CAP_0201_14mil
DNP,EC R3613 0 RES_0402_16mil
GND

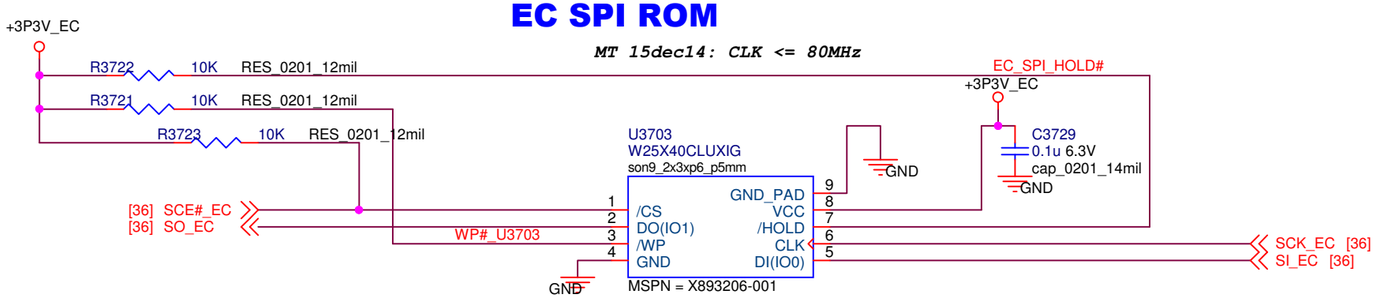
EV1.9 ADD



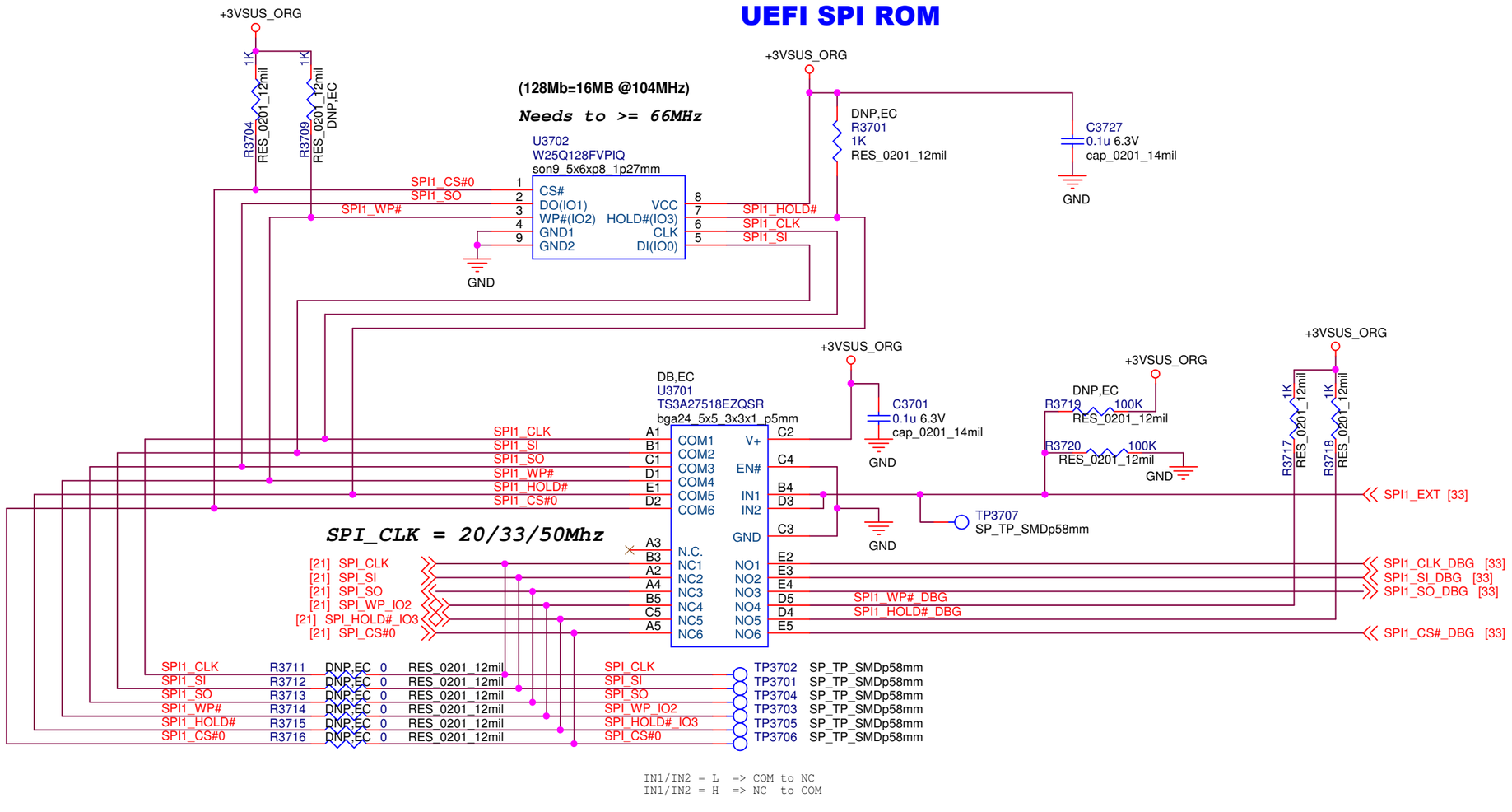
Title: EC-ITE 8528VG-1
Microsoft Engineer: Surface
Size C | Project Name U -- EV 1.90 | Rev 1.90.2
Date: Monday, May 11, 2015 Sheet 36 of 76

EC SPI ROM

MT 15dec14: CLK <= 80MHz

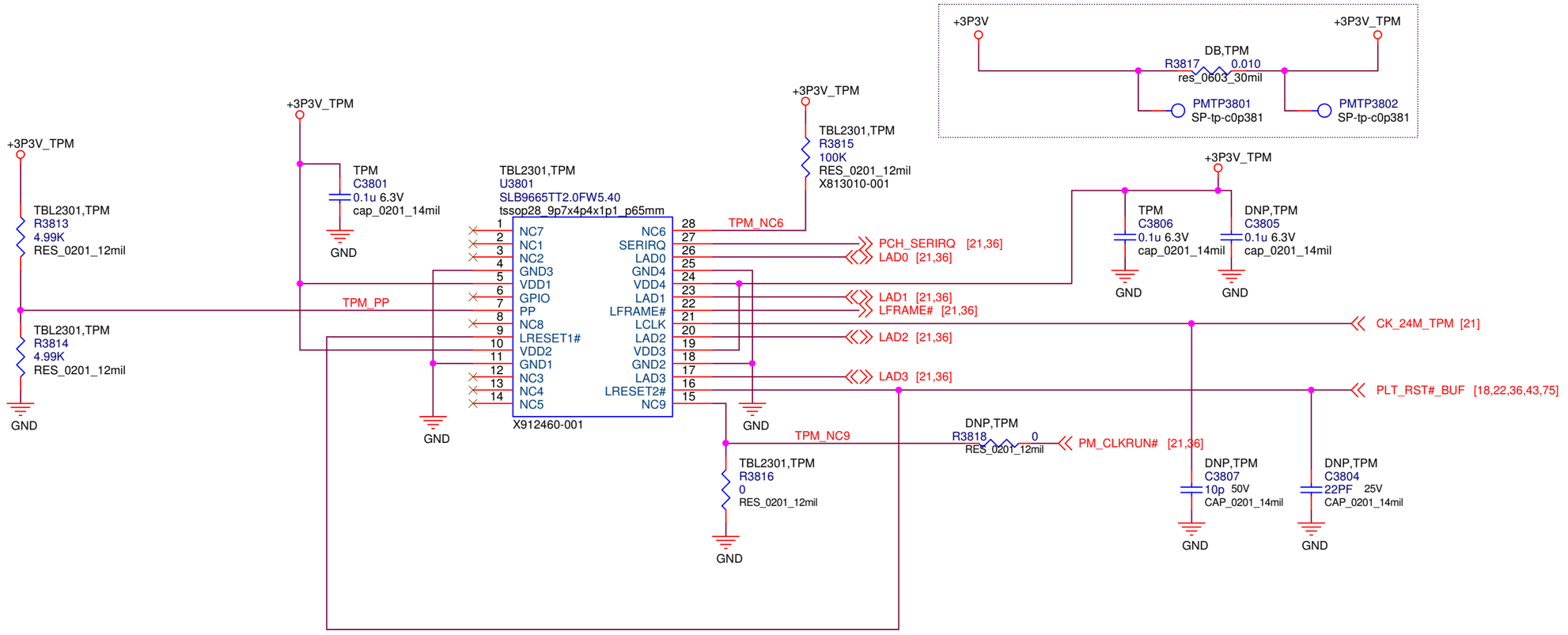


UEFI SPI ROM



Title:	EC-ITE 8528VG-2/SPI ROM	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 37 of 76	

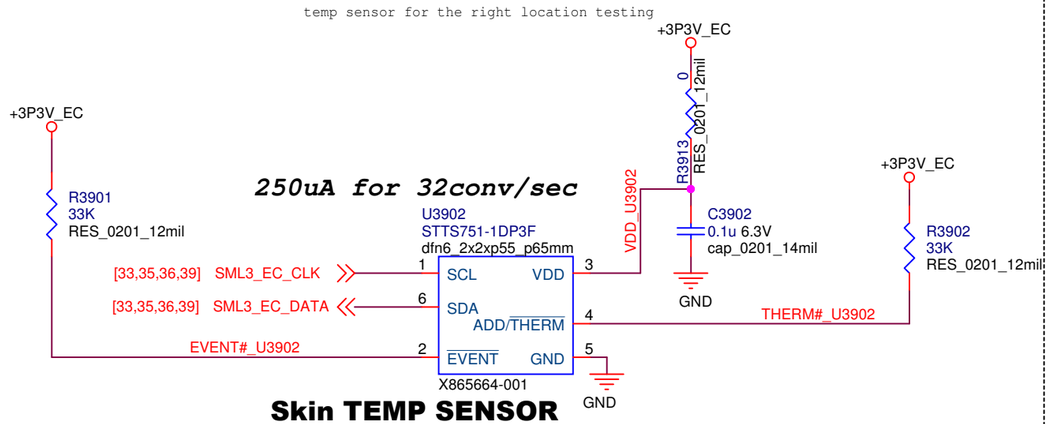
Trusted Platform Module

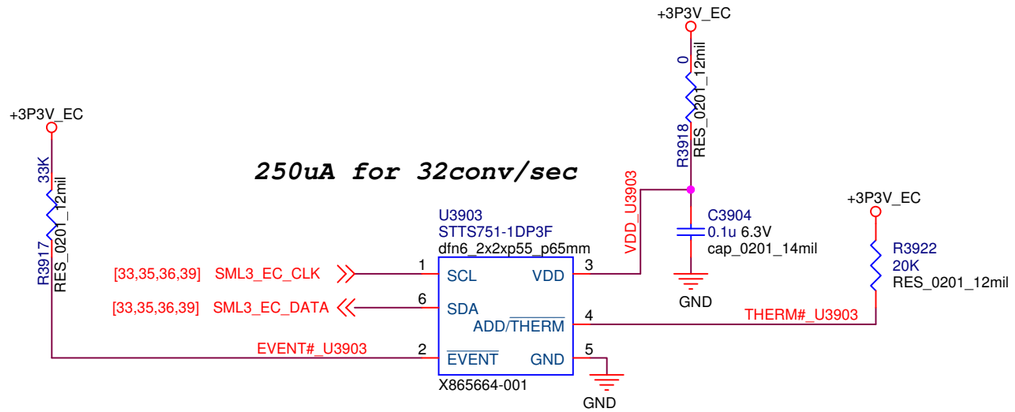


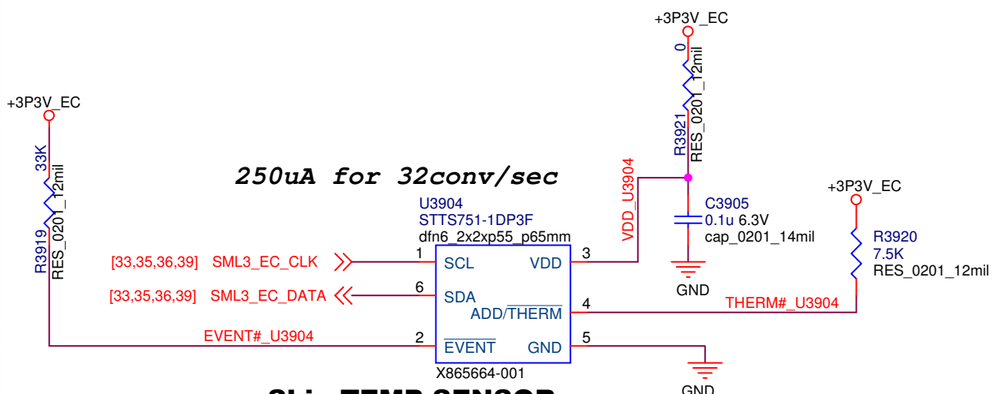
Title: TPM		
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 38 of 76	

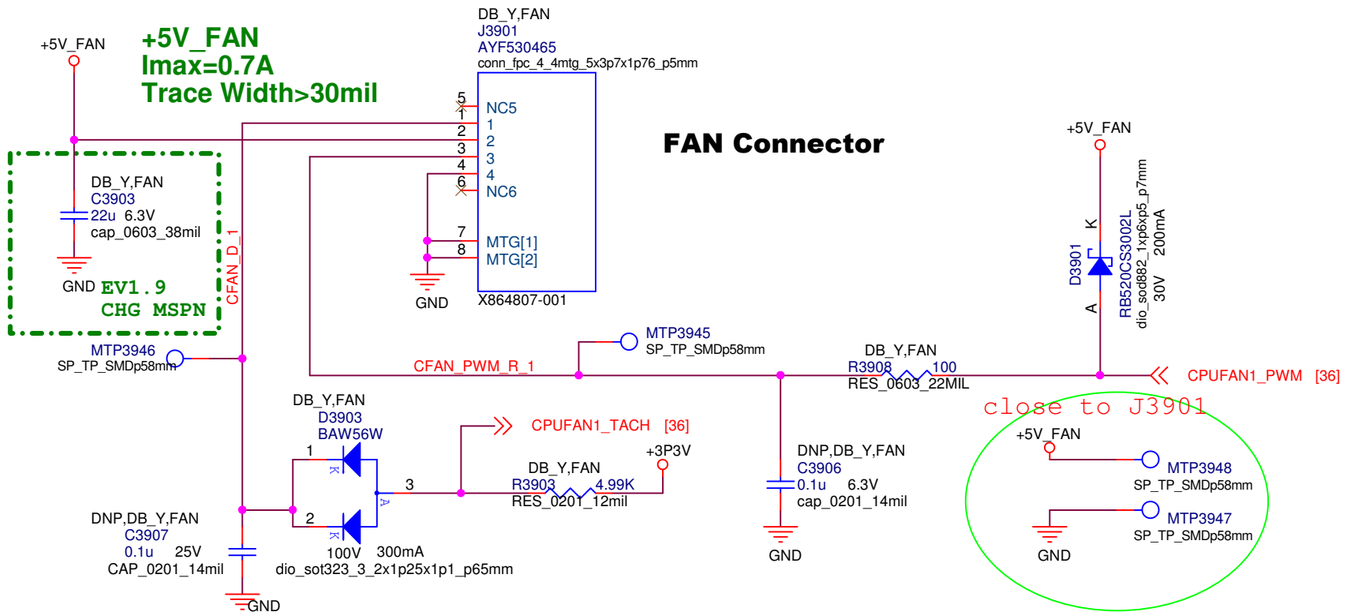
jks 6dec14: Only one sensor will be used for final product

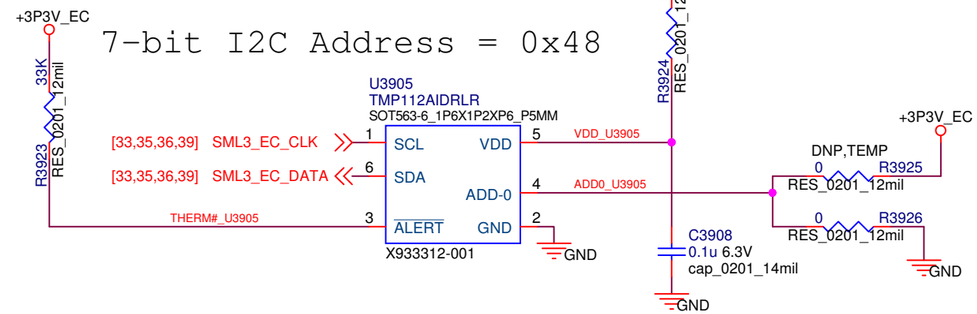
temp sensor for the right location testing

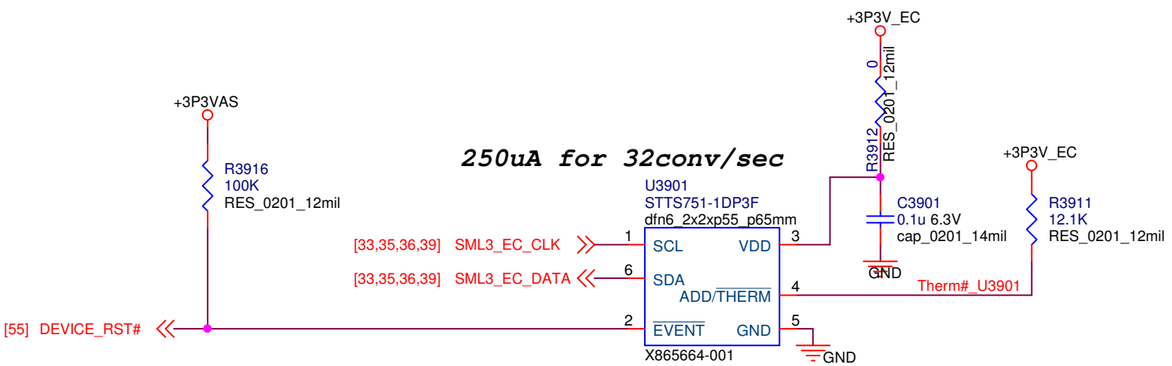












Title:	Temp Sensor/System Fan		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 39 of 76		

SPK Trace Width
1. Maximum trace resistance for each channel less than 0.5 ohms.
2. Each of 4 traces, measured from CODEC to speaker connector, less than 0.25 ohms

AUDIO_VREF
AC4019 2.2u CAP_0402_24mil 6.3V
AC4002 0.1u 6.3V cap_0201_14mil
AUDIO_VREF1
C4011 10u 6.3V CAP_0402_28mil
AC4010 0.1u 6.3V cap_0201_14mil
AGND

+5V_AUDIO
AR4034 0 res_0603_24mil
+5V_AUIDO_AVDD
C4010 10u 6.3V CAP_0402_28mil
AC4005 0.1u 6.3V cap_0201_14mil
L4010 600 OHM 2A ind_0805_44mil
+5V_AUIDO_PVDD
C4012 10u 10V cap_0603_36mil
AC4039 0.1u 6.3V cap_0201_14mil
C4014 10u 6.3V CAP_0402_28mil
AC4040 0.1u 6.3V cap_0201_14mil
GND

+1P8V_AUDIO
AR4014 0 res_0603_24mil
C4013 10u 6.3V CAP_0402_28mil
AC4021 0.1u 6.3V cap_0201_14mil
C4015 10u 6.3V CAP_0402_28mil
AC4041 0.1u 6.3V cap_0201_14mil
+1P8V_AUDIO_DVDD
EV1.9 WAS:10V

+1P8V_AUDIO
AR4008 10K RES_0201_12mil
CODEC_PD#_G
AR4007 10K RES_0201_12mil
Q4001 MMBT3904WT1G sot323_2x1p25x1p1_p65mm
[20,40] AZ_RST#_1
+1P8V_AUDIO
AR4018 100K RES_0201_12mil
[10] PCH_CODEC_IRQ

+1P8V_AUDIO
C4016 10u 6.3V CAP_0402_28mil
AC4003 0.1u 6.3V cap_0201_14mil
AC4014 2.2u 6.3V CAP_0402_22mil
AC4046 2.2u 6.3V CAP_0402_22mil
C4017 10u 6.3V CAP_0402_28mil
AGND

EV1.9 WAS:10V
AC4017 2.2u 6.3V CAP_0402_22mil
AC4018 2.2u 6.3V CAP_0402_22mil

DNP,AUDIO
AR4002 0 RES_0201_12mil
AR4001 0 RES_0201_12mil
GND AGND

TP4031 SP_TP_SMDp58mm
AGND
close to audio

U4009
ALC3269-CG
qfn57_7x7xp9_p4mm

43	VREF
21	VREF1
45	AVDD1
23	PCBEEP
46	PVDD1
51	PVDD2
7	DVDD
19	DVDD_IO
24	CPVDD/AVDD2
31	CPVEE
29	CPVPP
30	CPVREF
53	DMIC_CLK
54	DMIC_DATA1
41	MIC1_CAP
52	EAPD+PD#/GPIO11
6	HD_I2S_SEL/IRQOUT/GPIO0
5	I2S_IN/GPIO5
3	I2S_OUT/GPIO6
56	I2S_BCLK/GPIO7
55	I2S_MCLK/SPDIF_IN/GPIO8
1	I2S_LRCK/GPIO9
2	GPIO1/DMIC_CLK2/SPDIF_OUT/I2S_IN_JD
4	GPIO2/DMIC_DATA2/I2S_OUT_JD
28	CBN1
25	CNB2
27	CBP1
26	CBP2

CPVEE
CPVPP
[20,32,42] DMIC1_CLK
[20,32,42] DMIC1_DATA
ALC298_MIC1_CAP
CODEC_PD#
was I2S_IN (DSP)
was I2S_OUT (DSP)
was I2S_BCLK (DSP)
was AUD_RESET (DSP)
was I2S_LCLK (DSP)
CODEC_CBN1_R
CODEC_CBP1_R
CODEC_CBN2_R
CODEC_CBP2_R

TP4001 TP4002 SP_TP_SMDp58mm SP_TP_SMDp58mm

13	HDA_BCLK/I2S_BCLK
15	HDA_RESETB/I2S_MCLK
16	HDA_SDATA_IN/I2S_SDO
17	HDA_SDATA_OUT/I2S_SDI
14	HAD_SYNC/I2S_LRCK
9	HP_JD/LINE1_JD
32	HP_OUT_L
33	HP_OUT_R
12	I2C_CLK
11	I2C_DATA
8	I2S_OUT_JD/MIC_JD
44	LDO1_CAP
22	LDO2_CAP
18	LDO3_CAP
35	LINE1_L
34	LINE1_R
40	LINE1_VREFO
36	MIC1_L/RING2
37	MIC1_R/SLEEVE
38	MIC1_VREFO_L/AGPO_0
39	MIC1_VREFO_R/AGPO_1
48	SPK_OUT_LN
47	SPK_OUT_LP
49	SPK_OUT_RN
50	SPK_OUT_RP
42	AVSS1
20	AVSS2
10	VD33STB
57	E_PAD

SDATA_IN_R
AR4004 33 RES_0201_12mil
HPOUT_JD_R
HPOUT_L [41]
HPOUT_R [41]
COMBO_JACK [41]
DSP
DSP
MIC1_L [41]
MIC1_R [41]
MIC1_VREFO_L [41]
SPK_L- [41]
SPK_L+ [41]
SPK_R- [41]
SPK_R+ [41]
GND AGND

+1P8V_AUDIO
AR4019 100K RES_0201_12mil
AR4006 200K RES_0201_12mil
HPOUT_JD [41]
DNP,AUDIO AR4033 100K RES_0201_12mil
DNP,AUDIO AC4038 0.1u 6.3V cap_0201_14mil
DNP,AUDIO AC4012 22PF 25V CAP_0201_14mil
DNP,AUDIO AC4011 22PF 25V CAP_0201_14mil
GND

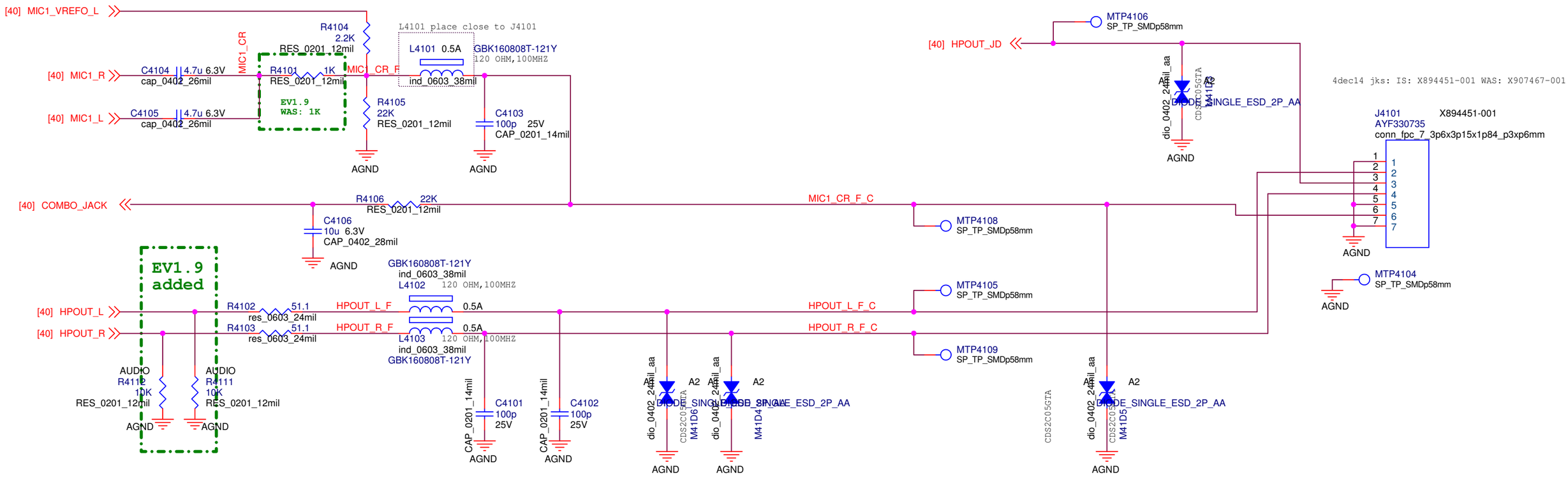
AZ_BITCLK_1 [20]
AZ_RST#_1 [20,40]
AZ_SDATA_IN0 [20]
AZ_SDATA_OUT_1 [20]
AZ_SYNC_1 [20]

CODEC_LDO1
CODEC_LDO2
CODEC_LDO3
AC4023 0.1u 6.3V cap_0201_14mil
AC4016 10u 6.3V CAP_0402_28mil
AC4024 0.1u 6.3V cap_0201_14mil
AC4025 10u 6.3V CAP_0402_28mil
AC4026 0.1u 6.3V cap_0201_14mil
AC4027 10u 6.3V CAP_0402_28mil
GND AGND

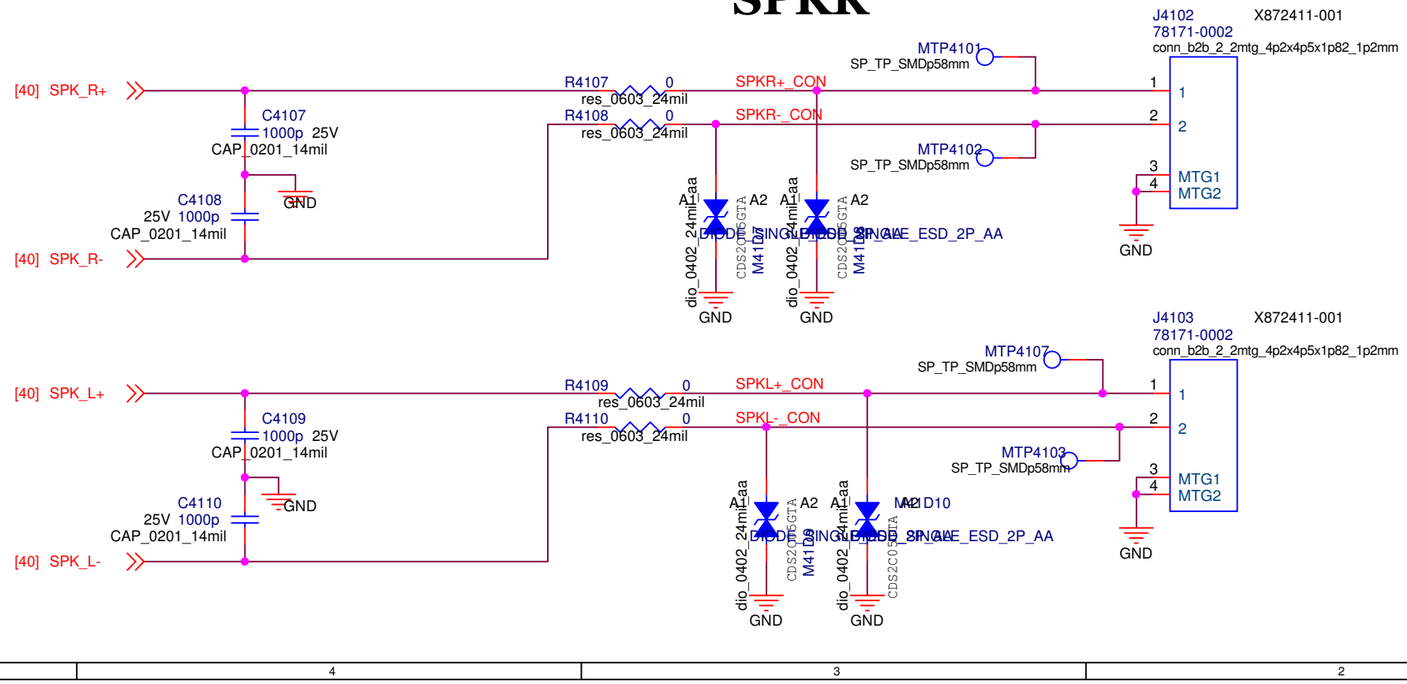
+5V_AUDIO
AR4035 10K RES_0201_12mil
ALC298_VD22STB
DNP,AUDIO AR4036 100K RES_0201_12mil
GND AGND GND

Title: REALTEK ALC3269 CODEC			
Microsoft	Engineer: Surface		
Size: A3	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 40 of 76		

Audio Jack/MIC1 Combo Jack

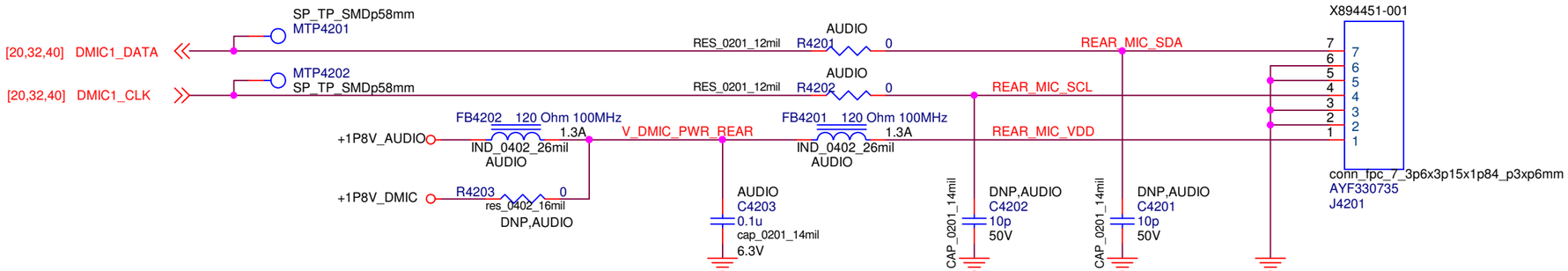


SPKR



Title:	Audio Jack/Speaker	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 41 of 76	

RearMicFlex

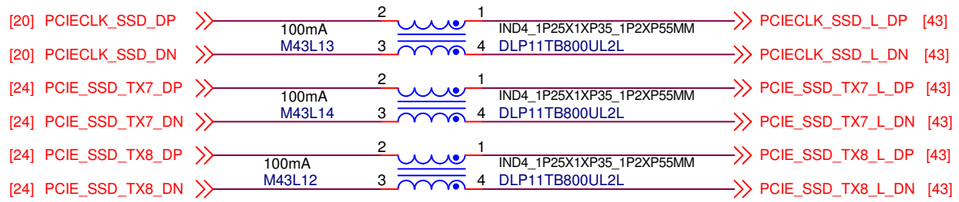


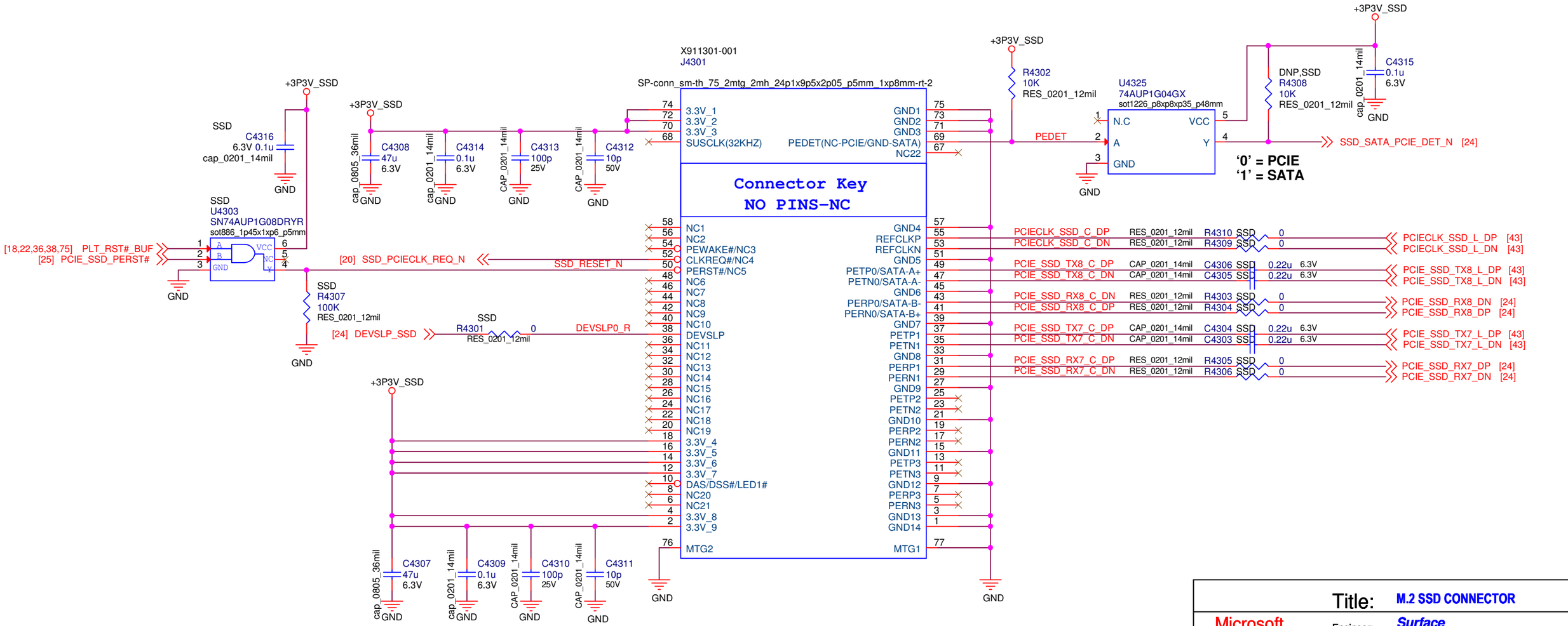
Title:	Microphones		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 42 of 76		

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen2/SATA	PCI Express* Gen3/SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF [2]	None	None [3]

2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.

3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. This option DOES NOT support DC coupled ODDs / Devices.





Title: M.2 SSD CONNECTOR

Microsoft Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 43 of 76

Title:	Empty
Microsoft	Engineer: Surface
Size: B	Project Name: U -- EV 1.90
Rev:	1.90.2
Date:	Monday, May 11, 2015
Sheet	44 of 76

UU4501
DF5G7M2N
dfn5_1p3xp8xp4_p45mm

USB3_TYPA_TX_DN 1 IO1
USB3_TYPA_RX_DP 3 IO2
USB3_TYPA_RX_DN 4 IO3
USB3_TYPA_TX_DP 5 IO5
GND 2
GND

[24] USB3_CONN_RX_DN
[24] USB3_CONN_RX_DP
L4502
DLP11TB800UL2L
IND4_1P25X1XP35_1P2XP55MM
USB3_TYPA_RX_DN
USB3_TYPA_RX_DP

cap_0201_14mil
[24] USB3_CONN_TX_DN
C4513 0.1u 6.3V
USB3_CONN_TX_C_DN
[24] USB3_CONN_TX_DP
C4512 0.1u 6.3V
USB3_CONN_TX_C_DP
100mA
L4501
IND4_1P25X1XP35_1P2XP55MM
DLP11TB800UL2L
USB3_TYPA_TX_DN
USB3_TYPA_TX_DP
cap_0201_14mil

MTP4501
SP_TP_SMDp58mm
MTTP_BF4501
sp_MTP0p8mm
MTTP_BF4502
sp_MTP0p8mm
MTP4502
SP_TP_SMDp58mm

U4503
IP3319CX6
bga6_2x3ns_p95x1p34xp6_p4mm
[24] USB2_CONN_DP
[24] USB2_CONN_DN
A1 DP_O
B1 DM_O
DP_I A2
DM_I B2
C2
ID
C1
GND
GND
USB2_TYPA_DP
USB2_TYPA_DN

MTP4503
SP_TP_SMDp58mm
GND
MTTP_BF4503
sp_MTP0p8mm
GND

+5V_USBPWR
EV1.9 was -003
J4501
X910059-004
SP-conn_usb3_9_10MTG_2MH_17p1x15p5x4p44_2p5mm
1 VBUS
2 D-
3 D+
4 GND
5 STDA_SSRX-
6 STDA_SSRX+
7 GND_DRAIN
8 STDA_SSTX-
9 STDA_SSTX+
MTG10 19
MTG9 18
MTG8 17
MTG7 16
MTG6 15
MTG5 14
MTG4 13
MTG3 12
MTG2 11
MTG1 10
MSPN = X910059-004

A1 D4501
dio_0402_24mil_aa
DIODE_SINGLE_ESD_2P_AA

1.5 => ILIM(11.8K) => 2 A
Imax = 2.1 A

MTTP_BF4504
sp_MTP0p8mm
MTP4504
SP_TP_SMDp58mm

+5VSB
C4511
1u 6.3V
CAP_0201_14mil

[24] USB_CONN_OC#
[36,60,61,62] SUSC_EC#
RES_0201_12mil R4515 0
RES_0201_12mil R4510 0
USB_CONN_OC#_R
U4504
NCP380HMUAJAATBG
dfn7_2x2xp55_p65mm
FLAG# IN
EN
GND1 OUT
GND2 ILIM
+5V_USBPWR_REG
+5V_USBPWR_ILIM
R4512
11.8K
res_0201_12mil
+5V_USBPWR_EN

jks 6dec14: chg from ceramic to tant for space saving

C7648 47u 16V cap_3p5x2p8x1p2mm
C7649 47u 16V cap_3p5x2p8x1p2mm
C7647 47u 16V cap_3p5x2p8x1p2mm

DB,USB
R4511 0.01
res_0402_22mil
PMTP4505
SP-tp-c0p381
PMTP4504
SP-tp-c0p381

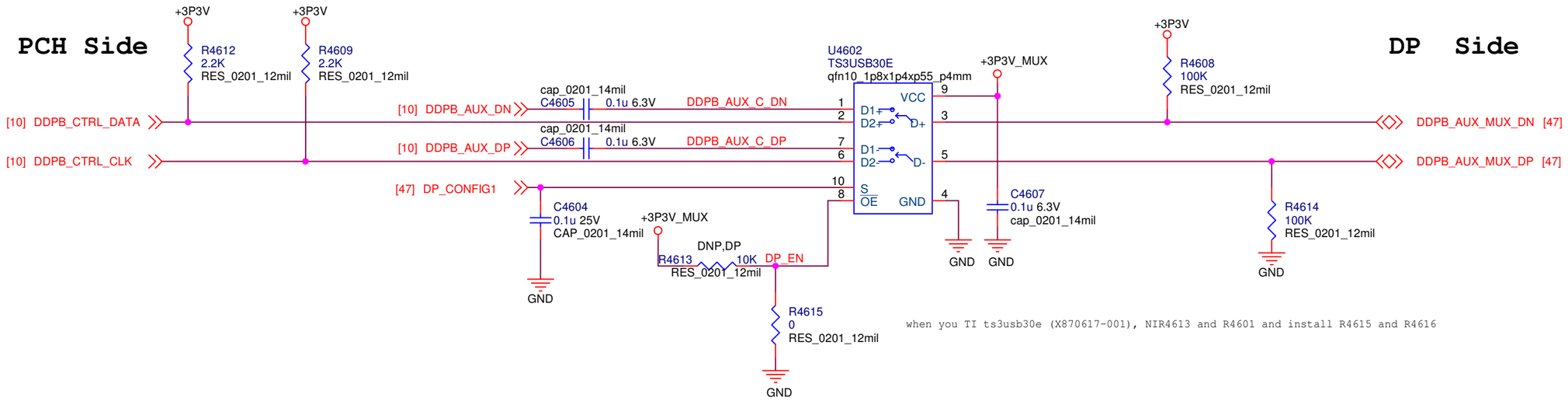
+5V_USBPWR
R4514
750
RES_0402_16mil
5.25**2/(750*.99)=37mW

+5V_USBPWR
Imin = 1.5A (ng 19dec14)
Imax=1.9A

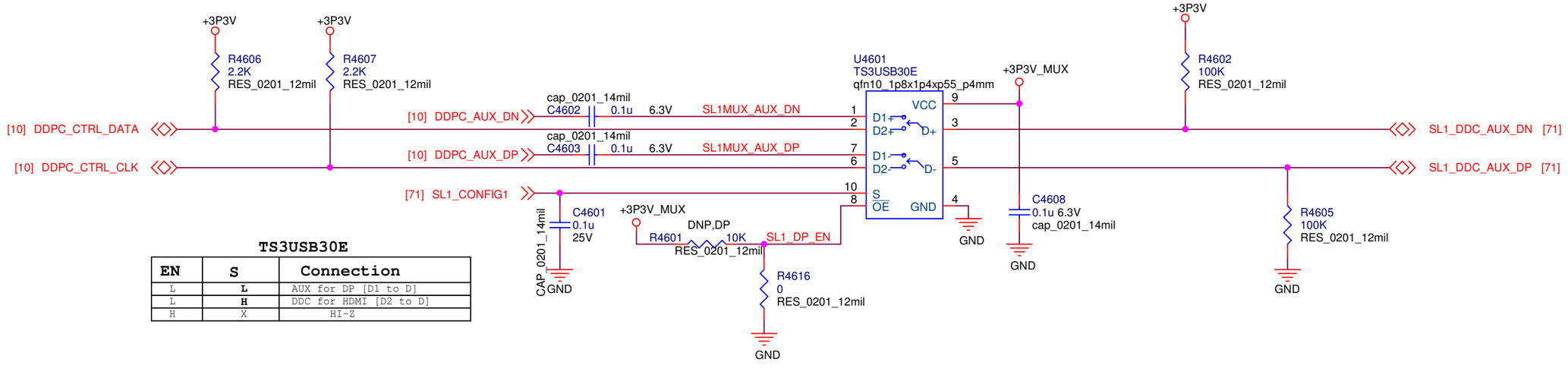
+3P3VSB
R4513
499K
RES_0201_12mil
+5V_USBPWR_DISC_CTRL
+5V_USBPWR_disc
Q4501A
NX3008NBKS
sot363_6_2x1p25x1p1_p65mm
Q4501B
NX3008NBKS
sot363_6_2x1p25x1p1_p65mm

Title:	USB3.0		
Microsoft	Engineer:	*Surface*	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 45 of 76	

mDP mux to HDMI/DVI Dongle control



SL1 DP mux to HDMI/DVI Dongle control



TS3USB30E

EN	S	Connection
L	**L**	AUX for DP [D1 to D]
L	**H**	DDC for HDMI [D2 to D]
H	X	HI-Z

Title:	DP Dongle Control	
Microsoft	Engineer: *Surface*	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 46 of 76	

NOTE:
Pass gate to prevent back-drive when sink device is on and PCH is powered down.

NOTE:
Place D4701 near to DP connector

NOTE:
Place those AC Caps near to DP connector.

EV1.9 was -003

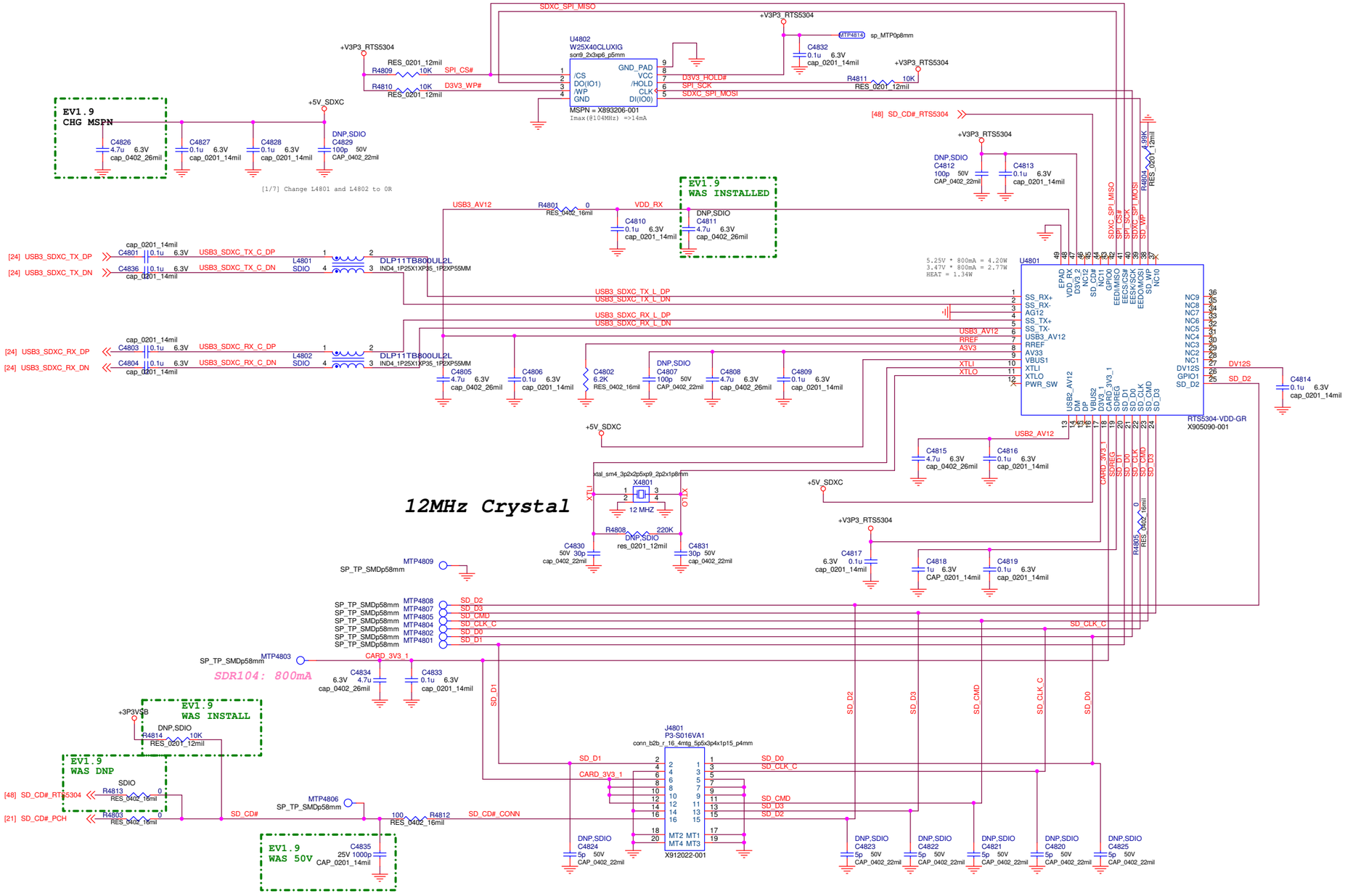
+3P3V
mDP conn
Imax = 0.5A

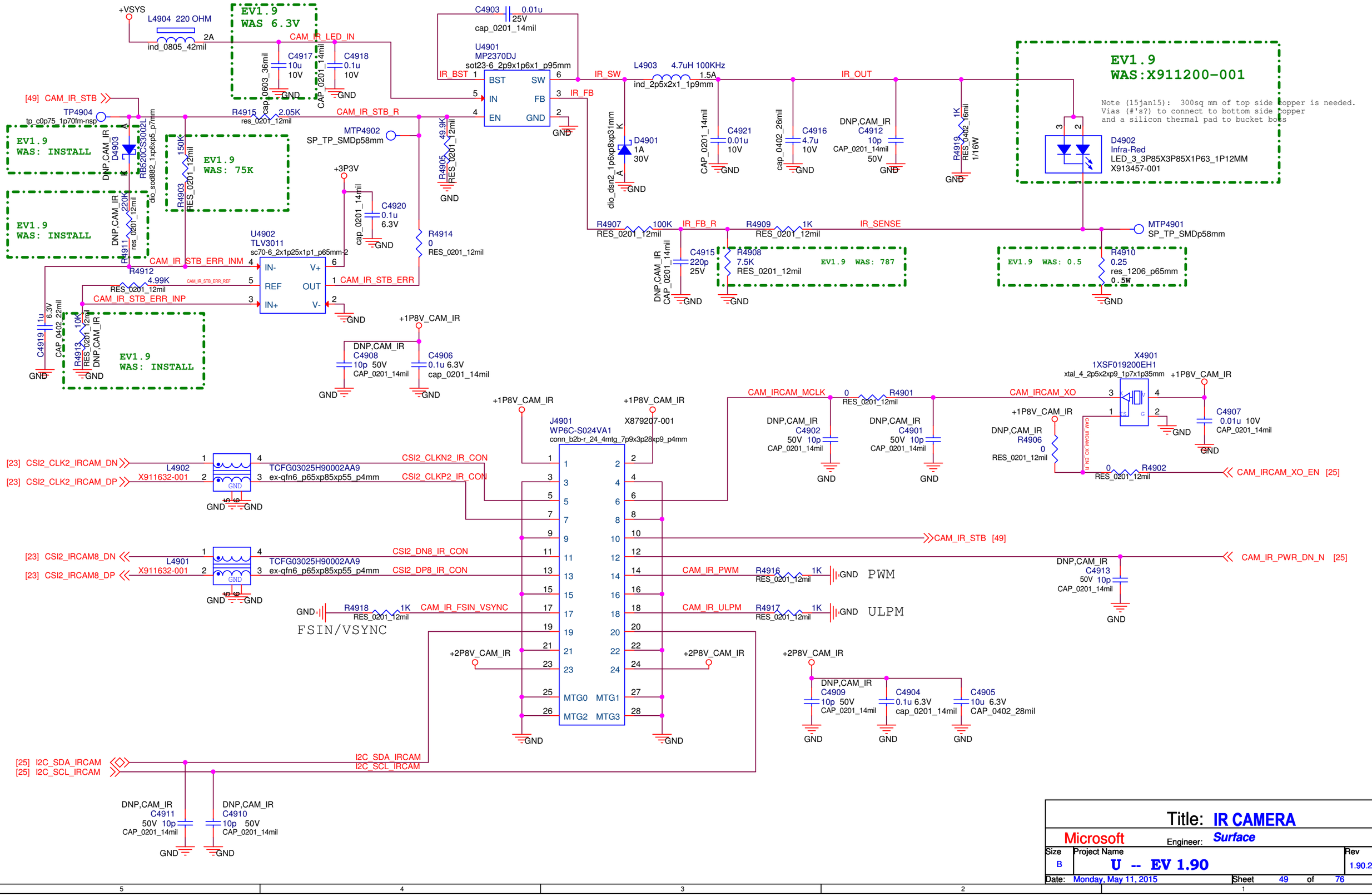
EV1.9 WAS:+3P3V

ILIM(33K) ~ 0.8A
meet VESA spec

EV1.9
was:16V

Title:	mDP		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 47 of 76		


SDXC_SPI_MISO
+V3P3_RTS5304
U4802
W25X40CLUXIG
son9_2x3xp6_p5mm
MTP4814
sp_MTP0p8mm
C4832
0.1u 6.3V
cap_0201_14mil
R4809 10K SPI_CS#
R4810 10K D3V3_WP#
RES_0201_12mil
/CS
DO(IO1)
/WP
GND
VCC
/HOLD
CLK
DI(IO0)
GND_PAD
D3V3_HOLD#
SPI_SCK
SDXC_SPI_MOSI
R4811 10K
MSPN = X893206-001
Imax(@104MHz) =>14mA
+5V_SDXC
EV1.9
CHG MSPN
C4826 4.7u 6.3V cap_0402_26mil
C4827 0.1u 6.3V cap_0201_14mil
C4828 0.1u 6.3V cap_0201_14mil
DNP,SDIO
C4829 100p 50V CAP_0402_22mil
[1/7] Change L4801 and L4802 to 0R
[48] SD_CD#_RTS5304
C4812 100p 50V CAP_0402_22mil
C4813 0.1u 6.3V cap_0201_14mil
R4804 499K RES_0201_12mil
USB3_AV12
R4801 0 RES_0402_16mil
VDD_RX
C4810 0.1u 6.3V cap_0201_14mil
EV1.9
WAS INSTALLED
DNP,SDIO
C4811 4.7u 6.3V cap_0402_26mil
5.25V * 800mA = 4.20W
3.47V * 800mA = 2.77W
HEAT = 1.34W
U4801
RTS5304-VDD-GR
X905090-001
[24] USB3_SDXC_TX_DP
[24] USB3_SDXC_TX_DN
C4801 0.1u 6.3V
C4836 0.1u 6.3V
cap_0201_14mil
USB3_SDXC_TX_C_DP
USB3_SDXC_TX_C_DN
L4801 SDIO
DLP11TB800UL2L
IND4_1P25X1XP35_1P2XP55MM
USB3_SDXC_TX_L_DP
USB3_SDXC_TX_L_DN
USB3_SDXC_RX_L_DP
USB3_SDXC_RX_L_DN
[24] USB3_SDXC_RX_DP
[24] USB3_SDXC_RX_DN
C4803 0.1u 6.3V
C4804 0.1u 6.3V
USB3_SDXC_RX_C_DP
USB3_SDXC_RX_C_DN
L4802 SDIO
C4805 4.7u 6.3V cap_0402_26mil
C4806 0.1u 6.3V cap_0201_14mil
C4802 6.2K RES_0402_16mil
DNP,SDIO
C4807 100p 50V CAP_0402_22mil
C4808 4.7u 6.3V cap_0402_26mil
C4809 0.1u 6.3V cap_0201_14mil
RREF
A3V3
XTLI
XTLO
+5V_SDXC
xtal_sm4_3p2x2p5xp9_2p2x1p8mm
X4801
12 MHZ
R4808 220K
DNP,SDIO
res_0201_12mil
C4830 50V 30p cap_0402_22mil
C4831 30p 50V cap_0402_22mil
12MHz Crystal
USB2_AV12
C4815 4.7u 6.3V cap_0402_26mil
C4816 0.1u 6.3V cap_0201_14mil
+V3P3_RTS5304
C4817 6.3V 0.1u cap_0201_14mil
C4818 1u 6.3V CAP_0201_14mil
C4819 0.1u 6.3V cap_0201_14mil
R4805 0 RES_0402_16mil
DV12S
SD_D2
C4814 0.1u 6.3V cap_0201_14mil
MTP4809
SP_TP_SMDp58mm
MTP4808 SD_D2
MTP4807 SD_D3
MTP4805 SD_CMD
MTP4804 SD_CLK_C
MTP4802 SD_D0
MTP4801 SD_D1
SD_CLK_C
MTP4803
CARD_3V3_1
SDR104: 800mA
C4834 6.3V 4.7u cap_0402_26mil
C4833 0.1u 6.3V cap_0201_14mil
EV1.9
WAS INSTALL
+3P3VSB
DNP,SDIO
R4814 10K RES_0201_12mil
EV1.9
WAS DNP
SDIO
[48] SD_CD#_RTS5304
R4813 0
[21] SD_CD#_PCH
R4803 0
RES_0402_16mil
SD_CD#
MTP4806
SP_TP_SMDp58mm
100 R4812 RES_0402_16mil
SD_CD#_CONN
EV1.9
WAS 50V
C4835 25V 1000p CAP_0201_14mil
J4801
P3-S016VA1
conn_b2b_r_16_4mtg_5p5x3p4x1p15_p4mm
X912022-001
DNP,SDIO
C4824 5p 50V CAP_0402_22mil
C4823 5p 50V CAP_0402_22mil
C4822 5p 50V CAP_0402_22mil
C4821 5p 50V CAP_0402_22mil
C4820 5p 50V CAP_0402_22mil
C4825 5p 50V CAP_0402_22mil
Title: SDXC
Microsoft
Engineer: Surface
Size C
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 48 of 76


+VSYS
L4904 220 OHM
2A
ind_0805_42mil
EV1.9
WAS 6.3V
CAM_IR_LED_IN
C4917
10u
10V
cap_0603_36mil
C4918
0.1u
10V
CAP_0201_14mil
GND
C4903
0.01u
25V
cap_0201_14mil
U4901
MP2370DJ
sot23-6_2p9x1p6x1_p95mm
IR_BST
BST
SW
IN
FB
EN
GND
IR_SW
IR_FB
L4903
4.7uH 100KHz
1.5A
ind_2p5x2x1_1p9mm
IR_OUT
[49] CAM_IR_STB
TP4904
tp_c0p75_1p70fm-nsp
R4915
2.05K
res_0201_12mil
CAM_IR_STB_R
MTP4902
SP_TP_SMDp58mm
49.9K
RES_0201_12mil
R4905
D4901
1A
30V
dio_dsn2_1p6xp8xp31mm
C4921
0.01u
10V
CAP_0201_14mil
C4916
4.7u
10V
cap_0402_26mil
DNP,CAM_IR
C4912
10p
50V
CAP_0201_14mil
R4919
1K
RES_0402_6mil
1/16W
EV1.9
WAS:X911200-001
Note (15jan15): 300sq mm of top side copper is needed.
Vias (#'s?) to connect to bottom side copper
and a silicon thermal pad to bucket boss
D4902
Infra-Red
LED_3_3P85X3P85X1P63_1P12MM
X913457-001
EV1.9
WAS: INSTALL
DNP,CAM_IR
D4903
RB520CS3002L
dio_sod882_1xp6xp5_p7mm
EV1.9
WAS: 75K
150K
RES_0201_12mil
R4903
+3P3V
C4920
0.1u
6.3V
cap_0201_14mil
EV1.9
WAS: INSTALL
DNP,CAM_IR
220K
res_0201_12mil
R4911
U4902
TLV3011
sc70-6_2x1p25x1p1_p65mm-2
R4914
0
RES_0201_12mil
R4907
100K
RES_0201_12mil
IR_FB_R
R4909
1K
RES_0201_12mil
IR_SENSE
C4915
220p
25V
DNP,CAM_IR
CAP_0201_14mil
R4908
7.5K
RES_0201_12mil
EV1.9 WAS: 787
MTP4901
SP_TP_SMDp58mm
EV1.9 WAS: 0.5
R4910
0.25
res_1206_p65mm
0.5W
CAM_IR_STB_ERR_INM
R4912
4.99K
RES_0201_12mil
CAM_IR_STB_ERR_REF
CAM_IR_STB_ERR_INP
IN-
V+
REF
OUT
IN+
V-
CAM_IR_STB_ERR
C4919
1u
6.3V
CAP_0402_22mil
R4913
10K
RES_0201_12mil
DNP,CAM_IR
EV1.9
WAS: INSTALL
+1P8V_CAM_IR
DNP,CAM_IR
C4908
10p 50V
CAP_0201_14mil
C4906
0.1u 6.3V
cap_0201_14mil
X4901
1XSF019200EH1
xtal_4_2p5x2xp9_1p7x1p35mm
CAM_IRCAM_MCLK
0
R4901
RES_0201_12mil
CAM_IRCAM_XO
C4907
0.01u 10V
CAP_0201_14mil
DNP,CAM_IR
C4902
50V 10p
CAP_0201_14mil
DNP,CAM_IR
C4901
50V 10p
CAP_0201_14mil
DNP,CAM_IR
R4906
0
RES_0201_12mil
CAM_IRCAM_XO_EN_R
R4902
RES_0201_12mil
CAM_IRCAM_XO_EN [25]
J4901
WP6C-S024VA1
conn_b2b-r_24_4mtg_7p9x3p28xp9_p4mm
X879207-001
[23] CSI2_CLK2_IRCAM_DN
[23] CSI2_CLK2_IRCAM_DP
L4902
X911632-001
TCFG03025H90002AA9
ex-qfn6_p65xp85xp55_p4mm
CSI2_CLKN2_IR_CON
CSI2_CLKP2_IR_CON
[23] CSI2_IRCAM8_DN
[23] CSI2_IRCAM8_DP
L4901
X911632-001
CSI2_DN8_IR_CON
CSI2_DP8_IR_CON
CAM_IR_STB [49]
CAM_IR_PWR_DN_N [25]
DNP,CAM_IR
C4913
50V 10p
CAP_0201_14mil
CAM_IR_PWM
R4916
1K
RES_0201_12mil
PWM
CAM_IR_ULPM
R4917
1K
RES_0201_12mil
ULPM
R4918
1K
RES_0201_12mil
CAM_IR_FSIN_VSYNC
FSIN/VSYNC
MTG0
MTG1
MTG2
MTG3
+2P8V_CAM_IR
DNP,CAM_IR
C4909
10p 50V
CAP_0201_14mil
C4904
0.1u 6.3V
cap_0201_14mil
C4905
10u 6.3V
CAP_0402_28mil
[25] I2C_SDA_IRCAM
[25] I2C_SCL_IRCAM
I2C_SDA_IRCAM
I2C_SCL_IRCAM
DNP,CAM_IR
C4911
50V 10p
CAP_0201_14mil
DNP,CAM_IR
C4910
10p 50V
CAP_0201_14mil
Title: IR CAMERA
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 49 of 76

OPTION HOST VIO

WIFI > PCIe3

Antenna spring x5

Antenna spring

Isolation Element

EEPROM

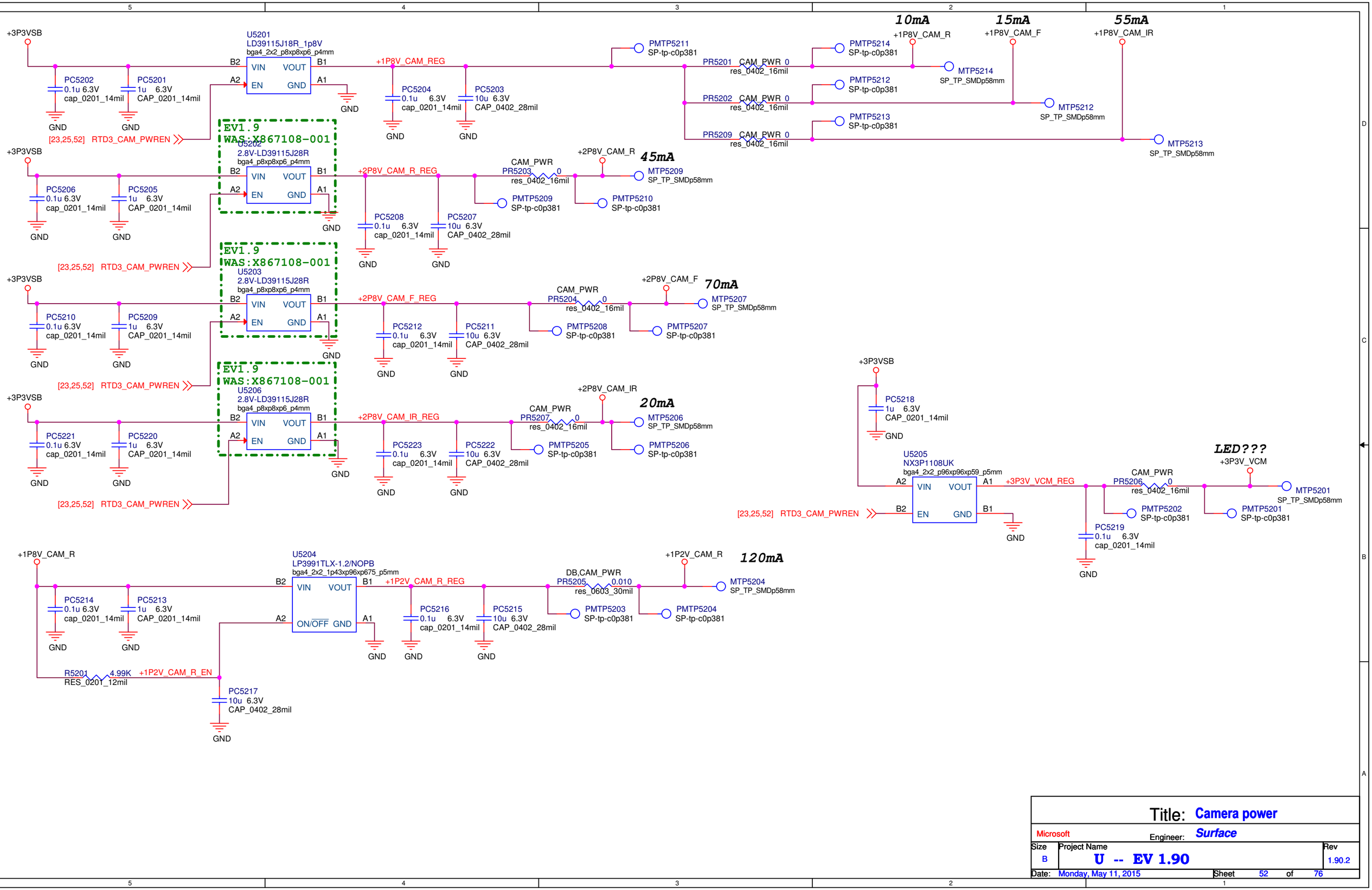
BT -> USB2.0(5)

PLACE TP's on BOTTOM,

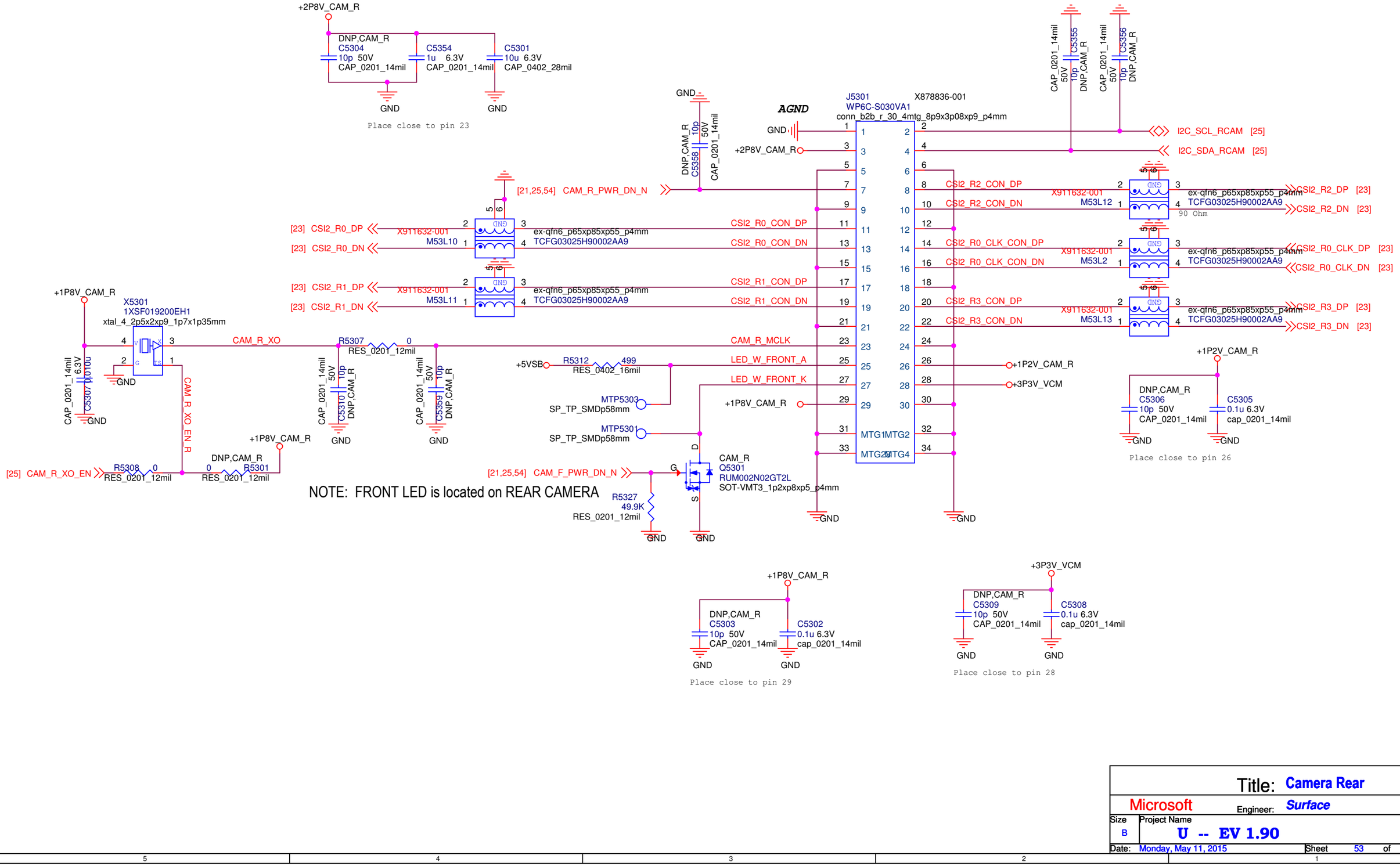
Title:	WI-FI_BT		
Microsoft	Engineer: Surface		
Size: A2	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 50 of 76		

EMPTY

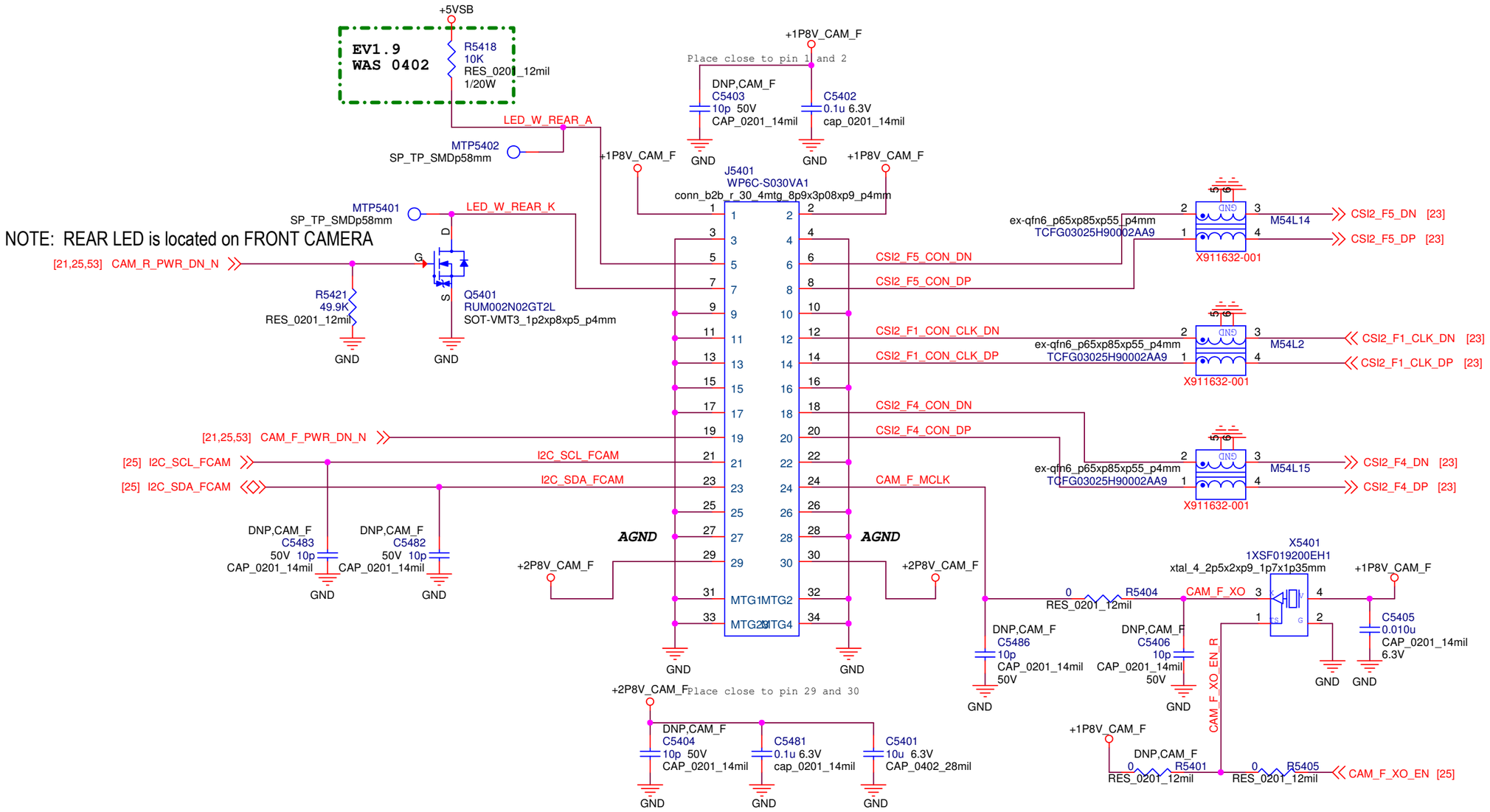
Title:	Empty		
Microsoft	Engineer:	*Surface*	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 51 of 76		



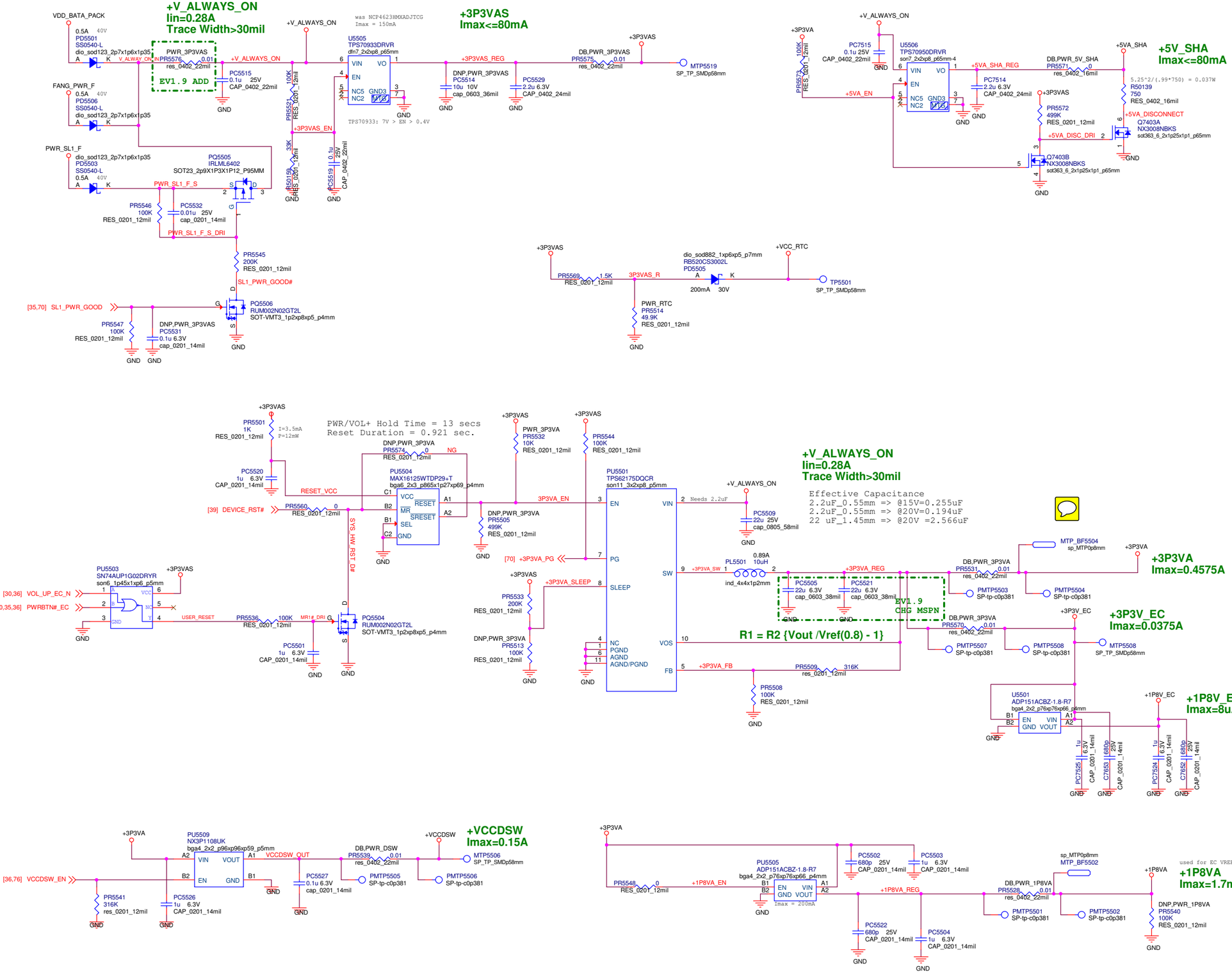
Title:	Camera power	
Microsoft	Engineer:	Surface
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 52 of 76	

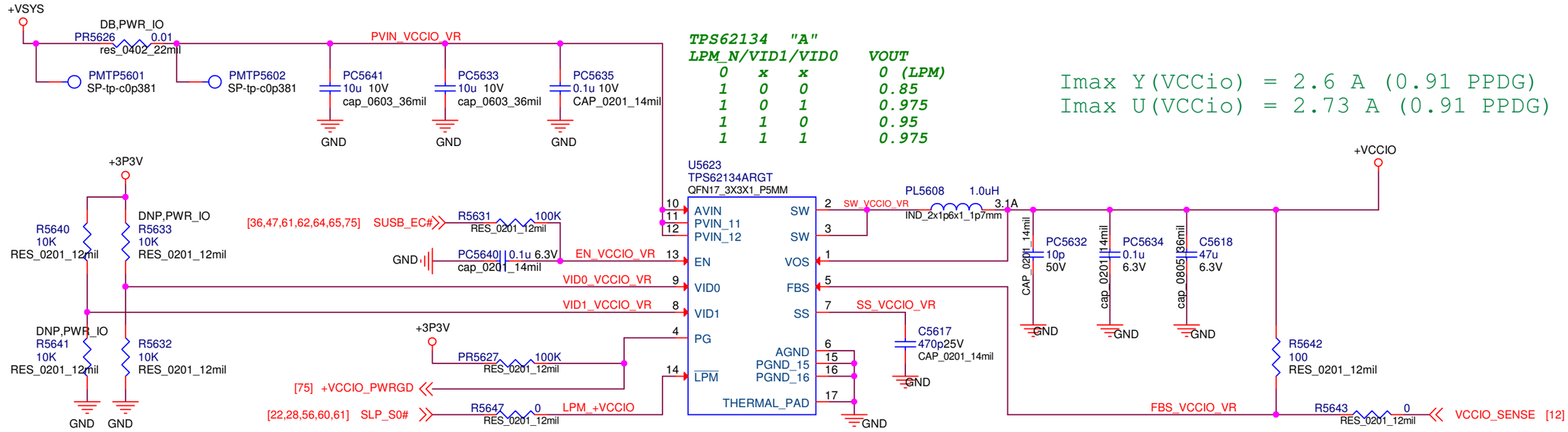


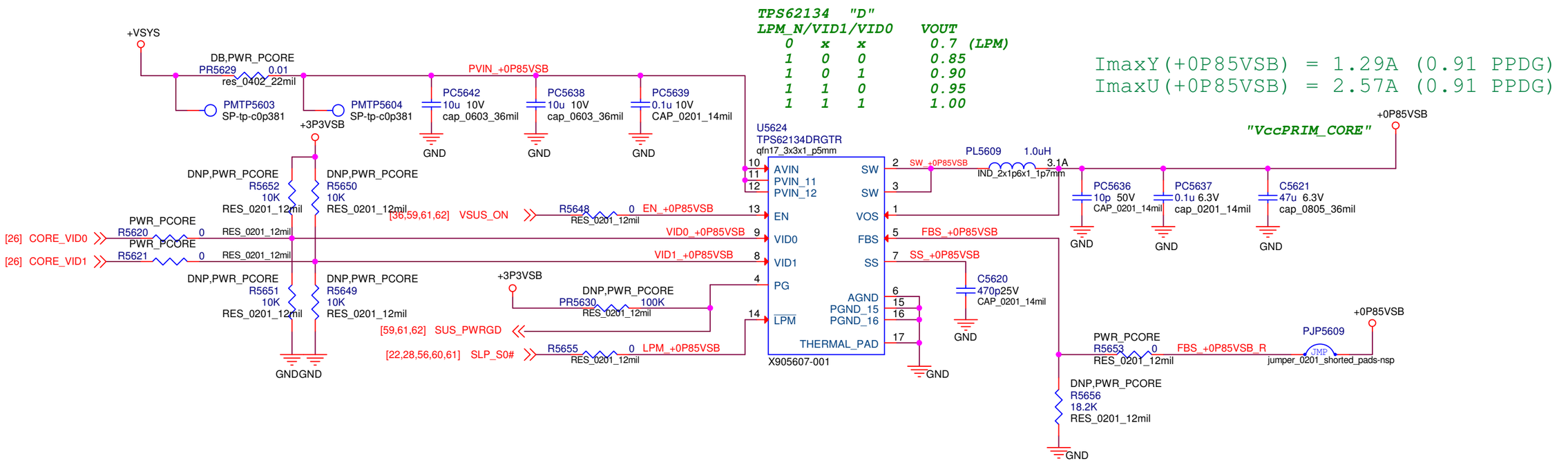
Title:	Camera Rear	
Microsoft	Engineer:	Surface
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 53 of 76	



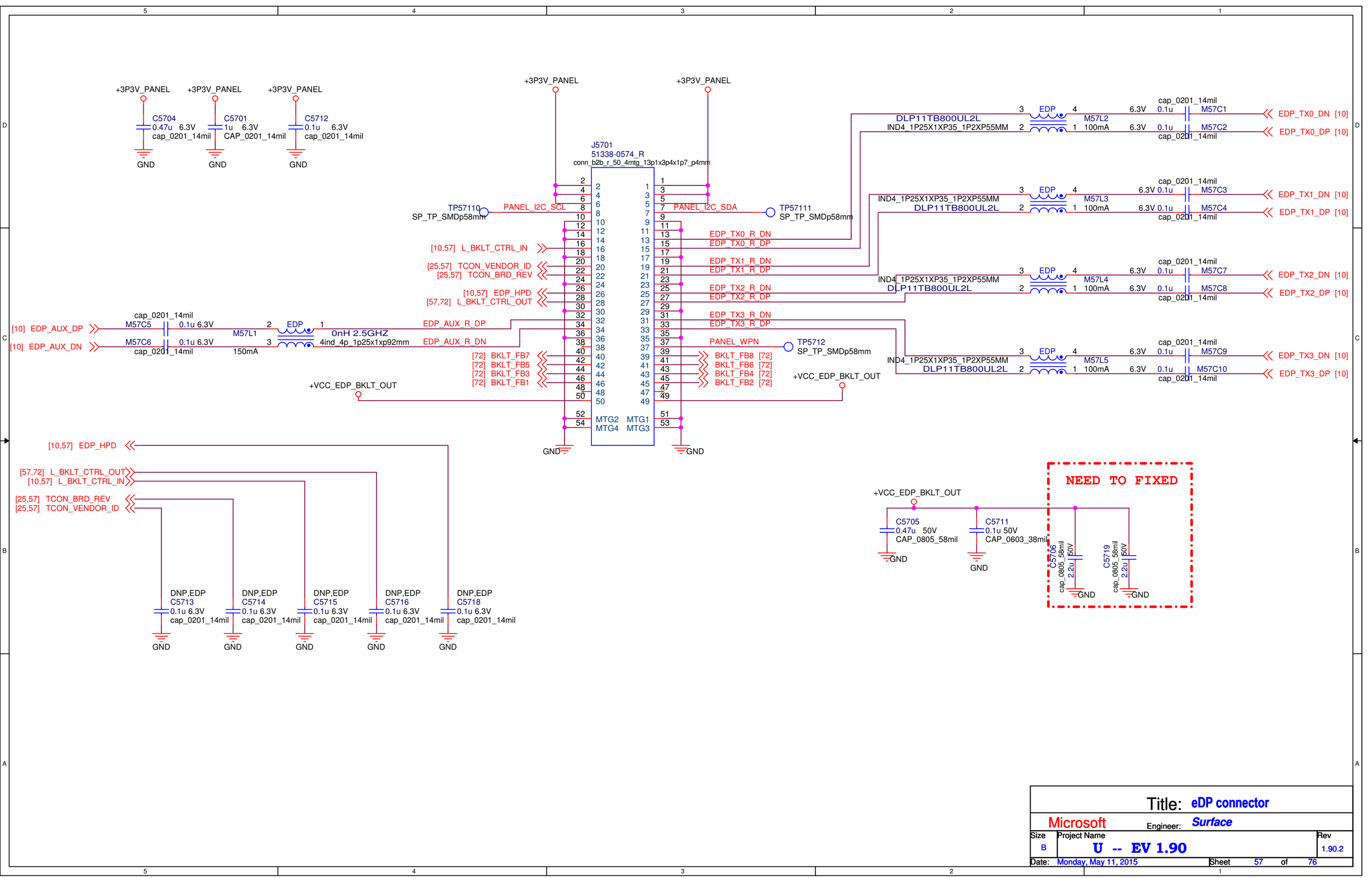
Title:	Camera Front		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 54 of 76		


+V_ALWAYS_ON
Iin=0.28A
Trace Width>30mil
was NCP4623HMXADJTCG
Imax = 150mA
+3P3VAS
Imax<=80mA
EV1.9 ADD
TPS70933: 7V > EN > 0.4V
+5V_SHA
Imax<=80mA
R1 = R2 {Vout /Vref(0.8) - 1}
EV1 . 9
CHG MSPN
PWR/VOL+ Hold Time = 13 secs
Reset Duration = 0.921 sec.
Effective Capacitance
2.2uF_0.55mm => @15V=0.255uF
2.2uF_0.55mm => @20V=0.194uF
22 uF_1.45mm => @20V =2.566uF
+3P3VA
Imax=0.4575A
+3P3V_EC
Imax=0.0375A
+1P8V_EC
Imax=8uA
+1P8VA
Imax=1.7mA
+VCCDSW
Imax=0.15A
Title: +3P3VA & +5VA
Microsoft
Engineer: Surface
Size C
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 55 of 76



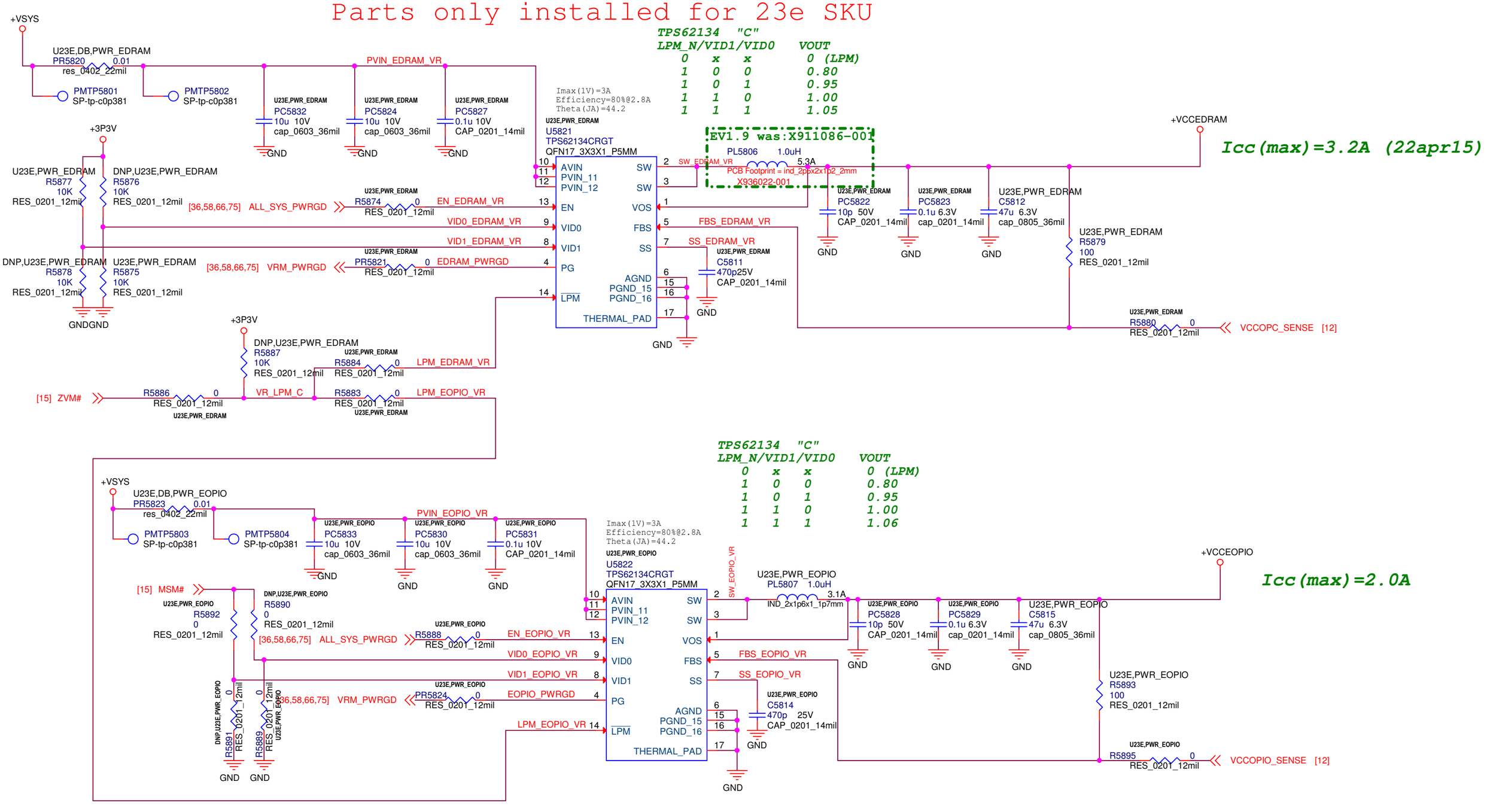


Title:	+VCCIO & 0P85VSB		
Microsoft	Engineer:	Surface	
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 56 of 76		

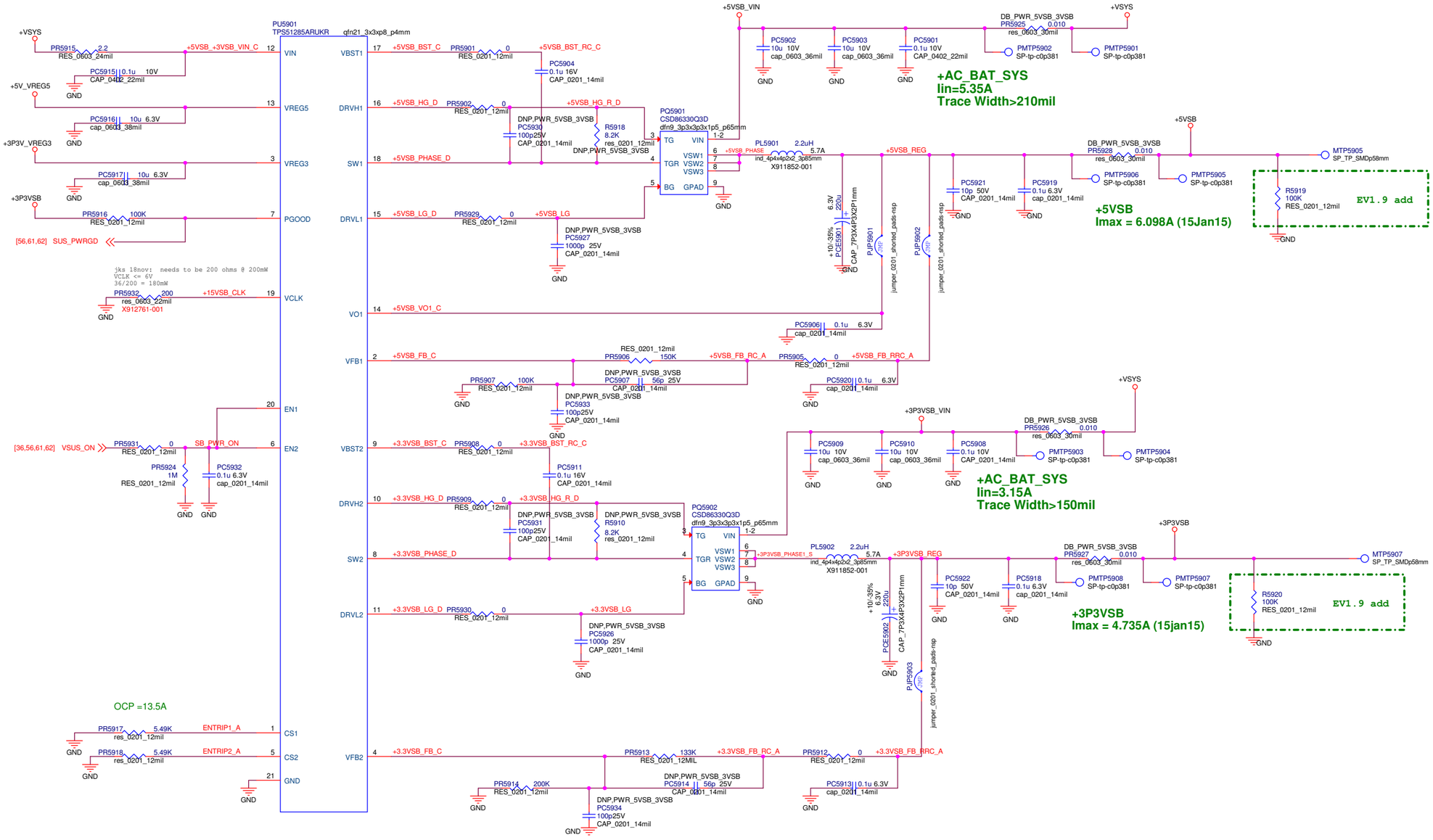


Title:	eDP connector	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 57 of 76	

Parts only installed for 23e SKU



Title:	+VCCEDRAM & +VCCEOPIO
Microsoft	Engineer: Surface
Size: B	Project Name: U -- EV 1.90
Rev:	1.90.2
Date:	Monday, May 11, 2015
Sheet	58 of 76



Title: +5VSB & +3P3VSB

Microsoft Engineer: Surface

Size	Project Name	Rev
C	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 59 of 76

PU6002
TPS51367RVER
qfn29_4p5x3p5x1_p4mm

+5VSB
PR6003 4.7 RES_0603_24mil +1P2V_DUAL_V5 18 V5
GND PC6002 2.2u 6.3V CAP_0402_24mil

[36,45,60,61,62] SUSC_EC# PR6005 0 RES_0201_12mil +1P2V_DUAL_EN 28 EN
GND PC6003 0.01u 10V CAP_0201_14mil

+1P2V_DUAL
DNP,PWR_1P2V_DUAL PR6016 100K RES_0201_12mil
[75] +1P2V_DUAL_PWRGD 1 PGOOD

Low power mode for Connected Stanby

GND PC6015 2700p +1P2V_DUAL_SL 21 SLEW
CAP_0402_22mil

DNP,PWR_1P2V_DUAL
[11,60] DDR_PG_CTRL PR6024 0 RES_0201_12mil
[22,28,56,61] SLP_S0# PR6025 0 RES_0201_12mil
PR6011 0 RES_0201_12mil +1P2V_DUAL_LP 2 LP#
DNP,PWR_1P2V_DUAL
GND

+5VSB
PR6007 10K RES_0201_12mil +1P2V_DUAL_OC 20 TRIP

OCP =12A

GND DNP,PWR_1P2V_DUAL PR6008 0 RES_0201_12mil

Fsw =800kHz

GND DNP,PWR_1P2V_DUAL PR6009 0 RES_0201_12mil +1P2V_DUAL_MD 3 MODE

+1P2V_DUAL_VREF
cap_0201_14mil PC6010 0.1u 6.3V
DNP,PWR_1P2V_DUAL PR6010 15K res_0201_12mil
DNP,PWR_1P2V_DUAL PR6001 10K RES_0201_12mil 26 VREF
+1P2V_DUAL_REFIN 25 REFIN

REFIN = FLOAT (1.2V)

DNP,PWR_1P2V_DUAL
GND PC6014 0.1u 6.3V cap_0201_14mil

PJP6001
+1P2V_DUAL JMP jumper_0201_shorted_pads-nsp +1P2V_DUAL_VSNS_C PR6013 0 RES_0201_12mil +1P2V_DUAL_VSNS 22 VSNS

Near DDR

PC6013 1000p 25V CAP_0201_14mil

PJP6002
GND JMP jumper_0201_shorted_pads-nsp +1P2V_DUAL_VGNS_C PR6014 0 RES_0201_12mil +1P2V_DUAL_VGNS 23 GSNS

GND DNP,PWR_1P2V_DUAL PC6012 0.1u 6.3V cap_0201_14mil

4 NC
27 RA
24 REFIN2
19 GND1
29 GND2
10 PGND1
11 PGND2
12 PGND3
13 PGND4
14 PGND5
GND

+1P2V_DUAL_VIN
15 VIN1
16 VIN2
17 VIN3
PC6019 10u 10V CAP_0201_14mil
PC6017 10u 10V cap_0603_36mil
PC6018 10u 10V cap_0603_36mil
GND

+VSYS
DB,PWR_1P2V_DUAL PR6019 0.010 res_0603_30mil
PMTP6001 SP-tp-c0p381
PMTP6002 SP-tp-c0p381

+VSYS
Iin=1.7A
Trace Width>80mil

25nov jks: REMOVE 0ohm 0805 from +1P2V_DUAL_BOOT

5 BST +1P2V_DUAL_BOOT
PC6001 0.1u 6.3V cap_0201_14mil

6 SW1 +1P2V_DUAL_PHASE
7 SW2
8 SW3
9 SW4
PL6001 0.33uH 12A ind_4p4x4p2x1p2_3p85mm

PCE6001 470u 2V 20% cap_7p3x4p3x2p1mm
PC6009 0.1u 6.3V cap_0201_14mil
PC6021 10p 50V CAP_0201_14mil
GND

+1P2V_DUAL

Imax Y(+1P2V_DUAL) = 4.5/3.5 A (0.91 PPDG)
Imax U(+1P2V_DUAL) = 4.5/3.5 A (0.91 PPDG)

+1P2V_DUAL
Imax = 7.950A (15Jan15)
TDC = 3.5A

+5VSB
PR6018 2.2 RES_0201_12mil
+5V
DNP,PWR_VTT PR6017 2.2 RES_0201_12mil +V_VDDQ_VTT_VDD 10 VDD
GND PC6006 0.1u 6.3V cap_0201_14mil

PU6001
TPS51206DSQR
son11_2x2xp8_p4mm

[11,60] DDR_PG_CTRL PR6026 0 RES_0201_12mil S3_VDDQ_VTT_REG 7 S3
[36,45,60,61,62] SUSC_EC# PR6027 0 RES_0201_12mil S5_VDDQ_VTT_REG 9 S5
+VDDQ_VREF
PC6016 0.22u 6.3V CAP_0201_14mil
6 VTTREF
8 GND1
11 GND2
VDDQSNS
VLDOIN
VTT
VTTSNS
PGND
GND

1 VDDQSNS_VDDQ_VTT_REG PR6023 0.010 res_0603_30mil
2 VLDOIN
PC6005 10u 10V cap_0603_36mil
PMTP6003 SP-tp-c0p381
PMTP6004 SP-tp-c0p381
+1P2V_DUAL
DB,PWR_VTT

3 VTT
5 VTTSNS_VDDQ_VTT_REG PR6022 0 RES_0201_12mil
DNP,PWR_VTT PC6020 1000p 25V CAP_0201_14mil
PC6007 10u 10V cap_0603_36mil
4 PGND
GND

+V_VDDQ_VTT

Imax Y(+V_VDDQ_VTT) = 0.6 A (0.91 PPDG)
Imax U(+V_VDDQ_VTT) = 0.6 A (0.91 PPDG)

+V_VDDQ_VTT
Imax=1A
Trace Width>40mil

+V_VDDQ_VTT
Imax = 0.600A (15Jan15)

+3P3VSB
+1P2V_DUAL
PU6003
SLG5NT1477VTR
dfn9_1p5x2xp8_p4mm
1 VDD
2 D1
3-4 D2
9 ON
S1 5-6
S2 7
GND 8
[61] S0iX_EN

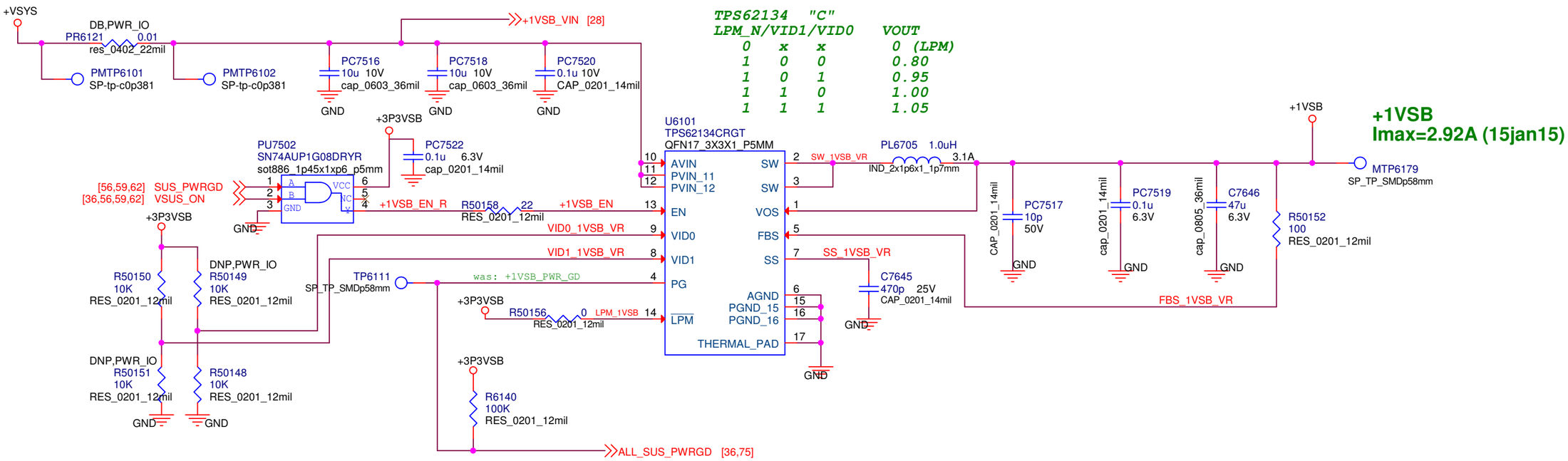
PC6022 0.1u 6.3V cap_0201_14mil
PC6025 1u 6.3V CAP_0201_14mil
GND

+VCCPLL_OC_REG
PC6023 1u 6.3V CAP_0201_14mil
PC6024 10u 10V cap_0603_36mil
GND

DB,PWR_PLL
PR6028 0.01 res_0402_22mil
PMTP6006 SP-tp-c0p381
+VCCPLL_OC
PMTP6005 SP-tp-c0p381

+VCCPLL_OC
Imax = 0.350A (15Jan15)

Title: +1P2V_DUAL&+VTT			
Microsoft	Engineer: Surface		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 60 of 76		


TPS62134 "C"
LPM_N/VID1/VID0 VOUT
0 x x 0 (LPM)
1 0 0 0.80
1 0 1 0.95
1 1 0 1.00
1 1 1 1.05
+1VSB
Imax=2.92A (15jan15)
+VCCSTG
Imax = 0.16A (15jan15)
+VCCST_CPU
160mA (15jan15)
+1V_MODPHY
Imax = 1.633 A (15jan15)
note: usb & pcie ports used
EV1.9 Add
EV1.9
WAS:INSTALL
Title: +1VSB
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 61 of 76

+VSYS
Iin=0.274A
Trace Width>30mil

+3P3VSB
DNP,PWR_1P8VSB
PR6201
100K
RES_0201_12mil

PU6202
TPS62140RGT
QFN17_3X3X1_P5MM

[56,59,61] SUS_PWRGD
[36,56,59,61] VSUS_ON
PR6203 0
RES_0201_12mil

+1P8VSB_VIN
PC6211 10u 10V cap_0603_36mil
PC6212 10u 10V cap_0603_36mil
PC6205 0.1u 10V CAP_0201_14mil
DB,PWR_1P8VSB
PR6205 0.01
res_0402_22mil
+VSYS
PMTP6202 SP-tp-c0p381
PMTP6201 SP-tp-c0p381

AVIN 10
PVIN3 12
PVIN2 11
PG 4
EN 13
+1P8VSB_EN
SW1 1
SW3 3
SW2 2
+1P8VSB_SW
PL6201 2.2uH 1.60A
ind_2x1p6x1_1p6mm
VOS 14
FSW 7
PR6225 100K
RES_0201_12mil
+1P8VSB_FSW
SS/TR 9
+1P8VSB_SS
DEF 8
FB 5
+1P8VSB_FB
PR6204 150K
RES_0201_12mil
AGND 6
GND 17
PGND1 16
PGND2 15
GND

PC6202 3300p 16V cap_0201_14mil
Tss=1.5ms

PC6218 10p 50V CAP_0201_14mil
EV1.9 was:6V
PC6203 22u 4V cap_0603_40mil
PC6204 22u 4V cap_0603_40mil

+1P8VSB
MTP6211 SP_TP_SMDp58mm
PR6214 100 RES_0201_12mil
+1P8VSB_disc

PR6211 120K RES_0201_12mil
R1 = R2 {Vout /Vref(0.8) - 1}

+1P8VSB
Imax=1.54A (15jan15)

+3P3VA
PR6215 499K RES_0201_12mil
+1P8VSB_DISC_CTRL
PQ6201A NX3008NBKS sot363_6_2x1p25x1p1_p65mm
PQ6201B NX3008NBKS sot363_6_2x1p25x1p1_p65mm

+1P8V_AUDIO
Imax=0.260A (15jan15)

+5VSB
PC6242 1u 6.3V CAP_0201_14mil
U6202
VDD 1
ON 2
D1-D2 3-4
S1-S2
CAP
GND
SLG59M1448V
dfn8_1p6X1Xp6_p4mm
DNP,PWR_1P8V_DUAL
[25,64] RTD3_AUD_PWR
PR6226 0
RES_0201_12mil
+1P8V_AUD_REG_EN
[36,47,56,61,62,64,65,75] SUSB_EC#
PR6227 0
RES_0201_12mil
+1P8VSB
C6248 6.3V 1u CAP_0201_14mil
5-6 +1P8V_AUD_REG
7 CAP_+1P8V_AUDIO
8
C6251 2200p 25V CAP_0201_14mil
PC6210 0.1u 6.3V cap_0201_14mil
DB,PWR_1P8V_DUAL
PR6210 0.01
res_0402_22mil
+1P8V_AUDIO
MTP6203 SP_TP_SMDp58mm
PMTP6204 SP-tp-c0p381
PMTP6203 SP-tp-c0p381

+1P8V
Imax=~0 (15jan15)

+1P8VSB
PC6206 1u 6.3V CAP_0201_14mil
PU6201
NX3P1108UK
bga4_2x2_p96xp96xp59_p5mm
A2 VIN VOUT A1
B2 EN GND B1
+1P8V_REG
[36,47,56,61,62,64,65,75] SUSB_EC#
PR6207 0
RES_0201_12mil
+1P8V_REG_EN
PC6207 0.1u 6.3V cap_0201_14mil
DB,PWR_1P8V
PR6202 0.01
res_0402_22mil
+1P8V
PMTP6208 SP-tp-c0p381
MTP6207 SP_TP_SMDp58mm
PMTP6207 SP-tp-c0p381

+1P8V_DUAL
Imax=0.620A (15jan15)

+5VSB
PC7526 1u 6.3V CAP_0201_14mil
U6203
VDD 1
ON 2
D1-D2 3-4
S1-S2
CAP
GND
SLG59M1448V
dfn8_1p6X1Xp6_p4mm
[36,45,60,61] SUSC_EC#
PR6233 0
RES_0201_12mil
+1P8V_DUAL_REG_EN
+1P8VSB
C6249 6.3V 1u CAP_0201_14mil
5-6 +1P8V_DUAL_REG
7 CAP_+1P8V_DUAL
8
C6252 2200p 25V CAP_0201_14mil
C6250 0.1u 6.3V cap_0201_14mil
DB,PWR_1P8V_DUAL
PR6231 0.01
res_0402_22mil
+1P8V_DUAL
MTP6205 SP_TP_SMDp58mm
PMTP6206 SP-tp-c0p381
PMTP6205 SP-tp-c0p381

+1P8V_TS
Imax=0.452A (15jan15)

+1P8VSB
PC6213 1u 6.3V CAP_0201_14mil
PU6205
NX3P1108UK
bga4_2x2_p96xp96xp59_p5mm
A2 VIN VOUT A1
B2 EN GND B1
+1P8V_TS_REG
[25,64] RTD3_TPANEL_PWR
PR6208 0
RES_0201_12mil
+1P8V_TS_REG_EN
PC6214 0.1u 6.3V cap_0201_14mil
DB,PWR_1P8_TS
PR6209 0.01
res_0402_22mil
+1P8V_TS
PMTP6210 SP-tp-c0p381
MTP6209 SP_TP_SMDp58mm
PMTP6209 SP-tp-c0p381

Title:	+1.8VSB & Load SW	
Microsoft	Engineer: Surface	
Size: A3	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 62 of 76	

CHGR_VIN
Iin=9.731A
Trace Width>389mil

+SYS
Iin=8A
Trace Width>320mil

+SYS
Imax = 12.0A
TDC = 10.0A

Cgs>=40*Cgd
Cgs*.9 >= 40*Cgd*1.1
Cgs >= (1.1/0.9)*40*1nF
Cgs >= 49nF

CHGR needs 200uF for loop stability
{2*f*pi = 1/sqrt(L*C)}

EffCap@20V=3.22uF*3=9.66uF

I(ripple)=Vin*DutyCycle*(1-DutyCycle)/(FreqSwitch*L)
I(ripple)= 20%~40% I(charge)
Vin(12.6V+/-10%) => I(ripple)@2.2uH => 1.93A, 40.5%
Vin(12.6V+/-10%) => I(ripple)@3.3uH => 1.29A, 27.0%
assuming 60W, DutyCycle=0.5, Freq=1020KHz

EV1.9 CHGR MSPN

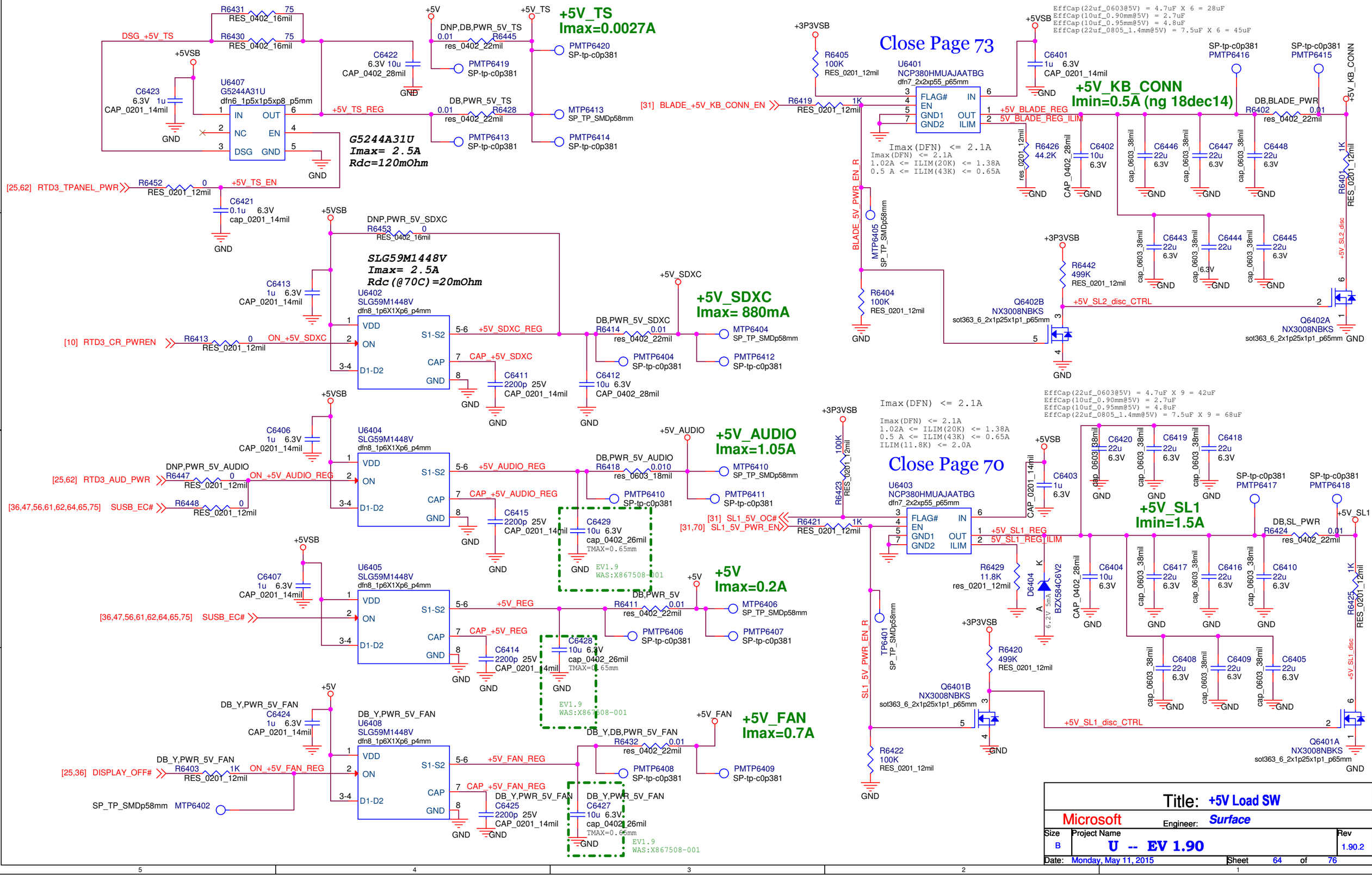
EV1.9 CHGR MSPN

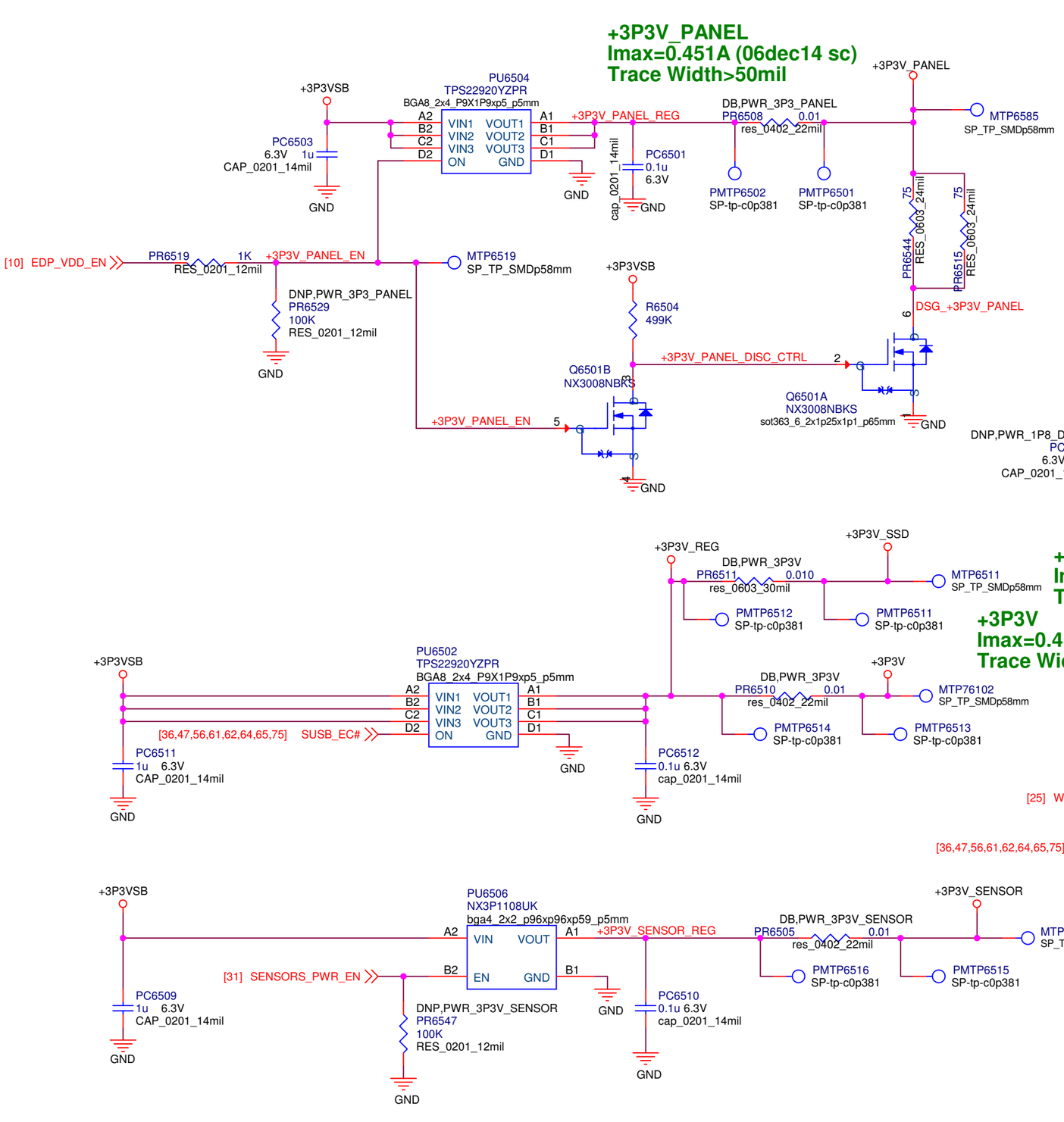
Title: CHARGER NVDC

Microsoft Engineer: Surface

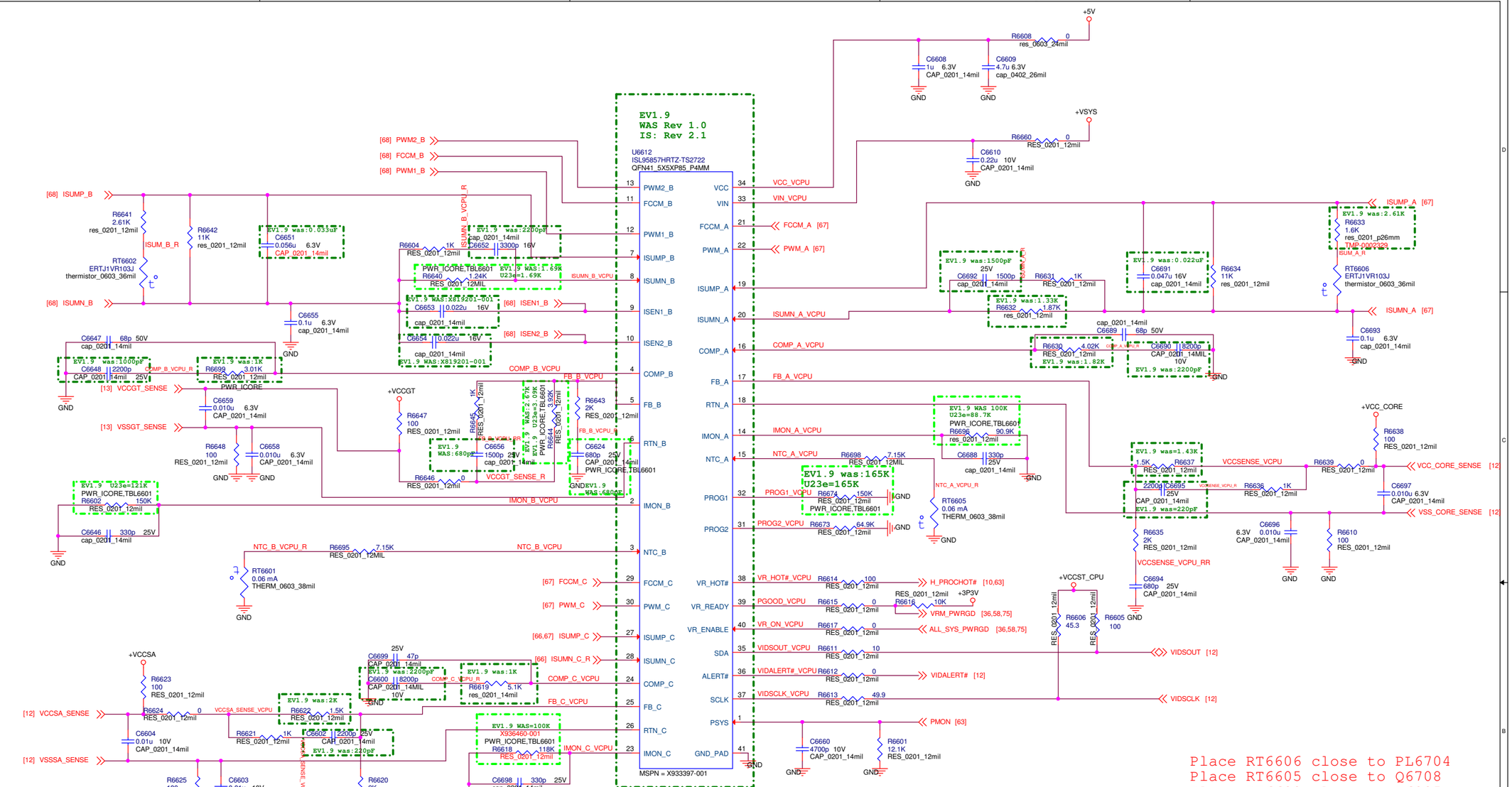
Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 63 of 76


+5V_TS
Imax=0.0027A
G5244A31U
Imax= 2.5A
Rdc=120mOhm
SLG59M1448V
Imax= 2.5A
Rdc(@70C)=20mOhm
+5V_SDXC
Imax= 880mA
+5V_AUDIO
Imax=1.05A
+5V
Imax=0.2A
+5V_FAN
Imax=0.7A
Close Page 73
+5V_KB_CONN
Imin=0.5A (ng 18dec14)
Close Page 70
+5V_SL1
Imin=1.5A
Imax(DFN) <= 2.1A
1.02A <= ILIM(20K) <= 1.38A
0.5 A <= ILIM(43K) <= 0.65A
ILIM(11.8K) <= 2.0A
EffCap(22uf_0603@5V) = 4.7uF X 6 = 28uF
EffCap(10uf_0.90mm@5V) = 2.7uF
EffCap(10uf_0.95mm@5V) = 4.8uF
EffCap(22uf_0805_1.4mm@5V) = 7.5uF X 6 = 45uF
EffCap(22uf_0603@5V) = 4.7uF X 9 = 42uF
EffCap(10uf_0.90mm@5V) = 2.7uF
EffCap(10uf_0.95mm@5V) = 4.8uF
EffCap(22uf_0805_1.4mm@5V) = 7.5uF X 9 = 68uF
Title: +5V Load SW
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 64 of 76



Title:	+3P3V Load SW	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 65 of 76	



	SKL-U 2+2 (15W)	SKL-U 2+3e (15W)
Intel SPEC		
ICCMAX/TDC of Vcore	28A/21A	29A/21A
ICCMAX/TDC of VCCGT	31A/18A	57A/32A
ICCMAX/TDC of VCCSA	4.5A/3.7A	5.1A/4.5A
ICCMAX/TDC of VCCGTx	N/A	7A/4A
DC_LL of Vcore	2.35 mohm	2.1 mohm
DC_LL of VCCGT	3.1 mohm	2 mohm
DC_LL of VCCSA	10.3 mohm	10.3 mohm
DC_LL of VCCGTx	N/A	6.9 mohm
Change items		
Vcore	No need to changed	No need to changed
VCCGT	R6674 : 150kohm (ICCMAX) R6640 : 1.24kohm (60A OCP) R6644 : 3.09kohm (LL 3.1mohm)	R6674 : 165kohm (ICCMAX) R6640 : 1.69kohm (80A OCP) R6644 : 2.68kohm(LL 2mohm)
VCCSA	No need to changed	No need to changed
VCCGTx	Disable U6916	Enable U6916

Place RT6606 close to PL6704
Place RT6605 close to Q6708
Place RT6602 close to L6805
Place RT6601 close to Q6811
Place RT6607 close to L6703
Place RT6904 close to Q6916
Place RT6903 close to PL6905

	U22	U23E
R6674	150K	165K
R6696	90.9K	88.7K
R6644	3.92K	3.09K
C6624	680pF	390pF
R6640	1.24K	1.69K
R6602	150K	121K
R6618	118K	100K

Title: VCPU contoller
Microsoft
Engineer: Surface
Size: C
Project Name: U -- EV 1.90
Rev: 1.90.2
Date: Monday, May 11, 2015
Sheet 66 of 76

9V to 12V

+VSYS

+VCORE_IN

DB,PWR_CORE
PR6712 0.010
res_0603_30mil

PMTP6702
SP-tp-c0p381

PMTP6701
SP-tp-c0p381

+5V

C6761
4.7u 10V
cap_0402_26mil

GND

U6713
ISL95808HRZ
dfn9_2x2x1_p5mm-2

VCC
FCCM
PWM
UGATE
PHASE
BOOT
LGATE
GND
MTG

[66] FCCM_A

[66] PWM_A

UGATE_VCORE

PHASE_VCORE

LGATE_VCORE

Q6710
BSZ065N03LS
mosfet8_3p3x3p3x1p1_65mm

5-8
D
G
S
1-3

CAP_0201_14mil
PC6714
1000p 25V

cap_0603_36mil
PC6715
10u 10V

PCE6743 22u 25V
20
CAP_3P5X2P8X2P1MM

+VCC_CORE

Icc(max) <= 29A
TDC[A] <= 21A

PL6704 0.15UH, 20A
18A
ind_7p05x6p6x1p8_6p05mm

EV1.9 WAS:3.65K

R6750
1.1K
RES_0402_16mil

ISUMP_A [66]

R6751
0
RES_0402_16mil

[66] ISUMN_A

C6762
220u 2V

C6763
220u 2V

cap_3_7p3x4p3x1_6p1mm

BOOT_VCORE

R6749 0
res_0603_24mil

PHASE_R_VCORE

C6760 0.22u 25V
cap_0603_36mil

Q6708
BSZ019N03LS
mosfet8_3p3x3p3x1p1_65mm

+5V

C6765
4.7u 10V
cap_0402_26mil

U6714
ISL95808HRZ
dfn9_2x2x1_p5mm-2

[66] FCCM_C

[66] PWM_C

UGATE_VCCSA

PHASE_VCCSA

LGATE_VCCSA

Q6706
BSZ0907ND
mosfet10_3x3xp9_p65mm

+VCCSA_IN

PC6716
1000p 25V
CAP_0201_14mil

PC6717
10u 10V
cap_0603_36mil

PC6718
10u 10V
cap_0603_36mil

DB,PWR_SA
PR6714 0.010
res_0603_30mil

PMTP6704
SP-tp-c0p381

PMTP6703
SP-tp-c0p381

+VSYS

Icc(max) <= 5.1A
TDC[A] <= 4.5A

X905644-001
L6703 0.56uH
6.5A
ind_4x15x4x2_3p7mm

R6753
3.65K
res_0402_22mil

ISUMP_C [66]

R6754
0
RES_0402_16mil

[66] ISUMN_C

PC6766
47u 6.3V
cap_0805_36mil

PC6719
47u 6.3V
cap_0805_36mil

+VCCSA

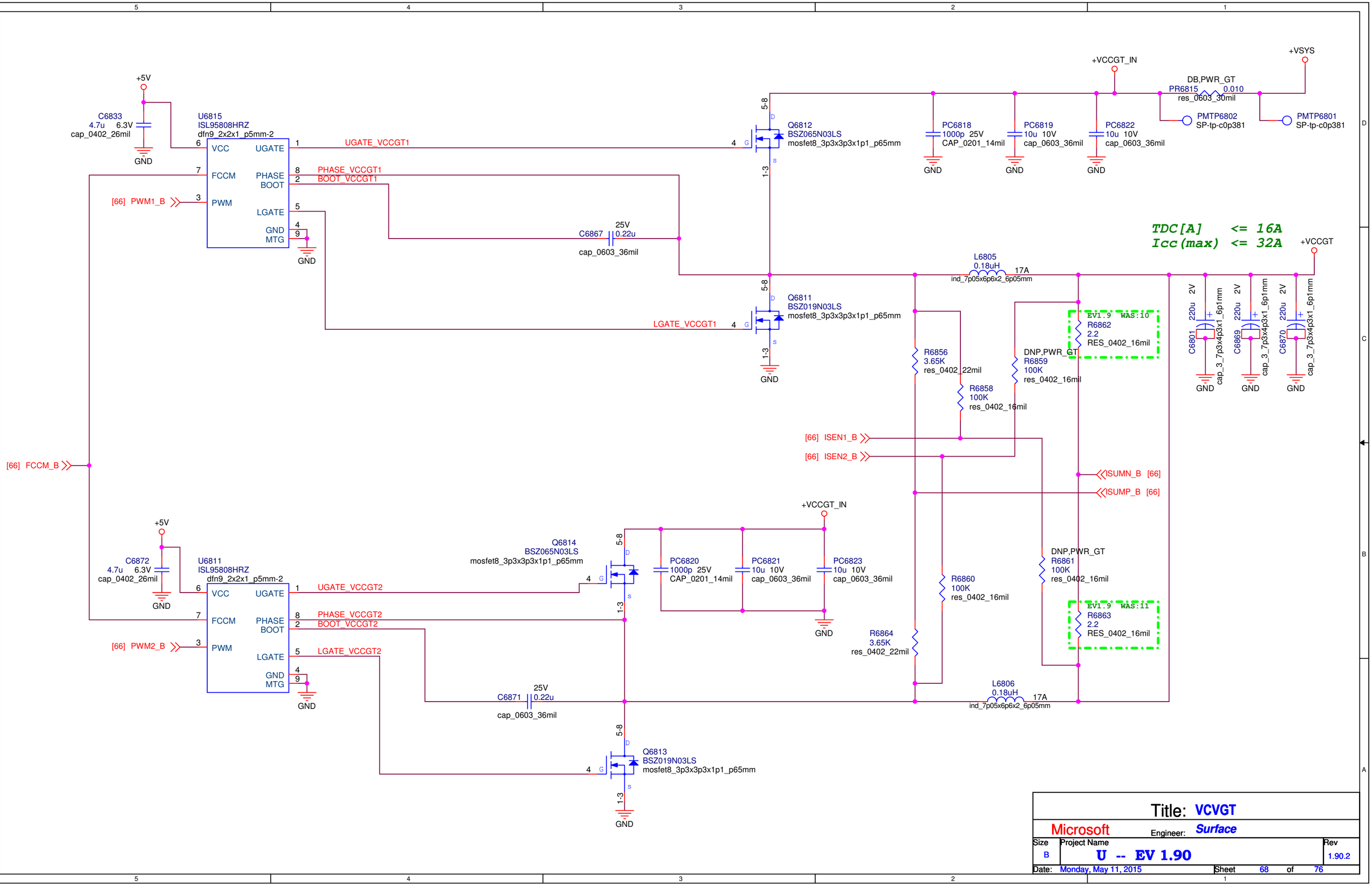
BOOT_VCCSA

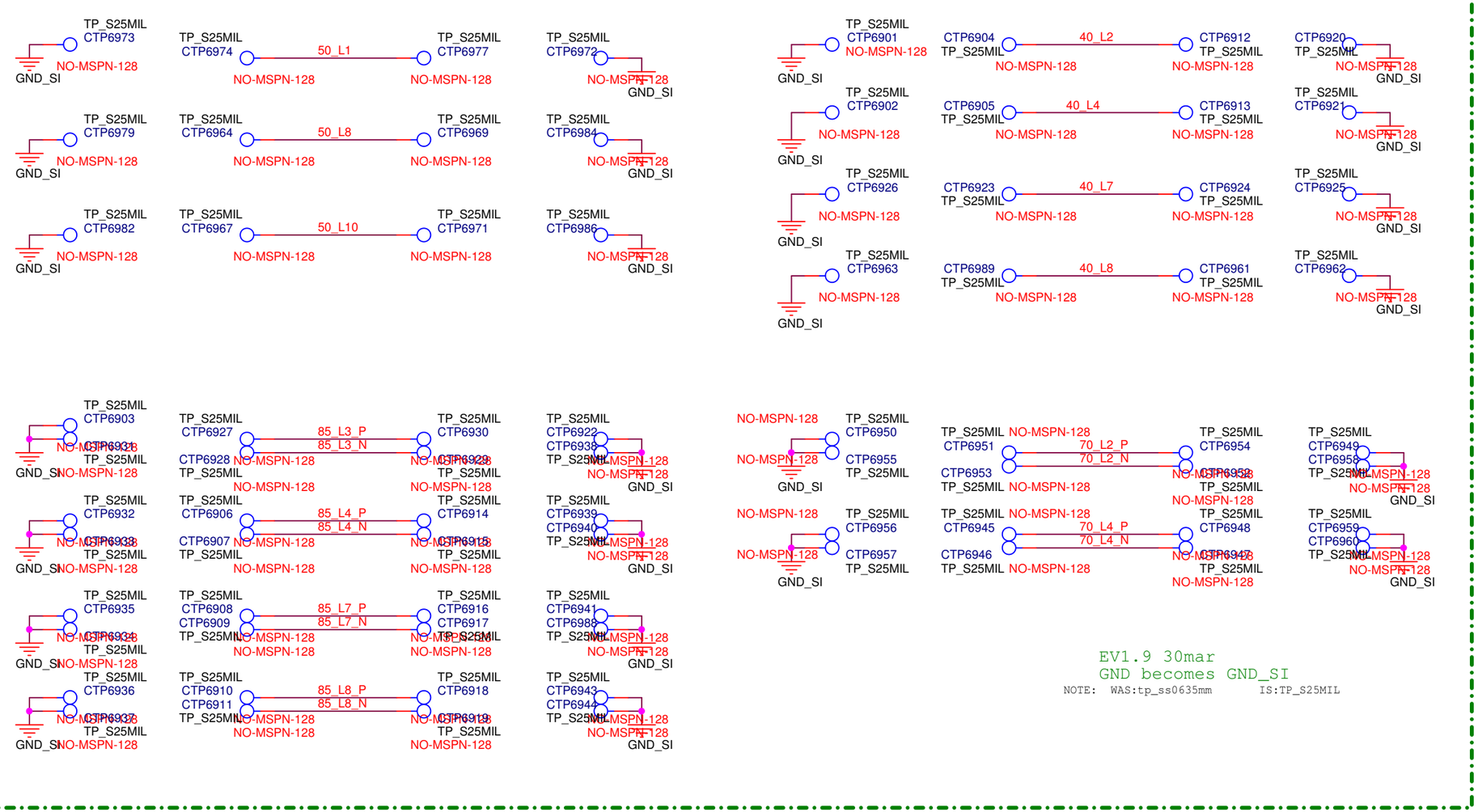
R6752 0
res_0603_24mil

PHASE_R_VCCSA

C6764 0.22u 25V
cap_0603_36mil

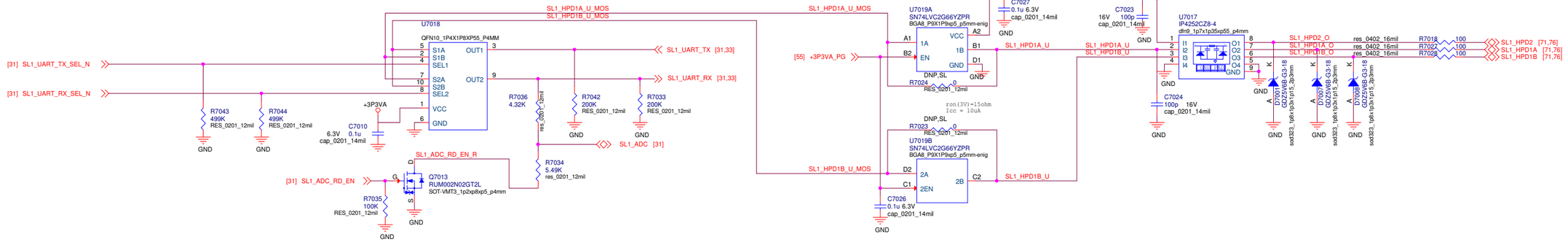
Title: VCORE VCCSA			
Microsoft	Engineer: Surface		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015		Sheet 67 of 76	


+5V
C6833
4.7u 6.3V
cap_0402_26mil
GND
U6815
ISL95808HRZ
dfn9_2x2x1_p5mm-2
VCC
FCCM
PWM
UGATE
PHASE
BOOT
LGATE
GND
MTG
[66] PWM1_B
UGATE_VCCGT1
PHASE_VCCGT1
BOOT_VCCGT1
LGATE_VCCGT1
C6867
25V
0.22u
cap_0603_36mil
Q6812
BSZ065N03LS
mosfet8_3p3x3p3x1p1_p65mm
Q6811
BSZ019N03LS
mosfet8_3p3x3p3x1p1_p65mm
+VCCGT_IN
PC6818
1000p 25V
CAP_0201_14mil
PC6819
10u 10V
cap_0603_36mil
PC6822
10u 10V
cap_0603_36mil
DB,PWR_GT
PR6815
0.010
res_0603_30mil
+VSYS
PMTP6802
SP-tp-c0p381
PMTP6801
SP-tp-c0p381
TDC[A] <= 16A
Icc(max) <= 32A
L6805
0.18uH
17A
ind_7p05x6p6x2_6p05mm
+VCCGT
C6801
C6869
C6870
220u 2V
cap_3_7p3x4p3x1_6p1mm
R6856
3.65K
res_0402_22mil
R6858
100K
res_0402_16mil
DNP,PWR_GT
R6859
100K
res_0402_16mil
EV1.9 WAS:10
R6862
2.2
RES_0402_16mil
[66] ISEN1_B
[66] ISEN2_B
ISUMN_B [66]
ISUMP_B [66]
[66] FCCM_B
+5V
C6872
4.7u 6.3V
cap_0402_26mil
U6811
ISL95808HRZ
dfn9_2x2x1_p5mm-2
[66] PWM2_B
UGATE_VCCGT2
PHASE_VCCGT2
BOOT_VCCGT2
LGATE_VCCGT2
Q6814
BSZ065N03LS
mosfet8_3p3x3p3x1p1_p65mm
Q6813
BSZ019N03LS
mosfet8_3p3x3p3x1p1_p65mm
+VCCGT_IN
PC6820
1000p 25V
CAP_0201_14mil
PC6821
10u 10V
cap_0603_36mil
PC6823
10u 10V
cap_0603_36mil
C6871
25V
0.22u
cap_0603_36mil
R6860
100K
res_0402_16mil
R6864
3.65K
res_0402_22mil
DNP,PWR_GT
R6861
100K
res_0402_16mil
EV1.9 WAS:11
R6863
2.2
RES_0402_16mil
L6806
0.18uH
17A
ind_7p05x6p6x2_6p05mm
Title: VCVGT
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 68 of 76

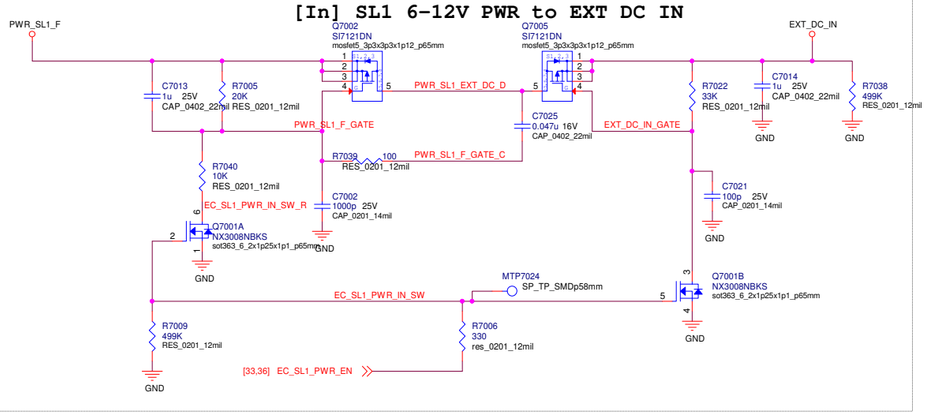


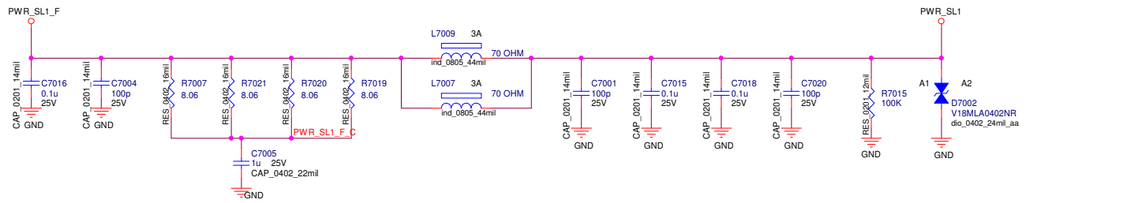
Title:	SI Coupon (was BOOST/GTX REG)	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 69 of 76	

HPD FOR SL1 (ONE/TWO WIRE UART)

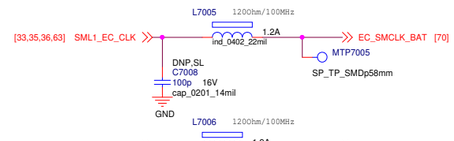


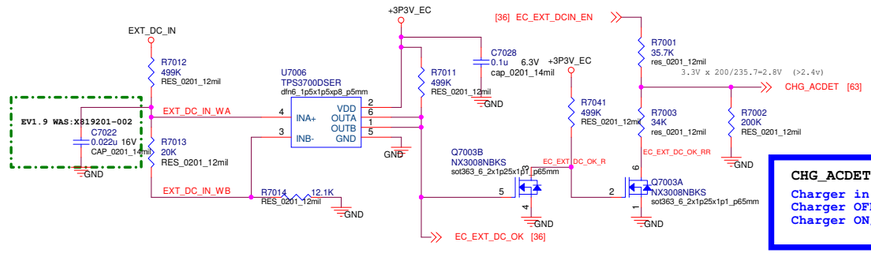
[In] SL1 6-12V PWR to EXT DC IN





Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed

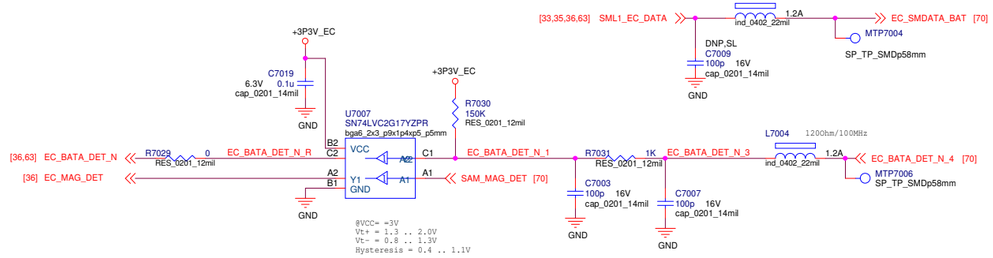


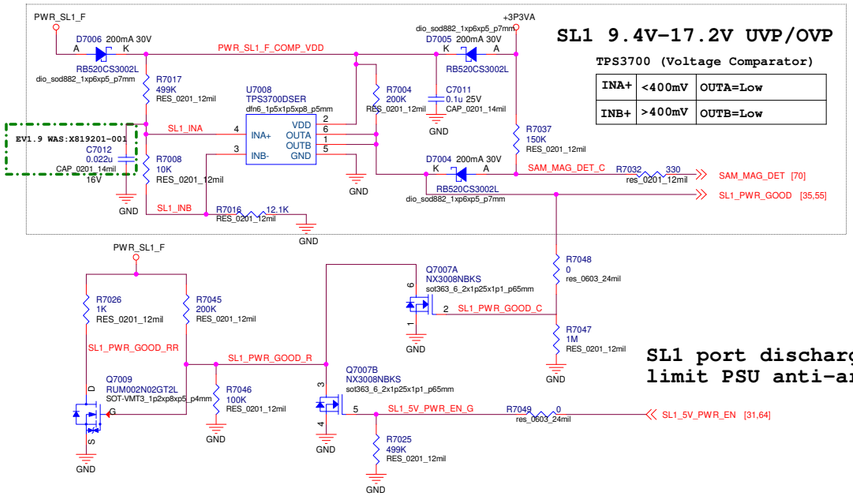


TPS3700 (Voltage Comparator)

INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

CHG_ACDET	EC_EXT_DCIN_EN	EXT_DC_IN >9V
Charger in RESET	0	X
Charger OFF/ SMBUS EN	1	No
Charger ON/ SMBUS EN	1	YES



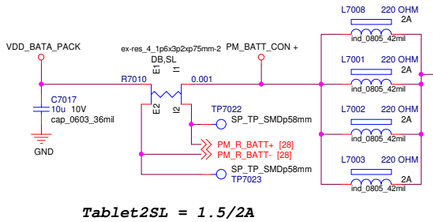


SL1 9.4V-17.2V UVP/OVP

TPS3700 (Voltage Comparator)

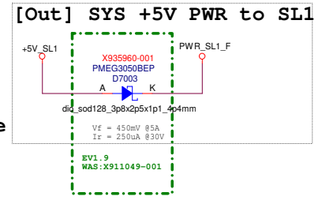
INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

SL1 port discharger limit PSU anti-arc pulse voltage



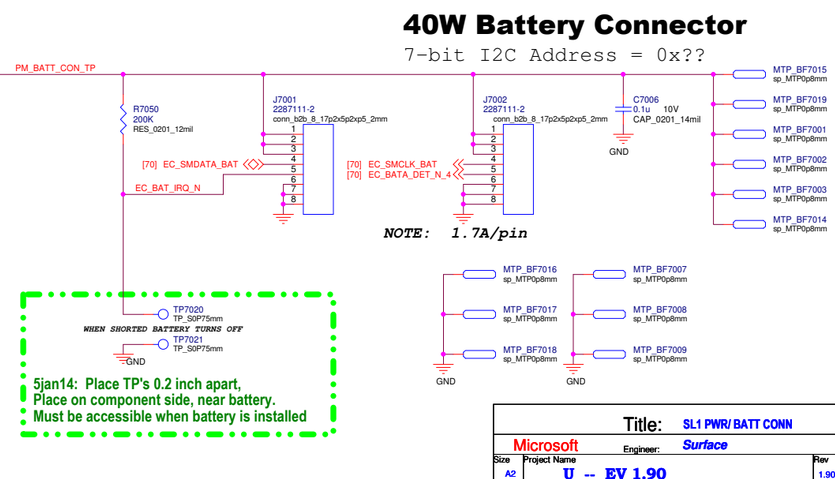
Tablet2SL = 1.5/2A

[Out] SYS +5V PWR to SL1



40W Battery Connector

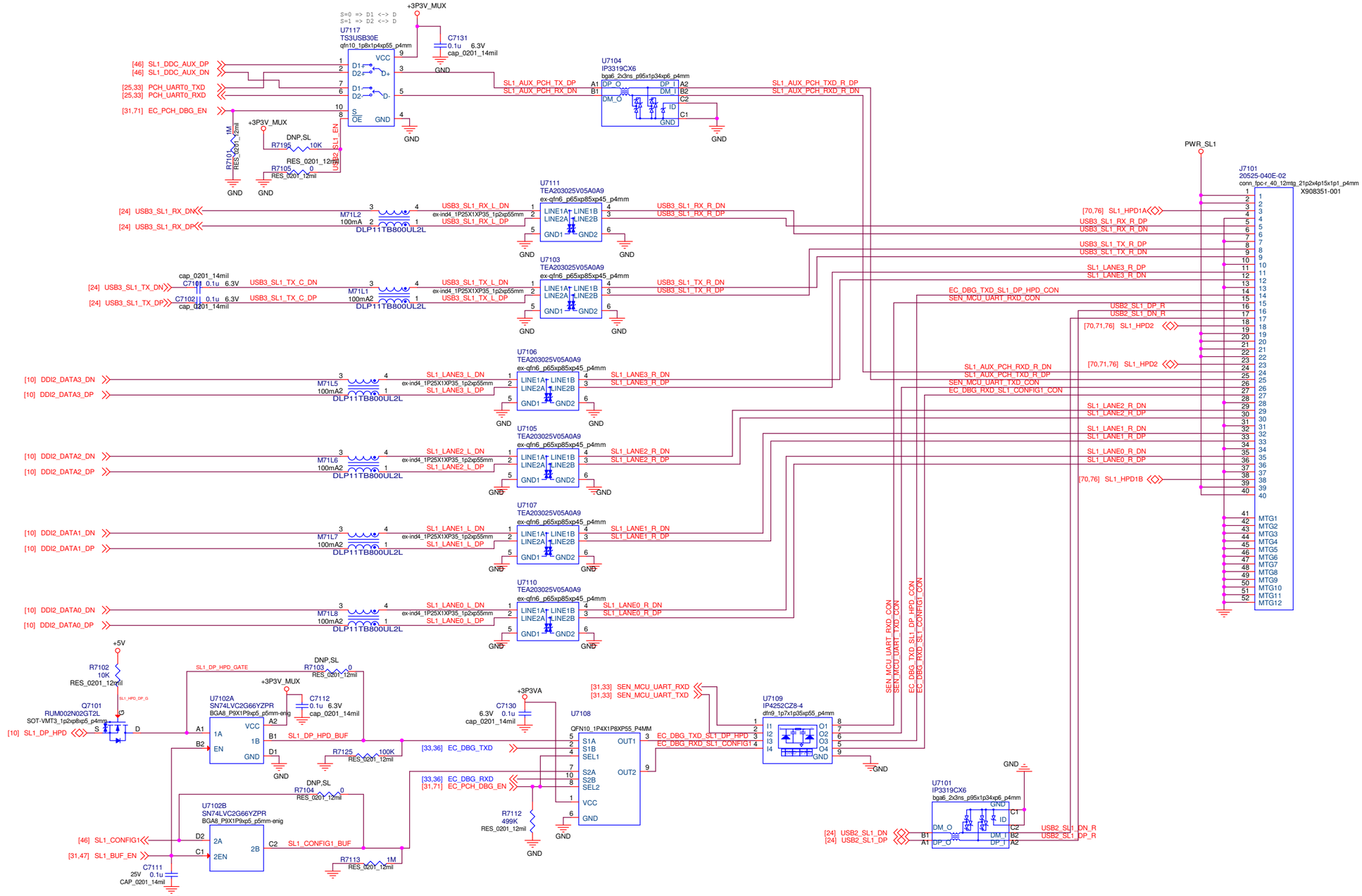
7-bit I2C Address = 0x??



NOTE: 1.7A/pin

5jan14: Place TP's 0.2 inch apart, Place on component side, near battery. Must be accessible when battery is installed

Title:	SL1 PWR/ BATT CONN		
Microsoft	Engineer:	Surface	
Size: A2	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 70 of 76		


U7117
TS3USB30E
qfn10_1p8x1p4xp55_p4mm
S=0 => D1 <-> D
S=1 => D2 <-> D
+3P3V_MUX
C7131
0.1u 6.3V
cap_0201_14mil
[46] SL1_DDC_AUX_DP
[46] SL1_DDC_AUX_DN
[25,33] PCH_UART0_TXD
[25,33] PCH_UART0_RXD
[31,71] EC_PCH_DBG_EN
SL1_AUX_PCH_TX_DP
SL1_AUX_PCH_RX_DN
U7104
IP3319CX6
bga6_2x3ns_p95x1p34xp6_p4mm
SL1_AUX_PCH_TXD_R_DP
SL1_AUX_PCH_RXD_R_DN
R7101 1M RES_0201_12mil
R7105 0 RES_0201_12mil
R7195 10K RES_0201_12mil
DNP,SL
U7102
SL1_EN
[24] USB3_SL1_RX_DN
[24] USB3_SL1_RX_DP
M71L2
100mA2
DLP11TB800UL2L
U7111
TEA203025V05A0A9
ex-qfn6_p65xp85xp45_p4mm
USB3_SL1_RX_L_DN
USB3_SL1_RX_L_DP
USB3_SL1_RX_R_DN
USB3_SL1_RX_R_DP
[24] USB3_SL1_TX_DN
[24] USB3_SL1_TX_DP
C7101 0.1u 6.3V
C7102 0.1u 6.3V
cap_0201_14mil
USB3_SL1_TX_C_DN
USB3_SL1_TX_C_DP
M71L1
U7103
USB3_SL1_TX_L_DN
USB3_SL1_TX_L_DP
USB3_SL1_TX_R_DN
USB3_SL1_TX_R_DP
[10] DDI2_DATA3_DN
[10] DDI2_DATA3_DN
M71L5
U7106
SL1_LANE3_L_DN
SL1_LANE3_L_DP
SL1_LANE3_R_DN
SL1_LANE3_R_DP
[10] DDI2_DATA2_DN
[10] DDI2_DATA2_DP
M71L6
U7105
SL1_LANE2_L_DN
SL1_LANE2_L_DP
SL1_LANE2_R_DN
SL1_LANE2_R_DP
[10] DDI2_DATA1_DN
[10] DDI2_DATA1_DP
M71L7
U7107
SL1_LANE1_L_DN
SL1_LANE1_L_DP
SL1_LANE1_R_DN
SL1_LANE1_R_DP
[10] DDI2_DATA0_DN
[10] DDI2_DATA0_DP
M71L8
U7110
SL1_LANE0_L_DN
SL1_LANE0_L_DP
SL1_LANE0_R_DN
SL1_LANE0_R_DP
PWR_SL1
J7101
20525-040E-02
conn_fpc-r_40_12mtg_21p2x4p15x1p1_p4mm
X908351-001
[70,76] SL1_HPD1A
[70,71,76] SL1_HPD2
[70,71,76] SL1_HPD2
[70,76] SL1_HPD1B
MTG1
MTG2
MTG3
MTG4
MTG5
MTG6
MTG7
MTG8
MTG9
MTG10
MTG11
MTG12
EC_DBG_TXD_SL1_DP_HPD_CON
SEN_MCU_UART_RXD_CON
SEN_MCU_UART_TXD_CON
EC_DBG_RXD_SL1_CONFIG1_CON
USB2_SL1_DP_R
USB2_SL1_DN_R
SL1_AUX_PCH_RXD_R_DN
SL1_AUX_PCH_TXD_R_DP
SL1_LANE2_R_DN
SL1_LANE2_R_DP
SL1_LANE1_R_DN
SL1_LANE1_R_DP
SL1_LANE0_R_DN
SL1_LANE0_R_DP
USB3_SL1_RX_R_DP
USB3_SL1_RX_R_DN
USB3_SL1_TX_R_DP
USB3_SL1_TX_R_DN
SL1_LANE3_R_DP
SL1_LANE3_R_DN
+5V
R7102 10K RES_0201_12mil
Q7101
RUM002N02GT2L
SOT-VMT3_1p2xp8xp5_p4mm
[10] SL1_DP_HPD
SL1_DP_HPD_GATE
SL1_HPD_DP_G
U7102A
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm-enig
R7103 0 RES_0201_12mil
C7112 0.1u 6.3V cap_0201_14mil
R7125 100K RES_0201_12mil
SL1_DP_HPD_BUF
[33,36] EC_DBG_TXD
U7102B
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm-enig
R7104 0 RES_0201_12mil
[46] SL1_CONFIG1
[31,47] SL1_BUF_EN
C7111 25V 0.1u CAP_0201_14mil
R7113 1M RES_0201_12mil
SL1_CONFIG1_BUF
[33,36] EC_DBG_RXD
[31,71] EC_PCH_DBG_EN
+3P3VA
C7130 6.3V 0.1u cap_0201_14mil
R7112 499K RES_0201_12mil
U7108
QFN10_1P4X1P8XP55_P4MM
EC_DBG_TXD_SL1_DP_HPD
EC_DBG_RXD_SL1_CONFIG1
[31,33] SEN_MCU_UART_RXD
[31,33] SEN_MCU_UART_TXD
U7109
IP4252CZ8-4
dfn9_1p7x1p35xp55_p4mm
U7110I
IP3319CX6
bga6_2x3ns_p95x1p34xp6_p4mm
[24] USB2_SL1_DN
[24] USB2_SL1_DP
USB2_SL1_DN_R
USB2_SL1_DP_R
Title: SL1 SIGNALS
Microsoft
Engineer: Surface
Size C
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 71 of 76

+3P3VAS
R7201
499K
RES_0201_12mil
+3P3V_HDP_EN
[31] SL1_3P3V_DIS
Q7201
RUM002N02GT2L
SOT-VMT3_1p2xp8xp5_p4mm
R7206
499K
RES_0201_12mil
GND
GND
U7201
RT9728AHZQW
dfn7_2x2xp8_p65mm-2
+3P3V_HDP_EN
EN/EN#
FAULT#
VIN
ILIM
VOUT
GND1
GND2
+3P3V_HDP
Imax=75mA
+3P3V_HDP
MTP7283
SP_TP_SMDp58mm
+3P3VAS
DB,PWR_3P3V_HPD
R7202 0.01
res_0402_22mil
C7209
10u 6.3V
CAP_0402_28mil
R7203 0
RES_0201_12mil
+3P3V_HPD_VIN
+3P3V_HPD_ILIMIT
DNP,PWR_3P3V_HPD
R7204
33K
RES_0201_12mil
C7202
10u 6.3V
CAP_0402_28mil
C7203
10u 6.3V
CAP_0402_28mil
isolated ground on layer 2 to tie Cin GND, Cout GND, and controller PGND together. Then tie this isolated ground plane to main GND under the exposed pads.

+VCC_EDP_BKLT_IN_REG [28]
SP-tp-c0p381
PMTP7221
SP-tp-c0p381
PMTP7222
+VSYS
Q7203
IRLML6402
SOT23_2p9X1P3X1P12_P95MM
DB,PWR_BKLT
R7209 0.01
res_0402_22mil
R7213
100K
RES_0201_12mil
C7224
1000p 25V
CAP_0201_14mil
DNP,PWR_BKLT
C7225
0.1u 10V
CAP_0201_14mil
BKLT_EDP_IN_DRI
R7212
200K
RES_0201_12mil
R7210
4.99K
RES_0201_12mil
R7211
4.99K
RES_0201_12mil
+VCC_EDP_BKLT_IN_DISC
Q7202B
SSM6N15AFU
SOT363_6_2x1p25X1_P65MM
BKLT_EDP_IN_DRI_R
+3P3V_PANEL
R7215 22K
RES_0201_12mil
R7214
100K
RES_0201_12mil
BKLT_EDP_IN_R
DNP,PWR_BKLT
C7253
0.1u 6.3V
cap_0201_14mil
Q7202A
SSM6N15AFU
SOT363_6_2x1p25X1_P65MM
GND

jks 15dec14:
EffCap (10u@8.7V) = 1.4uF
EffCap (22u@8.7V) = 3.6uF
Novatek: Cin = 4.7uF
+VCC_EDP_BKLT_IN
C7210
22u 10V
cap_0603_40mil
C7201
10u 10V
cap_0603_36mil

+VCC_EDP_BKLT_IN
Imax=??A
TDC=??A
Novatek 15dec14: Ipeak(Vin=6V) = 1.144A
L7204 10uH 2.5A
ind_5p4x5p2x1p8mm
X911507-001
Rdc = 154mOhm
X913828-001
PMEG6030EVP
D7201
dio_sod128_3p8x2p5x1p1_4p4mm
BKLT_LX
+VCC_EDP_BKLT_OUT_R
R7333 0
RES_0402_16mil
+VCC_EDP_BKLT_OUT
MTP7201
SP_TP_SMDp58mm

jks 15dec14:
EffCap (10u@28V) = 1.5uF
EffCap (4.7u@28V) = 0.8uF
Novatek: Cout = 4.7uF

R7230
681K
res_0201_12mil
R7231
20K
RES_0201_12mil
C7206 10u 50V cap_1206_72mil
C7207 10u 50V cap_1206_72mil DNP,PWR_BKLT
C7208 10u 50V cap_1206_72mil DNP,PWR_BKLT
EV1.9
was:INSTALL

R7207 10
res_0603_22mil
+VCC_BKLT
C7204 1u 10V
CAP_0402_22mil
EV1.9
WAS 0603

EV1.9
WAS NNT50273QG/A
U7202
MP3388SGR
qfn25_4x4xp9_p5mm
VIN
EN
OSC
PWMI
ISET
PWMO
COMP
PGND2
PGND1
AGND1
AGND2
VCC
SW2
SW1
OVP
LED8
LED7
LED6
LED5
LED4
LED3
LED2
LED1
FPWM
VFAULT
C7255
1u 10V
CAP_0402_22mil

[10] L_BKLTEN
R7208 1K
RES_0201_12mil
BKLT_EN
MTP7224
MTP7225
R7228 10K
RES_0201_12mil
BKLKT_OSC
BKLT_PWM_R
[57] L_BKLT_CTRL_OUT
R7226 1K
RES_0201_12mil
R7227 X936061-001 90.9K
res_0201_12mil
BKLT_ISET
R7232 0.068u
cap_0201_14mil
BKLT_MIX
C7211 0.47u
cap_0201_14mil
BKLT_COMP_R
R7229 X933171-001 270
res_0201_12mil
BKLT_COMP
BKLT_OVS
BKLT_FB8_R
BKLT_FB7_R
BKLT_FB6_R
BKLT_FB5_R
BKLT_FB4_R
BKLT_FB3_R
BKLT_FB2_R
BKLT_FB8_1
BKLT_SC1
BKLT_NG2
R7218 0
R7219 0
R7220 0
R7221 0
R7222 0
R7223 0
R7224 0
R7225 0
RES_0201_12mil
BKLT_FB8 [57,72]
BKLT_FB7 [57,72]
BKLT_FB6 [57,72]
BKLT_FB5 [57,72]
BKLT_FB4 [57,72]
BKLT_FB3 [57,72]
BKLT_FB2 [57,72]
BKLT_FB1 [57,72]
PWR_BKLT
C7254
150p 50V
CAP_0402_22mil
EV1.9 install
DNP,PWR_BKLT
R7239
1K
RES_0201_12mil

MTP7202 SP_TP_SMDp58mm BKLT_FB1 [57,72]
MTP7203 SP_TP_SMDp58mm BKLT_FB2 [57,72]
MTP7206 SP_TP_SMDp58mm BKLT_FB3 [57,72]
MTP7210 SP_TP_SMDp58mm BKLT_FB4 [57,72]
MTP7204 SP_TP_SMDp58mm BKLT_FB5 [57,72]
MTP7205 SP_TP_SMDp58mm BKLT_FB6 [57,72]
MTP7207 SP_TP_SMDp58mm BKLT_FB7 [57,72]
MTP7208 SP_TP_SMDp58mm BKLT_FB8 [57,72]

Title: +3P3V_HPD/LCD backlight
Microsoft
Engineer: Surface
Size: B
Project Name: U -- EV 1.90
Rev: 1.90.2
Date: Monday, May 11, 2015
Sheet 72 of 76

BLADE Connector

+5V_KB_CONN
Imax = 0.5A

SP_TP_SMDp58mm MTP7314
SP_TP_SMDp58mm MTP7315
SP_TP_SMDp58mm MTP7316
SP_TP_SMDp58mm MTP7317

[74] BLADE_TX_USB_D+
[74] BLADE_RX_USB_D-
[74] +5V_SHA_CONN_UART_RX_CONN
[74] BLADE_AUTH_DATA_UART_TX_CONN

J7302
2287111-2
conn_b2b_8_17p2x5p2xp5_2mm
X904496-001
1 2 3 4 5 6 7 8
GND

MTP_BF7305 sp_MTP0p8mm
MTP_BF7306 sp_MTP0p8mm
MTP_BF7313 sp_MTP0p8mm
MTP_BF7314 sp_MTP0p8mm
GND

MTP_BF7309 sp_MTP0p8mm
MTP_BF7310 sp_MTP0p8mm
MTP_BF7311 sp_MTP0p8mm
MTP_BF7312 sp_MTP0p8mm

FANG_PWR
D7301
A1 A2
V18MLA0402NR
dio_0402_24mil_aa
GND
R7301
100K
RES_0201_12mil
GND
C7301
0.1u 25V
CAP_0402_22mil
GND
L7301 220 OHM
2A
ind_0805_42mil
FANG_PWR_F

+5V_KB_CONN
L7304 120Ohm/100MHz
ind_0402_22mil
1.2A
+5V_KB
C7302
0.1u 6.3V
cap_0201_14mil
GND
A1 A2
D7302
V18MLA0402NR
dio_0402_24mil_aa
GND

SP_TP_SMDp58mm MTP7319
SP_TP_SMDp58mm MTP7318
GND

FANG_PWR
J7303
2287111-2
conn_b2b_8_17p2x5p2xp5_2mm
X904496-001
1 2 3 4 5 6 7 8
GND

eFang power = 3.5A max
using +1 rule

[In] BLADE 6-12V PWR to EXT DC IN

Imax=4.5A

EXT_DC_IN
Q7303
SI7121DN
mosfet5_3p3x3p3x1p12_p65mm
R7302
33K
RES_0201_12mil
EXT_DC_IN_FET_GATE
DNP,BLADE
C7310
1000p 25V
CAP_0201_14mil
GND
Q7302A
NX3008NBKS
sot363_6_2x1p25x1p1_p65mm
GND
FANG_DRAIN_FET_PWR
Q7301
SI7121DN
mosfet5_3p3x3p3x1p12_p65mm
DNP,BLADE
C7303
25V 0.047u
CAP_0402_22mil
DNP,BLADE
R7318 100
RES_0201_12mil
FANG_PWR_F
EV1.9
WAS 0603
C7304
1u 25V
CAP_0402_22mil
FANG_PWR_FET_GATE
R7304 20K
RES_0201_12mil
R7310
10K
RES_0201_12mil
DNP,BLADE
C7309 25V
1000p
CAP_0201_14mil
GND
EC_BLADE_PWR_IN_SW
Q7302B
NX3008NBKS
sot363_6_2x1p25x1p1_p65mm
MTP7301
SP_TP_SMDp58mm
R7308
499K
RES_0201_12mil
GND
R7303
330
RES_0402_16mil
[33,36] EC_BLADE_PWR_EN
GND

[31] BLADE_AUTH_PWR_EN
GND
R7311 1M
RES_0201_12mil

Rds(on)=120mOhm (typ)
Iq=170uA

+5VA_SHA
R7307 100K
RES_0201_12mil
+5VA_SHA
DB,BLADE
R7314 0.01
res_0402_22mil
PMTP7321
SP-tp-c0p381
PMTP7322
SP-tp-c0p381
BLADE
R7313 0
RES_0402_16mil
C7306
10u 6.3V
cap_0603_38mil
GND
EV1.9
CHG MSPN

U7301
RT9728AHZQW
dfn7_2x2xp8_p65mm-2
4 EN/EN# VOUT 1
3 FAULT#
6 VIN GND1 5
2 ILIM GND2 7
SHA_OC#
SHA_VIN
SHA_ILIMIT
DNP,BLADE
R7319
33K
RES_0201_12mil
GND

+5V_SHA_CONN
+5V_SHA_CONN
Imax=75mA
C7305 0.1u 6.3V cap_0201_14mil GND
R7305 2.2K RES_0201_12mil GND
C7307 1u 6.3V CAP_0201_14mil GND
C7308 22p 25V CAP_0201_14mil GND

Imax = 1.4A
50mA <= ILIM(connected to VIN) <=100mA

+VSYS
L7313 30OHMS @100MHZ
1.7A
IND_0402_24mil
L7312 30OHMS @100MHZ
1.7A
IND_0402_24mil
FANG_PWR_IN
C7312
2.2u
CAP_0603_38mil
25V
GND
C7313
0.1u
CAP_0201_14mil
25V
GND

V(operating) = 4.5 to 13.8 Max

U7302
TPS2592ZADRCR
son11_3x3x1_p5mm
5 VIN3 OUT1 6
4 VIN2 OUT2 7
3 VIN1 OUT3 8
BFET 9
2 EN/UVLO dV/dT ILIM 10 FANG_REG_ILIM
1 GND_PAD 11
GND

current = 3A
FANG_PWR_OUT
C7316
0.1u
CAP_0201_14mil
25V
GND
C7317
2.2u
CAP_0603_38mil
25V
GND

X935960-001
PMEG3050BEP
D7303
A K
dio_sod128_3p8x2p5x1p1_4p4mm
Vf = 450mV @5A
Ir = 250uA @30V
EV1.9
WAS:X911049-001

FANG_PWR_F
C7315
2.2u
CAP_0603_38mil
25V
GND

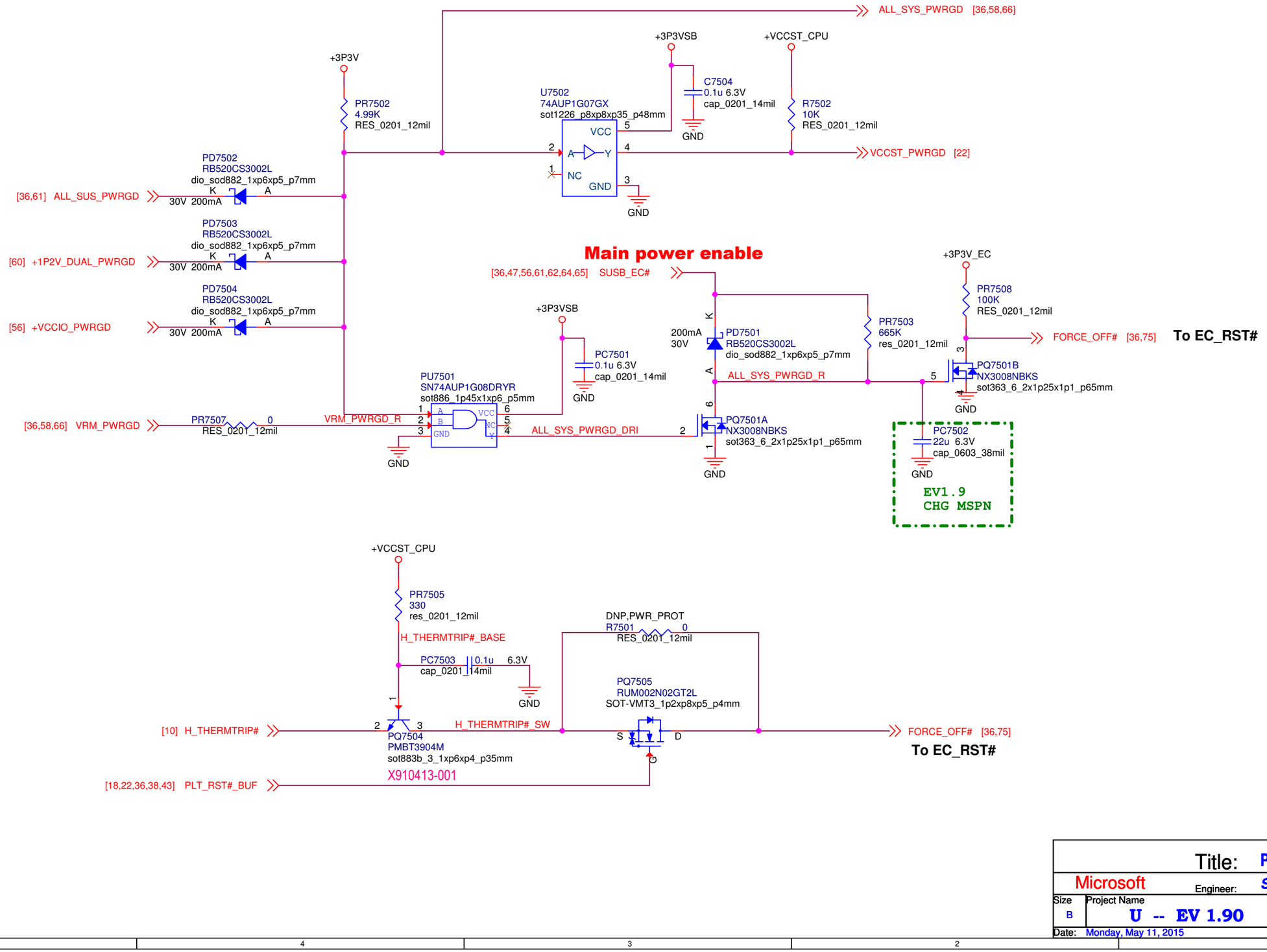
LTE eFANG PWR = 2.10A(min)
2.47A(nom)
2.84A(max)

[36] EC_BLADE_5VLDSW_EN
R7309 0
RES_0201_12mil
R7315
100K
RES_0201_12mil
GND
C7314
1000p
CAP_0201_14mil
25V 10%
GND
C7311
1000p
CAP_0201_14mil
25V 10%
GND
R7316 59K
RES_0201_12mil
GND
MTP7320
SP_TP_SMDp58mm

Title:	BLADE PWR	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 73 of 76	

+5VA_SHA
10uA
R7411
499K
RES_0201_12mil
LEGACY_MODE
[74] USB_MODE
Q7401A
NX3008NBKS
sot363_6_2x1p25x1p1_p65mm
GND
+5VA_SHA
10uA
R7409
499K
RES_0201_12mil
USB_MODE_R
Q7401B
NX3008NBKS
sot363_6_2x1p25x1p1_p65mm
GND
One Wire UART from SAM (HPD_DET_SL2)
[31] BLADE_AUTH_DATA
C7412
22p 25V
CAP_0201_14mil
Icc(max)=500uA
+5VA_SHA
U7402A
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm
VCC
1A
1B
EN
GND
A1
B2
A2
B1
D1
C7401
0.1u 6.3V
cap_0201_14mil
GND
C1
D2
2EN
2A
2B
C2
U7402B
+5V_SHA_CONN
C7413
0.1u 6.3V
cap_0201_14mil
GND
Icc(max)=500uA
+5VA_SHA
U7401A
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm
C7410
0.1u 6.3V
cap_0201_14mil
GND
+5V_SHA_CONN_UART_RX
R7415
150K
RES_0201_12mil
EV1.9 chg mspn
GND
U7401B
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm
R7403 DNP,BLADE0
RES_0402_16mil
OT_SHA_PWR_RX [33]
R7404 DNP,BLADE0
RES_0402_16mil
OT_SHA_DATA_TX [33]
DNP,BLADE
[33] OT_RX_SEN_MCU_DEBUG
R7401
0
RES_0402_16mil
[33] OT_TX_SEN_MCU_DEBUG
R7413
0
RES_0402_16mil
DNP,BLADE
+3P3V_EC
C7414
1u 6.3V
CAP_0201_14mil
GND
U7406
SN74AVC2T245
QFN10_1p8x1p4xp55_p4mm
VCCB VCCA
B1 A1
B2 A2
OE DIR1
DIR2
GND
+1P8V_EC
C7409
0.1u 6.3V
cap_0201_14mil
GND
[31] BLADE_UART_RX
[31] BLADE_UART_TX
OT_RX_SEN_MCU_IN_R
OT_TX_SEN_MCU_OUT_R
R7408
0
RES_0201_12mil
GND
Icca=8uA
Iccb=8uA
R7402
71.5K
res_0402_16mil
GND
GND
+1P8V_EC
DNP,BLADE
R7405
10K
RES_0201_12mil
R7414
33
RES_0402_16mil
OT_RX_SEN_MCU_IN_TI
R7407
33
RES_0402_16mil
OT_TX_SEN_MCU_OUT_TI
BZX584C3V6
dio_sod523_1p2xp8xp65_1p1mm
D7402
D7401
GND
GND
DNP,BLADE
C7407
0.1u 25V
CAP_0402_22mil
DNP,BLADE
C7408
0.1u 25V
CAP_0402_22mil
GND
C7416
0.1u 25V
CAP_0402_22mil
DNP,BLADE
C7411
0.1u 25V
CAP_0402_22mil
DNP,BLADE
GND
L7401
L7402
1.2A
120Ohm/100MHz
ind_0402_22mil
1.2A
120Ohm/100MHz
ind_0402_22mil
BLADE_AUTH_DATA_UART_TX
C7402
100p 25V
CAP_0201_14mil
C7403
100p 25V
CAP_0201_14mil
GND
GND
U7405
IP4252CZ8-4
dfn9_1p7x1p35xp55_p4mm
I1 O1
I2 O2
I3 O3
I4 O4
GND
GND
+5V_SHA_CONN_UART_RX_CONN [73]
BLADE_AUTH_DATA_UART_TX_CONN [73]
[24] USB2_BLADE_DP
[24] USB2_BLADE_DN
L7403
TCFG03025H90002AA9
qfn6_p65xp85xp55_p4mm
GND
GND
MUXED_ACC_D+_L
MUXED_ACC_D-_L
ACC plug
MUX
ACC Remove
No ACC
RX
TX
D+
D-
+5V_SHA_CONN
BLADE_AUTH_DATA
OT_TX
OT_RX
+5V_KB_CONN
CB=H :=> NO <-> COM
CP=L :=> NC <-> COM
+3P3VA
U7504
TS3USB30E
qfn10_1p8x1p4xp55_p4mm
VCC
D1+
D2+
D+
D1-
D2-
D-
S
OE
GND
C7415
0.1u
6.3V
cap_0201_14mil
GND
OT_TX_SEN_MCU_OUT_TI_F
OT_RX_SEN_MCU_IN_TI_F
BLADE_TX_USB_D+ [73]
BLADE_RX_USB_D- [73]
U7404
IP4292CZ10-TBR
DIO_ARRAY_10_ESD_1X2P5XP55_P5MM
NC
GND
DNP,BLADE
C7404
50V 100p
CAP_0402_22mil
DNP,BLADE
C7405
100p 50V
CAP_0402_22mil
GND
GND
[31] BLADE_UART_USB_N
R7410
0
USB_MODE
RES_0201_12mil
R7412
100K
RES_0201_12mil
GND
C7406
0.1u
6.3V
cap_0201_14mil
GND
R7406
100K
RES_0201_12mil
GND
BLADE_UART_MUX_EN
USB_MODE
[74]

Title:	Components for ME/ EMI		
Microsoft	Engineer: Surface		
Size: B	Project Name: U -- EV 1.90		Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 74 of 76		



Title:	Power Protect	
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 75 of 76	

SFT1 SHIELD
MSPN = X933943-001
SHIELD, FRAME, T1, V1
PCB Footprint = shield-X933943-001

SFT2 SHIELD
MSPN = X933944-001
SHIELD, FRAME, T2, V1
PCB Footprint = shield-X933944-001

SFT3 SHIELD
MSPN = X933945-001
SHIELD, FRAME, T3, V1
PCB Footprint = shield-X933945-001

SFT4 SHIELD
MSPN = X933946-001
SHIELD, FRAME, T4, V1
PCB Footprint = shield-X933946-001

SFT5 SHIELD
MSPN = X933947-001
SHIELD, FRAME, T5, V1
PCB Footprint = shield-X933947-001

SFT6 SHIELD
MSPN = X933948-001
SHIELD, FRAME, T6, V1
PCB Footprint = shield-X933948-001

SFT7 SHIELD
MSPN = X933949-001
SHIELD, FRAME, T7, V1
PCB Footprint = shield-X933949-001

GND

H7601
Value = X934367-001
washer-X934367-001
GND

H7602
Value = X934367-001
washer-X934367-001
GND

EV1.9 Add

SFT8 SHIELD
MSPN = X933950-001
SHIELD, FRAME, T8, V1
PCB Footprint = shield-X933950-001

SFT9 SHIELD
MSPN = X933951-001
SHIELD, FRAME, T9, V1
PCB Footprint = shield-X933951-001

SFT10 SHIELD
MSPN = X933952-001
SHIELD, FRAME, T10, V1
PCB Footprint = shield-X933952-001

SFT11 SHIELD
MSPN = X933953-001
SHIELD, FRAME, T11, V1
PCB Footprint = shield-X933953-001

SFT12 SHIELD
MSPN = X933954-001
SHIELD, FRAME, T12, V1
PCB Footprint = shield-X933954-001

GND

J7601
25SMT-4442-01
gndfoam_3p6x1p7x1p6
GND

J7602
25SMT-4442-01
gndfoam_3p6x1p7x1p6
GND

J7603
25SMT-4442-01
gndfoam_3p6x1p7x1p6
GND

J7604
25SMT-4442-01
gndfoam_3p6x1p7x1p6
GND

EV1.9 Add

SFB1 DNP,MECH_SHIELD SHIELD
MSPN = X933968-001
SHIELD, FRAME, B1, V1
PCB Footprint = shield-X933968-001

SFB2 MECH_SHIELD SHIELD
MSPN = X933969-001
SHIELD, FRAME, B2, V1
PCB Footprint = shield-X933969-001

SFB3 DNP,MECH_SHIELD SHIELD
MSPN = X933970-001
SHIELD, FRAME, B3, V1
PCB Footprint = shield-X933970-001

SFB4 MECH_SHIELD SHIELD
MSPN = X933971-001
SHIELD, FRAME, B4, V1
PCB Footprint = shield-X933971-001

SFB5 DNP,MECH_SHIELD SHIELD
MSPN = X933972-001
SHIELD, FRAME, B5, V1
PCB Footprint = shield-X933972-001

SFB6 MECH_SHIELD SHIELD
MSPN = X933973-001
SHIELD, FRAME, B6, V1
PCB Footprint = shield-X933973-001

SFB7 DNP,MECH_SHIELD SHIELD
MSPN = X933974-001
SHIELD, FRAME, B7, V1
PCB Footprint = shield-X933974-001

GND

SFB8 DNP,MECH_SHIELD SHIELD
MSPN = X933975-001
SHIELD, FRAME, B8, V1
PCB Footprint = shield-X933975-001

SFB9 MECH_SHIELD SHIELD
MSPN = X933976-001
SHIELD, FRAME, B9, V1
PCB Footprint = shield-X933976-001

SFB10 MECH_SHIELD SHIELD
MSPN = X933976-001
SHIELD, FRAME, B9, V1
PCB Footprint = shield-X933976-001

GND

[36,55] VCCDSW_EN >> MTP7669 SP_TP_SMDp58mm

[70,71] SL1_HPD2 <> MTP76101 SP_TP_SMDp58mm

[70,71] SL1_HPD1B <> MTP7682 SP_TP_SMDp58mm

[70,71] SL1_HPD1A <> MTP7684 SP_TP_SMDp58mm

MP7605
Value = X935458-001
MSPN = X935458-001
PCB Footprint = sp-pem_nut-x935458-001-1
GND

EV1.9 was:X912411-001
gold plating option provided
for both top and bottom layers

EV1.9
remove fence
x930139-001

MP7601
Value = X934094-001
MSPN = X934094-001
SP-PEM_NUT-X934094-001_3p60x2p45d
GND

MP7602
Value = X934094-001
MSPN = X934094-001
SP-PEM_NUT-X934094-001_3p60x2p45d
GND

EV1.9 was X911169-001

MP7603
Value = X934094-001
MSPN = X934094-001
SP-PEM_NUT-X934094-001_3p60x2p45d
GND

MP7604
Value = X934094-001
MSPN = X934094-001
SP-PEM_NUT-X934094-001_3p60x2p45d
GND

PWR_SL1
MTTP_BF7670 sp_MTP0p8mm
MTTP_BF7653 sp_MTP0p8mm
MTTP_BF7654 sp_MTP0p8mm
MTTP_BF7655 sp_MTP0p8mm
MTTP_BF76105 sp_MTP0p8mm
MTTP_BF76103 sp_MTP0p8mm

PWR_SL1
MTP_BF7670 sp_MTP0p8mm
MTP_BF7653 sp_MTP0p8mm
MTP_BF7654 sp_MTP0p8mm
MTP_BF7655 sp_MTP0p8mm
MTP_BF76105 sp_MTP0p8mm
MTP_BF76103 sp_MTP0p8mm

+0P85VSB >> MTP7686 SP_TP_SMDp58mm
+VCCGT >> MTP7652 SP_TP_SMDp58mm
+VCCSA >> MTP7657 SP_TP_SMDp58mm
+VCCIO >> MTP7662 SP_TP_SMDp58mm
+VCCST_CPU >> MTP7661 SP_TP_SMDp58mm
+VCCSTG >> MTP7659 SP_TP_SMDp58mm
+VCCEDRAM >> MTP7658 SP_TP_SMDp58mm
+VCCEOPIO >> MTP7660 SP_TP_SMDp58mm
+1P2V_DUAL >> MTP7611 SP_TP_SMDp58mm
+V_VDDQ_VTT >> MTP7612 SP_TP_SMDp58mm
+VCC_CORE >> MTP7613 SP_TP_SMDp58mm
+VDDQ_VREF >> TP7614 SP_TP_SMDp58mm

MTP_BF7656 sp_MTP0p8mm GND
MTP_BF7671 sp_MTP0p8mm GND
MTP_BF7672 sp_MTP0p8mm GND
MTP_BF7673 sp_MTP0p8mm GND
MTP_BF76104 sp_MTP0p8mm GND
MTP_BF76102 sp_MTP0p8mm GND

MTTP_BF7656 sp_MTP0p8mm GND
MTTP_BF7671 sp_MTP0p8mm GND
MTTP_BF7672 sp_MTP0p8mm GND
MTTP_BF7673 sp_MTP0p8mm GND
MTTP_BF76104 sp_MTP0p8mm GND
MTTP_BF76102 sp_MTP0p8mm GND

PTH18 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH1 c1p35x0p75d mtg_pin_c1p35x0p75d
PTH2 c1p35x0p75d mtg_pin_c1p35x0p75d
PTH3 c1p35x0p75d mtg_pin_c1p35x0p75d
GND

EV1.9 remove PTH4-PTH9

PTH19
MSPN = NO-MSPN-119
MTG_pin_slot-3p00x3p50_2p50X3p00d
GND

EV1.9
remove PTH20
slot-3p00x3p50_2p50X3p0

EV1.9
remove PTH10
MH31x2.5d

PTH11 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH12 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH13 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH14 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH15 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH16 MH3.1x2.5d mtg_hole_3p10x2p50d
PTH17 MH3.1x2.5d mtg_hole_3p10x2p50d
GND

Title: Test Point
Microsoft Engineer: Surface
Size: B | Project Name: U -- EV 1.90 | Rev: 1.90.2
Date: Monday, May 11, 2015 | Sheet 76 of 76