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CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors.

Property: BUILD-OPT
DNP = Do Not Place

S or DB = Replace after Debug

<Core Design>

Title: Table of Contents
Engineer: Surface
Size: A3 | Project Name: U -- EV 1.90 | Rev: 1.90.2
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Schematics Change History

Rev.	Date	Comments
0p9	28 Oct 2014	1. Starting with G_EV1_1021-1630.DSN 2. Added SL schematic from page 72 ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 3. Added External USB3 schematic from ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 4. Added external DP ...\T\MB\DV_RELEASED\Schematic\CASTLE2_DV_2014_1021_1100.DSN 5. Added IR_CAMERA from Front Camera...put in page 49 6. Removed page 73 PCIe GPU 7. Added Blade from T 8. Removed P72 T2B Pwr Transistors
0p10	3 Nov 2014	1. Changing to NVDC 2. Replaced GTX with GT, kept bypass caps 3. Replaced Charger with BQ24770
0p11	3 Nov 2014	1. Replace SKL-U with SKL-Y
0p12	11 Nov 2014	1. Model DDR connection from Intel SDS
0p13	18 Nov 2014	1. Added FUB information to all components 2. Changed Decretes.. sizing caps
0p14	20 Nov 2014	1. Added +5VA_SHA 2. Added T Cost Down/XCN's 3. Added SL +5V load Switch & Caps 4. Added Blade +5V load Switch & Caps
0p15	26 Nov 2014	1. Removed Boost 2. Re-adjusted usb ports on CPU 3. Removed Audio DSP
0p16	03 Dec 2014	1. changed +1VSB regulator 2. changed IR Camera/added diode 3. added power numbers from 0.91 PDG, Oct14 4. changed BLADE connector 5. cpu decoupling caps changed 6. changed +5V/+3V inductors (place holder)
0p17	05 Dec 2014	1. swapped M_A_CAA with MA_CAB on U1601/U1602 2. added two SAR chips, P32 3. remove tp's from csi lines on (p23) 4. change from 10 ceramic to 3 tantalum-poly on usb3 typeA (p45) 5. remove the RSENSE from output of +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) 6. change RSENSE input to 0402 from 0603 for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58)/+VCCEOPIO (p58)/+1VSB(p61)/+1P8VSB(p62) input regulator 7. change inductor for +VCCIO(p56)/+0p85VSB(p56)/+VCCEDRAM (p58) to HMLE20161B-1R0MDR-01 8. change RSENSE input to 0402 from 0603 for +5V_TS,+5V_SDXC,+5V_AUDIO,+5V, +5V_FAN(p64) 9. change RSENSE input to 0402 from 0603 for +3P3V_PANEL,+3P3V,+3P3V_SENSOR,+1P8V_DMIC (p65) 10. Replacing the SL connector with X908351-001 11. Replace PL5901 and PL5902 with CMLE042T-2R2MS-01 12. Replace 0402 1uf 6.3V with 0201 1uF 6.3V X5R 13. Replace L7201 with TOKO #A919CY-100M 14. Added VSYS -> BLADE FANG supply (p73)
0p18	09 Dec 2014	1. Reduced sizes of parts for Cameras (Resistors/Caps/Regulators)
0p19	12 Dec 2014	1. All 47uF caps become 0805/1mmZ 2. All 10uF caps become 0402...4V/6.3V
0p20	15 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x4 2. Shui Changes 3. more Shui Changes
0p21	16 Dec 2014	1. changed SAM flash to reduce size to 2x3 from 5x5 2. changes from EV_schematic_issue_check_1216_JDM1.xlsx 3. changed name of +6_12 to +V_ALWAYS_ON 4. Removed 2 Mikes & Front Mike & added FPC conn 5. Added 2nd BLADE connector
0p22	17 Dec 2014	1. Replaced SD connector with AY531465T 2. changes from EV_schematic_issue_check_viola_1217_JDM1.xlsx
0p23 - current		1. See apexUfixes_revXpXX.xlsx

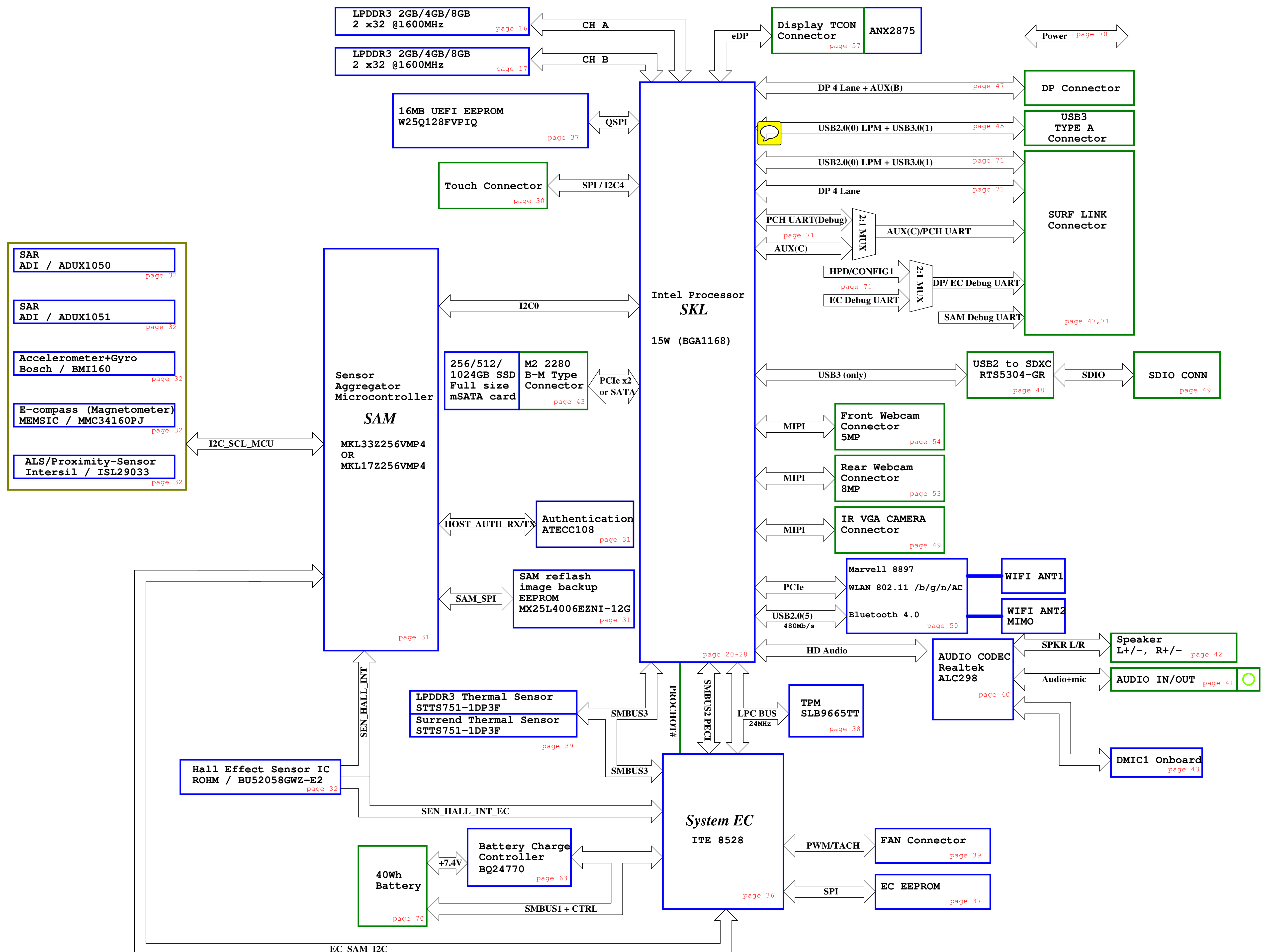
CAD Note:

Default component footprint is SMD 0201, X5R, 1% resistors

S = Short after design fixed

Property: BUILD-OPT

DNP = Not Installed Part.



Title:	BLOCK DIAGRAM		
Microsoft	Engineer:	Surface	
Size: Custom	Project Name: U -- EV 1.90		Rev: 1.90.2
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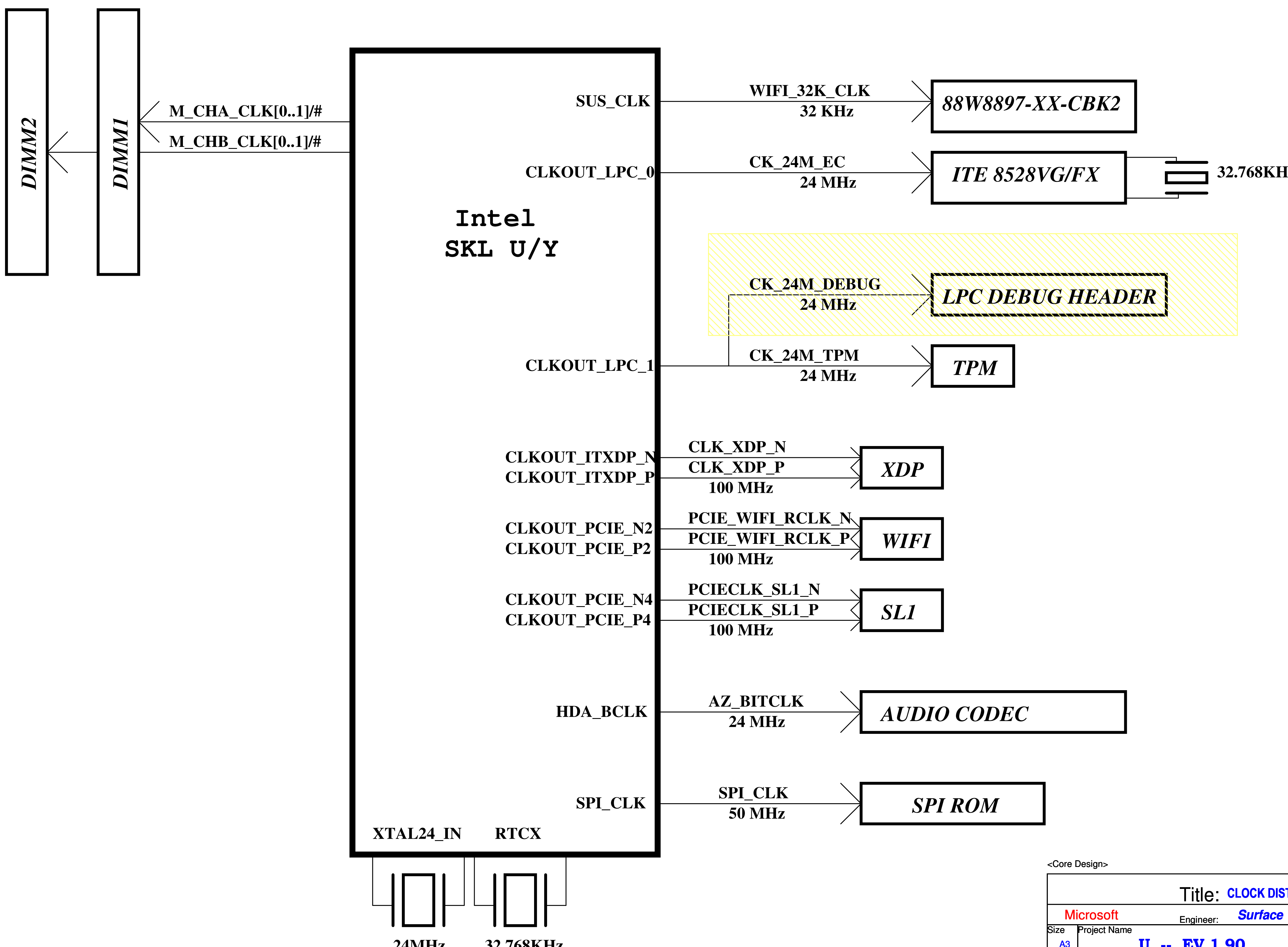
HSW Buffer Through Mode for Pre-Silicon



<Core Design>

Microsoft	Title: CLOCK DISTRIBUTION(TBD)		
	Engineer: Surface		
Size: A3	Project Name: U -- EV 1.90		Rev: 1.90.2
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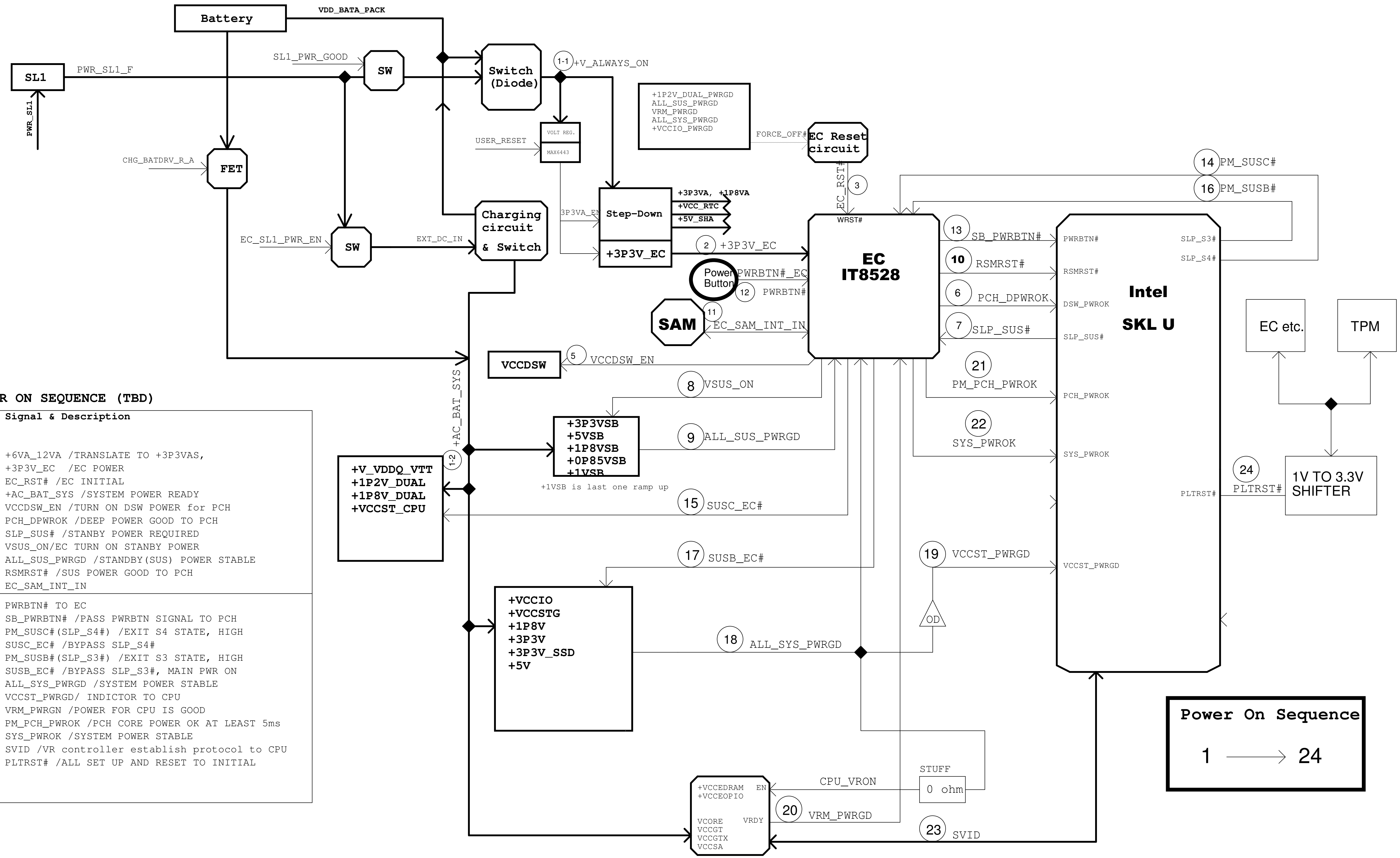

POWER ON SEQUENCE (TBD)

STEP	Signal & Description
1	+6VA_12VA /TRANSLATE TO +3P3VAS,
2	+3P3V_EC /EC POWER
3	EC_RST# /EC INITIAL
4.	+AC_BAT_SYS /SYSTEM POWER READY
5.	VCCDSW_EN /TURN ON DSW POWER for PCH
6.	PCH_DPWROK /DEEP POWER GOOD TO PCH
7.	SLP_SUS# /STANBY POWER REQUIRED
8.	VSUS_ON/EC TURN ON STANBY POWER
9.	ALL_SUS_PWRGD /STANDBY(SUS) POWER STABLE
10.	RSMRST# /SUS POWER GOOD TO PCH
11.	EC_SAM_INT_IN
12	PWRBTN# TO EC
13.	SB_PWRBTN# /PASS PWRBTN SIGNAL TO PCH
14.	PM_SUSC#(SLP_S4#) /EXIT S4 STATE, HIGH
15.	SUSC_EC# /BYPASS SLP_S4#
16.	PM_SUSB#(SLP_S3#) /EXIT S3 STATE, HIGH
17.	SUSB_EC# /BYPASS SLP_S3#, MAIN PWR ON
18.	ALL_SYS_PWRGD /SYSTEM POWER STABLE
19.	VCCST_PWRGD/ INDICTOR TO CPU
20.	VRM_PWRGN /POWER FOR CPU IS GOOD
21.	PM_PCH_PWROK /PCH CORE POWER OK AT LEAST 5ms
22.	SYS_PWROK /SYSTEM POWER STABLE
23.	SVID /VR controller establish protocol to CPU
24.	PLTRST# /ALL SET UP AND RESET TO INITIAL

Power On Sequence

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<Core Design>

Microsoft	Title: SIGNAL&RESET MAP	Engineer:	Surface
Size A2	Project Name U -- EV 1.90		Rev 1.90.2
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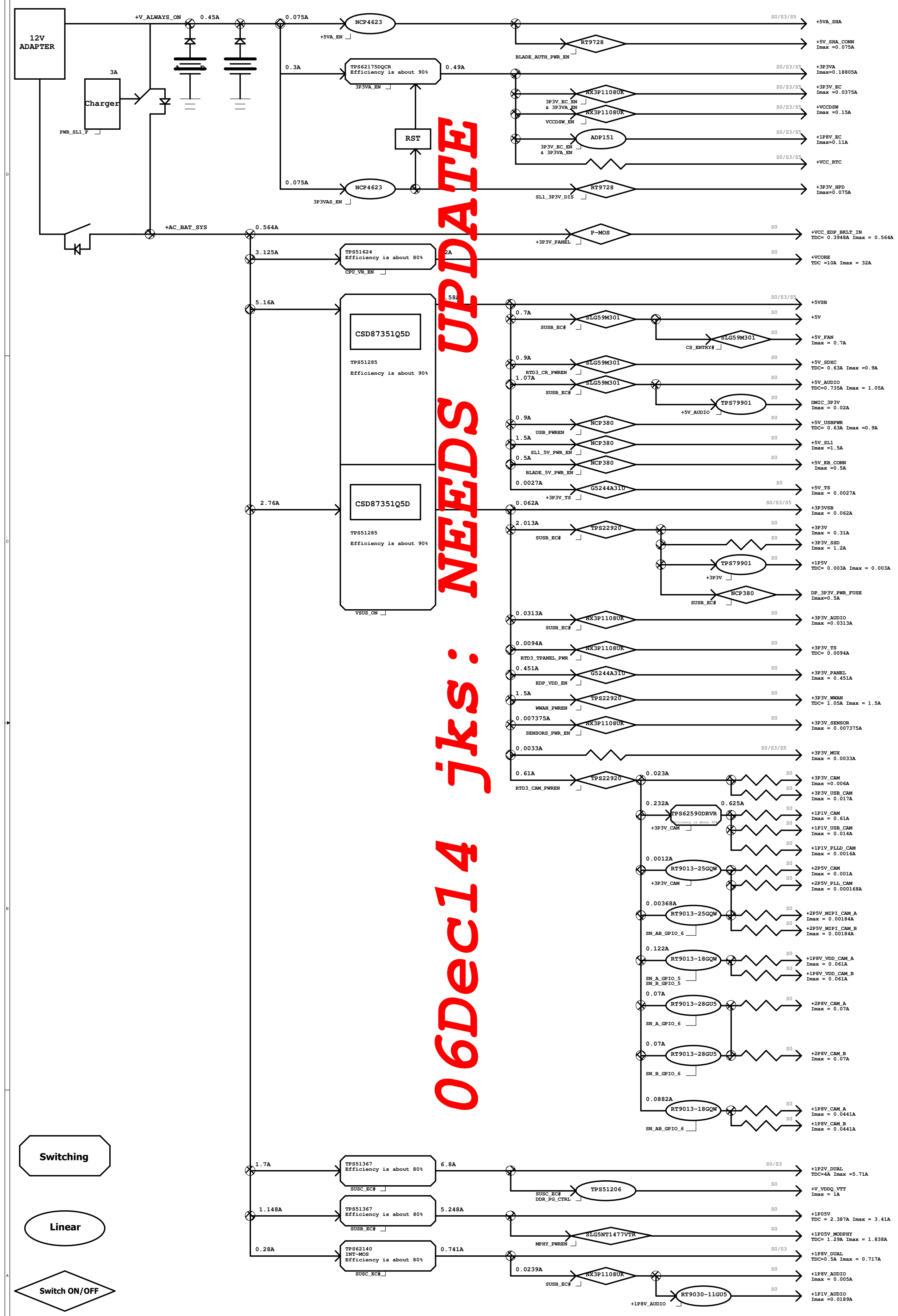

<Core Design>

	Title:	POWER FLOW	
Microsoft	Engineer:	Surface	
Size: Custom	Project Name: U -- EV 1.90		Rev: 1.90.2
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06Dec14 jks: NEEDS UPDATE

CPU Haswell ULT

Rail	Current
+VCORE	-> 32A
+1P05V	-> 0.6A
+DDR_V (+1P2V_DUAL)	-> 2.5A
+1P05V	-> 2.81A
+1P05V_MODPHY	-> 1.838A
+1P5V	-> 0.003A
+3P3V	-> 0.200A
+3P3VSB	-> 0.062A
+3P3VA	-> 0.099A

LPDDR3

Rail	Current
+1P8V_DUAL	-> 0.717A
+1P2V_DUAL	-> 3.210A
+VTT_DDQ_VTT(0.6V)	-> 1A

mSATA(SSD)

Rail	Current
+3P3V	-> 1.2A

EC

Rail	Current
+3P3V_EC	-> 0.012A

EC ROM

Rail	Current
+3P3V_EC	-> 0.005A
+3P3VA	-> 0.00025A

Temp sensor(STTS751)

Rail	Current
+3P3V_EC	-> 0.00025A

Camera

Rail	Current
+1P1V_CAM	-> 0.609A
+1P1V_PLLD_CAM	-> 0.0016A
+1P1V_USB_CAM	-> 0.0137A
+1P8V_CAM	-> 0.0882A
+1P8V_VDD_CAM	-> 0.122A
+2P5V_CAM	-> 0.001A
+2P5V_PLL_CAM	-> 0.000168A
+2P5V_MIPI_CAM	-> 0.00368A
+2P8V_CAM	-> 0.14A
+3P3V_CAM	-> 0.006A
+3P3V_USB_CAM	-> 0.0169A

TPM(Infineon SLB9665 ESS2)

Rail	Current
+3P3V_TPM (+3P3V)	-> 0.1A

SDXC

Rail	Current
+5V_SDXC	-> 0.9A

WiFi&BT

Rail	Current
+3P3V_WWAN	-> 1.5A

DMIC

Rail	Current
DMIC_+3P3V/+3P3V_AUDIO	-> 0.02A

FAN

Rail	Current
+5V_FAN	-> 0.7A

UEFI_SPI_BIOS_ROM

Rail	Current
+3P3V	-> 0.04A

Panel

Rail	Current
VCC_EDP_BKLT_IN	-> 0.564A
+3P3V_PANEL	-> [illegible]

Authentication IC (ECC108)

Rail	Current
+3P3VA	-> 0.005A

Touch Interface

Rail	Current
+3P3V_TS	-> 0.0094A
+5V_TS	-> 0.0027A

ALC3264 CODEC

Rail	Current
+3P3V_AUDIO	-> 0.005A
+5V_AUDIO	-> 1.05A
+1P8V_AUDIO	-> 0.005A

DSP (ES320)

Rail	Current
+3P3V_AUDIO	-> 0.0063A
+1P1V_AUDIO	-> 0.0189A

Sensor uC(ATUC256L3U-Z3UR)

Rail	Current
+3P3VA	-> 0.061A

SL1

Rail	Current
+3P3V_HPD	->0.075A
+5V_SL1	-> 1.5A

BLADE

Rail	Current
+5V_KB_CONN	-> 0.5A

Hall effect sensor(BU52058GWZ-E2)

Rail	Current
+3P3VA	->0.0028A

Compass(MMC3416XMA)

Rail	Current
+3P3V_SENSOR	->0.0012A

Acceleromte&Gyro(LSM330TR)

Rail	Current
+3P3V_SENSOR	-> 0.0061A

ALS(ISL29033IROZ-T7) FPC CON

Rail	Current
+3P3V_SENSOR	-> 0.000075A

MUX

Rail	Current
+3P3V_MUX	-> 0.033A

mini DP

Rail	Current
+3P3V	-> 0.5A

USB 3.0 connector

Rail	Current
+5VUSBPWR	-> 0.9A

Transceiver SN74AVCT245

Rail	Current
+1P8V_EC	-> 0.11A

Battery Charger BQ24735

Rail	Current
+V_ALWAYS_ON	-> 0.003A

<Core Design>

Title:	POWER DISTRIBUTION
Microsoft	Engineer: Surface
Size: Custom	Project Name: U -- EV 1.90
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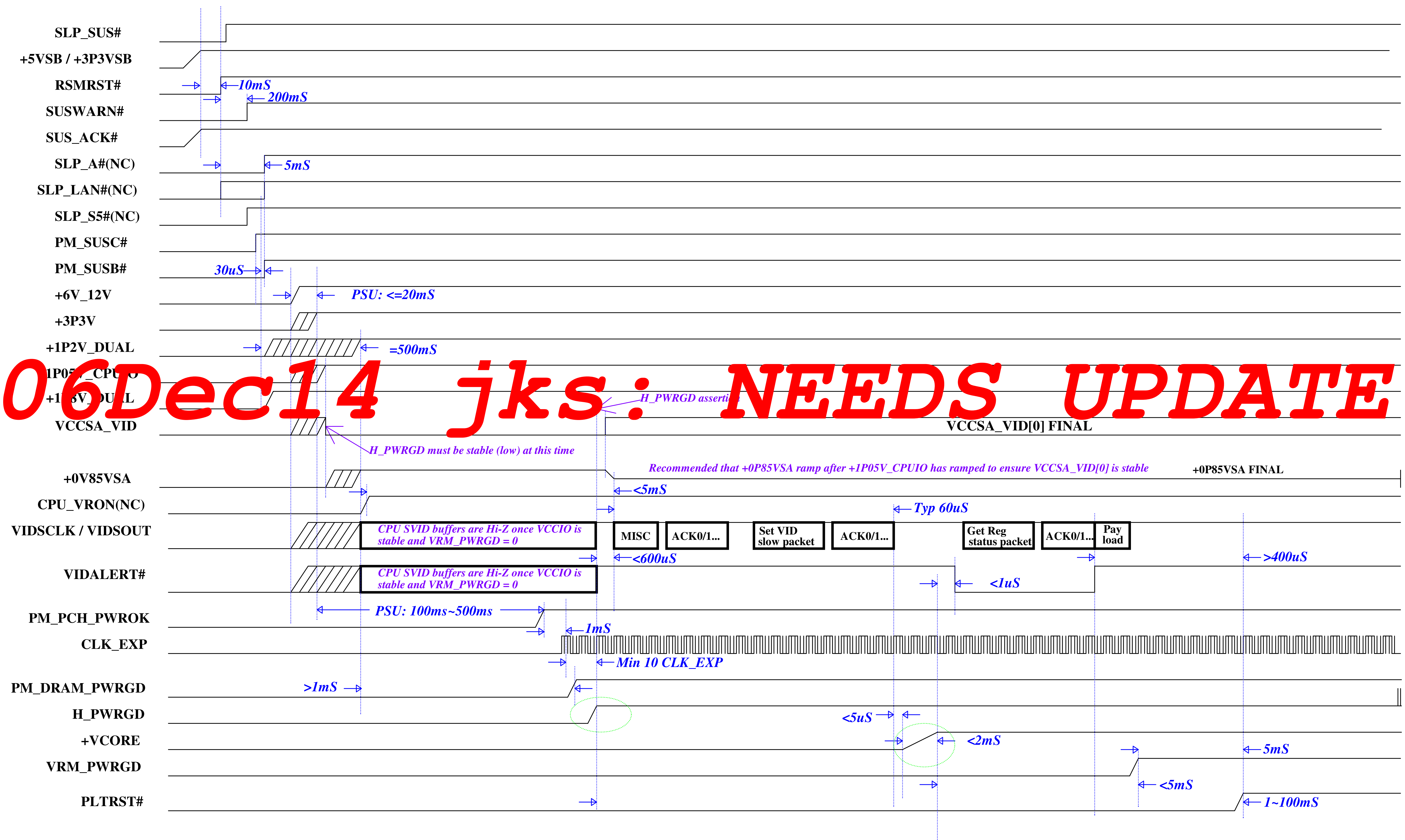
S5 to S0 Power Sequence



<Core Design>

Title:	POWER SEQUENCE	
Microsoft	Engineer:	Surface
Size A3	Project Name U -- EV 1.90	Rev 1.90.2
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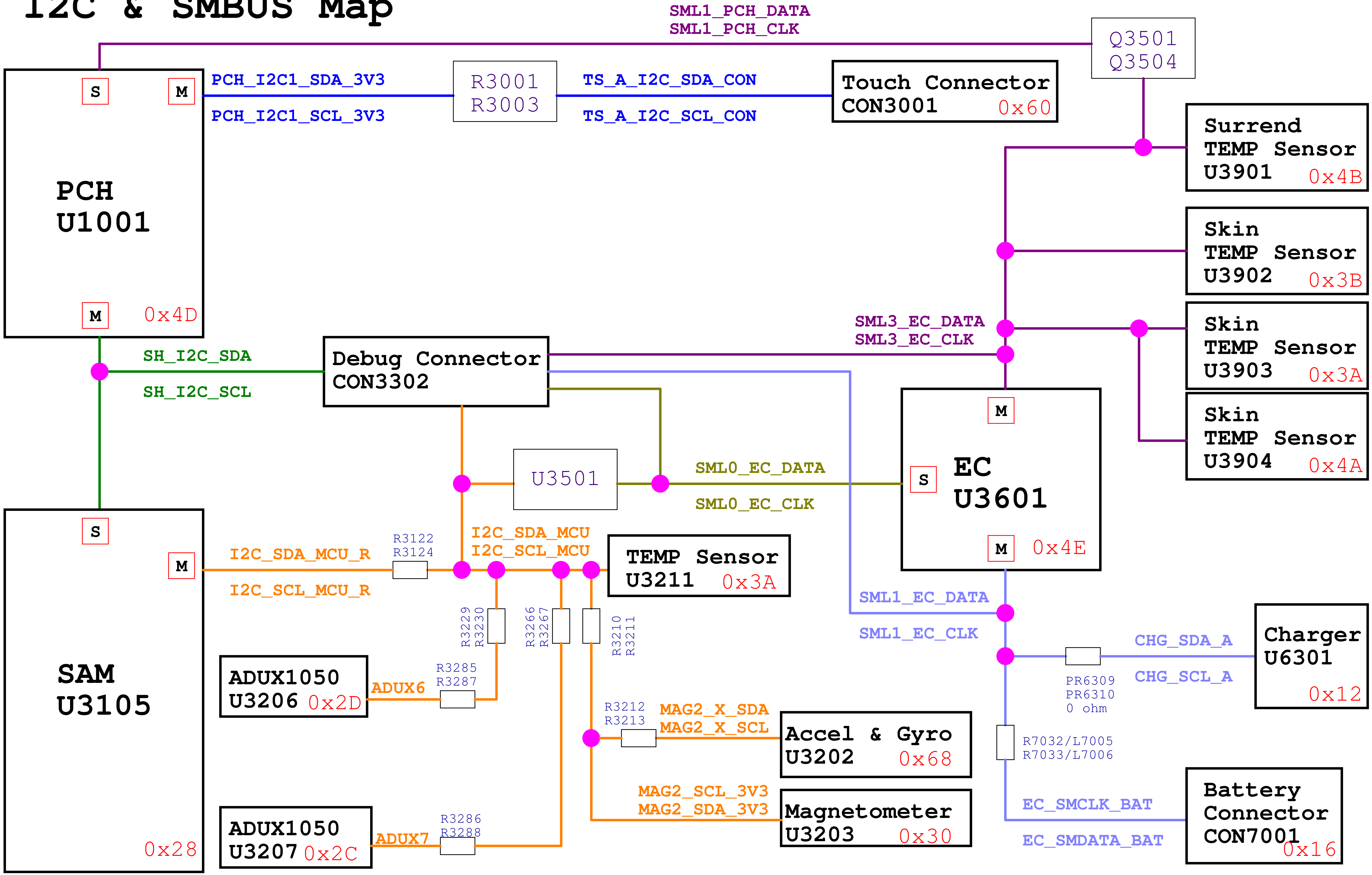
I2C & SMBUS Map



Title: 09. I2C MAP

Engineer: Surface

Size	Project Name	Rev
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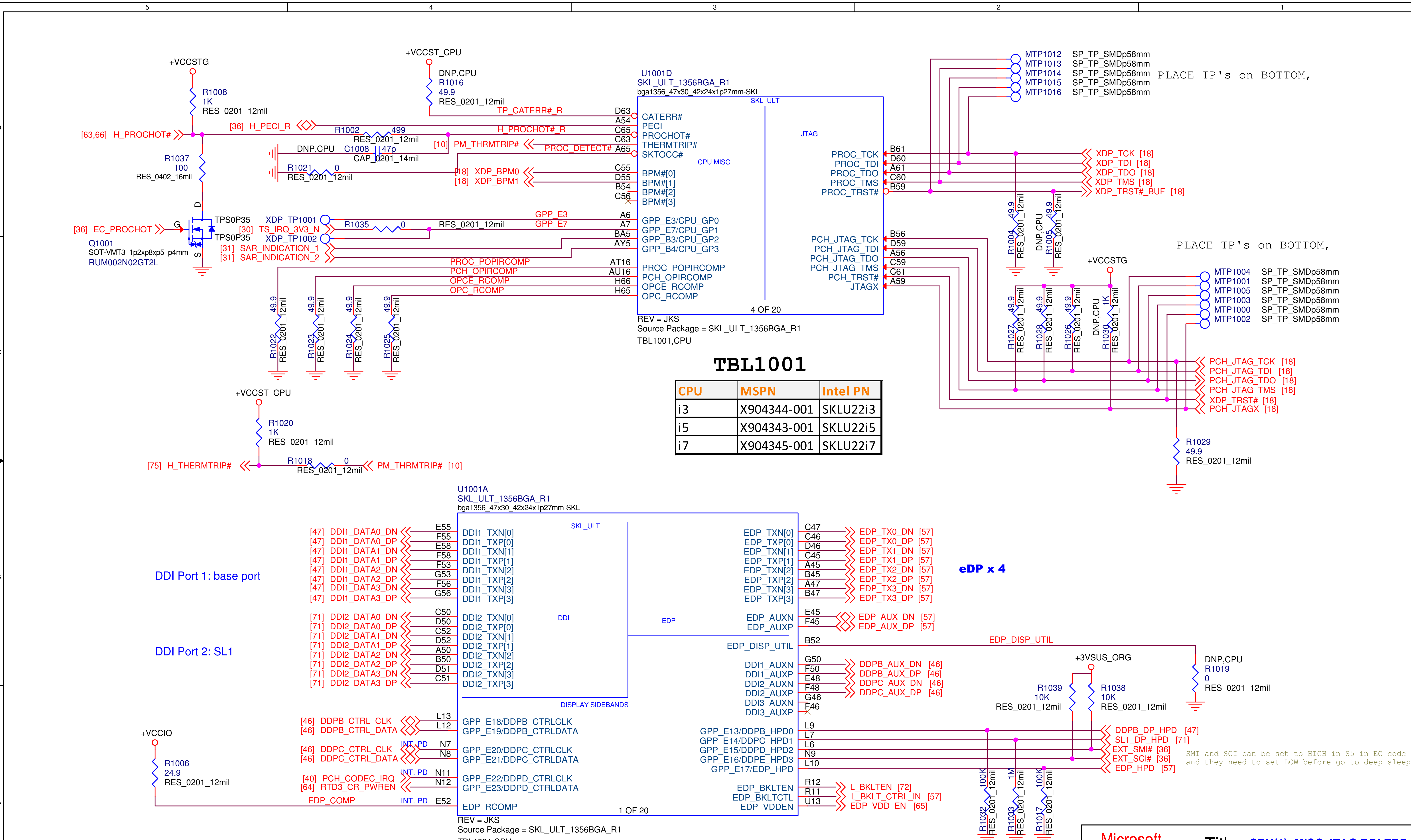

TBL1001

CPU	MSPN	Intel PN
i3	X904344-001	SKLU22i3
i5	X904343-001	SKLU22i5
i7	X904345-001	SKLU22i7

Microsoft

Title: **CPU(1)_MISC,JTAG,DDI,EDP**

Engineer: ***Surface***

Size	Project Name	Rev
B	**U -- EV 1.90**	1.90.2

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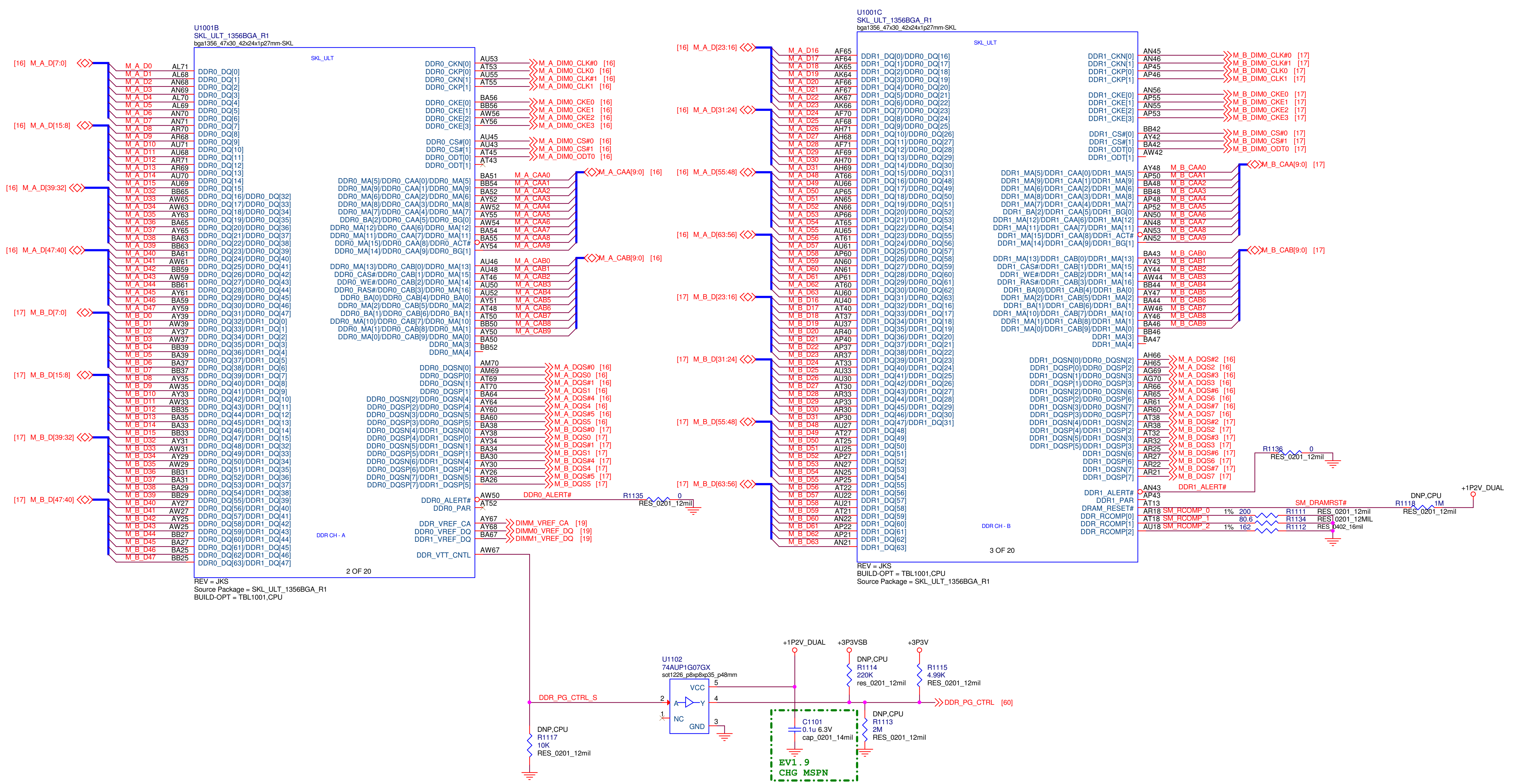

Microsoft	Title: CPU(2)_LPDDR3		
	Engineer: Surface		
Size C	Project Name U -- EV 1.90		Rev 1.90.2
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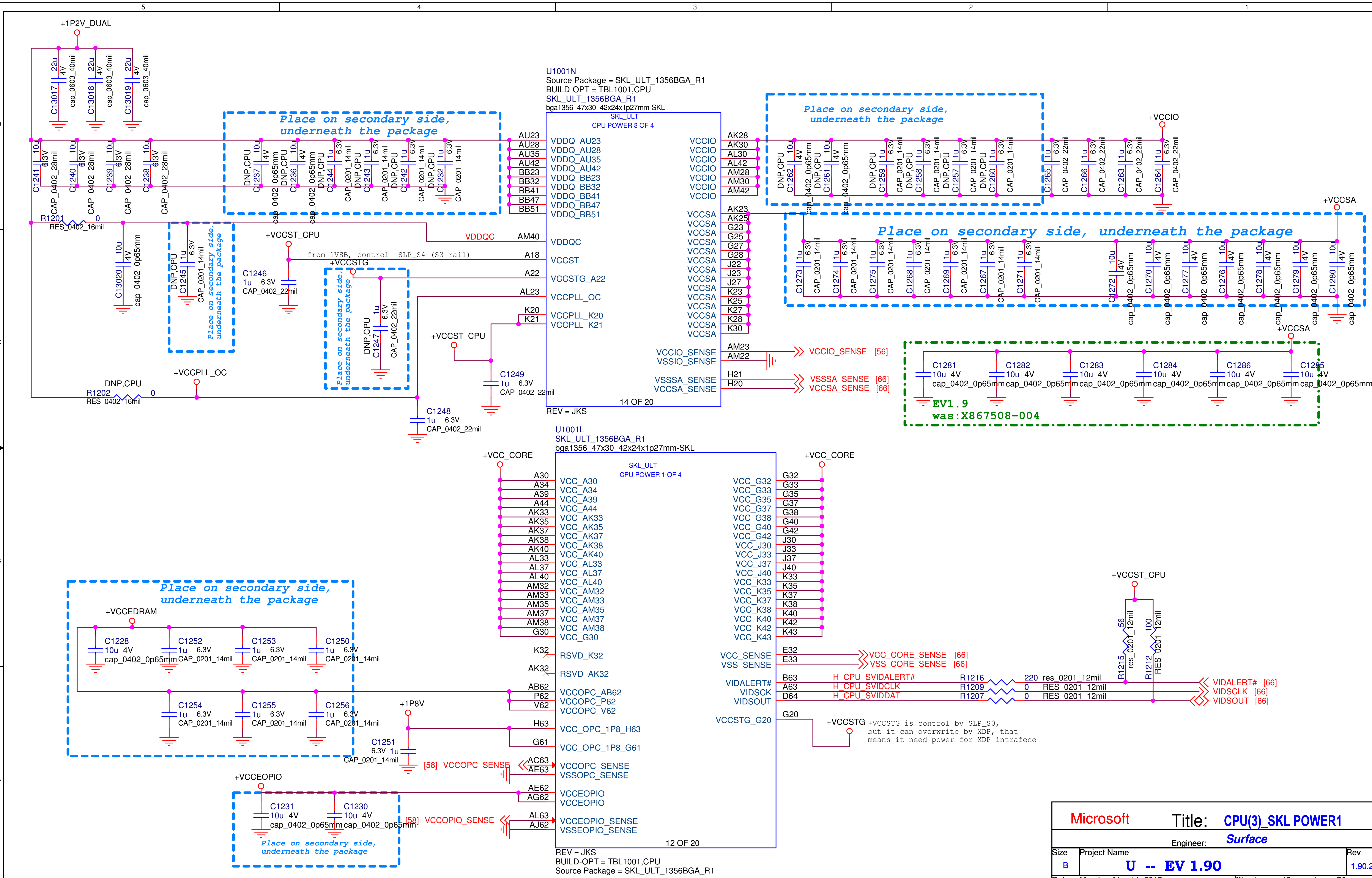

Microsoft

Title: CPU(3)_SKL POWER1

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

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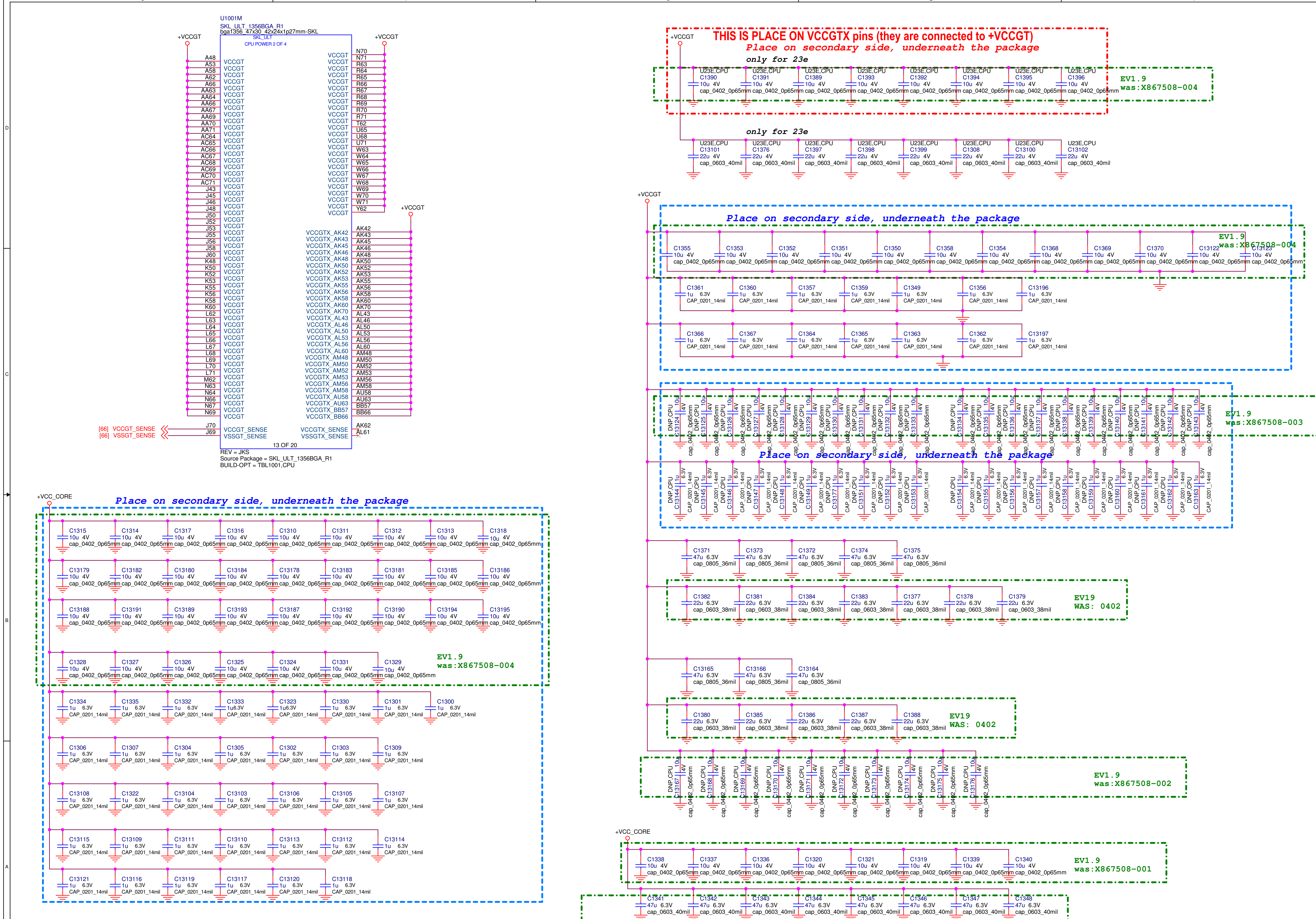

Microsoft	Title:	CPU(4)_SKL_POWER2
	Engineer:	Surface
Size: C	Project Name: U -- EV 1.90	Rev: 1.90.2
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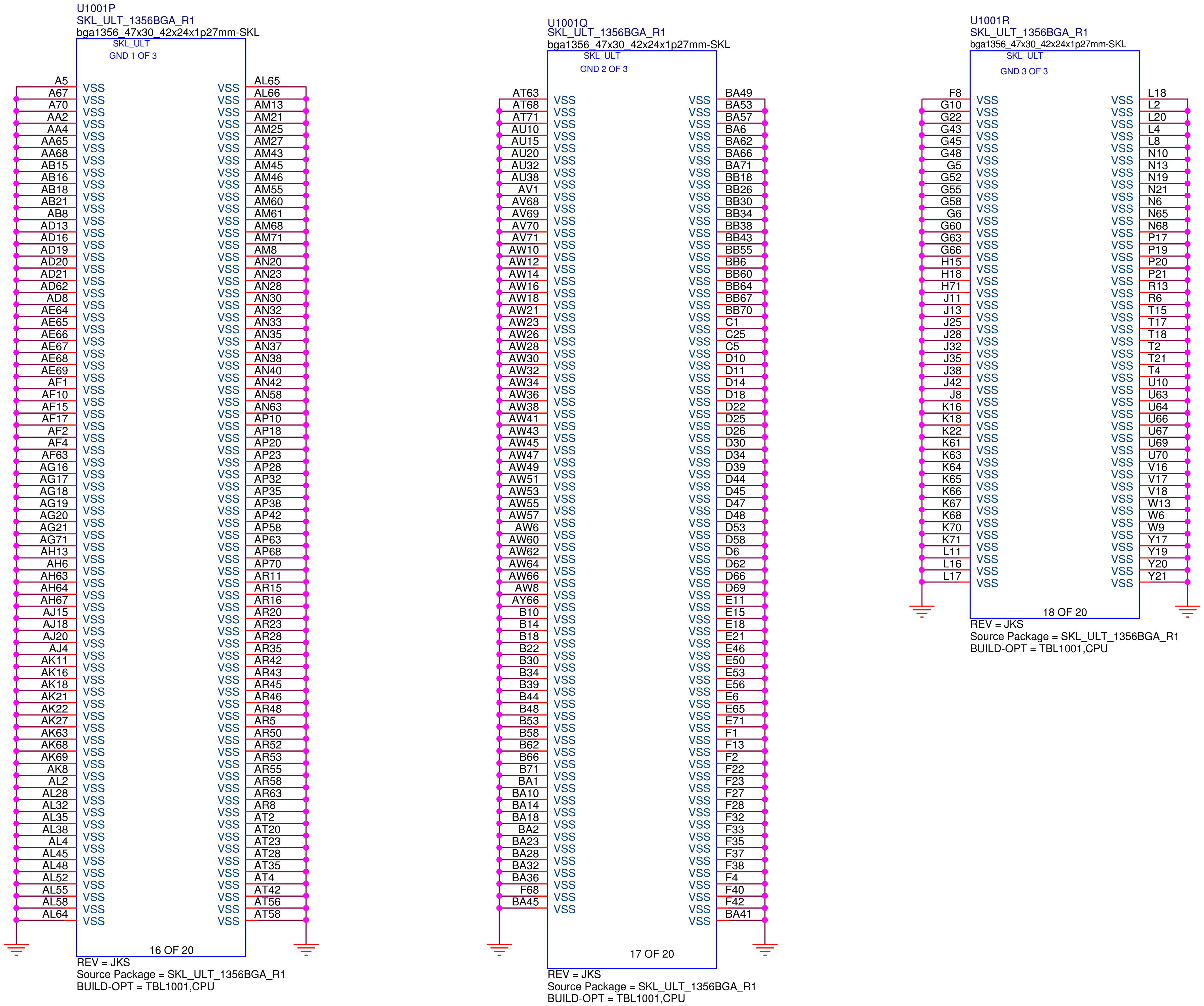

Microsoft

Title: CPU(5)_GND

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

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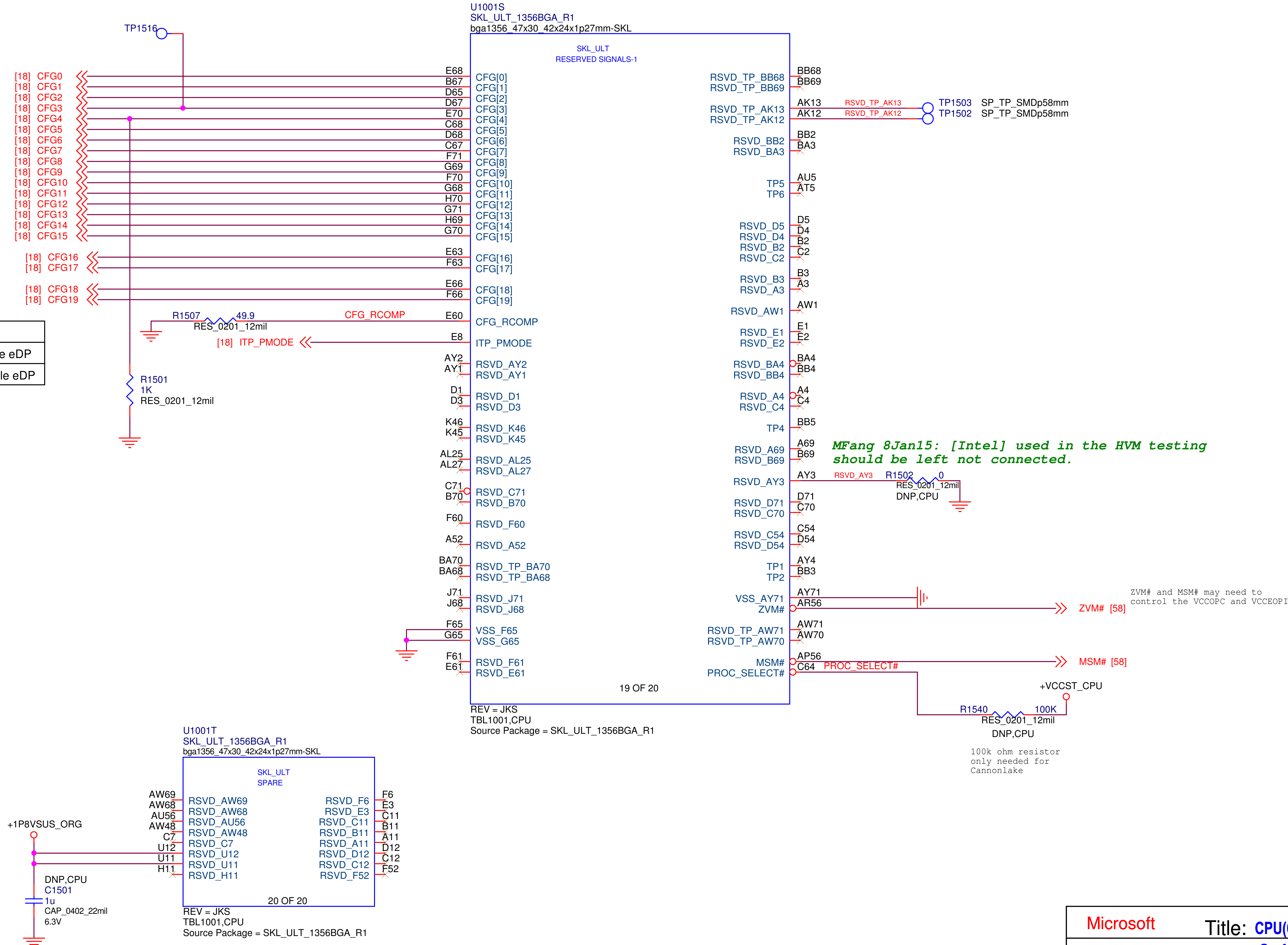

CFG4	
0 **Default**	enable eDP
1	Disable eDP

Microsoft

Title: **CPU(6)_CFG_RESERVED**

Engineer: ***Surface***

Size	Project Name	Rev
B	**U -- EV 1.90**	1.90.2

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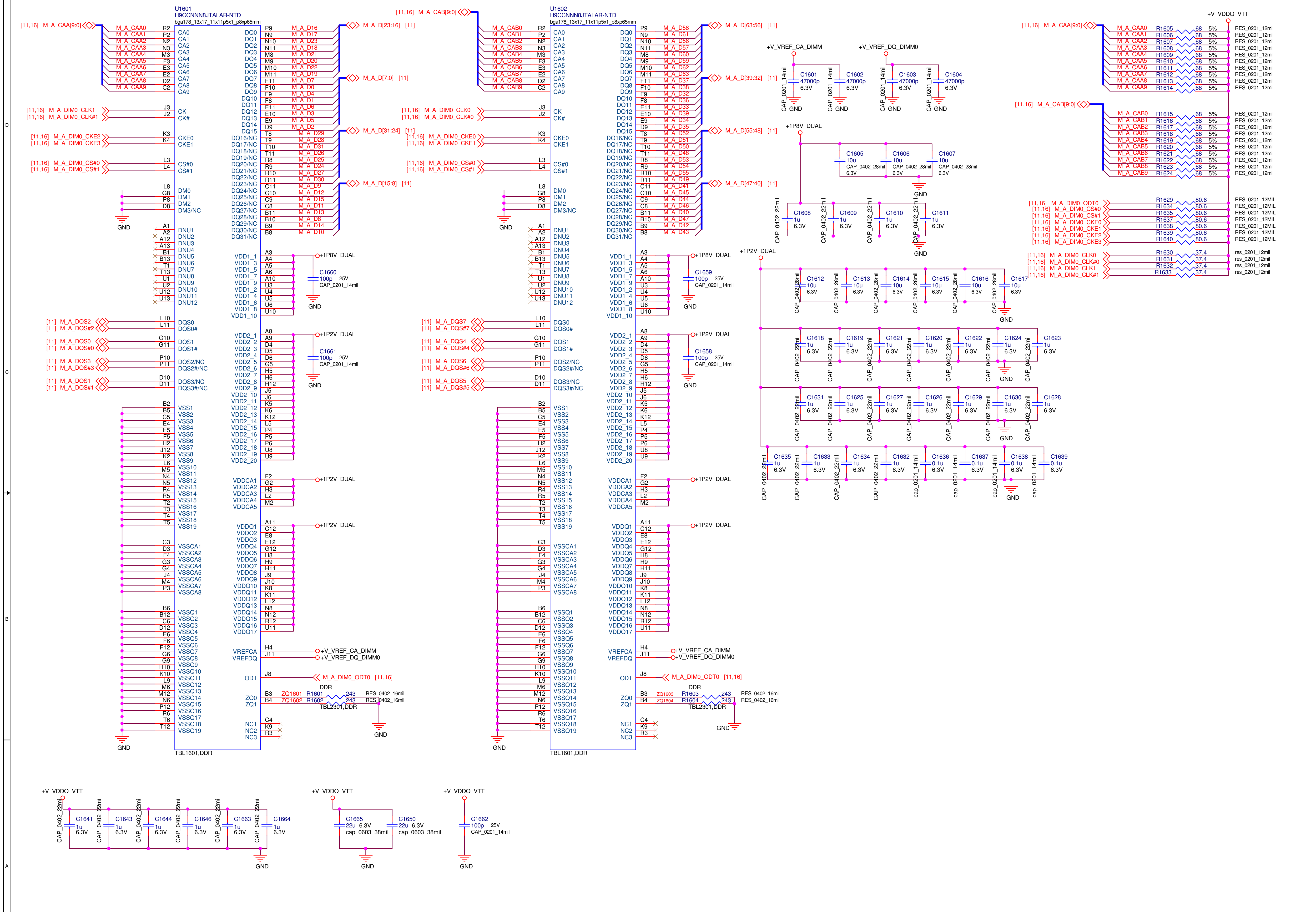

Title: LPDDR3(1)_MEMORY DOWN

Microsoft

Engineer: Surface

Size	Project Name	Rev
C	U -- EV 1.90	1.90.2

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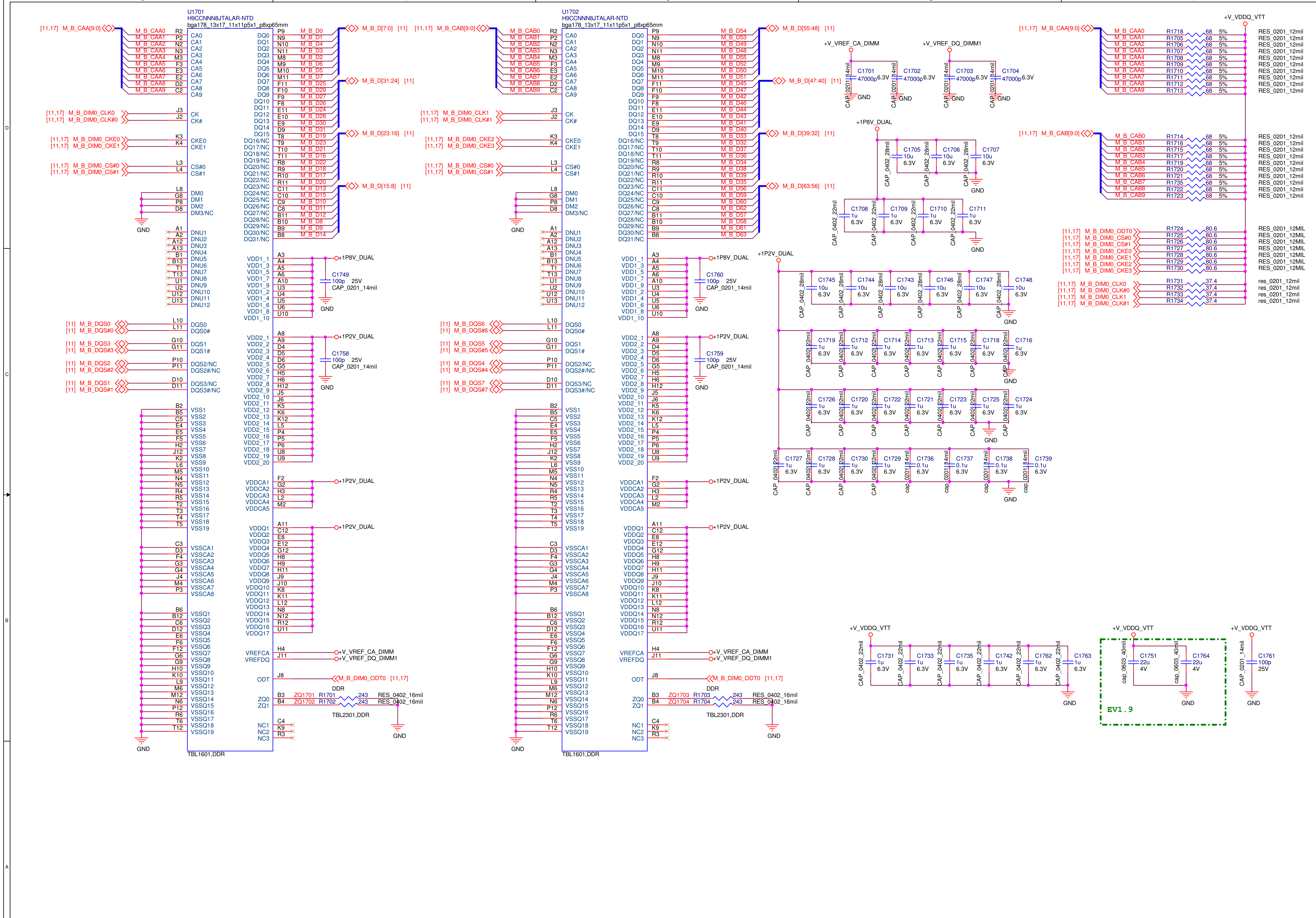

Title: LPDDR3(2)_MEMORY DOWN

Microsoft

Engineer: Surface

Size	Project Name	Rev
C	U -- EV 1.90	1.90.2

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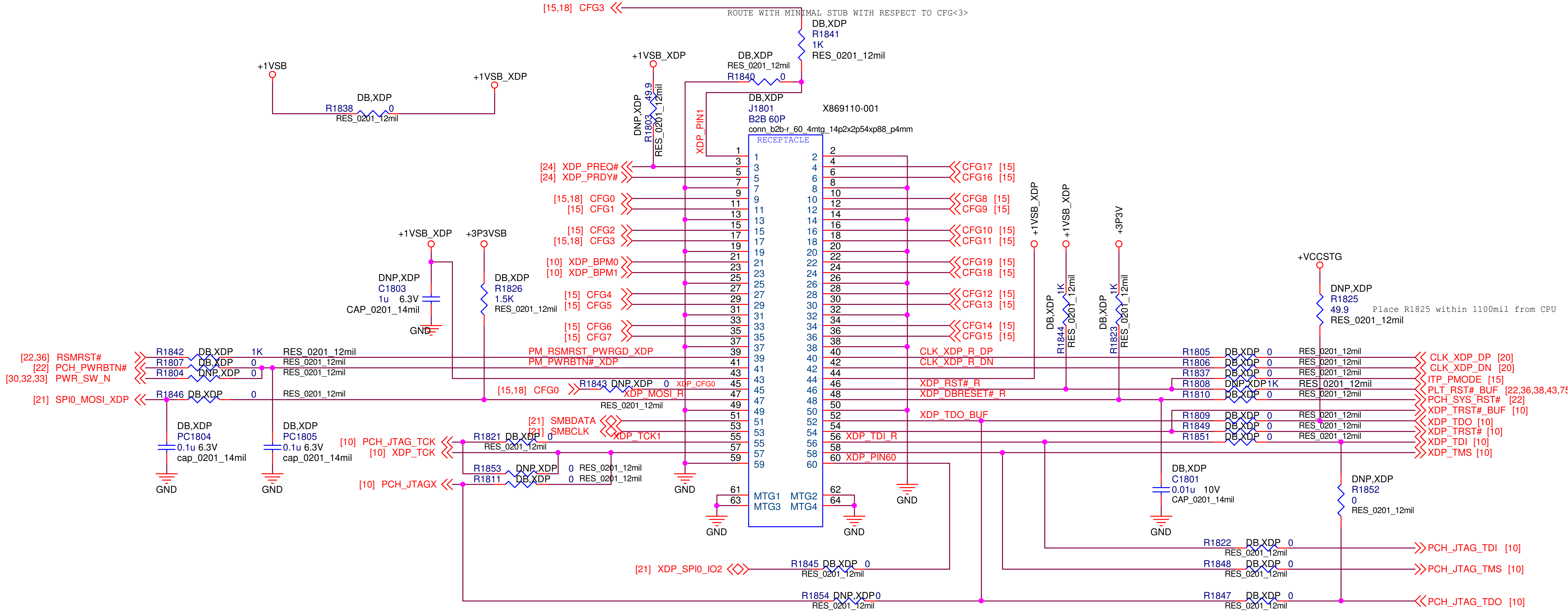
PRIMARY XDP connector



For the signals only go to XDP, the 0R should be close to XDP connector.
For the signals to both XDP and target circuit, the option resistor locaction should follow the target signal routing.

Microsoft	Title: XDP	
	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
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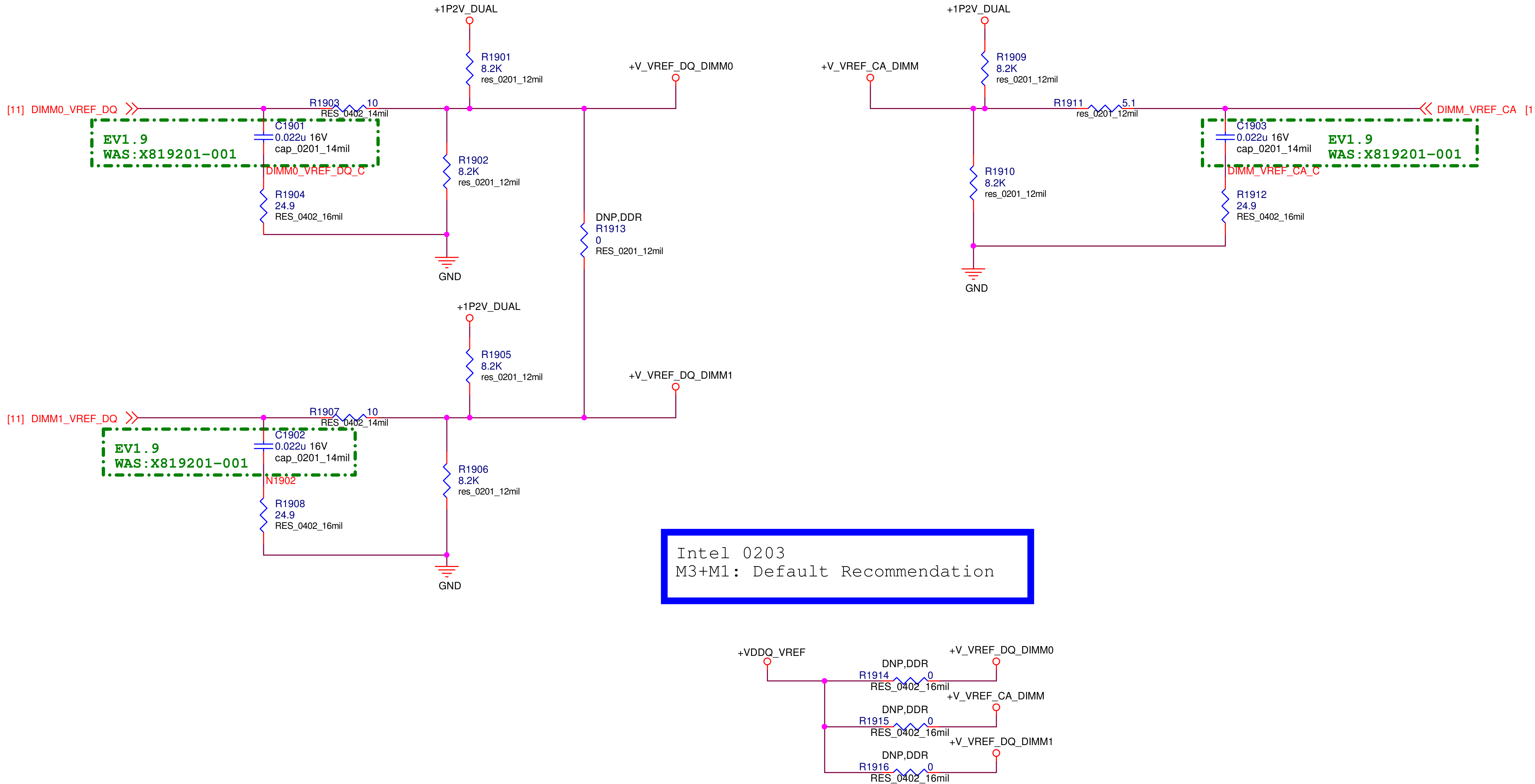
LPDDR3 Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



Microsoft	Title: LPDDR3(3)_CA/DQ Voltage		
	Engineer: Surface		
Size B	Project Name U -- EV 1.90		Rev 1.90.2
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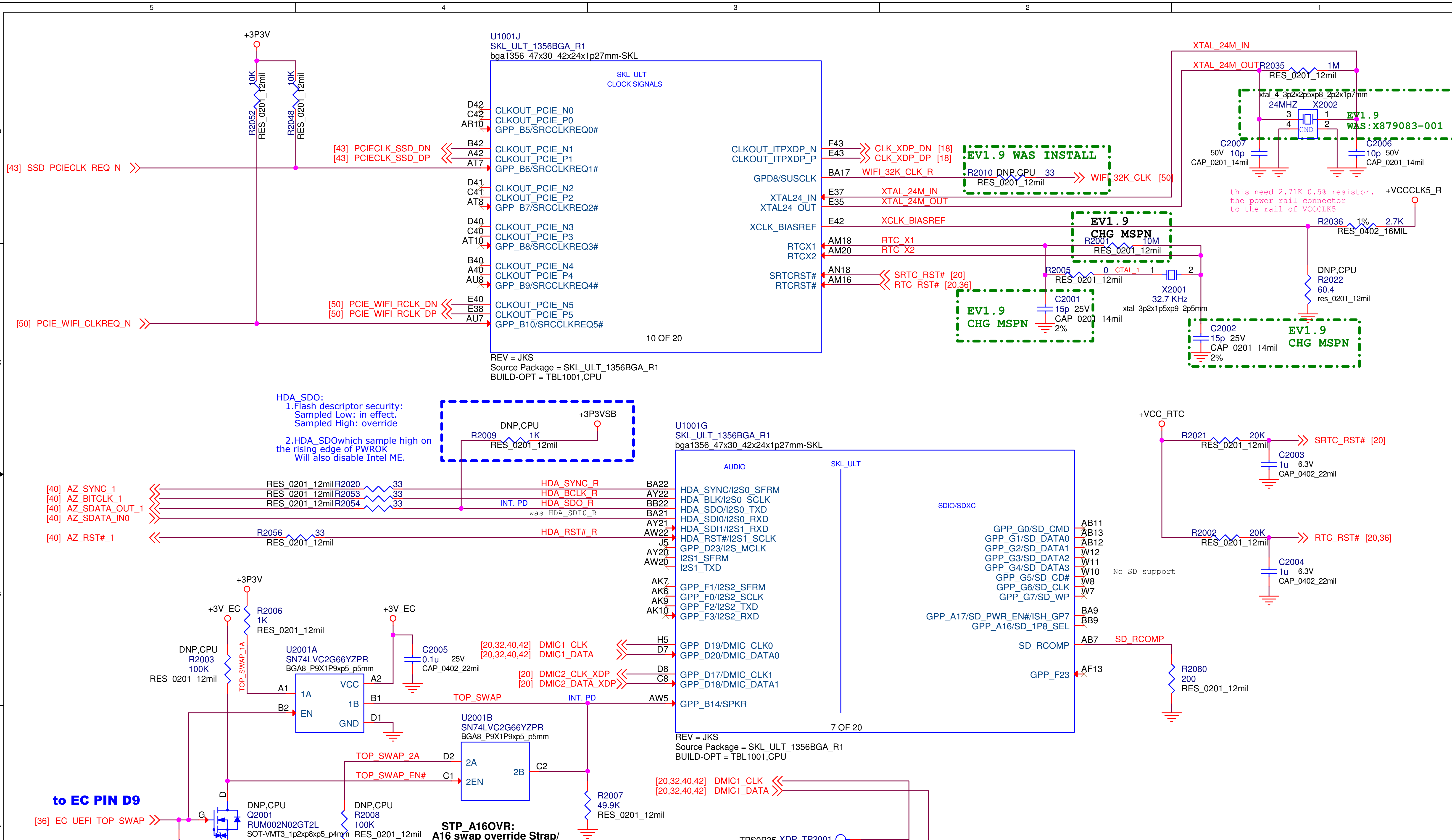

Title: PCH(1)_SD,HDA,RTC,CLK

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

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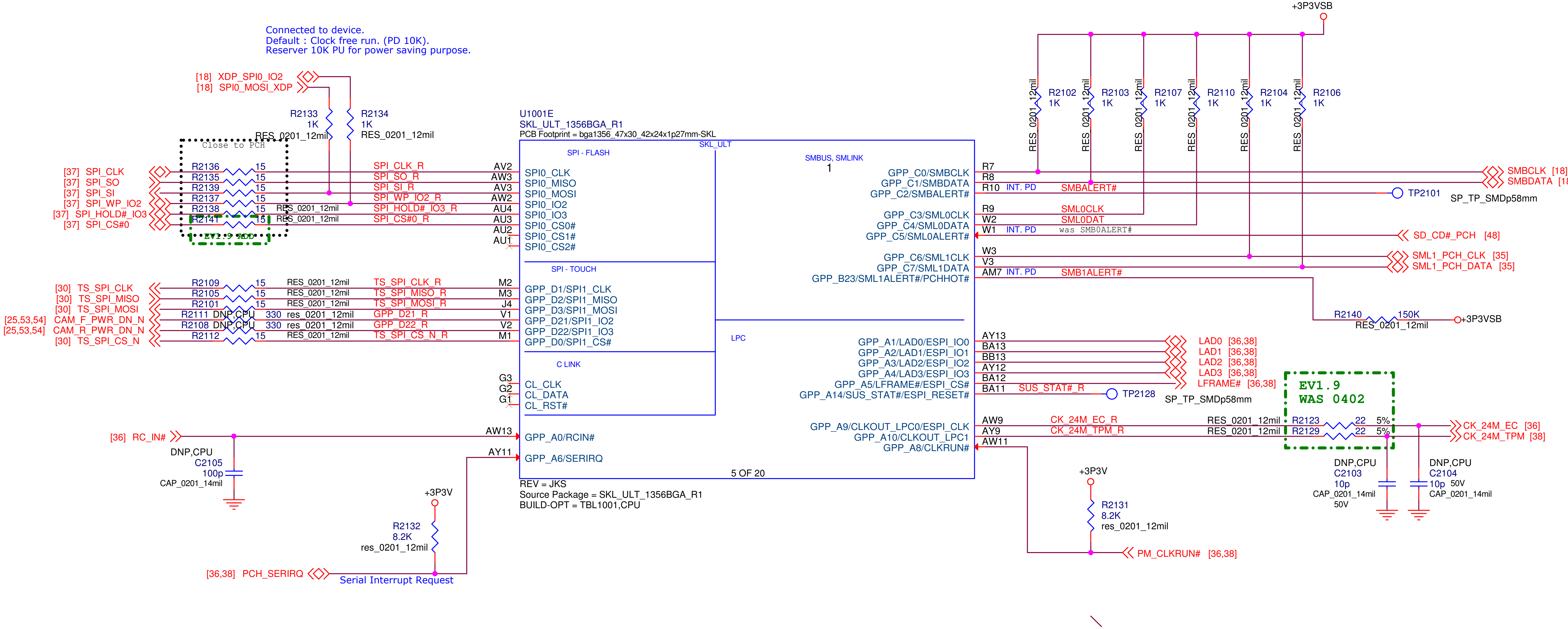

GPP_C2/SMBALERT#	
0 **Default**	Disable ME crypto TLS
1	Enable ME crypto TLS

Title: PCH(2)_CLK,SMB,LPC,SPI

Engineer: *Surface*

Size	Project Name	Rev
B	**U -- EV 1.90**	1.90.2

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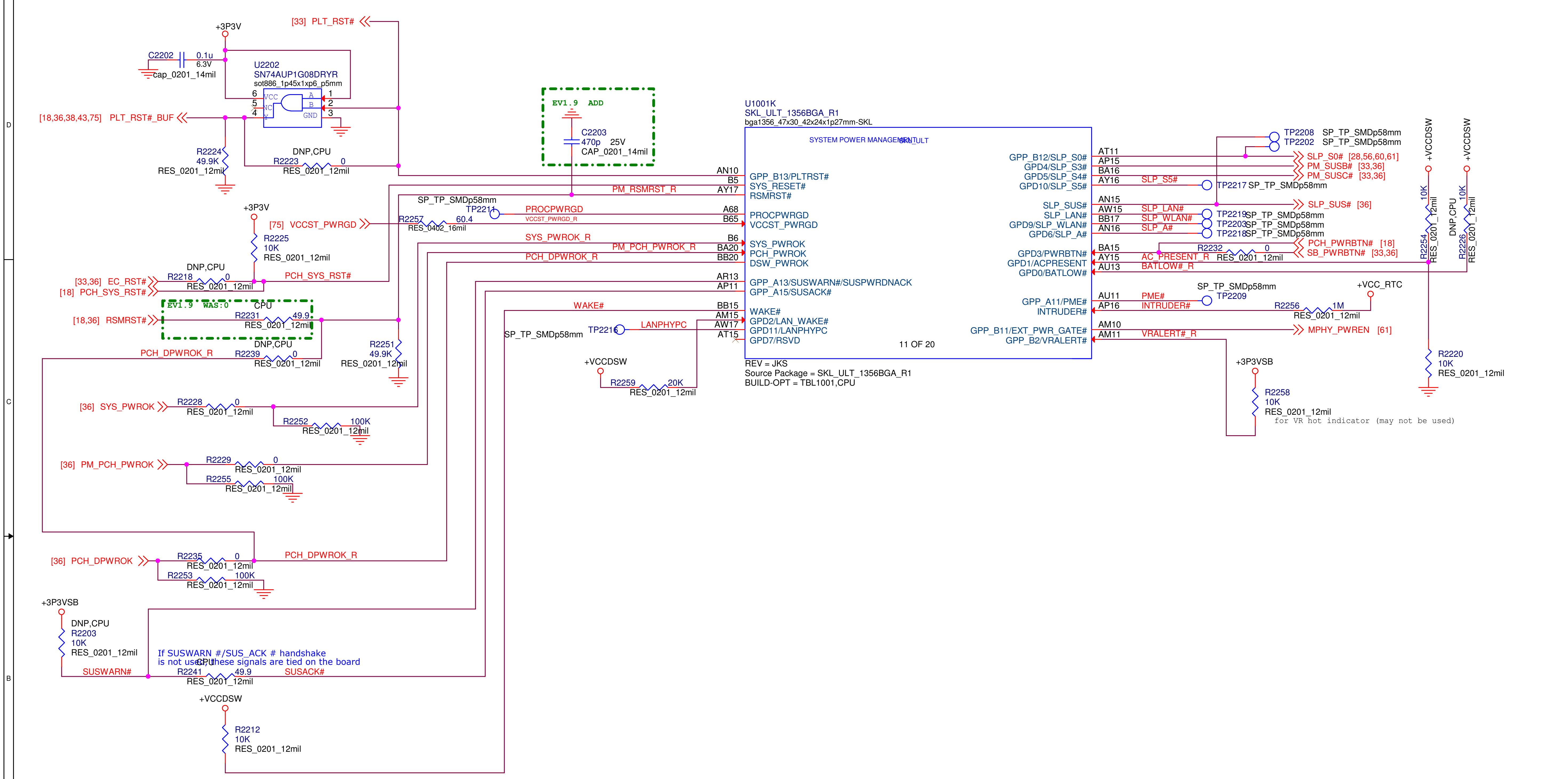

Title: PCH(3)_SYS PWR CONTR

Engineer: *Surface*

Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

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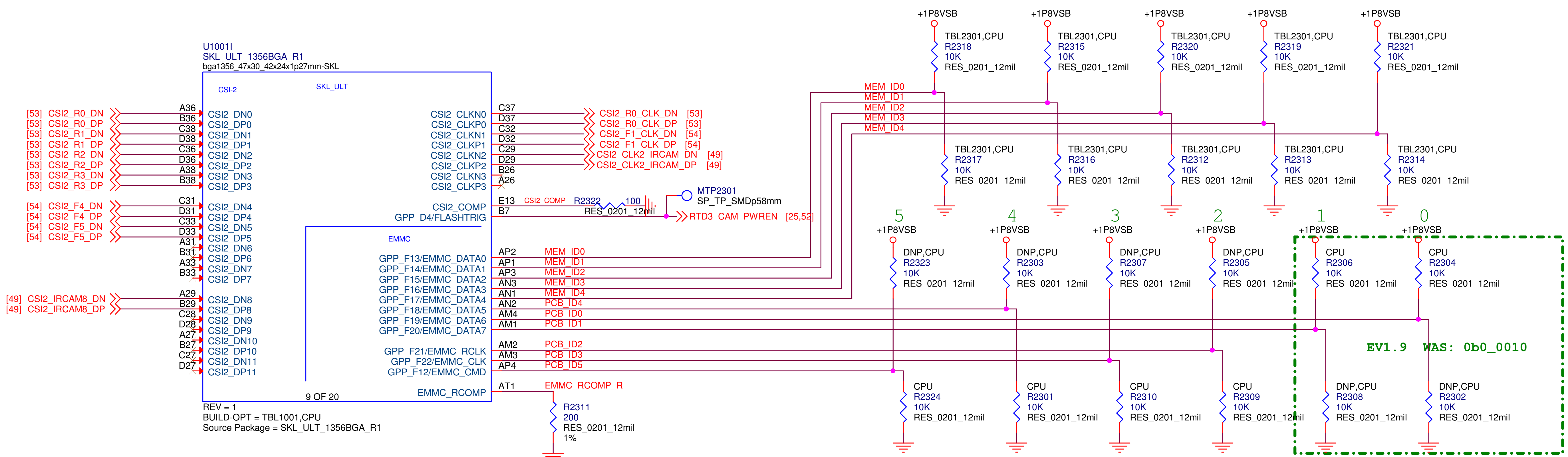
Rev 4	EC Processor ID		PCH Processor ID	TPM			EC Board Rev	PCH Board ID[3:0]				DRAM Manufacturer		RAM Speed	RAM Size & Calibration		
Signal	EC_ID1	ED_ID0	PCB_ID5	PCB_ID4			R3619	PCB_ID3	PCB_ID2	PCB_ID1	PCB_ID0	MEM_ID1	MEM_ID0	MEM_ID4	MEM_ID3	MEM_ID2	ZQ1
	1 = R3642 0 = R3643	1 = R3640 0 = R3641	1 = R2323 0 = R2324	1 = R2303 0 = R2301	R3813 R3815 R3816	R3814		1 = R2307 0 = R2310	1 = R2305 0 = R2309	1 = R2306 0 = R2308	1 = R2304 0 = R2302	1 = R2315 0 = R2316	1 = R2318 0 = R2317	1 = R2321 0 = R2314	1 = R2319 0 = R2313	1 = R2320 0 = R2312	R1602 R1604 R1702 R1704
	U22 = 0 U23E = 1 Y = 0 S = 1	**U22 = 0 U23E=0 Y = 1 S = 1**	U = 0 Y = 1	Infineon = 0 Nation Z = 1	Infineon = DNP NationZ = POP	Infineon = POP NationZ =DNP						**Hynix = 0 Samsung = 0**	**Hynix = 0 Samsung = 1**	1600 LPDDR3 = 0 1866 LPDDR3 = 1	4GB = 0 8GB = 0 16GB = 1	4 GB = 0 8 GB = 1 16 GB = 0	4GB = DNP 8GB = POP 16GB = POP
EV 0.9							80.6 Ω	0	0	0	0						
EV 1.0							169 Ω	0	0	0	1						
EV 1.5							698 Ω	0	0	1	0						
EV 1.9							909 Ω	0	0	1	1						

TBL2301



Title: PCH(4)_CCI, HWID

Engineer: Surface

Size A3 | Project Name U -- EV 1.90 | Rev 1.90.2

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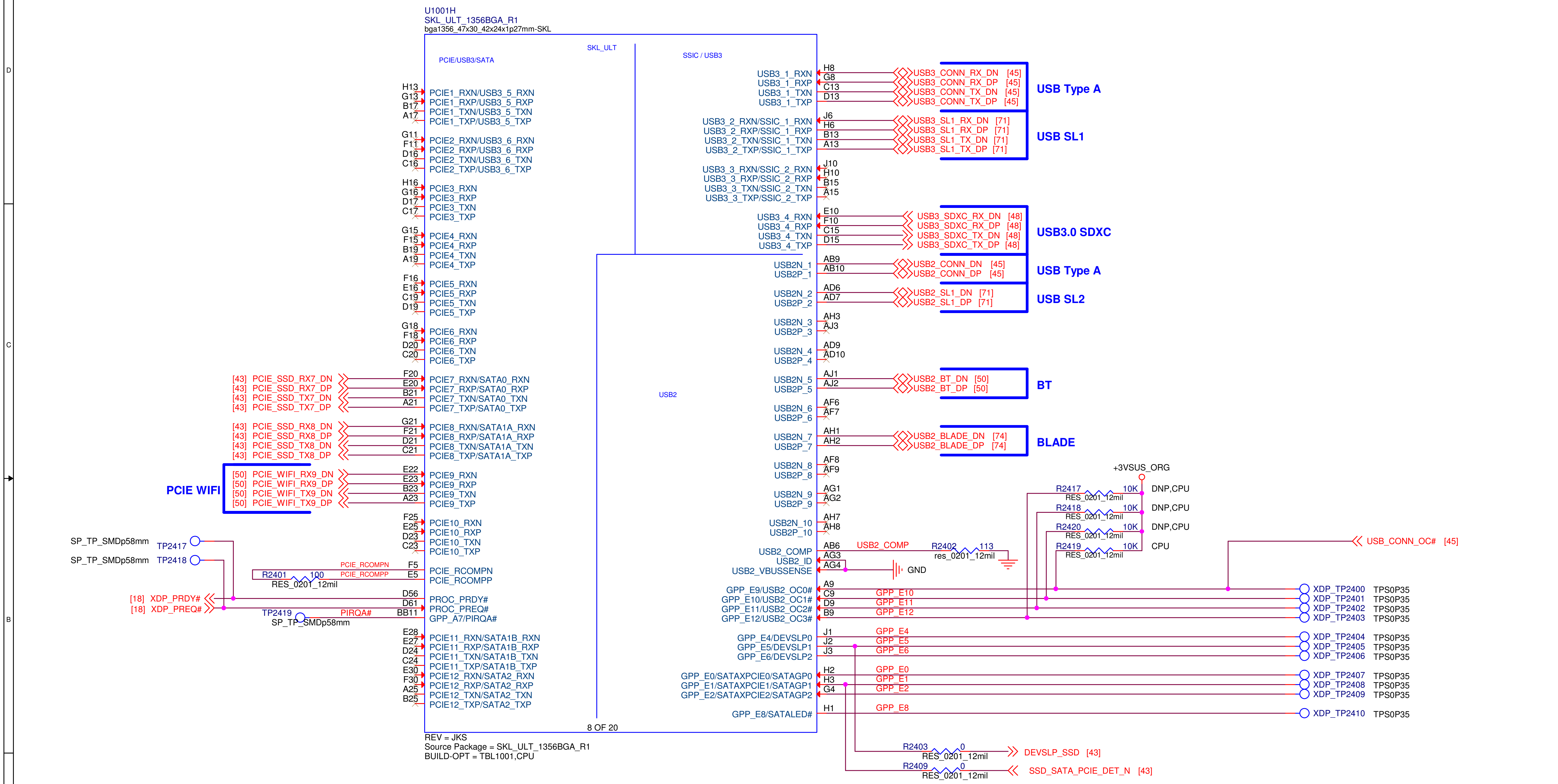

Title: PCH(5)_PCIE,USB

Engineer: *Surface*

Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

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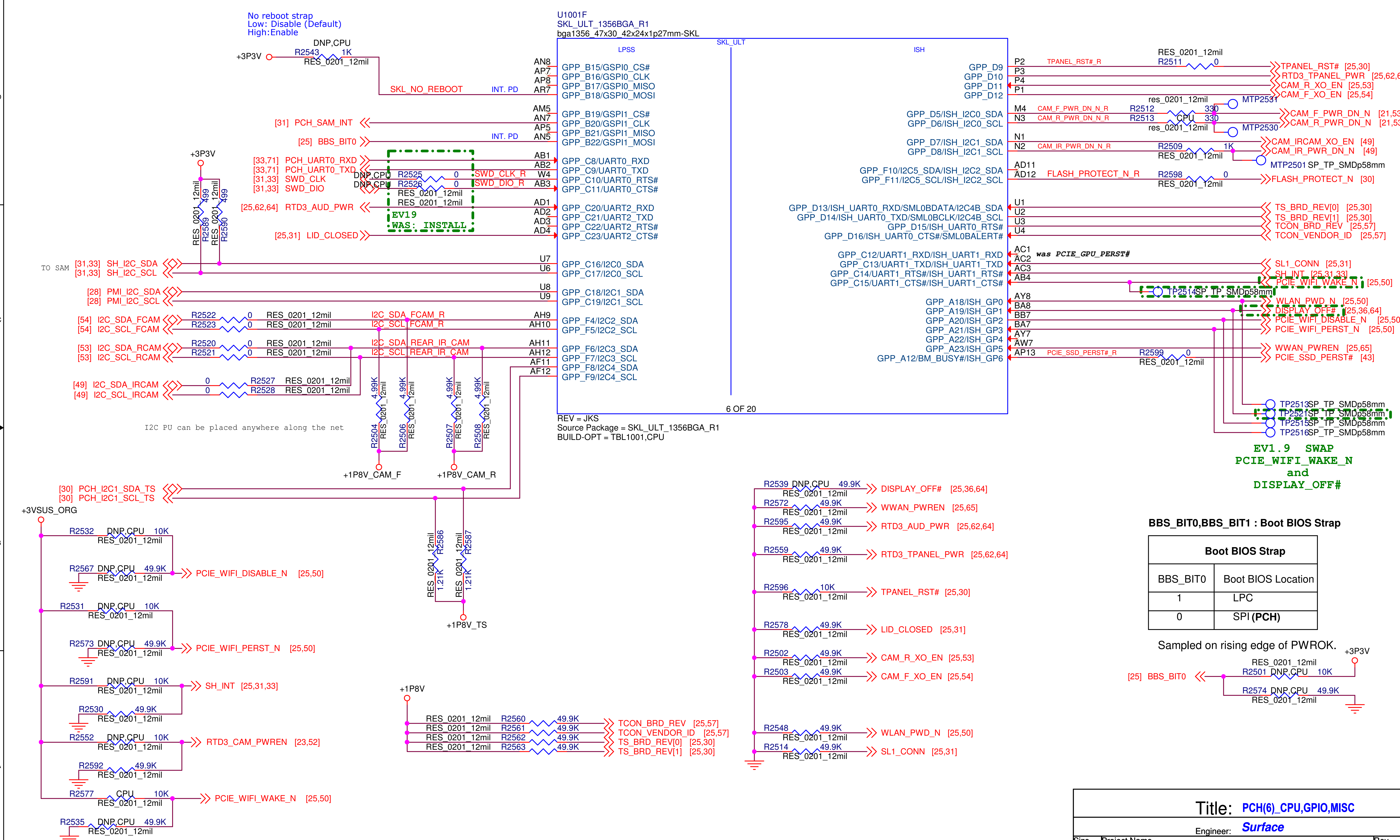

BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

Boot BIOS Strap	
BBS_BIT0	Boot BIOS Location
1	LPC
0	SPI **(PCH)**

Sampled on rising edge of PWROK.

Title: PCH(6)_CPU,GPIO,MISC

Engineer: *Surface*

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

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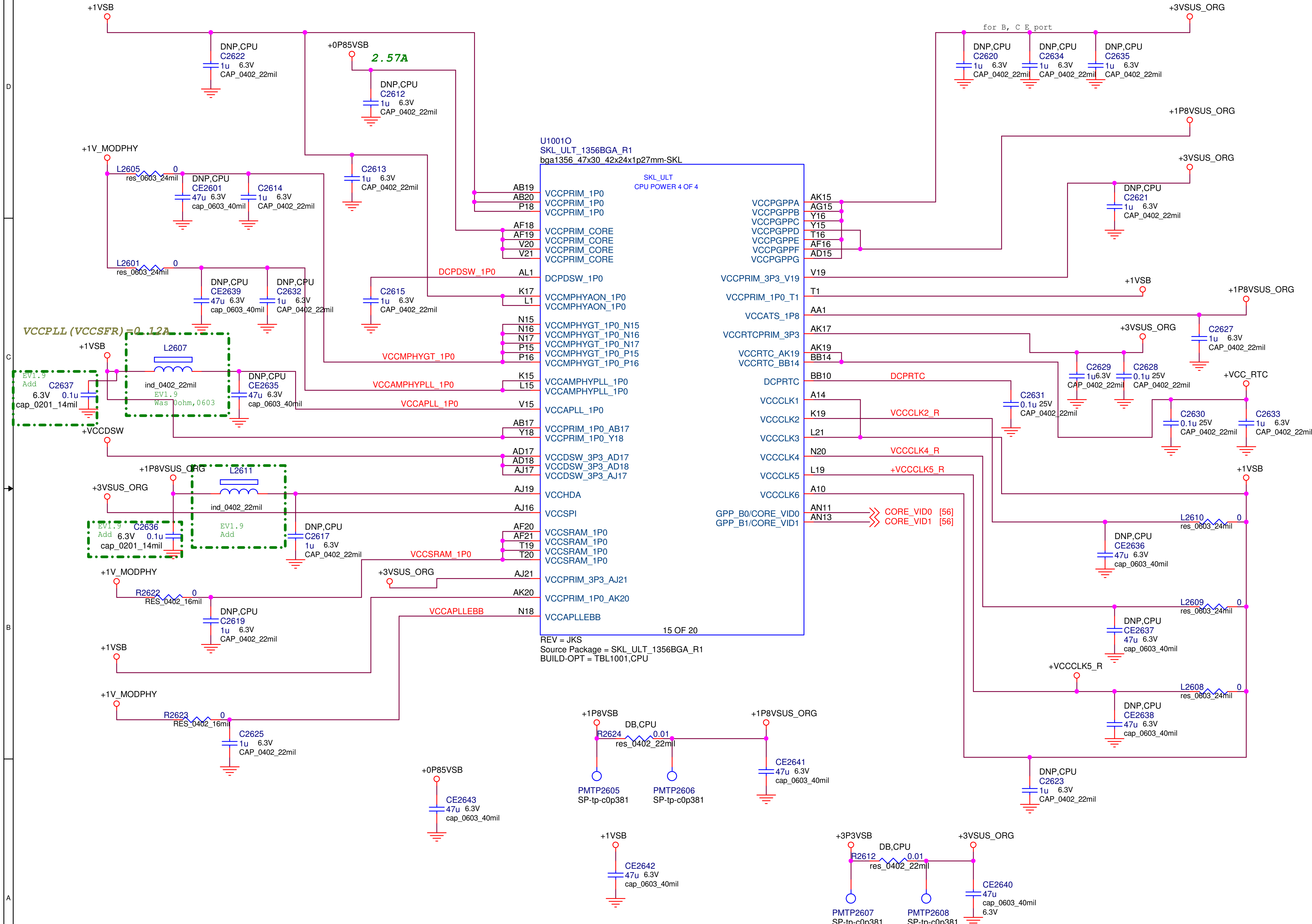

Title: PCH(7)_POWER

Engineer: Surface

Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

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Title: PCH(8)_empty

Engineer: Surface

Size	Project Name	Rev
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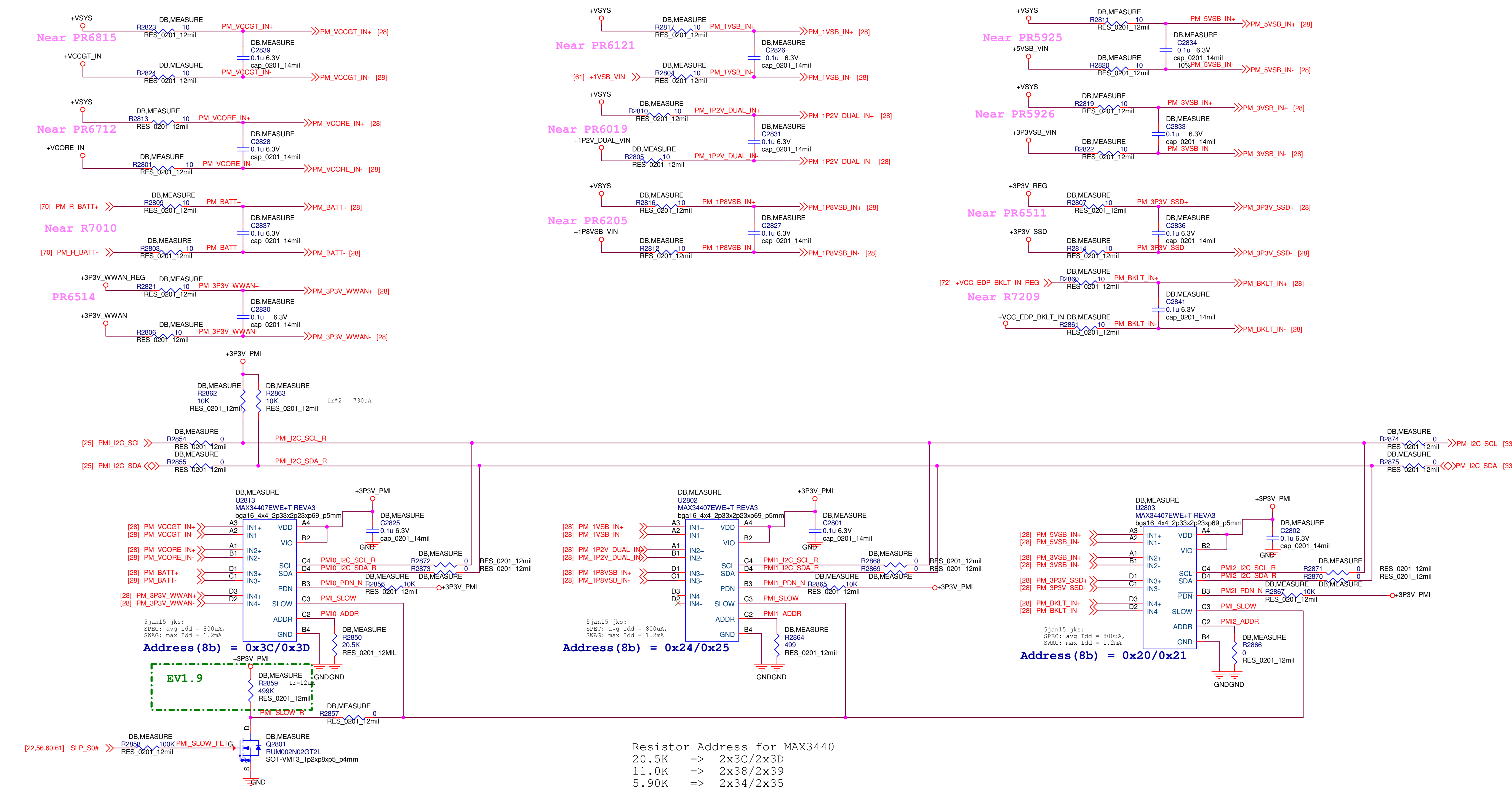


Resistor Address for MAX3440

20.5K	=>	2x3C/2x3D
11.0K	=>	2x38/2x39
5.90K	=>	2x34/2x35
3.16K	=>	2x30/2x31
1.74K	=>	2x2C/2x2D
931K	=>	2x28/2x29
499	=>	2x24/2x25
GND	=>	2x20/2x21

Title: Power Monitor

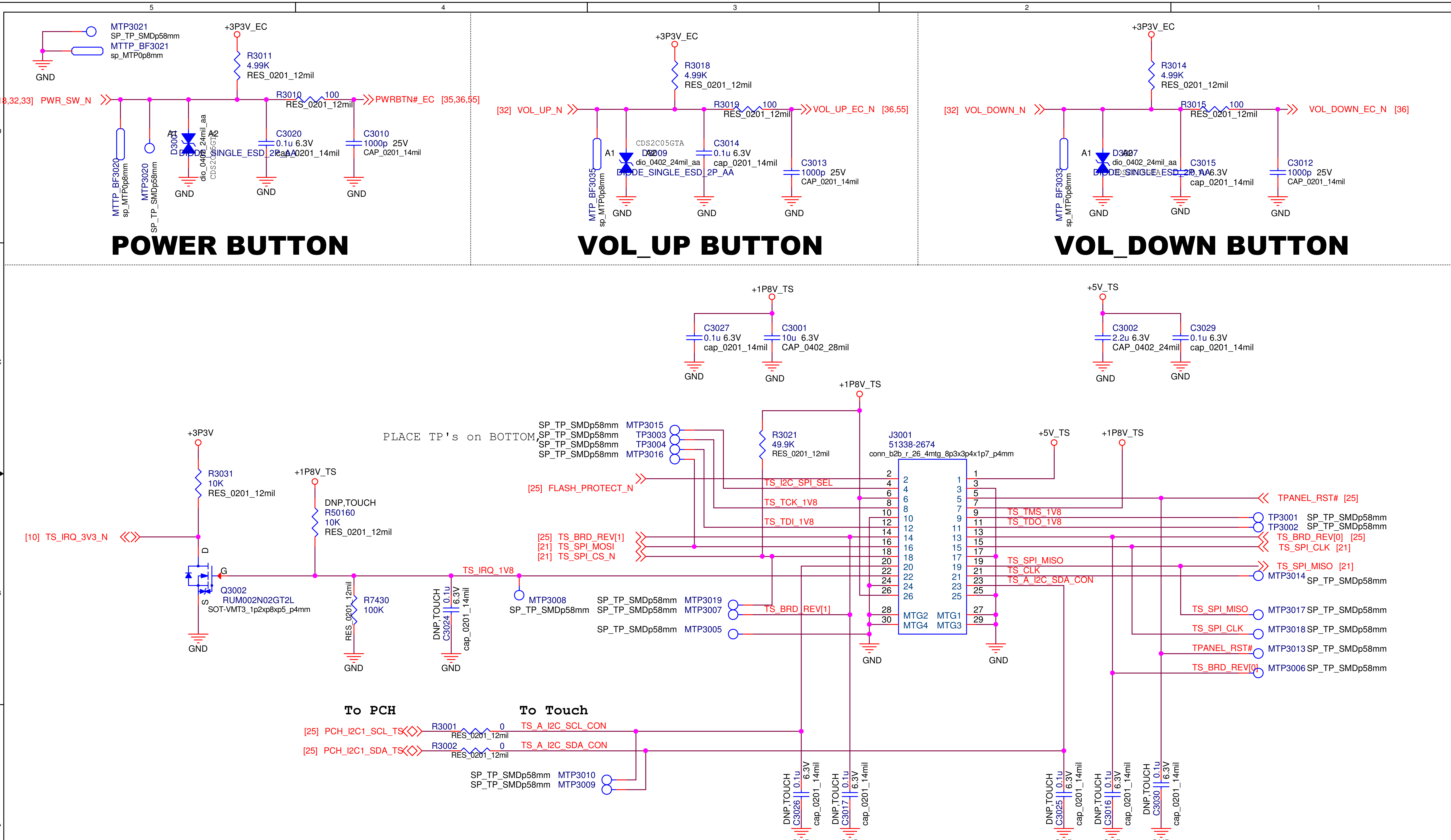
Engineer: Surface

Size: C | Project Name: U -- EV 1.90 | Rev: 1.90.2

Title:	**EMPTY**
Engineer:	***Surface***

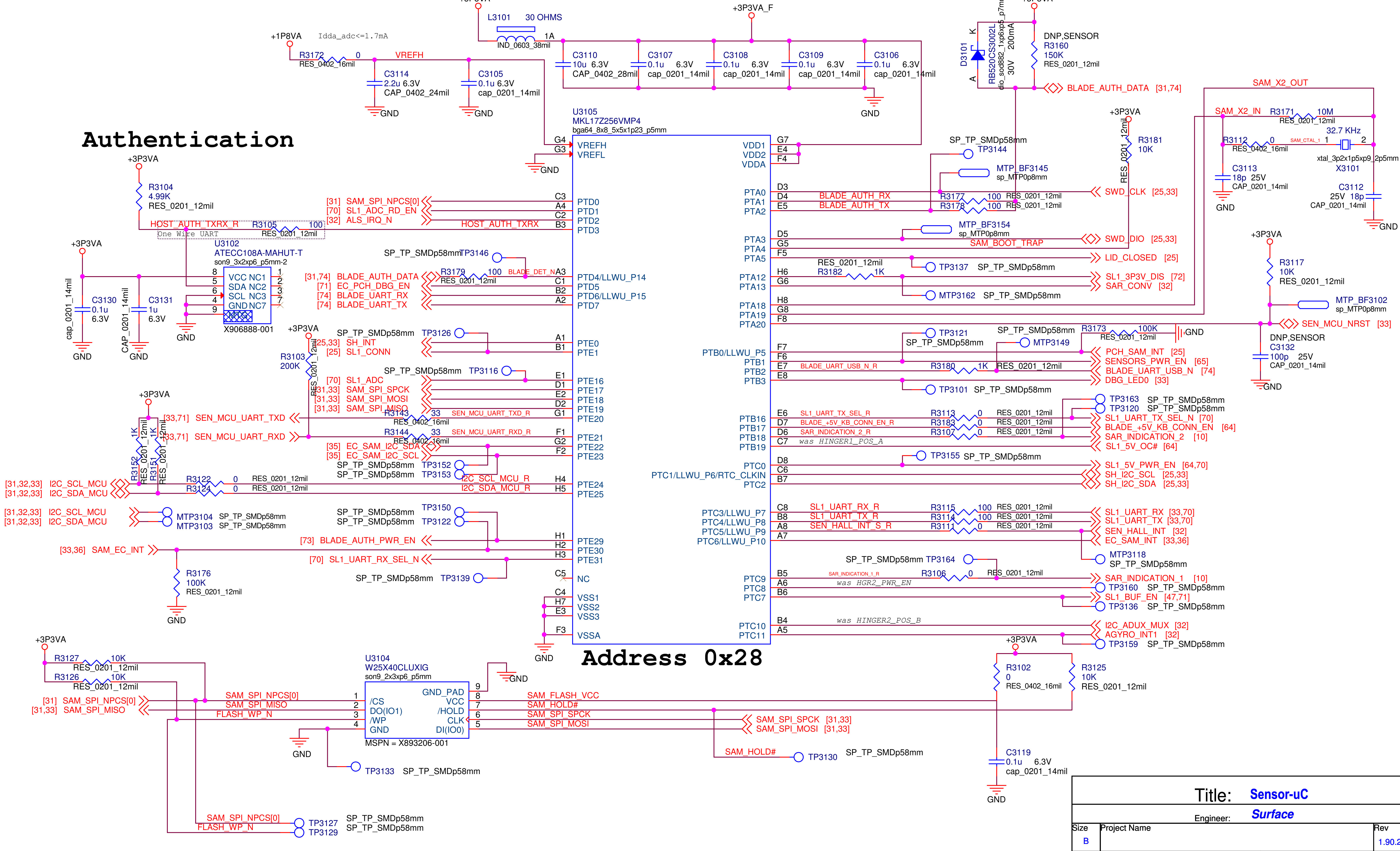
Size	Project Name	Rev
B	**U -- EV 1.90**	1.90.2

Date: Monday, May 11, 2015



Title:	Touch Con & Key
Engineer:	Surface
Size	B
Project Name	U -- EV 1.90
Rev	1.90.2
Date:	Monday, May 11, 2015
Sheet	30 of 76

SENSOR MCU

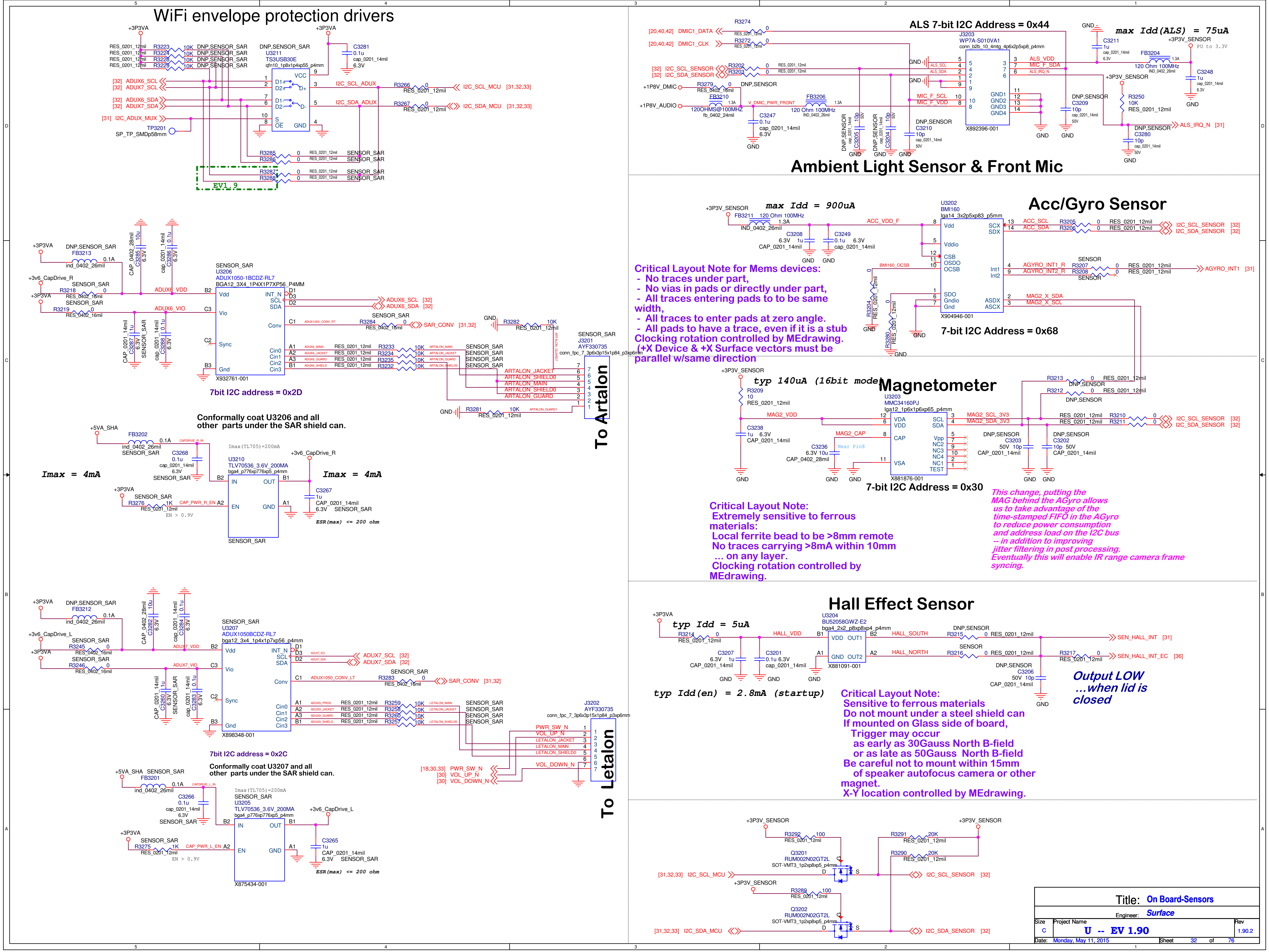


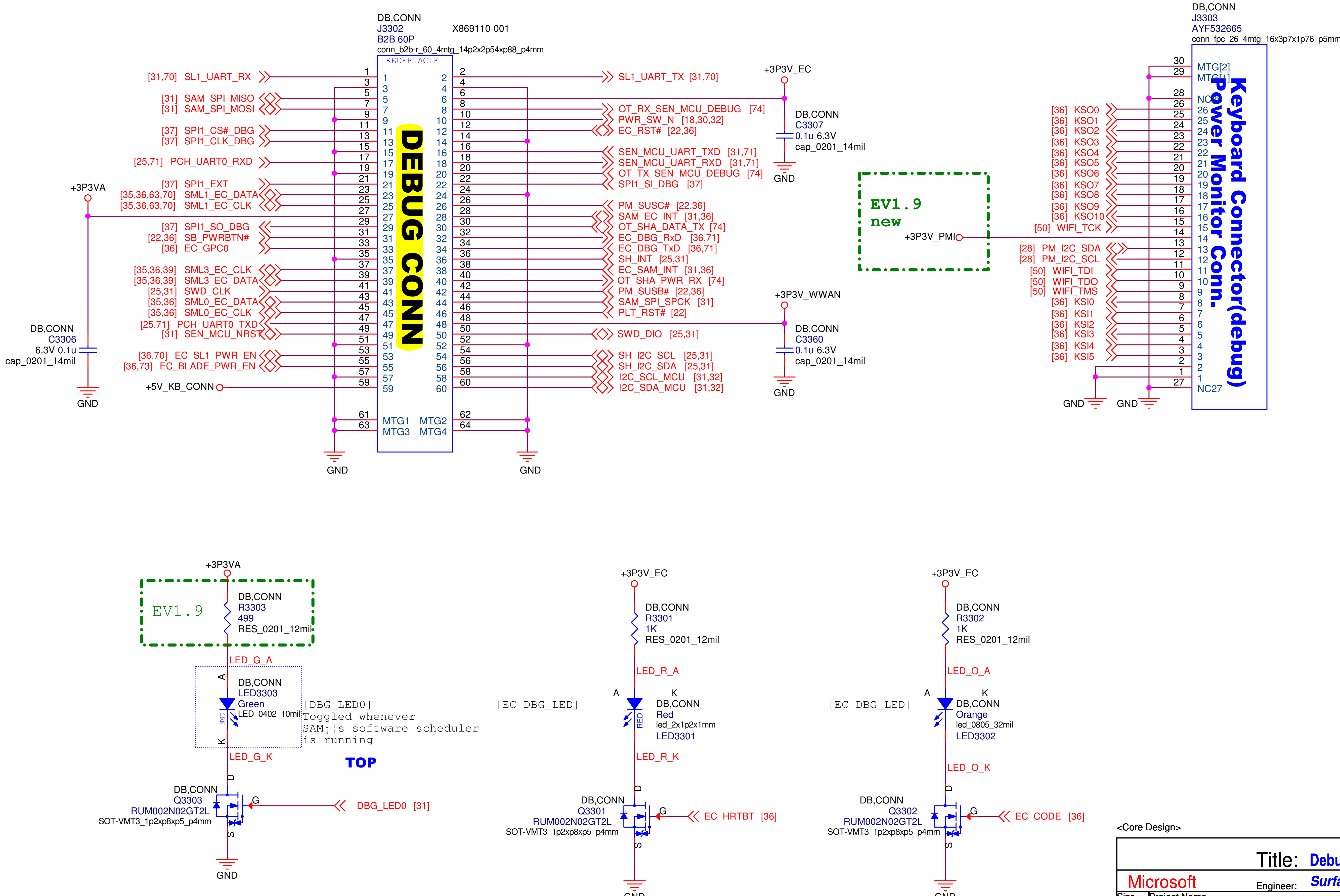
Title: **Sensor-uC**

Engineer: ***Surface***

Size	Project Name	Rev
B		1.90.2

Date: Monday, May 11, 2015 Sheet 31 of 76


WiFi envelope protection drivers
ALS 7-bit I2C Address = 0x44
max Idd(ALS) = 75uA
Ambient Light Sensor & Front Mic
max Idd = 900uA
Acc/Gyro Sensor
Critical Layout Note for Mems devices:
- No traces under part,
- No vias in pads or directly under part,
- All traces entering pads to be same width,
- All traces to enter pads at zero angle.
- All pads to have a trace, even if it is a stub
Clocking rotation controlled by MEdrawing.
(+X Device & +X Surface vectors must be parallel w/same direction
7-bit I2C Address = 0x68
7bit I2C address = 0x2D
To Artalon
Conformally coat U3206 and all other parts under the SAR shield can.
Imax = 4mA
Imax = 4mA
ESR(max) <= 200 ohm
typ 140uA (16bit mode)
Magnetometer
7-bit I2C Address = 0x30
Critical Layout Note:
Extremely sensitive to ferrous materials:
Local ferrite bead to be >8mm remote
No traces carrying >8mA within 10mm
... on any layer.
Clocking rotation controlled by MEdrawing.
This change, putting the MAG behind the AGyro allows us to take advantage of the time-stamped FIFO in the AGyro to reduce power consumption and address load on the I2C bus -- in addition to improving jitter filtering in post processing. Eventually this will enable IR range camera frame syncing.
Hall Effect Sensor
typ Idd = 5uA
typ Idd(en) = 2.8mA (startup)
Output LOW ...when lid is closed
Critical Layout Note:
Sensitive to ferrous materials
Do not mount under a steel shield can
If mounted on Glass side of board,
Trigger may occur
as early as 30Gauss North B-field
or as late as 50Gauss North B-field
Be careful not to mount within 15mm
of speaker autofocus camera or other magnet.
X-Y location controlled by MEdrawing.
7bit I2C address = 0x2C
Conformally coat U3207 and all other parts under the SAR shield can.
ESR(max) <= 200 ohm
To Letalon
Title: On Board-Sensors
Engineer: Surface
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 32 of 76



<Core Design>

Title: Debug Conn / LPC

Microsoft

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 33 of 76

5 4 3 2 1

D C B A

Title: **Empty**

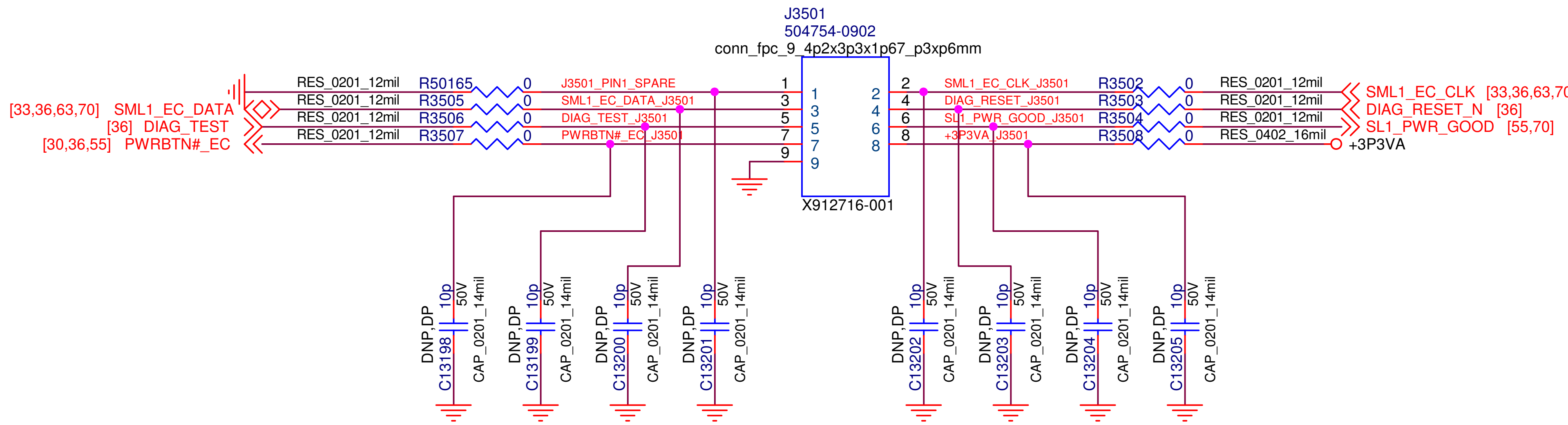
Microsoft

Engineer: ***Surface***

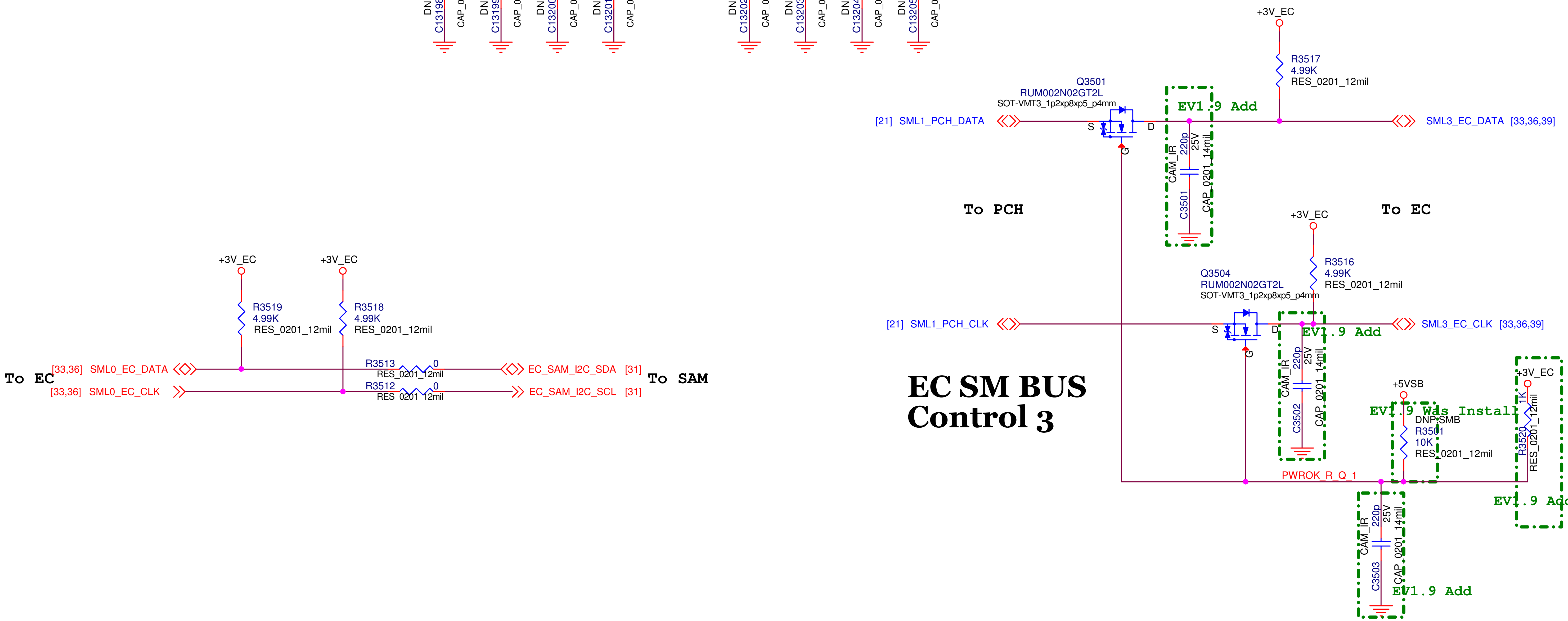
Size	Project Name	Rev
A	**U -- EV 1.90**	1.90.2

Date: Monday, May 11, 2015 Sheet 34 of 76

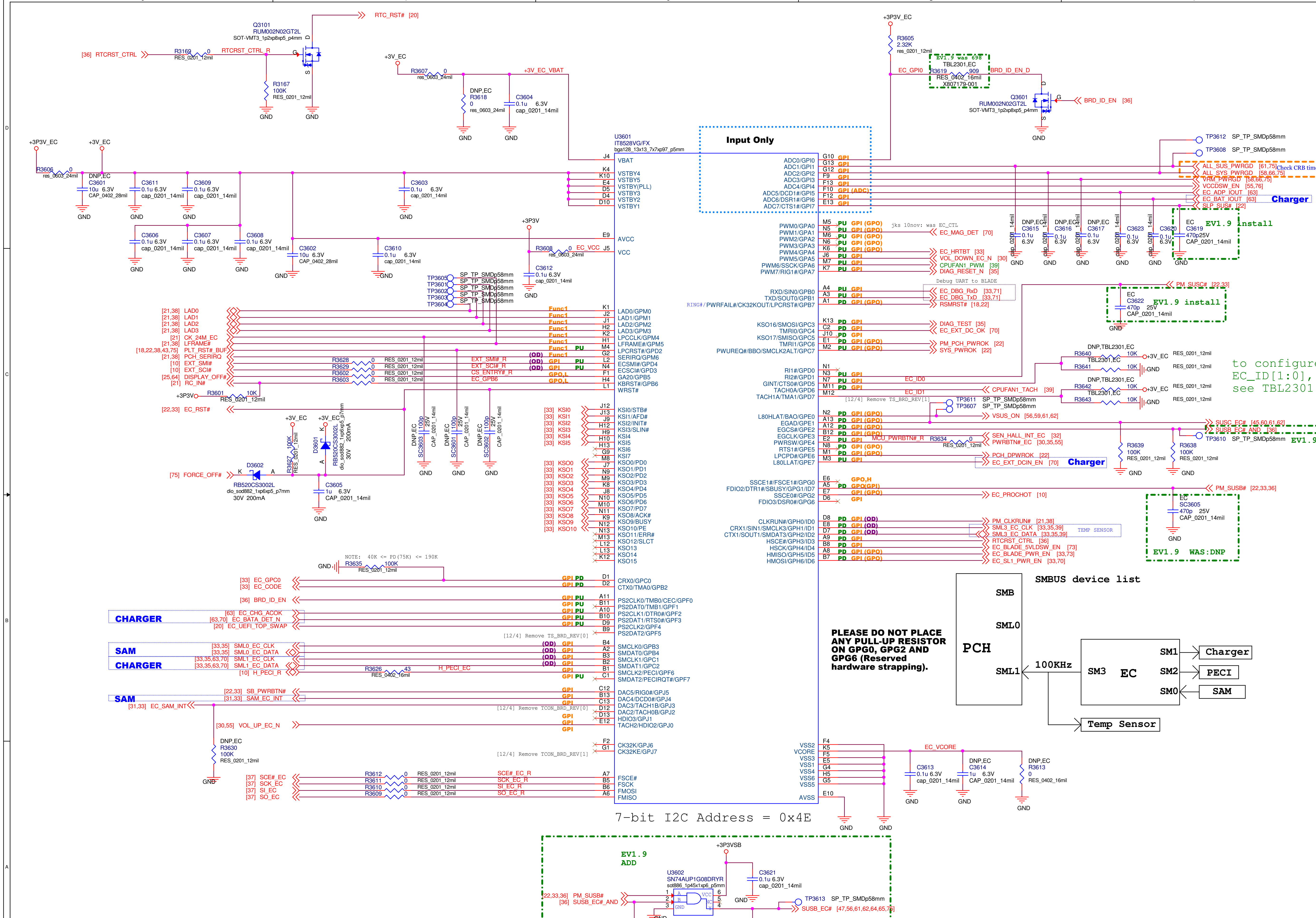
DIAGNOSTIC CONNECTOR



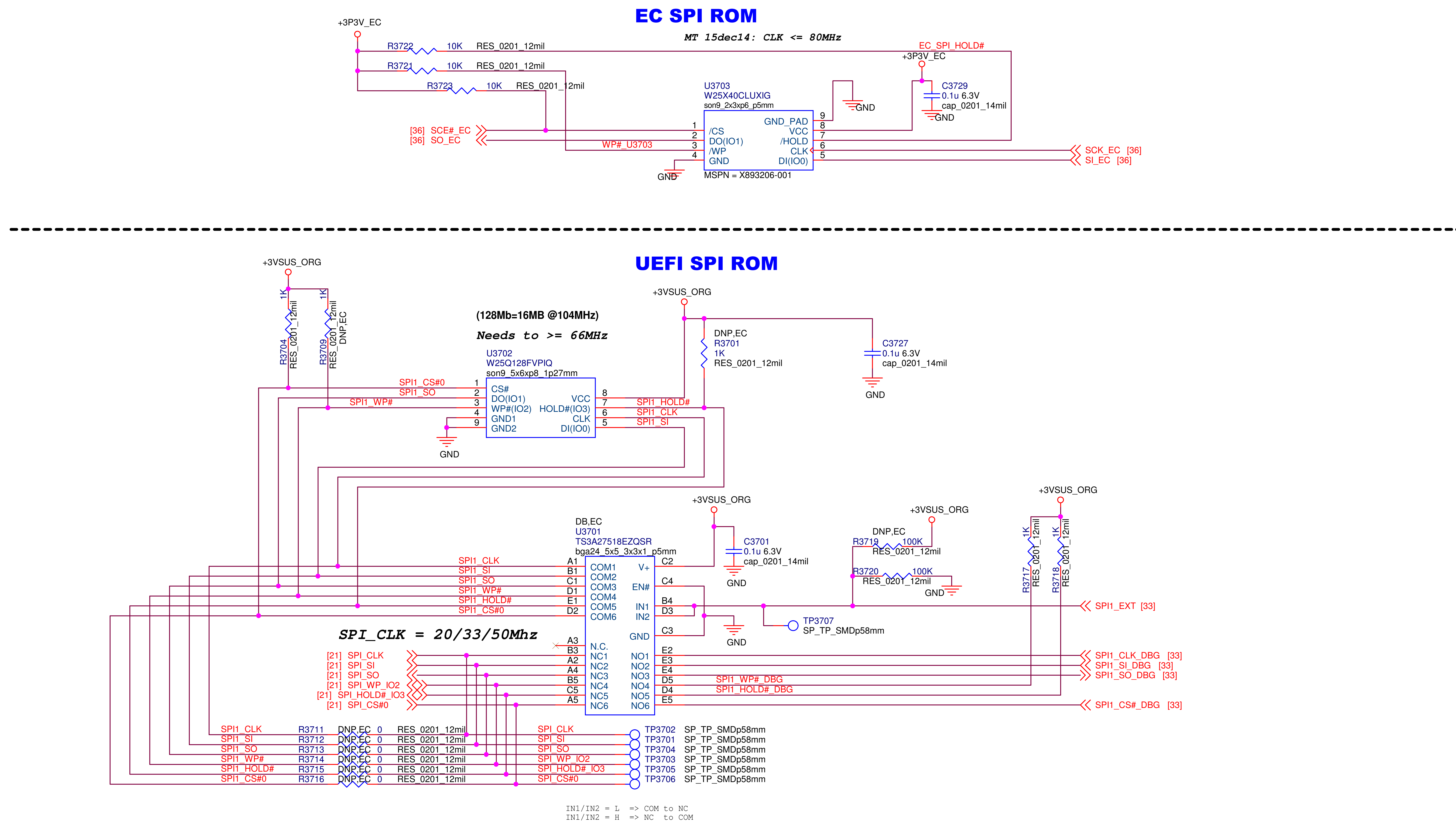
EC SM BUS Control 3



Title:	SM BUS/DIAG CONN
Microsoft	Engineer: Surface
Size: B	Project Name: U -- EV 1.90
Rev	1.90.2
Date: Monday, May 11, 2015	Sheet 35 of 76

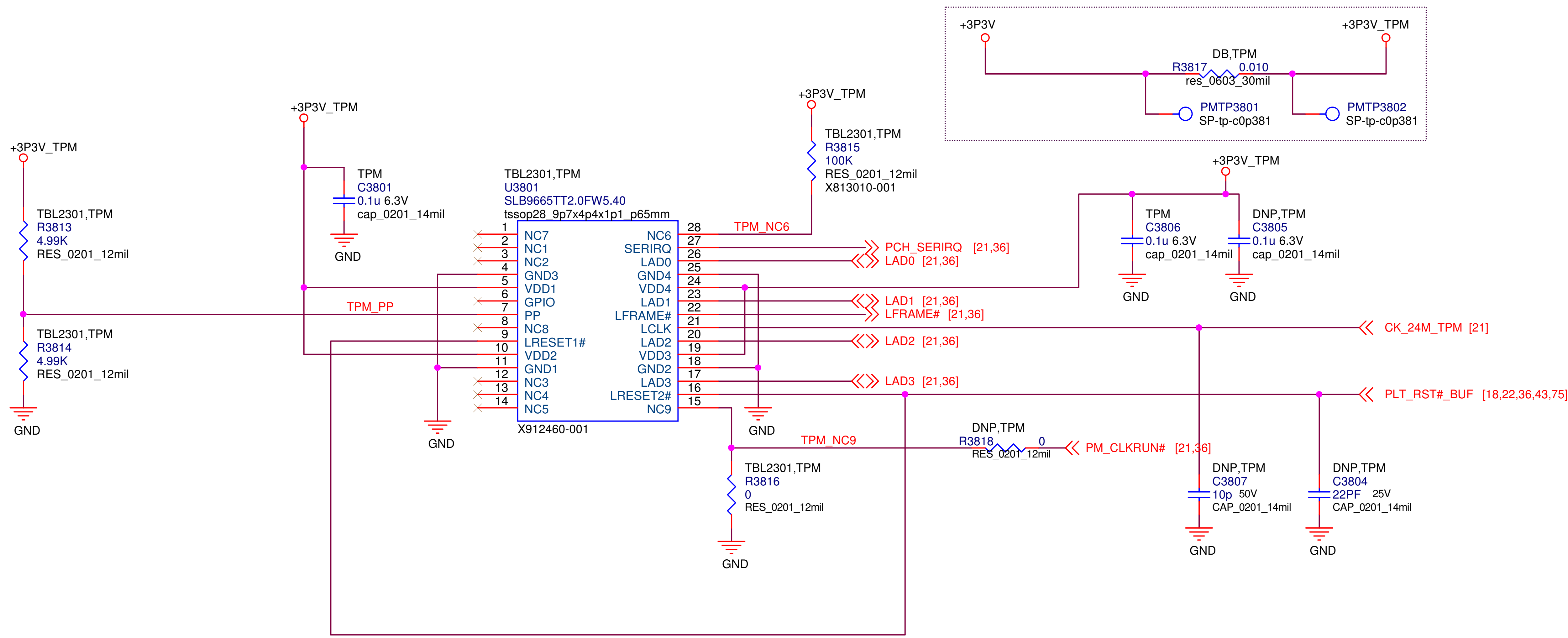


Title:	EC-ITE 8528VG-1		
Microsoft	Engineer: Surface		
Size C	Project Name U -- EV 1.90		Rev 1.90.2
Date: Monday, May 11, 2015		Sheet 36 of 76	

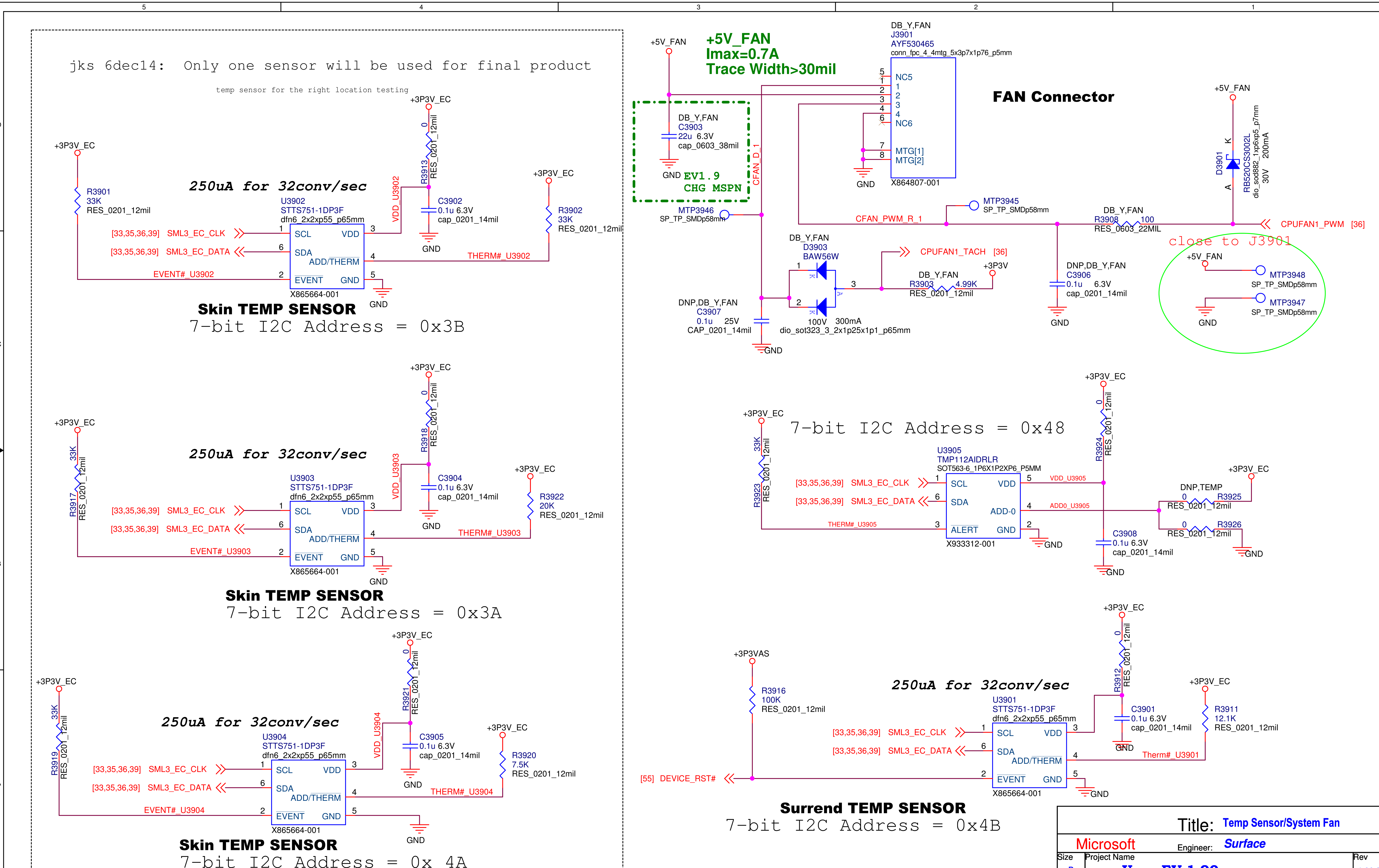


Title: EC-ITE 8528VG-2/SPI ROM		
Microsoft	Engineer: Surface	
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 37 of 76	

Trusted Platform Module



Title: TPM		
Microsoft	Engineer: Surface	
Size B	Project Name U -- EV 1.90	Rev 1.90.2
Date: Monday, May 11, 2015	Sheet 38 of 76	



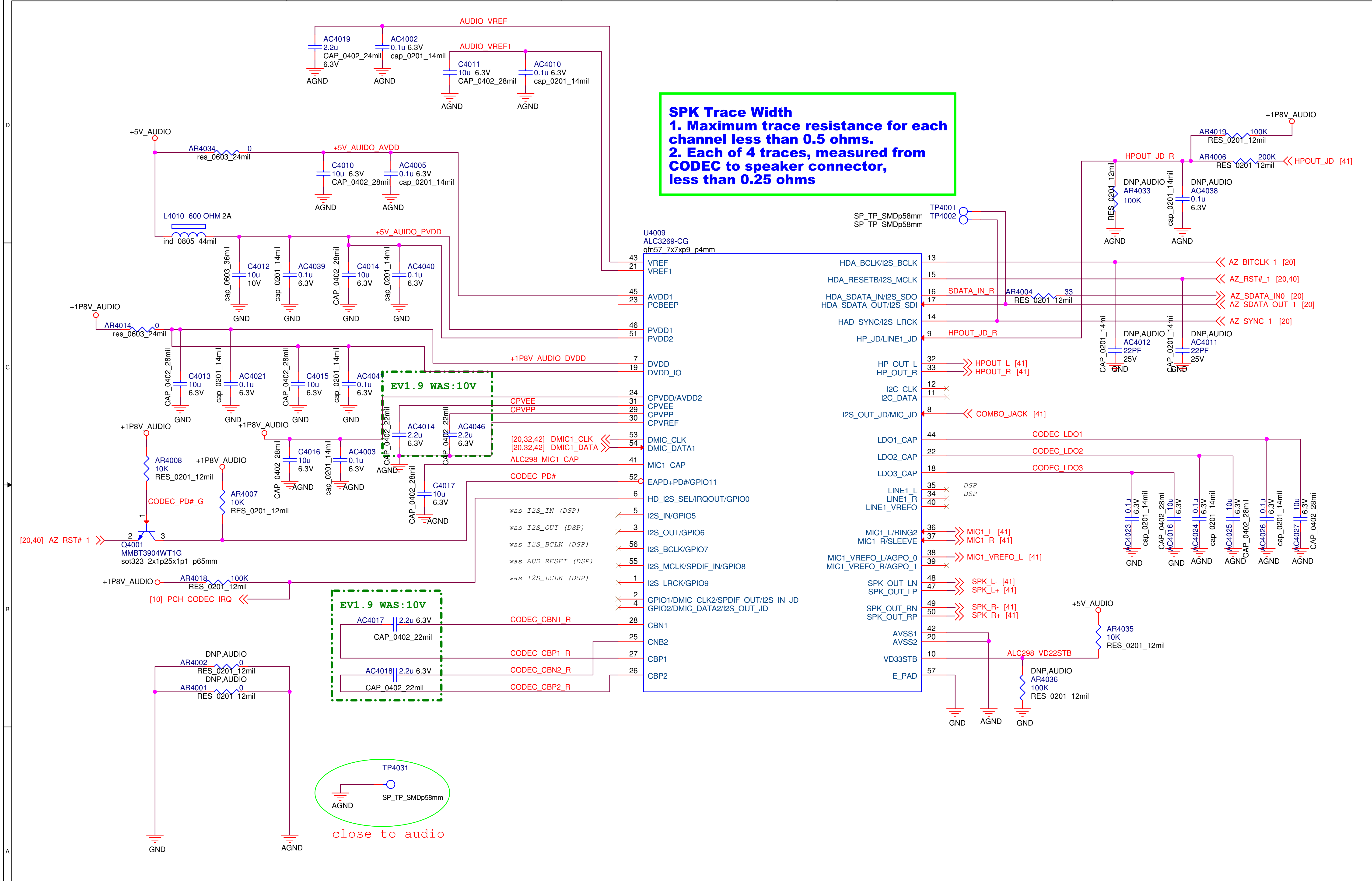
Title: Temp Sensor/System Fan

Microsoft

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 39 of 76



Title: REALTEK ALC3269 CODEC

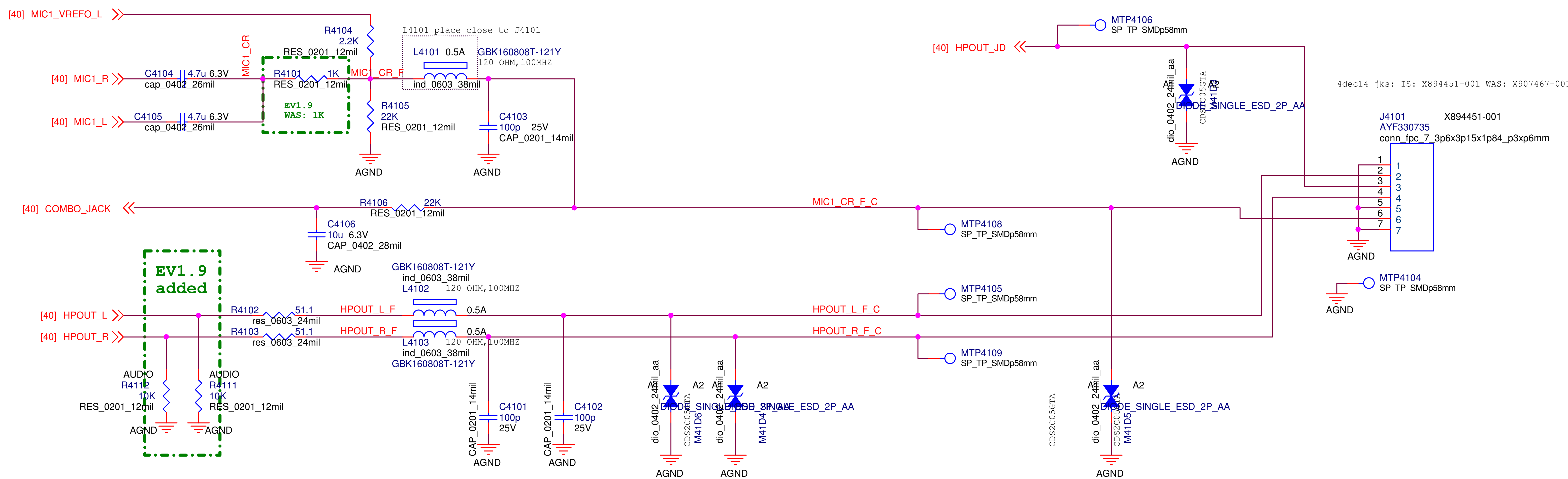
Microsoft

Engineer: *Surface*

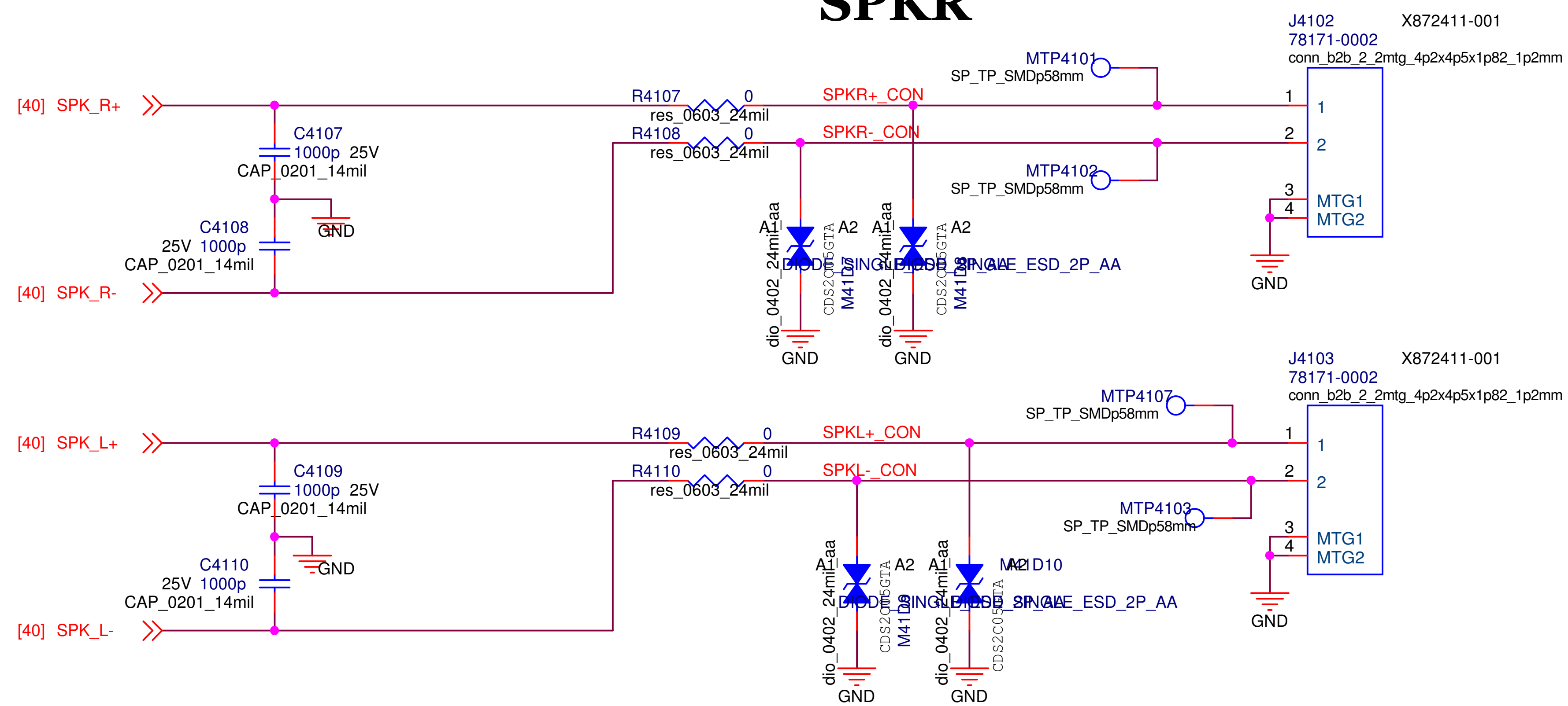
Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 40 of 76

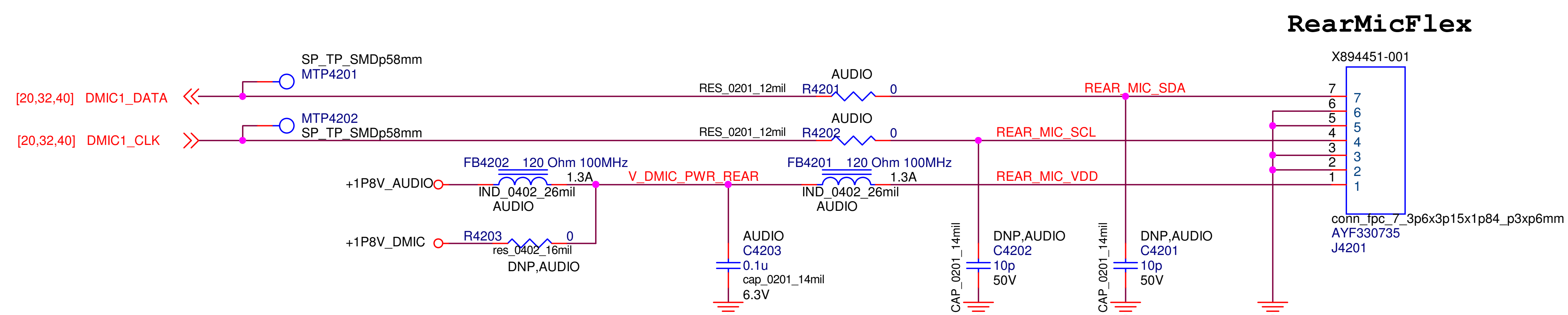
Audio Jack/MIC1 Combo Jack



SPKR



Title: Audio Jack/Speaker
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 41 of 76



Title: **Microphones**

Microsoft

Engineer: *Surface*

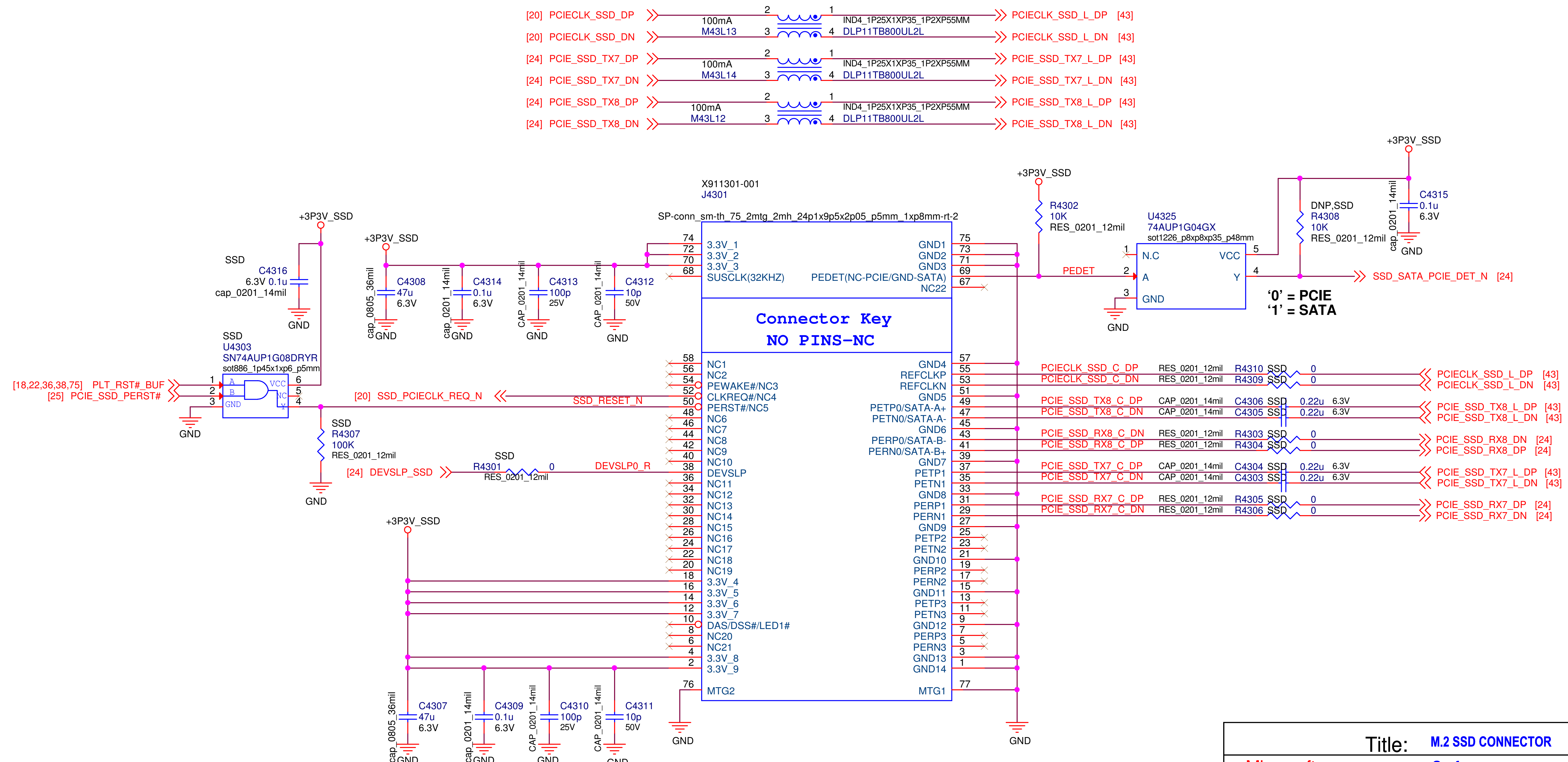
Size	Project Name	Rev
B	**U -- EV 1.90**	1.90.2

Date: Monday, May 11, 2015 Sheet 42 of 76

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen2/SATA	PCI Express* Gen3/SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF [2]	None	None [3]

2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.

3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. This option DOES NOT support DC coupled ODDs / Devices.

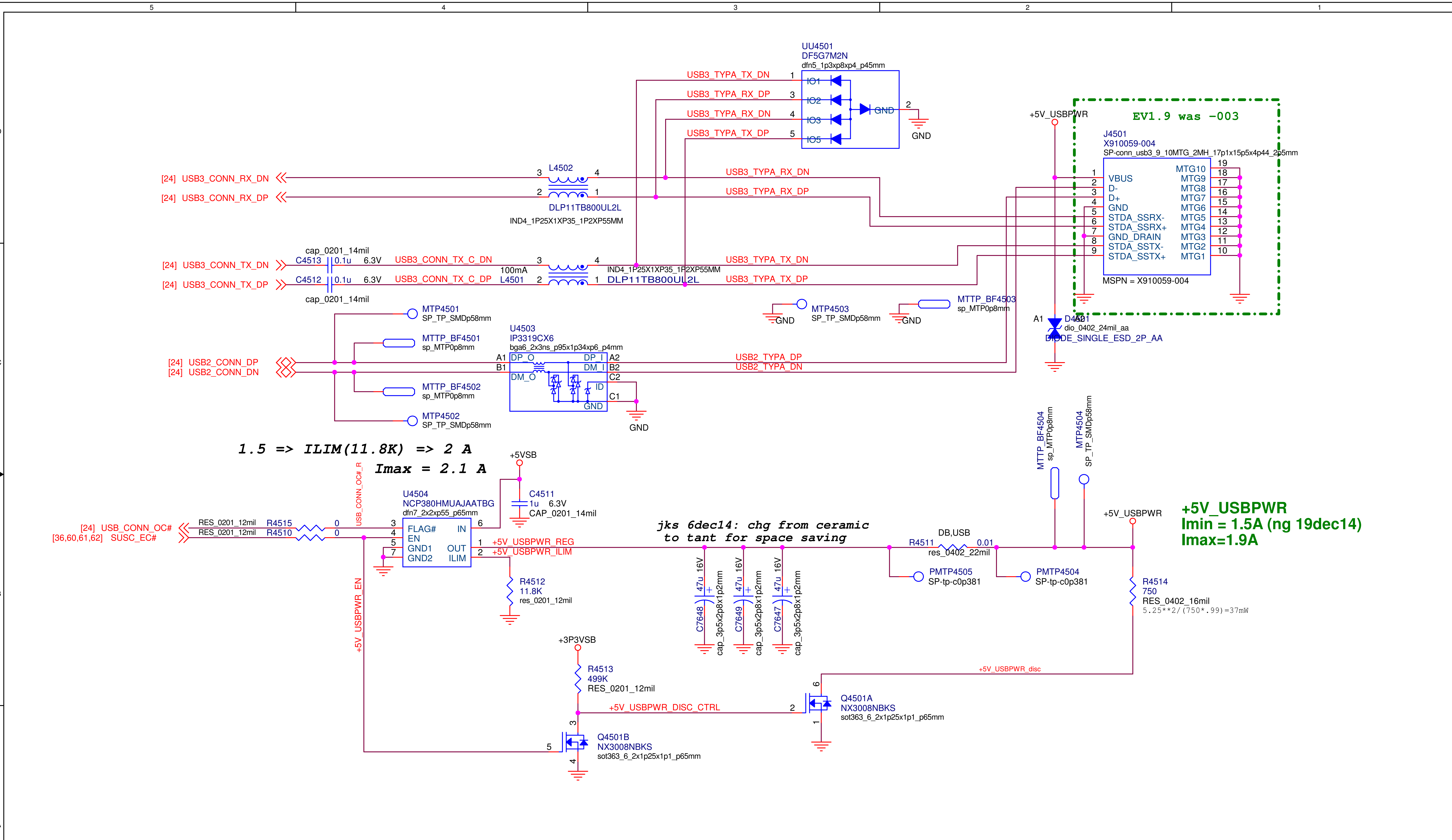


Title: M.2 SSD CONNECTOR			
Microsoft	Engineer: Surface		
Size B	Project Name U -- EV 1.90		Rev 1.90.2
Date: Monday, May 11, 2015		Sheet 43	of 76

5 4 3 2 1

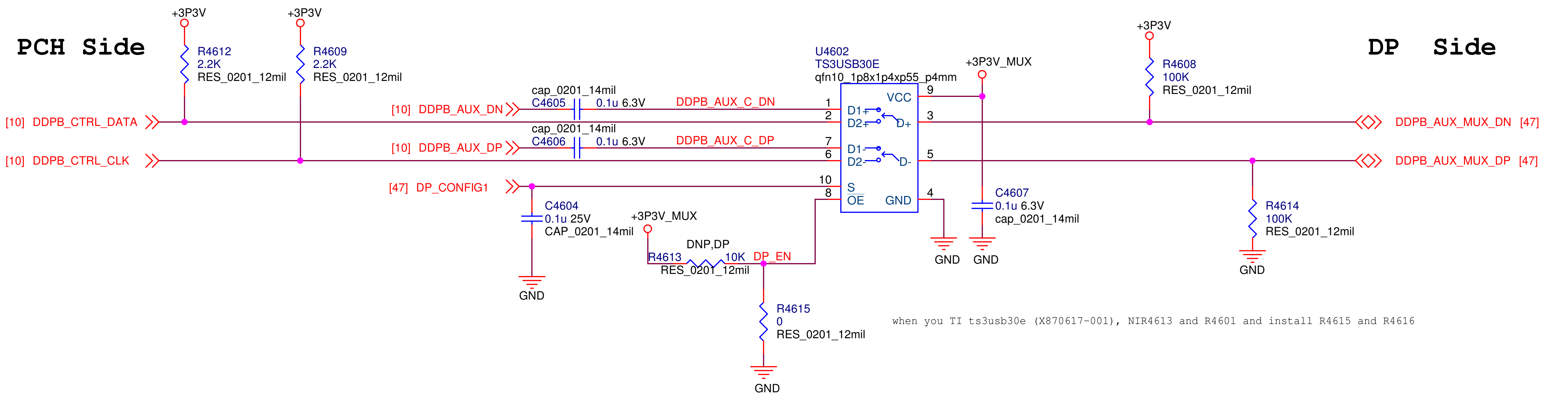
D C B A

	Title:	Empty
Microsoft	Engineer:	Surface
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 44	of 76

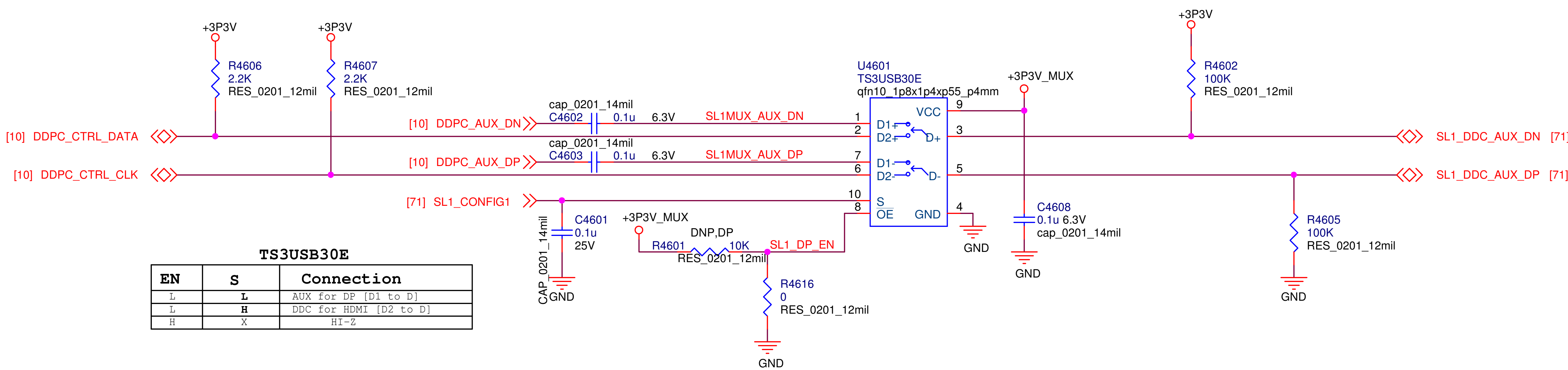


Title: USB3.0			
Microsoft	Engineer: Surface		
Size B	Project Name U -- EV 1.90		Rev 1.90.2
Date: Monday, May 11, 2015	Sheet 45	of 76	

mDP mux to HDMI/DVI Dongle control



SL1 DP mux to HDMI/DVI Dongle control



TS3USB30E

EN	S	Connection
L	L	AUX for DP [D1 to D]
L	H	DDC for HDMI [D2 to D]
H	X	HI-Z

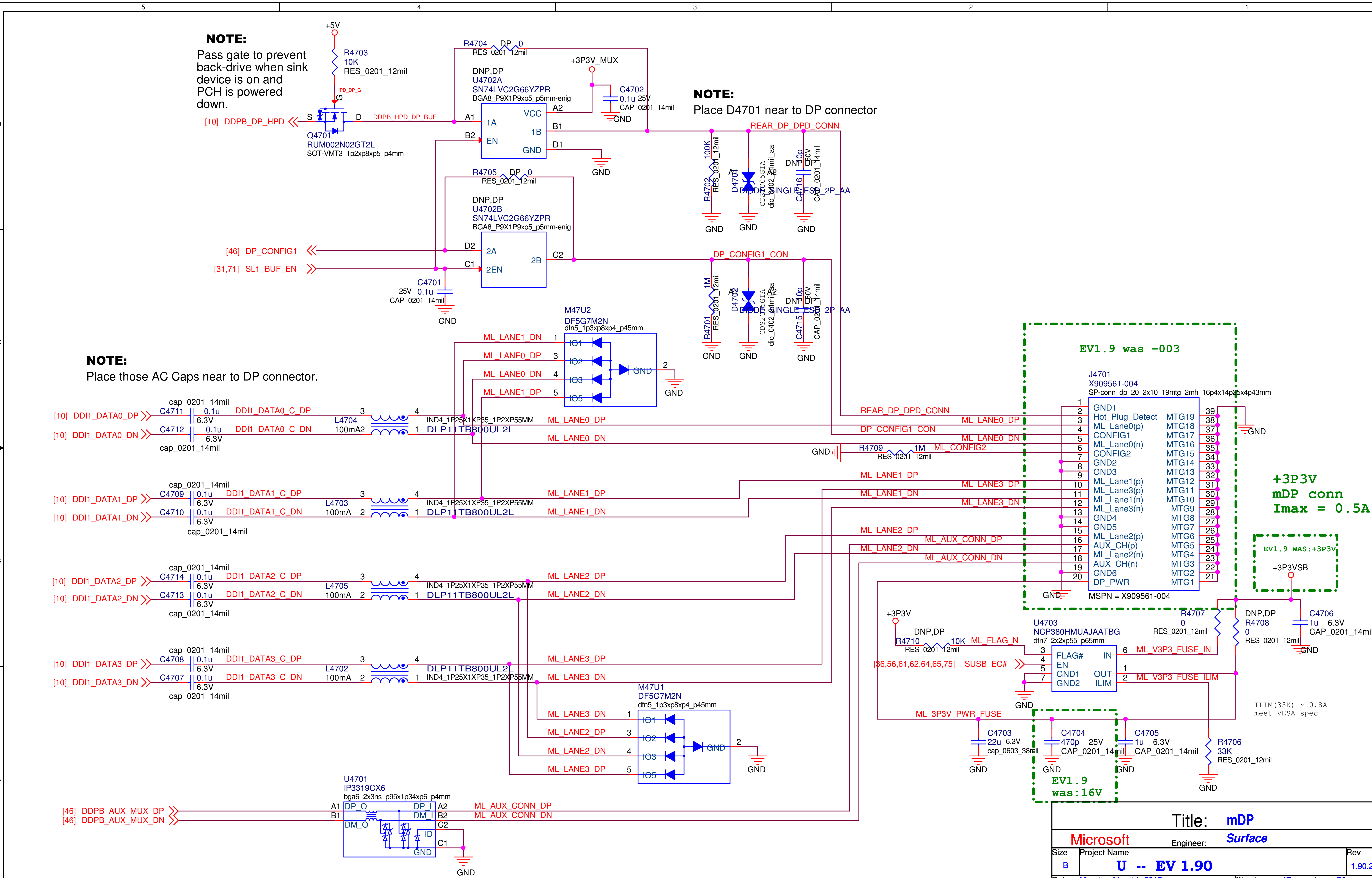
Title: **DP Dongle Control**

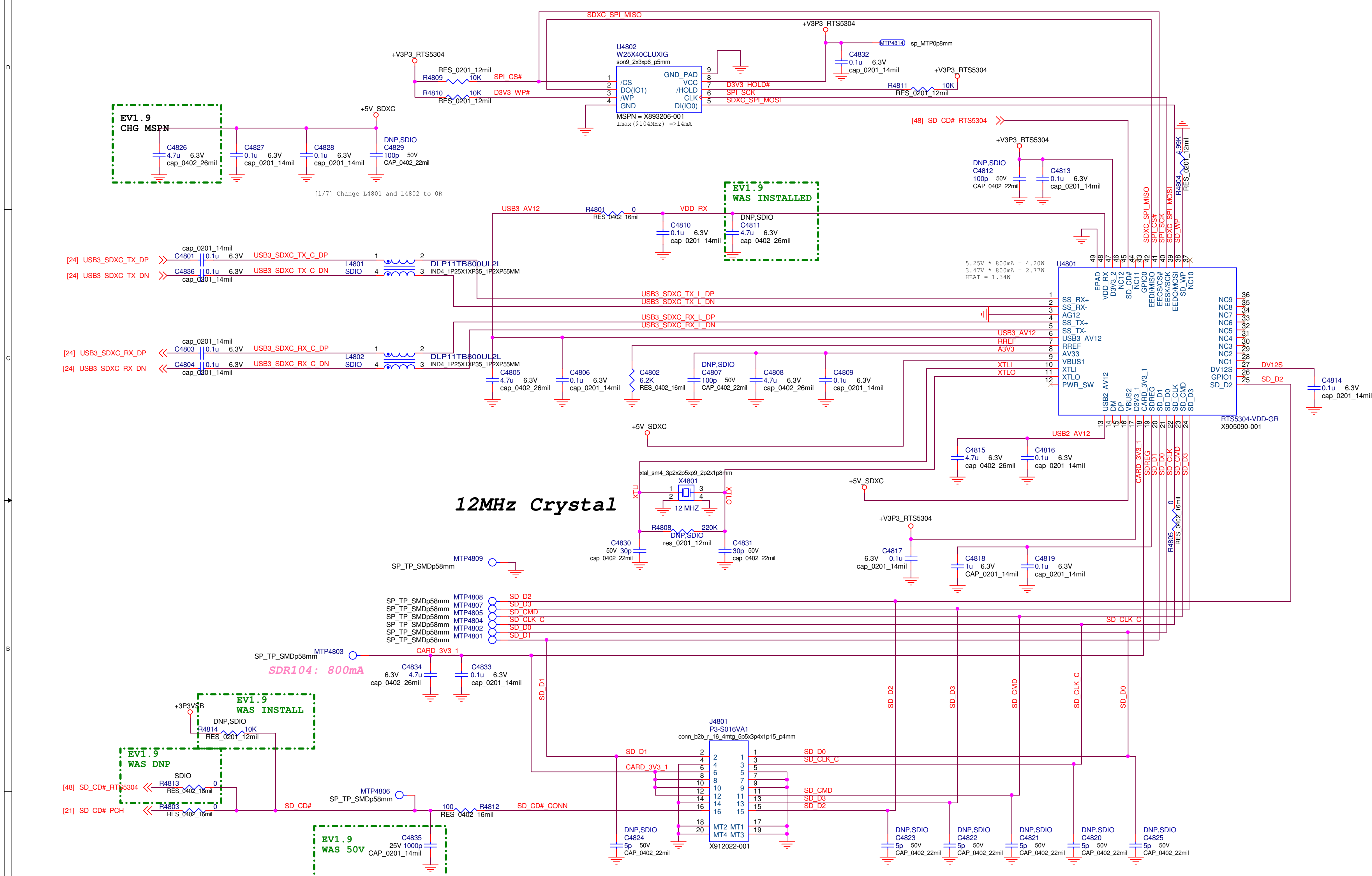
Microsoft

Engineer: *Surface*

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 46 of 76


NOTE:
Pass gate to prevent back-drive when sink device is on and PCH is powered down.
NOTE:
Place D4701 near to DP connector
NOTE:
Place those AC Caps near to DP connector.
EV1.9 was -003
J4701
X909561-004
SP-conn_dp_20_2x10_19mtg_2mh_16p4x14p25x4p43mm
MSPN = X909561-004
+3P3V
mDP conn
Imax = 0.5A
EV1.9 WAS:+3P3V
+3P3VSB
ILIM(33K) ~ 0.8A
meet VESA spec
EV1.9
was:16V
Q4701
RUM002N02GT2L
SOT-VMT3_1p2xp8xp5_p4mm
U4702A
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm-enig
U4702B
SN74LVC2G66YZPR
BGA8_P9X1P9xp5_p5mm-enig
M47U2
DF5G7M2N
dfn5_1p3xp8xp4_p45mm
M47U1
DF5G7M2N
dfn5_1p3xp8xp4_p45mm
U4701
IP3319CX6
bga6_2x3ns_p95x1p34xp6_p4mm
U4703
NCP380HMUAJAATBG
dfn7_2x2xp55_p65mm
L4704
L4703
L4705
L4702
DLP11TB800UL2L
IND4_1P25X1XP35_1P2XP55MM
[10] DDPB_DP_HPD
[46] DP_CONFIG1
[31,71] SL1_BUF_EN
[10] DDI1_DATA0_DP
[10] DDI1_DATA0_DN
[10] DDI1_DATA1_DP
[10] DDI1_DATA1_DN
[10] DDI1_DATA2_DP
[10] DDI1_DATA2_DN
[10] DDI1_DATA3_DP
[10] DDI1_DATA3_DN
[46] DDPB_AUX_MUX_DP
[46] DDPB_AUX_MUX_DN
[36,56,61,62,64,65,75] SUSB_EC#
REAR_DP_DPD_CONN
DP_CONFIG1_CON
ML_CONFIG2
ML_3P3V_PWR_FUSE
ML_V3P3_FUSE_IN
ML_V3P3_FUSE_ILIM
ML_FLAG_N
Title: mDP
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 47 of 76



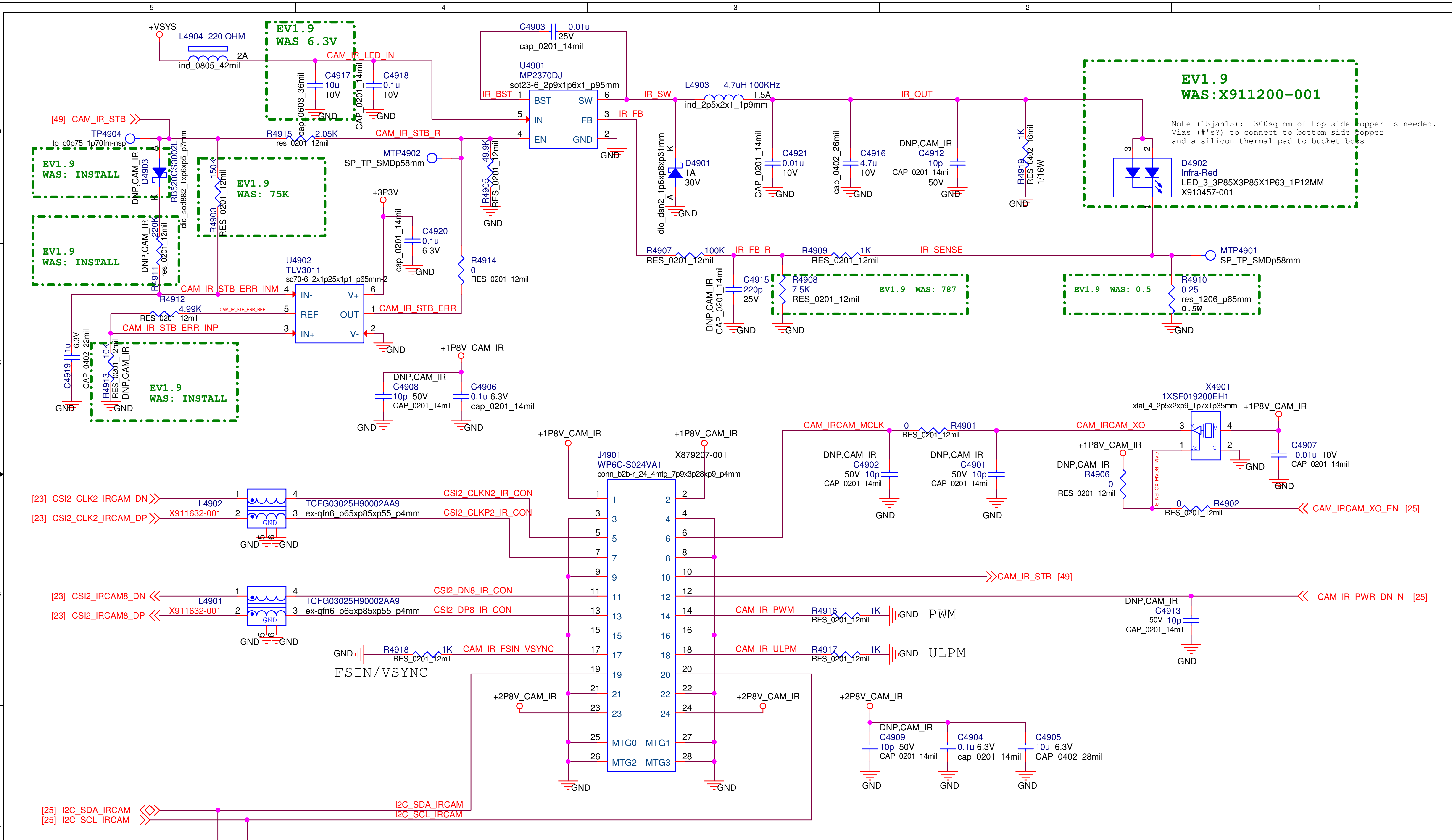
Title: SDXC

Microsoft

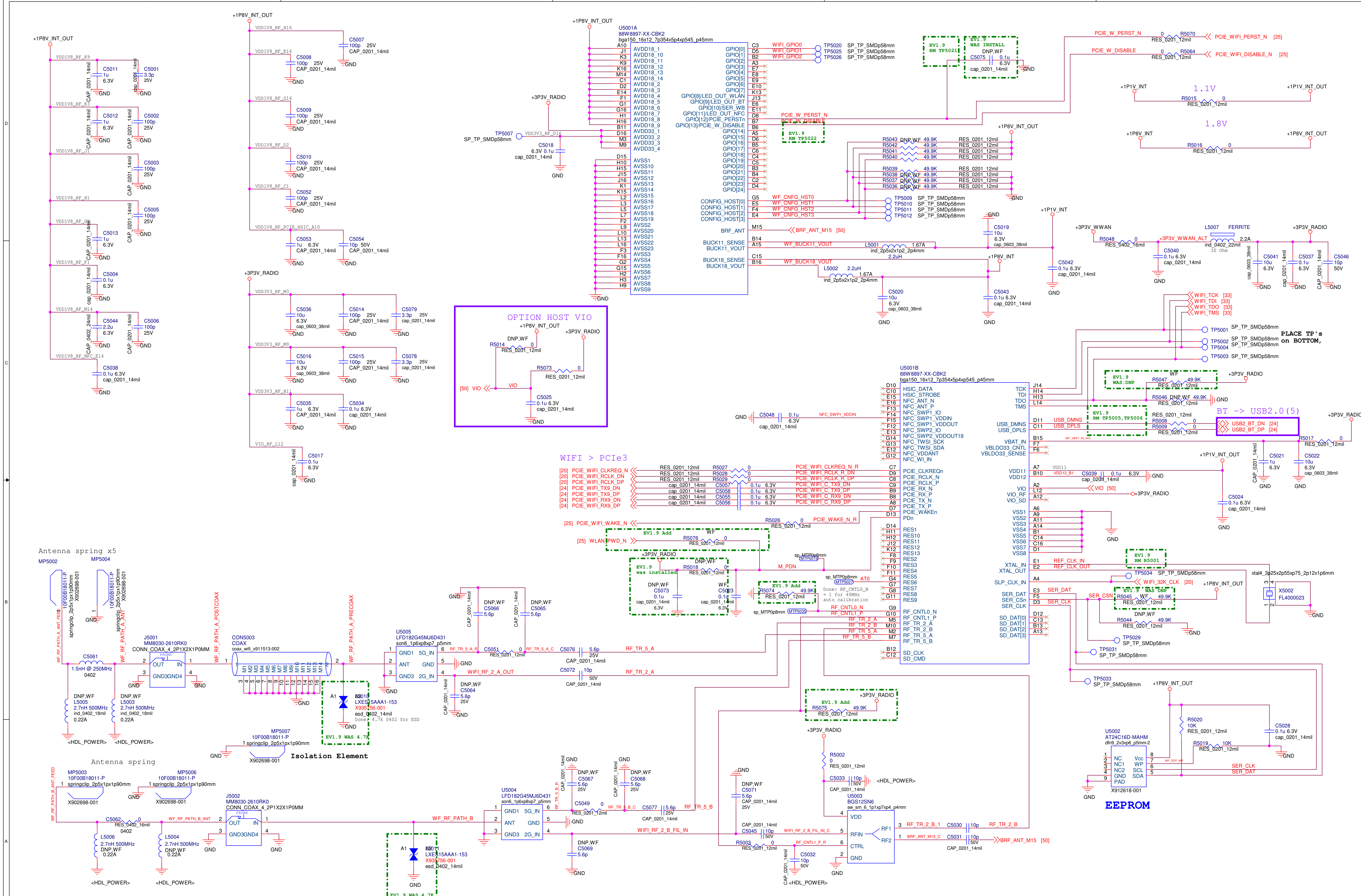
Engineer: Surface

Size	Project Name	Rev
C	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 48 of 76



Title: IR CAMERA			
Microsoft	Engineer: Surface		
Size B	Project Name U -- EV 1.90		Rev 1.90.2
Date: Monday, May 11, 2015		Sheet 49 of 76	



Title: Wi-Fi_BT

Microsoft

Engineer: Surface

Size	Project Name	Rev
A2	U -- EV 1.90	1.90.2

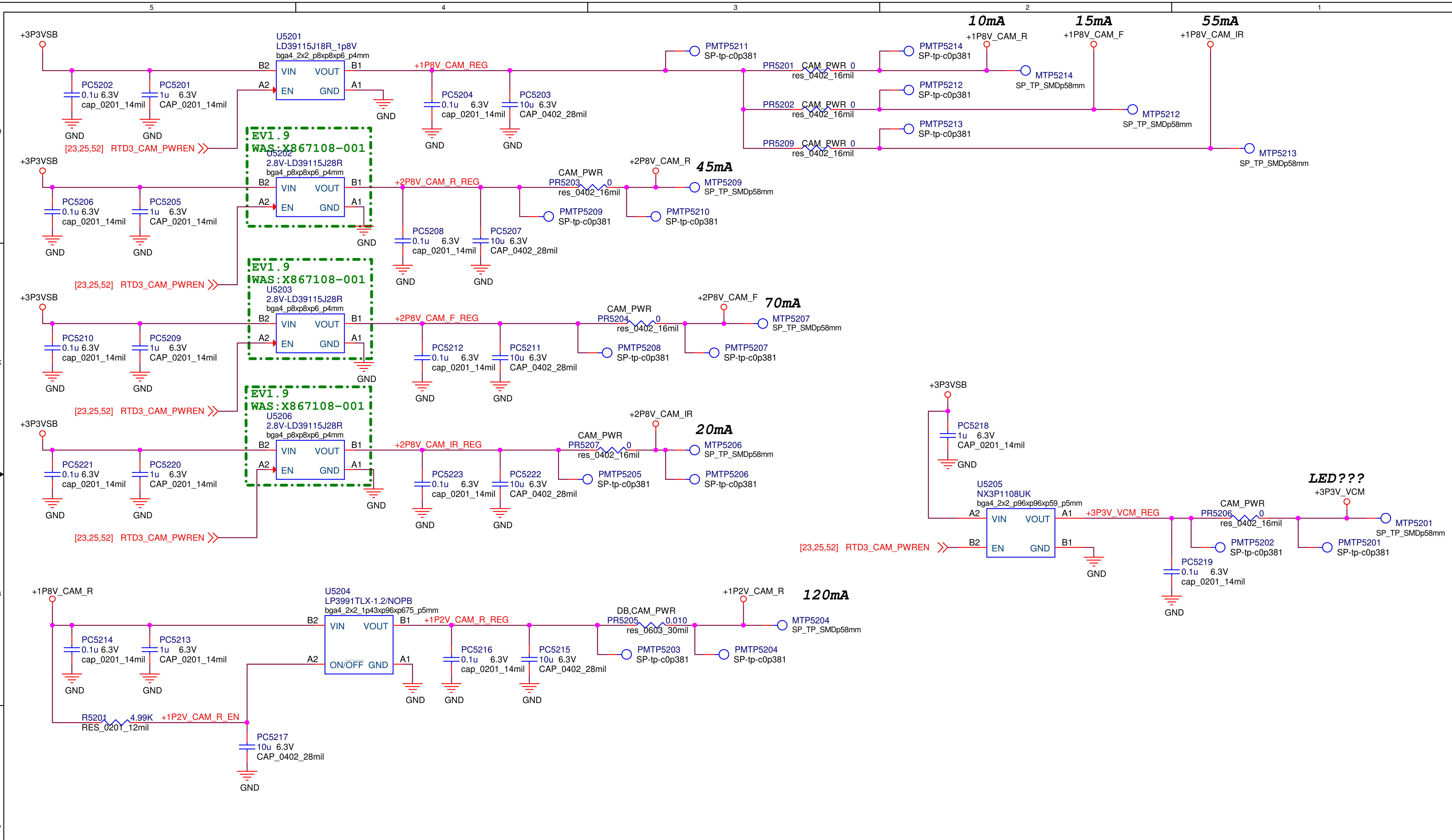
Date: Monday, May 11, 2015 Sheet 50 of 76

5 4 3 2 1

D C B A

EMPTY

	Title: Empty		
Microsoft	Engineer: ***Surface***		
Size B	Project Name **U -- EV 1.90**		Rev 1.90.2
Date: Monday, May 11, 2015		Sheet 51	of 76



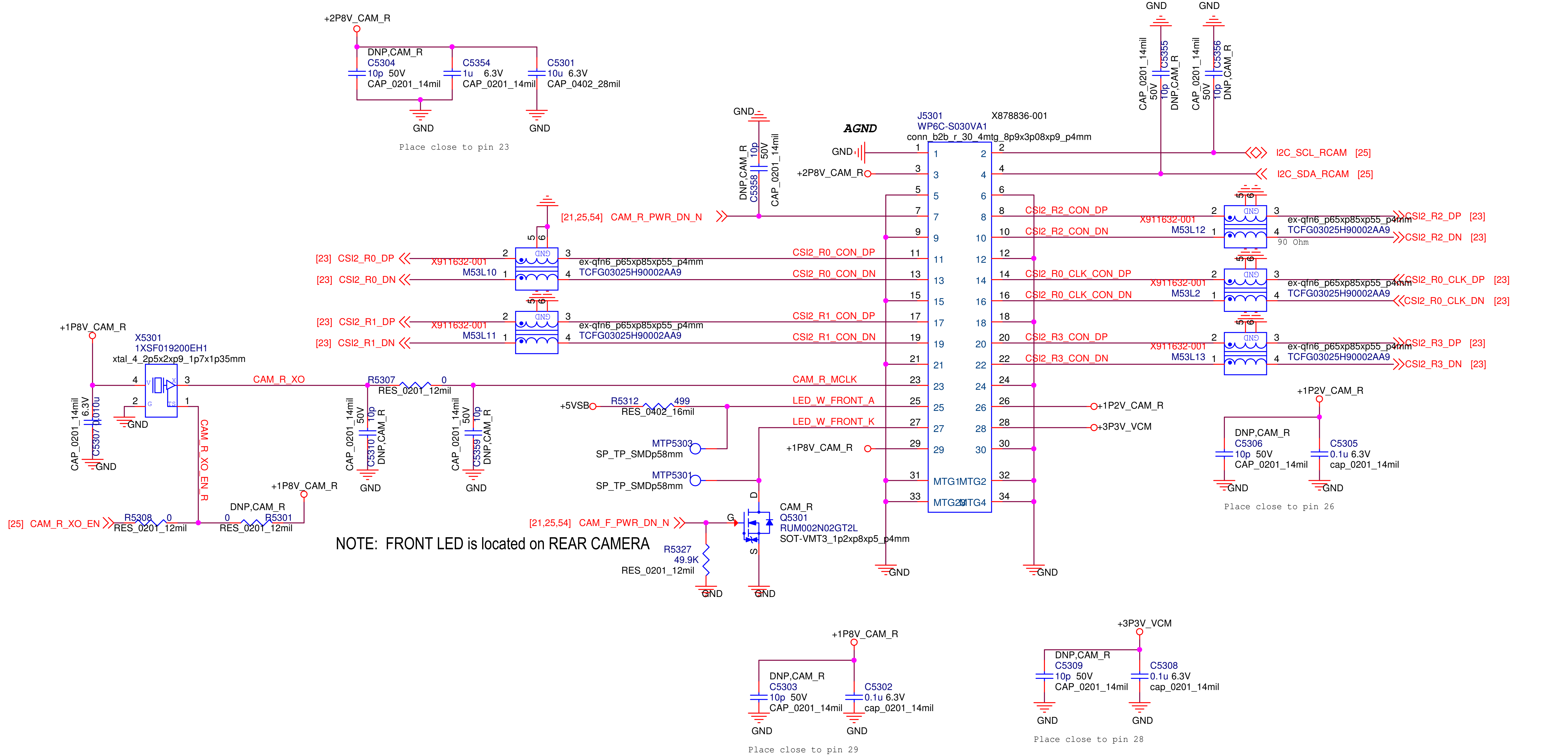
Title: **Camera power**

Microsoft

Engineer: **Surface**

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 52 of 76



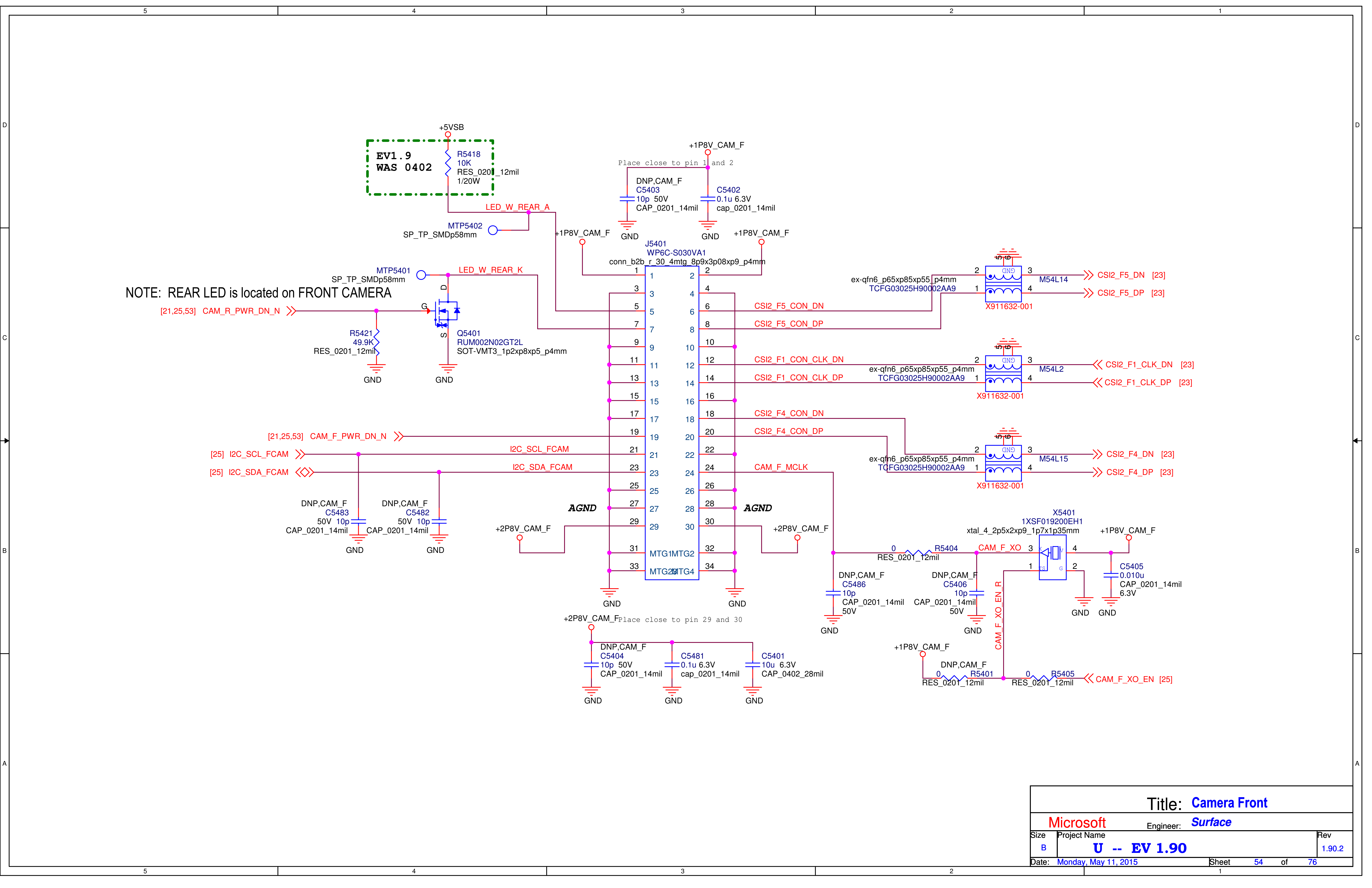
Title: **Camera Rear**

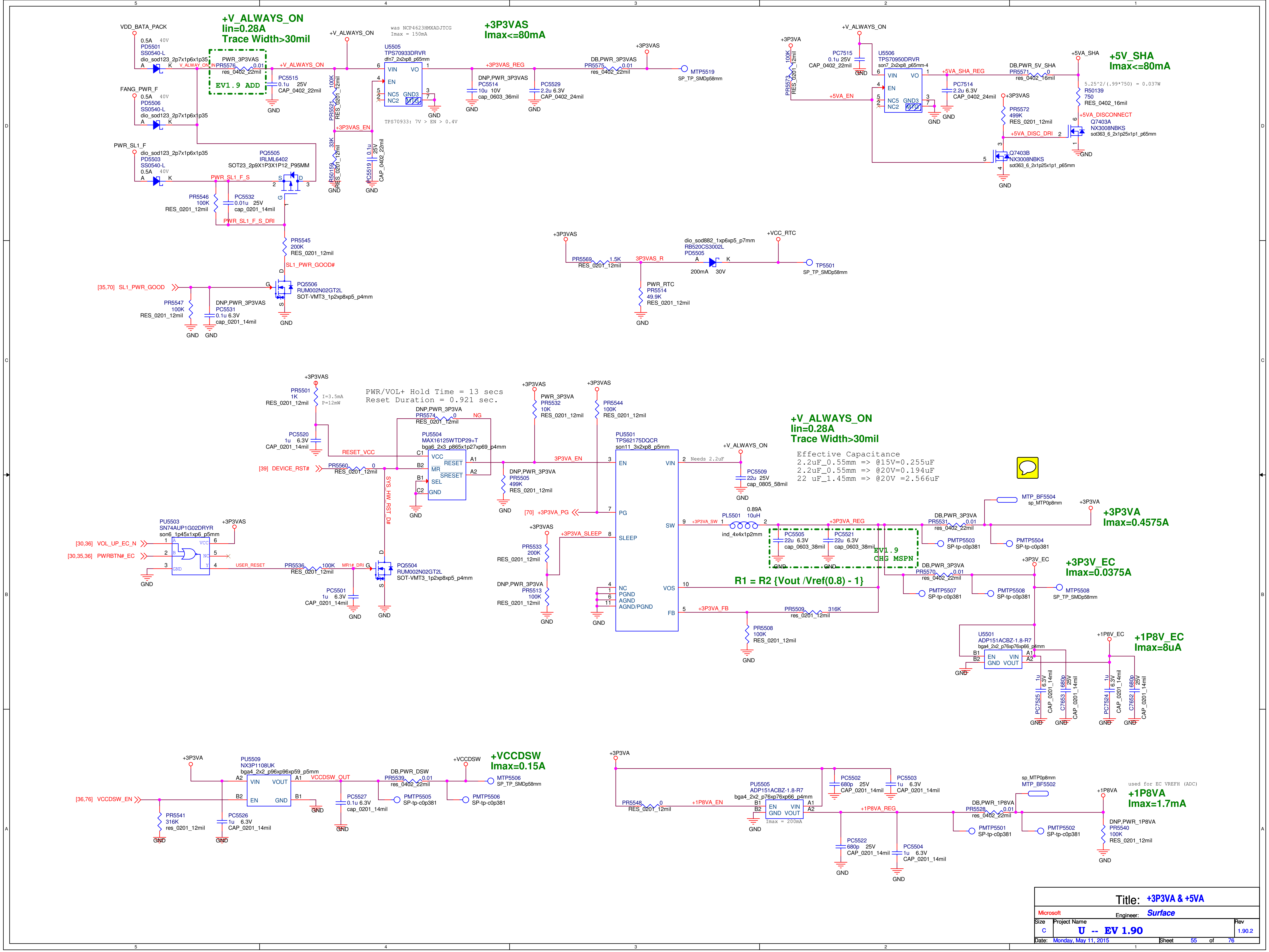
Microsoft

Engineer: **Surface**

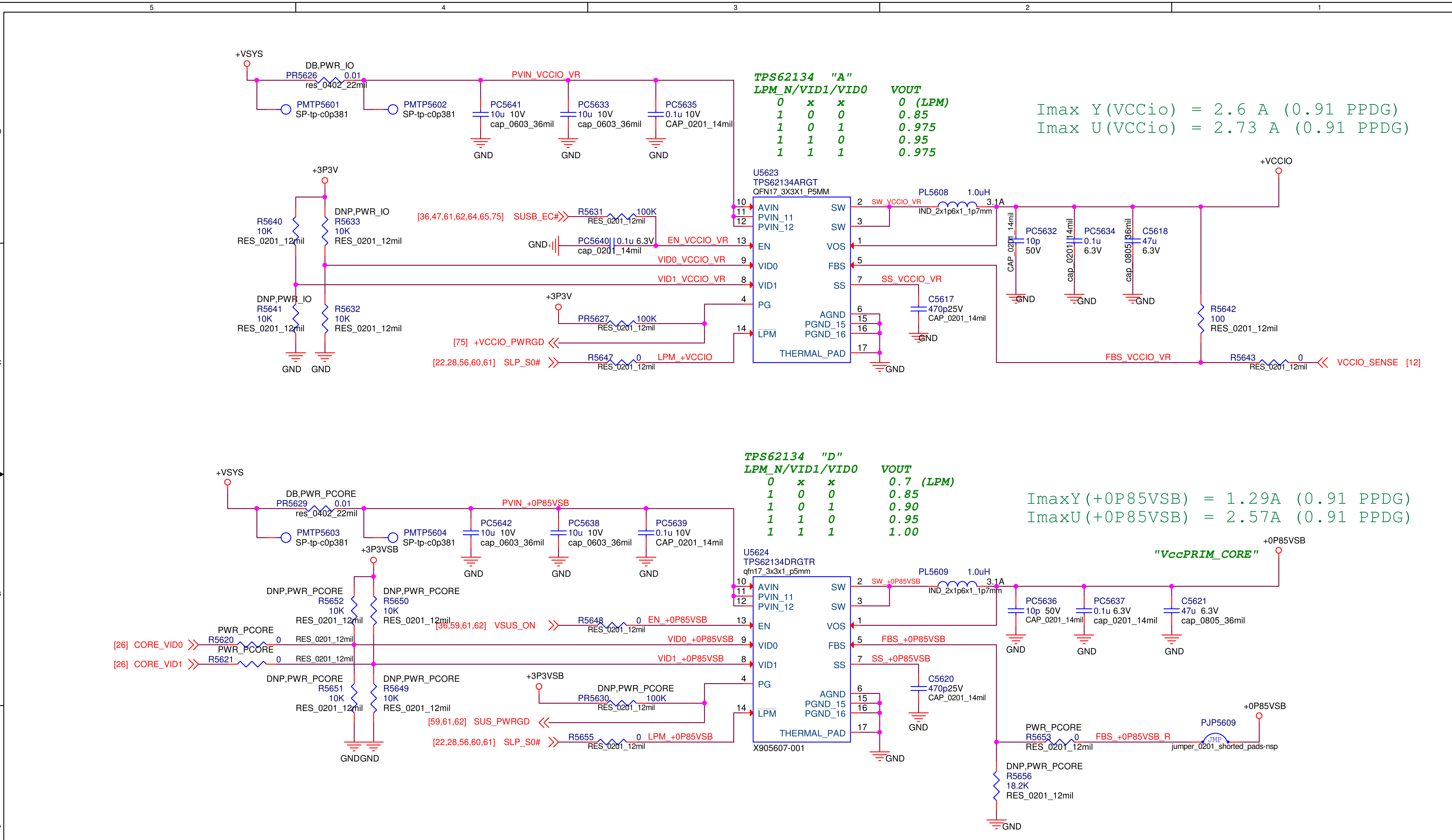
Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 53 of 76


NOTE: REAR LED is located on FRONT CAMERA
EV1.9
WAS 0402
+5VSB
R5418
10K
RES_0201_12mil
1/20W
LED_W_REAR_A
MTP5402
SP_TP_SMDp58mm
MTP5401
SP_TP_SMDp58mm
LED_W_REAR_K
[21,25,53] CAM_R_PWR_DN_N
R5421
49.9K
RES_0201_12mil
Q5401
RUM002N02GT2L
SOT-VMT3_1p2xp8xp5_p4mm
GND
+1P8V_CAM_F
Place close to pin 1 and 2
DNP,CAM_F
C5403
10p 50V
CAP_0201_14mil
C5402
0.1u 6.3V
cap_0201_14mil
J5401
WP6C-S030VA1
conn_b2b_r_30_4mtg_8p9x3p08xp9_p4mm
CSI2_F5_CON_DN
CSI2_F5_CON_DP
CSI2_F1_CON_CLK_DN
CSI2_F1_CON_CLK_DP
CSI2_F4_CON_DN
CSI2_F4_CON_DP
CAM_F_MCLK
[21,25,53] CAM_F_PWR_DN_N
[25] I2C_SCL_FCAM
[25] I2C_SDA_FCAM
I2C_SCL_FCAM
I2C_SDA_FCAM
DNP,CAM_F
C5483
50V 10p
CAP_0201_14mil
DNP,CAM_F
C5482
50V 10p
CAP_0201_14mil
AGND
+2P8V_CAM_F
MTG1 MTG2 MTG3 MTG4
ex-qfn6_p65xp85xp55_p4mm
TCFG03025H90002AA9
M54L14
X911632-001
CSI2_F5_DN [23]
CSI2_F5_DP [23]
M54L2
CSI2_F1_CLK_DN [23]
CSI2_F1_CLK_DP [23]
M54L15
CSI2_F4_DN [23]
CSI2_F4_DP [23]
X5401
1XSF019200EH1
xtal_4_2p5x2p9_1p7x1p35mm
R5404
RES_0201_12mil
CAM_F_XO
DNP,CAM_F
C5486
10p
CAP_0201_14mil
50V
DNP,CAM_F
C5406
10p
CAP_0201_14mil
50V
C5405
0.010u
CAP_0201_14mil
6.3V
CAM_F_XO_EN_R
DNP,CAM_F
R5401
RES_0201_12mil
R5405
RES_0201_12mil
CAM_F_XO_EN [25]
Place close to pin 29 and 30
DNP,CAM_F
C5404
10p 50V
CAP_0201_14mil
C5481
0.1u 6.3V
cap_0201_14mil
C5401
10u 6.3V
CAP_0402_28mil
Title: Camera Front
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 54 of 76



+V_ALWAYS_ON
Iin=0.28A
Trace Width>30mil
+3P3VAS
Imax<=80mA
+5V_SHA
Imax<=80mA
EV1.9 ADD
PWR/VOL+ Hold Time = 13 secs
Reset Duration = 0.921 sec.
+V_ALWAYS_ON
Iin=0.28A
Trace Width>30mil
Effective Capacitance
2.2uF_0.55mm => @15V=0.255uF
2.2uF_0.55mm => @20V=0.194uF
22 uF_1.45mm => @20V =2.566uF
+3P3VA
Imax=0.4575A
+3P3V_EC
Imax=0.0375A
EV1.9
CHG MSPN
R1 = R2 {Vout /Vref(0.8) - 1}
+1P8V_EC
Imax=8uA
+VCCDSW
Imax=0.15A
+1P8VA
Imax=1.7mA
used for EC VREFH (ADC)
Title: +3P3VA & +5VA
Microsoft
Engineer: Surface
Project Name
U -- EV 1.90
Size C
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 55 of 76



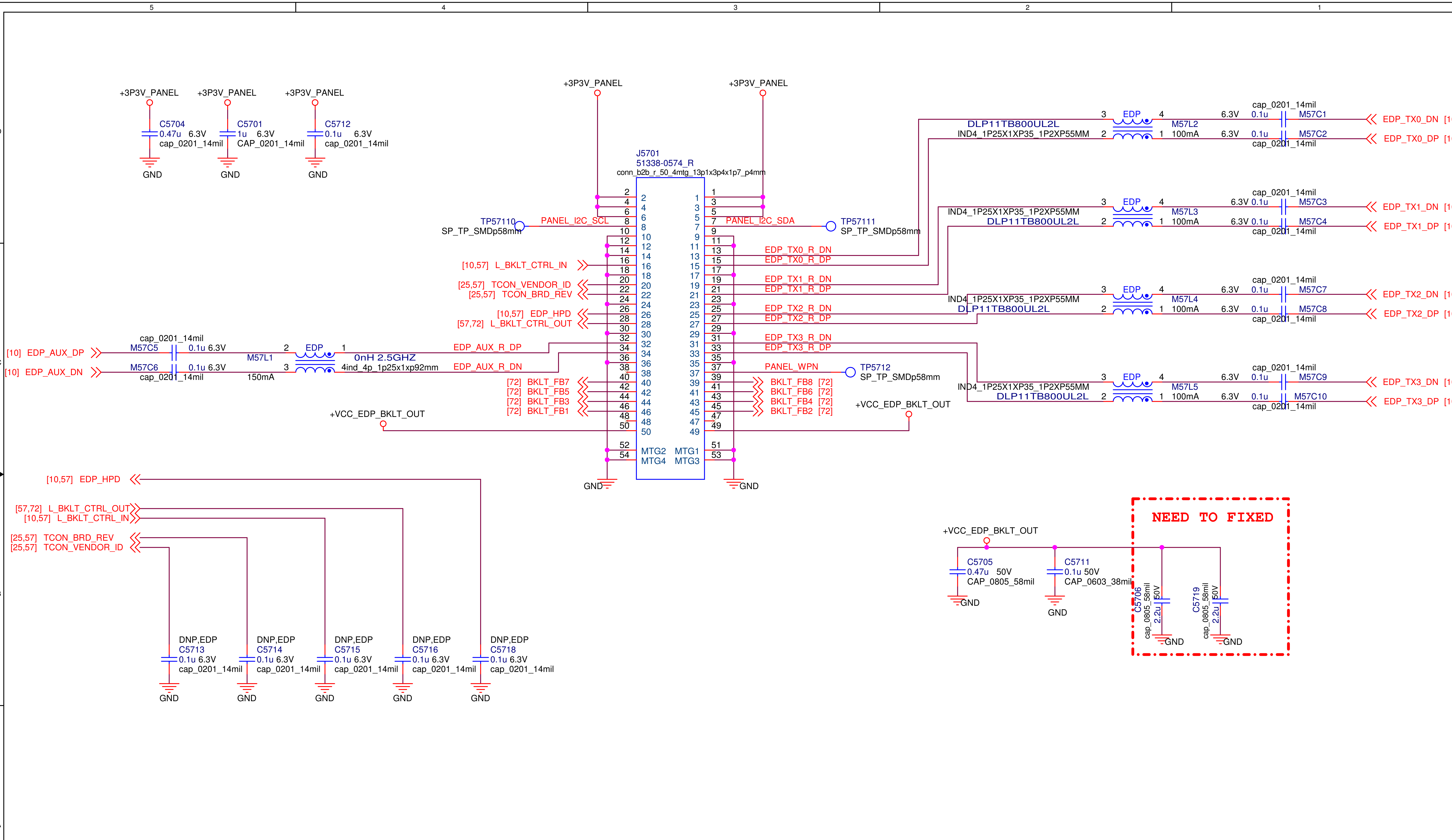
Title: +VCCIO & 0P85VSB

Microsoft

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 56 of 76



Title: eDP connector

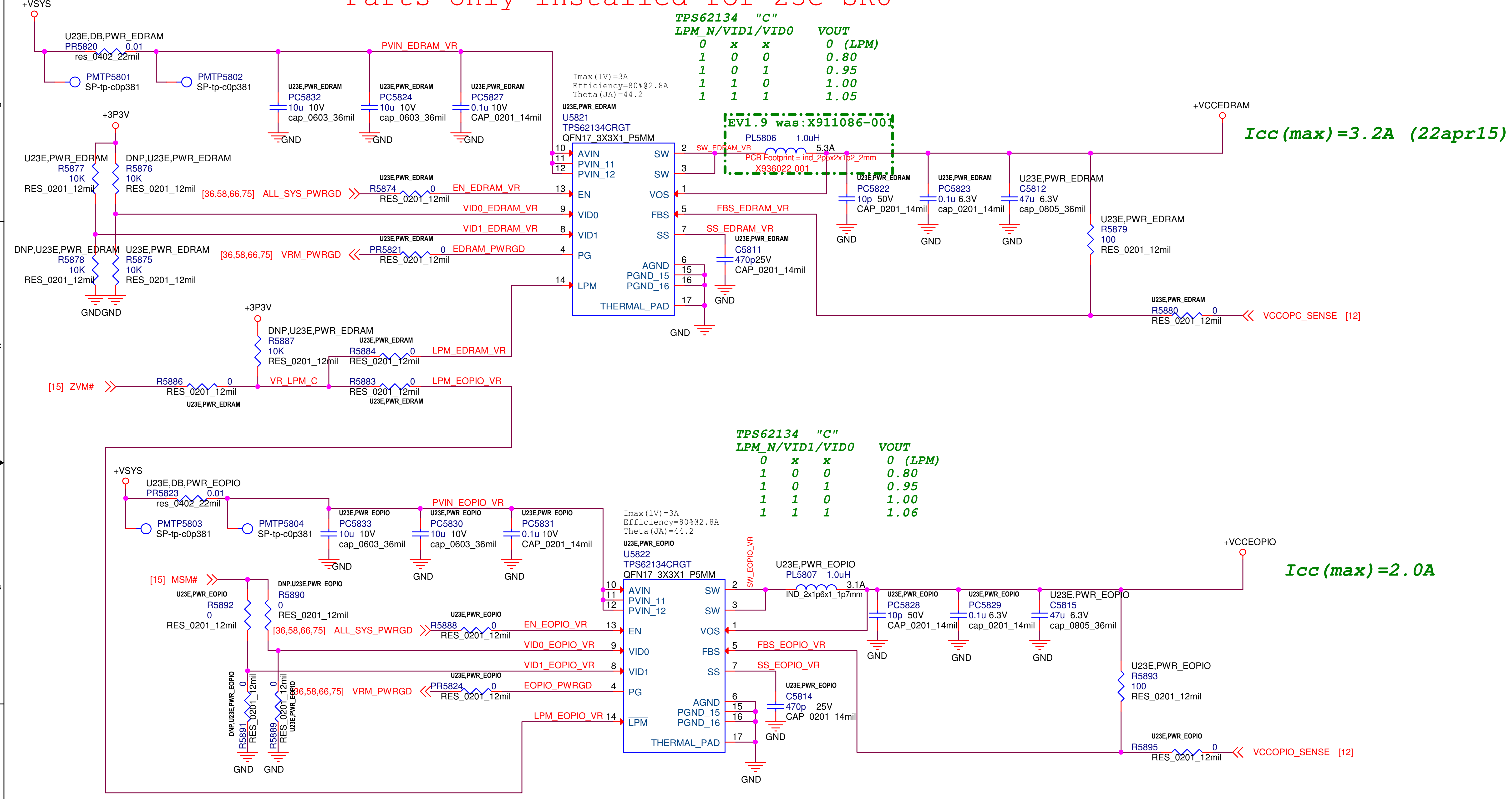
Microsoft

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015

Parts only installed for 23e SKU



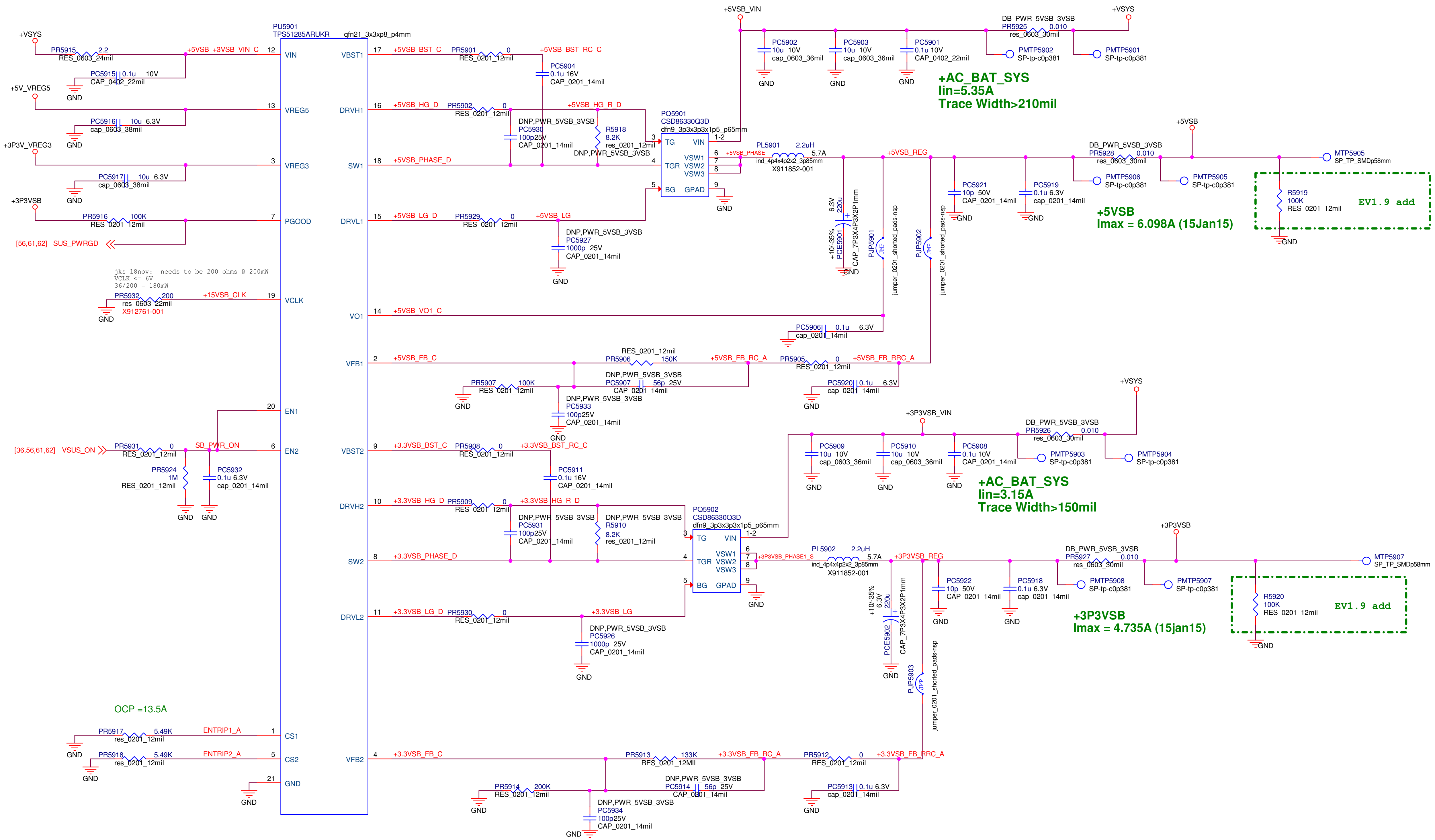
Title: +VCCEDRAM & +VCCEOPIO

Microsoft

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 58 of 76



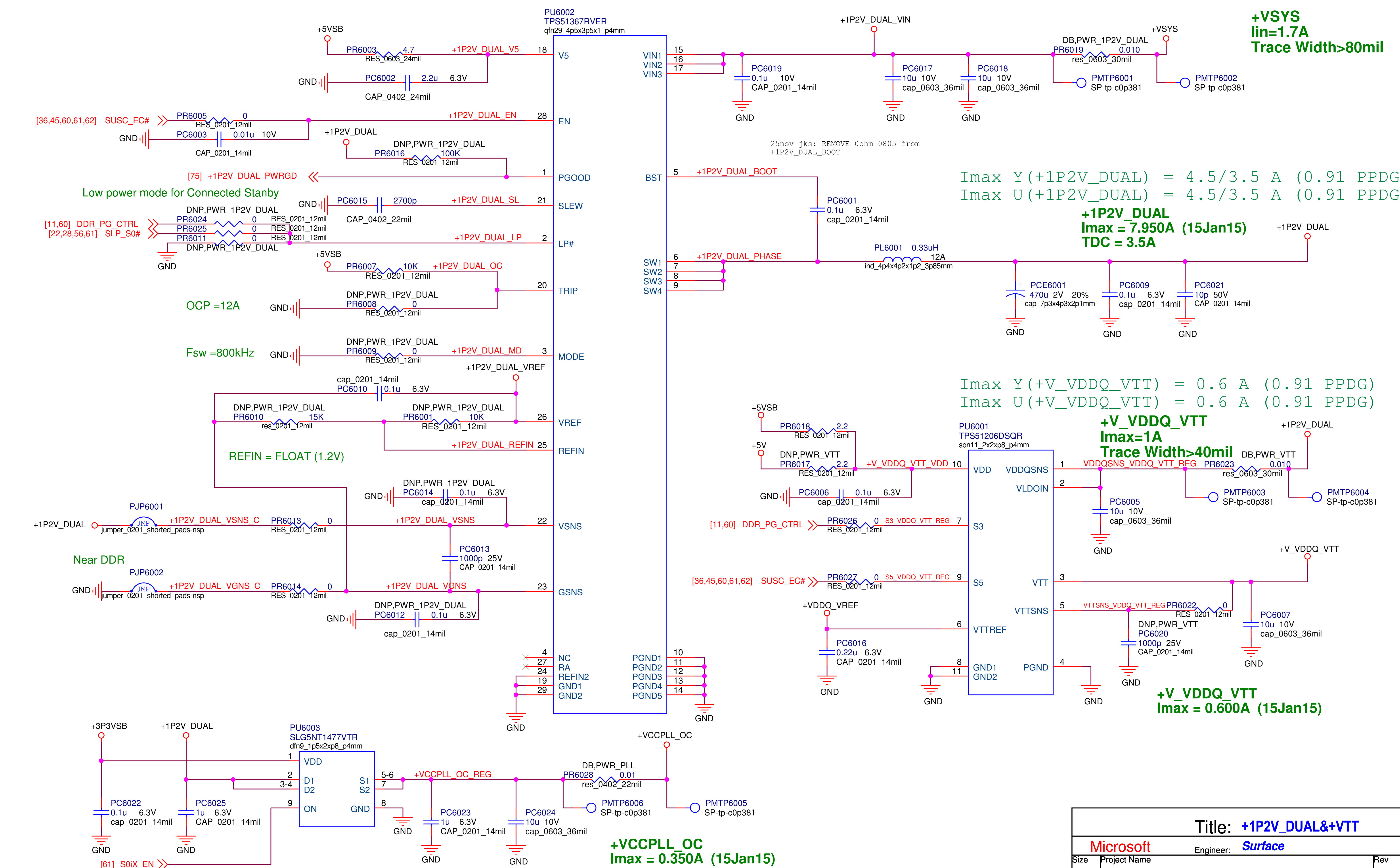
Title: +5VSB & +3P3VSB

Microsoft

Engineer: Surface

Size	Project Name	Rev
C	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 59 of 76

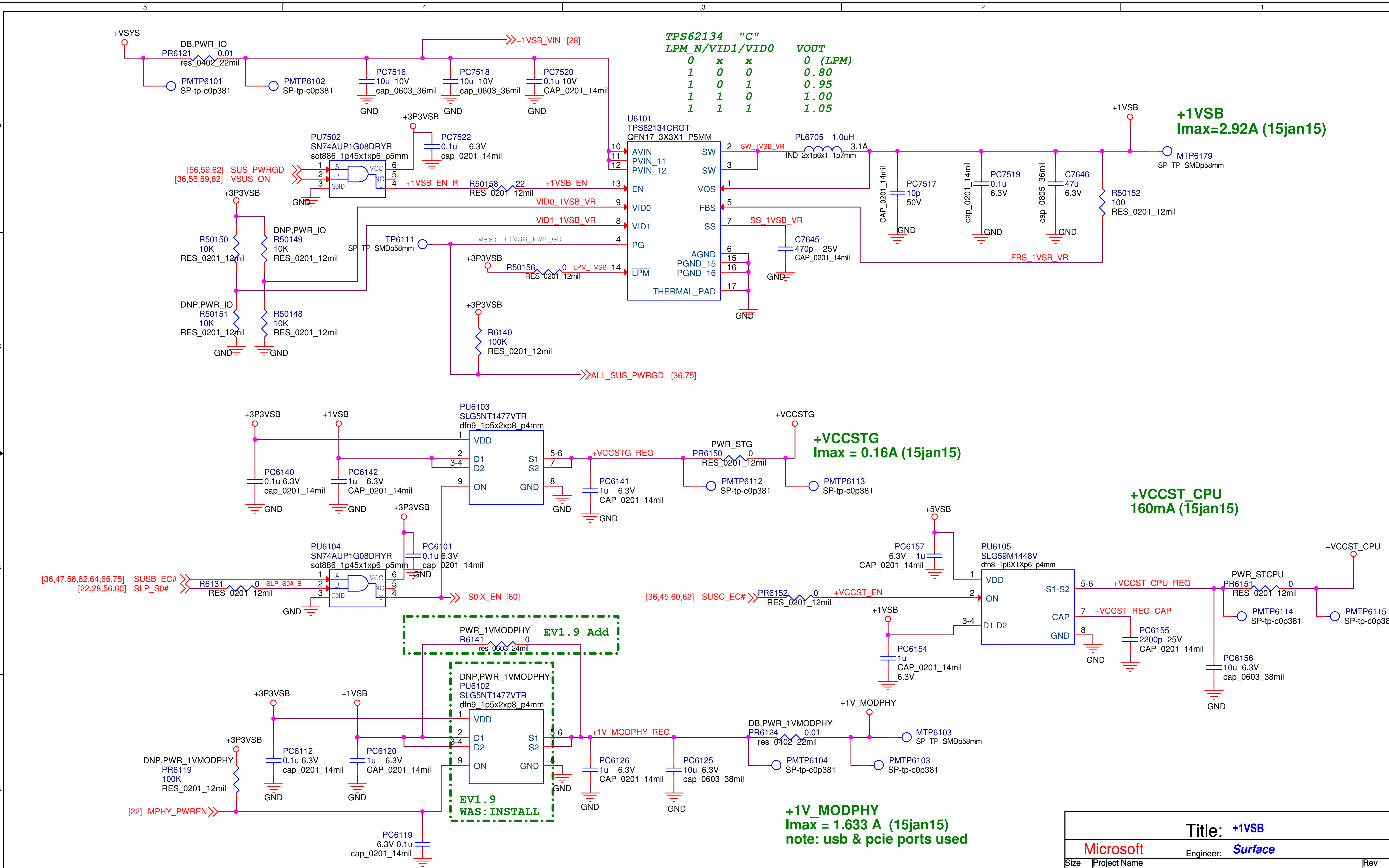


Title: +1P2V_DUAL&+VTT

Microsoft Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 60 of 76



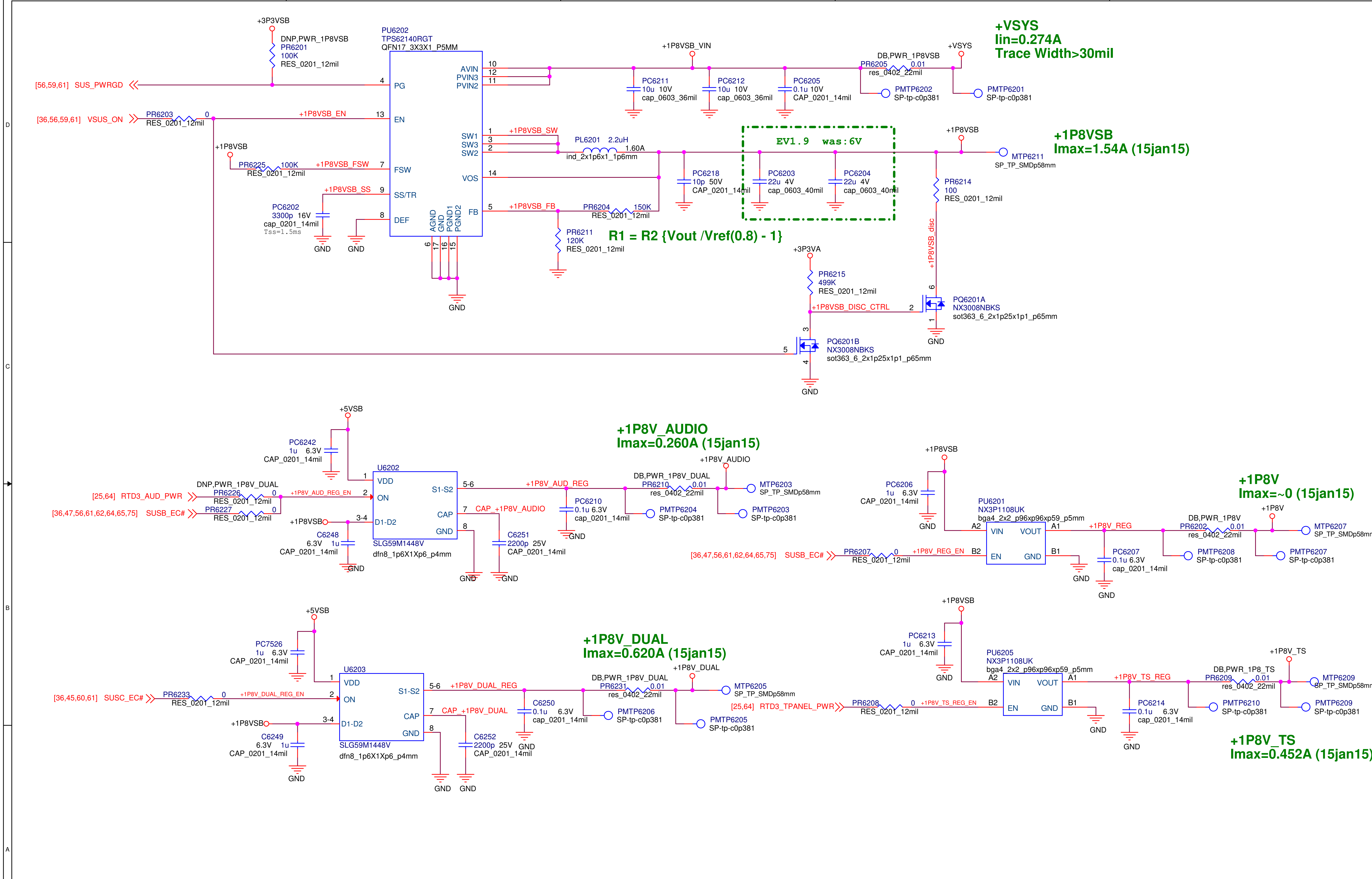
Title: +1VSB

Microsoft

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 61 of 76



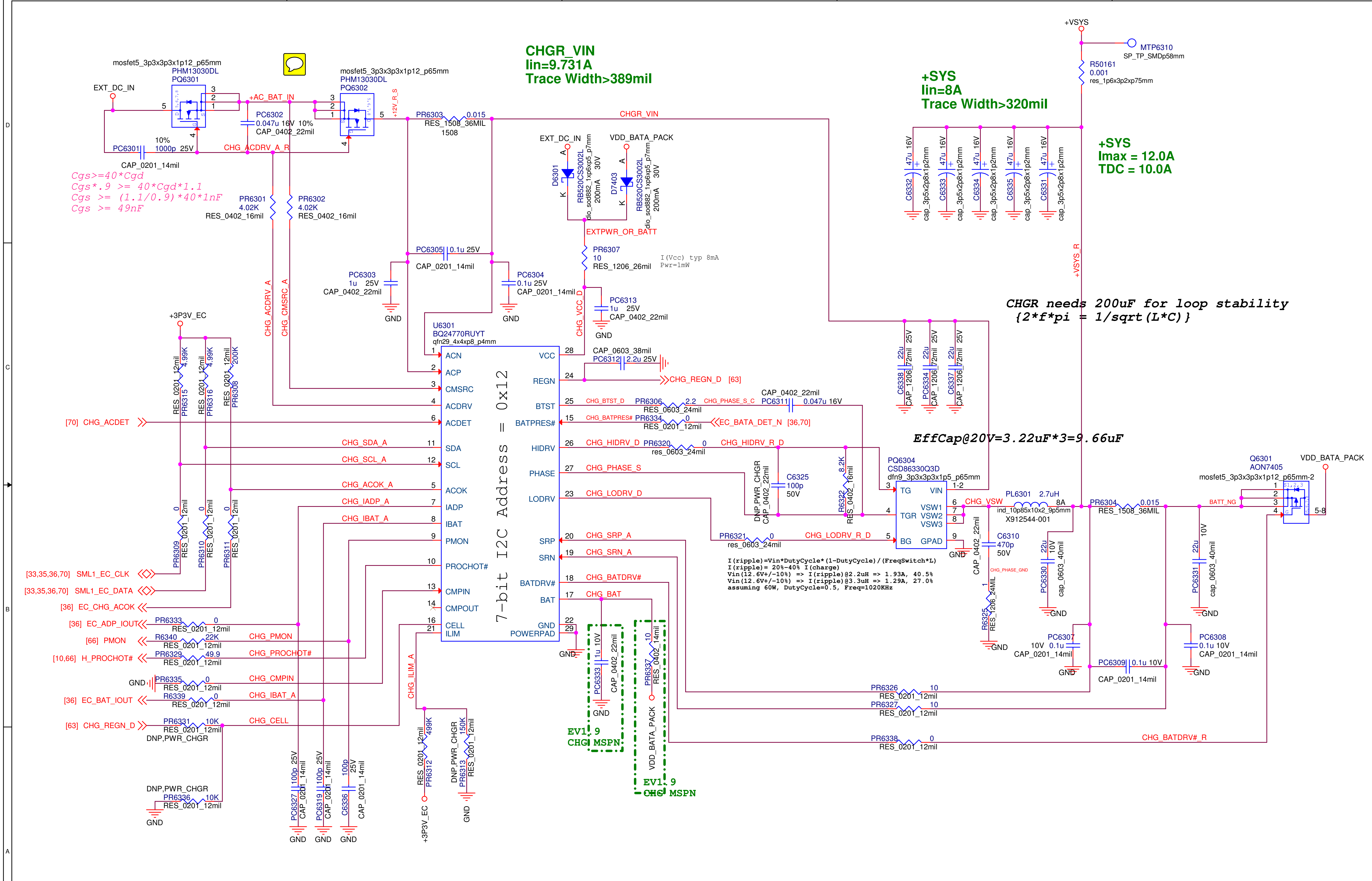
Title: +1.8VSB & Load SW

Microsoft

Engineer: Surface

Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 62 of 76



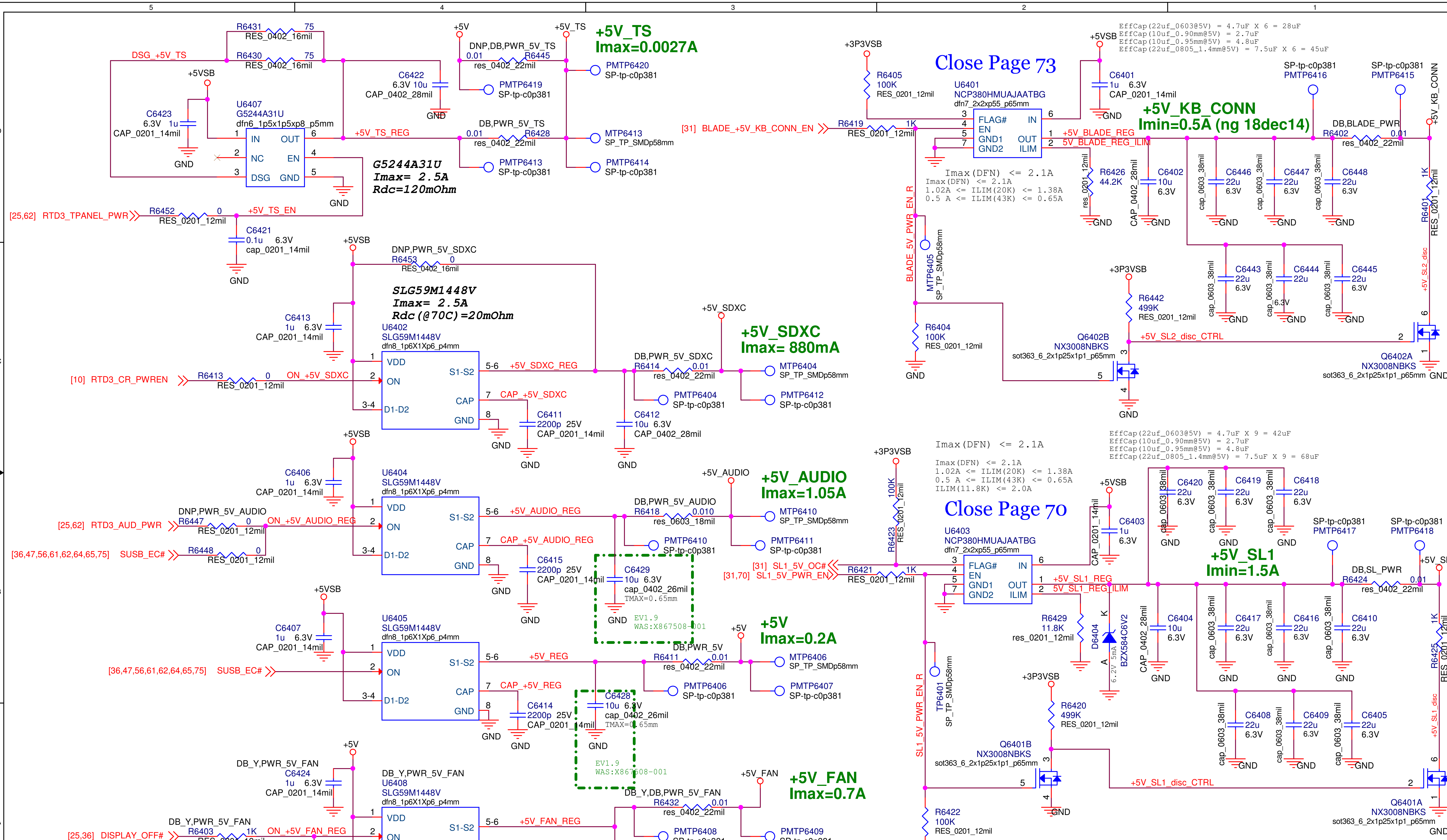
Title: CHARGER NVDC

Microsoft

Engineer: Surface

Size	Project Name	Rev
A3	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 63 of 76

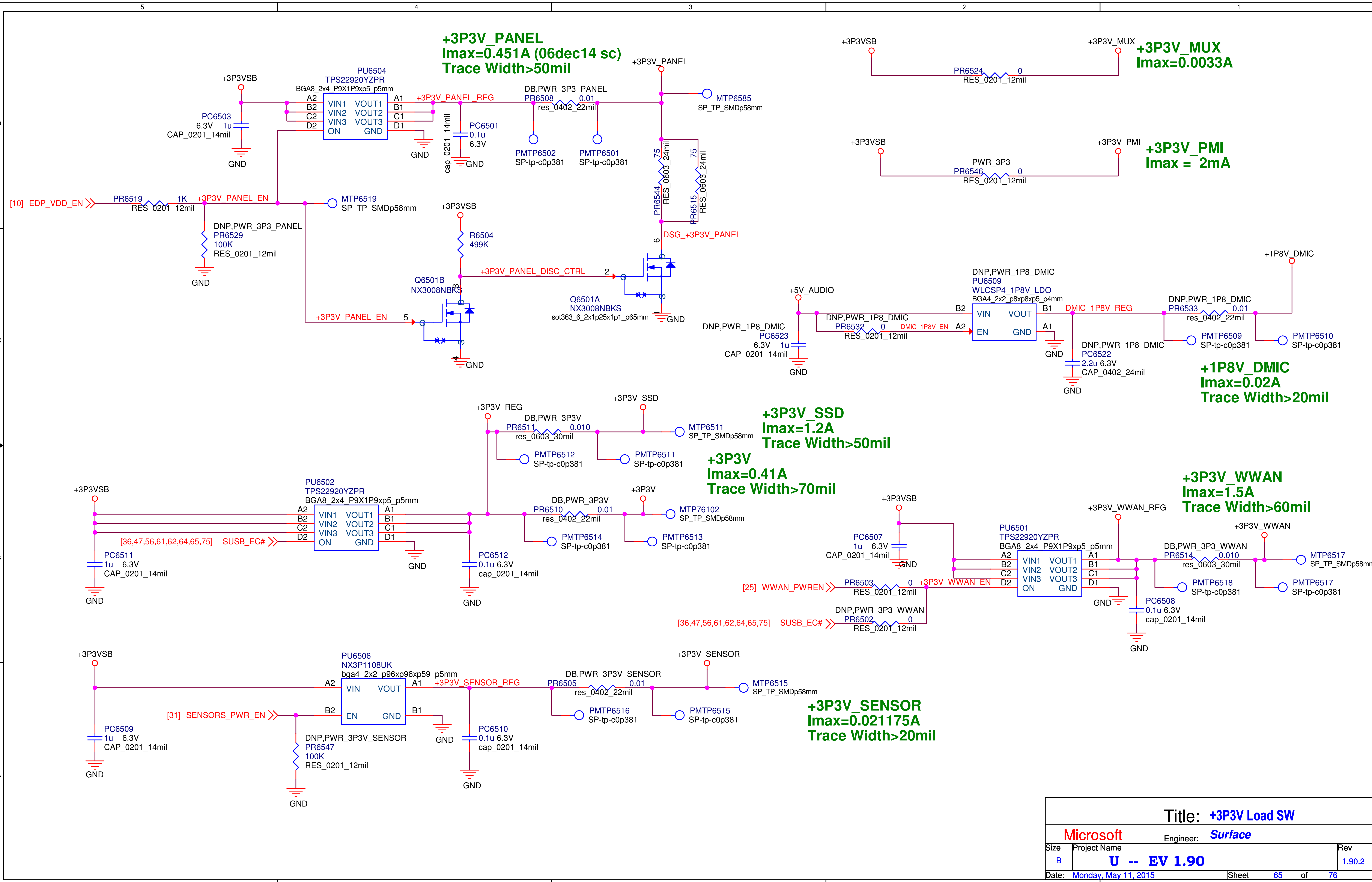


Title: +5V Load SW

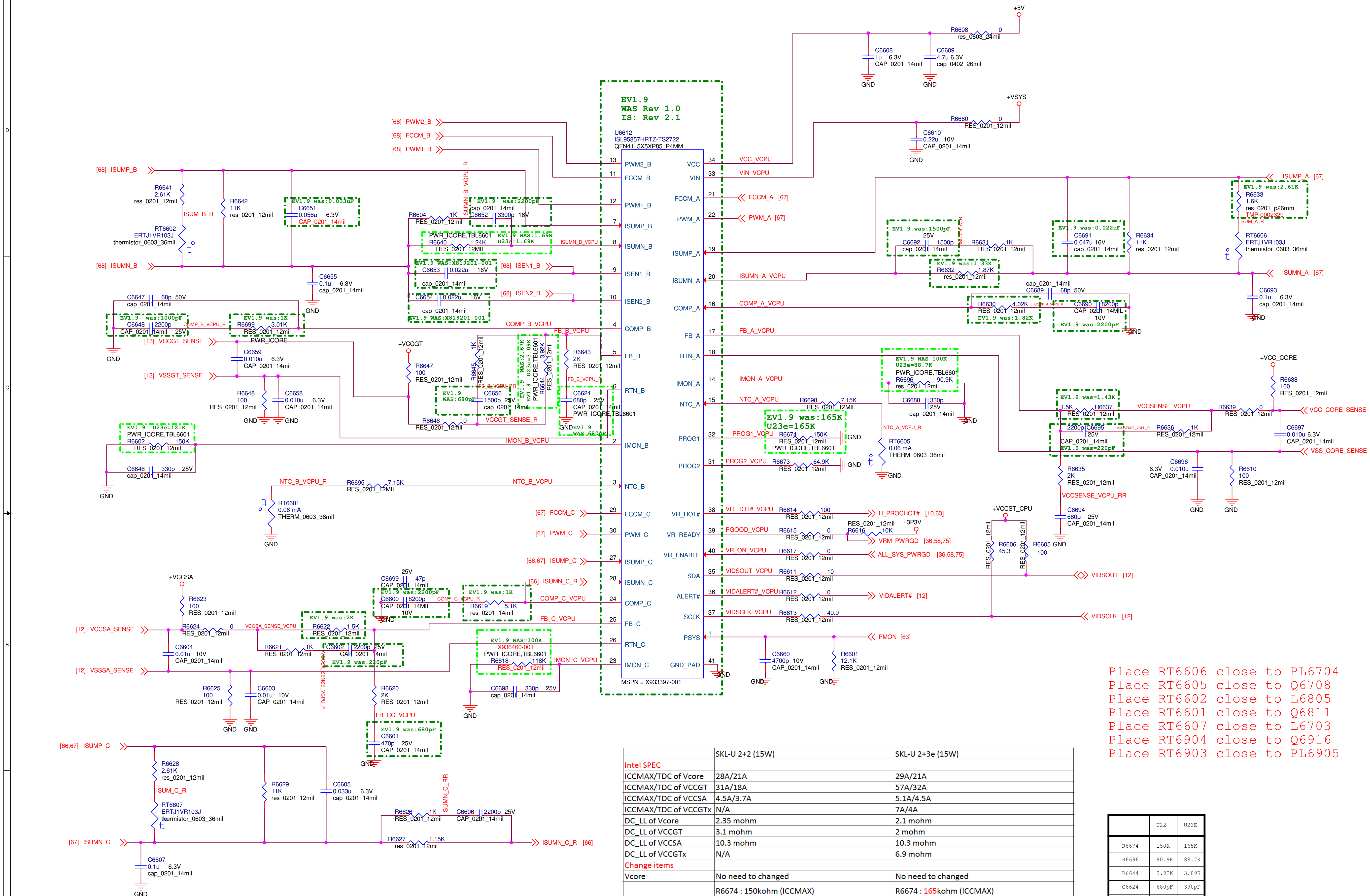
Microsoft Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 64 of 76



+3P3V_PANEL
Imax=0.451A (06dec14 sc)
Trace Width>50mil
+3P3VSB
PU6504
TPS22920YZPR
BGA8_2x4_P9X1P9xp5_p5mm
VIN1 VIN2 VIN3 ON VOUT1 VOUT2 VOUT3 GND
A2 B2 C2 D2 A1 B1 C1 D1
+3P3V_PANEL_REG
DB,PWR_3P3_PANEL
PR6508 0.01
res_0402_22mil
PC6501 0.1u 6.3V
cap_0201_14mil
PC6503 6.3V 1u
CAP_0201_14mil
GND
PMTP6502 SP-tp-c0p381
PMTP6501 SP-tp-c0p381
+3P3V_PANEL
MTP6585 SP_TP_SMDp58mm
PR6544 75 RES_0603_24mil
PR6515 75 RES_0603_24mil
DSG_+3P3V_PANEL
[10] EDP_VDD_EN
PR6519 1K RES_0201_12mil
+3P3V_PANEL_EN
MTP6519 SP_TP_SMDp58mm
DNP,PWR_3P3_PANEL
PR6529 100K RES_0201_12mil
R6504 499K
+3P3V_PANEL_DISC_CTRL
Q6501B NX3008NBKS
Q6501A NX3008NBKS
sot363_6_2x1p25x1p1_p65mm
+3P3VSB
PR6524 0
RES_0201_12mil
+3P3V_MUX
+3P3V_MUX
Imax=0.0033A
+3P3V_PMI
PWR_3P3
PR6546 0
RES_0201_12mil
+3P3V_PMI
Imax = 2mA
+1P8V_DMIC
DNP,PWR_1P8_DMIC
PU6509
WLCSP4_1P8V_LDO
BGA4_2x2_p8xp8xp5_p4mm
VIN VOUT EN GND
B2 B1 A2 A1
+5V_AUDIO
DMIC_1P8V_REG
PR6533 0.01 res_0402_22mil
PR6532 0 RES_0201_12mil
DMIC_1P8V_EN
PC6523 6.3V 1u CAP_0201_14mil
PC6522 2.2u 6.3V CAP_0402_24mil
PMTP6509 SP-tp-c0p381
PMTP6510 SP-tp-c0p381
+1P8V_DMIC
Imax=0.02A
Trace Width>20mil
+3P3V_REG
+3P3V_SSD
DB,PWR_3P3V
PR6511 0.010 res_0603_30mil
MTP6511 SP_TP_SMDp58mm
PMTP6512 SP-tp-c0p381
PMTP6511 SP-tp-c0p381
+3P3V_SSD
Imax=1.2A
Trace Width>50mil
+3P3V
Imax=0.41A
Trace Width>70mil
PU6502
TPS22920YZPR
BGA8_2x4_P9X1P9xp5_p5mm
[36,47,56,61,62,64,65,75] SUSB_EC#
PC6511 1u 6.3V CAP_0201_14mil
PC6512 0.1u 6.3V cap_0201_14mil
DB,PWR_3P3V
PR6510 0.01 res_0402_22mil
+3P3V
MTP76102 SP_TP_SMDp58mm
PMTP6514 SP-tp-c0p381
PMTP6513 SP-tp-c0p381
+3P3V_WWAN
Imax=1.5A
Trace Width>60mil
+3P3V_WWAN_REG
PU6501
TPS22920YZPR
BGA8_2x4_P9X1P9xp5_p5mm
PC6507 1u 6.3V CAP_0201_14mil
[25] WWAN_PWREN
PR6503 0 RES_0201_12mil
+3P3V_WWAN_EN
DNP,PWR_3P3_WWAN
PR6502 0 RES_0201_12mil
DB,PWR_3P3_WWAN
PR6514 0.010 res_0603_30mil
+3P3V_WWAN
MTP6517 SP_TP_SMDp58mm
PMTP6518 SP-tp-c0p381
PMTP6517 SP-tp-c0p381
PC6508 0.1u 6.3V cap_0201_14mil
PU6506
NX3P1108UK
bga4_2x2_p96xp96xp59_p5mm
VIN VOUT EN GND
+3P3V_SENSOR_REG
[31] SENSORS_PWR_EN
PC6509 1u 6.3V CAP_0201_14mil
DNP,PWR_3P3V_SENSOR
PR6547 100K RES_0201_12mil
PC6510 0.1u 6.3V cap_0201_14mil
DB,PWR_3P3V_SENSOR
PR6505 0.01 res_0402_22mil
+3P3V_SENSOR
MTP6515 SP_TP_SMDp58mm
PMTP6516 SP-tp-c0p381
PMTP6515 SP-tp-c0p381
+3P3V_SENSOR
Imax=0.021175A
Trace Width>20mil
Title: +3P3V Load SW
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 65 of 76



Place RT6606 close to PL6704
Place RT6605 close to Q6708
Place RT6602 close to L6805
Place RT6601 close to Q6811
Place RT6607 close to L6703
Place RT6904 close to Q6916
Place RT6903 close to PL6905

	SKL-U 2+2 (15W)	SKL-U 2+3e (15W)
Intel SPEC		
ICCMAX/TDC of Vcore	28A/21A	29A/21A
ICCMAX/TDC of VCCGT	31A/18A	57A/32A
ICCMAX/TDC of VCCSA	4.5A/3.7A	5.1A/4.5A
ICCMAX/TDC of VCCGTx	N/A	7A/4A
DC_LL of Vcore	2.35 mohm	2.1 mohm
DC_LL of VCCGT	3.1 mohm	2 mohm
DC_LL of VCCSA	10.3 mohm	10.3 mohm
DC_LL of VCCGTx	N/A	6.9 mohm
Change items		
Vcore	No need to changed	No need to changed
VCCGT	R6674 : 150kohm (ICCMAX) R6640 : 1.24kohm (60A OCP) R6644 : 3.09kohm (LL 3.1mohm)	R6674 : 165kohm (ICCMAX) R6640 : 1.69kohm (80A OCP) R6644 : 2.68kohm(LL 2mohm)
VCCSA	No need to changed	No need to changed
VCCGTx	Disable U6916	Enable U6916

	U22	U23E
R6674	150K	165K
R6696	90.9K	88.7K
R6644	3.92K	3.09K
C6624	680pF	390pF
R6640	1.24K	1.69K
R6602	150K	121K
R6618	118K	100K

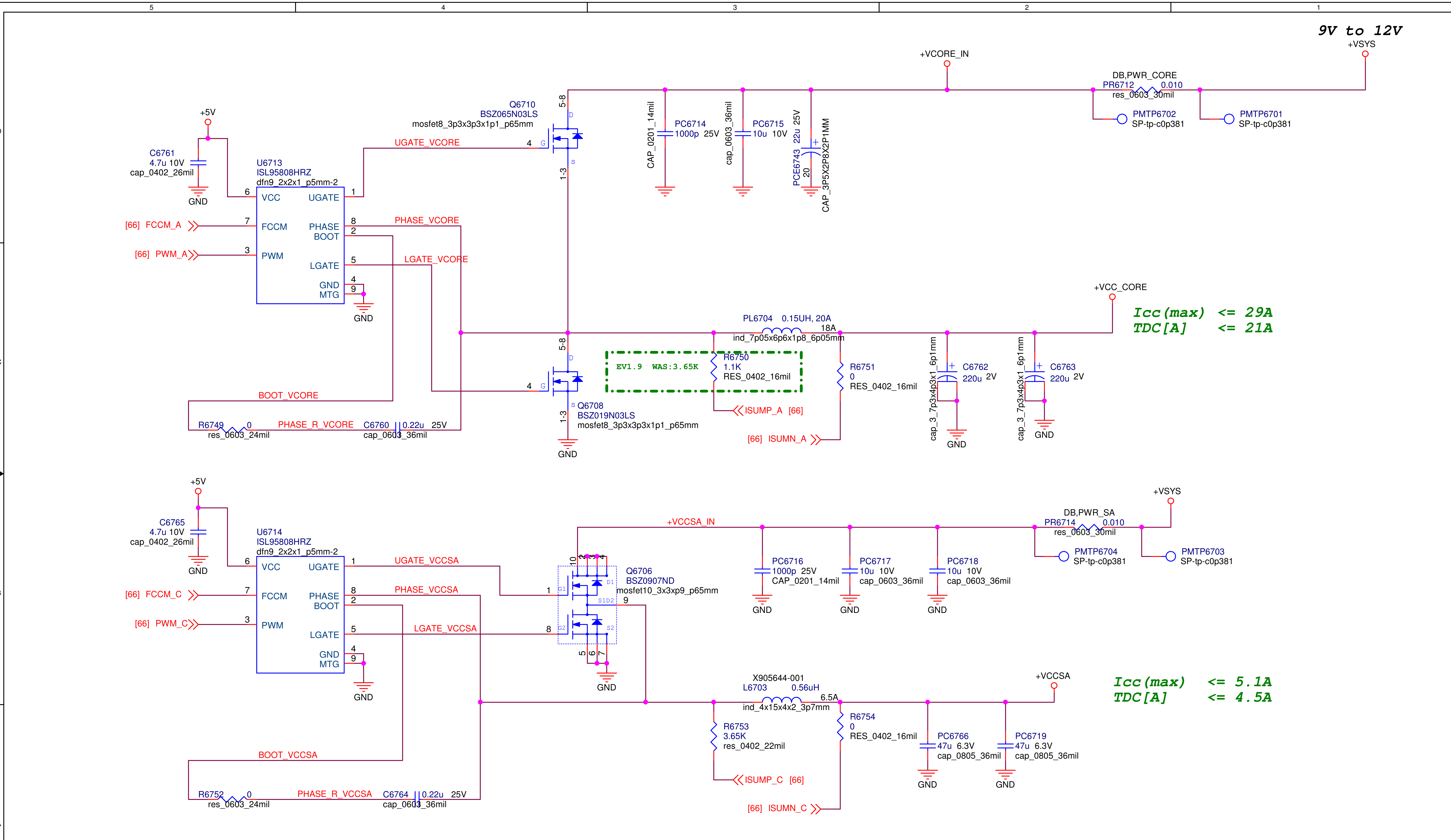
Title: VCPU contoller

Microsoft

Engineer: Surface

Size	Project Name	Rev
C	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 66 of 76



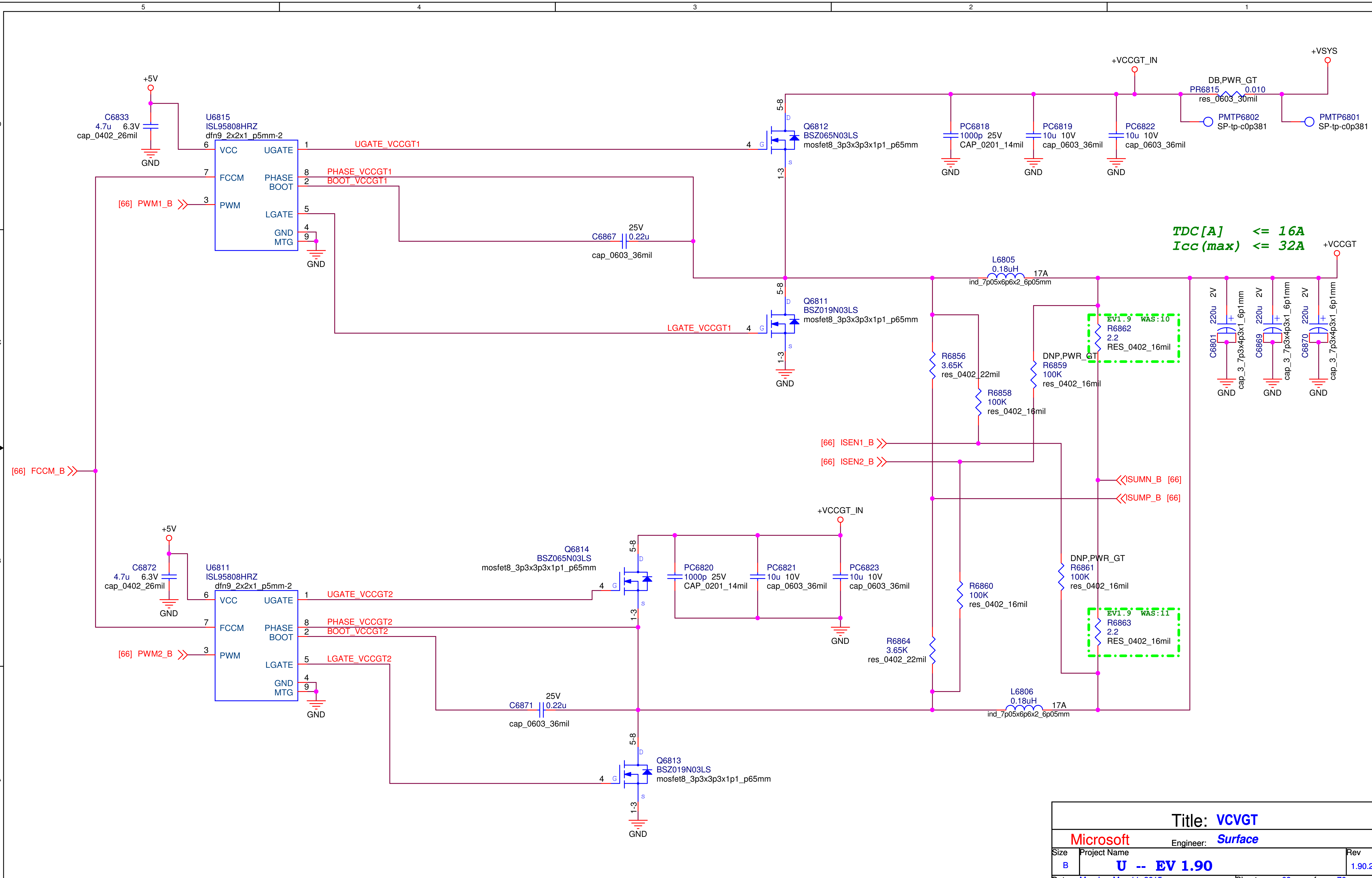
Title: VCORE VCCSA

Microsoft

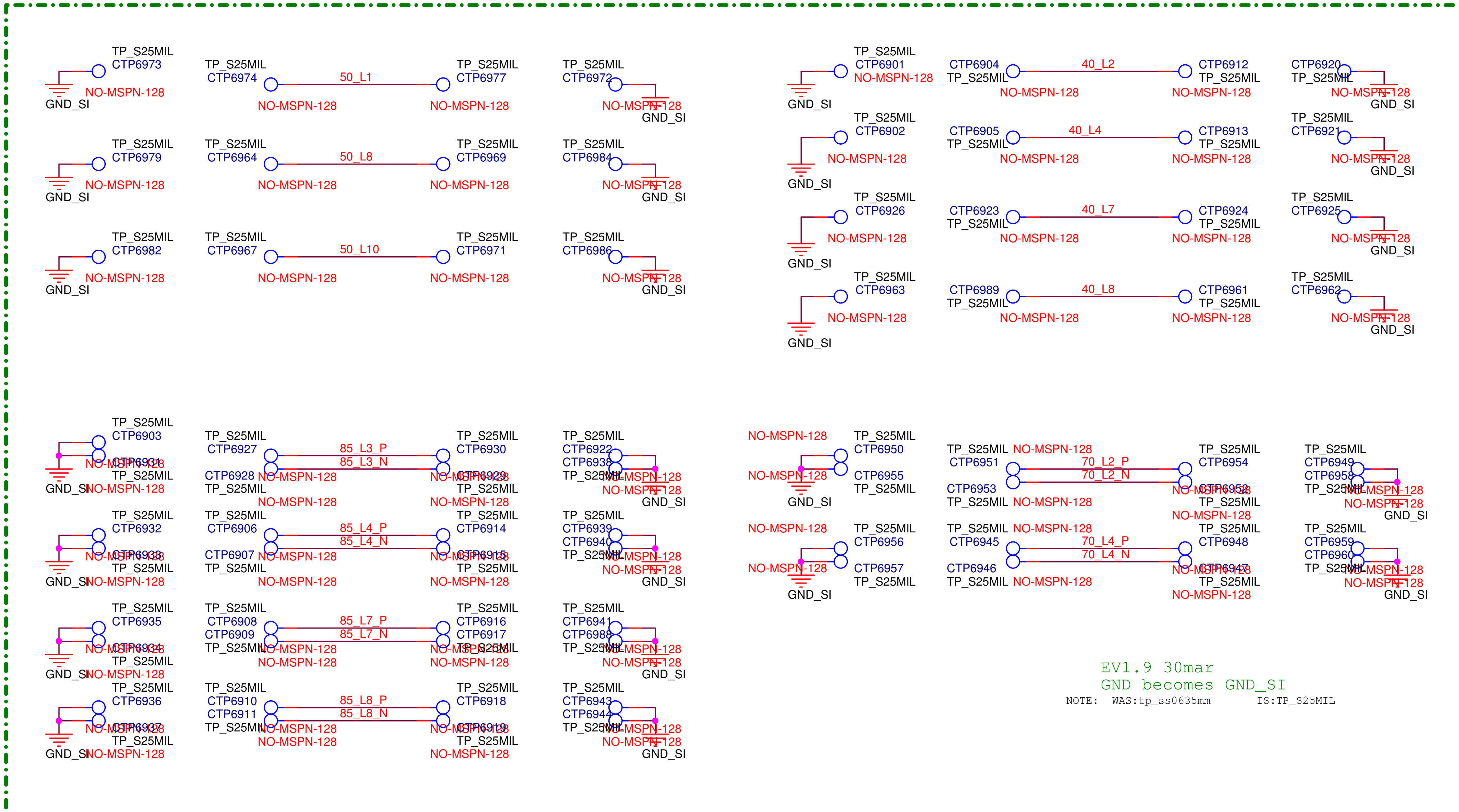
Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 67 of 76



+5V
C6833
4.7u 6.3V
cap_0402_26mil
GND
U6815
ISL95808HRZ
dfn9_2x2x1_p5mm-2
VCC
UGATE
FCCM
PHASE
BOOT
PWM
LGATE
GND
MTG
UGATE_VCCGT1
PHASE_VCCGT1
BOOT_VCCGT1
[66] PWM1_B
C6867
25V
0.22u
cap_0603_36mil
Q6812
BSZ065N03LS
mosfet8_3p3x3p3x1p1_p65mm
Q6811
BSZ019N03LS
mosfet8_3p3x3p3x1p1_p65mm
LGATE_VCCGT1
+VCCGT_IN
+VSYS
DB,PWR_GT
PR6815 0.010
res_0603_30mil
PC6818
1000p 25V
CAP_0201_14mil
PC6819
10u 10V
cap_0603_36mil
PC6822
10u 10V
cap_0603_36mil
PMTP6802
SP-tp-c0p381
PMTP6801
SP-tp-c0p381
TDC[A] <= 16A
Icc(max) <= 32A
+VCCGT
L6805
0.18uH
17A
ind_7p05x6p6x2_6p05mm
EV1.9 WAS:10
R6862
2.2
RES_0402_16mil
C6801 220u 2V cap_3_7p3x4p3x1_6p1mm
C6869 220u 2V cap_3_7p3x4p3x1_6p1mm
C6870 220u 2V cap_3_7p3x4p3x1_6p1mm
R6856
3.65K
res_0402_22mil
R6858
100K
res_0402_16mil
DNP,PWR_GT
R6859
100K
res_0402_16mil
[66] ISEN1_B
[66] ISEN2_B
ISUMN_B [66]
ISUMP_B [66]
[66] FCCM_B
+5V
C6872
4.7u 6.3V
cap_0402_26mil
U6811
ISL95808HRZ
dfn9_2x2x1_p5mm-2
UGATE_VCCGT2
PHASE_VCCGT2
BOOT_VCCGT2
LGATE_VCCGT2
[66] PWM2_B
Q6814
BSZ065N03LS
mosfet8_3p3x3p3x1p1_p65mm
+VCCGT_IN
PC6820
1000p 25V
CAP_0201_14mil
PC6821
10u 10V
cap_0603_36mil
PC6823
10u 10V
cap_0603_36mil
R6860
100K
res_0402_16mil
DNP,PWR_GT
R6861
100K
res_0402_16mil
EV1.9 WAS:11
R6863
2.2
RES_0402_16mil
R6864
3.65K
res_0402_22mil
C6871
25V
0.22u
cap_0603_36mil
L6806
0.18uH
17A
ind_7p05x6p6x2_6p05mm
Q6813
BSZ019N03LS
mosfet8_3p3x3p3x1p1_p65mm
GND
Title: VCVGT
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 68 of 76



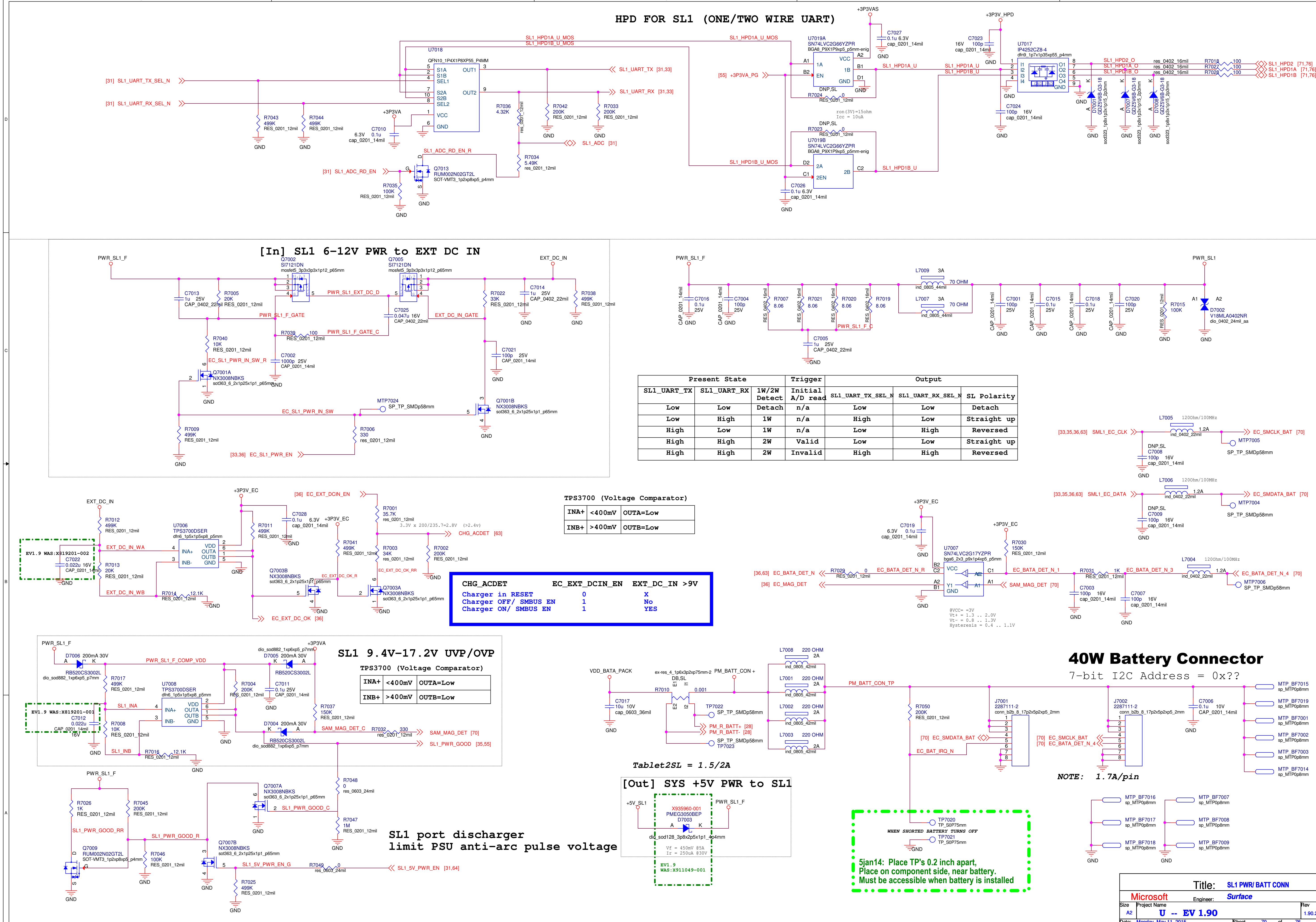
Title: SI Coupon (was BOOST/GTX REG)

Microsoft

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 69 of 76



Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed

TPS3700 (Voltage Comparator)

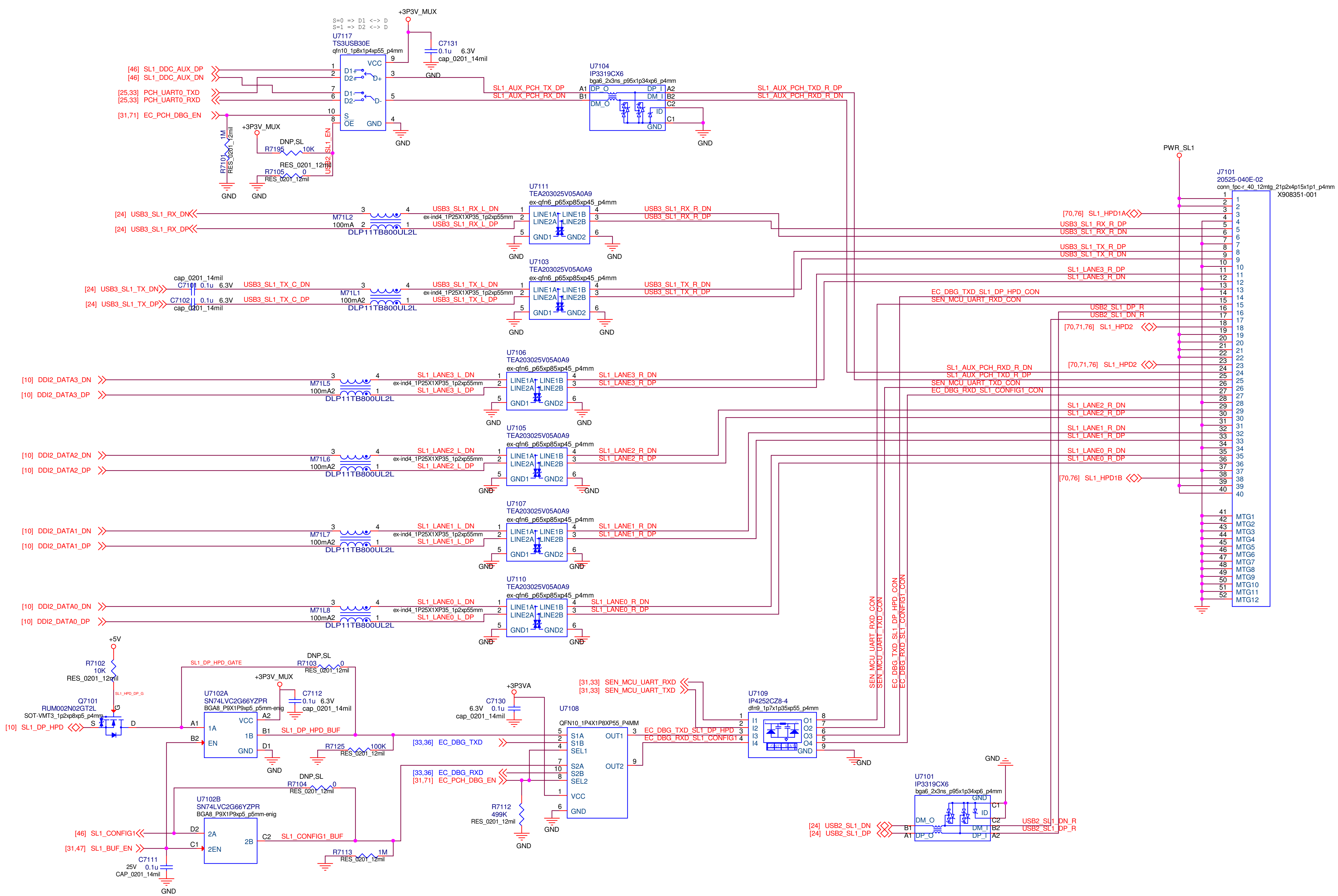
INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

CHG_ACDET	EC_EXT_DCIN_EN	EXT_DC_IN >9V
Charger in RESET	0	X
Charger OFF/ SMBUS EN	1	No
Charger ON/ SMBUS EN	1	YES

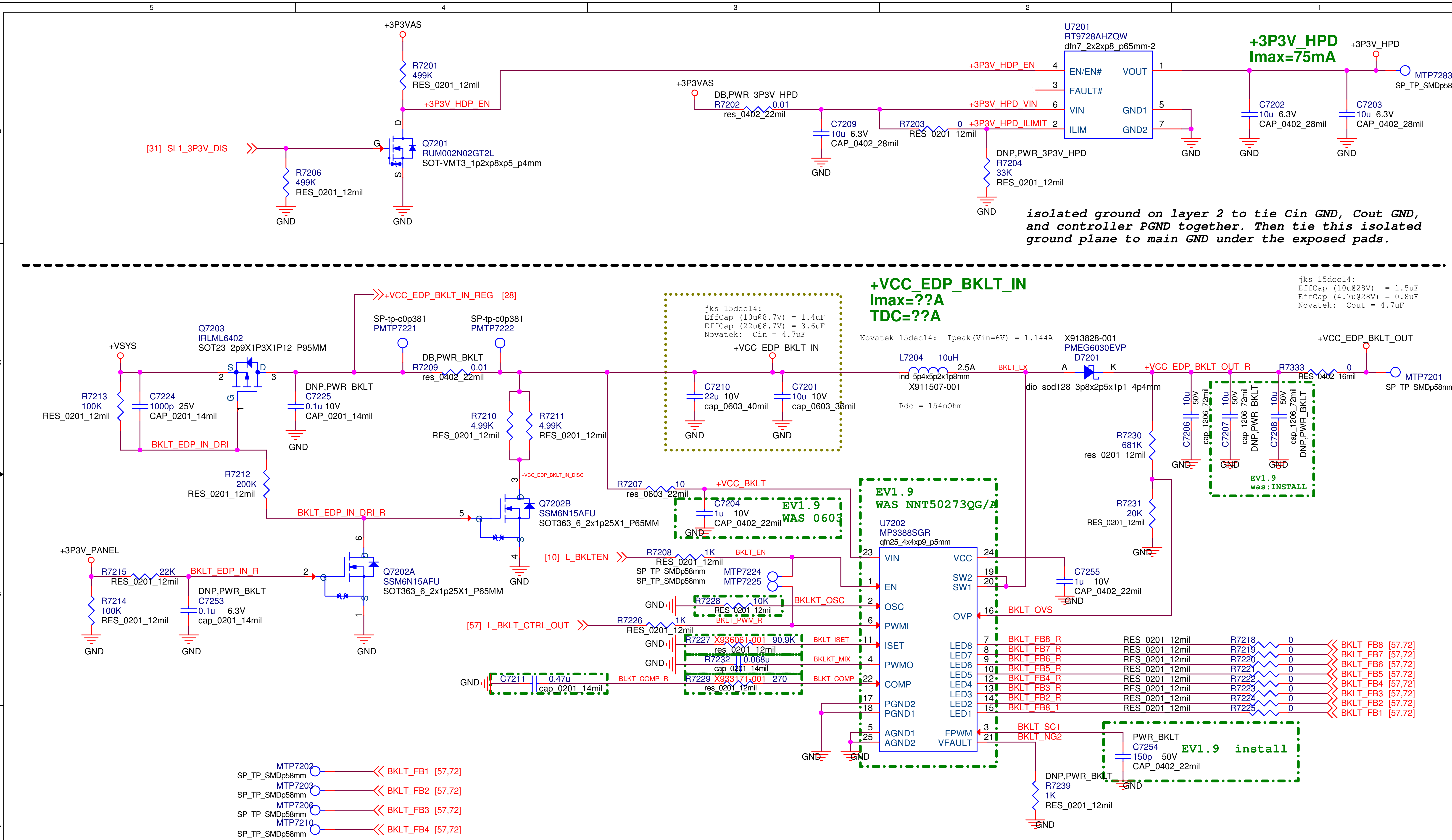
TPS3700 (Voltage Comparator)

INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

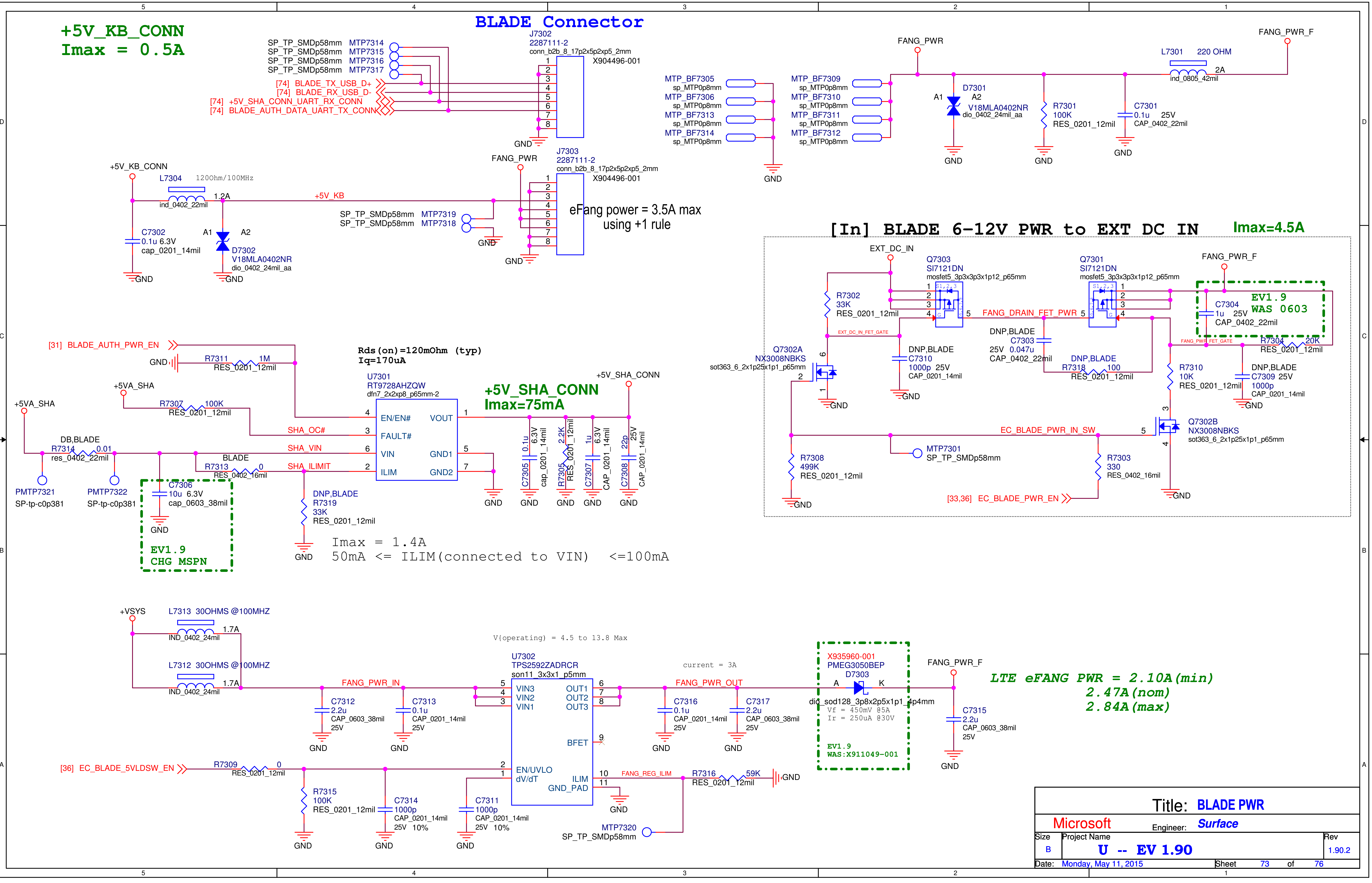
Microsoft	Title: SL1 PWR/ BATT CONN	Engineer: Surface	
Size A2	Project Name U -- EV 1.90		Rev 1.90.2
Date: Monday, May 11, 2015		Sheet 70 of 76	

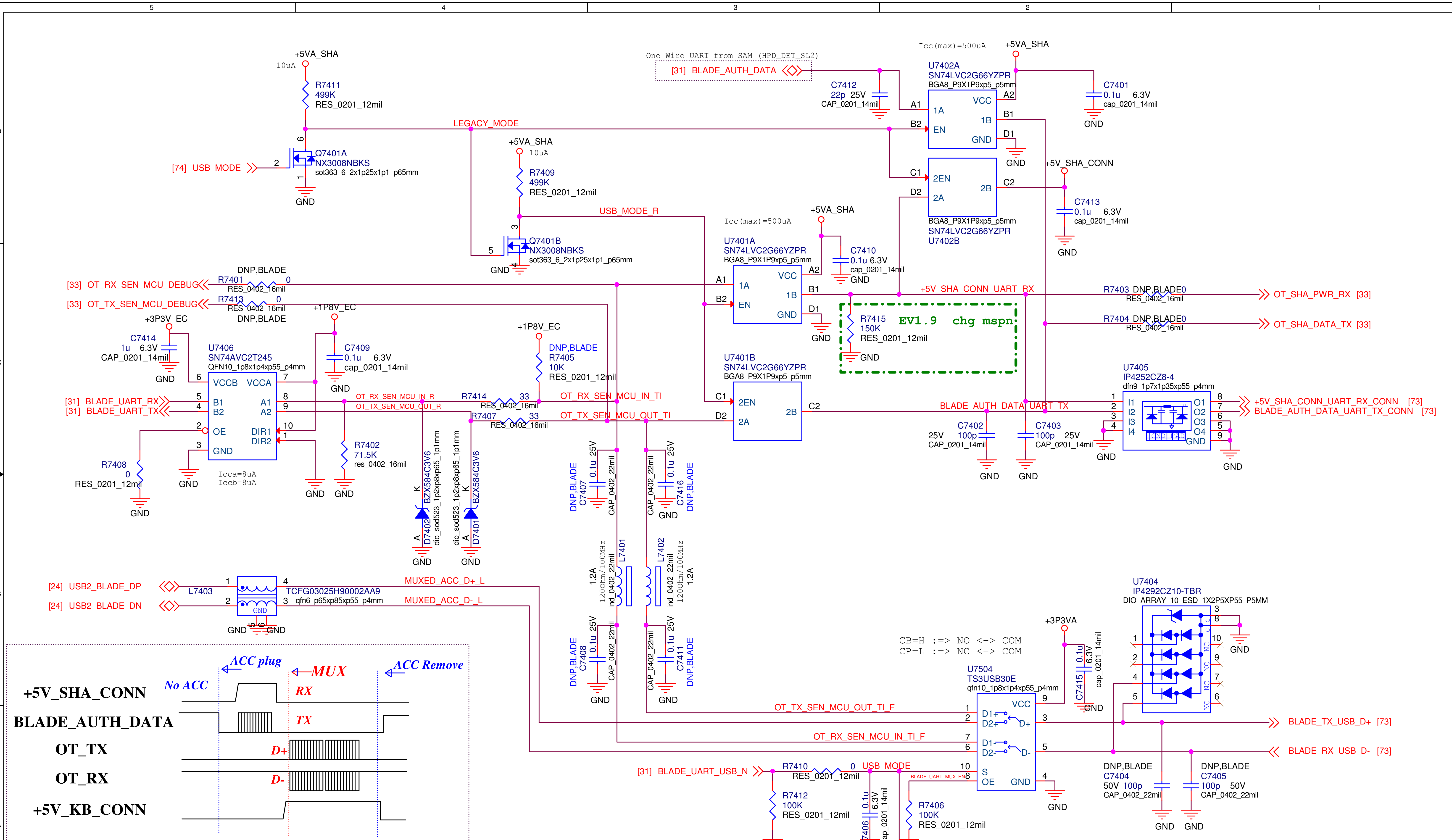


Microsoft	Title: SL1 SIGNALS		
	Engineer: Surface		
Size C	Project Name U -- EV 1.90		Rev 1.90.2
Date: Monday, May 11, 2015		Sheet 71 of 76	



Title:	+3P3V_HPD/LCD backlight
Microsoft	Engineer: Surface
Size: B	Project Name: U -- EV 1.90
Rev	1.90.2
Date: Monday, May 11, 2015	Sheet 72 of 76


+5V_KB_CONN
Imax = 0.5A
BLADE Connector
J7302
2287111-2
conn_b2b_8_17p2x5p2xp5_2mm
X904496-001
SP_TP_SMDp58mm MTP7314
SP_TP_SMDp58mm MTP7315
SP_TP_SMDp58mm MTP7316
SP_TP_SMDp58mm MTP7317
[74] BLADE_TX_USB_D+
[74] BLADE_RX_USB_D-
[74] +5V_SHA_CONN_UART_RX_CONN
[74] BLADE_AUTH_DATA_UART_TX_CONN
MTP_BF7305 sp_MTP0p8mm
MTP_BF7306 sp_MTP0p8mm
MTP_BF7313 sp_MTP0p8mm
MTP_BF7314 sp_MTP0p8mm
MTP_BF7309 sp_MTP0p8mm
MTP_BF7310 sp_MTP0p8mm
MTP_BF7311 sp_MTP0p8mm
MTP_BF7312 sp_MTP0p8mm
FANG_PWR
D7301 V18MLA0402NR dio_0402_24mil_aa
R7301 100K RES_0201_12mil
C7301 0.1u 25V CAP_0402_22mil
L7301 220 OHM ind_0805_42mil 2A
FANG_PWR_F
+5V_KB_CONN
L7304 120Ohm/100MHz ind_0402_22mil 1.2A
+5V_KB
C7302 0.1u 6.3V cap_0201_14mil
D7302 V18MLA0402NR dio_0402_24mil_aa
J7303 2287111-2 conn_b2b_8_17p2x5p2xp5_2mm X904496-001
SP_TP_SMDp58mm MTP7319
SP_TP_SMDp58mm MTP7318
eFang power = 3.5A max using +1 rule
[In] BLADE 6-12V PWR to EXT DC IN
Imax=4.5A
EXT_DC_IN
Q7303 SI7121DN mosfet5_3p3x3p3x1p12_p65mm
Q7301 SI7121DN mosfet5_3p3x3p3x1p12_p65mm
R7302 33K RES_0201_12mil
FANG_DRAIN_FET_PWR
EXT_DC_IN_FET_GATE
C7304 1u 25V CAP_0402_22mil
EV1.9 WAS 0603
DNP,BLADE C7303 25V 0.047u CAP_0402_22mil
DNP,BLADE R7318 100 RES_0201_12mil
R7304 20K RES_0201_12mil
FANG_PWR_FET_GATE
Q7302A NX3008NBKS sot363_6_2x1p25x1p1_p65mm
DNP,BLADE C7310 1000p 25V CAP_0201_14mil
R7310 10K RES_0201_12mil
DNP,BLADE C7309 25V 1000p CAP_0201_14mil
EC_BLADE_PWR_IN_SW
Q7302B NX3008NBKS sot363_6_2x1p25x1p1_p65mm
MTP7301 SP_TP_SMDp58mm
R7308 499K RES_0201_12mil
R7303 330 RES_0402_16mil
[33,36] EC_BLADE_PWR_EN
[31] BLADE_AUTH_PWR_EN
R7311 1M RES_0201_12mil
Rds(on)=120mOhm (typ)
Iq=170uA
U7301 RT9728AHZQW dfn7_2x2xp8_p65mm-2
EN/EN# VOUT FAULT# VIN GND1 ILIM GND2
+5V_SHA_CONN
Imax=75mA
+5VA_SHA
R7307 100K RES_0201_12mil
SHA_OC#
SHA_VIN
SHA_ILIMIT
DB,BLADE R7314 0.01 res_0402_22mil
BLADE R7313 0 RES_0402_16mil
PMTP7321 SP-tp-c0p381
PMTP7322 SP-tp-c0p381
C7306 10u 6.3V cap_0603_38mil
EV1.9 CHG MSPN
DNP,BLADE R7319 33K RES_0201_12mil
C7305 0.1u 6.3V cap_0201_14mil
R7305 2.2K RES_0201_12mil
C7307 1u 6.3V CAP_0201_14mil
C7308 22p 25V CAP_0201_14mil
Imax = 1.4A
50mA <= ILIM(connected to VIN) <=100mA
+VSYS
L7313 30OHMS @100MHZ IND_0402_24mil 1.7A
L7312 30OHMS @100MHZ IND_0402_24mil 1.7A
V(operating) = 4.5 to 13.8 Max
U7302 TPS2592ZADRCR son11_3x3x1_p5mm
VIN3 VIN2 VIN1 OUT1 OUT2 OUT3 BFET EN/UVLO dV/dT ILIM GND_PAD
FANG_PWR_IN
C7312 2.2u CAP_0603_38mil 25V
C7313 0.1u CAP_0201_14mil 25V
current = 3A
FANG_PWR_OUT
C7316 0.1u CAP_0201_14mil 25V
C7317 2.2u CAP_0603_38mil 25V
X935960-001 PMEG3050BEP D7303
dio_sod128_3p8x2p5x1p1_4p4mm
Vf = 450mV @5A
Ir = 250uA @30V
EV1.9 WAS:X911049-001
FANG_PWR_F
C7315 2.2u CAP_0603_38mil 25V
LTE eFANG PWR = 2.10A(min) 2.47A(nom) 2.84A(max)
[36] EC_BLADE_5VLDSW_EN
R7309 0 RES_0201_12mil
R7315 100K RES_0201_12mil
C7314 1000p CAP_0201_14mil 25V 10%
C7311 1000p CAP_0201_14mil 25V 10%
FANG_REG_ILIM
R7316 59K RES_0201_12mil
MTP7320 SP_TP_SMDp58mm
GND
Title: BLADE PWR
Microsoft
Engineer: Surface
Size B
Project Name U -- EV 1.90
Rev 1.90.2
Date: Monday, May 11, 2015
Sheet 73 of 76



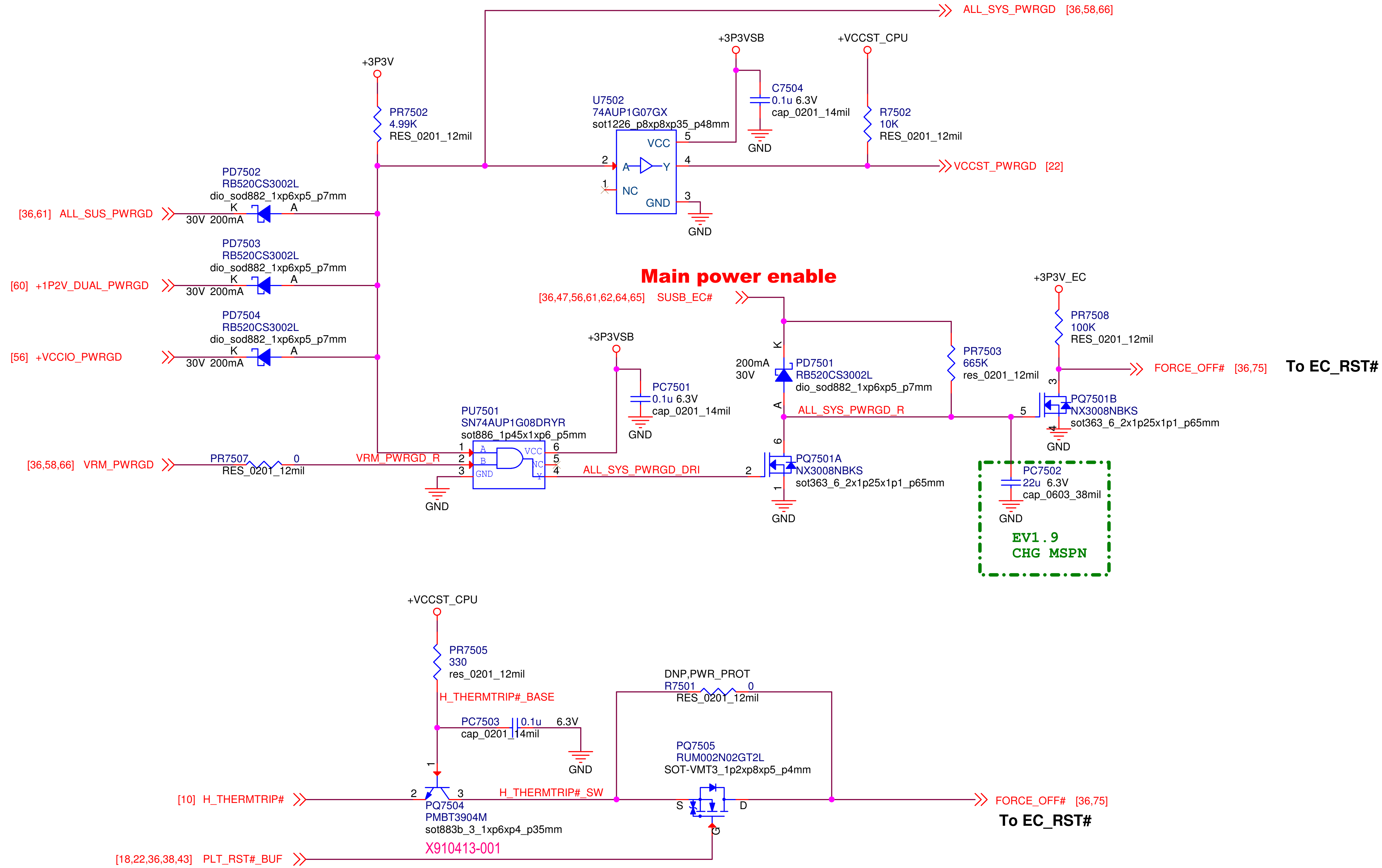
Title: Components for ME/ EMI

Microsoft

Engineer: Surface

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 74 of 76



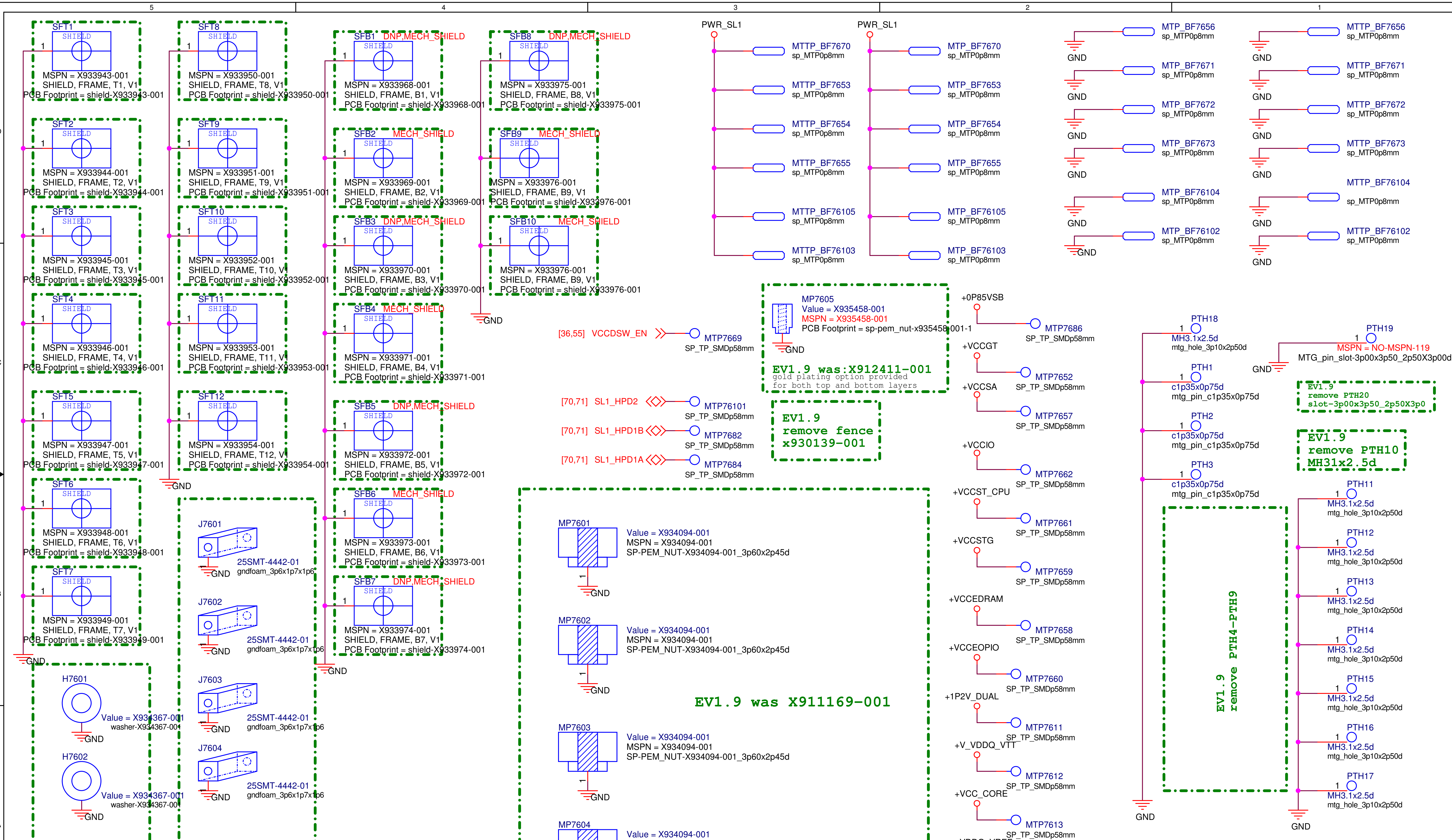
Title: **Power Protect**

Microsoft

Engineer: *Surface*

Size	Project Name	Rev
B	U -- EV 1.90	1.90.2

Date: Monday, May 11, 2015 Sheet 75 of 76



Title:	Test Point	
Microsoft	Engineer:	Surface
Size: B	Project Name: U -- EV 1.90	Rev: 1.90.2
Date: Monday, May 11, 2015	Sheet 76 of 76	