MS-7C51 Ver:1.1

CPU:
AMD AM4

System Chipset:
Promontory A320
(Value DIY or System Builder)

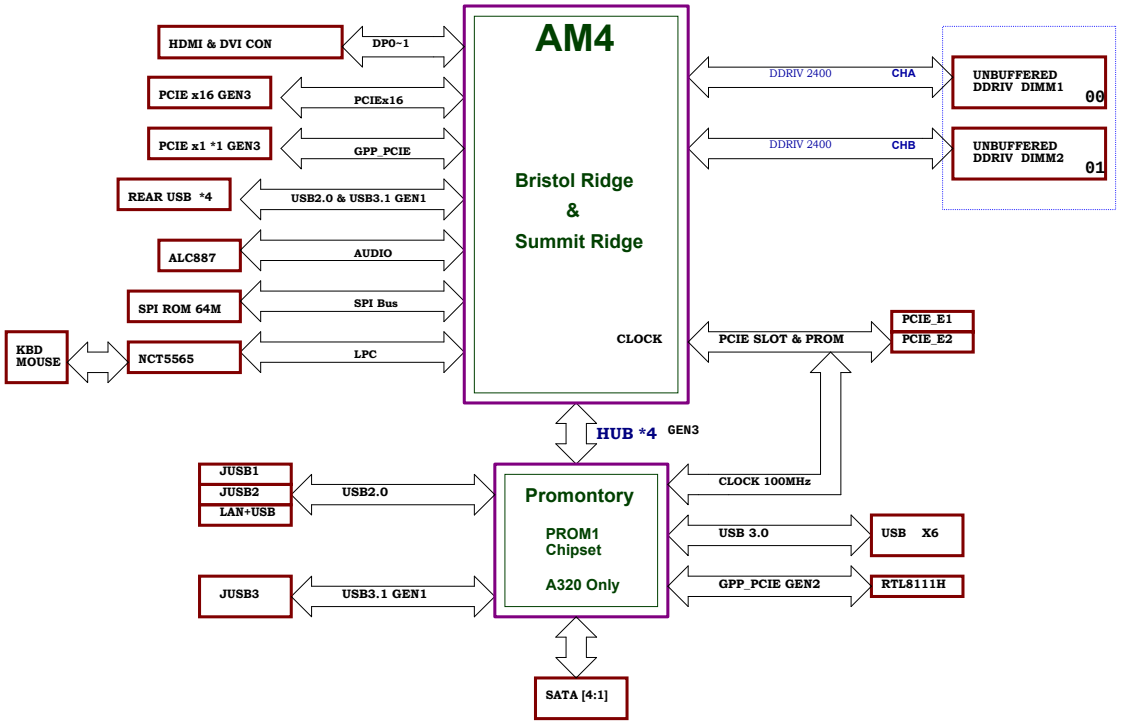
Main Memory:
DDR IV * 2 MAX:64 GB

VRM
RT8894 3+2

On Board Chipset:
LPC Super I/O --NCT5565
LAN RTL8111H
Azalia CODEC - Realtek ALC887

Expansion Slots:
From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1

FUSION BLOCK DIAGRAM



MICRO-START INT'L CO.,LTD.

Title: Block Diagram		
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 1 of 50	

AMD AM4

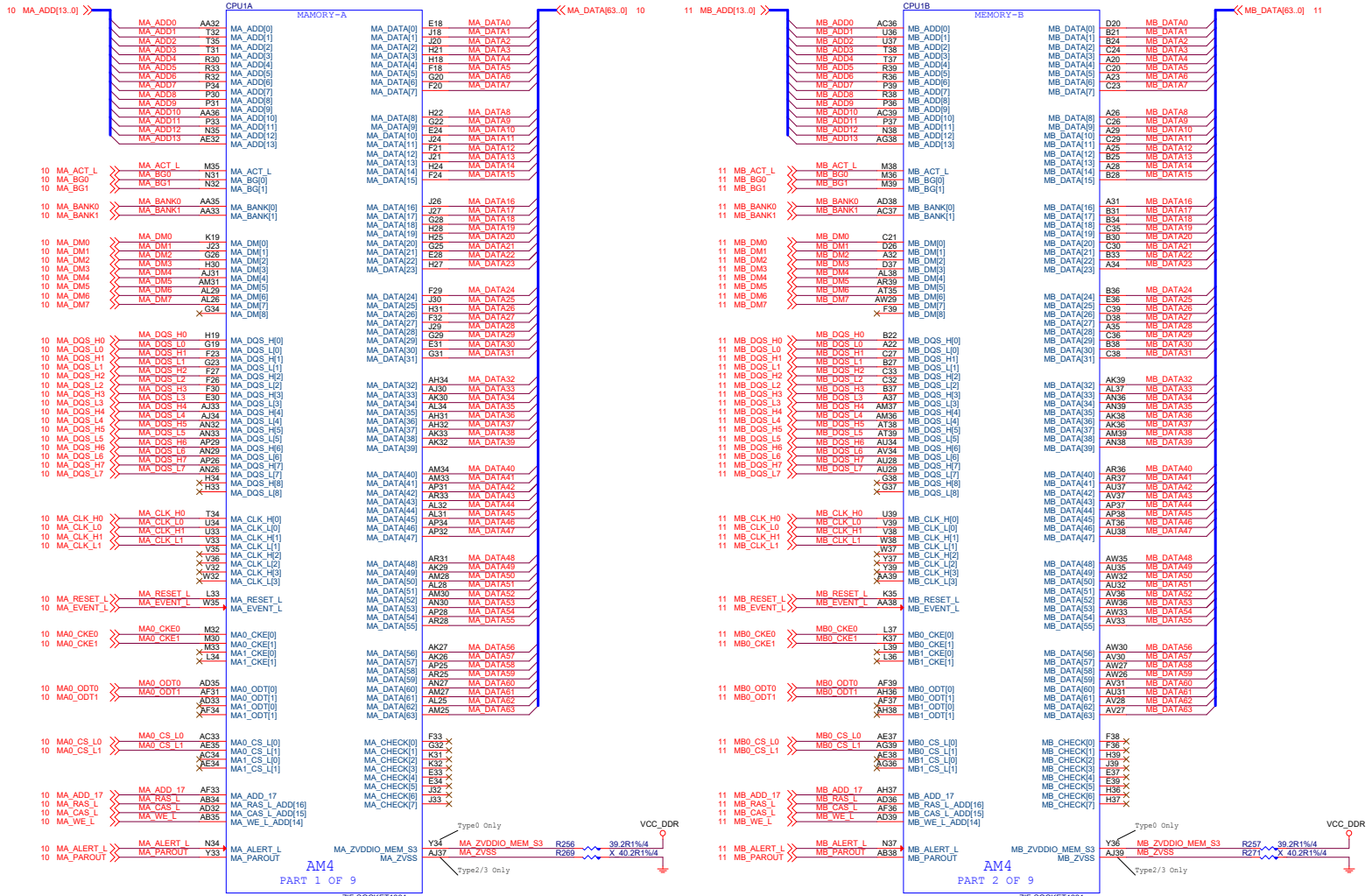
01 Block Diagram	36 CPU Power VDDP-RT8125E
02 Cover Sheet	37 CPU Power Connector/PWRGD
03 FM4 DDR4 I/F	38 CPU Power uP9505 3+2 Phase
04 AM4 PCIE/SATAE	39 CPU Power Phase 1-3
05 AM4 Display/Audio	40 CPU Power NB Phase 1-2
06 AM4 SVI/ACPI/GPIO	41 CPU Power NB Switch/NCT3933
07 AM4 LPC/SPI/USB/CLK/STRAP	42 UP6273 CURRENT SENSE
08 AM4 Power/RTC Power/ 09 AM4 GND	43 ATX/Front Panel
10,11 DDR4-DIMM CH-A/B	44 ALL LED Control
12,13 DDR4-POWER/GND	45 BOM Option
14 Promontory-PCIE/SATA/SATAE	46 RTC Circuit/Moat Cap
15 Promontory-USB/OC	47 History
16 Promontory-CLK/ACPI/GPIO	48 Power Sequence
17 Promontory-Power / 18 Promontory-GND	49 Power Delivery
19 PCIE X16(X1*2) SLOT	50 GPIO MAP
20 SIO NCT5565	
21 CPU/SYS FAN Control TYPE K	
22 LAN-RTL8111H	
23 / 24 Audio ALC887	
25 USB Rear PS2+USB2.0	
26 USB Rear LAN+USB3.1 GEN1	
27 USB Front Side	
28 SATA Connector	
29 DVI Connector	
30 DP to VGA ITE6516	
31 ACPI uPI-5VDIMM&3VSB	
32 PM-NB681-1.05V/GS7133-2.5V	
33 DDR PWR VPP25/VTT-MP2143	
34 DDR Power-RT8231AGQW	
35 CPU Power 1P8V-MP2147	

MSI MICRO-START INT'L CO.,LTD.

Title: COVER SHEET

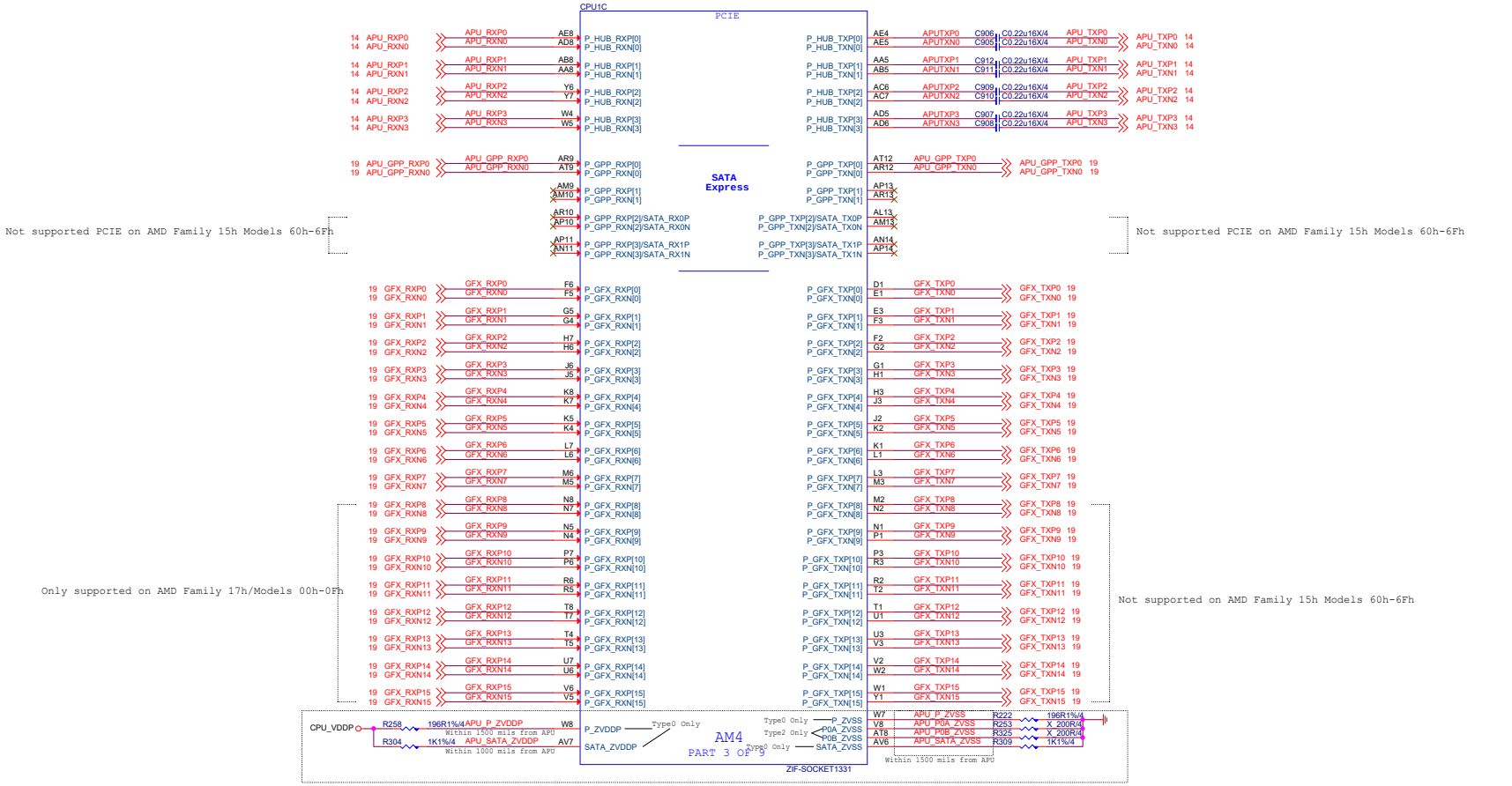
Size: Custom | Document Number: MS-7C51 | Rev: 1.1

Date: Thursday, July 04, 2019 | Sheet 2 of 50

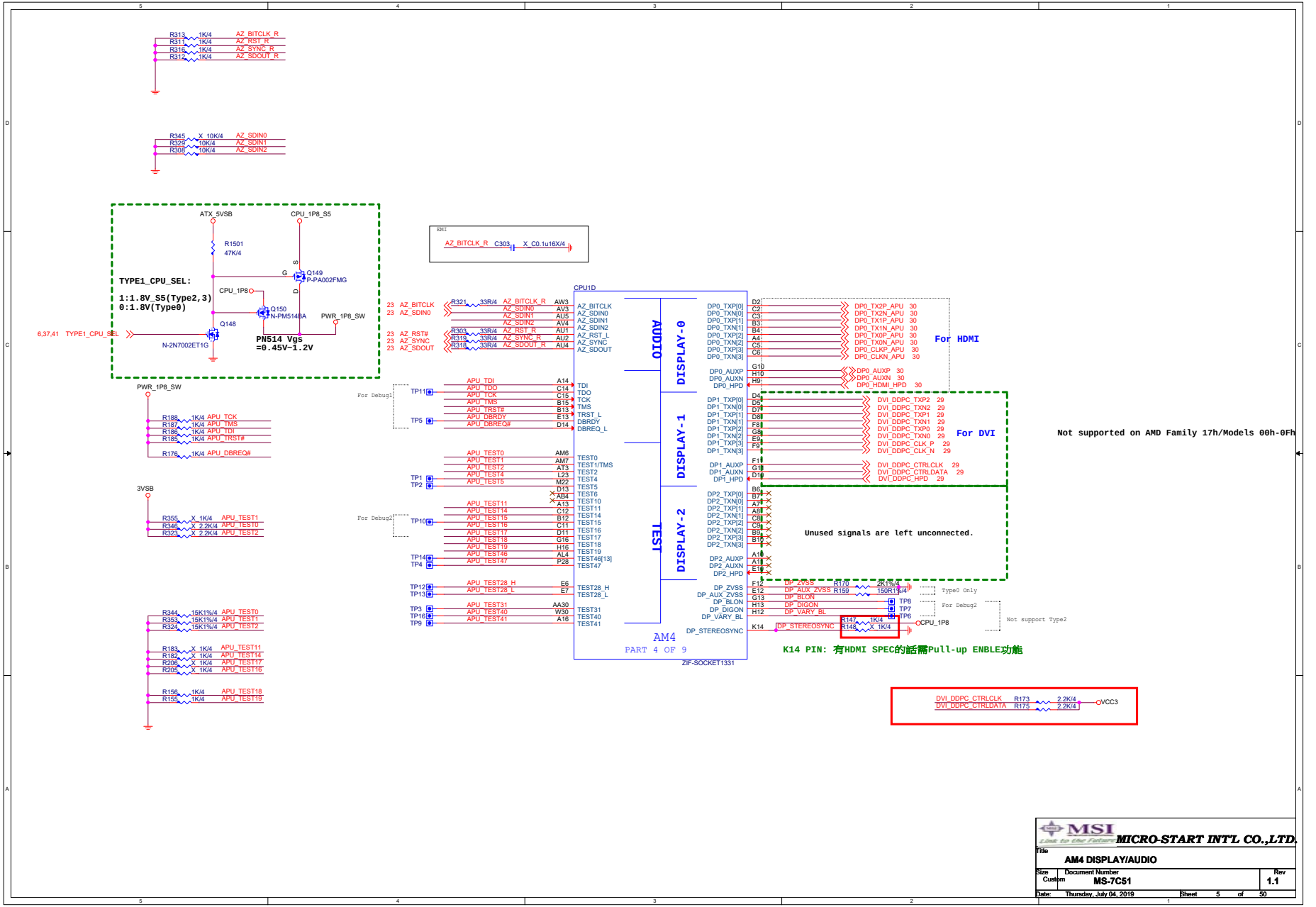


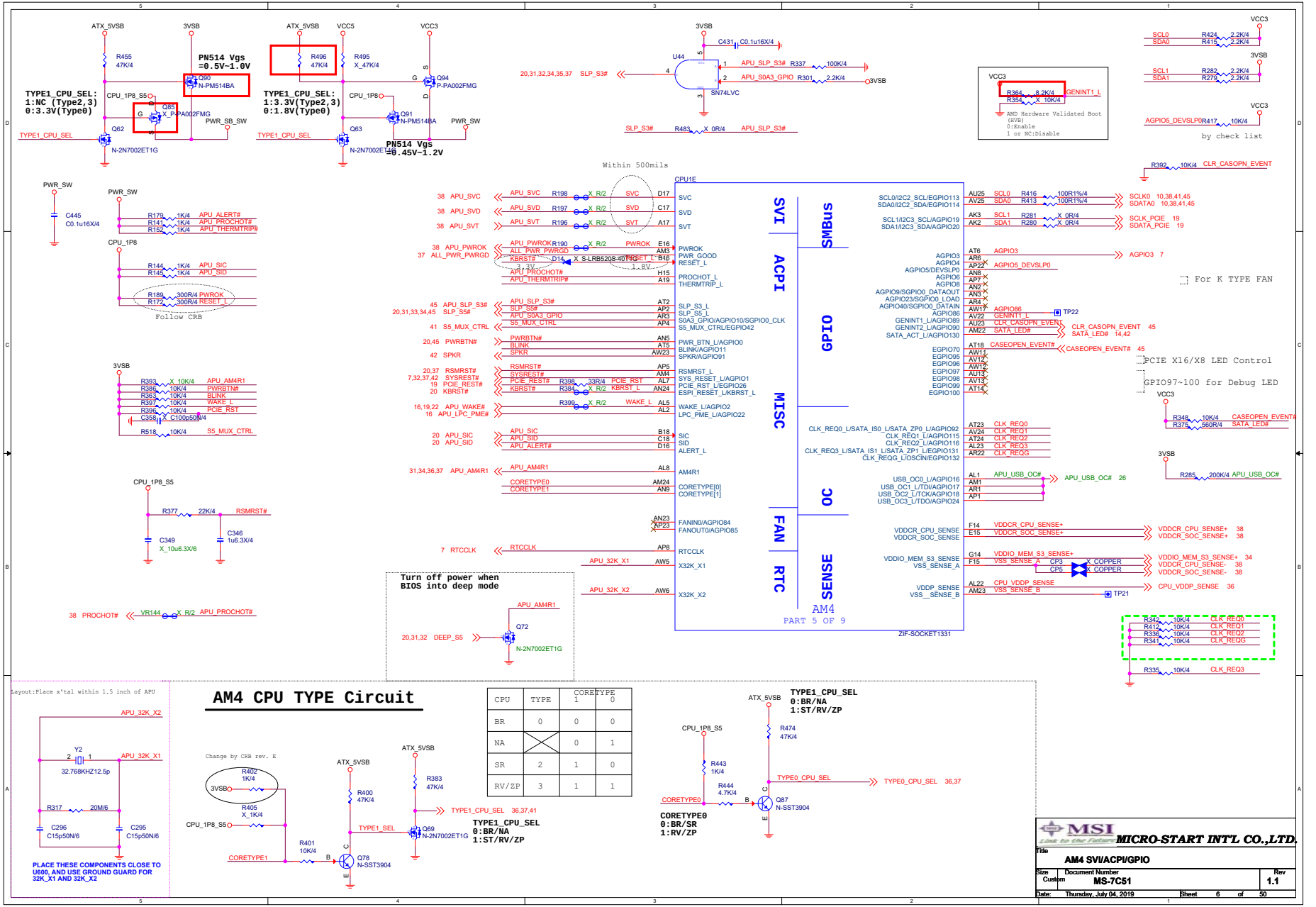
MICRO-START INT'L CO.,LTD.

Title	AM4 DDR4 I/F	
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 3 of 50	

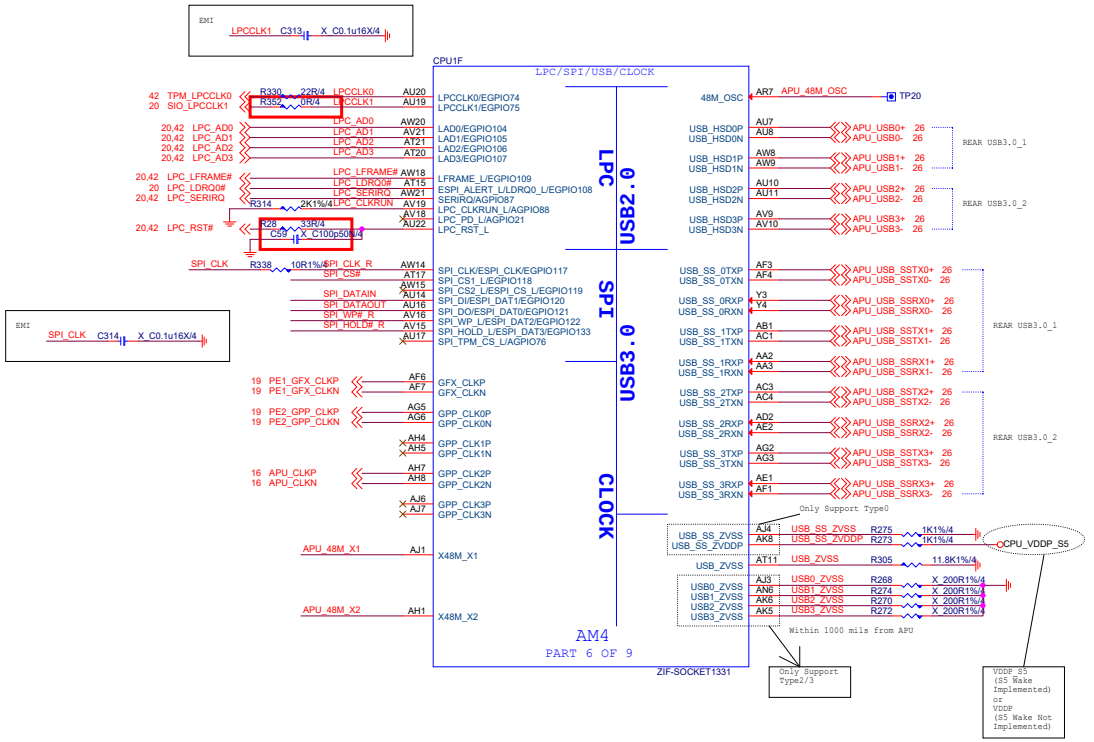


MSI MICRO-START INT'L CO.,LTD.			
Title: AM4 PCIE/SATAE			
Size: Custom	Document Number: MS-7C51		Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 4 of 50		

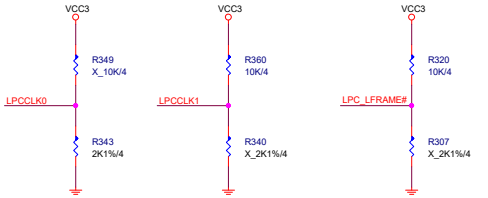

R313 1K/4 AZ_BITCLK_R
R311 1K/4 AZ_RST_R
R316 1K/4 AZ_SYNC_R
R312 1K/4 AZ_SDOUT_R
R345 X_10K/4 AZ_SDIN0
R329 10K/4 AZ_SDIN1
R308 10K/4 AZ_SDIN2
ATX_5VSB
CPU_1P8_S5
R1501 47K/4
TYPE1_CPU_SEL:
1:1.8V_S5(Type2,3)
0:1.8V(Type0)
Q149 P-PA002FMG
Q150 N-PM514BA
Q148 N-2N7002ET1G
CPU_1P8
PWR_1P8_SW
6,37,41 TYPE1_CPU_SEL
PN514 Vgs
=0.45V~1.2V
EMI
AZ_BITCLK_R C303 X_C0.1u16X/4
CPU1D
AUDIO
DISPLAY-0
DISPLAY-1
TEST
AM4
PART 4 OF 9
ZIF-SOCKET1331
23 AZ_BITCLK
23 AZ_SDIN0
23 AZ_RST#
23 AZ_SYNC
23 AZ_SDOUT
R321 33R/4 AZ_BITCLK_R
R303 33R/4 AZ_RST_R
R319 33R/4 AZ_SYNC_R
R316 33R/4 AZ_SDOUT_R
AZ_SDIN0
AZ_SDIN1
AZ_SDIN2
AW3 AZ_BITCLK
AV3 AZ_SDIN0
AU5 AZ_SDIN1
AV4 AZ_SDIN2
AU1 AZ_RST_L
AU2 AZ_SYNC
AU4 AZ_SDOUT
For Debug1
TP11
TP5
APU_TDI A14 TDI
APU_TDO C14 TDO
APU_TCK C15 TCK
APU_TMS B15 TMS
APU_TRST# B13 TRST_L
APU_DBRDY E13 DBRDY
APU_DBREQ# D14 DBREQ_L
TP1
TP2
APU_TEST0 AM6 TEST0
APU_TEST1 AM7 TEST1/TMS
APU_TEST2 A13 TEST2
APU_TEST4 L23 TEST4
APU_TEST5 M22 TEST5
D13 TEST6
AB4 TEST10
For Debug2
TP10
APU_TEST11 A13 TEST11
APU_TEST14 C12 TEST14
APU_TEST15 B12 TEST15
APU_TEST16 C11 TEST16
APU_TEST17 D11 TEST17
APU_TEST18 G16 TEST18
APU_TEST19 H16 TEST19
TP14
TP4
APU_TEST46 AL4 TEST46[13]
APU_TEST47 P28 TEST47
TP12
TP13
APU_TEST28_H E6 TEST28_H
APU_TEST28_L E7 TEST28_L
TP3
TP16
TP9
APU_TEST31 AA30 TEST31
APU_TEST40 W30 TEST40
APU_TEST41 A16 TEST41
DP0_TXP[0] D2
DP0_TXN[0] C2
DP0_TXP[1] C3
DP0_TXN[1] B3
DP0_TXP[2] B4
DP0_TXN[2] A4
DP0_TXP[3] C5
DP0_TXN[3] C6
DP0_AUXP G10
DP0_AUXN H10
DP0_HPD H9
DP0_TX2P_APU 30
DP0_TX2N_APU 30
DP0_TX1P_APU 30
DP0_TX1N_APU 30
DP0_TX0P_APU 30
DP0_TX0N_APU 30
DP0_CLKP_APU 30
DP0_CLKN_APU 30
DP0_AUXP 30
DP0_AUXN 30
DP0_HDMI_HPD 30
For HDMI
DP1_TXP[0] D4
DP1_TXN[0] D5
DP1_TXP[1] D7
DP1_TXN[1] D8
DP1_TXP[2] F8
DP1_TXN[2] G8
DP1_TXP[3] E9
DP1_TXN[3] F9
DP1_AUXP F11
DP1_AUXN G11
DP1_HPD D10
DVI_DDPC_TXP2 29
DVI_DDPC_TXN2 29
DVI_DDPC_TXP1 29
DVI_DDPC_TXN1 29
DVI_DDPC_TXP0 29
DVI_DDPC_TXN0 29
DVI_DDPC_CLK_P 29
DVI_DDPC_CLK_N 29
DVI_DDPC_CTRLCLK 29
DVI_DDPC_CTRLDATA 29
DVI_DDPC_HPD 29
For DVI
Not supported on AMD Family 17h/Models 00h-0Fh
DP2_TXP[0] B6
DP2_TXN[0] B7
DP2_TXP[1] A7
DP2_TXN[1] A8
DP2_TXP[2] C8
DP2_TXN[2] C9
DP2_TXP[3] B9
DP2_TXN[3] B10
DP2_AUXP A10
DP2_AUXN A11
DP2_HPD E10
Unused signals are left unconnected.
DP_ZVSS F12
DP_AUX_ZVSS E12
DP_BLON G13
DP_DIGON H13
DP_VARY_BL H12
DP_STEREOSYNC K14
R170 2K1%/4
R159 150R1%/4
Type0 Only
TP8
TP7
TP6
For Debug2
R147 1K/4
R148 X_1K/4
CPU_1P8
Not support Type2
K14 PIN: 有HDMI SPEC的話需Pull-up ENBLE功能
R344 15K1%/4 APU_TEST0
R353 15K1%/4 APU_TEST1
R324 15K1%/4 APU_TEST2
R183 X_1K/4 APU_TEST11
R182 X_1K/4 APU_TEST14
R206 X_1K/4 APU_TEST17
R205 X_1K/4 APU_TEST15
R156 1K/4 APU_TEST18
R155 1K/4 APU_TEST19
PWR_1P8_SW
R188 1K/4 APU_TCK
R187 1K/4 APU_TMS
R186 1K/4 APU_TDI
R185 1K/4 APU_TRST#
R176 1K/4 APU_DBREQ#
3VSB
R355 X_1K/4 APU_TEST1
R346 X_2.2K/4 APU_TEST0
R323 X_2.2K/4 APU_TEST2
DVI_DDPC_CTRLCLK R173 2.2K/4
DVI_DDPC_CTRLDATA R175 2.2K/4
VCC3
MSI
MICRO-START INT'L CO.,LTD.
Title
AM4 DISPLAY/AUDIO
Size Custom
Document Number MS-7C51
Rev 1.1
Date: Thursday, July 04, 2019
Sheet 5 of 50



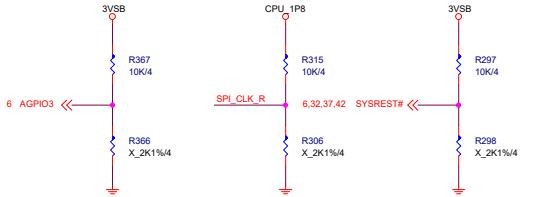
CPU	TYPE	CORETYPE 1	0
BR	0	0	0
NA		0	1
SR	2	1	0
RV/ZP	3	1	1



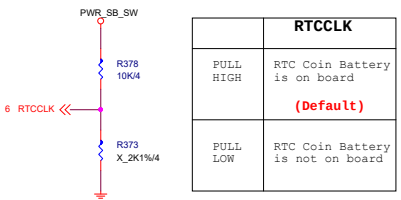
Strapping Options



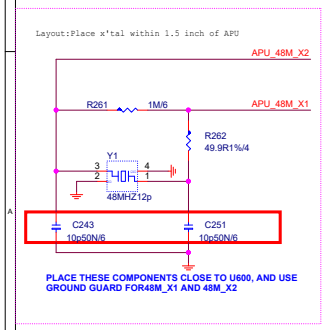
	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM



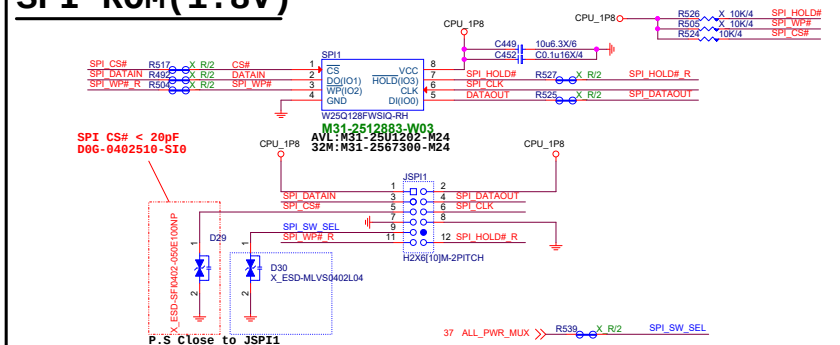
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board

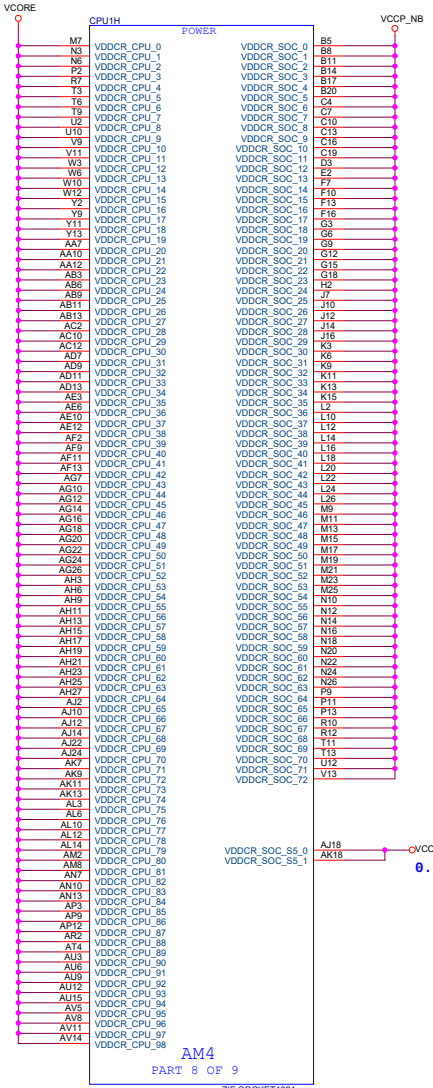


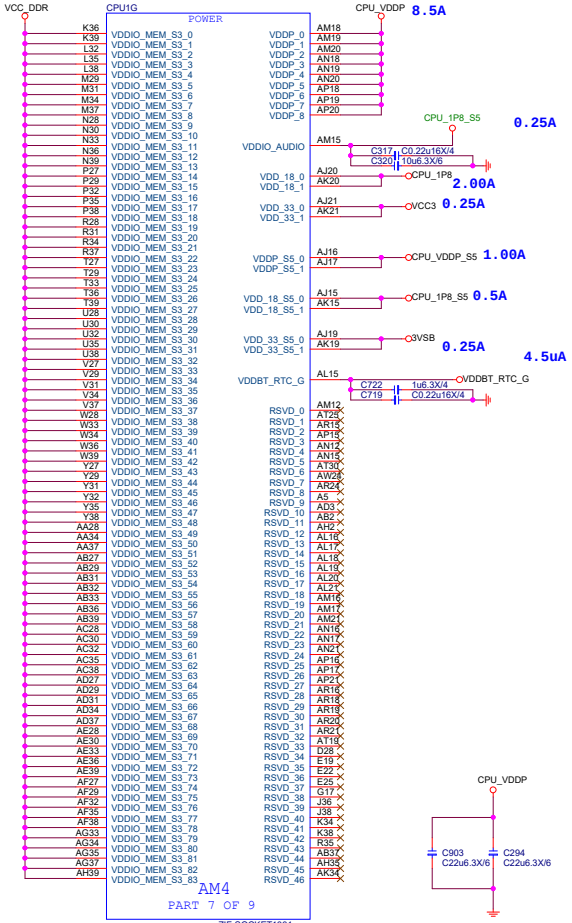
SPI ROM(1.8V)



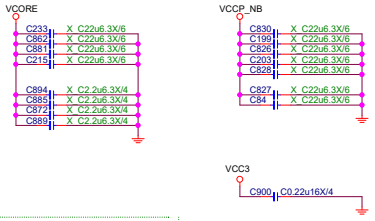
Title	MICRO-START INT'L CO.,LTD.		
	AM4 LPC/SPI/USB/CLK/STRAP		
Size: Custom	Document Number: MS-7C51		Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 7	of 50	

VDDIO_AUDIO Circuit

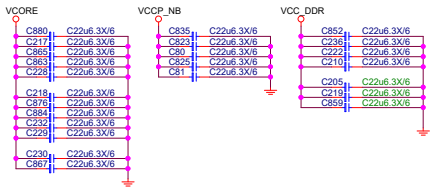




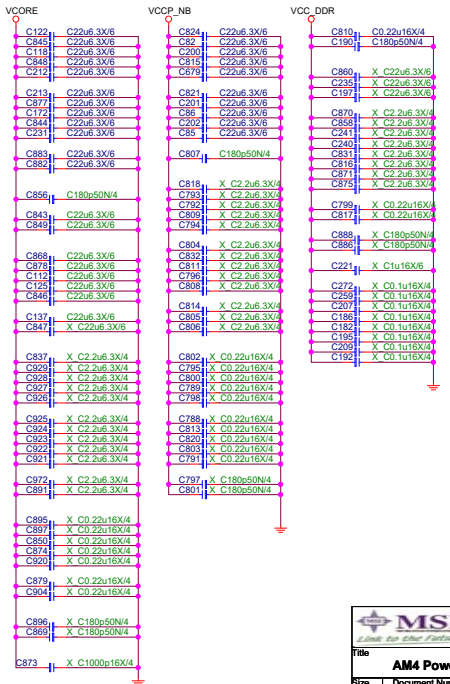
TOP SIDE



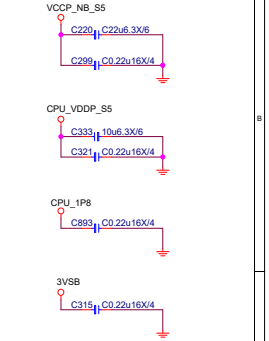
TOP CAVITY



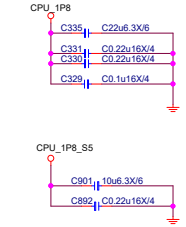
BOTTOM CAVITY



BOTTOM SIDE

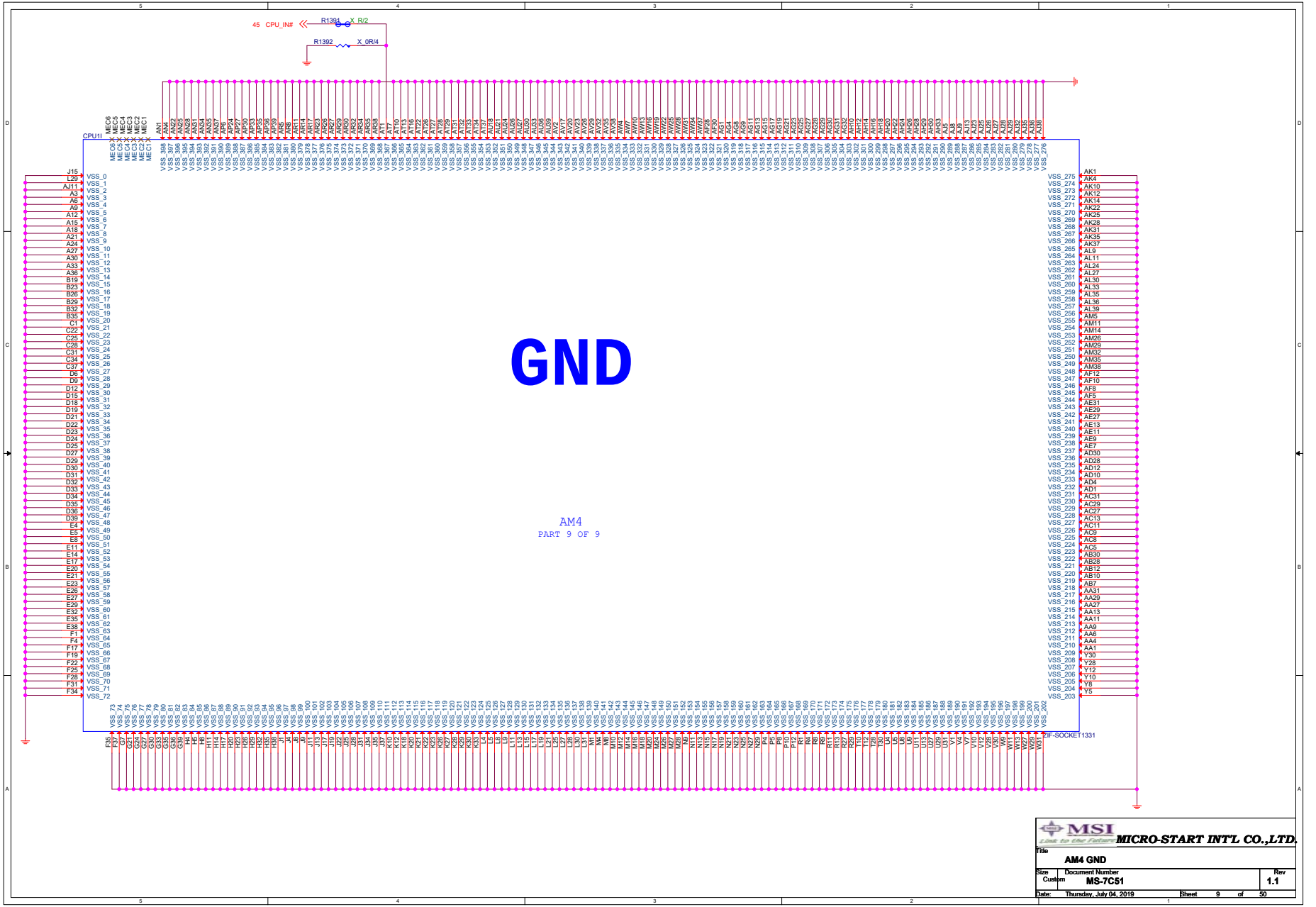


CPU_1P8

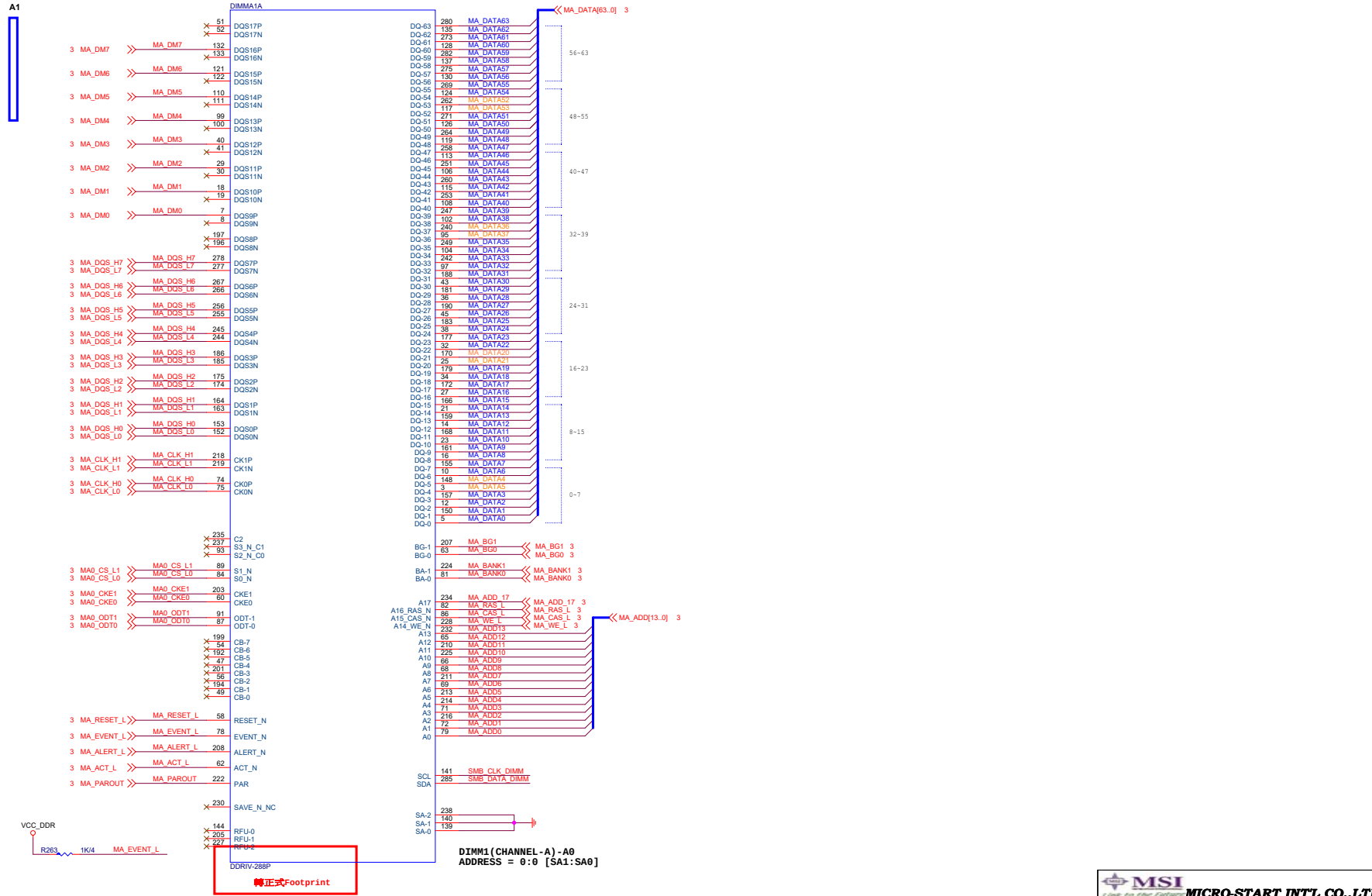


CPU_1P8_S5

MSI — Link for the Future	MICRO-START INT'L CO.,LTD.	
Title: AM4 Power/RTC Power		
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 8 of 50	

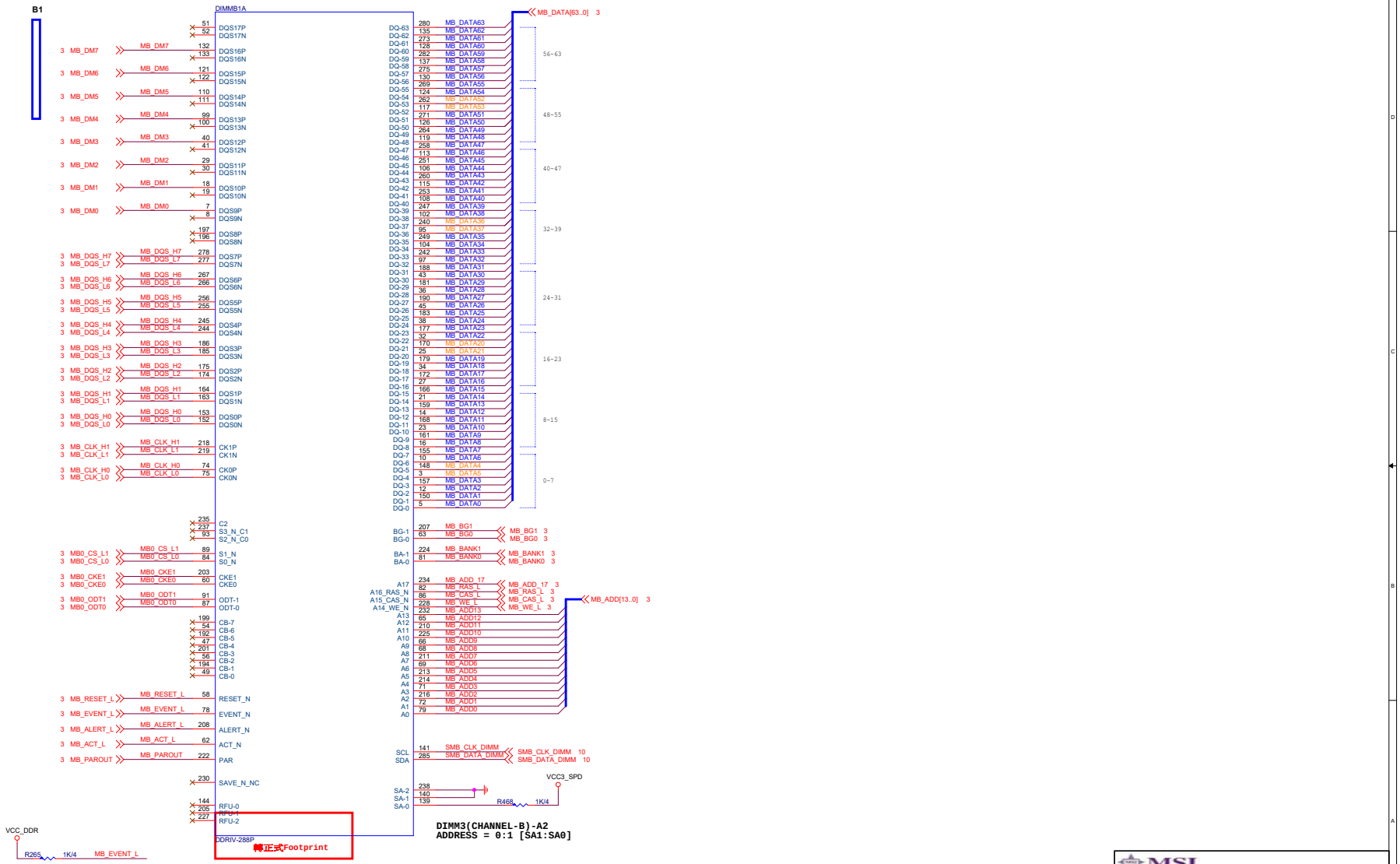


MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	AM4 GND		
Size: Custom	Document Number: MS-7C51	Rev: 1.1	
Date: Thursday, July 04, 2019	Sheet 9 of 50		



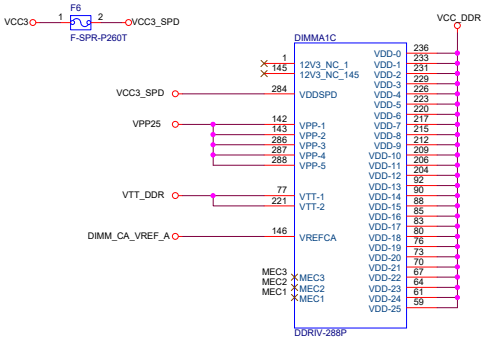
Title	DDR4 DIMM CH-A
Size	Custom
Document Number	MS-7C51
Rev	1.1
Date:	Thursday, July 04, 2019
Sheet	10 of 50

MICRO-START INT'L CO.,LTD.

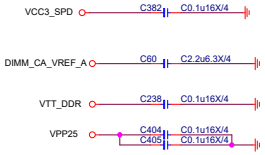


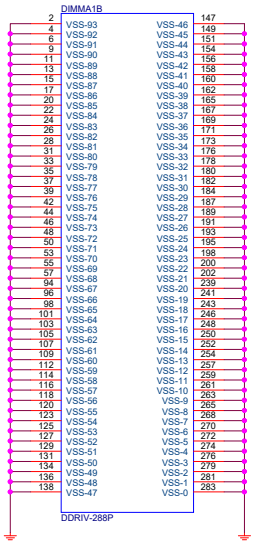
Title	DDR4 DIMM CH-B
Size	Custom
Document Number	MS-7C51
Rev	1.1
Date:	Thursday, July 04, 2019
Sheet	11 of 50

MSI Link to the Future MICRO-START INT'L CO.,LTD.



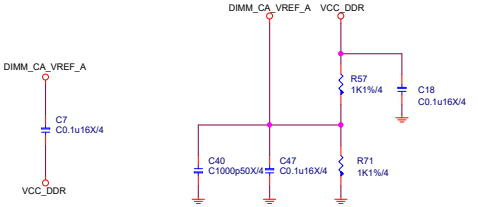
DIMM SLOT PN BY SPEC





DDR VREF

(place resistors close to DIMMs)

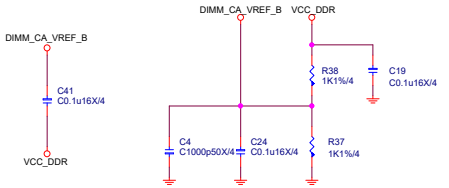


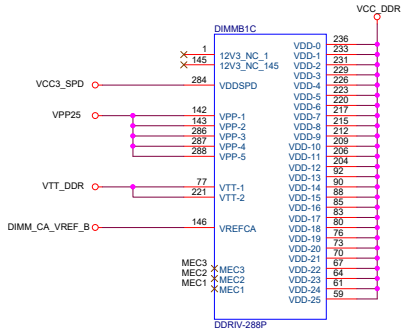
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

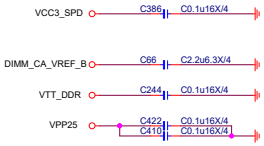
Title	DDR4-POWER/GND-1	
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 12 of 50	

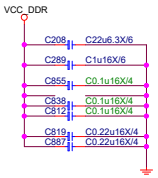
DDR VREF

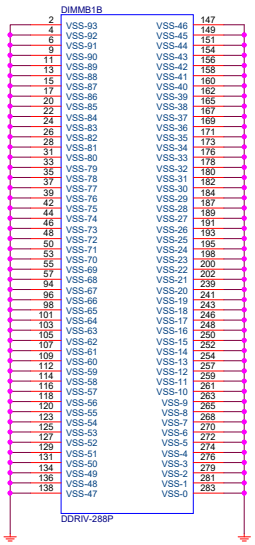
(place resistors close to DIMMs)



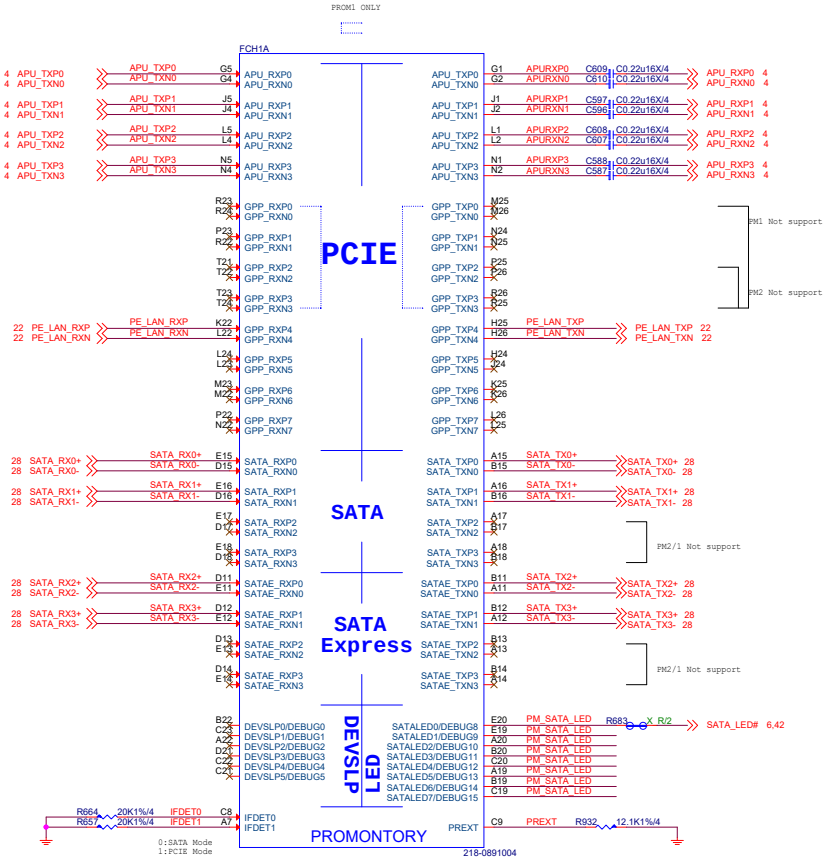




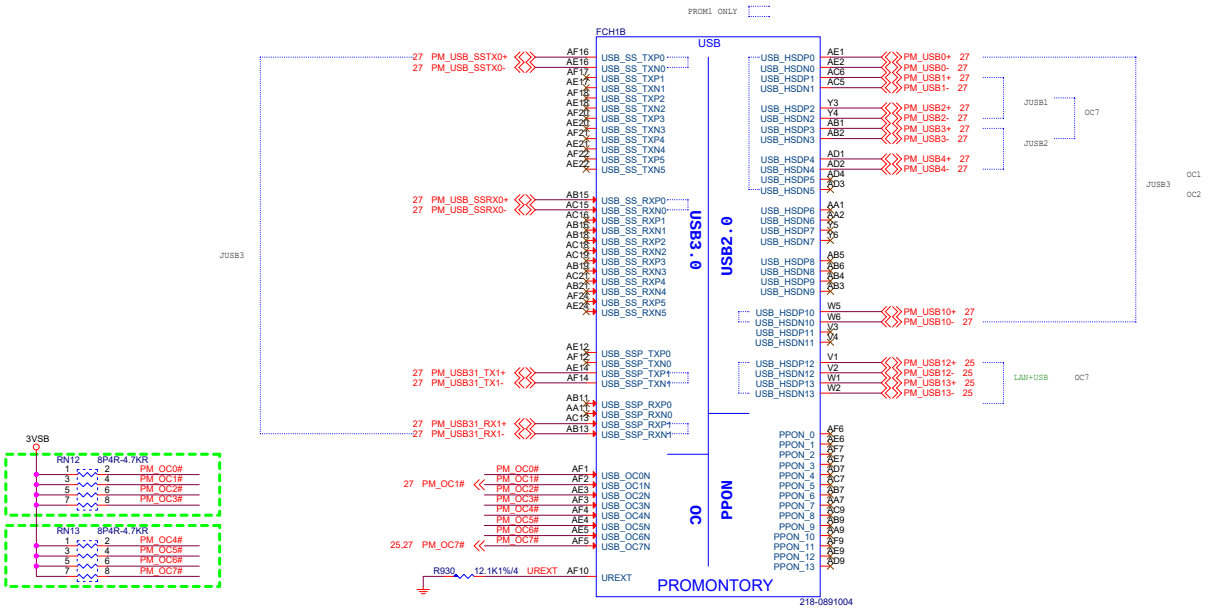




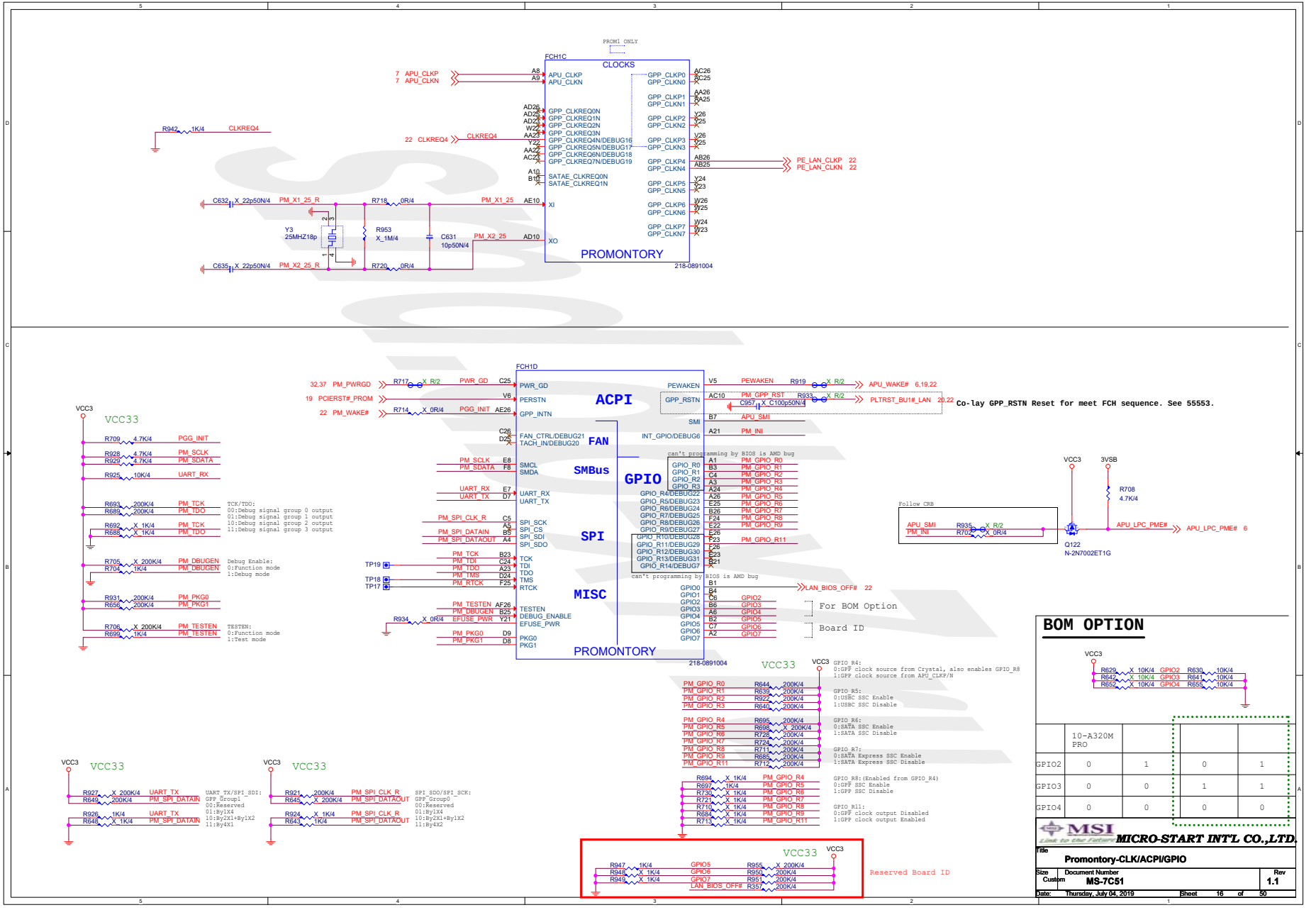
MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	DDR4-POWER/GND-2		
Size: Custom	Document Number: MS-7C51		Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 13 of 50		

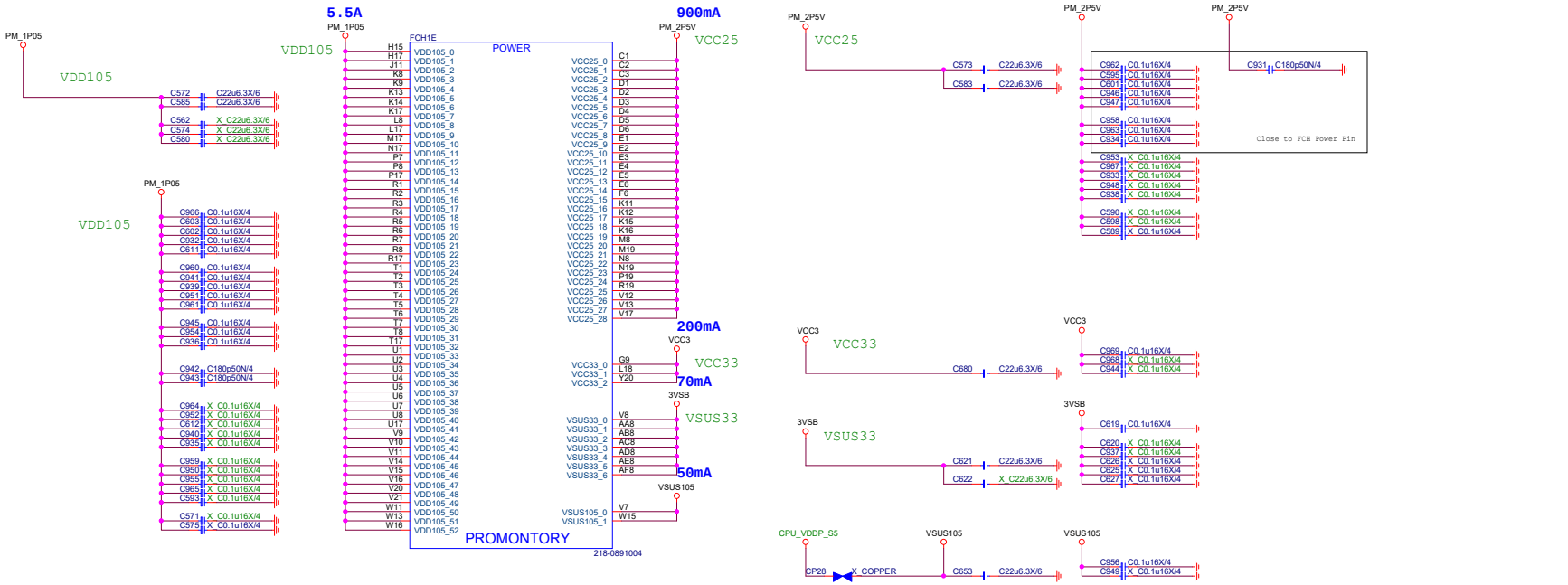


MSI	MICRO-START INT'L CO.,LTD.
Title	Promontory-PCIE/SATA/SATAE
Size: Custom	Document Number: MS-7C51
Rev	1.1
Date: Thursday, July 04, 2019	Sheet 14 of 50

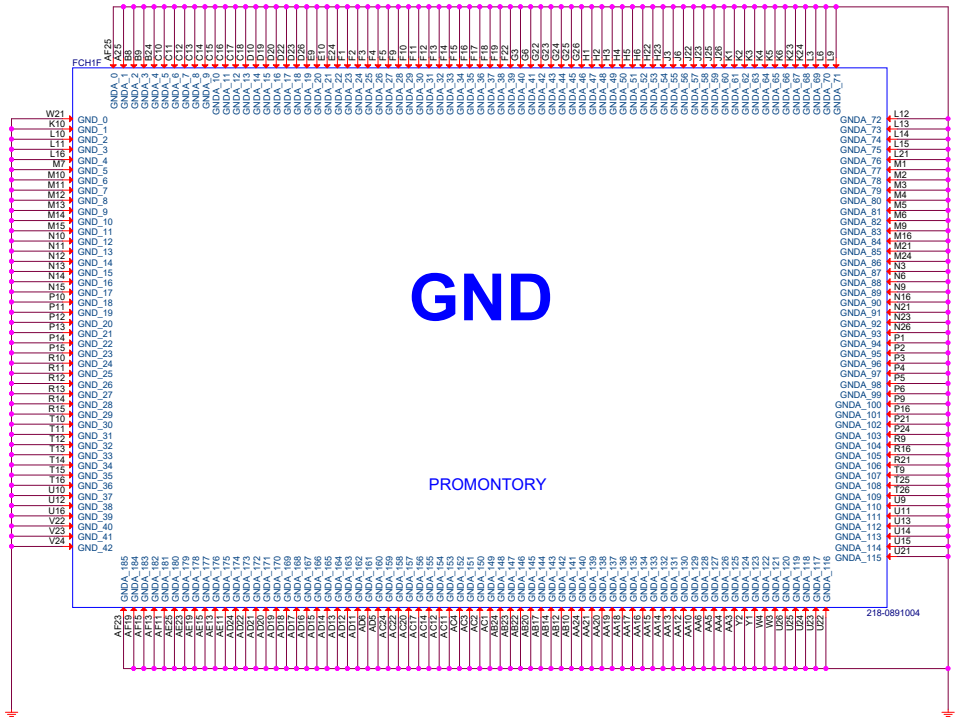


MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	Promontory-USB/OC		
Size: Custom	Document Number: MS-7C51		Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 15 of 50		


PROM1 ONLY
FCH1C
CLOCKS
7 APU_CLKP
7 APU_CLKN
APU_CLKP
APU_CLKN
GPP_CLKP0
GPP_CLKN0
GPP_CLKP1
GPP_CLKN1
GPP_CLKP2
GPP_CLKN2
GPP_CLKP3
GPP_CLKN3
GPP_CLKP4
GPP_CLKN4
GPP_CLKP5
GPP_CLKN5
GPP_CLKP6
GPP_CLKN6
GPP_CLKP7
GPP_CLKN7
PE_LAN_CLKP 22
PE_LAN_CLKN 22
22 CLKREQ4
CLKREQ4
R942 1K/4 CLKREQ4
GPP_CLKREQ0N
GPP_CLKREQ1N
GPP_CLKREQ2N
GPP_CLKREQ3N
GPP_CLKREQ4N/DEBUG16
GPP_CLKREQ5N/DEBUG17
GPP_CLKREQ6N/DEBUG18
GPP_CLKREQ7N/DEBUG19
SATAE_CLKREQ0N
SATAE_CLKREQ1N
C632 X 22p50N/4 PM_X1_25_R
R718 0R/4
PM_X1_25
AE10 XI
Y3 25MHz18p
R953 X_1M/4
C631 10p50N/4
PM_X2_25
AD10 XO
C635 X 22p50N/4 PM_X2_25_R
R720 0R/4
PROMONTORY
218-0891004
FCH1D
ACPI
FAN
SMBus
GPIO
SPI
MISC
PROMONTORY
218-0891004
32,37 PM_PWRGD
19 PCIERST#_PROM
22 PM_WAKE#
R717 X R/2
R714 X 0R/4
PWR_GD
PERSTN
GPP_INTN
PGG_INIT
PEWAKEN
GPP_RSTN
PM_GPP_RST
R919 X R/2
R933 X R/2
APU_WAKE# 6,19,22
PLTRST_BU1#_LAN 20,22
C957 X C100p50N/4
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
SMI
APU_SMI
PM_INI
INT_GPIO/DEBUG6
FAN_CTRL/DEBUG21
TACH_IN/DEBUG20
SMCL
SMDA
PM_SCLK
PM_SDATA
UART_RX
UART_TX
SPI_SCK
SPI_CS
SPI_SDI
SPI_SDO
PM_SPI_CLK_R
PM_SPI_DATAIN
PM_SPI_DATAOUT
TCK
TDI
TDO
TMS
RTCK
PM_TCK
PM_TDI
PM_TDO
PM_TMS
PM_RTCK
TESTEN
DEBUG_ENABLE
EFUSE_PWR
PM_TESTEN
PM_DBUGEN
R934 X 0R/4
PKG0
PKG1
PM_PKG0
PM_PKG1
can't programming by BIOS is AMD bug
GPIO_R0
GPIO_R1
GPIO_R2
GPIO_R3
GPIO_R4/DEBUG22
GPIO_R5/DEBUG23
GPIO_R6/DEBUG24
GPIO_R7/DEBUG25
GPIO_R8/DEBUG26
GPIO_R9/DEBUG27
GPIO_R10/DEBUG28
GPIO_R11/DEBUG29
GPIO_R12/DEBUG30
GPIO_R13/DEBUG31
GPIO_R14/DEBUG7
PM_GPIO_R0
PM_GPIO_R1
PM_GPIO_R2
PM_GPIO_R3
PM_GPIO_R4
PM_GPIO_R5
PM_GPIO_R6
PM_GPIO_R7
PM_GPIO_R8
PM_GPIO_R9
PM_GPIO_R11
LAN_BIOS_OFF# 22
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
For BOM Option
Board ID
VCC3
VCC33
3VSB
R709 4.7K/4 PGG_INIT
R928 4.7K/4 PM_SCLK
R929 4.7K/4 PM_SDATA
R925 10K/4 UART_RX
R693 200K/4 PM_TCK
R689 200K/4 PM_TDO
TCK/TDO:
00:Debug signal group 0 output
01:Debug signal group 1 output
10:Debug signal group 2 output
11:Debug signal group 3 output
R692 X 1K/4 PM_TCK
R688 X 1K/4 PM_TDO
R705 X 200K/4 PM_DBUGEN
R704 1K/4 PM_DBUGEN
Debug Enable:
0:Function mode
1:Debug mode
R931 200K/4 PM_PKG0
R656 200K/4 PM_PKG1
R706 X 200K/4 PM_TESTEN
R699 1K/4 PM_TESTEN
TESTEN:
0:Function mode
1:Test mode
TP19
TP18
TP17
Follow CRB
APU_SMI
PM_INI
R935 X R/2
R702 X 0R/4
Q122
N-2N7002ET1G
R708 4.7K/4
APU_LPC_PME#
APU_LPC_PME# 6
R927 X 200K/4 UART_TX
R649 200K/4 PM_SPI_DATAIN
R926 1K/4 UART_TX
R648 X 1K/4 PM_SPI_DATAIN
UART_TX/SPI_SDI:
GPP_Group1
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X1
R921 200K/4 PM_SPI_CLK_R
R645 X 200K/4 PM_SPI_DATAOUT
R924 X 1K/4 PM_SPI_CLK_R
R643 1K/4 PM_SPI_DATAOUT
SPI_SDO/SPI_SCK:
GPP_Group0
00:Reserved
01:By1X4
10:By2X1+By1X2
11:By4X2
GPIO_R4:
0:GPP clock source from Crystal, also enables GPIO_R8
1:GPP clock source from APU_CLKP/N
GPIO_R5:
0:USBC SSC Enable
1:USBC SSC Disable
GPIO_R6:
0:SATA SSC Enable
1:SATA SSC Disable
GPIO_R7:
0:SATA Express SSC Enable
1:SATA Express SSC Disable
GPIO_R8:(Enabled from GPIO_R4)
0:GPP SSC Enable
1:GPP SSC Disable
GPIO_R11:
0:GPP clock output Disabled
1:GPP clock output Enabled
R947 1K/4 GPIO5
R948 X 1K/4 GPIO6
R949 X 1K/4 GPIO7
R955 X 200K/4
R950 200K/4
R951 200K/4
LAN_BIOS_OFF# R357 200K/4
Reserved Board ID
BOM OPTION
R629 X 10K/4 GPIO2 R630 10K/4
R642 X 10K/4 GPIO3 R641 10K/4
R652 X 10K/4 GPIO4 R655 10K/4
10-A320M PRO
GPIO2 0 1 0 1
GPIO3 0 0 1 1
GPIO4 0 0 0 0
MSI
MICRO-START INT'L CO.,LTD.
Title
Promontory-CLK/ACPI/GPIO
Size Custom
Document Number MS-7C51
Rev 1.1
Date: Thursday, July 04, 2019
Sheet 16 of 50



MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	Promontory-Power		
Size: Custom	Document Number: MS-7C51		Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 17 of 50		

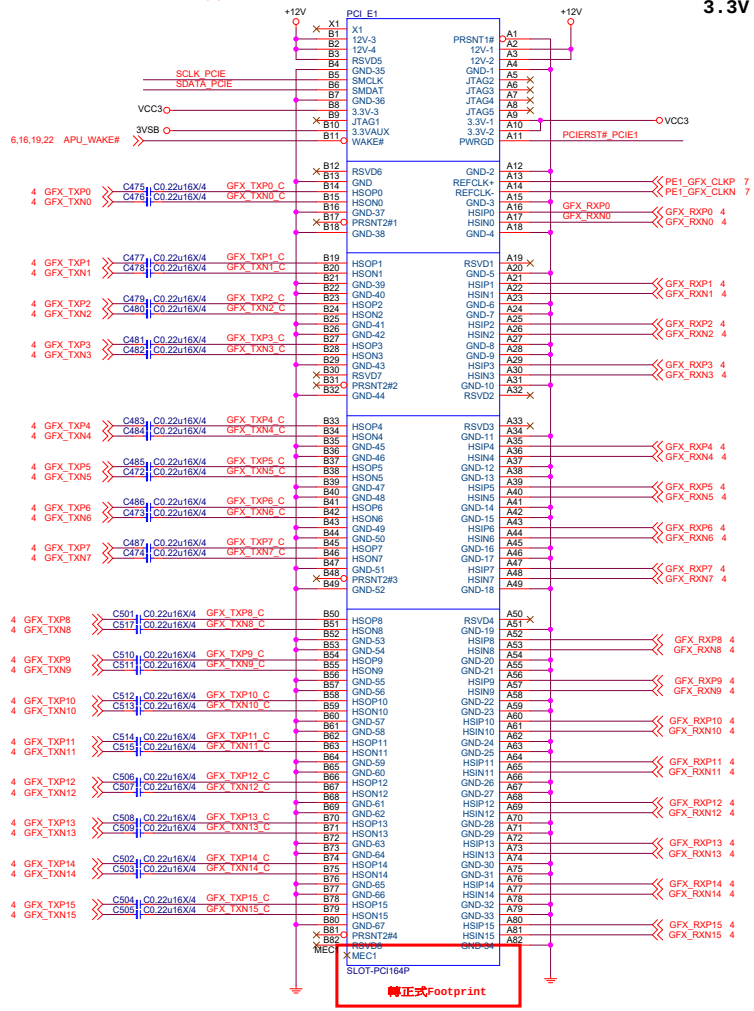


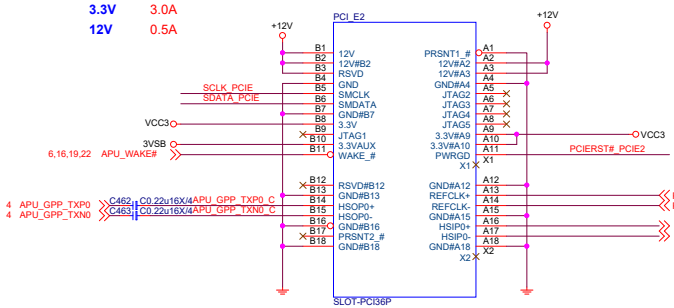
MSI Link to the Future	MICRO-START INT'L CO.,LTD.			
Title	Promontory-GND			
Size: Custom	Document Number: MS-7C51			Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 18 of 50			

PCI EXPRESS x16 Slot

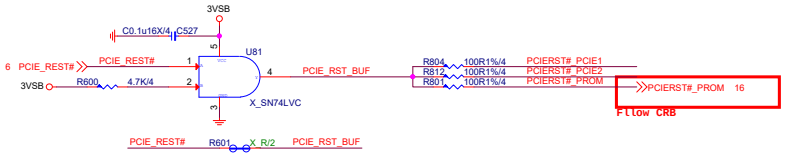
3.3V 3.0A
12V 5.5A

PCIEX1 12V 0.5A
3.3V weak 375mA

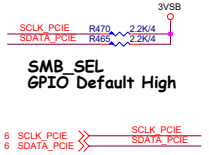




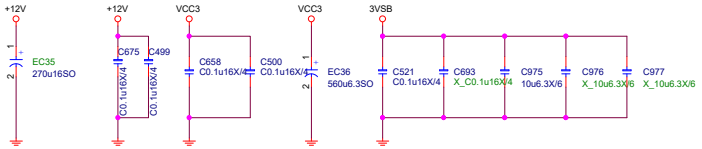
within 500mil

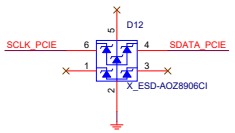


SMBus separate circuit



SMB_SEL
GPIO Default High





MSI	MICRO-START INT'L CO.,LTD.		
Title	PCIE X16(X1*2) SLOT		
Size: Custom	Document Number: MS-7C51		Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 19 of 50		

GP70 的GPIO可以選成GRN_LED ， 所以有呼吸燈的功能 ， 但有兩項要注意 ：
1, GRN_LED在您的案子應該會是PWR LED (LED_VCC)
2, GP70有DSW_EN的hardware strapping , 所以外部會有
pull-up 到SIO_3VA.

U46

ESPI/LPC Interface
PLTRST#/LRESET#
ESPI_CLK/LCLK
ESPI_RST#/LDRQ#
SERIRQ
ESPI_CS#/LFRAME#
ESPI_IO0/LAD0
ESPI_IO1/LAD1
ESPI_IO2/LAD2
ESPI_IO3/LAD3

UART SIR
RIA#/GP87
DCDA#/GP86
(TESTMODE1_EN)SOUTA/GP85
SINA/GP84
(FANOUT_DEF_EN)DTRA#/GP83
(2E_4E_SEL)RTSA#/GP82
DSRA#/GP81
CTSA#/GP80

KBC Function
KBRST#
(ESPI_EN)GA20M
AUXFANIN2/GP20/KDAT
CIRRX/AUXFANOUT2/GP21/KCLK
AUXFANIN3/GP22/MDAT
AUXFANOUT3/GP23/MCLK

DSW Interface
GP54/SLP_SUS#
DPWROK
DEEP_S5_1/CASEOPEN*/#
USBEN/3VSBSW/PWROK/ATXPGDO

Hardware Monitor
VIN2
VIN1
VIN0
CPUVCORE
VREF
AUXTIN0/VIN4
CPUTIN

FAN Control
CPUFANIN
CPUFANOUT
SYSFANIN
SYSFANOUT

ACPI Function
RSMRST#
PSIN#
PSOUT#
SLP_S3#
SLP_S5#
PSON#
ATXPGD
PWROK
RSTOUT0#/GP74
GP57/AUXFANIN2
GP56/AUXFANOUT2

Power Pin
PWR_FAULT#GP26/TSIC
PECI/TSID
GPO/GP73/CUT_VBAT
(DSW_EN)GP70
VIN7/AUXTIN3/ATX_5VSB
PAD_CAP
PCHVSB
VTT
VBAT
3VSB
AVSB
3VCC
PAD_VDD
VSS
CPUD-/AGND

NCT5565D

Change P/N

20181029
update to G3下可clean CMOS.

D49 S-LRB520S-40T1G

default Push-Pull

Stuff for New version IO

1.5V

=1.527V

<1.2V DPWROK LOW FOR AC POWER LOSS

close to PIN11

COM PORT

NO USE UART PORT1

GD75232DBR

JCOM1

CN2 X_8P4C-470p50X/6

CN1 X_8P4C-470p50X/6

POWER ON STRAPPING PIN FOR NCT5565D

PIN	5563D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	FANOUT_DEF_EN	DTRA#	CPU FANOUT default RPM 50%.	CPU FANOUT default RPM 100%
21	TESTMODE1_EN	SOUTA	DISABLE TEST1MODE	ENABLE TEST1MODE
14	ESPI_EN	GA20M	ENABLE LPC	ENABLE ESPI
35	DSW_EN	DSW_EN	DISABLE	ENABLE DSW_EN

HW Monitor - Voltage

VCORE R350 10K1%/4 CPUVcore
R368 X_10K1%/4 C356 10u6.3X/6

+12V R369 220K1%/4 VIN0
R370 20K1%/4 C344 C0.1u16X/4

VCC5 R372 12K1%/4 VIN1
R359 3K1%/4 C351 C0.1u16X/4

VCCP_NB R362 10K1%/4 VIN2
R407 X_10K1%/4 C316 10u6.3X/6

3V Analog Power

SIO_3VA DEEP_S5 R814 47K/4

SIO_3VA CP24 X_COPPER AVCC3 AVCC3
C415 C0.1u16X/4 C318 10u6.3X/6

default Push-Pull

LPC_LDRQ0# R1500 4.7K/4
PLTRST_BUI#_R R462 4.7K/4
CHIP_PWGD R390 1K/4
R374 X_4.7K/4

CPUTIN R385 X_1K/4

PWRBTIN R356 10K1%/4
C384 C0.1u16X/4

HM_VREF C391 4.7u6.3X/6

C388 10u6.3X/6 C406 1u6.3X/4
close to pin3

C396 10u6.3X/6 C370 1u6.3X/4
close to pin24

Thermal Monitor

For CPU Under Socket

HM_VREF R719 10K1%/4 CPUTIN
RT5 10KT1%/4 C684 C2200p50X/4 GNDHM

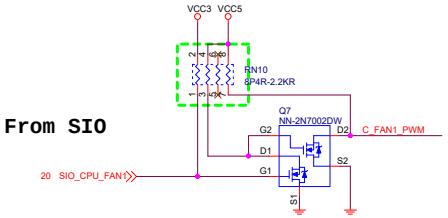
For System Close to SIO

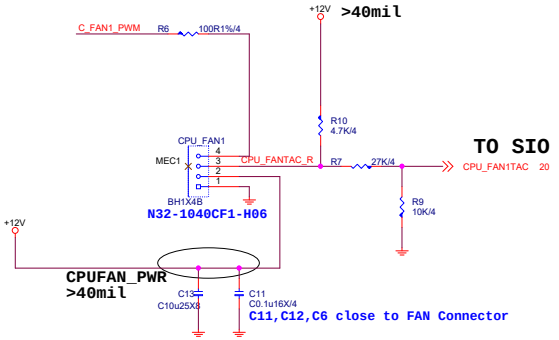
Q52 P-PMBS3907 SYSTIN
C379 2200p50X/4 GNDHM

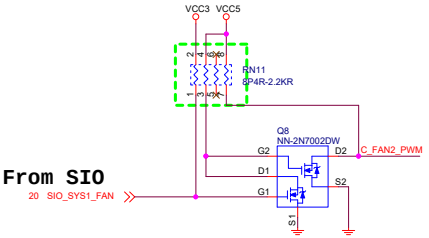
MSI MICRO-START INT'L CO.,LTD.

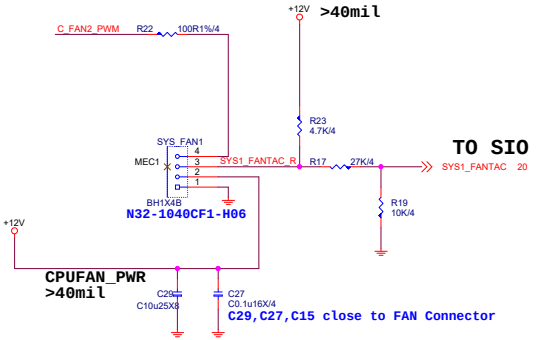
Title	SIO NCT5565	
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 20 of 50	

直拉FAN





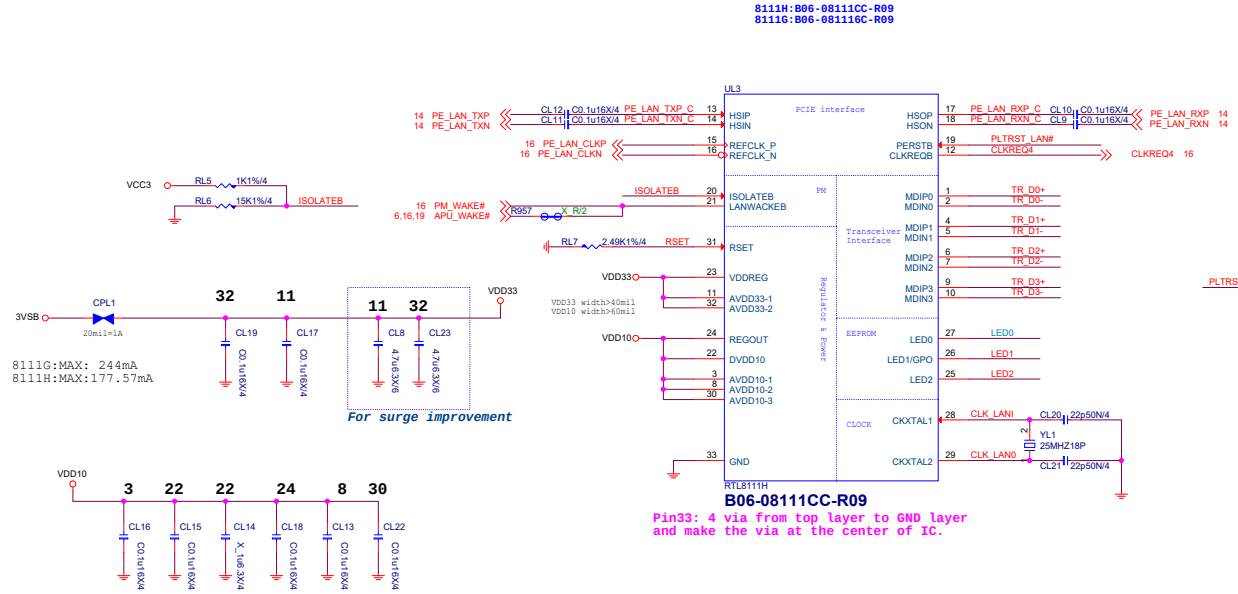




MSI MICRO-START INT'L CO.,LTD.

Title: CPU FAN Control		
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 21 of 50	

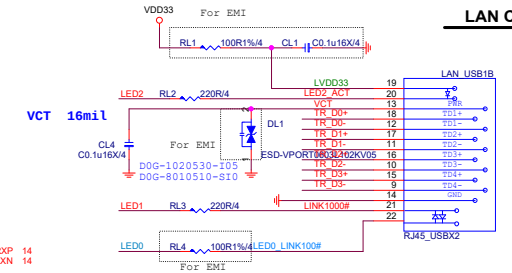
RTL8111G/RTL8111H Giga LAN

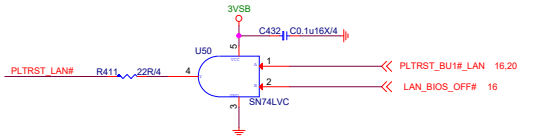


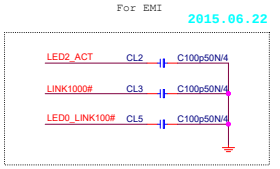
B06-08111CC-R09

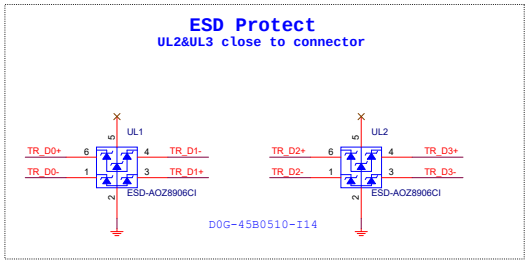
Pin33: 4 via from top layer to GND layer and make the via at the center of IC.

LAN Connector









8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

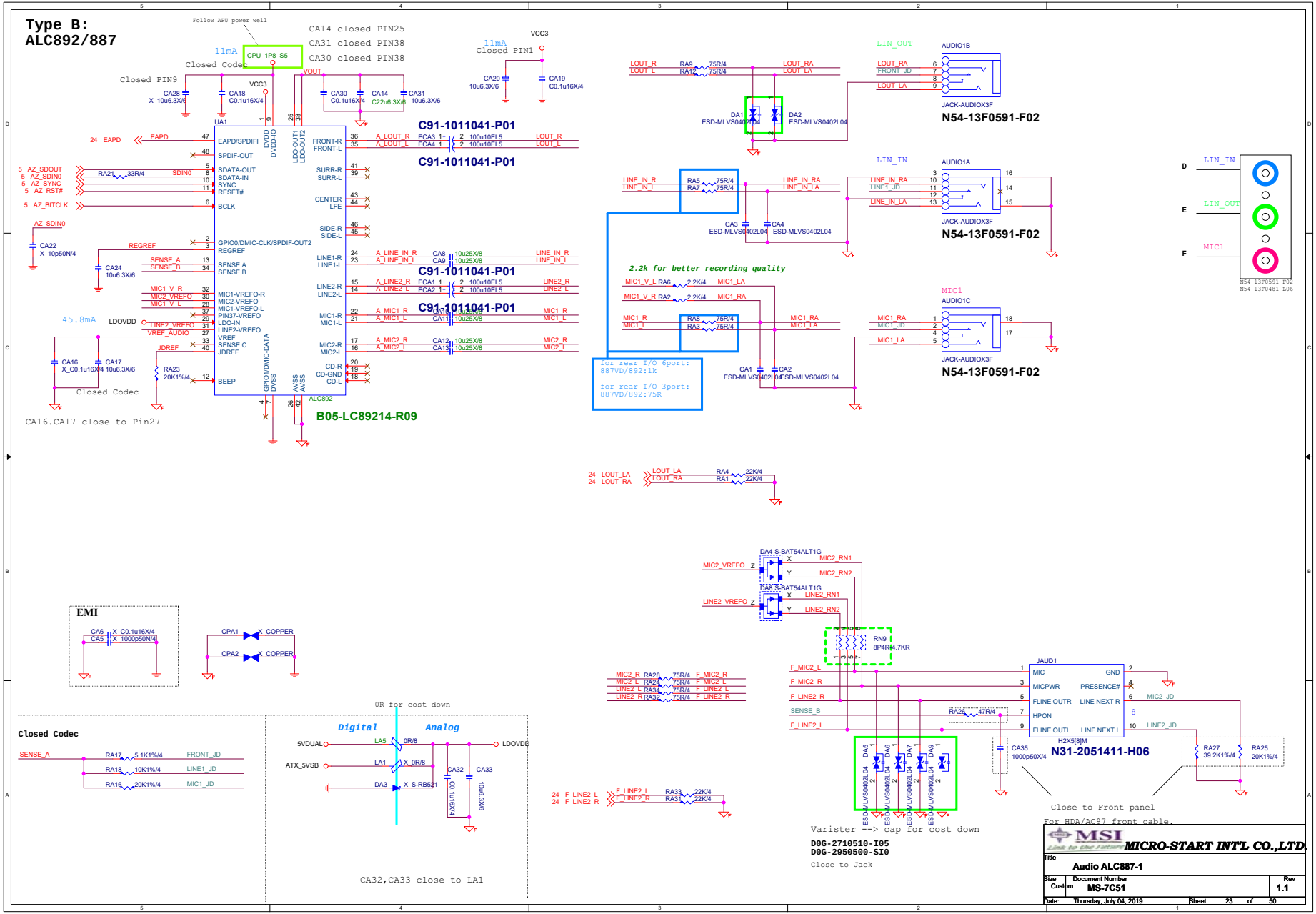
8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MSI Link for the Future **MICRO-START INT'L CO.,LTD.**

Title: LAN-RTL8111H		
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 22 of 50	

Type B:
ALC892/887

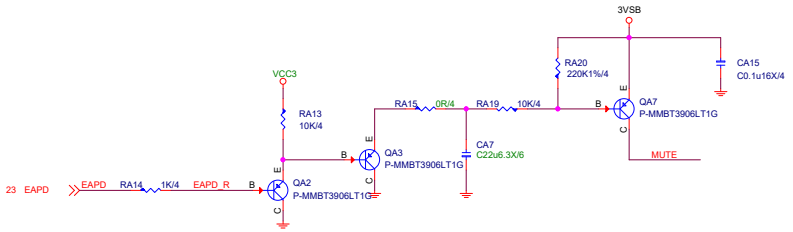


MICRO-START INT'L CO.,LTD.

Title	Audio ALC887-1		
Size: Custom	Document Number: MS-7C51		Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 23 of 50		

Rear Line OUT De-POP circuit

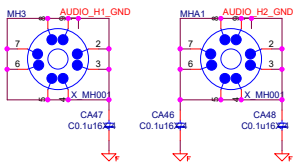
De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog

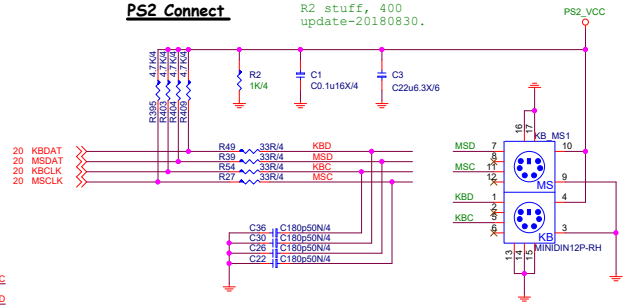
20181203 使用測光LED
Remove Audio LED,
RA73、RA71、RA72、RA74、RA75、RA76、LEDA4、LEDA2、LEDA3、LEDA6、LEDA5、LEDA7、QA4、QA5 unstuff.
20190426
Remove 預留線路

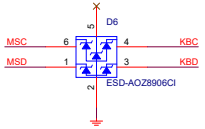


MSI Link for the Future **MICRO-START INT'L CO.,LTD.**

Title	Audio ALC887-2	
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 24 of 50	

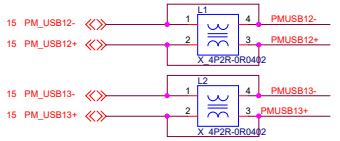
PS2

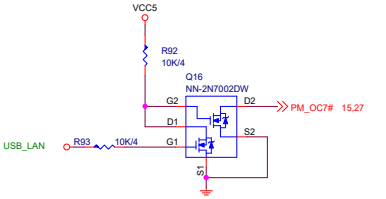


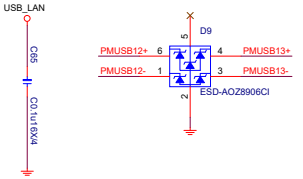


layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

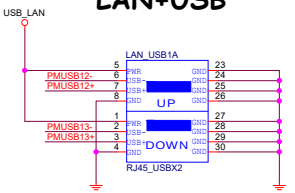
LAN USB2.0



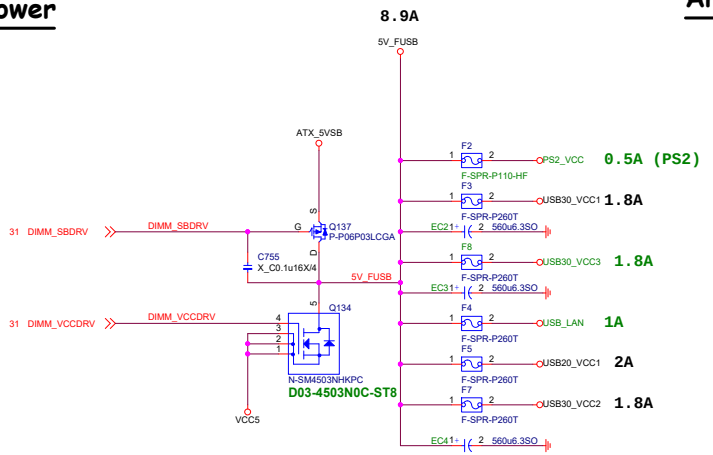


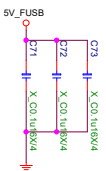


LAN+USB

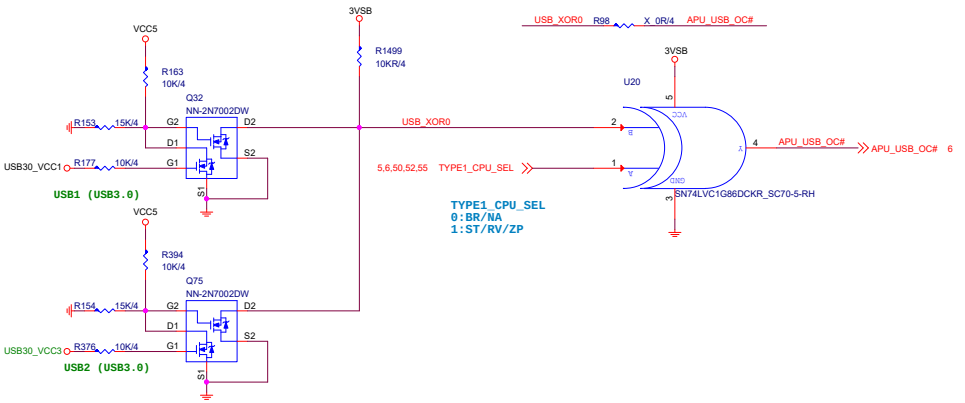


USB Power





APU_USB_OC



	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

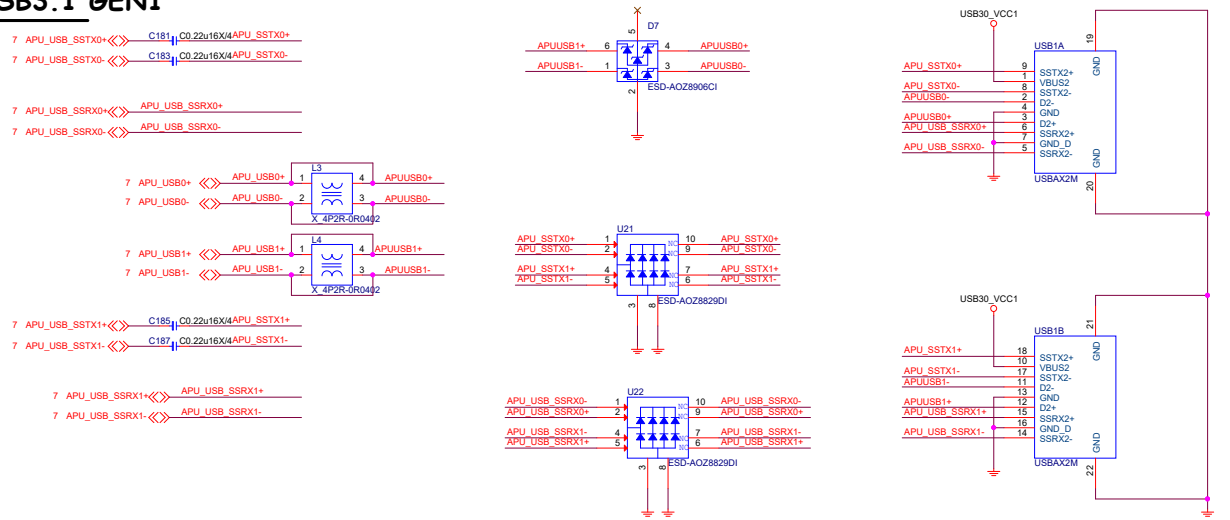
MSI MICRO-START INT'L CO.,LTD.

Title: USB Rear PS2+USB2.0

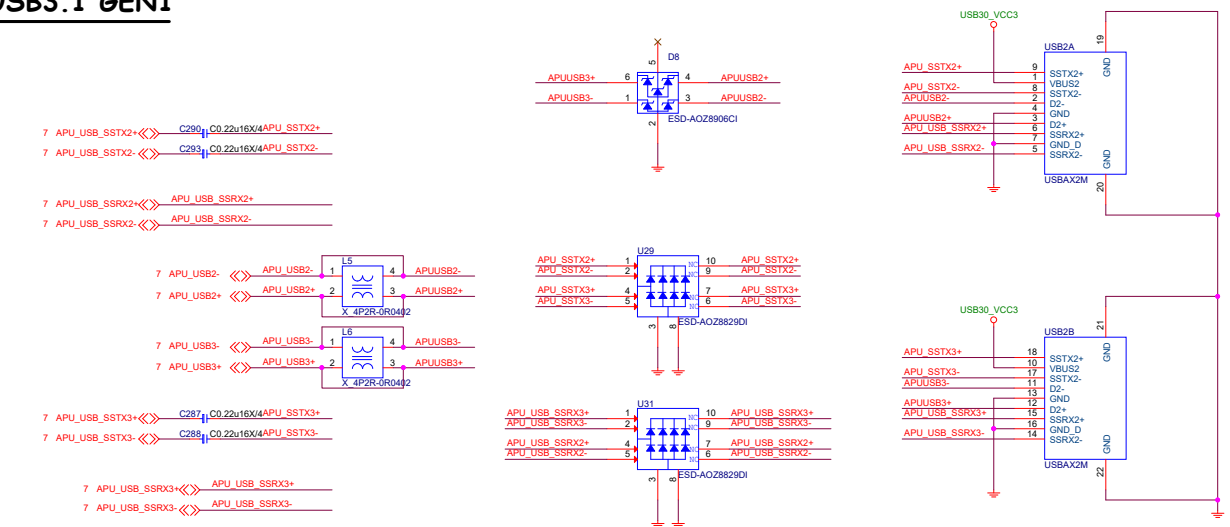
Size	Document Number	Rev
Custom	MS-7C51	1.1

Date: Thursday, July 04, 2019 Sheet 25 of 50

USB3.1 GEN1

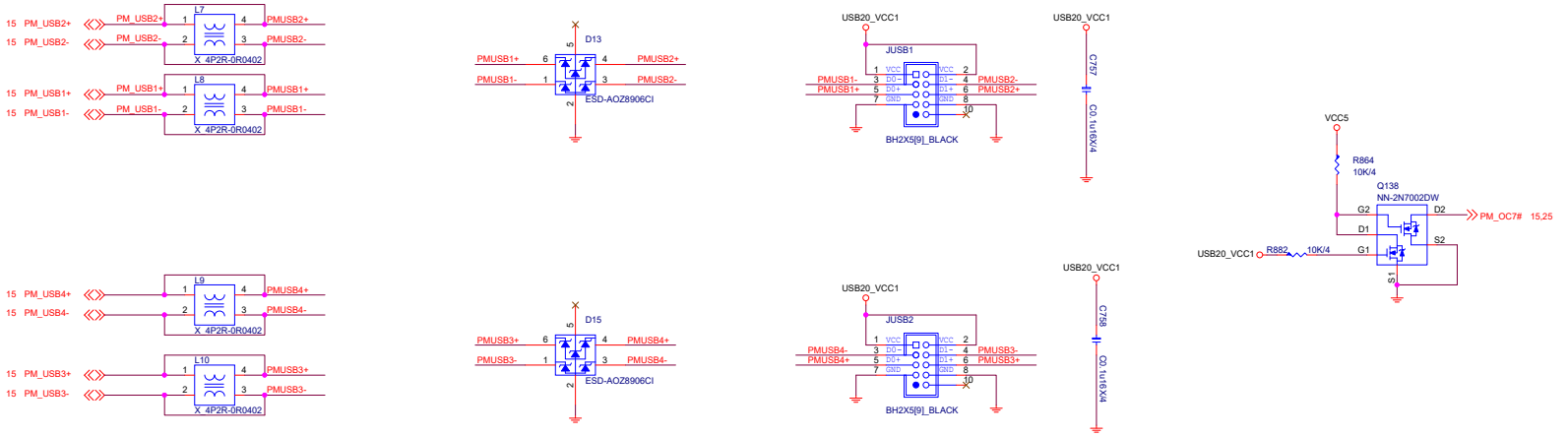


USB3.1 GEN1

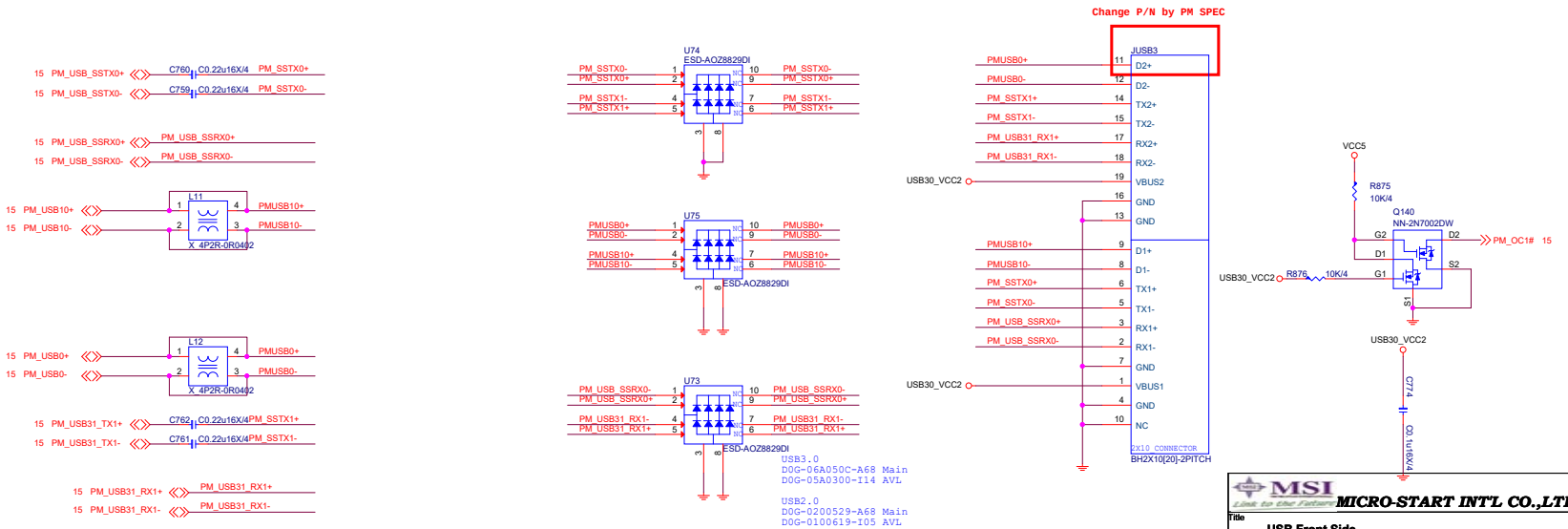


MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	USB Rear LAN+USB3.1 GEN1		
Size: Custom	Document Number: MS-7C51		Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 26 of 50		

Front USB2.0

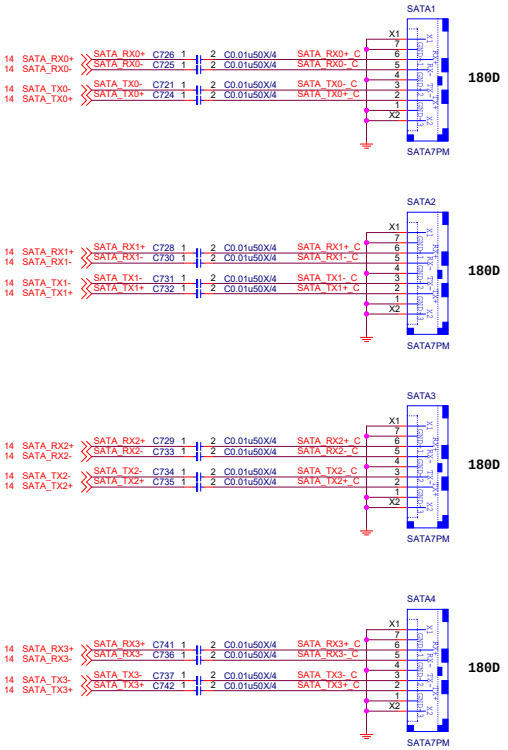


Front USB3.1 GEN1



MSI Link for the Future	MICRO-START INT'L CO.,LTD.		
Title: USB Front Side			
Size: Custom	Document Number: MS-7C51		Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 27 of 50		

SATA Connector

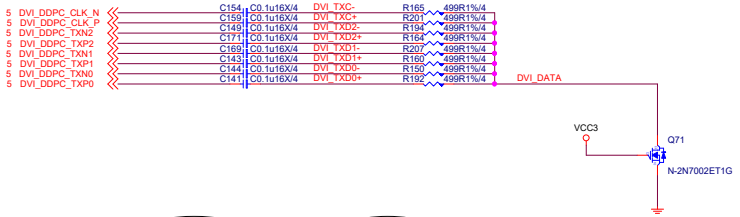


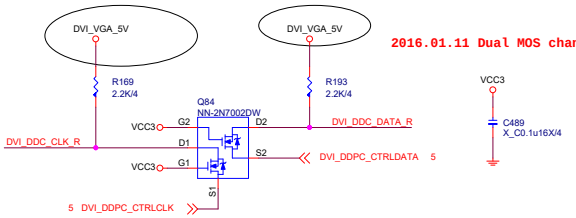
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: SATA Connector		
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 28 of 50	

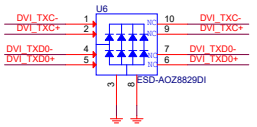
DVI level shifter

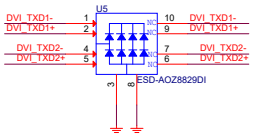
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

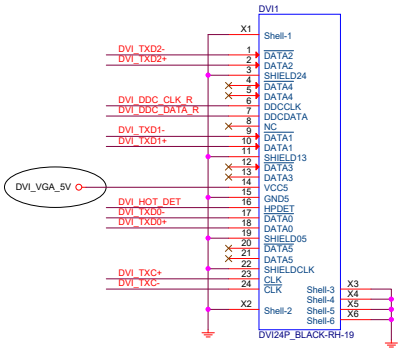


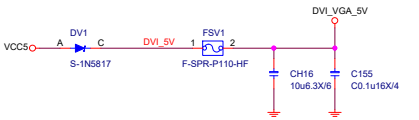


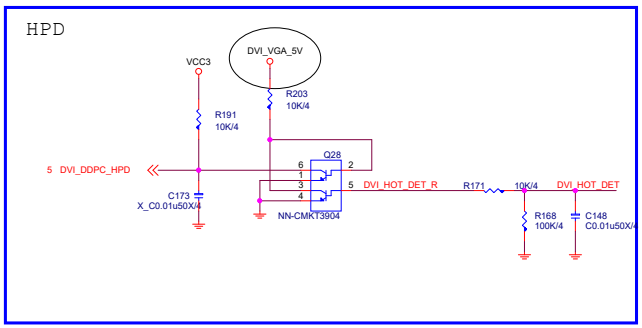
2016.01.11 Dual MOS change to single MOS,reduce CM noise by EMI Suggestion

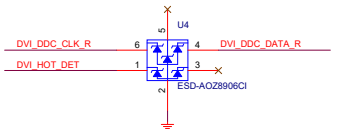


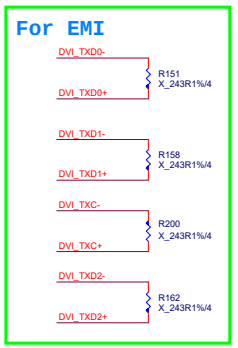


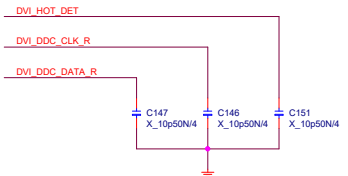










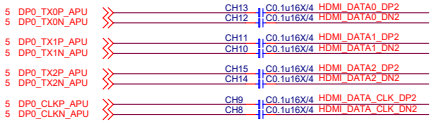


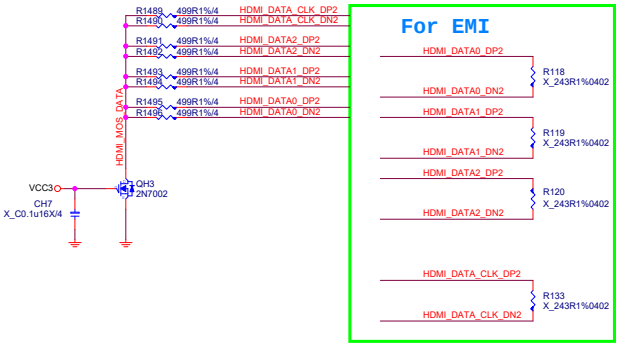
MICRO-START INT'L CO.,LTD.

Title: DVI Connector		
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 29 of 50	

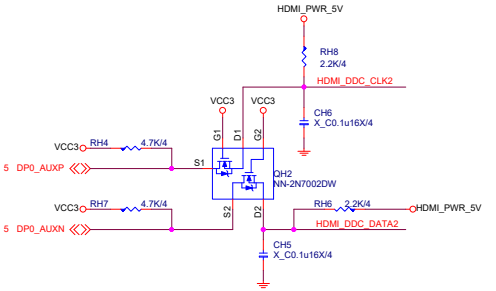
HDMI CONNECTOR

For HDMI 1.4

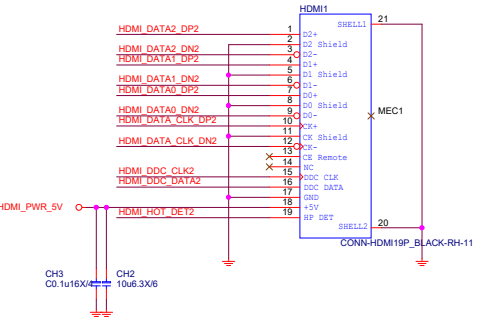




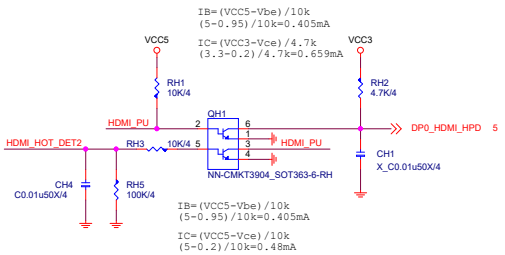
AUX Level Shifter



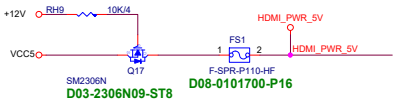
Connector



HPD Circuit



Connector Power

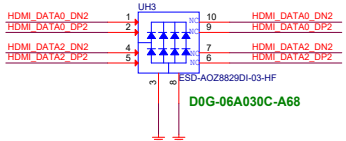


D03-2306N09-ST8

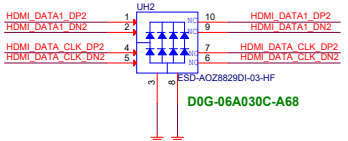
D08-0101700-P16

如果用DIODE SA測試電壓會不過

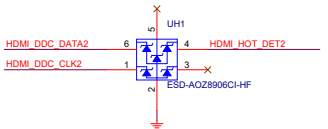
For EMI



D0G-06A030C-A68



D0G-06A030C-A68



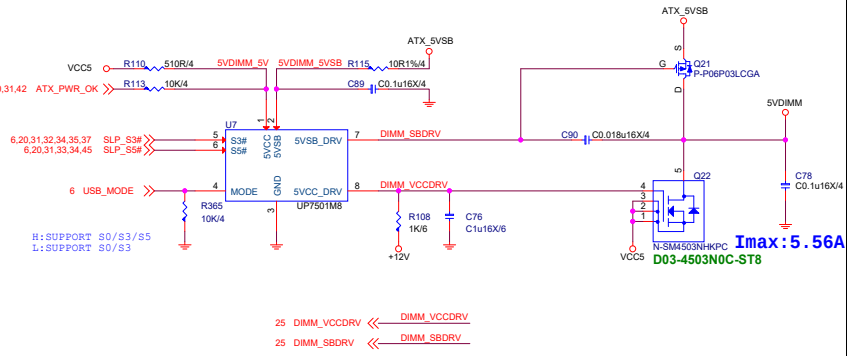
MSI MICRO-START INT'L CO.,LTD.

Title: DP to VGA ITE6516

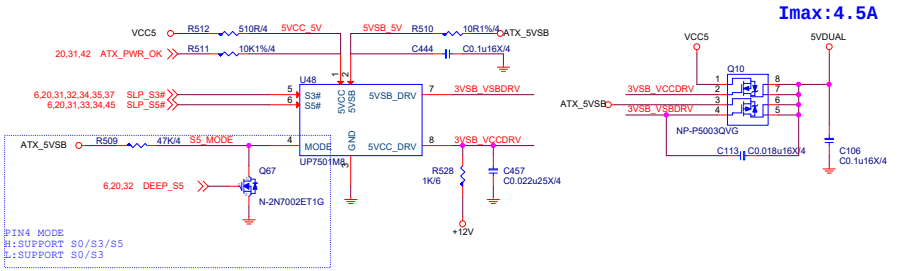
Size: Custom | Document Number: MS-7C51 | Rev: 1.1

Date: Thursday, July 04, 2019 | Sheet 30 of 50

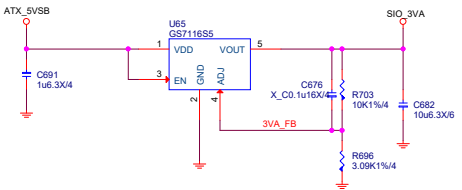
5VDIMM FOR DDR



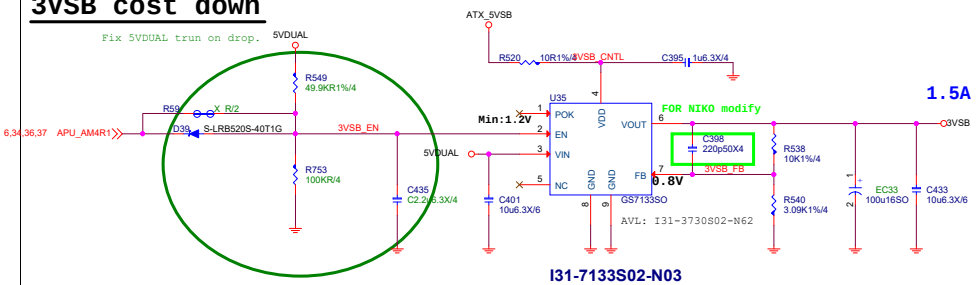
5VDUAL For 3VSB、CPU 1.8V 、 VDDP



SIO_3VA



3VSB cost down



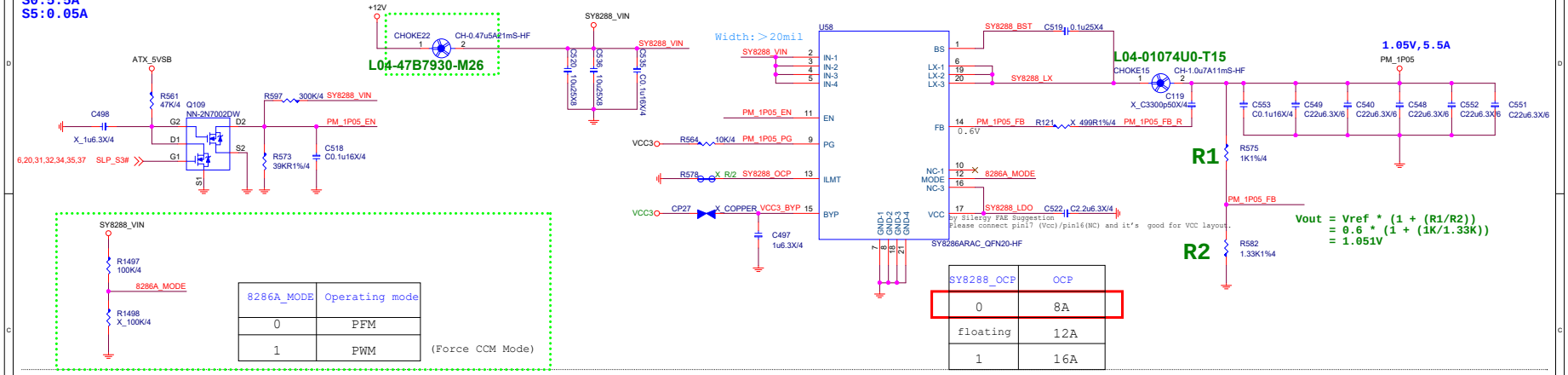
MSI
MICRO-START INT'L CO.,LTD.

Title	ACPI uPI-5VDIMM&3VSB	
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 31 of 50	

FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

Input Current= (5.5A*1.05V)/12V/0.8=0.6A



8286A_MODE	Operating mode
0	PFM
1	PWM

(Force CCM Mode)

SY8288_OCP	OCP
0	8A
floating	12A
1	16A

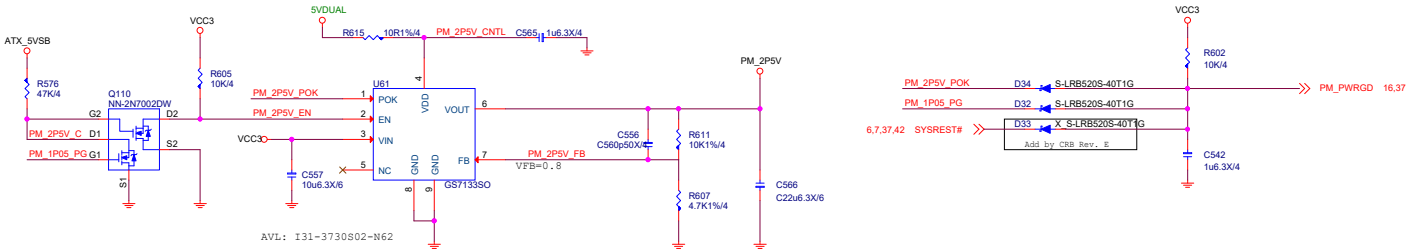
FOR Promontory 1.05V_S5

0.05A

PM_1P05_S5改用CPU_VDDP_S5

Promontory-2.5V

2.5V; 900mA



MSI MICRO-START INT'L CO.,LTD.

Title: Promontory-NB685GQ-1.05V/GS7133-2.5V

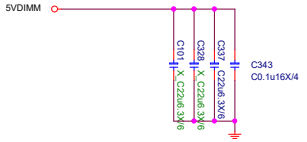
Size	Document Number	Rev
Custom	MS-7C51	1.1

Date: Thursday, July 04, 2019 Sheet 32 of 50

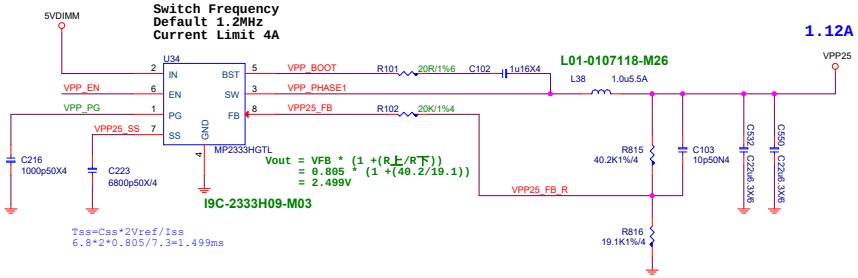
2DIMM :1.12A FOR DDR VPP2.5V

Iin lim=IOCP*Vout/0.8/Vin
=4A*2.5V/0.8/5V=2.5A

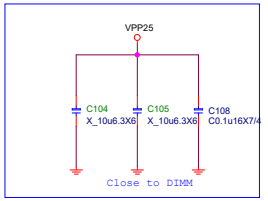
Input Current= Iout*Vout/0.8/Vin
= 1.12A*2.5V/0.8/5V=0.7A

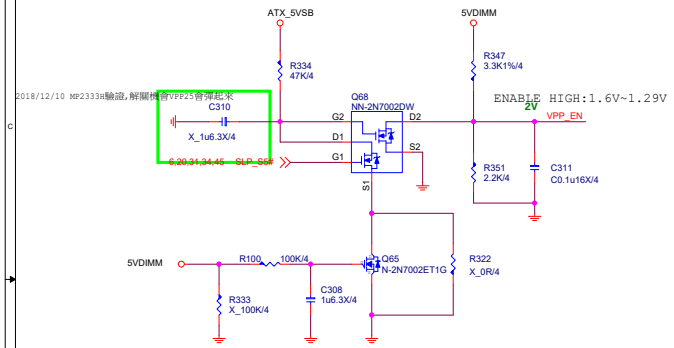


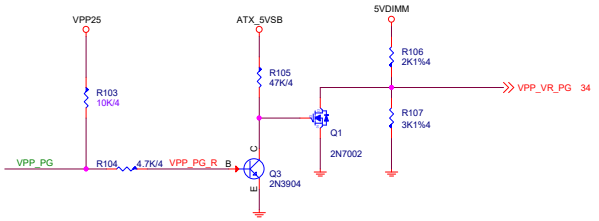
Switch Frequency
Default 1.2MHz
Current Limit 4A



1.12A







IB=(VPP25-Vbe)/14.7K
(2.5-0.95)/14.7K=0.105mA
IC=(ATX_5VSB-Vce)/47K
(5-0.2)/47=0.102mA
IB*hfe*0.4=0.105mA*12*0.4=0.504mA>IC=0.102mA

MSI MICRO-START INT'L CO.,LTD.

Title: DDR PWR VPP25/VTT-MP2143

Size	Document Number	Rev
Custom	MS-7C51	1.1

Date: Thursday, July 04, 2019 Sheet 33 of 50

DDR4_1.2V 15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU

4.75A FOR 2DIMM

0.6A FOR DDR VTT

R178: 280K，OCP實測28.8A.

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

L04-22B7700-T15

VID	Reference Voltage (V)
H	0.675
L	0.75

2V

f:400KHz

By layout modify

OCP:27.5A

Imax: 20.85A

Rd(on)=5.1m, OCP:27.45A

FB:0.75V

I32-8231A0C-R11

Close to PIN19

20181031
VCC_DDR由上2下2改成上1下1.

MAX:20.85A

1.2V

0.1uFx1 per dimm

D03-4337N0C-ST8

D03-4503N0C-ST8

L04-11A7331-T15

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K

MSI	MICRO-START INT'L CO.,LTD.	
Title: DDR Power-RT8231AGQW		
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 34 of 50	

FOR CPU 1.8V S5

0.5A

FOR VCCP_SOC_S5

0.9A

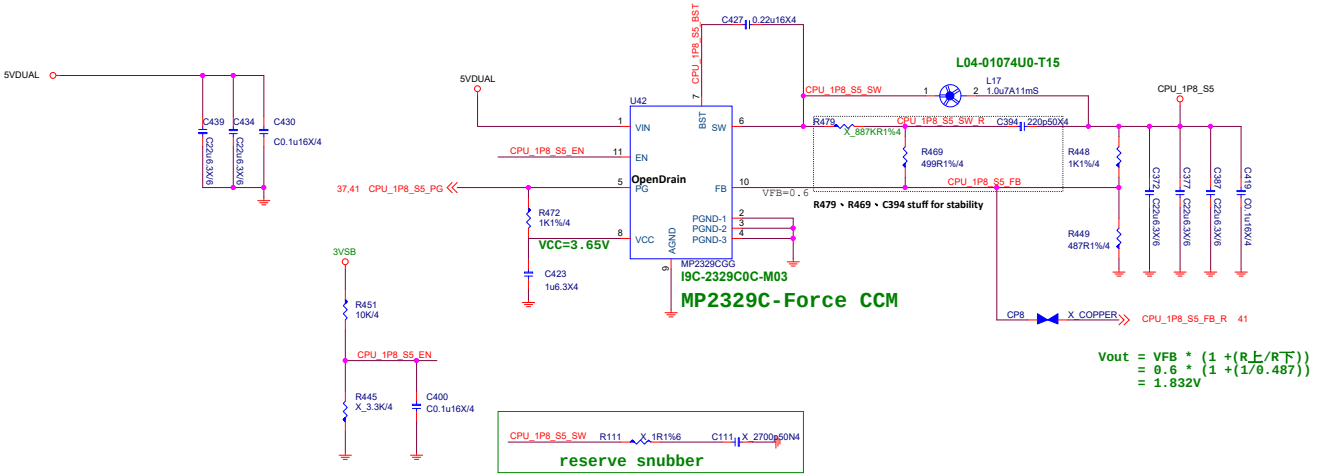
FOR CPU 1.8V S0

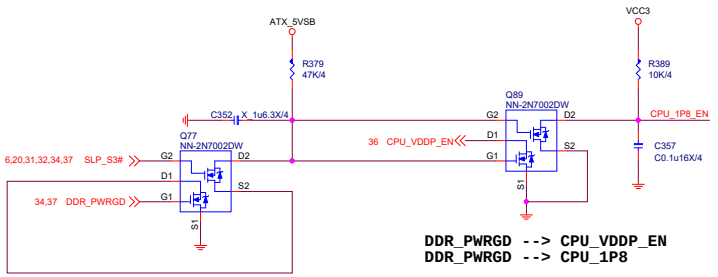
2.0A

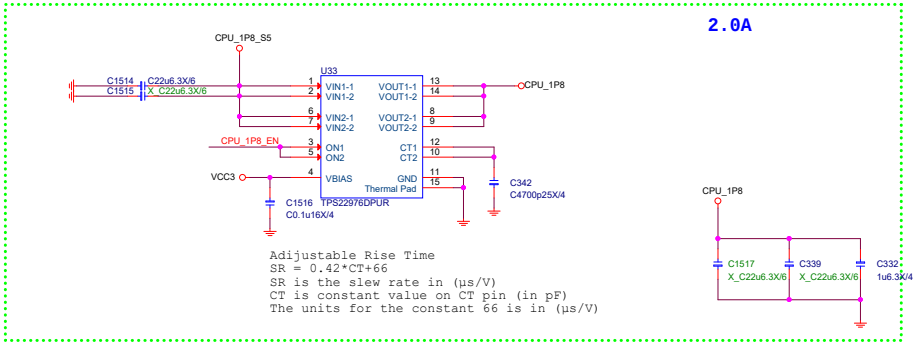
0.5A + 2.0A + 0.9A =3.4A

0.5A + 2.0A + 0.9A =3.4A

FOR CPU_VDDP_S5





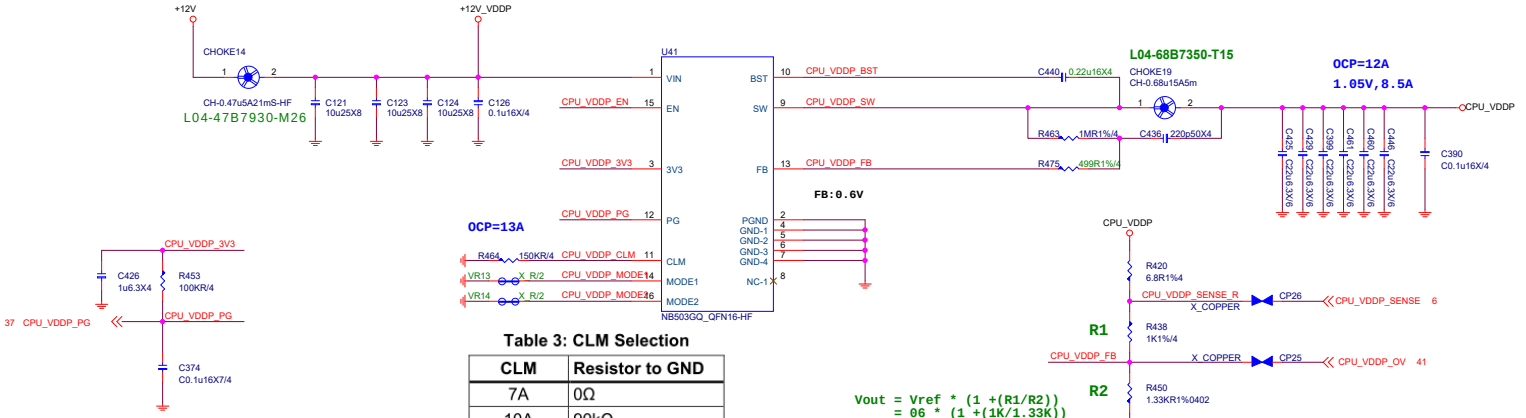


MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	CPU Power 1P8V-MP2147	
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 35 of 50	

CPU_VDDP_S0

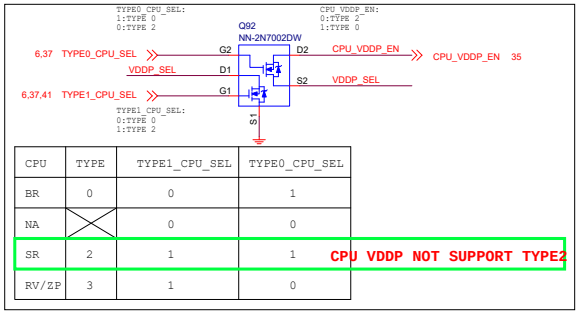
1.05V/0.9
S0:8.5A



Vout = Vref * (1 +(R1/R2))
= 06 * (1 +(1K/1.33K))
= 1.0511V

Table 3: CLM Selection

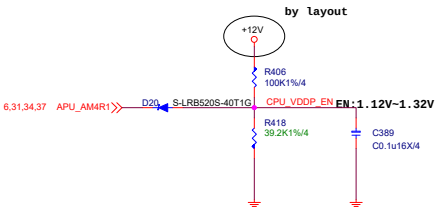
CLM	Resistor to GND
7A	0Ω
10A	90kΩ
13A	150kΩ
16A	>230kΩ or float



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

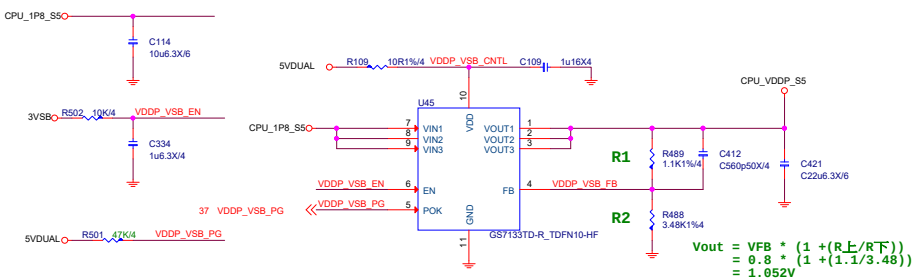
by layout



reserve snubber

CPU_VDDP_S5

VDDP_S5 1.05V
S5:1A

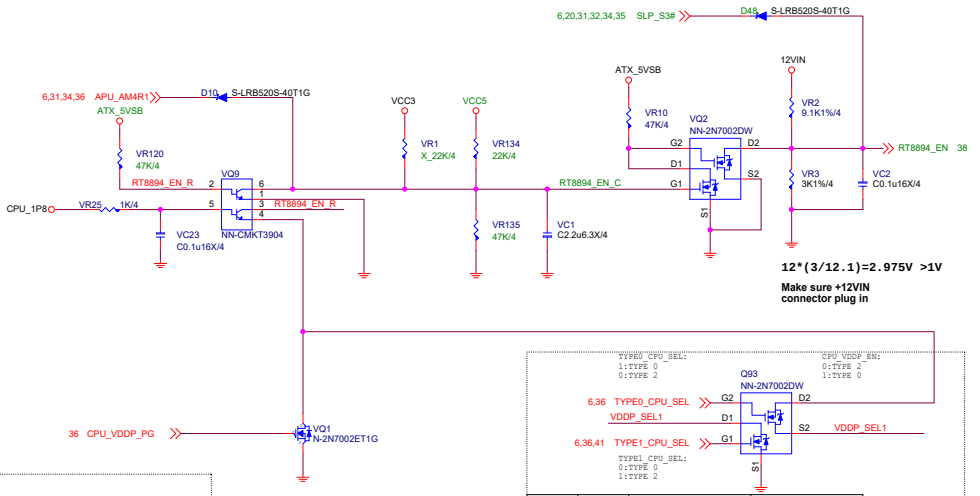


Vout = VFB * (1 +(R上/R下))
= 0.8 * (1 +(1.1/3.48))
= 1.052V

MSI Link for the Future
MICRO-START INT'L CO.,LTD.

Title	CPU Power VDDP-RT8125E	
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 36 of 50	

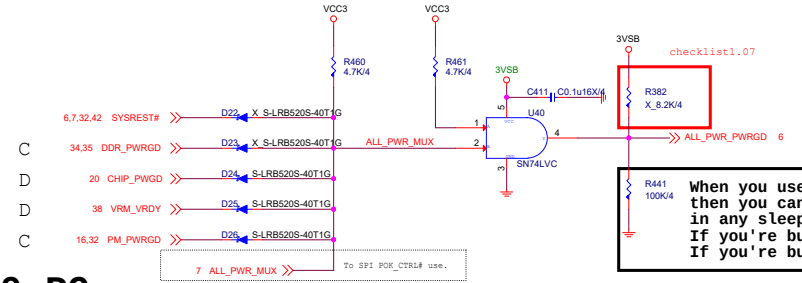
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

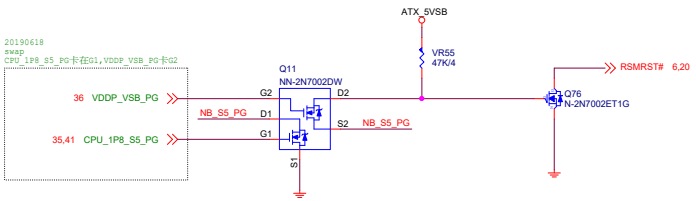


R441 100K/4

When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

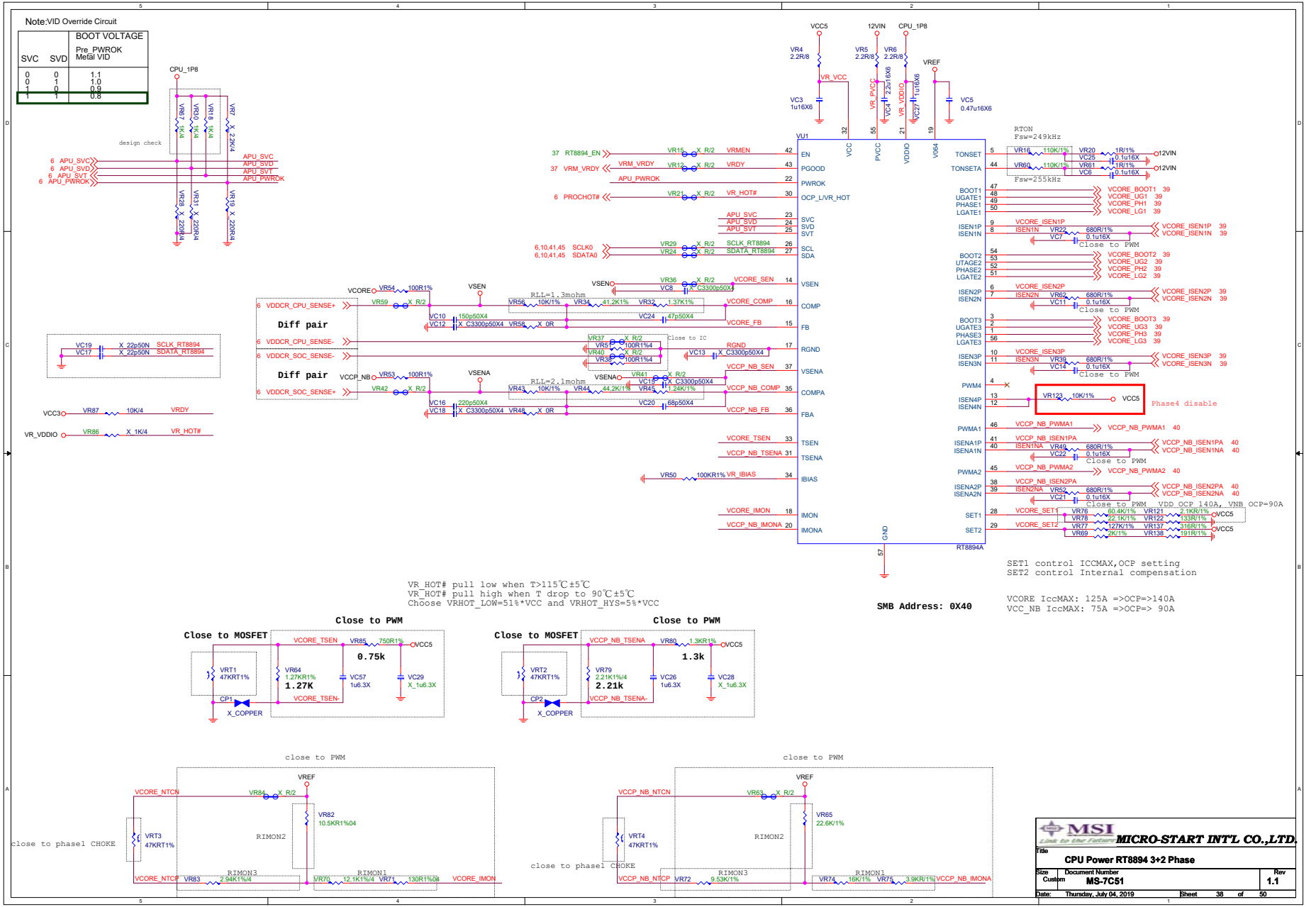
S5 PG



MSI Link for the Future	MICRO-START INT'L CO.,LTD.		
Title	CPU PWR-IR3599		
Size: Custom	Document Number: MS-7C51		Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 37 of 50		

Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



MICRO-START INT'L CO.,LTD.

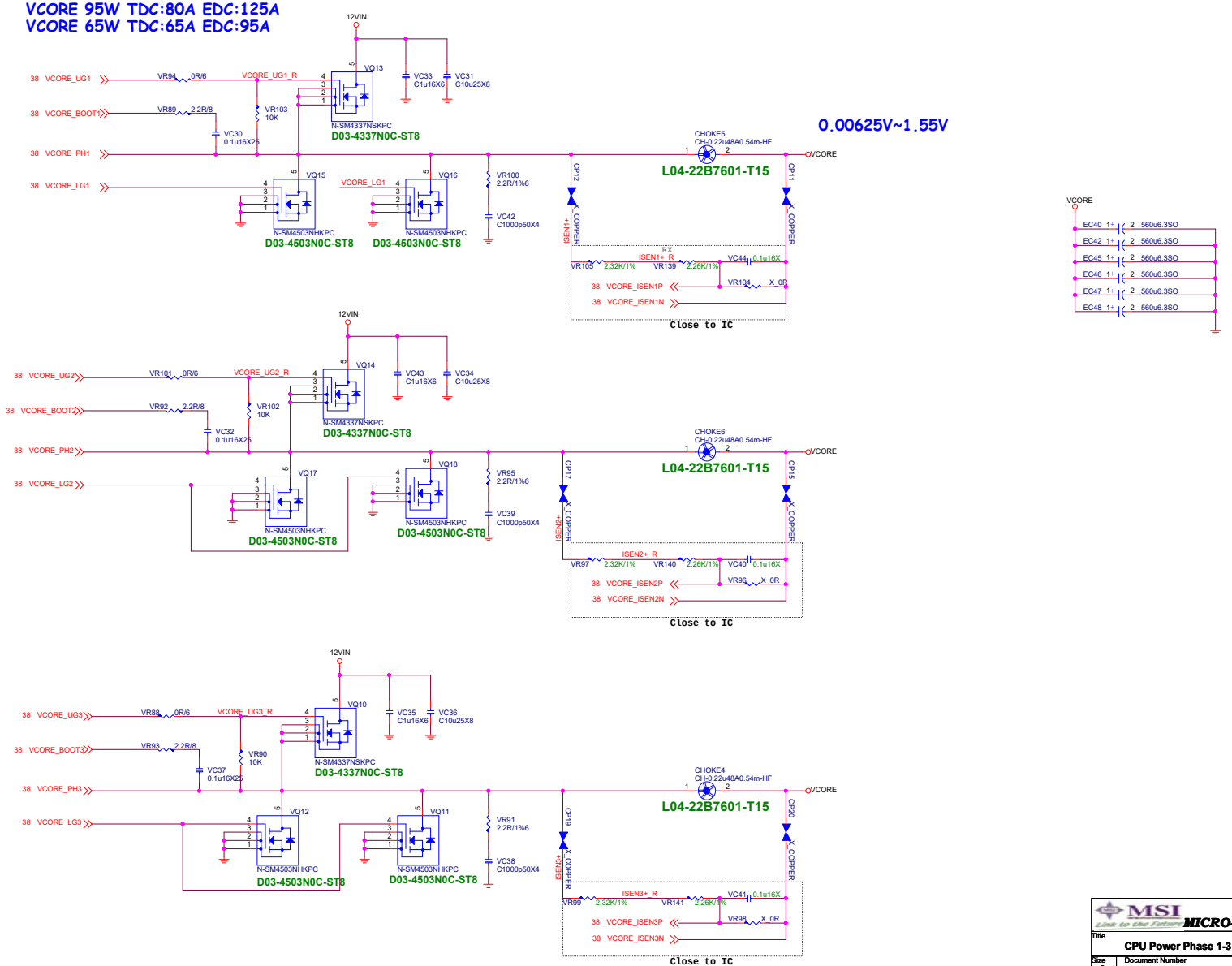
Title: CPU Power RT8894 3+2 Phase

Size	Document Number	Rev
Custom	MS-7C51	1.1

Date: Thursday, July 04, 2019 Sheet 38 of 50

VCORE 105W TDC:95A EDC:140A
VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A

0.00625V~1.55V



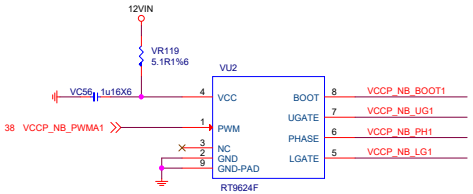
MSI Link to the Future MICRO-START INT'L CO.,LTD.

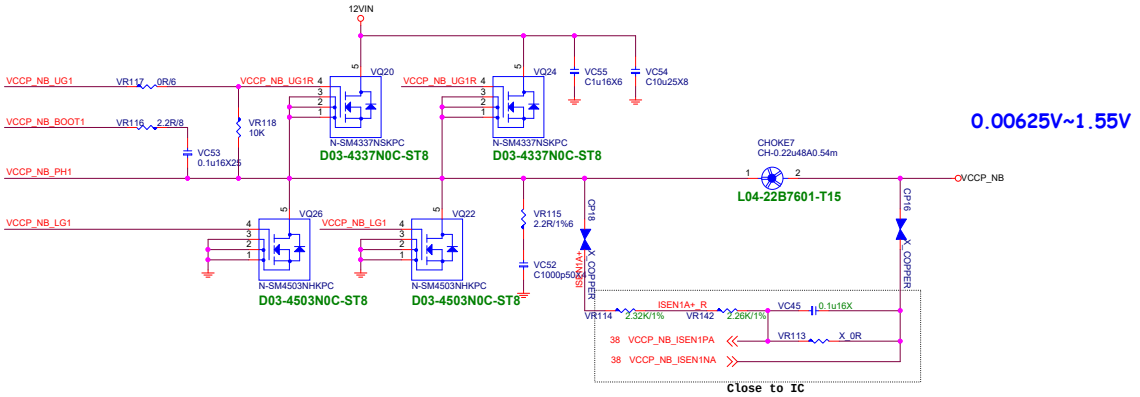
Title: CPU Power Phase 1-3

Size	Document Number	Rev
Custom	MS-7C51	1.1

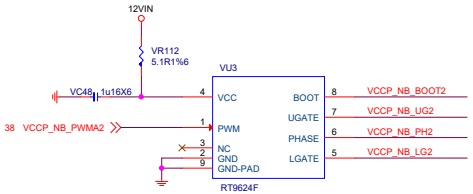
Date: Thursday, July 04, 2019 Sheet 39 of 50

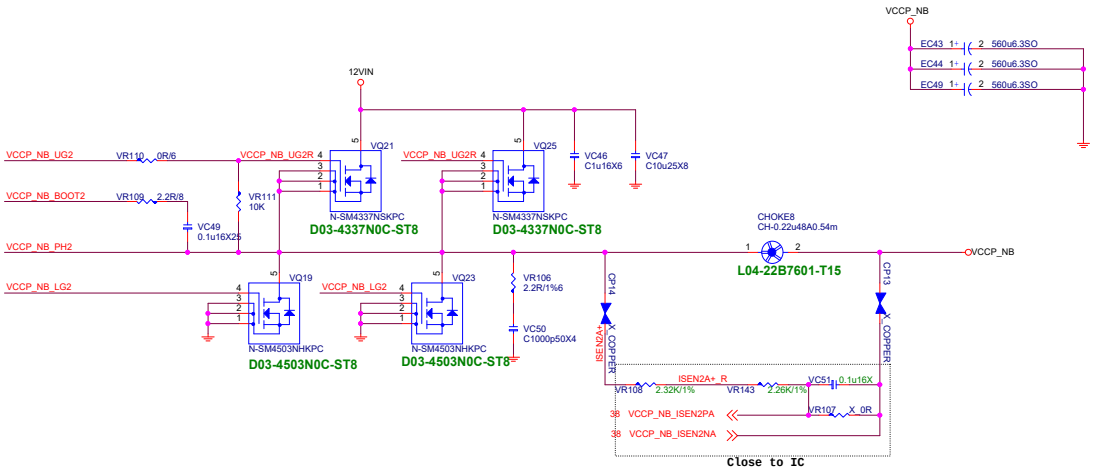
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A





0.00625V~1.55V





MSI MICRO-START INT'L CO.,LTD.

Title	CPU Power NB Phase 1-2	
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 40 of 50	

FOR VCCP_SOC_s5

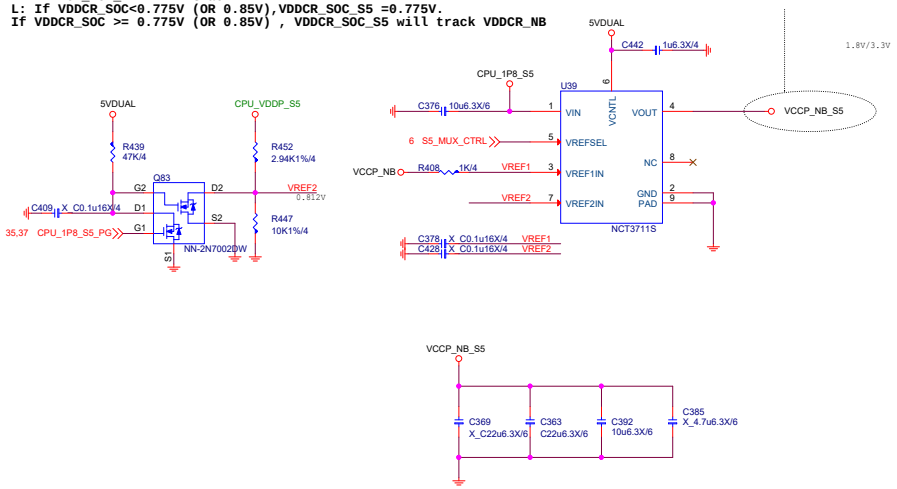
0.9A

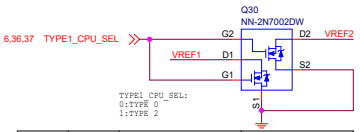
TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)Bristol Ridge TYPE0



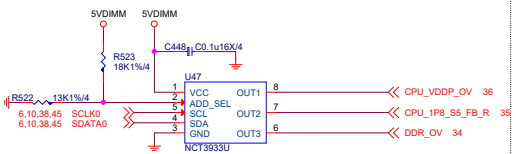


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

Over Voltage Control IC

0x26:RH=18K,RL=13K



除非超壓對功能有任何幫助，否則不上NCT3933與開超壓選項

0x20:RH=10K,RL=OPEN

0x2A:RH=OPEN,RL=10K

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

MSI Link for the Future MICRO-START INT'L CO.,LTD.

Title: CPU Power NB Switch / NCT3933 OV

Size: Custom | Document Number: MS-7C51 | Rev: 1.1

Date: Thursday, July 04, 2019 | Sheet 41 of 50

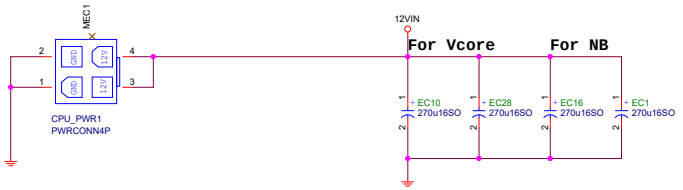
uP6273 CURRENT SENSE

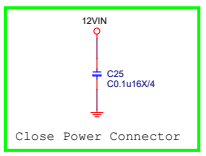
CPU POWER CONNECTOR

uP6273 CURRENT SENSE

VCORE EDC MAC 125A

NB EDC MAX75A





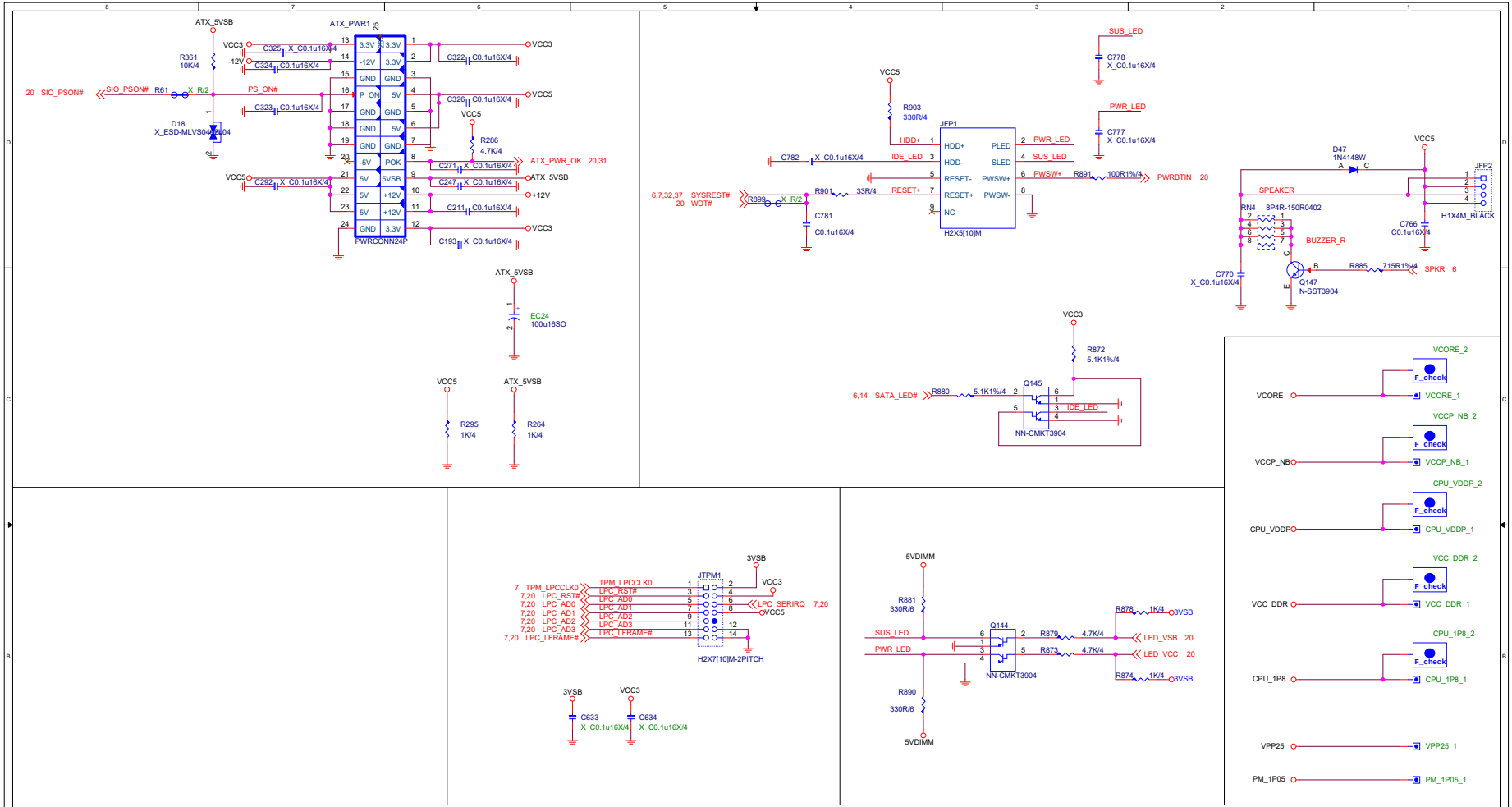
Irms = Iout * SQRT{D/N- (D)^2]}

CORE:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=3
=125A*SQRT(0.0388-0.0136)
=19.8A

NB:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=2
=75A*SQRT(0.0583-0.0136)
=15.8A

MICRO-START INT'L CO.,LTD.

Title: uP6273 CURRENT SENSE		
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 42 of 50	



MSI
Link for the Future
MICRO-START INT'L CO.,LTD.

Title	ATX/Front Panel	
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 43 of 50	

EZ Debug LED

LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED Control by SIO

1.0 SPEC Removed

DDR LED

Removed P/N by PM SPEC

PCI Express LED Control

Removed P/N by PM SPEC

LED	x16	x8	x4
PCIE2	Red	White	White

LED \ GPIO	EGPIO95	EGPIO96
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

AM4 APU Detect LED Circuit

Removed GPU_LED1 by PM SPEC
2019/06/24

iGPU GPU_LED1 OFF
dGPU GPU_LED1 Always ON

Bottom LED

Removed P/N by PM SPEC

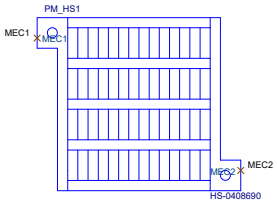
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: ALL LED Control

Size: Custom | Document Number: MS-7C51 | Rev: 1.1

Date: Thursday, July 04, 2019 | Sheet 44 of 50

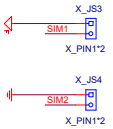
HEAT SINK



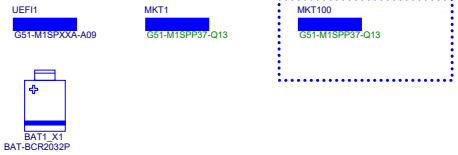
CPU Socket

E95-0000022-C22

Simulation

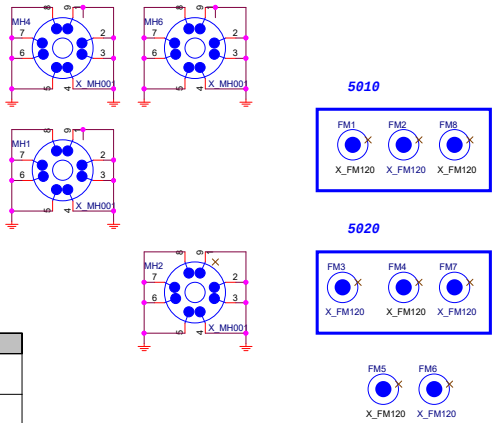


MANUAL PART



PK0-07C5111-G37,精成
PK0-07C5111-E48,競華

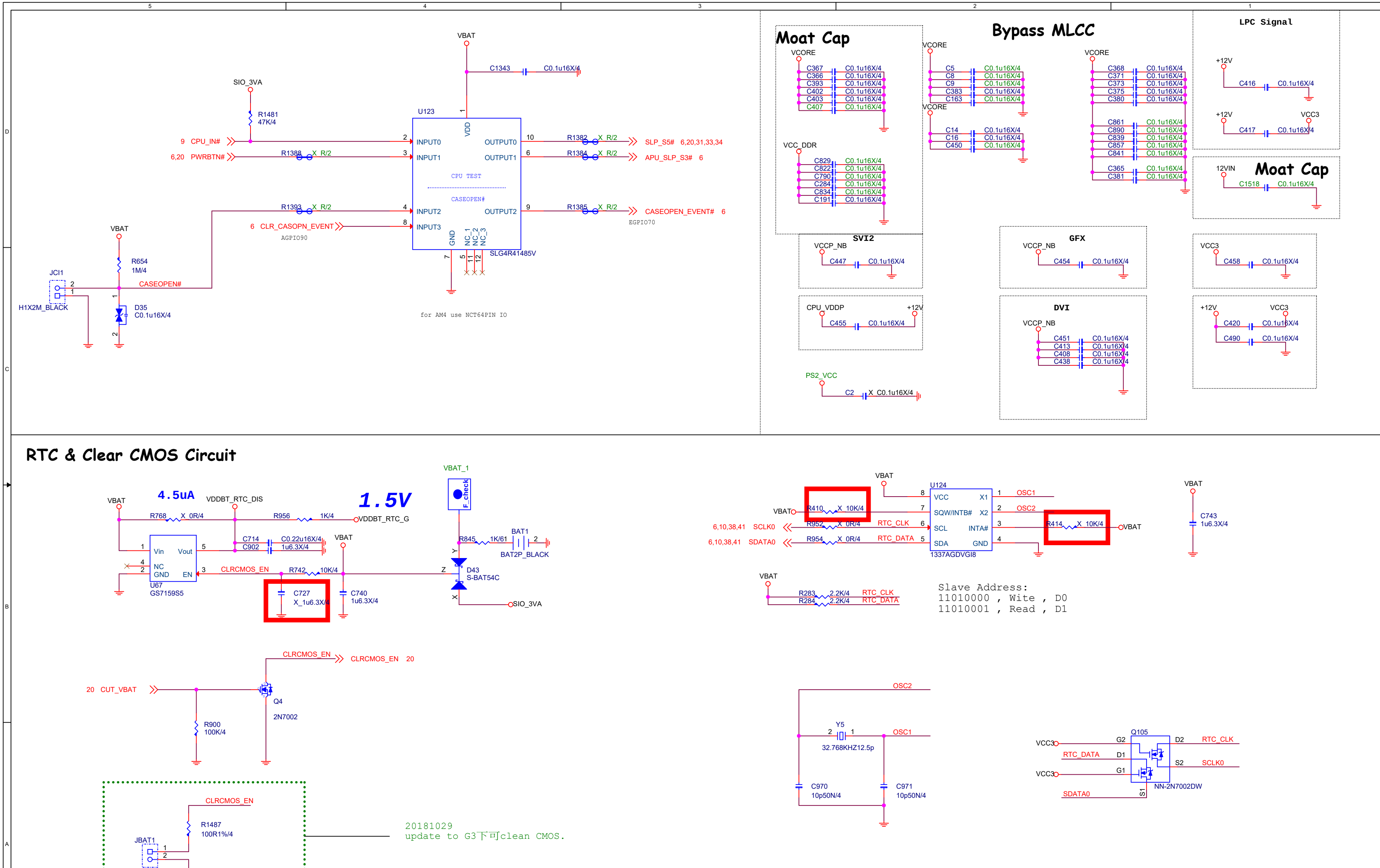
Optics Orientation Holes



OPT	Configure	BOM	Function

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: BOM OPTION		
Size: Custom	Document Number: MS-7C51	Rev: 1.1
Date: Thursday, July 04, 2019	Sheet 45 of 50	



Moat Cap
Bypass MLCC
LPC Signal
Moat Cap
SVI2
GFX
DVI
VCORE
VCC_DDR
VCCP_NB
CPU_VDDP
PS2_VCC
+12V
VCC3
12VIN
VBAT
SIO_3VA
U123
SLG4R41485V
INPUT0
INPUT1
INPUT2
INPUT3
OUTPUT0
OUTPUT1
OUTPUT2
CPU TEST
CASEOPEN#
9 CPU_IN#
6,20 PWRBTN#
6 CLR_CASOPN_EVENT
AGPIO90
SLP_S5# 6,20,31,33,34
APU_SLP_S3# 6
CASEOPEN_EVENT# 6
EGPIO70
for AM4 use NCT64PIN IO
JCI1
H1X2M_BLACK
R654
1M/4
D35
C0.1u16X/4
R1481
47K/4
C1343
C0.1u16X/4
RTC & Clear CMOS Circuit
4.5uA
1.5V
VDDBT_RTC_DIS
VDDBT_RTC_G
VBAT_1
F_check
U67
GS7159S5
CLRCMOS_EN
BAT1
BAT2P_BLACK
D43
S-BAT54C
C727
X_1u6.3X/4
C740
1u6.3X/4
20 CUT_VBAT
CLRCMOS_EN 20
Q4
2N7002
R900
100K/4
R1487
100R1%/4
JBAT1
H1X2M_BLACK
20181029
update to G3下可clean CMOS.
U124
1337AGDVGI8
VCC
SQW/INTB#
SCL
SDA
X1
X2
INTA#
GND
OSC1
OSC2
RTC_CLK
RTC_DATA
6,10,38,41 SCLK0
6,10,38,41 SDATA0
R410 X_10K/4
R414 X_10K/4
C743
1u6.3X/4
R283 2.2K/4
R284 2.2K/4
Slave Address:
11010000 , Wite , D0
11010001 , Read , D1
Y5
32.768KHZ12.5p
C970
10p50N/4
C971
10p50N/4
Q105
NN-2N7002DW

MICRO-START INT'L CO.,LTD.

Title: RTC Circuit

Size: Custom | Document Number: MS-7C51 | Rev: 1.1

Date: Thursday, July 04, 2019 | Sheet 46 of 50