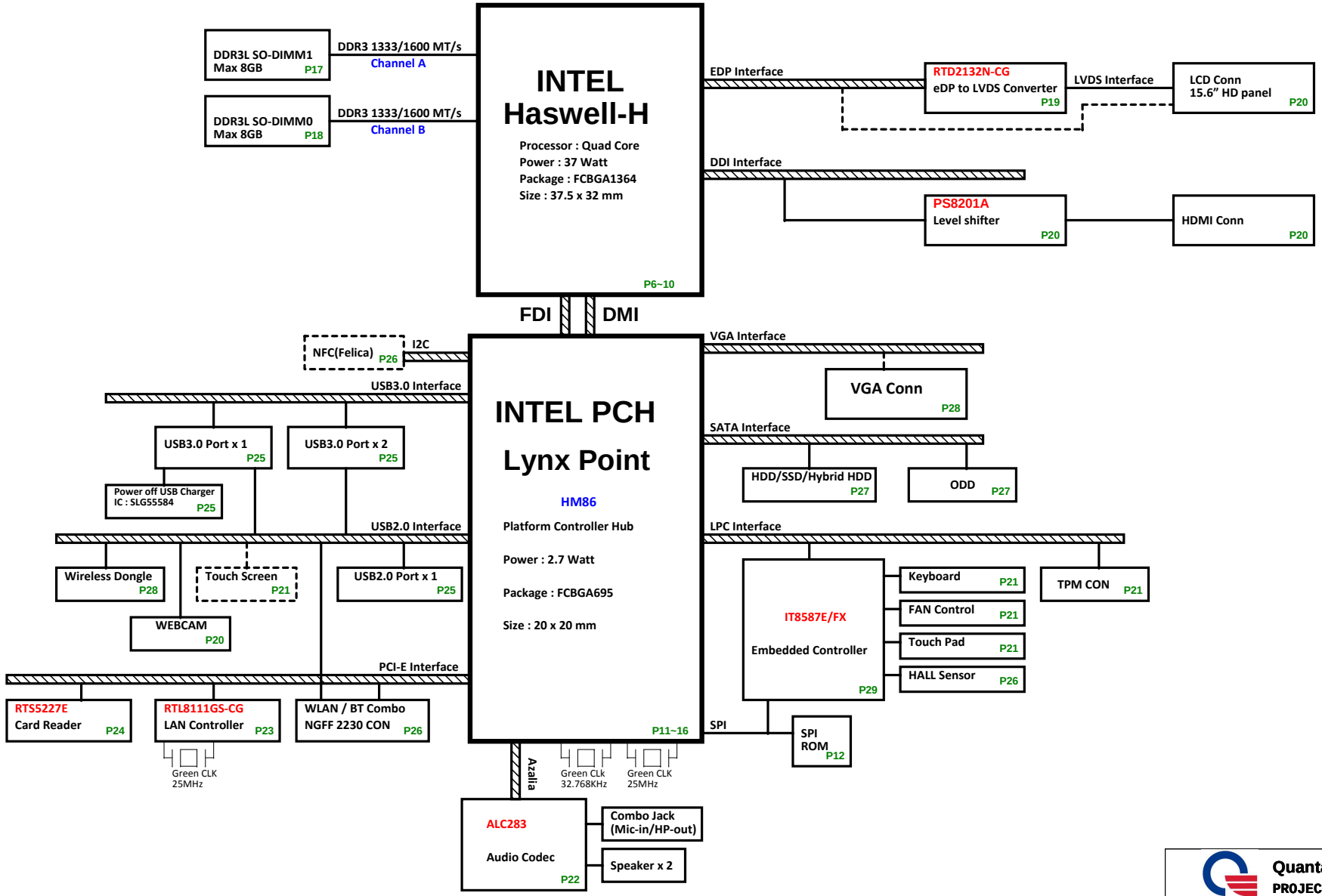
FH8A UMA (15.6") Haswell-H Platform Block Diagram

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Quanta Computer Inc.
PROJECT : FH8A

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Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
3V_RTC	3V	ON	ON	ON	ON	ON	
VIN	19V	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in
5V_S5	5V	ON	ON	ON	ON	OFF	S5_ON
3V_S5	3.3V	ON	ON	ON	ON	OFF	S5_ON
1.35V_S3	1.35V	ON	ON	OFF	OFF	OFF	S3_ON
5V_S3	5V	ON	ON	OFF	OFF	OFF	S3_ON
3VDUAL_LAN	3.3V	ON	OFF	OFF	OFF	OFF	LAN_ON_EC
3V_WLAN	3.3V	ON	ON	ON	ON	OFF	S5_ON
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON_2
3V_S0	3.3V	ON	OFF	OFF	OFF	OFF	S0_ON_2
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON_2
1.05V_S0	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_1
1.05V_VCCST	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_1
DDR_VTERM	0.675V	ON	OFF	OFF	OFF	OFF	S0_ON_1
VCC_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON

Function list

USB2		PCIE		Display		USB3		SATA	
Port 0	Co-lay USB3.0	Port 1	USB3.0 Conn	Port A	LVDS or eDP	Port 1	USB3.0 Conn	Port 0	NC
Port 1	Co-lay USB3.0	Port 2	NC	Port B	HDMI	Port 2	USB3.0 Conn	Port 1	NC
Port 2	Co-lay USB3.0	Port 3	GLAN	Port C	NC	Port 3	USB3.0 Conn	Port 2	NC
Port 3	Wireless Dongle	Port 4	NC	Port D	NC	Port 4	NC	Port 3	NC
Port 4	NC	Port 5	Card Reader			Port 5	NC	Port 4	HDD
Port 5	NC	Port 6	WLAN			Port 6	NC	Port 5	ODD
Port 6	NC	Port 7							
Port 7	NC	Port 8							
Port 8	Blue Tooth								
Port 9	USB2.0 Conn								
Port 10	NC								
Port 11	Camera								
Port 12	Touch screen								
Port 13	NC								

Function Select

N@	NFC
L@	RTD2132N-CG
E@	Internal eDP
M@	MMB
TS@	Touch screen
C@	CRT

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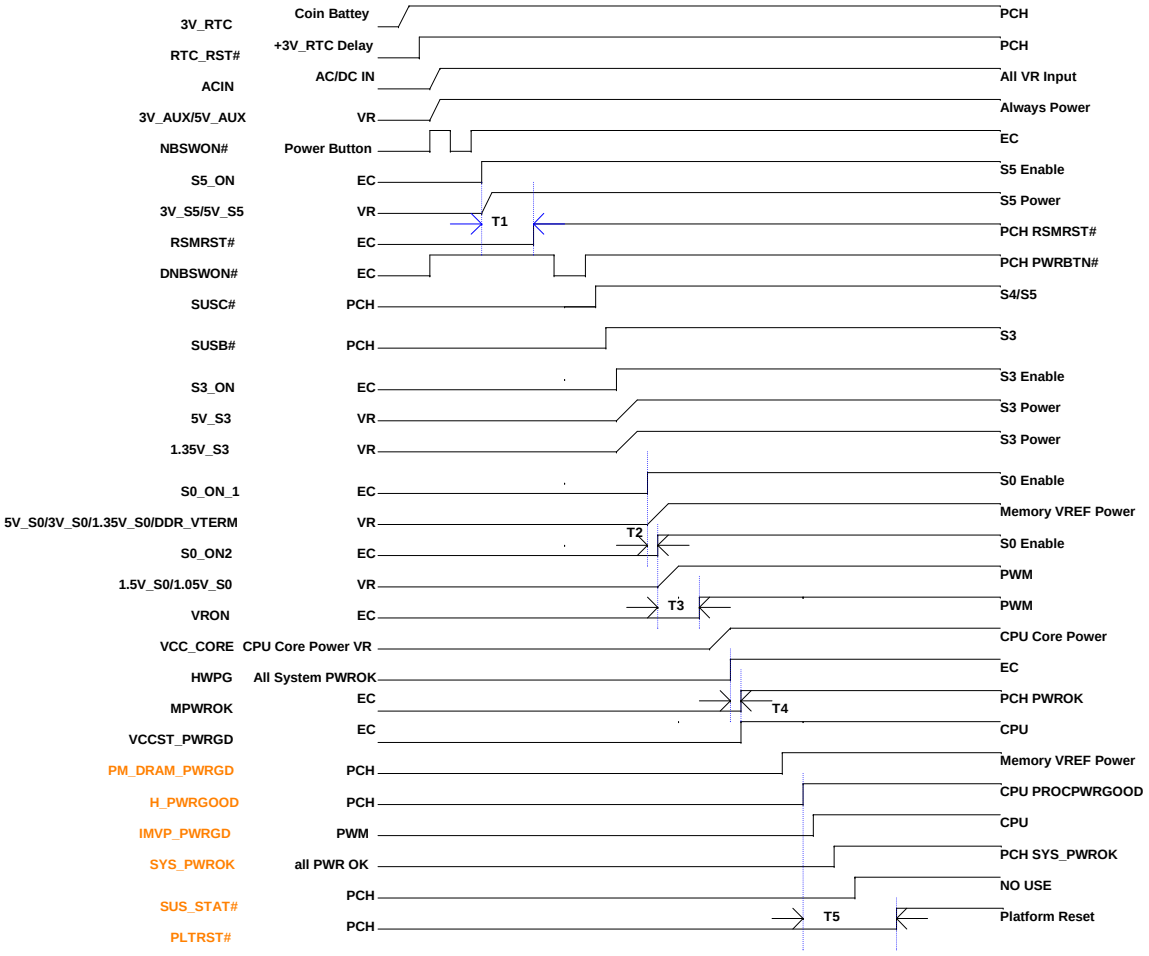
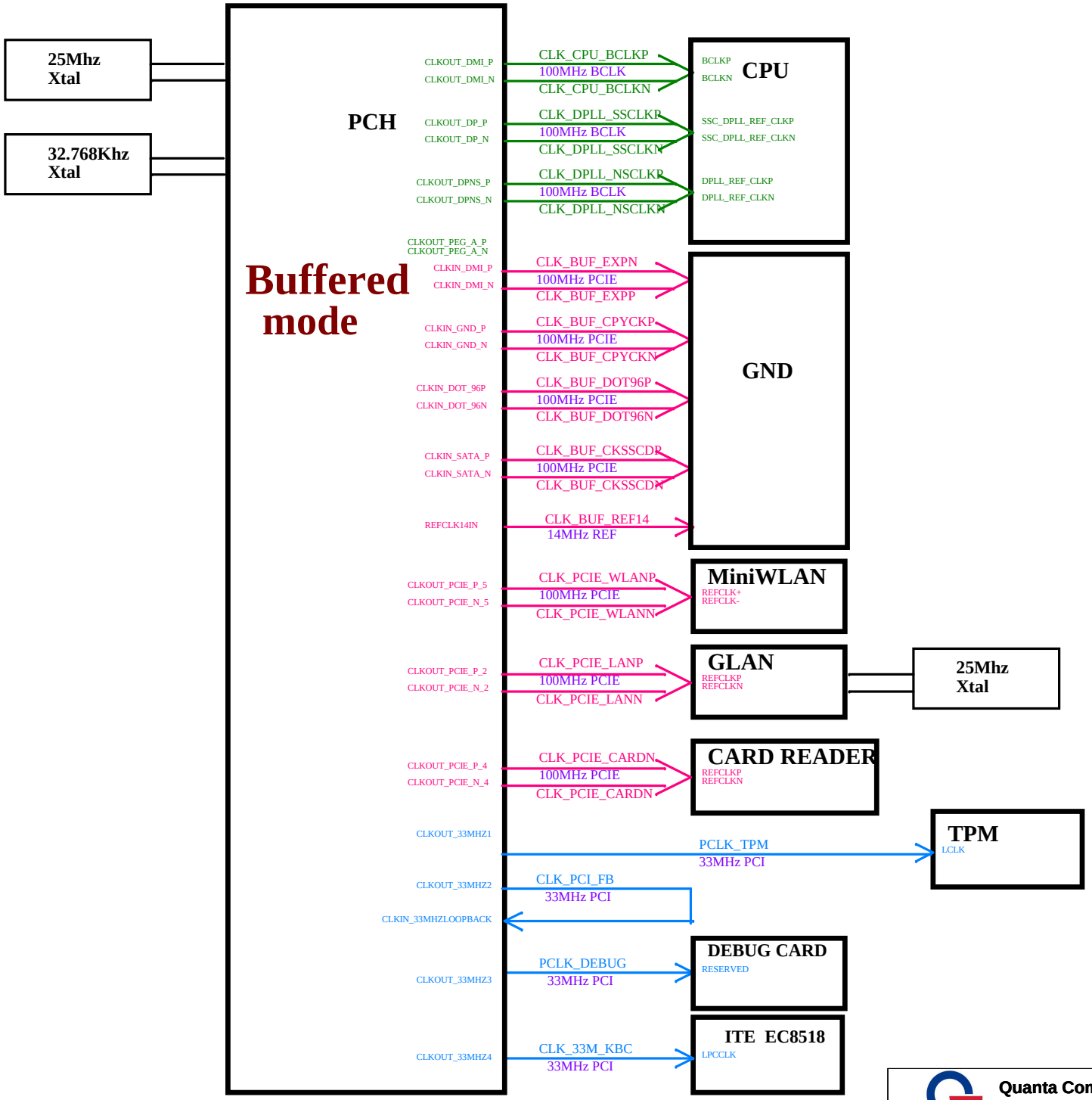
POWER Sequence

FH8A SYSTEM POWER-ON SEQUENCE



System Power Sequence

- T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)
- T2: S0_ON1 TO S0_ON2 = 500us
- T3: S0_ON2 TO VRON = 10ms
- T4: HWPG TO MPWROK = 110ms (spec：>5~ 99ms)
- T5：H_CPUPWRGD to PLTRST# >1ms
- T6：VCC_CORE stable to H_PWRGOOD 5~650ms



Quanta Computer Inc.
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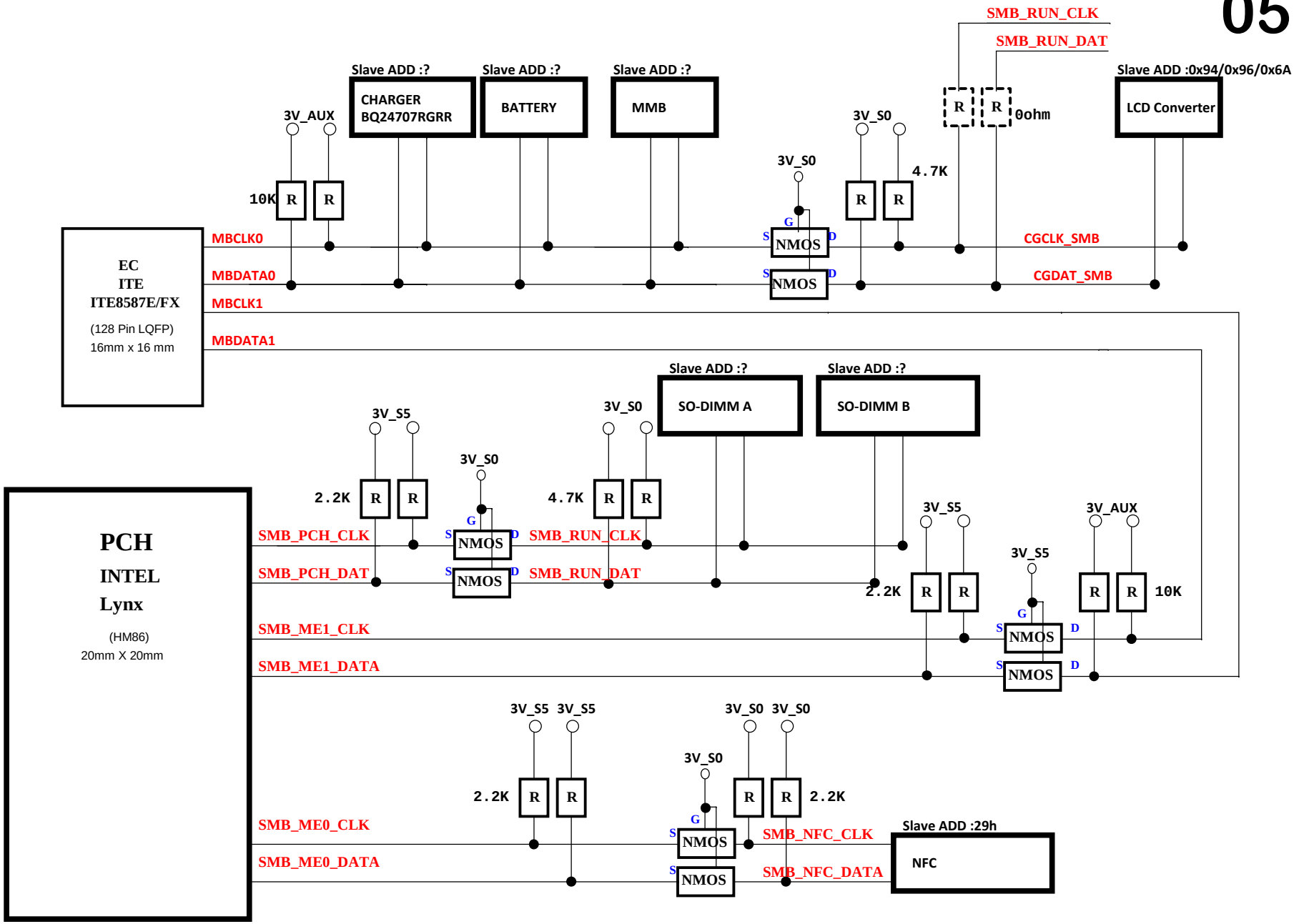

Quanta Computer Inc.		
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Haswell Processor (DMI,PEG,FDI)

PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

VCCIOA_OUT
R77 24.9/F_4
PEG_RCOMP

U20A HASWELL_BGA_E

DMI_TXN0 (11)
DMI_TXN1 (11)
DMI_TXN2 (11)
DMI_TXN3 (11)
DMI_TXP0 (11)
DMI_TXP1 (11)
DMI_TXP2 (11)
DMI_TXP3 (11)
DMI_RXN0 (11)
DMI_RXN1 (11)
DMI_RXN2 (11)
DMI_RXN3 (11)
DMI_RXP0 (11)
DMI_RXP1 (11)
DMI_RXP2 (11)
DMI_RXP3 (11)

A-27
FDI_CSYNC (11)
FDI_INT (11)
R306 *short_4
FDI_CSYNC_R
FDI_CSYNC_R F11
FDI_CSYNC DISP_INT F12

FDI_CSYNC & FDI_INT
Trace length < 10000 Mils
Impendance = 50 ohm

PEG_RCOMP AH6
PEG_TXN0 … PEG_TXN15
PEG_TXP0 … PEG_TXP15
PEG_RXN0 … PEG_RXN15
PEG_RXP0 … PEG_RXP15

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Haswell Processor (CLK,MISC,JTAG)

1.05V_S0
BDW only, unstaff
R414 BDW@1K_4

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

R3 Close to CPU.

H_PECI (14,29)
H_PROCHOT# (29,35)
PM_THRMTRIP# (14)
R56 56_4
H_PROCHOT#_R
PM_THRMTRIP#_R

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

PM_SYNC (11)
H_PWRGOOD (14)
CPU_PLTRST# (14)
R58 *SHORT_4
R326 *SHORT_4
H_PWRGOOD_R
PM_DRAM_PWRGD_R
CPU_RST#_R

CLK_DPLL_NSCLKN (13)
CLK_DPLL_NSCLKP (13)
CLK_DPLL_SSCLKN (13)
CLK_DPLL_SSCLKP (13)
CLK_CPU_BCLKN (13)
CLK_CPU_BCLKP (13)
R337 R336 R328 R324 R330 R332 SHORT_4
CLK_DPLL_NSCLKN_R
CLK_DPLL_NSCLKP_R
CLK_DPLL_SSCLKN_R
CLK_DPLL_SSCLKP_R
CLK_CPU_BCLKN_R
CLK_CPU_BCLKP_R

U20B HASWELL_BGA_E
MISC: PROC_DETECT, CATERR, PECI, PROCHOT, THERMTRIP
PWR: PM_SYNC, PWRGOOD, SM_DRAMPWROK, PLTRSTIN
CLOCK: DPLL_REF_CLKN, DPLL_REF_CLKP, SSC_DPLL_REF_CLKN, SSC_DPLL_REF_CLKP, BCLKN, BCLKP
JTAG: PRDY, PREQ, TCK, TMS, TRST, TDI, TDO, DBR
DDR3: SM_RCOMP0, SM_RCOMP1, SM_RCOMP2, SM_DRAMRST

TP62 PROC_DETECT# C51
TP8 CATERR# G50
G51
H_PECI E50
H_PROCHOT#_R
PM_THRMTRIP#_R D53
DS2
F50
AP48
L54
AC6
AE6
V6
Y6
AB6
AA6

SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

SM_RCOMP_0 BB51 R106 100/F_4
SM_RCOMP_1 BB53 R104 75/F_4
SM_RCOMP_2 BB52 R105 100/F_4
CPU_DRAMRST# BE51

TCK,TMS
Trace Length < 9000mils

XDP_PRDY# N53 TP79
XDP_PREQ# N52 TP78
XDP_TCLK N54 TP82
XDP_TMS M51 TP75
XDP_TRST# M53 TP76
XDP_TDI N49 TP20
XDP_TDO M49 TP31
XDP_DBRST# F53
XDP_DBRST# (11)
C445 *0.01U/25V_4

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

XDP_BPM#0 R51 TP80
XDP_BPM#1 R50 TP24
XDP_BPM#2 P49 TP22
XDP_BPM#3 N50 TP21
XDP_BPM#4 R49 TP23
XDP_BPM#5 P53 TP81
XDP_BPM#6 U51 TP83
XDP_BPM#7 P51 TP77

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Reserve for ESD

*TVL FB02 01 AC1 D4 H_PWRGOOD_R
*TVL FB02 01 AC1 D3 H_PROCHOT#_R
*TVL FB02 01 AC1 D5 PM_THRMTRIP#
Close to CPU side

Thermal Trip

1.05V_S0
(11,35) IMVP_PWRGD
Q4 *DMN601K-7
R73 *100K_4
R72 *1K_4
PM_THRMTRIP#
Q3 *METR3904-G
SYS_SHDN# R71 *0_4 S5_ON (29,31)

PM_DRAM_PWRGD_R (50ohm)
Trace Length: 2~8 inches

1.35V_S3
R86 1.8K/F_4
A-38
PM_DRAM_PWRGD (50ohm)
Trace Length: 2~8 inches
(11) PM_DRAM_PWRGD
R88 *short_4
PM_DRAM_PWRGD_R
R87 3.3K/F_4

PU/PD of CPU

VCCIO_OUT
H_PROCHOT# R315 62_4
H_PWRGOOD_R R57 10K_4
VCCIO_OUT
CLK_DPLL_SSCLKP_R R323 *10K_4
CLK_DPLL_SSCLKN_R R327 *10K_4
R531 *10K_4

Reserved For buffer reset of PLTRSRIN#

B-2
3V_S0
1.05V_S0
U19 *74LVC1G07GW
(11,21,23,24,26,29) PLTRST#
C385 *0.01U/16V_4
R334 *1K_4
R329 *43_4
CPU_PLTRST#_Q
CPU_RST#_R
R331 *20K/F_4

SM_DRAMRST# Topology

DDR3_DRAMRST# (50ohm)
Trace Length < 6 inches

1.35V_S3
R180 470/F_4
A-27
CPU_DRAMRST#
R179 *short_4
DDR3_DRAMRST#
DDR3_DRAMRST# (17,18)
C241 *0.1U/16V/X7R_4

Haswell ULT DRAMRST#

XDP PU/PD

XDP_TCLK
XDP_TRST#
R338 51_4
R335 51_4
1.05V_S0
R406 *51_4 XDP_TDO

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	Haswell 1/5 (PEG/DMI/FDI)	2A
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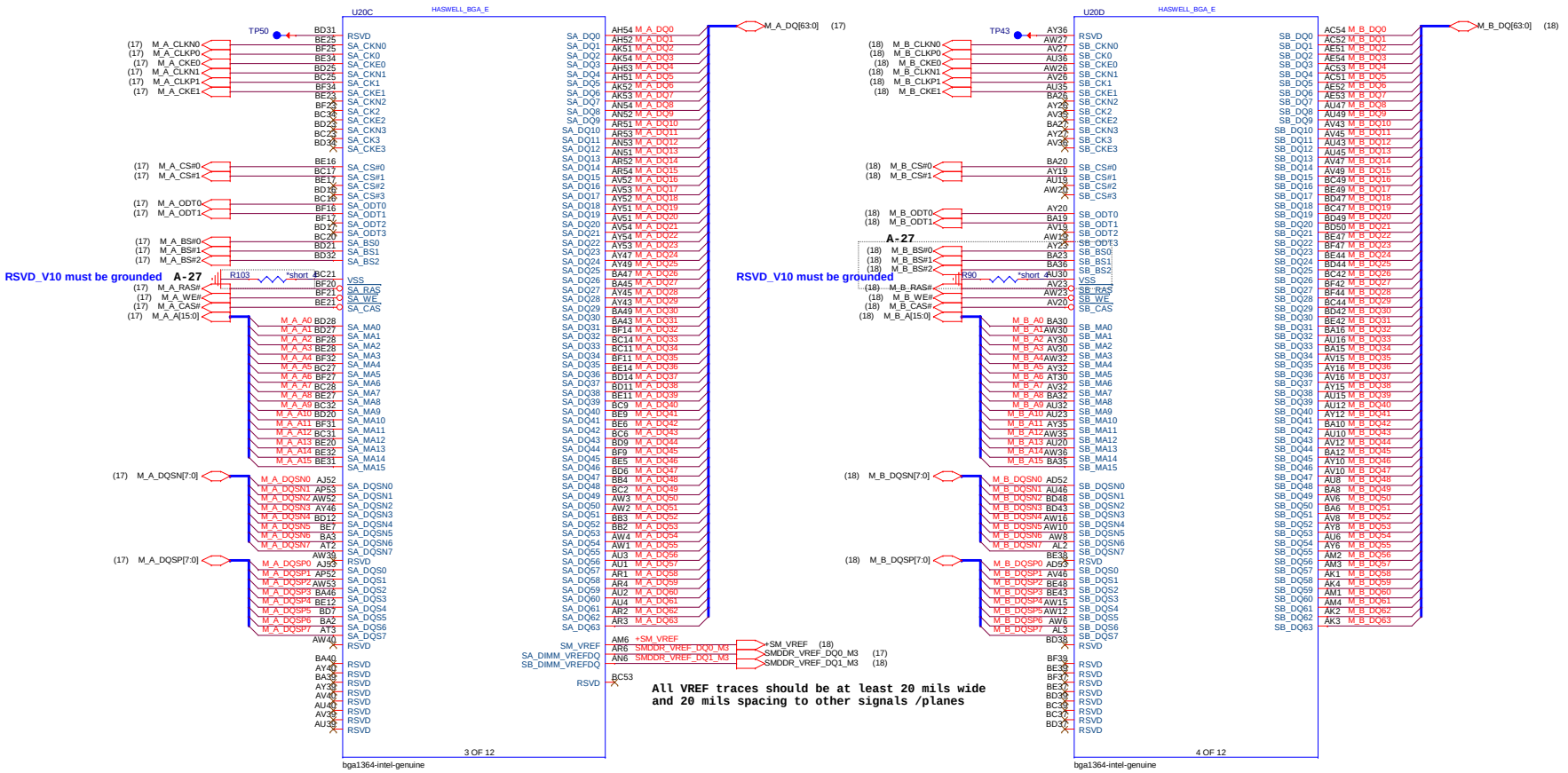
Haswell Processor (DDR3)



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Size	Document Number		Rev
	Haswell 2/5 (DDR3 I/F)		2A
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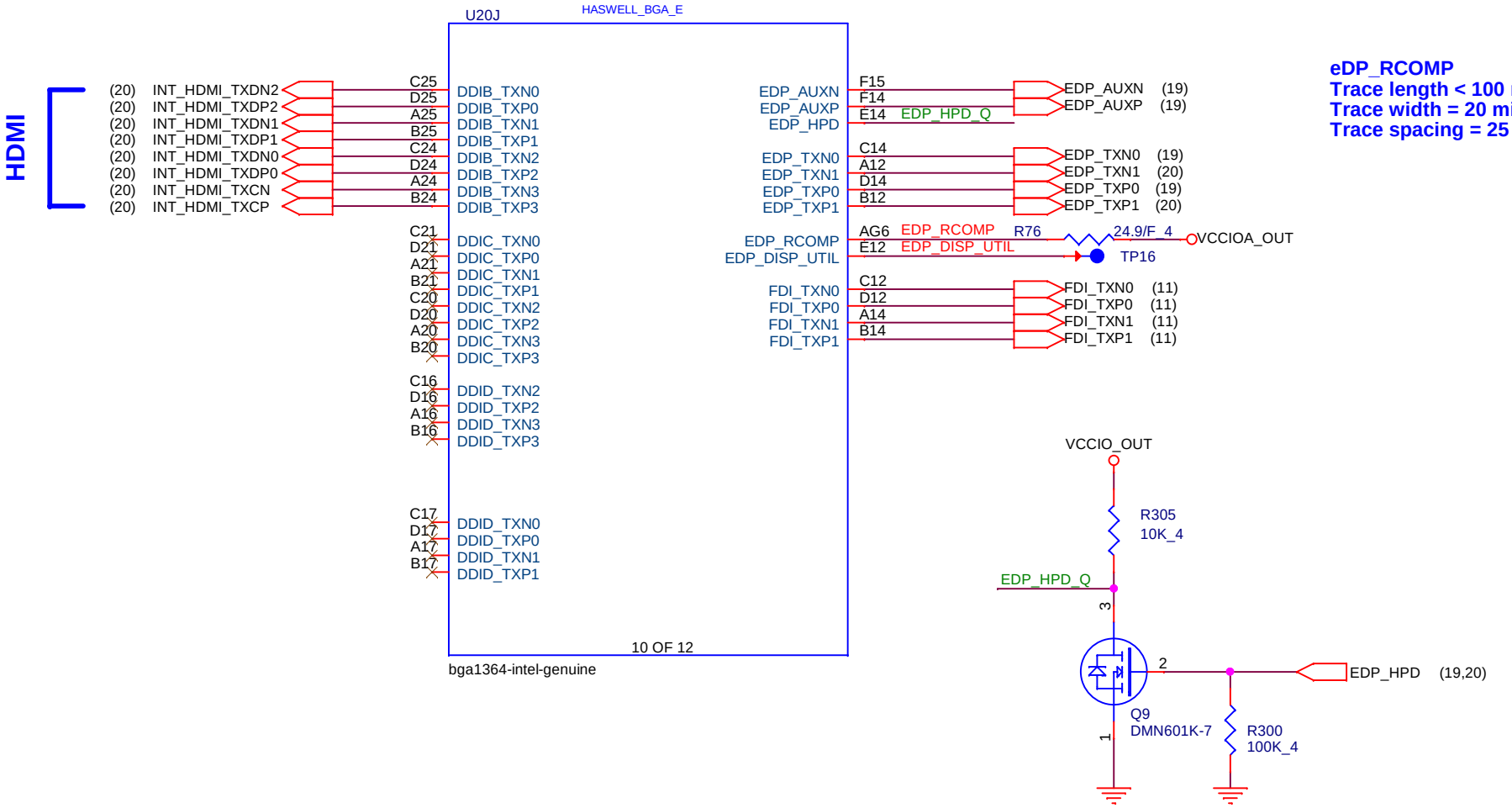
Haswell Processor (DDI,eDP,FDI)

08



Quanta Computer Inc.		
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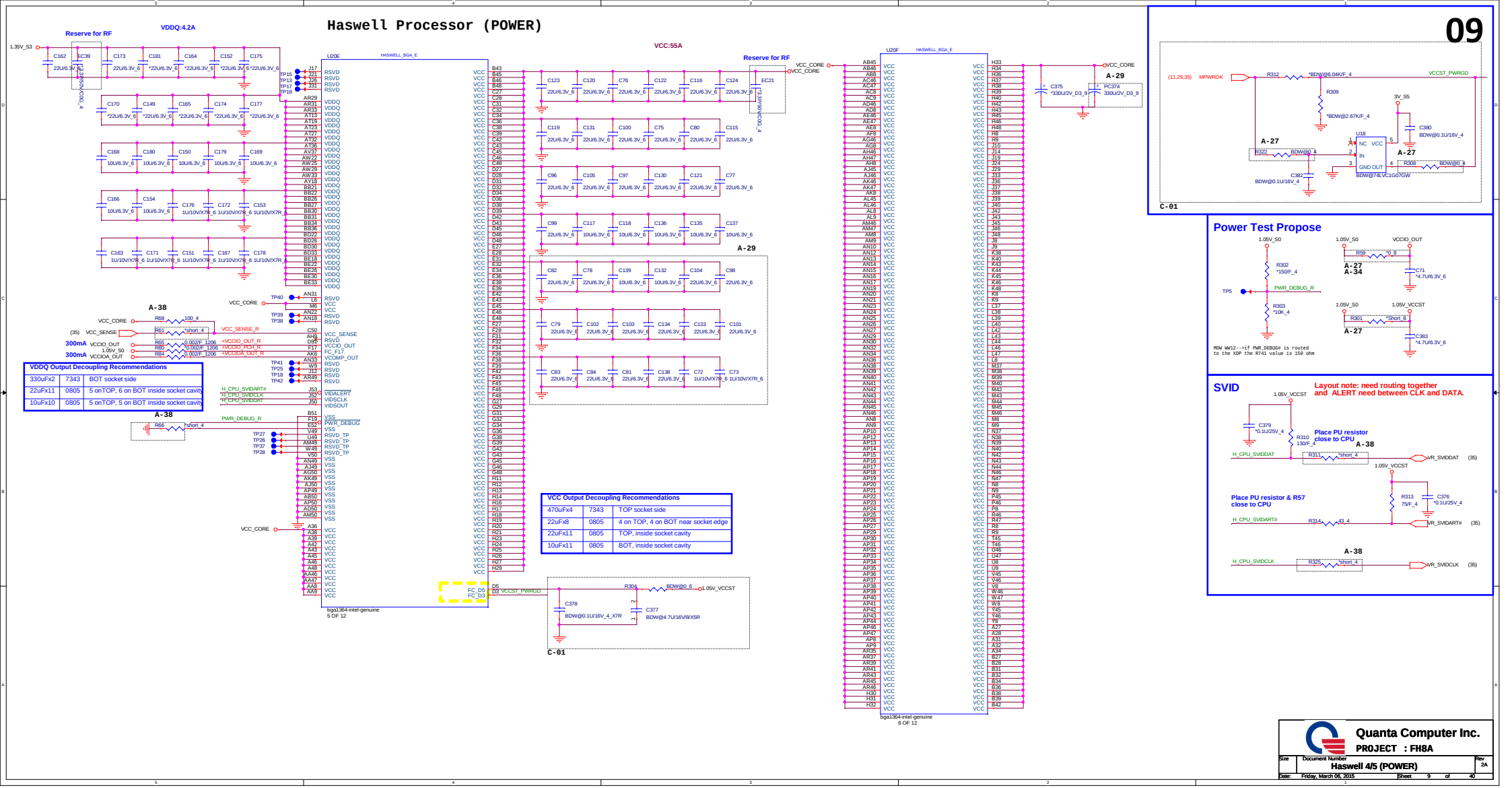
Haswell Processor (POWER)



09

Power Test Propose

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

Quanta Computer Inc.		
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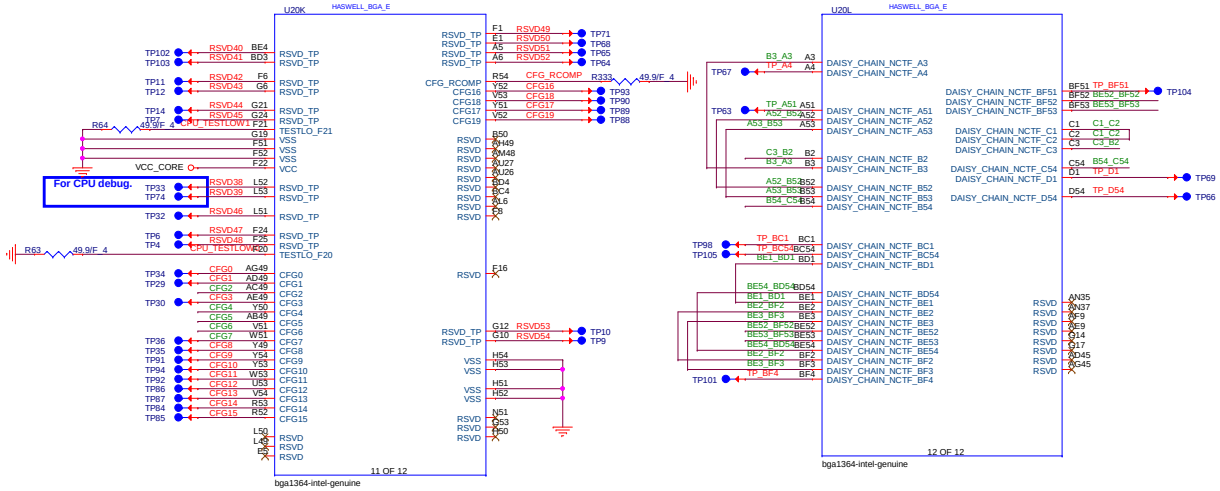
Haswell Processor (GND)

Haswell Processor (CFG,RSVD)



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R83 *1K 4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R81 1K 4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R341 *1K 4 CFG5 R82 *1K 4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	CFG7 R80 *1K 4

C-7

R62 *SHORT 4 VSS_SENSE (35)

R67 100 4

VSS_SENSE_R — VSS_SENSE

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	Haswell 5/5 (CFG/GND)		2A
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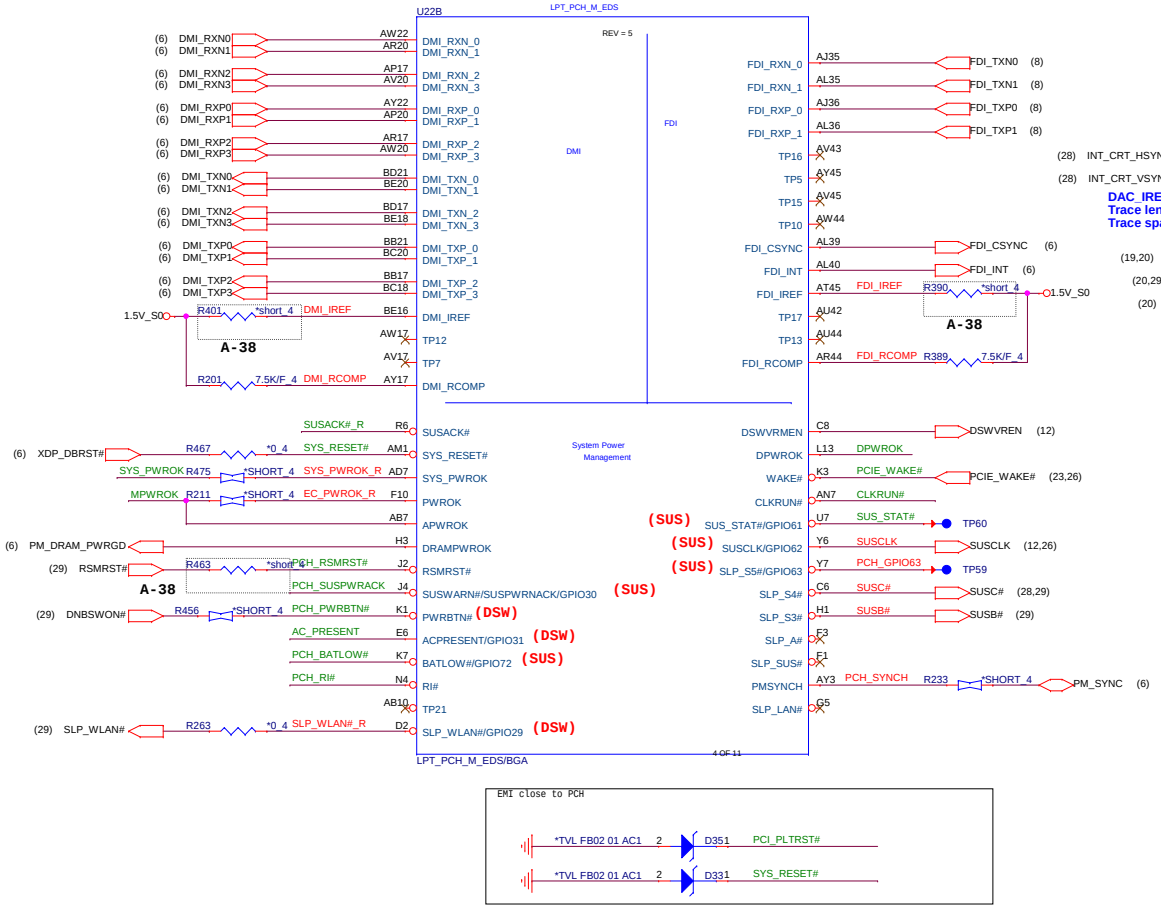
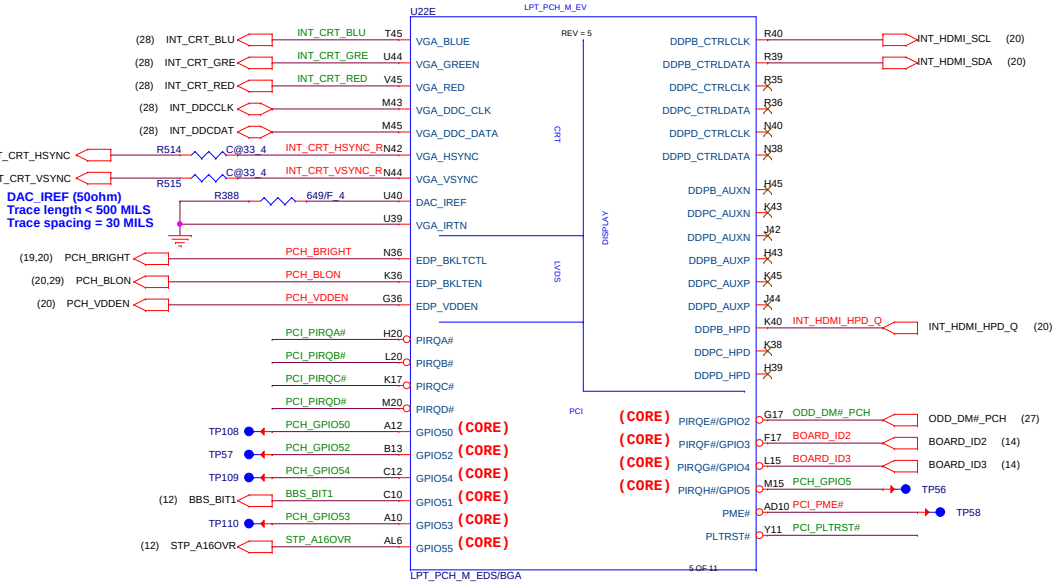
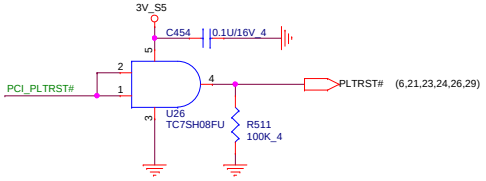
Lynx Point (DMI,FDI,PM)



Lynx Point (CRT,PCI,DDI CNTL)

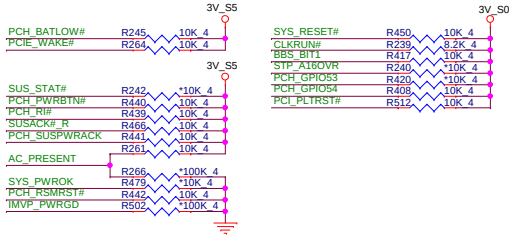


PLTRST# Buffer

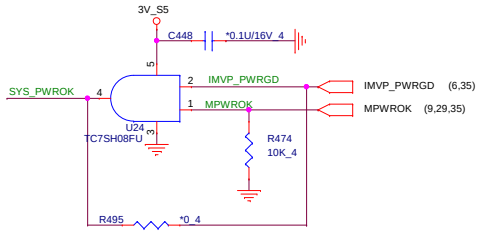


VGA PD

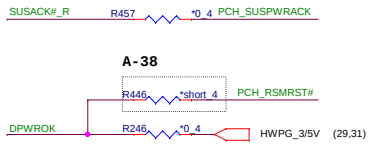
PCH PM PU/PD



SYSPWOK

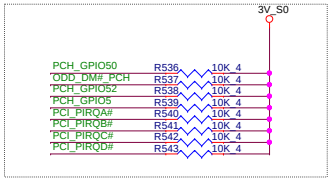


DSW Circuit



PCI PU

B-4



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	LPT 1/6 (DMI/FDI/VGA)	2A
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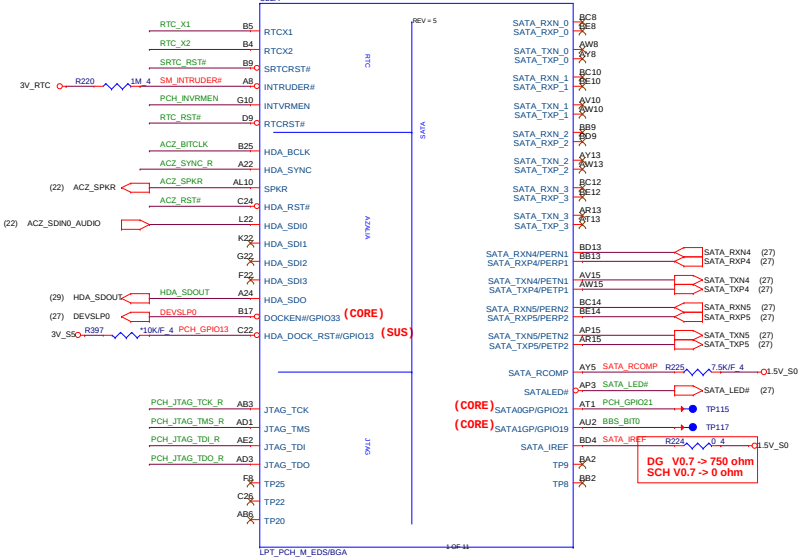
Lynx Point (RTC,IHDA,SATA,JTAG)



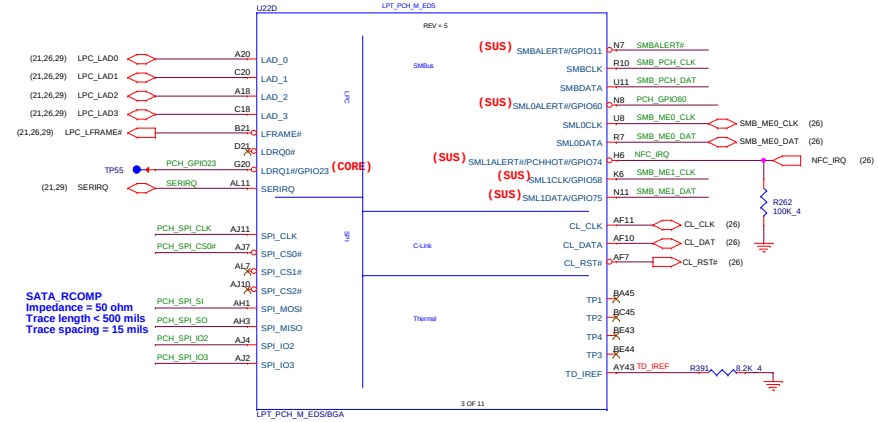
HDD

ODD

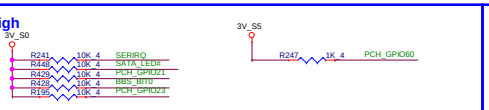
SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

DG V0.7 -> 750 ohm
SCH V0.7 -> 0 ohm

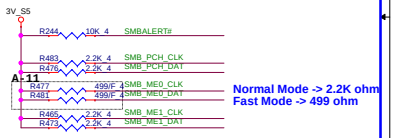
Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)



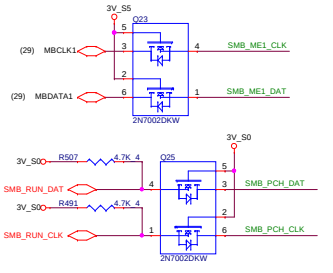
Pull High



SMBus



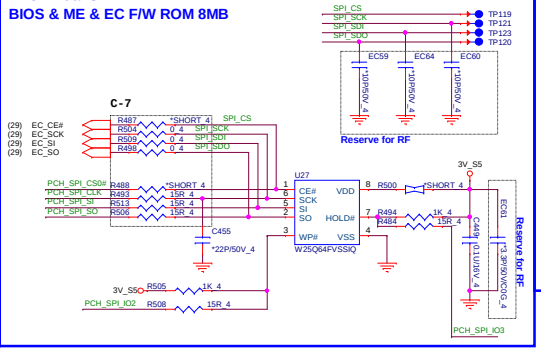
SMBus/Pull-up(CLG)



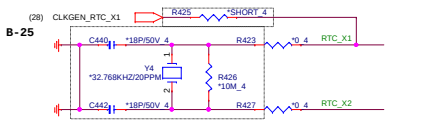
PCH STRAPING

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	ACZ_SPKR R260 *10K_4 3V_S0
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	(11,26) SUSCLK R256 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	(11) STP_A16OVR R259 *4.7K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R214 330K_4 3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 0 1 Reserved 1 0 Reserved 1 1 SPI 0 0 LPC	(11) BBS_BIT1 R415 *1K_4 BBS_BIT0 R464 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	HDA_SDOUT R215 *1K_4 R216 *20K_4 3V_S5
SATA2GP/GPIO36	RSVD	PWROK	Internal PD	(14) PCH_GPIO36 R430 *200K_4 3V_S0
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	(14) PCH_GPIO37 R472 *1K_4 3V_S5
GPIO8	RSVD	RSMRST#	Internal PU	(14) PCH_GPIO8 R435 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Enable 1 = Disable Must be PU to VCCRTC	(11) DSWVREN R218 330K_4 R221 *330K_4 3V_RTC

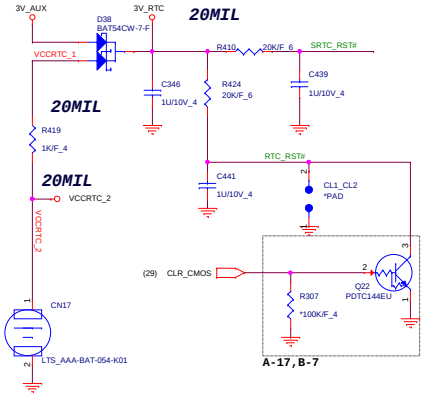
PCH Dual SPI
BIOS & ME & EC F/W ROM 8MB



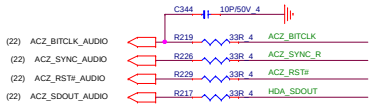
RTC Clock 32.768KHz (RTC)



RTC Circuitry (RTC)

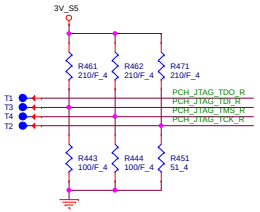


HDA



PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

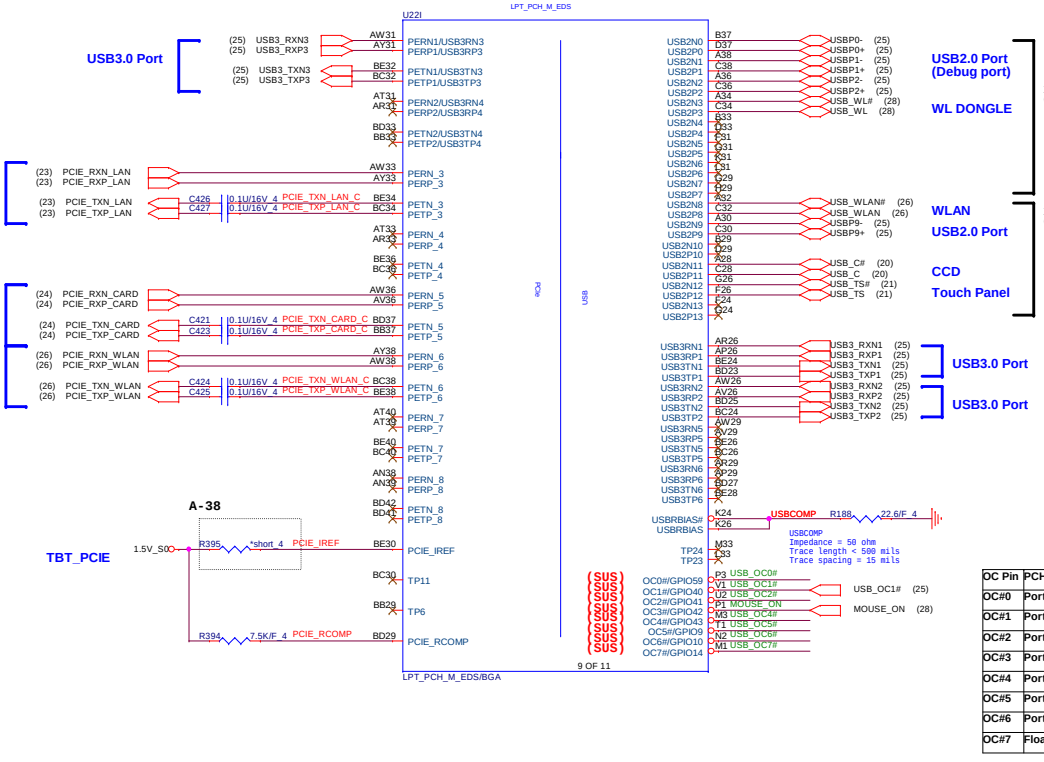


Quanta Computer Inc.
PROJECT : FH8A

Size	Document Number	Rev
	LPT 2/6 (SATA/HDA/SPI)	2A

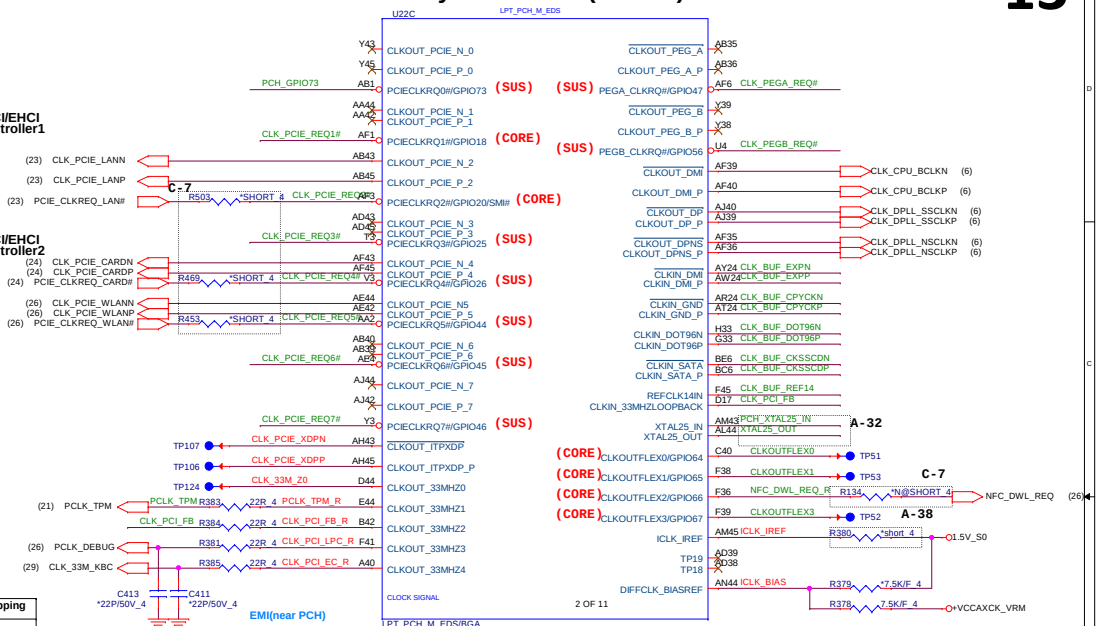
Date: Friday, March 06, 2015 Sheet 12 of 40

Lynx Point (PCIE,USB3.0,USB2.0)

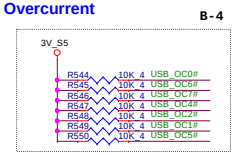


OC Pin	PCH Mapping
OC#0	Port0&1
OC#1	Port2&3
OC#2	Port4&5
OC#3	Port6&7
OC#4	Port8&9
OC#5	Port10&11
OC#6	Port12&13
OC#7	Floater OC#

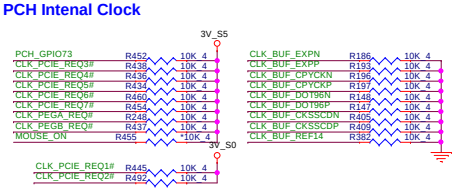
Lynx Point (CLOCK)

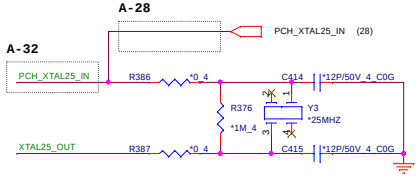


USB Overcurrent



PCH Intenal Clock

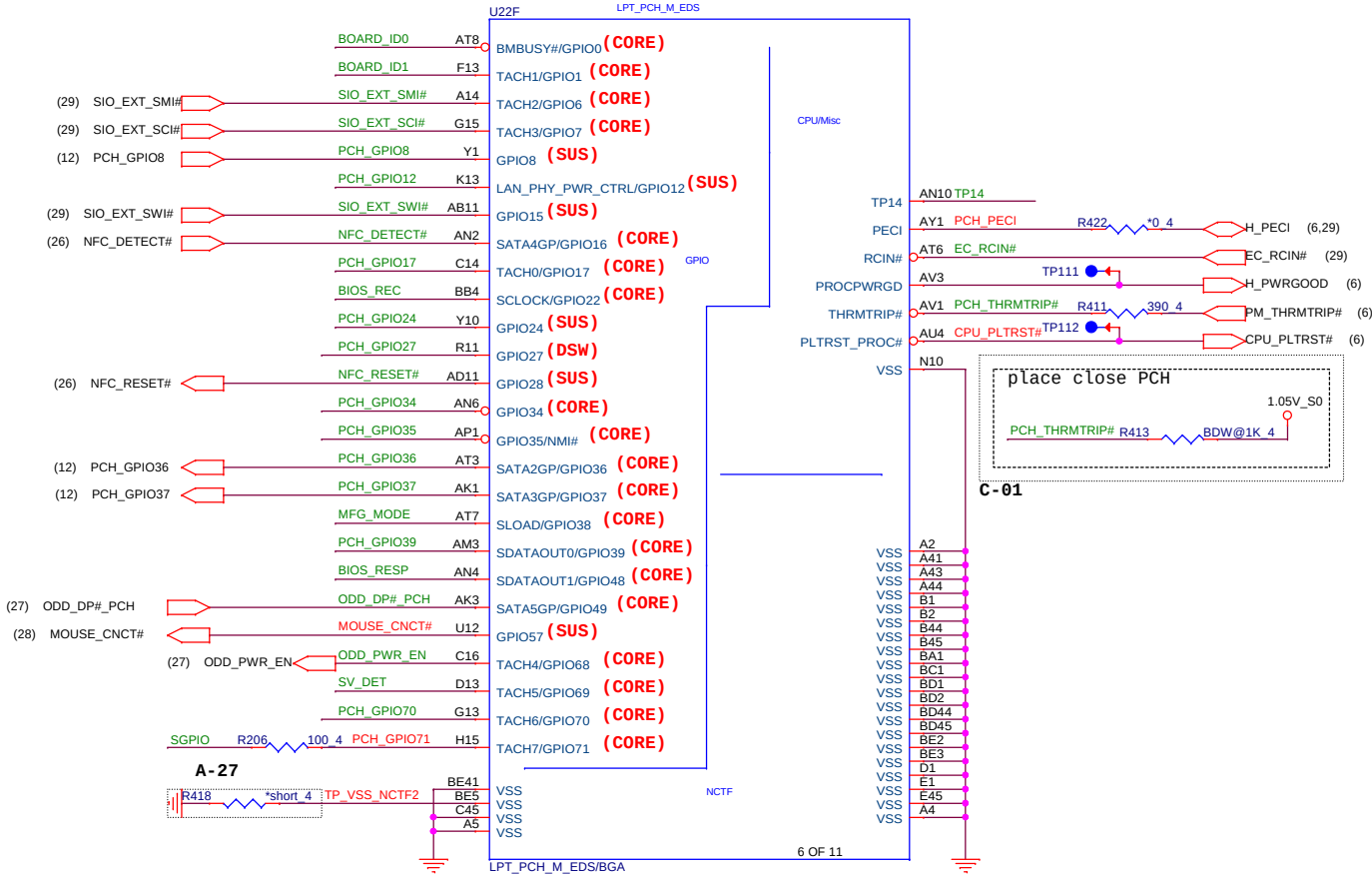


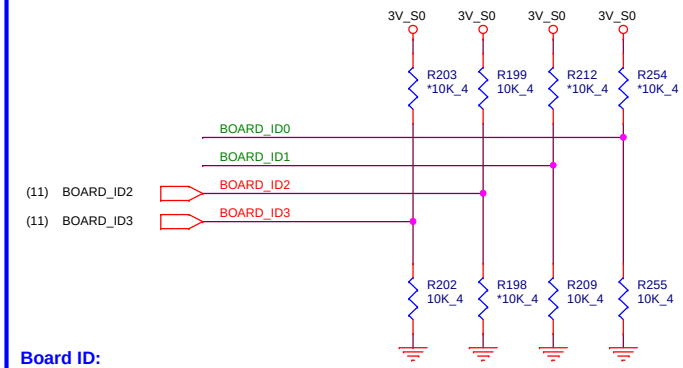


PCH PU

Quanta Computer Inc.	
PROJECT : FH8A	
Size	Document Number: LPT 3/6 (PCIE/USB/CLK) — Rev: 2A
Date: Friday, March 06, 2015	Sheet 13 of 40

Lynx Point (GPIO,CPU/MISC,NCTF)





Board ID:

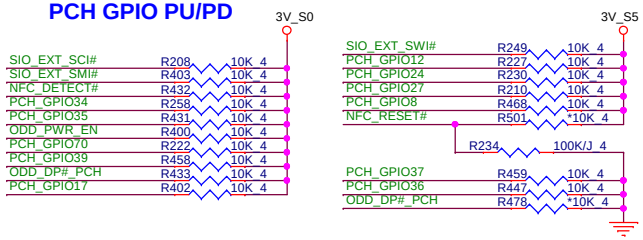
BOARD_ID0	PCH_CPIO0
UMA	0
DIS	1

BOARD_ID3	PCH_CPIO4
Touch	0
Non-touch	1

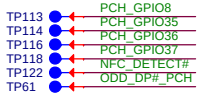
BOARD_ID1	PCH_CPIO1
LVDS	0
eDP	1

BOARD_ID2	PCH_CPIO3
VGA	0
non-VGA	1

PCH GPIO PU/PD



XDP Signal



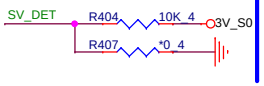
PCH MISC PU/PD

BIOS RECOVERY 0 = Enable 1 = Disable

Swap GPIO 0 = SGPIO 1 = Default

MFG TEST

SV Detect 0 = SV Detect 1 = Default



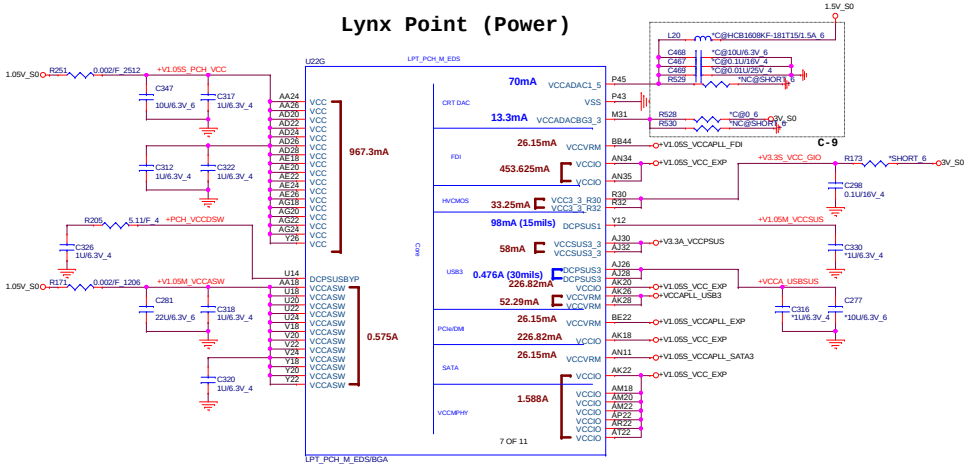
BIOS_RESP 0 = BIOS RESP 1 = Default

Quanta Computer Inc.

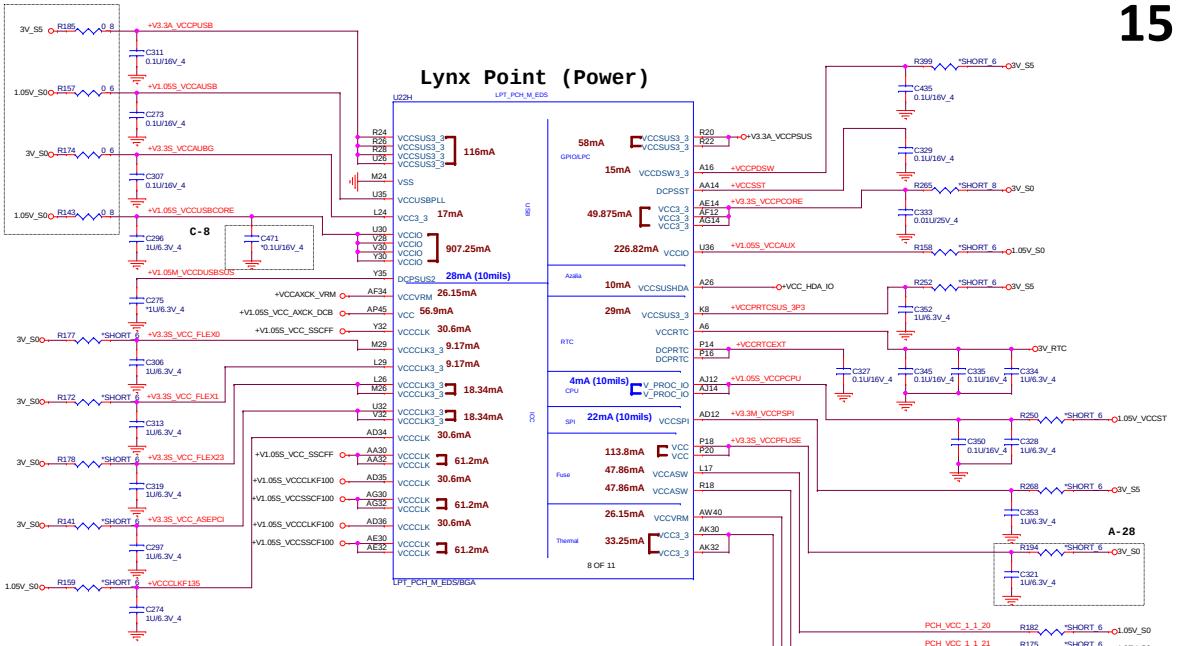
PROJECT : FH8A

Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	2A
Date: Friday, March 06, 2015	Sheet 14 of 40	

Lynx Point (Power)



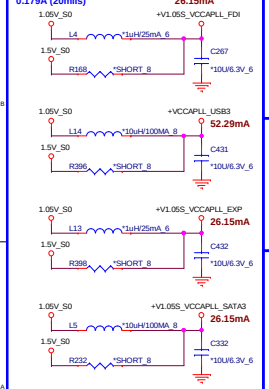
Lynx Point (Power)



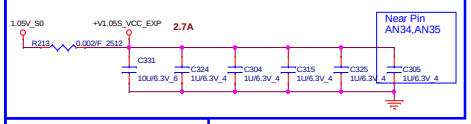
PCH VRM Power

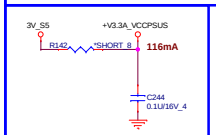
1.05V OPTION IS PROVIDED FOR VALIDATION PURPOSES

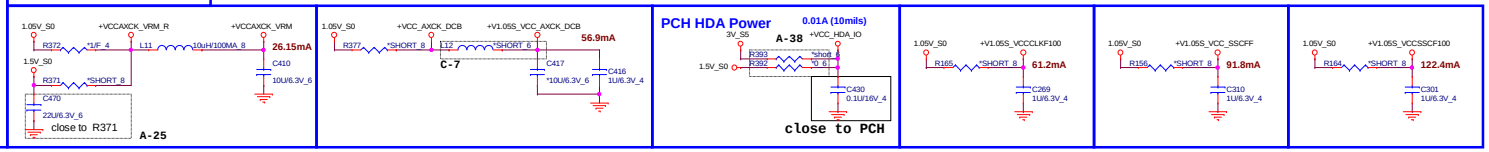
0.179A (20mils)



PCH VCCIO Power







PCH HDA Power

0.01A (10mils)

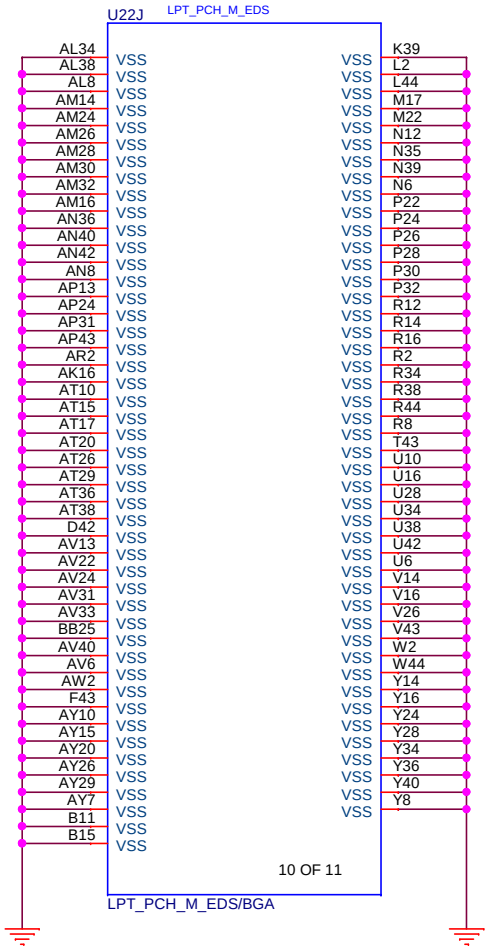
Quanta Computer Inc.

PROJECT : FH8A

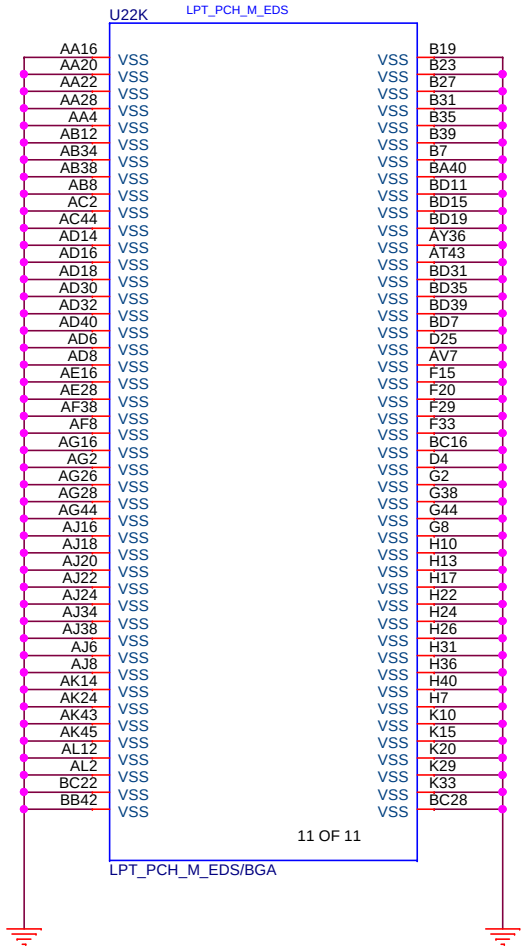
Size	Document Number	Rev
	LPT 5/6 (POWER)	2A

Date: Friday, March 06, 2015 Sheet 15 of 40

Lynx Point (GND)



Lynx Point (GND)

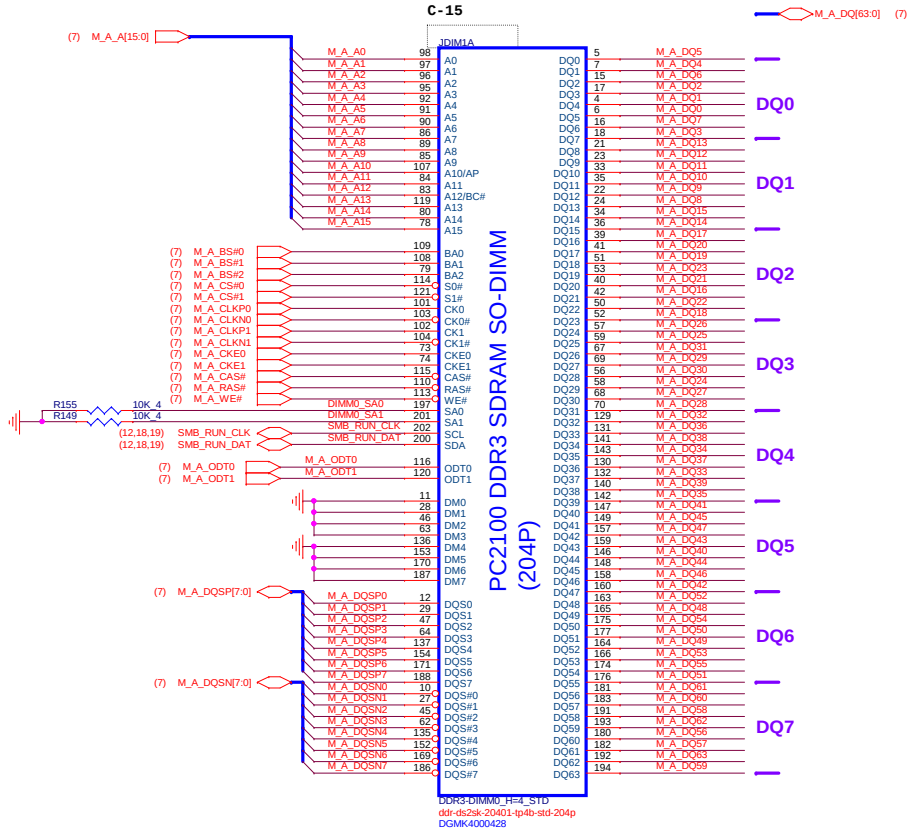


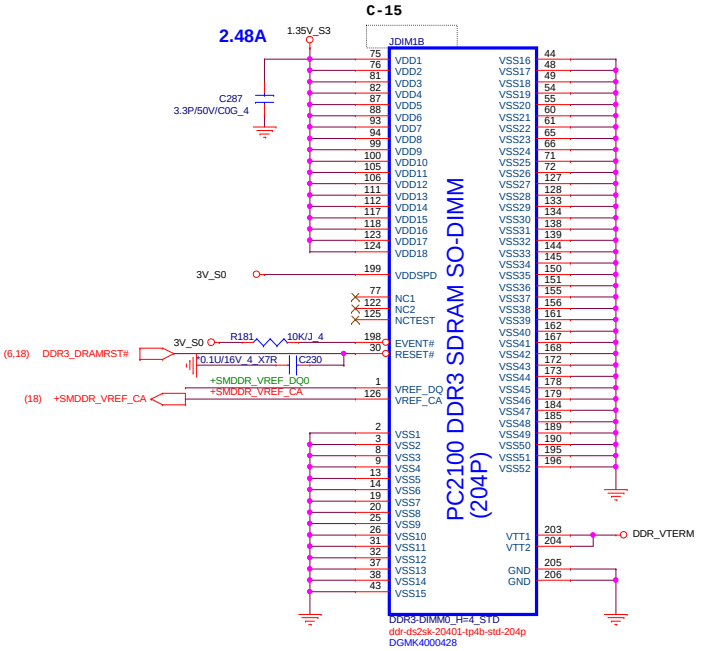
Quanta Computer Inc.

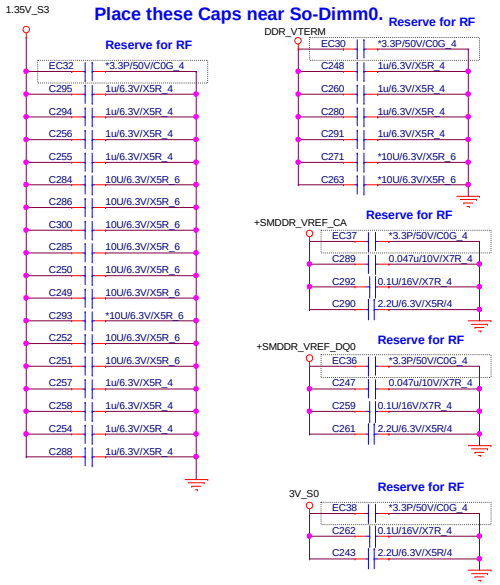
PROJECT : FH8A

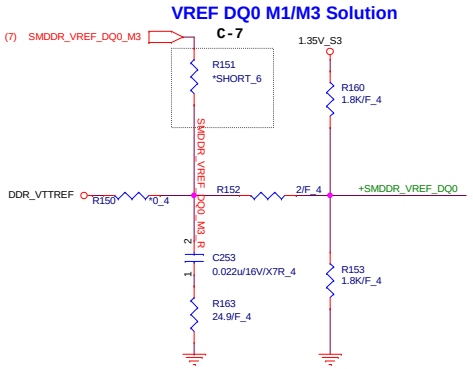
Size	Document Number	Rev
	LPT 6/6 (GND)	2A

Date: Friday, March 06, 2015 Sheet 16 of 40



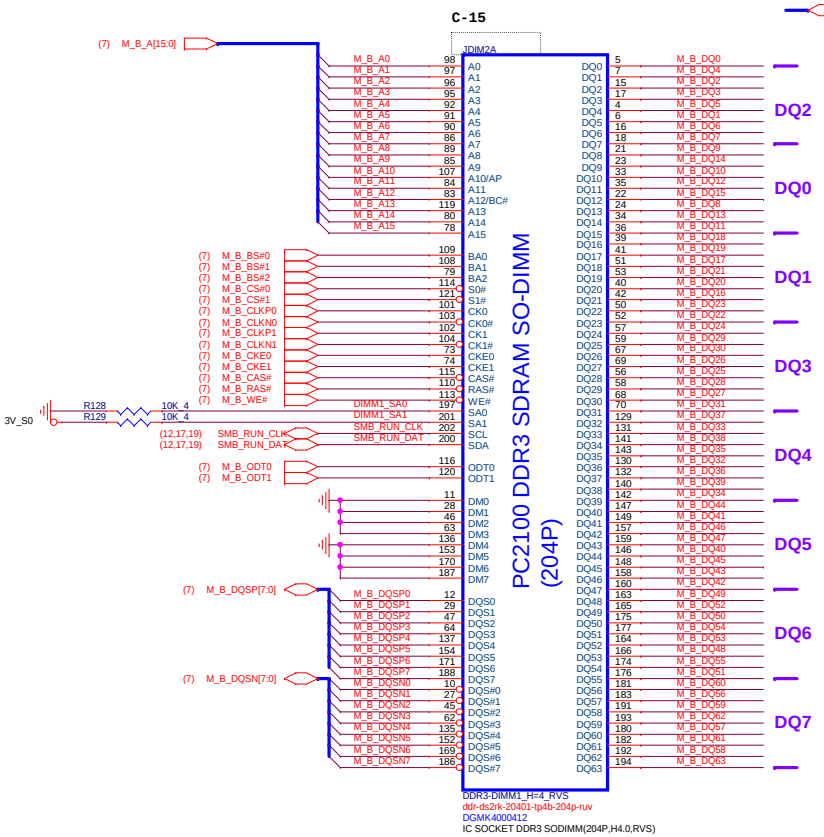


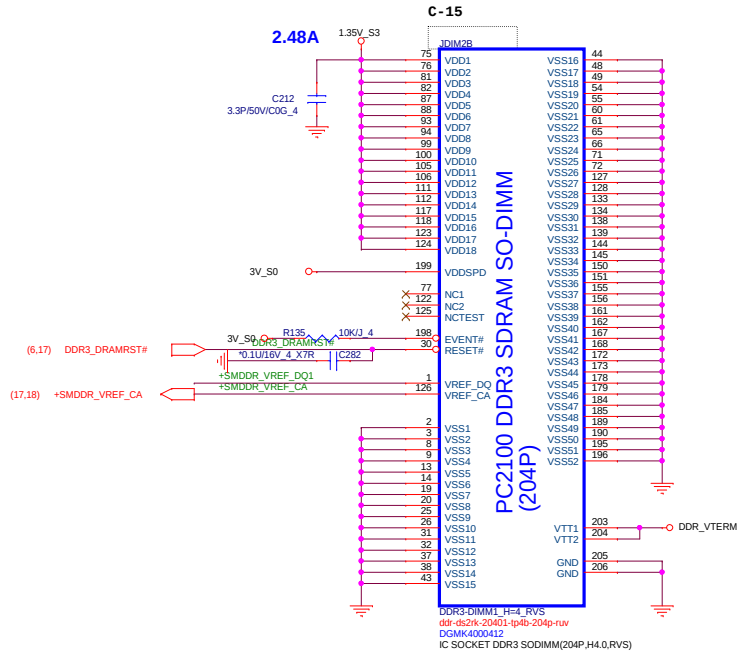




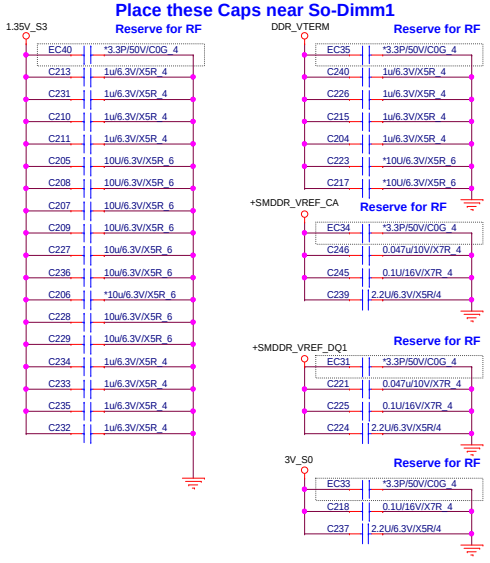
Quanta Computer Inc.
PROJECT : FH8A

Size	Document Number	Rev
	DDR3L DIMM0-STD (4.0H)	2A
Date: Friday, March 06, 2015	Sheet 17 of 40	



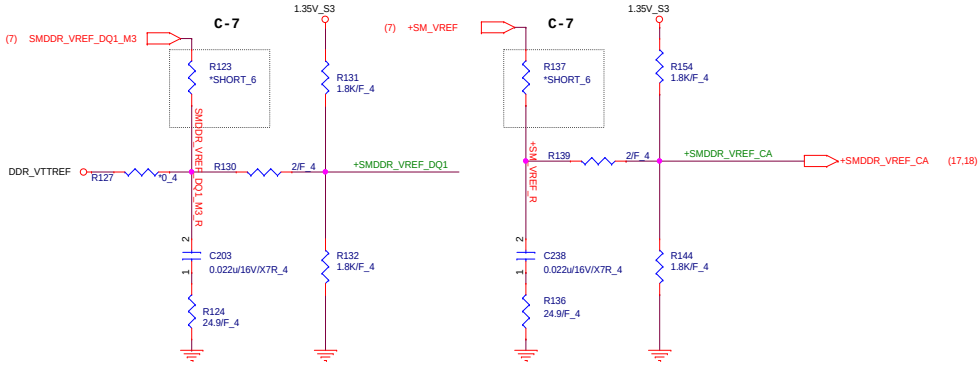


Place these Caps near So-Dimm1



VREF DQ1 Solution

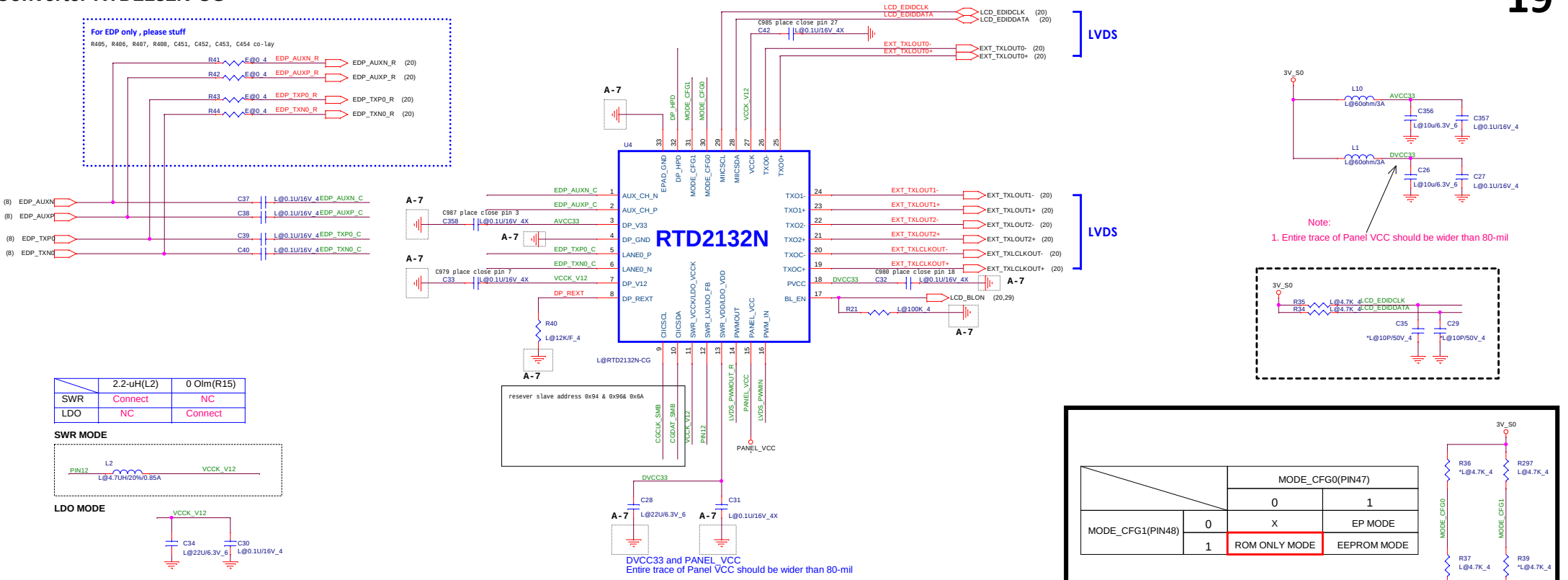
All VREF traces should be at least 20 mils wide and 20 mils spacing to other signals /planes



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT : FH8A		
Size	Document Number	Rev
	DDR3L DIMM1-RVS (4.0H)	2A
Date: Friday, March 06, 2015	Sheet 18 of 40	

Converter RTD2132N-CG



	2.2-uH(L2)	0 Olm(R15)
SWR	Connect	NC
LDO	NC	Connect

SWR MODE

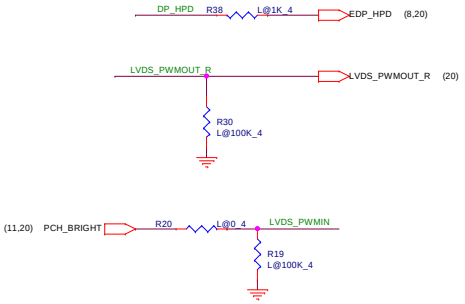
LDO MODE

1. C41 10-uF capacitor should be X5R material
2. Inductor should be withstand current >600-mA
3. Capacitors should be closed to PIN12

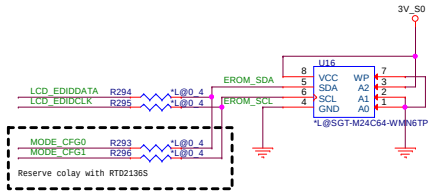
Note:
1. Entire trace of Panel VCC should be wider than 80-mil

MODE_CFG1(PIN48)	MODE_CFG0(PIN47) 0	MODE_CFG0(PIN47) 1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

HPD/ Back Light/ BL PWM

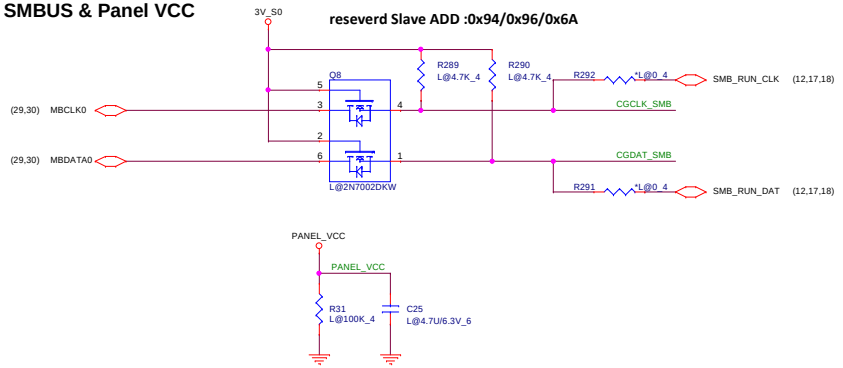


Reserve EEPROM Address=0xA8



SMBUS & Panel VCC

reseverd Slave ADD :0x94/0x96/0x6A



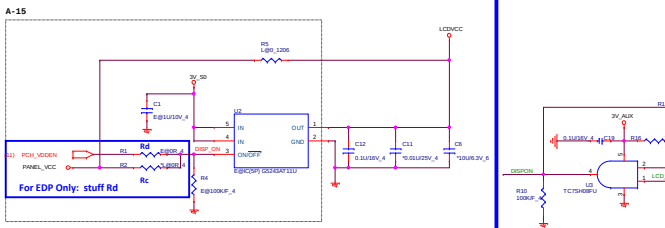
Quanta Computer Inc.

PROJECT : FH8A

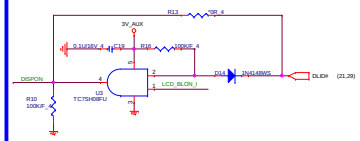
Size	Document Number	Rev
	eDP to LVDS (RTD2132N)	2A

Date: Friday, March 06, 2015 Sheet 19 of 40

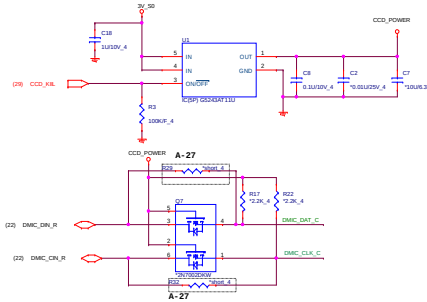
LCD POWER SWITCH



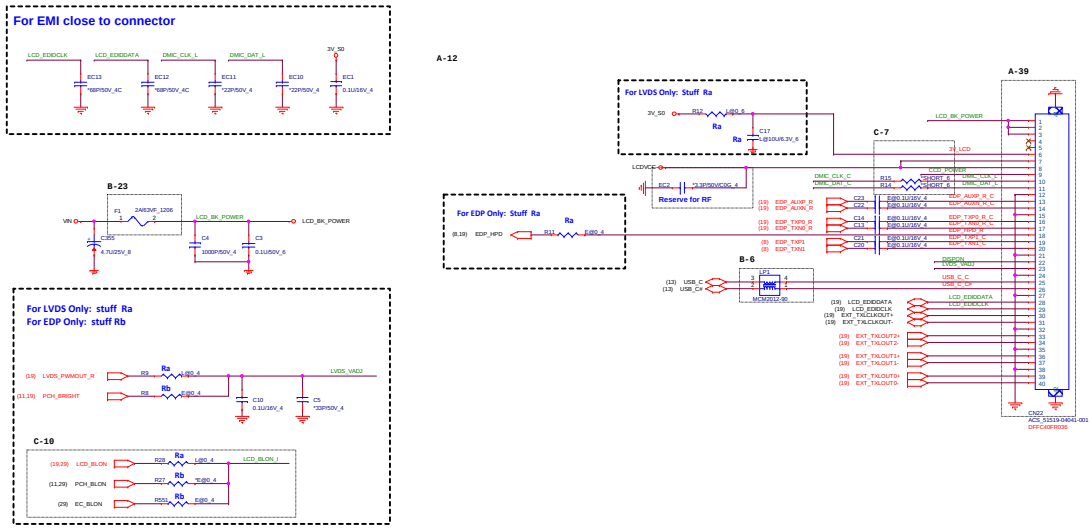
PANEL BACKLIGHT CONTROL



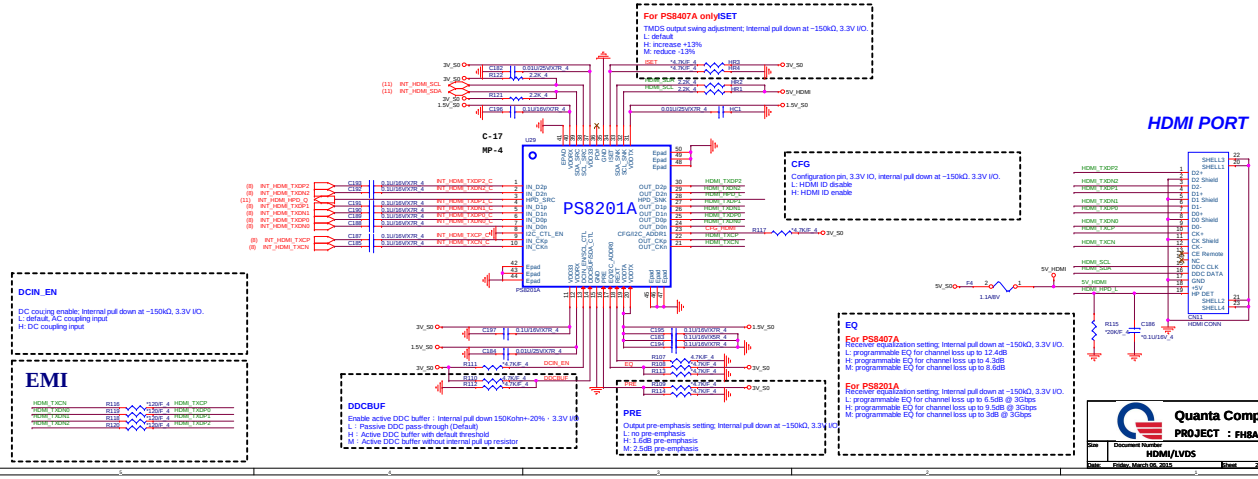
CCD KILL



LCD CONNECTOR

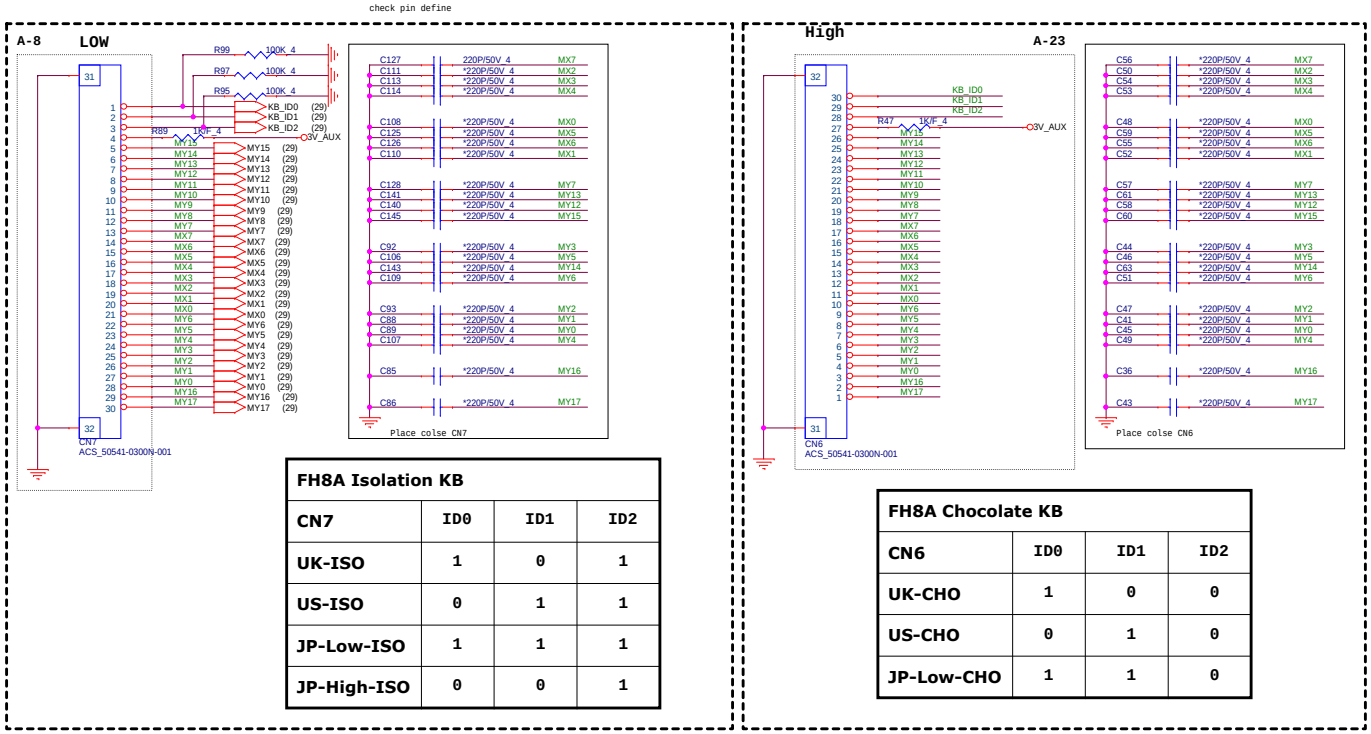


HDMI



Quanta Computer Inc.
PROJECT : FH8A
Size | Document Number: HDMI/LVDS | Rev: 3A
Date: Friday, March 09, 2012 | Sheet 20 of 40

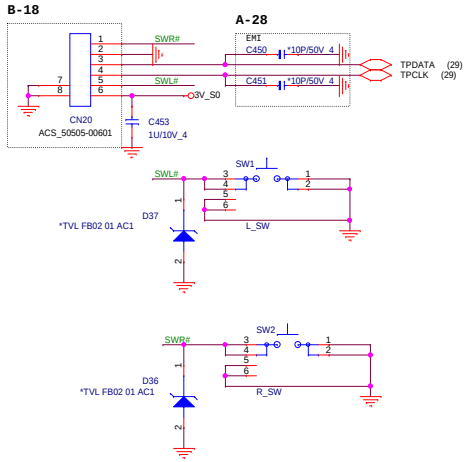
Keyboard Connector



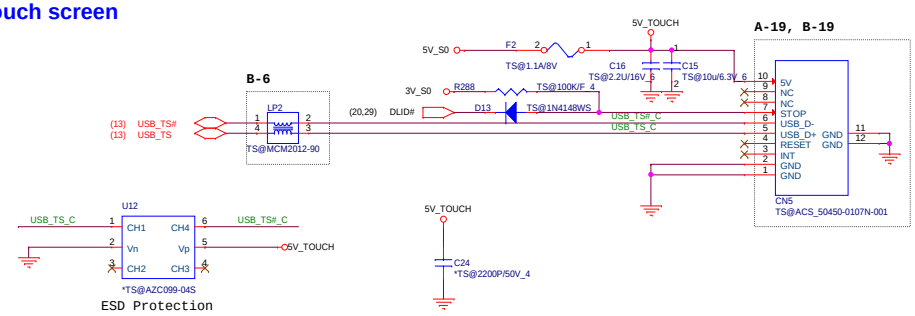
FH8A Isolation KB			
CN7	ID0	ID1	ID2
UK-ISO	1	0	1
US-ISO	0	1	1
JP-Low-ISO	1	1	1
JP-High-ISO	0	0	1

FH8A Chocolate KB			
CN6	ID0	ID1	ID2
UK-CHO	1	0	0
US-CHO	0	1	0
JP-Low-CHO	1	1	0

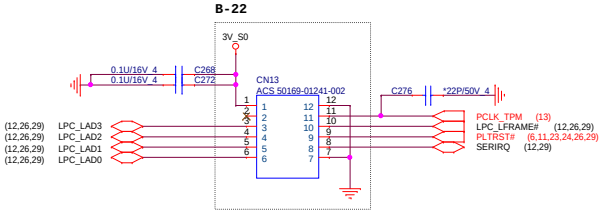
Touch Pad Connector



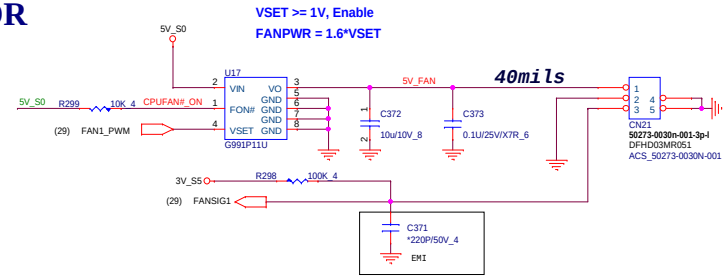
Touch screen



TPM module type



FAN CONNECTOR



Quanta Computer Inc.
PROJECT : FH8A

Size	Document Number	Rev
	KB/FAN/TP/TPM/TOUCH SCREEN	2A

Date: Friday, March 06, 2015 Sheet 21 of 40

Audio Code (ALC283)

DGND plane | AGND plane

B-7 B-12 C-11

AUDIO return path 1 | AUDIO return path 2 | AUDIO return path 3 | AJK1 EMI path | ACON1 EMI path

Universal Audio Jack

(ALC283 supported iPhone/Nokia headset, Headphone, Line-In and Microphone)

A-4 A-13 B-15

B-11

Place close to Pin 26

EMI requirement

ALC283

Place close to Pin 27

AC18 place close to Codec

Place next to pin 38

place close to Codec

CLOSE TO PIN 39

CLOSE TO PIN 46

Reserve for RF

Place next to pin 1

Place next to pin 9

place close to Codec

AGND

DGND

1.6Vrms

EMI

A-22

A-38

A-3

C-7

digital ground

Place near Audio Codec

Internal SPK

DGND plane | AGND plane

Place close to Codec

Codec AVDD(AC68 placed close to power source)

V: 1.5V

5/28 upadted

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

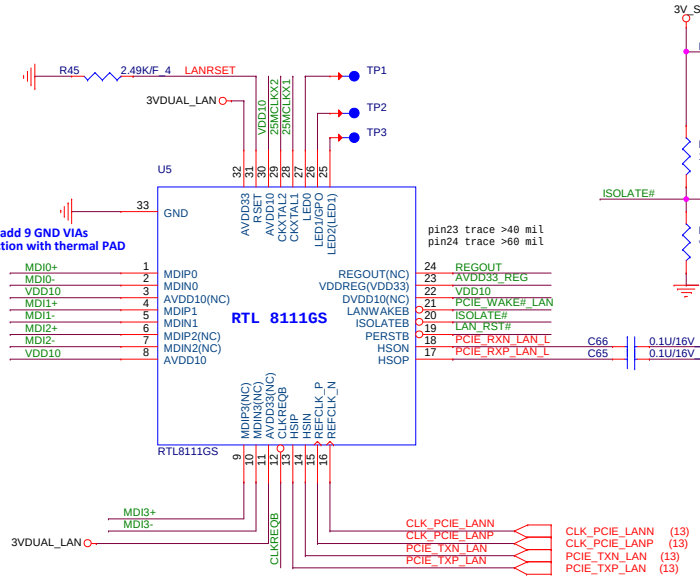
Quanta Computer Inc.

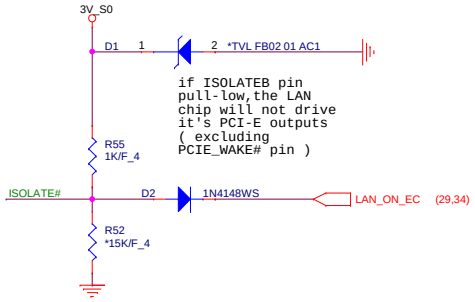
PROJECT : FH8

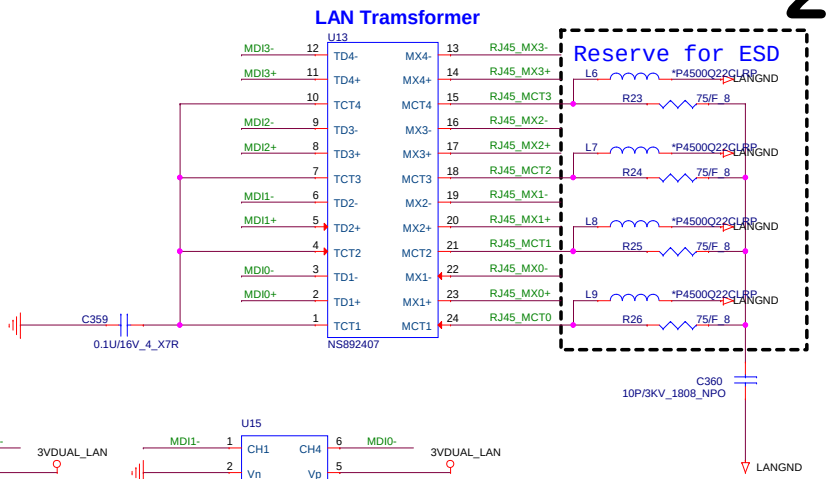
Audio Code (ALC283)

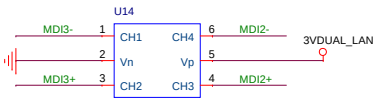
Size | Document Number | Rev 2A

Date: Friday, March 06, 2015 | Sheet 22 of 40

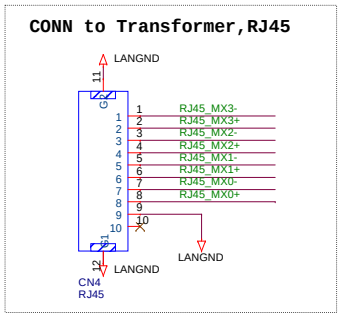






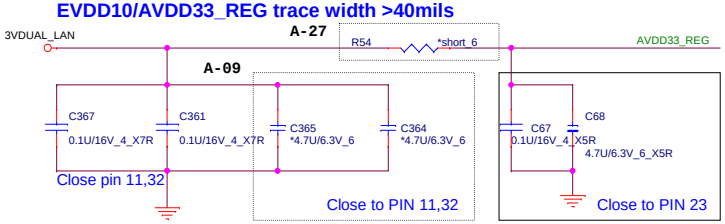


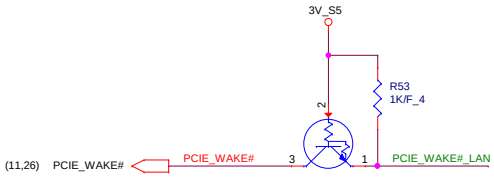
A-16
B-20



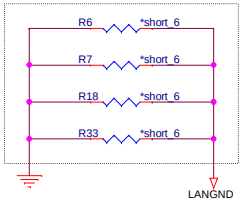
LAN POWER

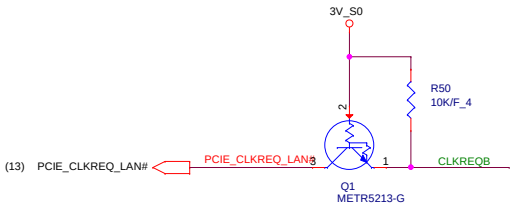
EVDD10/AVDD33_REG trace width >40mils



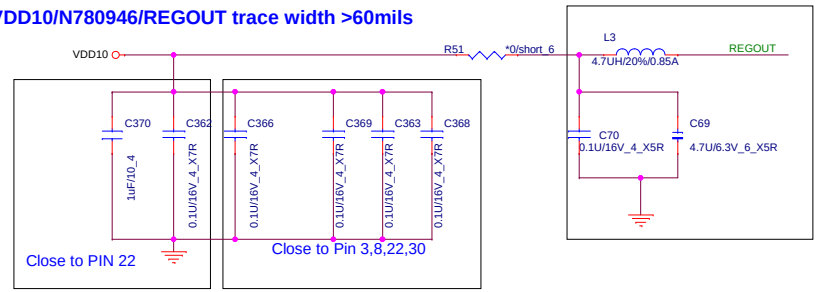


A-38

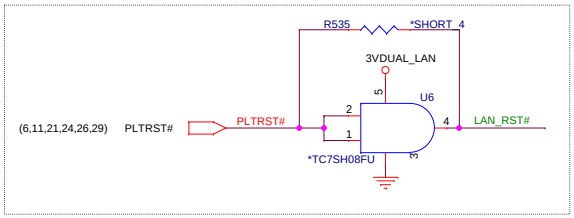


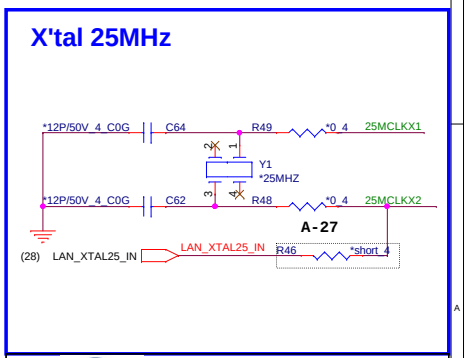


EVDD10/N780946/REGOUT trace width >60mils



B-3 C-7





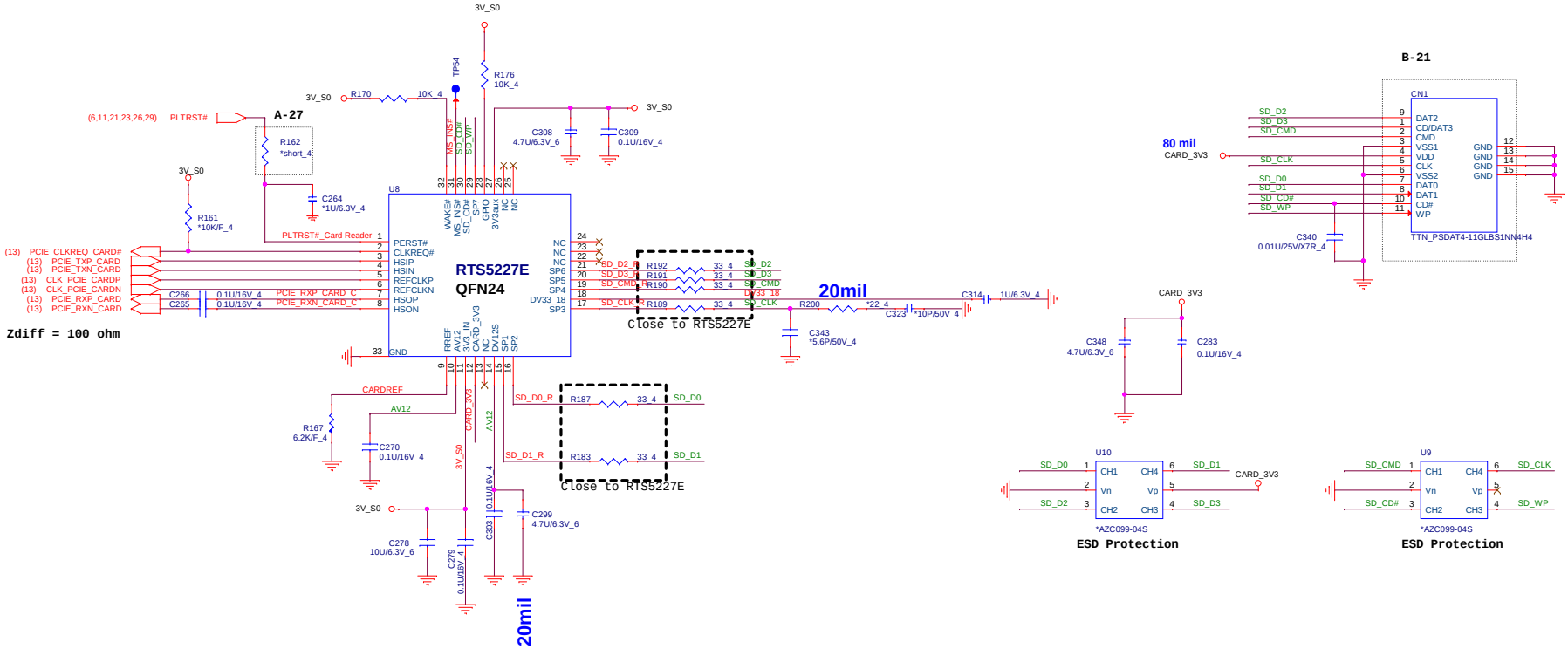
Quanta Computer Inc.

PROJECT : FH8A

Size	Document Number	Rev
	LAN RTL8111GS/RJ45 conn	2A

Date: Friday, March 06, 2015 Sheet 23 of 40

Card Reader RTS5227E



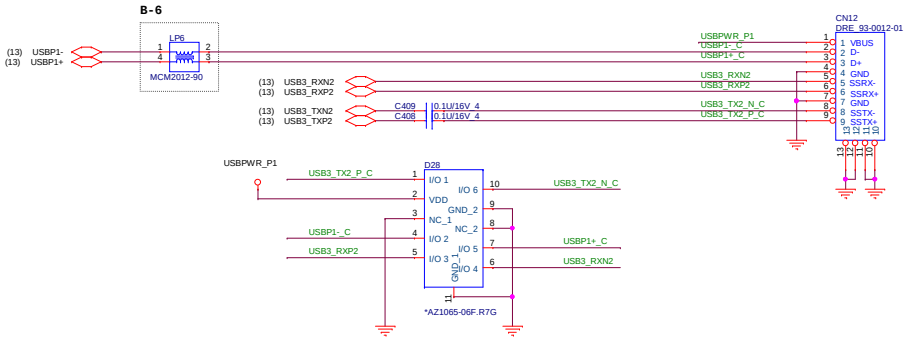
Quanta Computer Inc.

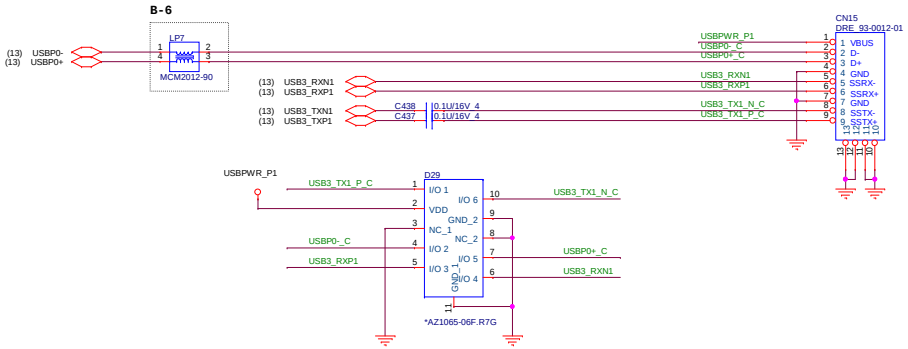
PROJECT : FH8A

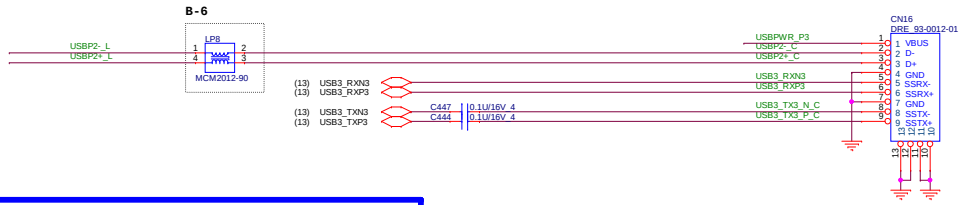
Size	Document Number	Rev
	Card reader RTS5227E	2A

Date: Friday, March 06, 2015 Sheet 24 of 40

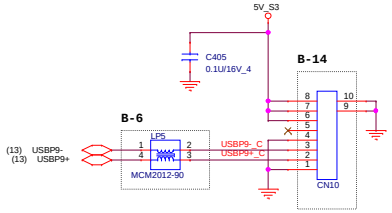
USB 3.0

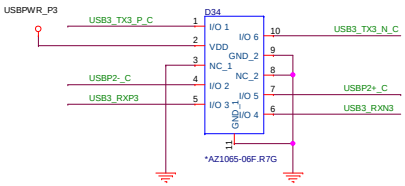


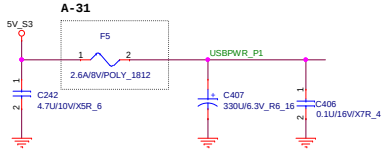




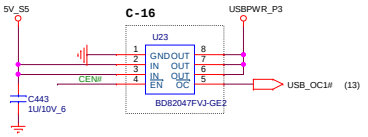
To USB/B

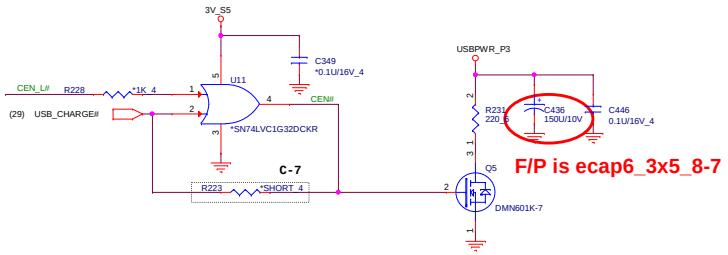


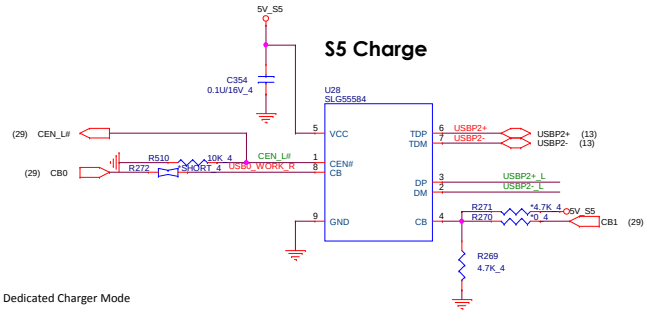




USB Charger







Force Dedicated Charger Mode

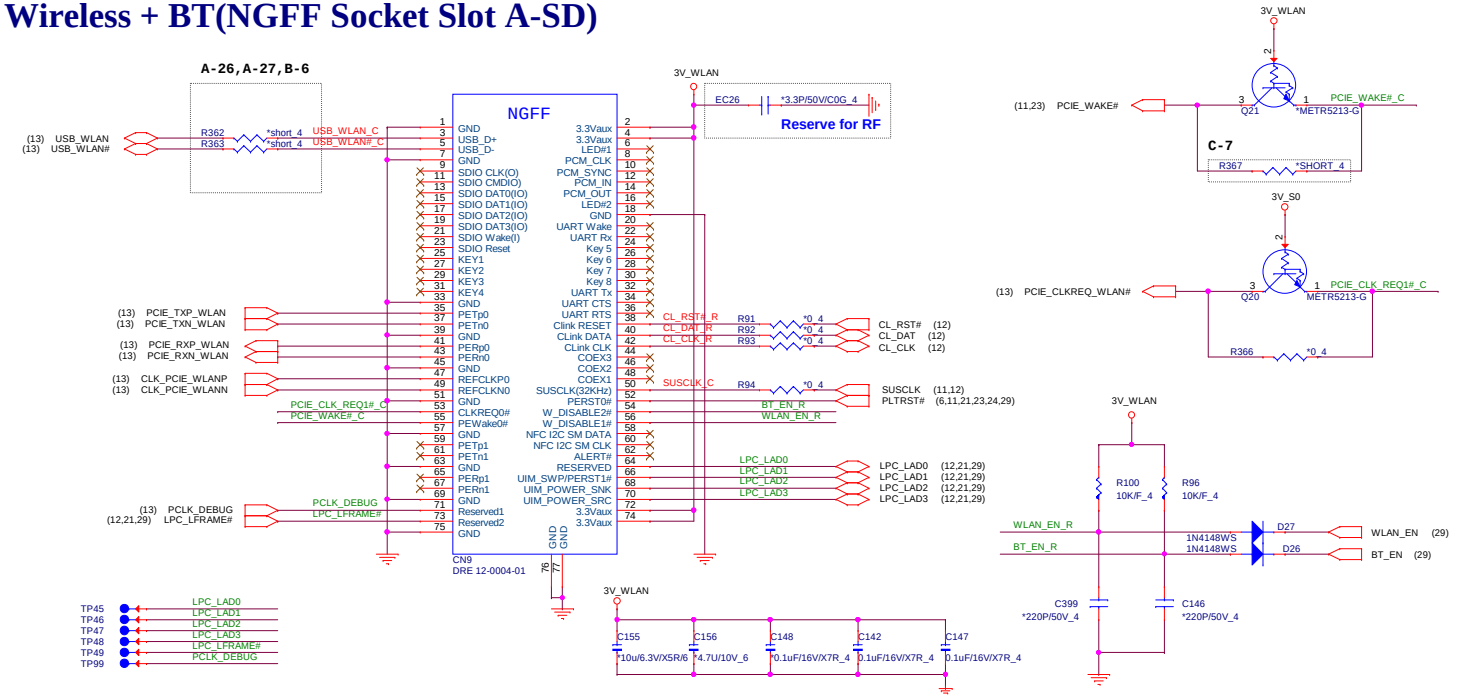
CB0	CB1	Status
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only(depending on external device) And, when Non-CDP phone is plugged in, the CDP mode will be changes automatically to SDP mode during handshaking protocol for supporting data communication.

Quanta Computer Inc.
PROJECT : FH8A

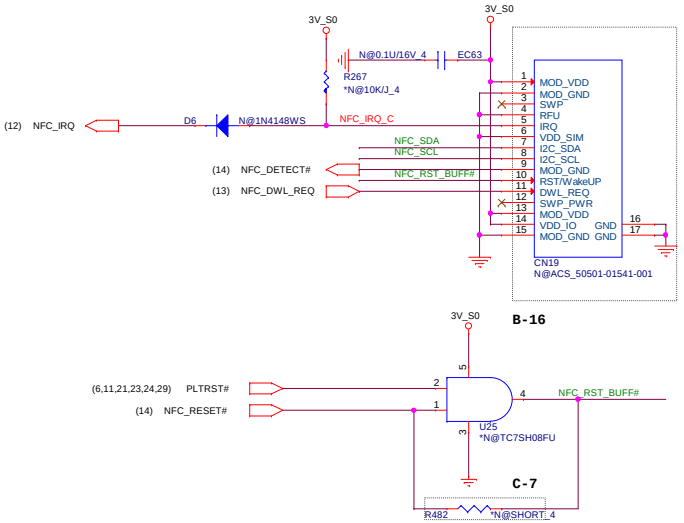
Size	Document Number	Rev
	USB3.0/Charger/USB2.0	2A

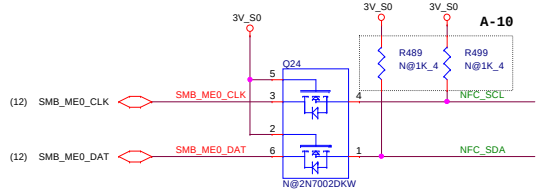
Date: Friday, March 06, 2015 Sheet 25 of 40

Wireless + BT(NGFF Socket Slot A-SD)

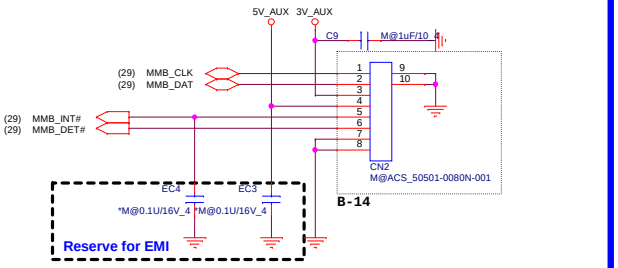


NFC

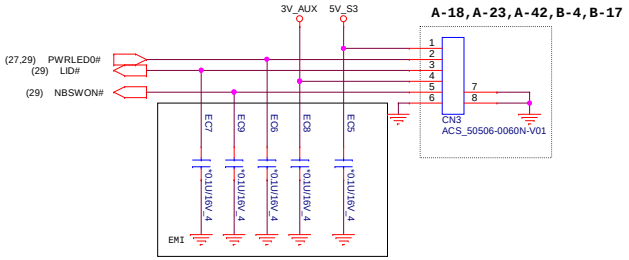




TO MMB/B



TO PWR/B



Quanta Computer Inc.
PROJECT : FH8A

Size	Document Number	Rev
	WLAN/BT/WL Dongle/MMB	2A
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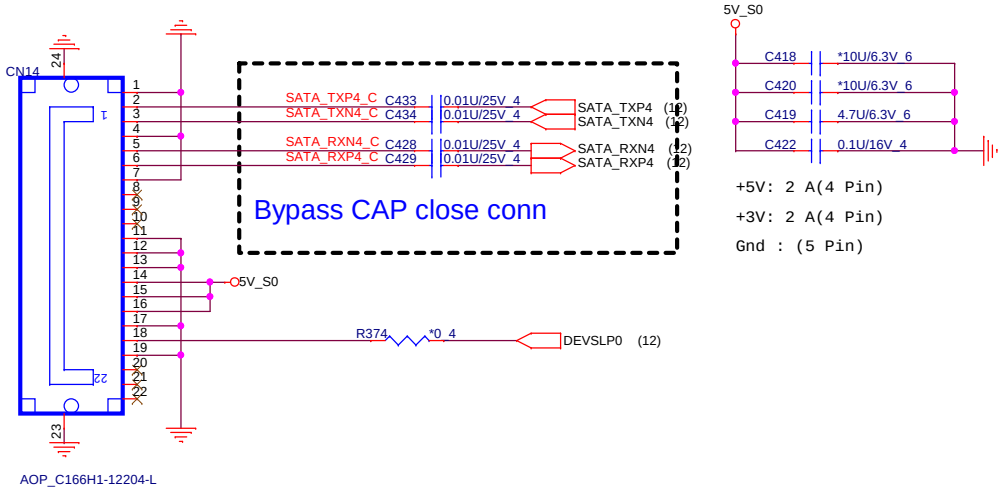
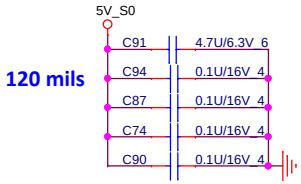
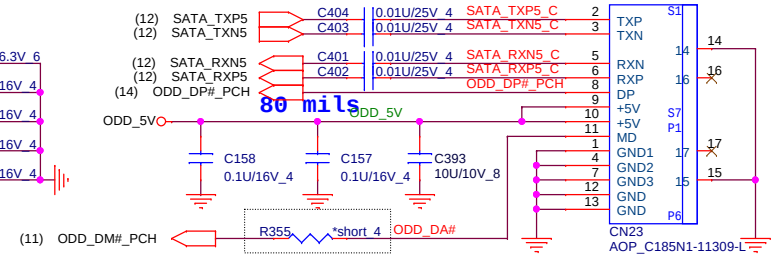
SATA HDD Connector



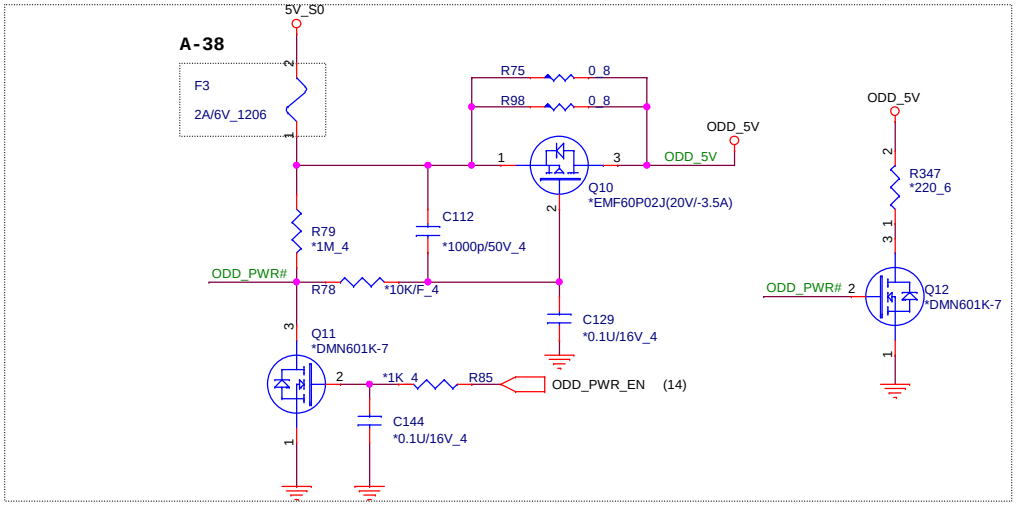
+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd : (5 Pin)

SATA ODD Connector





MP1-01 A-27



LED

B-2

CAPS LED

(29) CAPSLED# 1N4148WS D11 CAPSLED#_D LED4 WHITE CAPSLED#_R LIT_LTW-C191UC5 R274 150_6 5V_S0

WLAN

(29) LED_WLAN# 1N4148WS D7 LED_WLAN#_D LED1 WHITE LED_WLAN#_R LIT_LTW-C191UC5 R277 150_6 5V_S5

Battery

(29) BAT_LED1# 1N4148WS D12 BAT_LED1#_D R282 220_6 BAT_LED1#_R 4
(29) BAT_LED0# R280 150_6 BAT_LED0#_R 3 LED6 AMBER
LIT_LTW-C195UCKF-5A C-7
R275 *0_6 5V_S5
R281 *SHORT_6 5V_AUX

Power Status

(26,29) PWRLED0# 1N4148WS D9 PWRLED0#_D R279 150_6 PWRLED0_R# 3
(29) PWRLED1# 1N4148WS D8 PWRLED1#_D R278 220_6 PWRLED1_R# 4 LED5 WHITE WHITE
LIT_LTW-C195UCKF-5A AMBER 5V_S5

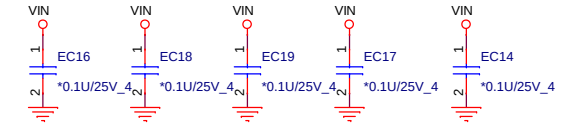
HDD/ODD

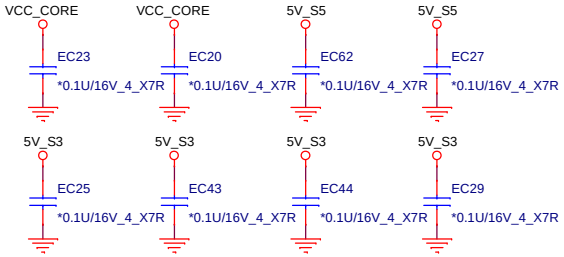
3V_S0
Q6 METR5213-G
(12) SATA_LED# SATA_LED#_D LED2 WHITE SATA_LED#_R LIT_LTW-C191UC5 R283 150_6 5V_S0

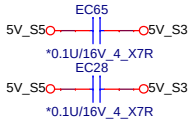
NUM LED

(29) NUMLED# 1N4148WS D10 NUMLED#_D LED3 WHITE NUMLED#_R LIT_LTW-C191UC5 R273 150_6 5V_S0

EMI







stiching cap for EMI

Quanta Computer Inc.
PROJECT : FH8A

Size	Document Number	Rev
	HDD/ODD/LED/EMI	2A
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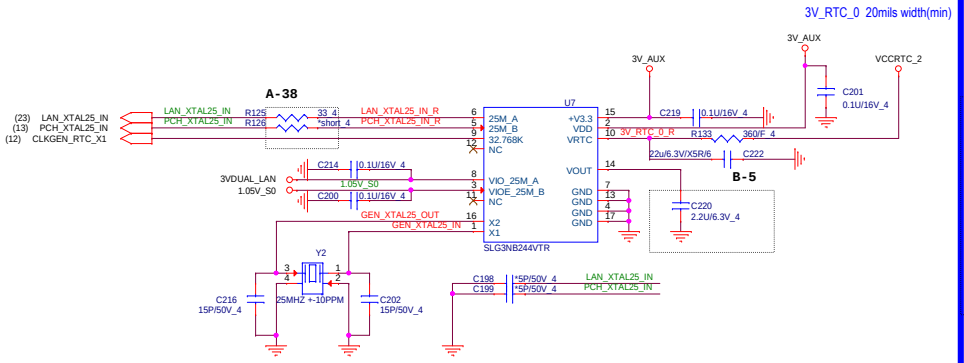
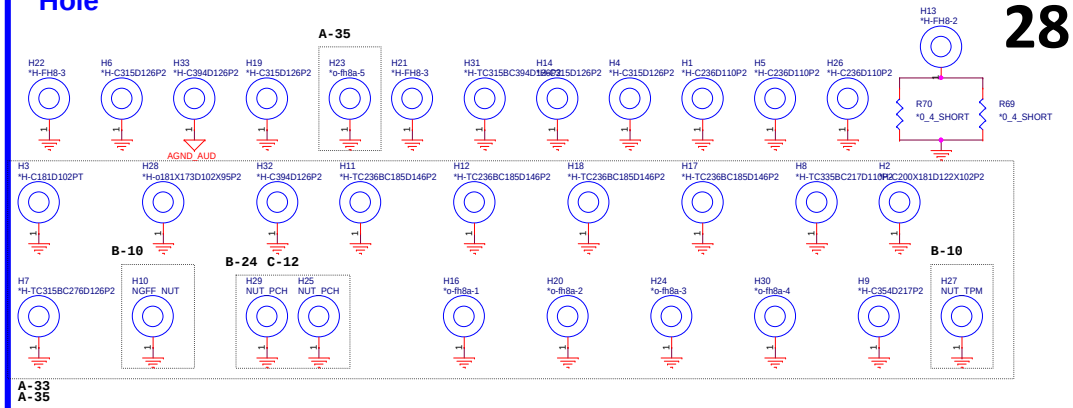
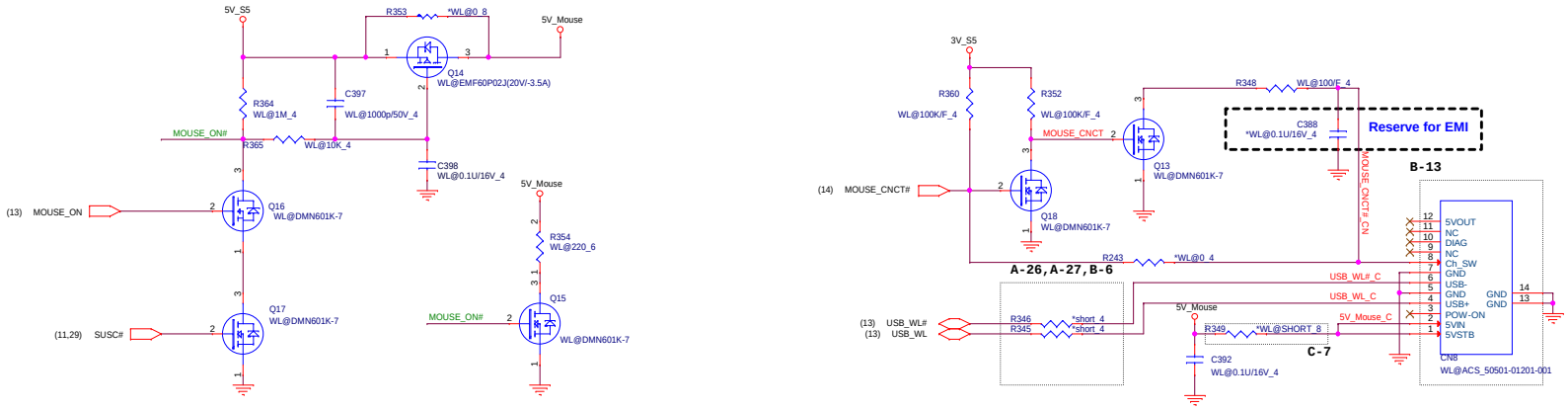
Green CLK Circuitry



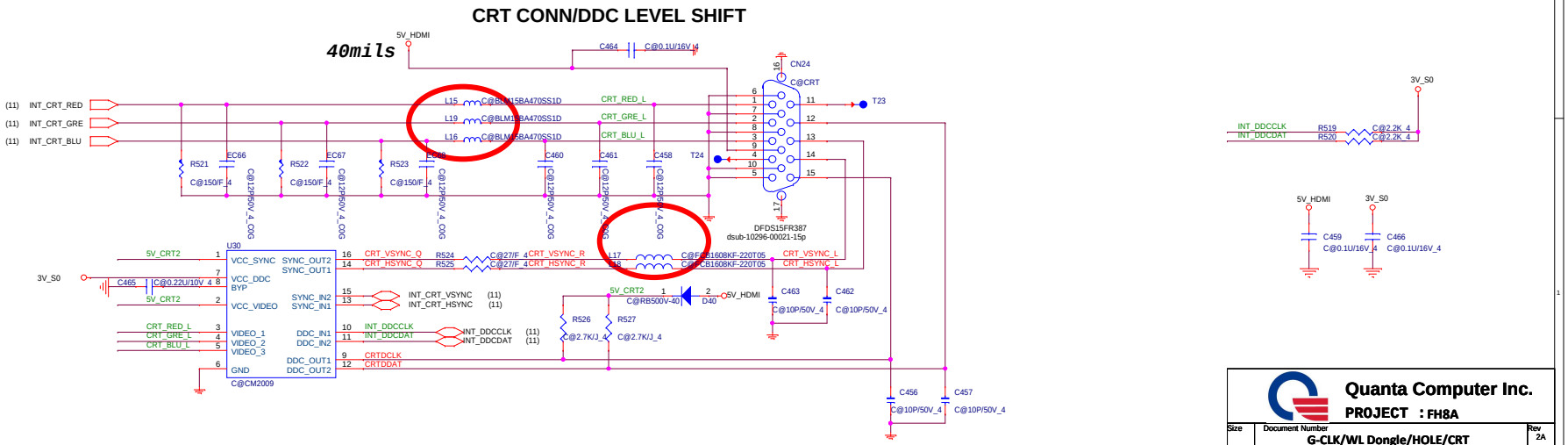
Hole



Wireless Dongle



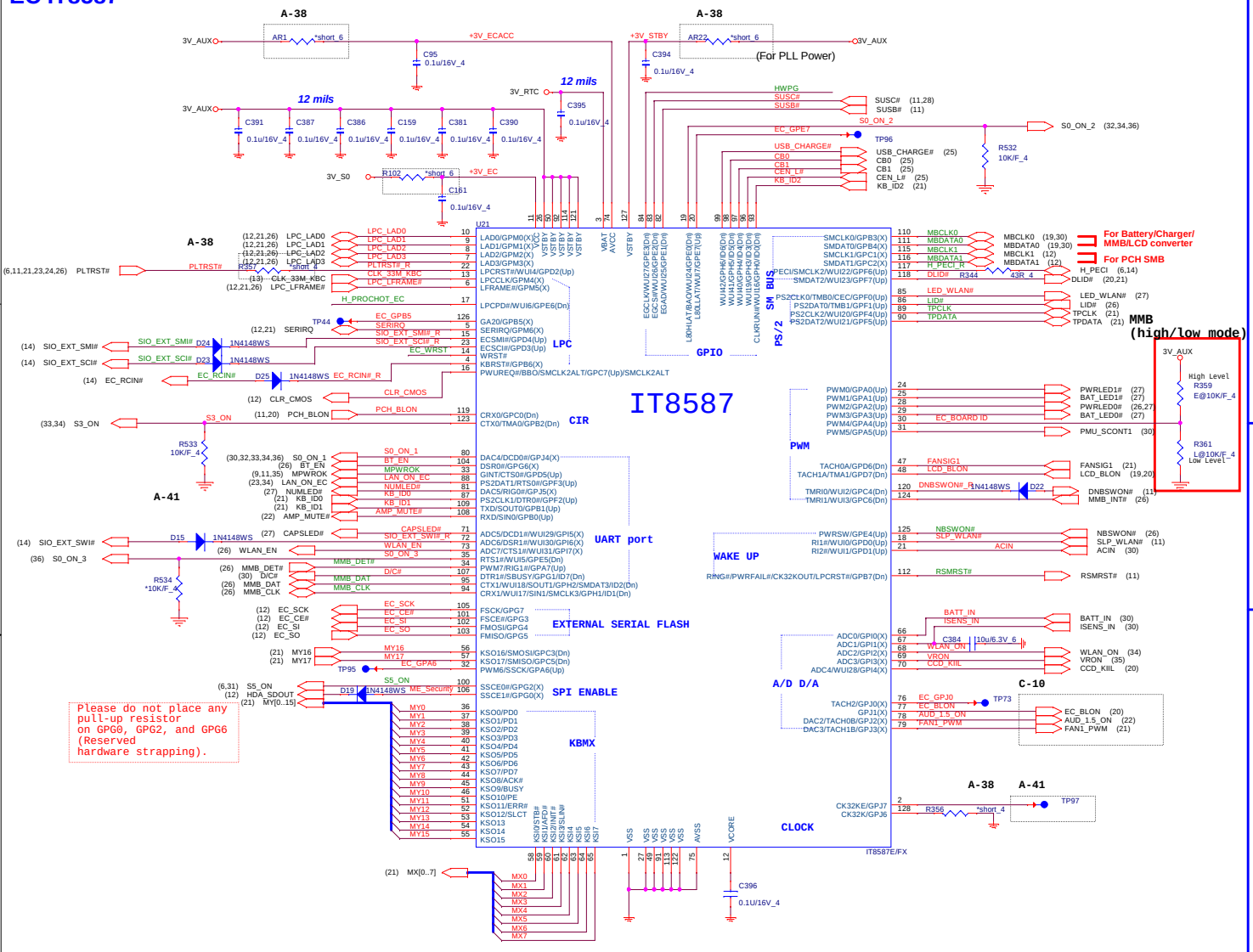
CRT PORT



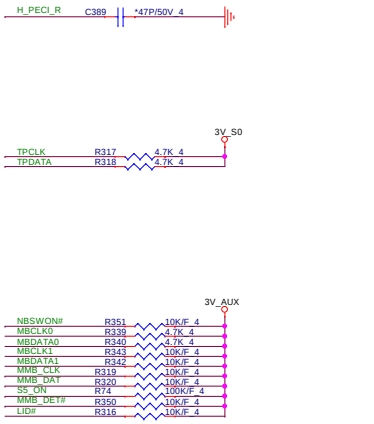
Quanta Computer Inc.
PROJECT : FH8A

Size	Document Number	Rev
	G-CLK/WL Dongle/HOLE/CRT	2A
Date: Friday, March 06, 2015	Sheet 28 of 40	

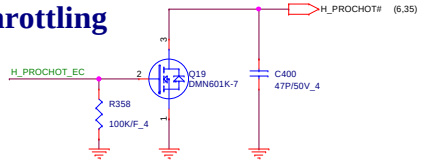
EC IT8587

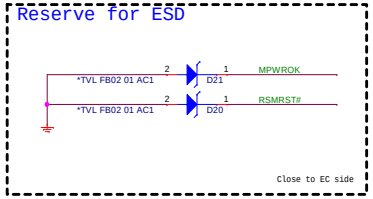


Pull Up/Dn

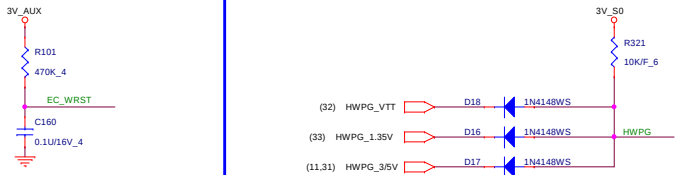


For throttling

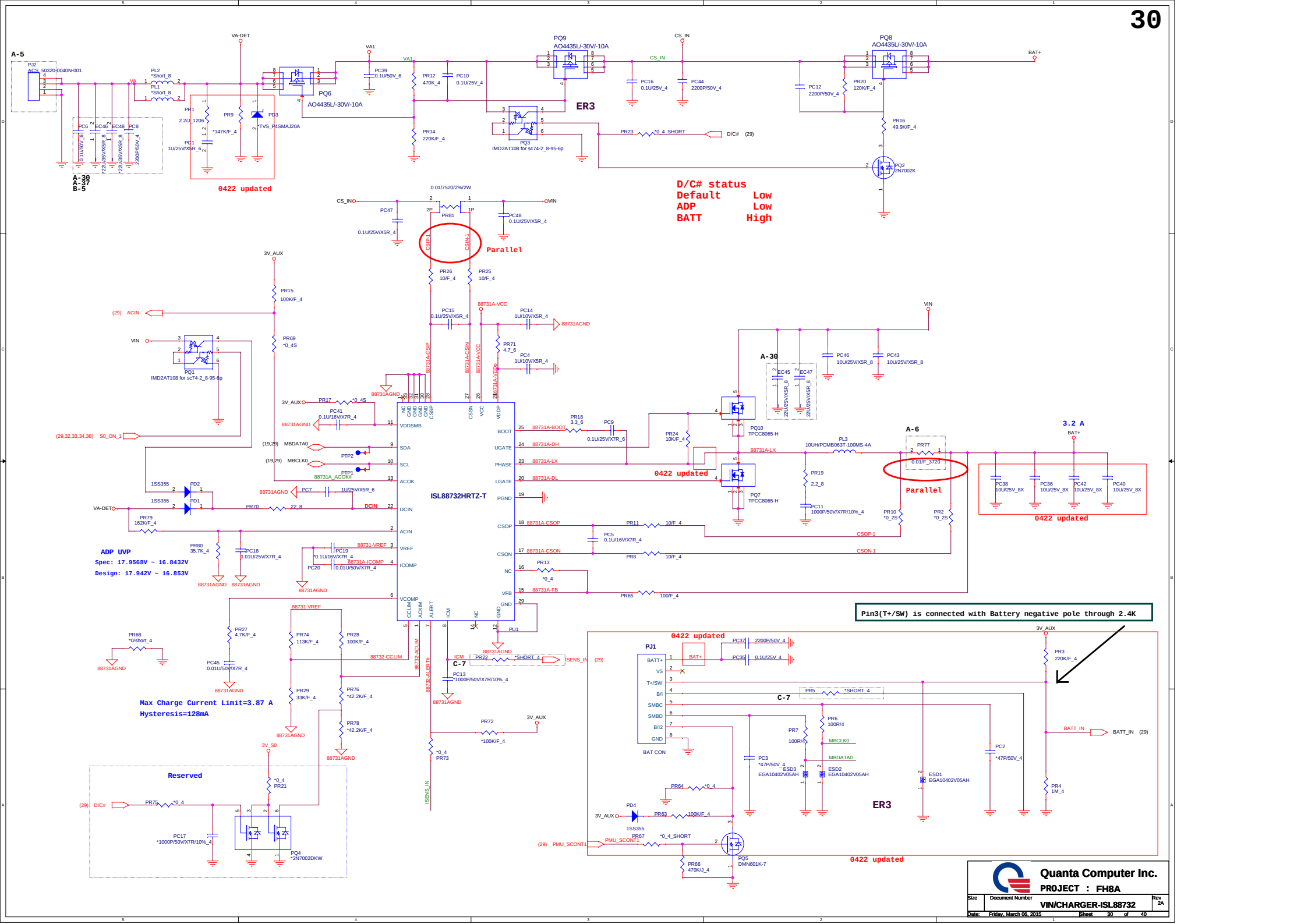




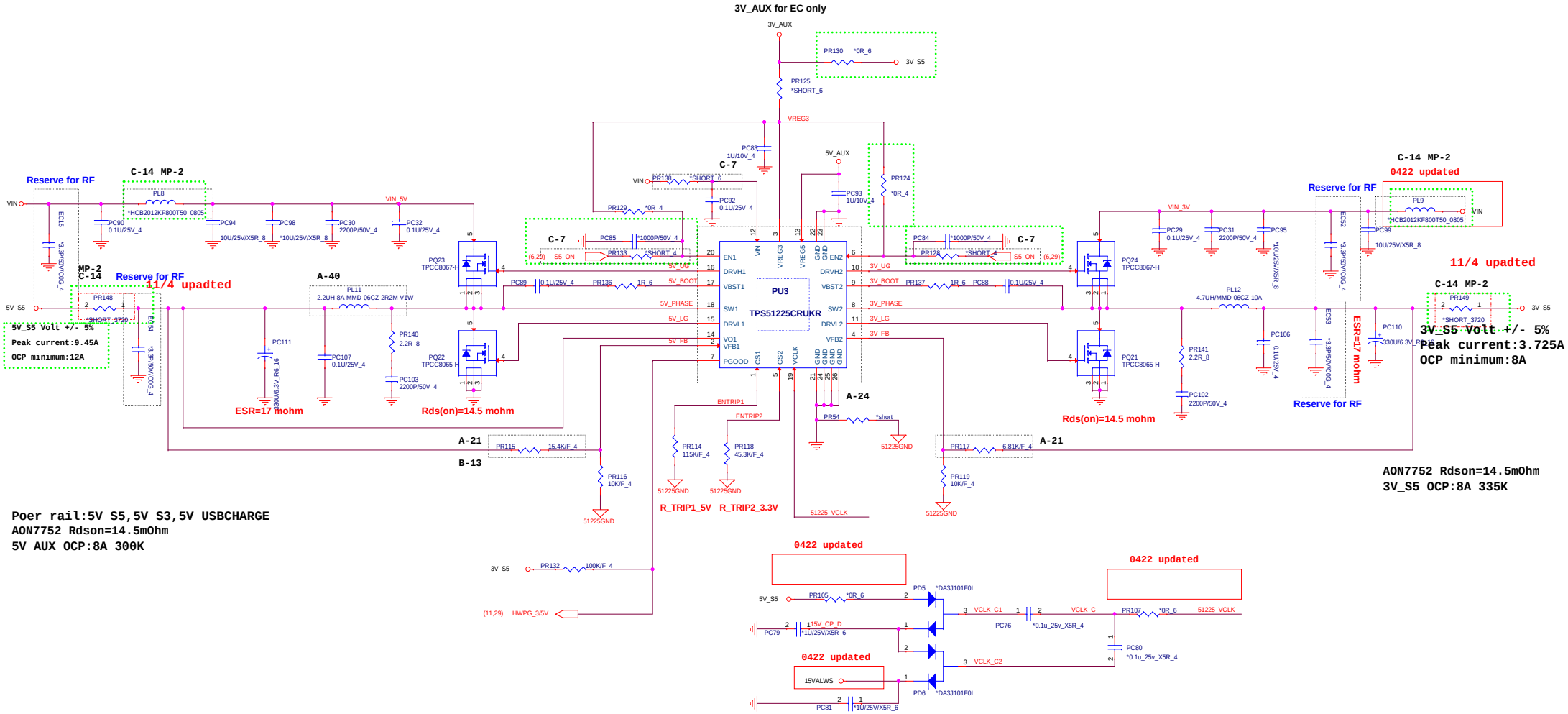
HWPG Circuit



Quanta Computer Inc.
PROJECT : FH8A
Size | Document Number: EC_IT8587E/FX | Rev 2A
Date: Friday, March 06, 2015 | Sheet 29 of 40


ISL88732HRTZ-T
ER3
Parallel
0422 updated
D/C# status
Default Low
ADP Low
BATT High
ADP UVP
Spec: 17.9568V ~ 16.8432V
Design: 17.942V ~ 16.853V
Max Charge Current Limit=3.87 A
Hysteresis=128mA
Reserved
Pin3(T+/SW) is connected with Battery negative pole through 2.4K
3.2 A
Quanta Computer Inc.
PROJECT : FH8A
VIN/CHARGER-ISL88732
Friday, March 06, 2015

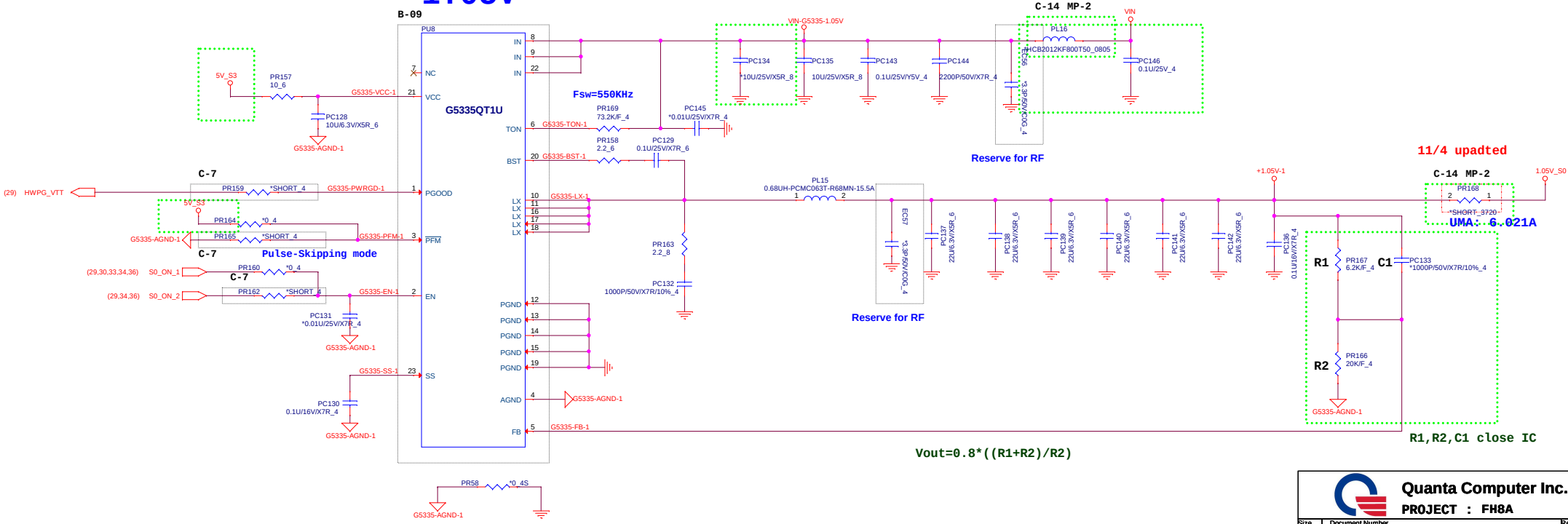
System 3V / 5V (TPS51225RUKR)



Quanta Computer Inc.			
PROJECT : FH8A			
Size	Document Number		Rev
	SYSTEM 5V/3V(TPS51225RUK)		2A
Date: Friday, March 06, 2015	Sheet 31	of 40	

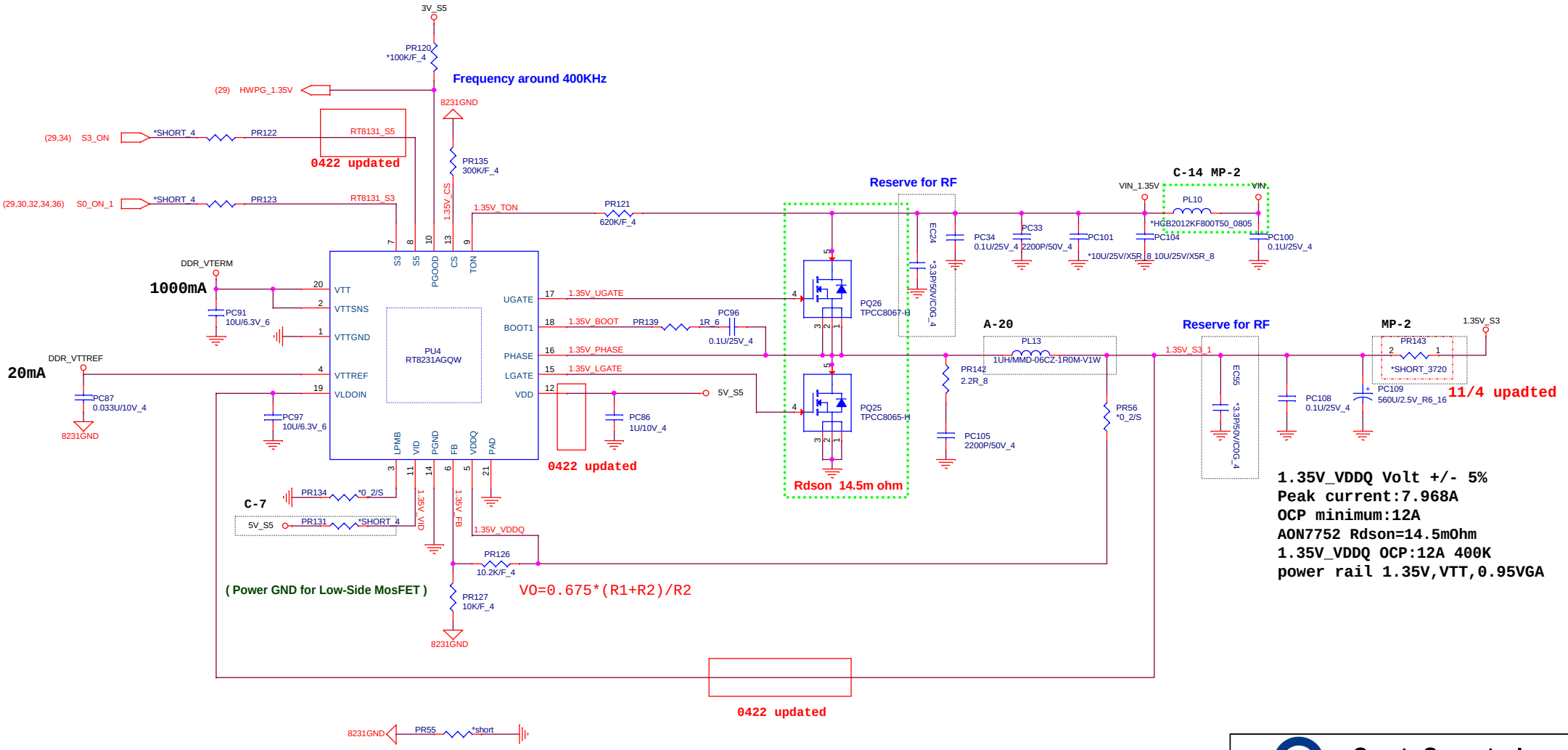
+1.05V

1.05V

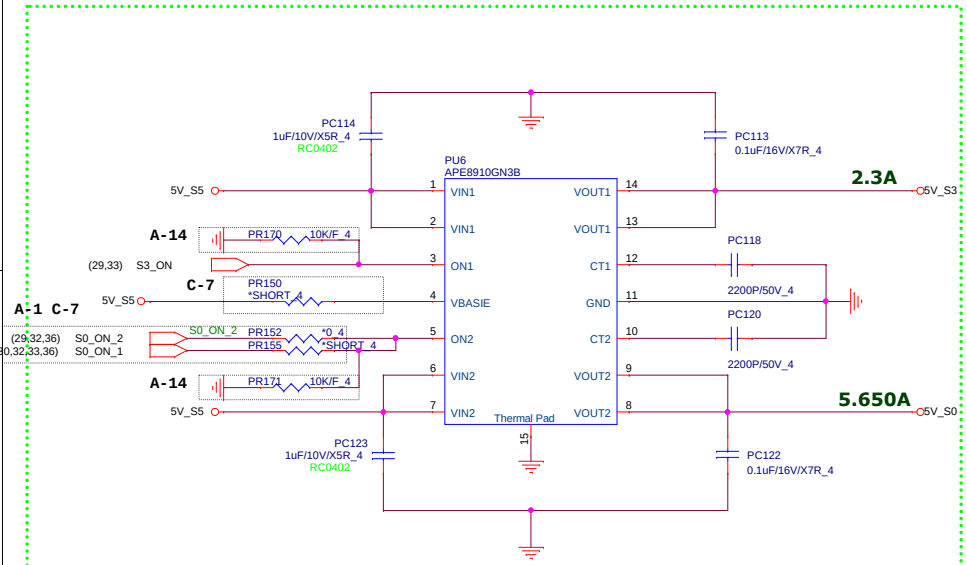


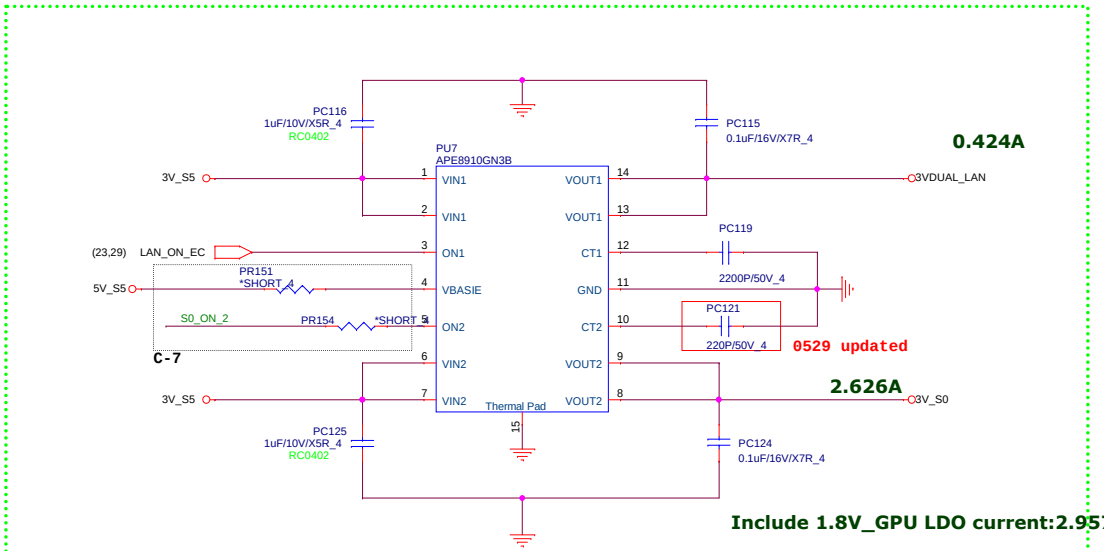
Quanta Computer Inc.		
PROJECT : FH8A		
Size	Document Number: 1.05V-G5335	Rev: 2A
Date: Friday, March 06, 2015	Sheet 32 of 40	

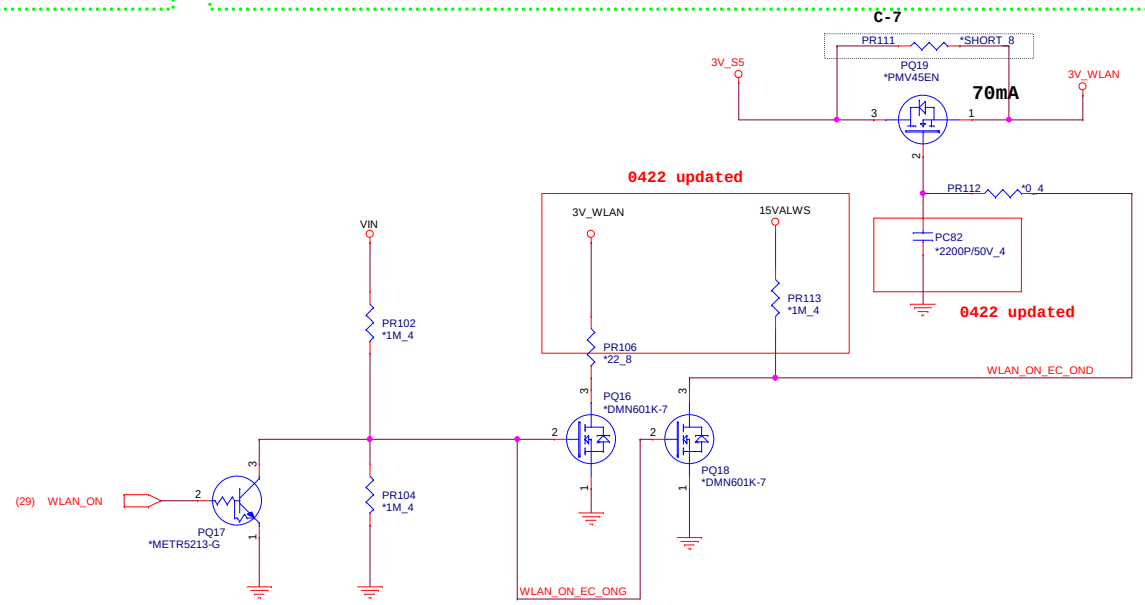
1.35V_VDDQ(RT8231AGQW)



Quanta Computer Inc.		
PROJECT : FH8A		
Size	Document Number: DDR3L 1.35V(RT8231AGQW)	Rev 2A
Date: Friday, March 06, 2015	Sheet 33 of 40	







Quanta Computer Inc.

PROJECT : FH8A

Size	Document Number	Rev
	SWITCH	2A

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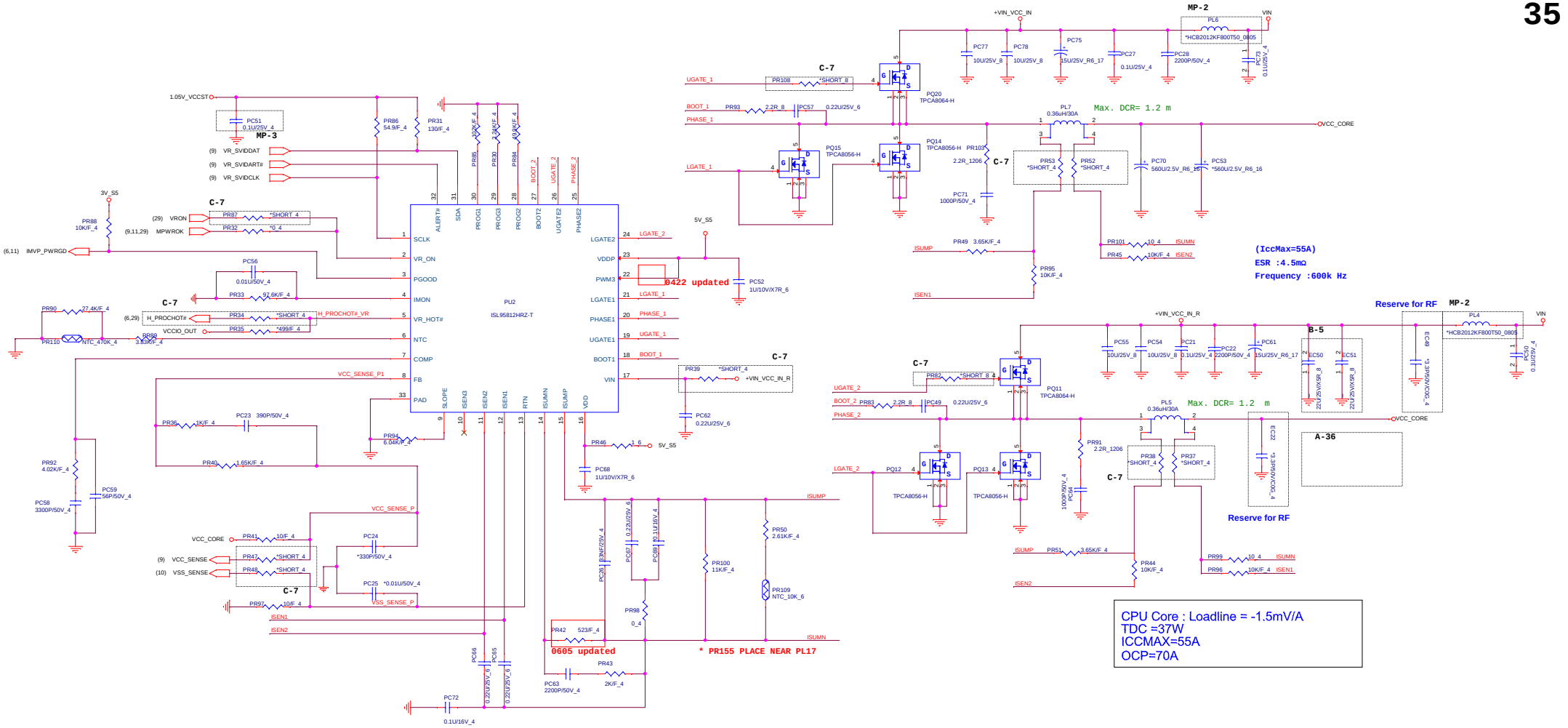
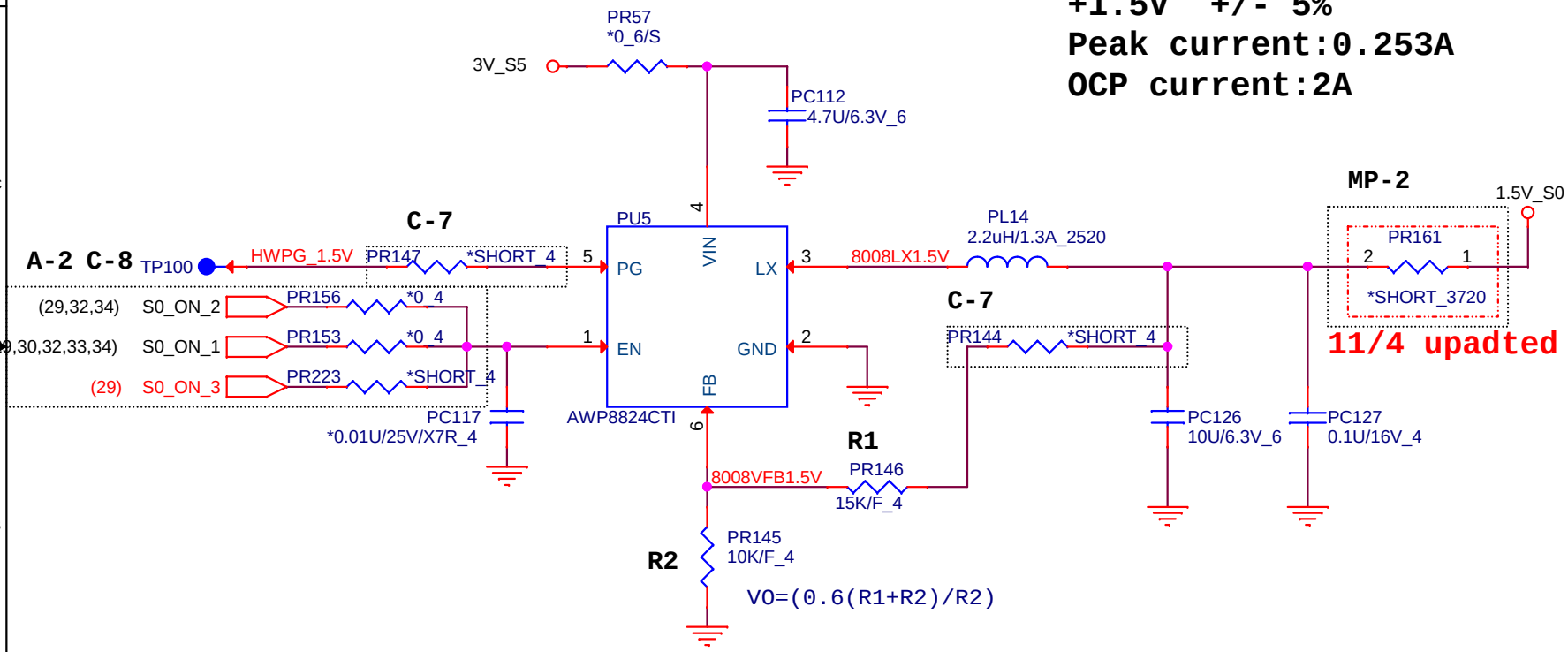
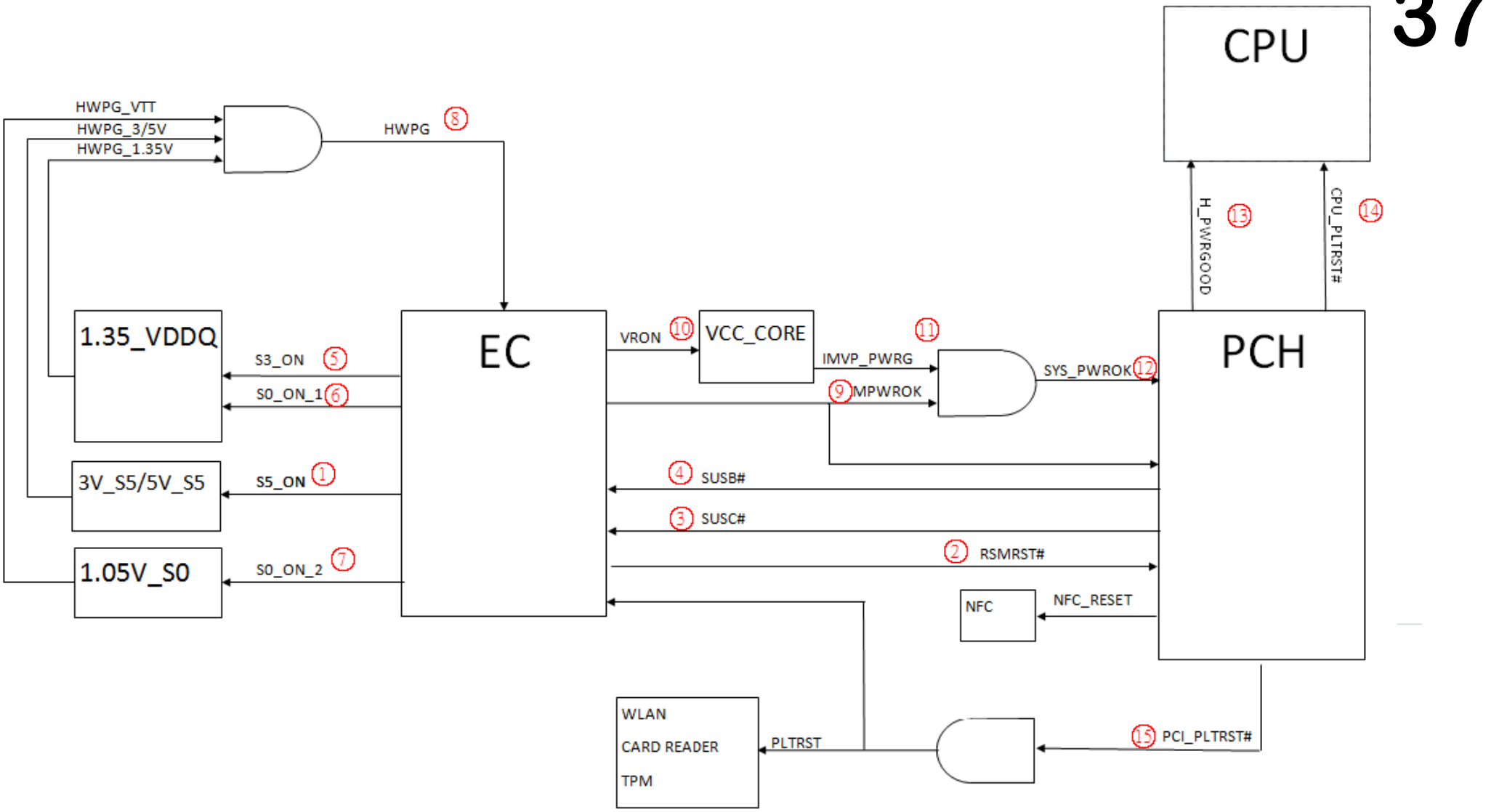


Quanta Computer Inc.	
PROJECT : FH8A	
Size	Document Number: CPU_CORE(ISL95812) 37W — Rev: 2A
Date: Friday, March 06, 2015	Sheet 35 of 40

+1.5V +/- 5%
Peak current:0.253A
OCP current:2A

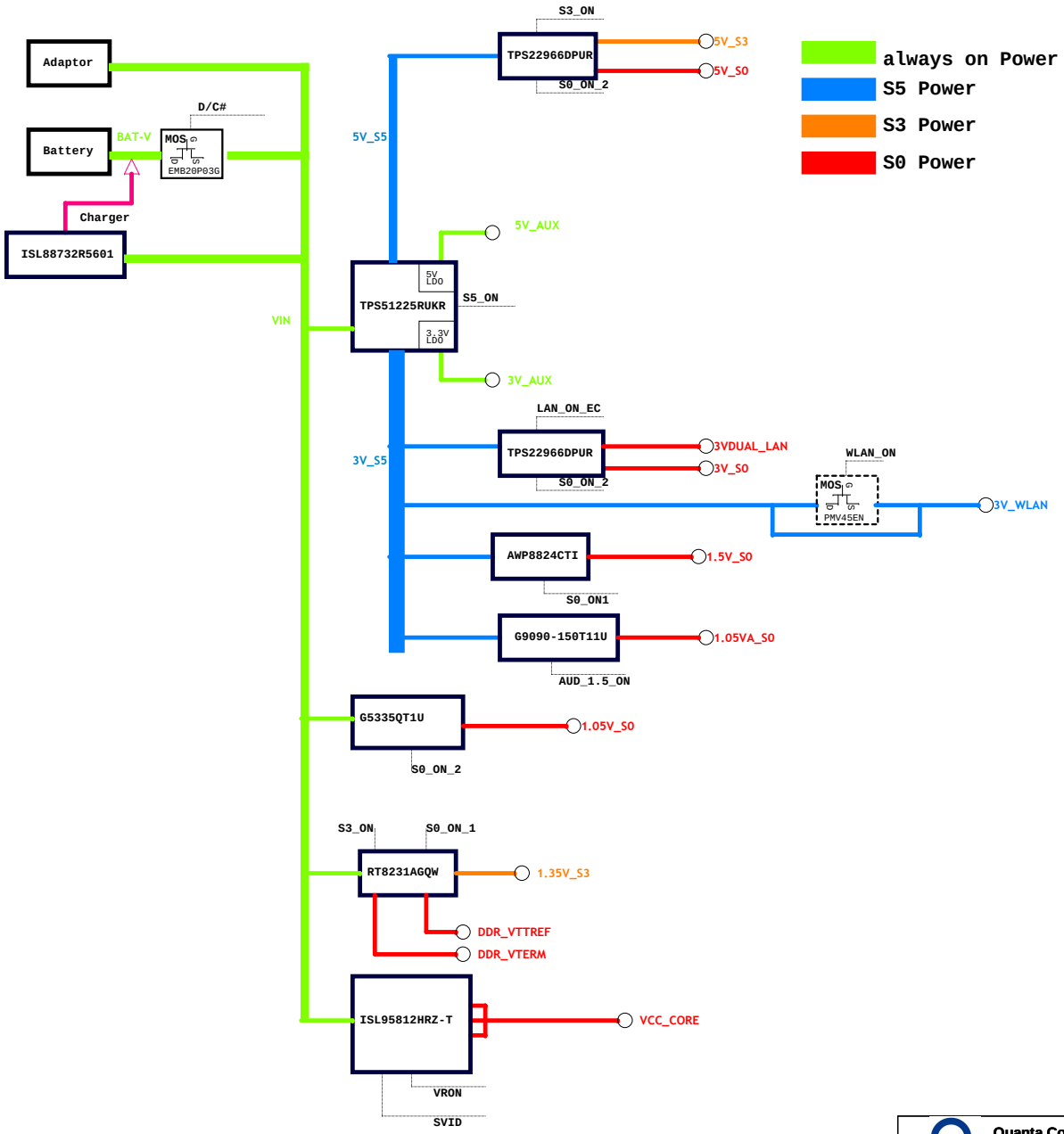


Quanta Computer Inc.		
PROJECT : FH8A		
Size	Document Number: 1.5V_S0	Rev: 2A
Date: Friday, March 06, 2015	Sheet 36 of 40	



Quanta Computer Inc.		
PROJECT : FH8A		
Size	Document Number: RESET/PWROKMAP	Rev: 2A
Date: Friday, March 06, 2015	Sheet 37 of 40	

Power Rail	Destination	Voltage
VCC_CORE	CPU VCC ---- Processor core power rail.	
1.5V_S0	PCH: VCCPLL ---- for VCCPLL provides isolated power for internal PCH PLLs PCH : +VCCAXCK_VRM for 1.5V power supply for VCC_VRM HDMI LEVEL SHIFTER : VDDTX/RX for level shifter TX/RX power Mini PCIE : +1.5V(WLAN) AUDIO : +1.5VA --- for Codec AVDD2 AUDIO : +AZA_VDD --- for Codec DVDDIO	
1.35V_S3	CPU: I/O supply voltage for DDR3L. DIMM : DDR3L power	
DDR_VTERM	DDRIII Terminator:	
1.05V_S0	PCH :PCH VccCore PCH : VccASW --- +V1.05M_VCCASW for the Active Sleep Well PCH : +V1.05S_VCCUSBCORE ---USB core PCH : +V1.05S_VCCAUX: VCCIO for GPIO/LPC IO PCH : VCCIO ---+V1.05S_VCC_EXP for FDI voltage PCH : VCCIO ---+V1.05S_VCC_EXP for USB3 voltage PCH : VCCVRM --- +V1.05S_VCCAPLL_EXP for PCIE/DMI PCH : VCCIO --- +V1.05S_VCCAPLL_EXP for SATA PCH : VCCIO --- +V1.05S_VCCAPLL_EXP for VCCMPHY PCH : VCCVRM ---+VCCAXCK_VRM for ICC PCH : VCC ---+V1.05S_VCC_AXCK_DCB for ICC PCH : VCCCLK --- +VCCCLKF135 for ICC PCH : VCCCLK --- +V1.05S_VCC_SSCFF for ICC PCH : VCCCLK --- +V1.05S_VCCSSCF100F for ICC PCH : VCCST POWER GREEN CLOCK : VIOE_25MB: for PCH 25 CLOCK VDD	PCH :VCCIO: +V1.05S_VCCAUX for GPIO/LPC PCH :VCCASW: PCH_VCC_1_1_20/21 for FUSE CPU : VCCIO_OUT --- +VCCIO_OUT_R CPU :VCCST: 1.05V_VCCST
3V_AUX	PCH: RTC EC:VSTBY KB : KB ID KB : KB ID MMB : MMB VDD HALL SENSOR : SENSOR VDD	
3V_S5	PCH: VccSus3_3 -- +VCCPRTCSUS_3P3forRTC. PCH:VCCDSW3_3 -- +VCCPDSW supply for Deep S4/S5 wells. PCH:VCCSPI -- +V3.3M_VCCPSPI for SPI PCH:VCC -- +V3.3S_VCCPFUSE for PCH fuse SPI ROM : VCC for SPI ROM WLAN: 3V_WLAN for WLAN VCC	PCH : VCCSUSHDA ---- +VCC_HDA_IO for Azalia Power. PCH :VCCSUS3_3 ---- USB3/USB2 SUS power,
3V_S0	PCH: Vcc3_3 --- for core well I/O buffers. PCH: Vcc3_3_R30/R32 --- for HVCMOS PCH: VCCCLK3_3 --- for ICC. PCH: VCC --- for FUSE. PCH: Vcc3_3 --- for THERMAL. **DDR3: SPDVDD** **VGA Port Companion Circuit** **HDMI LEVEL SHITER POWER** **LVDS power** **CCD power**	**TOUCH PAD POWER** **TPM power** **Card reader(RTS5227E)power** **NFC POWER** **EC: VCC**
3V_WLAN	Mini PCIE : 3V power	
3VDUAL_LAN	LAN Power	
5V_AUX		
5V_S5	USB CHARGER : USB CHARGER POWER WL DONGLE: WL DONGLE POWER	
5V_S3	USB2.0 power TTOUCH SCREEN POWER	
5V_S0	FAN power HDMI power pin HDD power ODD power Audio codec IC power VGA power pin	
VIN	CONVERTER power	
BAT-V		



Quanta Computer Inc.
PROJECT : FH8A
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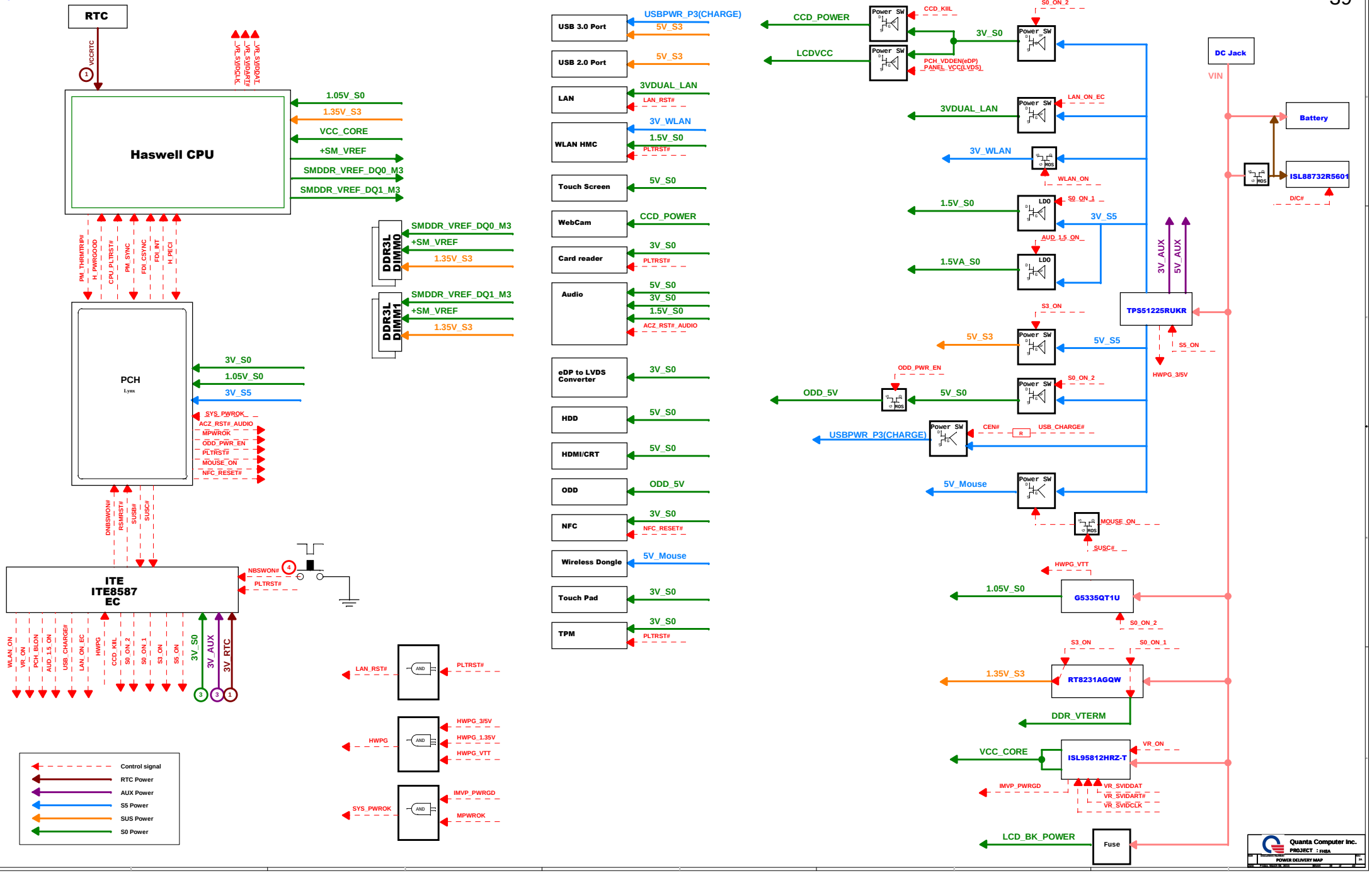
RTC
VCCRTC
VR_SVIDDAT
VR_SVIDCLK
Haswell CPU
1.05V_S0
1.35V_S3
VCC_CORE
+SM_VREF
SMDDR_VREF_DQ0_M3
SMDDR_VREF_DQ1_M3
PW_THRMTRIP#
H_PWRGOOD
CPU_PLTRST#
PW_SYNC
FDI_CSYNC
FDI_INT
H_PECI
DDR3L DIMM0
DDR3L DIMM1
PCH
Lynx
3V_S0
1.05V_S0
3V_S5
SYS_PWROK
ACZ_RST#_AUDIO
MPWROK
ODD_PWR_EN
PLTRST#
MOUSE_ON
NFC_RESET#
DNBSWON#
RSMRST#
SUSB#
SUSC#
ITE
ITE8587
EC
NBSWON#
PLTRST#
WLAN_ON
VR_ON
PCH_BLON
AUD_1.5_ON
USB_CHARGE#
LAN_ON_EC
HWPG
CCD_KIL
S0_ON_2
S0_ON_1
S3_ON
S5_ON
3V_S0
3V_AUX
3V_RTC
Control signal
RTC Power
AUX Power
S5 Power
SUS Power
S0 Power
LAN_RST#
PLTRST#
HWPG
HWPG_3/5V
HWPG_1.35V
HWPG_VTT
SYS_PWROK
IMVP_PWRGD
MPWROK
AND
USB 3.0 Port
USBPWR_P3(CHARGE)
5V_S3
USB 2.0 Port
5V_S3
LAN
3VDUAL_LAN
LAN_RST#
WLAN HMC
3V_WLAN
1.5V_S0
PLTRST#
Touch Screen
5V_S0
WebCam
CCD_POWER
Card reader
3V_S0
PLTRST#
Audio
5V_S0
3V_S0
1.5V_S0
ACZ_RST#_AUDIO
eDP to LVDS Converter
3V_S0
HDD
5V_S0
HDMI/CRT
5V_S0
ODD
ODD_5V
NFC
3V_S0
NFC_RESET#
Wireless Dongle
5V_Mouse
Touch Pad
3V_S0
TPM
3V_S0
PLTRST#
CCD_POWER
LCDVCC
Power SW
CCD_KIL
3V_S0
PCH_VDDEN(eDP)
PANEL_VCC(LVDS)
S0_ON_2
3VDUAL_LAN
LAN_ON_EC
3V_WLAN
WLAN_ON
1.5V_S0
S0_ON_1
3V_S5
AUD_1.5_ON
1.5VA_S0
LDO
DC Jack
VIN
Battery
ISL88732R5601
DIC#
3V_AUX
5V_AUX
TPS51225RUKR
S3_ON
5V_S3
5V_S5
S5_ON
HWPG_3/5V
ODD_PWR_EN
ODD_5V
5V_S0
S0_ON_2
USBPWR_P3(CHARGE)
CEN#
R
USB_CHARGE#
5V_Mouse
MOUSE_ON
SUSC#
HWPG_VTT
1.05V_S0
G5335QT1U
S0_ON_2
S3_ON
S0_ON_1
1.35V_S3
RT8231AGQW
DDR_VTERM
VCC_CORE
ISL95812HRZ-T
VR_ON
IMVP_PWRGD
VR_SVIDDAT
VR_SVIDART#
VR_SVIDCLK
LCD_BK_POWER
Fuse
Quanta Computer Inc.
PROJECT : FHBA
POWER DELIVERY MAP

Change List

Item	Stage	Page	Owner	Change explanation
01	Pre A->A	34	EE	Change control signal from S0_ON_2 to S0_ON_1 for meet intel DGS power sequency
02	Pre A->A	36	EE	Change 1.5V_S0 controled by S0_ON_3
03	Pre A->A	22	EE	Un-stuff PC196/PR222/PC196/PU10/PC197 stuff AR36 for audio codec 1.5V power change to 1.5V_S0
04	Pre A->A	22	PWR	Change CN18 to 10 pin & add sleeve, ring2 pin for MIC cross talk issue
05	Pre A->A	30	PWR	Change PJ2 pin define for FJ in common use
06	Pre A->A	30	PWR	Change PR77 from to CS+0018FL00 to CS+0108GL13 for battery charge function
07	Pre A->A	19	EE	Change U4 DGND to GND for LVDS no display
08	Pre A->A	21	EE	CN7 reverse pin define for keyboard assembly
09	Pre A->A	23	EE	Un-stuff C364 & C365 for vender suggest
10	Pre A->A	26	EE	Change R489/R490 from 2.2K to 1K ohm for NFC fast mode.
11	Pre A->A	12	EE	Change R477/R481 from 2.2K to 499 ohm for NFC fast mode.
12	Pre A->A	20	EE	Change LCD conn power & signal pin define to avoid RTD2132 damaged.
13	Pre A->A	22	PWR	change the CN18 to 10 pins for Audio CONN change
14	Pre A->A	34	PWR	Add PR170,PR171 for S3_ON/S0_ON_2 PD for pulse issue.
15	Pre A->A	20	EE	un-stuff R1,R2, stuff R5 for LVDS BOM for H/W C/D.
16	Pre A->A	23	ME	Modify CN4 pin define, pin10 NC.
17	Pre A->A	12	EE	R307 for EC clear CMOS.
18	Pre A->A	26	ME	change CN3 FP to 50506-00641-v01-6p-l
19	Pre A->A	21	ME	change CN5 to DFHD10MS119 and reverse pin define.
20	Pre A->A	41	PWR	Change PL13 to CV-10M0MZ02 for Standard part
21	Pre A->A	31	PWR	Change PR115 to 15.8K and PR117 to 6.8K ohm for adjust 5V_S5/3V_S5 voltage
22	Pre A->A	22	PWR	Change PR114 to 15K and PR112 to 16.18K ohm for adjust 5V_S5/3V_S5 voltage
23	Pre A->A	21,26	ME	change PWR CONN(CN3) to DFFC06FR106 , High SKU KB CON(CN6) to DFFC30FR091
24	Pre A->A	31	PWR	change PU11 to TPS51225CRUKR(AL051Z50001) for MMB/Battery LED
25	Pre A->A	15	EE	Add C470 22uF cap to reduced 1.5V_S0 ripple noise
26	Pre A->A	26,28	EE	Un-stuff USB LP3,LP4 for C/D
27	Pre A->A	06,07,09, 14,20,23, 24,26,27, 28	EE	Change R29,R32,R46,R54,R59,R90,R103,R162,R179,R184,R301,R304,R306,R308,R322,R355, R362,R363,R345,R346 to short pad.
28	Pre A->A	13,15,21	EE	Remove R184,R370,R485,R486 for C/D
29	Pre A->A	09	PWR	Stuff and rename C374 to PC374 and change C81,C82,C83,C84,C76,C79,C98,C104,C101,C102,C103, C133,C134,C138 to CH622IM9900 CAP 22U 6.3V for improve VccCore power quality
30	Pre A->A	30	EMI	Stuff EC45 EC47 EC48 for EMI issue.
31	Pre A->A	25	EE	Change F5 to DK260TPU003 polymer type
32	Pre A->A	13	EE	Correct net name to PCH_XTAL25_IN
33	Pre A->A	28	ME	Change H25, H29 Nuts to MBFH8001010
34	Pre A->A	09	EE	Un-stuff R59 to meet Intel EDS
35	Pre A->A	28	EE	Change H3,H7,H8,H16,H20,H23,H24,H25,H28,H29,H30 footprint for layout require
36	Pre A->A	35	PWR	Remove PC60,PC74 for layout spaceing require(PC60,PC74 not used)
37	Pre A->A	30	EMI	Change EC48 EC46 to CH6225M9A00 CAP CHIP 22UF 35V(+-20%,X5R,0805) for EMI input inrush issue
38	Pre A->A	06,09,11 13,15,22 23,28,27 29	EE	Change R88,R61,R446,R463,F3,R380,R395,R311,R325,R390,R401,R393,R6,R7,R18,R33,AR6,AR3,AR4, AR1,AR22,R102,R357,R356,R126 to short pad.
39	Pre A->A	20	EE	Change CN22 footprint to 51519-04001-001-40P-1 due to vendor P/N was change
40	Pre A->A	31	PWR	Change the PL11 to CV-2280MZ05 IND SMD 2.2UH 20% 8A MMD-06CZ-2R2M-V1W for the current load
41	Pre A->A	29	EE	Change CLR_CMOS Trace from U21 PIN2 to U21 PIN16
42	Pre A->A	21	EE	Change CN7 footprint from 50696-0300n-001-30p-l to 50541-0300n-001-30p-l
43	Pre A->A	26	EE	Change CN3 footprint from 50696-0060n-v02-6p-l to 196479-06041-3-6p-l

Item	Stage	Page	Owner	Change explanation
				B Stage
01	A -> B	01	EE	Current block diagram discription from Boardwell-H to Haswell-H
02	A -> B	27	EE	Change R273,R274,R277,R279,R280,R283 to 150 ohm for LED brightness.
03	A -> B	26	ME	Change CN3 to DFFC06FR050 for ASSY. line request ME change connector type.
04	A -> B	30,35	EMI	Stuff the EC50 and EC51 and de-pop EC48 for EMI issue.
05	A -> B	20,21,25,26 28	SMT	Delete R284,R285,R286,R287,R373,R375,R416,R421,R480,R490,R368,R369,LP3,LP4 for SMT suggest
06	A -> B	12	EE	Stuff Q32 and un-stuff R307 for CLR_CMOS funtion
			EMI	Change AR2,AR10,AR14,AR16,AR17 to shortpad for C/D
07	A -> B	22		
08	A -> B	27	EE	Delete R276 and 3V_S5 for Battery LED power
09	A -> B	32	PWR	Delete PU8 pin 24,25 for F/P change
10	A -> B	28	PWR	change H10 to H-TC217BC185D146P2,H27 to H-TC256BC197D150P2
11	A -> B	22	PWR	AR5 / AR23 swap with AL6 / AL7 for audio pop noise.
12	A -> B	22	PWR	Change AR2,AR10,AR14,AR16,AR17 to 0ohm for debug.
13	A -> B	28	ME	CN8 change PN to DFFC12FR117 & DFFC12FS000 , and F/P to 50501-01201-001-12p-l for ME request.
14	A -> B	26	ME	CN2,CN10 change PN to DFFC08FR093 & DFFC08FR055,F/P to 50501-0080n-001-8p-l for ME request.
15	A -> B	22	ME	CN18 change PN to DFFC10FR123,F/P to 51619-0100n-001-10p-l for ME request.
16	A -> B	26	ME	CN19 change PN to DFFC15FR010 & DFFC15FR013, F/P to 50501-01541-001-15p-l for ME request.
17	A -> B	26	ME	CN3 change PN to DFFC06FR177 & DFFC06FR172,F/P to 50506-0060n-v01-6p-l for ME request
18	A -> B	21	ME	CN20 add 2nd source PN DFFC06FR179 for ME request
19	A -> B	21	ME	CN5 change to DFHD10MS236 & DFHD10MS235 for ME request
20	A -> B	23	ME	CN4 change to DFHD10MS237 & DFHD10MS238, F/P to 50273-01001-001-10p-l for ME request
21	A -> B	24	ME	CN1 DFHD11MR028 EOL, change to DFHD11FR163
22	A -> B	21	ME	CN13 change to DFHS12FS032,F/P to 50169-01241-002-12p-ldh for SMT add Mylar
23	A -> B	20	EE	change F1 to DK200UFU002 & DK200UFU006 for STD part.
24	A -> B	21	ME	change H25,H29 to MBFH8002010 for Me change.
25	A -> B	12	EE	un-stuff Y4,R426,C440,C442 for cancel reserve X'tal function.
				C Stage
01	B -> C	9,14	EE	un-stuff U18,C382,C389,R413,C378,C377,change R304,R322,R308 to 0ohm and un-stuff for HSW.
02	B -> C	6	EE	un-stuff U19,C385,R334,R331 for cost down.
03	B -> C	23	EE	un-stuff U6,add R535 for cost down
04	B -> C	11,13	EE	change RP1,RP2 to 0402 resistor(R536~R550) for cost down
05	B -> C	28	EE	C220 change to 0402 from 0603 for cost down.
06	B -> C	15	EE	change R185,R157,R174,R143 to 0ohm from short pad for USB2.0 debug.
07	B -> C	30,35,31,33 36,34,32,10 13,25,12,26 23,22,29,18 17,27,28	EE,PWR	change 0ohm to short pad for C/D: PR5,PR22,PR34,PR37,PR38,PR39,PR47,PR48,PR52,PR53,PR87,PR128 PR133,PR131,PR144,PR147,PR155,PR159,PR162,PR165,PR223,PR150,PR151,PR154,R62,R134,R223,R425 R453,R469,R487,R488,R503,R367,R482,R535,AR26,L12,PR125,PR138,R14,R15,R123,R1378,,R151,R281,AR18 AR21,AR19,AR30,AR20,PR82,PR108,PR110,R349
08	B -> C	15	EE	add 0.1uF(C471) on +V1.05S_VCCUSBCORE for USB2.0 debug reserve.
09	B -> C	15	EE	change 0ohm to short pad for C/D: R529,R530.
10	B -> C	20,37	EE	change EDP BLON control form PCH to EC for panel on off sequency delay control,ADD R551,unstuff R27.
11	B -> C	22	EE	change 0ohm to short pad : AR14,AR2,AR17,AR16,AR10. Un-stuff AC21,AC10,AC25,AC26,AC39 for C/D
12	B -> C	28	ME	change H25,H29 to h-tc236bc197d146p2 for layout.
13	B -> C	31	EE	change PR115 to 15.4K from 15.8K for adjust 5V range
14	B -> C	31,32,33, 35,36	EE	change PL4,PL6,PL8,PL9,PL10,PL16 to bead and change PR143,PR148,PR149,PR161,PR168 current sensor for power consumption measurement
15	B -> C	17,18	EE	swap name JDIM1 & JDIM2 for SMT

Item	Stage	Page	Owner	Change explanation
				C Stage
16	B -> C	25	EE	change U23 to BD82047FVJ-GE2 for DCP to 2.5A.
17	B -> C	20	EE	change U29 toPS8407 for HDMI 7-10 item
				MP Stage
1	C -> MP	27	EE	un-stuff Q10,Q11,Q12,R78,R79,R85,R347,C112,C129,C144,stuff R75,R98,F3 for drop ZPODD function
2	C -> MP	31,32,33,35 36	PWR	change to short F/P:PL4,PL6,PL8,PL9,PL10,PL16,PR143,PR148,PR149,PR161,PR168 for C/D
3	C -> MP	35	EE	stuff PC51 for 1.05V_VCCST power
4	C -> MP	20	EE	change U29 to PS8201A & R107 to 4.7K for C/D

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Change History