# COMPAL CONFIDENTIAL

**MODEL NAME :** EDA50

**PCB NO :** LA-H271P

**BOM P/N :** 451AG331L01

**GPIO MAP:** X10_CFLH_GPIO map Rev1.5_20181224

# WHITEHAVEN MLK 15

## Coffee Lake H-type (2 chip)

**REV : 1.0(A00)**

**2019.4.10**

**Pop Component**

**EMI@, RF@, ESD@ : EMI/ESD/RF part POP**
**CONN@ : Connector Component**
**XDP@ : Total debug Component (pop them until ST)**
**NDS3@ : non Deep sleep support**
**eSPI@ : eSPI interface**
**RTD3@ : TBT RTD3 support**

**@ : Nopop Component**

**@EMI@, @RF@, @ESD@ : EMI/ESD/RF part nopop**
**DS3@ : Deep sleep support**
**LPC@ : LPC interface**
**NRTD3@ : non TBT RTD3 support**

Layout Dell logo

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REV: X00
PWB: XXXXX
DATE: 1707-03

PCB 26J LA-H271P REV0 MB 3

| Part Number | Description |
|---|---|
| DAB0004C000 | PCB 26J LA-H271P REV0 MB 3 |

Power CKT:
0108

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Title: Cover

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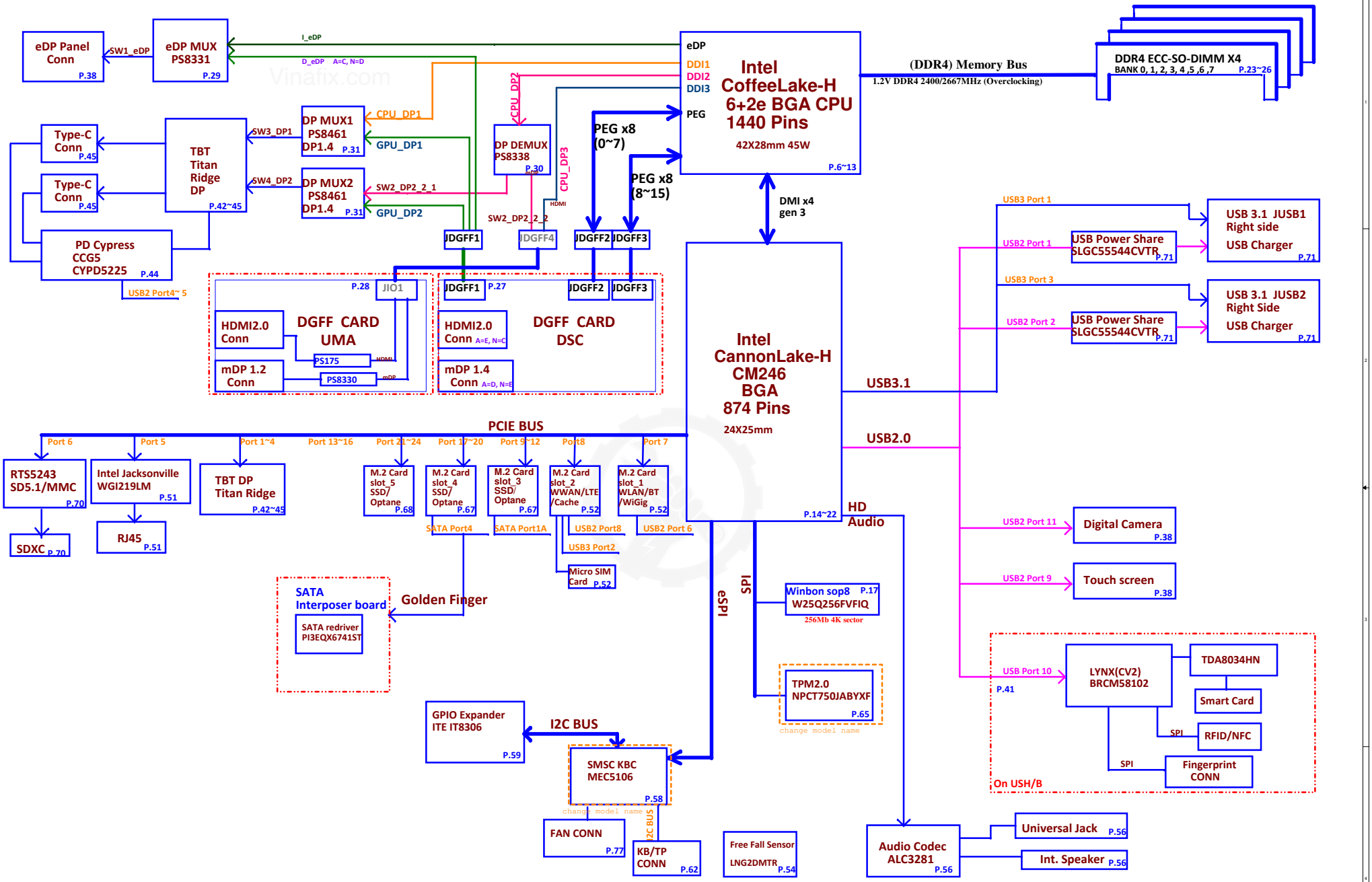
Date: Tuesday, April 09, 2019 | Sheet 1 of 103

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Title: Block Diagram

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Date: Tuesday, April 09, 2019 Sheet 2 of 103

## POWER STATES

| State \ Signal | SLP S3# | SLP S4# | SLP S5# | S4 STATE# | ALWAYS PLANE | RUN PLANE | CLOCKS |
|---|---|---|---|---|---|---|---|
| S0 (Full ON) / M0 | HIGH | HIGH | HIGH | HIGH | ON | ON | ON |
| S3 (Suspend to RAM) / M1 | LOW | HIGH | HIGH | HIGH | ON | OFF | OFF |
| S4 (Suspend to DISK) / M1 | LOW | LOW | HIGH | LOW | ON | OFF | OFF |
| S5 (SOFT OFF) / M1 | LOW | LOW | LOW | LOW | ON | OFF | OFF |
| S3 (Suspend to RAM) / M-OFF | LOW | HIGH | HIGH | HIGH | ON | OFF | OFF |
| S4 (Suspend to DISK) / M-OFF | LOW | LOW | HIGH | LOW | ON | OFF | OFF |
| S5 (SOFT OFF) / M-OFF | LOW | LOW | LOW | LOW | ON | OFF | OFF |

## PM TABLE

| power plane \ State | +PWR_SRC<br>+5V_ALW<br>+3.3V_ALW<br>+3.3V_ALW2<br>+3.3V_ALW_DSW<br>+3.3V_ALW_PCH<br>+3.3V_RTC_LDO<br>+1.8V_ALW<br>+1.0V_PRIM<br>+1.8V_PRIM | +3.3V_SUS<br>+1.2V_MEM<br>+2.5V_MEM<br>+1.0V_VCCST | +5V_RUN<br>+3.3V_RUN<br>+1.2V_RUN<br>+3.3V_DGFF<br>+5V_DGFF<br>+DGFF_PWR_SRC<br>+0.675V_DDR_VTT | (M-OFF)<br>+VCC_CORE<br>+VCC_GT<br>+VCC_IO<br>+VCC_SA<br>+1.0V_VCCSTG<br>+1.8V_RUN |
|---|---|---|---|---|
| S0 | ON | ON | ON | ON |
| S3 | ON | ON | OFF | OFF |
| S5 S4/AC | ON | OFF | OFF | OFF |
| S5 S4/AC don't exist | OFF | OFF | OFF | OFF |

| Layer No. | Name | Er for polar | DF | Material | Thickness (Material SPEC.) Unit : mil | Thickness (Actuality) Unit : mil |
|---|---|---|---|---|---|---|
| | S/M | 3.7 | 0.047 | SolderMask | HF GA-HF-15 | 0.80 |
| 1 | Top | | | Copper foil | Hoz+plating | 1.55 |
| | | 3.7 | 0.018 | Prepreg | pp1086LR | 2.55 |
| 2 | GND/PWR | | | Copper foil | 1oz | 1.30 |
| | | 3.8 | 0.0153 | Core | 4mil core | 4.00 |
| 3 | IN1 | | | Copper foil | Hoz | 0.65 |
| | | 3.8 | 0.017 | Prepreg | pp2116HR | 4.70 |
| 4 | GND/PWR | | | Copper foil | Hoz | 0.65 |
| | | 3.7 | 0.0186 | Core | 3mil core | 3.00 |
| 5 | IN2 | | | Copper foil | Hoz | 0.65 |
| | | 3.8 | 0.017 | Prepreg | pp2116HR | 4.30 |
| 6 | GND/PWR | | | Copper foil | 2oz | 2.60 |
| | | 3.7 | 0.0186 | Core | 3mil core | 3.00 |
| 7 | GND/PWR | | | Copper foil | 2oz | 2.60 |
| | | 3.8 | 0.017 | Prepreg | pp2116HR | 4.30 |
| 8 | IN3 | | | Copper foil | Hoz | 0.65 |
| | | 3.7 | 0.0186 | Core | 3mil core | 3.00 |
| 9 | GND/PWR | | | Copper foil | Hoz | 0.65 |
| | | 3.8 | 0.017 | Prepreg | pp2116HR | 4.70 |
| 10 | IN4 | | | Copper foil | Hoz | 0.65 |
| | | 3.8 | 0.0153 | Core | 4mil core | 4.00 |
| 11 | GND/PWR | | | Copper foil | 1oz | 1.30 |
| | | 3.7 | 0.018 | Prepreg | pp1086LR | 2.55 |
| 12 | Bottom | | | Copper foil | Hoz+plating | 1.55 |
| | S/M | 3.7 | 0.047 | SolderMask | | 0.80 |
| verall Thickness (1.45mm ± 10%) | | | | | | 56.50000 |
| | | | | | | 1.4351 |

| USB3.0 | DESTINATION |
|---|---|
| Port 1 | JUSB1 |
| Port 2 | M.2 Slot-2 (WWAN/LTE) |
| Port 3 | JUSB2 |
| Port 4 | NA |
| Port 5 | NA |
| Port 6 | NA |

| SATA | DESTINATION |
|---|---|
| SATA 0B | NA |
| SATA 1A | SLOT3 SSD |
| SATA 2 | NA |
| SATA 3 | NA |
| SATA 4 | SATA HDD |
| SATA 5 | NA |

| | USB2 PORT# | DESTINATION |
|---|---|---|
| PCH | 1 | JUSB1 |
| | 2 | JUSB2 |
| | 3 | NA |
| | 4 | Cypress PD |
| | 5 | Cypress PD |
| | 6 | NA |
| | 7 | NA |
| | 8 | M.2 Slot-2 (WWAN/LTE) |
| | 9 | 17" NA/ 15" Touch screen |
| | 10 | USH |
| | 11 | Camera |
| | 12 | NA |
| | 13 | NA |
| | 14 | M.2 Slot-1 (BT) |

| | | |
|---|---|---|
| USH | 0 | BIO |
| | 1 | NA |

| PCI EXPRESS | DESTINATION |
|---|---|
| PORT 1~4 | TBT-Titan Ridge |
| PORT 5 | 10/100/1G LOM |
| PORT 6 | MMI(Card reader) |
| PORT 7 | M.2 Slot-1 (WLAN/Wigig) |
| PORT 8 | M.2 Slot-2 (WWAN/LTE) |
| PORT9~12 | SLOT3 SSD 2280/ Optane |
| PORT13~16 | NA |
| PORT17~20 | SLOT4 SSD 2280/ Optane |
| PORT21~24 | SLOT5 PCIE ONLY 2280/ Optane |

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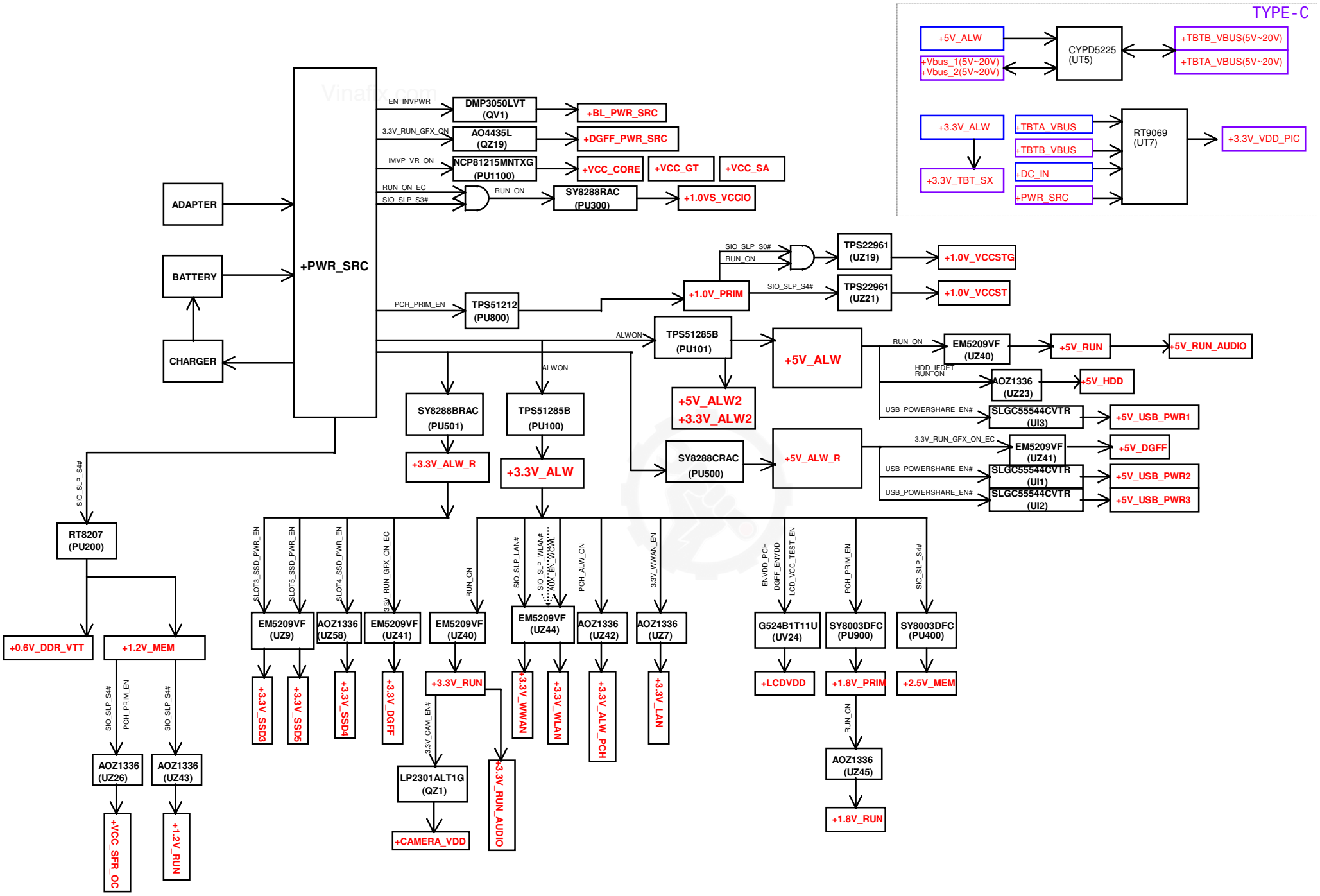


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Title: Power MAP

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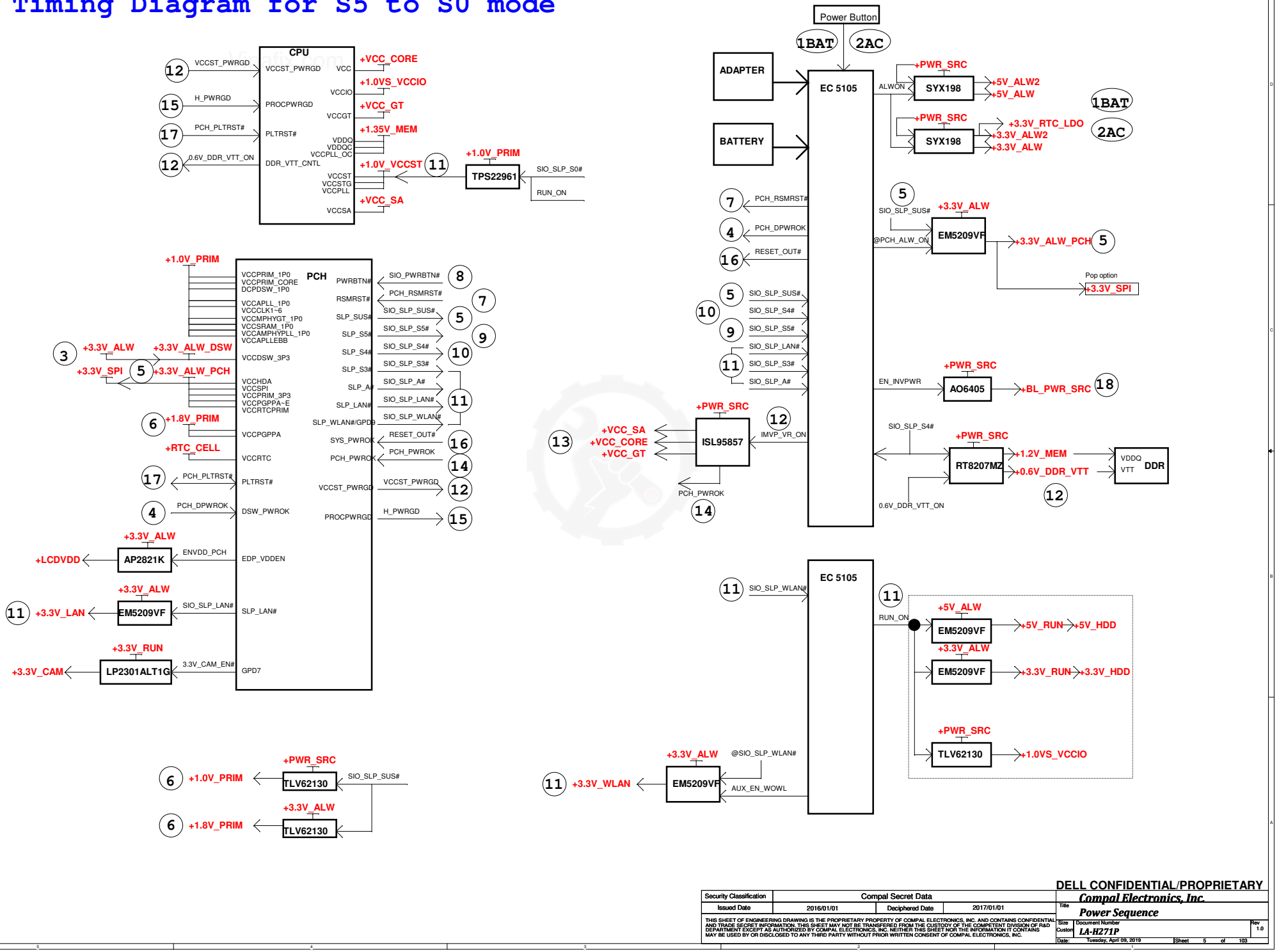
# Timing Diagram for S5 to S0 mode

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Title: Power Sequence

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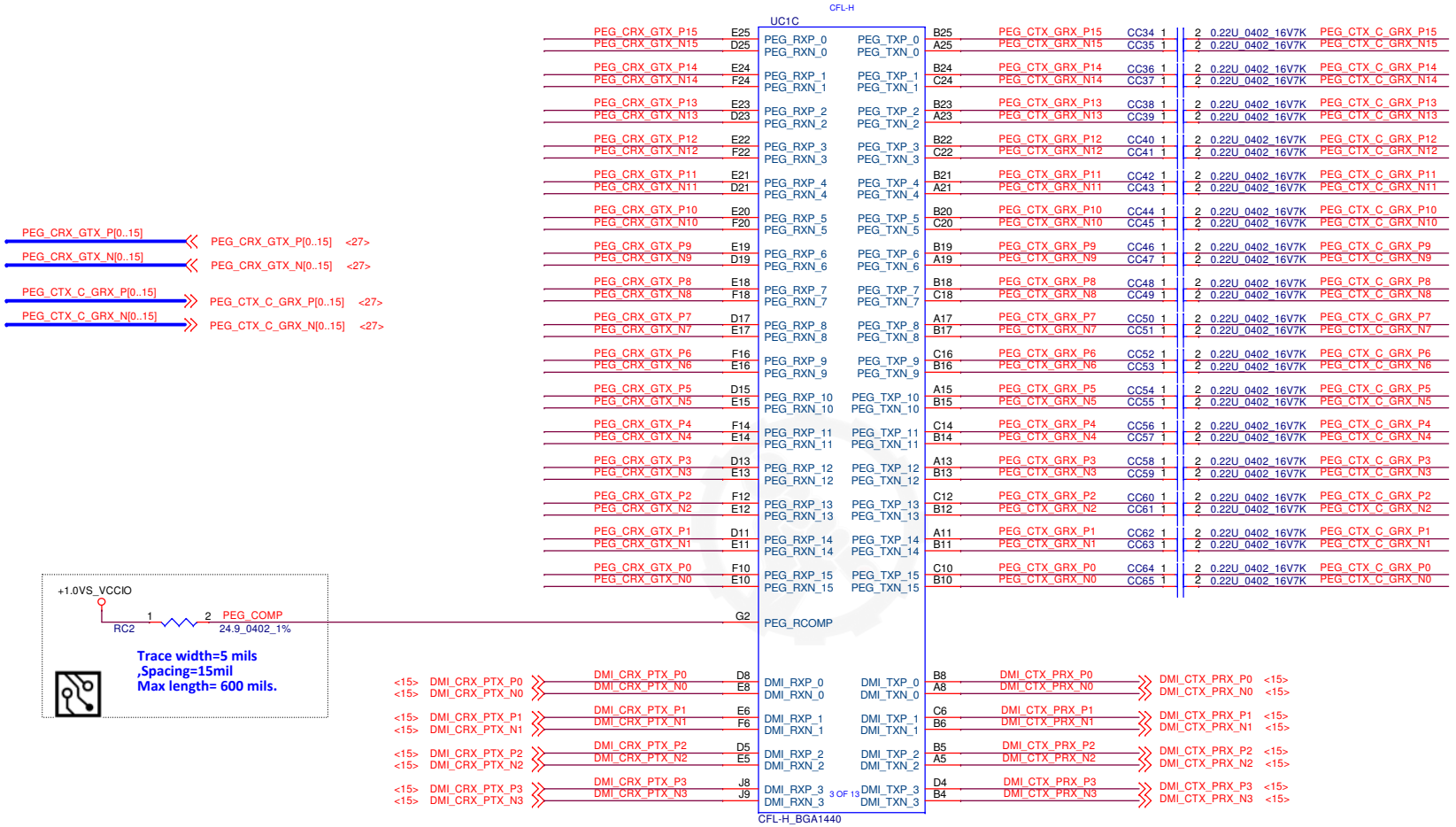


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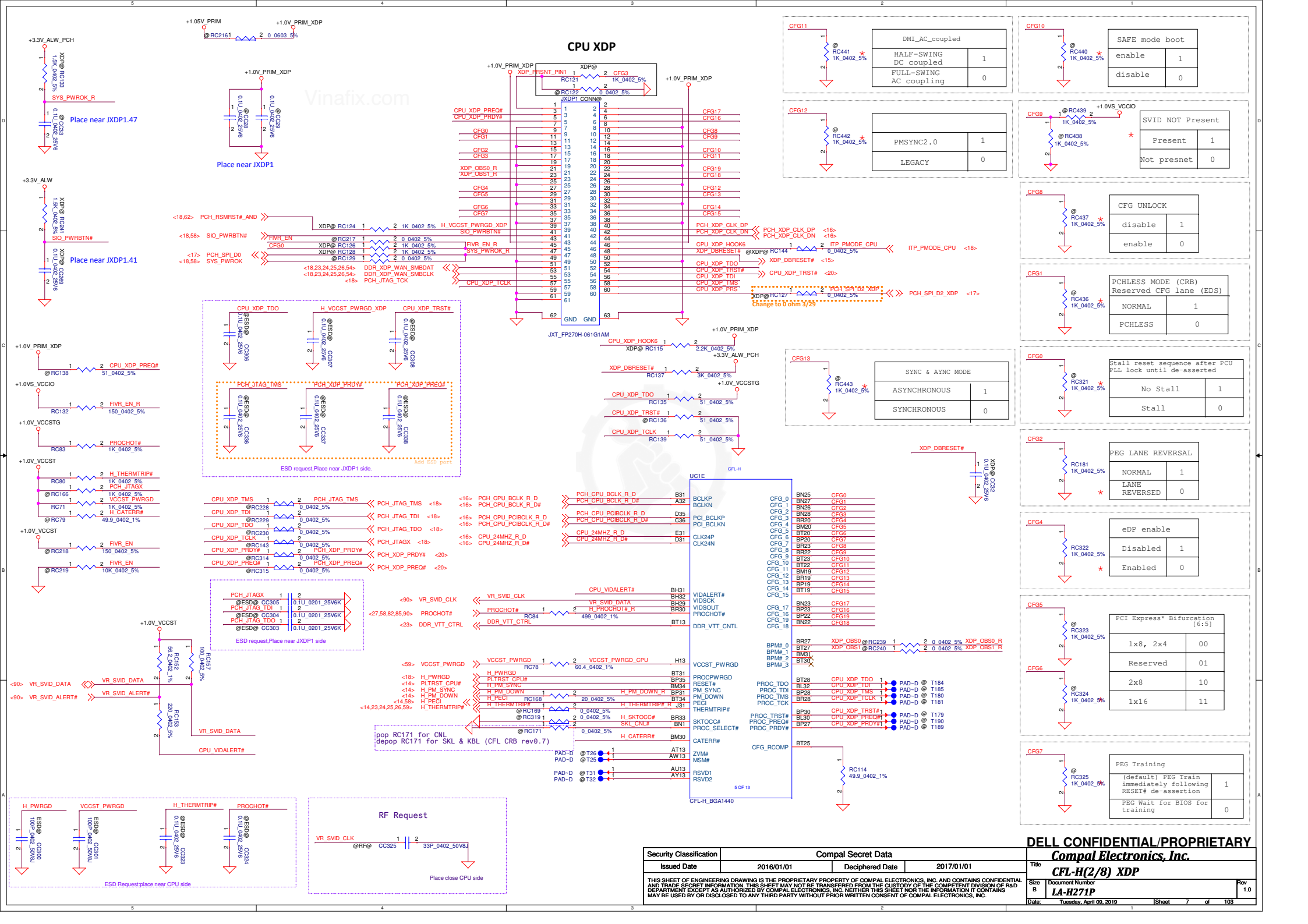
# CPU XDP

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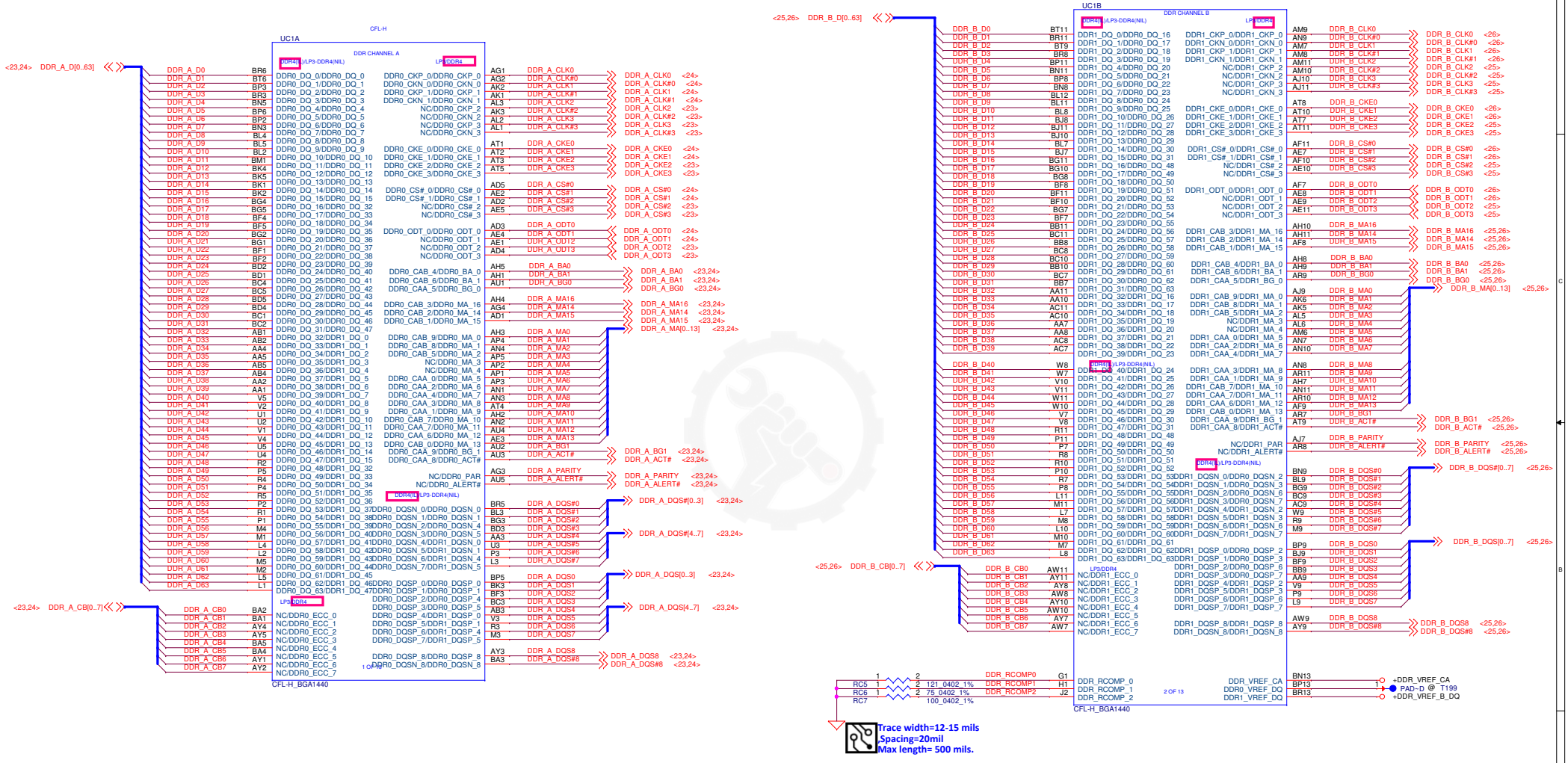


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Title: *CFL-H(3/8) DDR4*

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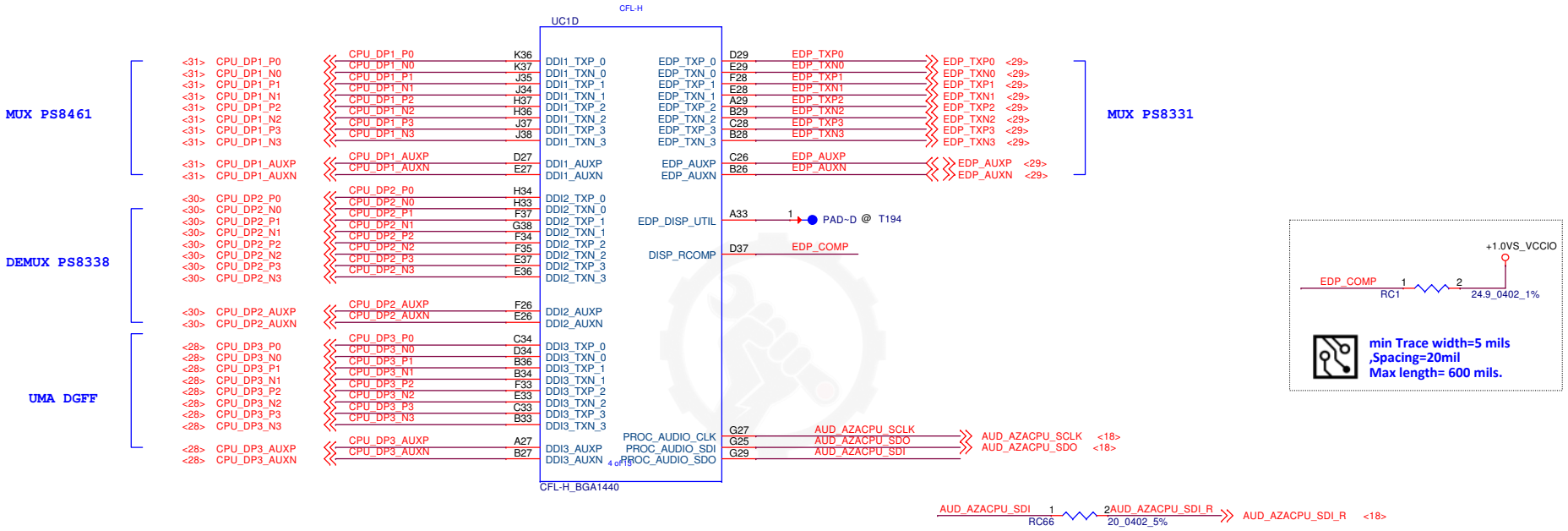


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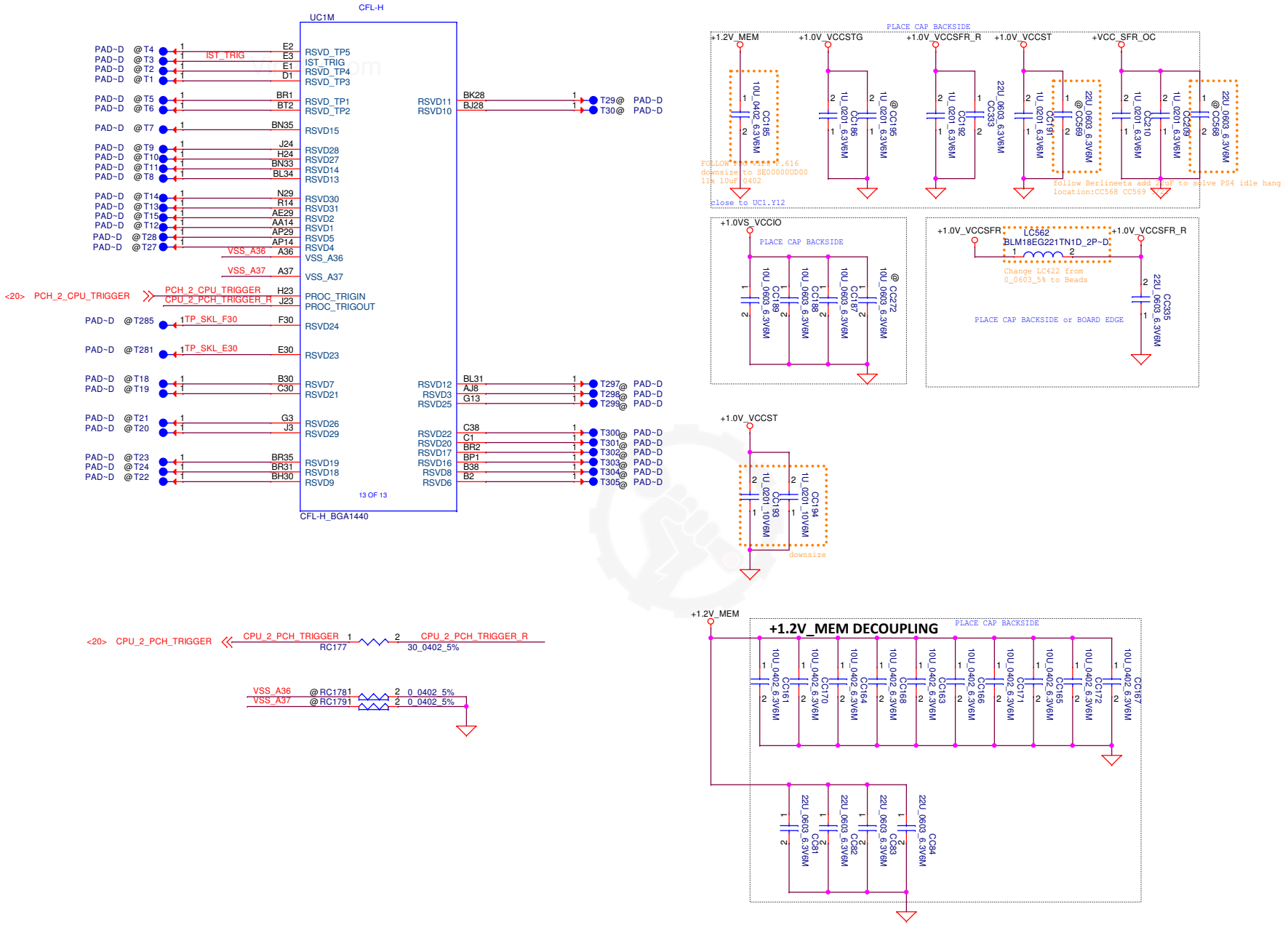


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Title: CFL-H(5/8) RSVD,Decoupling

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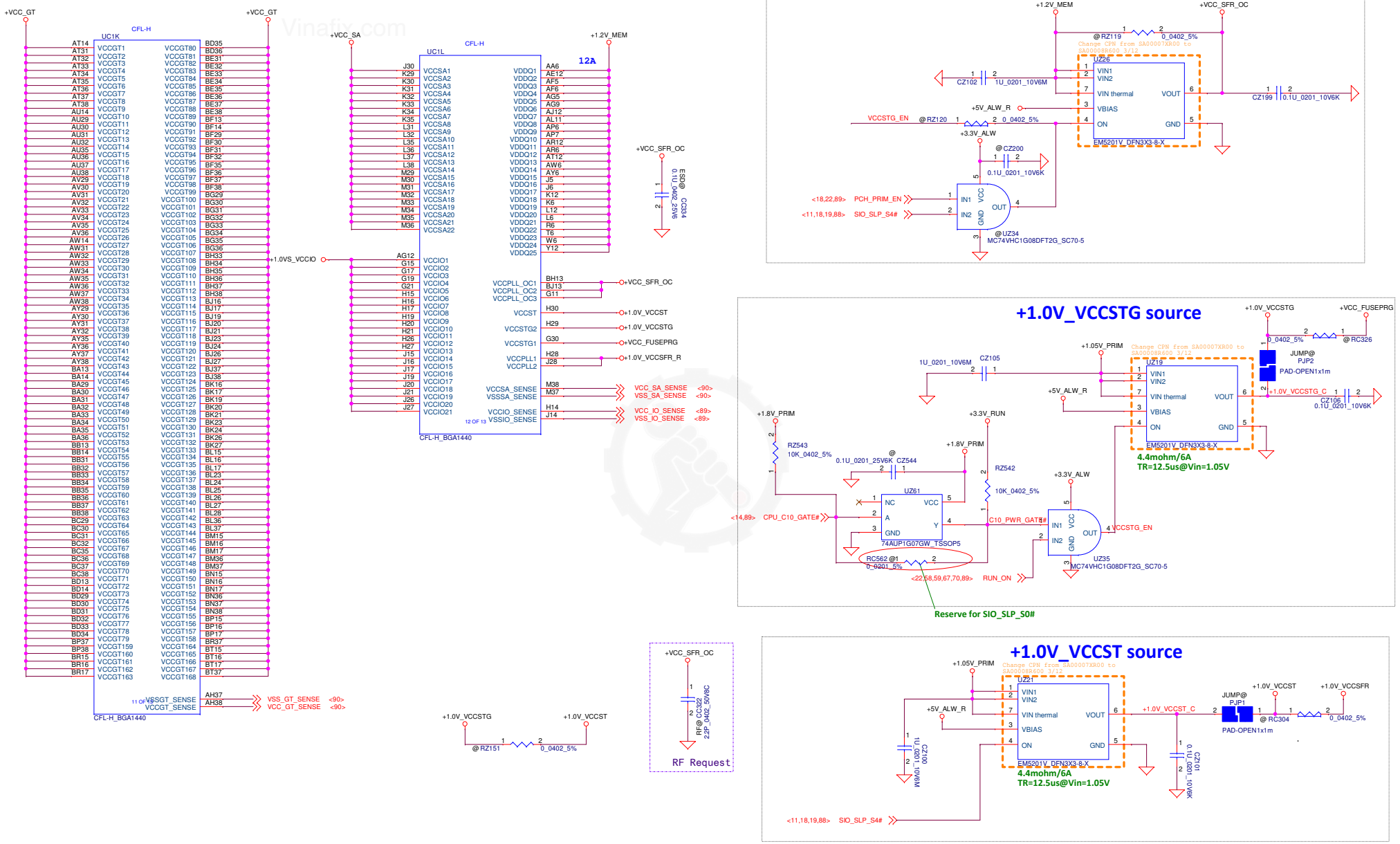


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Title: **CFL-H(6/8) PWR**

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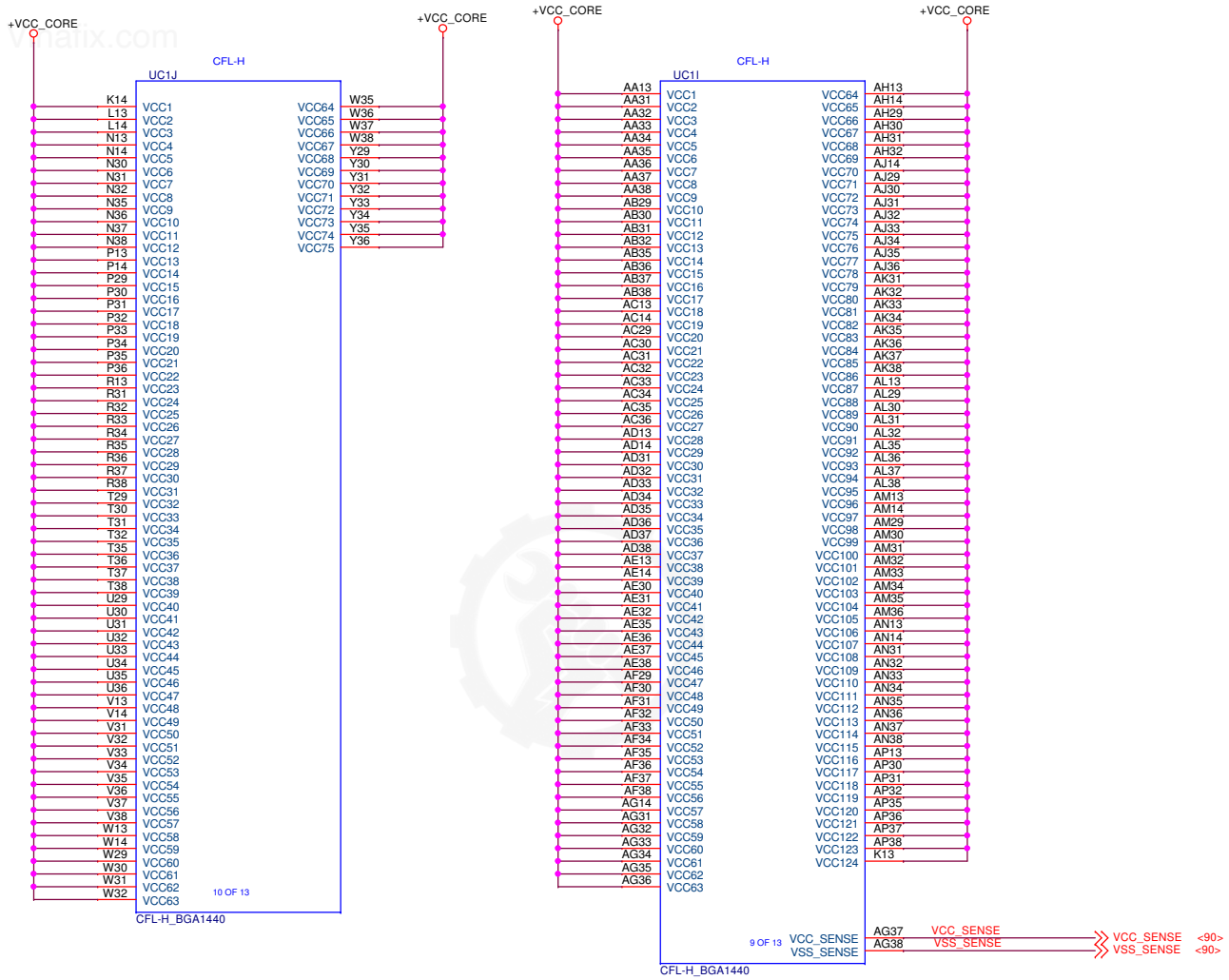
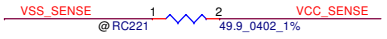



CFL change form +VCCGT to +VCC_CORE

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Title: CFL-H(7/8) +VCC_CORE

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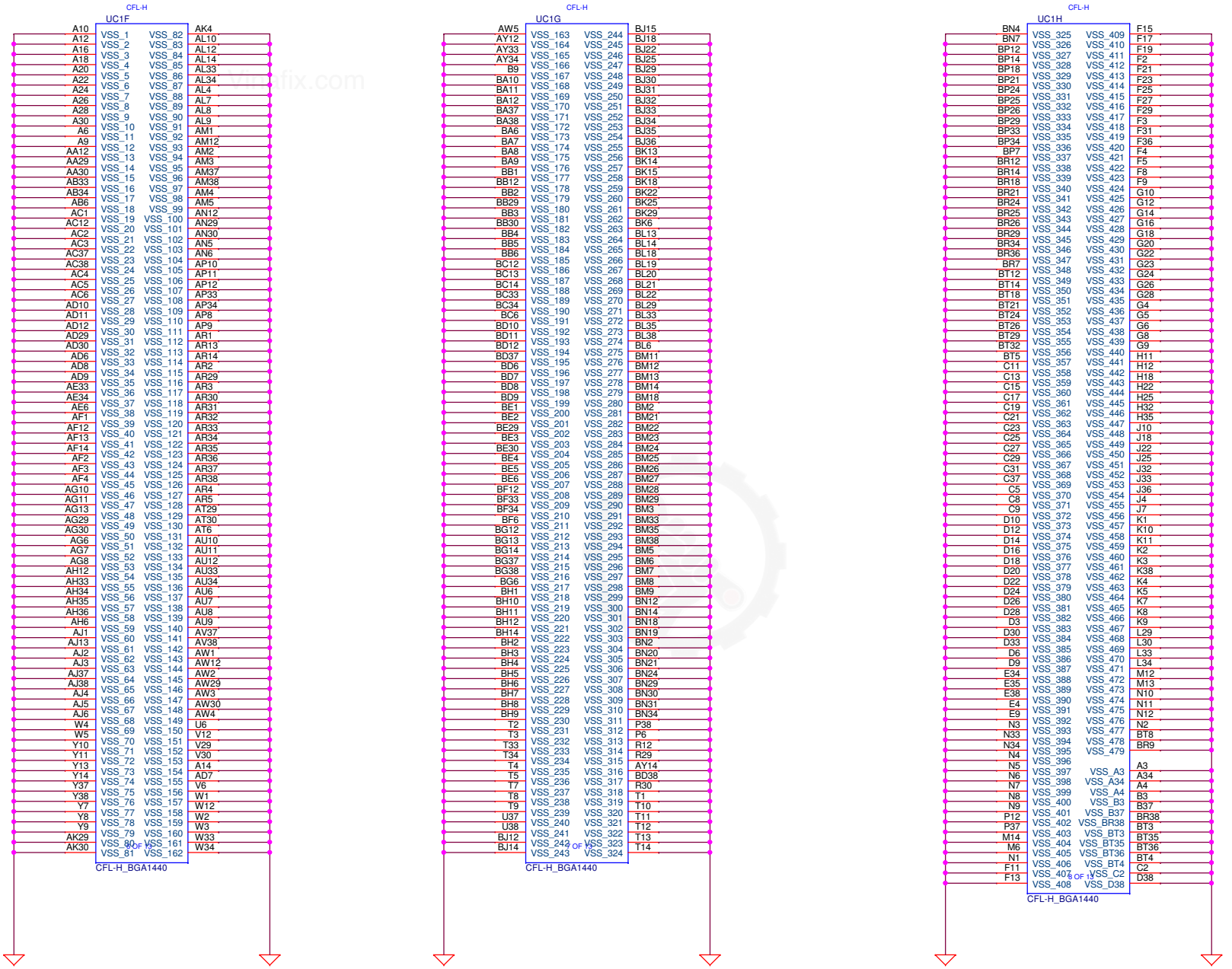


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Title: CFL-H(8/8) GND

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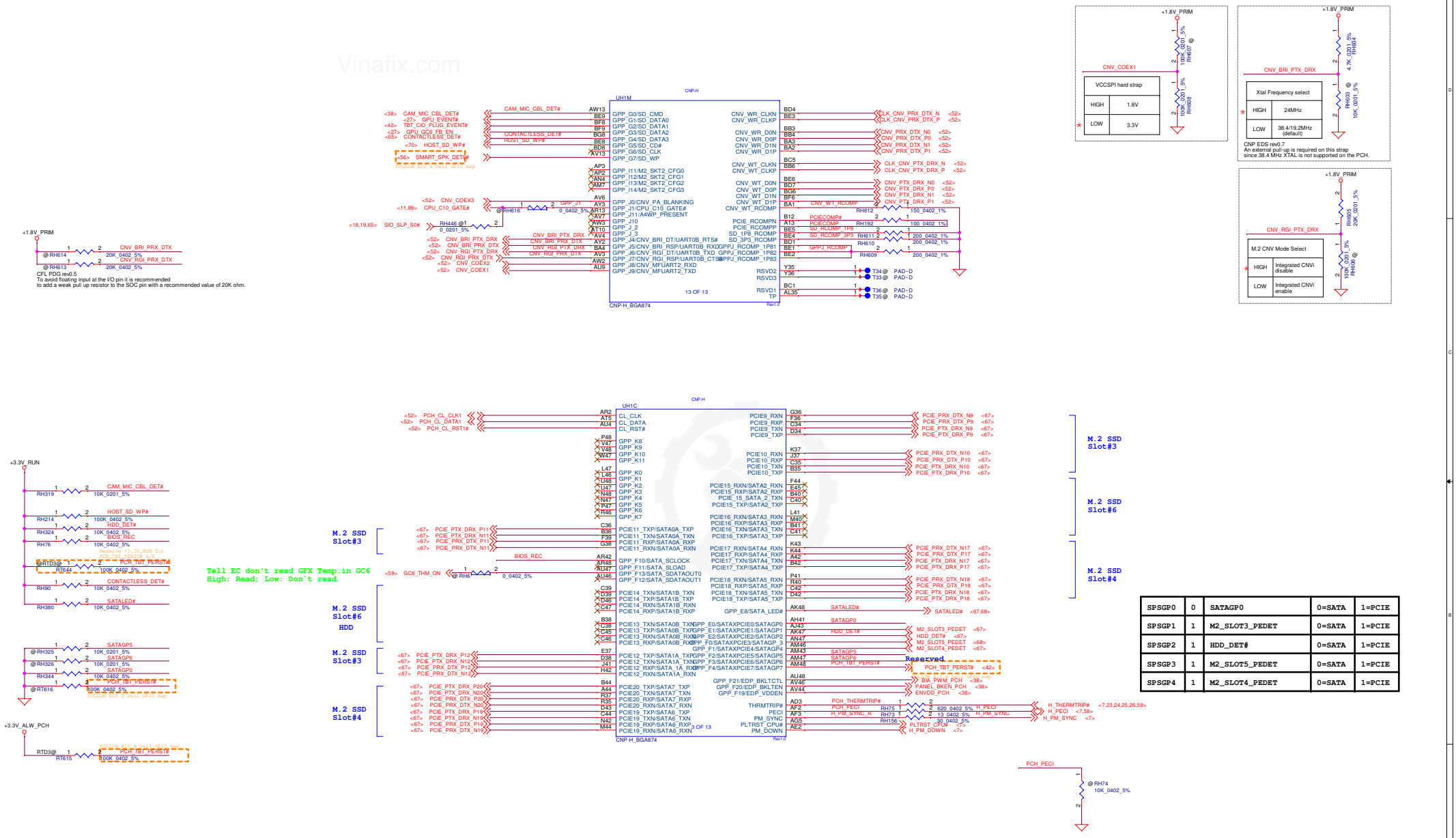


| | | | | |
|---|---|---|---|---|
| SPSGP0 | 0 | SATAGP0 | 0=SATA | 1=PCIE |
| SPSGP1 | 1 | M2_SLOT3_PEDET | 0=SATA | 1=PCIE |
| SPSGP2 | 1 | HDD_DET# | 0=SATA | 1=PCIE |
| SPSGP3 | 1 | M2_SLOT5_PEDET | 0=SATA | 1=PCIE |
| SPSGP4 | 1 | M2_SLOT4_PEDET | 0=SATA | 1=PCIE |

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Title: CNP-H(1/9) PCIE,CNV
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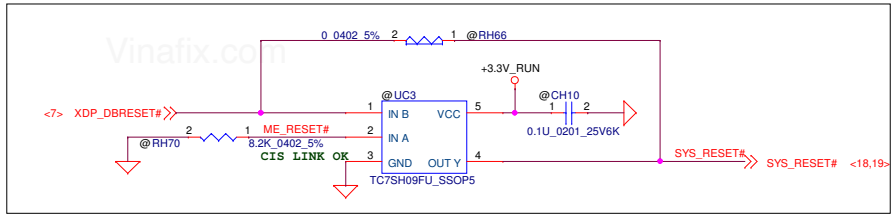
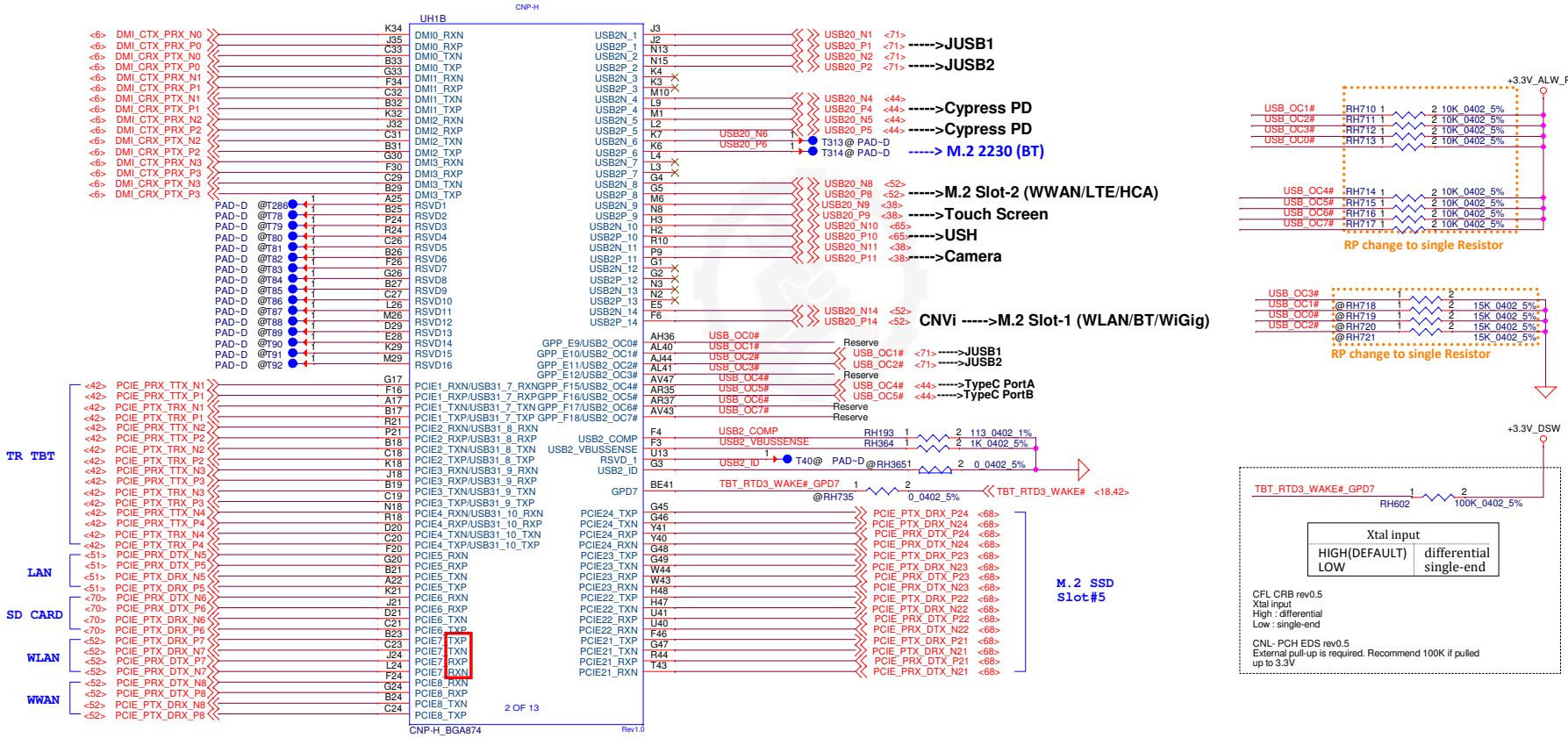
Date: Tuesday, April 09, 2019 | Sheet 14 of 103

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| Issued Date | 2016/01/01 | Deciphered Date | 2017/01/01 |

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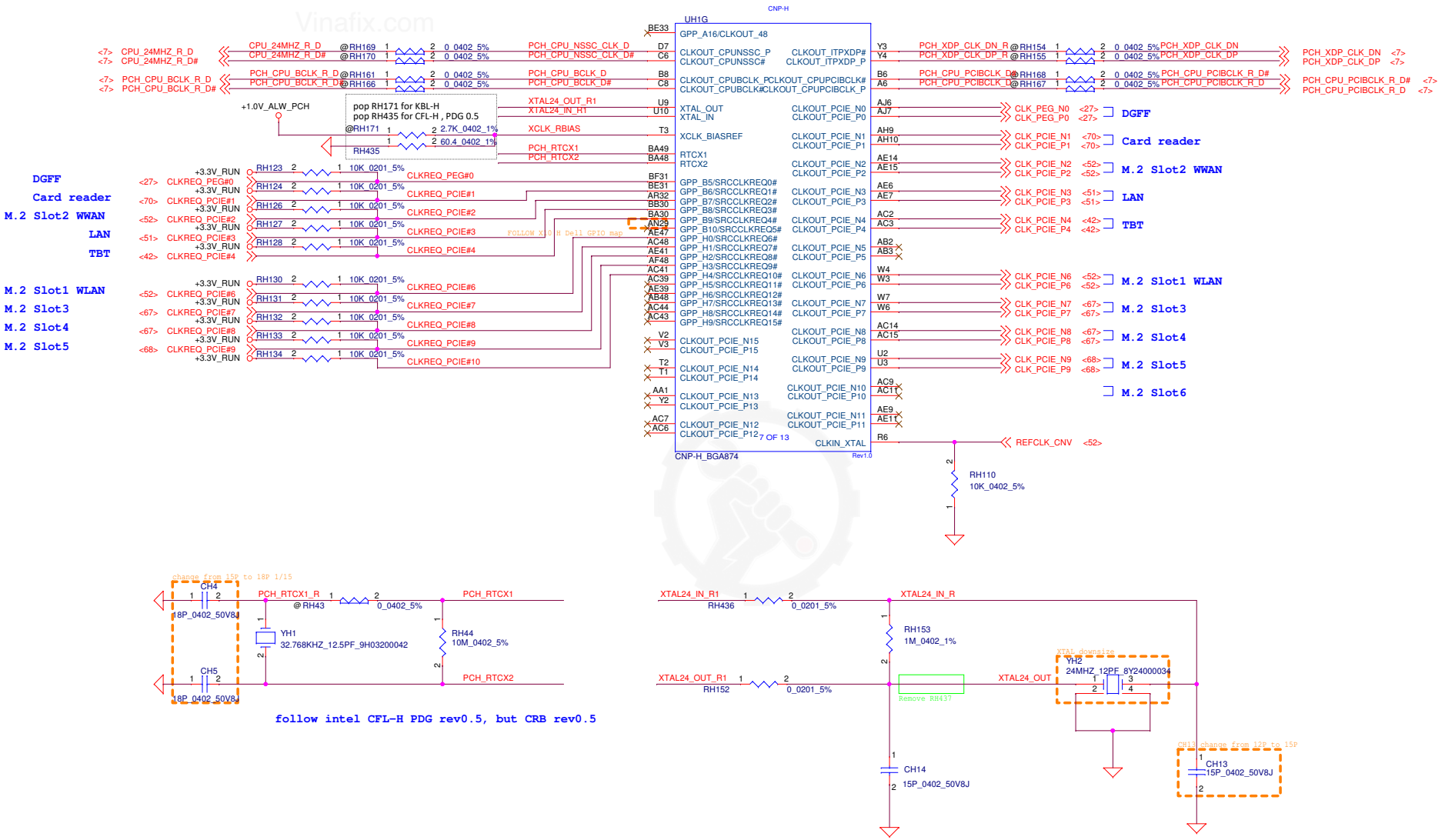
| Compal Electronics, Inc. | | | |
| Title | CNP-H(2/9) PCIE,DMI,USB | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 15 of 103 | | |


UH1G
CNP-H
CNP-H_BGA874
Rev1.0
7 OF 13
DGFF
Card reader
M.2 Slot2 WWAN
LAN
TBT
M.2 Slot1 WLAN
M.2 Slot3
M.2 Slot4
M.2 Slot5
M.2 Slot6
pop RH171 for KBL-H
pop RH435 for CFL-H , PDG 0.5
follow intel CFL-H PDG rev0.5, but CRB rev0.5
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Compal Electronics, Inc.
CNP-H(3/9) CLK
LA-H271P
Rev 1.0
Tuesday, April 09, 2019
Sheet 16 of 103
Compal Secret Data
2016/01/01
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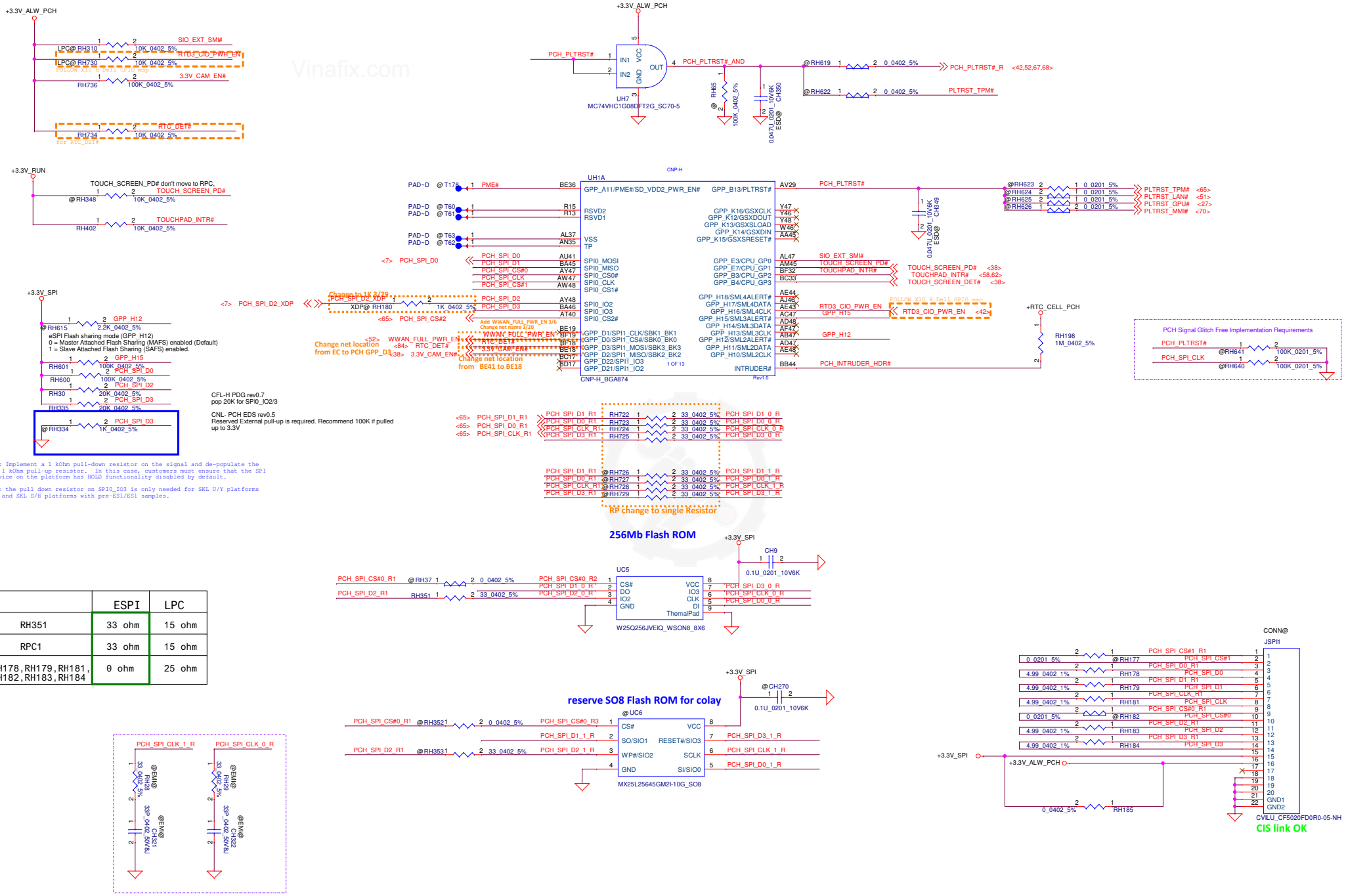


| | ESPI | LPC |
|---|---|---|
| RH351 | 33 ohm | 15 ohm |
| RPC1 | 33 ohm | 15 ohm |
| RH178,RH179,RH181, RH182,RH183,RH184 | 0 ohm | 25 ohm |


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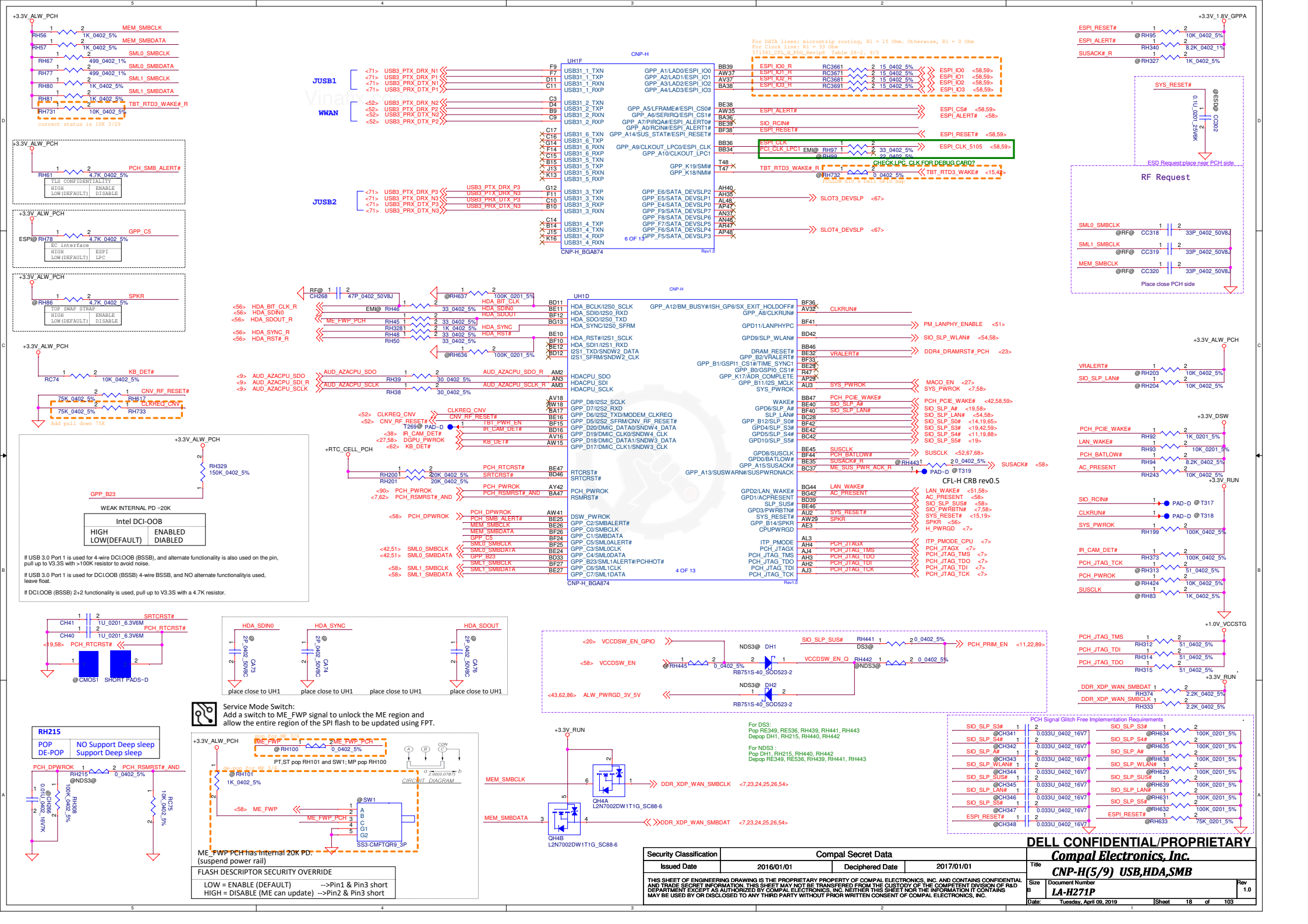
| | | | |
|---|---|---|---|
| Title | CNP-H(4/9) SPI,PLTRST | | |
| Size | Document Number | | Rev |
| B | LA-H271P | | 1.0 |
| Date: | Tuesday, April 09, 2019 | Sheet | 17 of 103 |


JUSB1
JUSB2
WWAN
UH1F
CNP-H
CNP-H_BGA874
UH1D
CNP-H_BGA874
RF Request
ESD Request place near PCH side
Place close PCH side
CFL-H CRB rev0.5
Intel DCI-OOB
HIGH ENABLED
LOW(DEFAULT) DISABLED
WEAK INTERNAL PD ~20K
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and
allow the entire region of the SPI flash to be updated using FPT.
RH215
POP NO Support Deep sleep
DE-POP Support Deep sleep
ME_FWP PCH has internal 20K PD.
(suspend power rail)
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin2 & Pin3 short
For DS3:
Pop RE349, RE536, RH439, RH441, RH443
Depop DH1, RH215, RH440, RH442
For NDS3 :
Pop DH1, RH215, RH440, RH442
Depop RE349, RE536, RH439, RH441, RH443
PCH Signal Glitch Free Implementation Requirements
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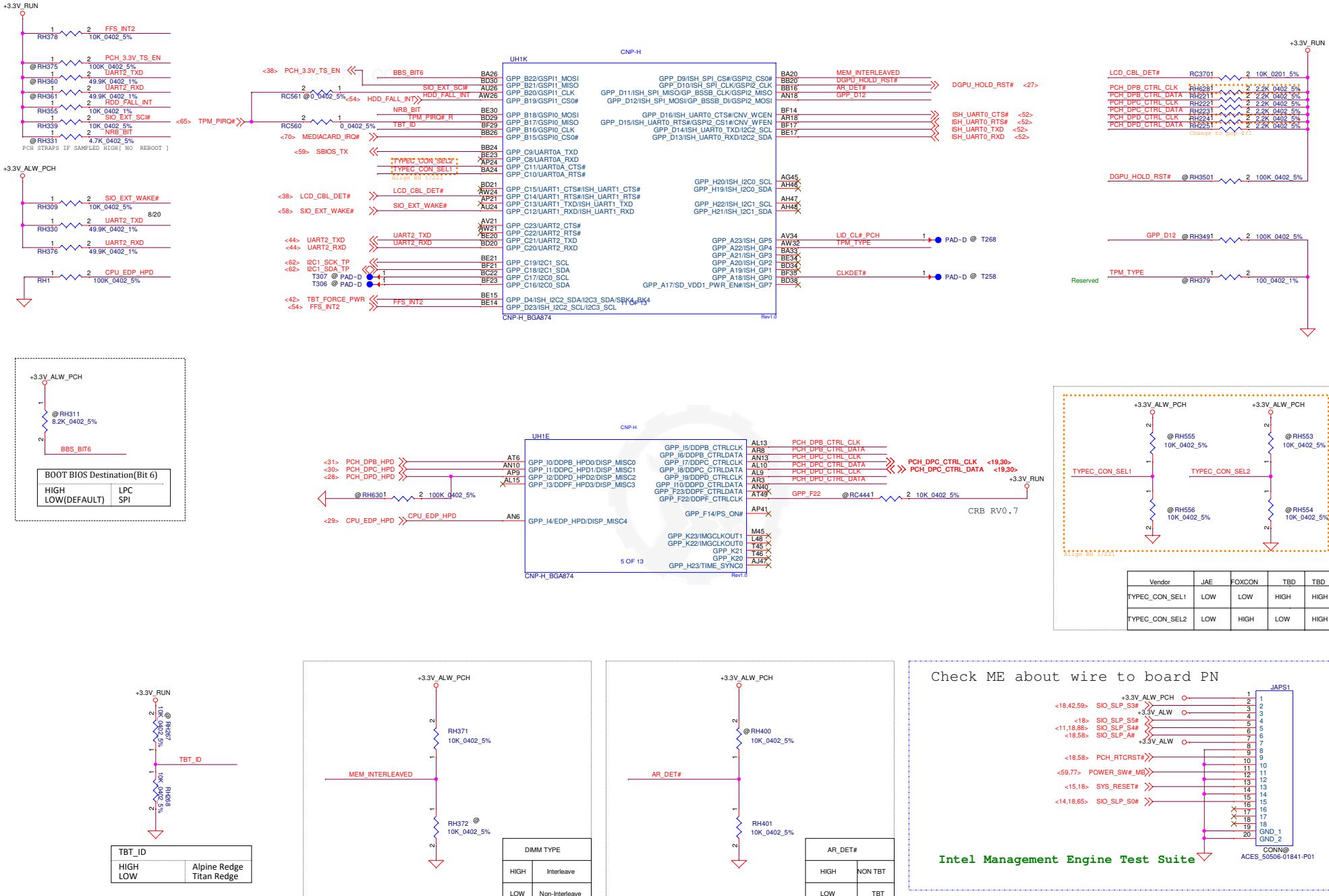
CNP-H(5/9) USB,HDA,SMB
LA-H271P
Rev 1.0
Tuesday, April 09, 2019
Sheet 18 of 103

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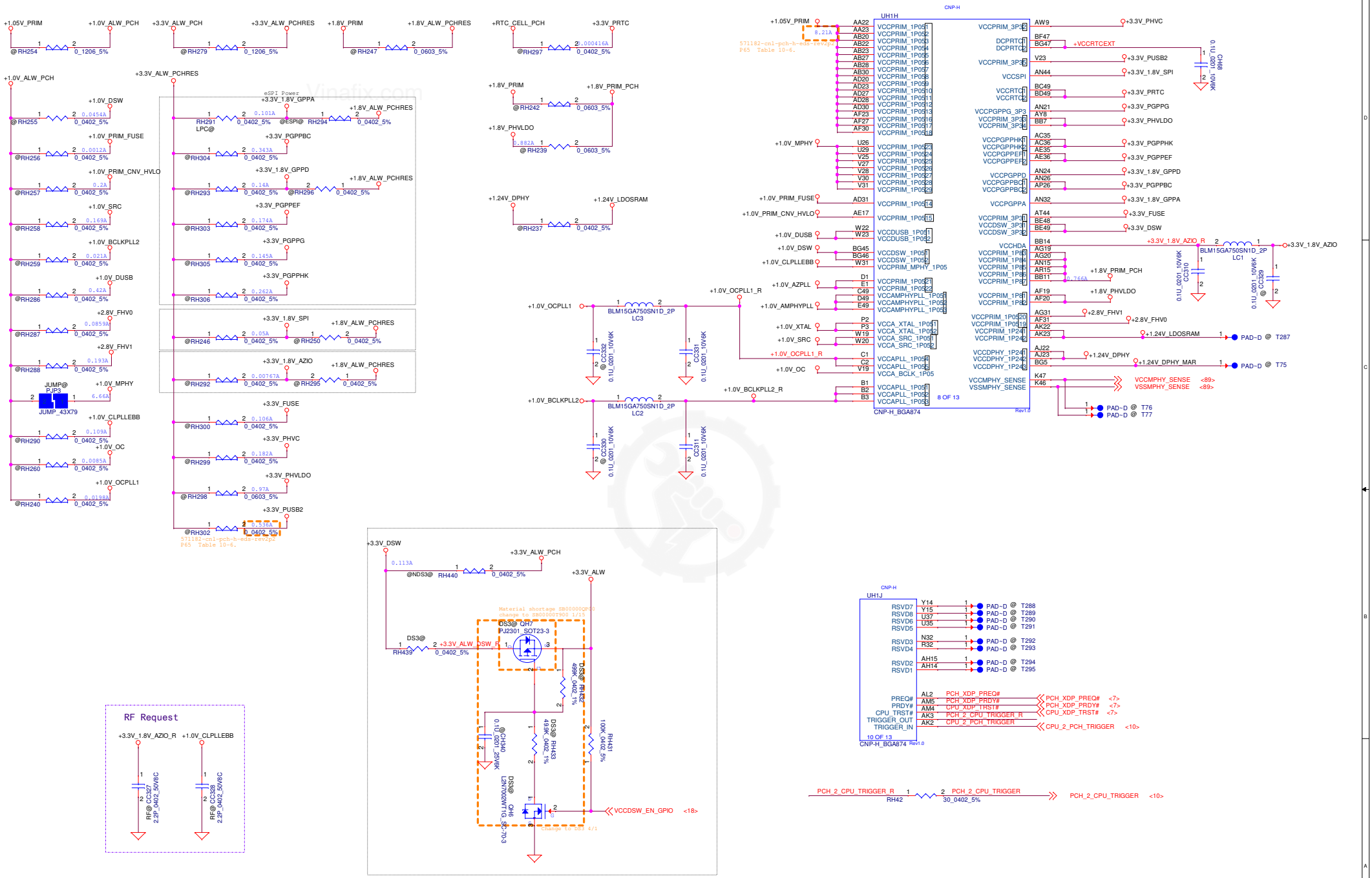
Compal Electronics, Inc.

Title: CNP-H(5/9) USB,HDA,SMB

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 19 of 103





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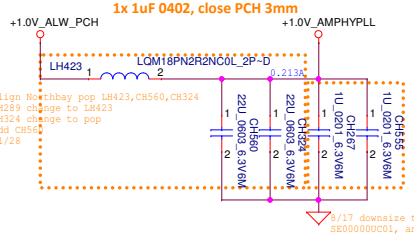
Compal Electronics, Inc.

Title: CNP-H(7/9) PWR,RSVD

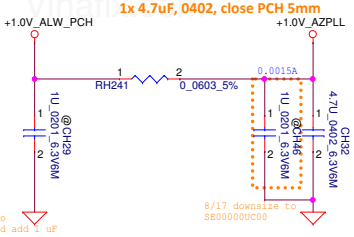
Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 20 of 103

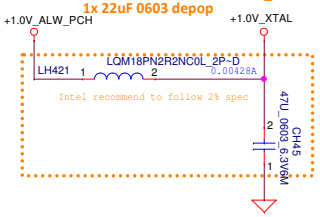
PDG V1P8 Table 50-8 +1.0V_AMPHYPLL
1x 1uF 0402, close PCH 3mm



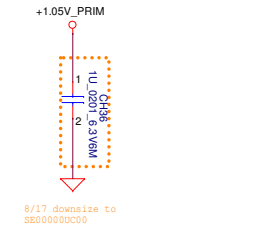

PDG V1P8 Table 50-8. +1.0V_AZPLL
1x 4.7uF, 0402, close PCH 5mm



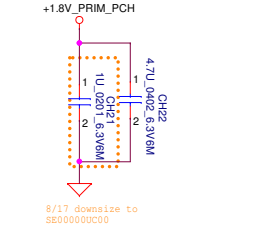

PDG V1P8 Table 50-9. +1.0V_XTAL
1x 22uF 0603 depop



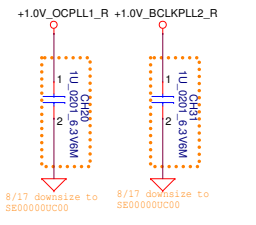

PDG V1P8 Table 50-8 +1.05V_PRIM
1x 1uF, 0402, close PCH 3mm



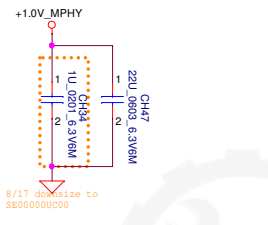

PDG V1P8 Table 50-8 +VCCPRIM_1P8
1x 4.7uF 0603, close PCH 3mm
1x 1uF 0402, close PCH 3mm



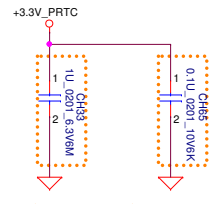

PDG V1P8 Table 50-8 VCCAPLL_1P05
1x 1uF, 0402, close PCH 5mm



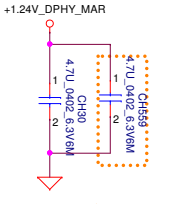

PDG V1P8 Table 50-8 +VCCPRIM_1P05
1x 1uF 0402, 3mm, close PCH 5mm
1x 22uF 0805, 5mm, close PCH 5mm



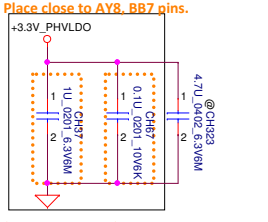

PDG V1P8 Table 50-8 +VCCRTC
1x 0.1uF 0402, close PCH 3mm
1x 1uF 0402, close PCH 5mm



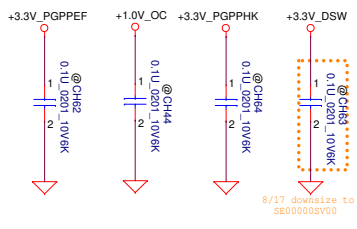

PDG V1P8 Table 50-8 +VCCDPHY_1P24
1x 4.7uF 0402, close PCH 5mm



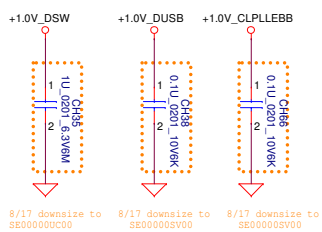

PDG V1P8 Table 50-8 +VCCPRIM_3P3
1x 1uF, 0603, close PCH 3mm
Place close to AY8, BB7 pins.

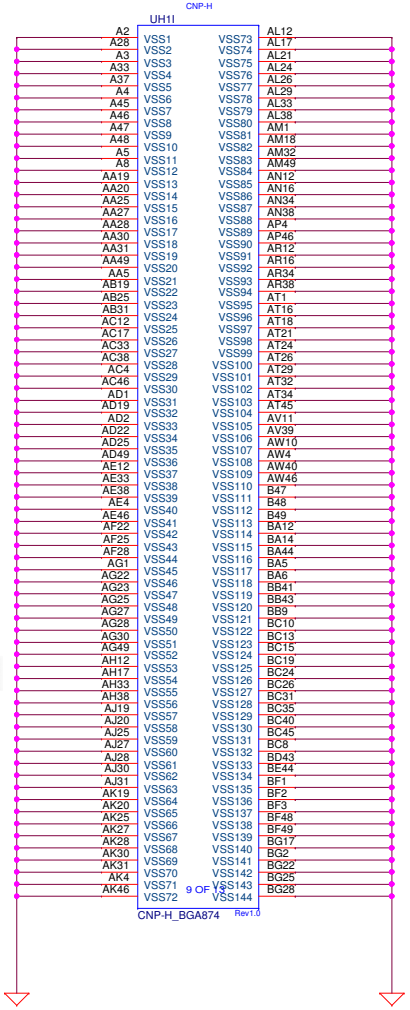


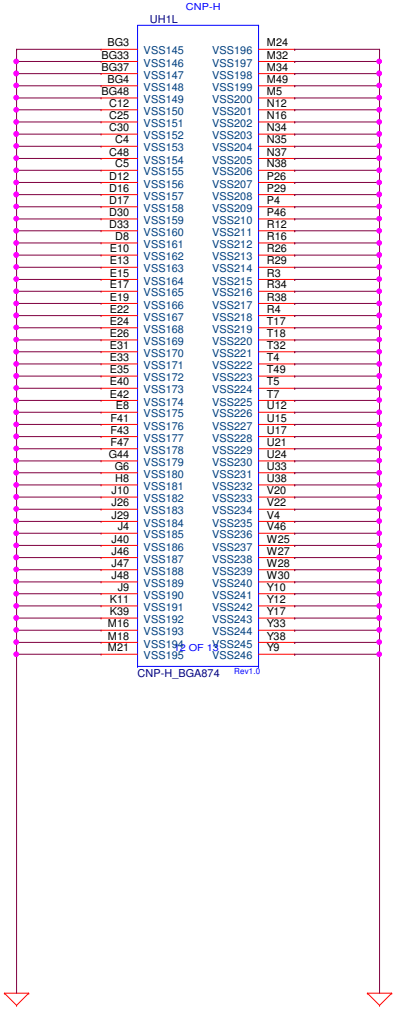

CFL-H PDG rev0.5 4.7uF x1
CRB-H rev0.7 0.1uF x1, 1uF x1




PDG V1P8 Table 50-8 depop, but reserved

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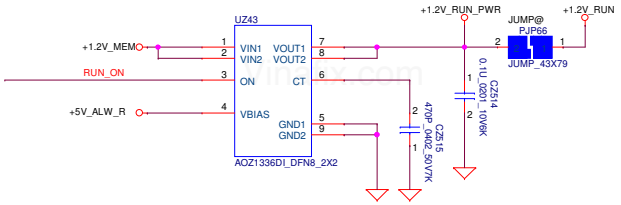
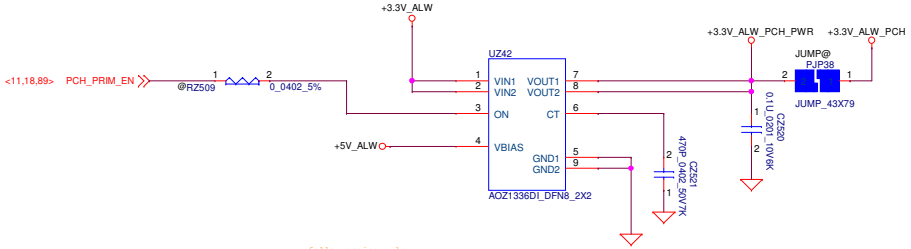
|---|---|---|
| Title | CNP-H(8/9) PWR,CAP | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 21 of 103 | |

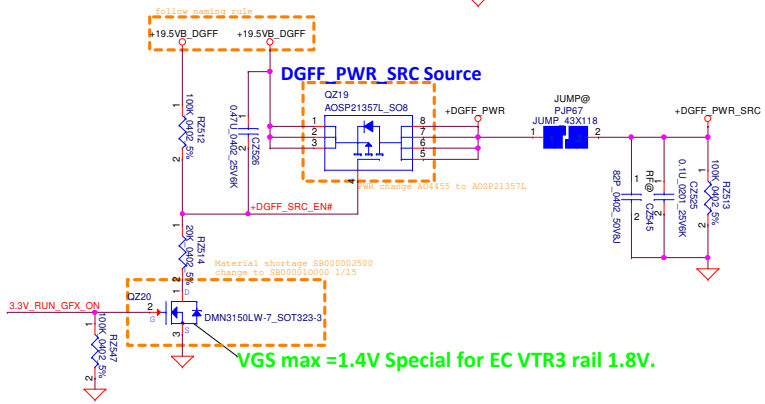
## +1.2V_RUN Source



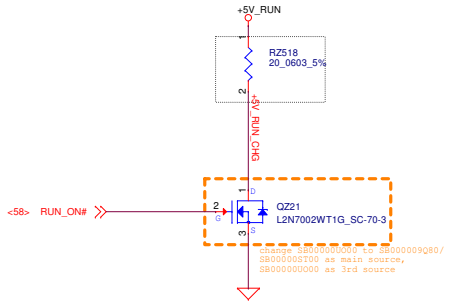

## +3.3V_ALW_PCH Source



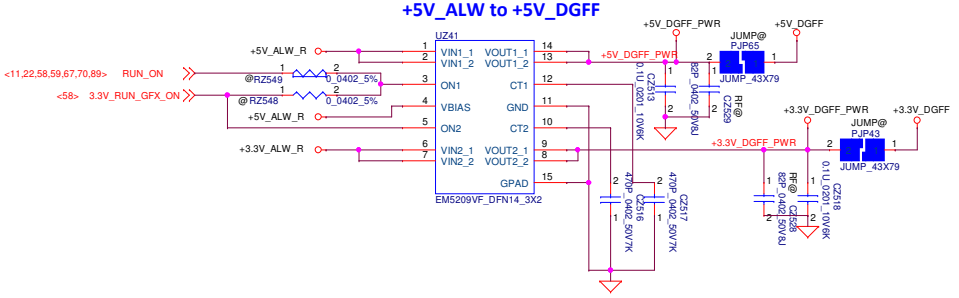

## DGFF_PWR_SRC Source



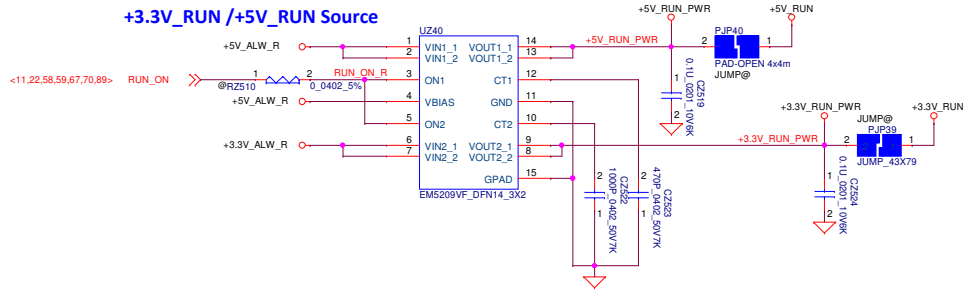

## Discharg Circuit



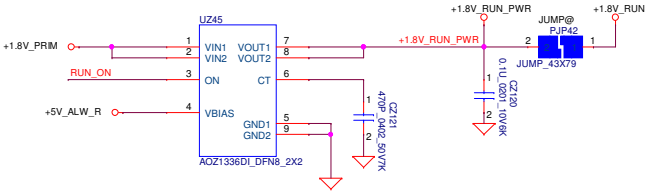

## +3.3V_ALW to +3.3V_DGFF
## +5V_ALW to +5V_DGFF




## +3.3V_RUN /+5V_RUN Source




## +1.8V_RUN Source

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*Compal Electronics, Inc.*

Title: ***CNP-H(9/9) Power Control***

| Size | Document Number | Rev |
|---|---|---|
| Custom | *LA-H271P* | 1.0 |

Date: Tuesday, April 09, 2019 | Sheet 22 of 103

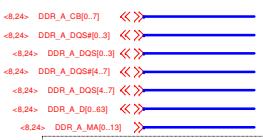
# JDIMM1 REV Type H=5.2

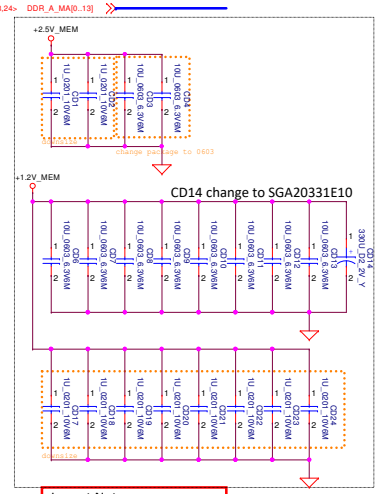
All VREF traces should have 10 mil trace width

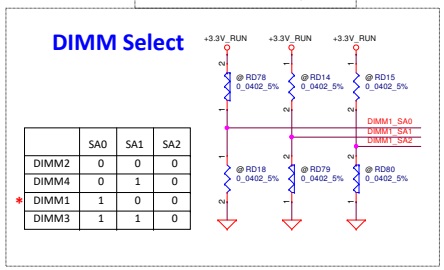
CH-B REV JDIMM4 -->CKE0,1 (D) JDIMM3 -->CKE2,3 STD

CH-A STD JDIMM2 -->CKE0,1 (B) Top Side (A) Bottom Side JDIMM1 -->CKE2,3 REV

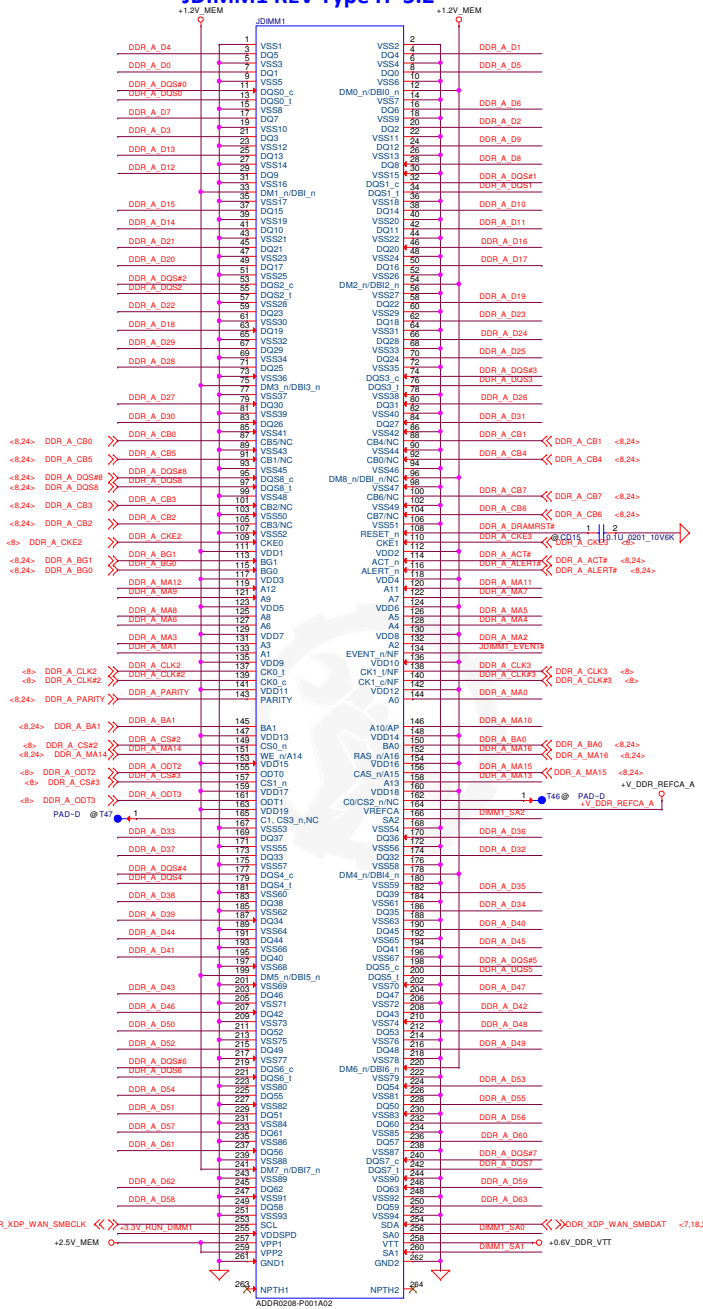
CPU B A



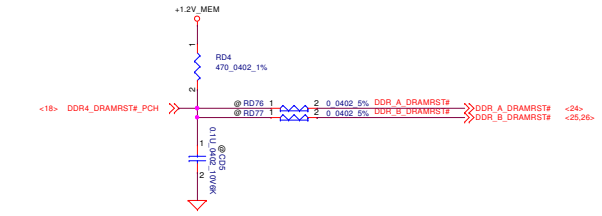


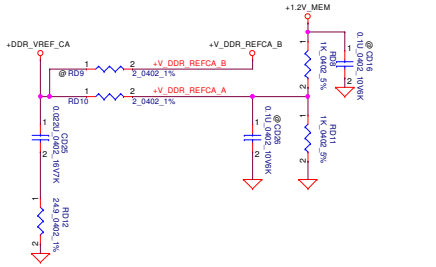



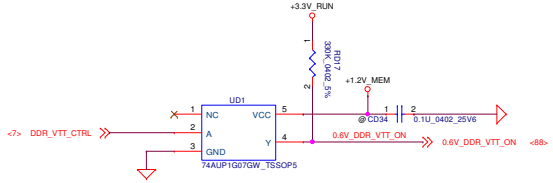

| | SA0 | SA1 | SA2 |
|---|---|---|---|
| DIMM2 | 0 | 0 | 0 |
| DIMM4 | 0 | 1 | 0 |
| * DIMM1 | 1 | 0 | 0 |
| DIMM3 | 1 | 1 | 0 |




SP07001JH0L

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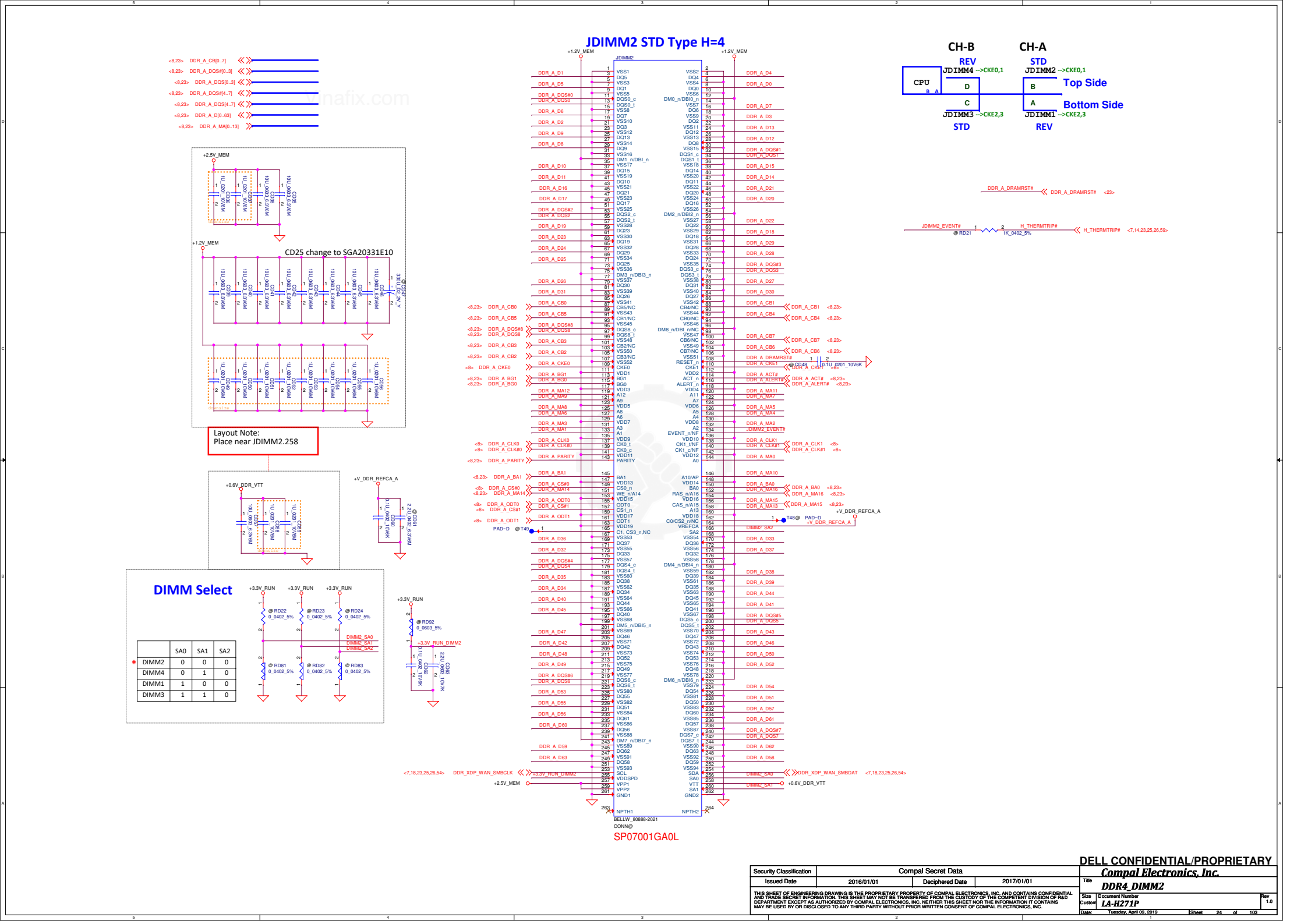
Compal Electronics, Inc.

Title: DDR4_DIMM1

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 23 of 103

# JDIMM2 STD Type H=4




| | SA0 | SA1 | SA2 |
|---|---|---|---|
| * DIMM2 | 0 | 0 | 0 |
| DIMM4 | 0 | 1 | 0 |
| DIMM1 | 1 | 0 | 0 |
| DIMM3 | 1 | 1 | 0 |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| Issued Date | 2016/01/01 | Deciphered Date | 2017/01/01 |

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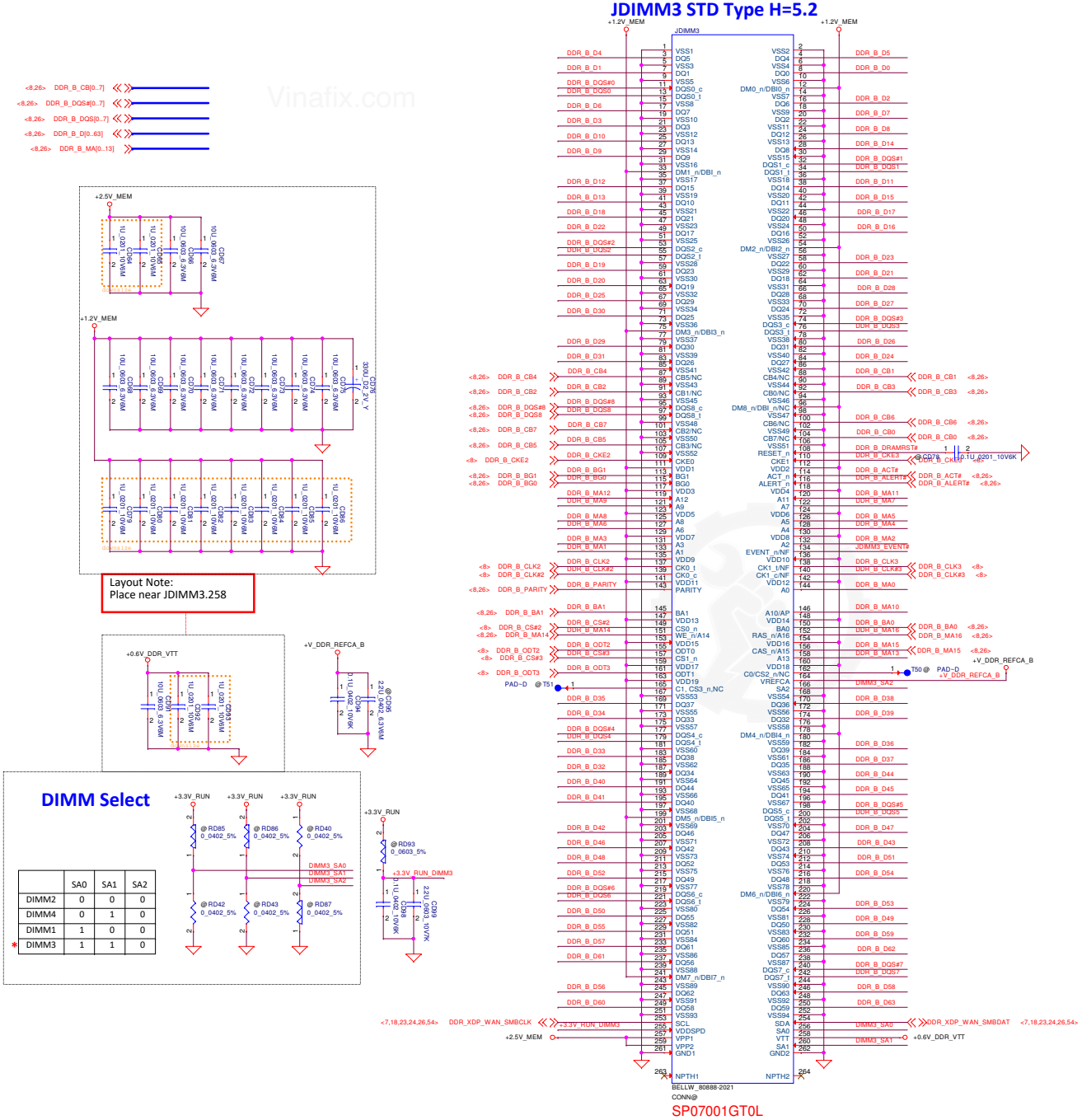
Compal Electronics, Inc.

Title: DDR4_DIMM2

Size: Custom | Document Number: LA-H771P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 24 of 103

# JDIMM3 STD Type H=5.2



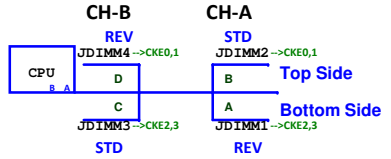


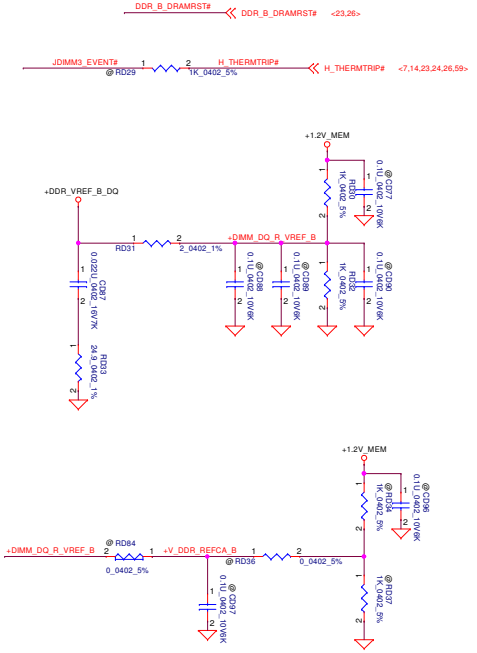


Layout Note:
Place near JDIMM3.258

## DIMM Select

| | SA0 | SA1 | SA2 |
|---|---|---|---|
| DIMM2 | 0 | 0 | 0 |
| DIMM4 | 0 | 1 | 0 |
| DIMM1 | 1 | 0 | 0 |
| * DIMM3 | 1 | 1 | 0 |

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| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/01/01 | Deciphered Date | 2017/01/01 |

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Title: DDR4_DIMM3

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 25 of 103

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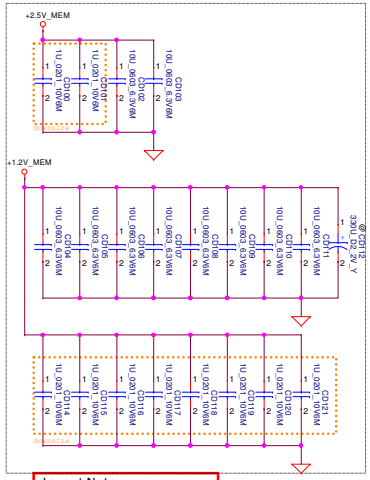
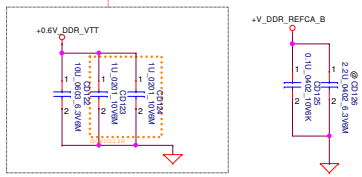
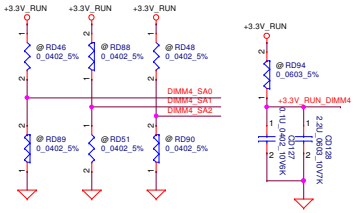
# JDIMM4 REV Type H=4

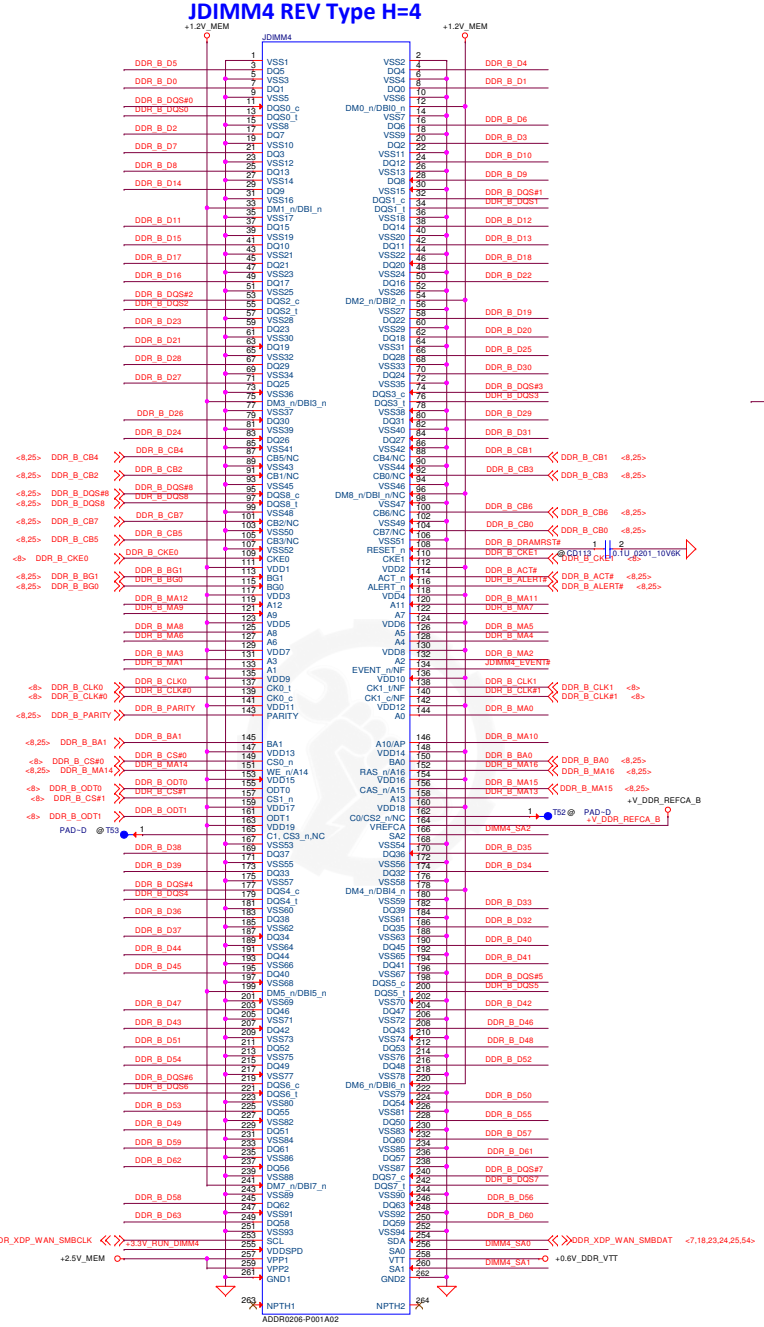



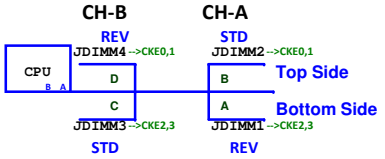



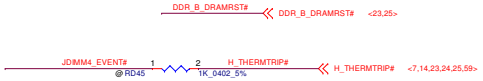

## DIMM Select

| | SA0 | SA1 | SA2 |
|---|---|---|---|
| DIMM2 | 0 | 0 | 0 |
| * DIMM4 | 0 | 1 | 0 |
| DIMM1 | 1 | 0 | 0 |
| DIMM3 | 1 | 1 | 0 |

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Compal Electronics, Inc.

Title: DDR4_DIMM4

| Size | Document Number | Rev |
|---|---|---|
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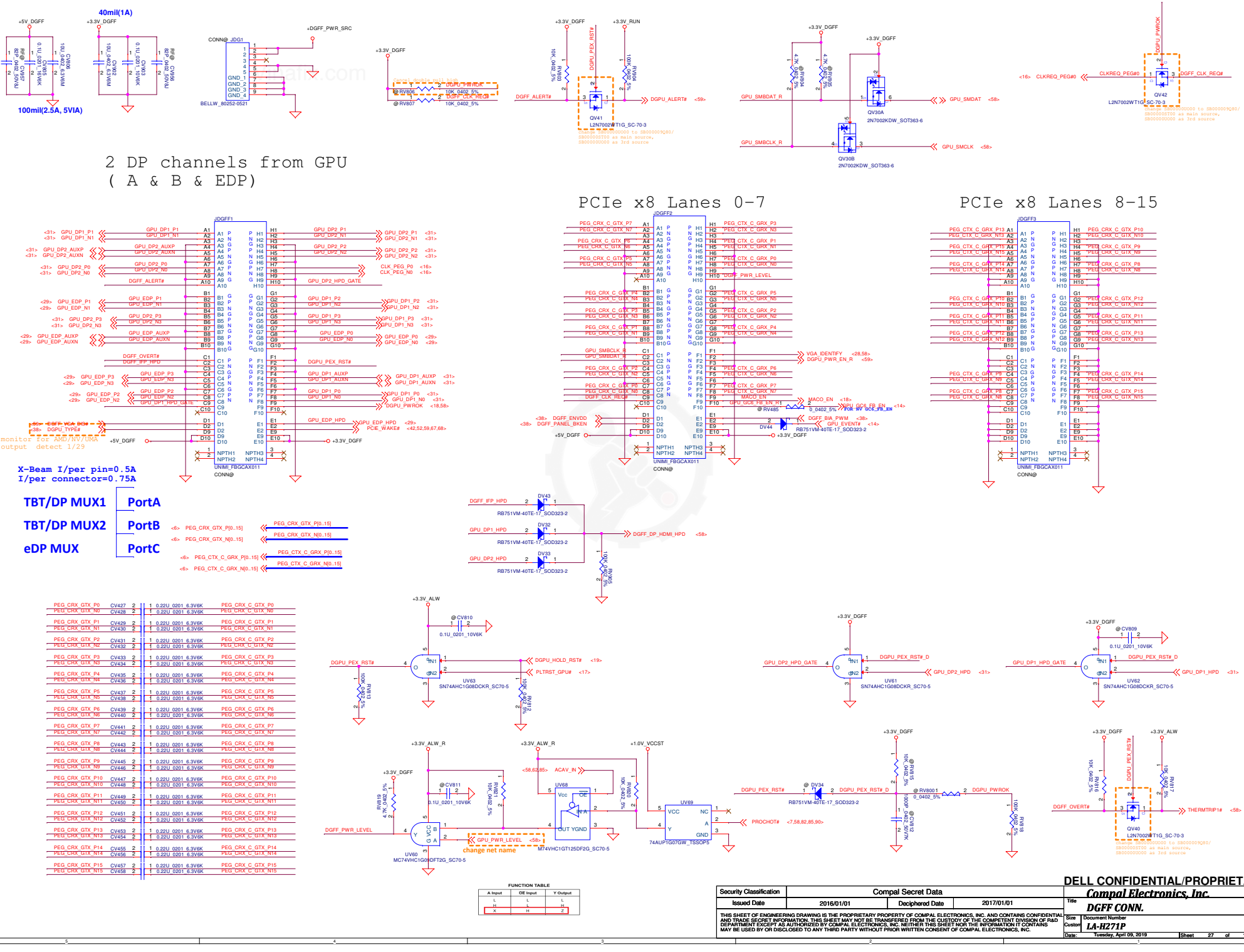
40mil(1A)
100mil(2.5A, 5VIA)
2 DP channels from GPU
( A & B & EDP)
PCIe x8 Lanes 0-7
PCIe x8 Lanes 8-15
JDGFF1
JDGFF2
JDGFF3
UNIMI_FBGCAX011
CONN@
HDR monitor for AMD/NV/UMA
edp output detect 1/29
X-Beam I/per pin=0.5A
I/per connector=0.75A
TBT/DP MUX1 PortA
TBT/DP MUX2 PortB
eDP MUX PortC
UV63
SN74AHC1G08DCKR_SC70-5
UV61
SN74AHC1G08DCKR_SC70-5
UV62
SN74AHC1G08DCKR_SC70-5
UV60
MC74VHC1G08DFT2G_SC70-5
M74VHC1GT125DF2G_SC70-5
74AUP1G07GW_TSSOP5
QV41
QV42
QV30A
QV30B
2N7002KDW_SOT363-6
L2N7002WT1G_SC-70-3
FUNCTION TABLE
A Input
OE Input
Y Output
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Compal Electronics, Inc.
DGFF CONN.
Security Classification
Compal Secret Data
Issued Date
2016/01/01
Deciphered Date
2017/01/01
LA-H271P
Rev 1.0
Tuesday, April 09, 2019
Sheet 27 of 103

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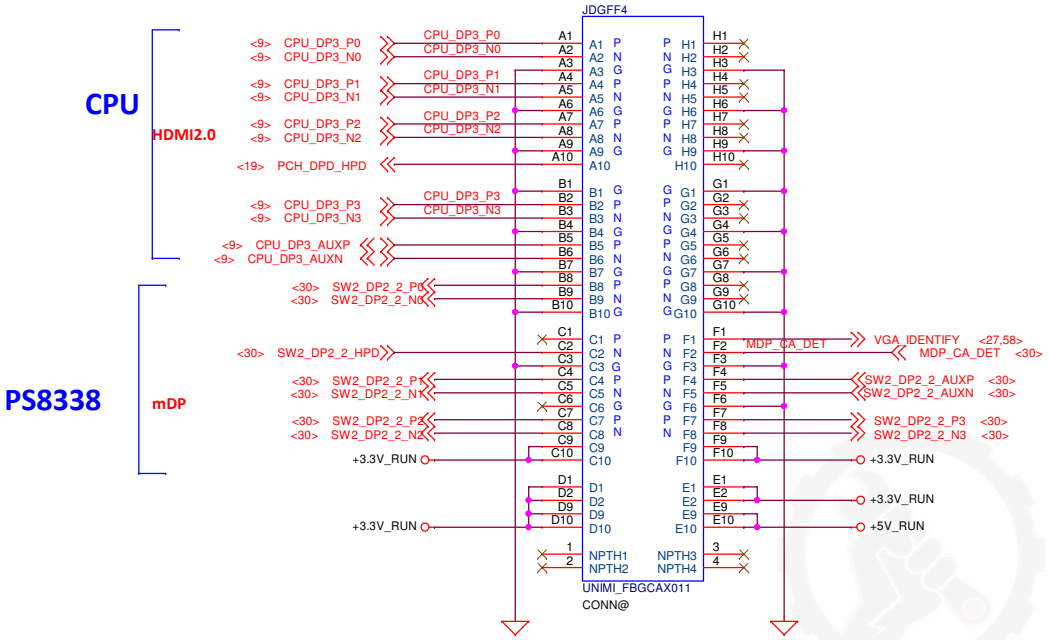
# UMA DGFF CON.

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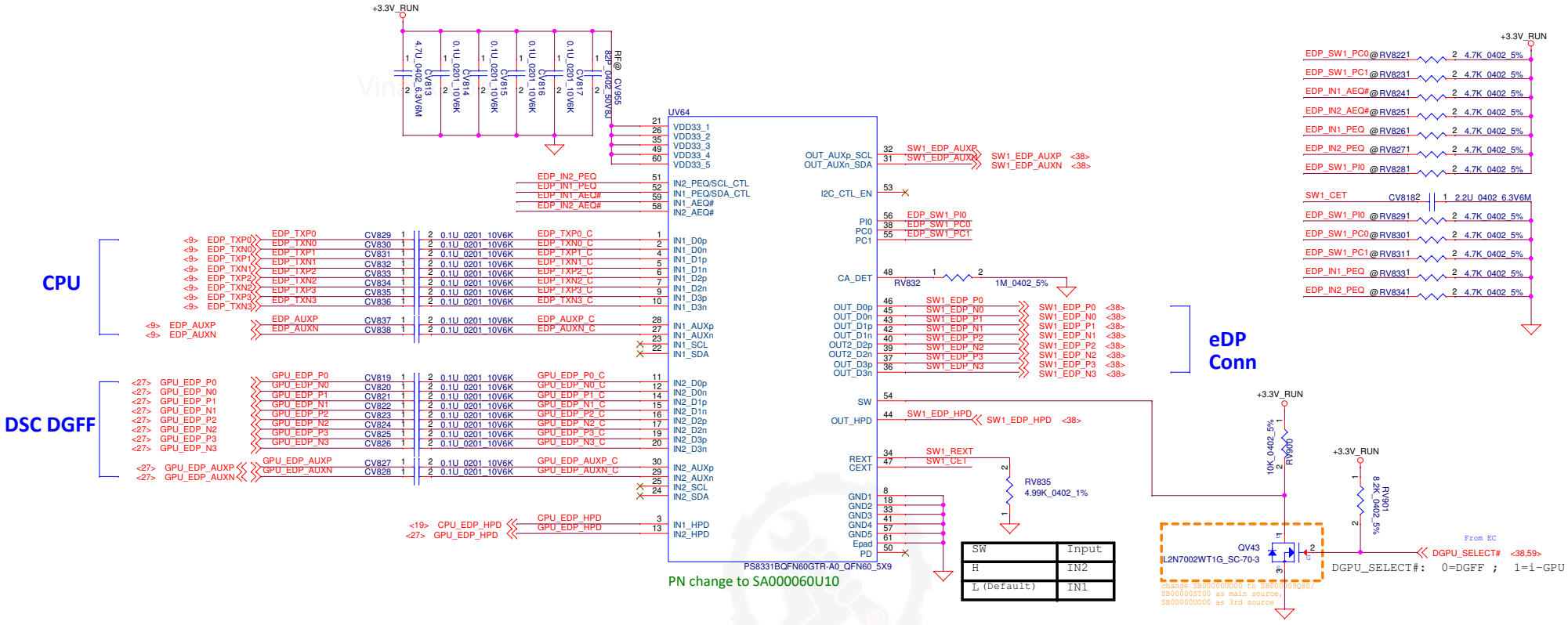
Compal Electronics, Inc.

Title: DGFF CONN.

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 28 of 103




INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

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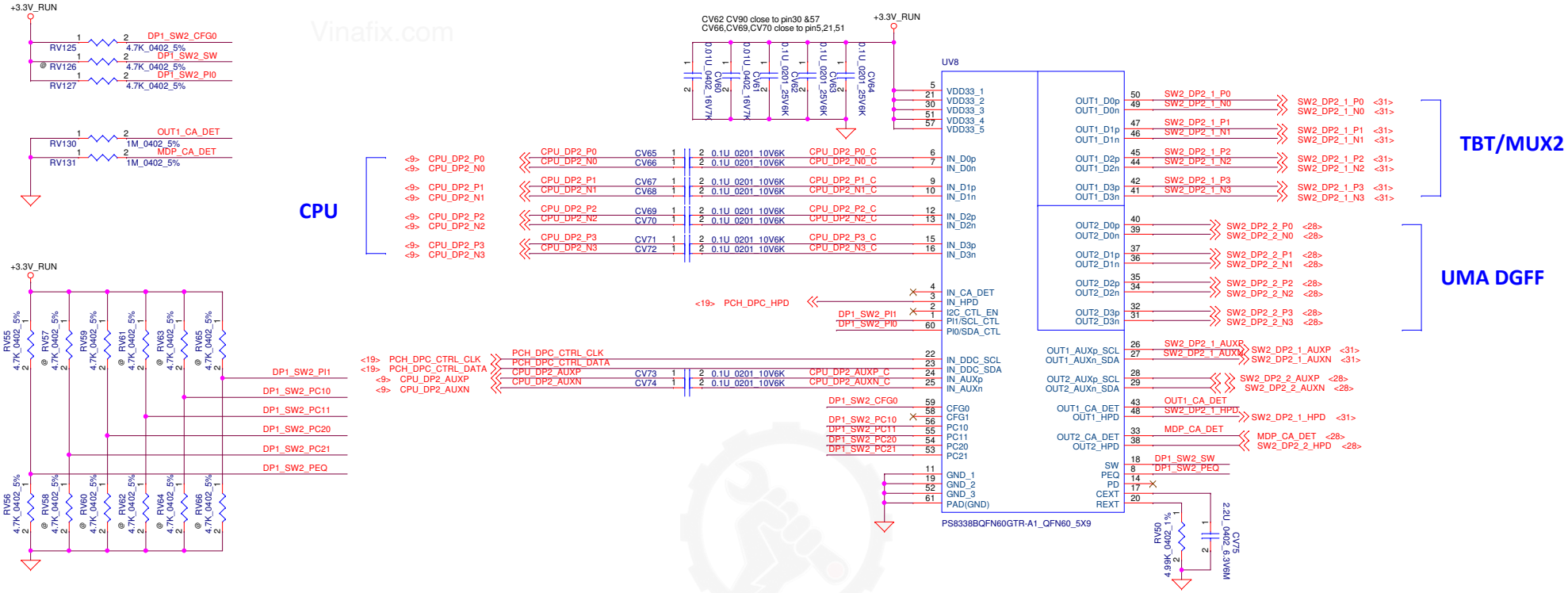
Compal Electronics, Inc.

Title: eDP MUX (PS8331)

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 29 of 103




Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected

For Automatic Switching Mode (CFG0 = H): (By OUT1_HPD and OUT2_HPD)
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

| | H | L |
|---|---|---|
| CFG0 | V | |
| SW | | V |

Programmable input equalization levels. Internal pull down at ~150KΩ, 3.3V I/O

PEQ =

L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2

H: HEQ, compensate channel loss up to 14.5dB @ HBR2

M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

***Overwritten by I2C register in I2C Control Mode***

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| Issued Date | 2016/01/01 | Deciphered Date | 2017/01/01 |

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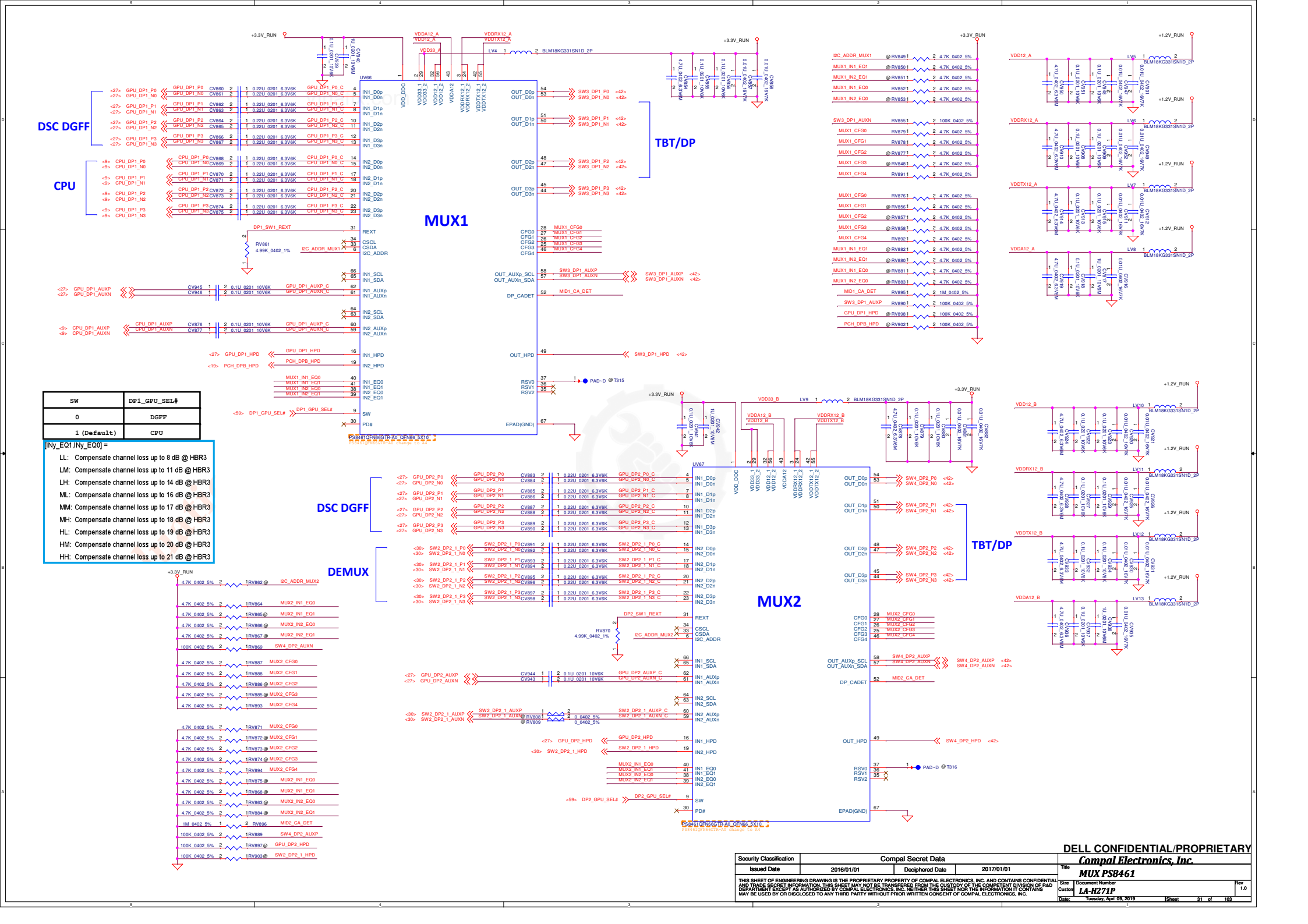
Compal Electronics, Inc.

Title: DP DeMUX (PS8338)

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 30 of 103

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Compal Electronics, Inc.

Title: MUX PS8461

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 31 of 103

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| Compal Electronics, Inc. | | | |
| Title: DGPU | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 32 of 103 | | |

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| Title: DGPU | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 33 of 103 | | |

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| Title: DGPU | | |
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| Date: Tuesday, April 09, 2019 | Sheet 34 of 103 | |

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| Title: DGPU | | |
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| Date: Tuesday, April 09, 2019 | Sheet 35 of 103 | |

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| Title: DGPU | | |
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| Date: Tuesday, April 09, 2019 | Sheet 36 of 103 | |

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| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: DGPU | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 37 of 103 | | |

same 111H40-100100-G4-R

CONN@
ACES_50398-04041-001
JEDP1

+BL_PWR_SRC
+LCDVDD
+CAMERA_VDD
+3.3V_RUN_R
DMIC_CLK
DMIC0
USB20_N11_R
USB20_P11_R
EMI@ LV1
BLM15PX221SN1D_2P
DISP_ON
LCD_CBL_DET# <19>
LCD_TST <58>
SW1_EDP_HPD <29>
DID2_GPIO1_MUX
SW1_EDP_AUXP_C
SW1_EDP_AUXN_C
SW1_EDP_N3_C
SW1_EDP_P3_C
SW1_EDP_N2_C
SW1_EDP_P2_C
SW1_EDP_N1_C
SW1_EDP_P1_C
SW1_EDP_N0_C
SW1_EDP_P0_C
0.1U_0201_10V6K
CV1 ... CV848

| Output | | Input | |
|---|---|---|---|
| | JEDP1 P28 | DID2_GPIO1 | DGPU_TYPE# |
| Intel/AMD | H | H | H |
| Intel/AMD | H | L | H |
| Intel/AMD | H | H | L |
| N/A | L | L | L |

+3.3V_RUN
@RV739 10K_0402_5%
DID2_GPIO1_HDR
QV44A L2N7002DW1T1G_SC88-6
RV740 10K_0402_5%
DID2_GPIO1_R
QV44B L2N7002DW1T1G_SC88-6
RV741 1K_0402_5%
DID2_GPIO1 <59>
RV742 0_0201_5%
DGPU_TYPE# <27>
RV737 0_0201_5%
RV738 0_0201_5%
CAM_MIC_CBL_DET# <14>
BIA_PWM

HDR monitor for AMD/NV/UMA
edp output detect 1/29

DV35 RB751VM-40TE-17_SOD323-2
PANEL_BKEN_PCH <14>
DV36 RB751VM-40TE-17_SOD323-2
DGFF_PANEL_BKEN <27>
DV37 RB751VM-40TE-17_SOD323-2
PANEL_BKEN_EC <58>
RV636 4.7K_0402_5%
DISP_ON
DMIC_CLK @EMI@ CV842 100P_0402_50V8J
DMIC0 @EMI@ CV843 100P_0402_50V8J

DV38 RB751VM-40TE-17_SOD323-2
BIA_PWM_PCH <14>
DV39 RB751VM-40TE-17_SOD323-2
DV40 RB751VM-40TE-17_SOD323-2
BIA_PWM_EC <58>
RV639 4.7K_0402_5%
CV844 0.1U_0201_10V6K
UV65 M74VHC1GT125DF2G_SC70-5
PN change to SA00000RY00
DGPU_SELECT# <29,59>
DGFF_BIA_PWM <27>

Touch Screen

TOUCH_SCREEN_DET#
RV8 10K_0402_5%
USB20_N9_R
USB20_P9_R
TOUCH_SCREEN_PD#
TOUCH_SCREEN_DET#
+5V_TSP +3.3V_TSP
140mA
JTS1 CVILU_CII106M1HRG-NH
CONN@
CV859 0.1U_0201_25V6K

back to TS only

+5V_TSP_+3.3V_TSP
1A_6V_T0603FF1000TM
+5V_RUN
Remove RV899
Material shortage SB000002P00 change to SB000003900 1/15
QV8 PJ2301_SOT23-3
+5V_TSP_+3.3V_TSP_F
RV6 47K_0402_5%
RV326 100K_0402_5%
3.3V_TS_EN_R
@RZ546 0_0201_5%
@RV323 0_0402_5%
@RV324 0_0402_5%
<58> 3.3V_TS_EN
<19> PCH_3.3V_TS_EN
QV7 L2N7002WT1G_SC-70-3
@CV953 0.1U_0201_25V6K

+BL_PWR_SRC +LCDVDD
CV849 0.1U_0402_50V7K
CV120 0.1U_0201_25V6K
Close to JEDP1

<15> USB20_N11
<15> USB20_P11
EMI@ LV2 MCM1012B900F06BP_4P
USB20_N11_R
USB20_P11_R
EMC request change main source to SM070003Z00
ESD@ DV41 PESD5V0U2BT_SOT23-3

For BL_PWR_SRC & LCDVDD monitor

+BL_PWR_SRC +3.3V_ALW +LCDVDD
RV907 4.3M_0402_1%
RV909 100K_0402_5%
RV910 100K_0402_5%
PANEL_MONITOR <58>
RV908 3M_0402_1%
QV23A L2N7002DW1T1G_SC88-6
QV23B L2N7002DW1T1G_SC88-6
RV911 1M_0402_1%
Keep PANEL_MONITOR voltage on 3V,change to 1M 3/29
RV907 change to 4.3M 1/23
RV908 change to 3M 4/8

<15> USB20_P9
<15> USB20_N9
MCM1012B900F06BP_4P EMI@ LV3
USB20_P9_R
USB20_N9_R
@ESD@ DV30 PESD5V0U2BT_SOT23-3
Close to JTS1

Close to JEDP1
DV4 ESD@ AZ5125-02S.R7G_SOT23-3
DMIC_CLK
DMIC0

+3.3V_RUN
SW1_EDP_AUXN 100K_0402_5% RV840
SW1_EDP_AUXP 100K_0402_5% RV842
+LCDVDD
SW1_EDP_HPD 4.7K_0402_5% @RV7
PS8331 HPD input internal PD 150K

Webcam PWR CTRL

+3.3V_RUN_R
RZ551 0_0603_5%
+3.3V_RUN_R_F
RZ550 0_0603_5%
+CAMERA_VDD
+3.3V_RUN
FZ1 1A_65V_T0603FF1000TM
QZ1 PJ2301_SOT23-3
+CAMERA_VDD_F
Reserve for FUSE location
@RZ545 0_0201_5%
@CZ510 10U_0402_6.3V6M
CZ531 0.1U_0201_25V6K
10P_0402_50V8J
CV954 0.1U_0201_25V6K
CZ529 0.1U_0201_25V6K
3.3V_CAM_EN# <17>
Close to JEDP1

JIR1 ACES_50208-0060N-P01 CONN@
IR_CAM_DET# <18>
IR_F
FZ2 1A_65V_T0603FF1000TM
+19.5VB

60mil
+19.5VB
FV1 1A_65V_T0603FF1000TM
QV1 AO6405_TSOP6
+BL_PWR_SRC_F
60mil
BL_PWR_SRC_ON
QV2 L2N7002WT1G_SC-70-3
RV4 100K_0402_5%
RV5 47K_0402_5%
<58> EN_INVPWR
CV13 1U_0603_50V6K
CV14 0.01U_0402_50V7K
CV15 0.1U_0402_50V7K
CV839 82P_0402_50V8J
RF require
CV840 82P_0402_50V8J
CV841 22P_0402_50V8J
CV842 22P_0402_50V8C
Panel backlight power control by EC

LCD Power

RF require
+LCDVDD
10P_0402_50V8J
CV851
CV852 82P_0402_50V8J
CV853 2.2P_0402_50V8C
CV16 10U_0402_6.3V6M
JUMP@ PJP12 PAD-OPEN1x1m
+EDP_VDD
UV24 G524B1T11U_SOT23-5
VOUT VIN GND EN /OC
@RV843 100K_0402_5%
+3.3V_ALW
DV42 RB751VM-40TE-17_SOD323-2
<14> ENVDD_PCH
<58> LCD_VCC_TEST_EN
<27> DGFF_ENVDD
DV3 BAT54CW_SOT323-3
RV3 100K_0402_5%

| | | | |
|---|---|---|---|
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| Issued Date | 2016/01/01 | Deciphered Date | 2017/01/01 |

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|---|---|---|---|
| Title | eDP / CAM / TS | | |
| Size | Document Number | | Rev |
| Custom | LA-H271P | | 1.0 |
| Date: | Tuesday, April 09, 2019 | Sheet | 38 of 103 |

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|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: DP | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
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|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: HDMI2.0 | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
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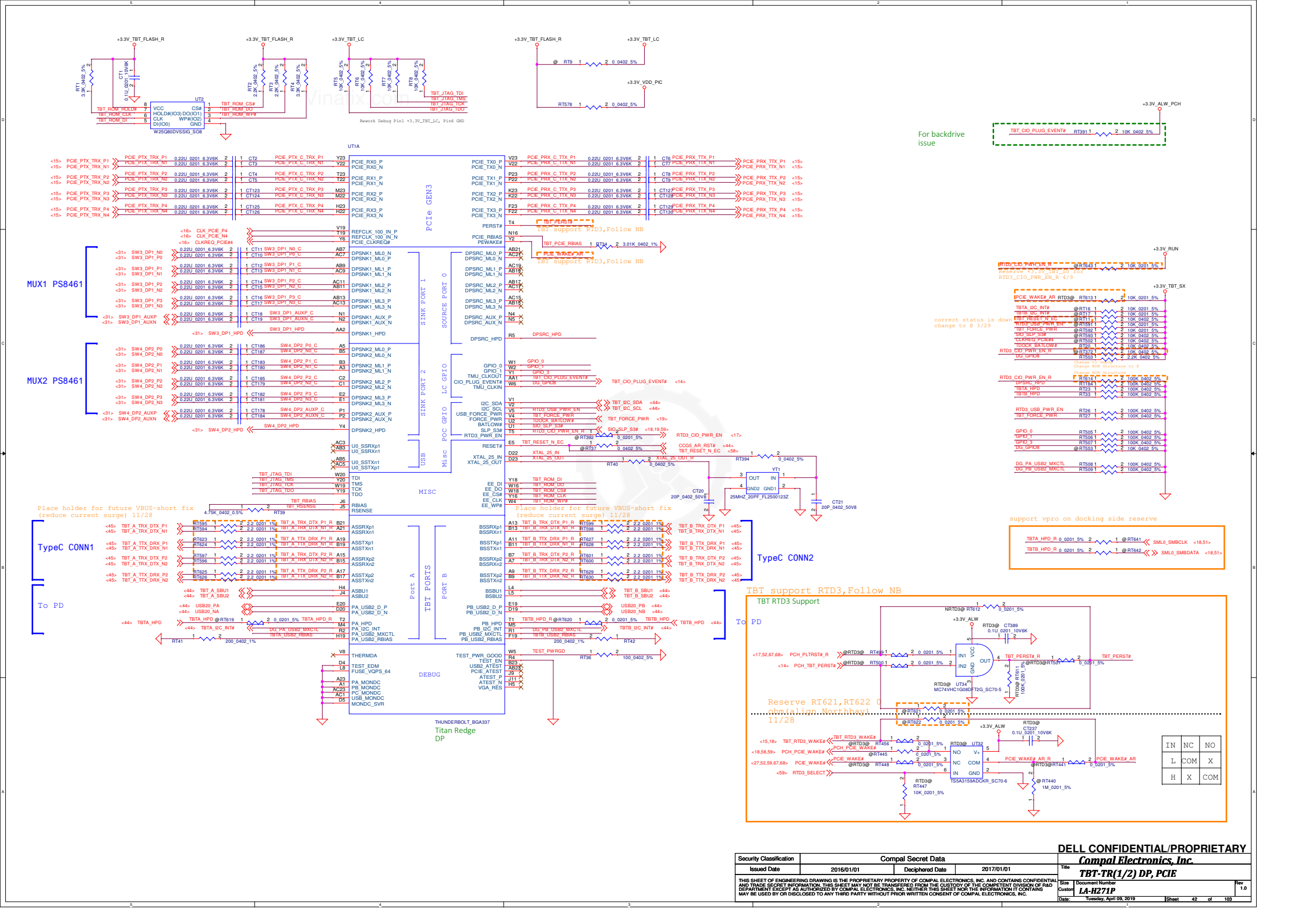
| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: CRT | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 41 of 103 | |


MUX1 PS8461
MUX2 PS8461
TypeC CONN1
TypeC CONN2
To PD
UT1A
PCIe GEN3
SINK PORT 1
SOURCE PORT 0
SINK PORT 2
LC GPIO
POC GPIO
USB
Misc
MISC
TBT PORTS
Port A
PORT B
DEBUG
THUNDERBOLT_BGA337
Titan Redge
DP
For backdrive issue
TBT support RTD3,Follow NB
TBT RTD3 Support
Reserve RT621,RT622 0 ohm(align Northbay) 11/28
support vpro on docking side reserve
Place holder for future VBUS-short fix (reduce current surge) 11/28
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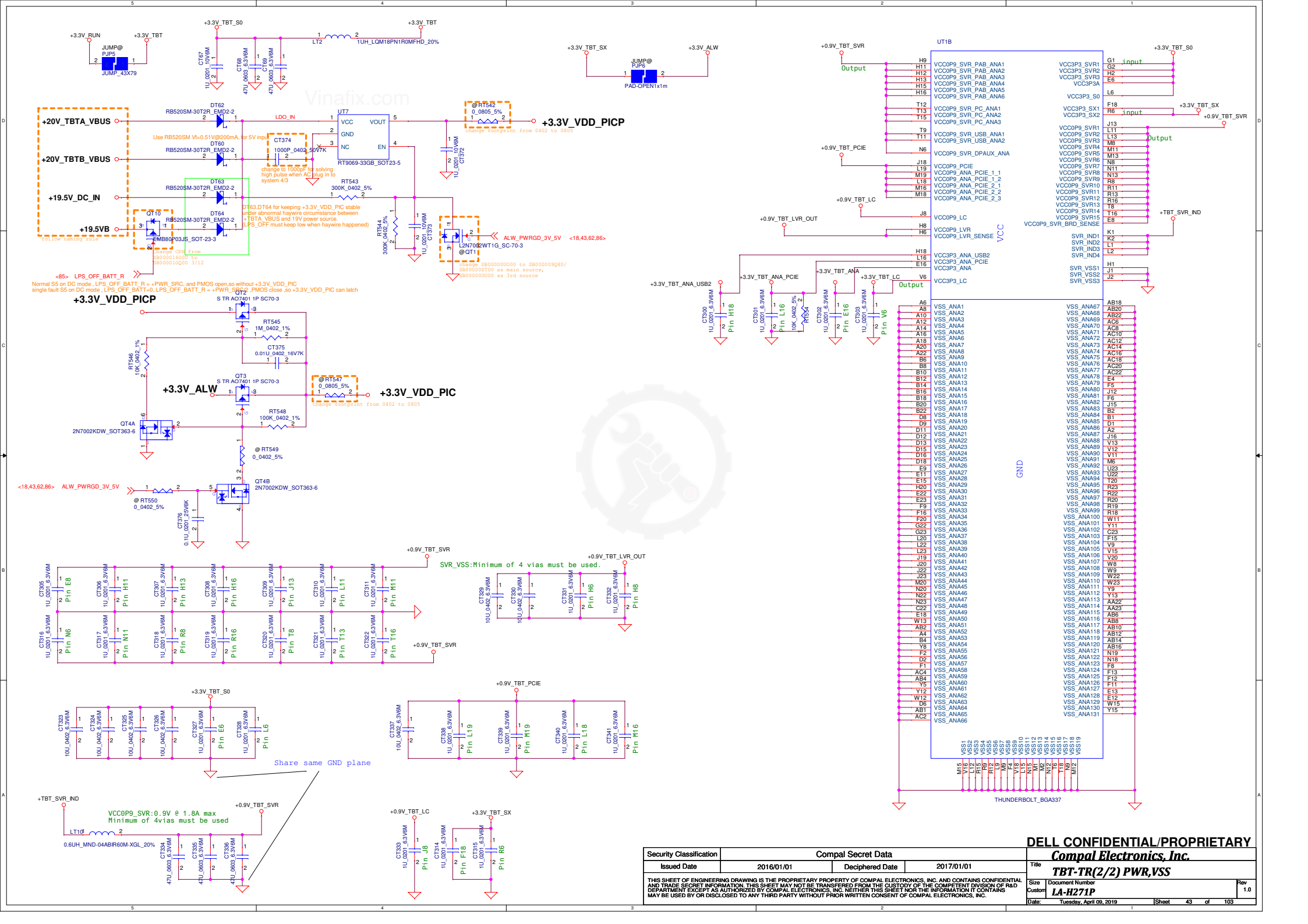
Compal Electronics, Inc.
TBT-TR(1/2) DP, PCIE
LA-H271P
Rev 1.0
Tuesday, April 09, 2019
Sheet 42 of 103
Security Classification
Compal Secret Data
Issued Date
2016/01/01
Deciphered Date
2017/01/01

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|---|---|---|---|
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Title: **TBT-TR(2/2) PWR,VSS**

| Size | Document Number | Rev |
|---|---|---|
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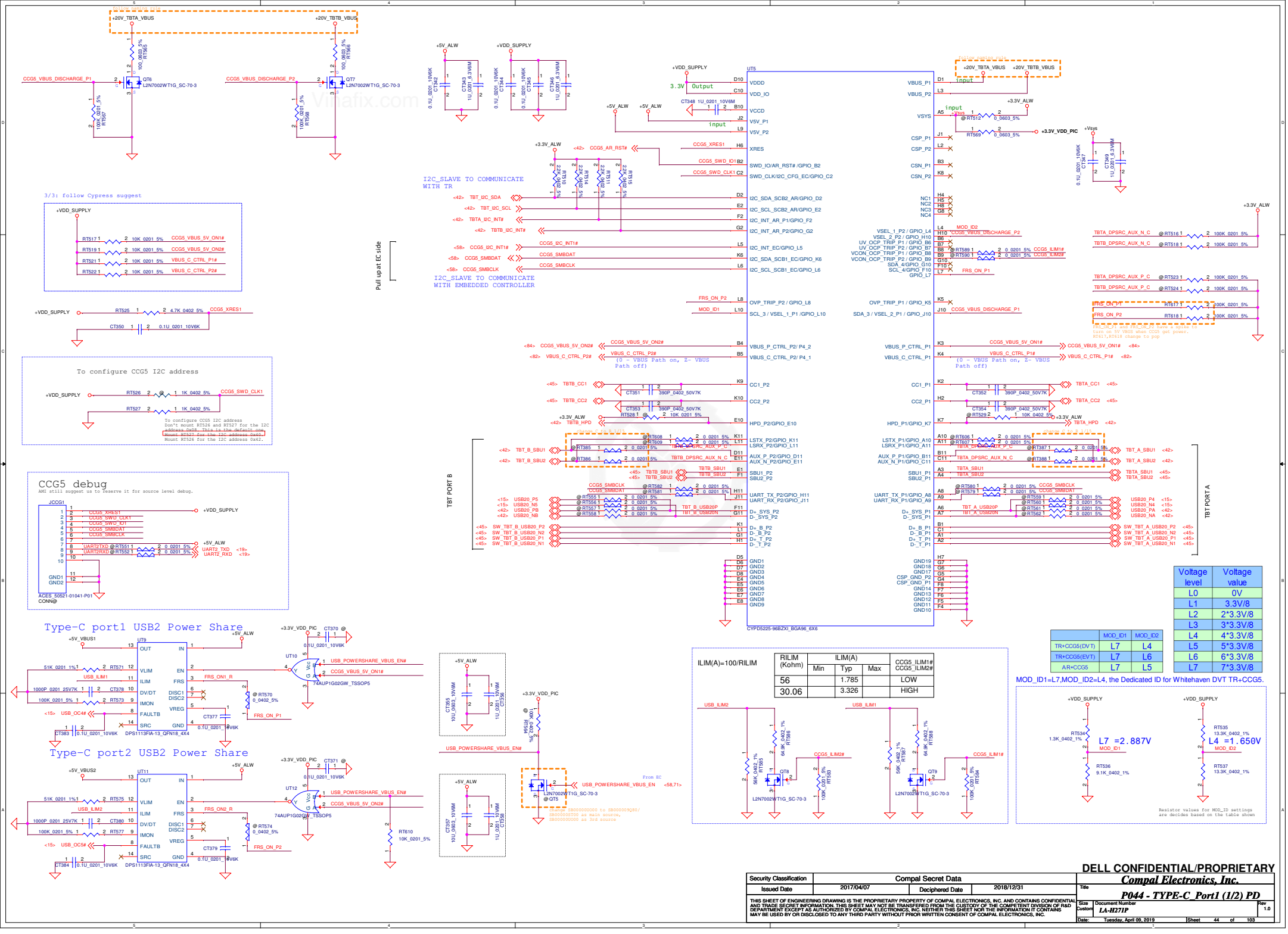
Date: Tuesday, April 09, 2019 | Sheet 43 of 103

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|---|---|
| Security Classification | Compal Secret Data |
| Issued Date | 2017/04/07 |
| Deciphered Date | 2018/12/31 |

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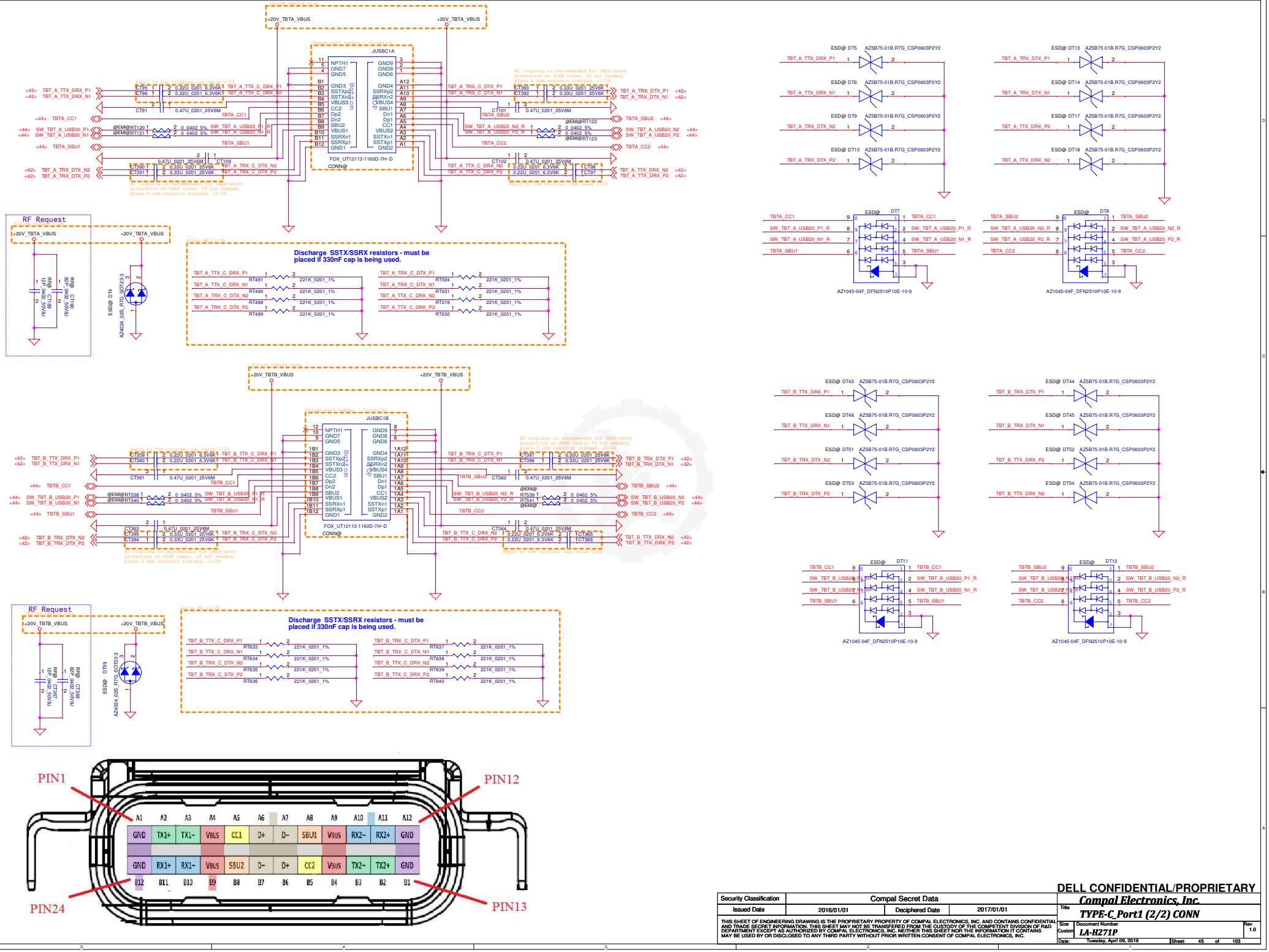
*Compal Electronics, Inc.*

Title: **P044 - TYPE-C_Port1 (1/2) PD**

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-H271P | 1.0 |

Date: Tuesday, April 09, 2019 | Sheet 44 of 103







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| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: TYPE-C_Port2-1 | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
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|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: TYPE-C_Port2-2 | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 47 of 103 | | |

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|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: TYPE-C_Port3-1 | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 48 of 103 | | |

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| Compal Electronics, Inc. | | | |
| Title: TYPE-C_Port3-2 | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 49 of 103 | | |

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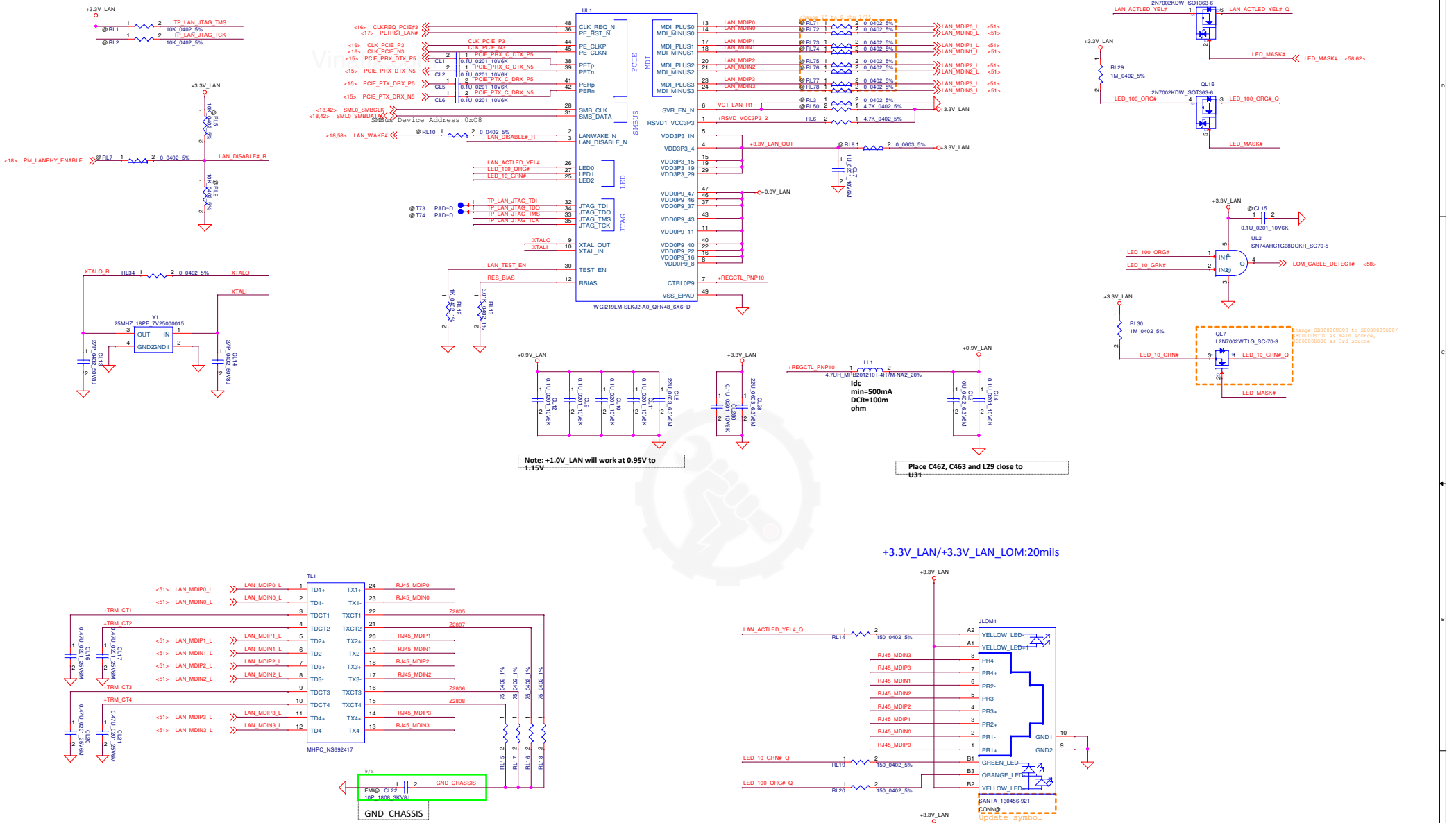
| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: TYPE-C_PWR Path | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 50 of 103 | |

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| Security Classification | Compal Secret Data | | |
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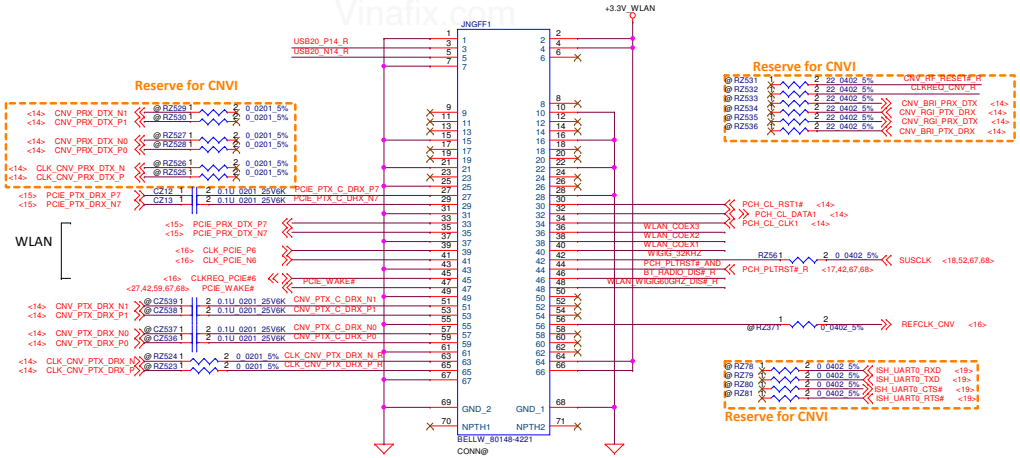
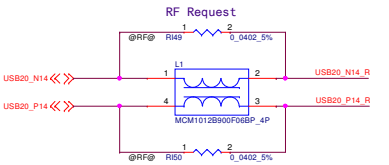
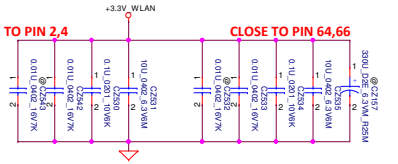
|---|---|---|---|
| Title | LAN / LAN SW | | |
| Size | Document Number | | Rev |
| Custom | LA-H271P | | 1.0 |
| Date: | Tuesday, April 09, 2019 | Sheet | 51 of 103 |

# WLAN/BT

## NGFF slot_1 Key A

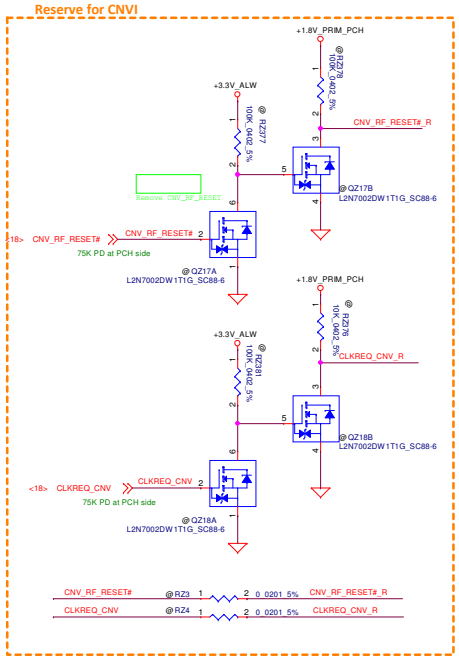


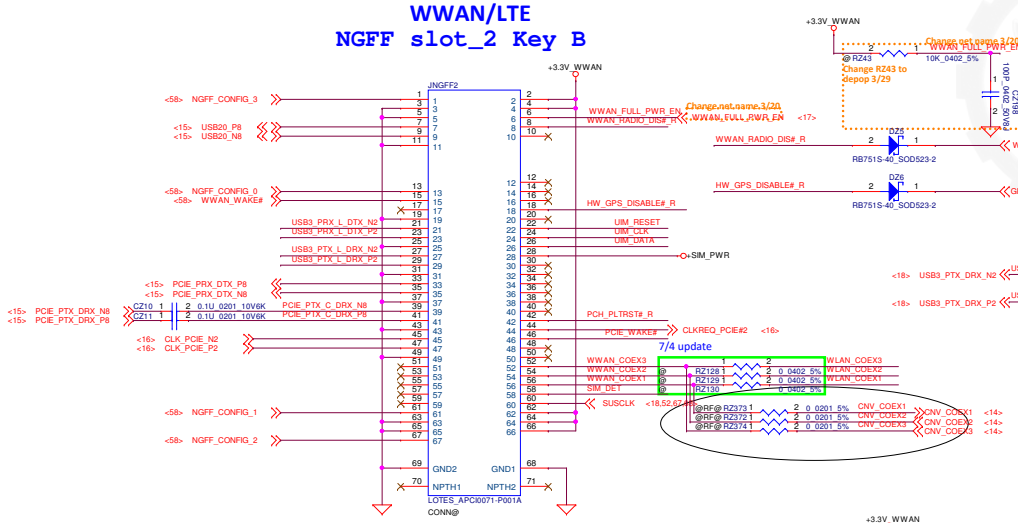


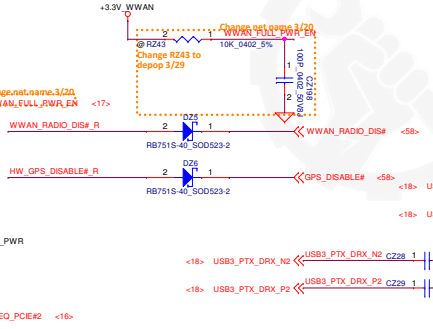


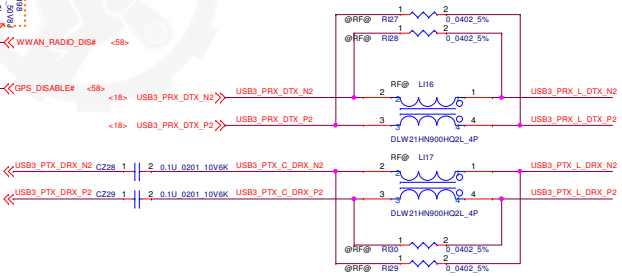



# WWAN/LTE

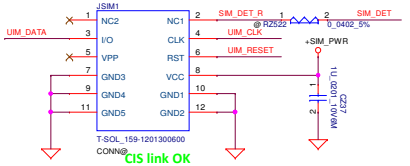
## NGFF slot_2 Key B

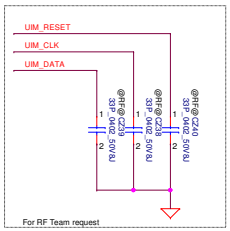


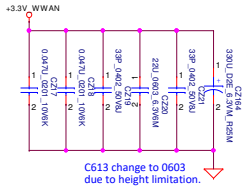




## SIM Card Push-Push




| STATE # | CONFIG_0 | CONFIG_1 | CONFIG_2 | CONFIG_3 | Module Type |
|---|---|---|---|---|---|
| ~~0~~ | ~~0~~ | ~~0~~ | ~~0~~ | ~~0~~ | ~~SSD-SATA~~ |
| 8 | 1 | 0 | 0 | 0 | WWAN |
| ~~14~~ | ~~1~~ | ~~0~~ | ~~1~~ | ~~1~~ | ~~HCA-PCIE~~ |
| ~~15~~ | ~~1~~ | ~~1~~ | ~~1~~ | ~~1~~ | ~~Cache~~ |




C613 change to 0603 due to height limitation.

C615 footprint change to C_APXK2R5ARA331MF451

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| Issued Date | 2016/01/01 | Deciphered Date | 2017/01/01 |

Compal Electronics, Inc.

Title: WLAN (w/ CNVi) / WWAN

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| Custom | LA-H271P | 1.0 |
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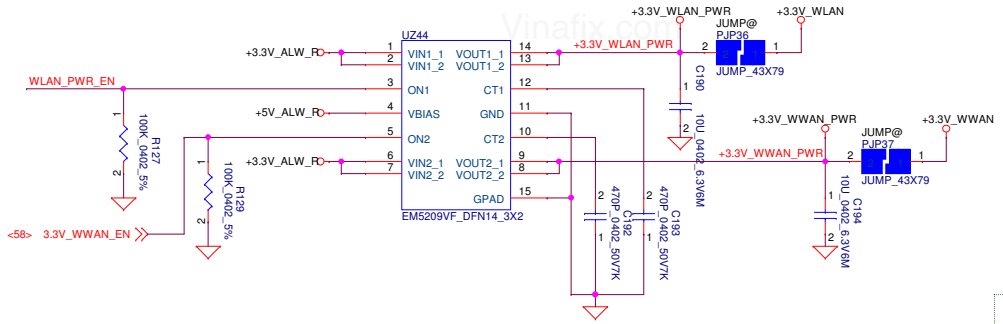
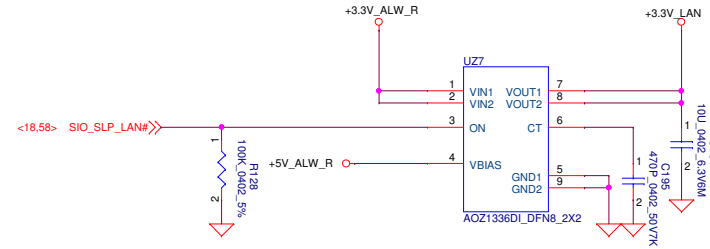
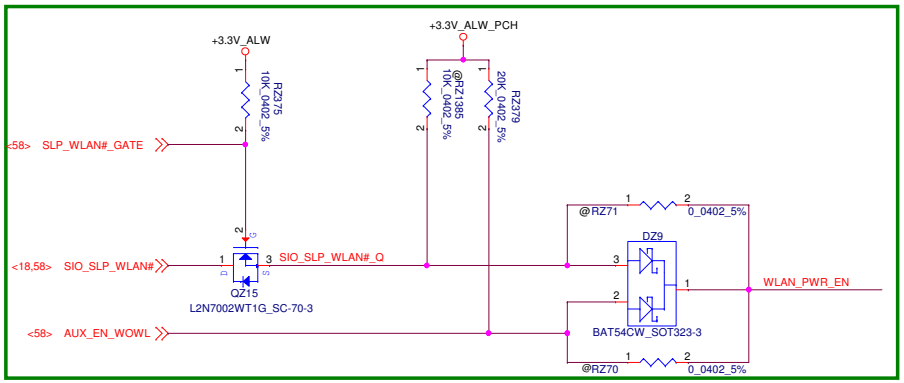
| Compal Electronics, Inc. | | | |
| Title: WIGIG / WIDI | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 53 of 103 | | |

# Power Control for WLAN &WWAN



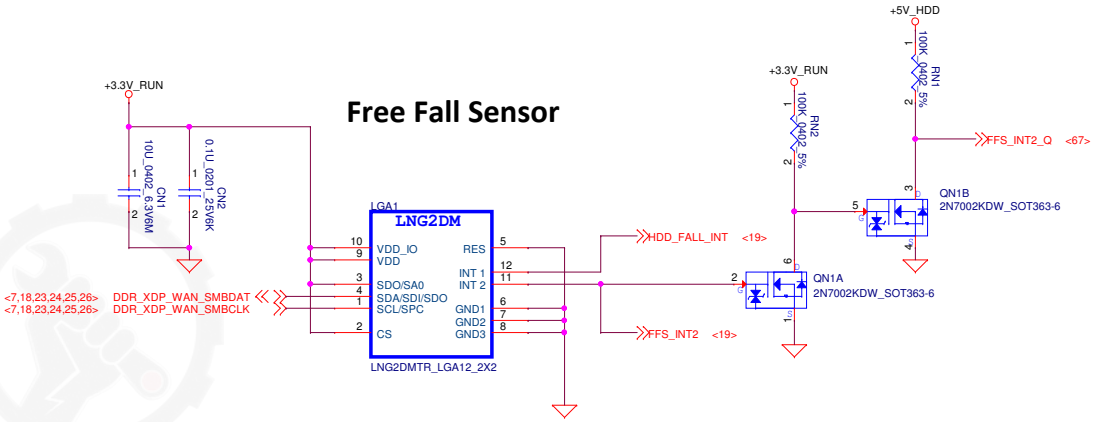

# Power Control for LAN



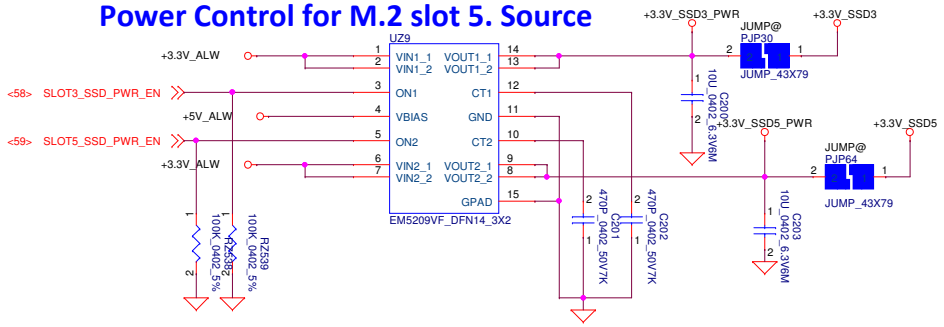




EC request to reserve OR gate for WLAN power enable

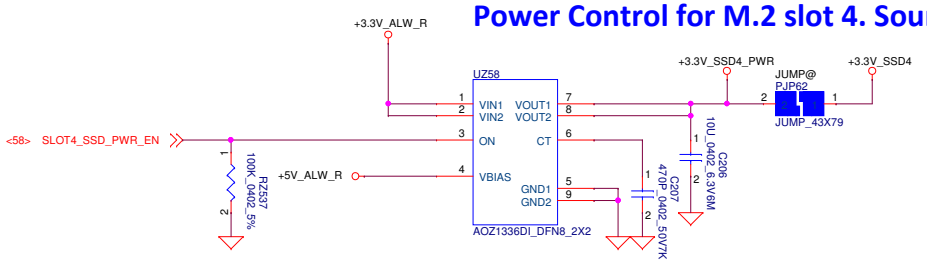
# Free Fall Sensor




# Power Control for M.2 slot 3. Source
# Power Control for M.2 slot 5. Source




# Power Control for M.2 slot 4. Source




| | | | |
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Compal Electronics, Inc.

Title: WLAN / WWAN PWR

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 54 of 103

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| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: PCIE device | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 55 of 103 | | |

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

## Internal Speakers Header

40 mils trace keep 20 mil spacing

Close to UA1 pin42~45

Close to UA1 pin14

place close to UA1 pin6

Verb table configures as 1 JD mode with internal 47K pull high to save external rBOM.

Add for solve pop noise and detect issue

CLASS-D POWER DOWN CONTROL CIRCUIT

2.5A

500mA

place at AGND and DGND plane

NO DOCK

Place CA29 close to Codec
only Samsung,Taiyo,Murata can use;

Place RA9 close to codec

Change BOM Structure to EMI# 1/21

Place CA70 close to codec

RF Request

HP-Out-Right
HP-Out-Left
Nokia-MIC
iPhone-MIC

Global Headset
Universal Jack

Update symbol

Place CA12 & CA13
close to Audio Jack

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| Security Classification | Compal Secret Data | | |
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Compal Electronics, Inc.

Title: Codec_ALC3281

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 56 of 103

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| Issued Date | 2016/01/01 | Deciphered Date | 2017/01/01 |

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| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: Audio Ampfilper | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 57 of 103 | | |

| | GPIO223 | GPIO224 | GPIO227 | GPIO016 | GPIO056 | GPIO055 |
|---|---|---|---|---|---|---|
| eSPI | NA | NA | PRIM_PWRGD | NA | NA | PCH_RSMRST# |
| LPC | SHD_IO0 | SHD_IO1 | SHD_IO2 | SHD_IO3 | SHD_CLK | SHD_CS# |

* For Version B IC

| | GPIO204 | GPIO011 | GPIO100 | GPIO021 | GPIO067 |
|---|---|---|---|---|---|
| eSPI | NA | NA | NA | SIO_RCIN# | NA |
| LPC | RSMRST# | SIO_EXT_SMI# | SIO_EXT_SCI# | LPCPD# | CLKRUN# |

## RF Request

## RP change to single Resistor

## For EMI request

## 32 KHz Clock

| Deep Sleep support | |
|---|---|
| non Deep Sleep | 1 |
| Deep Sleep | 0 |

| | VGA_ID0 |
|---|---|
| Discrete | 0 |
| UMA | 1 |

Connect to GND on DSC CARD
NC on UMA card.

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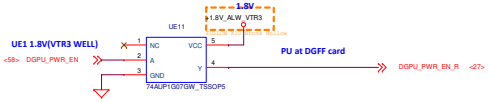
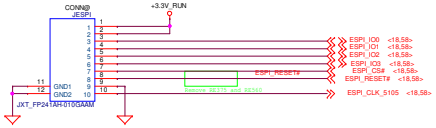
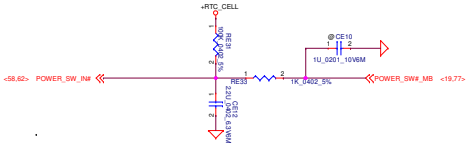
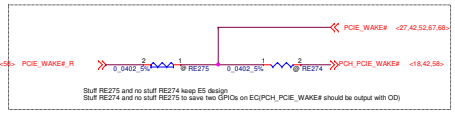
| | | |
|---|---|---|
| Title | EC MEC5106 | |
| Size | Document Number | Rev |
| Custom | LA-H271P | 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 58 of 103 | |

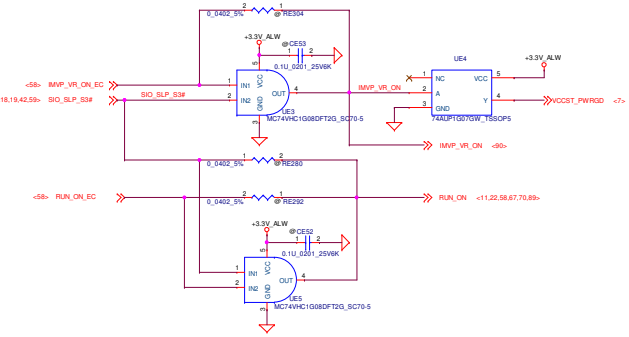


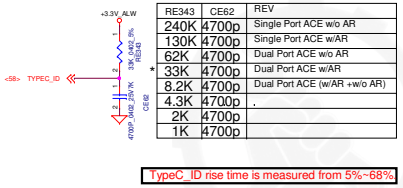




| LPC 80Port Debug | LPC | ESPI |
|---|---|---|
| 1 | +3.3V_RUN | +3.3V_RUN |
| 2 | +3.3V_RUN | +3.3V_RUN |
| 3 | LPC_LAD0 | ESPI_IO0 |
| 4 | LPC_LAD1 | ESPI_IO1 |
| 5 | LPC_LAD2 | ESPI_IO2 |
| 6 | LPC_LAD3 | ESPI_IO3 |
| 7 | LPC_FRAME# | ESPI_CS# |
| 8 | PCH_PLTRST# | NA |
| 9 | GND | GND |
| 10 | LPC_CLOCK | ESPI_CLK |

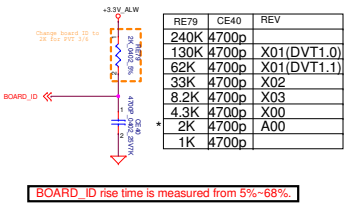


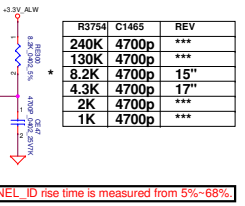




| RE343 | CE62 | REV |
|---|---|---|
| 240K | 4700p | Single Port ACE w/o AR |
| 130K | 4700p | Single Port ACE w/AR |
| 62K | 4700p | Dual Port ACE w/o AR |
| 33K | 4700p | Dual Port ACE w/AR |
| 8.2K | 4700p | Dual Port ACE (w/AR +w/o AR) |
| 4.3K | 4700p | . |
| 2K | 4700p | |
| 1K | 4700p | |

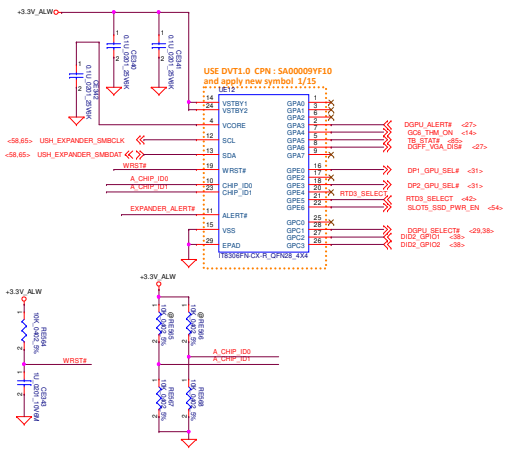



| RE79 | CE40 | REV |
|---|---|---|
| 240K | 4700p | |
| 130K | 4700p | X01(DVT1.0) |
| 62K | 4700p | X01(DVT1.1) |
| 33K | 4700p | X02 |
| 8.2K | 4700p | X03 |
| 4.3K | 4700p | X00 |
| 2K | 4700p | A00 |
| 1K | 4700p | |




| R3754 | C1465 | REV |
|---|---|---|
| 240K | 4700p | *** |
| 130K | 4700p | *** |
| 8.2K | 4700p | 15" |
| 4.3K | 4700p | 17" |
| 2K | 4700p | *** |
| 1K | 4700p | *** |

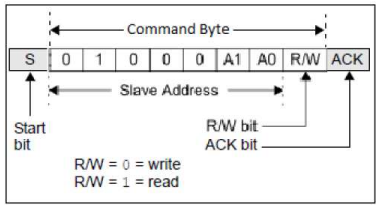
# SIO IT8306

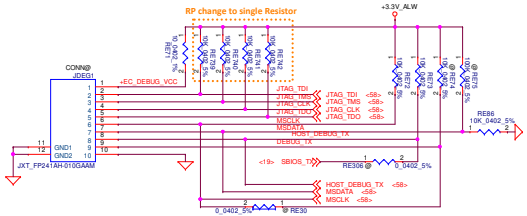


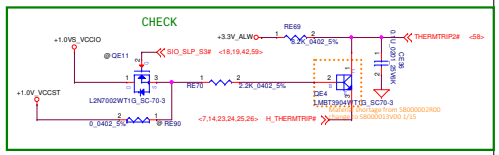


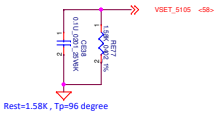
For I2C SAD+Read/Write patterns

| Command | SAD[7:3] | ID[1] | ID[0] | R/W= | SAD+R/W |
|---|---|---|---|---|---|
| Read | 01000 | 0 | 0 | 1 | 01000001 (41h) |
| Write | 01000 | 0 | 0 | 0 | 01000000 (40h) |
| Read | 01000 | 0 | 1 | 1 | 01000011 (43h) |
| Write | 01000 | 0 | 1 | 0 | 01000010 (42h) |
| Read | 01000 | 1 | 0 | 1 | 01000101 (45h) |
| Write | 01000 | 1 | 0 | 0 | 01000100 (44h) |
| Read | 01000 | 1 | 1 | 1 | 01000111 (47h) |
| Write | 01000 | 1 | 1 | 0 | 01000110 (46h) |



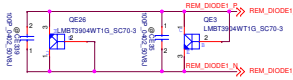



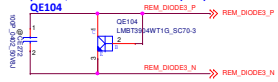

| Channel | Location |
|---|---|
| DP1/DN1 | CPU OTP |
| DP1A/DN1A | CPU VR |
| DP2A/DN2A | M.2 2280 |
| DP3/DN3 | DIMM(TOP) |
| DP4/DN4 | WWAN |
| | |

DP1/DN1 for CPU OTP on QE3, place QE3 close to CPU and CE35 close to QE3.

DN1a/DP1a for CPU VR(PU1100) on QE26, place QE26 close to CPU and CE339 close to QE26

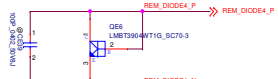



DP3/DN3 for SODIMM(TOP) on QE104, place QE104 close to SODIMM(TOP) and CE272 close to QE104




DN2A/DP2A for M.2 2280 on QE7, place QE7 close to JNGFF3 and CE46 close to QE7.


DP4/DN4 for WWAN on QE6, place QE6 close to JNGFF1 and CE39 close to QE6




QE26,QE3,QE104,QE7,QE6 change from SB000008P00 to SB000013V00

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Title: EC MEC5106 SUPPORT

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 59 of 103

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| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: Secure & Reset IC | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 60 of 103 | |

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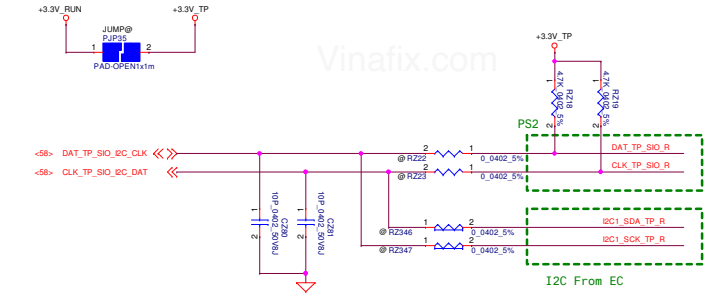
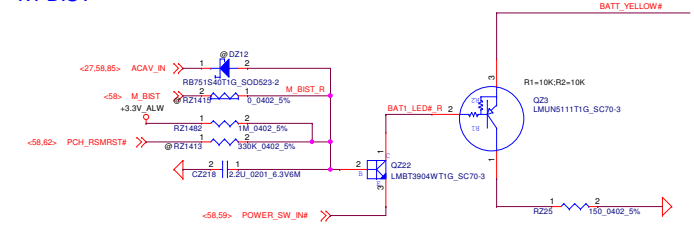
| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: LEDs(Controller) | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 61 of 103 | |

## Touch Pad



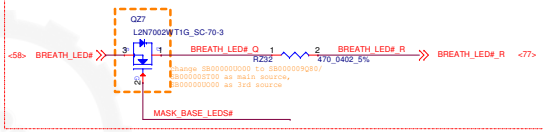

Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

## M BIST

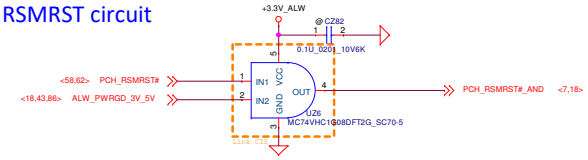



## Battery LED

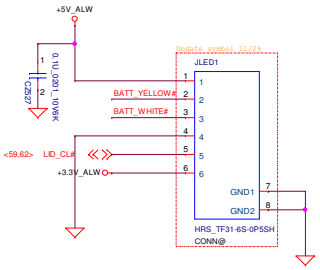

## Breath LED

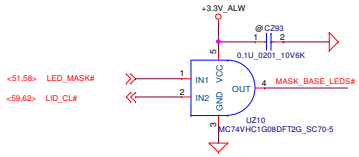



## RSMRST circuit



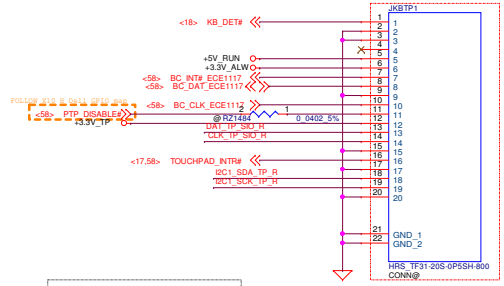

## To LED/B Conn




| LED Circuit Control Table | | |
|---|---|---|
| | LED_MASK# | LID_CL# |
| Mask All LEDs (Sniffer Function) | 0 | X |
| Mask Base MB LEDs (Lid Closed) | 1 | 0 |
| Do not Mask LEDs (Lid Opened) | 1 | 1 |

## Keyboard

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| Title | KB / TP / LED / LID | | |
|---|---|---|---|
| Size | Document Number | | Rev |
| Custom | LA-H271P | | 1.0 |
| Date: | Tuesday, April 09, 2019 | Sheet | 62 of 103 |

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|---|---|---|
| Compal Electronics, Inc. | | |
| Title: KB / TP / LED / LID | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 63 of 103 | |

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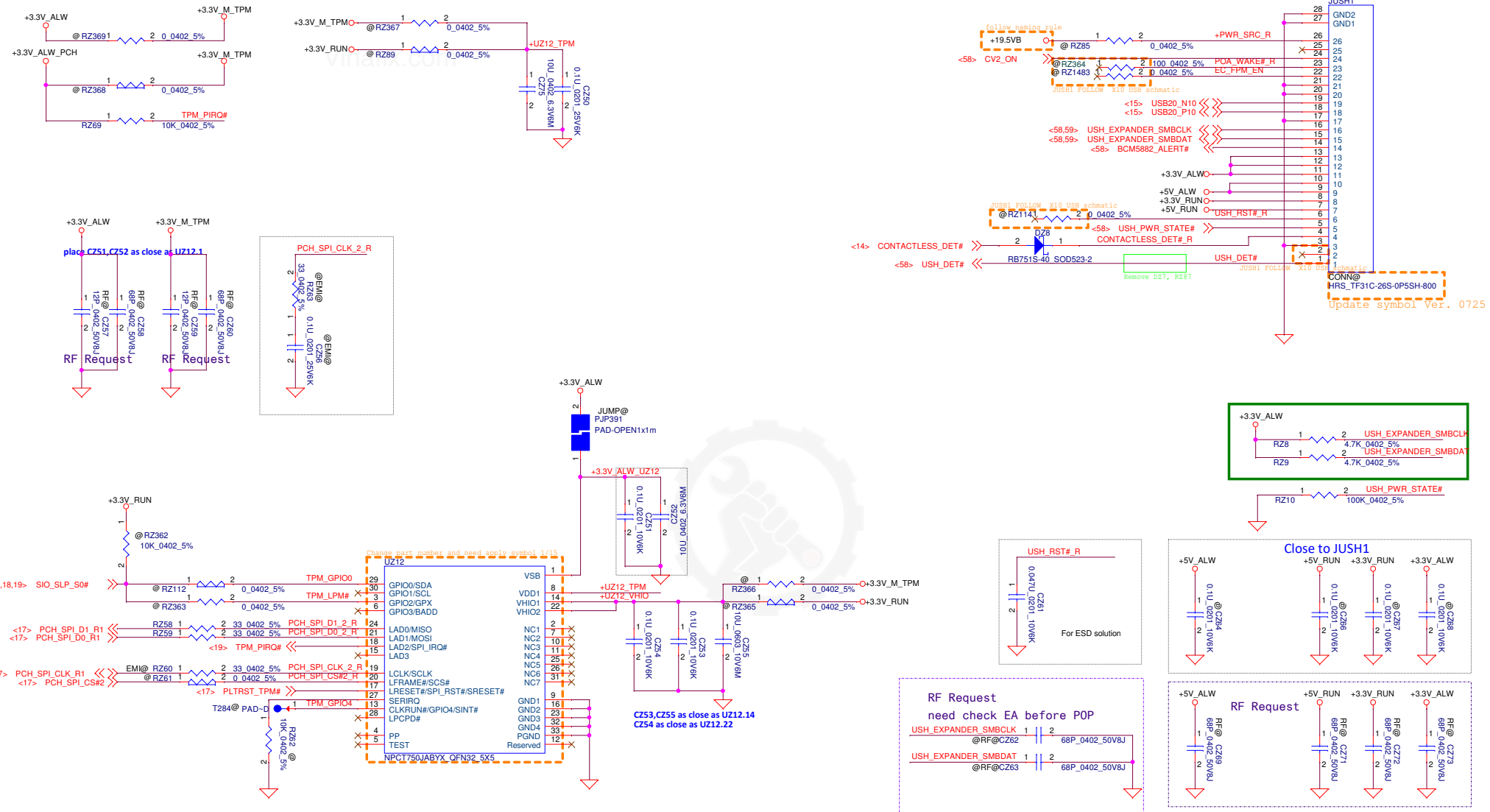
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: KB / TP / LED / LID | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 64 of 103 | |




| | Pop | Depop | Comment |
|---|---|---|---|
| NPCT65x | RZ89, RZ366, RZ62 | RZ365, RZ367 | VDD - V_RUN Power<br>VHIO - V_SPI Power |
| NPCT75x | RZ89, RZ365 | RZ367, RZ366, RZ62 | Option1 (recommended)<br>VDD and VHIO - V_RUN power |
| NPCT75x | RZ367, RZ366 | RZ89, RZ365, RZ62 | Option2 (for Z1 sample [early sample])<br>VDD and VHIO - V_SPI power |

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Compal Electronics, Inc.

Title: TPM/USH

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 65 of 103

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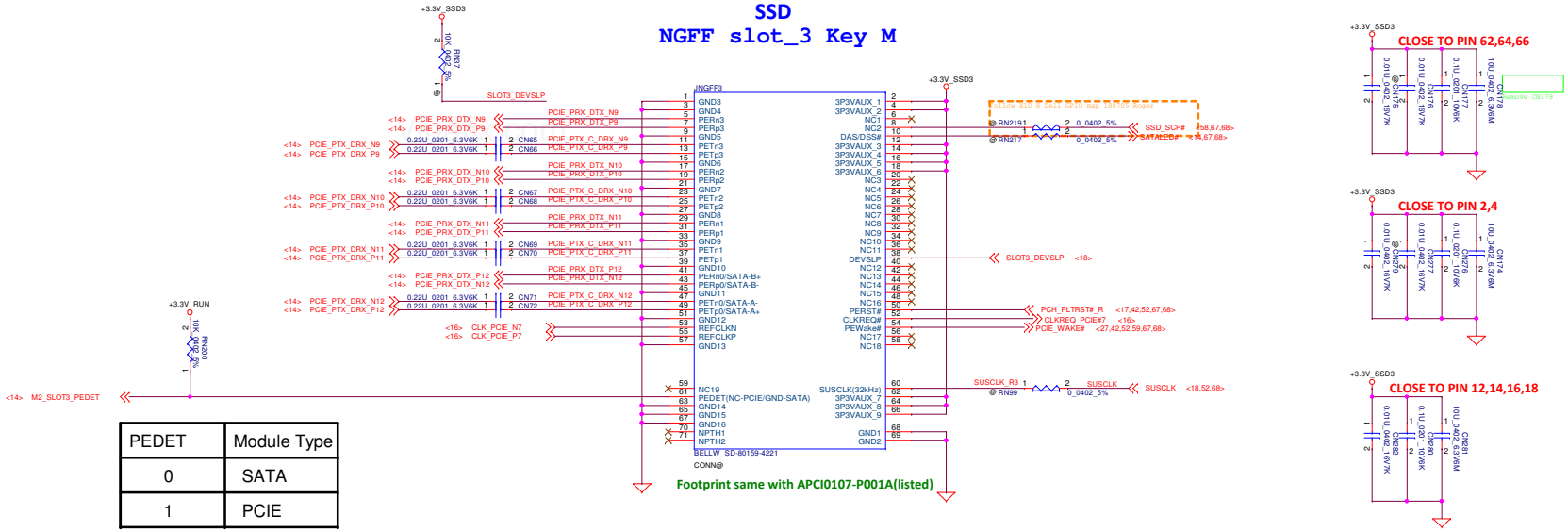
| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: HDD/ODD/FFS Conn | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 66 of 103 | |

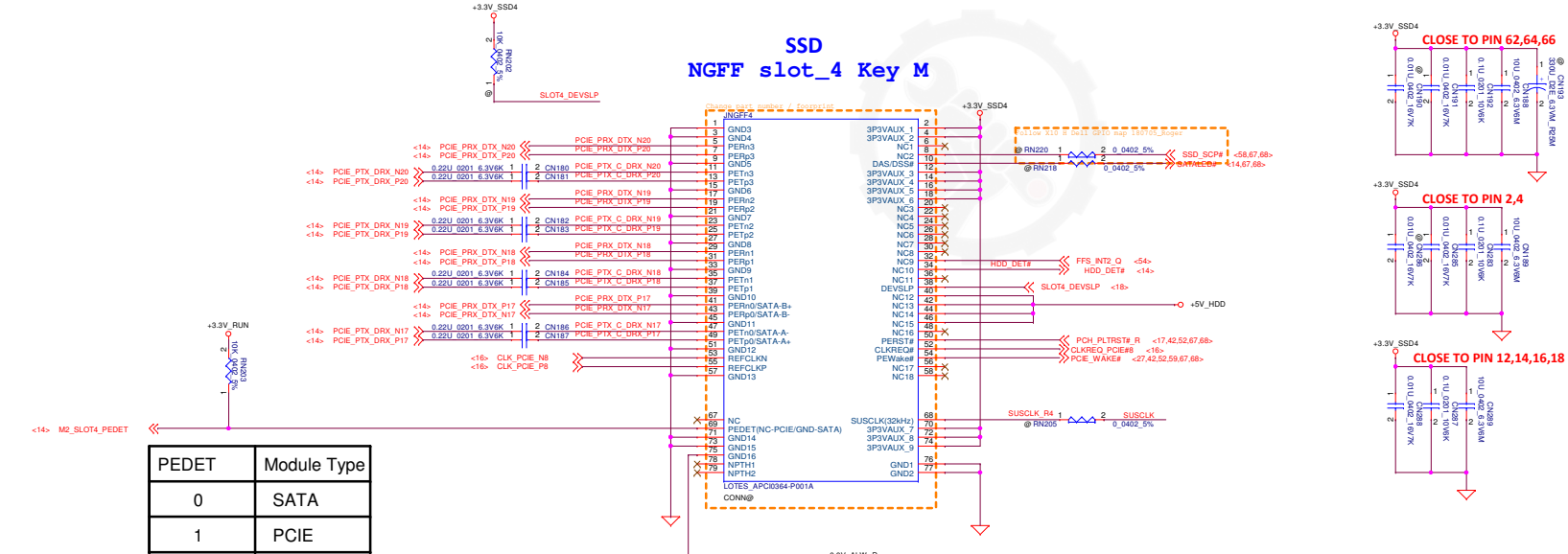
# SSD
# NGFF slot_3 Key M



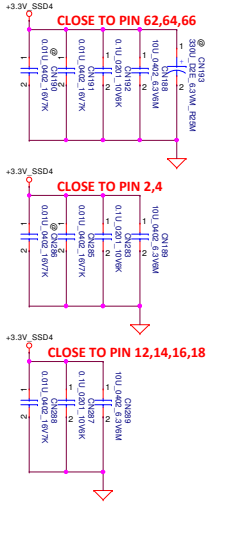

| PEDET | Module Type |
|---|---|
| 0 | SATA |
| 1 | PCIE |



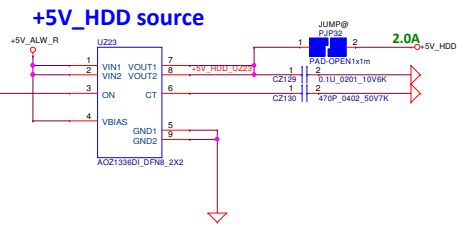

# SSD
# NGFF slot_4 Key M




| PEDET | Module Type |
|---|---|
| 0 | SATA |
| 1 | PCIE |




## +5V_HDD source




| HDD_IFDET | Module Type |
|---|---|
| 0 | NVME |
| 1 | HDD |

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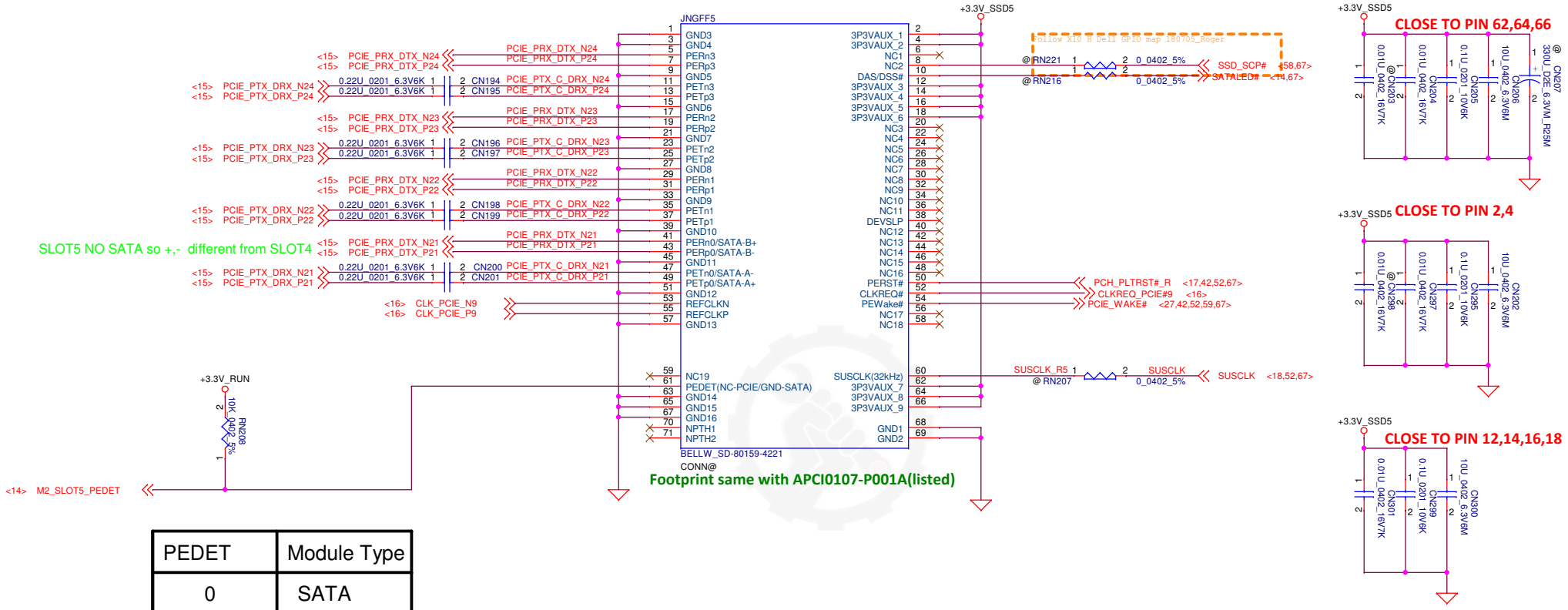
Title: SSD SLOT3 / 4

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 67 of 103

# SSD
# NGFF slot_5 Key M




| PEDET | Module Type |
|---|---|
| 0 | SATA |
| 1 | PCIE |

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Title: SSD SLOT5

Size: Custom | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 68 of 103

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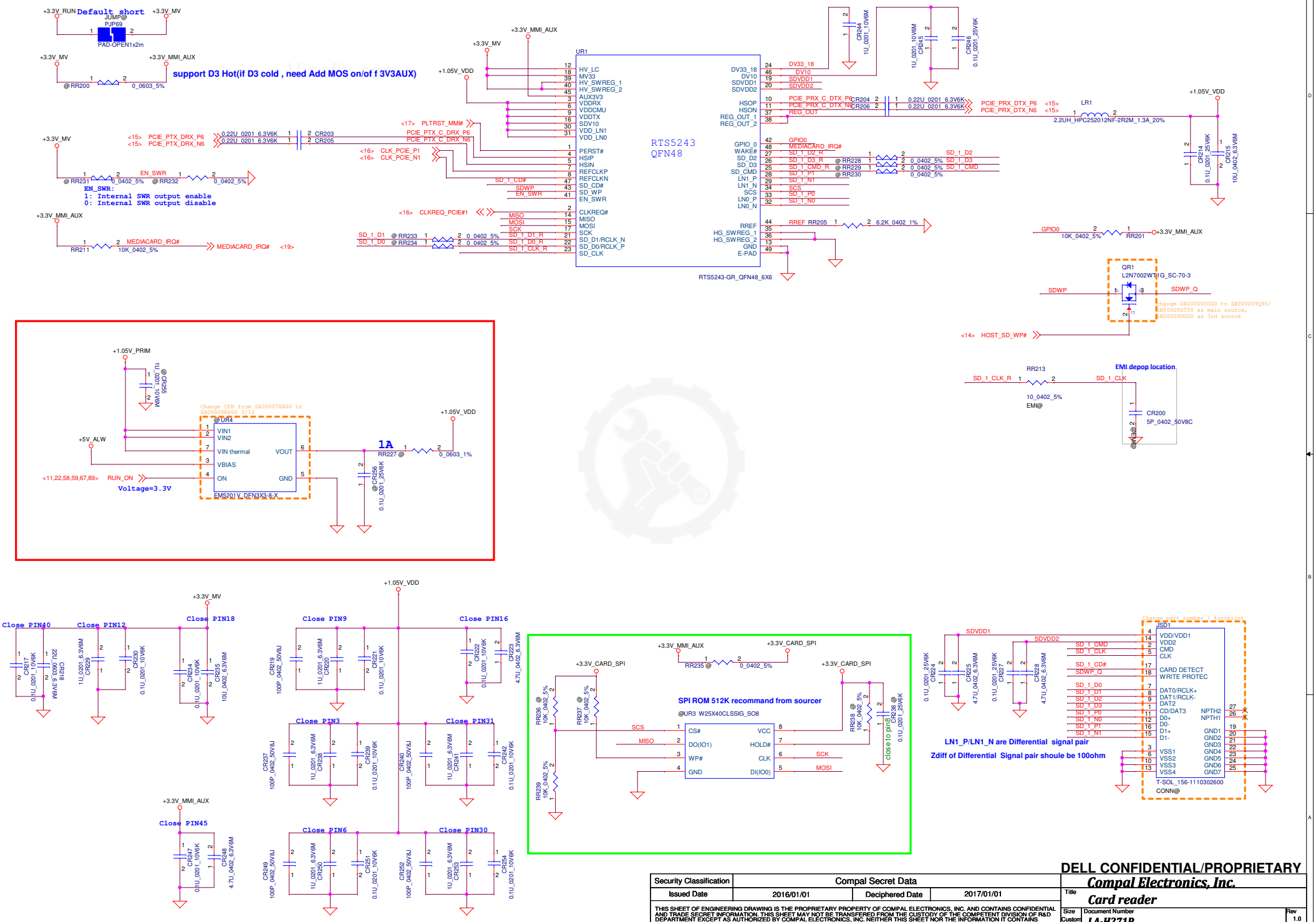
| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: eMMC / UFS | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 69 of 103 | |

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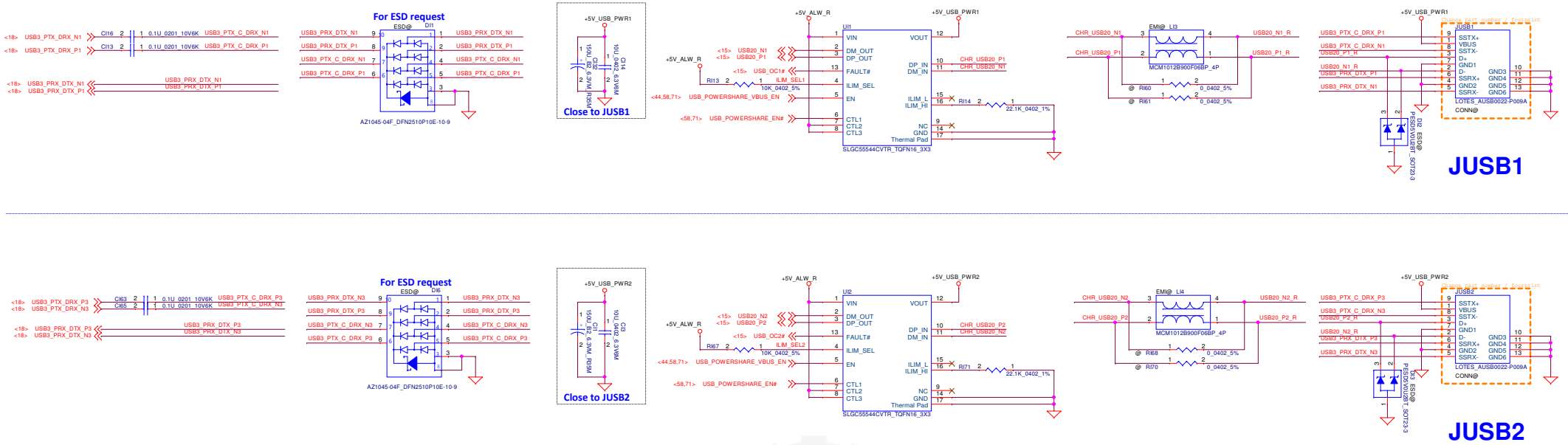
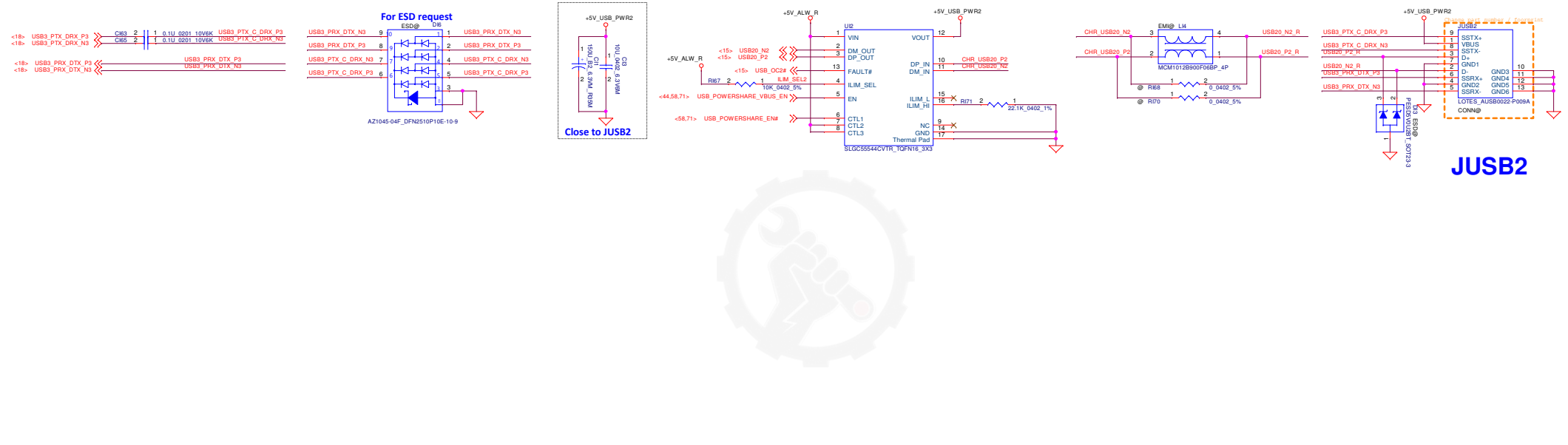
*Compal Electronics, Inc.*

Title: *Card reader*

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-H271P | 1.0 |

Date: Tuesday, April 09, 2019 | Sheet 70 of 103

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|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: USB2/USB3 TYPEA | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | | Sheet 71 of 103 | |

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|---|---|---|
| Compal Electronics, Inc. | | |
| Title: USB2/USB3 TYPEA | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 72 of 103 | |

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|---|---|---|
| Compal Electronics, Inc. | | |
| Title: USB2/USB3 DB | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 73 of 103 | |

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|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: Dock | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 74 of 103 | | |

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| Compal Electronics, Inc. | | |
| Title: USB | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 75 of 103 | |

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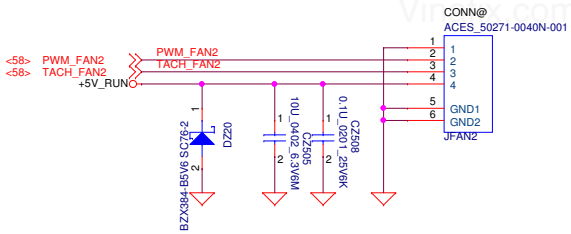
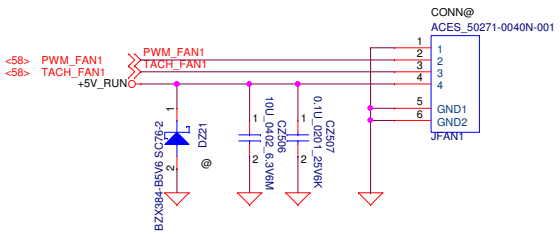
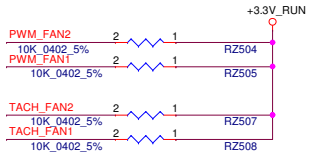
| Compal Electronics, Inc. | | |
| Title: USB | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 76 of 103 | |

# DGFF FAN

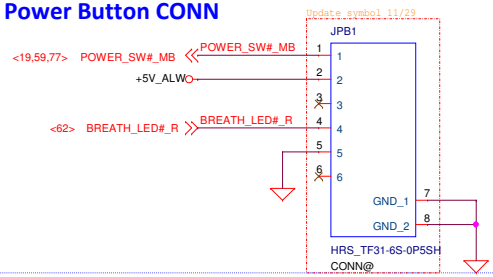



# CPU FAN

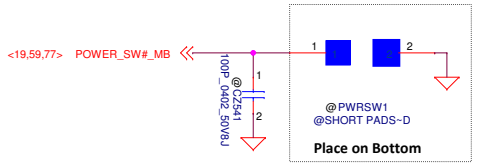



## Power Button CONN

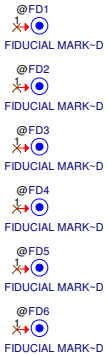


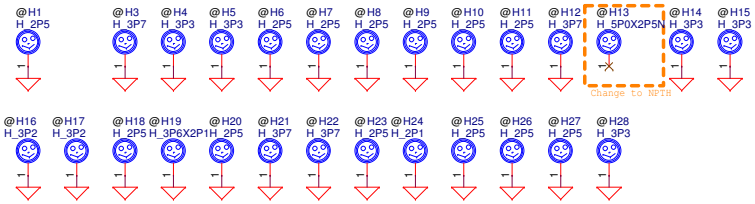

## Power Switch for debug

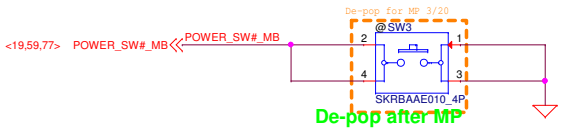




## Fiducial Mark

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|---|---|---|
| Title | <Title> | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 77 of 103 | |

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|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: DC INTERFACE & Sequence | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 78 of 103 | | |

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|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: XDP/CMC/APS...debug | | | |
| Size: Custom | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 79 of 103 | | |

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| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: Google Debug & INAs | | |
| Size: Custom | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 80 of 103 | |

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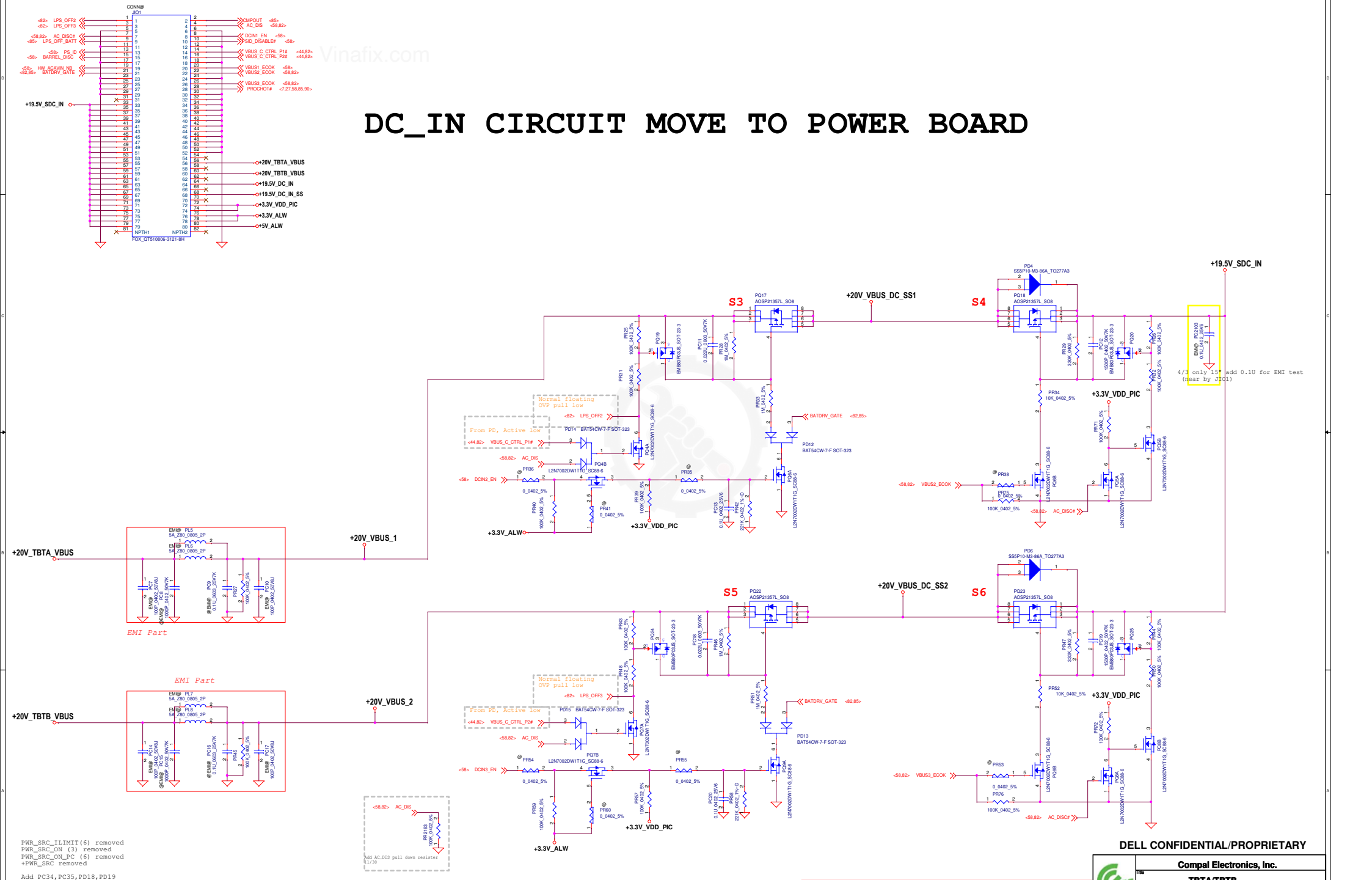
| | | |
|---|---|---|
| | Compal Electronics, Inc. | |
| | Title: Reserve | |
| Size | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 81 of 103 | |

# DC_IN CIRCUIT MOVE TO POWER BOARD



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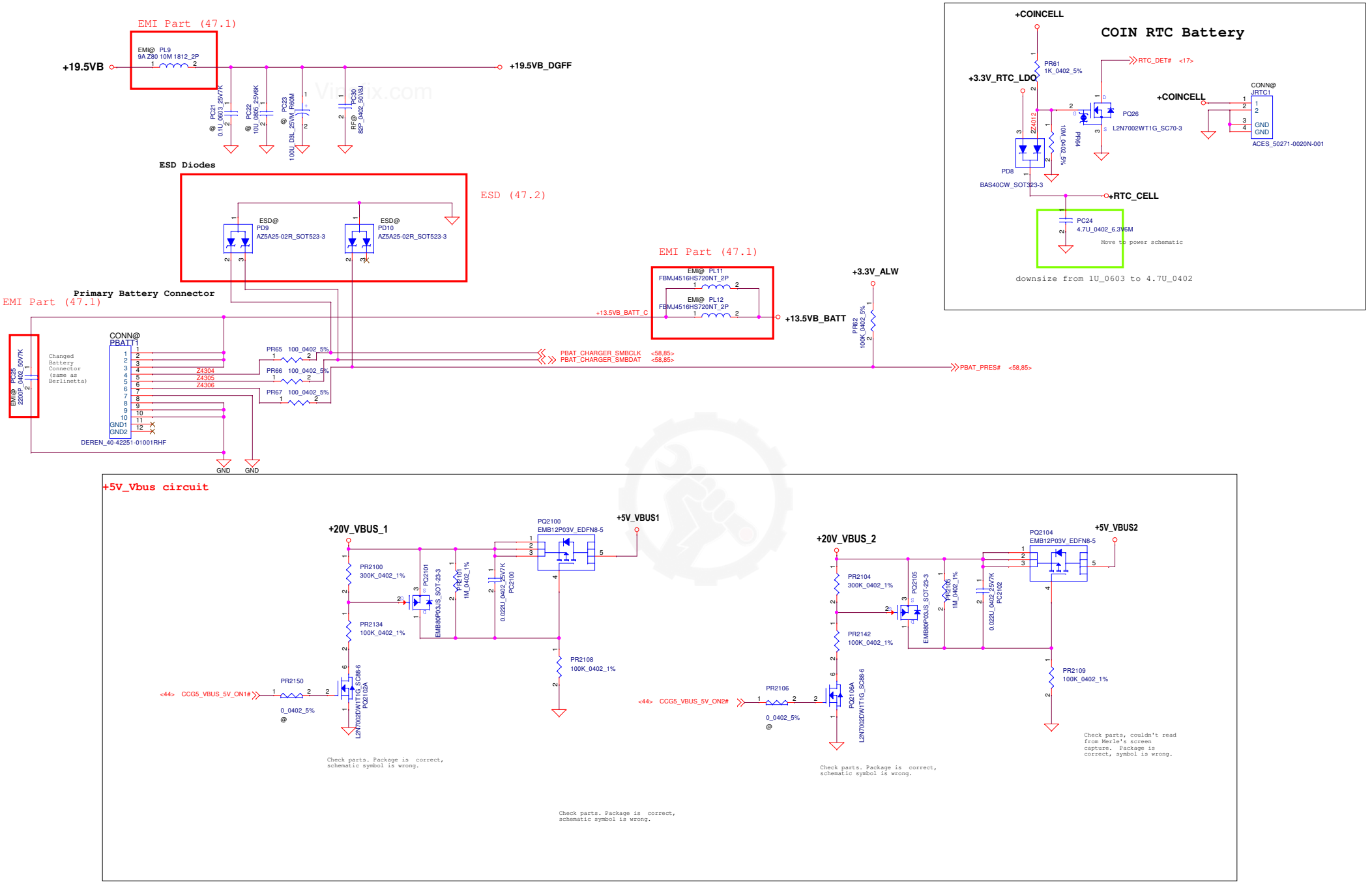
# PD COMPARATOR CIRCUIT MOVE TO POWER BOARD

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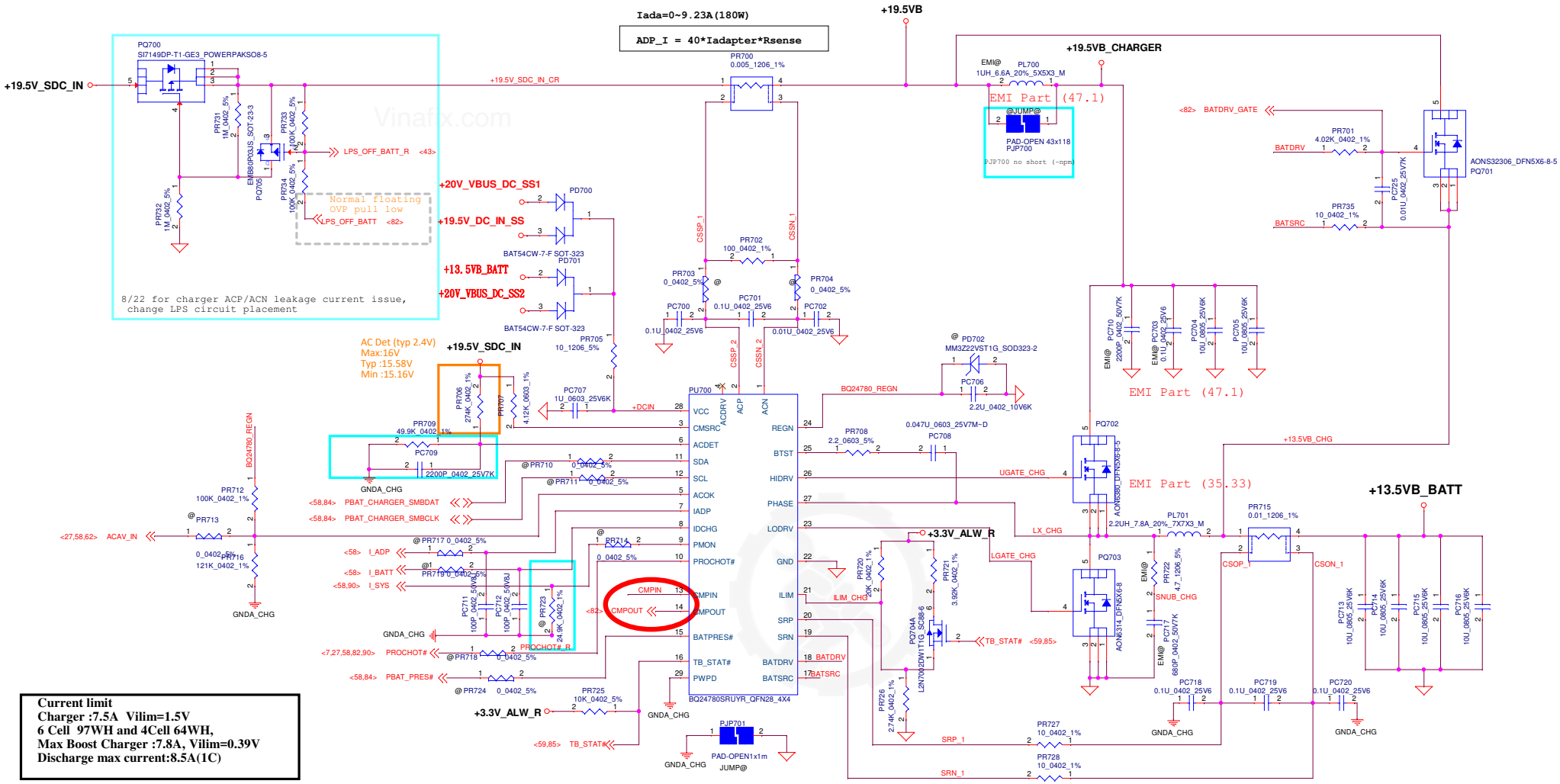
Title: BATT/DGFF/RTC/5V_VBUS

Size | Document Number: LA-H271P | Rev: 1.0

Date: Tuesday, April 09, 2019 | Sheet 84 of 103


Iada=0~9.23A(180W)
ADP_I = 40*Iadapter*Rsense
+19.5VB
+19.5V_SDC_IN
+19.5VB_CHARGER
EMI Part (47.1)
EMI Part (47.1)
EMI Part (35.33)
+13.5VB_BATT
+20V_VBUS_DC_SS1
+19.5V_DC_IN_SS
+13.5VB_BATT
+20V_VBUS_DC_SS2
Normal floating
OVP pull low
LPS_OFF_BATT
8/22 for charger ACP/ACN leakage current issue,
change LPS circuit placement
AC Det (typ 2.4V)
Max:16V
Typ :15.58V
Min :15.16V
PU700
BQ24780SRUYR_QFN28_4X4
Current limit
Charger :7.5A Vilim=1.5V
6 Cell 97WH and 4Cell 64WH,
Max Boost Charger :7.8A, Vilim=0.39V
Discharge max current:8.5A(1C)
2016/7/22
For Temp voltage test ,
+DC_IN setting for ACAVIN_NB need less than 17.55V ,
so change PR737 from SD034665380
(S RES 1/16W 665K +-1% 0402) to
SD034634380(S RES 1/16W 634K +-1% 0402)
CMP_REF=2.3V
+DC_IN>17V then ACAV_IN_NB high
for 3cell battery 13.05V
(CMP_REF=2.3V
+DC_IN>17.6V then ACAV_IN_NB high
for 4cell battery 17.4V[Miramar setting])
Crane and Miramar setting
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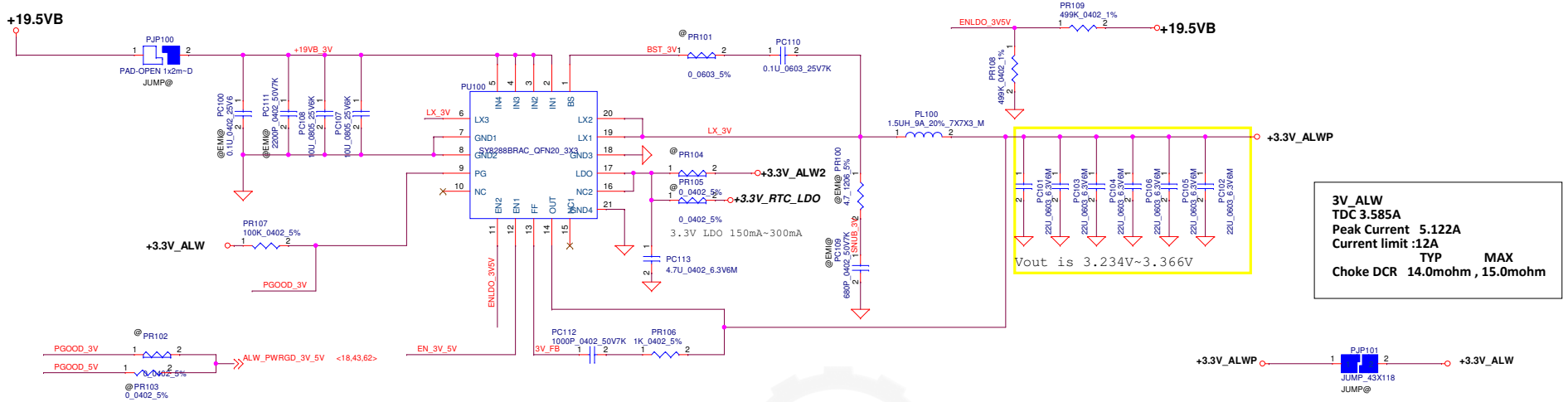
Compal Electronics, Inc.
Charger
LA-H271P
Tuesday, April 09, 2019
85
103

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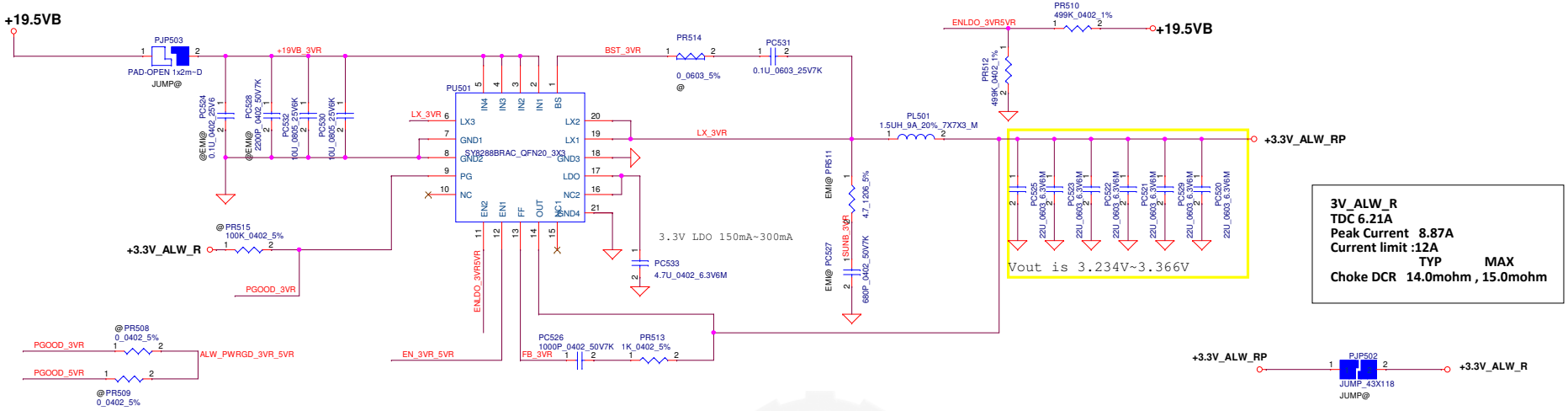
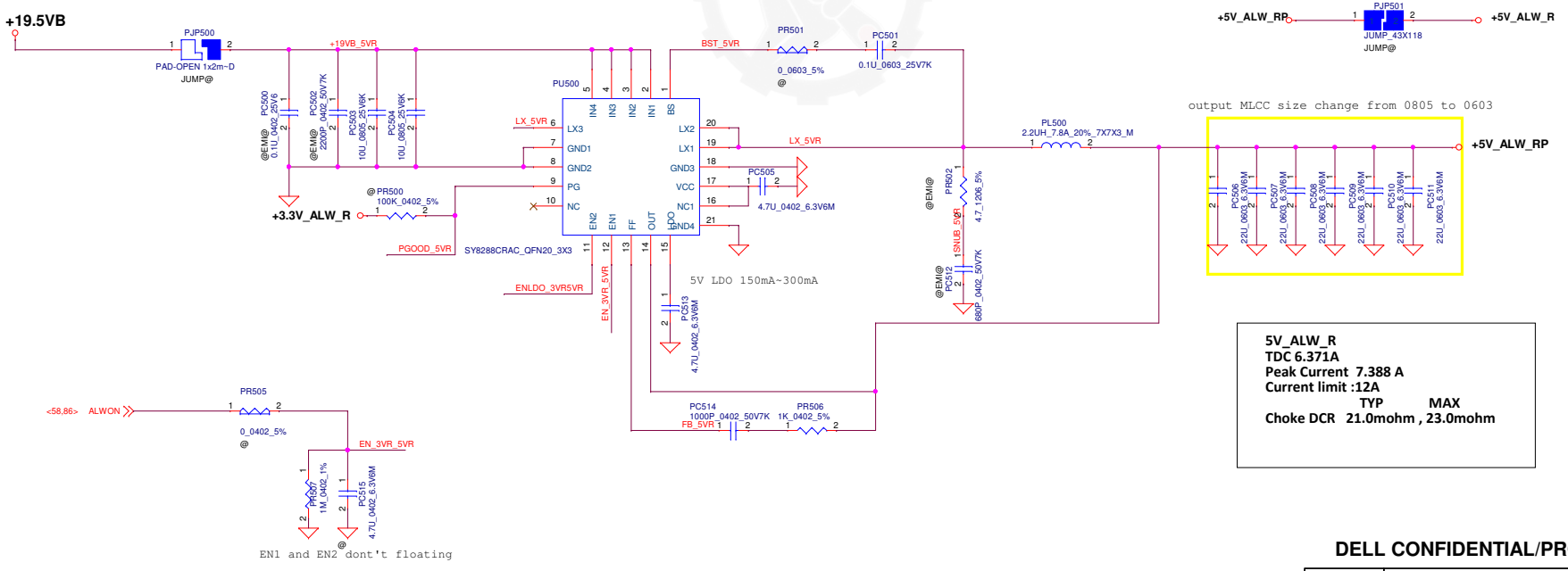
| Title | 5V_ALW/3V_ALW |
| Size | Document Number: LA-H271P |
| Rev | 1.0 |
| Date: | Tuesday, April 09, 2019 |
| Sheet | 86 of 103 |

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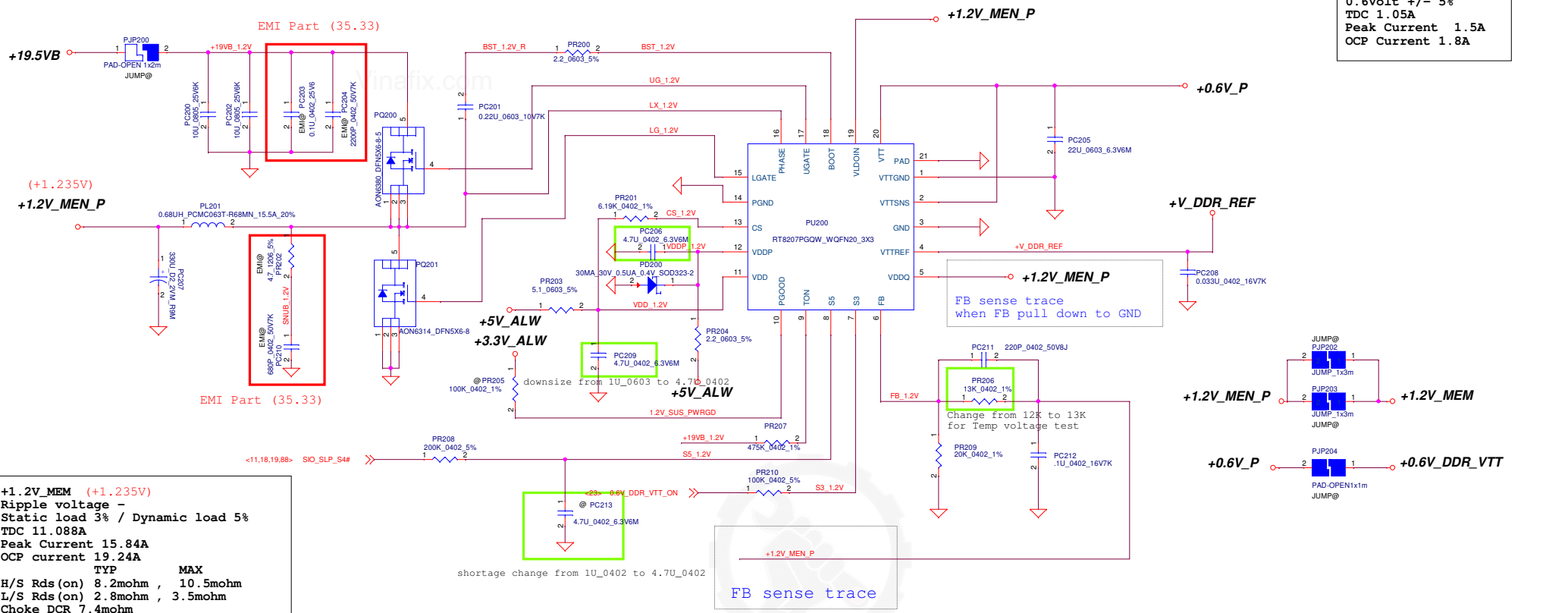
| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | 5V_ALW_R/3V_ALW_R |
| Size | Document Number: LA-H271P |
| Rev | 1.0 |
| Date: | Tuesday, April 09, 2019 |
| Sheet | 87 of 103 |



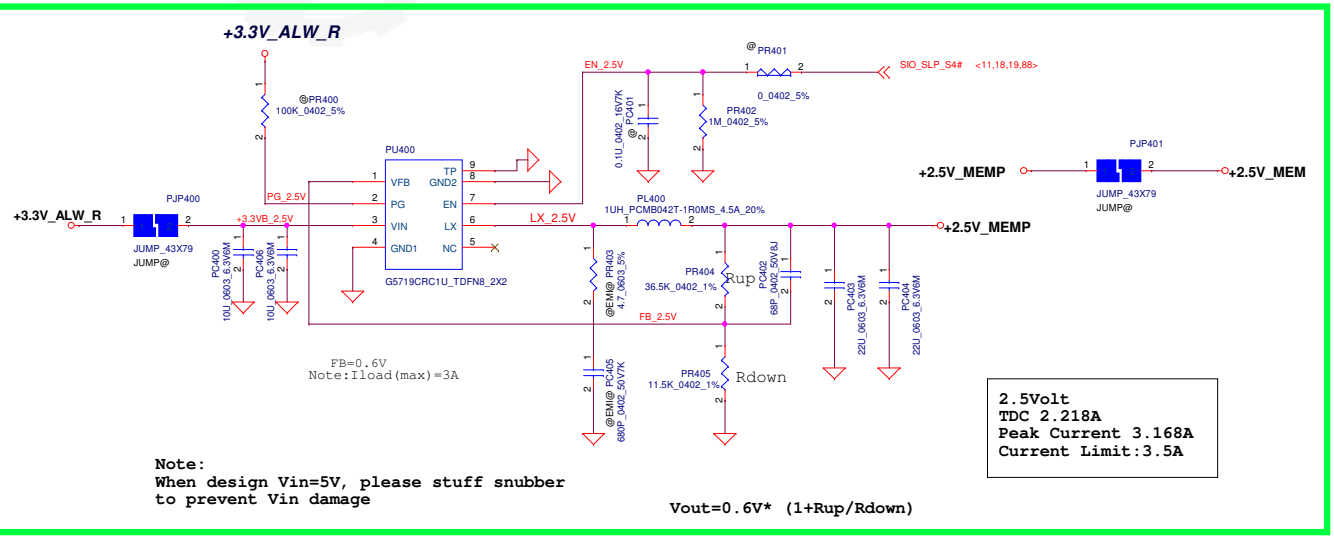

0.6Volt +/- 5%
TDC 1.05A
Peak Current 1.5A
OCP Current 1.8A

**+1.2V_MEM (+1.235V)**
**Ripple voltage –**
**Static load 3% / Dynamic load 5%**
**TDC 11.088A**
**Peak Current 15.84A**
**OCP current 19.24A**

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | 8.2mohm , | 10.5mohm |
| L/S Rds(on) | 2.8mohm , | 3.5mohm |

**Choke DCR 7.4mohm**
**Bulk cap ESR 9mohm**
**Switching Frequency: 533kHz**

| Mode | S3 | S5 | +1.2V_MEN | +V_DDR_REF | +0.6V_P |
|---|---|---|---|---|---|
| S5 | L | L | off | off | off |
| S3 | L | H | on | on | off(Hi-Z) |
| S0 | H | H | on | on | on |




**Note:**
**When design Vin=5V, please stuff snubber to prevent Vin damage**

Vout=0.6V* (1+Rup/Rdown)

2.5Volt
TDC 2.218A
Peak Current 3.168A
Current Limit:3.5A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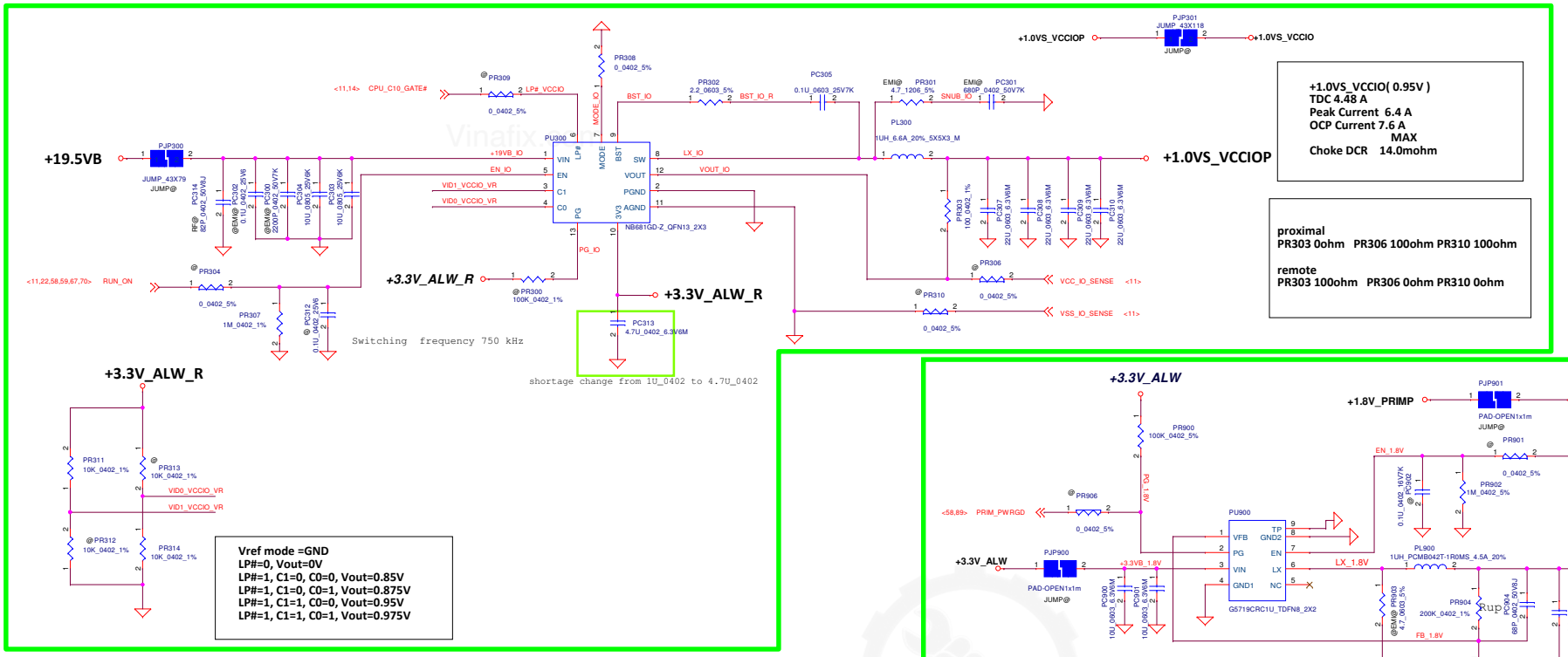
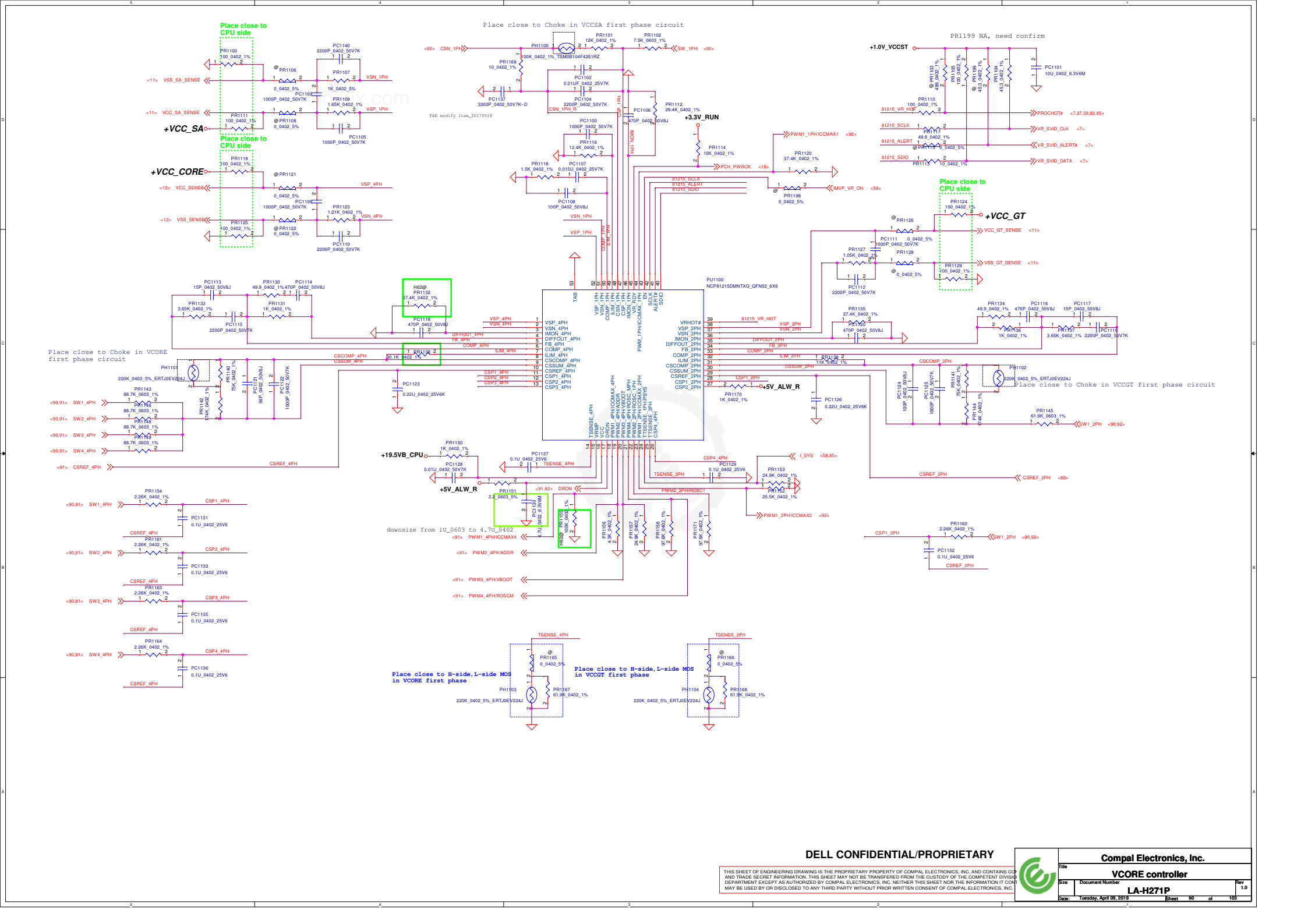
| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | 1.2VP/0.6V/2.5V |
| Size | Document Number: LA-H271P |
| Rev | 1.0 |
| Date: | Tuesday, April 09, 2019 |
| Sheet | 88 of 103 |




| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | VCC_IO/1.8V/1.0VPRIM |
| Size | Document Number: LA-H271P |
| Rev | 1.0 |
| Date: | Tuesday, April 09, 2019 |
| Sheet | 89 of 103 |


Place close to CPU side
Place close to Choke in VCCSA first phase circuit
PR1199 NA, need confirm
+VCC_SA
+VCC_CORE
+VCC_GT
+3.3V_RUN
+1.0V_VCCST
+19.5VB_CPU
+5V_ALW_R
PU1100
NCP81215DMNTXG_QFN52_6X6
Place close to Choke in VCORE first phase circuit
Place close to Choke in VCCGT first phase circuit
downsize from 1U_0603 to 4.7U_0402
Place close to H-side,L-side MOS in VCORE first phase
Place close to H-side,L-side MOS in VCCGT first phase
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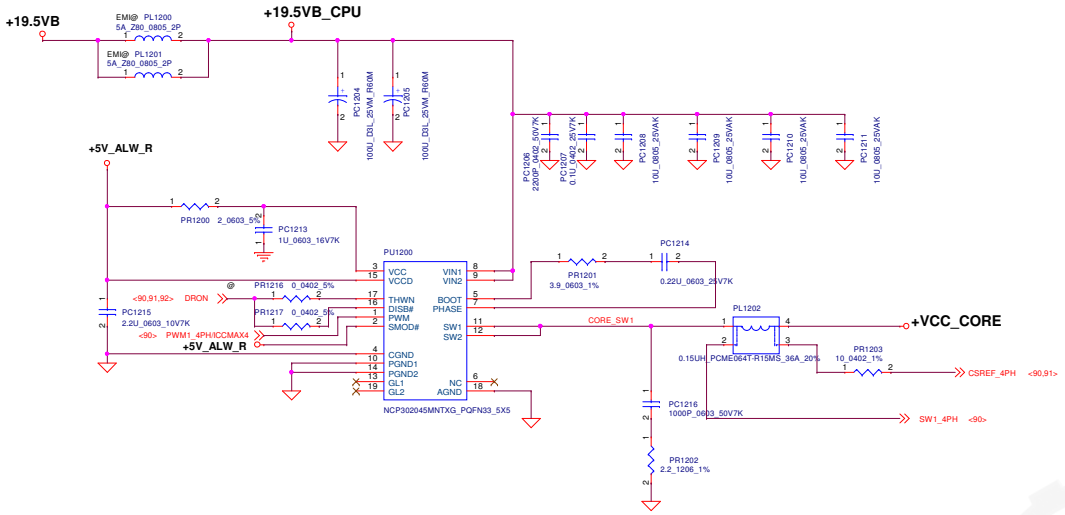
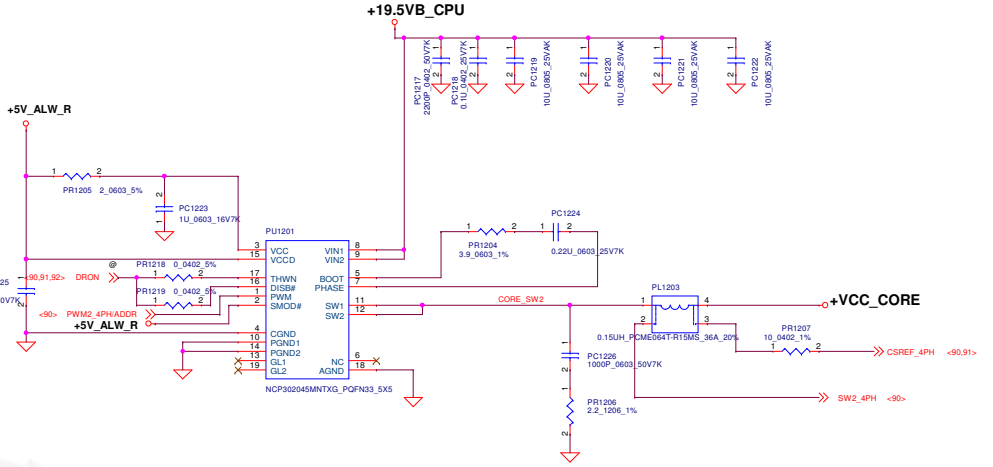
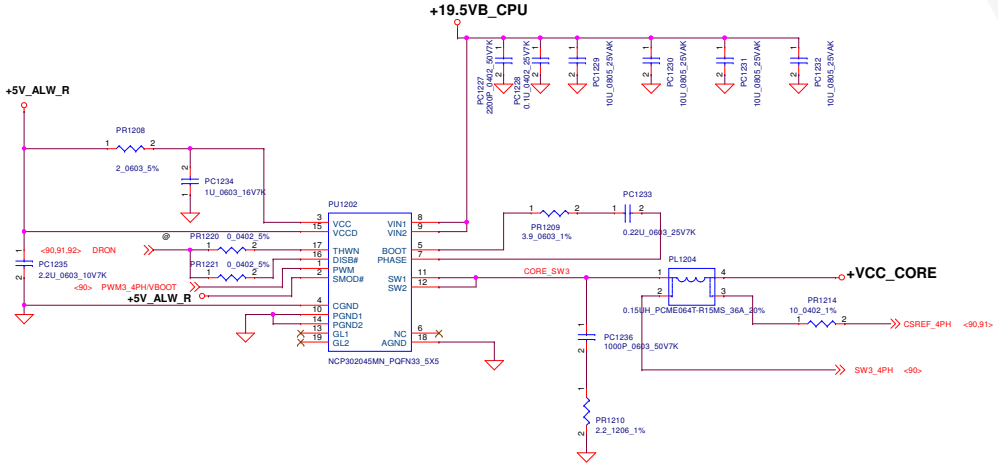
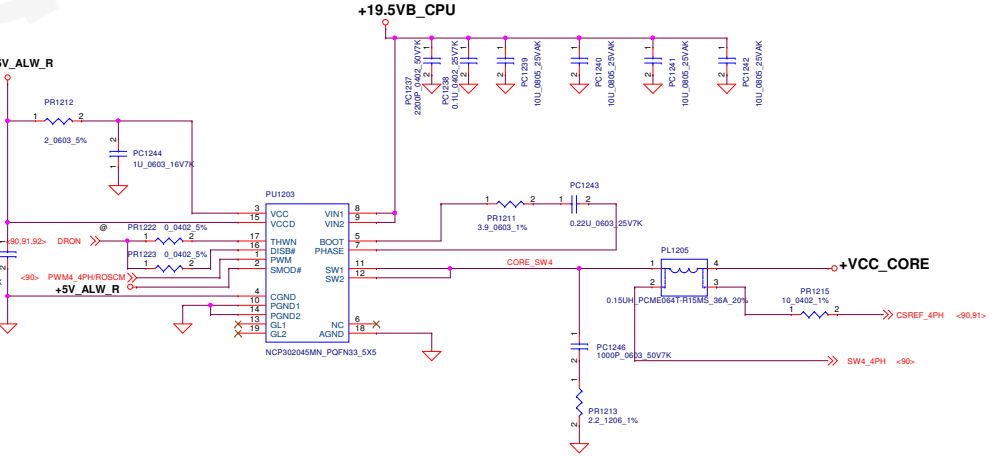
VCORE controller
LA-H271P
Tuesday, April 09, 2019

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/01/06 | Deciphered Date | 2017/01/06 |

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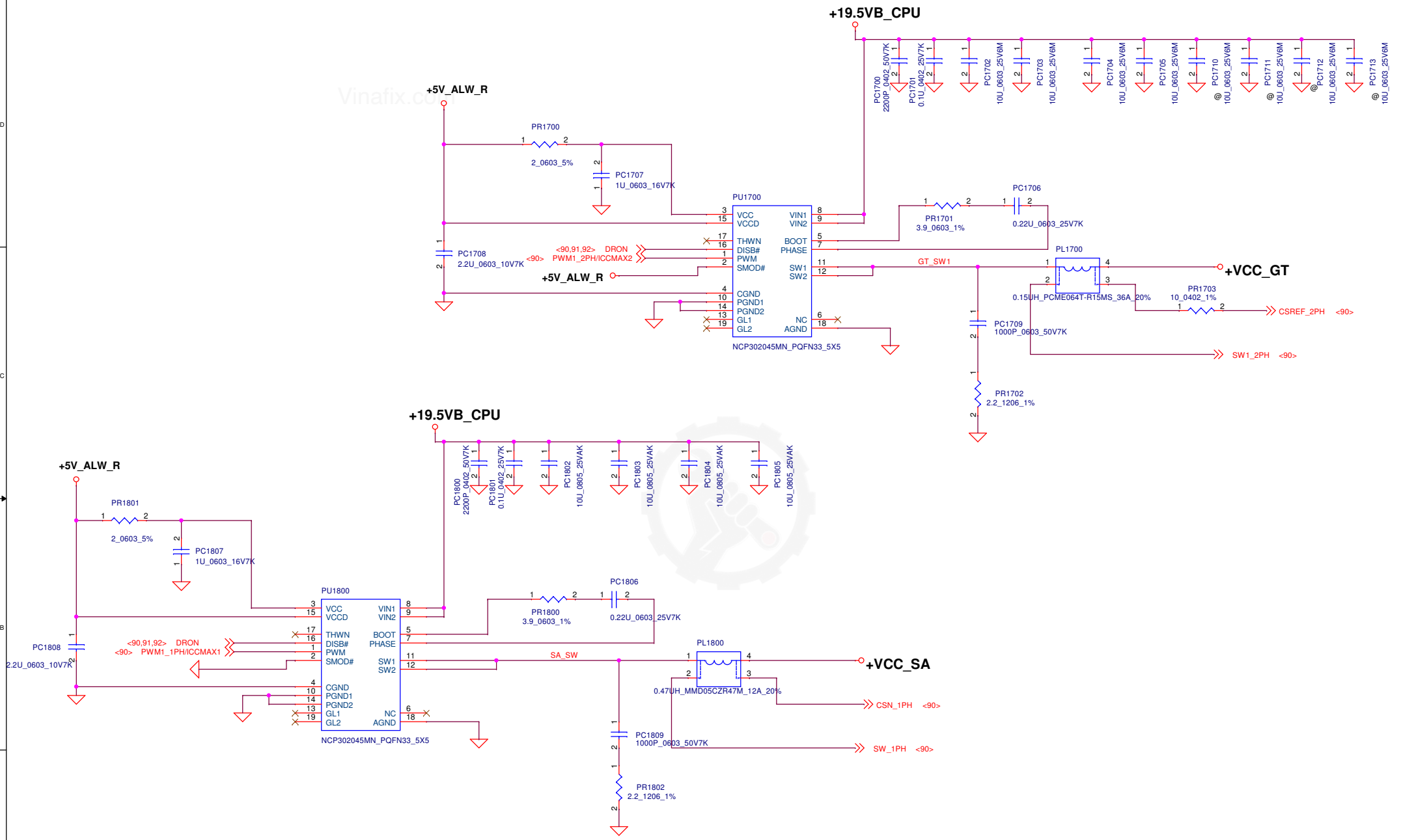
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | +VCC_CORE | | |
| Size | Document Number | LA-H271P | Rev 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 91 of 103 | | |

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| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/01/06 | Deciphered Date | 2017/01/06 |

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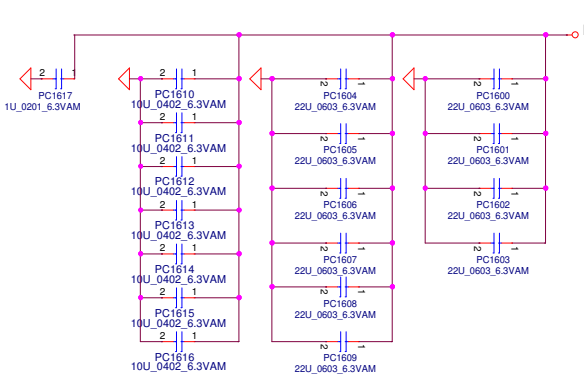
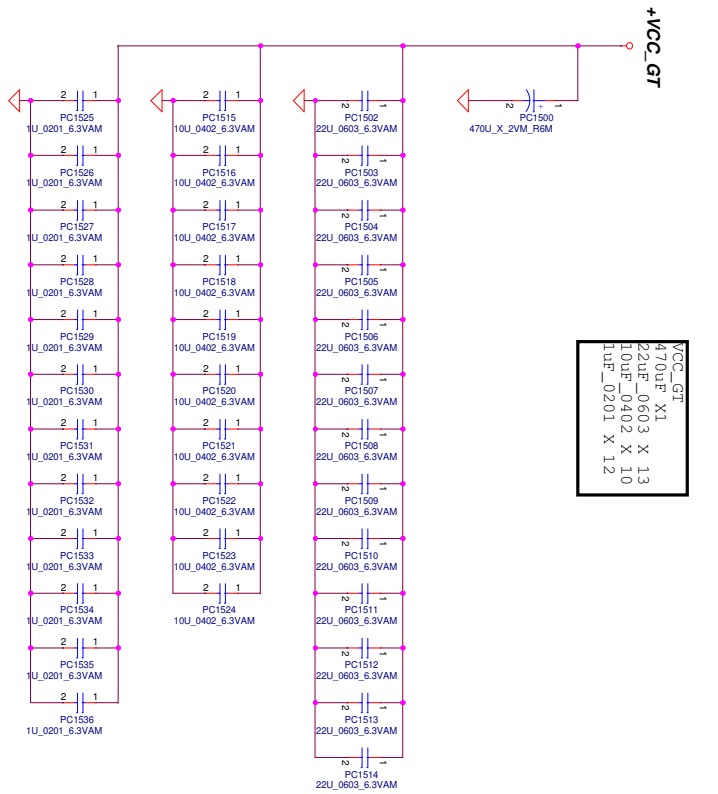
| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | +VCC_GT/+VCC_SA |
| Size | Document Number: LA-H271P |
| Rev | 1.0 |
| Date: | Tuesday, April 09, 2019 |
| Sheet | 92 of 103 |


| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: CPU_DECOUPLING | | | |
| Size: | Document Number: LA-H271P | | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet: 63 | of: | 103 |

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| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: BOM option component | | |
| Size | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 94 of 103 | |

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| | | |
|---|---|---|
| | Compal Electronics, Inc. | |
| | Title: Reserve | |
| Size | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 95 of 103 | |

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| | Title: Reserve | |
| Size | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 96 of 103 | |

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| | Title: Reserve | |
| Size | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 97 of 103 | |

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| | Title: Reserve | |
| Size | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 98 of 103 | |

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| Title: Reserve | | |
| Size | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 99 of 103 | |

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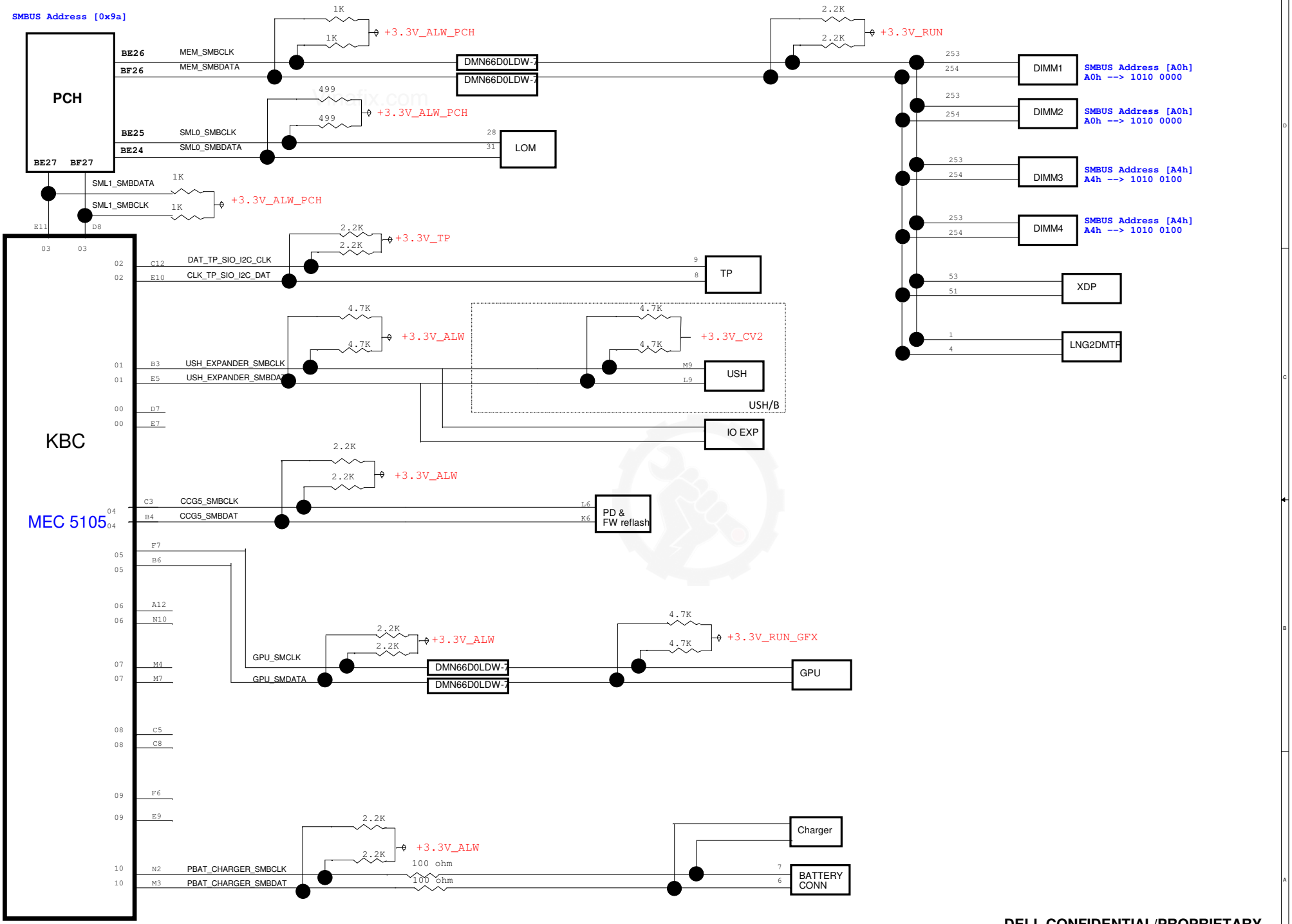
|---|---|---|
| | Compal Electronics, Inc. | |
| | Title: Reserve | |
| Size | Document Number: LA-H271P | Rev: 1.0 |
| Date: Tuesday, April 09, 2019 | Sheet 100 of 103 | |

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| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | SMBUS Block |
| Size | Document Number: LA-H281P |
| Rev | 1.0 |
| Date: | Tuesday, April 09, 2019 |
| Sheet | 101 of 103 |

# Version Change List ( P. I. R. List )



| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|---|---|---|---|---|---|---|---|
| 1 | 82 | POWER | 11/30 | COMPAL | AC_DIS pull high when AC plug in to make system can't boot | Add pull down resister PR2163 to solve | 0.2(X01) |
| 2 | 86 87 88 | POWER | 11/30 | COMPAL | MLCC downsize for shortage issue | PC205 change from SE000001120 to SE00000M000<br>PC109/PC126/PC527/PC512/PC210 change from SE025681K80 to SE074681K80 | 0.2(X01) |
| 3 | 91 | POWER | 4/1 | COMPAL | NCP302155 change to NCP302045 for all type CPU due to UIS package test | PU1200/PU1201/PU1202/PU1203 for H82 change from SA0000C8M00 to SA0000AOI00 | 1.0(A00) |
| 4 | 82 | POWER | 4/8 | COMPAL | For EMI test, need to add MLCC on +19VB path | add PC2103 SE00000G880 0.1U_0402_25V6 | 1.0(A00) |
| 5 | | POWER | | COMPAL | | | |
| 6 | | POWER | | COMPAL | | | |
| 7 | | POWER | | COMPAL | | | |
| 8 | | POWER | | COMPAL | | | |
| 9 | | POWER | | COMPAL | | | |
| 10 | | POWER | | COMPAL | | | |
| 11 | | POWER | | COMPAL | | | |
| 12 | | POWER | | COMPAL | | | |
| 13 | | POWER | | COMPAL | | | |
| 14 | | POWER | | COMPAL | | | |
| 15 | | POWER | | COMPAL | | | |

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Version Change List ( P. I. R. List )

| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|---|---|---|---|---|---|---|---|
| 1 | 56 | EE | 2018/10/2 | Compal | Fix CA232 no function | CA29 and CA232 are parallel, and connector to UA1.23 | 0.2(X01) |
| 2 | 10 | EE | 2018/10/2 | Compal | FOLLOW PDG V1P8 P.616 downsize from 0603 to 0402 | CC185 change to 0402 | 0.2(X01) |
| 3 | 44 | EE | 2018/10/2 | Compal | FRS_ON_P1 and FRS_ON_P2 have a spike to turn on 5V VBUS when CCG5 get power. | RT617,RT618 change to pop | 0.2(X01) |
| 4 | 43 | EE | 2018/10/12 | Compal | Correct downsize error | RT542,RT547 change footprint from 0402 to 0805 | 0.2(X01) |
| 5 | 31 | EE | 2018/10/12 | Compal | PS8461QFN66GTR-A0 change to A4 | UV66,UV67 | 0.2(X01) |
| 6 | 58 | EE | 2018/10/12 | Compal | MEC5105 change CPN to SA00009GL30 | UE1 | 0.2(X01) |
| 7 | 18,38,52,58 | EE | 2018/10/12 | Compal | Change CPN from SB00000ZU00 to SB00000PV00 | QE2,QH4,QV23,QZ17,QZ18 | 0.2(X01) |
| 8 | 77 | EE | 2018/10/12 | Compal | Correct error | H20,H23 Change to NPTH | 0.2(X01) |
| 9 | 42 | EE | 2018/11/27 | Compal | Place holder for future VBUS-short fix (reduce current surge) (align Northbay) | Reserve RT621,RT622 0 ohm | 0.2(X01) |
| 10 | 21 | EE | 2018/11/27 | Compal | Align Northbay pop LH423,CH560,CH324 | RH289 change LH423, CH324 change to pop, Add CH560 | 0.2(X01) |
| 11 | 42 | EE | 2018/11/27 | Compal | TypeC CONN1,2 0 ohm change to 2.2ohm Align BH | RT594~RT601, RT623~RT630 | 0.2(X01) |
| 12 | 42 | EE | 2018/11/27 | Compal | TypeC CONN1,2 Add 0.33u Align BH | CT390~CT397 | 0.2(X01) |
| 13 | 42 | EE | 208/11/27 | Compal | Add SSTX/SSRX resistors Align BH | RT633~RT640 | 0.2(X01) |
| 14 | 62 | EE | 208/11/27 | Compal | Update JKBTP1,JLED1,JPB1 symbol | JKBTP1,JLED1,JPB1 | 0.2(X01) |
| 15 | 10 | EE | 208/11/30 | Compal | Change LC562 from 0_0603_5% to Beads Align BH | RC422 change to LC562 | 0.2(X01) |
| 16 | 42 | EE | 2018/12/5 | Compal | Support vpro on docking side reserve | Add RT641,RT642 | 0.2(X01) |
| 17 | 58,59 | EE | 2018/12/7 | Compal | Correct RTD3_SELECT to right GPIO | Change RTD3_SELECT from UE1.E4 to UE12.21.Add RE750 to UE1.E4. UE1.E4 no use. | 0.2(X01) |
| 18 | 38,59 | EE | 2018/12/7 | Compal | Reserve GPIO pins for DID2.0 feature | Add Net "DID2_GPIO1,DID2_GPIO2" | 0.2(X01) |
| 19 | 65 | EE | 2019/1/15 | Compal | TPM ES Chip change to MP(QS) part(UZ12) | Change to SA0000AQ270 | 0.2(X01) |
| 20 | 77 | EE | 2019/1/15 | Compal | CLIP1,CLIP2 | Change to @RF@ | 0.2(X01) |
| 21 | 62 | EE | 2019/1/15 | Compal | Board ID | Change to 62Kohm | 0.2(X01) |
| | 58 | EE | 2019/1/15 | Compal | TBT_RESET_N_EC (RE506) | Change to pop | 0.2(X01) |
| 22 | 16 | EE | 2019/1/15 | Compal | Crystal EA change to 18PF (CH4,CH5) | Change to SE071180J80 | 0.2(X01) |
| 23 | 45 | EE | 2019/1/15 | Compal | SE00001M700 change to SE00000Y300 | CT95,CT96,CT97,CT98,CT359,CT360,CT356,CT366 | 0.2(X01) |
| 24 | 59,22,20,58,38,22,38 | EE | 2019/1/15 | Compal | Before DVT1.0,PPM feedback material shortage(RD check ok for install material)<br>SB000002R00 change to SB000013V00<br>SB00000J500 change to SB000010O00<br>SB00000QP00 change to SB00000T900<br>SB000010C00 change to SB000008S80 | QE4, QZ20, QH7, QE15, QV8, QZ1 QV1 | 0.2(X01) |
| 25 | 51 | EE | 2019/1/15 | Compal | LAN IEEE EA change to 0ohm (RL71~RL78) | Change to SD028000080 | 0.2(X01) |
| 26 | 44 | EE | 2019/1/15 | Compal | TYPE C AUX change to 0ohm (CT385~CT388) | Change to SD043000080 | 0.2(X01) |
| 27 | 59 | EE | 2019/1/15 | Compal | UE12 USE DVT1.0 CPN : SA00009YF10 and apply new symbol | Change to SA00009YF10 | 0.2(X01) |
| 29 | 56 | EE | 2019/1/21 | Compal | Change BOM Structure to EMI@ | CA224 CA225 | 0.2(X01) |
| 30 | 59 | EE | 2019/1/18 | Compal | Board ID(DVT1.1) (RE79) | Change to 33Kohm | 0.3(X02) |
| 31 | 38 | EE | 2019/1/18 | Compal | Fuse change to one time used (FV1) | T0603FF1000TM (15") | 0.3(X02) |
| 32 | 38 | EE | 2019/1/21 | Compal | BL_PWR_SRC & LCDVDD monitor | RV907 change to 4.3M, RV908 change to 1.2M | 0.3(X02) |
| 33 | 38 | EE | 2019/1/21 | Compal | Align NB reserve fuse FZ3, FZ4 and netname | Change to T0603FF1000TM | 0.3(X02) |
| 34 | 19 | EE | 2019/1/21 | Compal | Align BH GPIO TYPEC_CON_SEL1 / TYPEC_CON_SEL2 | RH553~RH556 | 0.3(X02) |
| 35 | 38 | EE | 2019/1/24 | Compal | Add RV911 for pull down float voltage | RV911 | 0.3(X02) |
| 36 | 59 | EE | 2019/1/29 | Compal | Update UE12 symbol | Change to SA00009YF10 | 0.3(X02) |
| 37 | 27,38 | EE | 2019/1/29 | Compal | HDR monitor for AMD/NV/UMA edp output detect | RV737~742, QV44 | 0.3(X02) |
| 38 | 38 | EE | 2019/1/30 | Compal | Change the power rail to +3.3V_RUN | RV739,RV740 | 0.3(X02) |
| 39 | 38 | EE | 2019/1/31 | Compal | Change net name from +CAMERA_VDD_F to +CAMERA_VDD | CZ510, CZ511, CZ512 | 0.3(X02) |
| 40 | 42 | EE | 2019/2/12 | Compal | Change to depop, Change BOM Structure to @ | RT372 | 0.3(X02) |
| 41 | 42 | EE | 2019/2/12 | Compal | Change BOM Structure | RT614 | 0.3(X02) |
| 42 | 27 | EE | 2019/2/21 | Compal | Cancel double pull high | RV806 | 0.3(X02) |

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