Pinehills MLK 13" Schematics
WhiskyLake - U

2019-09-16
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>

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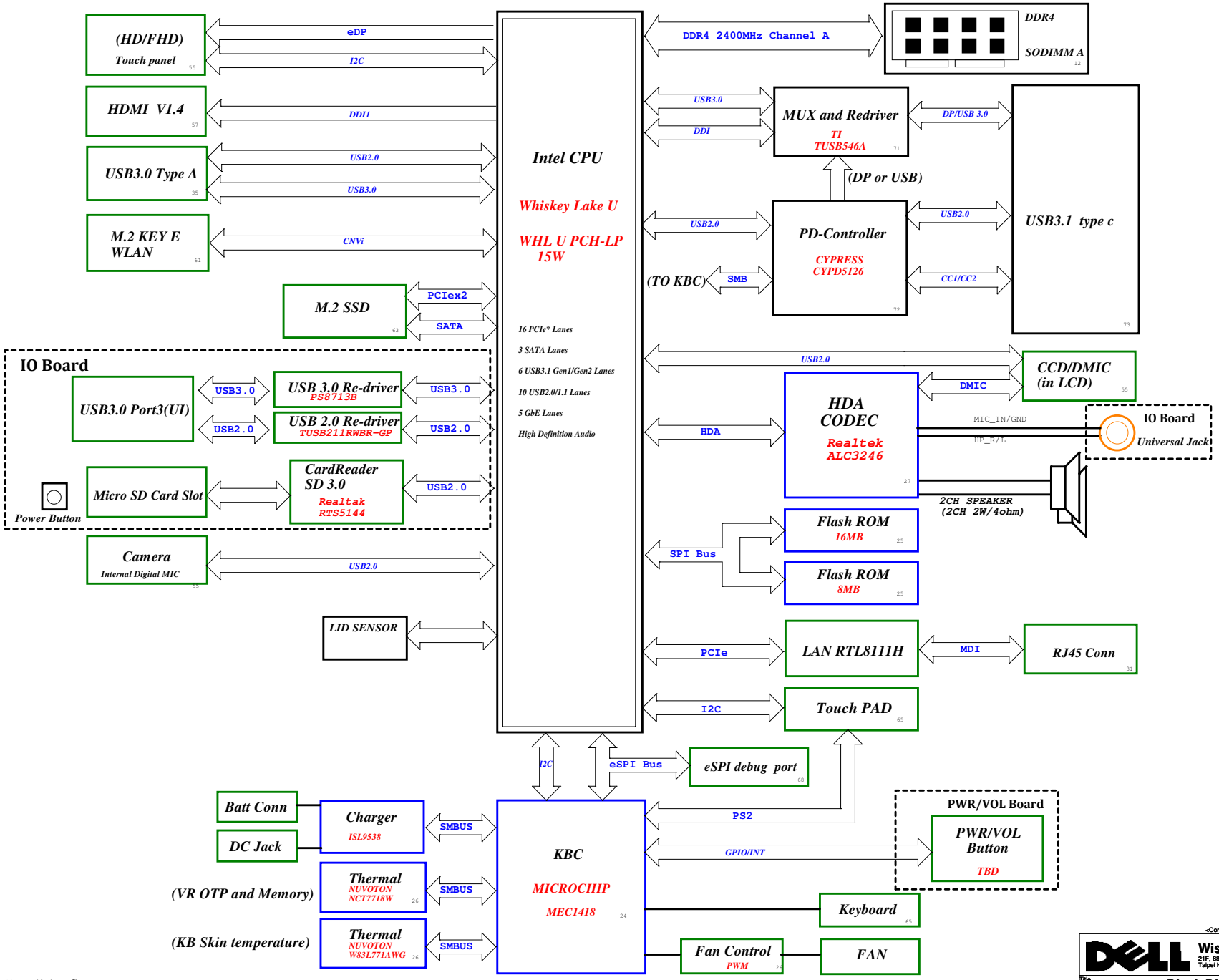
Title: *Cover Page*		
Size: A3	Document Number: Pinehills 13" WHL-U	Rev: X02
Date: Monday, September 23, 2019	Sheet 1 of 106	

Project code: 4PD0J8010001
PCB P/N: TBD
PCB No. : 19717
Revision: A00

Pinehills MLK WHL Block Diagram



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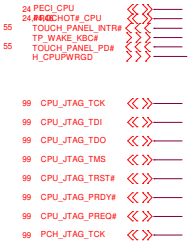
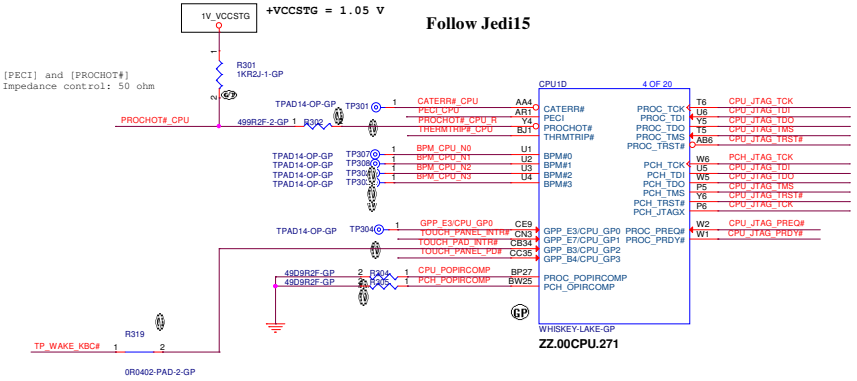
Title: Block Diagram

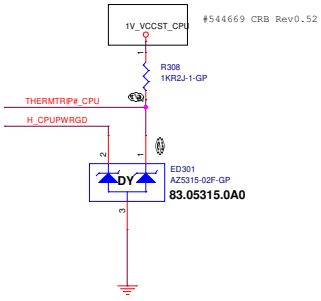
Size	Document Number	Rev
Custom		X02

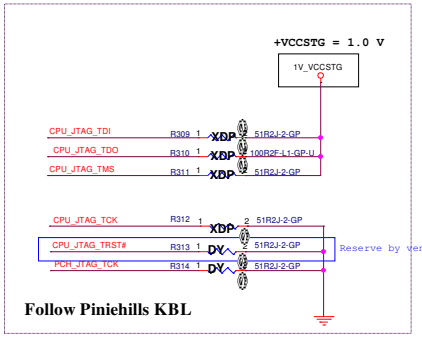
Date: Monday, September 23, 2019 Sheet 2 of 106

Main Func = CPU









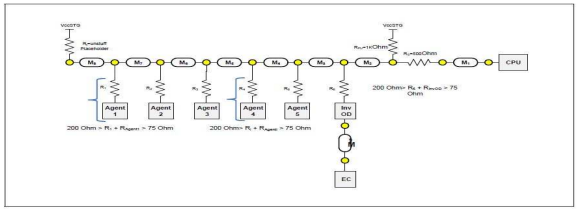


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
Topology Guidelines							
Platform resistors values	Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω						
Platform resistors tolerances	± 5%						

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Size	Document Number	Rev
A2	Pinehills 13" WHL-U	X02

Date: Monday, September 23, 2019 Sheet 3 of 106

Main Func = CPU

DP to HDMI1.4

HDMI_DDI_TX_N0 57
HDMI_DDI_TX_P0 57
HDMI_DDI_TX_N1 57
HDMI_DDI_TX_P1 57
HDMI_DDI_TX_N2 57
HDMI_DDI_TX_P2 57
HDMI_DDI_TX_N3 57
HDMI_DDI_TX_P3 57
CPU_DP1_CTRL_DATA 57
CPU_DP1_CTRL_CLK 57

HDMI_HPD_CPU 57

DP for Type-C Mux

DP2_DDI_TX_N0 71
DP2_DDI_TX_P0 71
DP2_DDI_TX_N1 71
DP2_DDI_TX_P1 71
DP2_DDI_TX_N2 71
DP2_DDI_TX_P2 71
DP2_DDI_TX_N3 71
DP2_DDI_TX_P3 71
71 DP2_AUX_CPU_P
71 DP2_AUX_CPU_N

eDP_TX_CPU_N0 55
eDP_TX_CPU_P0 55
eDP_TX_CPU_N1 55
eDP_TX_CPU_P1 55
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
eDP_HPD_CPU 55
CPU_DP_HPD_R 71,72

L_BKLT_EN 24
L_BKLT_CTRL 55
EDP_VDD_EN 55

GPP_H17_STRAP 15

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

3D3V_S0
RN401 SRN2K2J-1-GP
1 2 4 3 CPU_DP1_CTRL_DATA CPU_DP1_CTRL_CLK
RN402 SRN2K2J-1-GP
2 1 4 3 CPU_DP2_CTRL_DATA CPU_DP2_CTRL_CLK

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	Max = 600 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Follow Jedi15

Port B DP to HDMI 1.4
Port C DP for Type-C Mux

CPU1A 1 OF 20

HDMI_DDI_TX_N0 AL5
HDMI_DDI_TX_P0 AL6
HDMI_DDI_TX_N1 AJ6
HDMI_DDI_TX_P1 AJ5
HDMI_DDI_TX_N2 AF6
HDMI_DDI_TX_P2 AF5
HDMI_DDI_TX_N3 AE5
HDMI_DDI_TX_P3 AE6
DDI1_TXN0
DDI1_TXP0
DDI1_TXN1
DDI1_TXP1
DDI1_TXN2
DDI1_TXP2
DDI1_TXN3
DDI1_TXP3

DP2_DDI_TX_N0 AC4
DP2_DDI_TX_P0 AC3
DP2_DDI_TX_N1 AC1
DP2_DDI_TX_P1 AC2
DP2_DDI_TX_N2 AE4
DP2_DDI_TX_P2 AE3
DP2_DDI_TX_N3 AE1
DP2_DDI_TX_P3 AE2
DDI2_TXN0
DDI2_TXP0
DDI2_TXN1
DDI2_TXP1
DDI2_TXN2
DDI2_TXP2
DDI2_TXN3
DDI2_TXP3

EDP_TXN0 AG4 eDP_TX_CPU_N0
EDP_TXP0 AG3 eDP_TX_CPU_P0
EDP_TXN1 AG2 eDP_TX_CPU_N1
EDP_TXP1 AG1 eDP_TX_CPU_P1
EDP_TXN2 AJ4
EDP_TXP2 AJ3
EDP_TXN3 AJ2
EDP_TXP3 AJ1

EDP_AUX_N AH4 eDP_AUX_CPU_N
EDP_AUX_P AH3 eDP_AUX_CPU_P
DISP_UTILS AM7
DDI1_AUX_N AC7
DDI1_AUX_P AC6
DDI2_AUX_N AD4 DP2_AUX_CPU_N
DDI2_AUX_P AD3 DP2_AUX_CPU_P
DDI3_AUX_N AG7
DDI3_AUX_P AG6

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 HDMI_HPD_CPU
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6 DP1_HPD_CPU_R
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7 SIO_EXT_SMI#
GPP_E16/DPPE_HPD3/DISP_MISC3 CM7 eDP_HPD_CPU
GPP_E17/EDP_HPD/DISP_MISC4

EDP_BKLTEN CK11 L_BKLT_EN
EDP_VDDEN CG11 EDP_VDD_EN
EDP_BKLTCTL CH11 L_BKLT_CTRL

RCOMP SHOULD BE VSS REFERNCE AND SHIELDED
1V_VCCIO
CHECK WHL design guide: DISP_RCOMP
1 R491 24D9R2F-1-GP
eDP_RCOMP_CPU AM6
DISP_RCOMP

CPU_DP1_CTRL_CLK CC8
CPU_DP1_CTRL_DATA CC9
GPP_E18/DDPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DDPB_CTRLDATA
CPU_DP2_CTRL_CLK CH4
CPU_DP2_CTRL_DATA CH3
GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA

TPAD14-OP-GP TP402 1 GPP_E23 CP4 CN4
GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLDATA
GPP_H17_STRAP CR26 CP26
GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLDATA
WHISKEY-LAKE-GP

ZZ.00CPU.271

3D3V_S0
SIO_EXT_SMI# 1 R402 2 10KR2J-3-GP

RTC Gen 9 reset circuit

3D3V_S5_PCH
R406 10KR2J-3-GP
RTC_RST
3D3V_S5_PCH
R405 10KR2J-3-GP
RTC_RST
Q401
DP1_HPD_CPU_R
CPU_DP_HPD_R
CPU_DP_HPD_P
RTC_RST
common part
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
R407 100KR2J-1-GP
RTC_RST

Layout Placement Request
DP1_HPD_CPU_R
R404 0R0402-PAD-2-GP
CPU_DP_HPD_R
DP for Type-C Mux
R403 100KR2J-1-GP

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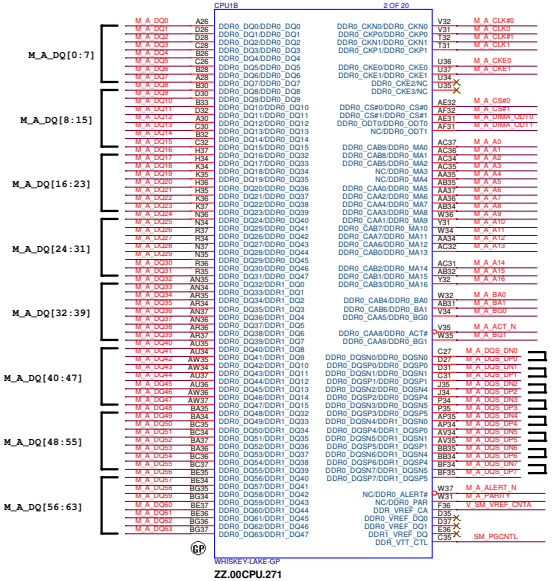
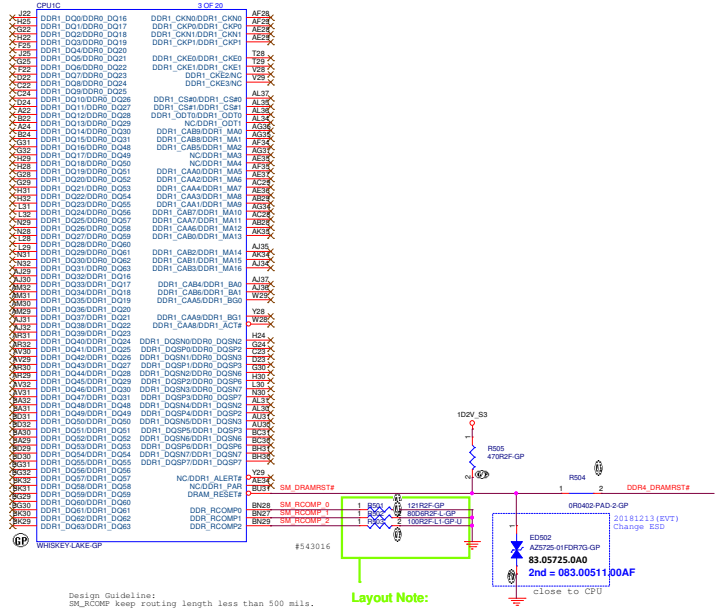
Title: CPU_(JTAG/CPU SIDE BAND)
Size: A2
Document Number: Pinehills 13" WHL-U
Rev: X02
Date: Monday, September 23, 2019 Sheet 4 of 106

Main Func = CPU

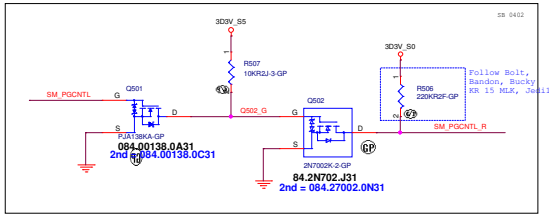
DDR4 ball type: Interleaved Type

Follow KY MLK 15





DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.



PDG: DDR/ODT

4.3 ODT Connectivity

Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

Note:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

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Title: CPU_(DDR)
Size: Custom | Document Number: Pinehills 13" WHL-U | Rev: X02
Date: Monday, September 23, 2019 | Sheet 5 of 106

Main Func = CPU

CFG3 CFG4 15,99 15

ITP_PMODE 99

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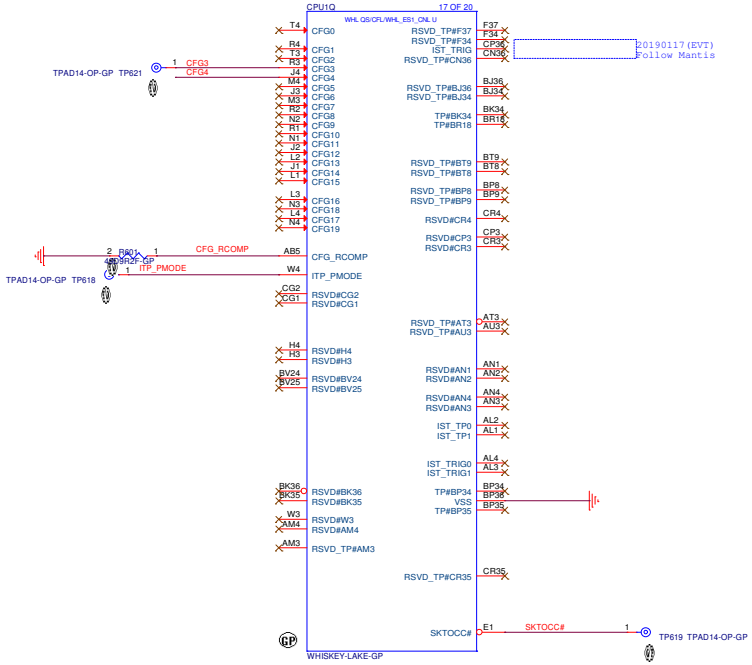

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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Title: CPU_(RESERVED)

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

Date: Monday, September 23, 2019 | Sheet 6 of 106

Main Func = CPU

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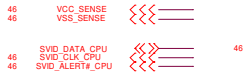

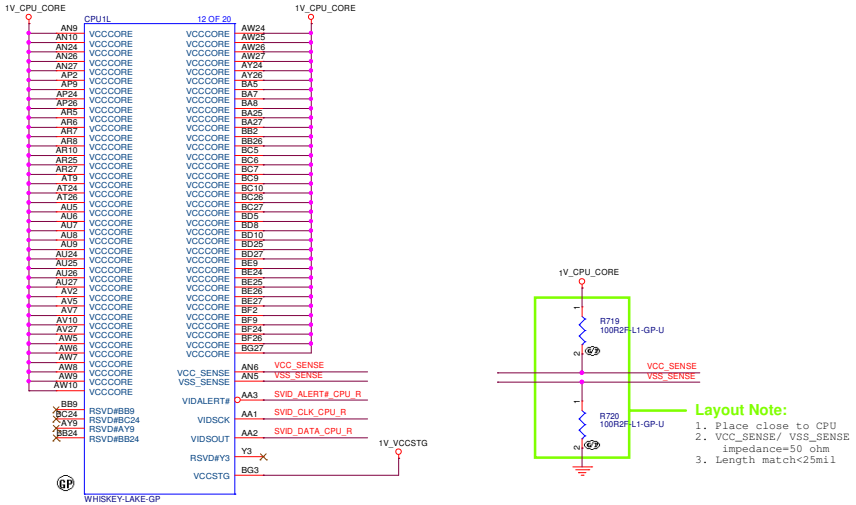

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID_543016:

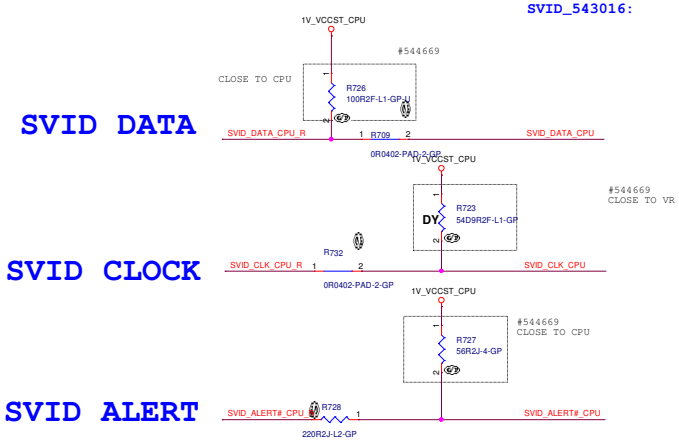

Figure 7-19. Routing Illustration for SVID Topology

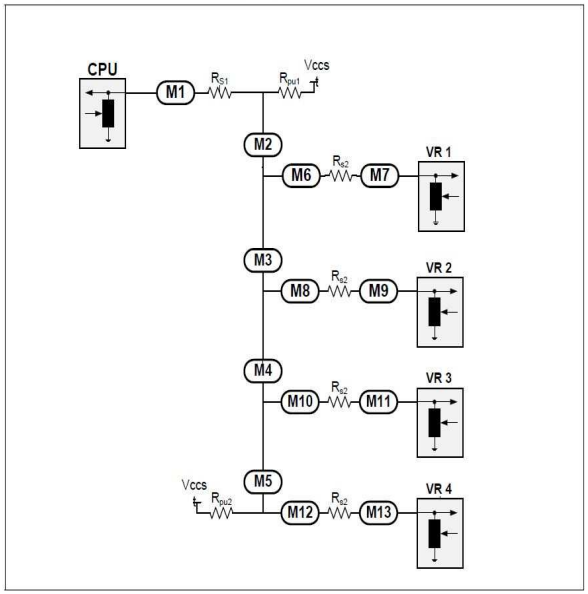

Table 7-18. SVID# Routing Guidelines (Sheet 2 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11
Topology Guidelines							
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#						
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω						
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω						
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω						
Platform resistors tolerances	± 5%						
Route ordering	When routing at minimum spacing route Alert between Data and Clock						
Length Matching Rules							
Length Matching between VIDSOUT and VIDSCK	± 100mils						

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Title: CPU(VCC_CORE)
Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02
Date: Monday, September 23, 2019 | Sheet 7 of 106

Main Func = CPU

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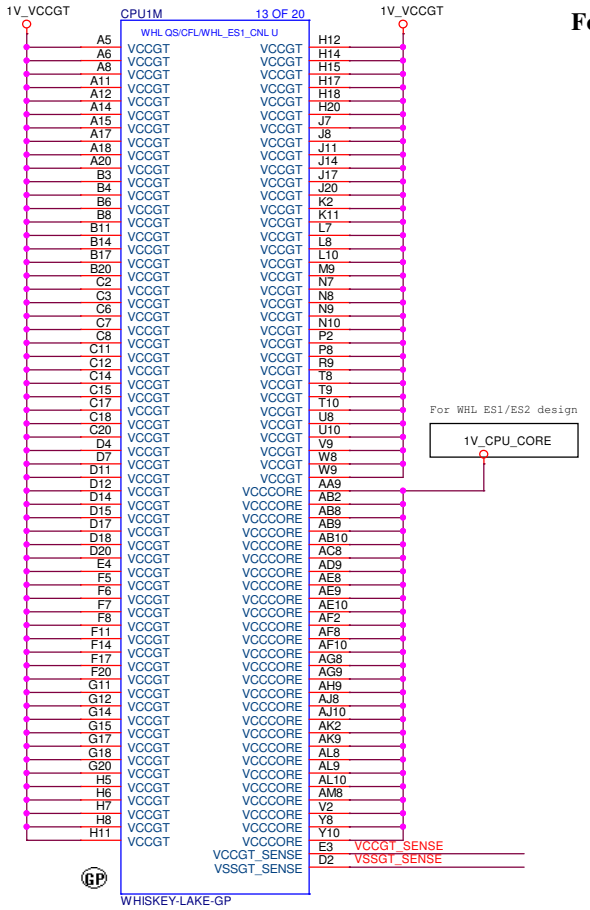
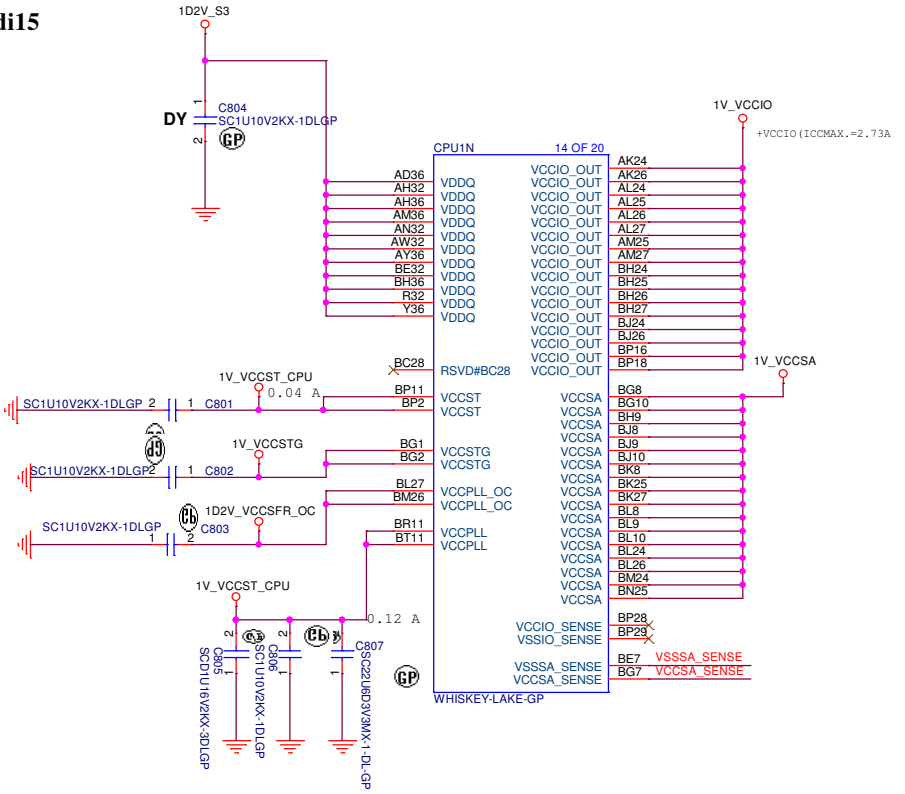
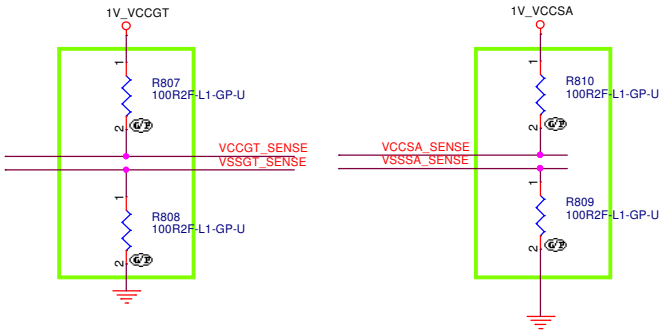
46 VSSSA_SENSE
46 VCCSA_SENSE
46 VCCGT_SENSE
46 VSSGT_SENSE

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE







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Title: CPU (DISPLAY)
Size: A3
Document Number: Pinehills 13" WHL-U
Rev: X02
Date: Monday, September 23, 2019
Sheet 8 of 106

(Blanking)

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Title: *(Reserved)*

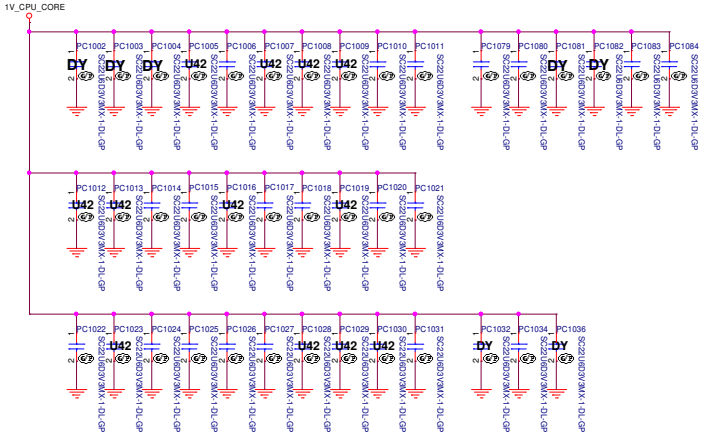
Size: A3 | Document Number: *Pinehills 13" WHL-U* | Rev: *X02*

Date: Monday, September 23, 2019 | Sheet 9 of 106

Main Func = CPU

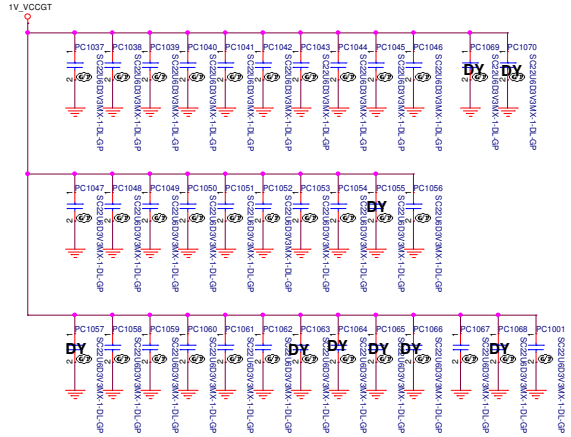
1V_CPU_CORE

22U 0603 x 39 (7DY)



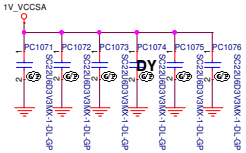
VCCGT

22U 0603 x 35 (13 DY)



VCCSA

22U 0603 x 8 (3DY)



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11.3.1 Whiskey Lake U 4+2 Decoupling Requirement

Table 11-1. Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc_{CORE} Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

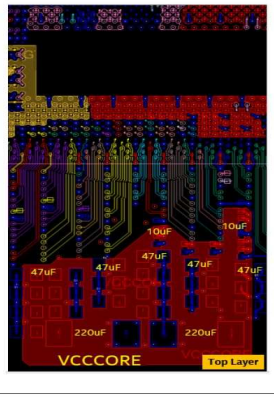
Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{CORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
Vcc_{GT}	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	

Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{SA}		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
Vcc_{IO}	4x 1uF 0201		Place as close to the package as possible
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*
Vcc_{PLL_OC}	1x 1uF 0402		Do not merge Vcc_{PLL}, Vcc_{PLL_OC} and Vcc_{ST} to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
Vcc_{PLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
Vcc_{ST}	1x 1uF 0402		
Vcc_{STG}	1x 1uF 0402		

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps >Power source.

Figure 11-8. Whiskey Lake U 4+2 Vcc_{CORE} Routing Guideline



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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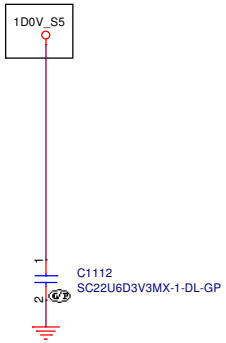
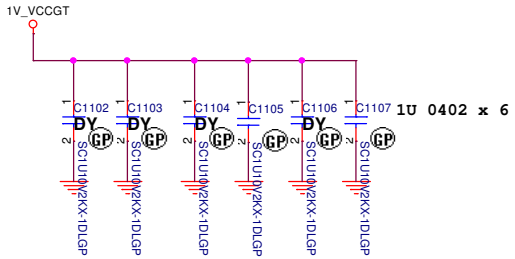
Title: CPU (Power CAP1)
Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02
Date: Monday, September 23, 2019 | Sheet 10 of 106

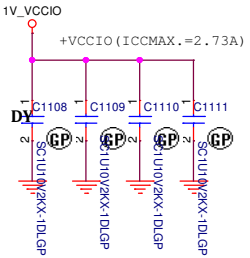
Main Func = CPU

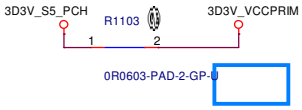
PCH DERIVED RAILS UNSLICED GT VCCIO

Follow R013

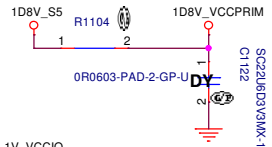


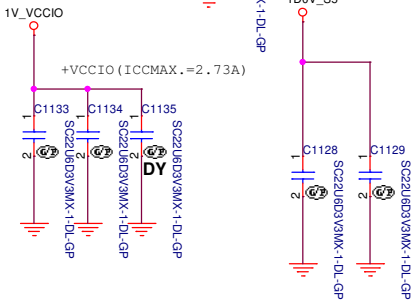


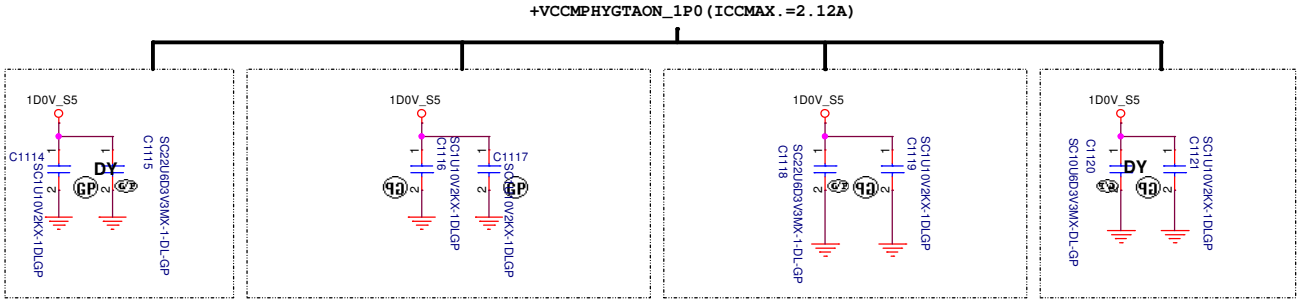




Layout Placement Request

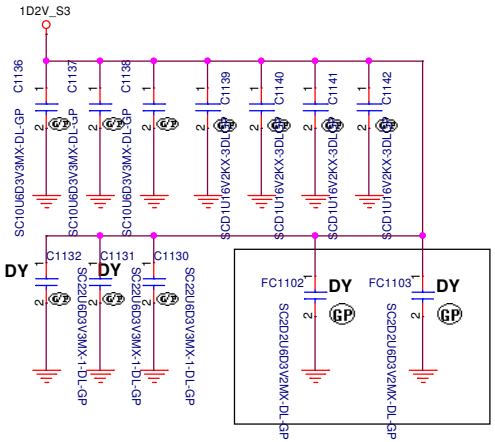






Layout Note:

1uF:
C1114 near N15
C1116 near K15
C1117 near AF20
C1119 near N18
C1121 near AB19
22uF :
C1115 C1118 near N15
10uF:
C1120 near N15



RF request 2016/01/12 modify

U-line 23e 28W
IccMax current-10ms max = 34 A

<Core Design>

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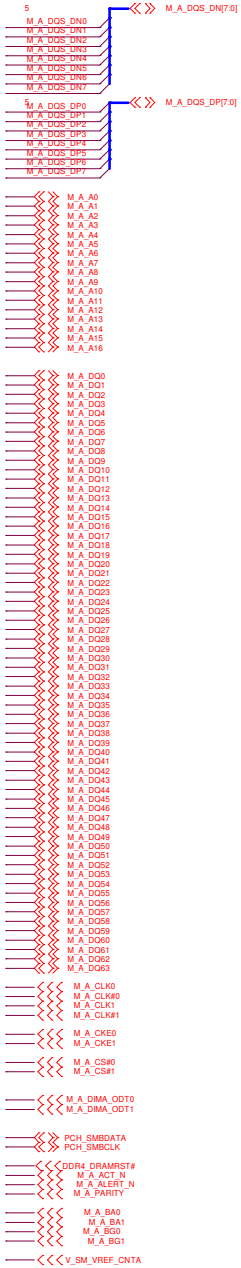
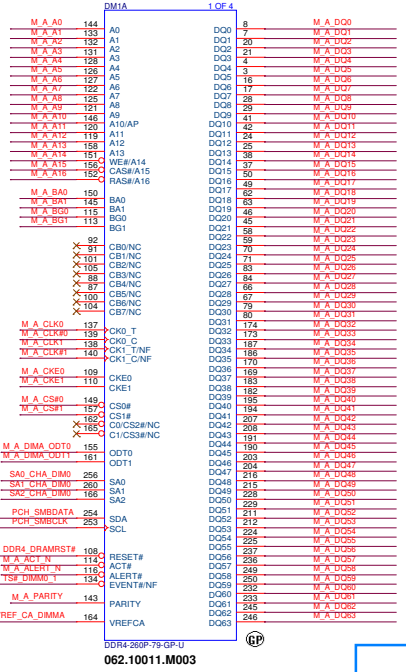
Taipei Hsien 221, Taiwan, R.O.C.

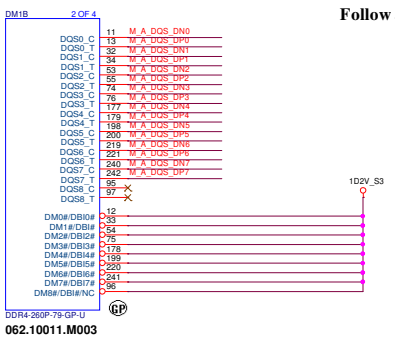
Title: CPU (Power CAP2)
Size: A3
Document Number: Red Hawk 13" WHL-U
Rev: X02
Date: Monday, September 23, 2019
Sheet 11 of 106

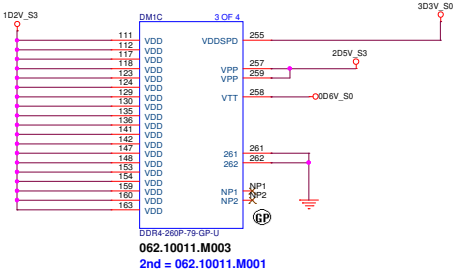
Main Func = MEMORY

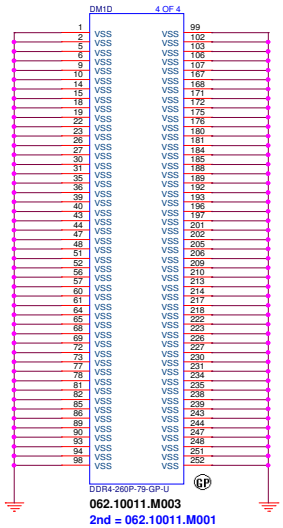
Follow Jedi15

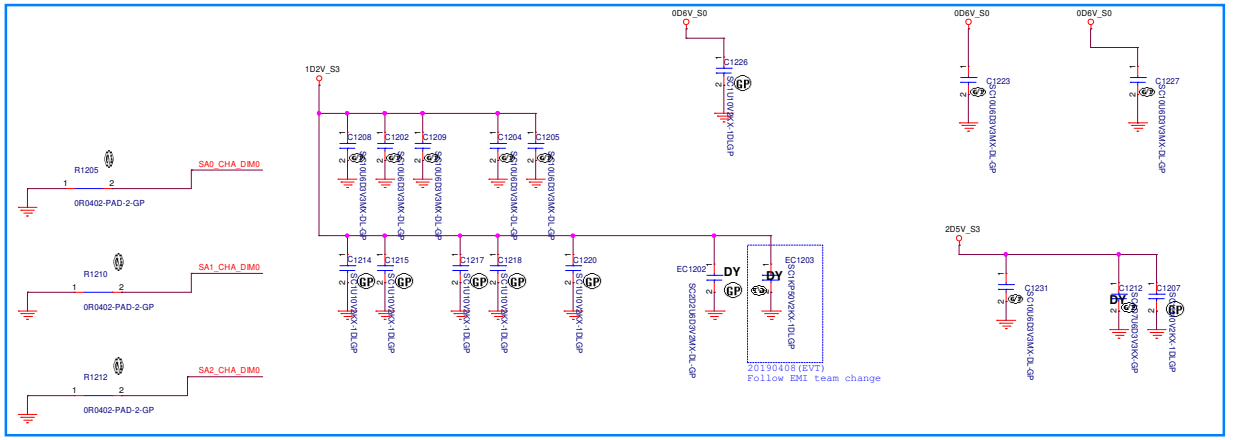




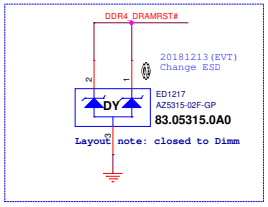


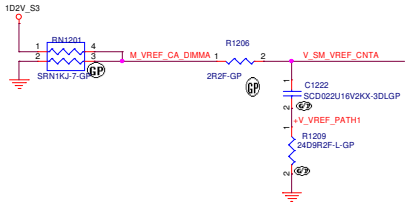






Layout Placement Request





<Core Design>

Wistron Corporation
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Title: DDR3-SODIMM1

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

Date: Monday, September 23, 2019 | Sheet 12 of 106

Main Func = MEMORY

(Blanking)

<Core Design>

Wistron Corporation
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Title

(Reserved)

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

Date: Monday, September 23, 2019 Sheet 13 of 106

(Blanking)

<Core Design>

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Title
(Reserved)_SODIMM _SODIMM4

Size	Document Number	Rev
A4	*Pinehills 13" WHL-U*	*X02*

Date: Monday, September 23, 2019 Sheet 14 of 106

Main Func = PCH

GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 and A17 of all cycles targeting the lower two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit 4). 4. This signal is in the primary well.

GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit 685	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. The combination using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6 — Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected to the PCH and have a SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap will only affect SPI accesses and will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.

SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

Page 4 RN401 2.2K PU 3.3V_S0

GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.

GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

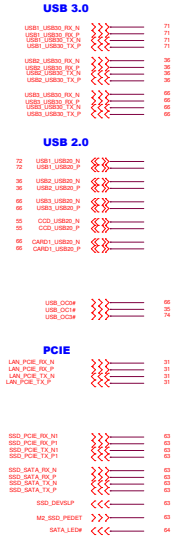
PCH strap pin:

DELL Wistron Corporation

CPU (CS-2/EMMC)

Pinehills 15" WHL-U

Main Func = PCH



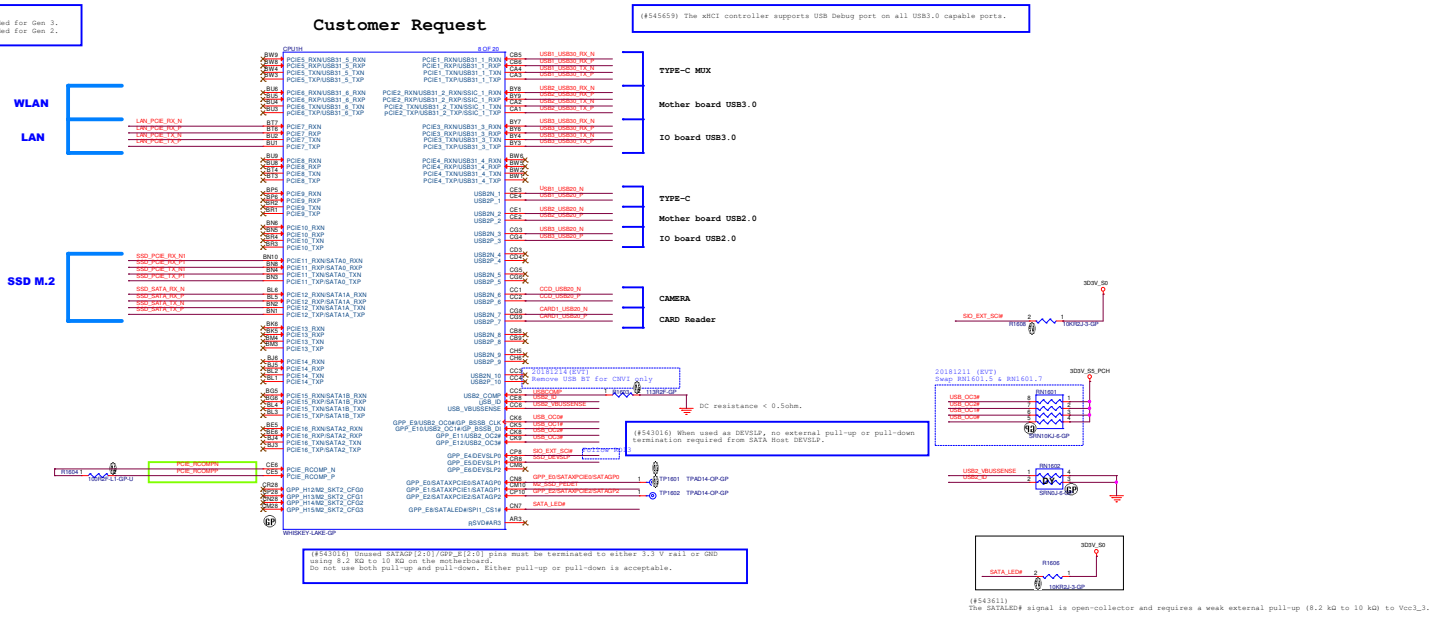
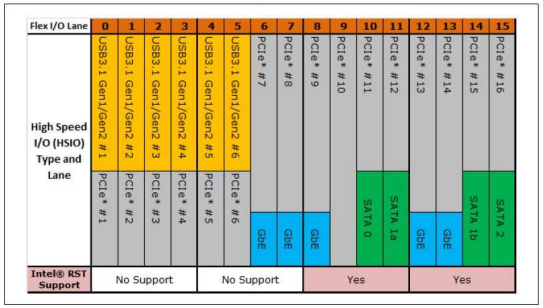


Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP



6.3.1 PCH PCI Express* Interface Configuration Details

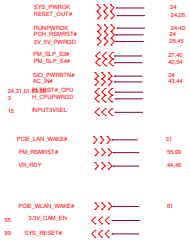
Figure 6-2. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3				PCIe* Controller #4			
										Cycle Router #2				Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9		RP16	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

Table 1-3. PCH HSIO Detail

SKU	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Mainstream/ Base-U	USB 3.1 Gen1	USB 3.1 Gen1	USB 3.1 Gen1	USB 3.1 Gen1	PCIe*	PCIe*	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	SATA 0/ PCIe*	SATA 1A/ PCIe*	GbE 0D/ PCIe*	GbE 0E/ PCIe*	PCIe*	PCIe*
Premium-U	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	PCIe*/ SATA 0	PCIe*/ SATA 1A	GbE 0D/ PCIe*	GbE 0E/ PCIe*	PCIe*/ SATA 1B	PCIe*/ SATA 2
Premium-Y	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	PCIe*/ SATA 0	PCIe*/ SATA 1A	GbE 0D/ PCIe*	GbE 0E/ PCIe*	Not Available	Not Available

Main Func = PCH



Software set GPD0 avoid 屬性BATLOW# PU會漏電

20190408(EVT)
Del R1723

Follow Jedi15

#544669 (CRB): 330k.

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

GPD11 pull high by Intel PDG1.3 request

20190611(DVT1)
Follow Jedi15, Bandon, WASP
20190627(DVT1)
Change back to 10k
20190729 (DVT2)
Follow Bandon

AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us

FOLLOW KEYSTONE 13

75.00056.07D
2nd = 75.00056.I7D

remove R1724 R1735 C1704 EC1710 and +VCCMPHYGTAON_1P0_LS_SIP change to 1D0V_S5.

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

20190424(EVT)
Reverse R1705, R1739 by Dell Andy
20190611(DVT1)
Add D1703

83.R2003.A8M
2nd = 083.52030.008F

VCCST_PWRGD is the same RUNPWROK on KBL.
RUNPWROK align with EC GPIO net name

Dis-wire with XDP_PM_RSMRST_PWRGD_XDP

83.05315.0A0

R1722 & EC1708 modify to 100k and 0.01uF at DVT1

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

75.05125.07D
2ND = 075.00353.0A7D

75.05125.07D
2ND = 075.00353.0A7D

83.R2003.A8M
2ND = 083.52030.008F

75.27002.F7C
2nd = 075.27002.0E7C

Reserve by NON DS3 function 20150413

20181217(EVT)
Follow bandon add PU 100k

BATLOW#:
Pull-up required even if not implemented.

20190408(EVT)
Follow EMI team change

Layout Placement Request

75.00138.0A7C
2nd = 075.00138.0E7C

<Core Design>

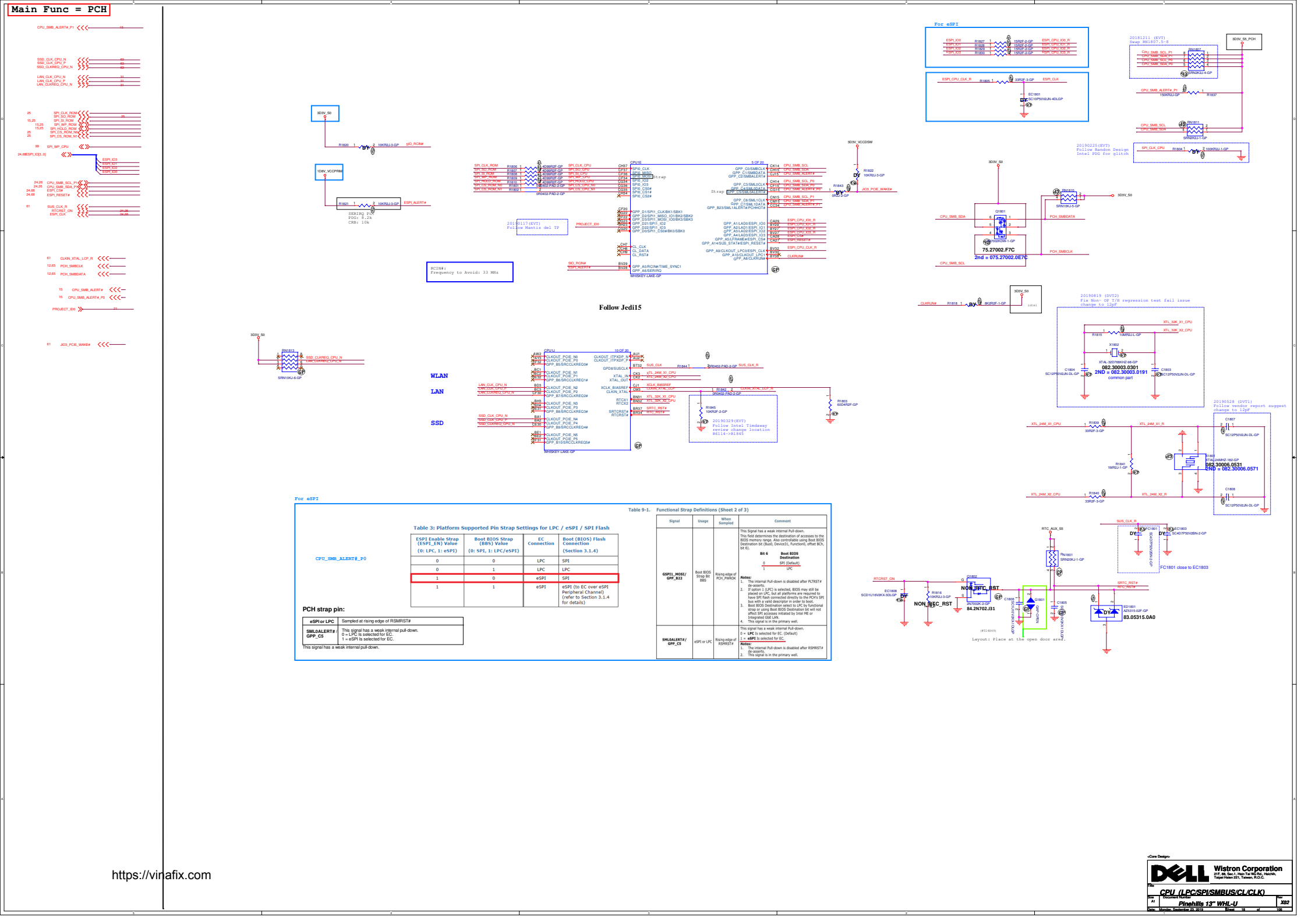
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)

Size: A1 | Document Number: Pinehills 13" WHL-U | Rev: X02

Date: Monday, September 23, 2019 | Sheet 17 of 106

Main Func = PCH



Main Func = PCH

Follow Jedi15

BT_PCMFRM_RSTN
61 BT_PCMOUT_CLKREQ0
55 DMIC_PCH_DATA
55 DMIC_PCH_CLK
15,27 SPKR
27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
68 ME_FWP_SW
27 HDA_SDOUT_CODEC
SD_READ_MODE# 66
HDA_SDOUT_CPU 15

3D3V_S5
R1910 10KR2J-3-GP
TPM_ID
R1911 10KR2J-3-GP

CPU1G 7 OF 20
HDA_SYNC_CPU BN34
HDA_BITCLK_CPU BN37
HDA_SDOUT_CPU BN36
HDA_SDIN0_CPU BN35
BL36
BL35
CK23
BL37
BL34
TPAD14-OP-GP TP1903
HDA_RST_N_CPU
HDA_SYNC/I2S0_SFRM
HDA_BCLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD/SNDW1_DATA
HDA_RST#/I2S1_SCLK/SNDW1_CLK
GPP_D23/I2S_MCLK
I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA
GPP_G0/SD_CMD CH36
GPP_G1/SD_DATA0 CL34
GPP_G2/SD_DATA1 CL33
GPP_G3/SD_DATA2 CM35
GPP_G4/SD_DATA3 CN35
GPP_G5/SD_CD# CH35
GPP_G6/SD_CLK CK36
GPP_G7/SD_WP CK34
SD_READ_MODE# Follow Bandon
WHISKEY-LAKE-GP

intel
BT_PCMFRM_RSTN 1 R1923 33R2J-2-GP
BT_PCMOUT_CLKREQ0 1 R1922 33R2J-2-GP
GPP_H1_SFRM CJ32
GPP_H2_CLKREQ0 CH32
CH29
CH30
GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO

DMIC_PCH_CLK CP24
DMIC_PCH_DATA CN24
TPM_ID CK25
CJ25
SPKR CF35
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_A16/SD_1P8_SEL
GPP_D20/DMIC_DATA0/SNDW4_DATA
SD_1P8_RCOMP
SD_3P3_RCOMP
GPP_D17/DMIC_CLK1/SNDW3_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_B14/SPKR
BW36
BY31
CK33
CM34
SD_RCOMP R1901 1 2.200R2F-L-GP

EMC
EC1901 1 1 SC10P50V2JN-4DLGP HDA_BITCLK_CODEC

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable *

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin: SPKR

TOP SWAP OVERRIDE	
HDA_SPKR	* High = TOP SWAP ENABLED Low = DISABLED (WEAK INTERNAL PD)

The internal pull-up

delete ED1901

HDA_SYNC_CODEC 1 R1908 2 HDA_SYNC_CPU
0R0402-PAD-2-GP

R1920~R1921 need to close for merge prepare

HDA_BITCLK_CODEC R1920 1 0R0402-PAD-2-GP HDA_BITCLK_CPU
HDA_SDOUT_CODEC R1921 1 33R2J-3-GP HDA_SDOUT_CPU
intel
ME_FWP_SW R1909 1 1KR2J-1-GP

HDA_SDOUT_CODEC
EC1903 DY 2 SC33P50V2JN-3DLGP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(AUDIO/SDIO/SDXC)
Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02
Date: Monday, September 23, 2019 | Sheet 19 of 106

Main Func = PCH

55 3.3V_TS_EN
55 CPU_I2C_SDA_P1
55 CPU_I2C_SCL_P1
65 CPU_I2C_SDA_P0
65 CPU_I2C_SCL_P0
55 DBC_PANEL_EN

UART_2_CRXD_DTXD 68
UART_2_CTXD_DRXD 68
SIO_EXT_WAKE# 24
KB_DET# 65

RTC_DET# 15,25

BOARD_ID2 21

61 CNV_BRI_RSP
15,65 CNV_RGI_DT_R
61 CNV_BRI_DT_R
61 CNV_RGI_RSP

51 LCD_CBL_DET#

NRB_BIT 15

GPP_B22_GSPI1_MOSI 15

NB_MODE# 24

LID_CL_SIO# 24,64,69

1D8V_VCCPRIM
R2053 1 DY 2 10KR2J-3-GP PIRQA#

3D3V_S0
51KR2J-1-GP 1 DEBUG 2 R2048 UART_2_CRXD_DTXD
51KR2J-1-GP 1 DEBUG 2 R2049 UART_2_CTXD_DRXD
10KR2J-3-GP 1 DY 2 R2043 DBC_PANEL_EN
10KR2J-3-GP 1 R2045 KB_DET#
100KR2F-L1-GP 1 R2046 IR_CAM_DET#
10KR2J-3-GP 1 R2001 3.3V_TS_EN
10KR2F-2-GP 1 R2054 CPU_I2C_SDA_P1
10KR2F-2-GP 1 R2055 CPU_I2C_SCL_P1
20190612(DVT1)
Add 10k PU for Touch panel

3D3V_S5_PCH
10KR2J-3-GP 1 2 R2041 SIO_EXT_WAKE#

1D8V_S5
SB 0326
R2029 1 DY 2 20KR2J-L2-GP CNV_RGI_RSP
R2030 1 DY 2 20KR2J-L2-GP CNV_BRI_RSP

TPAD
Touch panel

20181214(EVT)
Follow Intel PDG 33 ohm
CNV_RGI_DT_R R2006 1 33R2J-2-GP
CNV_BRI_DT_R R2007 1 33R2J-2-GP

Follow Jedi15

CPU1F
6 OF 20
WHISKEY-LAKE-GP

PIRQA# CC27 GPP_B15/GSPI0_CS0#
CC32 GPP_A7/PIRQA#/GSPI0_CS1#
VRAM_ID1 CE28 GPP_B16/GSPI0_CLK
NRB_BIT CE27 GPP_B17/GSPI0_MISO
CE29 GPP_B18/GSPI0_MOSI
Strap
DBC_PANEL_EN CA31 GPP_B19/GSPI1_CS0#
CA32 GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
3.3V_TS_EN CC29 GPP_B20/GSPI1_CLK
GPP_B22_GSPI1_MOSI CC30 GPP_B21/GSPI1_MISO
CA30 GPP_B22/GSPI1_MOSI
CNV_BRI_RSP CK20 GPP_F5/CNV_BRI_RSP
CNV_RGI_DT CG19 GPP_F6/CNV_RGI_DT
CNV_BRI_DT CJ20 GPP_F4/CNV_BRI_DT
CNV_RGI_RSP CH19 GPP_F7/CNV_RGI_RSP
UART_2_CRXD_DTXD CR12 GPP_C20/UART2_RXD
UART_2_CTXD_DRXD CP12 GPP_C21/UART2_TXD
SIO_EXT_WAKE# CN12 GPP_C22/UART2_RTS#
KB_DET# CM12 GPP_C23/UART2_CTS#
CPU_I2C_SDA_P0 CM11 GPP_C16/I2C0_SDA
CPU_I2C_SCL_P0 CN11 GPP_C17/I2C0_SCL
CPU_I2C_SDA_P1 CK12 GPP_C18/I2C1_SDA
CPU_I2C_SCL_P1 CJ12 GPP_C19/I2C1_SCL
CF27 GPP_H4/I2C2_SDA
CF29 GPP_H5/I2C2_SCL
CH27 GPP_H6/I2C3_SDA
CH28 GPP_H7/I2C3_SCL
CJ30 GPP_H8/I2C4_SDA
CJ31 GPP_H9/I2C4_SCL

GPP_D9/ISH_SPI_CS#/GSPI2_CS0# CN22 IR_CAM_DET#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK CM25 RTC_DET#
GPP_D11/ISH_SPI_MISO/GSPI2_MISO CP22
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI
GPP_D5/ISH_I2C0_SDA CK22
GPP_D6/ISH_I2C0_SCL CH20
GPP_D7/ISH_I2C1_SDA CH22
GPP_D8/ISH_I2C1_SCL CJ22
GPP_H10/I2C5_SDA/ISH_I2C2_SDA CJ27
GPP_H11/I2C5_SCL/ISH_I2C2_SCL CJ29
GPP_D13/ISH_UART0_RXD CM24
GPP_D14/ISH_UART0_TXD CN23 VRAM_ID2
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1# CR24
GPP_D16/ISH_UART0_CTS#/SML0BALERT# CG12 BOARD_ID1
GPP_C12/UART1_RXD/ISH_UART1_RXD CH12 LCD_CBL_DET#
GPP_C13/UART1_TXD/ISH_UART1_TXD CF13
GPP_C14/UART1_RTS#/ISH_UART1_RTS# CG14
GPP_C15/UART1_CTS#/ISH_UART1_CTS# BW35
GPP_A18/ISH_GP0 BW33
GPP_A19/ISH_GP1 CA37
GPP_A20/ISH_GP2 CA36
GPP_A21/ISH_GP3 CA35
GPP_A22/ISH_GP4 CA34
GPP_A23/ISH_GP5 BW32 LID_CL_SIO#
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF#

Layout Placement Request
KBLR:GPP_F10~F11: 1.8V only
CFLU:GPP_H10~H11: ?V
20190226(EVT)
Follow Bandon

SA 1228 intel

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

VRAM_ID[2:1] 11: UMA
01: DIS+4G VRAM
00: DIS+2G VRAM

3D3V_S0 R2038 10KR2J-3-GP UMA VRAM_ID2
3D3V_S0 R2035 10KR2J-3-GP UMA VRAM_ID1

3D3V_S0 R2010 10KR2J-3-GP DY BOARD_ID1
BOARD_ID2 R2008 10KR2J-3-GP CLAM
BOARD_ID1 R2009 10KR2J-3-GP WHL-U

BOARD_DI[2:1]=10 for WHLU

Follow RO 13

20190408(EVT)
Del 2in1 Part in PH MLK

NB_MODE# R2052 10KR2J-3-GP CLAM

3D3V_S0 R2016 100KR2F-L1-GP LCD_CBL_DET#
DY R2017 10KR2J-3-GP
20190605(DVT1)
Follow Bandon 100k

PCH strap pin: NRB_BIT

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

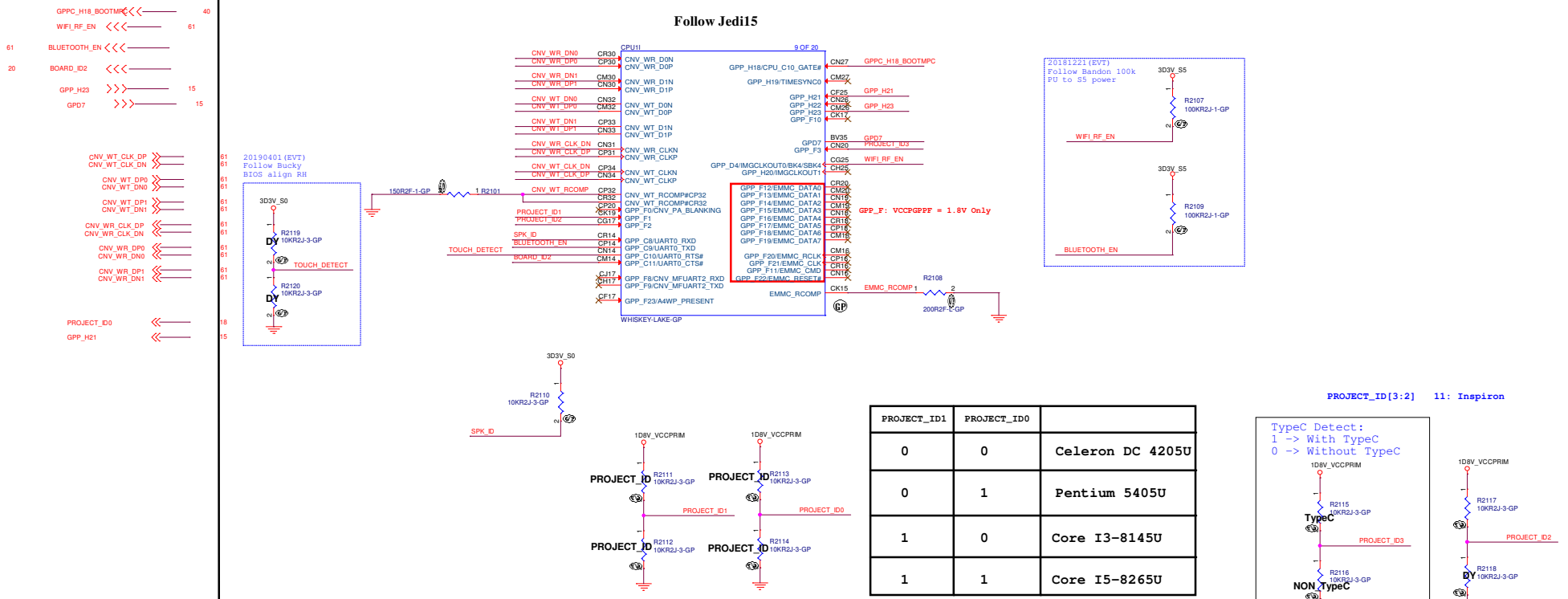
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPSS/ISH)
Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02
Date: Monday, September 23, 2019 | Sheet 20 of 106

Main Func = PCH

Follow Jedi15



PROJECT_ID1	PROJECT_ID0	
0	0	Celeron DC 4205U
0	1	Pentium 5405U
1	0	Core I3-8145U
1	1	Core I5-8265U

PROJECT_ID[3:2] 11: Inspiron

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

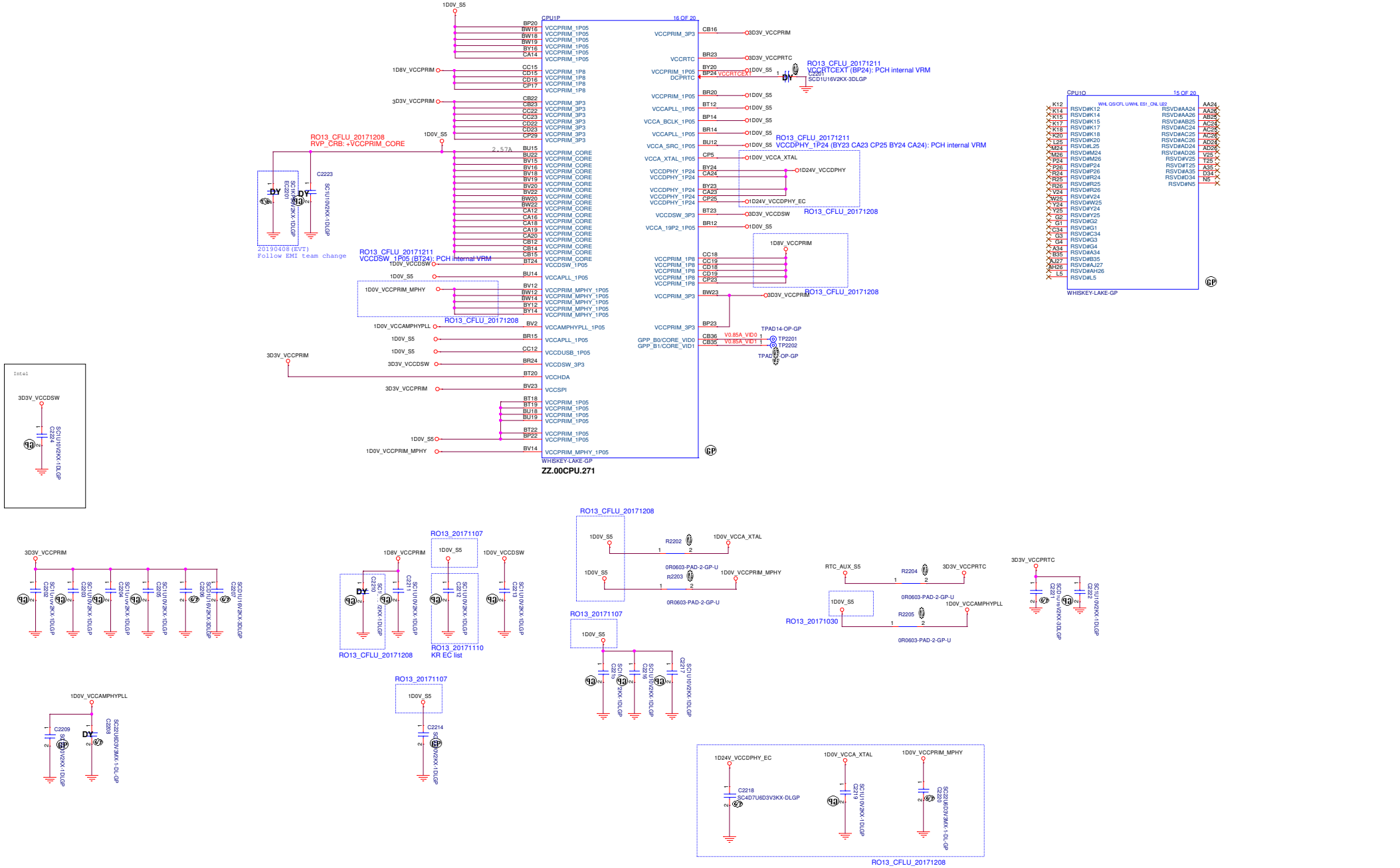
Title: CPU_(POWER1)

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

Date: Monday, September 23, 2019 | Sheet 21 of 106

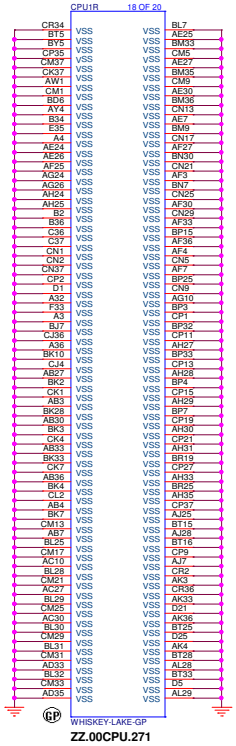
Main Func = PCH

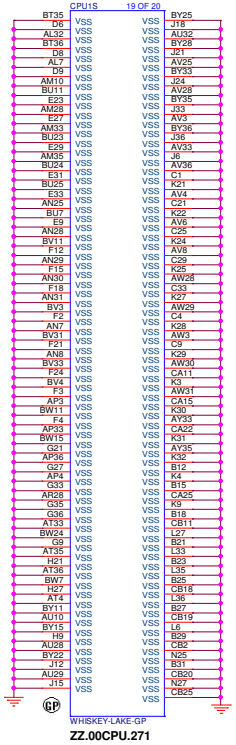
Follow Jedi15

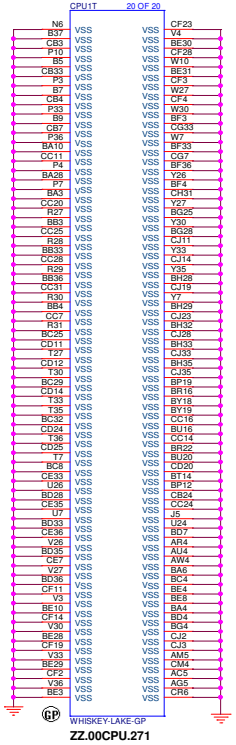


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Main Func = PCH







Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

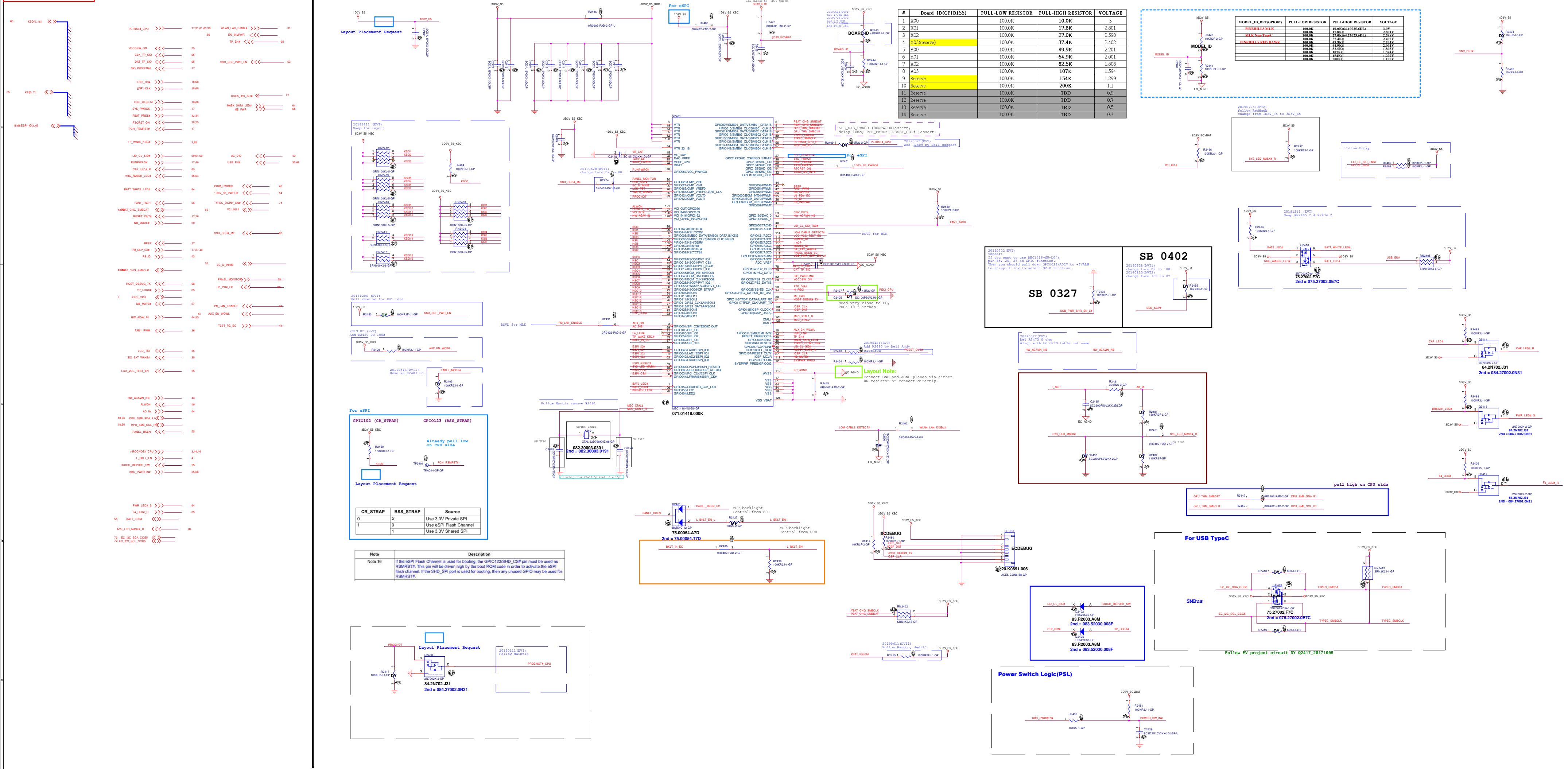
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

Date: Monday, September 23, 2019 | Sheet 23 of 106

Main Func = KBC



#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE285PA0DX

Size: A0 | Document Number: Pinehills 13" WHL-U | Rev: X02

Date: Monday, September 23, 2019 | Sheet 24 of 106

Main Func = SPI Flash

Follow Intel PDG #575412

20190905(ENG)
Remove SSKT1 and SSKT2

Source	QUAD/DUAL fast read	DUAL fast read
072.25128.0D61	O	O
072.25128.0851	O	O
072.25647.000D	O	O
072.25Q64.0H01	O	O

Follow Pinehills KBL

072.25128.0D61
2nd = 072.25128.0B51

Follow Mantis

072.25647.000D
2nd = 072.25Q64.0H01

Main Func = RTC

Follow RO15

75.00054.A7D
2nd = 75.00054.T7D

84.2N702.J31
2nd = 084.27002.0N31

20.F1639.002

084.03415.0031
2nd = 084.02421.0031

84.2N702.J31
2nd = 084.27002.0N31

RTC_RST
75.BAT54.07D
2nd = 75.00054.R7D

RTC_RST
074.06288.007B
2nd = 074.03553.007F

Add RTC Gen 9 reset circuit_20170726

Layout Placement Request

29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

<Core Design>

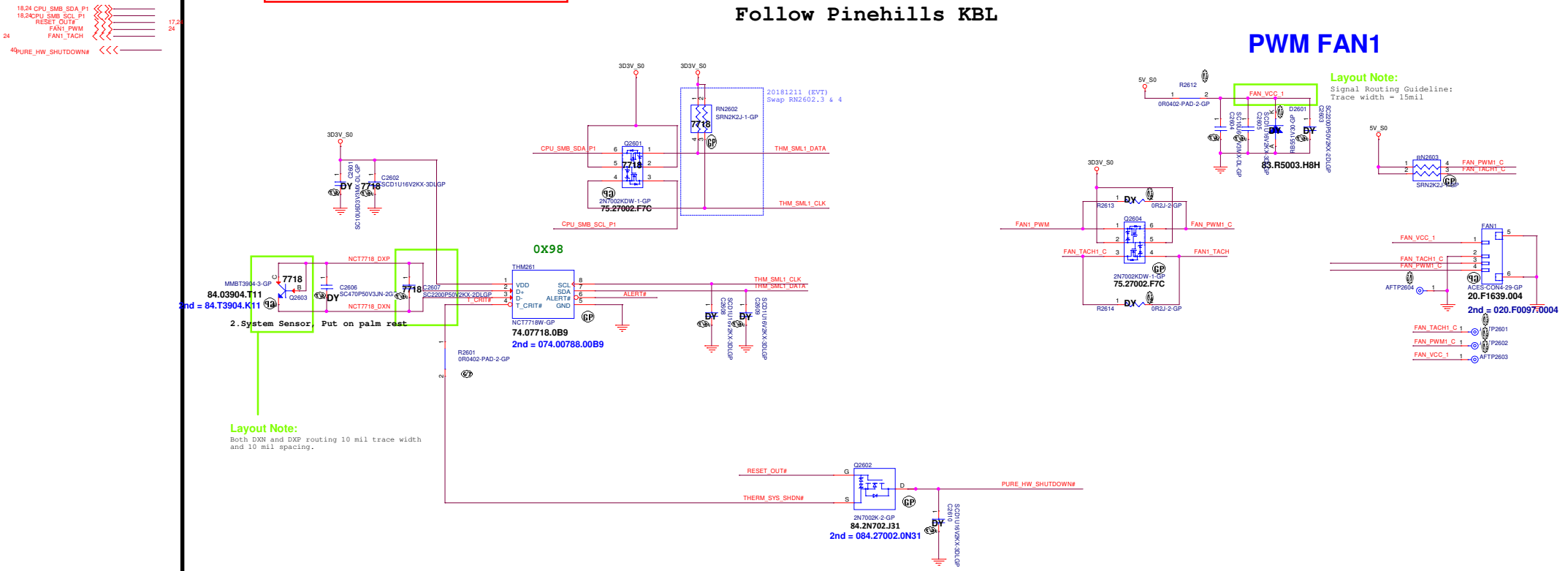
Wistron Corporation
2IF, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

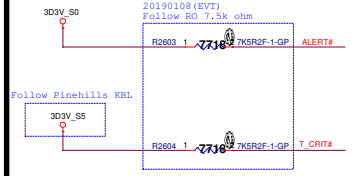
Title: Flash/RTC
Size: Custom | Document Number: Pinehills 13" WHL-U | Rev: X02
Date: Monday, September 23, 2019 | Sheet 25 of 106

Main Func = Thermal Sensor

Follow Pinehills KBL

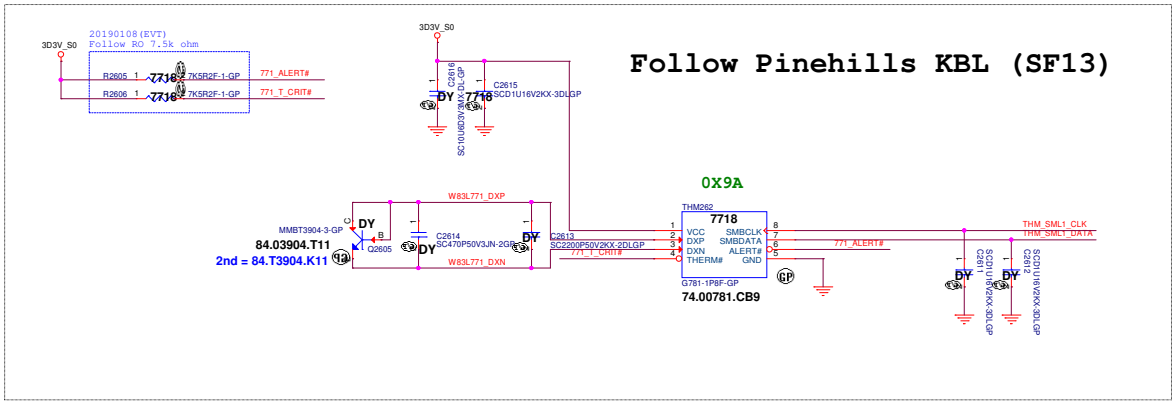
PWM FAN1





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Follow Pinehills KBL (SF13)



<Core Design>

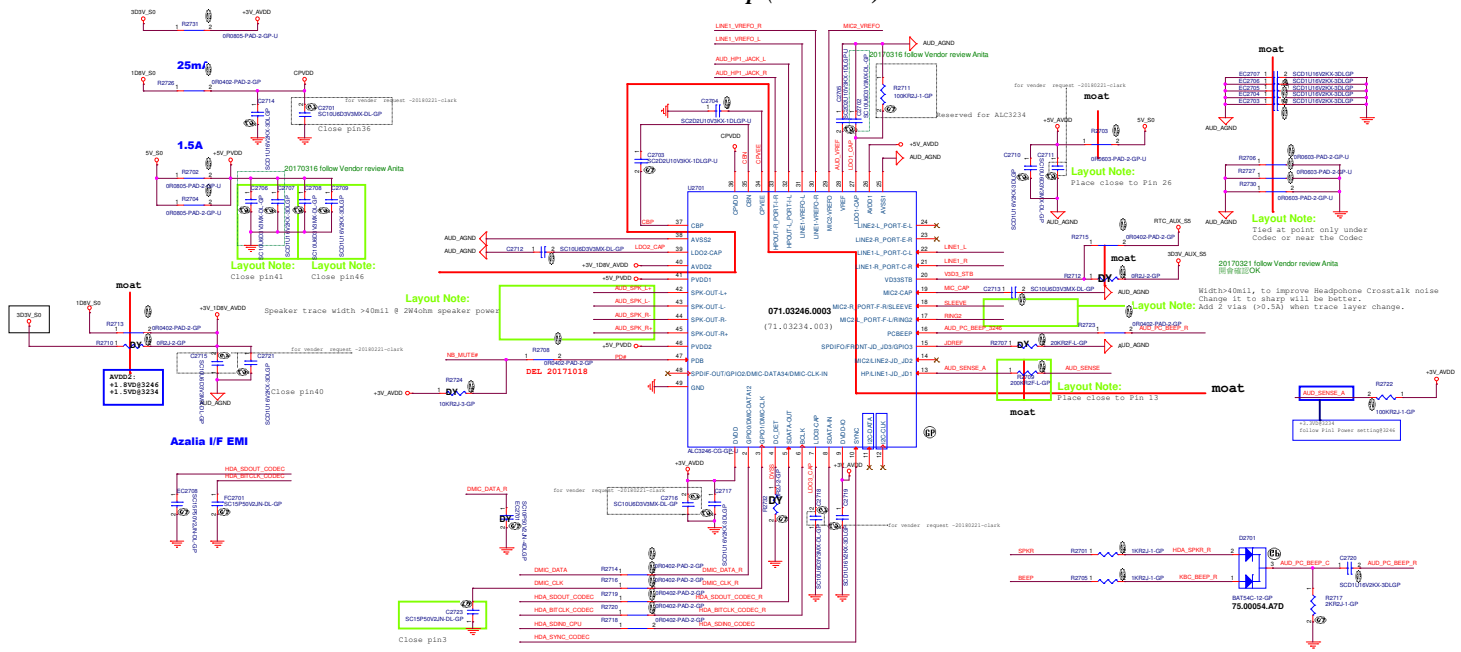
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (Thermal/Fan)
Size: A2
Document Number: Pinehills 13" WHL-U
Rev: X02
Date: Monday, September 23, 2019
Sheet 26 of 106

Main Func = Audio

Follow Pinehills KBL

Audio Codec Chip (ALC3246)



Power requirement:

DVDD must >=DVDD_IO

+3.3V_1.8V_DVDD	+3.3V_1.8V_DVDD_IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: Audio_(Codec ALC3254)	
Size: A3	Document Number: Pinehills 13" WHL-U
Rev: X02	
Date: Monday, September 23, 2019	Sheet 27 of 106

(Blanking)

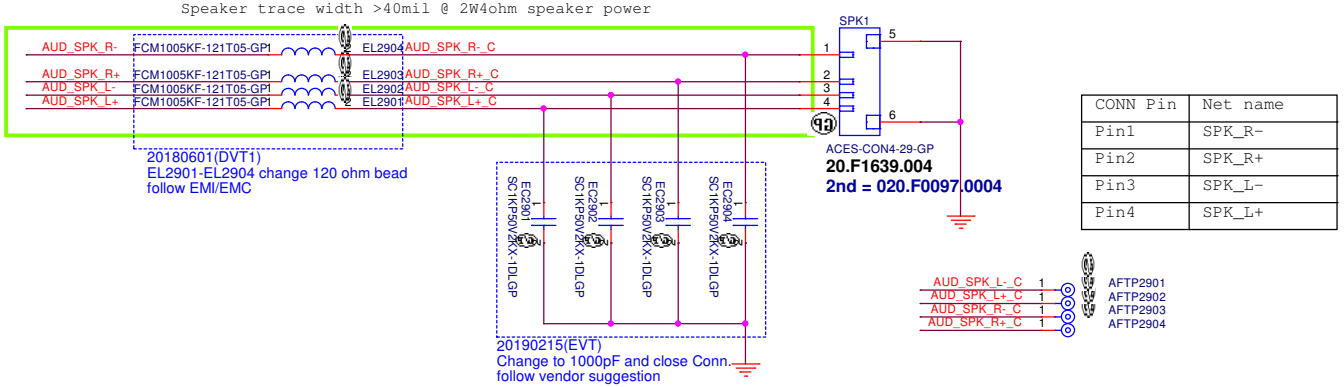
Main Func = Audio

AUD_SPK_R-
AUD_SPK_R+
AUD_SPK_L-
AUD_SPK_L+
MIC2_VREFO
27,29,66 SLEEVE
LINE1_L
AUD_HP1_JACK_L
LINE1_VREFO_L
AUD_HP1_JACK_R
LINE1_R
LINE1_VREFO_R
27,29,66 RING2
SLEEVE
66 AUD_HP1_JACK_L1
JACK_PLUG
66 AUD_HP1_JACK_R1
RING2
AUD_SENSE

Follow Pinehills KBL

Speaker

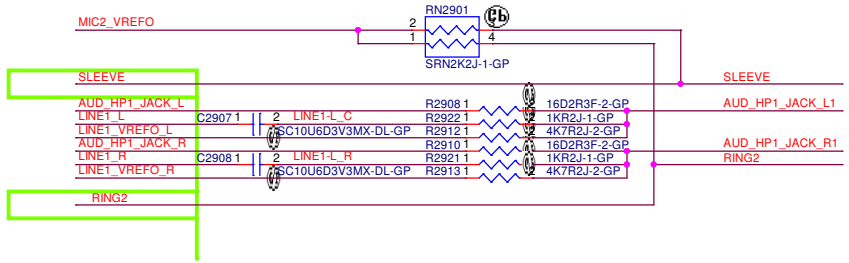
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



CONN Pin	Net name
Pin1	SPK_R-
Pin2	SPK_R+
Pin3	SPK_L-
Pin4	SPK_L+

Follow Pinehills KBL

Universal Jack (Moved to I/O Board)



Layout Note:
Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio_(SPK/Audio_Jack)
Size: A3
Document Number: Pinehills 13" WHL-U
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Date: Monday, September 23, 2019
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

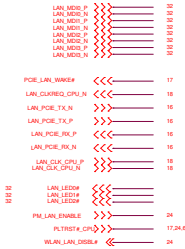
(Reserved)

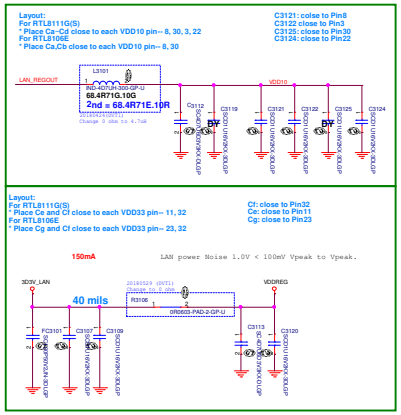
Size	Document Number	Rev
A3	Pinehills 13" WHL-U	X02

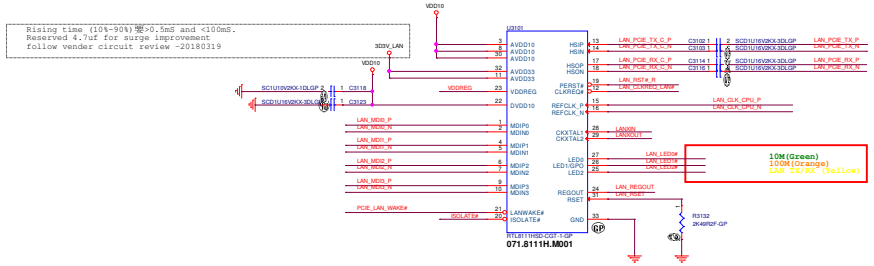
Date: Monday, September 23, 2019 Sheet 30 of 106

SSID = LAN

Follow Pinehills KBL (KS13)

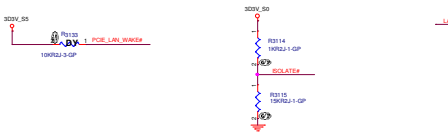


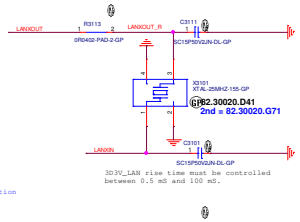


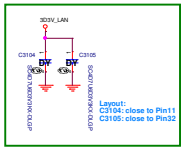


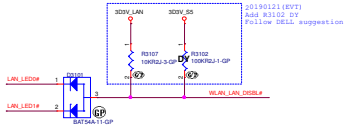
	BOM Option	1.0V Source	Ra	Ch	Cc	Cd	Ce	La	Ci	Cj	Ck	Cl	Cg
RTL8111H-CG (071.8111H.0003)	8111H	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111HSD-CGT-1 (071.8111H.M001)	LAN_SW	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	8106E	LDO	X	X	X	X	X	X	X	X	X	X	O

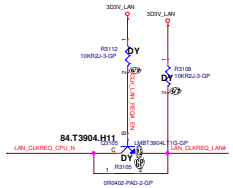
RTL8111H-CG
(071.8111H.0003)

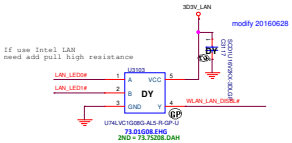


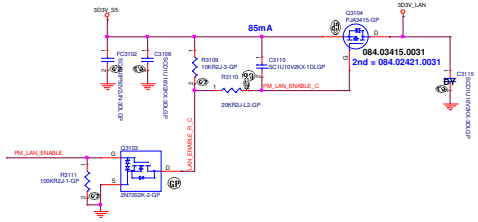












<Core Design>
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Title: LAN
Size: A1
Document Number: Pinehills 13" WHL-U
Rev: X02
Date: Monday, September 09, 2019
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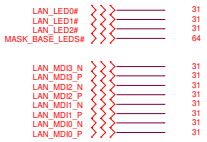
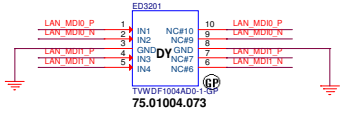
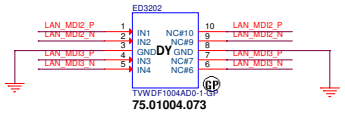
Main Func = LAN

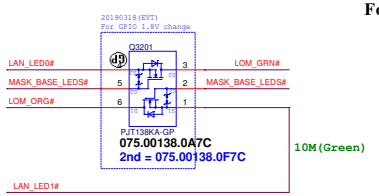
LAN TransFormer

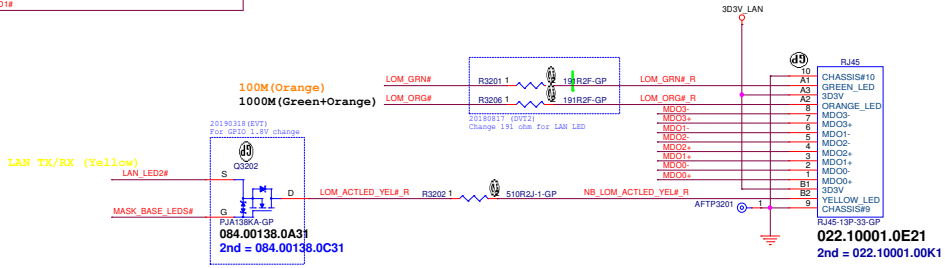
Follow Pinehills KBL (KS13)

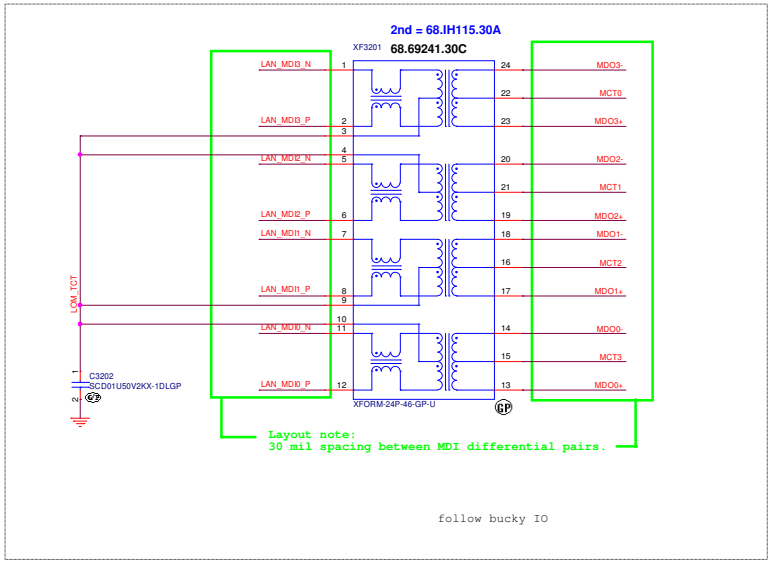


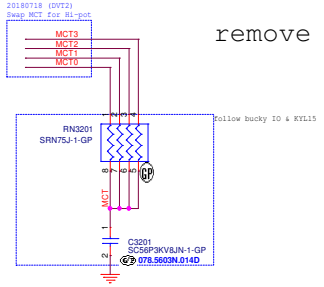












remove TP follow kyloren 15 IO

layout 空間不足

<Core Design>

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Title: RJ45/Transformer

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

Date: Monday, September 23, 2019 | Sheet 32 of 106

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	*Pinehills 13" WHL-U*	*X02*

Date: Monday, September 23, 2019 Sheet 33 of 106

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A3	***Pinehills 13" WHL-U***	***X02***

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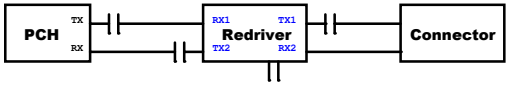
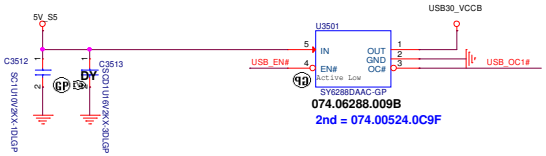
USB_OC1# 16

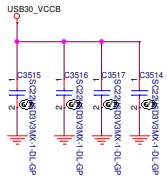
24,66 USB_EN#

Main Func = USB3.0 Port2



Follow Pinehills KBL





<Core Design>

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Title: USB (USB Power switch/Redr)

Size | Document Number: Pinehills 13" WHL-U | Rev: X02

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Main Func = USB3.0 MB Left Side

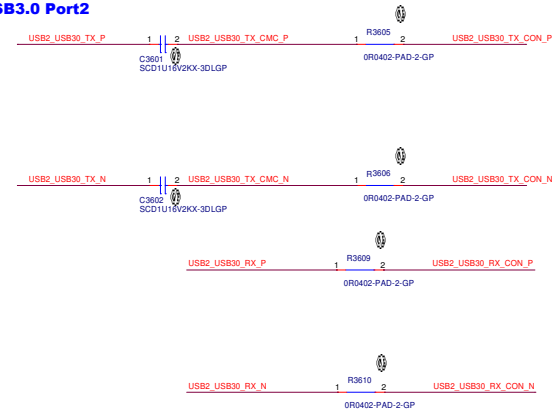
16 USB2_USB20_N
16 USB2_USB20_P

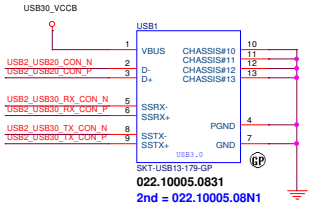
USB2_USB30_TX_P
USB2_USB30_TX_N
16 USB2_USB30_RX_P
16 USB2_USB30_RX_N

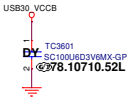
16
16

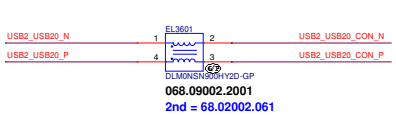
Follow Pinehills KBL

USB3.0 Port2

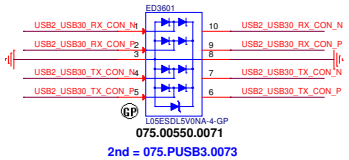


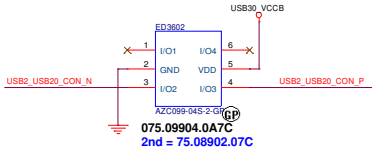






Stuff for ESD R2 spec





USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

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Title: USB_(USB3.0 CONN)

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

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<Core Design>

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Title

USB30

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

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<Core Design>

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Title

USB30

Size	Document Number	Rev
A4	*Pinehills 13" WHL-U*	*X02*

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<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A2	*Pinehills 13" WHL-U*	*X02*

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Main Func = Power Plane & Sequence

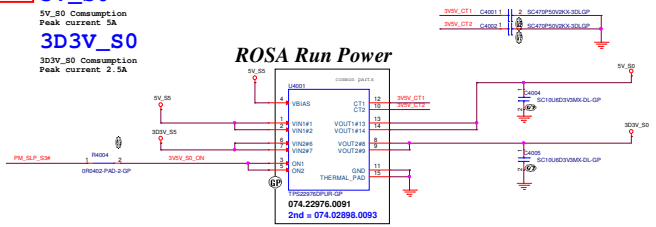
5V_S0

5V_S0 Comsumption
Peak current 5A

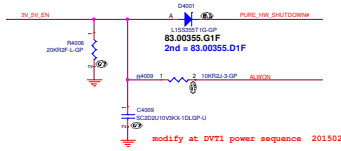
3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

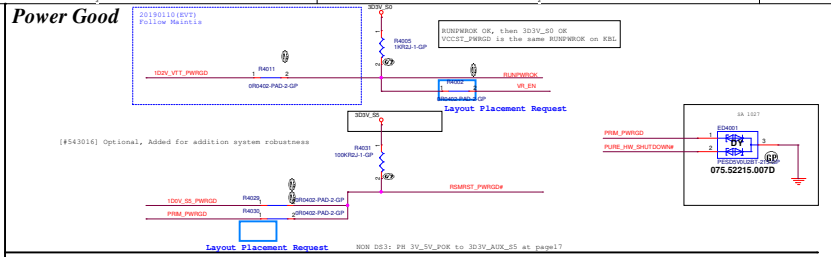
ROSA Run Power



Follow Pinehills KBL



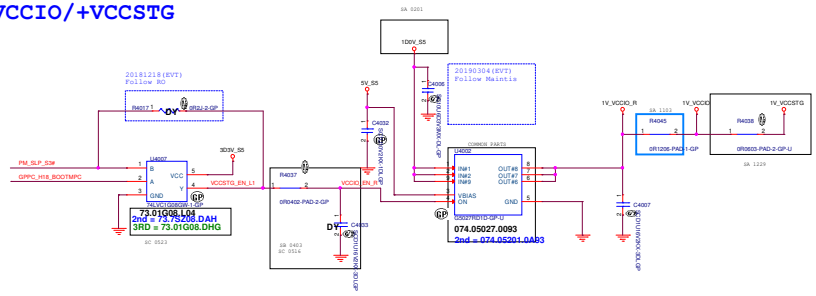
Power Good



RUNPWROK OK, then 3D3V_S0 OK
VCCST_PWRGD is the same RUNPWROK on KBL

Follow Jedi15

+VCCIO/+VCCSTG



EOPIO and EDRAM

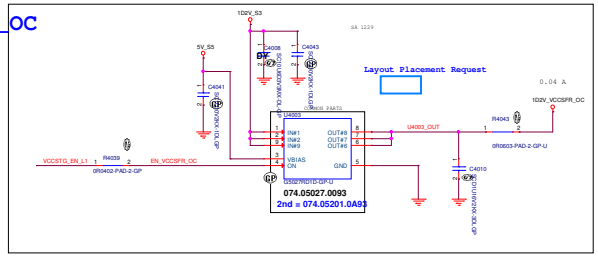
+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

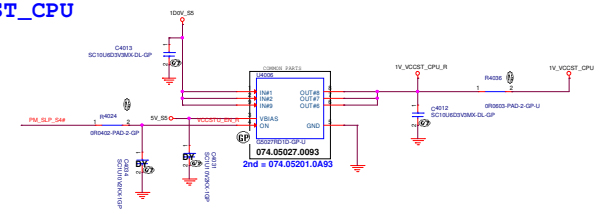
1D2V_VCCSFR_OC



VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

MANAGEMENT RAIL POWER GENERATION

VCCST_CPU



+V1.8S0

https://vinafix.com

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Power Plane Enable

Size: M | Document Number: Pinehills 13" WHL-U | Rev: X02

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20190524 (DVT1)
Change to DY

TEST_PG_EC <<<

24

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.3	0.64	0.9	V

3D3V_S5

R4104 100KR2J-1-GP DY

Q4104_G

Q4104 2N7002K-2-GP DY GP

84.2N702.J31
2nd = 084.27002.0N31

3D3V_S5

R4108 100KR2J-1-GP DY

1V_VCCST_CPU

R4101 100KR2J-1-GP DY

Q4101 PJE8408-R1-00001-GP DY GP

084.08408.0031

3D3V_S5

R4105 100KR2J-1-GP DY

Q4105_G

Q4105 2N7002K-2-GP DY GP

84.2N702.J31
2nd = 084.27002.0N31

1D2V_VCCSFR_OC

R4102 100KR2J-1-GP DY

Q4102 PJE8408-R1-00001-GP DY GP

084.08408.0031

TEST_PG

R4107 0R2J-2-GP DY

TEST_PG_EC

3D3V_S5

R4106 100KR2J-1-GP DY

Q4106_G

Q4106 2N7002K-2-GP DY GP

84.2N702.J31
2nd = 084.27002.0N31

1V_VCCSTG

R4103 100KR2J-1-GP DY

Q4103 PJE8408-R1-00001-GP DY GP

084.08408.0031

<Core Design>

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Title: Connected_Standby(1/2)+DS3

Size: A4 | Document Number: Pinehills 13" WHL-U | Rev: X02

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
A2	Pinehills 13" WHL-U	X02

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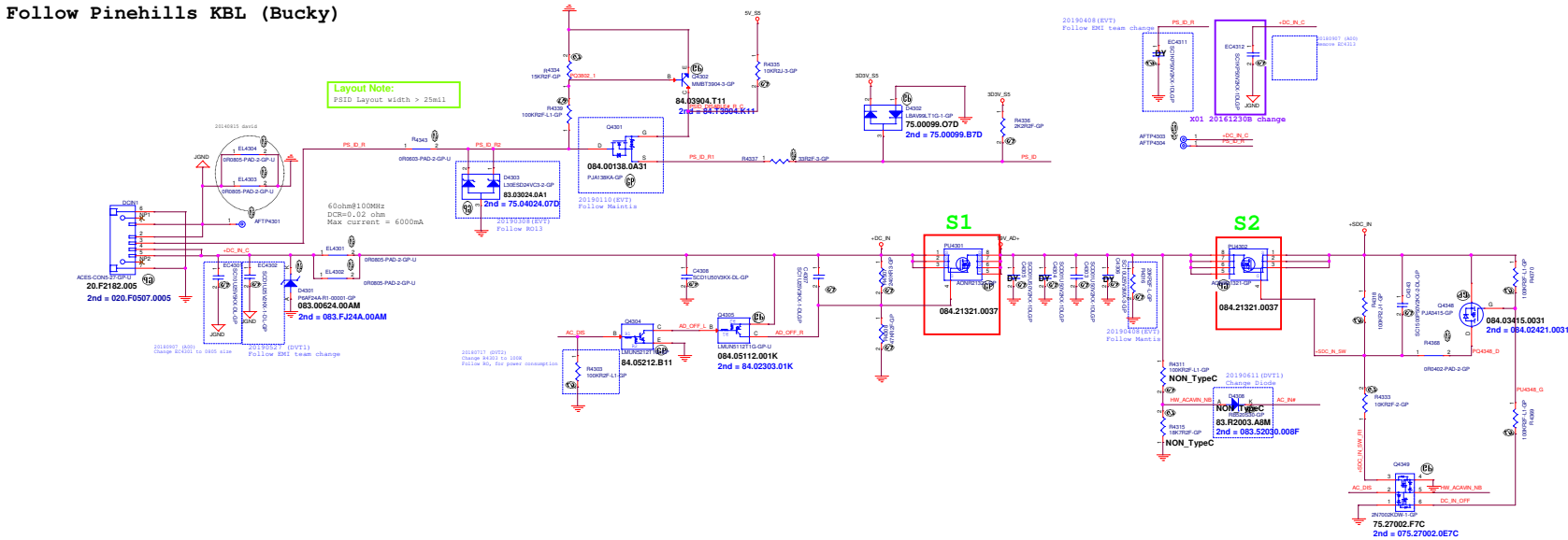
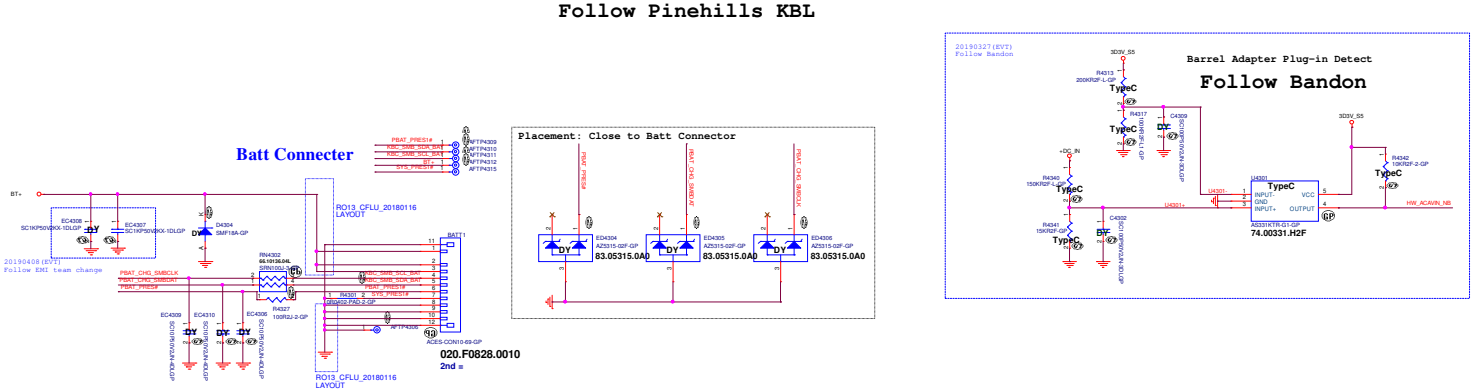
Main Func = ADT Input



Main Func = M-BAT Input



https://vinafix.com

Main Func = Charger

Need EE Check

Follow custormer circuits.

CHECK EE
follow custormer circuits.

+3D3V_VDD_DCIN

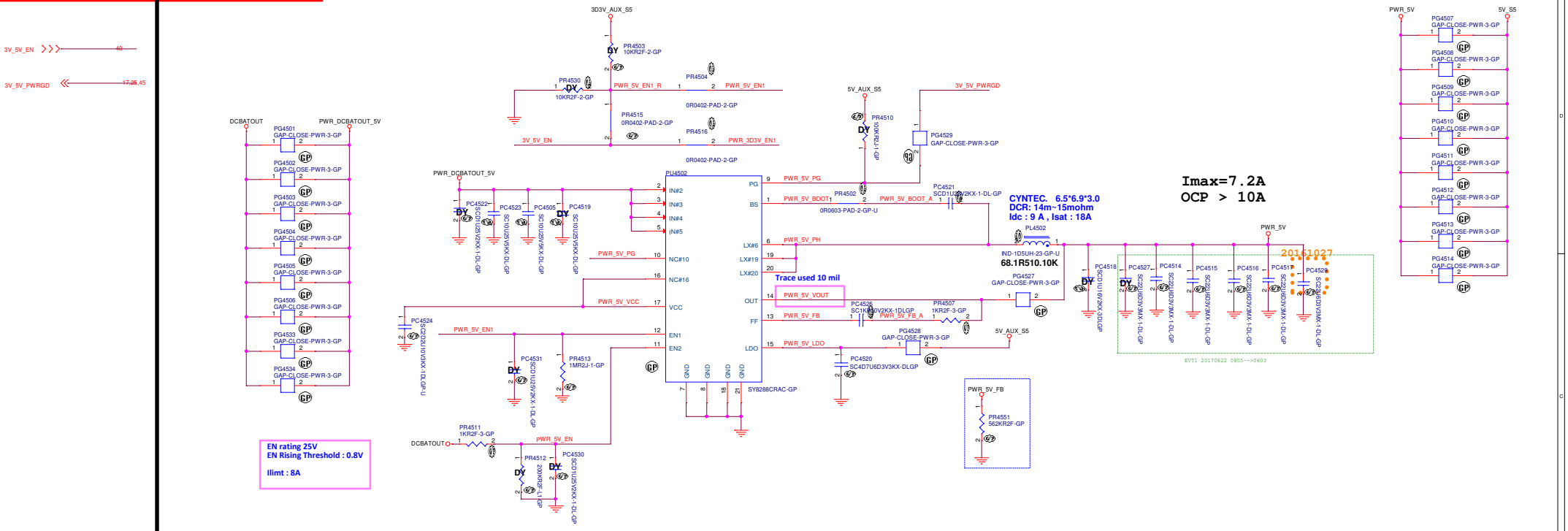
Vcore_OVP

Vsys_UVP

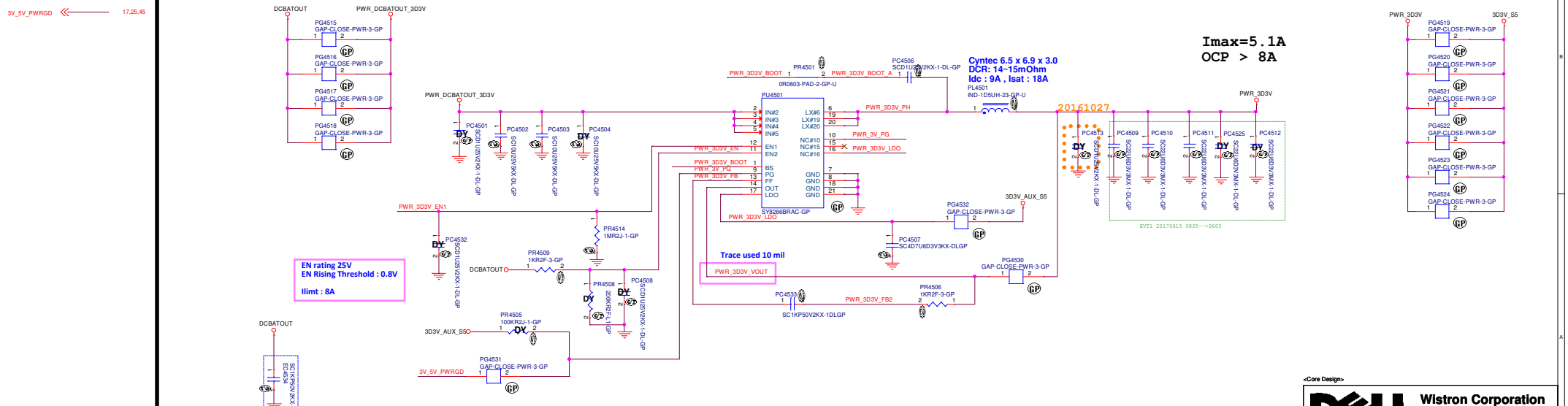
PROG-GND RESISTANCE (kΩ)				DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
MIN	TYP ±1%	MAX	CELL #			
0			1	733kHz	No	0.476
6.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

Wistron Corporation
Charger
Red Hawk 13" WHL-U

SSID = PWR.Plane.Regulator_5V



SSID = PWR.Plane.Regulator_3D3V



<Core Design>

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Title: 5V/3D3V

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

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Main Func = CPU_CORE

SVID

- 7 SVID_CLK_CPU
- 7 SVID_ALERT#_CPU
- 7 SVID_DATA_CPU

VCORE SENSE

- 7 VCC_SENSE
- 7 VSS_SENSE

VCCGT SENSE

- 8 VSSGT_SENSE
- 8 VCCGT_SENSE

VCCSA SENSE

- 8 VSSSA_SENSE
- 8 VCCSA_SENSE

- VR_EN → 30,44
- PROCHOT#_CPU → 3,24,44
- CHGR_PSYS_IMVP → 44

- PWR_VCCGT_ISUMP → 48
- PWR_VCCGT_ISUMN → 48
- PWR_VCCGT_ISEN1 → 48
- PWR_VCCGT_ISEN2 → 48
- PWR_VCCGT_FCCM → 48
- PWR_VCCGT_PWMA → 48
- PWR_VCCGT_PWMB → 48

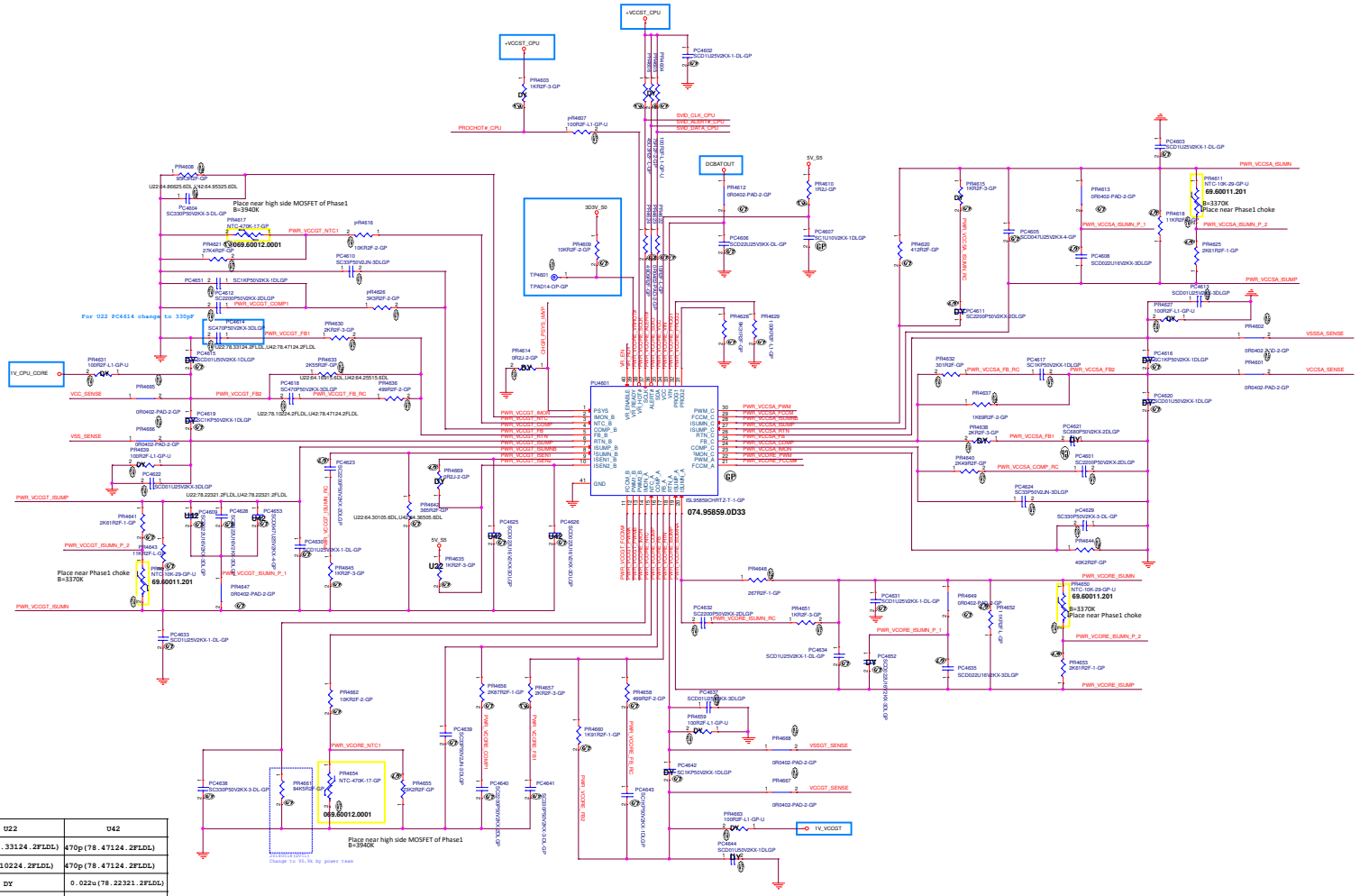
- PWR_VCORE_ISUMN → 47
- PWR_VCORE_ISUMP → 47
- PWR_VCORE_PWM → 47
- PWR_VCORE_FCCM → 47

- PWR_VCCSA_ISUMN → 50
- PWR_VCCSA_ISUMP → 50
- PWR_VCCSA_PWM → 50
- PWR_VCCSA_FCCM → 50

- 17,44 VR_RDY

EE side Link
SVID Pull High V

1V_VCCST_CPU — PG4901 GAP-CLOSE-PWR-3-GP — +VCCST_CPU
PWR_CORE_VCCST



	U22	U42
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)
PC4625	DY	0.022u(78.22321.2FLDL)
PC4626	DY	0.022u(78.22321.2FLDL)
PR4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4642	301(64.30105.6DL)	365 (64.36505.6DL)
PC4630	0.1uF(78.10422.5FLDL)	0.1uF(78.10422.5FLDL)
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)
PC4609	DY	22nF(78.22321.2FLDL)
PC4653	DY	47nF(078.47322.02FD)
PR4633	1.69K(64.16915.6DL)	2.55K(64.25515.6DL)
PR4608	86.6K(64.86625.6DL)	95.3K (64.95325.6DL)

MLK SKU1 CEL U22

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File: ISL95859C_CPU_VCORE(1/3)

Size	Document Number	Rev
A1	Pinehills 13" WHL-U	X02

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Main Func = CPU_CORE

PWR_VCORE_PWM >>> 46
PWR_VCORE_FCCM# >>> 46
PWR_VCORE_ISUMP <<< 46
PWR_VCORE_ISUMN <<< 46

20190613(DVT1)
Remove L4702, L4703
By power team
20190730 (DVT2)
Change to 0805 SPD
20190613(DVT1)
PWR_DCBATOUT_VCORE -> DCBATOUT
20190617(DVT1)
add 0.2m ohm for EMI DVT1 test

DCBATOUT
PWR_DCBATOUT_VCORE
R4701 0R0805-PAD-2-GP-U
R4702 0R0805-PAD-2-GP-U

PWR_DCBATOUT_VCORE
PC4701 SC10U25V3MX-5-GP
PC4702 SC10U25V3MX-5-GP
PC4703 SC10U25V3MX-5-GP
PC4704 SC10U25V3MX-5-GP
U42

PWR_DCBATOUT_VCORE
20190820(DVT2)
Switch TC4702 main source and 2nd
TC4702 ST33U25VDM-5-GP
077.23361.0001
2nd = 79.33612.20L

5V_S5
PR4704 2D2R2F-GP
PWR_VCORE_VCC_R
PC4708 SC1U10V2KX-1DLGP
PC4766 SC1U10V2KX-1DLGP

PR4702 0R0402-PAD-2-GP
PWR_VCORE_PWM
PR4712 5K11R2F-L1-GP
20180518(DVT1)
DY by power team

PWR_DCBATOUT_VCORE

PU4701
VCC
PVCC
VIN
NC#31
PWM
FCCM
NC#30
NC#6
GL#27
GL#35
NC#4
AGND
PGND
BOOT
VSWH#7
VSWH#16
VSWH#17
VSWH#18
VSWH#19
VSWH#20
VSWH#21
VSWH#22
VSWH#23
VSWH#24
VSWH#25
VSWH#26
074.05038.0A73
2nd = 074.03035.0073
AOZ5038QI-05-GP
20180723 (DVT2)
Change P/N by power team

PWR_VCORE_PWM_R
PWR_VCORE_FCCM#
PR4706 0R0402-PAD-2-GP
PWR_VCORE_FCCM#_R

PWR_VCORE_BOOT_RC
PR4705 2D2R3-1-U-GP
PC4707 SCD22U25V3KX-DL-GP
20190807(DVT2)
follow Powerteam request
PWR_VCORE_BOOT
PWR_VCORE_BOOTR
PWR_VCORE_SW

Cyntec 6.8mmx7.6mmx4.0mm
DCR: 0.66m ohm +/-7%
Idc : 36A , Isat : 45A

PL4701 IND-D15UH-14-GP
068.R1510.1021
2nd = 68.R1510.20A

1V_VCCGT

PR4703 2D2R6J-3-GP
PWR_VCORE_SNB
PC4706 SC1KP50V2KX-1DLGP

PG4707 GAP-CLOSE-PWR-3-GP
PG4708 GAP-CLOSE-PWR-3-GP
PWR_VCORE_ISUMP_G
PWR_VCORE_ISUMN_G

PT4701 SE330U2VDM-4-GP
PANASONIC
ESR: 9 mohm
79.33719.20C
2nd = 80.3371V.L01

PR4708 3K65R2F-1-GP
PR4701 0R0402-PAD-2-GP
PWR_VCORE_ISUMP
PWR_VCORE_ISUMN

WHL_U42_15W
Icc(max)=31A
TDC=18A

Confirm with EE
22uF/0603 total 32pcs
(78.22610.5BLDL)

<Core Design>

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Title: ISL95859C_CPU_VCORE(2/3)
Size: A3
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Main Func = CPU_CORE

PWR_VCCGT_PWMA 46
PWR_VCCGT_FCCM# 46
PWR_VCCGT_ISEN1 46,48
PWR_VCCGT_ISUMP 46,48
PWR_VCCGT_ISUMN 46,48
PWR_VCCGT_ISEN2 46,48
PWR_VCCGT_PWMB 46
PWR_VCCGT_ISEN2 46,48
PWR_VCCGT_ISUMP 46,48
PWR_VCCGT_ISUMN 46,48
PWR_VCCGT_ISEN1 46,48

20190613(DVT1) Remove L4803, L4804 By power team
20190613(DVT1) PWR_DCBATOUT_VCORE -> DCBATOUT
20190617(DVT1) add 0.2m ohm for EMI DVT1 test
20190730 (DVT2) Change to 0805 SPD
DCBATOUT
PWR_DCBATOUT_VCCGTA
R4801 0R0805-PAD-2-GP-U
R4802 0R0805-PAD-2-GP-U

PC4802 PC4803 PC4804 PC4805 SC10U25V5MX-5-GP

20190820(DVT2) Switch TC4805 TC4806 main source and 2nd
DCBATOUT
TC4805 ST33U25VDM-5-GP
077.23361.0001
2nd = 79.33612.20L
DCBATOUT 20181205 (EVT) Change TC4401 place Rename to TC4806
U42
TC4806 ST33U25VDM-5-GP
077.23361.0001
2nd = 79.33612.20L

For acoustic noice

WHL_U42_15W
Icc(max)=70A
TDC= 428A

Confirm with EE
22uF/0603 total 36pcs
(78.22610.5BLDL)

Modify netname refer STD rule
2017.10.24

5V_S5
PR4803 2D2R2F-GP
PC4877 SC1U10V2KX-1DLGP
PC4809 SC1U10V2KX-1DLGP
PWR_VCCGT_VCCDA
PWR_DCBATOUT_VCCGTA

PR4802 0R0402-PAD-2-GP
PWR_VCCGT_PWMA
PR4817 5K11R2F-L1-GP DY
20180518(DVT1) DY by power team
PWR_VCCGT_PWMA_RA
PWR_VCCGT_FCCM#
PR4806 0R0402-PAD-2-GP
PWR_VCCGT_FCCM#_RA

PU4801
NC#31 PWM FCCM NC#30 NC#6 GL#27 GL#35
VCC PVCC VIN VIN VIN VIN VIN
BOOT VSWH#7
VSWH#16 VSWH#17 VSWH#18 VSWH#19 VSWH#20 VSWH#21 VSWH#22 VSWH#23 VSWH#24 VSWH#25 VSWH#26
NC#4 AGND PGND PGND PGND PGND PGND
074.05038.0A73
2nd = 074.03035.0073
AOZ5038QI-05-GP
20180723 (DVT2) Change P/N by power team

PWR_VCCGT_BOOTA_RC
PR4804 2D2R3-1-U-GP
PC4808 SCD22U25V3KX-DL-GP
PWR_VCCGT_BOOTA
PWR_VCCGT_BOOTRA
PWR_VCCGT_SWA

20190807(DVT2) follow Powertrain request
PL4801 IND-D15UH-14-GP
068.R1510.1021
2nd = 68.R1510.20A
Cyntec 6.8mmx7.6mmx4.0mm
DCR: 0.66m ohm +/-7%
Idc : 36A , Isat : 45A

1V_CPU_CORE
PT4801 SE330U2VDM-4-GP
PANASONIC
ESR: 9 mohm
79.33719.20C
2nd = 80.3371V.L01

PR4805 2D2R6J-3-GP DY
PWR_VCCGT_SNB1
PC4810 SC1KP50V2KX-1DLGP DY
PG4808 GAP-CLOSE-PWR-3-GP
PG4809 GAP-CLOSE-PWR-3-GP
PWR_VCCGT_ISUMN_GA
PWR_VCCGT_ISUMP_GA
PWR_VCCGT_ISEN1
PWR_VCCGT_ISUMP
PWR_VCCGT_ISUMN
PWR_VCCGT_ISEN2
PR4821 100KR2F-L1-GP
PR4808 3K65R2F-1-GP
PR4809 10R2F-L-GP
PR4822 100KR2F-L1-GP DY

PWR_DCBATOUT_VCCGTA
PC4816 PC4817 PC4814 PC4815 U42 SC10U25V5MX-5-GP

5V_S5
PR4813 2D2R2F-GP U42
PC4866 SC1U10V2KX-1DLGP U42
PC4812 SC1U10V2KX-1DLGP U42
PWR_VCCGT_VCCDB
PWR_DCBATOUT_VCCGTA

PR4811 0R0402-PAD-2-GP
PWR_VCCGT_PWMB
PR4818 5K11R2F-L1-GP DY
20180518(DVT1) DY by power team
PR4812 0R0402-PAD-2-GP
PWR_VCCGT_FCCM#
PWR_VCCGT_PWMB_RB
PWR_VCCGT_FCCM#_RB

PU4802
NC#31 PWM FCCM NC#30 NC#6 GL#27 GL#35
VCC PVCC VIN VIN VIN VIN VIN
BOOT VSWH#7
VSWH#16 VSWH#17 VSWH#18 VSWH#19 VSWH#20 VSWH#21 VSWH#22 VSWH#23 VSWH#24 VSWH#25 VSWH#26
NC#4 AGND PGND PGND PGND PGND PGND
074.05038.0A73
2nd = 074.03035.0073
U42
AOZ5038QI-05-GP
20180723 (DVT2) Change P/N by power team

PWR_VCCGT_BOOTB_RC
U42 PR4810 2D2R3-1-U-GP
U42 PC4811 SCD22U25V3KX-DL-GP
PWR_VCCGT_BOOTB
PWR_VCCGT_BOOTRB
PWR_VCCGT_SWB

Modify netname refer STD rule
2017.10.24

Cyntec 6.8mmx7.6mmx4.0mm
DCR: 0.66m ohm +/-7%
Idc : 36A , Isat : 45A
PL4802 IND-D15UH-14-GP
U42
068.R1510.1021
2nd = 68.R1510.20A

1V_CPU_CORE
U42 PT4803 SE330U2VDM-4-GP
U42 79.33719.20C
2nd = 80.3371V.L01

PR4814 2D2R6J-3-GP DY
PWR_VCCGT_SNB2
PC4813 SC1KP50V2KX-1DLGP DY
PG4813 GAP-CLOSE-PWR-3-GP
PG4815 GAP-CLOSE-PWR-3-GP
PWR_VCCGT_ISUMN_GB
PWR_VCCGT_ISUMP_GB
PWR_VCCGT_ISEN2
PWR_VCCGT_ISUMP
PWR_VCCGT_ISUMN
PWR_VCCGT_ISEN1
PR4823 100KR2F-L1-GP
PR4816 3K65R2F-1-GP
PR4815 10R2F-L-GP
PR4824 100KR2F-L1-GP DY

<Core Design>

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Title: ISL95859C_CPU_VCCGT(3/3)
Size: A2
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<Core Design>

Wistron Corporation
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Title: NCP81210MN_CPU_VCCGTUS

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

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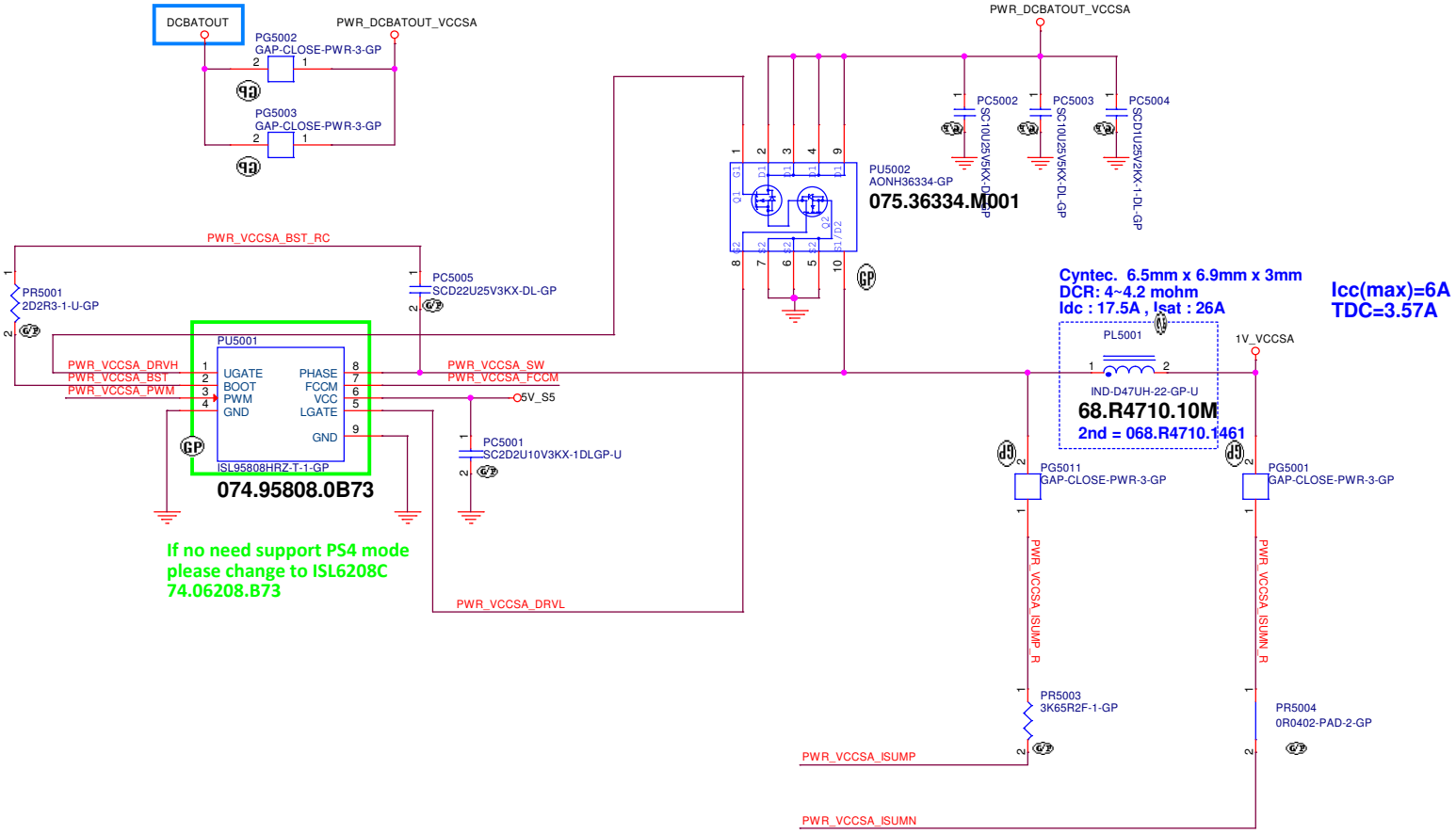
Main Func = VCCSA

068.R4710.2141
Cyntec. 4.85mm x4.7mm x3.0mm
DCR: 5.0~5.9mohm
Idc : 14A , Isat : 14.2A

Icc(max)=6A
TDC=4.5A

PWR_VCCSA_PWM >>> 46
46 PWR_VCCSA_ISUMP <<<
46 PWR_VCCSA_ISUMN <<<
PWR_VCCSA_FCCM >>> 46



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Title		
VCCSA		
Size A3	Document Number: Pinehills 13" WHL-U	Rev: X02
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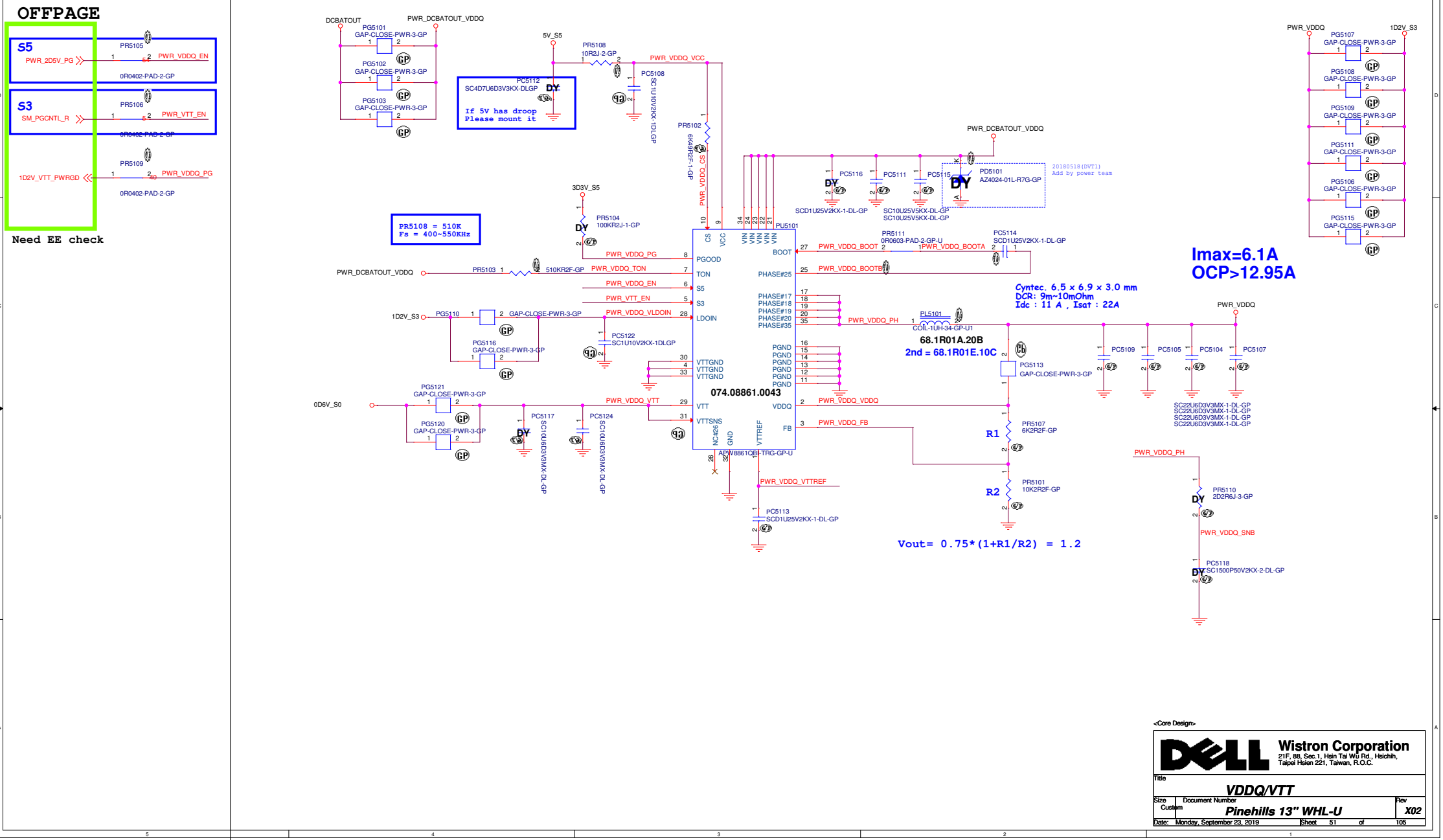
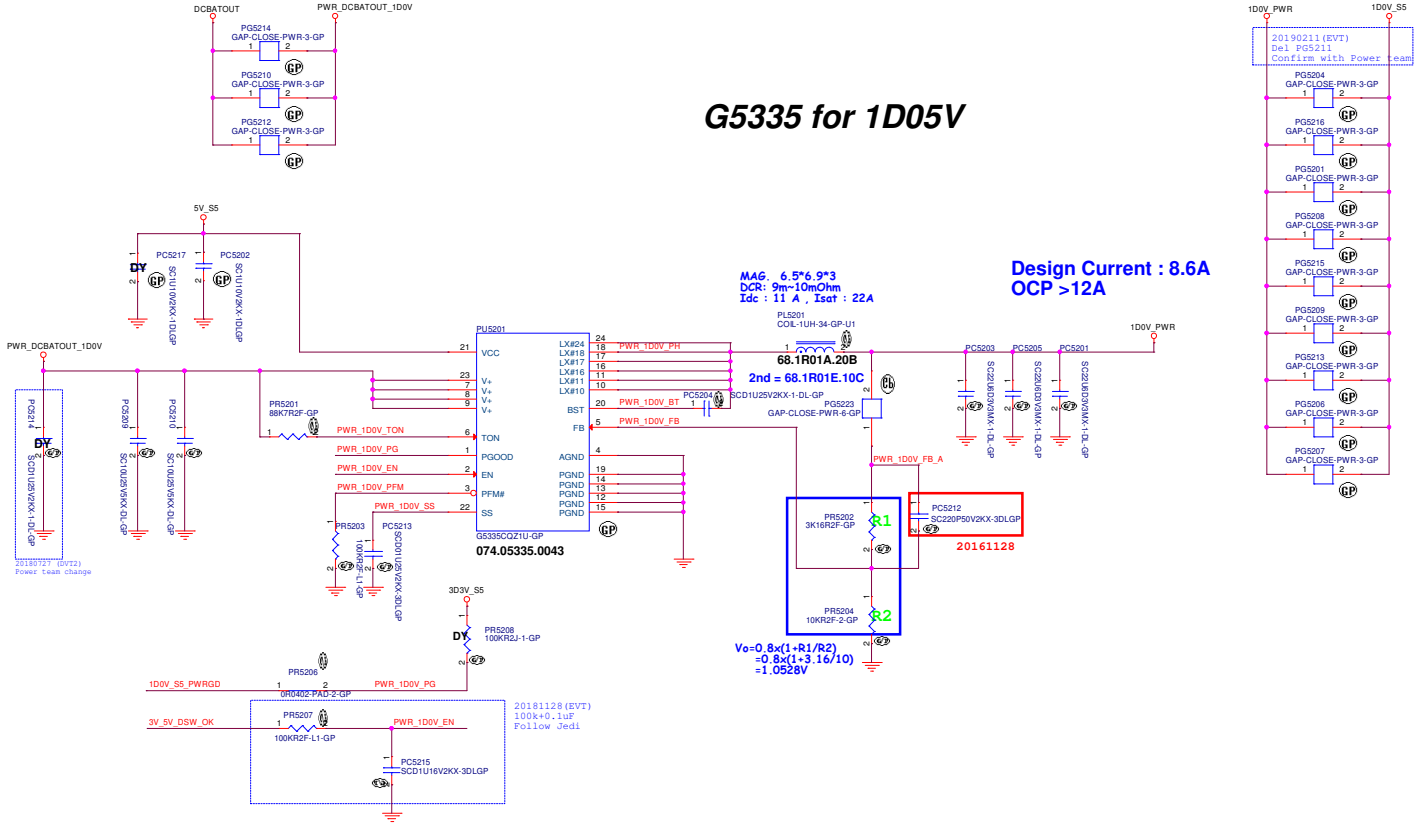


SSID = PWR.Plane.Regulator_1D0V

1D0V_S5_PWRGD <<< 40

3V_5V_DSW_OK >>> 25,54



<Core Design>

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Title: 1D05V_S5

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SSID = PWR.Plane.Regulator_VCCIO/VCCPRIM_CORE

<Core Design>

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Title: (Reserved)

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Main Func = 2D5V/ 1D8V

PM_SLP_S4# >>> 17,40

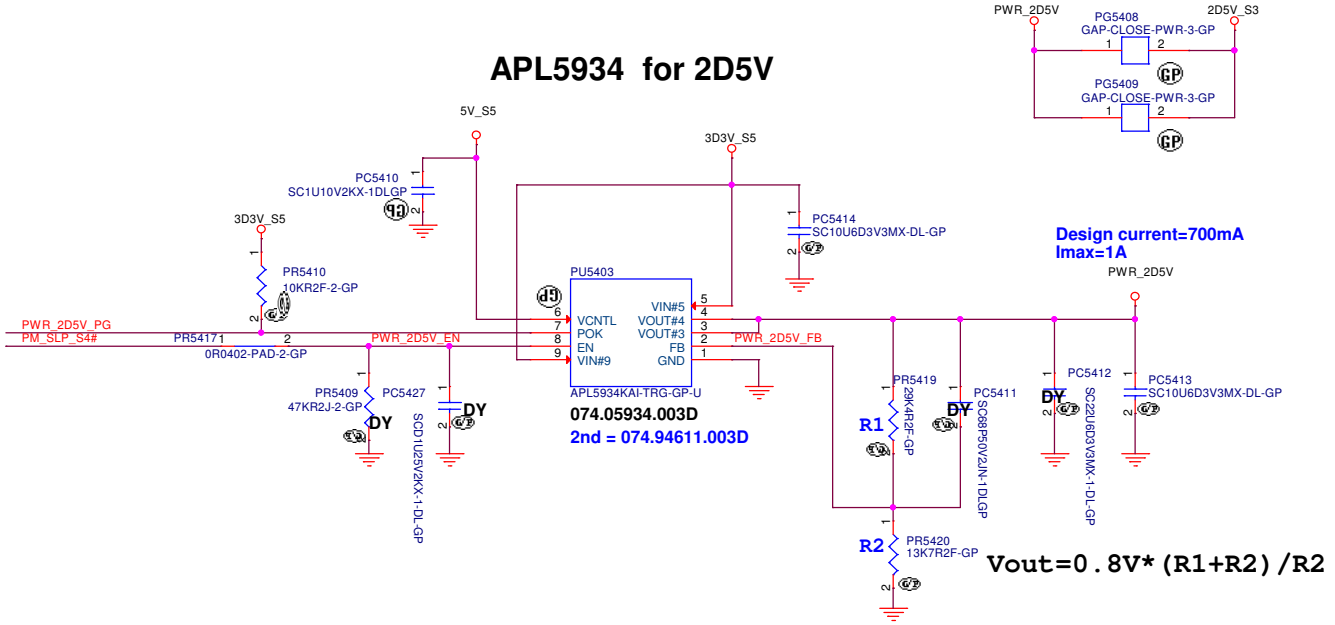
PWR_2D5V_PG <<< 51

3V_5V_DSW_OK >>> 25,52

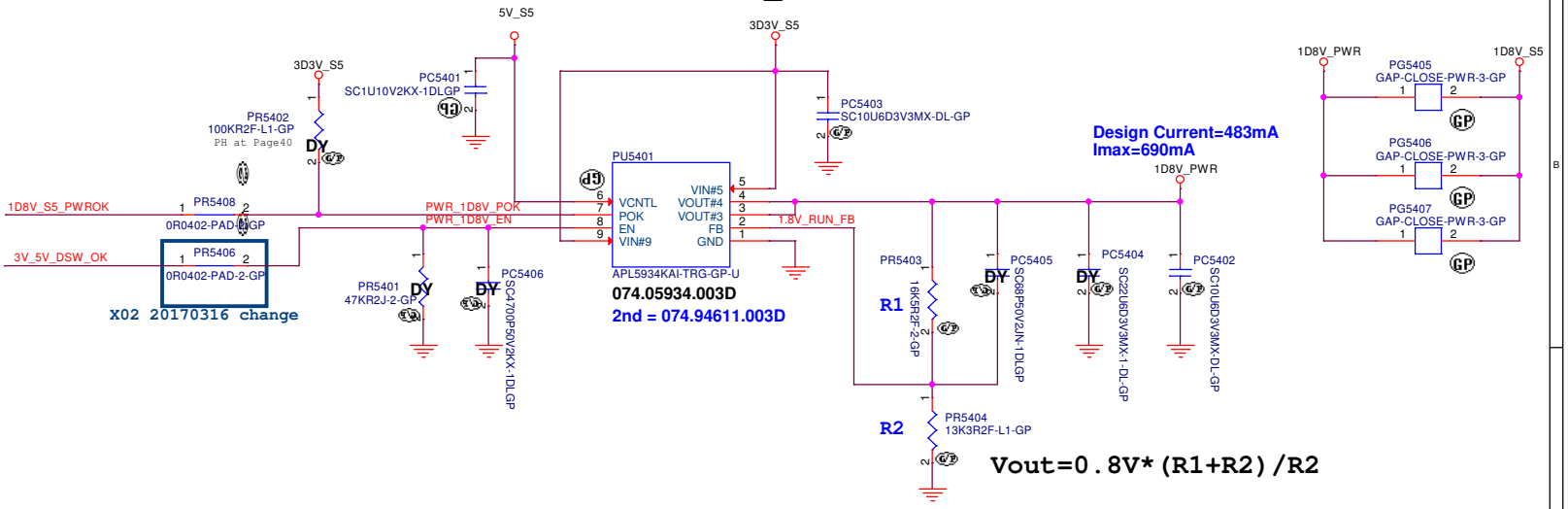
24 1D8V_S5_PWROK <<<

Main Func = 2D5V/ 1D8V

APL5934 for 2D5V



APL5934 for 1D8V_S5



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Title: (Reserved)

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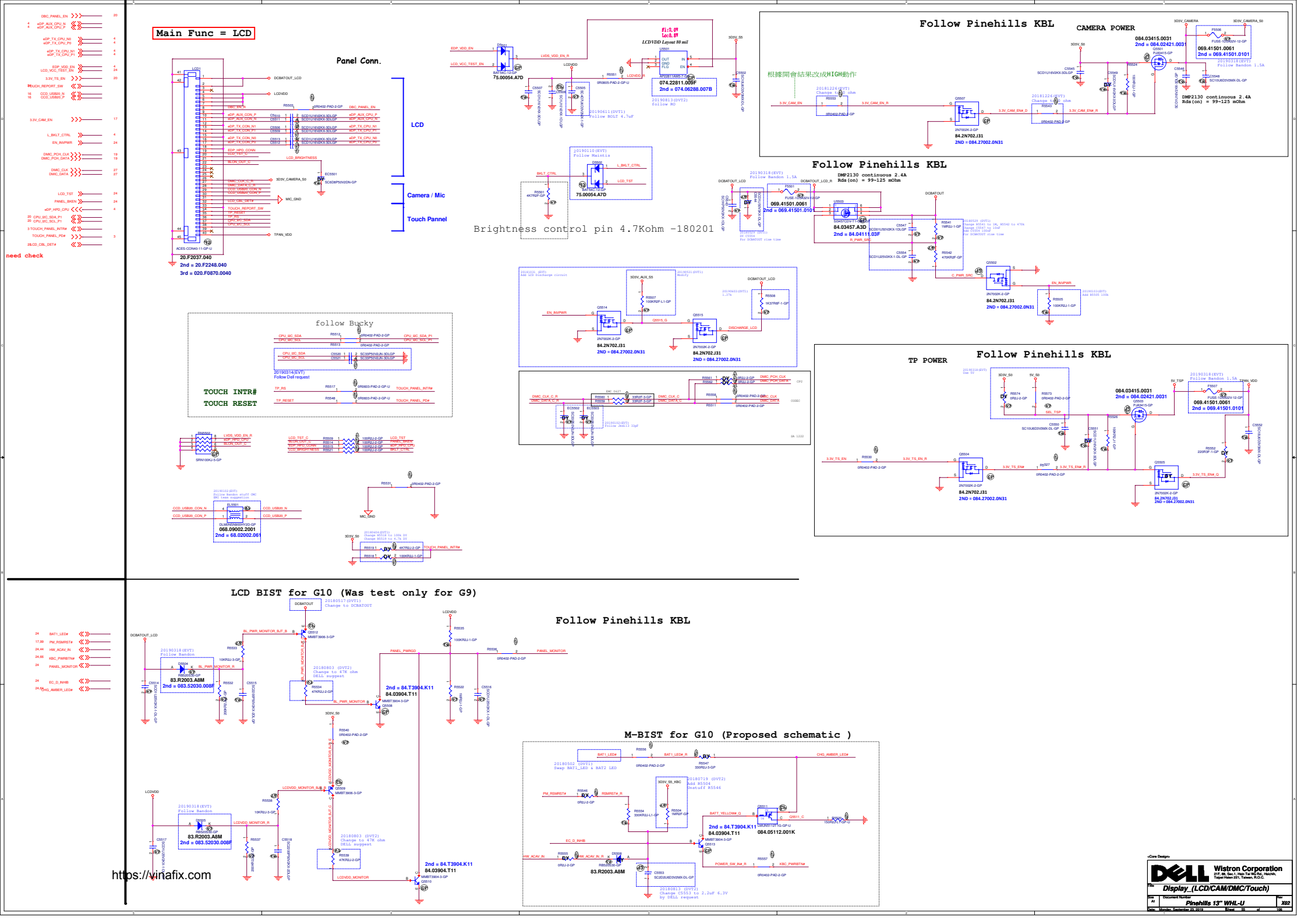
Main Func = LCD
Panel Conn.
LCD
Camera / Mic
Touch Pannel
20.F2037.040
2nd = 020.F2248.040
3rd = 020.F0870.0040
Brightness control pin 4.7Kohm -180201
Follow Pinehills KBL
CAMERA POWER
084.03415.0031
2nd = 084.02421.0031
069.41501.0061
2nd = 069.41501.0101
DMP2130 continuous 2.4A
Rds(on) = 99~125 mOhm
84.2N702.J31
2ND = 084.27002.0N31
84.03457.A3D
2nd = 84.04111.03F
TP POWER
follow Bucky
TOUCH INTR#
TOUCH RESET
need check
LCD BIST for G10 (Was test only for G9)
M-BIST for G10 (Proposed schematic)
83.R2003.A8M
2nd = 083.52030.008F
2nd = 84.T3904.K11
84.03904.T11
084.05112.001K
https://vinafix.com
Wistron Corporation
Display_(LCD/CAM/DMC/Touch)
Pinehills 13" WHL-U
X02

Main Func = IR CAM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT***

Size	Document Number	Rev
A4	***Pinehills 13" WHL-U***	***X02***

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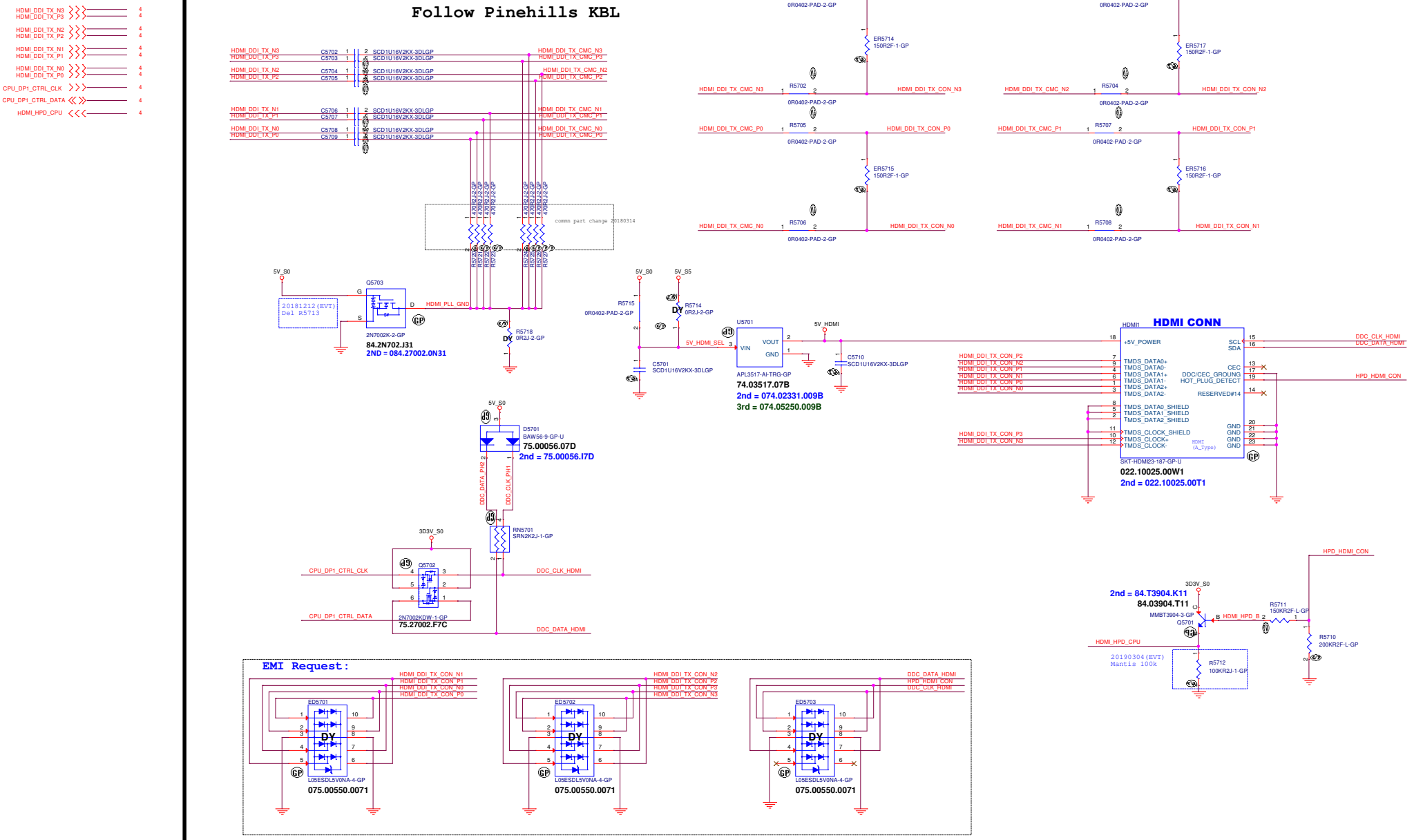
Main Func = HDMI

Follow Pinehills KBL



https://vinafix.com

<Core Design>

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Title: Display (HDMI LS/CONN)

Size	Document Number	Rev
A2	Pinehills 13" WHL-U	X02

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<Core Design>

Wistron Corporation
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Title
(Reserved)

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<Core Design>

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Title
(Reserved)

Size	Document Number	Rev
A3	*Pinehills 13" WHL-U*	*X02*

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<Core Design>

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Title

(Blanking)

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

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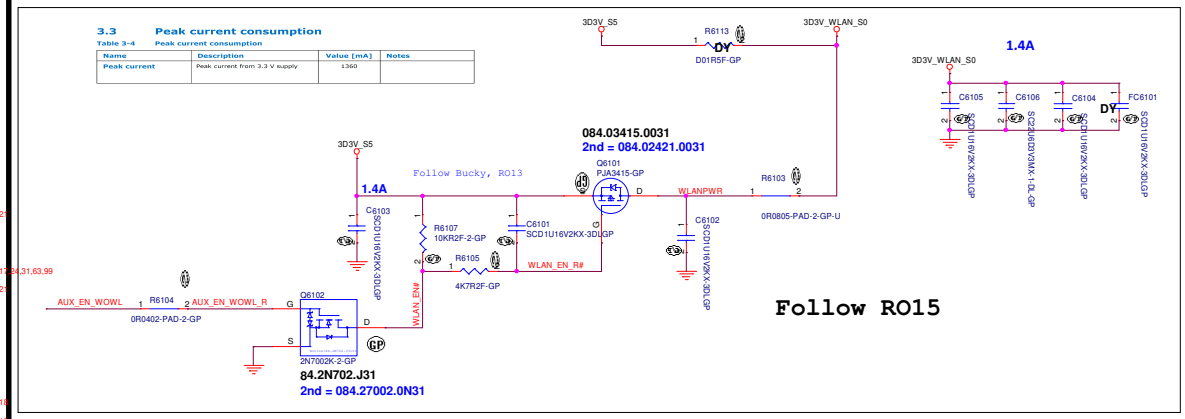
Main Func = WLAN

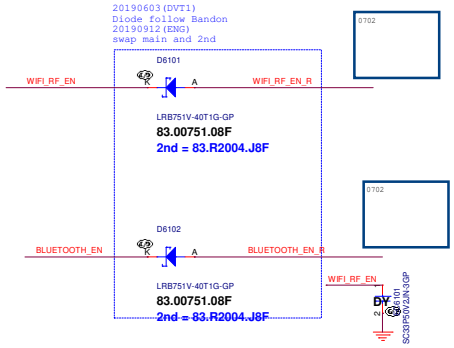
3.3 Peak current consumption

Table 3-4 Peak current consumption

Name	Description	Value [mA]	Notes
Peak current	Peak current from 3.3 V supply	1360	

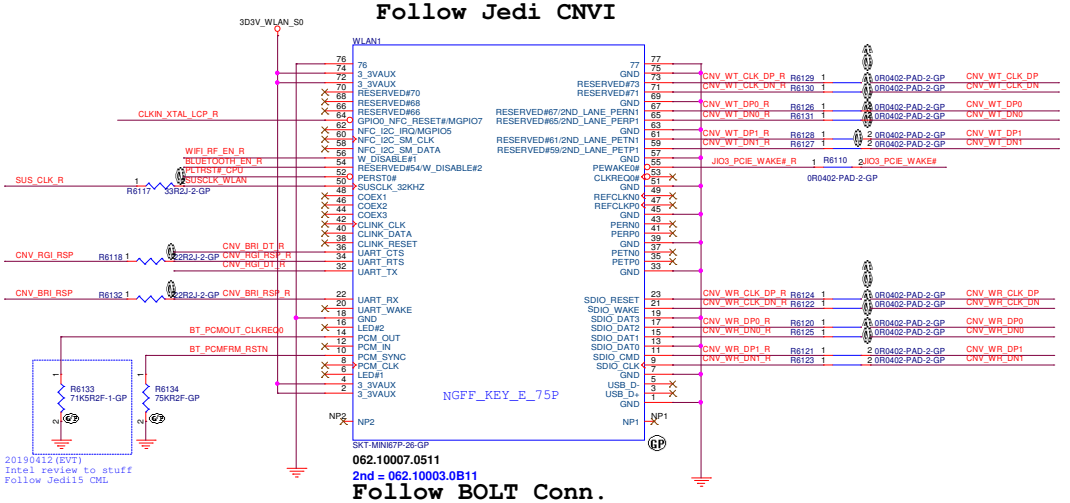


WIFI_RF_EN
PLTRST#_CPU
BLUETOOTH_EN



CLKIN_XTAL_LCP_R
BT_PCMOUT_CLKREQ0
BT_PCMFRM_RSTN
JIO3_PCIE_WAKE#
PCIE_WLAN_WAKE#
AUX_EN_WOWL
SUS_CLK_R
CNV_RGI_RSP
CNV_BRI_RSP
CNV_BRI_DT_R
CNV_RGI_DT_R
CNV_WT_CLK_DP
CNV_WT_CLK_DN
CNV_WT_DP0
CNV_WT_DN0
CNV_WT_DP1
CNV_WT_DN1
CNV_WR_CLK_DP
CNV_WR_CLK_DN
CNV_WR_DP0
CNV_WR_DN0
CNV_WR_DP1
CNV_WR_DN1

Follow Jedi CNVI



https://vinafix.com

<Core Design>

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Title: NGFF_WLAN CONN

Size: A2 | Document Number: Jedi15"/17" WHL-U | Rev: X02

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(Blanking)

<Core Design>

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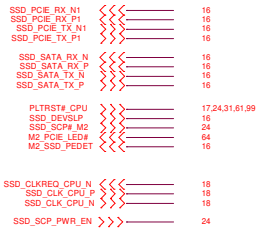
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Pinehills 13" WHL-U***	***X02***

Date: Monday, September 23, 2019 Sheet 62 of 106



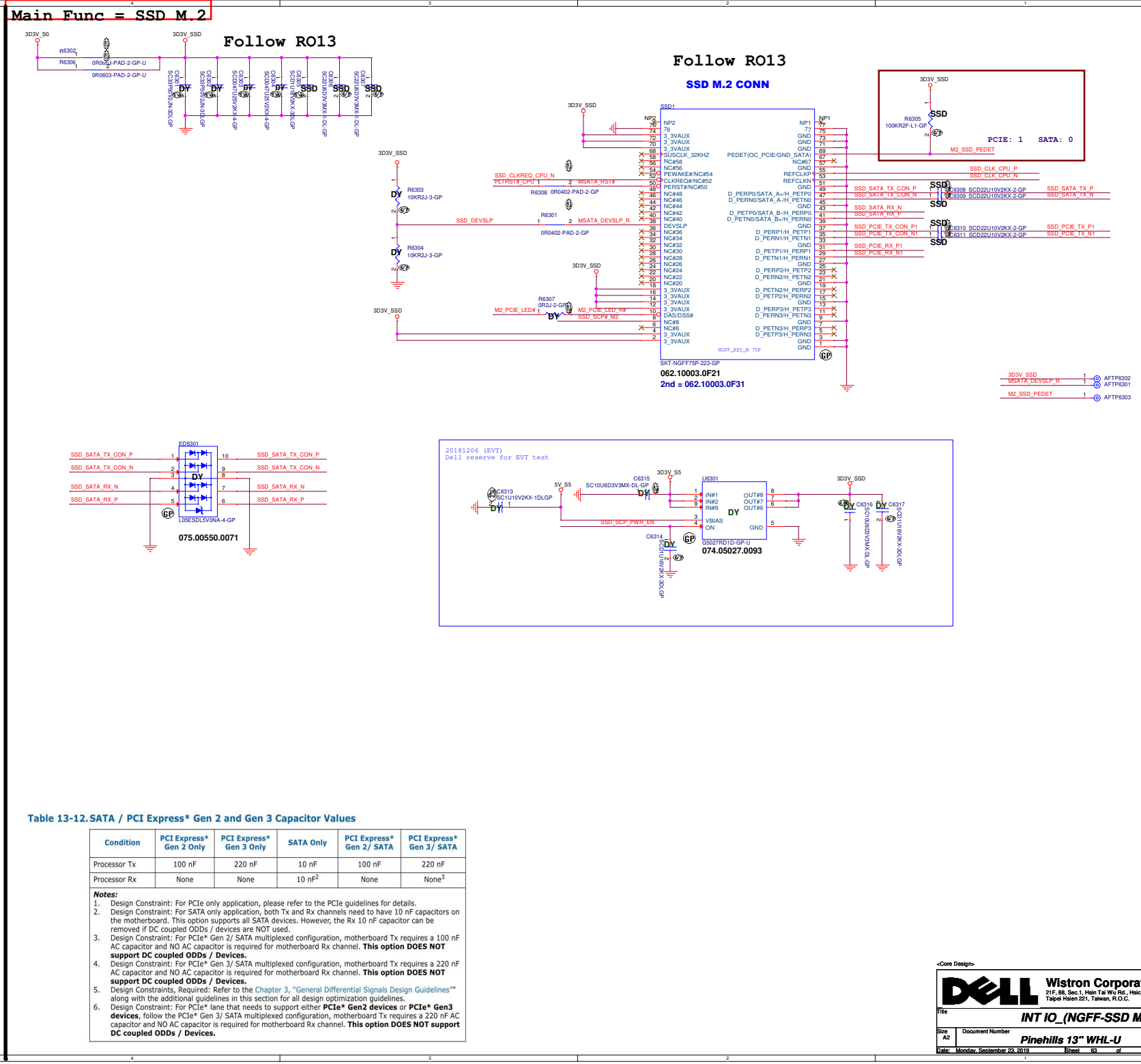


Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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Title: INT IO_(NGFF-SSD M.2)

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

Date: Monday, September 23, 2019 | Sheet 53 of 106

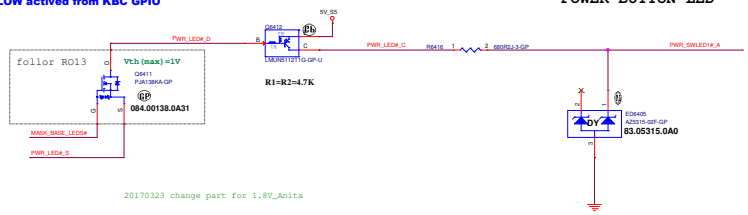
RED HAWK

Main Func = Power BTN

Power LED
LOW actived from KBC GPIO

follow keystone 13

POWER BUTTON LED

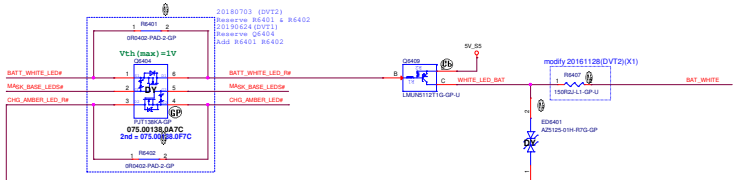


Main Func = Battery LED

follow keystone 13

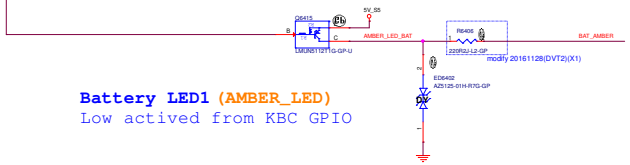
Battery LED2 (WHITE_LED)

Low actived from KBC GPIO



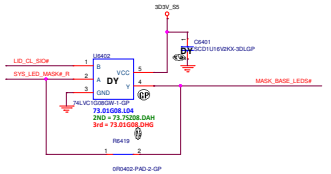
20170323 change part for 1.8V_Anita

Follow KEYSTONT 13



Battery LED1 (AMBER_LED)

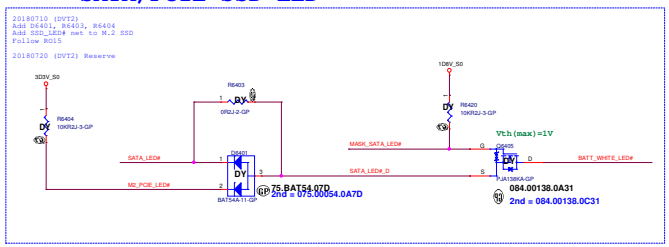
Low actived from KBC GPIO



Main Func = SATA/PCIE SSD LED

Follow Pinehills KBL

SATA/PCIE SSD LED



<Core Design>

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File: INT IO (KB/TP)

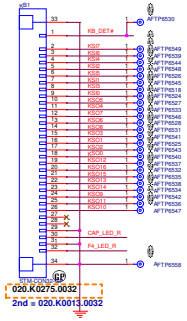
Size	Document Number	Rev
A1	Pinehills 13" WHL-U	X02

Date: Monday, September 23, 2019 Sheet 64 of 106

Main Func = KB

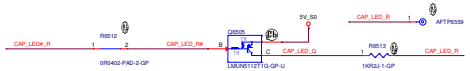
Follow Pinehills KBL (SF13)

Internal KeyBoard Connector



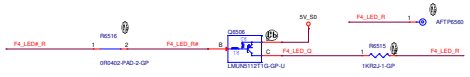
MB Pin NO.	Description	Module Pin NO.
1	Diagnostic	1
2	KSI[7]:S8	2
3	KSI[6]:S7	3
4	KSI[4]:S5	4
5	KSI[2]:S3	5
6	KSI[5]:S6	6
7	KSI[1]:S2	7
8	KSI[3]:S4	8
9	KSI[0]:S1	9
10	KSO[5]:D6	10
11	KSO[4]:D5	11
12	KSO[7]:D8	12
13	KSO[6]:D7	13
14	KSO[8]:D9	14
15	KSO[3]:D4	15
16	KSO[1]:D2	16
17	KSO[2]:D3	17
18	KSO[0]:D1	18
19	KSO[12]:D13	19
20	KSO[16]:D17	20
21	KSO[15]:D16	21
22	KSO[13]:D14	22
23	KSO[14]:D15	23
24	KSO[9]:D10	24
25	KSO[11]:D12	25
26	KSO[10]:D11	26
27	NC	27
28	NC	28
29	GND	29
30	Caps Lock LED	30
31	GND	31
32	F4 LED(MIC Mute LED)	32

CAP LED Control
LOW actived from KBC GPIO



R1=R2=4.7K

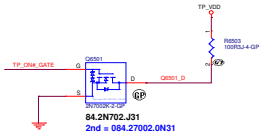
F4 LED (MIC Mute LED) Control
LOW actived from KBC GPIO



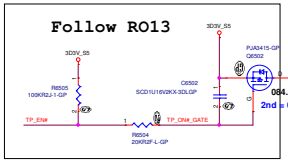
R1=R2=4.7K

Main Func = TPAD

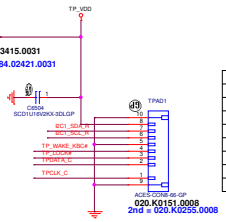
TP_VDD Discharge Circuit



Follow RO13



Precision Touch Pad Connector



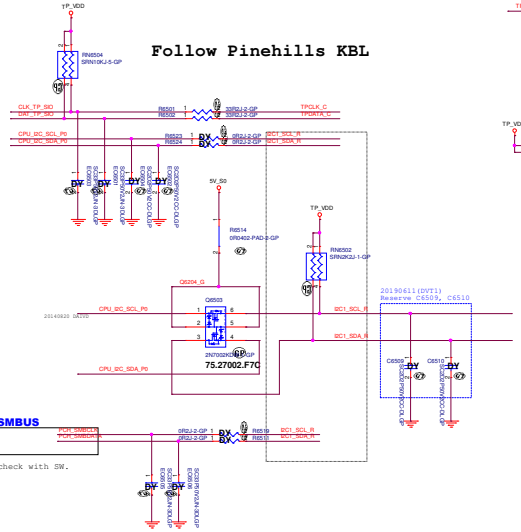
Pin number	Pin name
8	VDD
7	DAT(I2C)
6	CLK(I2C)
5	GND
4	ATTN
3	GPIO
2	DAT(PS2)
1	CLK(PS2)

Follow Pinehills KBL

Support PTP

PS2

I2C



SMBUS

Need to check with SW.

<Core Design>
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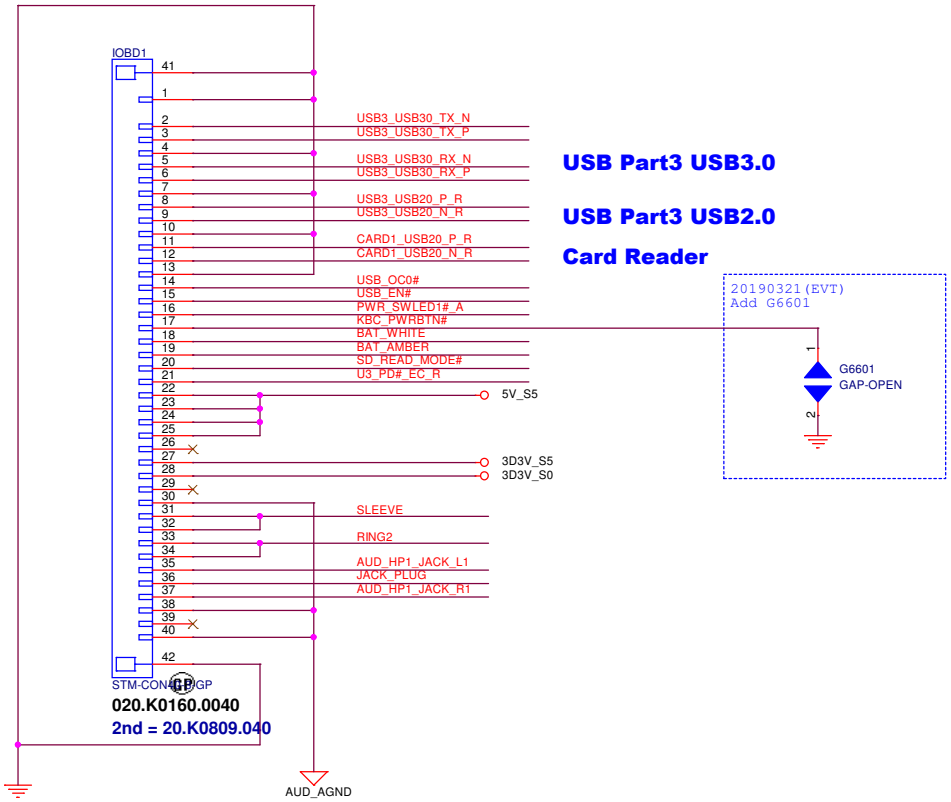
Title: INT IO (KB/TP)
Size: M | Document Number: Pinehills 13" WHL-U | Rev: X02
Date: Monday, September 23, 2019 | Sheet 65 of 106

Main Func = IO Connector

Follow Pinehills KBL



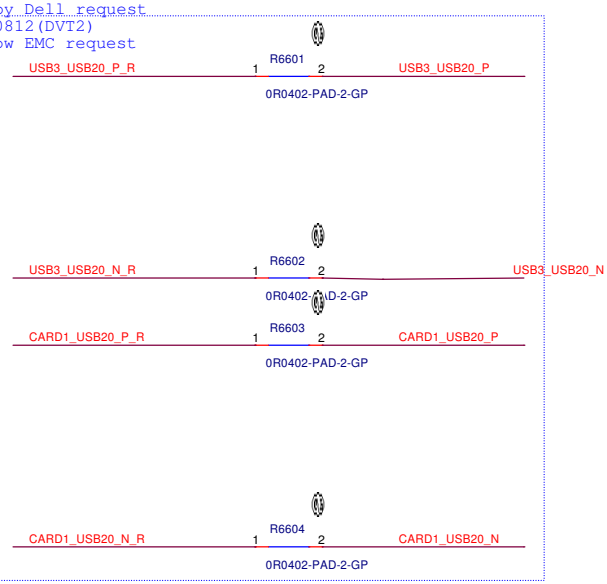
USB Part3 USB3.0

USB Part3 USB2.0

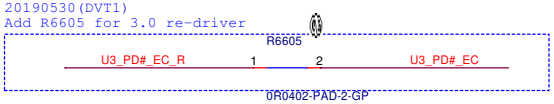
Card Reader

20190321(EVT)
Add G6601

20190425(EVT)
Add by Dell request
20190812(DVT2)
follow EMC request



20190530(DVT1)
Add R6605 for 3.0 re-driver



Follow REDHAWK

<Core Design>

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Title: IO Board Conn (USB/AUDIO)

Size: A3 | Document Number: Pinehills 13" WHL-U | Rev: X02

Date: Monday, September 23, 2019 | Sheet 66 of 106

Main Func = HALL SENSOR

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Lid_Wake

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

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Main Func = Debug

Follow Jedi 15

ESPI_CLK 18,24

HOST_DEBUG_TX 24

UART_2_CTXD_DRXD 20

UART_2_CRXD_DTXD 20

ESPI_RESET# 18,24

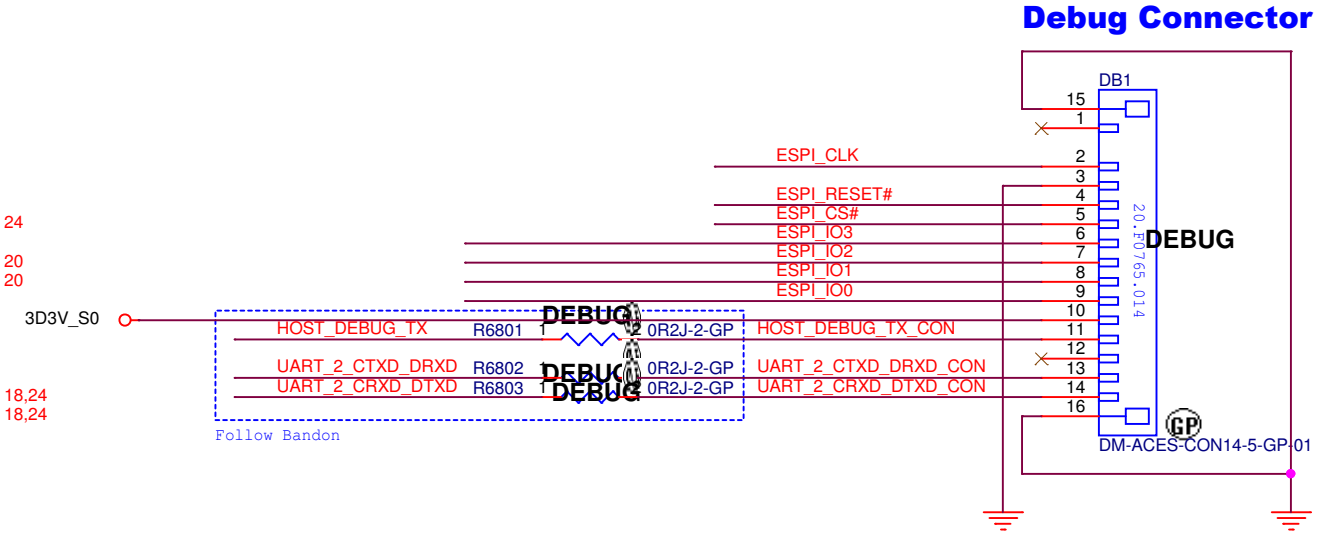
ESPI_CS# 18,24

18,24 ESPI_IO[3..0]

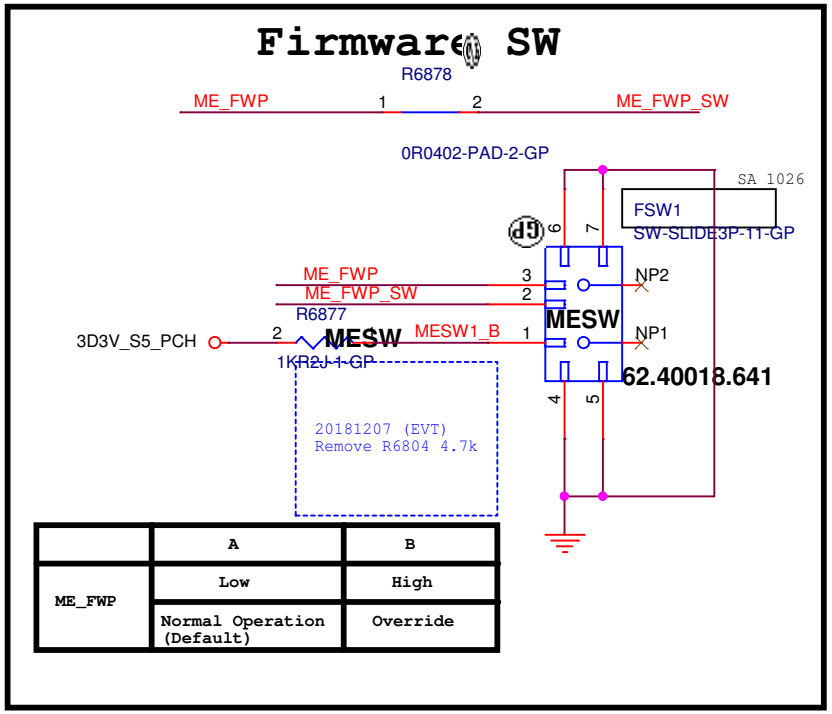
ME_FWP 24

ME_FWP_SW 19

Debug Connector



EE Note:
Use ZZ.F0765.01401 DUMMY PAD for MP



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

https://vinafix.com

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

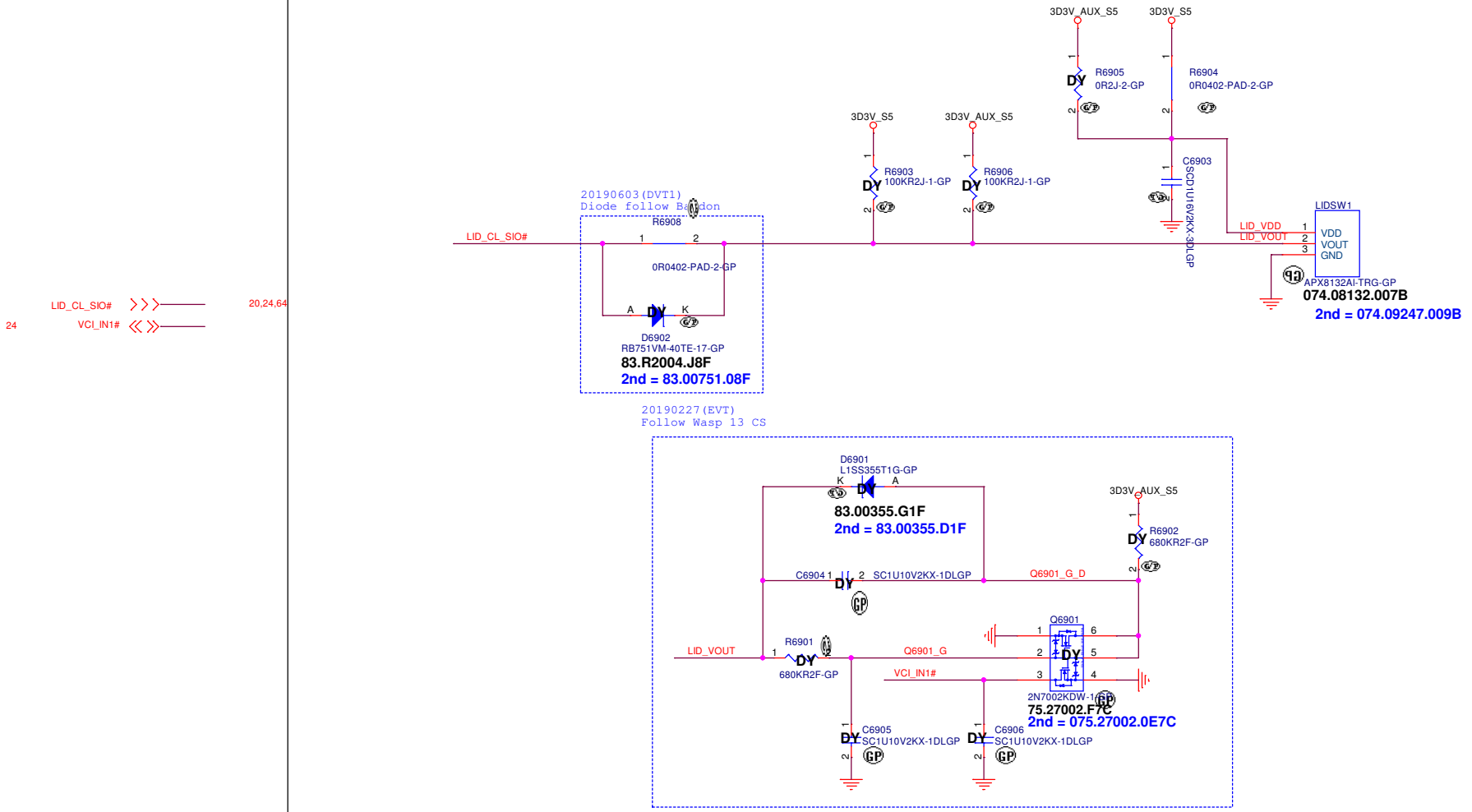
Title: *Dubug connector*

Size	Document Number	Rev
A4	*Pinehills 13" WHL-U*	*X02*

Date: Monday, September 23, 2019 Sheet 68 of 106

LID sensor for MLK

Follow WASP 13



LID_CL_SIO# 20,24,64

24 VCI_IN1#

<Core Design>

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Title: Reserved

Size	Document Number	Rev
A3	Pinehills 13" WHL-U	X02

Date: Monday, September 23, 2019 Sheet 69 of 106

Main Func = Free Fall Sensor

Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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Title: (Reserved)

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

Date: Monday, September 23, 2019 | Sheet 70 of 106

Main Func = Thunderbolt

For displayport function at dead battery condition

Follow Pinehills KBL (Bucky)

DisplayPort Source

4 DP2_DDI_TX_P0
4 DP2_DDI_TX_N0
4 DP2_DDI_TX_P1
4 DP2_DDI_TX_N1
4 DP2_DDI_TX_P2
4 DP2_DDI_TX_N2
4 DP2_DDI_TX_P3
4 DP2_DDI_TX_N3

USB3.0 TYPEC CONNECTOR

73 USB1_SSRX_C_P1
73 USB1_SSRX_C_N1
73 USB1_SSRX_C_P2
73 USB1_SSRX_C_N2

73 USB1_SSTX_C_P1
73 USB1_SSTX_C_N1
73 USB1_SSTX_C_P2
73 USB1_SSTX_C_N2

USB HOST

USB1_USB30_TX_N
USB1_USB30_TX_P
USB1_USB30_RX_N
USB1_USB30_RX_P

16,72 USB1_USB20_P
16,72 USB1_USB20_N

DisplayPort HPD

4,72 CPU_DP_HPD_R

4 DP2_AUX_CPU_P
4 DP2_AUX_CPU_N

TypeC CC

72 CCG5_SBU1
72 CCG5_SBU2

72,73 USB1_SBU1
72,73 USB1_SBU2

MUX I2C

72 CCG5_I2C_SCL_MUX
72 CCG5_I2C_SDA_MUX

3D3V_S5
R7102 0R0402-PAD-2-GP
3D3V_MUX
SCD1U16V2KX-3DLGP
TYPEC

R7103 10KR2J-3-GP DY
R7104 4K7R2J-2-GP DY
CAD_SNK
HPDIN

R7123 0R0402-PAD-2-GP USB1_SBU1
R7124 0R0402-PAD-2-GP USB1_SBU2
USB1_SBU1_R
USB1_SBU2_R
R7125 0R2J-2-GP DY CCG5_SBU1
R7126 0R2J-2-GP DY CCG5_SBU2

20180623(DVT2)
Change P/N

U7101
TUSB546-DCIRNQR-1-GP
071.00546.M001
TypeC

VCC
HPDIN/DCI_CLK
CAD_SNK/DCI_DAT
I2C_EN
DP0P
DP0N
DP1P
DP1N
DP2P
DP2N
DP3P
DP3N
RX1P
RX1N
RX2P
RX2N
TX1P
TX1N
TX2P
TX2N
SSRXP
SSRXN
SSTXP
SSTXN
EQ0
EQ1
I2CEN
SBU1
SBU2
AUXP
AUXN
DPEQ0_A1
DPEQ1
SSEQ0_A0
SSEQ1
FLIP/SCL
CTL0/SDA
CTL1/HPDIN
GND

DisplayPort Source
USB HOST

R7108 100KR2F-L1-GP DP2_AUX_C_N
R7109 100KR2F-L1-GP DP2_AUX_C_P

C7101 C7115 SCD1U16V2KX-3DLGP DP2_AUX_CPU_P DP2_AUX_CPU_N
R7105 R7106 R7107 0R0402-PAD-2-GP
I2C_CLK_PD_MUX CCG5_I2C_SCL_MUX
I2C_DATA_PD_MUX MUX_HPD_PD CCG5_I2C_SDA_MUX CPU_DP_HPD_R

CCG5_I2C_SCL_MUX C7121 SC33P50V2JN-3DLGP
CCG5_I2C_SDA_MUX C7122 SC33P50V2JN-3DLGP

20190311(EVT)
Common Part

R7110 1KR2F-3-GP DY EQ0
R7111 1KR2F-3-GP DY EQ1
R7112 1KR2F-3-GP TypeC I2CEN
R7113 1KR2F-3-GP DY DPEQ1
R7114 1KR2F-3-GP DY DPEQ0_A1
R7115 1KR2F-3-GP DY SSEQ1
R7116 1KR2F-3-GP DY SSEQ0_A0
R7117 1KR2F-3-GP TypeC
R7118 1KR2F-3-GP TypeC
R7119 1KR2F-3-GP DY
R7101 1KR2F-3-GP TypeC
R7120 1KR2F-3-GP TypeC
R7121 1KR2F-3-GP TypeC
R7122 1KR2F-3-GP TypeC

FLIP POL	CTL0 AMSEL	CTL1 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

DCI	mode DCI	
23 CTL1/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode	DP Enable Pin GPIO mode Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

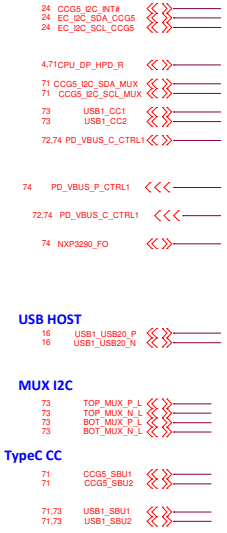
20190114(EVT)
CCG5 remove 2.0 MUX

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

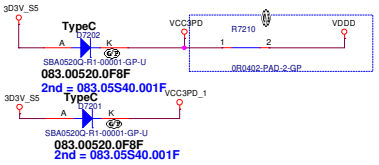
Title: EXT IO_(TBT(1/5)/MUX)
Size: A2
Document Number: Pinehills 13" WHL-U
Rev: X02
Date: Monday, September 23, 2019 Sheet 71 of 106

Main Func = CCG5

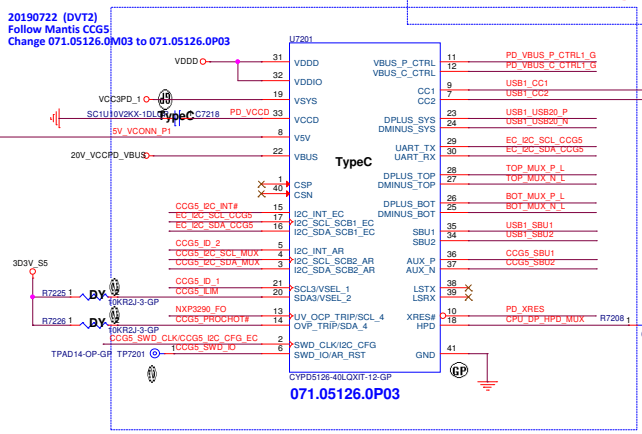


From System

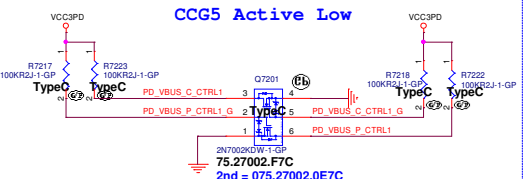
20190524 (DVT1)
For debattery

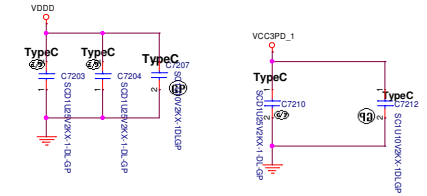


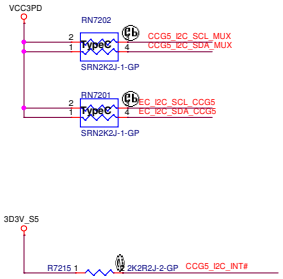
Follow Mantis CCG5

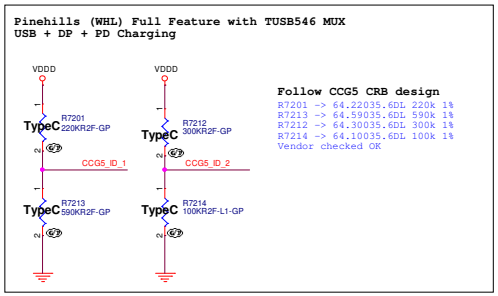


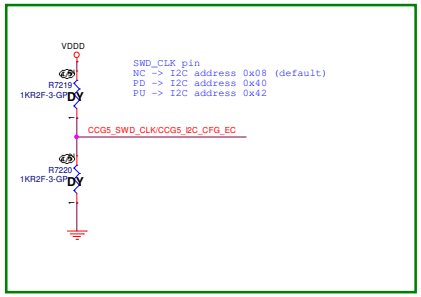
CCG5 Active Low

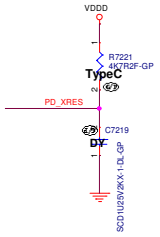












	CCG5_ID	R7201 R7212	R7213 R7214	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.12035.6DL (120K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

MOD_ID Settings

Mux MOD_ID Settings			
MUX	MOD_ID1	MOD_ID2	Description
Titan Ridge	L1	N/A	TBT Configuration
PS8802	L4	L0	PS8802 Equalizer config #1
PS8802	L4	L1 - L3	Reserved for PS8802 Equalizer config #2,3,4 reserved
ANX7443	L5	L0	ANX7443 Equalizer config #1
ANX7443	L5	L1 - L3	Reserved for ANX7443 Equalizer config #2,3,4 reserved
TUSB546	L6	L0	TUSB546 Equalizer config #1
TUSB546	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved
TUSB544	L6	L4	TUSB544 Equalizer config #1
TUSB544	L6	L5 - L7	Reserved for TUSB544 Equalizer config #2,3,4 reserved

Voltage Levels
L0 = 0V
L1 = VDDD/8
L2 = 2*VDDD/8
L3 = 3*VDDD/8
L4 = 4*VDDD/8
L5 = 5*VDDD/8
L6 = 6*VDDD/8
L7 = 7*VDDD/8

<Core Design>

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Title: EXT IO (TBT(2/5)/PD)

Size: A2 | Document Number: Pinehills 13" WHL-U | Rev: X02

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Main Func = TYPEC MUX

USB3.0 TYPEC CONNECTOR

71 USB1_SSRX_C_P1
71 USB1_SSRX_C_N1
71 USB1_SSRX_C_P2
71 USB1_SSRX_C_N2
71 USB1_SSTX_C_P1
71 USB1_SSTX_C_N1
71 USB1_SSTX_C_P2
71 USB1_SSTX_C_N2

TypeC CC

71,72 USB1_SBU1
71,72 USB1_SBU2
72 USB1_CC1
72 USB1_CC2

72 TOP_MUX_P_L
72 TOP_MUX_N_L
72 BOT_MUX_P_L
72 BOT_MUX_N_L

20V_VCCPD_VBUS — 3A

20180703 (DVT2) Remove C7301

C7302 C7303 C7304 C7305 — TYPEC — 0.22UF-25V-20%-Y5V-1-GP

remove C7306 follow bucky

Vendor check CAP modify 20171013

Follow Pinehills KBL (Bucky)

20V_VCCPD_VBUS

USB1_SSTX_CON_P1 / USB1_SSTX_CON_N1 / USB1_CC1 / TOP_MUX_P / TOP_MUX_N / USB1_SBU1 / USB1_SSRX_CON_N2 / USB1_SSRX_CON_P2

USB1 — GND, SSTXP1, SSTXN1, VBUS#A4, CC1, DP1, DN1, RFU1, VBUS#A9, SSRXN2, SSRXP2, GND, NP1, NP2, GROUND, CHASSIS#13–#22 — TYPEC

R7301 2MR2F-GP — TYPEC

ED7301 AZ4024-01L-R7G-GP — TypeC

083.04024.0AA1

2nd = 075.03524.0077

SKT-USB34-21-GP-U1

022.10005.M021

2nd = 022.10005.M022

R7302 2MR2F-GP — TYPEC

20V_VCCPD_VBUS

USB1_SSTX_C_P1 — C7307 1 — USB1_SSTX_CMC_P1 — R7304 1 — 2 0R0402-PAD-2-GP — USB1_SSTX_CON_P1

SCD1U16V2KX-3DLGP — TYPEC

20190305(EVT) Change 0.33uF 0402 Follow R015

USB1_SSTX_C_N1 — C7308 1 — USB1_SSTX_CMC_N1 — R7307 1 — 2 0R0402-PAD-2-GP — USB1_SSTX_CON_N1

SCD1U16V2KX-3DLGP — TYPEC

USB1_SSRX_C_P1 — C7309 1 — USB1_SSRX_CMC_P1 — R7308 1 — 2 0R0402-PAD-2-GP — USB1_SSRX_CON_P1

SCD33U6D3V2KX-3-GP — TypeC

R7315 220KR2F-GP

USB1_SSRX_C_N1 — C7310 1 — USB1_SSRX_CMC_N1 — R7310 1 — 2 0R0402-PAD-2-GP — USB1_SSRX_CON_N1

SCD33U6D3V2KX-3-GP — TypeC

R7316 220KR2F-GP

USB1_SSRX_C_P2 — C7311 1 — USB1_SSRX_CMC_P2 — R7311 1 — 2 0R0402-PAD-2-GP — USB1_SSRX_CON_P2

SCD33U6D3V2KX-3-GP — TypeC

R7317 220KR2F-GP

USB1_SSRX_C_N2 — C7312 1 — USB1_SSRX_CMC_N2 — R7312 1 — 2 0R0402-PAD-2-GP — USB1_SSRX_CON_N2

SCD33U6D3V2KX-3-GP — TypeC

R7318 220KR2F-GP

USB1_SSTX_C_P2 — C7313 1 — USB1_SSTX_CMC_P2 — R7313 1 — 2 0R0402-PAD-2-GP — USB1_SSTX_CON_P2

SCD1U16V2KX-3DLGP — TYPEC

USB1_SSTX_C_N2 — C7314 1 — USB1_SSTX_CMC_N2 — R7314 1 — 2 0R0402-PAD-2-GP — USB1_SSTX_CON_N2

SCD1U16V2KX-3DLGP — TYPEC

ED7310 — TypeC — L0SESDL5V0NA-4-GP

USB1_SSTX_CON_N1 / USB1_SSTX_CON_P1 / USB1_SSRX_CON_N1 / USB1_SSRX_CON_P1

075.00550.0071

2nd = 075.PUSB3.0073

ED7302 — TypeC — L0SESDL5V0NA-4-GP

USB1_SSRX_CON_P2 / USB1_SSRX_CON_N2 / USB1_SSTX_CON_P2 / USB1_SSTX_CON_N2

075.00550.0071

2nd = 075.PUSB3.0073

20180801 (DVT2) Change by EMC team confirm Remove co-lay R7303, R7305

TOP_MUX_N_L / TOP_MUX_P_L — EL7302 — TypeC — DLW05BSN900HY2D-GP — TOP_MUX_N / TOP_MUX_P

068.09002.2001

2nd = 68.02002.061

20180801 (DVT2) Change by EMC team confirm Remove co-lay R7306, R7309

BOT_MUX_N_L / BOT_MUX_P_L — EL7301 — TypeC — DLW05BSN900HY2D-GP — BOT_MUX_N / BOT_MUX_P

068.09002.2001

2nd = 68.02002.061

ED7303 — TypeC — L0SESDL5V0NA-4-GP

TOP_MUX_P / TOP_MUX_N / BOT_MUX_N / BOT_MUX_P

075.00550.0071

2nd = 075.PUSB3.0073

ED7305 — DY — AZ5315-02F-GP — USB1_CC1 / USB1_CC2

ED7309 — DY — AZ5315-02F-GP — USB1_SBU1 / USB1_SBU2

83.05315.0A0

83.05315.0A0

<Core Design>

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Title: EXT IO_(TBT(3/5)/TYPEC CON)

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Follow Bucky

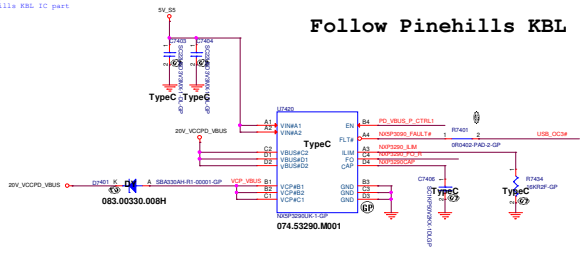
P/N: 071.17030.000U
C TYPE-C PD CTRL SN1703018ZQZR BGA 96P

GPIO0 (USB_OC3#): default HI Set open drain to meet unplug , GPIO is high condition
GPIO1 (PD_OVP_TRIP_P1): default LO OK
GPIO4 (DP1_HPD_CPU): default LO OK
GPIO6 (PD_VBUS_C_CTRL1): default LO OK
GPIO7 (VBUS_P_CTRL): default LO OK

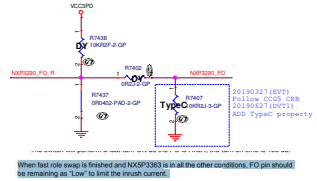
PD_VBUS_C_CTRL1 72
72 NXP3290_FO

20190320(EVT)
Follow Pinehills KBL IC part

Follow Pinehills KBL

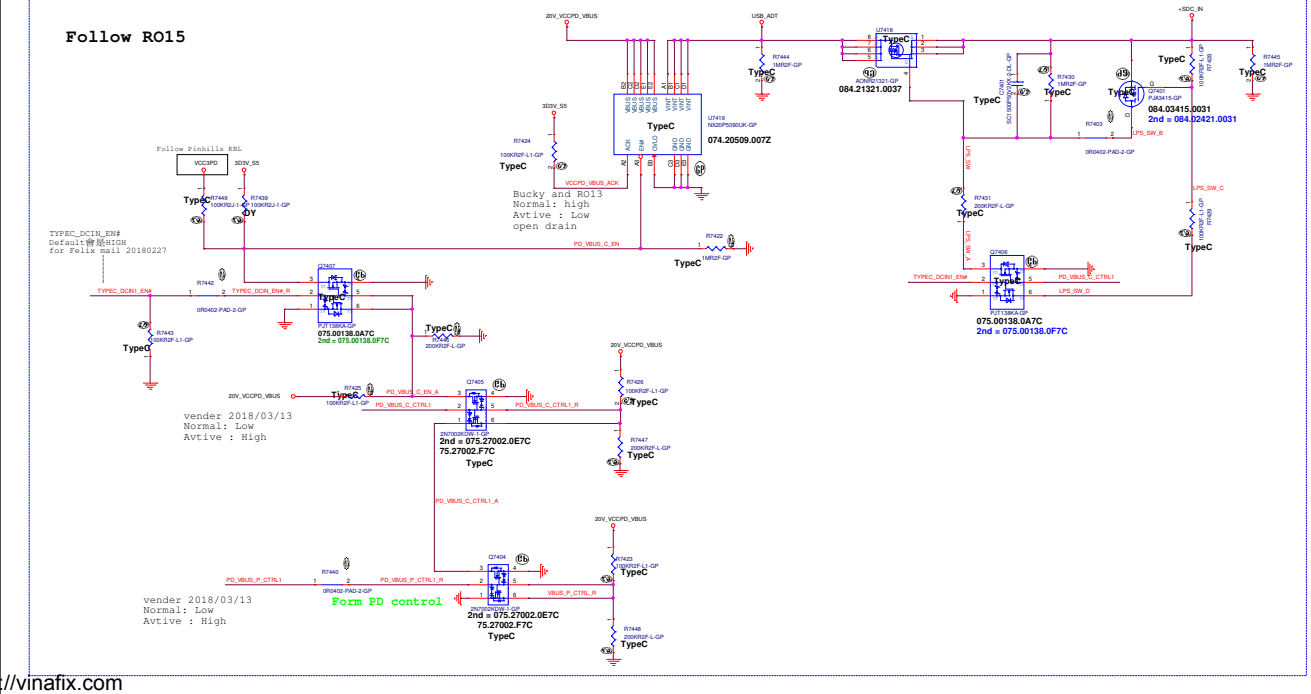


Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OCP}	over current protection current	V_{VCPA} = 4.0 to 5.5 V; T_{amb} = −40 °C to +85 °C; see Figure 11.				
		R_{ILIM} = 140 kΩ	330	400	465	mA
		R_{ILIM} = 100 kΩ	480	550	625	mA
		R_{ILIM} = 54 kΩ	915	1013	1107	mA
		R_{ILIM} = 33 kΩ	1505	1650	1780	mA
		R_{ILIM} = 24.5 kΩ	2024	2220	2398	mA
		R_{ILIM} = 20 kΩ	2450	2640	2820	mA
		R_{ILIM} = 16 kΩ	3100	3300	3531	mA
		ILIM shorted to VIN	168	210	273	mA



20180427(DVT1)
Follow RO15 design

Follow RO15



16 USB_OC3#
72 PD_VBUS_P_CTRL1
44 VCCPD_VBUS_ACK
24 TYPEC_DCIN1_EN#

https://vinafix.com

+3D3V_VDD_DCIN

DC_IN_OK invert

Barrel Adapter Piug-in Detect

Barrel Adapter Piug-in Disable S4

PD_VBUS_C_CTRL1 invert

<Core Design>

DELL Wistron Corporation
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Title: EXT IO (TBT(4/5)/LPS)
Size: A1 | Document Number: Pinehills 13" WHL-U | Rev: X02
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Main Func = Thunderbolt

(Blanking)

<Core Design>

Wistron Corporation
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Title

(Reserved)

Size	Document Number	Rev
A4	*Pinehills 13" WHL-U*	*X02*

Date: Monday, September 23, 2019 Sheet 75 of 106

Main Func = dGPU

(Blanking)

<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

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Main Func = dGPU

(Blanking)

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

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Main Func = dGPU

(Blanking)

<Core Design>

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Title
(Reserved)

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

Date: Monday, September 23, 2019 Sheet 78 of 106

Main Func = dGPU

(Blanking)

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

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Main Func = dGPU

(Blanking)

<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

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Main Func = dGPU

(Blanking)

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

Date: Monday, September 23, 2019 Sheet 81 of 106

Main Func = dGPU

(Blanking)

<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

Date: Monday, September 23, 2019 Sheet 82 of 106

Main Func = dGPU

(Blanking)

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

Date: Monday, September 23, 2019 Sheet 83 of 106

Main Func = dGPU

(Blanking)

<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

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Main Func = dGFX_CORE

(Blanking)

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	*Pinehills 13" WHL-U*	*X02*

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Main Func = dGPU

(Blanking)

<Core Design>

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Title: (Reserved)

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

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<Core Design>

Wistron Corporation
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Title
GPU (RSVD)

Size: A3
Document Number: Pinehills 13" WHL-U
Rev: X02

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<Core Design>

Wistron Corporation
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Title

UNUSED PARTS_(RSVD)

Size	Document Number	Rev
A	***Pinehills 13" WHL-U***	***X02***

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Main Func = UnusedParts

ZZ.SCREW.W91

H1 HOLE233R154-GP, H2 HOLE233R154-GP, H3 HOLE233R154-GP, H4 HOLE233R154-GP

ZZ.SCREW.W91 ZZ.SCREW.W91 ZZ.SCREW.W91 ZZ.SCREW.W91

ZZ.00PAD.D11

H5 HOLE256R115-GP, H6 HOLE256R115-GP

ZZ.00PAD.D11 ZZ.00PAD.D11

ZZ.00PAD.7F1

H7 HOLE335R178-GP, H8 HOLE335R178-GP, H9 HOLE335R178-GP, H10 HOLE335R178-GP, H11 HOLE335R178-GP

ZZ.00PAD.7F1 ZZ.00PAD.7F1 ZZ.00PAD.7F1 ZZ.00PAD.7F1 ZZ.00PAD.7F1

HS1 STF237R113H86-GP, HS2 STF237R113H62-4-GP

434.07K0E.0001 34.4SE26.001

20190805(DVT2)
DY SPR1 by EMC team

EMI STOP

SPR1
SPRING-12-GP-U1
DY
34.41Y19.001

20181212 (EVT)
Remove SPR2

ZZ.00PAD.921

H12 HOLE237R95-GP, H13 HOLE237R95-GP, H14 HOLE237R95-GP

ZZ.00PAD.921 ZZ.00PAD.921 ZZ.00PAD.921

3D3V_S0

EC8918 EC8919 EC8920 EC8921 EC8926
EC8922 EC8923 EC8924 EC8925 EC8950

5V_S0

EC8927 EC8928 EC8929 EC8930 EC8954 EC8953
EC8931 EC8932 EC8952 EC8951

20190411(EVT)
EMI remove EC8973~EC8982

20190805(DVT2)
DY EC8908~EC8911 by EMC team
DY EC8915~EC8917 by EMC team
DY EC8937~EC8939 by EMC team

DCBATOUT

EC8908 EC8909 EC8910 EC8911 EC8915 EC8916 EC8917 EC8937 EC8938 EC8939

3D3V_S5

EC8933 EC8934 EC8935 EC8936 EC8955 EC8957 EC8956 EC8958 EC8959 EC8960

5V_S5

EC8912 EC8913 EC8914 EC8963 EC8961 EC8962 EC8964 EC8966 EC8965 EC8967

20190527 (DVT1)
Add EC8973, EC8974 by EMC team

PWR_DCBATOUT_VCCGTA

EC8973 EC8974 EC8977 EC8978 EC8979 EC8980

DCBATOUT

20190805(DVT2)
DY EC8981~EC8985 by EMC team

EC8981 EC8982 EC8983 EC8984 EC8985

20190617(DVT1)
Add EC8977~EC8985 by EMC team
20190805(DVT2)
DY EC8978 by EMC team
Change EC8973 EC8974 EC8977 EC8979 EC8980 to 1000p by EMC Team

20190527 (DVT1)
Add EC8975, EC8976 by EMC team

+SDC_IN

EC8975 EC8976

BT+

EC8971 EC8968 EC8969 EC8970 EC8972

1D2V_S3

EC8940 EC8942 EC8943 EC8944 EC8941 EC8945 EC8949 EC8946 EC8947 EC8948

SSID = EMI

Mind the voltage rating of the caps.

SSID = RF

1D2V_S3

FC8920 FC8921 FC8922

Layout Placement Request

X01 20161230B change

DCBATOUT

FC8927 FC8928 FC8929

1D2V_S3

FC8933 FC8934 FC8935

Layout Placement Request

X01 20161230B change

+SDC_IN

FC8961

Layout Placement Request

20190527 (DVT1)
Remove FC8960, FC8964 by EMC team

1V_CPU_CORE

FC8967 FC8970

1V_VCCSA

FC8971

1V_VCCIO

FC8972

SB 0323

Layout Placement Request

https://vinafix.com

<Core Design>

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Title: UNUSED PARTS/EMI Capacitors

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<Core Design>

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Title: M-BIST

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SSID = TPM

(Blanking)

<Core Design>

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Title: (Reserved)

Size: A3 | Document Number: Pinehills 13" WHL-U | Rev: X02

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<Core Design>

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Title: *Finger Print*

Size: A3 | Document Number: *Pinehills 13" WHL-U* | Rev: *X02*

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(Blanking)

<Core Design>

Wistron Corporation
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Title: *(Reserved)*

Size: A3 | Document Number: *Pinehills 13" WHL-U* | Rev: *X02*

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(Blanking)

<Core Design>

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Title: *(Reserved)*

Size: A3 | Document Number: *Pinehills 13" WHL-U* | Rev: *X02*

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(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size: A3 | Document Number: *Pinehills 13" WHL-U* | Rev: *X02*

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(Blanking)

<Core Design>

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Title: *(Reserved)*

Size: A3 | Document Number: *Pinehills 13" WHL-U* | Rev: *X02*

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(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *LVDS_Switch*

Size: A3 | Document Number: Pinehills 13" WHL-U | Rev: X02

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(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT_Switch*

Size: A3 | Document Number: Pinehills 13" WHL-U | Rev: X02

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Main Func = Debug (MIPI)

20181126 (EVT)
Follow Dell EE Andelon suggestion
Only use 12 XDP signal

Follow Bandon Modify

CFG3 6,15

ITP_PMODE 6

3 PCH_JTAG_TCK
3 CPU_JTAG_PRDY#
3 CPU_JTAG_PREQ#
3 CPU_JTAG_TRST#
3 CPU_JTAG_TCK
3 CPU_JTAG_TDI
3 CPU_JTAG_TDO
3 CPU_JTAG_TMS
SYS_RESET# 17
18 SPI_WP_CPU
PLTRST#_CPU 17,24,31,61,63
17,55 PM_RSMRST#

https://vinafix.com

CFG3 1 — R9928 1K5R2F-2-GP — XDP_PRSNT_PIN1

CPU_JTAG_PREQ#
CPU_JTAG_PRDY#

1D0V_S5_XDP — R9907 0R3J-0-U-GP — 1D0V_S5_XDP

XDP1 (PAD-60P-GP)

EE Note:
Use ZZ.00PAD.Q81 DUMMY PAD for MP.

1D0V_S5_XDP — C9902 SCD1U16V2KX-3DLGP

PM_RSMRST# — R9920 1KR2F-3-GP — XDP_RSMRST#

R9903 0R3J-0-U-GP — 1D05V_CPU_XDP_AB

PCH_JTAG_TCK
CPU_JTAG_TCK

XDP_ITP_PMODE
XDP_DBRESET#
CPU_JTAG_TDO
XDP_JTAG_TRST#
CPU_JTAG_TDI
CPU_JTAG_TMS
XDP_PRSNT

D9901 RB751VM-40TE-17-GP
83.R2004.J8F
2nd = 83.00751.08F

CPU_JTAG_TRST# — R9901 0R2J-2-GP — XDP_JTAG_TRST#

SPI_WP_CPU_R — R9923 1KR2F-3-GP — SPI_WP_CPU

XDP_DBRESET# — R9913 0R2J-2-GP — SYS_RESET#

C9901 SCD1U16V2KX-3DLGP

1D0V_S5_XDP — R9929 1K5R2F-2-GP

ITP_PMODE — R9917 0R2J-2-GP — XDP_ITP_PMODE

PLTRST#_CPU — R9918 0R2J-2-GP

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Title: Debug (XDP debug)

Size	Document Number	Rev
A4	Pinehills 13" WHL-U	X02

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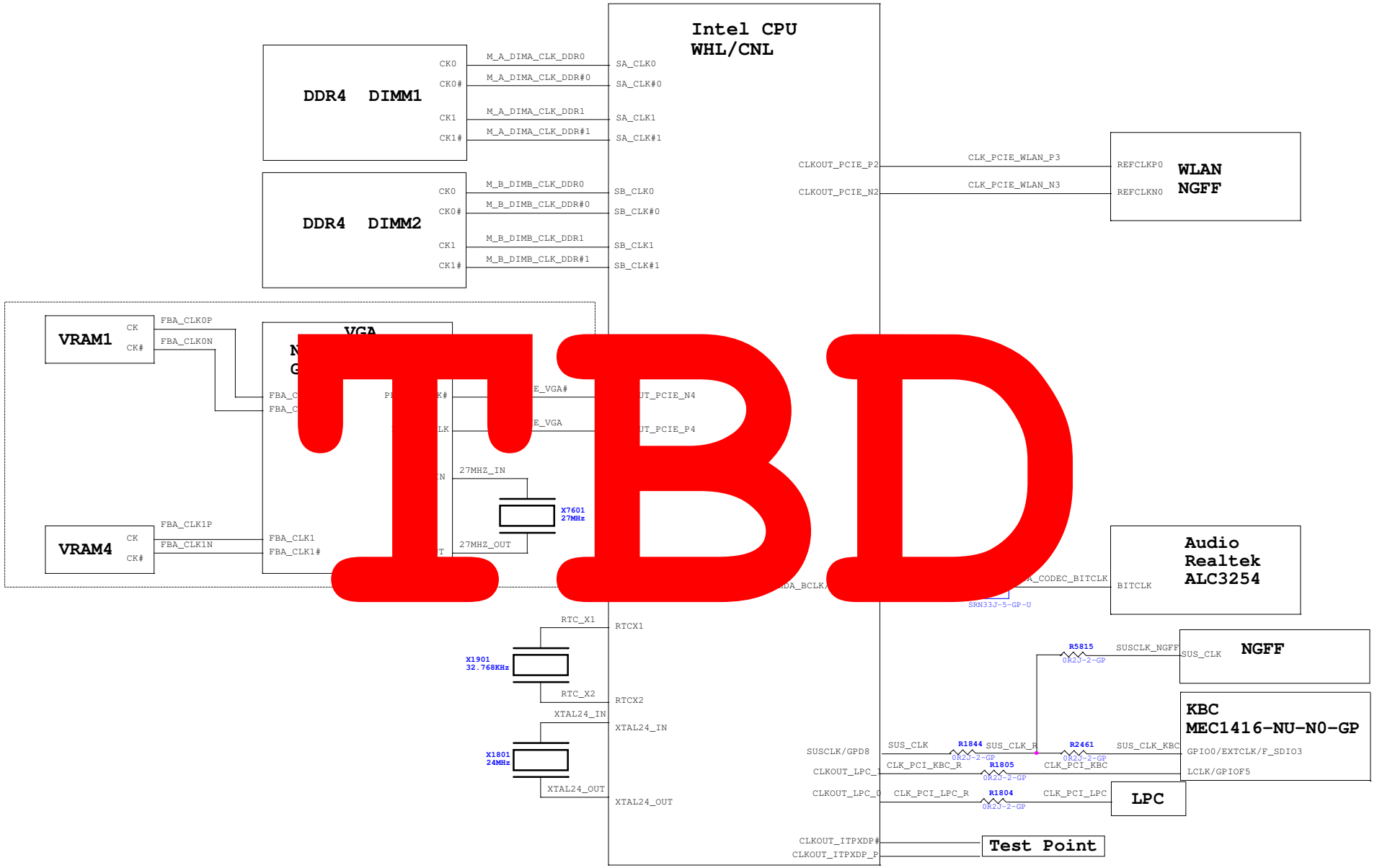
CLK Block Diagram



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Title: CLK Block Diagram
Size: A2
Document Number: Pinehills 13" WHL-U
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Change notes –

DATE	VERSON	DATE	Page	Modify List	OWNER

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Title: *Change History*

Size	Document Number	Rev
A3	*Pinehills 13" WHL-U*	*X02*

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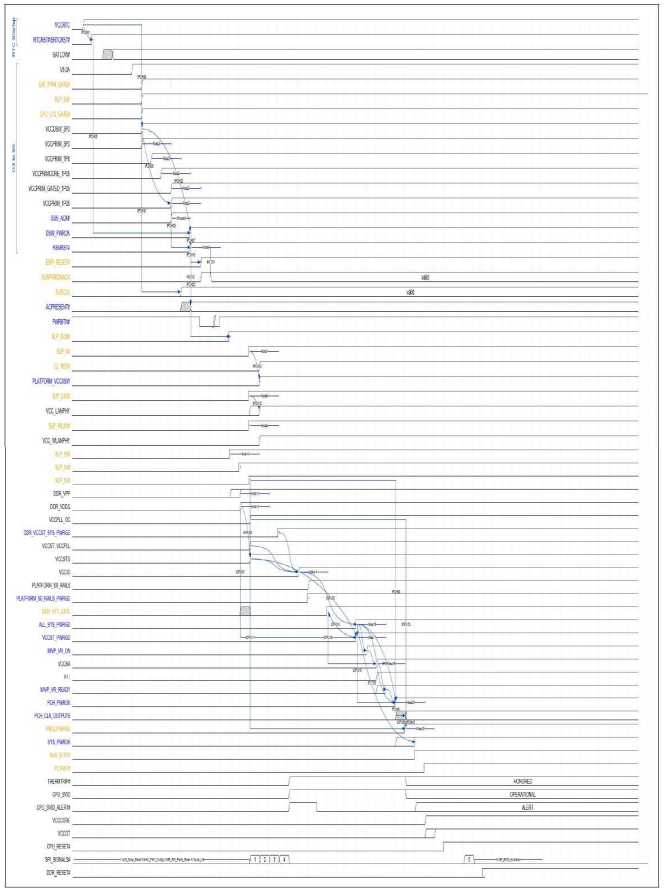
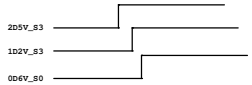
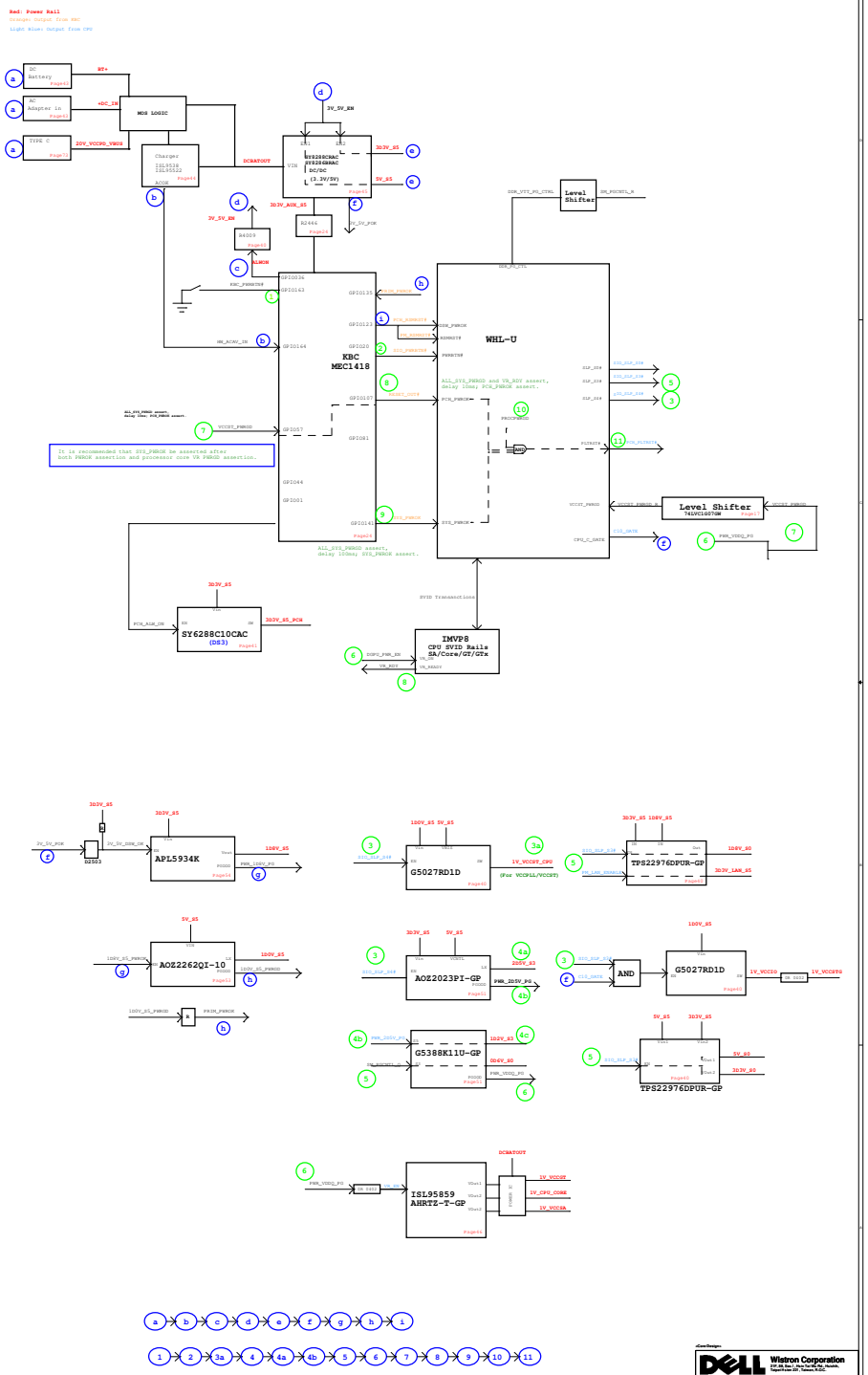
WHL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]

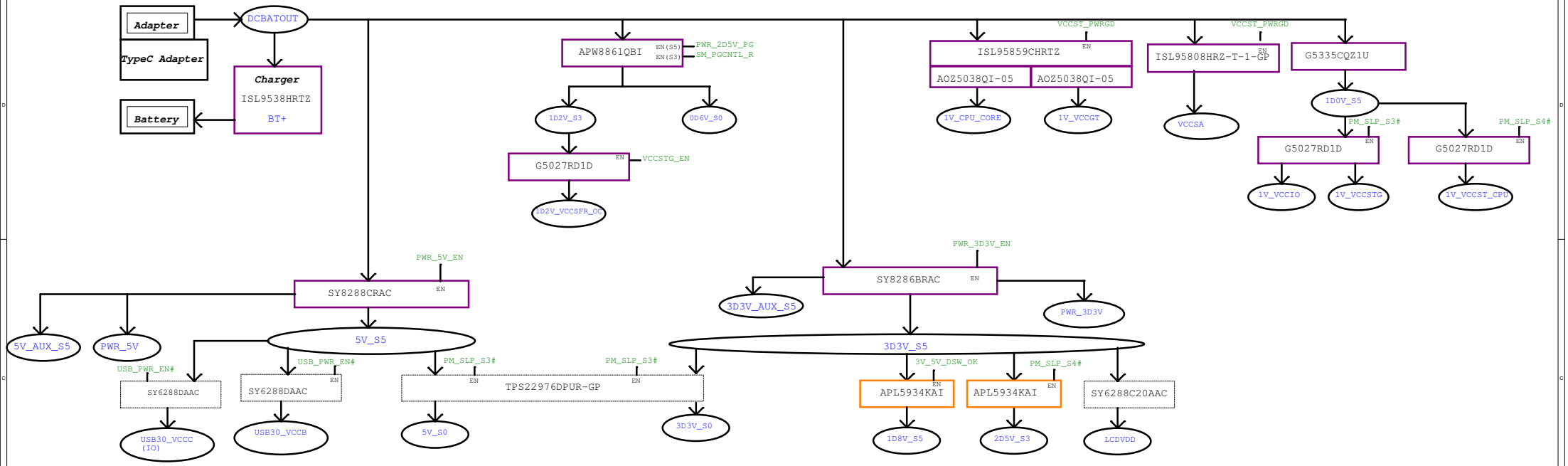


For DDR4 power sequence



WhiskyLake POWER UP SEQUENCE DIAGRAM





Power Shape

Regulator	LDO	Switch

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Title		
Power Block Diagram		
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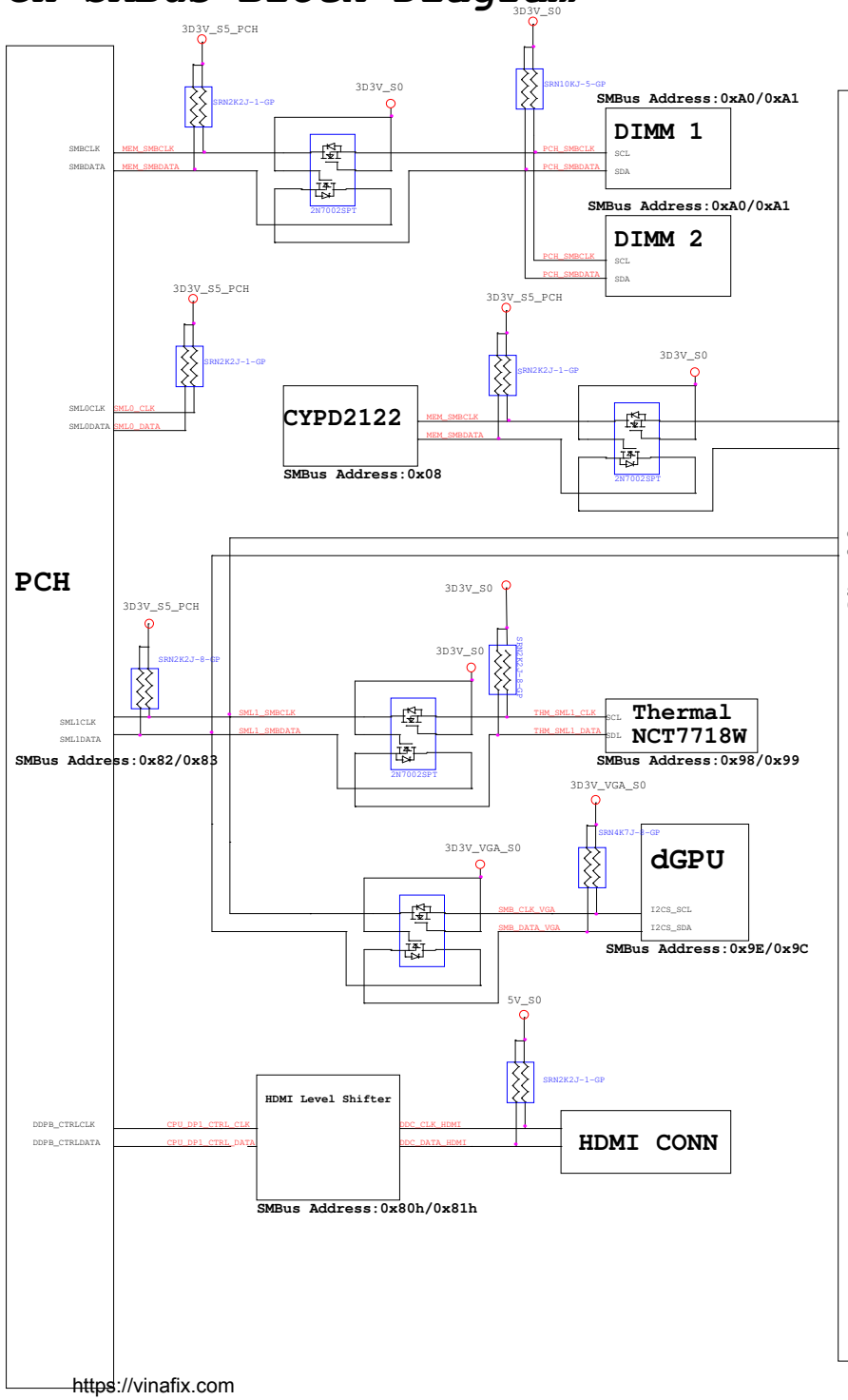
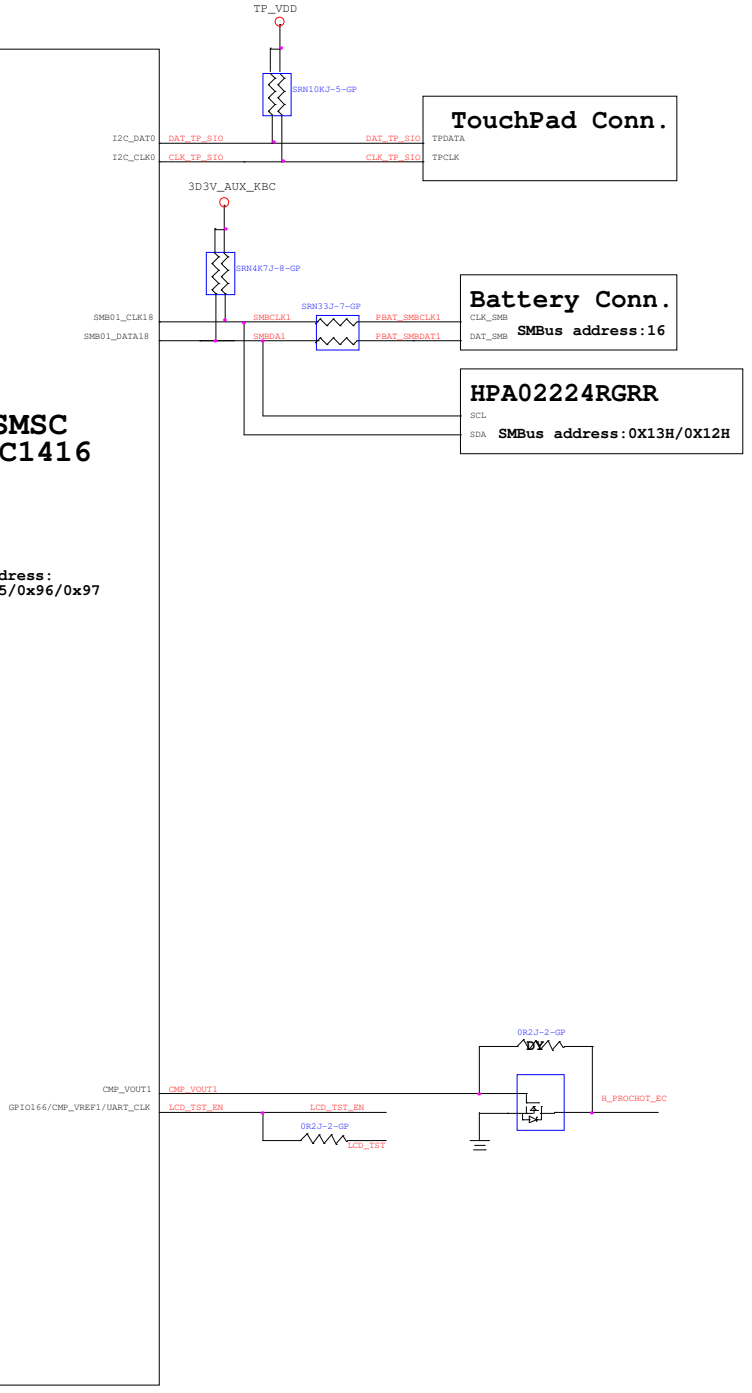
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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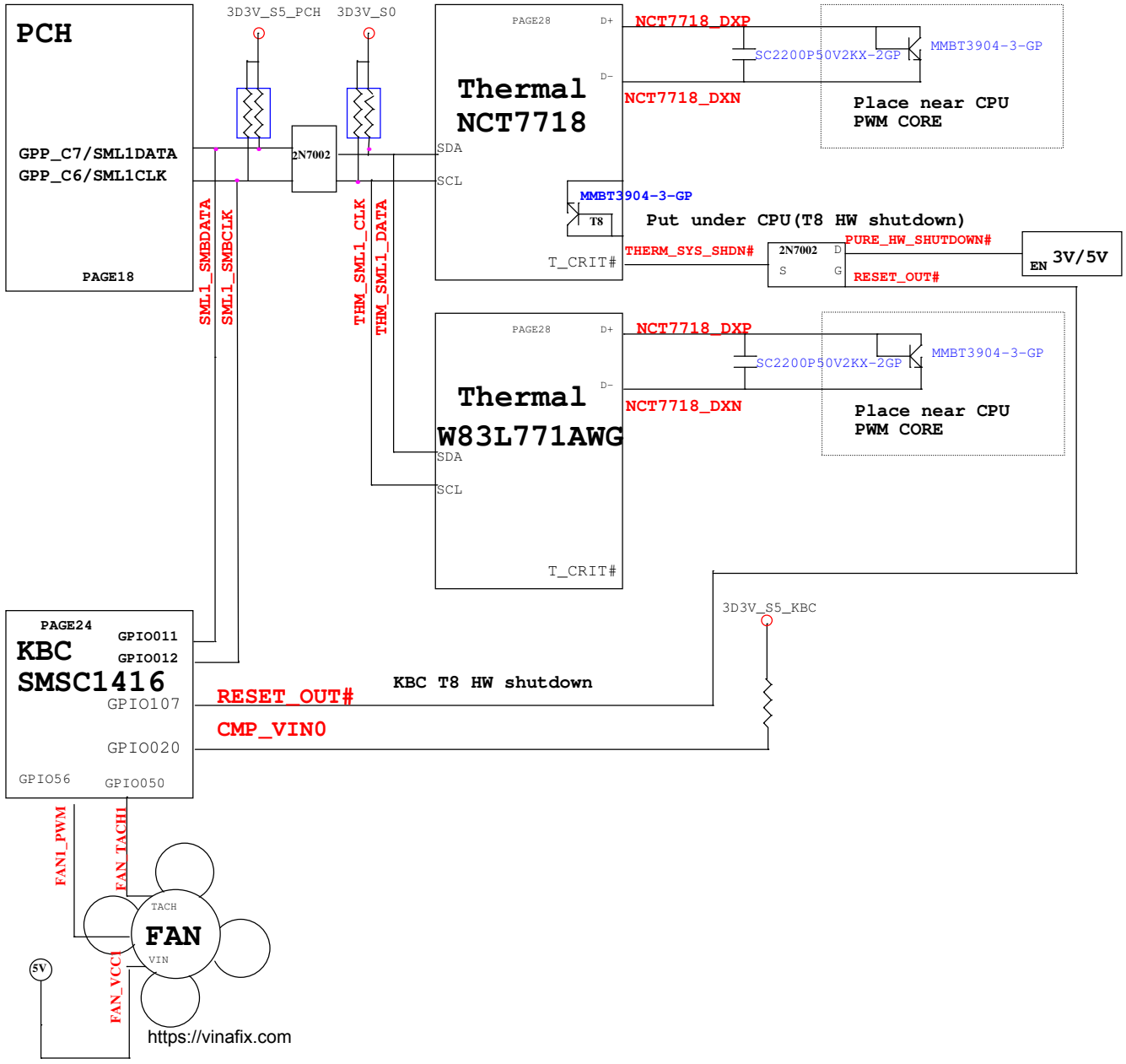
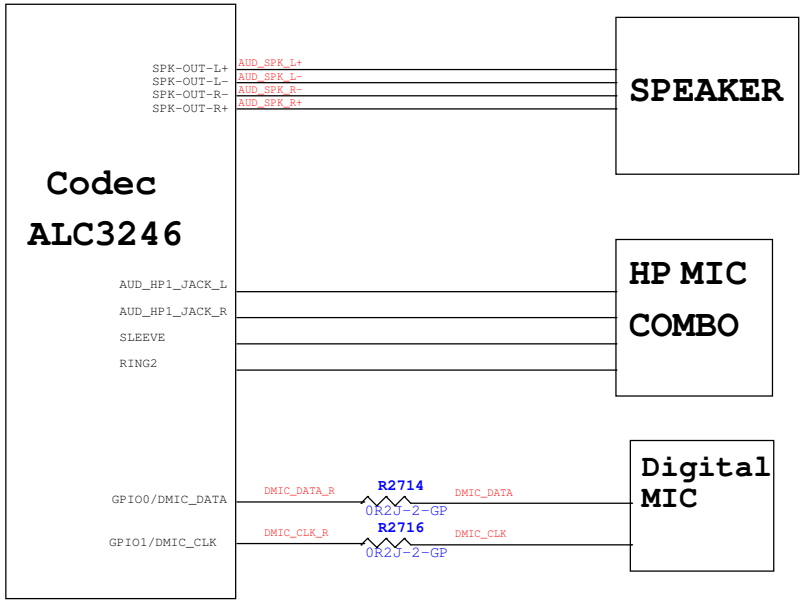
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Pinehills 13" WHL-U | Rev: X02

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