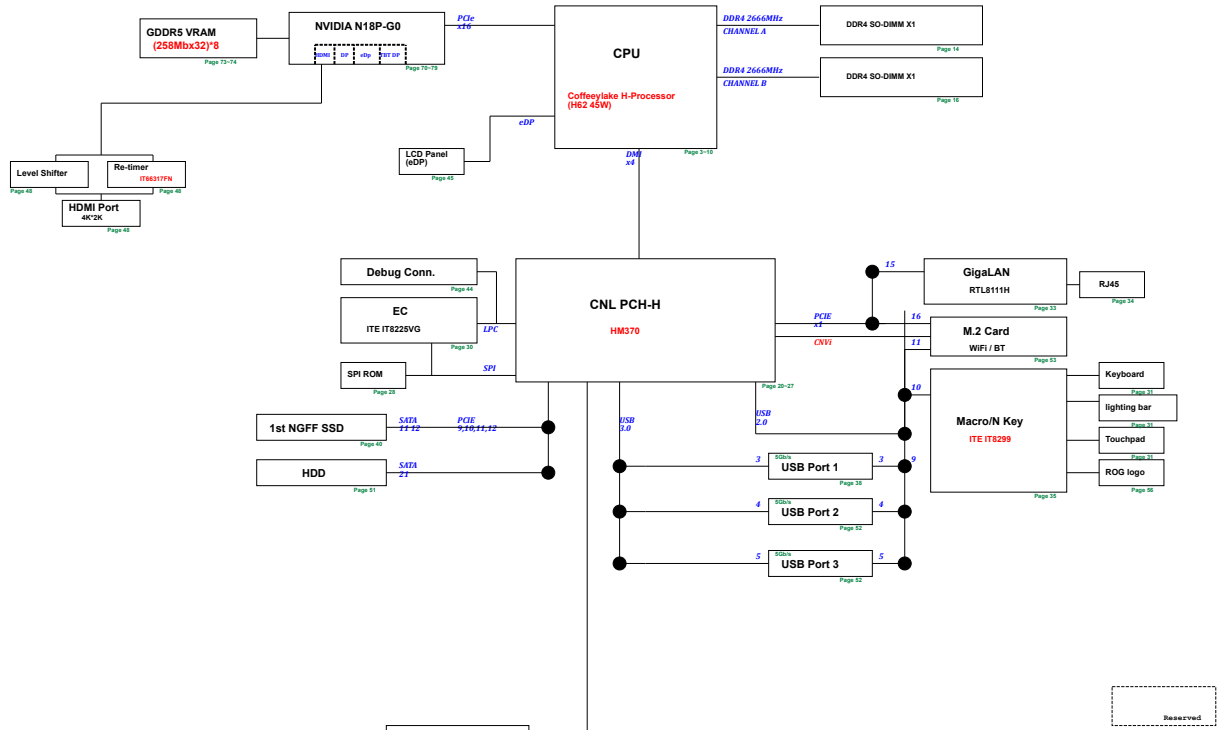
G531GT Block Diagram

Coffeelake H Platform



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Power

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Project Name	G711GW
Rev	0.1
Title :	Block Diagram
Size	D
Dept.	ASUSTeK COMPUTER
Engineer	Gaming RD
Date	Wednesday, April 17, 2019
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PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	BC1B#	Native	BC_1B#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_XBCH21_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_CHARGE_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GP1	GP1	PCH_GPP_A12			
GPP_A13	SUSWARN#	Native	ME_BusPwrDnAck		PD 10K(8)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GP2	GP1	GPP_A16			
GPP_A17	GP1	GP1	(N.C)			
GPP_A18	GP1	GP1	(N.C)			
GPP_A19	GP1	GP1	(N.C)			
GPP_A20	GP1	GP1	(N.C)			
GPP_A21	GP1	GP1	(N.C)			
GPP_A22	GP1	GP1	(N.C)			
GPP_A23	GP1	GP1	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GP1	GP1	(N.C)			
GPP_B3	GP1	GP1	(N.C)			
GPP_B4	GP1	GP1	(N.C)			
GPP_B5	GP1	Native	CLK_FBCA_REQ0# _X1		PU 10K	+3VSUS
GPP_B6	GP1	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GP1	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GP1	Native	CLKREQ3_WLAN# _X1		PU 10K	+3VSUS
GPP_B9	GP1	Native	CLKREQ4_CLKM# _X1		PU 10K	+3VSUS
GPP_B10	GP1	Native	CLKREQ5_TBT# _X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MSWY_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPP914	PD		
GPP_B15	GP1	Native	GSPI0_CS#			
GPP_B16	GP1	Native	GSPI0_CLK			
GPP_B17	GP1	Native	GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPP918	PD		
GPP_B19	GP1	GPO	PCH_GPP919/WT_ON_PCH		PD 10K(8)	
GPP_B20	GP1	GPO	PCH_GPP920/NV_GPU_EVENT#		PU 10K(8)	+3VSUS
GPP_B21	GP1	GP1	PCH_GPP921/NV_GC6_FB_EN		PD 10K(8)	+3VS
GPP_B22	GPO	Strap	PCH_GPP922	PD		
GPP_B23	GPO	GPO	SMLIALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GP1	Strap	PCH_GPP02			
GPP_C3	SMLOCLK	Native	SMLO_CLK		PU 2.2K	+3VSUS
GPP_C4	SMLOSATA	Native	SMLO_DAT		PU 2.2K	+3VSUS
GPP_C5	GP0	Strap	PCH_GPP05	PD		
GPP_C6	GP1	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GP1	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GP1	GP1	PCH_GPPC8			
GPP_C9	GP1	GP1	PCH_GPPC9			
GPP_C10	GP1	GP1	PCH_GPPC10			
GPP_C11	GP1	GP1	PCH_GPPC11			
GPP_C12	GP1	GP1	DIMM_SEL0		PD 10K	
GPP_C13	GP1	GP1	DIMM_SEL1		PD 10K	
GPP_C14	GP1	GP1	DIMM_SEL2		PD 10K	
GPP_C15	GP1	GP1	BPC_ID		PD 10K	+3VSUS
GPP_C16	GP0	GPO	AOAC_WLANLED		PU 10K(8)	+3VSUS
GPP_C17	GP1	GPO	PCH_GPPC17		PU 10K(8)	+3VS
GPP_C18	GP1	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GP1	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GP1	GP1	PCH_GPPC20/DGPU_PWROK		PD 10K(8)	
GPP_C21	GP1	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GP1	GPO	PCH_GPPC22/DGPU_PWR_EN#		PD 1K	
GPP_C23	GP1	GP1	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GP1	GP1	CIO_PLUG_EVENT		PD 10K	+VCC3V3_EN
GPP_D1	GPO	GPO	GPIO_3_PCHCE_PWR		PD 10K	
GPP_D2	GP1	GP1	EXT_SMI#		PU 10K	+3VS
GPP_D3	GP1	GP1	EXT_SCI#		PU 10K	+3VS
GPP_D4	GP1	GP1	(N.C)			
GPP_D5	GP1	GP1	(N.C)			
GPP_D6	GP1	GP1	(N.C)			
GPP_D7	GP1	GPO	WLAN_ON#			
GPP_D8	GP1	GP1	(N.C)			
GPP_D9	GP1	Strap	PCH_ID0		PD 10K	
GPP_D10	GP1	Strap	PCH_ID1		PD 10K	
GPP_D11	GP1	Strap	TOUCHPAD_ID			
GPP_D12	GP1	Strap	TOUCH_PANEL_ID			
GPP_D13	GP1	GP1	PCH_GPP_D13		PU 10K(8)	+3VSUS
GPP_D14	GP0	GPO	PCH_GPP_D14/WLAN_LED		PD 100K	
GPP_D15	GP0	GPO	PCH_GPP_D15/WLAN_BT_LED		PD 100K	
GPP_D16	GP1	GP1	(N.C)			
GPP_D17	GP1	GP1	(N.C)			
GPP_D18	GP1	GP1	(N.C)			
GPP_D19	GP1	GP1	(N.C)			
GPP_D20	GP1	GP1	(N.C)			
GPP_D21	GP1	GPO	LED_Record			
GPP_D22	GP1	GP1	(N.C)			
GPP_D23	GP1	GP1	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GP1	GP1	SATAPCIE_DET0		PU 10K	+3VS
GPP_E1	GP1	GP1	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GP1	GP1	SATAPCIE_DET2		PU 10K	+3VS
GPP_E3	GP1	GP1	(N.C)			
GPP_E4	GP1	Native	MOFF2_DEVSLP			
GPP_E5	GP1	Native	(N.C)			
GPP_E6	GP1	Native	MOFF1_DEVSLP			
GPP_E7	GP1	GP1	(N.C)			
GPP_E8	GP1	Native	SATA_LED#		PU 10K(8)	+3VS
GPP_E9	GP1	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GP1	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GP1	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GP1	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GP1	GP1	SATAPCIE_DET3		PU 10K	+3VS
GPP_F1	GP1	GPO	(N.C)			
GPP_F2	GP1	GP1	(N.C)			
GPP_F3	GP1	GP1	(N.C)			
GPP_F4	GP1	GP1	(N.C)			
GPP_F5	GP1	Native	(N.C)			
GPP_F6	GP1	Native	(N.C)			
GPP_F7	GP1	GP1	(N.C)			
GPP_F8	GP1	GP1	(N.C)			
GPP_F9	GP1	GP1	(N.C)			
GPP_F10	GP1	GP1	(N.C)			
GPP_F11	GP1	GP1	(N.C)			
GPP_F12	GP1	GP1	(N.C)			
GPP_F13	GP1	GP1	(N.C)			
GPP_F14	GP1	GP1	(N.C)			
GPP_F15	GP1	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GP1	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GP1	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GP1	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GP1	Native	I_VCCEN_PCH_X1			
GPP_F20	GP1	Native	LCD_BACKEN_PCH_X1			
GPP_F21	GP1	Native	I_RESYNTL_PCH_X1			
GPP_F22	GP1	GP1	(N.C)			
GPP_F23	GP1	GP1	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GP1	GP1	(N.C)		PU 10K	+3VSUS
GPP_G1	GP1	GP1	(N.C)		PU 10K	+3VSUS
GPP_G2	GP1	GP1	(N.C)		PU 10K	+3VSUS
GPP_G3	GP1	GP1	(N.C)			
GPP_G4	GP1	GP1	(N.C)			
GPP_G5	GP1	GP1	(N.C)			
GPP_G6	GP1	GP1	(N.C)			
GPP_G7	GP1	GP1	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GP1	GP1	(N.C)			
GPP_G13	GP1	GP1	(N.C)			
GPP_G14	GP1	GP1	(N.C)			
GPP_G15	GP1	GP1	(N.C)			
GPP_G16	GP1	GP1	(N.C)			
GPP_G17	GP1	GP1	(N.C)			
GPP_G18	GP1	GP1	PCH_GPP_G18			
GPP_G19	GP1	GP1	PCH_GPP_G19			
GPP_G20	GP1	GP1	(N.C)			
GPP_G21	GP1	GP1	(N.C)			
GPP_G22	GP1	GP1	(N.C)			
GPP_G23	GP1	GP1	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GP1	Native	CLKREQ6_MSFF1# _X1		PU 10K	+3VSUS
GPP_H1	GP1	Native	CLKREQ7_SSD1# _X1		PU 10K	+3VSUS
GPP_H2	GP1	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GP1	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GP1	Native	(N.C)		PU 10K	+3VSUS
GPP_H5	GP1	Native	(N.C)		PU 10K	+3VSUS
GPP_H6	GP1	Native	(N.C)		PU 10K	+3VSUS
GPP_H7	GP1	Native	(N.C)		PU 10K	+3VSUS
GPP_H8	GP1	Native	(N.C)		PU 10K	+3VSUS
GPP_H9	GP1	Native	(N.C)		PU 10K	+3VSUS
GPP_H10	GP1	GP1	(N.C)			
GPP_H11	GP1	GP1	(N.C)			
GPP_H12	GP0	GPO	(N.C)	PD		
GPP_H13	GP1	GP1	(N.C)			
GPP_H14	GP1	GP1	(N.C)			
GPP_H15	GP1	GP1	(N.C)			
GPP_H16	GP1	GP1	(N.C)			
GPP_H17	GP1	GP1	(N.C)			
GPP_H18	GP1	GP1	(N.C)			
GPP_H19	GP1	GP1	(N.C)			
GPP_H20	GP1	GP1	(N.C)			
GPP_H21	GP1	GP1	(N.C)			
GPP_H22	GP1	GP1	(N.C)			
GPP_H23	GP1	GP1	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GP1	Native	(N.C)		PD 100K	
GPP_I1	GP1	Native	(N.C)		PD 100K	
GPP_I2	GP1	GP1	(N.C)			
GPP_I3	GP1	Native	(N.C)			
GPP_I4	GP1	Native	SSD_I4		PD 100K	
GPP_I5	GP1	Native	(N.C)		PU 2.2K	+3VS
GPP_I6	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I7	GP1	Native	(N.C)		PU 2.2K	+3VS
GPP_I8	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I9	GP2	Native	(N.C)		PU 2.2K(8)	+3VS
GPP_I10	GPO	Native	(N.C)	PD	PU 2.2K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(8)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUS3#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUS5#		PD 100K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	GPO	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(8)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PHYEN		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PU 1K	
GPA1	OD	GPO	CHG_LED#	PU 10K (8)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (8)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN2_PWM		
GPA6	Alt	PWM	PM_LED_PWM		
GPA7	O	GPO	GS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_EC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	HDMI_ON#2	PD 10K	
GPB6	OD	GPO	BC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (8)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_THRMTRIP#	PU 10K (8)	+3VSUS
GPC4	I	GPI	EC_SATA/INT#4	PD 10K	+3VSUS
GPC5	I	GPI	PM_SUSC#	PU 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	
GPC7	O	GPO	EC_SPI7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/WL_AC_PRESENT	PU 100K	+3VA_DSW
GPD2	Alt	GPI	BUF_PLT_RST#	PU 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/USB_SS#		
GPD6	Alt	GPI	FAN2_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PU 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PU 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	SUSACK#_WOC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUSB#	PU 100K	
GPE6	OD	GPO	CAP_LED#		
GPE7	OD	GPO	THRO_CPU#	PU 10K (8)	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VDUS_ON	PU 100K±5% 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K±5% 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0 CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0 DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	GPI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PMBLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GP2		EC_SCK#/EC_SCK#_PCH		
GPG4	GP2		EC_SI/EC_SI_PCH		
GPG5	GP2		EC_SO/EC_SO_PCH		
GPG6	O	GPO	USB30_5VSUS		
GPG7	GP2		EC_SCK_PCH	PU 10K (8)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3 CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3 DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_SUSC#7#	PU 10K (8)	
GPH4	O	GPO	DPWROK_EC	PU 10K	
GPH5	O	GPO	PM_PWROK	PU 10K	
GPH6	O	GPO	PM_SYSPWROK	PU 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_S0#		
GPI1	I	GPI	SYSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP9_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PU 0	+3VACC
GPI7	Alt	AD	WA_MAX_POWER	PU 100K x 9Q 54K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB11_5VSUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VAUSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_USB_STA7#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5	PU 2.2K	
GPJ6	I	GPI	PM_WAKE#	PU 100K	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EC0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EC01		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EC02		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EC03		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/EC0CK		CLK_XBCH21_PCH		
GPM5	LFRAME#/EC0#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
on board memory CHA	
SO-DIMM B(0)	A4h

EC Master (SMB1)	SM-Bus Address
SM-Bus Device	
VGA Thermal Sensor	90h
CPU Thermal Sensor	98h
Power Thermal Sensor	70h

Device Identification

CPU Thermal Sensor		
1st	0x4d3213b9	MCT777U
2nd		

GX501VIP/CIE & USB Function define

Kabylake HM175

GID	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3.0 MB Port1(Charger)	
02	USB3#02 / SSIC#01	USB3.0 Port2	
03	USB3#03 / SSIC#02	USB3.0 Port3	
04	USB3#04	USB3.0 Port4	
05	USB3#05		
06	USB3#06		
07	USB3#07 / PCIE#01	CardReader_USB3(RSV)	
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE		
11	PCIE#05 / GBE	Thunderbolt	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	SATA*1 SSD port0	
16	PCIE#10 / SATA#1	PCIE*4 SSD	SRC6
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3		
23			
24			
25			
26			

USB 2.0	Function
USB2_01	USB3.0 MB Port1(Charger)
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4
USB2_06	
USB2_07	Card Reader
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

SKL PCH-H Z170 HSIO

1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7	PCIE #1	x 2	x 4	NA	
8	USB3 #8	PCIE #2				
9	USB3 #9	PCIE #3	x 2			
10	USB3 #10	PCIE #4	GbE			
11	PCIE #5		GbE	x 2	x 4	NA
12	PCIE #6					
13	PCIE #7			x 2		
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23	SATA #4			x 2	x 4	Intel IRST PCIE Storage Device #3
24	SATA #5					
25	PCIE #19	SATA #6				
26	PCIE #20	SATA #7				

SKL PCH-H H170 HSIO

1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7					
8	USB3 #8					
9	PCIE #3		x 2	NA	NA	
10	PCIE #4	GbE				
11	PCIE #5	GbE	x 2	x 4	NA	
12	PCIE #6					
13	PCIE #7		x 2			
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23	SATA #4			NA	NA	NA
24	SATA #5					
25	PCIE #19			x 2		
26	PCIE #20					

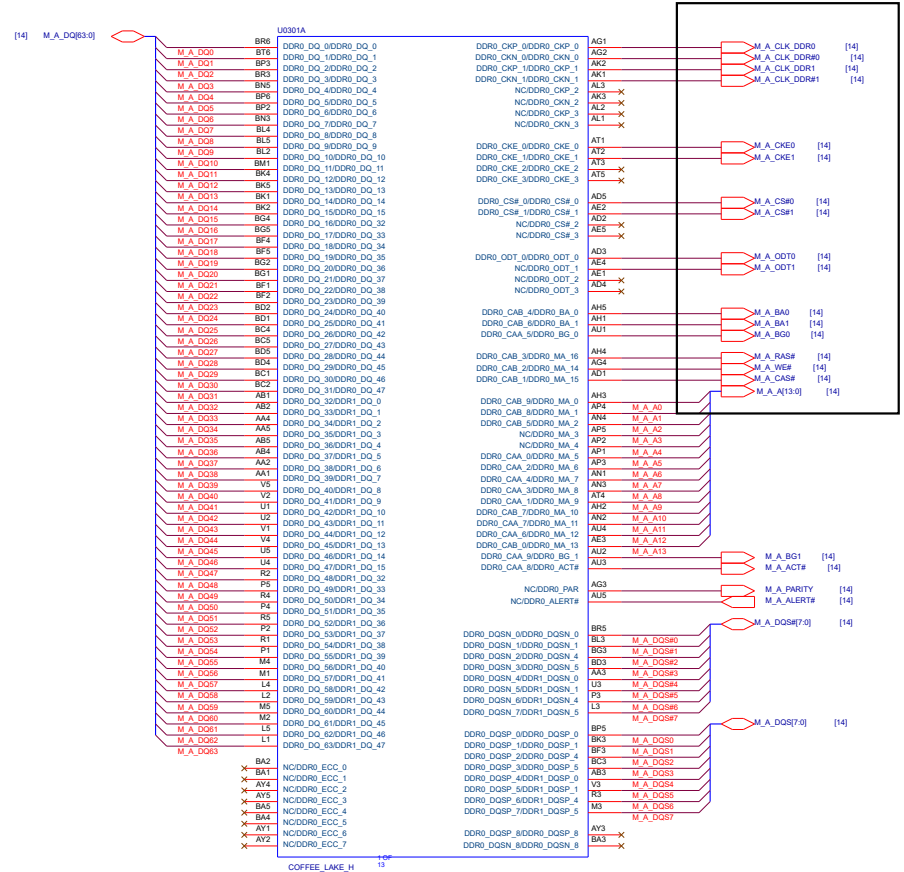
SKL PCH-H HM170 HSIO

1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7	PCIE #1	x 2	x 4	NA	
8	USB3 #8	PCIE #2				
9	PCIE #3		x 2			
10	PCIE #4	GbE				
11	PCIE #5	GbE	x 2	x 4	NA	
12	PCIE #6					
13	PCIE #7		x 2			
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23				NA	NA	NA
24						
25				NA		
26						

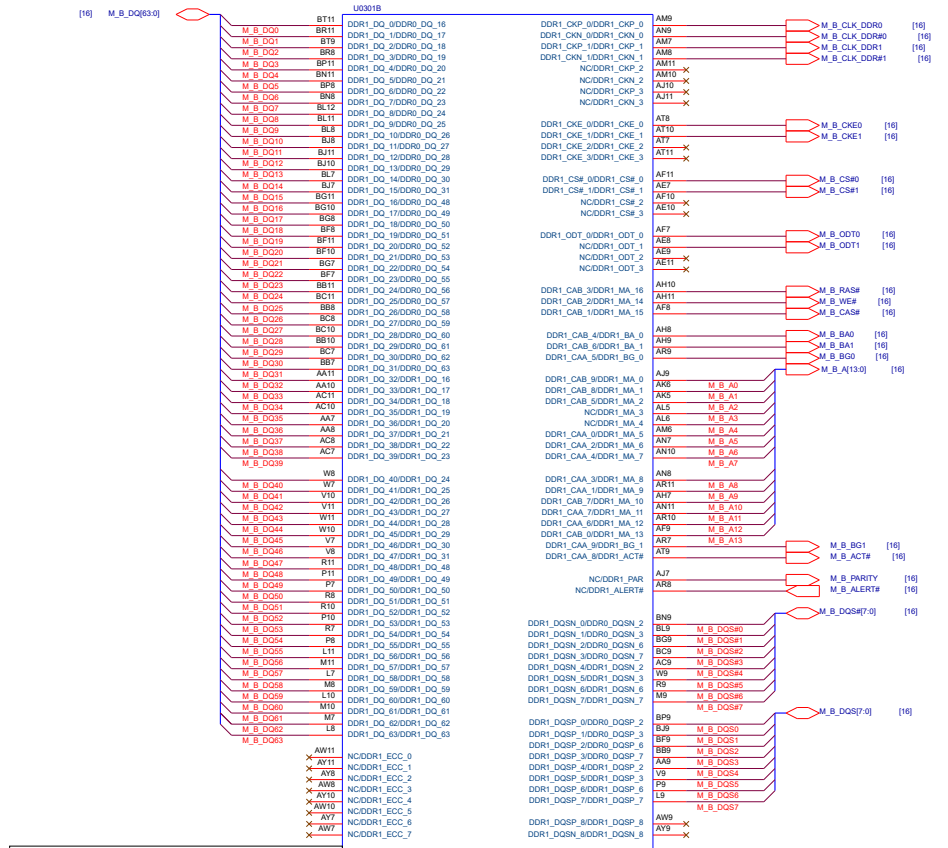
ASUS	Project Name: G711GW		Rev: 1.0
Title: System Setting			
Size:	Document Number:		Rev: 1.0
Date: Wednesday, April 11, 2018	Sheet: 1 of 70		

Memory Channel A

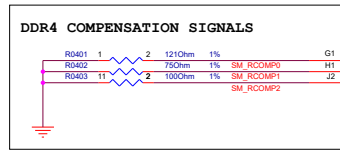
Chris



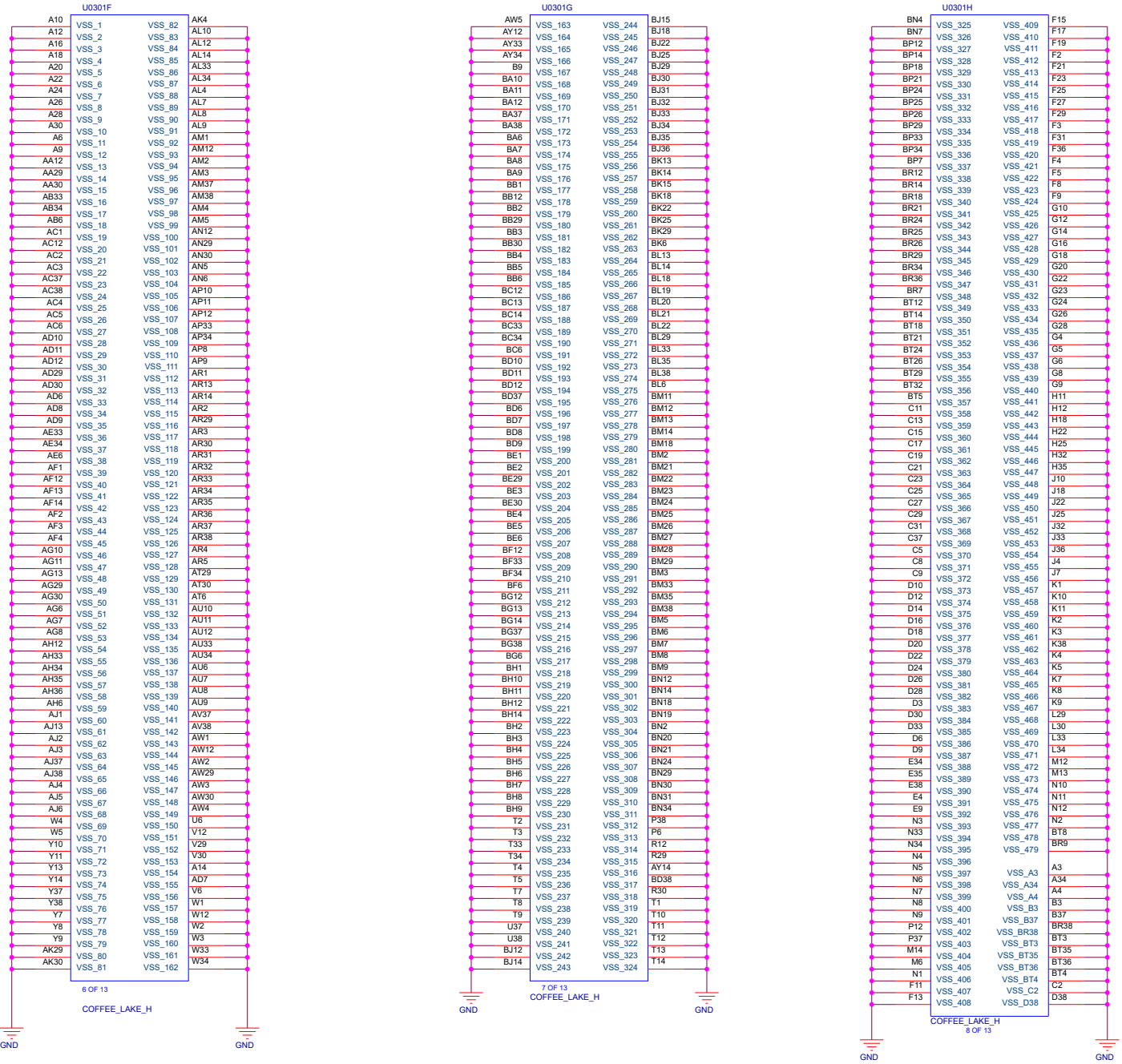
Memory Channel B



DDR4 COMPENSATION SIGNALS

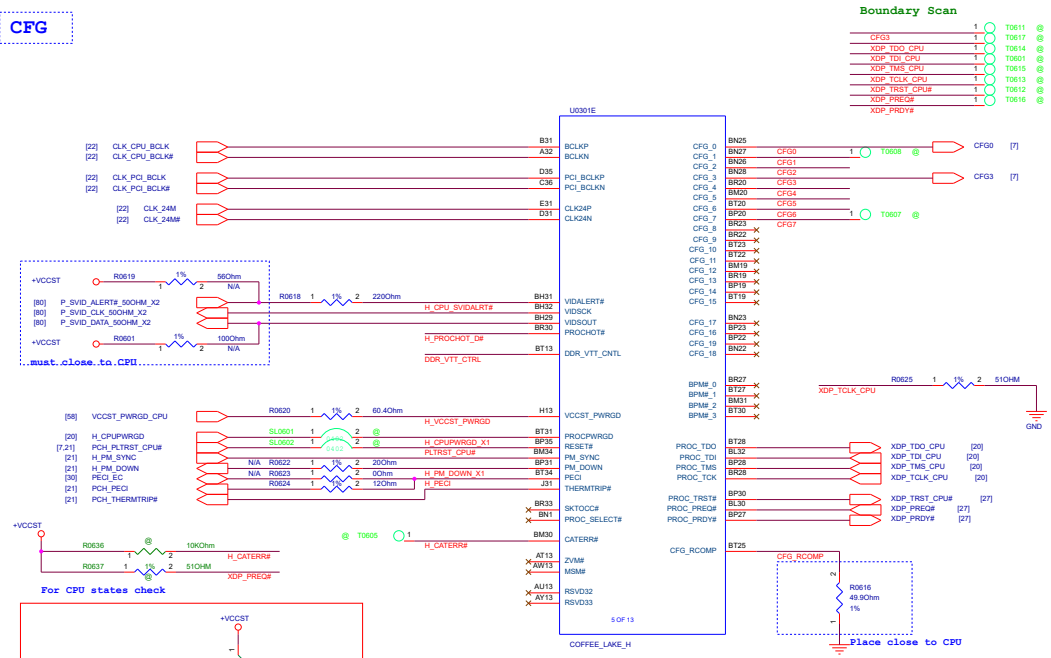


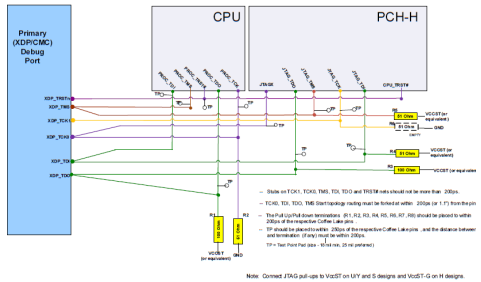
Project Name: G711GW			Rev: 1.0
Title : CPU_DDR4			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 4 of 103		



Project Name: G711GW			Rev: 1.0
Title : CPU_CFG,RSVD,GND			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 5 of 103		

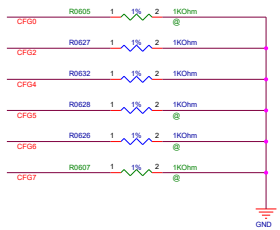
CFG





Chris

CFG Straps



CFG Straps for Processor

ref : Intel 570805_Coffeelake_EDS_Vol_1_Rev1.4 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

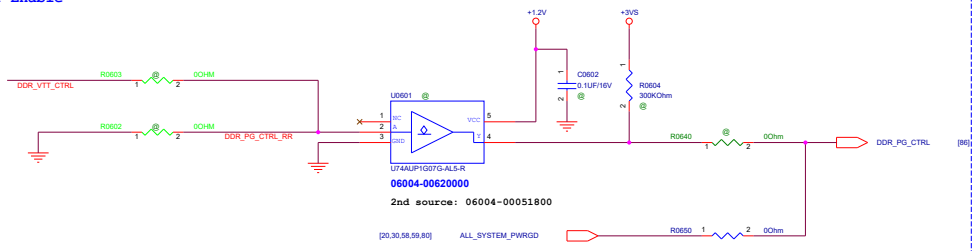
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

CFG[19:8] : Reserved Configuration Lanes

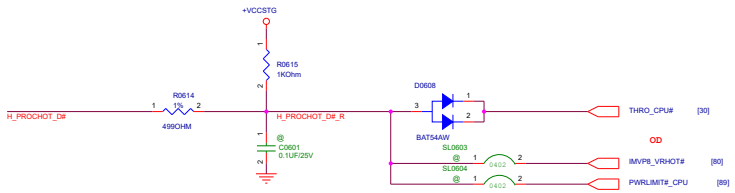
Reserved Configuration Lanes

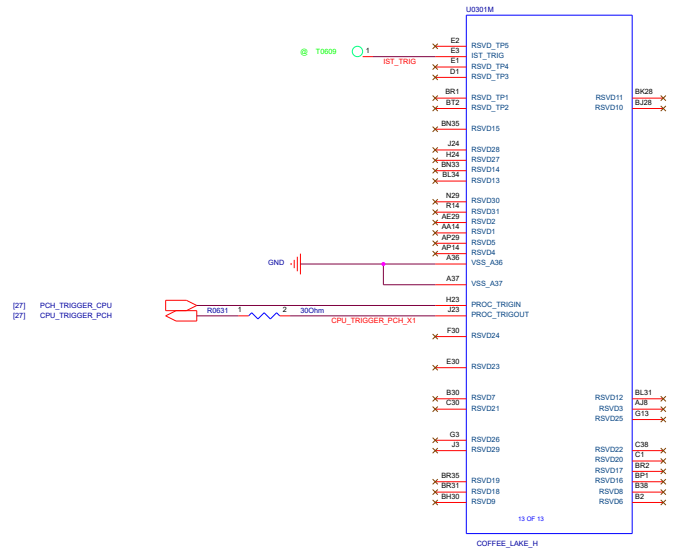
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116

VTT Enable



CPU SIDEBAND SIGNALS





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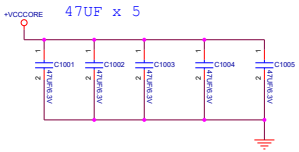
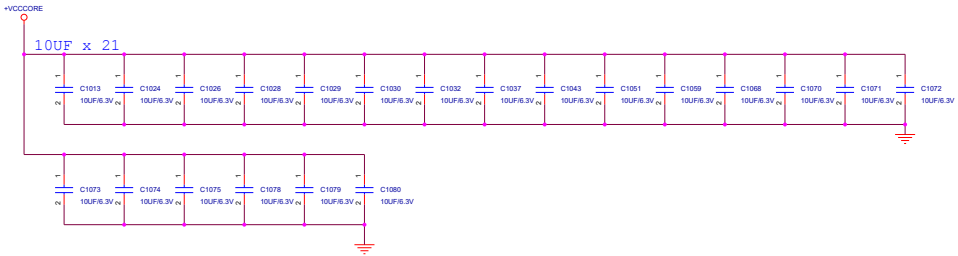
Project Name: G711GW		Rev: 1.0
Title : CPU_CFG,RSVD		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 6 of 103	

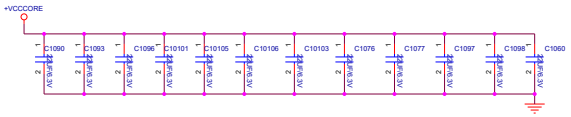
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

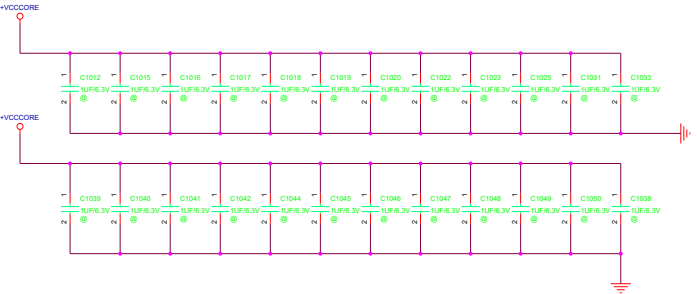
+VCCORE near CPU



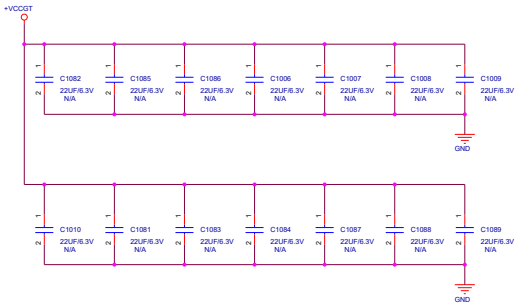
+VCCORE DECAPS Place Back Side (TOP)



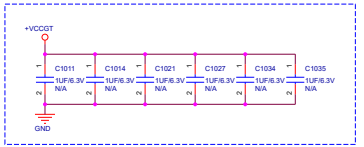




+VCCGT cap near CPU **22uF x14**



1107 add for VCCGT PI issue



ASUS	Project Name: G711GW		Rev: 1.0
Title : 010_CPU_POWER_CAP			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 10 of 103		

	Project Name G711GW	Rev R1.0

Title : TBT_Alpine-Ridge

Size	Dept.:	Engineer:
C	ASUSTeK COMPUTER	Gaming RD

Date: Wednesday, April 17, 2019	Sheet 11 of 103

<Variant Name>

Title : DDR4_TERMINATION

ASUSTeK COMPUTER

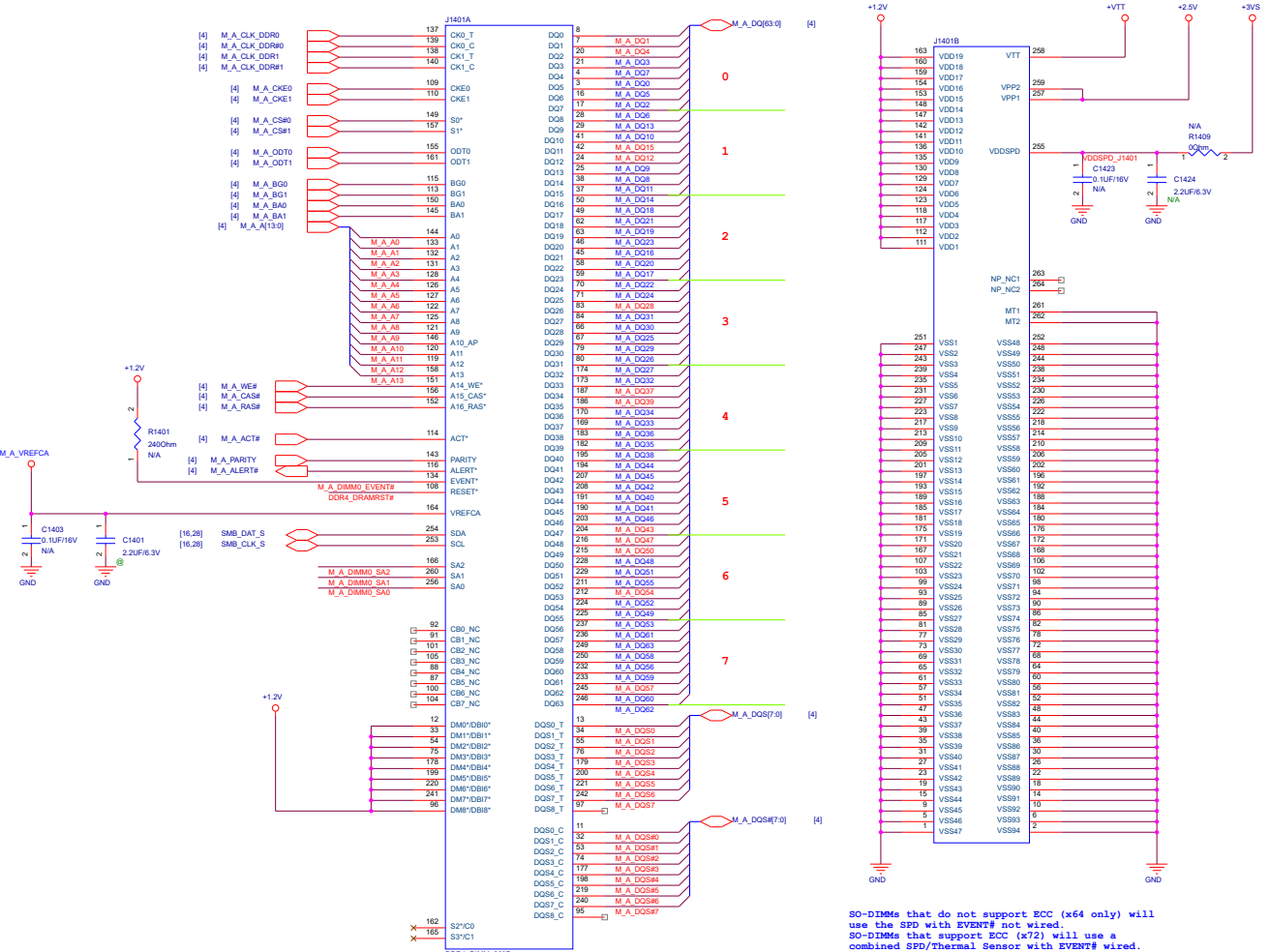
Engineer: Gaming RD

Size	Project Name	Rev
Custom	**G711GW**	1.0

Date:	Wednesday, April 17, 2019	Sheet	13	of	103

Chris

SODIMM CHA-DIMM0
TOP H4.0mm REV (J1401)

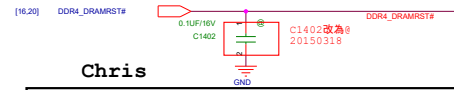


SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

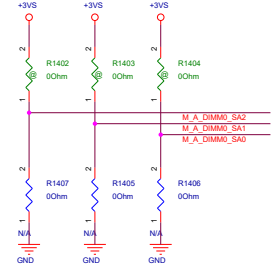
DDR4_DIMM_260P

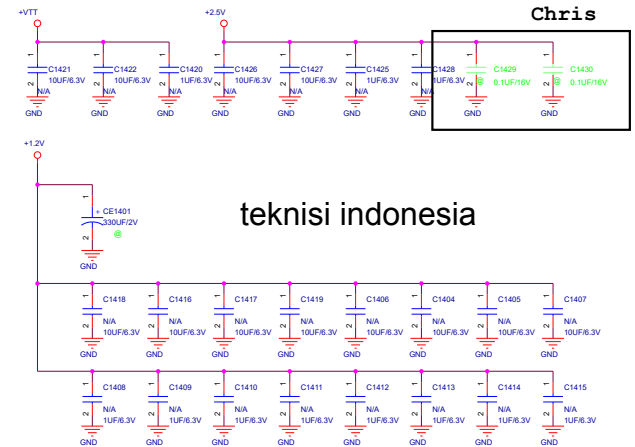
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

Main Board



Chris





Chris

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ASUS	Project Name: G711GW	Rev: R1.0
Title :	DIM_DDR4 SO-DIMM A1	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 14 of 103	

<Variant Name>

Title : DDR4_ON-BOARD_A2

ASUSTeK COMPUTER

Engineer: Gaming RD

Size	Project Name	Rev
C	**G711GW**	1.0

Date:	Wednesday, April 17, 2019	Sheet	15	of	103

<Variant Name>

Title : NB_****

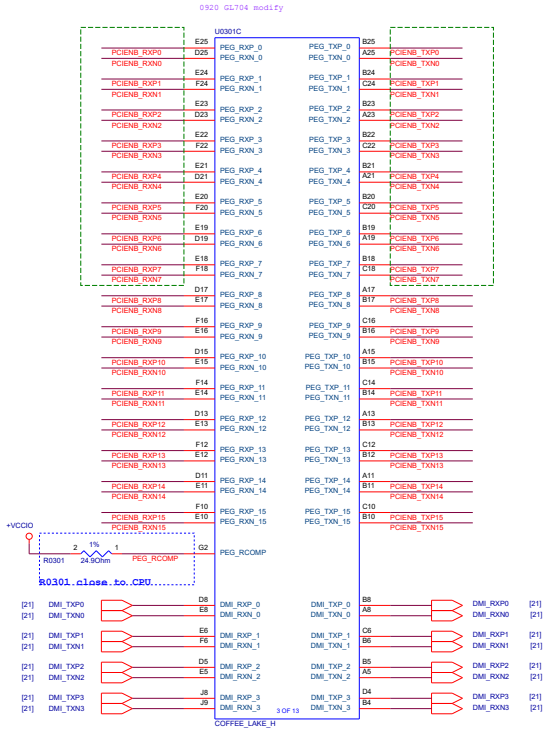
ASUSTeK COMPUTER

Engineer: Gaming RD

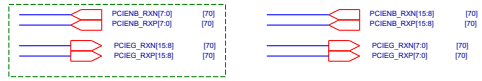
Size	Project Name	Rev
A	**G711GW**	1.0

Date:	Wednesday, April 17, 2019	Sheet	17	of	103

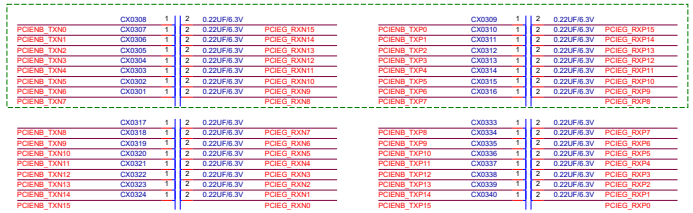
PCIEG



CFG2=0 -> Reversed
CFG5=0 -> PCIEG 2x8



modify to PCIE x16
2018_0917



Display

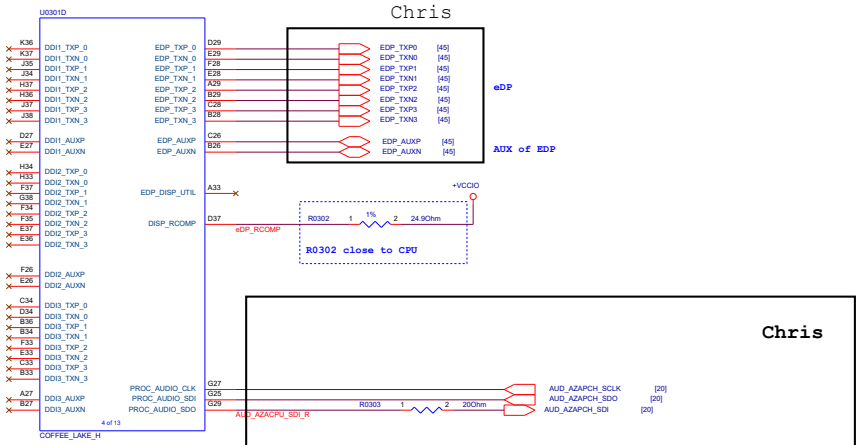


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

Refer to CFL-H PDG P.363 (Doc.571391)

31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected.

ASUS	Project Name: G711GW	Rev: R1.1
Title : CPU_DMI,PEG,FDI,eDP,DDI		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 3 of 103	

Figure 4-23. CFL H DDR4 x16 Memory Down V_{REF-CA} Overview

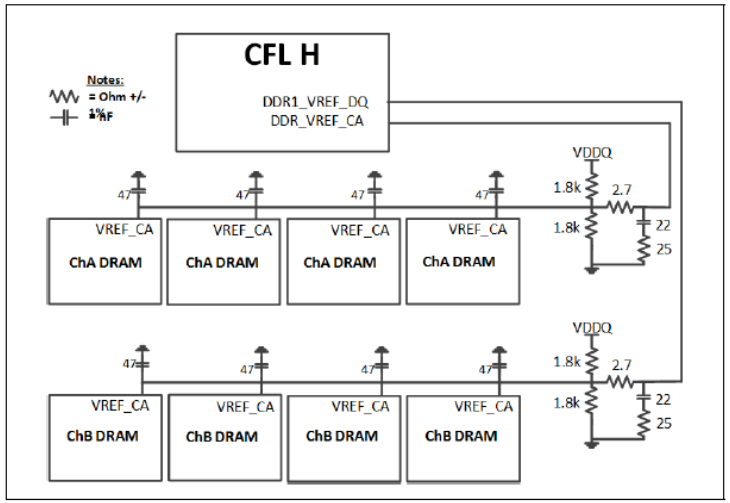
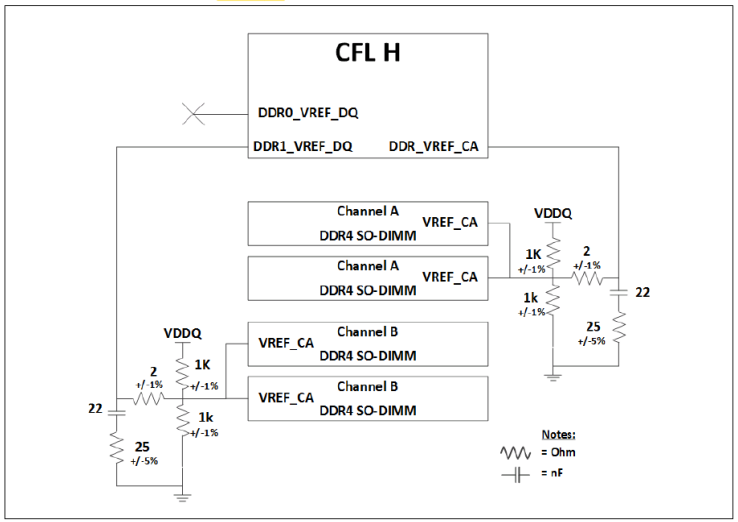
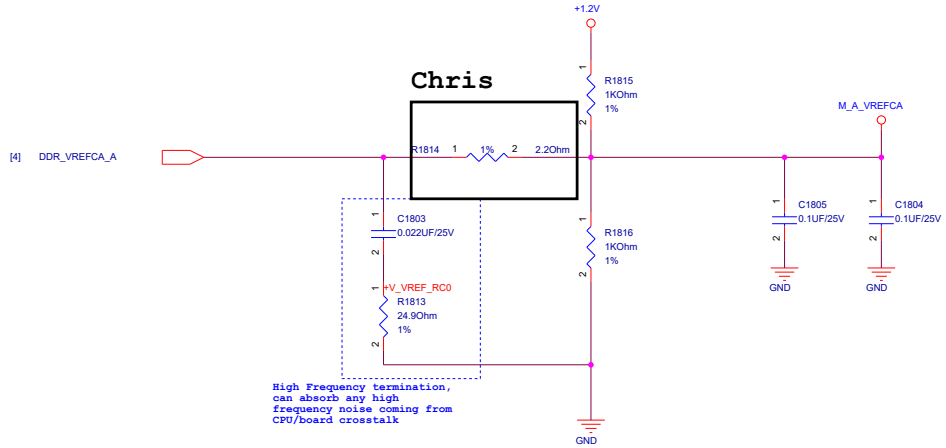


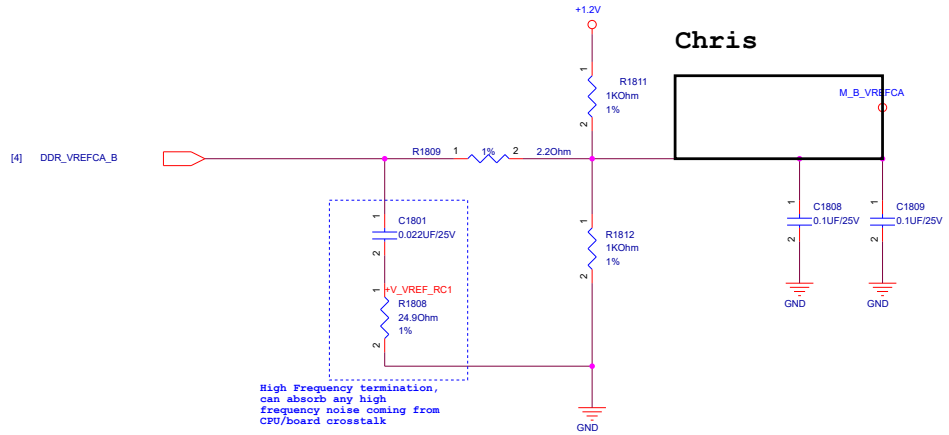
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview



Vref for CHA_DIMM0



Vref for CHB_DIMM0



Main Board

Project Name: G711GW		Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 18 of 103	

<Variant Name>

ASUSTeK COMPUTER	Title : *****	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 19 of 103	

HD Audio

follow HDAv1.0
RM2001 33ohm for HDA 3.3V
RM2001 33ohm for HDA 1.8V

RF requirement

Chris

ACZ_SDOUT:
(1)PCH:
Internal PD 20k ohm,
VIL=0.35V,VIH=0.65~3.3V
(2)ALC269:
VIL<0.35*3.3V,VIH>0.65*3.3V

ACZ_SDOUT is a signal used for Flash Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override

EMI-GX501GI

Power failure solution (S0-->G3,S5-->G3):

09/11 RF change

Chris

Main Board

Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.05VSUS	+VCCST		
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	+V3.3A_V1.8A_VCCPAZIO
		+3VS		

eSPI or LPC

PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

TLS Confidentiality

PU	Enable
PD	Disable (default)

Top Swap Override

PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

SMBUS

EMI-GX501GI

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

PM_PWROK,PM_RSMRST#: previous platform solution.

ME_PWROK,ME_AC_PRESENT: reserved for test.

09'MoW04:
Optional if ME FW is Ignition FW

D2207: Prevent EC drive high, SUS_PWRGD sink low in S5-->G3.

Power failure solution (S0-->G3,S5-->G3):

R1.0-34

PCH_GPPC2: weak internal pull down

Power failure solution (S0-->G3,S5-->G3):

SKL-H

DIMM

Change D2040 to 10Kohm if mount D2006

Deep SX discharge (S0-->DSX,S5-->DSX)

R1.1-03

RTC battery

1st :12017-00020200
2nd :12017100002C
USE RTC Battery:
P/N: 0B100-00040500 BATT-LI CR1220 3V

Project Name	G711GW
Rev	1.0
Title :	PCH-CPT(1)SATA,HDA,RTC,JTAG
Size	Custom
Dept.:	ASUSTeK COMPUTER
Engineer:	Gaming RD
Date:	Wednesday, April 17, 2019
Sheet	20 of 103

Main Board

PCIE Setting

GX501GI PCIE/SATA Function define

CNL HM370

HSIO Capabilities	Function
PCIEG (From GPU)	
PCIE#01 - USB3.1#07	
PCIE#02 - USB3.1#08	
PCIE#03 - USB3.1#09	
PCIE#04 - USB3.1#10	
PCIE#05	
PCIE#06	
PCIE#07	
PCIE#08	
PCIE#09	PCIE*4 SSD
PCIE#10	
PCIE#11- SATA-0a	
PCIE#12- SATA-1a	
PCIE#13- SATA-0b	
PCIE#14- SATA-1b	
PCIE#15 / SATA#2	
PCIE#16 / SATA#3	WLAN
PCIE#17 / SATA#4	
PCIE#18 / SATA#5	
PCIE#19 / SATA#6	
PCIE#20 / SATA#6	
PCIE#21	TBT (x4)
PCIE#22	
PCIE#23	
PCIE#24	

	Function
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	CR
CLKREQ-3	WLAN
CLKREQ-4	
CLKREQ-5	TBT AR
CLKREQ-6	PCIE SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	

USB Setting

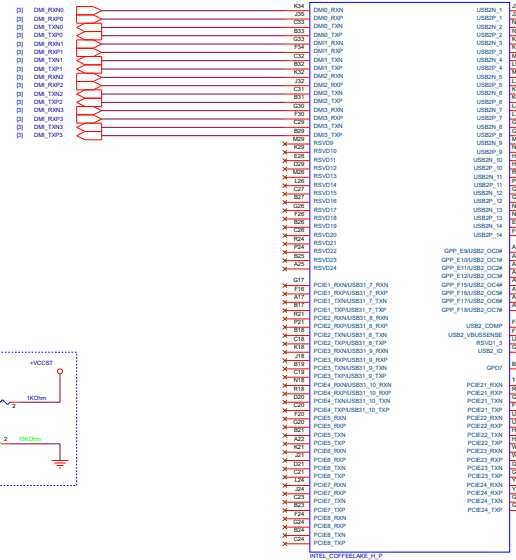
GX501GI USB Function define

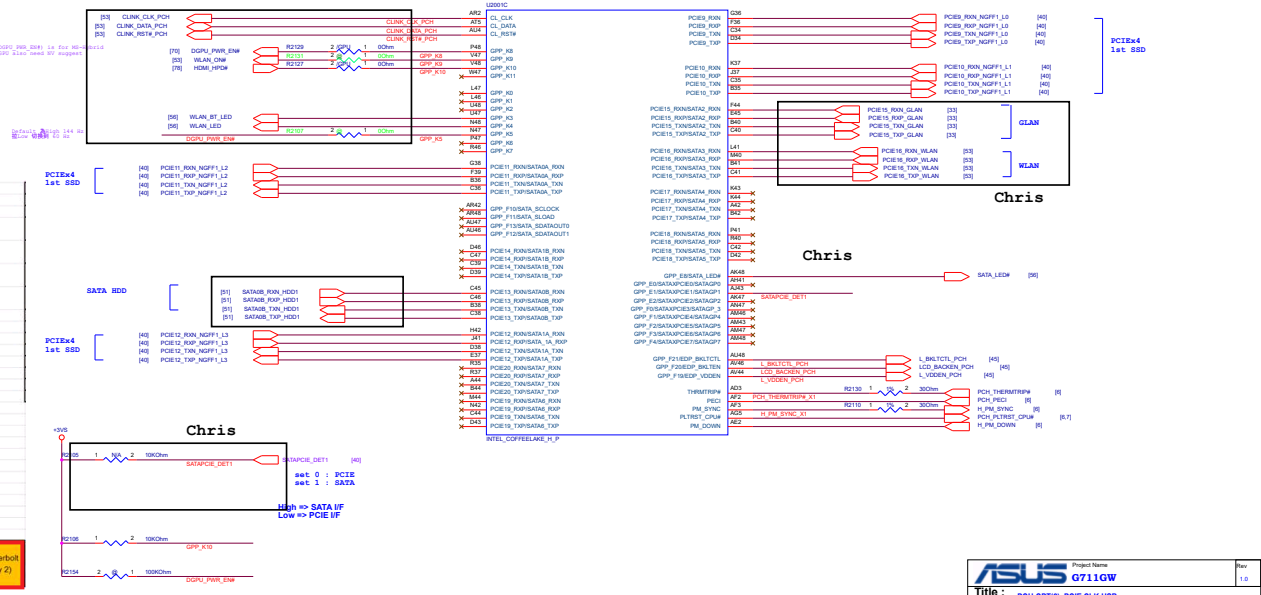
CNL HM370

USB 2.0	Function
USB2_01	USB3.0 MB Port1
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4(Charger)
USB2_06	TBT
USB2_07	
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

USB 3.0	Function
USB3.1#01	USB3.1MB Port1 (Support Gen2)
USB3.1#02	USB3.0 MB Port2 (Support Gen2)
USB3.1#03	USB3.0 MB Port3 (Support Gen2)
USB3.1#04	USB3.0 MB Port4 (Support Gen2)
USB3.1#05	
USB3.1#06	
USB3.1#07	
USB3.1#08	

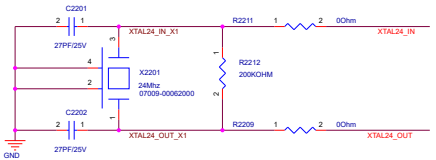
HSIO	HM370	QM370	CM246	IRST			Devices Assign
0	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1				(port1) USB3.1 Type C
1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2				(port2) USB3.1 Type C
2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3				(port1) USB3.0 Type A USB3.1 Type A
3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4				(port2) USB3.0 Type A USB3.1 Type A
4	USB3.1 Gen1 #5	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #5				(port3) USB3.0 Type A USB3.1 Type A only for QM370 / CM246
5	USB3.1 Gen1 #6	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #6				(port4) USB3.0 Type A USB3.1 Type A only for QM370 / CM246
6	USB3.1 Gen1 #7	USB3.1 Gen1 #7	USB3.1 Gen1 #7	PCIE #1			CR (USB3.0 / PCIE)
7	USB3.1 Gen1 #8	USB3.1 Gen1 #8	USB3.1 Gen1 #8	PCIE #2	NO	x2	
8	NA	USB3.1 Gen1 #9	USB3.1 Gen1 #9	PCIE #3		x4	
9	NA	USB3.1 Gen1 #10	USB3.1 Gen1 #10	PCIE #4			
10	NA GbE	PCIE #5 GbE	PCIE #5 GbE	PCIE #5	NO	x4	Thunderbolt (priority 1)
11	NA	PCIE #6	PCIE #6	PCIE #6		x2	
12	NA	PCIE #7	PCIE #7	PCIE #7		x2	
13	NA	PCIE #8	PCIE #8	PCIE #8			
14	PCIE #9 GbE	PCIE #9 GbE	PCIE #9 GbE	PCIE #9 GbE	Yes	x4	1st M.2 SSD (PCIE*4 / SATA#1a) (PCIE*4, optane) 1st M.2 SSD (PCIE*2, optane)
15	PCIE #10	PCIE #10	PCIE #10	PCIE #10		x2	
16	PCIE #11 SATA #0a	PCIE #11 SATA #0a	PCIE #11 SATA #0a	PCIE #11 SATA #0a			
17	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE			
18	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	NO	x4	HDD (SAT#0b) ODD (SAT#1b)
19	PCIE #14 SATA #1b	PCIE #14 SATA #1b	PCIE #14 SATA #1b	PCIE #14 SATA #1b		x2	GLAN
20	PCIE #15	PCIE #15	PCIE #15	PCIE #15 SATA #2			WLAN
21	PCIE #16	PCIE #16	PCIE #16	PCIE #16 SATA #3			
22	PCIE #17 SATA #4	PCIE #17 SATA #4	PCIE #17	PCIE #17 SATA #4	Yes	x4	2nd M.2 SSD (PCIE*4 / SATA#4) (PCIE*4, optane) 2nd M.2 SSD (PCIE*2, optane)
23	PCIE #18 SATA #5	PCIE #18 SATA #5	PCIE #18	PCIE #18 SATA #5		x2	
24	PCIE #19	PCIE #19	PCIE #19	PCIE #19 SATA #6			
25	PCIE #20	PCIE #20	PCIE #20	PCIE #20 SATA #7			
26	PCIE #21	PCIE #21	PCIE #21				
27	PCIE #22	PCIE #22	PCIE #22		Yes	x4	3rd M.2 SSD (PCIE*4) (PCIE*4, optane) 3rd M.2 SSD (PCIE*2, optane) 10G LAN (PCIE*4) optional Thunderbolt (priority 2)
28	PCIE #23	PCIE #23	PCIE #23			x2	
29	PCIE #24	PCIE #24	PCIE #24				



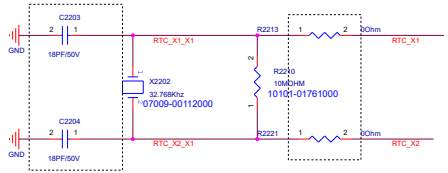


Project Name	G711GW
Rev	1.0
Title :	PCH-CPT(2)_PCIE,CLK,USB
Size	Custom
Dept.:	ASUSTeK COMPUTER
Engineer:	Gaming RD
Date:	Wednesday, April 17, 2019
Sheet	21 of 103

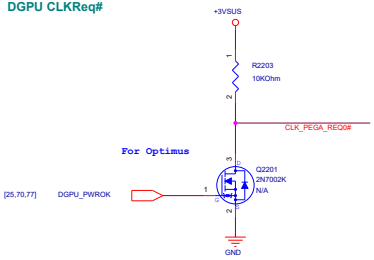
XTAL 24MHz



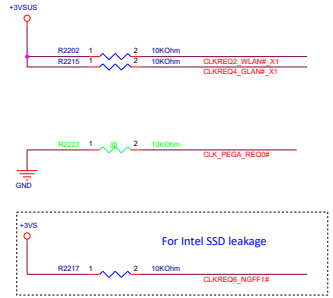
RTC CRYSTAL 32.768KHz

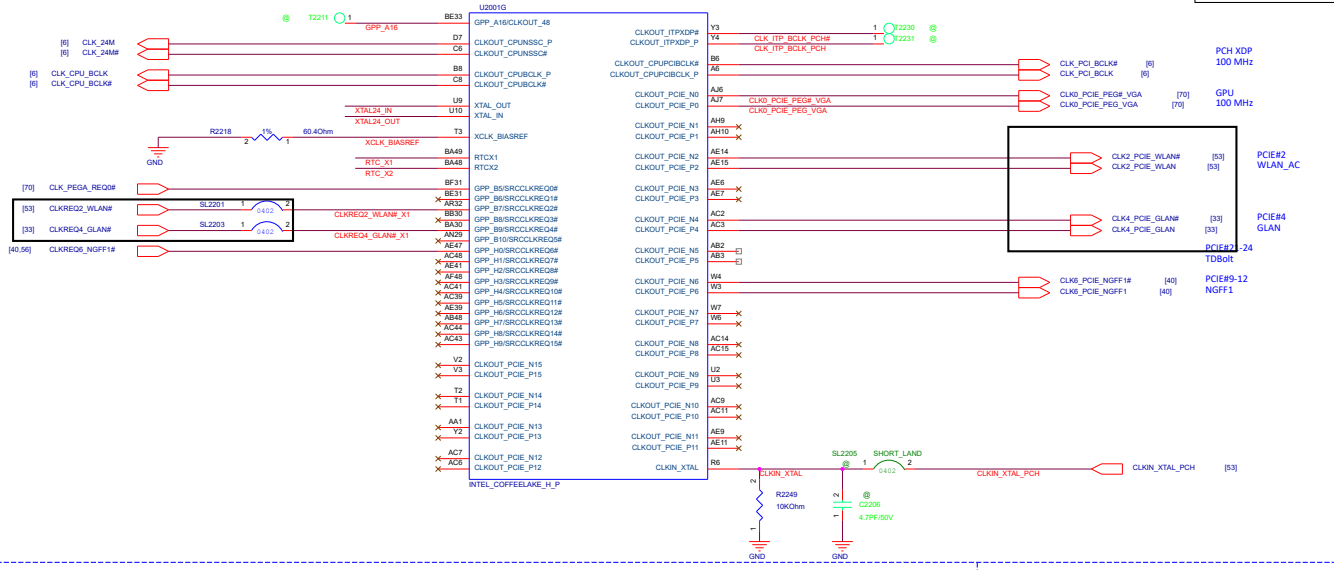


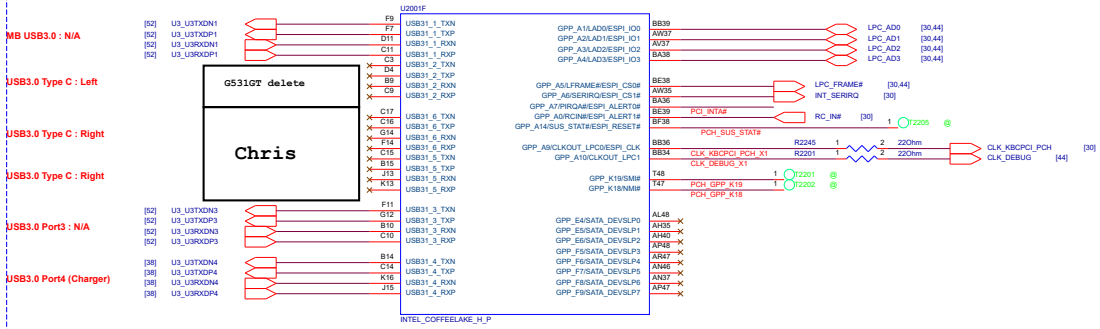
DGPU CLKReq#



PCH CLKREQ Setting:







Project Name: G711GW			Rev: 1.0
Title: PCH-CPT(3)_FDI,DMI,SYS PWR			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 22 of 103		

HPD0 to DP

HPD1 to HDMI

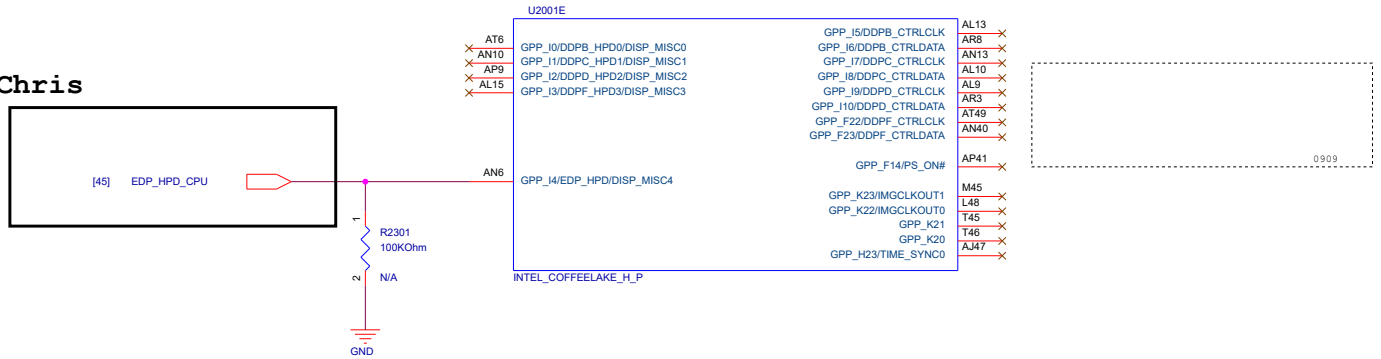
HPD2 to TBT

HPD3 to VGA

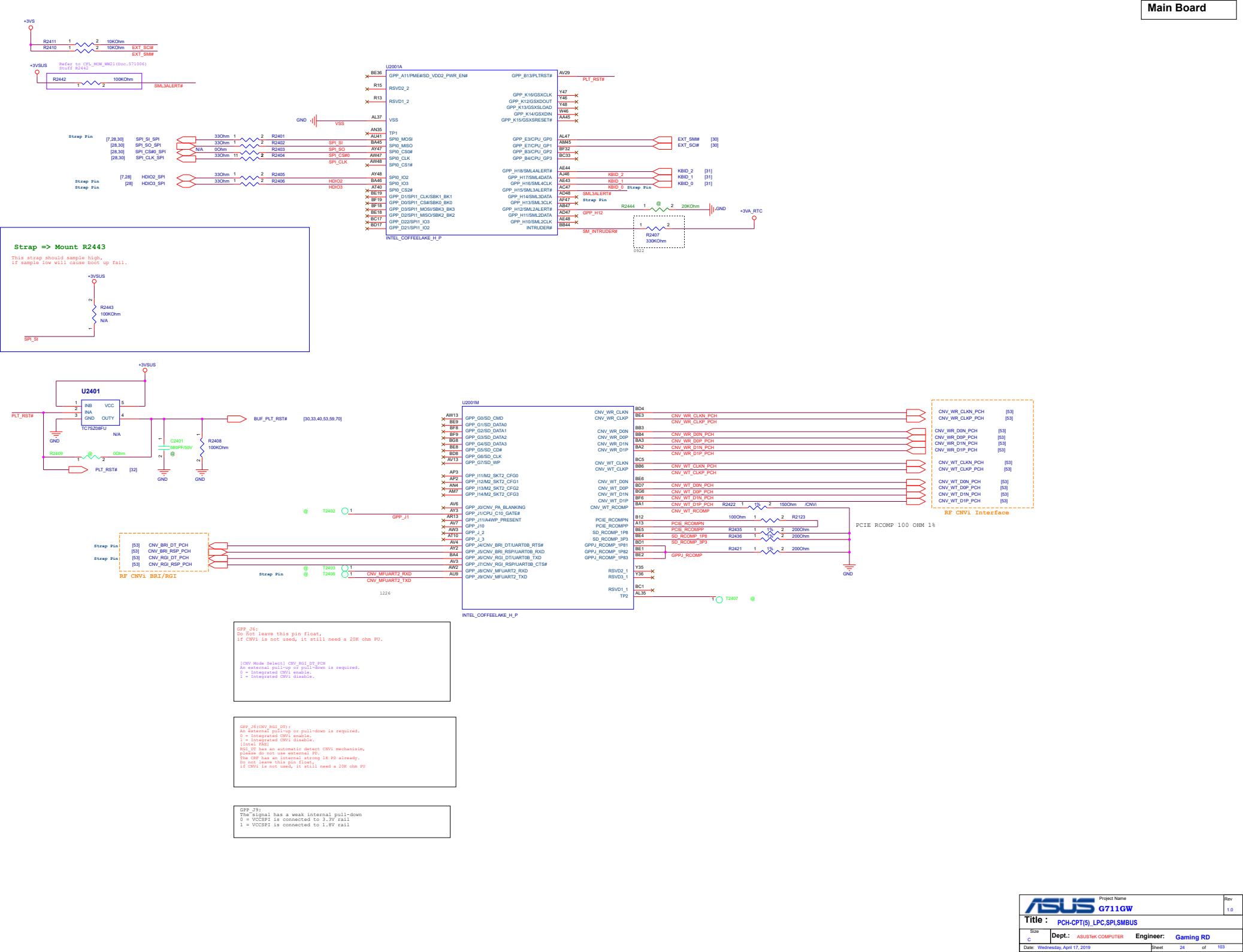
HPD4 to EDP Panel

DDP Strap Setting Update :
0 = Port is not detected (Default)
1 = Port is detected

Chris



Project Name: G711GW			Rev: 1.0
Title : PCH-CPT(4)_eDP,PCI,DP			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019		Sheet 23 of 103	



Strap => Mount R2443

This strap should sample high,
if sample low will cause boot up fail.

GPP_J6:
Do Not leave this pin float,
if CNVi is not used, it still need a 20K ohm PU.

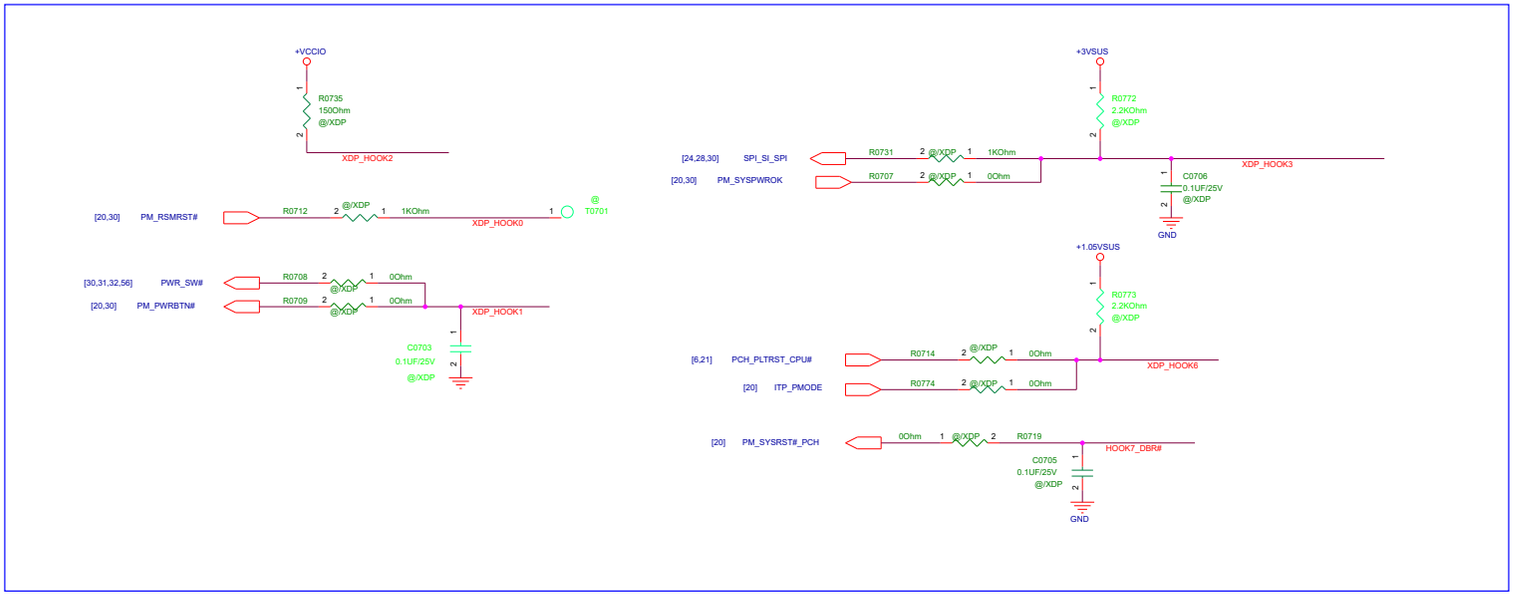
[CNV Mode Select] CNV_RGI_DT_PCH
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

GPP_J6(CNV_RGI_DT):
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
[Intel FAE]
RGI_DT has an automatic detect CNVi mechanism,
please do not use external PD.
The CRF has an internal strong 1K PD already.
Do not leave this pin float.
if CNVi is not used, it still need a 20K ohm PU

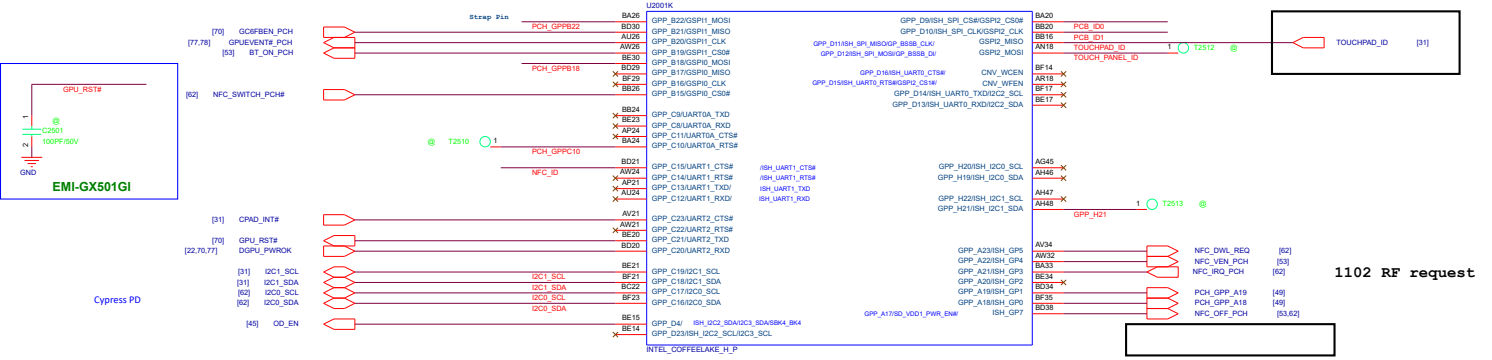
GPP_J9:
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

Project Name: G711GW		Rev: 1.0
Title : PCH-CPT(5)_LPC,SPI,SMBUS		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 24 of 103	

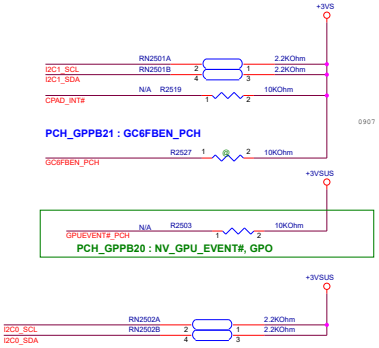
CPU XDP



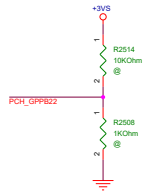
Project Name: G711GW		Rev: 1.0
Title : CPU XDP		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 7 of 103	



1102 RF request

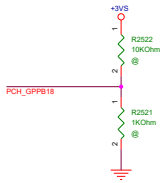


Boot BIOS Strap Bit BBS



PCH_GPPB22: weal internal pull down	
PU	LPC
PD	SPI (Default)

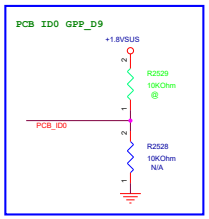
No Reboot



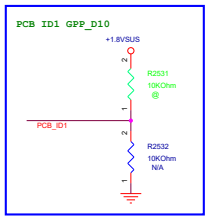
NOTE: Enable No Reboot
PCH will disable the TCO
Timer system reboot feature.
This function is useful when running ITP/XDP.

PCH_GPPB18: weak internal pull down	
PU	Enable
PD	Disable (Default)

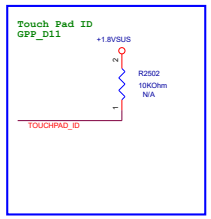
PCB ID0 GPP_D9



PCB ID1 GPP_D10

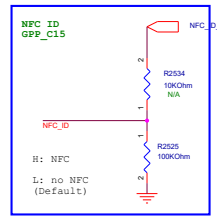


Touch Pad ID GPP_D11



Touch Panel ID GPP_D12

NFC ID GPP_C15



X-tal Frequency Select

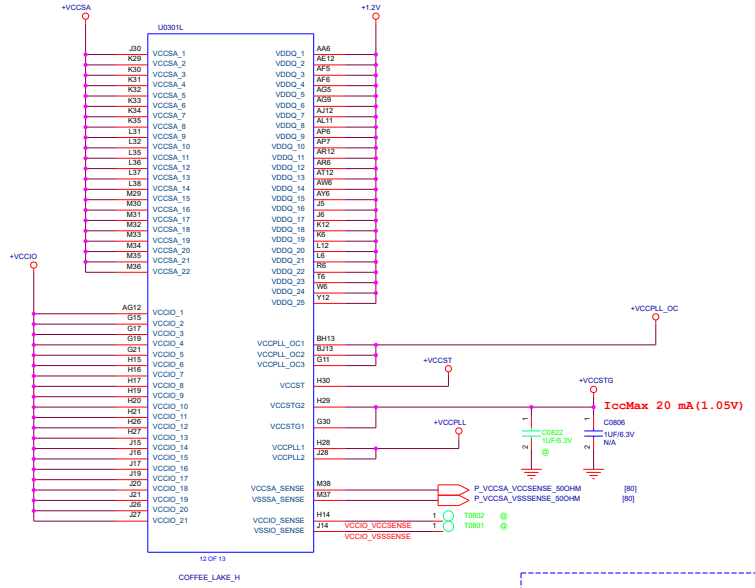
Cannon Lake PCH-LP

- XTAL_Freq_Select = GPP_H21
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

Cannon Lake PCH-H

- XTAL_Freq_Select = GPP_J4
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

Project Name: G711GW			Rev: 1.0
Title: PCH-CPT(6)_GPIO,MISC			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 25 of 103		



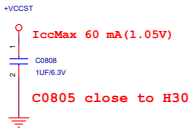
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	
		+VCCSTG	
	+1.2V	+VTT	
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	

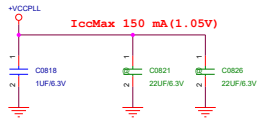
Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
VccST off in S3	On in S3	+25-30mW
VccPLL_OC off in S0/C10	On in S0/C10	+3-10mW
VccPLL_OC off in S0ix	On in S0ix	+3-10mW

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for gating off VccSTG, VccPLL_OC and VccIO (CFL-H) in the S0/C10 system state in order to save power.

+VCCST/+VCCPLL DECAPS Place Back Side (TOP)





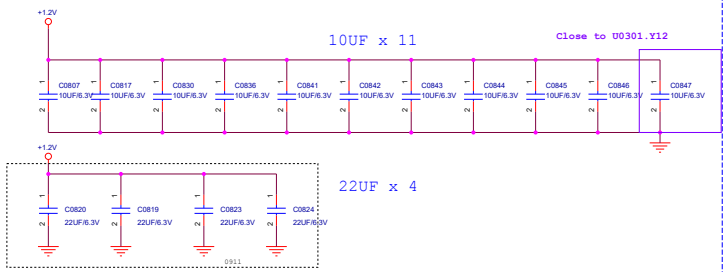
CFL U/H PDG Update for VCCPLL Power Rail Design Guidelines

Due to Display PLL lock issues observed on systems with high noise level on VCCPLL, CFL-H [BP#571391 and CFL-U [BP#571021 Platform design guidelines has been updated with new recommendation for VCCPLL power rail.

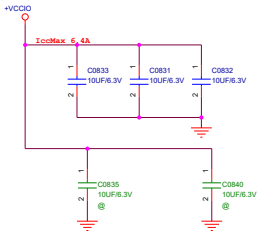
An additional capacitor 0805 size placeholder near CPU BGA ball is recommended for better power delivery, this should be stuffed when encountered a noisy VCCPLL power rail.

This new recommendation not required for systems that follows the PDG Power Integrity guidance and kept low noise level on VCCPLL.

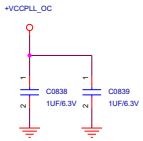
+VDDQ DECAPS Place Back Side (TOP)



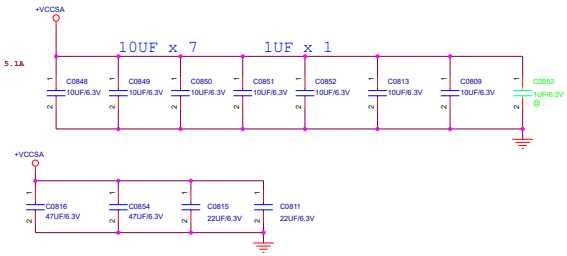
+VCCIO DECAPS Place Back Side (TOP)



+VCCPLL_OC DECAPS Place Back Side (TOP)

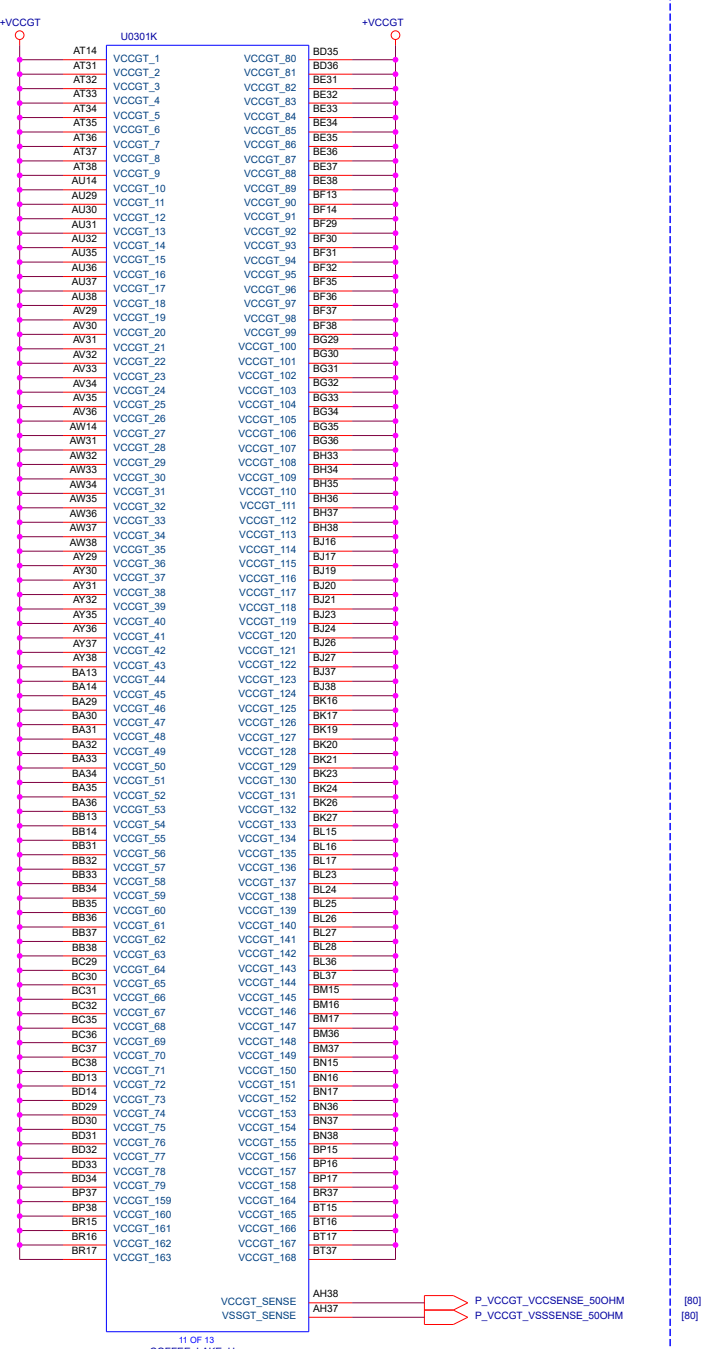


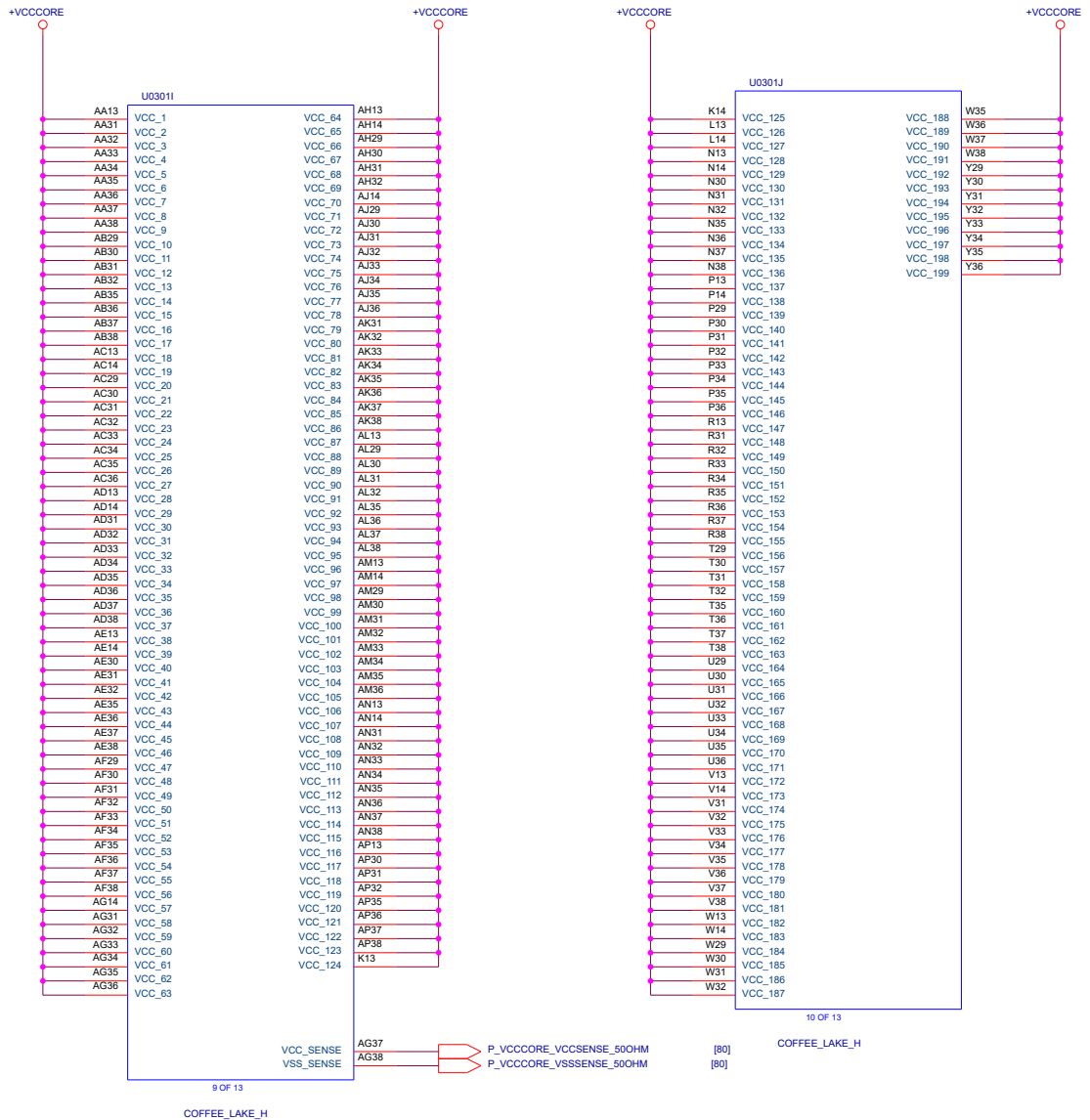
+VCCSA DECAPS Place Back Side (TOP)



+VCCSA near CPU

ASUS	Project Name: G711GW		Rev: 1.0
Title : CPU_PWR			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 8 of 103		





Project Name	G711GW	Rev 1.0
Title :	CPU_PWR	
Size B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 9 of 103	

ASUS	Project Name: G711GW		Rev: 1.0
Title : PCH-CPT(8)_POWER,GND			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 27 of 103		

Project Name

G711GW

Rev

R1.3

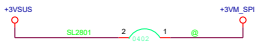
Title : CYPRESS CCG4

Size	Dept.:	Engineer:
D	ASUSTeK COMPUTER	Gaming RD

Date: Wednesday, April 17, 2019

Sheet 12 of 103

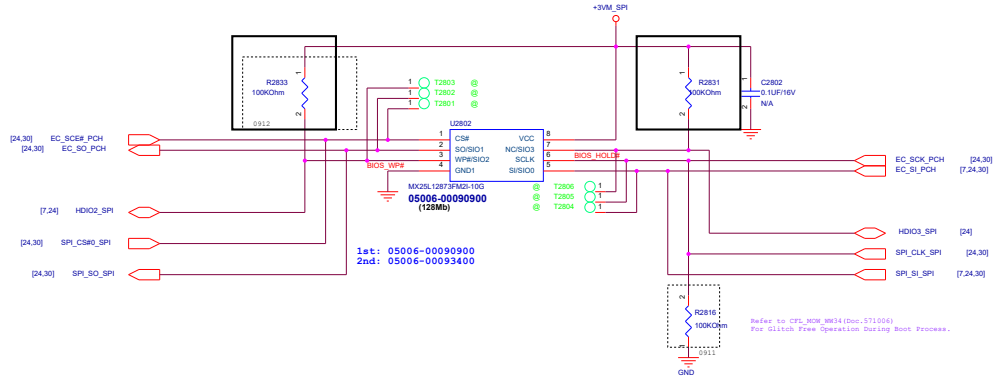
SPI Power



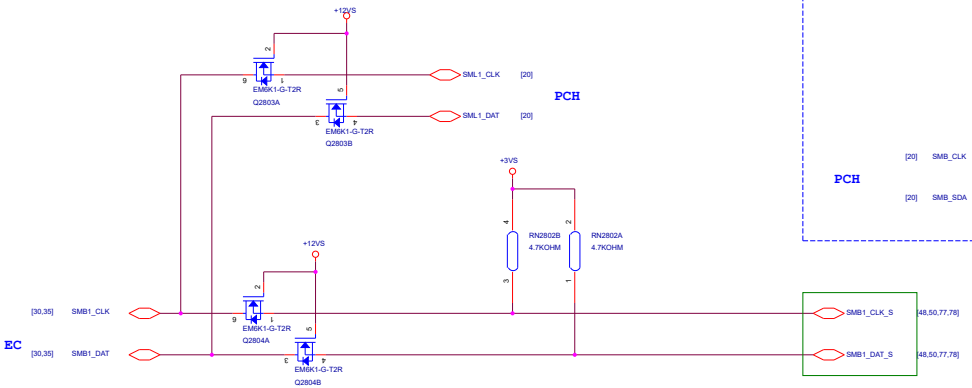
1st SPI ROM

1st: 05006-00090900 FLASH MXIC MX25L12873FM2I-10G 128M SOP-8L
2nd: 05006-00093100 FLASH GD25B127DSIGG IGADEVICE 128MB SOP8

Main Board



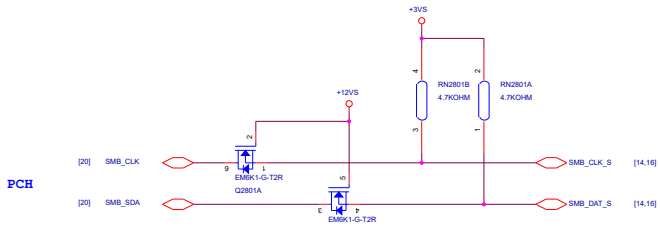
System Management Interface

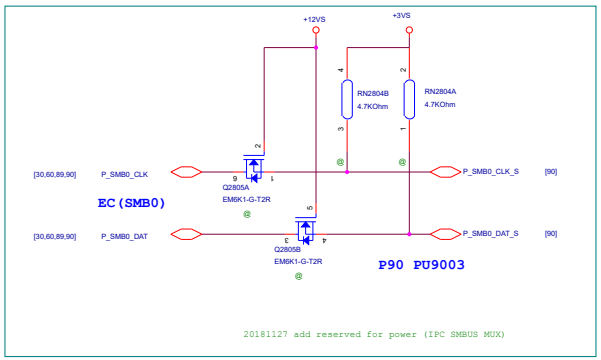


R0.1-13 R1.0-01

CPU,VGA Thermal Sensor
Power Thermal Sensor

SMBus Interface





ASUS	Project Name: G711GW		Rev: 1.0
Title : PCH-SPI ROM,OTH			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 28 of 103		

Main Board

ASUS	Project Name: G711GW	Rev: 1.0
Title : PCH-XDP		
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 29 of 103	

EC 8995

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

ITE Version	ASUS P/N
IT8225VG/BX	06037-00260000

Power

R1.0-29

+3VA_EC, +3VPLL, SL3005, C3051 0.1UF/16V, C3052 0.1UF/16V, C3053 0.1UF/16V, C3054 0.1UF/16V, C3004 0.1UF/16V N/A, C3005 0.1UF/16V N/A, C3007 0.1UF/16V N/A

+3VS_AUD_DVDD, EM6K1-G-T2R Q3003B, EM6K1-G-T2R Q3003A, EC_GPA7, AMP_SLEEP# [36,37]

2017.03.21 AMP Change SNL04M25555

+3VS, +3VPLL, +3VACC, +3VA_EC, 0.1UF/16V C3002 N/A, LCD_BACKOFF# [45]

U3001 IT8225VG-128/CX 06037-00260300

LPC_AD0 [22,44], LPC_AD1 [22,44], LPC_AD2 [22,44], LPC_AD3 [22,44], CLK_KBCPCI_PCH [22], LPC_FRAME# [22,44], BUF_PLT_RST# [24,33,40,53,59,70], INT_SERIRQ [22]

N key

EC_GPG6

DGPU_LIMIT [78], EC_SCK_PCH [24,28], EC_GPG6 [90], EC_SO_PCH [24,28], EC_SI_PCH [7,24,28], EC_SCE#_PCH [24,28]

KSI0_EC [44] … KSI7_EC [44]

KSO0_EC [44] … KSO9_EC [44]

PM_PWRBTN# [7,20], PM_SUSC# [20,86], NKey_INT# [35], CAP_LED# [56]

Battery: P_SMB0_CLK [28,60,89,90], P_SMB0_DAT [28,60,89,90]

GX501VS remove PS2

Thermal sensor: PWR_SW# [7,31,32,56], PS_ON_EC [32], SMB1_CLK [28,35], SMB1_DAT [28,35], PECI_EC [6], PCH_SPI_OV [20]

PWR_LED [56], CHG_LED# [56], CHG_FULL_LED# [56], FAN1_PWM [50], FAN0_PWM [50], AC_IN_OC# [89], LID_SW# [31,56], BAT1_IN_OC# [89], NKEY_PWR_EN [35], MF_AC_PRESENT [20], OP_SD# [36,37], FAN0_TACH [50], FAN1_TACH [50], SUSB_EC# [45,57,70,88], SUSC_EC# [38,57], 5VSUS_ON [87], 1.2V_ON [86], VSUS_ON [57,83,84,88], 3VADSW_ON [57,87], WLAN_PWR_EN [53], THRO_CPU# [6], PCH_SUSACK# [20], PM_SUSB# [20,57,58,70,88,98], PM_CLKRUN# [20], SMB3_CLK, SMB3_DAT, PM_RSMRST# [7,20], DPWROK_EC [20,58], PM_PWROK [20], PM_SYSPWROK [7,20], PM_SLP_SUS# [20], 3VSUS_PWRGD [58,83,84], ALL_SYSTEM_PWRGD [6,20,58,59,80], IMVP8_PWRGD [20,59,80], SUSWARN# [20], P_IMVP8_PSYS_INFO [80,89], GC_STATE_EC [70], PD1_I2C_INT_EC, EC_GPJ5

3VA_DSW_PWRGD_EC, EC_GPJ0

C3016 N/A 0.1UF/16V close to U3001.E6

C3008 0.1UF/16V N/A, C3015 0.1UF/16V N/A, SL3006, EC_GAND 單點下地

C3019 @EMC 0.1UF/25V PM_PWROK

R1.0-34

+3VA_DSW, R3055 100KOhm, 3VA_DSW_PWRGD; +3VS, R3054 100KOhm, IMVP8_PWRGD; @ SL3011 3VA_DSW_PWRGD_EC → 3VA_DSW_PWRGD [20,58,87]

EMI-GX501GI

C3003 EC_RST# 100PF/50V
C3009 BUF_PLT_RST# @EMI 100PF/50V
C3011 RC_IN# @EMI 100PF/50V
C3012 3VA_DSW_PWRGD_EC @EMI 100PF/50V
C3013 3VSUS_PWRGD @EMI 100PF/50V
C3014 3VA_DSW_PWRGD @EMI 100PF/50V
GND

For EMI

C3025 CHG_FULL_LED# 100PF/50V
C3026 PWR_LED 100PF/50V
C3027 CHG_LED# 100PF/50V
C3028 MF_AC_PRESENT 100PF/50V
@EMI

C3018 CLK_KBCPCI_PCH 8.2PF/50V
C3010 PWR_SW# 0.01UF/25V

PU/PD

THRO_CPU# R3032 10KOhm, NKey_WRST R3050 10KOhm N/A, R3013 N/A 10KOhm

PWR_SW# R3037 100KOhm, AC_IN_OC# R3026 100KOhm, LID_SW# R3063 100KOhm

CHG_LED# R3043 10KOhm, CHG_FULL_LED# R3044 10KOhm, EC_GPA7 R3027 100KOhm, EC_GPG2 R3021 100KOhm

SMB1_DAT RN3001A 2.7KOHM, SMB1_CLK RN3003B 2.7KOHM, P_SMB0_CLK RN3003A 2.7KOHM, P_SMB0_DAT RN3002B 2.7KOHM, SMB3_DAT RN3002A 2.7KOHM, SMB3_CLK R3007 100KOhm, PD1_I2C_INT_EC

3VADSW_ON R3053 100KOhm, 5VSUS_ON R3006 100KOhm, R3056 1MOHM, VSUS_ON R3051 100KOhm, R3030 1MOHM

for load code

TP_DAT RN3004A 4.7KOHM, TP_CLK RN3004B 4.7KOHM

PM_PWRBTN# R3041 10KOhm, RC_IN# R3003 10KOhm N/A

BAT1_IN_OC# R3065 100KOhm, N501, R3008 100KOhm

20170901

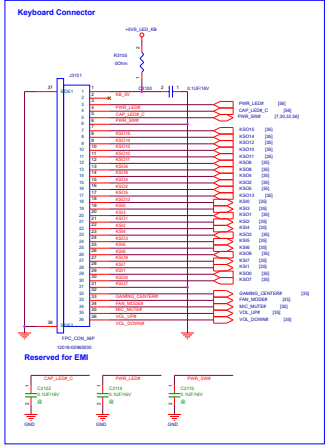
PM_SLP_SUS# R3019 100KOhm, PM_SUSC# R3004 100KOhm, PM_SUSB# R3005 100KOhm, SUSB_EC# R3092 4.7KOhm, SUSC_EC# R3001 4.7KOhm, WLAN_PWR_EN R3015 100KOhm, PM_RSMRST# R3058 10KOhm, PM_SYSPWROK R3022 100PF/50V, DPWROK_EC R3023 100PF/50V, SUSWARN# R3024 680PF/50V, 3VADSW_ON R3039 100KOhm, GC_STATE_EC C3001 15PF/25V

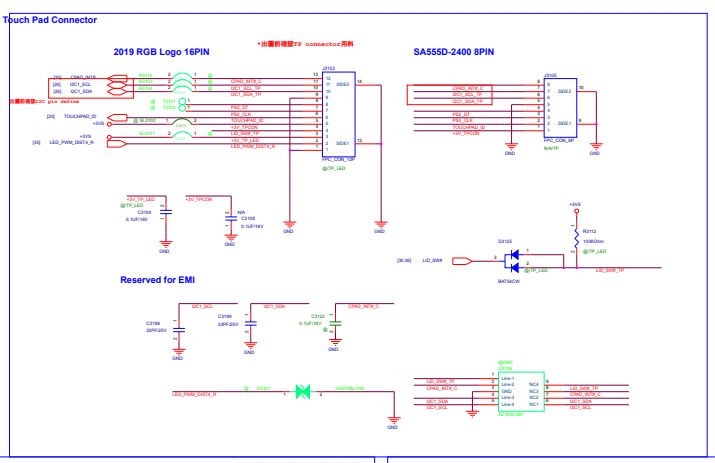
C3029 680PF/50V, C3006 100PF/50V

<Variant Name>

ASUSTeK COMPUTER

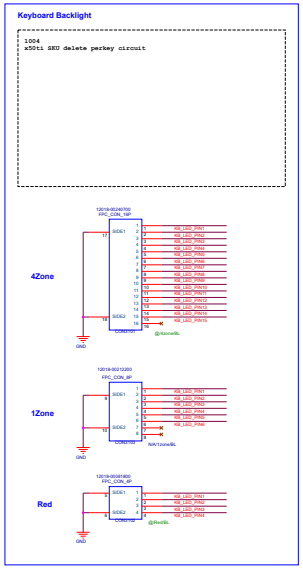
Title : CR_KBC_IT8521
Engineer: Gaming RD
Size C | Project Name G711GW | Rev 1.0
Date: Wednesday, April 17, 2019 | Sheet 30 of 103

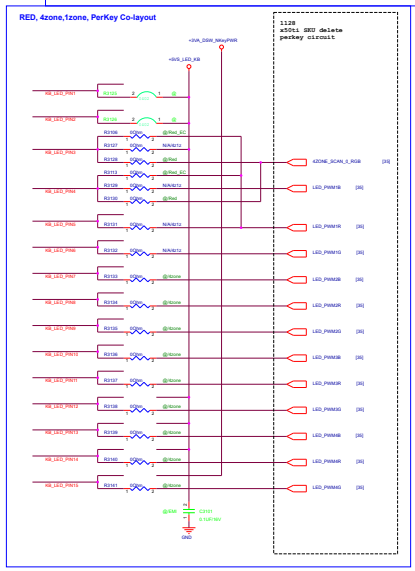


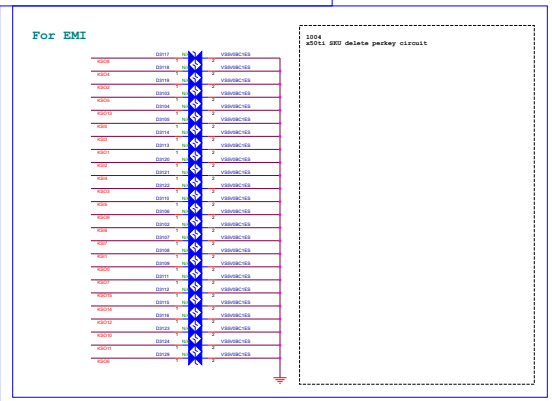


G531GT P.31 差異

MP_60_PN	PCB	J3102	J3105	C3104	D3125	R3112
60NR01L0-MB3010	R1.4	12018-00102300	NA	11G23210411360	07G004069020	10G212100314010
60NR01L0-MB3210	R1.4	12018-00102300	NA	11G23211041360	07G004069021	10G-02147483648
60NR01L0-MB3310	R1.4	NA	12018-00212200	NA	NA	NA
60NR01L0-MB3410	R1.4	NA	12018-00212200	NA	NA	NA
60NR01L0-MB3110	R1.4	NA	12018-00212200	NA	NA	NA

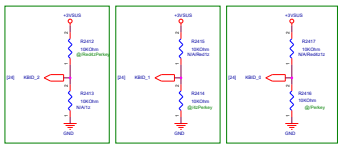






	RED-4pin	1zone RGB_8pin	4zone-16pin	per key-20pin
pin1	VCC	VCC green	VCC green	COM7
pin2	VCC	VCC red	VCC red	COM6
pin3	GND	VCC blue	VCC blue	COM5
pin4	GND	LED1 blue	LED1 blue	COM4
pin5		LED1 red	LED1 red	COM3
pin6		LED1 green	LED1 green	COM2
pin7		NC	LED2 blue	COM1
pin8		NC	LED2 red	COM0
pin9			LED2 green	GND
pin10			LED3 blue	GND
pin11			LED3 red	GND
pin12			LED3 green	VCC
pin13			LED4 blue	VCC
pin14			LED4 red	VCC
pin15			LED4 green	VDD-33
pin16			NC	NC
pin17				GCLK
pin18				SDI
pin19				DCLK
pin20				LE

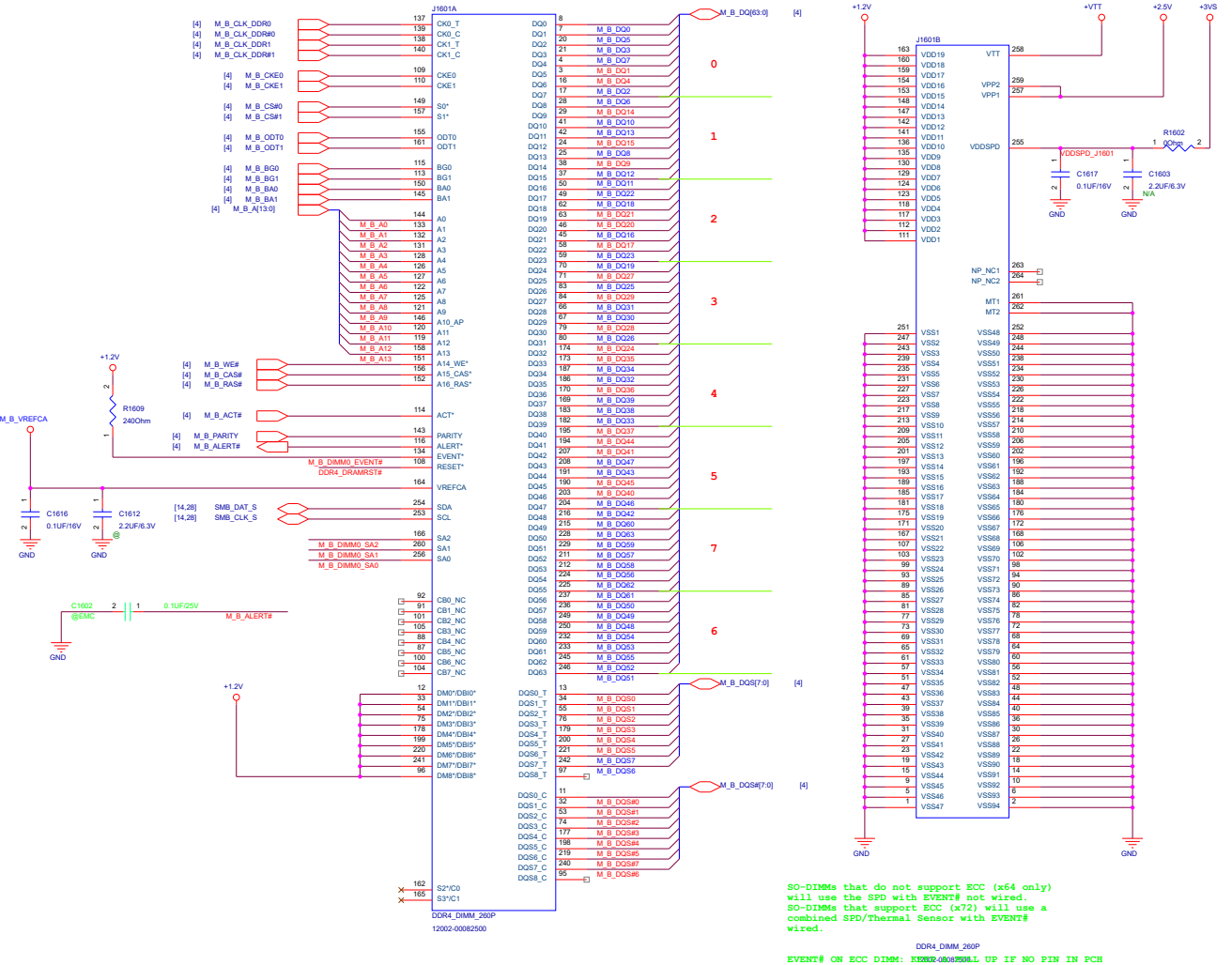
Keyboard ID



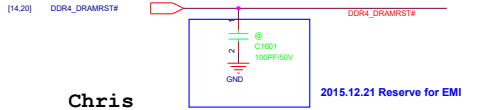
KB ID PCH Side(HW請依照此表格做設計判斷) *BIOS會再反向

Code	ROG RGB KB Type	KBID 2 (GPP_H18)	KBID 1 (GPP_H17)	KBID 0 (GPP_H16)
0x00	Normal Keyboard	H	H	H
0x01	QWERASD Partition Keyboard	H	H	L
0x02	4 Zone RGB Keyboard	H	L	H
0x03	Per Key RGB Keyboard	H	L	L
0x04	1 Zone RGB Keyboard	L	H	H

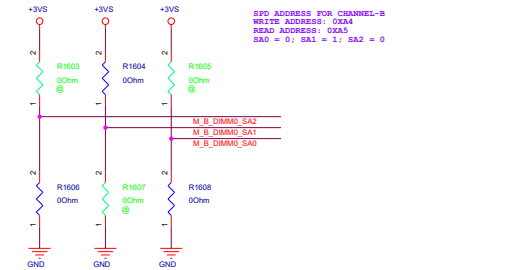
SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)



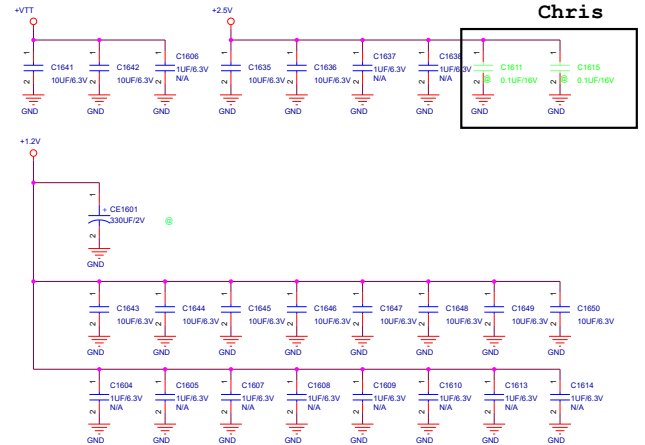
Main Board



Chris



Chris



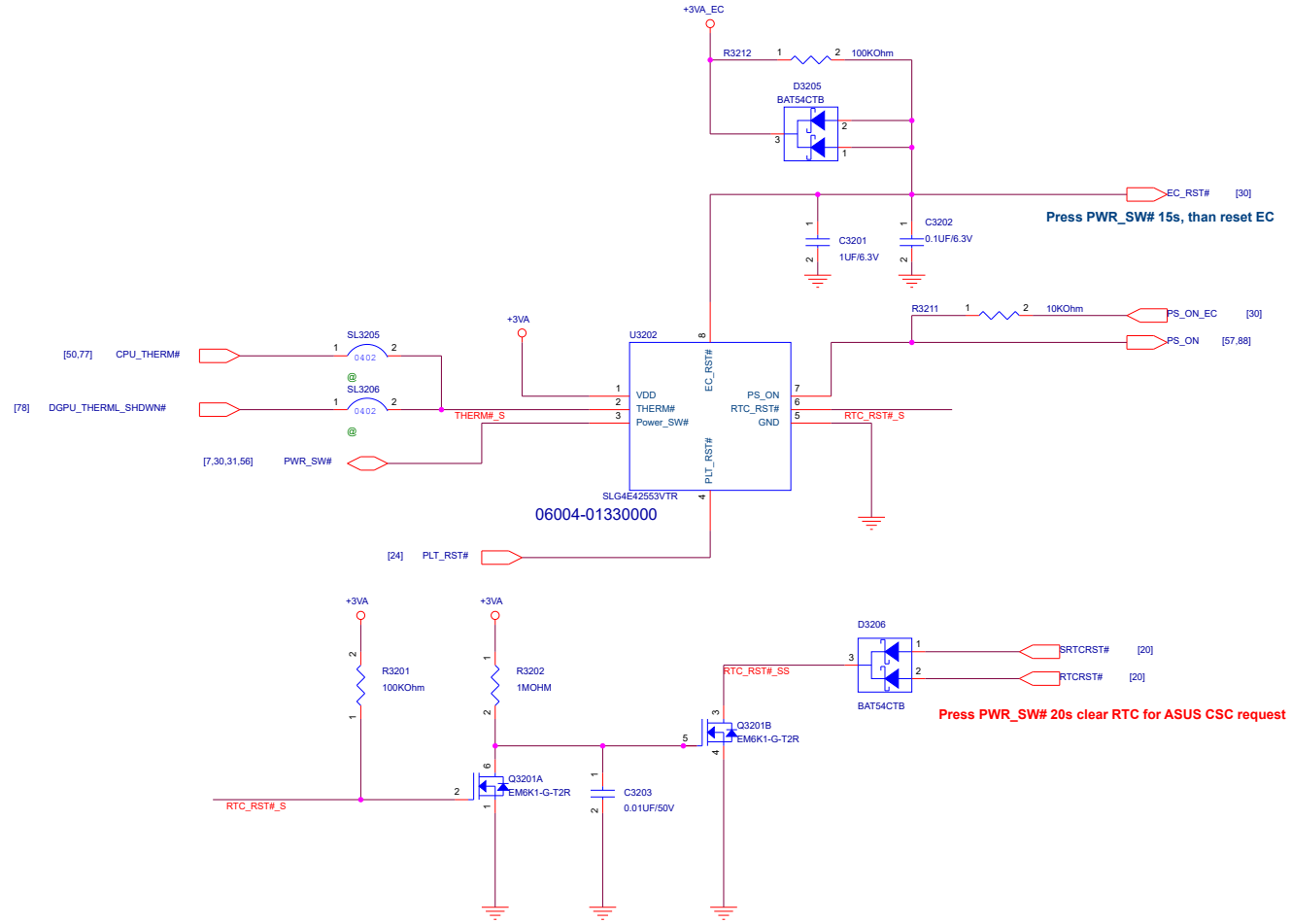
ASUS	Project Name: G711GW	Rev: 1.0
Title :	DIM_DDR4 SO-DIMM B1	
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 16 of 103	

Modern standby project should use Silego solution for EC/RTC reset (Microsoft hardware requirements)

6.6.2 Power button behavior

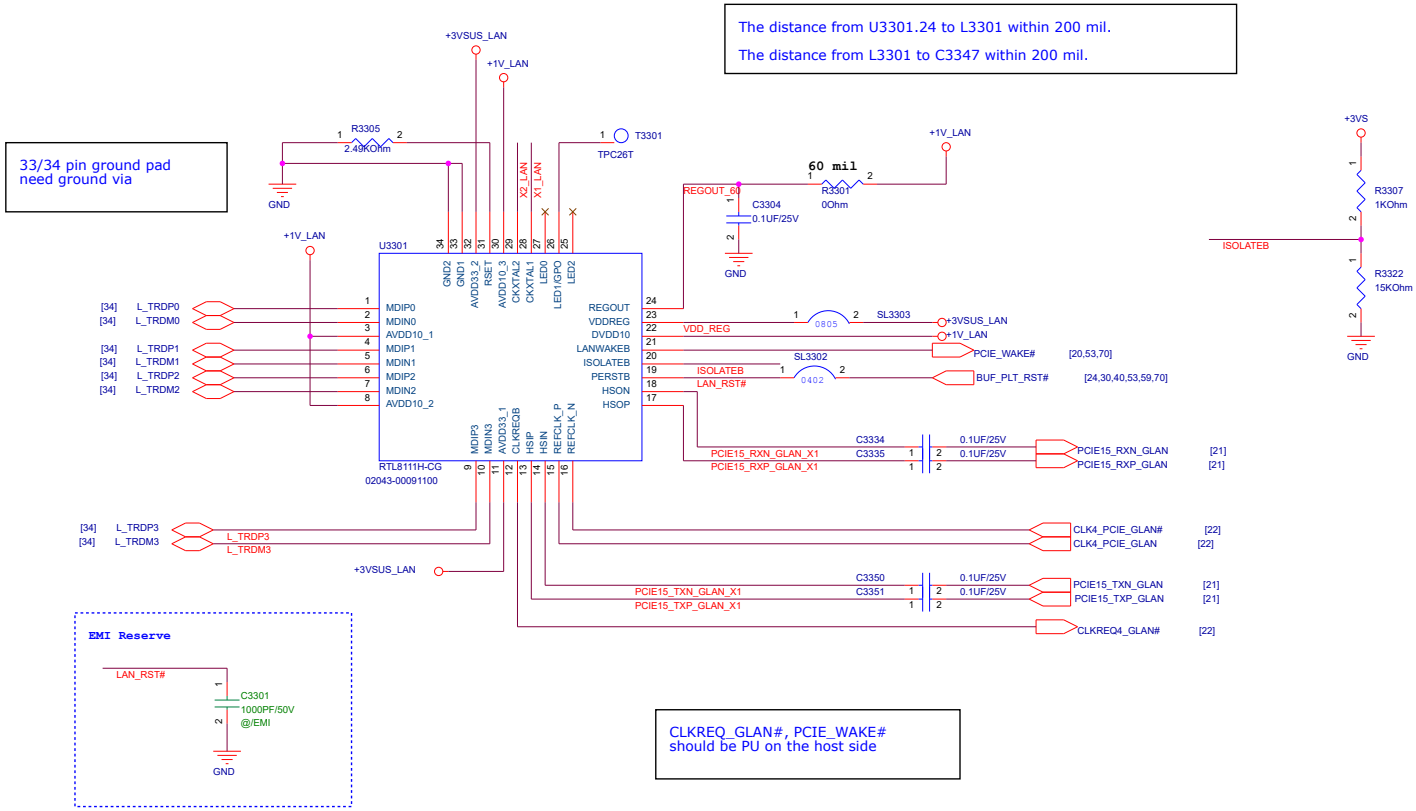
https://docs.microsoft.com/en-us/windows-hardware/design/minimum/minimum-hardware-requirements-overview#section-60---shared-minimum-hardware-requirements-for-components

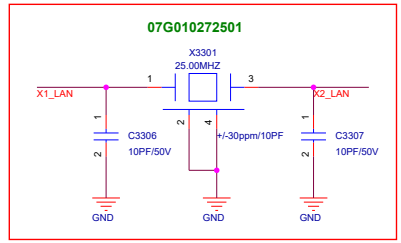
UX362FA R1.3 board will verify this circuit 7/E



<Variant Name>

ASUSTeK COMPUTER	Title : RST_Reset Circuit	
	Engineer: Gaming RD	
Size: B	Project Name: G711GW	Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 32 of 103	



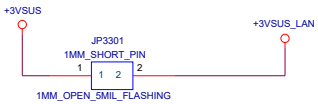


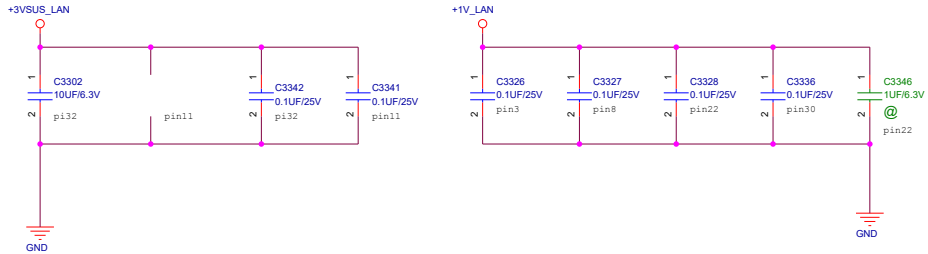
X3301: 25MHZ +/-30ppm/10pF (3225)

1st: P/N:07G010272501 TXC/7V25000011

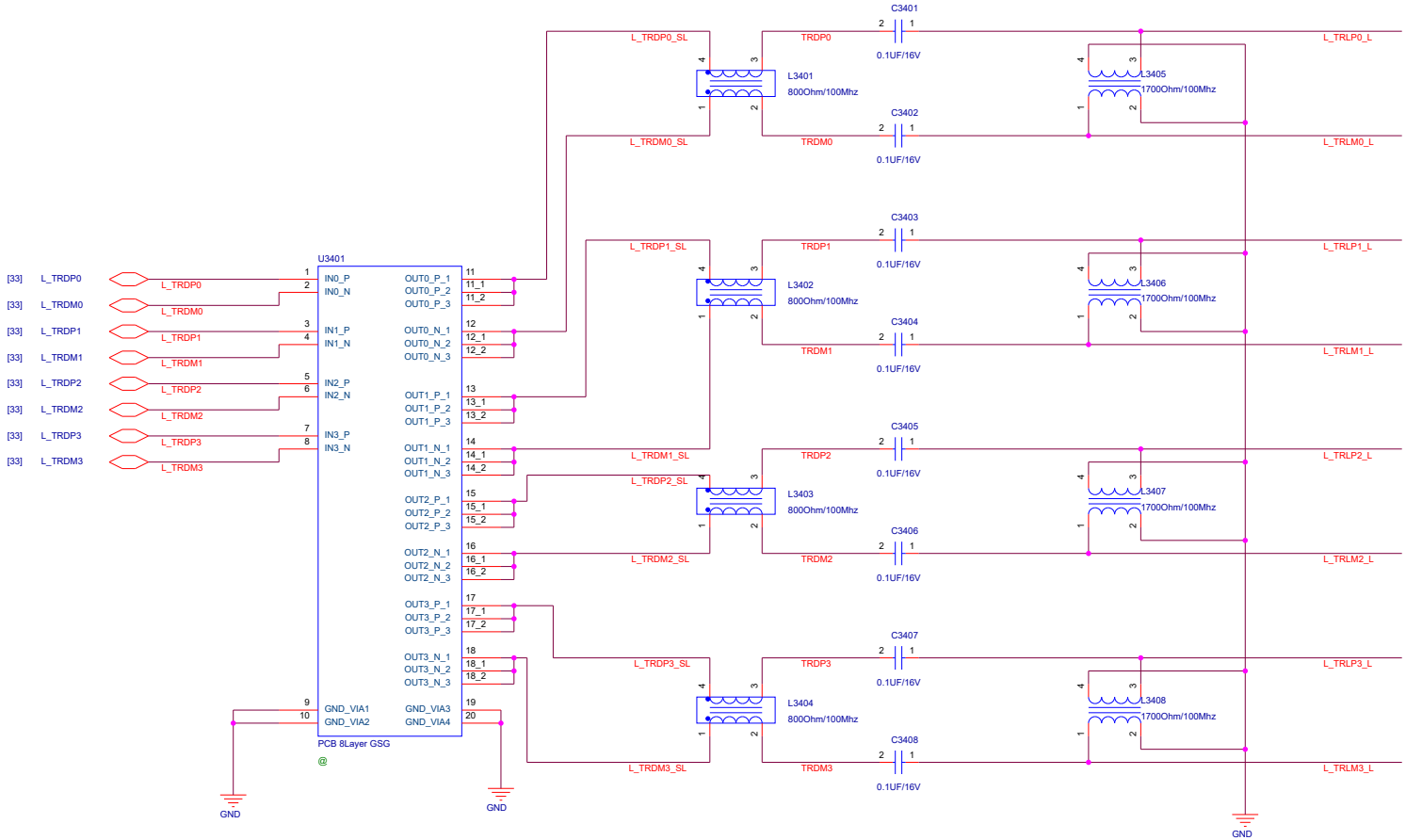
2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms

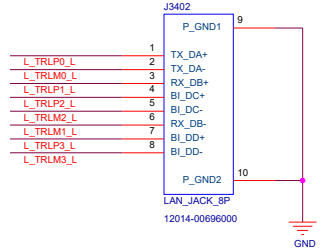


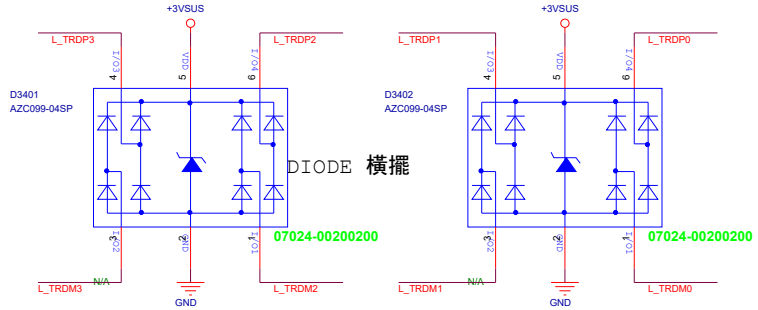


Project Name: GX502GX			Rev: 1.0
Title: LAN RTL8111GUX-CG			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1	
Date: Wednesday, April 17, 2019	Sheet 33 of 103		



LAN Connector





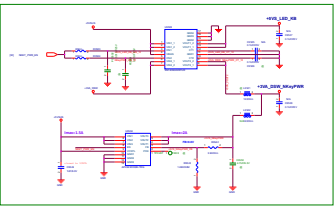
D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

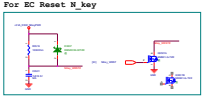
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

ASUS	Project Name: GX502GX		Rev: 1.0
Title : LAN_RJ45_CON			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: NB1 RD2 EE1	
Date: Wednesday, April 17, 2019	Sheet 34 of 103		

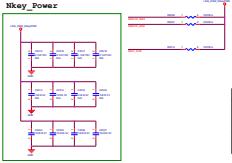
N_KEY_IT8299E



For EC Reset N_key



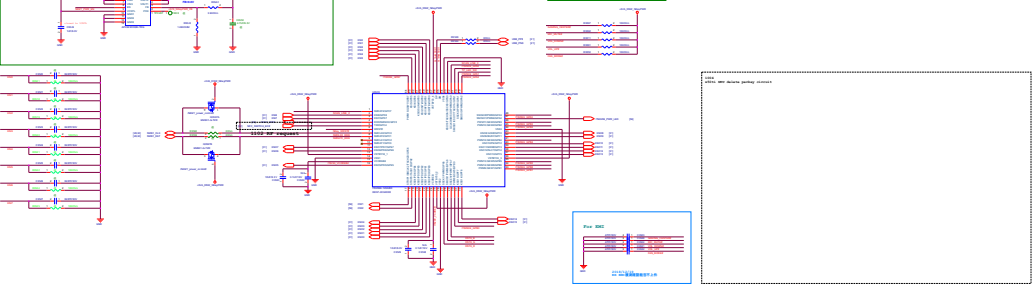
Nkey_Power



GS31GF P_35 版具

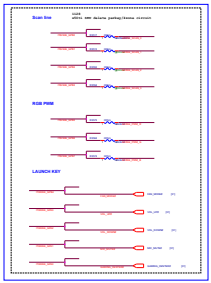
MP SN P/N	PCB	Sticker
69N0J1L12-MB3S10	R1.0	1S52123035140S10
69N0J1L12-MB3S20	R1.0	1S52123035140S10
69N0J1L12-MB3S30	R1.0	NA
69N0J1L12-MB3S40	R1.0	NA
69N0J1L12-MB3S50	R1.0	NA

IT8299E

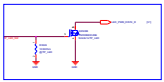


KB RGB Per Key LED

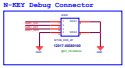
KB RGB co-layout



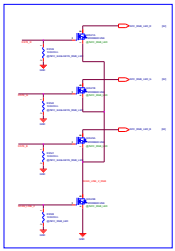
TP LED



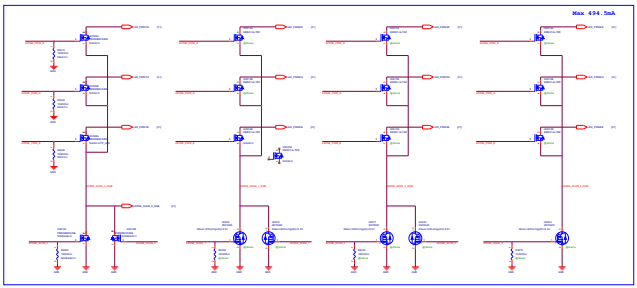
N-KEY Debug Connector



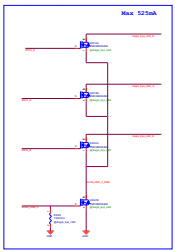
NFC RGB LED



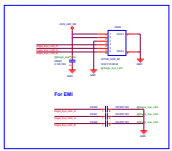
KB RGB 4Zone and 1Zone LED



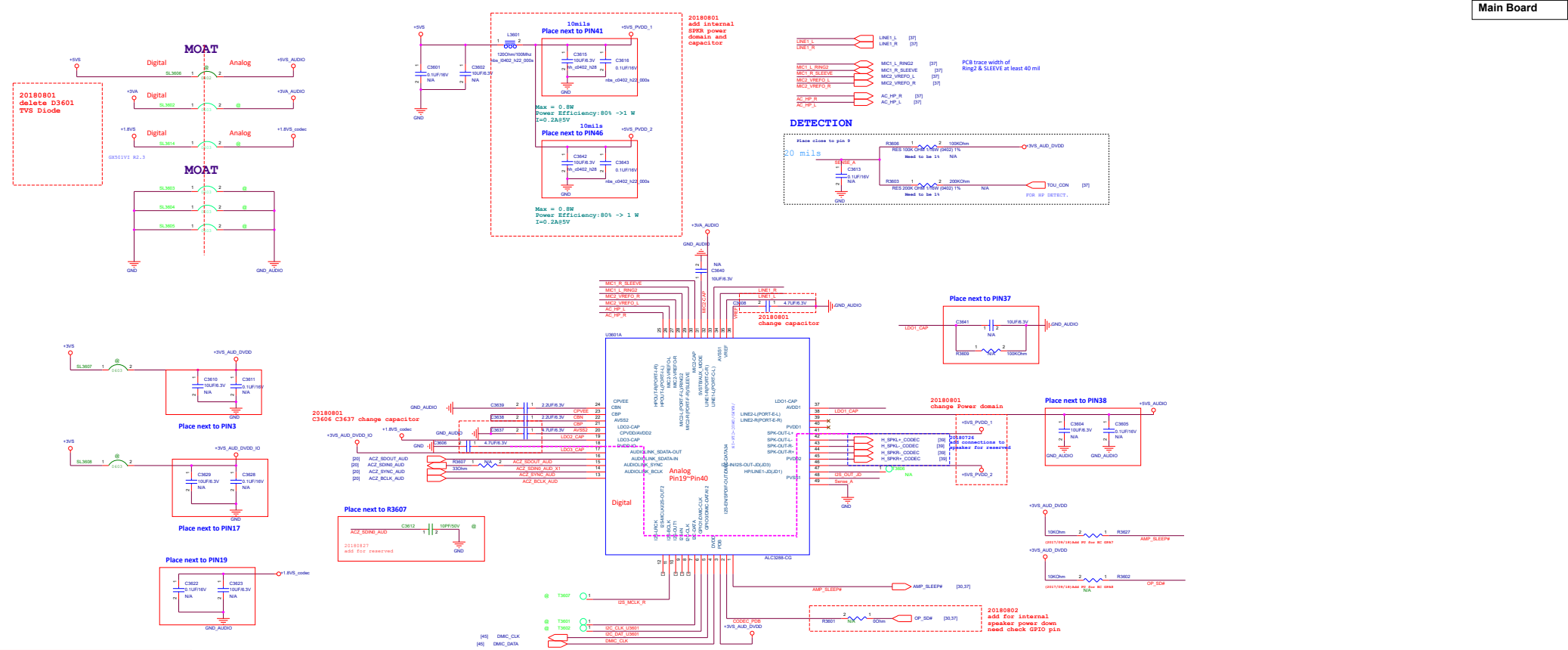
Eagle Eye LED



Eagle Eye LED Conn



Title :		LOC REV:	
Engineer:		Gaming NB	
Size	Document Number		Rev
	GS31GNR		
Date:	Sheet of		



DVDD must lead AVDD2. Figure 4 illustrates the recommended power sequence.

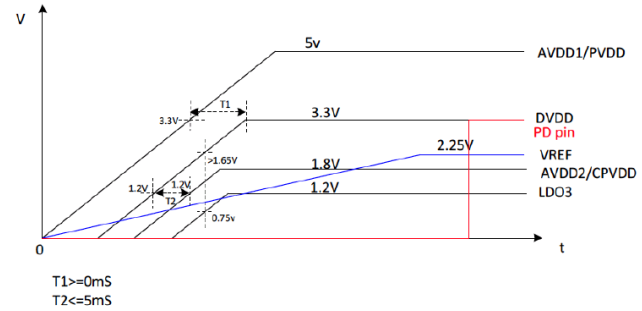
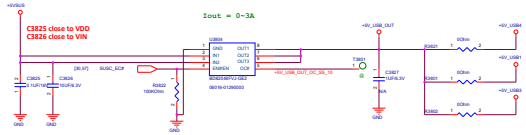


Figure 4. Power sequence

ASUS	Project Name: G711GW	Rev: 1.0
Title :	AUDIO ALC3236-CG/VB2	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li
Date: Wednesday, April 17, 2019	Sheet 36 of 103	



Chris

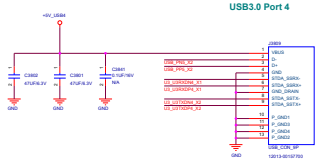
USB3.0_PORT4 (Support USB Charge Circuit)

J3809 USB3.0 Connector

1st Source: P/N:12013-00018300 FOXCONN/UEA1111-N40AM2-7H

2nd Source: P/N:12013-00080400 SINGATRON/2UB4006-310101F

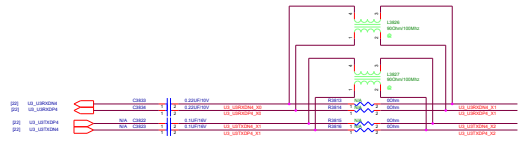
USB3.0 Port 4



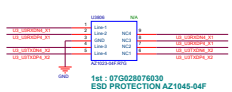
USB3.0 Pin define	
1	VBUS
2	D-
3	D+
4	GND
5	RX-
6	RX+
7	GND
8	TX-
9	TX+

USB Charge Circuit (For PORT 4)

USB3.0_PORT4

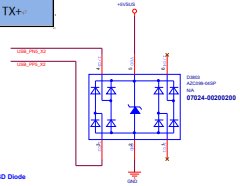


USB3.0 ESD-Protection



1st : 07G028076030
ESD PROTECTION AZ1045-04F

2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB



D3802 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

ASUSTeK COMPUTER	Title :	Aud_HP Jack, MIC	
	Engineer:	Gaming RD	
Size: D	Project Name: G711GW		Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet	38 of	103

20180801
delete 0ohm

[36] H_SPKR+_CODEC
[36] H_SPKR-_CODEC
[36] H_SPKL+_CODEC
[36] H_SPKL-_CODEC

L3901 1 2 120Ohm/100MHz
L3902 1 2 120Ohm/100MHz
L3903 1 2 120Ohm/100MHz
L3904 1 2 120Ohm/100MHz

Max = 8W / Channel (@PVDD=12V)
I = 1.57A (@Speaker : 8 Ohm)
Efficiency=90% @ 8W

SPK L+ L- R+ R- trace width
Speaker 8 ohm ==> 30 mils

H_SPKR+_CON
C3948 1000PF/50V N/A
GND
C3950 1000PF/50V N/A
H_SPKR-_CON
H_SPKL+_CON
C3951 1000PF/50V N/A
GND
C3953 1000PF/50V N/A
H_SPKL-_CON

D3901 @EMC
H_SPKR+_CON
ESD9B5.0ST5G

D3902 @EMC
H_SPKR-_CON
ESD9B5.0ST5G

D3903 @EMC
H_SPKL-_CON
ESD9B5.0ST5G

D3904 @EMC
H_SPKL+_CON
ESD9B5.0ST5G

GND

INTERNAL SPK Conn.

Speaker = 1.5W / channel

Check Pin1

J3901
4 SIDE2
3
2
1 SIDE1
6
5
H_SPKR+_CON
H_SPKR-_CON
H_SPKL-_CON
H_SPKL+_CON
WTOB_CON_4P
12017-00072500

1113 change connector

GND

<Variant Name>

ASUSTeK COMPUTER INC. NB1

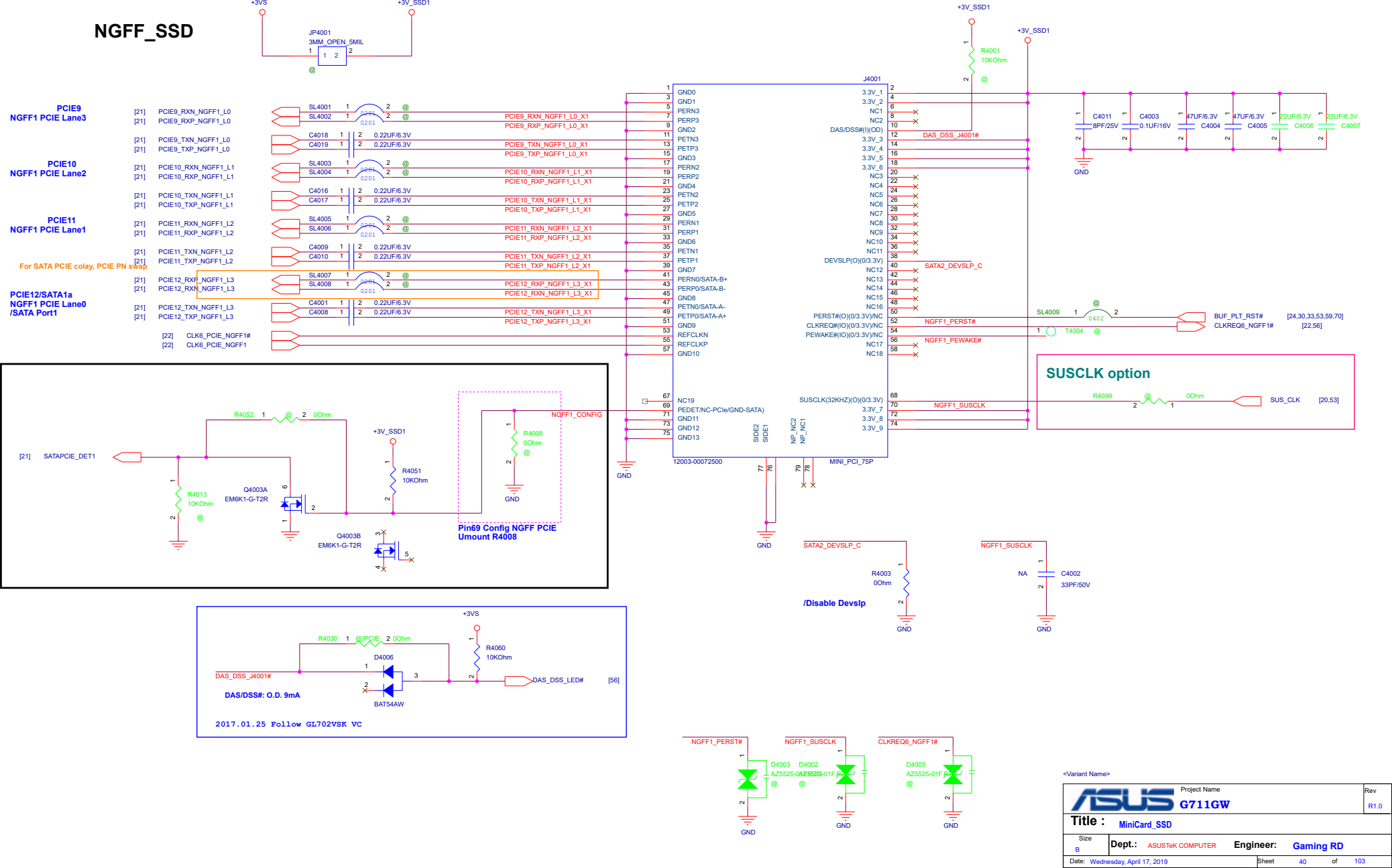
Title : Aud_Woofer_**

Engineer: EE

Size	Project Name	Rev
B	G711GW	1.0

Date: Wednesday, April 17, 2019 Sheet 39 of 103

NGFF_SSD



<Variant Name>

Project Name: G711GW		Rev: R1.0
Title : MiniCard_SSD		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 40 of 103	

<Variant Name>

Title : CB_*****

ASUSTeK COMPUTER

Engineer: Gaming RD

Size	Project Name	Rev
C	G711GW	1.0

Date:	Wednesday, April 17, 2019	Sheet	41	of	103

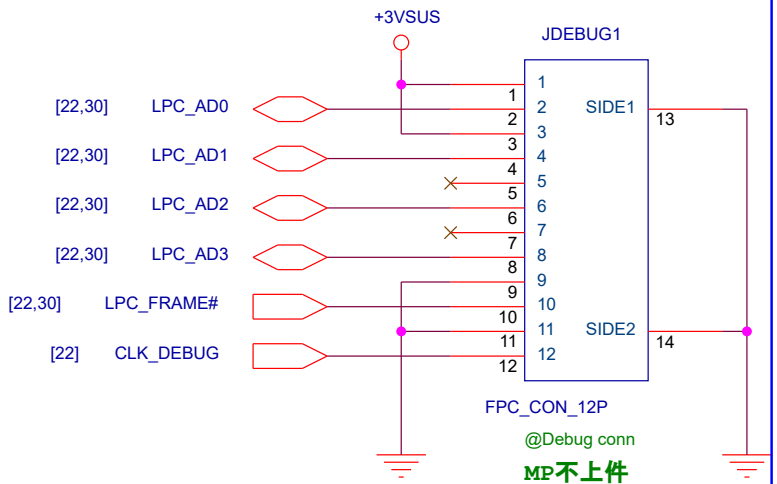
ASUSTeK COMPUTER	Title :	HDMI_DP_Switch	
	Engineer:	Gaming RD	
Size: C	Project Name: G711GW		Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 42 of 103		

Main Board

ASUS	Project Name: G711GW	Rev: 1.0
Title : CB IO CON		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 43 of 103	

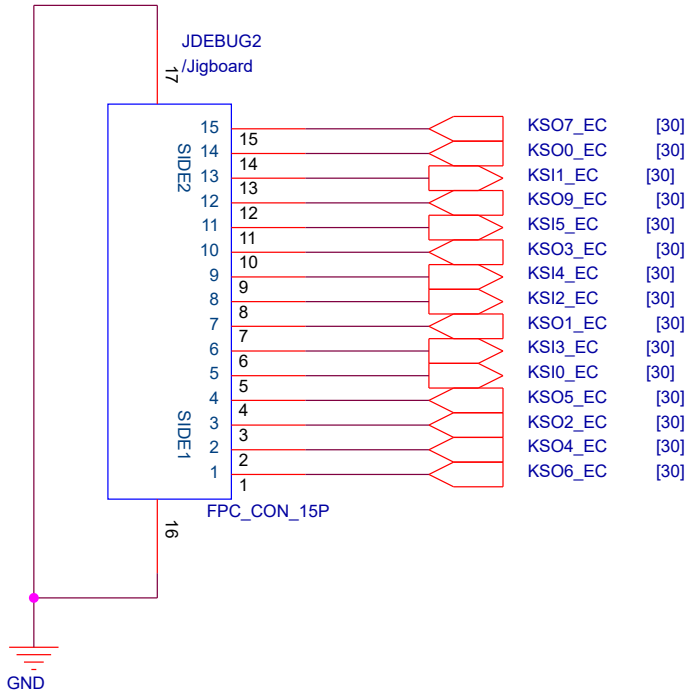
2017/11/10

LPC Debug Port



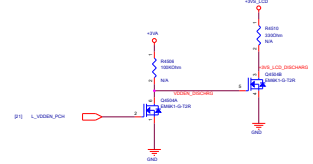
ER2 stuff

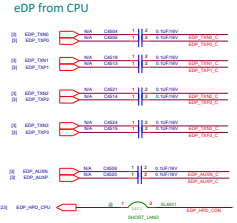
2017/11/10

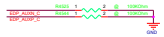


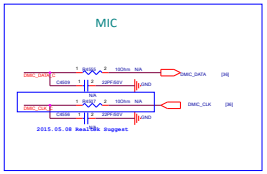
<Variant Name>

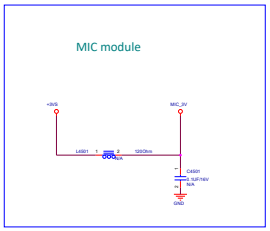
ASUSTeK COMPUTER	Title : DEBUG_LPC	
	Engineer: Gaming RD	
Size: A	Project Name: G711GW	Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 44 of 103	

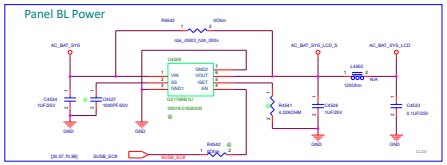


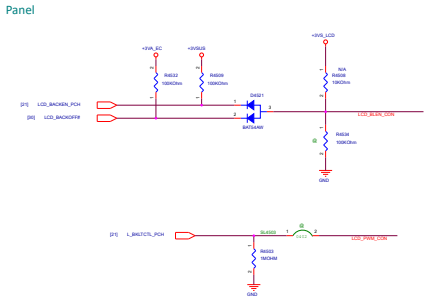


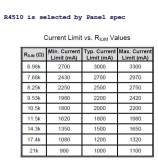


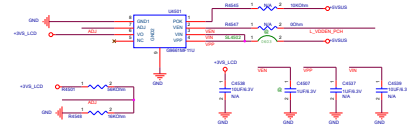


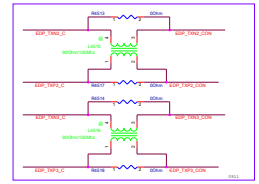


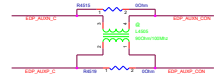


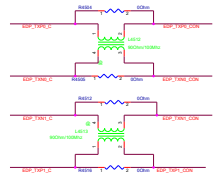


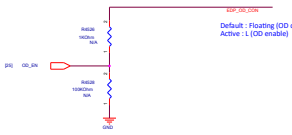


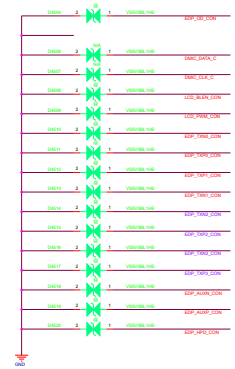


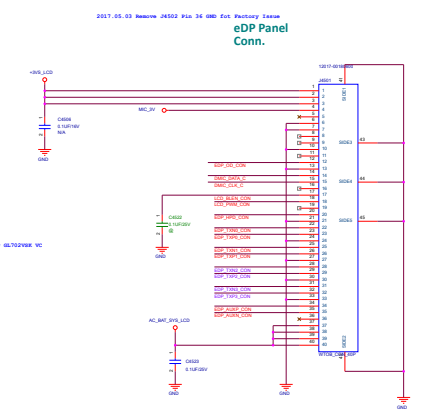












Variant Name:

Title :	CRT_eDP	
Engineer:	Gaming RD	
Size: D	Project Name: G711GW	Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 46 of 100	

Main Board

ASUS	Project Name: G711GW			Rev: 1.0
Title : PD_IT8851FN				
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Wendell_Lo		
Date: Wednesday, April 17, 2019		Sheet 46	of	103

Main Board

Internal Regulator option

LDO OUT

LDO IN

20180813
change to +1.8VS for improving transfer efficiency

20180815
SL4801: bead change to shortland

C4811 close to IC as close as possible

C4815 close to IC as close as possible

20180815
delete short land

HDMI Active-Level Shift

HDMI PWR_+5VS_HDMI

HDMI Conn.

20180810
change to 2K ohm

20180810
delete 0ohm

20180810
R4816 change to 47kohm

20180731
change HDMI retimer to IT66317

20180813
最高设置成I2C盖用不同
最大盖用在Cable/box才需接TX

IFW update path

HDMI EMI

20180813
add 0ohm and choke umount

N56V C.M Choke : M 09G092090110

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Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

20180810
add 10K pull-up

PCADR: Control of serial programming device address
0:0x78 (defaul , internal pull down)
1:0x7A

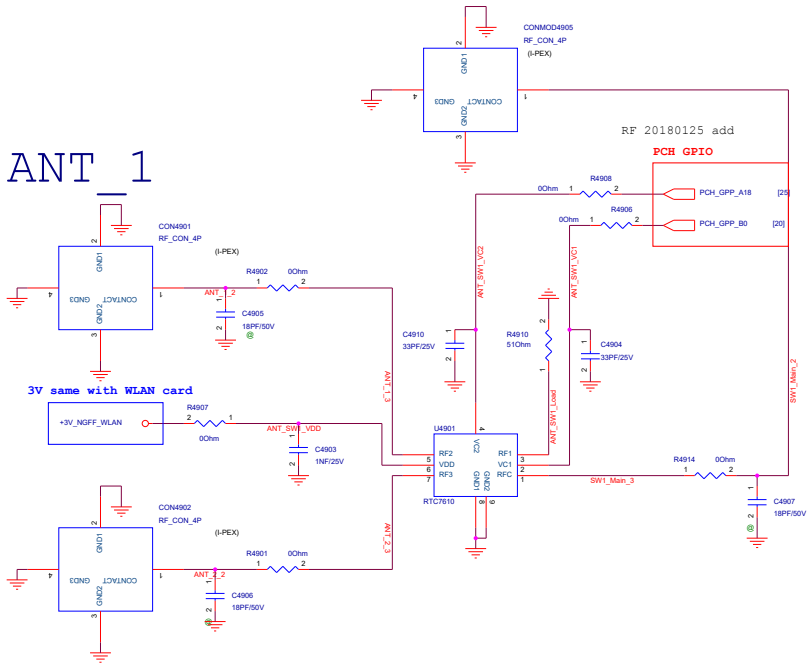
20180807
add for output swing HW control

Project Name	G711GW
Rev	1.3
Title :	HDMI
Size	Custom
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	EE1_RD3
Date:	Wednesday, April 17, 2019
Sheet	48 of 103

G531GT P.49 差異

MP 60 PN	PCB	All pages' components
60NR01L0-MB3010	R1.4	mount
60NR01L0-MB3210	R1.4	mount
60NR01L0-MB3310	R1.4	mount
60NR01L0-MB3410	R1.4	mount
60NR01L0-MB3110	R1.4	unmount

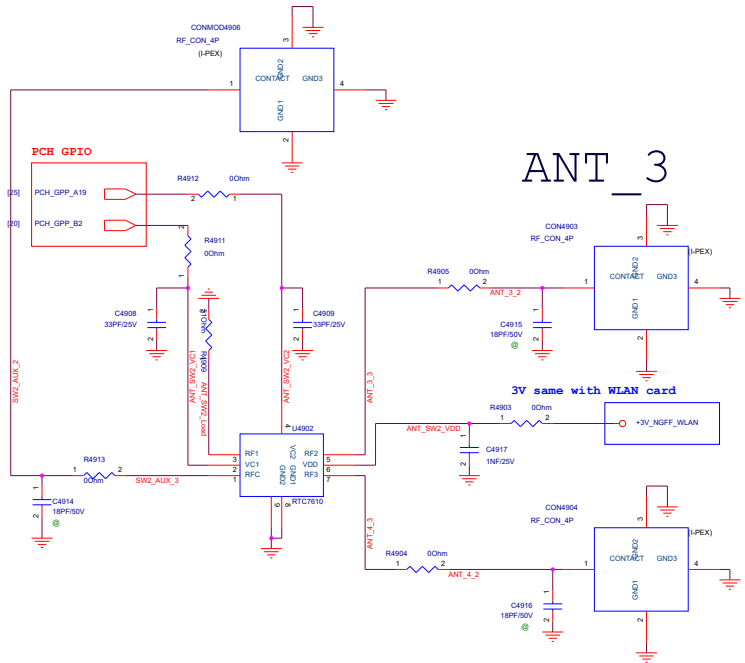
Module_AUX



U4901 RTC7610			
ANT	Port	VC1 GPP_B0	VC2 GPP_A18
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

Module_MAIN



U4902 RTC7610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Ω	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

<Core Design>

ASUS	Project Name: GX502GX	Rev: 1.0
Title : ANT		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, April 17, 2019	Sheet 49 of 103	

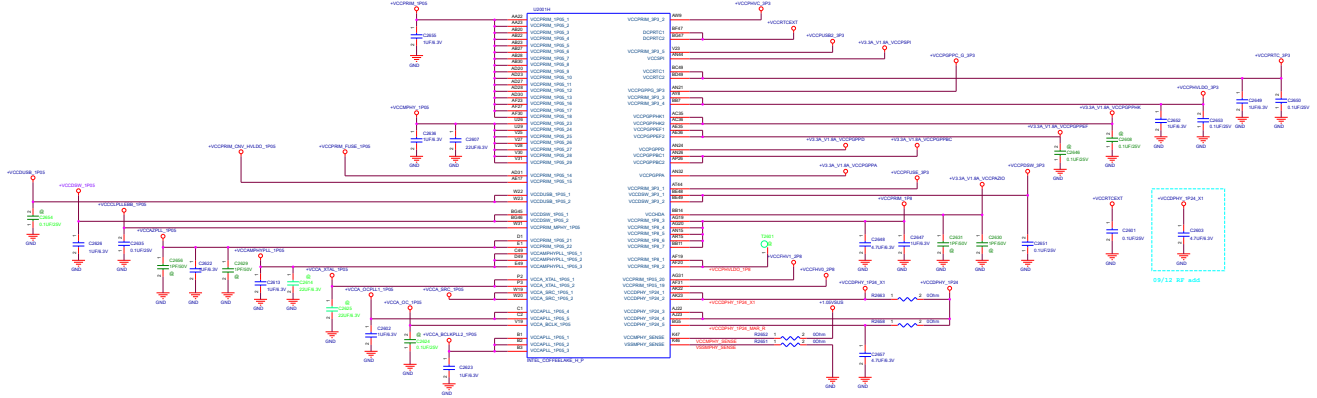
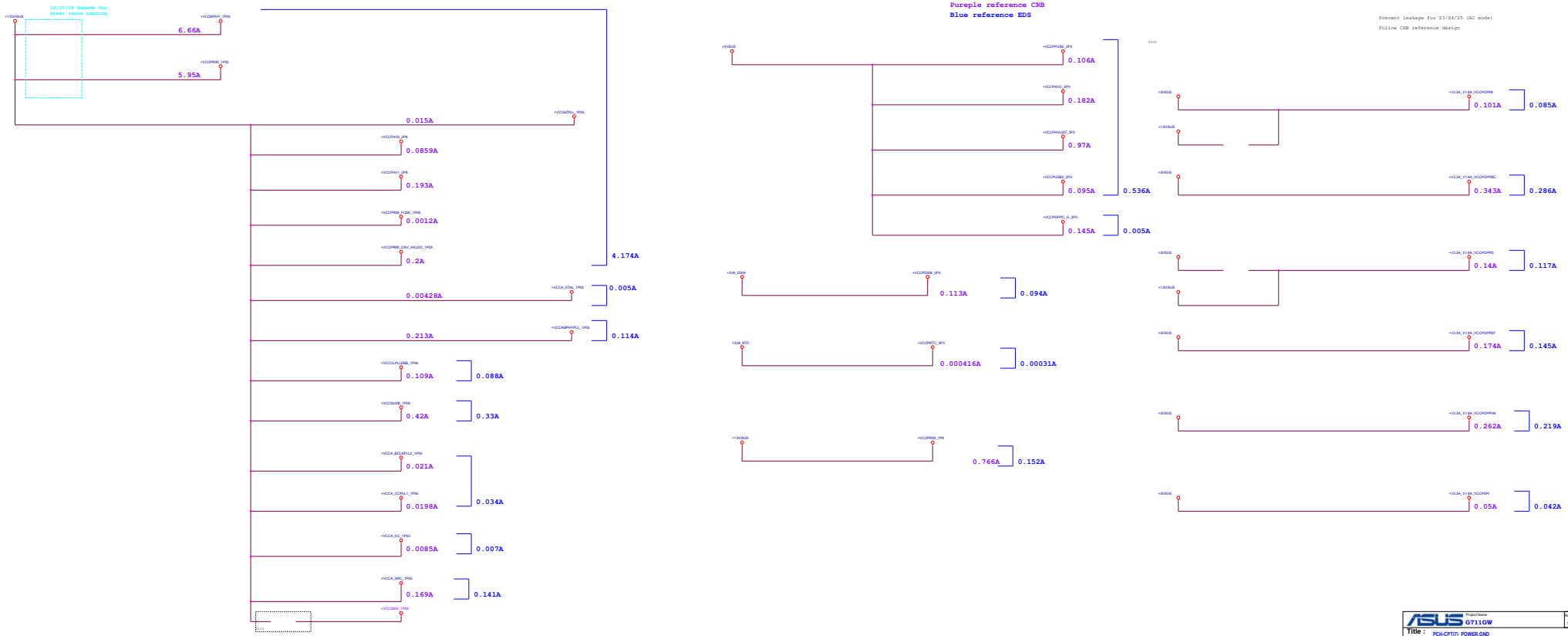


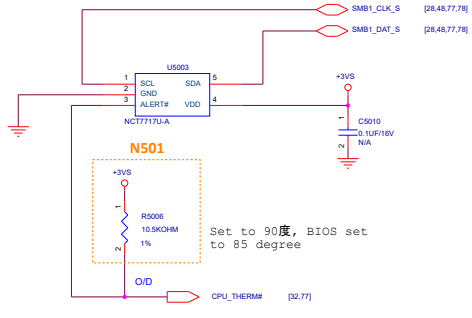
Table 8-1. Power Descriptions for PCH in CNL-H

Name	Description
VCCPHVLDO_1P8	**1.8V Primary Well.** On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	1.8V or 3.3V for GPP_A group.
VCCPGPPBC	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCPGPPD	1.8V or 3.3V for GPP_D group.
VCCPGPPEF	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCPGPPG_3P3	3.3V for GPP_G group.
VCCPGPPHK	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
VSSMPHY_SENSE	0V (Ground) Sense Line.
VSS	Ground.



ASUS	Project Name: G711GW		Rev: 1.0
Title: PCH-CPT(7)_POWER,GND			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 26 of 103		

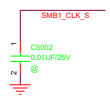
CPU Thermal Sensor



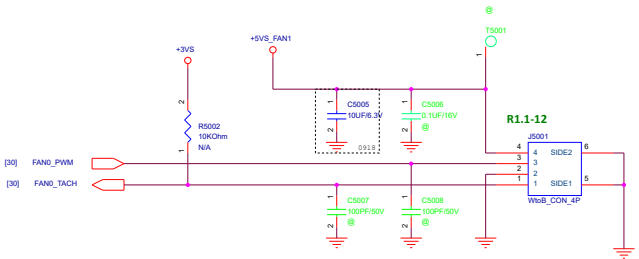
SMBUS address=10010000 (90)

Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

Reserve for powr noise

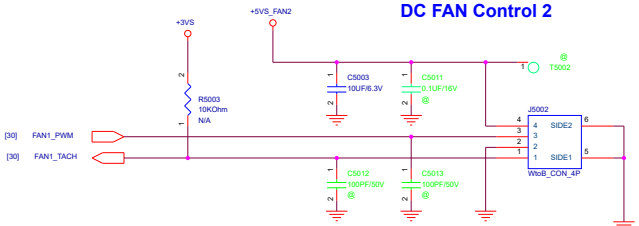


DC FAN Control 1



1st: 12017-00330300
2nd :12G171010049

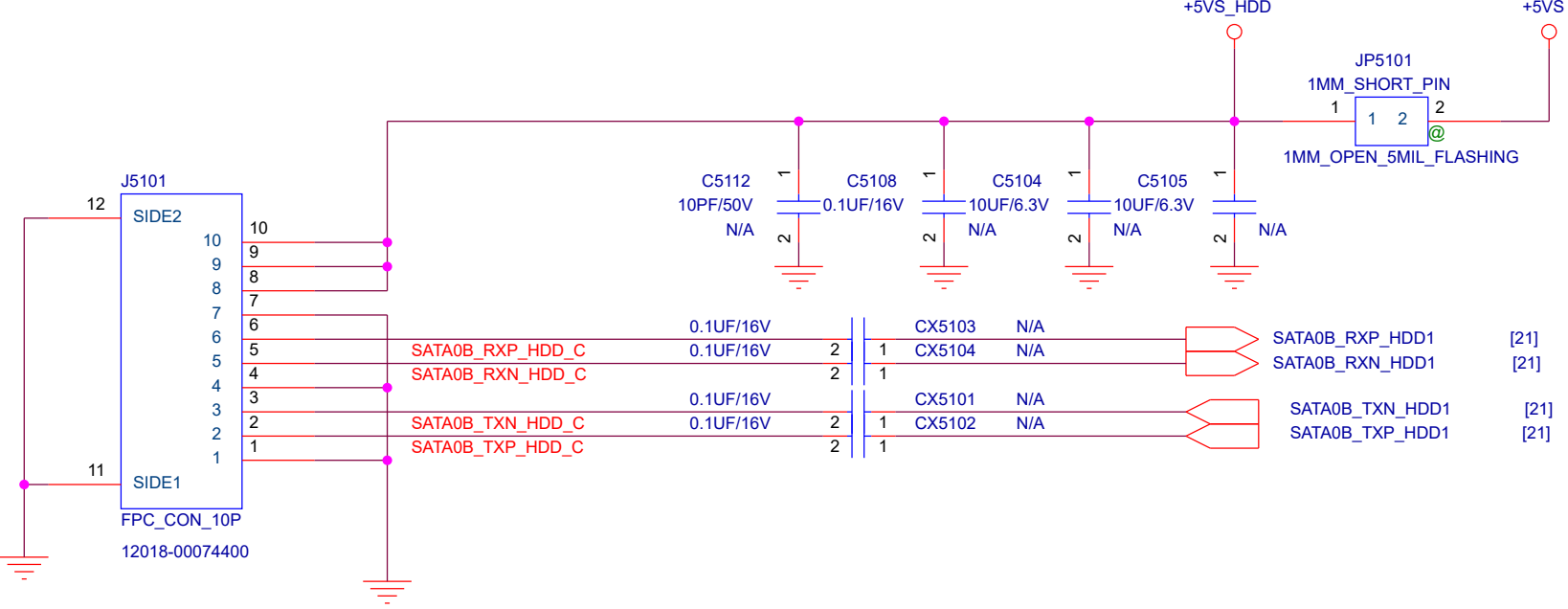
DC FAN Control 2



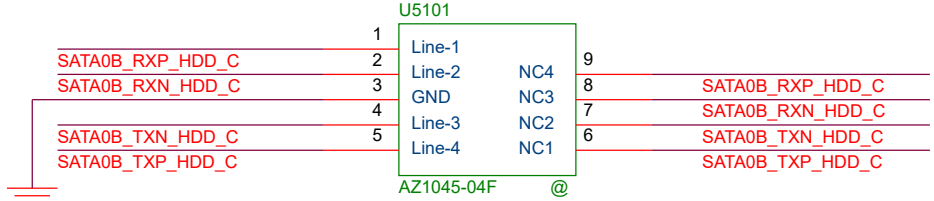
1st: 12017-00330300
2nd :12G171010049

<Variant Name>

ASUSTeK COMPUTER	Title : FAN_Thermal Sensor & Fan	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 50 of 103	



PIN #	Description
1	5V
2	5V
3	5V
4	GND
5	RX+
6	RX-
7	GND
8	TX-
9	TX+
10	GND



teknisi indonesia

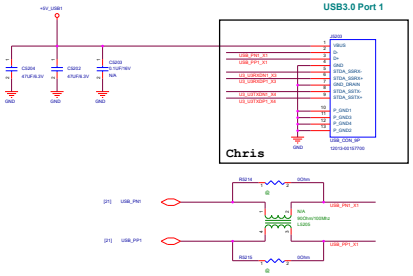
<Variant Name>

ASUSTeK COMPUTER	Title : XDD_HDD & ODD CON	
	Engineer: Gaming RD	
Size: A	Project Name: G711GW	Rev: R1.0
Date: Wednesday, April 17, 2019	Sheet 51 of 103	

Main Board

Chris

USB3.0 Port 1



Chris

USB3.0 ESD-Protection

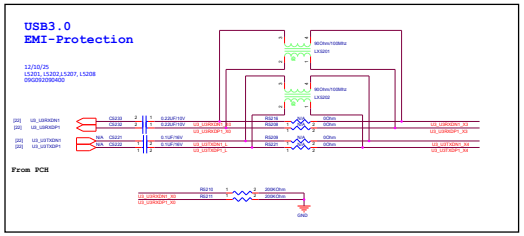
1st : 07G028076030
ESD PROTECTION AZ1045-04F

2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

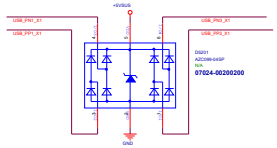
Chris

USB3.0
EMI-Protection

12/10/25
LS201, LS202,LS207, LS208
09G093209400



USB2.0
ESD-Protection



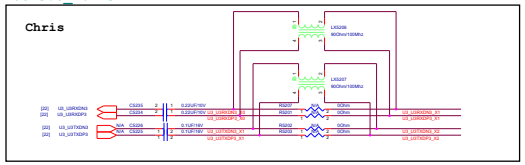
D5301 ESD Diode

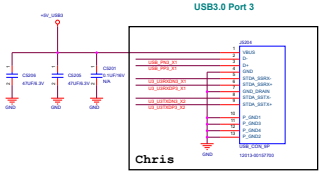
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

Chris

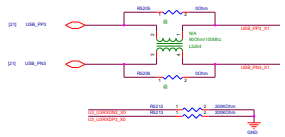
USB3.0_PORT3





USB3.0 Port 3

Chris



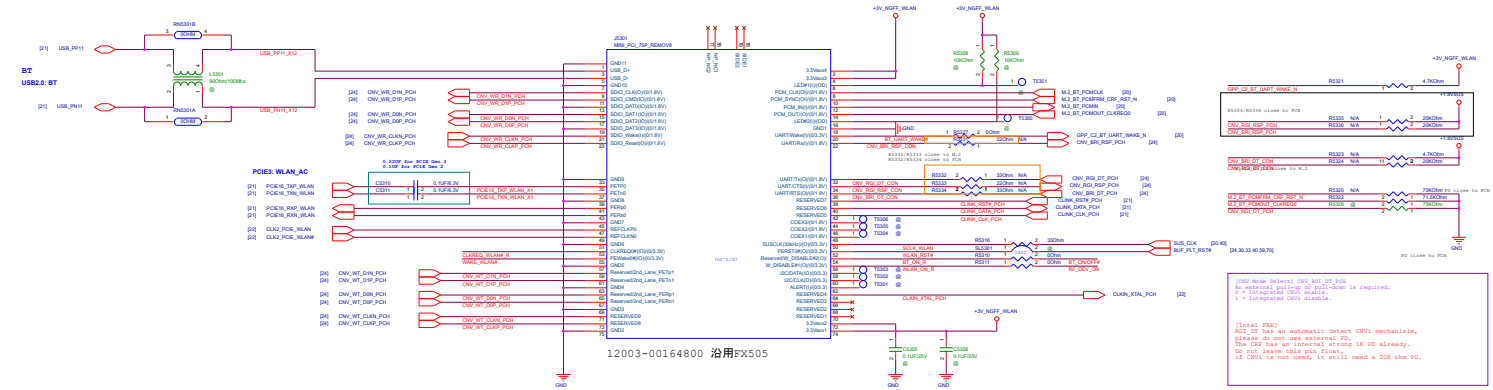
USB3.0 ESD-Protection

1st : 07G028076030
ESD PROTECTION AZ1045-04F

2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

Chris

NGFF M.2 TYPE_E-KEY WIFI



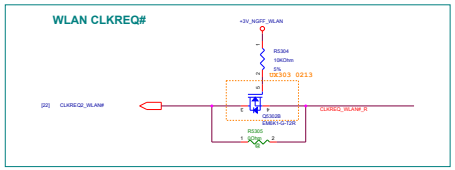
J5301_NGFF E-KEY WLAN Connector H=2.0mm

1st Source: P/N:12003-00076000 ARGOSY/NASE0-S6701-TP20

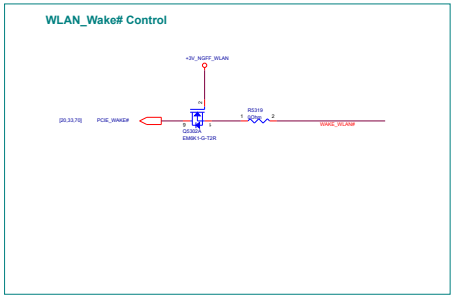
2nd Source: P/N:12003-00075200 DRAGONSTATE/213EBAA2FFB

3rd Source: P/N:12003-00075800 LOTES/APCI0062-P001A

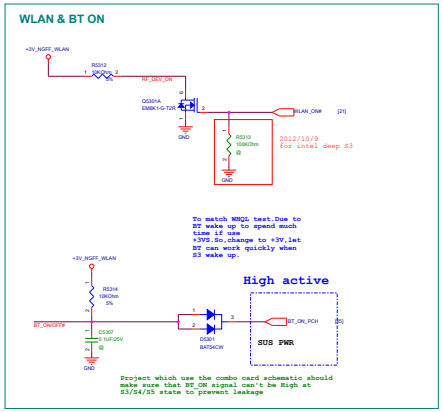
WLAN CLKREQ#



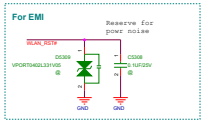
WLAN_Wake# Control



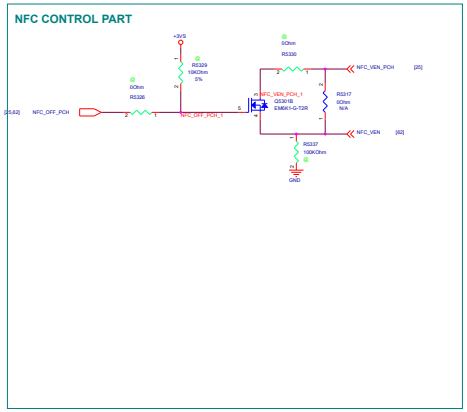
WLAN & BT ON



For EMI



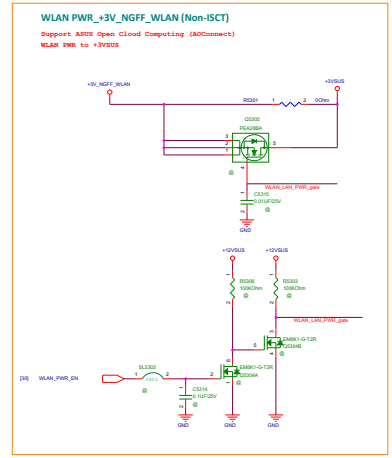
NFC CONTROL PART

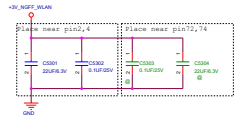


WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)

WLAN PWR to +3VSUS





<Core Design>
ASUSTeK COMPUTER
Title : WiFi/WiMax
Engineer: EE
Size: D
Project Name: GX502GX
Rev: 1.0
Date: Wednesday, April 17, 2019
Sheet 53 of 103

<Variant Name>

Title : IO Con. to MB

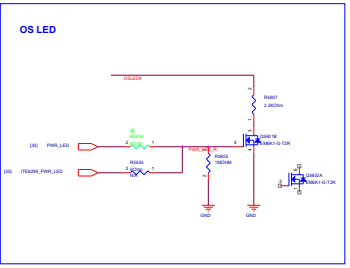
ASUSTeK COMPUTER

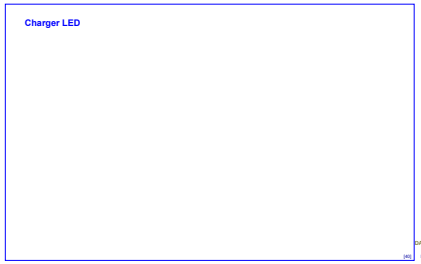
Engineer: Gaming RD

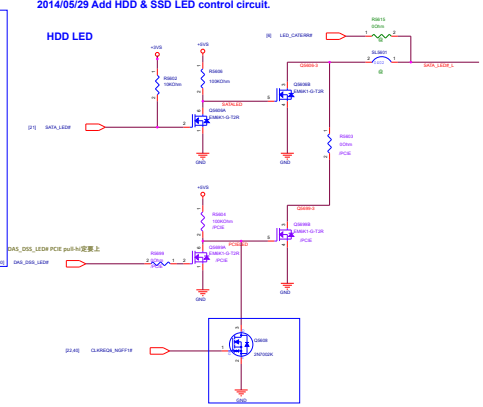
Size	Project Name	Rev
Custom	**G711GW**	1.0

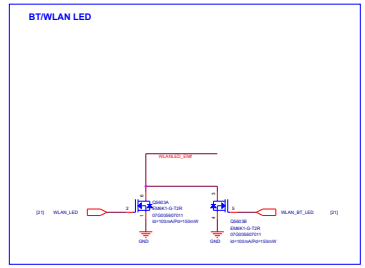
Date:	Wednesday, April 17, 2019	Sheet	55	of	103

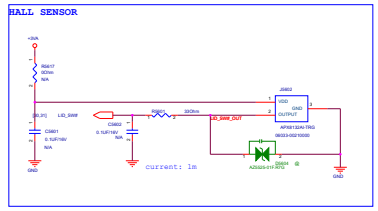
2014/05/29 Add HDD & SSD LED control circuit.

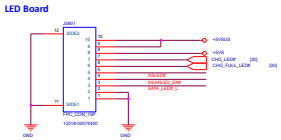


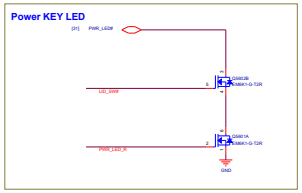


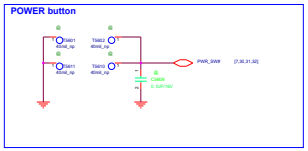


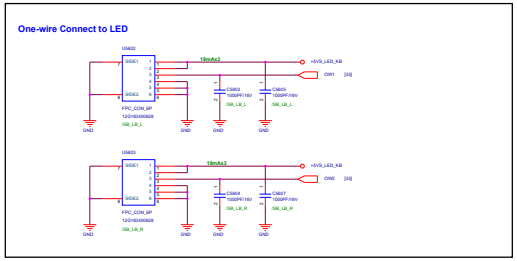












Chris

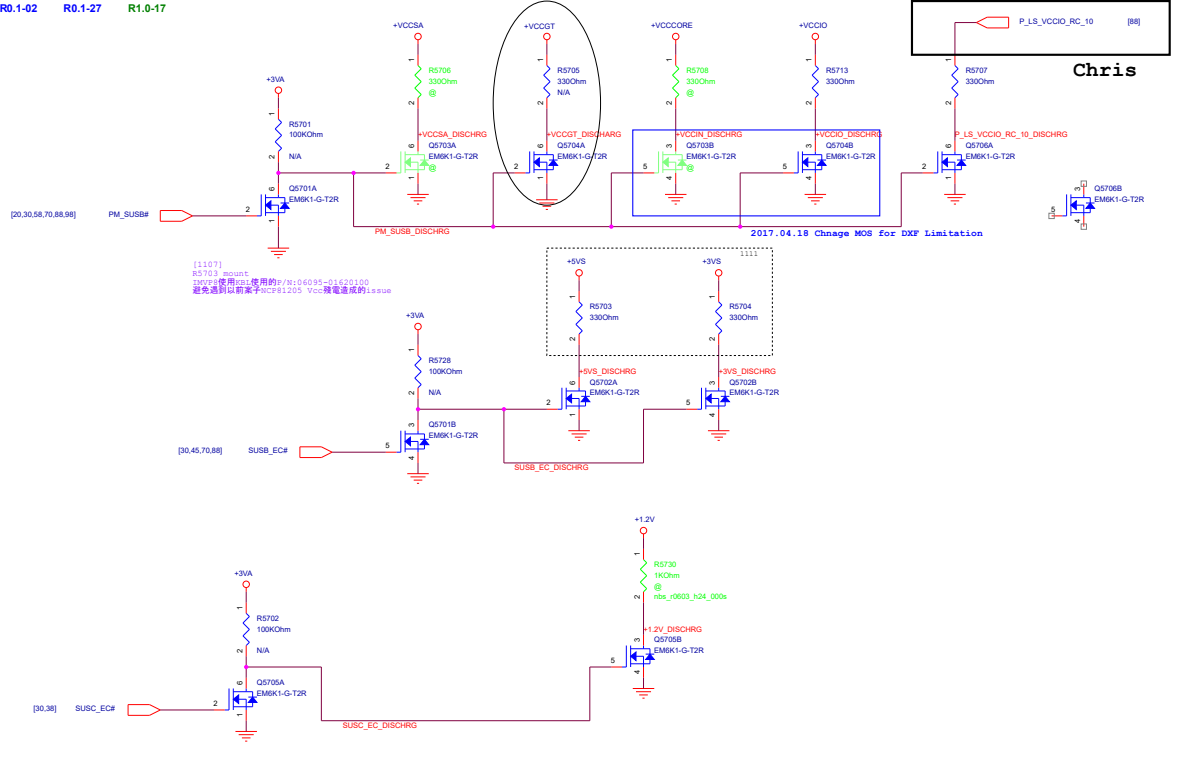
G531GT P.56 差異

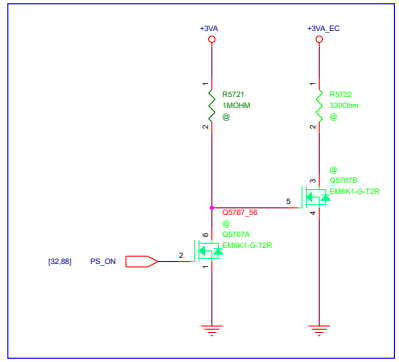
MP 60 PN	PCB	U5602/U5603	C5603/C5604/C5605/C5607
60NR01L0-MB3010	R1.4	12G183400628	11G232110211030
60NR01L0-MB3210	R1.4	12G183400628	11G232110211030
60NR01L0-MB3310	R1.4	12G183400628	11G232110211030
60NR01L0-MB3410	R1.4	12G183400628	11G232110211030
60NR01L0-MB3110	R1.4	NA	NA

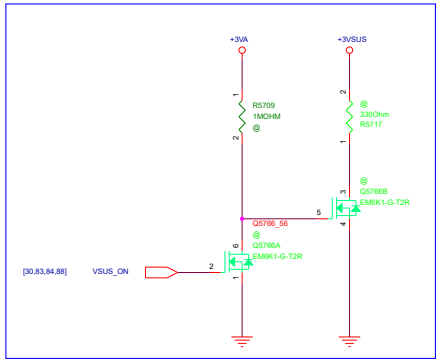
Standard Notice

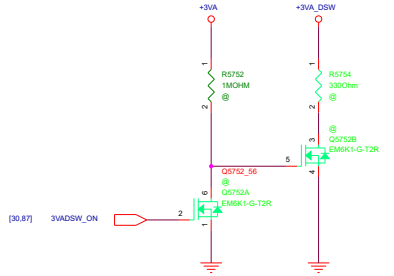
ASUSTeK COMPUTER	Title :	LED & LID
	Engineer:	Gaming RD
Size: D	Project Name: G711GW	Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 56 of 105	

R0.1-02 R0.1-27 R1.0-17



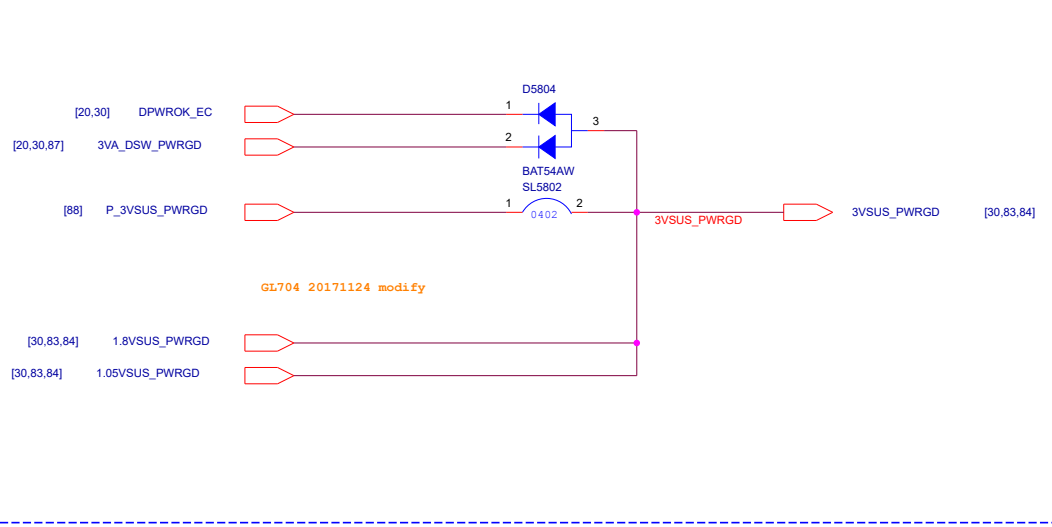


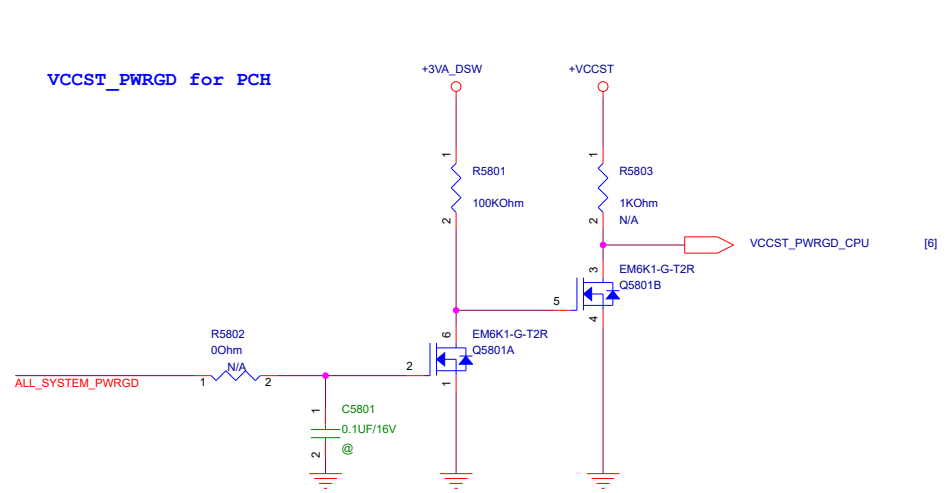


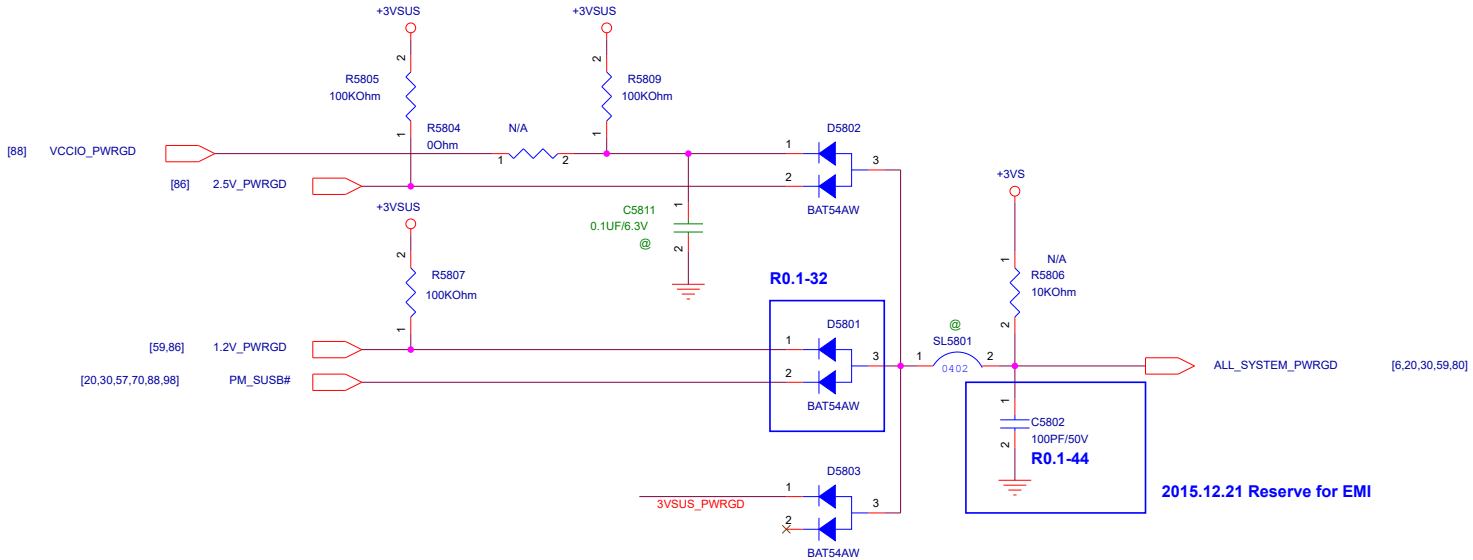


<variant_name>

ASUSTeK COMPUTER	Title :	DSG_Discharge	
	Engineer:	Gaming RD	
Size: C	Project Name: G711GW		Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 57 of 103		



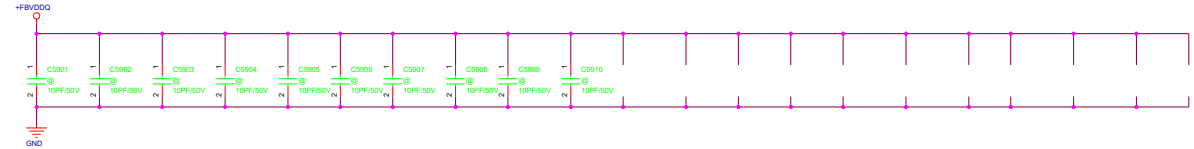


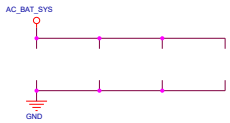


<Variant Name>

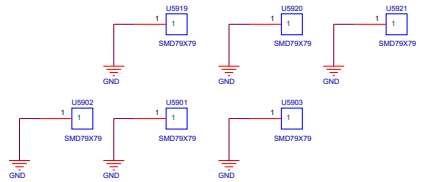
ASUSTeK COMPUTER	Title : Power Protect	
	Engineer: Gaming RD	
Size: Custom	Project Name: G711GW	Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 58 of 103	

EMI

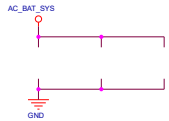




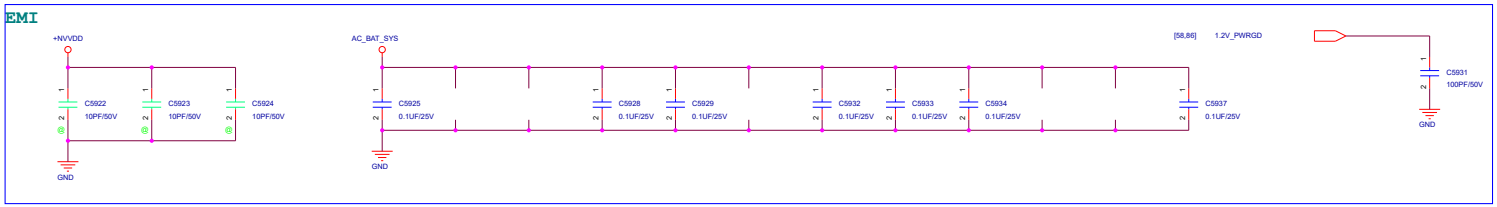
CLIP 13NB0I40T01011

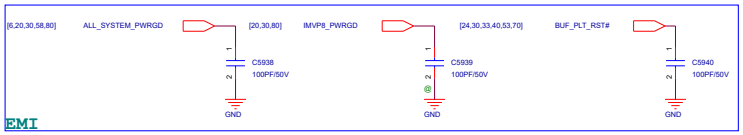


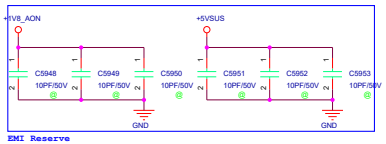
EMI

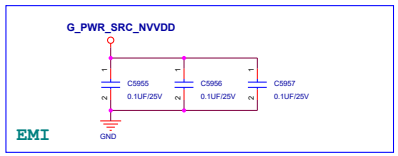


EMI







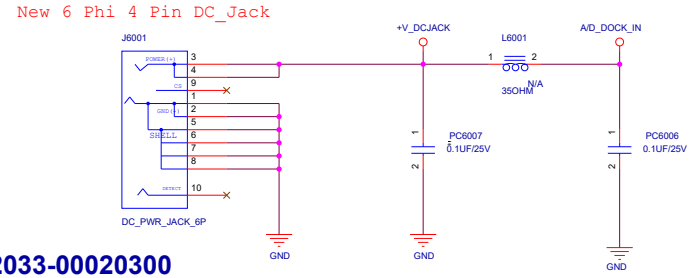


<Variant Name>

ASUSTeK COMPUTER	Title : I/O_Main board Conn.	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 59 of 103	

DC-IN Connector

DC Jack使用請詢用River_Hsu

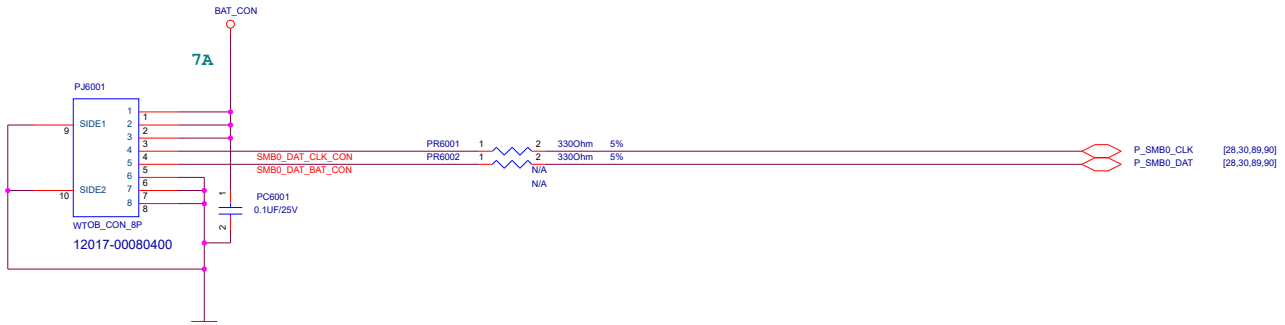


12033-00020300

J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

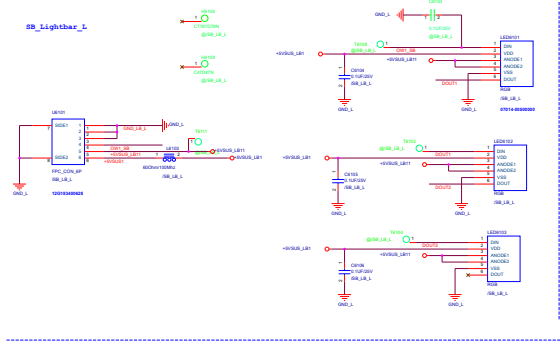
Mode	ADP_INSERT_NG#	AC_IN_OC#
AC Mode	0 (POP,throttling, stop charging)	0
	1	

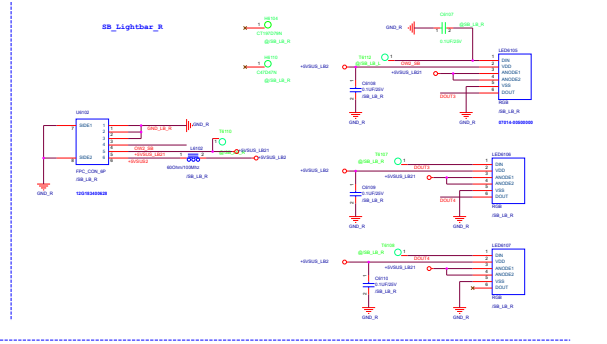
Battery Connector



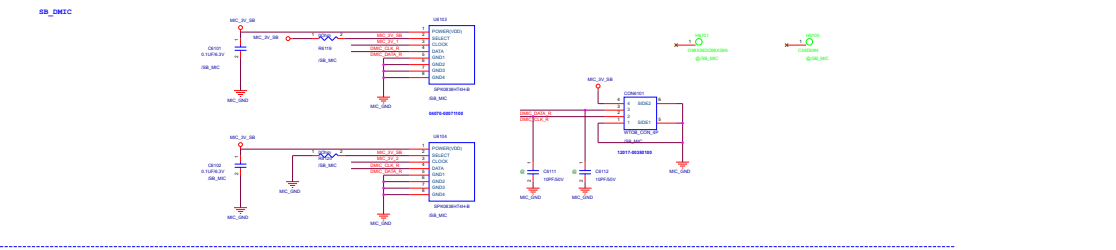
Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

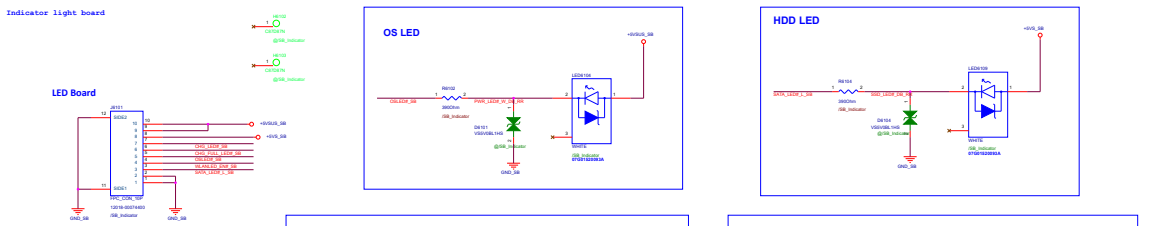
ASUS	Project Name: GX700		Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: Benson	
Date: Wednesday, April 17, 2019	Sheet 60 of 103		

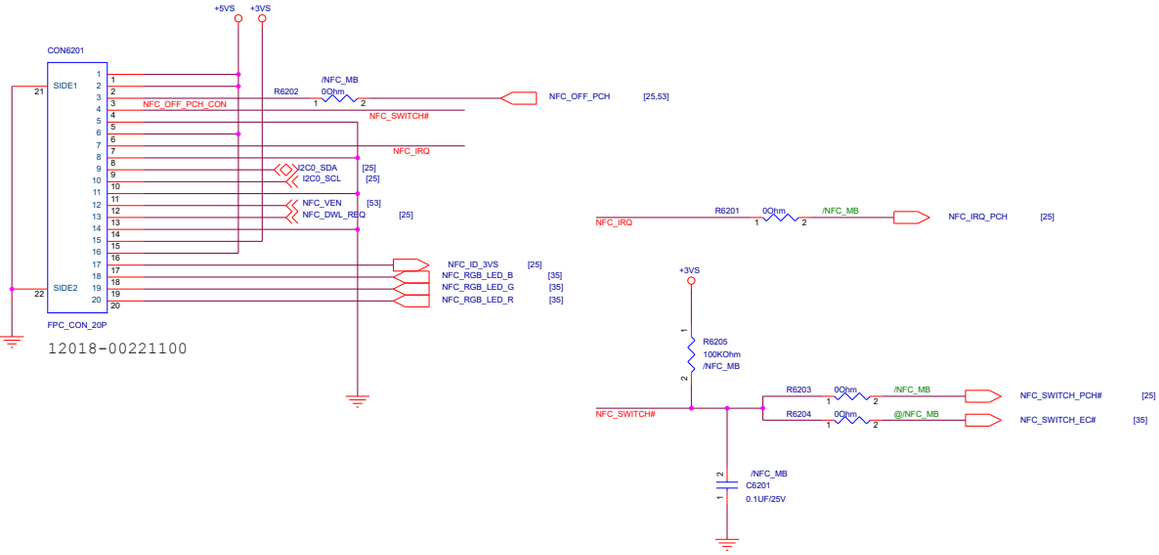

SB_Lightbar_L



SB_Lightbar_R


SB_DMIC


Indicator light board
LED Board
OS LED
HDD LED
Charger LED
BT/WLAN LED
UD(Bright Amber):1.0~2.4V
BY(White):2.9~3.3V
IF=5mA



<variant_name><Variant Name></variant_name>

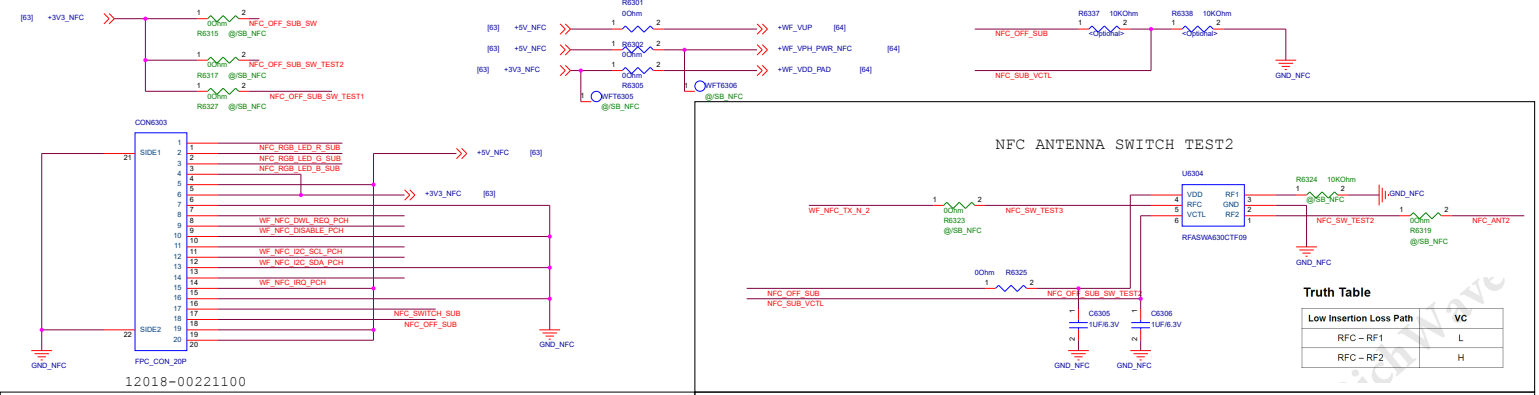
ASUSTeK COMPUTER

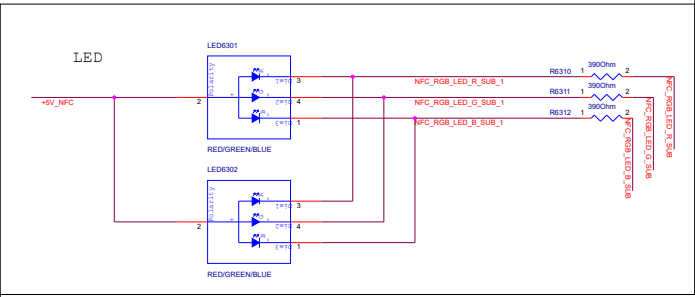
Title : USB3_*****

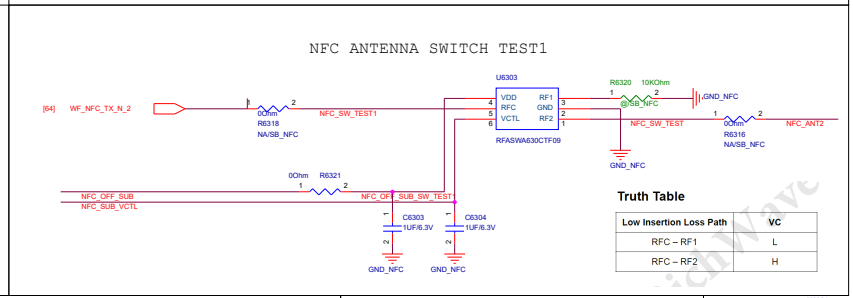
Engineer: Gaming RD

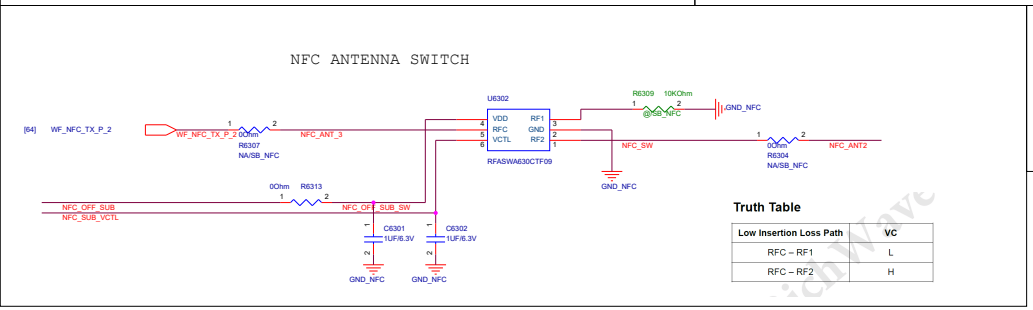
Size	Project Name	Rev
Custom	G731GX	1.0

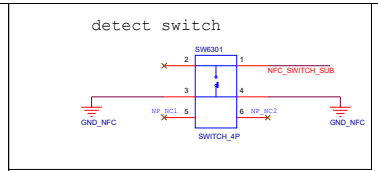
Date: Wednesday, April 17, 2019 Sheet 62 of 103

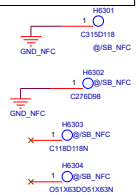




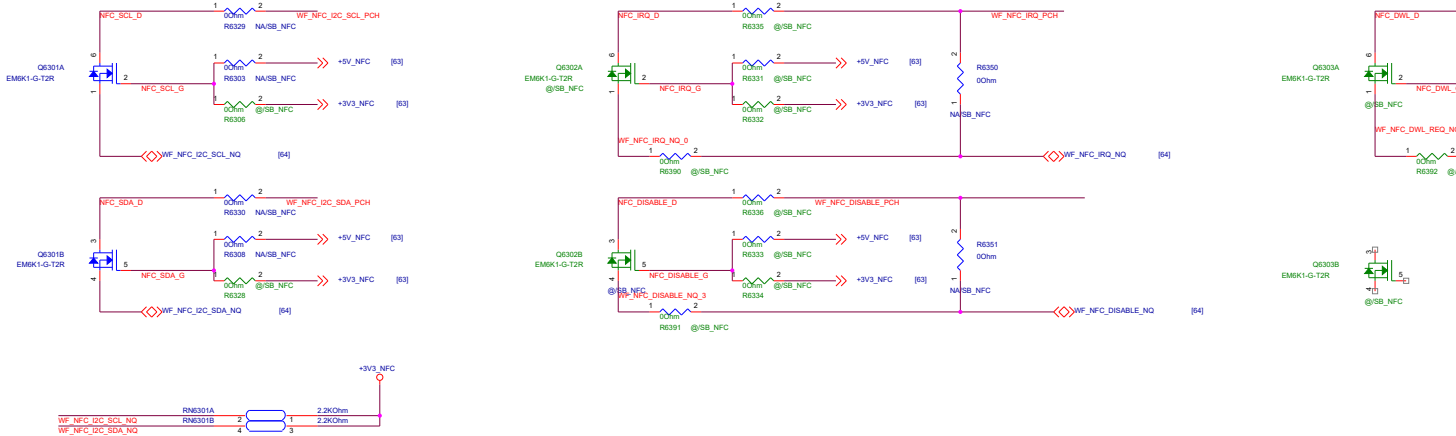






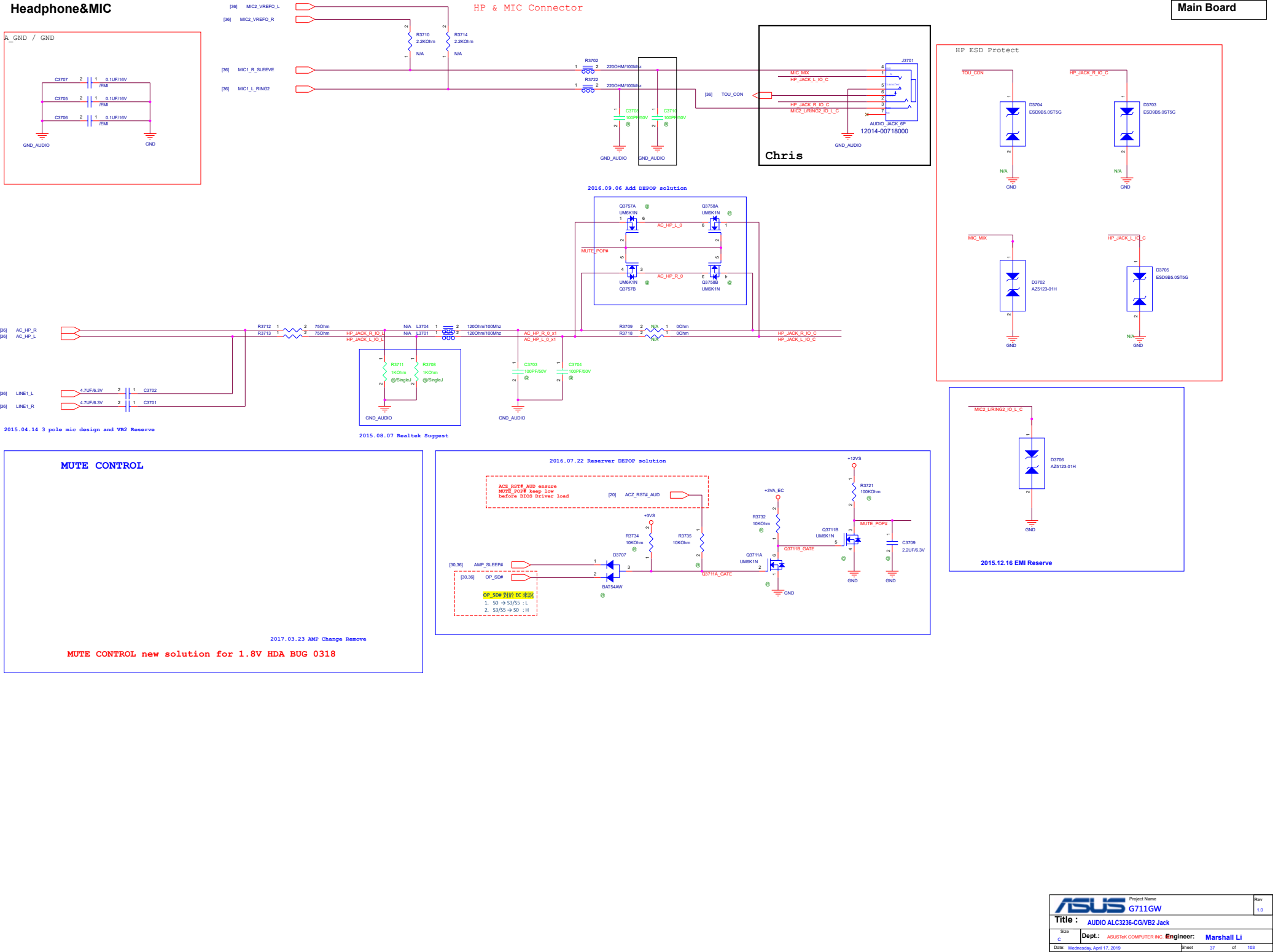


teknisi indonesia



Headphone&MIC

Main Board



Project Name: G711GW			Rev: 1.0
Title : AUDIO ALC3236-CG/VB2 Jack			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Marshall Li	
Date: Wednesday, April 17, 2019	Sheet 37 of 103		

<Variant Name>

Title :

ASUSTeK COMPUTER

Engineer: Gaming RD

Size	Project Name	Rev
D	**G711GW**	1.0

Date:	Wednesday, April 17, 2019	Sheet	66	of	103

<Variant Name>

Title : I/O board FUNC key

ASUSTeK COMPUTER

Engineer: Gaming RD

Size	Project Name	Rev
E	G711GW	1.0

<Variant Name>

	Project Name G711GW	Rev R1.0

Title : Thunderbolt

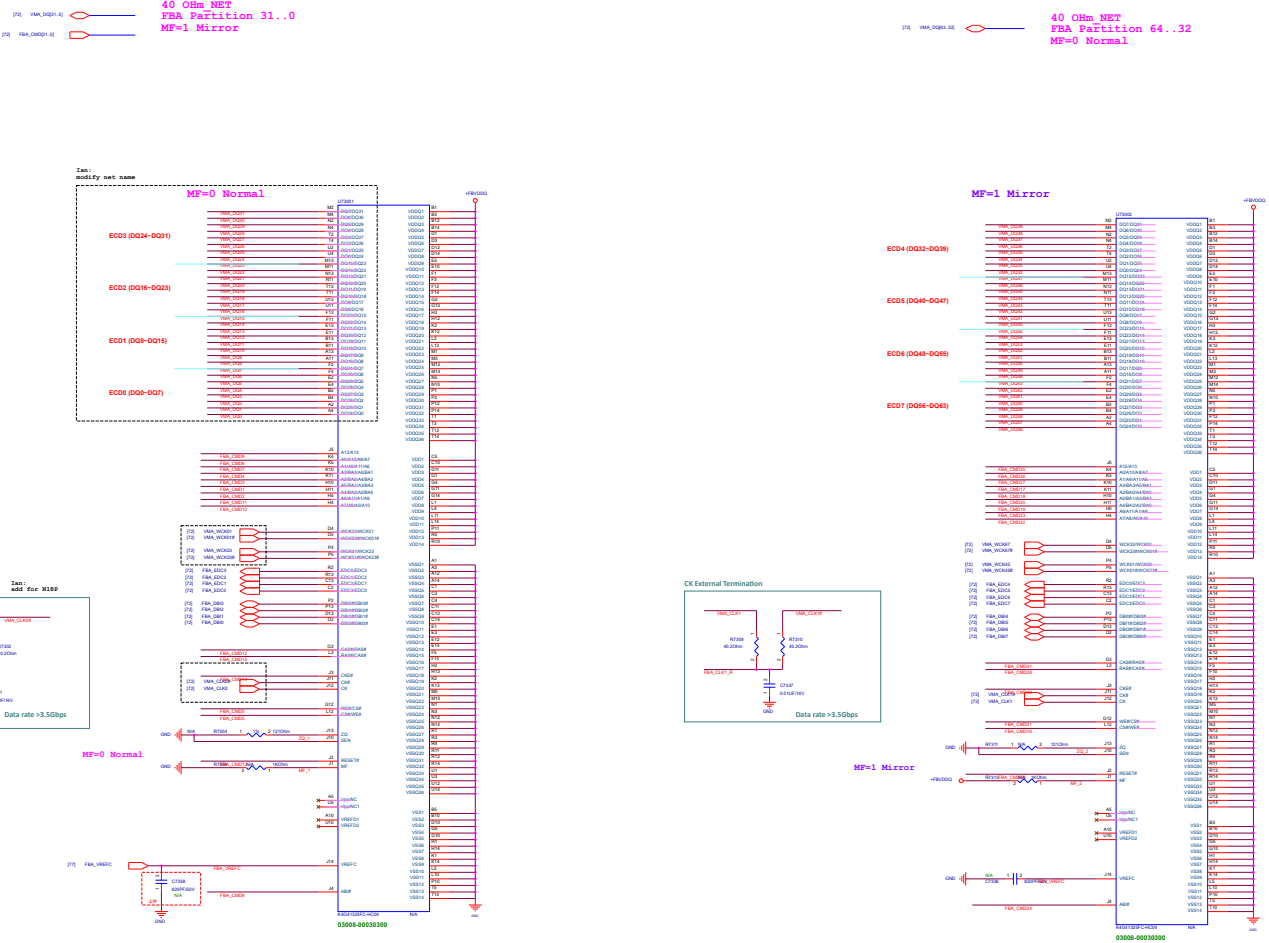
Size Custom	**Dept.:** ASUSTeK COMPUTER	**Engineer:** Gaming RD
Date: Wednesday, April 17, 2019	Sheet 68 of 103	

<Variant Name>

ASUSTeK COMPUTER	Title : OTH_EMI	
	Engineer: Gaming RD	
Size: C	Project Name: G711GW	Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 69 of 103	

TYPE-C USB3.1

	Project Name: G711GW		Rev: 0.0
Title : TYPE-C USB3.1_R1.5_4			
Size: A	Dept.: ASUSTeK COMPUTER INC	Engineer: Ashton_yang	
Date: Wednesday, April 17, 2019		Sheet 47 of 103	



Priority	Company	Model Name	ASUS P/N	Process
1	Micron	MT51J256M32HF-80:B	03008-00051600	17nm
2	Hynix	H5AN(H)8G(C)BHAAR-R2C	03008-00052000	18nm(AL)

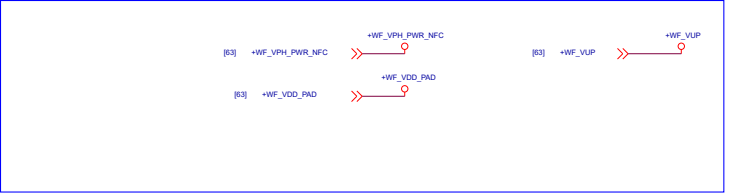
Table 4. N18P-G0 GDDR5 Recommended Memories

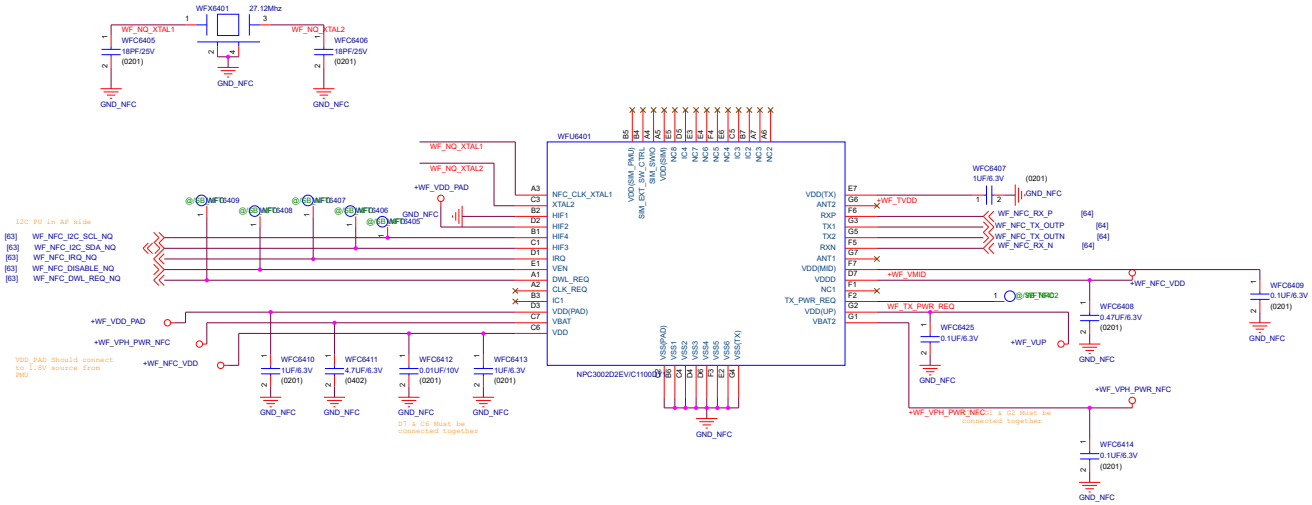
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35 V and 1.5V[2]	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Samsung	K4G80325FC-HC25	C-die	0x0	8 Gbps	N/A	Full	Production candidate

<Variant Name>

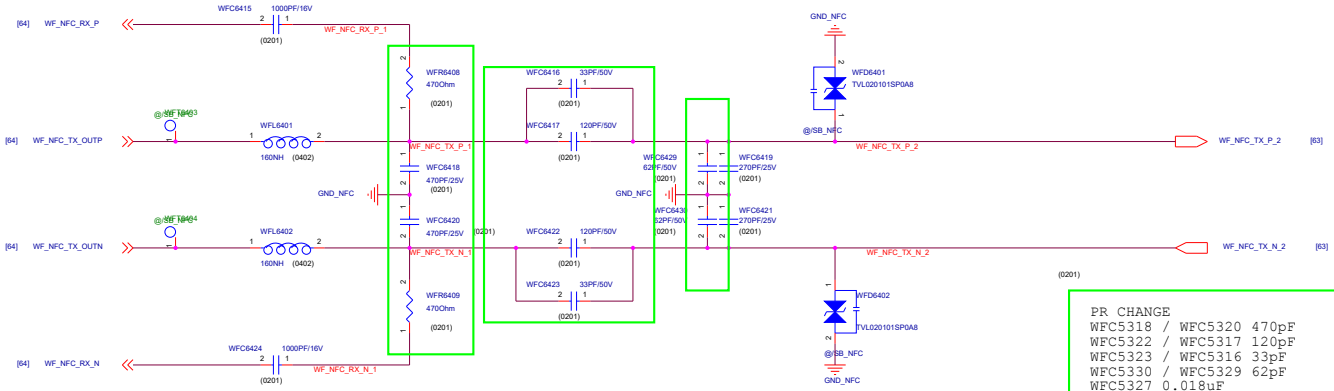
Title <Title>		
Size A1	Document Number G731GX	Rev R1.0
Date: Wednesday, April 17, 2019	Sheet 75 of 103	

Title <Title>		
Size A1	Document Number G731GX	Rev R1.0
Date: Wednesday, April 17, 2019	Sheet 76 of 103	





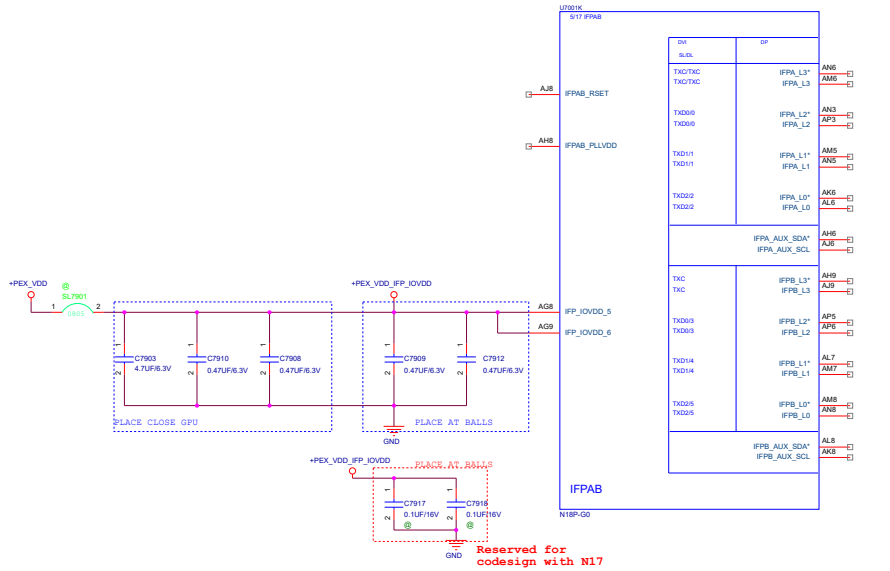
NFC Matching



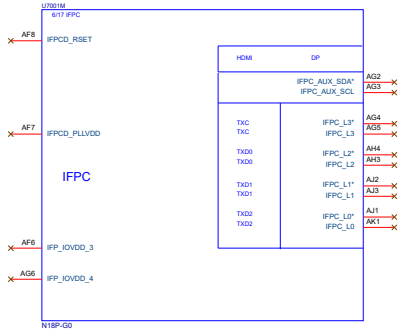
PR CHANGE
WFC5318 / WFC5320 470pF
WFC5322 / WFC5317 120pF
WFC5323 / WFC5316 33pF
WFC5330 / WFC5329 62pF
WFC5327 0.018uF
WFR5308 /WFR5309 470 Ohm

<Variant Name>

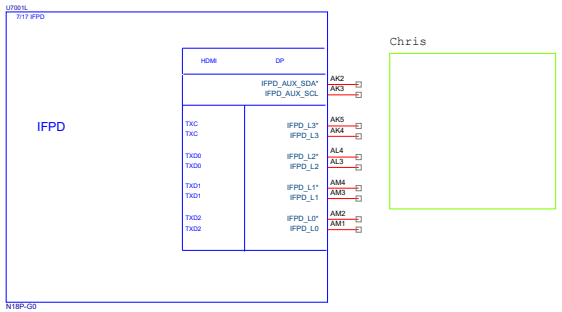
ASUSTeK COMPUTER	Title :	USB3_*****	
	Engineer:	Gaming RD	
Size: C	Project Name: G731GX		Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet 64 of 103		



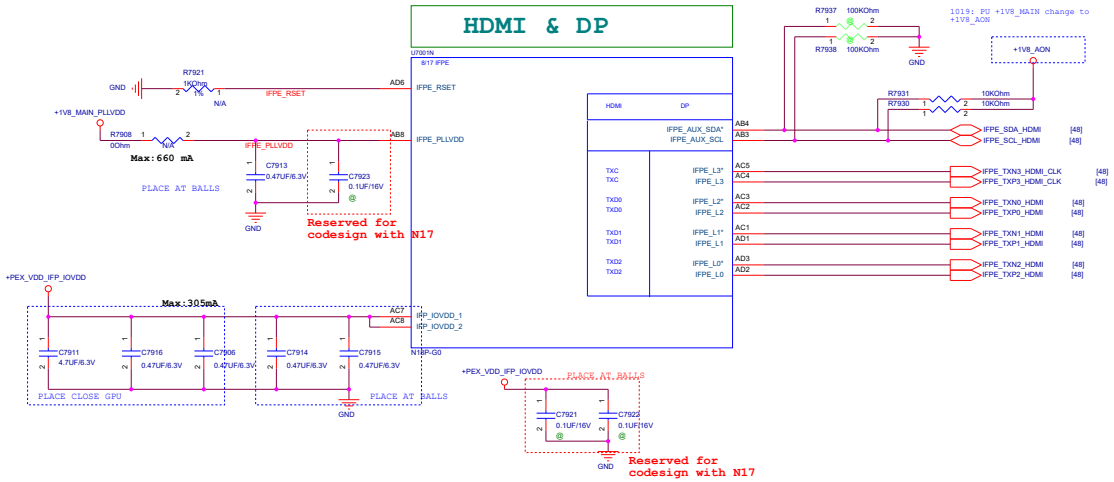
DP(Type-C)



EDP(4Lane Panel)



HDMI & DP

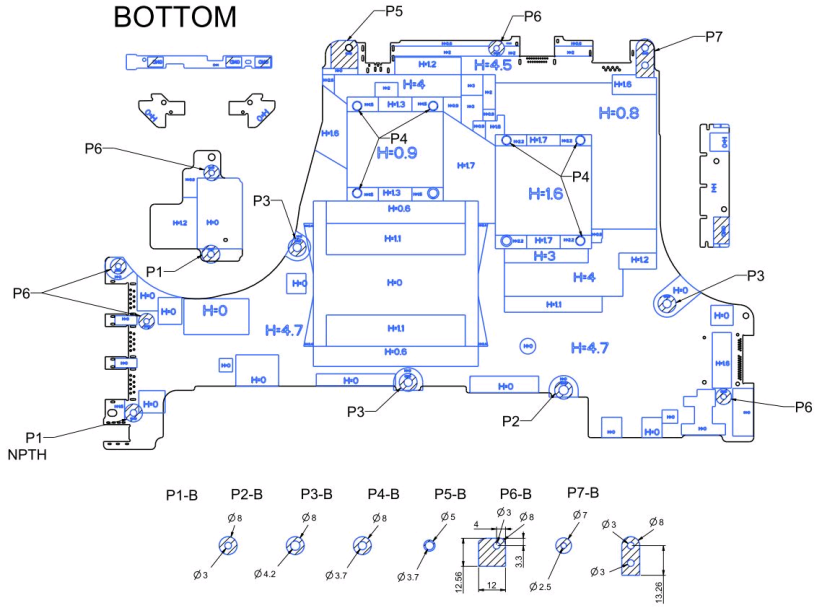


GPU	Type		Footprint	Population N18	Population N17	Location
IFP_IOVDD Supply Rails						
GB4C-128, GB4D-128	0.1 µF	X7R	0402	0	6	Under GPU; 1 per ball
	0.47 µF[1]	X6S	0201W	6	0	Under GPU; 1 per ball
	1.0 µF[2]	X6S	0402 or 0201W	0	3	Near GPU
	0.47 µF[2]	X6S	0201W	6	0	Near GPU
	4.7 µF	X6S	0603	3	3	Near GPU
	Bead Type					
	180 Ω @ 100 MHz (ESR=0.2 Ω)		0603	0	0	Near GPU

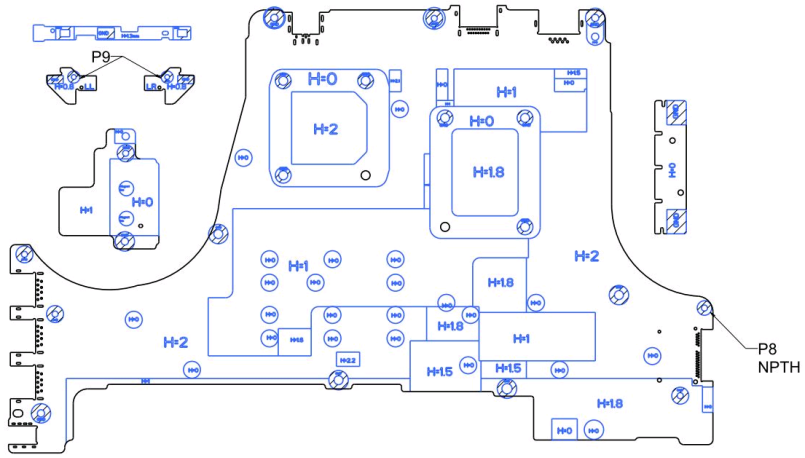
GPU	Type		Footprint	Population N18	Population N17	Location
IFPAB_PLLVDD Supply Rail						
GB4C-128 GB4D-128	0.1 µF	X7R	0402	0	1	Under GPU
	0.47 µF[1]	X6S	0201W	1	0	Under GPU
	Bead Type					
	300 Ω @ 100 MHz (ESR=0.25 Ω)		0603	0	0	Near GPU
N17: IFPCD_PLLVDD and IFPEF_PLLVDD Supply Rails N18: IFPCD_PLLVDD and IFPE_PLLVDD Supply Rails						
GB4C-128 GB4D-128	0.1 µF	X7R	0402	0	2	Under GPU; 1 per ball
	0.47 µF[1]	X6S	0201W	2	0	Under GPU; 1 per ball
	Bead Type					
	300 Ω @ 100 MHz (ESR=0.25 Ω)		0603	0	0	Near GPU

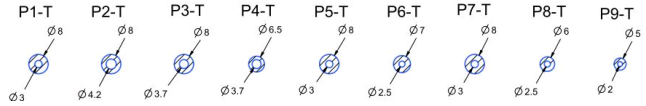
ASUS	Project Name: G731GX	Rev: 2.0
Title : GPU_DP/EDP/HDMI		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD
Date: Wednesday, April 17, 2019	Sheet 79 of 103	

BOTTOM

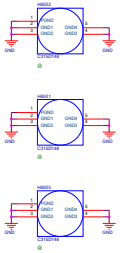


TOP

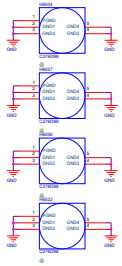




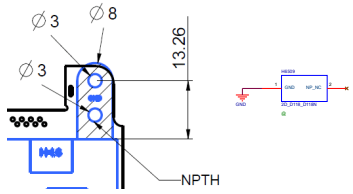
P3: PTH 8 /3.7mm



P6: PTH 7 /2.5mm

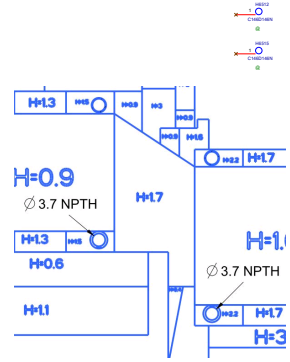


P7: PTH 8 /3mm+ NPTH 3mm

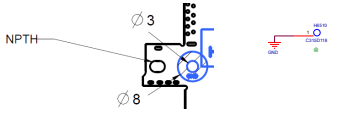


P4: PTH 6.5 /5 /3.7 mm

NPTH 3.7 mm

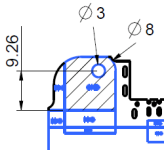


P1: PTH 8 /3 mm

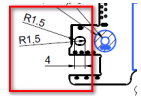


P2: PTH 8 /4.2 mm

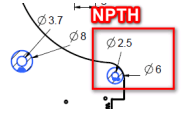
P5: PTH 8/3mm (Ext.)



NPTH 1.5/ 4mm

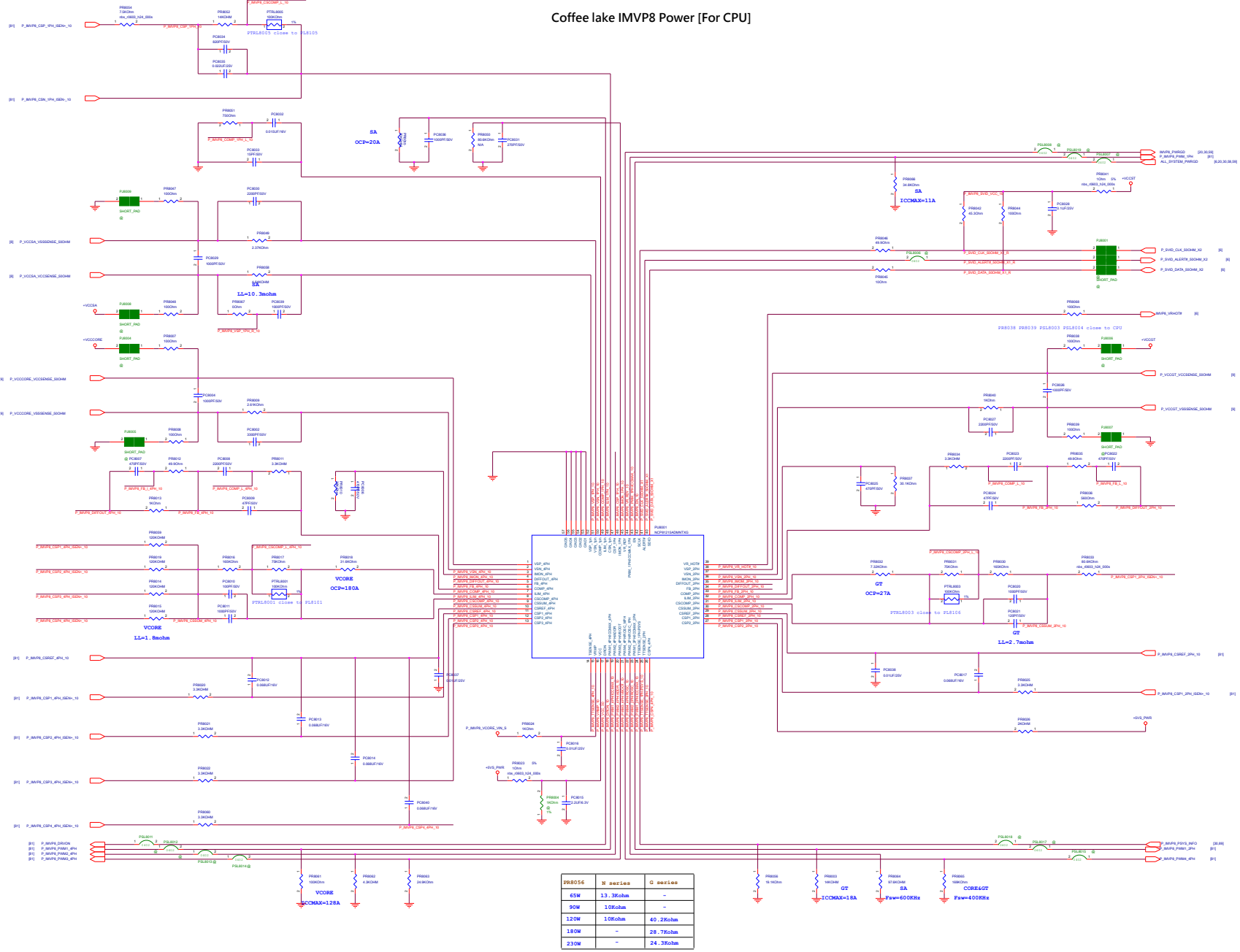


NPTH 6/ 2.5 mm



ASUSTeK COMPUTER	Title :	MC_Screw Hole & Nut	
	Engineer:	Gaming RD	
SIZE: D	Project Name:	G711GW	Rev: 1.0
Date: Wednesday, April 17, 2019	Sheet: 65 of 103		

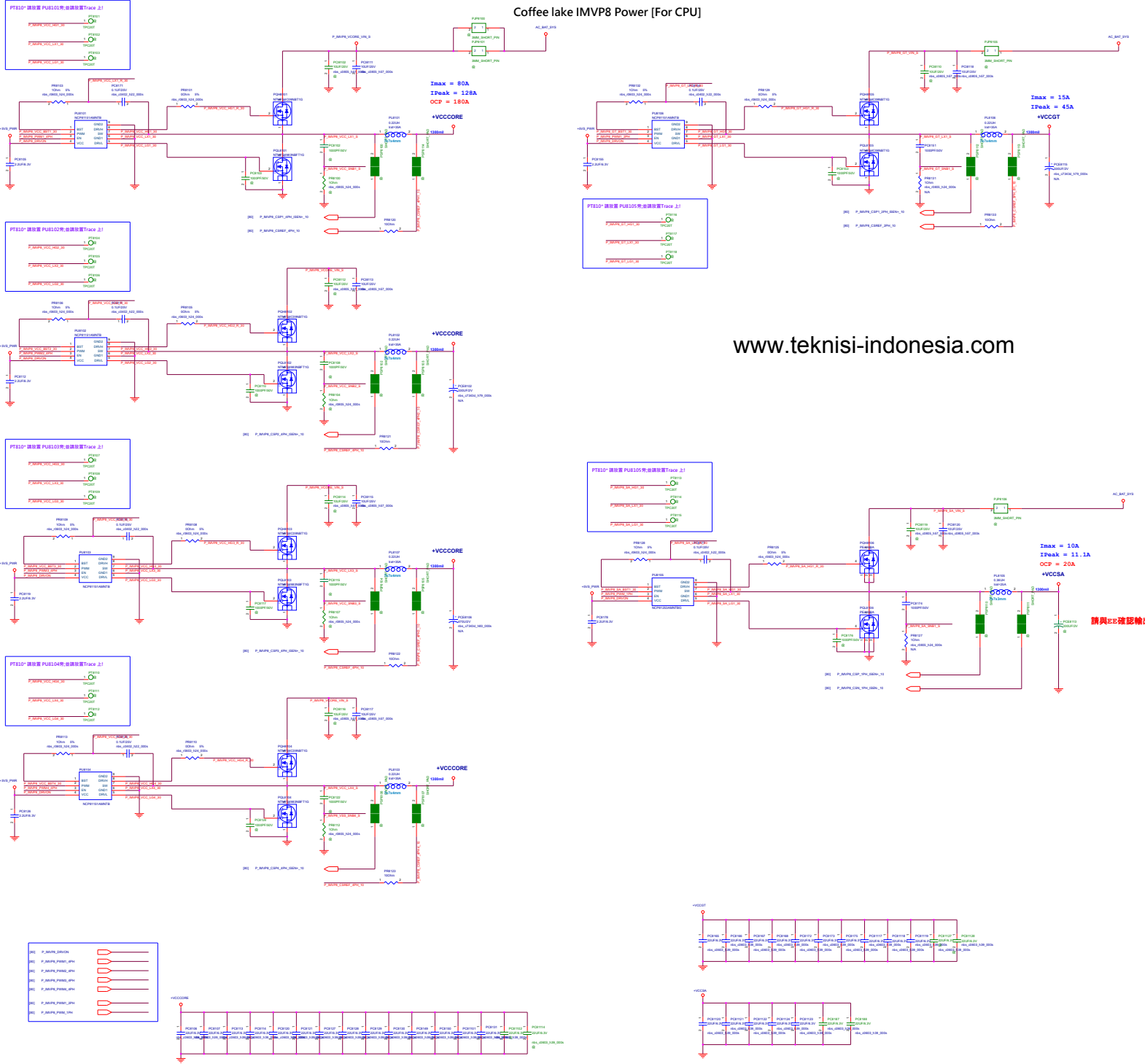
Coffee lake IMVP8 Power [For CPU]



PR8056	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm

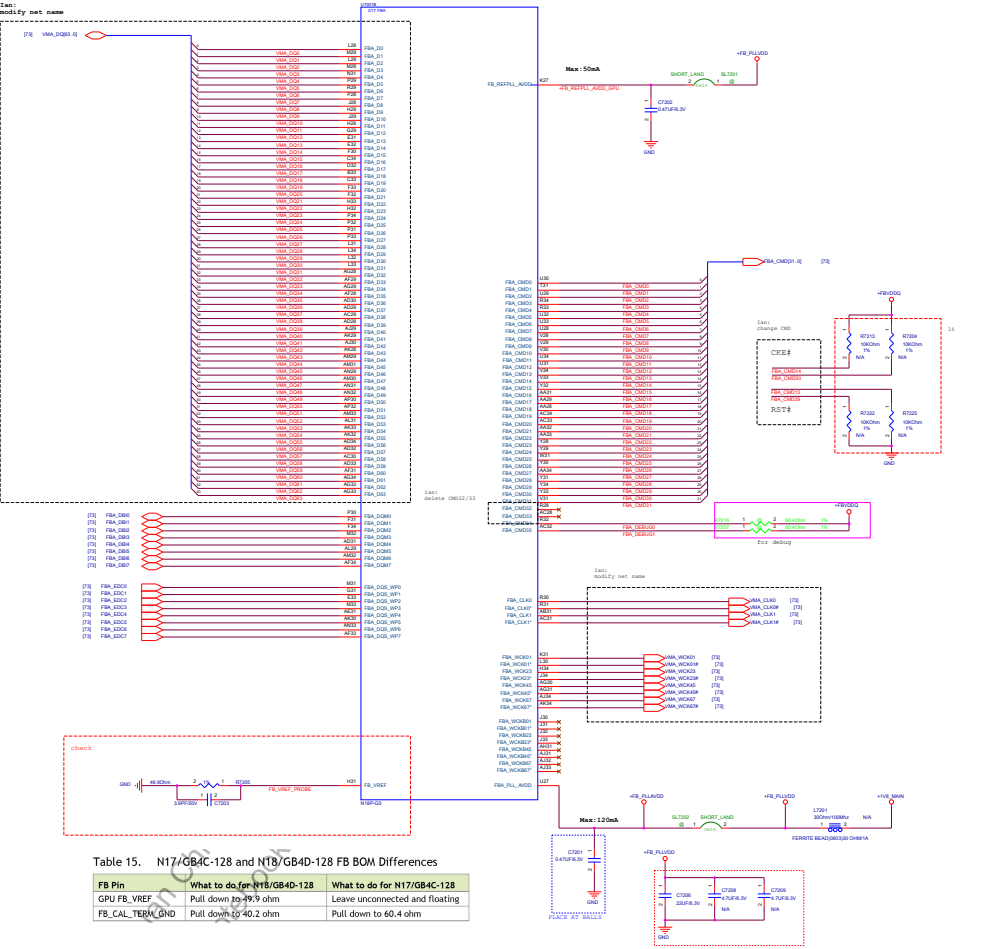
ASUS	Project Name: GL704GM	Rev: 81.0
Title : PW_Coffeelake (1)		
Size: D	Dept.: NB Power team	Engineer: Hon
Date: Wednesday, April 17, 2019	Sheet 80 of 103	

Coffee lake IMVP8 Power [For CPU]



Project Name	G711GW
Title :	PW_COFFELAKE (2)
Dept.:	NB Power team
Engineer:	Neil
Date:	Wednesday, April 17, 2019

MEMORY: GPU FB Partition A



MEMORY: GPU FB Partition B

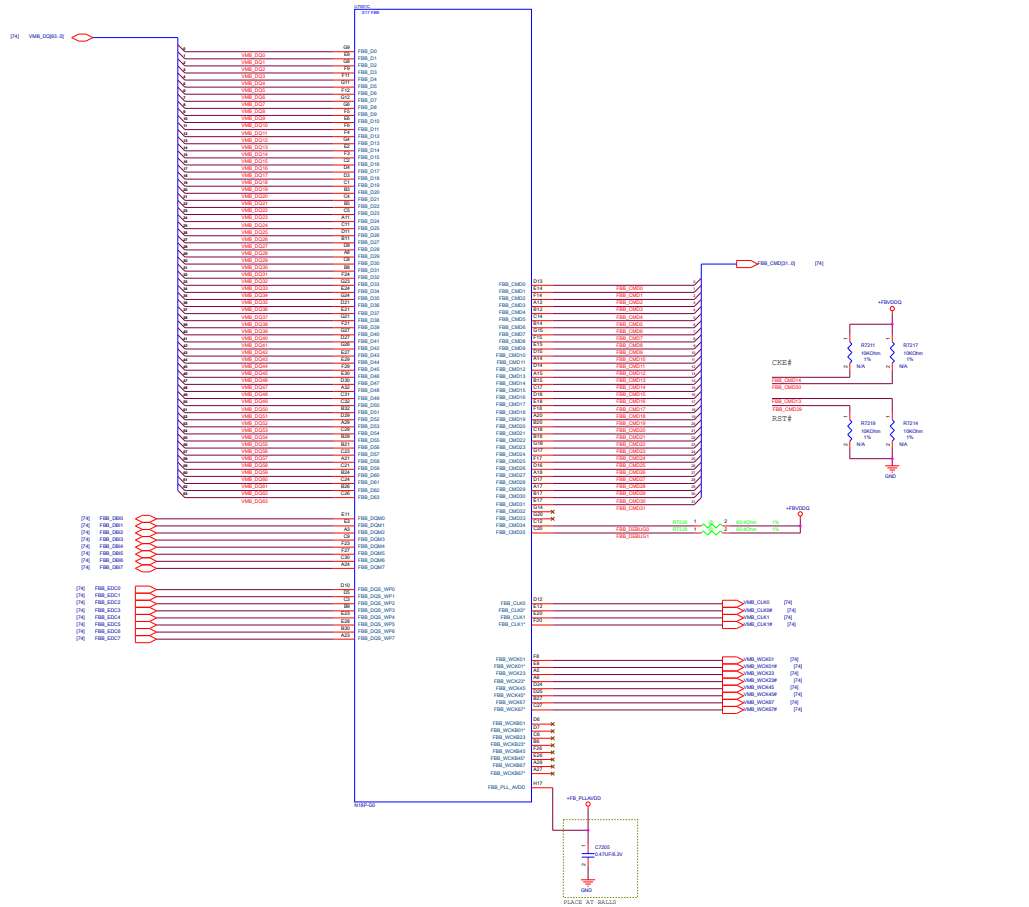
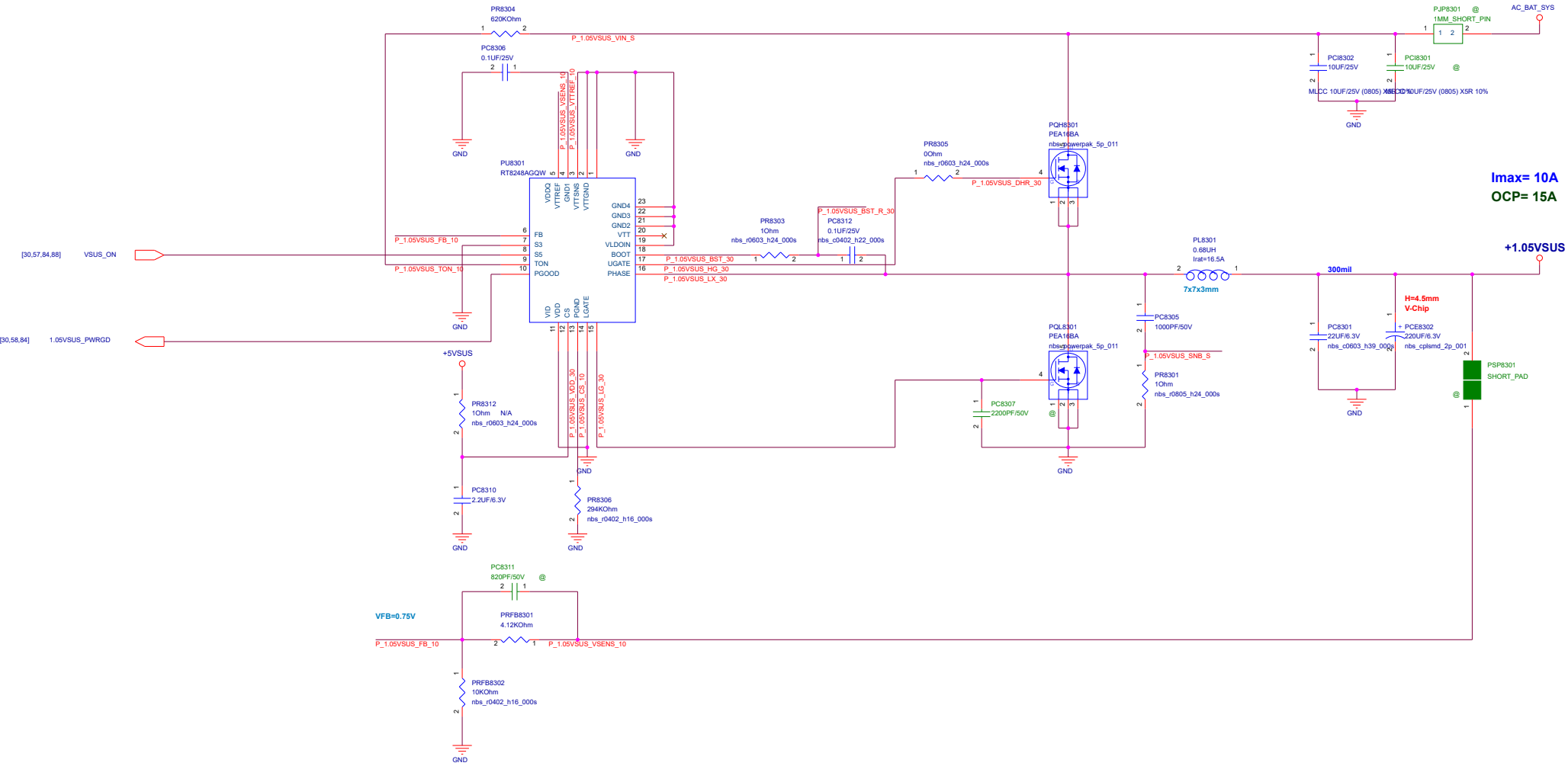


Table 15. N17/GB4C-128 and N18/GB4D-128 FB BOM Differences

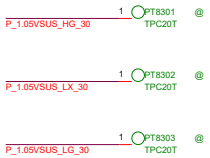
FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm

ASUS	Project Name: G731GX		Rev: 31.0
Title : GPU_FRAME BUFFER			
Size: D	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019		Sheet 72 of 103	

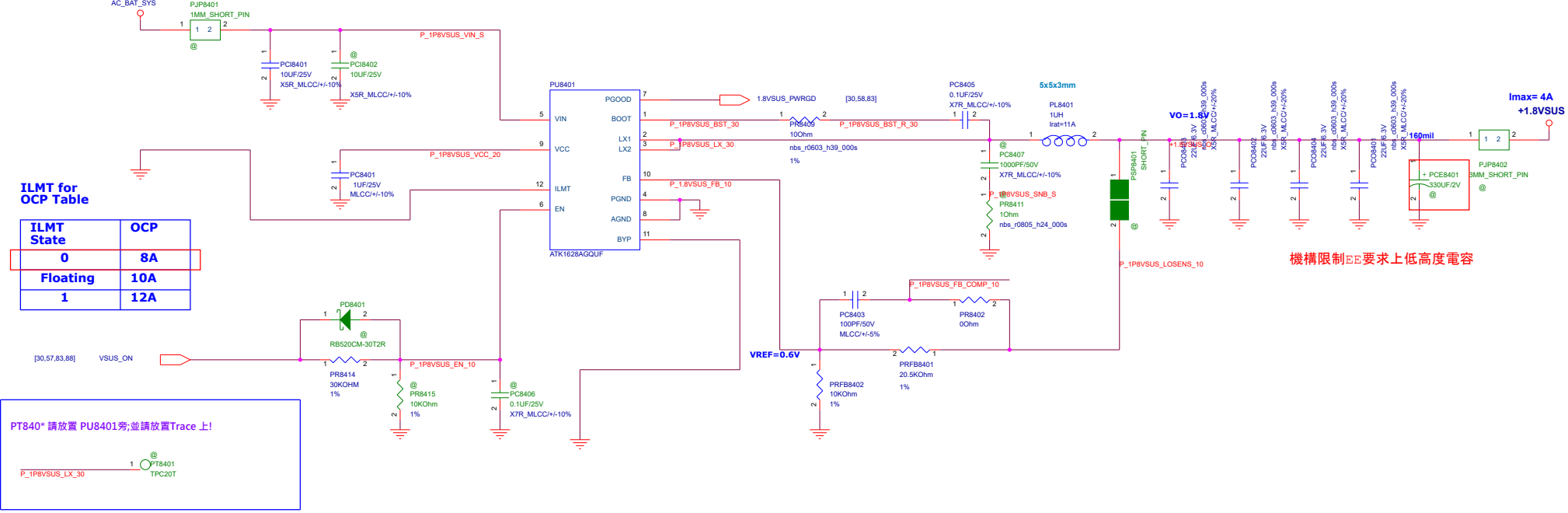
+1.05VSUS [For PCH]



PT830* 請放置 PU8301旁;並請放置Trace 上!



ASUS	Project Name: G711GW		Rev: R1.0
Title : PW_+1.0VSUS			
Size: A3	Dept.: NB Power team	Engineer: Neil	
Date: Wednesday, April 17, 2019	Sheet 83 of 103		



<Variant Name>

Project Name: FX505DY		Rev: R1.0
Title : PW_+1.8VSUS		
Size: A3	Dept.: NB Power team	Engineer: CS Lin
Date: Wednesday, April 17, 2019	Sheet 84 of 103	

<Variant Name>

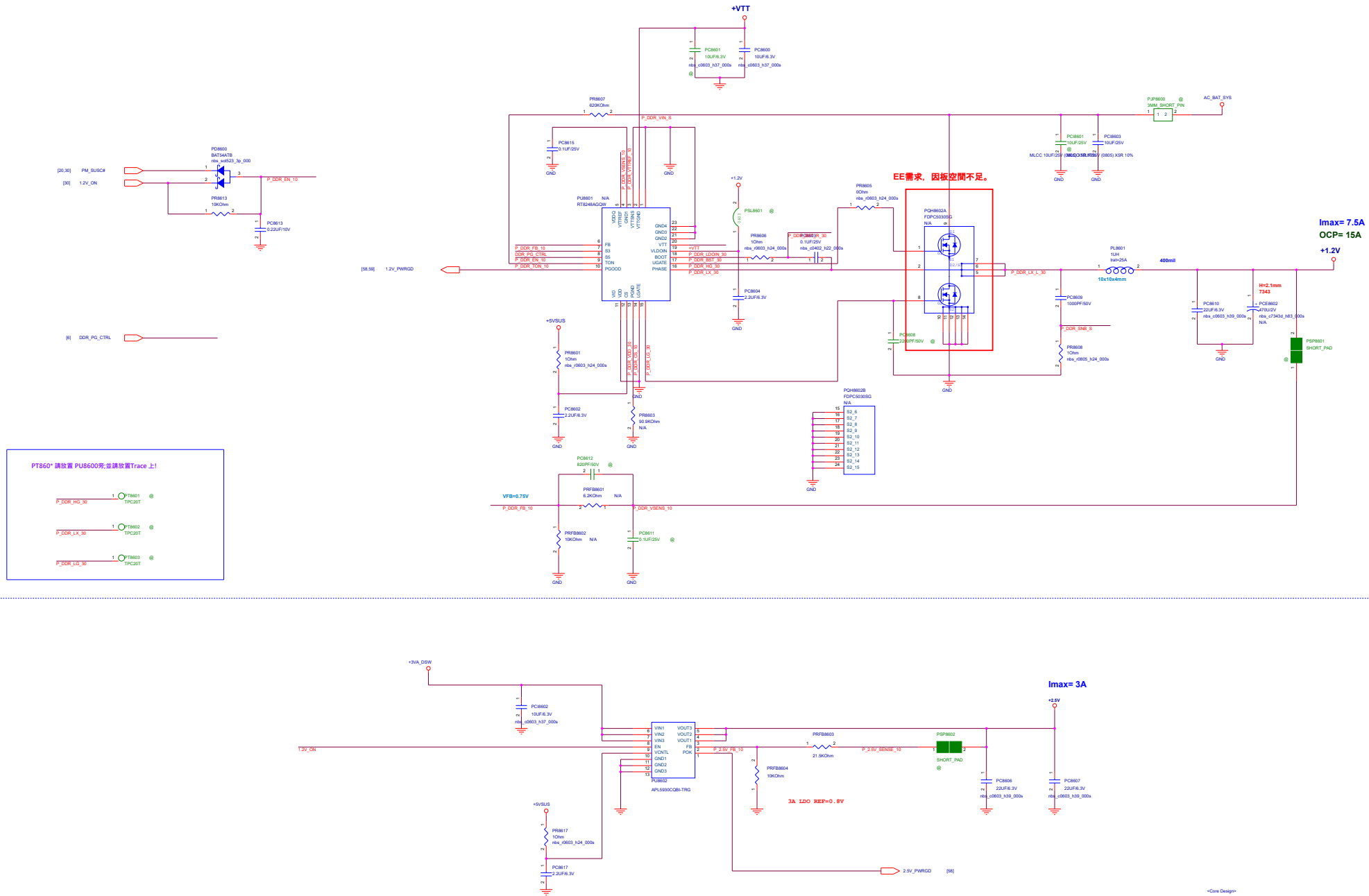
	Project Name GM531GX	Rev R1.0

Title : Thunderbolt

Size		
Custom	**Dept.:** ASUS Power Team	**Engineer:** Joe

Date: Wednesday, April 17, 2019	Sheet 85 of 103	

+1.2V / +VTT / +2.5V[For Memory]



<Core Design>

ASUS	Project Name: G711GW	Rev: R1.0
Title : PW_+1.2V/+VTT/+2.5V		
Size: A2	Dept.: NB Power team	Engineer: Neil
Date: Wednesday, April 17, 2019	Sheet 86 of 103	

40 OHm_NET
FBB Partition 31..0
MF=1 Mirror

[72] VMB_DQ[31..0]

[72] FBB_CMD[31..0]

MF=0 Normal

ECD3 (DQ24~DQ31)

ECD2 (DQ16~DQ23)

ECD1 (DQ8~DQ15)

ECD0 (DQ0~DQ7)

10/26 N18P/N17P pin swap
U74003.E11 <-> U74003.F13
U74003.M2 <-> U74003.M4
U74003.M11 <-> U74003.M13
U74003.M13 <-> U74003.M11
U74003.N11 <-> U74003.M11

+FBVDDQ

U74003

03008-00030300

CK External Termination

R7401 40.2Ohm

R7402 40.2Ohm

C7401 0.01uF/16V

Data rate >3.5Gbps

MF=0 Normal

R7436 1 N/A 2 1210hm

R7435 1 N/A 2 1K0hm

C7433 820PF/50V

MF=1 Mirror

40 OHm_NET
FBB Partition 64..32
MF=0 Normal

[72] VMB_DQ[63..32]

MF=1 Mirror

ECD4 (DQ32~DQ39)

ECD5 (DQ40~DQ47)

ECD6 (DQ48~DQ55)

ECD7 (DQ56~DQ63)

+FBVDDQ

U74004

03008-00030300

CK External Termination

R7409 40.2Ohm

R7410 40.2Ohm

C7436 0.01uF/16V

Data rate >3.5Gbps

MF=1 Mirror

R7411 1 N/A 2 1210hm

R7412 1 N/A 2 1K0hm

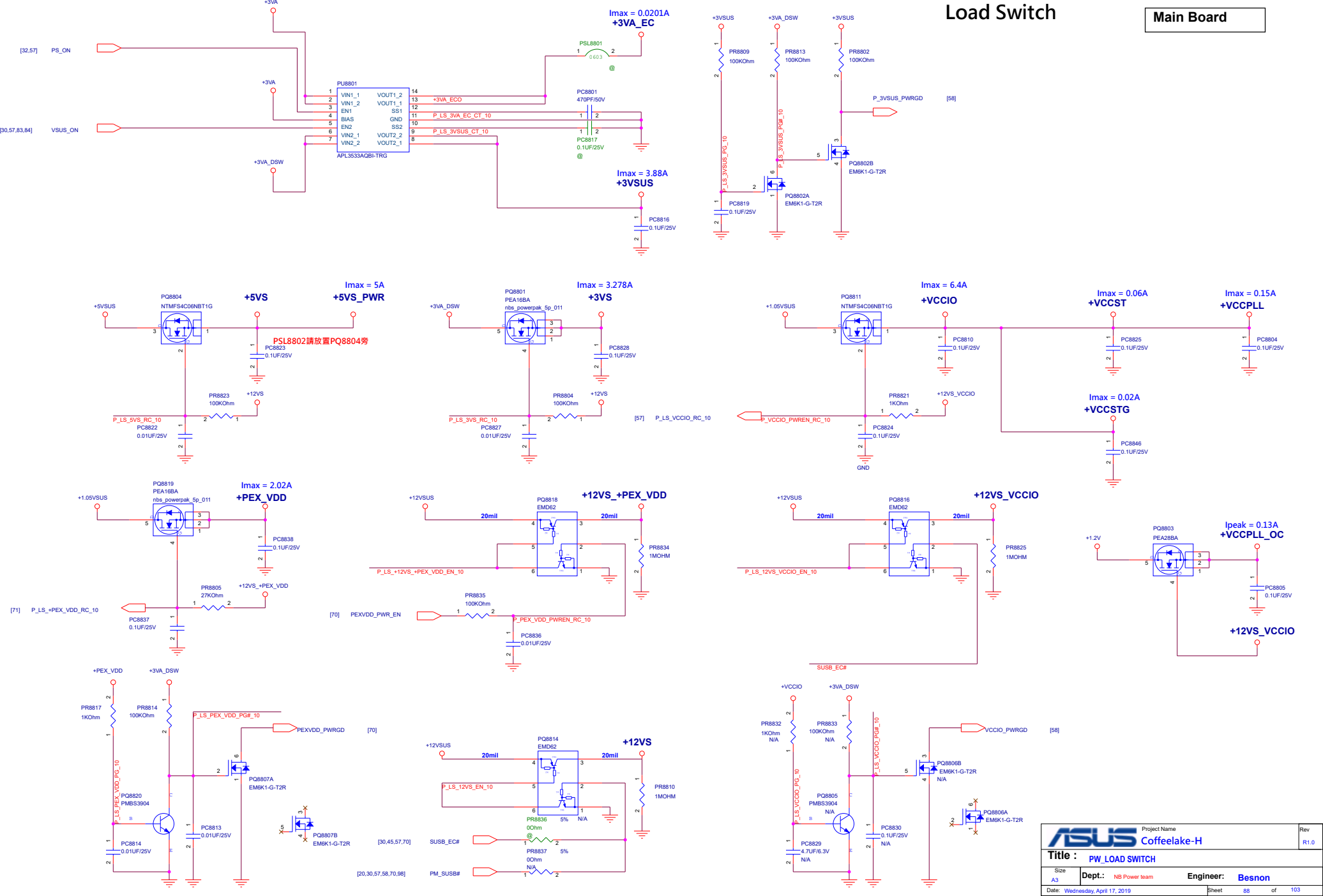
C7440 N/A

<Variant Name>

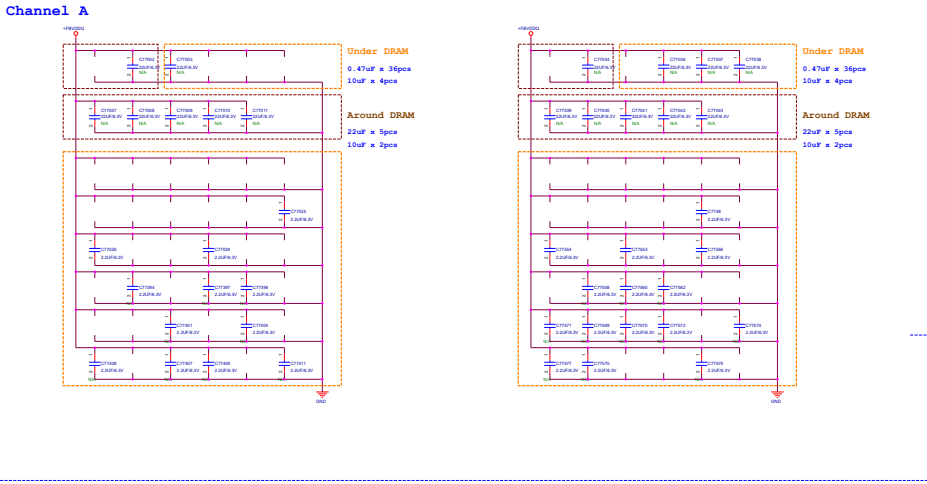
Title: <Title>			
Size: A1	Document Number: GT3YJ0K		Rev: 0.0.0
Date: Wednesday, April 17, 2019	Sheet: 73	of: 100	

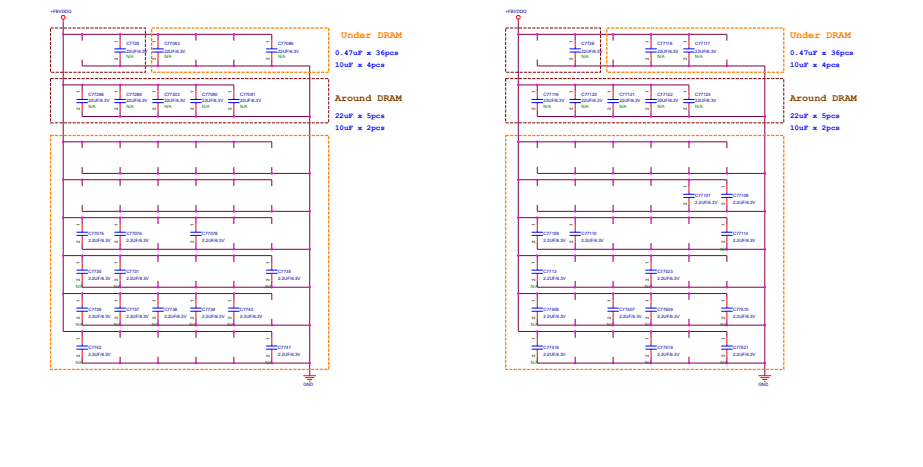
Load Switch

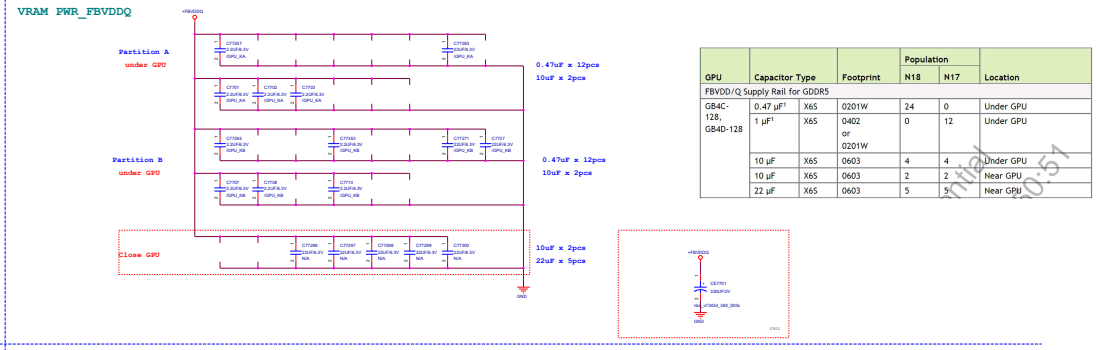
Main Board



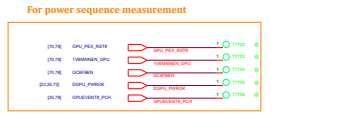
Project Name: Coffeelake-H			Rev: R1.0
Title: PW_LOAD SWITCH			
Size: A3	Dept.: NB Power team	Engineer: Besnon	
Date: Wednesday, April 17, 2019	Sheet 88 of 103		

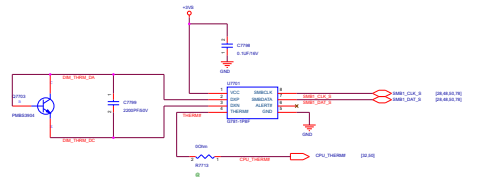






GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB4C-128, GB4D-128	0.47 µF[1]	X6S	0201W	24	0	Under GPU
	1 µF[1]	X6S	0402 or 0201W	0	12	Under GPU
	10 µF	X6S	0603	4	4	Under GPU
	10 µF	X6S	0603	2	2	Near GPU
	22 µF	X6S	0603	5	5	Near GPU





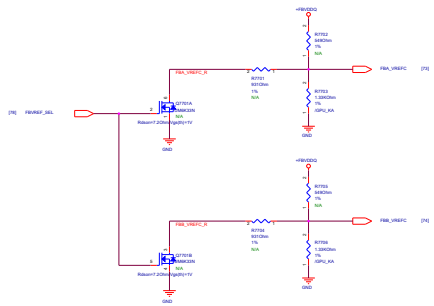


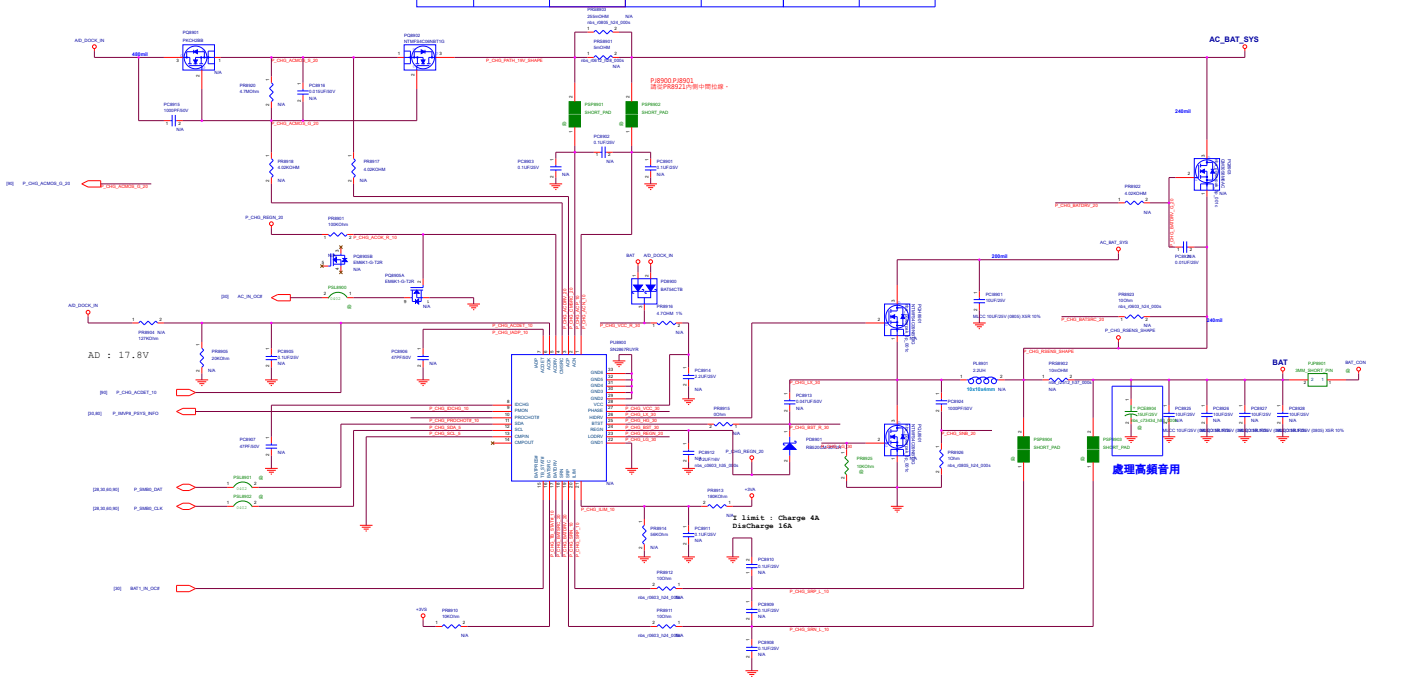
Table 8.42 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size NOTE 1]	Quantity	Placement (by DRAM Interface Mode)
Combined FBVDD-FBVDDQ Rail			
0.47 uF	X6S [0201W]	36 NOTE 2	Under the DRAM FBVDD or FBVDDQ ball. Add 16 of the 36 caps (or 16 of the 18 caps if using the alternate decoupling solution described in Note 2) under the DRAM FBVDD/Q ball; should share existing FBVDD/Q ball via if possible.
10 uF	X6S [0603]	4	Under the DRAM FBVDD or FBVDDQ ball.
10 uF	X6S [0603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X6S [0603]	5	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.

ASUS	Project Name: G731GX		Rev: X1.0
Title : VRM			
Size:	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 77 of 100		

PR88901	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-0008B100	10108-0008B000	10108-0009B000

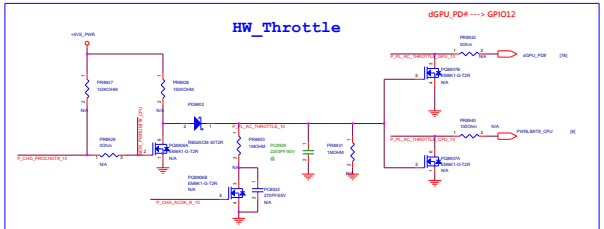
PR88903	ADP>120W	ADP=150W	ADP=180W	ADP=230W	ADP=280W	ADP=330W
	200m	255m	X	X	X	560m
	10114-0018B000	10114-0022I000	X	X	X	10114-0021I000



Adaptor select
total power = 90% ADP

Adaptor select

	M Series	S Series
PR8921	10m	5m
PR8936		
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	280W
270K	2.4V	90W	330W
560K	2.8V	120W	400W



ASUS	Project Name: Coffee lake-H	Rev: R1.0
Title :	PW_CHARGER	
Size: A2	Dept.: MB Power Team	Engineer: Benson
Date: Wednesday, April 17, 2019	Sheet: 85 of 103	

Address Selection Table

Address	0x98	0x90	0x9A	0x9E	0x92	0x96	0x9C	0xA0
R54(0Ω)	10k	5.23k	2k	3.32k	3.32k	5.23k	5.11k	8k
R54(0Ω)	Open	8.25k	6.23k	6.65k	6.75k	8.25k	8.75k	10k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	R	W	W	R	R	R	W
Function	Temp. alert threshold setting			Ground temp. data			bit 6 = 0 bit 5 = 0 bit 4 = 0 When ALERT# asserts.

PROTECTION

Cost-down不開

Cost-down不開

Cost-down不開

Cost-down不開

Cost-down不開

Cost-down不開

Cost-down不開

Cost-down不開

Cost-down不開

Table 2. TRUTH TABLE

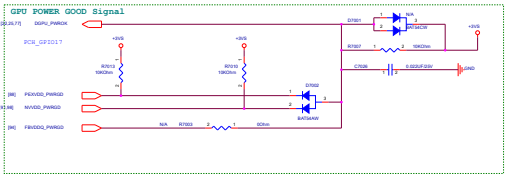
S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

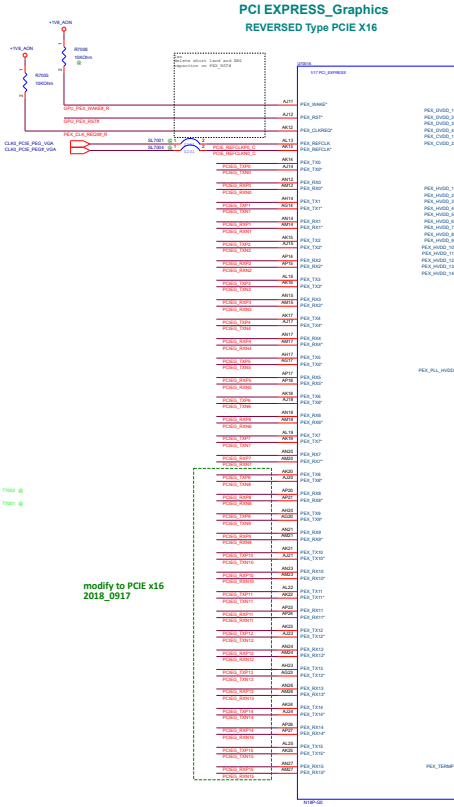
單獨下地

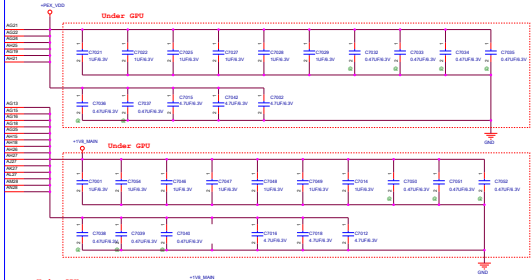
OVP Protection circuit 24V-=>Cost down

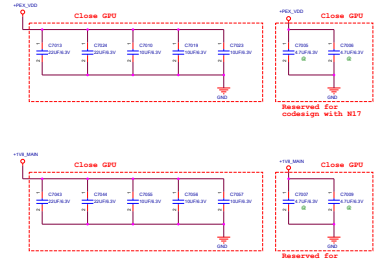
AC_Short_Protection

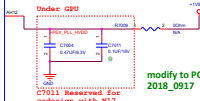
ASUS	Project Name: GM501GS		Rev: R1.0
Title: PW Reference			
Size: A3	Dept.: NB Power Team	Engineer: Edison	
Date: Wednesday, April 17, 2019	Sheet: 90 of 105		



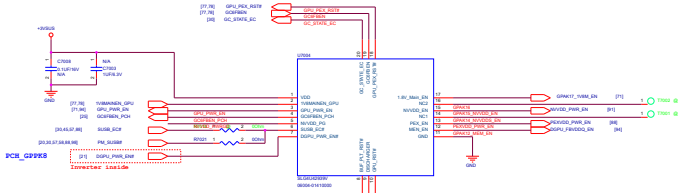


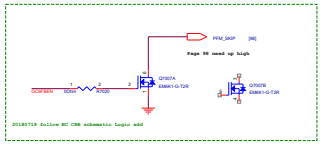






GPU POWER SEQUENCE CONTROL





Optimus

DGPU_PWR_EN#	FUNCTION
H	GC OFF
L	GC ON

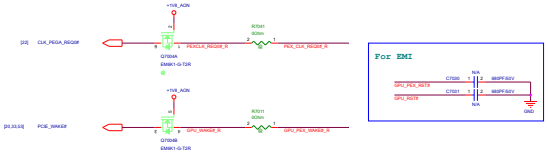


Table 6. PEX PLLs Decoupling and Filtering

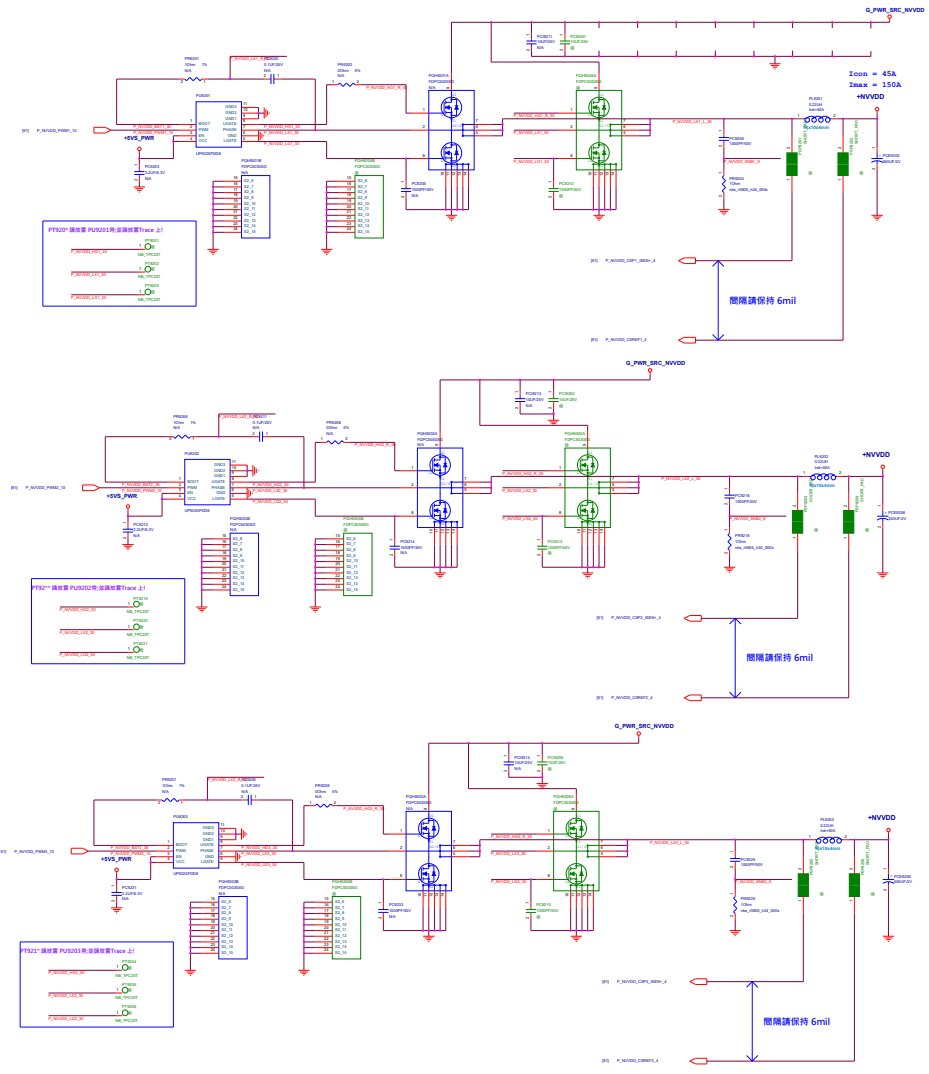
GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
PEX_PLL_HVDD Supply Rail					
GB4C-128, GB4D-128	0.1 µF	X7R	0402	0	1	Under GPU
	0.47 µF[1]	X6S	0201W	1	0	Under GPU

PEX_DVDD Supply Rail						
GB4C-128, GB4D-128	1.0 µF[1]	X6S	0402 or 0201W	0	4	Under GPU
	0.47 µF[1]	X6S	0201W	12	0	Under GPU
	4.7 µF	X6S	0603	0	2	Near GPU
	4.7 µF	X6S	0603	3	0	Under GPU
	10 µF	X5R	0805	0	1	Midway between GPU and power supply
	10 µF	X6S	0805	3	0	Near GPU
	22 µF	X5R	0805	0	1	Midway between GPU and power supply
	22 µF	X6S	0805	2	0	Near GPU

PEX_HVDD Supply Rail						
GB4C-128, GB4D-128	1.0 µF[1]	X6S	0402 or 0201W	0	4	Under GPU
	0.47 µF[1]	X6S	0201W	13	0	Under GPU
	4.7 µF	X6S	0603	0	2	Near GPU
	4.7 µF	X6S	0603	3	0	Under GPU
	10 µF	X5R	0805	0	2	Midway between GPU and power supply
	10 µF	X6S	0805	3	0	Near GPU
	22 µF	X5R	0805	0	1	Midway between GPU and power supply
	22 µF	X6S	0805	2	0	Near GPU

modify to PCIE x16 2018_0716

+NVVDD [For DGPU]



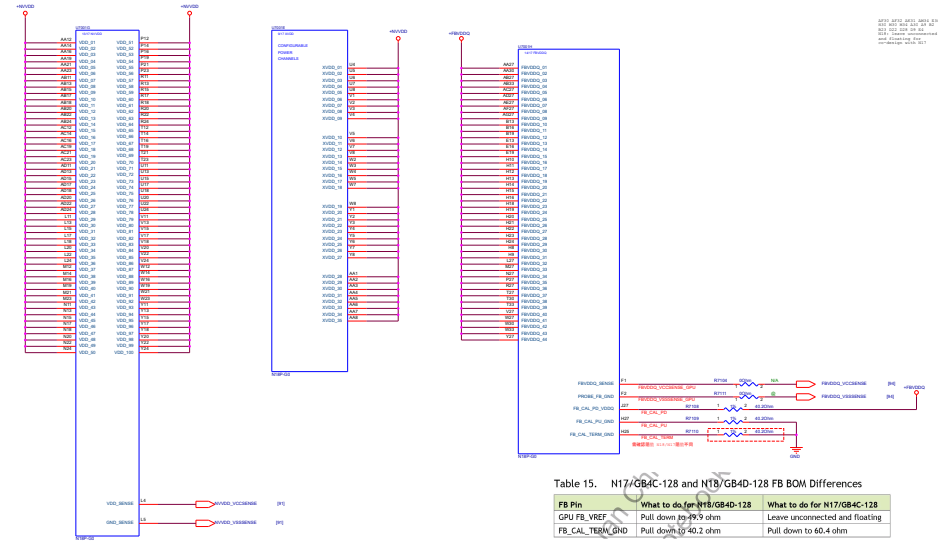
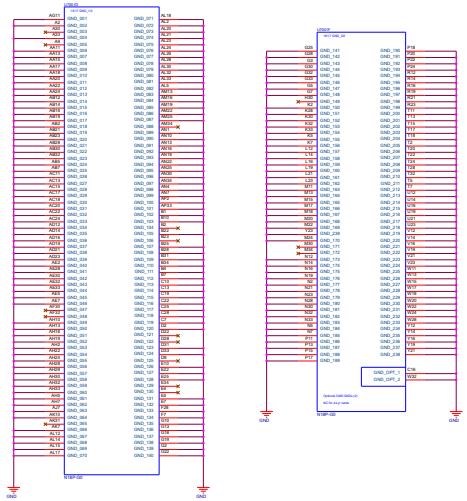
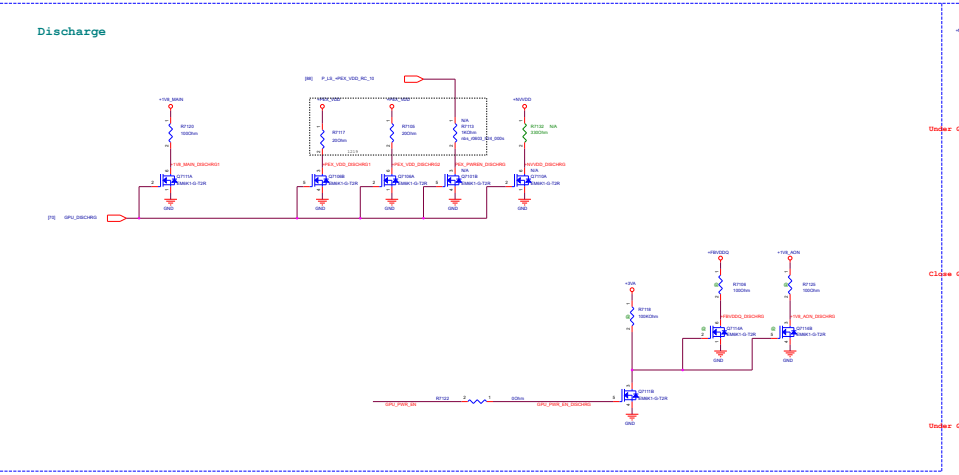
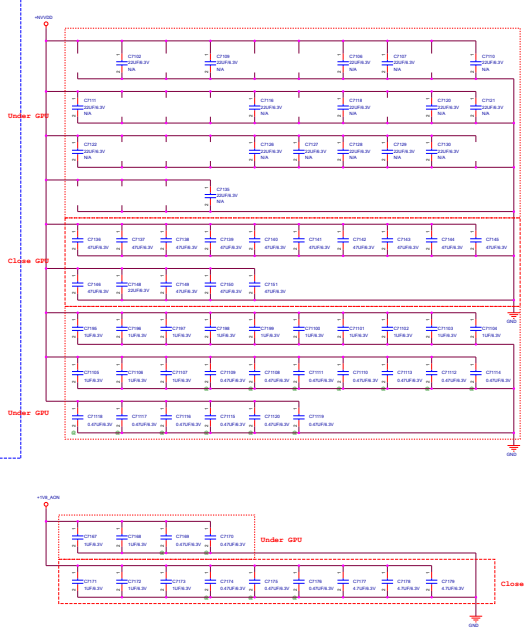


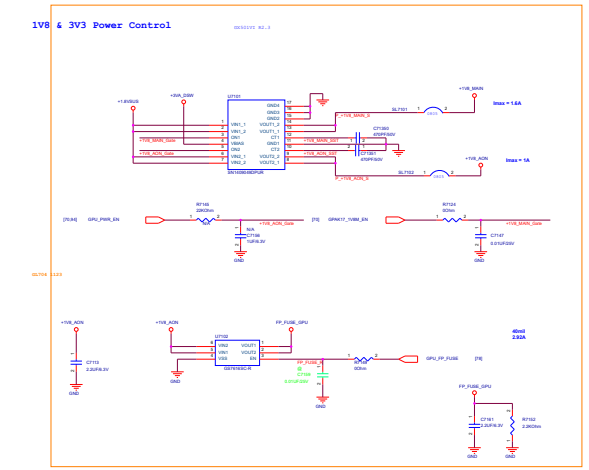
Table 15. N17/GB4C-128 and N18/GB4D-128 FB BOM Differences

FB Pin	What to do for N18/GB4D-128	What to do for N17/GB4C-128
GPU FB_VREF	Pull down to 49.9 ohm	Leave unconnected and floating
FB_CAL_TERM_GND	Pull down to 40.2 ohm	Pull down to 60.4 ohm









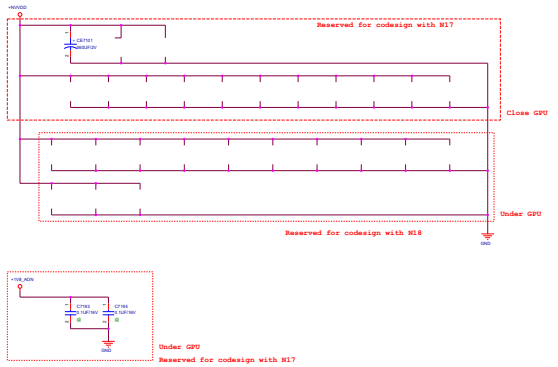


Table 2. NVVDD Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N18	Population N17	Location
NVVDD Supply Net						
GB4C-128, GB4D-128	10 µF	X6S	0603	34	21	Under GPU
	1 µF[1]	X6S	0402 or 0201W	0	13	Under GPU
	0.47 µF[1]	X6S	0402 or 0201W	26	0	Under GPU
	10 µF	X6S	0603	0	11	Near GPU
	22 µF	X6S	0805	15	10	Near GPU
	4.7 µF	X6S	0603	0	2	Near GPU
	330 µF	POS	7343	0	1	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

1V8_AON Supply Rail						
GB4C-128, GB4D-128	0.1 µF	X7R	0402	0	2	Under GPU
	0.47 µF[1]	X6S	0201W	4	0	Under GPU
	1.0 µF[1]	X6S	0402 or 0201W	0	1	Near GPU
	0.47 µF[1]	X6S	0201W	6	0	Near GPU
	4.7 µF	X6S	0603	3	1	Near GPU

ASUS	Project Name: GX701		Rev: 2.0
Title: GPU_POWER			
Size: A3	Dept.: ASUSTeK COMPUTER INC.	Engineer: Ashton_yang	
Date: Wednesday, April 17, 2019	Sheet: 77 of 100		

<Variant Name>

	Project Name **GX531GM**	Rev R1.0

Title : PW_PEX_VDD/+1.8V_GPU

Size			
Custom	**Dept.:** NB Power Team	**Engineer:** Joe	
Date: Wednesday, April 17, 2019	Sheet 93	of 117	

<Core Design>

	Project Name GM531GM	Rev R1.0

Title : PW_+VCCIO

Size		
A3	**Dept.:** NB Power team	**Engineer:** *Joe*

Date: Wednesday, April 17, 2019	Sheet	82	of 103

+FBVDDQ [For VRAM]

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.5V	1.35V
PR9404	10KOhm	
PR9409	35.7KOhm	
PR9423	54.9KOhm	

Imax= 20A
OCP= 40A

+FBVDDQ

PT940* 請放置 PU9401旁;並請放置Trace 上!

<Variant Name>

	Project Name **GX531GM**	Rev R1.0

Title : PW_PEX_VDD/+1.8V_GPU

Size			
Custom	**Dept.:** NB Power Team	**Engineer:** Joe	
Date: Wednesday, April 17, 2019	Sheet 95	of 117	

<Variant Name>

	Project Name **Coffeelake-H**	Rev R1.0

Title : PW_+12VS_FAN

Size			
B	**Dept.:** NB Power team	**Engineer:** Hon	
Date: Wednesday, April 17, 2019	Sheet 96	of 103	

Project Name

GX531GM

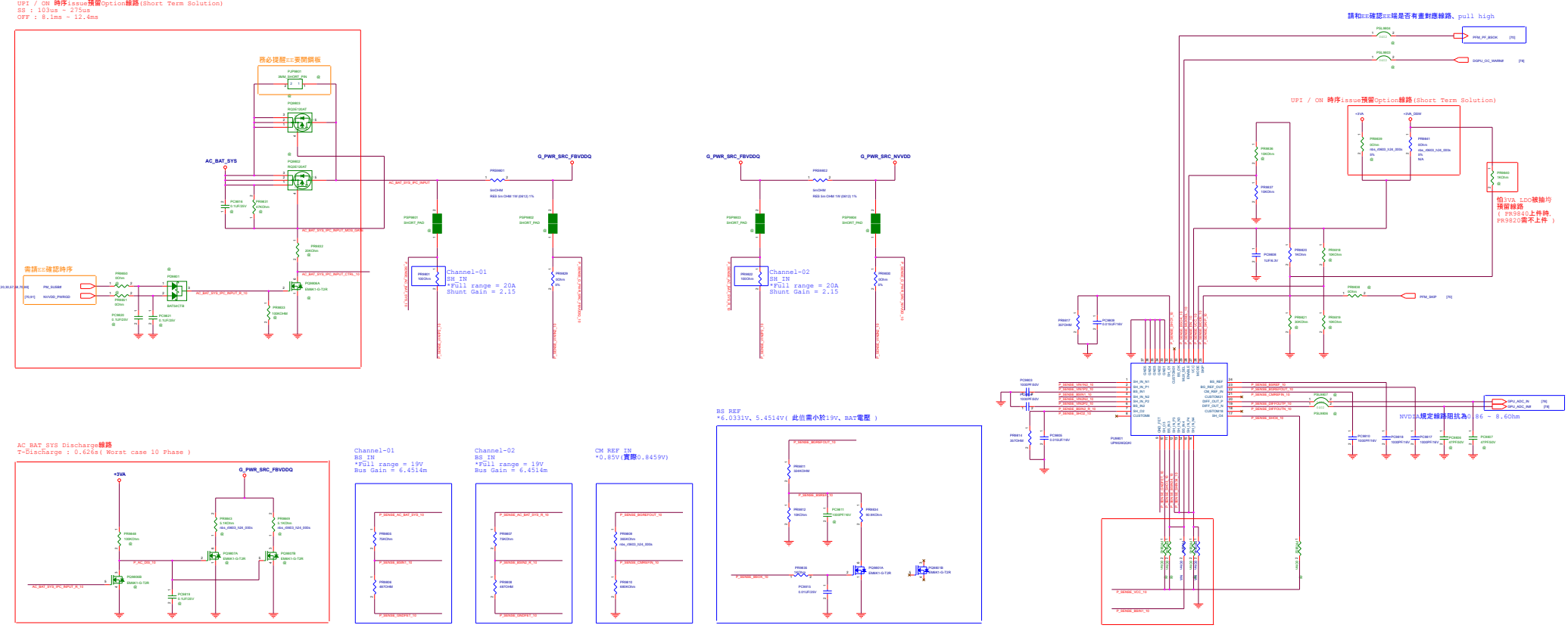
Rev

R1.0

Title : Type C LDO 3V3

Size	Dept.:	Engineer:
Custom	ASUSTeK COMPUTER INC.	Joe

Date:	Sheet	of
Wednesday, April 17, 2019	97	103



N18E

150W+

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100Ω(10G212100014010)	
PR9817	127Ω (10G212127014010)	169Ω (10G212169014010)
PR9822	100Ω(10G212100014010)	
PR9814	127Ω (10G212127014010)	169Ω (10G212169014010)
PR9805	75kΩ(10G212750214010)	
PR9806	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9807	75kΩ(10G212750214010)	
PR9808	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9811	324kΩ (10G212324314010)	243kΩ (10G212243314010)
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

115W ~ 130W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	143Ω (10G212143014010)	191Ω (10G212191014010)
PR9814	143Ω (10G212143014010)	191Ω (10G212191014010)

100W ~ 110W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	165Ω (10G212165014010)	221Ω (10G212221014010)
PR9822		
PR9814	165Ω (10G212165014010)	221Ω (10G212221014010)

75W ~ 90W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	215Ω (10102-00571000)	287Ω (10G212287014010)
PR9822		
PR9814	215Ω (10102-00571000)	287Ω (10G212287014010)

75W-

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9822		
PR9814	357Ω (10G212357014010)	475Ω (10G212475014010)

N18P

75W-

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100Ω(10G212100014010)	
PR9817	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9822	100Ω(10G212100014010)	
PR9814	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9805	75kΩ(10G212750214010)	
PR9806	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9807	75kΩ(10G212750214010)	
PR9808	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9811	324kΩ (10G212324314010)	243kΩ (10G212243314010)
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

150w+

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G212200014010)	
PR9817	127Ω (10G212127014010)	
PR9822	200Ω(10G212200014010)	
PR9814	127Ω (10G212127014010)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

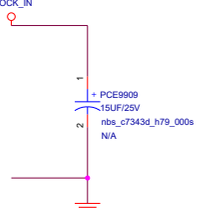
115W ~ 130W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G212200014010)	
PR9817	143Ω (10G212143014010)	
PR9822	200Ω(10G212200014010)	
PR9814	143Ω (10G212143014010)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

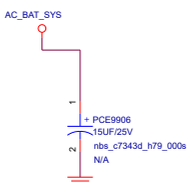
75W ~ 90W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G212200014010)	
PR9817	215Ω (10102-00571000)	
PR9822	200Ω(10G212200014010)	
PR9814	215Ω (10102-00571000)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

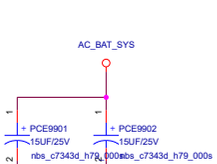
A/D_DOCK_IN



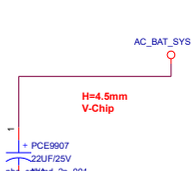
5VSUS



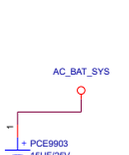
VCORE



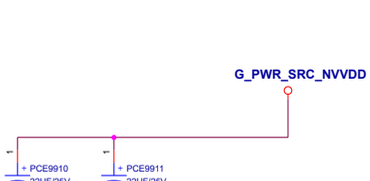
Charger



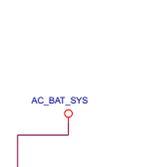
GT



NVVDD (X50)



1.05



FBVDDQ

1.2

***共11顆**
***請將對應電容放置對應PWR VRM輸入端**

<Variant Name>

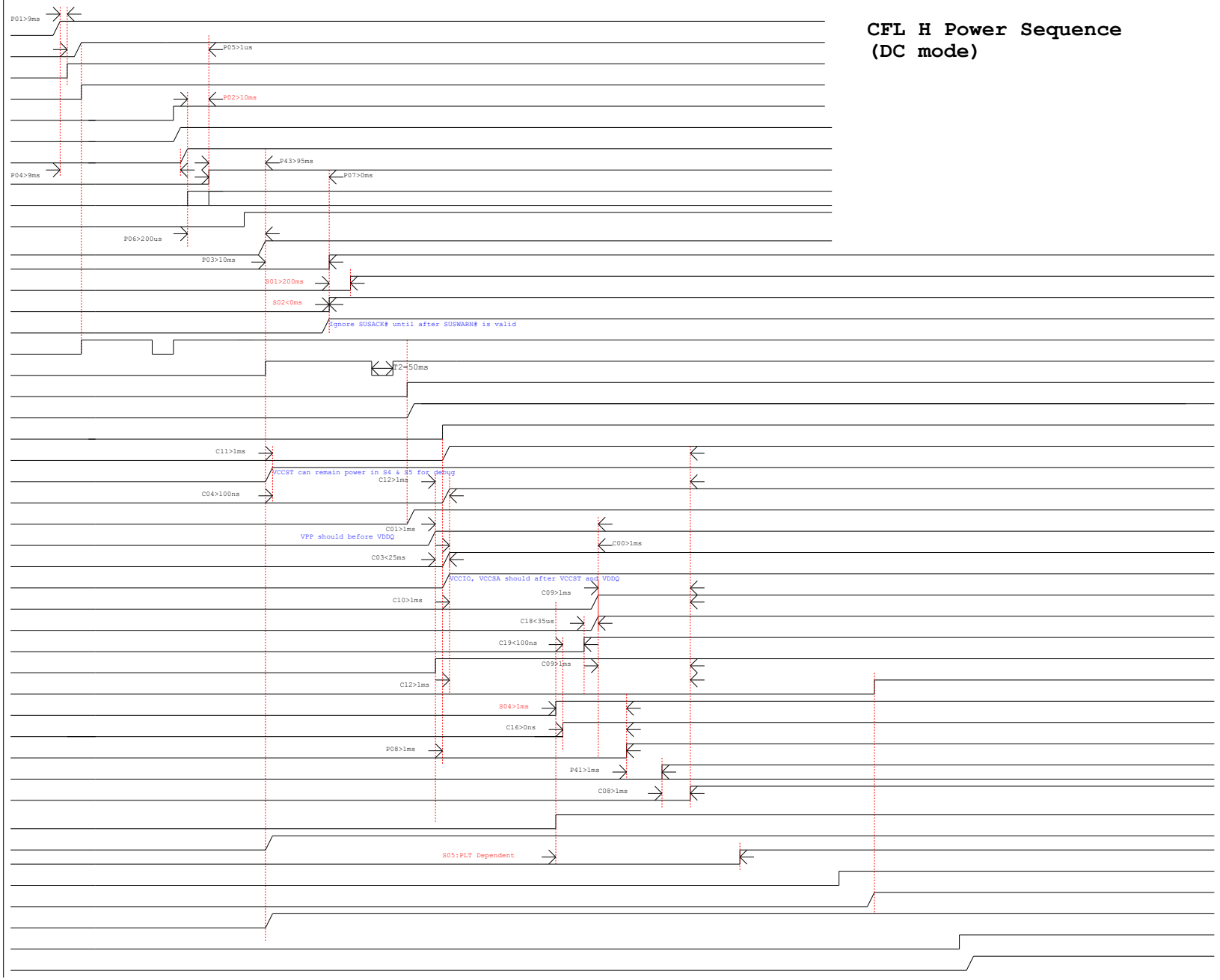
ASUS	Project Name: GM531GX	Rev: R1.0
Title : PW_Input CAP		
Size: Custom	Dept.: Power Team	Engineer: Joe
Date: Wednesday, April 17, 2019	Sheet 99 of 102	

CFL H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT)+3VA_RTC
(AC_BAT_SYS)+3VA/+5VA
(+3VA_RTC)RTCRST#(PCH)
(Power)AC_IN_OC#(EC)
(EC)PS_ON(+3VA_EC)
(PS_ON)+3VA_EC(EC)
(3VADSW_ON)+3VA_DSW(3VA_DSW_PWRGD)
(EC)DPWROK_EC(PCH)
(+3VA_DSW)PM_BATLOW#(PCH)
(PCH)PM_SLP_SUS#(EC)
(VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
(EC)PM_RSMRST#_PCH(PCH)
(PCH)SUSWARN#(EC)
(EC)ME_AC_PRESENT_PCH(PCH)
(EC)PCH_SUSACK#(PCH)
(PWR Switch)PWR_SW#(EC)
(EC)PM_PWRBTN#(PCH)
(EC)SUSC_EC#(Power)
(SUSC_EC#)+12V/+5V/+3V
(EC)SUSB_EC#(Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(VSUS_ON)+1.0V_VCCST,VCCPLL(VCCST_PWRGD)
(+VCCIO)+VCCSTG
(1.2V_ON)+2.5V(2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO(VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU)DDR_VTT_CTRL(Power)
(Power)1.2V_PWRGD(AND)
(Power)IMVP8_PWRGD
(AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
(EC)PM_PWROK_PCH(PCH)
(PCH)CLK_PCH_BCLK(CPU)
(PCH)H_CPUPWRGD(CPU)
(ALL_SYSTEM_PWRGD)P_IMVP8_EN_10(Power)
(CPU)P_SVID_DATA_X2(Power)
(EC)PM_SYSPWROK_PCH(PCH)
(PCH)PLT_RST#(CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
(CPU)H_THERMTRIP#(PCH)
(PCH)DDR4_DRAMRST#(Memory)
+VCCGT



Project Name: G731GX			Rev: R1.0
Title: Power On Timing-DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 101 of 103		

Rev	Date	Description
1.0	2017.03.03	P21 Remove CN
	2017.03.04	Q5602, Q5601 change for DXF Limitation
	2017.03.10	+1V9_MAIN, +3VS_NV Follow G753 Power sequence setting
	2017.03.11	R7821 Follow GL702 GPU Power seq
	2017.03.11	+PEX_VDD GPU Sequence update
	2017.03.14	PCE8104, PCE8107, PCE8106 update Cap for DXF Limit
	2017.03.14	GX501VIK Remove useless nut in P67
	2017.03.15	J5301 Connector list update
	2017.03.15	H6716, H6706, H6724, H6723 Screw Hole update
	2017.03.16	J5602 change LID SW for Angle Simulation
	2017.03.17	EMI Reserve C5606, C5607 Cap
	2017.03.17	RM3002, L4512, L4513, L4504, L4515, L4505 SWAP for Layout
1.1	2017.03.21	P30, P37, P39 AMP Change SNL04M25555
	2017.03.21	EMI Reserve P30 C77360 Cap and P69 Caps and Spring
	2017.03.23	AMP Change Remove P37 MUTE CONTROL schematic
	2017.03.23	AMP Change Reserve Q3701
	2017.03.27	P71 +PBVDDQ Discharge setting Follow G753 Power sequence setting
	2017.03.29	P12 Remove TBT Power Low Switch for Layout
1.2	2017.03.30	Change Cap C7105, C7101 for thermal request
	2017.03.30	Thermal Request for H6728
	2017.04.05	EMI Reserve Cap and Spring in P69
	2017.04.06	Reserve C2601 for +VCCPGPP_EF Ripple
	2017.04.07	25.00MHZ Cap C1126, C1124 change for Vendor Suggest
	2017.04.07	27MHz Cap C7811, C7801 change for Vendor Suggest
2.0	2017.04.11	P48 Reserve 0 ohm for SDA and SCL
	2017.04.17	P71 Add Caps for NVVDD Ripple
	2017.04.18	Q5704 Chnage MOS for DXF Limitation
	2017.04.20	P71 Add Caps for NVVDD Ripple
	2017.04.21	P67 Screw Hole H6705 update
	2017.04.21	P71 Add Caps for NVVDD Ripple C71119~C71122
	2017.04.25	P71 C7122, C7123, C7127, C7135, C7143, C7144, C7156, C7164, C7166,, C7186, C7187 change to 100UF
	2017.04.25	P70 C7007, C7002 change to 4.7UF
	2017.04.25	P70 C7020, C7024 change to 22UF
	2017.05.02	EMI Reserve C6948, C6949, C6950, C6951, C6952, C6953, C6954 and remove U6913
	2017.05.02	H6711, H6712 change screw hole type fot EMI Solution
	2017.05.03	Remove J4502 Pin 36 GND fot Factory Issue
	2017.05.05	P88, P58 Remove VCCST_PWRGD signal
	2017.05.05	P79, P45 Remove eDP Lan2 and Lan3 Signal
	2017.08.10	P31 R3121,R3122 change to unmount

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK COMPUTER INC.

Title : Revision History

Engineer: Gaming RD

Size	Project Name	Rev
D	G731GX	1.0

Date: Wednesday, April 17, 2019 Sheet 102 of 103

EE PART

G731GX SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							
60NB0H10-MB1030	R2.0	GX501VSK SKU1	/I7-7700HQ	/230W	8G_Hynix	V8G_Samsung			
60NB0H10-MB2000	R2.0	GX501VSK SKU2	/I5-7300HQ	/230W	8G_Hynix	V8G_Samsung			

1. CPU: INT I7-7700HQ 2.8G/6M SR32Q BGA 01001-01380600
CPU: INT I5-7300HQ 2.5G/6M SR32S BGA 01001-01380500

2. dGPU: nVidia N17E-G2-A1 FCBGA2152 02004-00480500

4. EC: ITE IT8995VG-128/DX --06037-00050800

5.onboard menory
8G_ Hynix 03012-00030400

9. Card Reader: AU6435--02G630002400 (Page42)

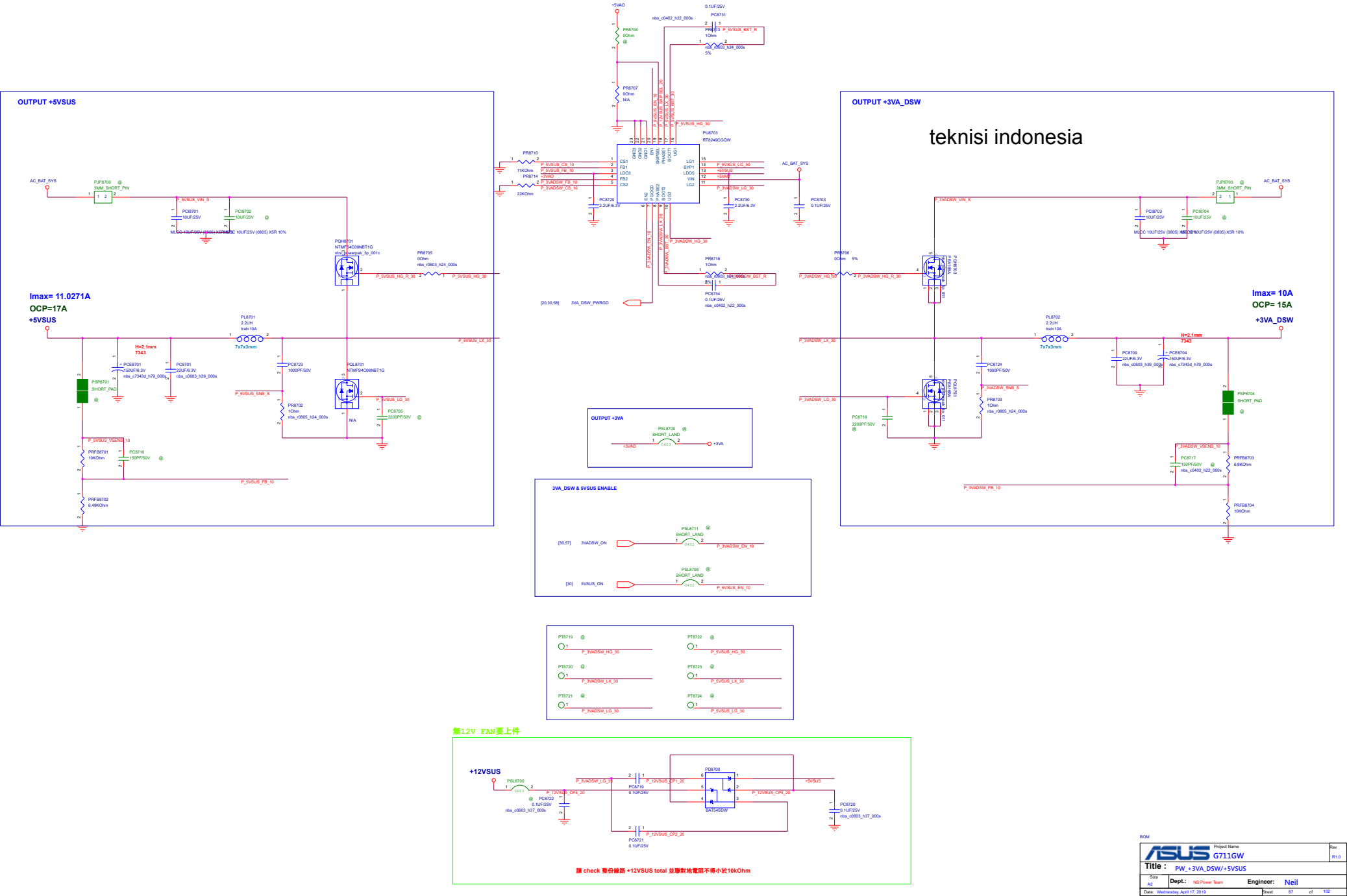
10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

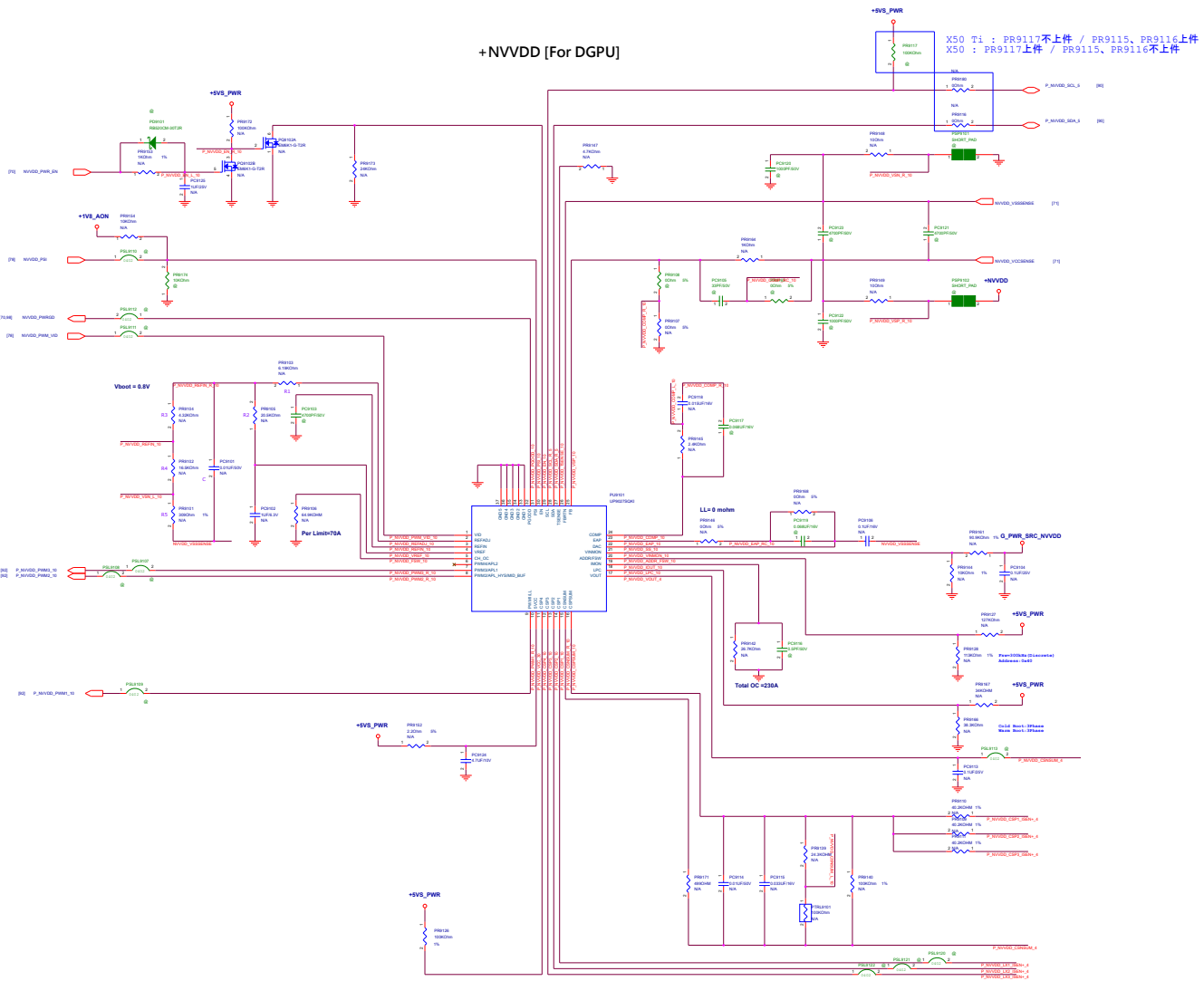
		Title :	UX362_SKU Table_R1.0
ASUSTeK COMPUTER		Engineer:	Gaming RD
Size	Project Name		Rev
C	G731GX		R1.0
Date:	Wednesday, April 17, 2019	Sheet	of 103

+3VA_DSW / +5VSUS [System Power]



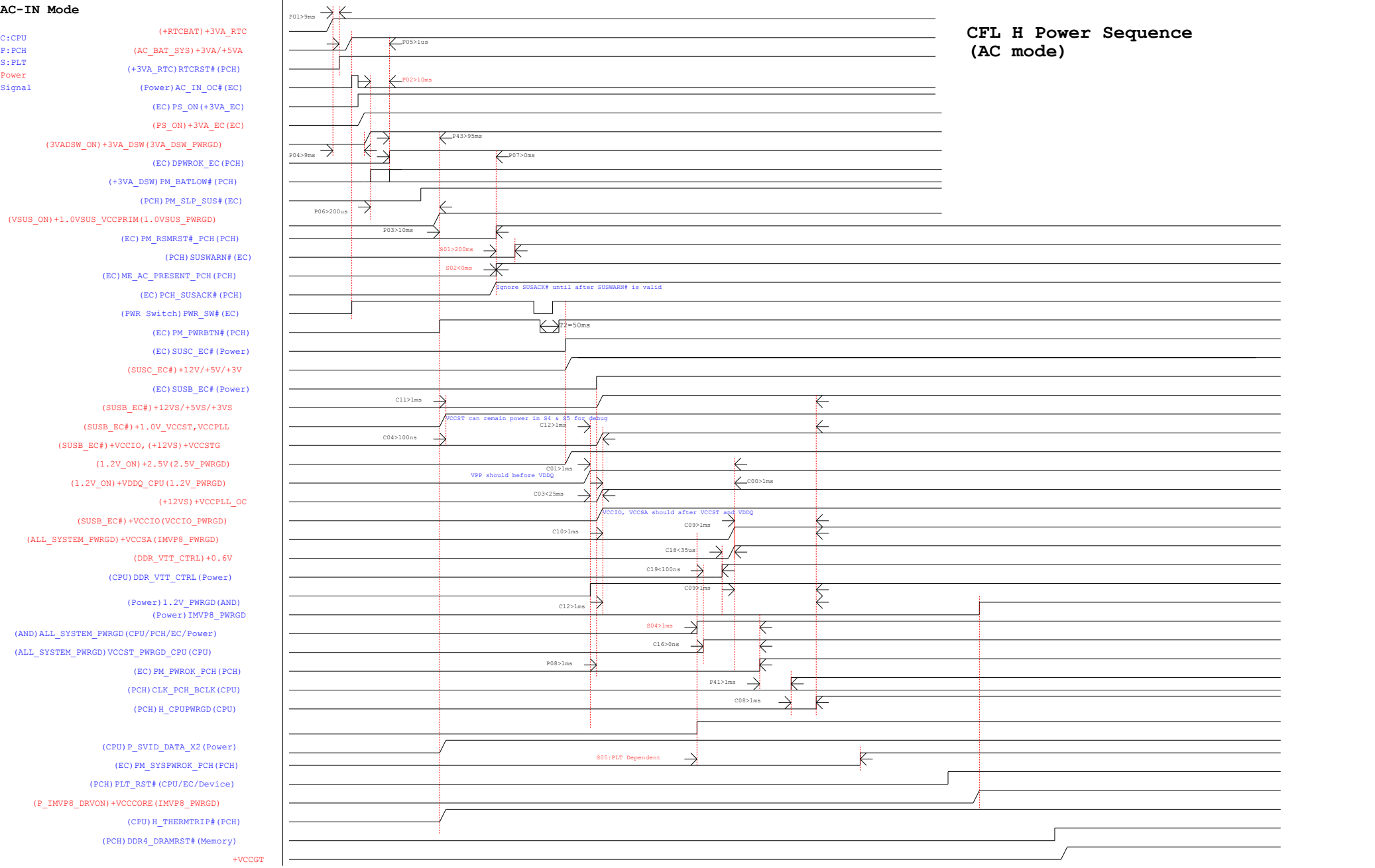
BOM

ASUS	Project Name: G711GW		Rev: R1.0
Title :	PW_+3VA_DSW/+5VSUS		
Size: A2	Dept.: NB Power Team	Engineer: Neil	
Date: Wednesday, April 17, 2019	Sheet 87 of 102		



ASUS	Project Name: G711GW		Rev: 30.0
Title :	PW_+NVVDD (1)		
Size: Custom	Dept.: KB Power team	Engineer: Neil	
Date: Wednesday, April 17, 2019	Sheet: 61 of 103		

AC-IN Mode



CFL H Power Sequence (AC mode)

ASUS	Project Name: G731GX		Rev: R1.0
Title : Power On Timing--AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, April 17, 2019	Sheet 100 of 103		

XS_PLLVDD (N18: XSN_PLLVDD) Supply Rail						
GB4C-128	0.1 µF	X7R	0402	0	1	Under GPU
GB4D-128	0.47 µF	X6S	0201W	1	0	Under GPU
	Bead Type					
	300 Ω @ 100 MHz (ESR=0.2 Ω)		0402	0	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails						
GB4C-128, GB4D-128	0.1 µF	X7R	0402	0	2	Under GPU
	0.47 µF[1]	X6S	0201W	2	0	Under GPU
	Bead Type					
	300 Ω @ 100 MHz (ESR=0.010 Ω)		0603	0	0	Near GPU
GPCPLL_AVDD Supply Rail						
GB4C-128, GB4D-128	0.1 µF	X7R	0402	0	1	Under GPU
	0.47 µF[1]	X6S	0201W	1	0	Under GPU
	4.7 µF	X6S	0603	1	1	Near GPU

GPU	Type	Footprint	Population N18	Population N17	Location
	22 µF	X5R	0805	0	1	Near GPU
	22 µF	X6S	0805	1	0	Near GPU
	Bead Type					
	30 Ω @ 100 MHz (ESR=0.010 Ω)		0603	1	1	Near GPU

Note:
1. Design may alternatively use one 0201W 0.47 µF X6S for each 0.22 µF.

Table 15.1 GPIO Descriptions for GB4D-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	No PU/PD
GPIO1	GC6: GC6_FB_EN	I/O	FB Enable for GC6 2.1	10 kΩ pull-down
GPIO Number	**GPIO Name**	**I/O**	**Functional Description**	**I/O Termination**
GPIO2	GC6:GPU_EVENT	I/O	GPU wake signal for GC6 2.1	10 kΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	UNUSED	O		
GPIO4	GC6: 1V8_MAIN_EN	I	GPU power sequencing for GC6 2.1	10 kΩ pull-up to 1V8_AON
GPIO5	FRAME_LOCK*	O	Active low Frame Lock	10 kΩ pull-up to 1V8_AON
GPIO6	NVVDD_PSI*		Phase Shedding Pace Section 15.2.1	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	LCD Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or "power supply overdraw input	10K Pull Up
GPIO13	UNUSED			
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	10K Pull Up to 1V8_AON
GPIO15	HPD_IFPB*	I	Hot Plug	10K Pull Up to 1V8_AON
GPIO16	UNUSED			
GPIO17	HPD_IFPD*	I	Hot Plug Detect for IFPD	10K Pull Up to 1V8_AON
GPIO18	HPD_IFPE*	I	Hot Plug Detect for IFPE	10K Pull Up to 1V8_AON
GPIO19	UNUSED	O		
GPIO20	GC6:NB_GC6	I/O		10K Pull Down
GPIO21	LCD_BLEN	O	LCD Panel Backlight enable	100K Pull Down
GPIO22	INA_HT* / ADC_MUX_SEL			2.2K Pull Up See circuit
GPIO23	Reserved			100K Pull Down
GPIO24	UNUSED	I		
GPIO25	FBVDD_PSI*			PU/PD with series resistor depending on PSI topology
GPIO26	FP_FUSE			10K Pull Down
GPIO27	HPD_IFPC*	I	Hot Plug detect for IFPC	10K Pull Up to 1V8_AON

Table 4. N18P-G0 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade
8 Gb	256Mbx32	1.35 V and 1.5V[1]	Micron	MT51J256M32HF-80:B	B-die	0x51	8 Gbps
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps
		1.35V and 1.55V[1]	Samsung	K4G80325FC-HC25	B-die	0x0	8 Gbps

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x000D)
L	L	H	1 (0x001)
L	H	L	2 (0x002)
L	H	H	3 (0x003)
H	L	L	4 (0x004)
H	L	H	5 (0x005)
H	H	L	6 (0x006)
H	H	H	7 (0x007)
L	L	R	8 (0x008)
L	H	R	9 (0x009)
L	M	R	10 (0x00A)
L	M	H	11 (0x00B)
L	M	L	12 (0x00C)
R	L	H	13 (0x00D)

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
R	H	L	14 (0x00E)
R	H	R	15 (0x00F)
H	L	R	16 (0x010)
H	M	L	17 (0x011)
H	M	H	18 (0x012)
H	M	R	19 (0x013)
L	M	R	20 (0x014)
R	M	R	21 (0x015)
R	M	L	22 (0x016)
R	M	M	23 (0x017)
R	M	H	24 (0x018)
H	L	L	25 (0x019)
H	M	M	26 (0x01A)

Strap Pins see Note			Functions Selected by This Strapping
STRAP6	STRAP4	STRAP3	SAR_ALT_ADDR	NB/VB_SEL	PCIE_CP9	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	1	1
L	L	R	0	1	0	0
L	H	L	0	1	1	1
L	H	H	1	0	0	0
L	H	R	1	0	1	1
L	M	L	1	1	0	0
L	M	H	1	1	1	1
H	L	L	1	1	0	0
H	L	H	1	1	1	1

Strap Pins see Note			Resulting SOR1_EXPOSED Enablements
ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	L	ENABLED	disabled	disabled	ENABLED
0	H	H	H	disabled	disabled	disabled	disabled
	A	A	A	Reserved, do not configure			
	All other Strap Configurations			Reserved, do not configure (Invalid)			

Strap Pins see Note			Physical Configuration
ROM_SO	ROM_SI	ROM_SCLK	Level Option	Pull-Up to 1.8V via resistor (see Note 1) (Notebook designs also see Note 2.)	Pull-Down to GND via resistor Ron
L	L	L	1.8V ("HIGH") Level	Populate	No Stuff
L	L	H	0.9V ("MIDDLE") Level	No Stuff	Populate
L	H	L	GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 200K Ohms, 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull down the VDD_AON_1V8 rail rather than to 1V8 MAIN.

Assorted Configuration Straps:
1. SMB_ALT_ADDR Enable: "0" (pull SMB_ALT_ADDR_EN low) Disabled, "1" (pull SMB_ALT_ADDR_EN high) Enabled, see Address assoc
2. DEVID_SEL: 0-sync function – "0"=normal GPU ID, "1" support 0-sync GPU ID.
3. PCIE_CFG: PCIE Swing – "0": PCIE Swing default, "1" PCIE swing reduce.
4. VGA_DEVICE: Graphics circuit –"0"; MS-Hybrid, "1" Discrete.

Strap Pins see Note			FS_OVERT Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT function ENABLED
L	L	H	FS_OVERT function DISABLED (Reserved, do not configure)
all other configurations			(Invalid, do not configure)

Base Index	Strap Pins see Note			Resulting SOR1_EXPOSED Enablements
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	L	ENABLED	disabled	disabled	ENABLED
0	H	H	H	disabled	disabled	disabled	disabled
	A	A	A	Reserved, do not configure			
	All other Strap Configurations			Reserved, do not configure (Invalid)			

Total Display Links (HDM, DP or DVI)				See Titan Bom at Table 5.6
	Total Enabled for Audio (HDM, DP or DVI)			
	Is eDP Supported on:			
	IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	
4	4	---	---	15
4	3	yes	---	14
4	3	---	yes	13
3	3	---	---	12
3	2	yes	---	11
3	2	---	yes	10
2	2	---	---	9
2	1	yes	---	8
2	1	---	yes	7
1	1	---	---	6
1	0	yes	---	5
1	0	---	yes	4

for N18x

Total Display Links (HDM, DP or DVI)				See Titan Bom at Table 5.6
	Total Enabled for Audio (HDM, DP or DVI)			
	Is eDP Supported on:			
	IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	
4	4	---	---	15
4	3	yes	---	14
4	3	---	yes	13
3	3	---	---	12
3	2	yes	---	11
3	2	---	yes	10
2	2	---	---	9
2	1	yes	---	8
2	1	---	yes	7
1	1	---	---	6
1	0	yes	---	5
1	0	---	yes	4

for N17x

VGA INT. Thermal sensor address 0x98 and 0x9C

VGA EXT. Thermal Sensor

Thermal Protection

Level shift HPD Invert

GPU GPIO INPUT

STRAP PIN

ASUS	Document Number: G733QX		Rev: 2.0
Title:	GPU_CLOCK&STRAPPING		
Size:	Dept: ASUSTeK COMPUTER	Engineer: Gaming RD	
Date: Wednesday, March 07, 2018		Sheet 19 of 141	