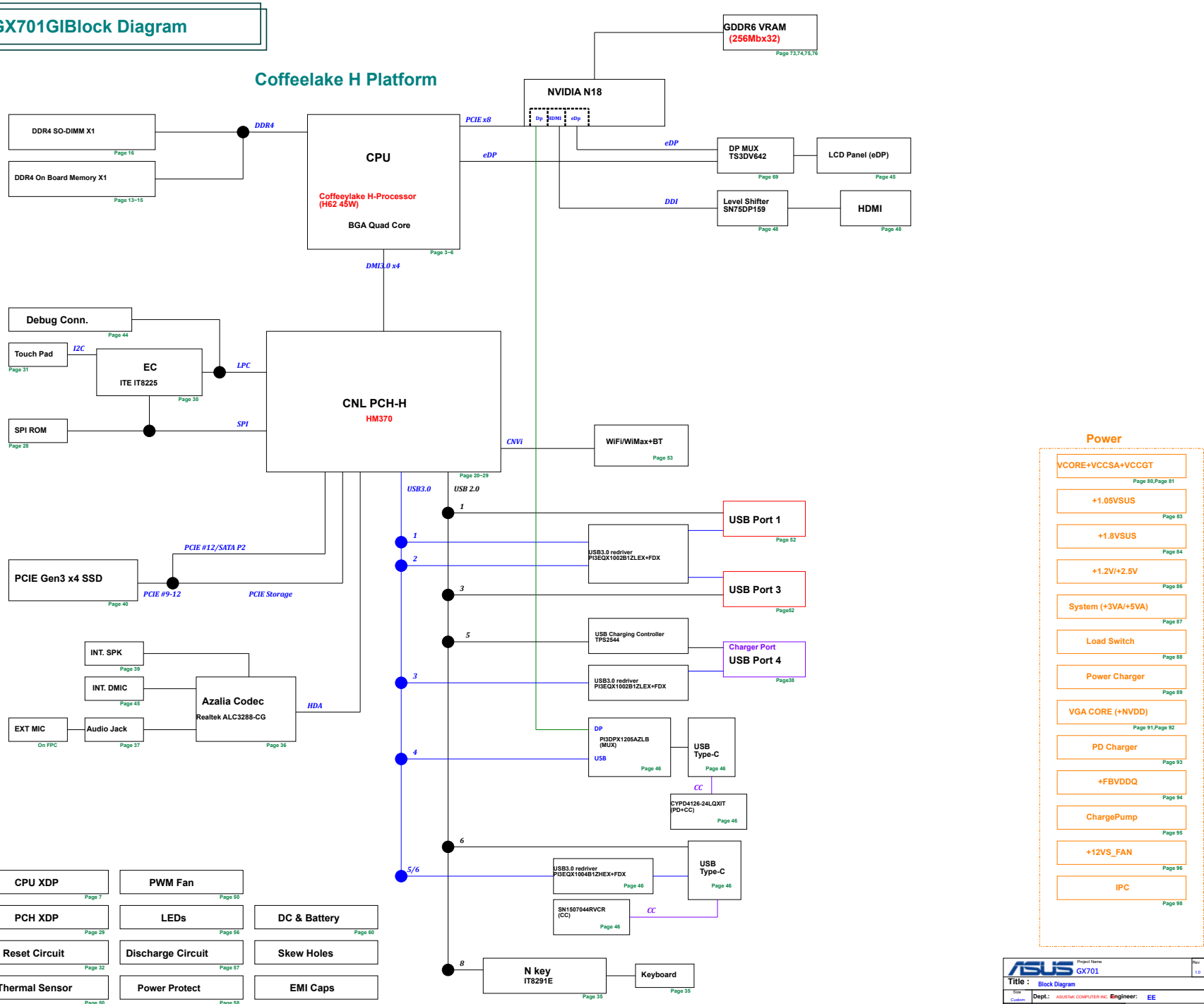
01. Block Diagram
02. System Setting
03. CPU_DMI/PEG/eDP/DDI
04. CPU_DDR4
05. CPU_GND
06. CPU_CFG/RSVD
07. CPU_XDP
08. CPU_PWR
09. CPU_PWR
10. CPU_POWER_CAP
11. TBT_Alpine-Ridge
12. TBT_TPS65982/Type C
13. DDR4_TERMINATION
14. DDR4_ON-BOARD_A(1)
16. DIM_DDR4 SO-DIMM B(0) TOP
18. DIM_CA/DQ Voltage
19. TBT_PWR
20. PCH-CPT(1)_IHDA/RTC/JTA
21. PCH-CPT(2)_PCIE/USB2/MISC
22. PCH-CPT(3)_CLK/LPC/USB3
23. PCH-CPT(4)_CRT/eDP/DP
24. PCH-CPT(5)_SPI
25. PCH-CPT(6)_GPIO
26. PCH-CPT(7)_POWER/GND
27. PCH-CPT(8)_POWER/GND
28. PCH-SPI ROM/OTH
29. PCH-XDP
30. KBC_IT8995
31. KBC_KB/TP
32. RST_Reset Circuit
35. Mac&N_KEY_IT8912E&MG84FG516
36. AUD-ALC295CG
37. AUD-Headphone
38. USB3.0 port
39. AUD-Speaker
40. NGFF_SSD
43. CB_GL3213
44. DEBUG_LPC
45. CRT_eDP
48. HDMI
50. FAN_Thermal Sensor & Fan
52. USB Charger
53. NGFF Type_WLAN&BT
56. LED & CON
57. DSG_Discharge
58. PRO_Protect
60. DC/BAT IN
67. screw hold
69. OTH_EMI
70. GPU_PCIE I/F
71. GPU_POWER
72. GPU_FRAME BUFFER
73. VRAM-CHANNEL A
74. VRAM-CHANNEL B
75. VRAM-CHANNEL C
76. VRAM-CHANNEL D
77. VRAM CAP/UP1905
78. GPU_CLOCK/STRAP/GPIO
79. GPU_LVDS/HDMI/Edp/DP/CRT
80. PW_KABYLAKE (1)
81. PW_KABYLAKE (2)
83. PW_+1.0VSUS
84. PW_+VCCIO
86. PW_1.2V/+VTT/2.5V
87. PW_+3VADSW/+5VSUS
88. PW_LOAD Switch
89. PW_CHARGER
90. PW_PROTECTION
91. PW_+NVVDD (1)
92. PW_+NVVDD (2)
93. PW_+NVVDDS
94. PW_+FBVDDQ
95. PW_OV
97. PW_PEX_VDD/+1.8V_GPU
98. PW_IPC
99. PW_FLOW CHART
100. Power On Timing--AC mode
101. Power On Timing--DC mode
102. History

GX701GIBlock Diagram

Coffeelake H Platform

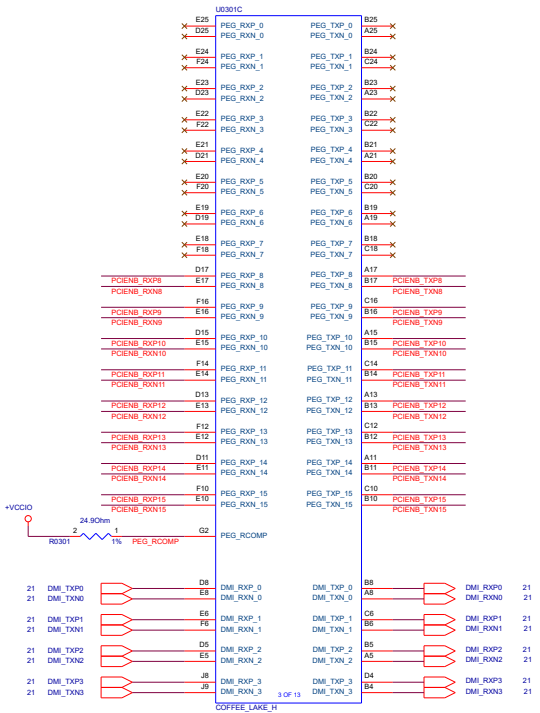


Power

- VCORE+VCCSA+VCCGT — Page 80,Page 81
- +1.05VSUS — Page 83
- +1.8VSUS — Page 84
- +1.2V/+2.5V — Page 86
- System (+3VA/+5VA) — Page 87
- Load Switch — Page 88
- Power Charger — Page 89
- VGA CORE (+NVDD) — Page 91,Page 92
- PD Charger — Page 93
- +FBVDDQ — Page 94
- ChargePump — Page 95
- +12VS_FAN — Page 96
- IPC — Page 98

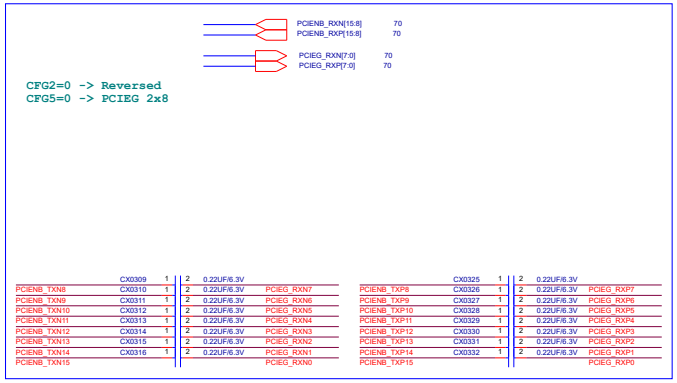
Project Name	GX701
Rev	1.0
Title :	Block Diagram
Size	Custom
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	EE
Date:	Wednesday, March 06, 2019
Sheet	1 of 100

PCIEG

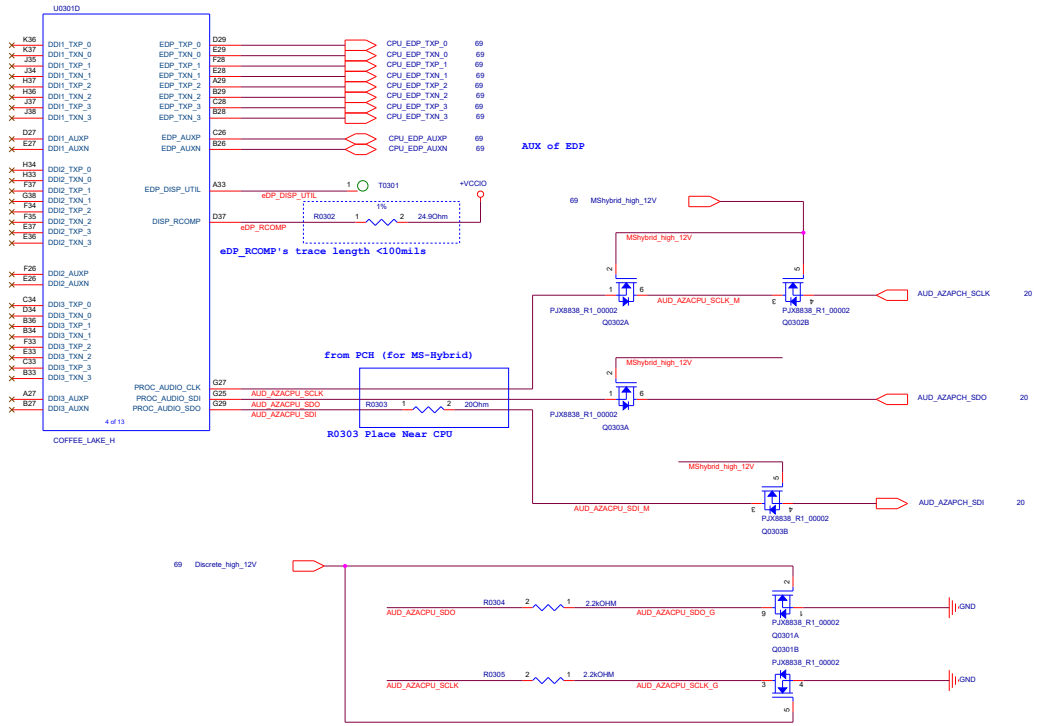


R0301 close to CPU
PEG_COMP trace length <400mils

R0.1-25



Display

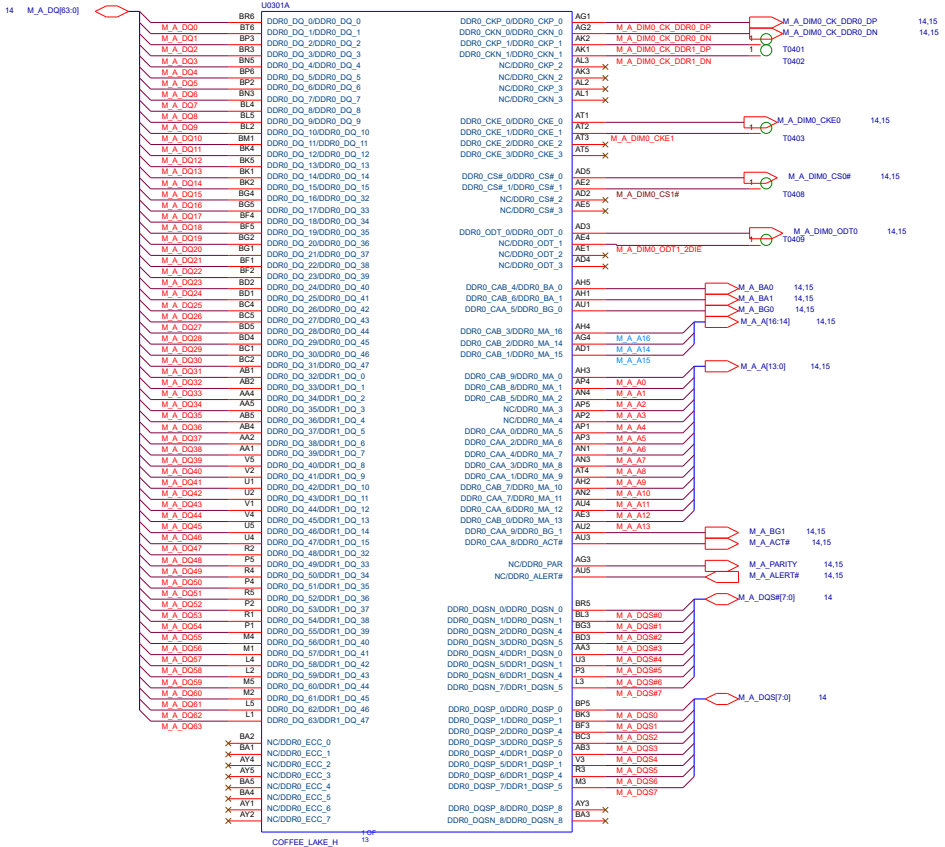


31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

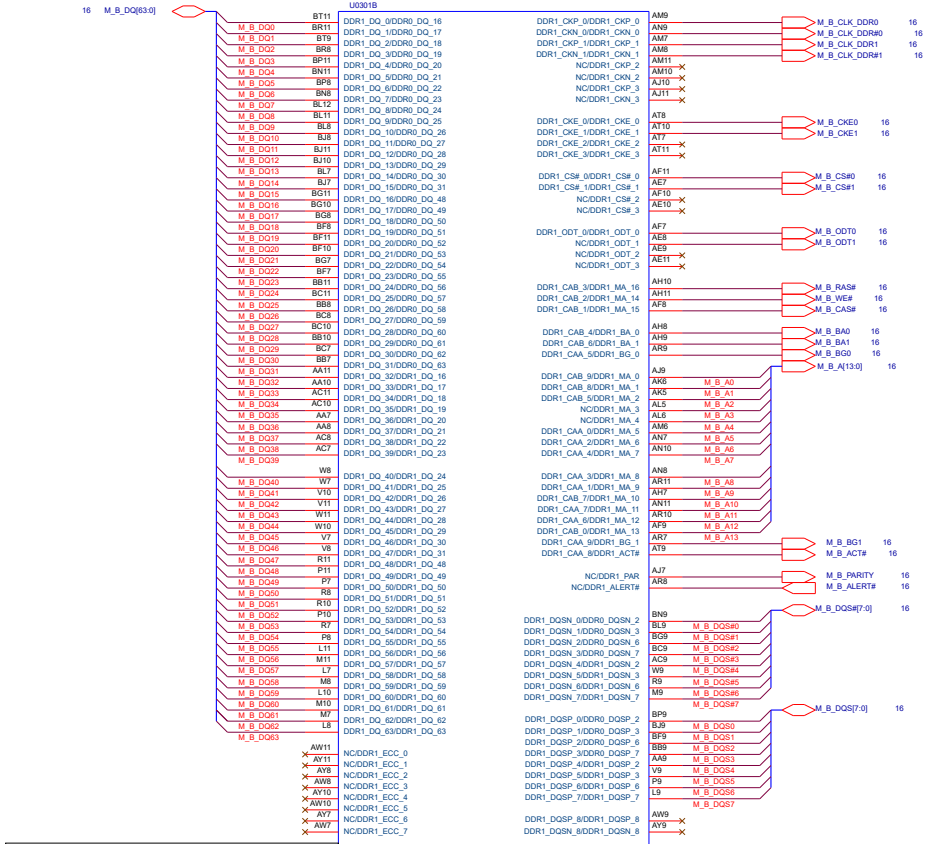
When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected.

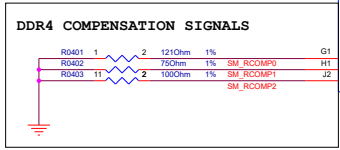
Memory Channel A



Memory Channel B

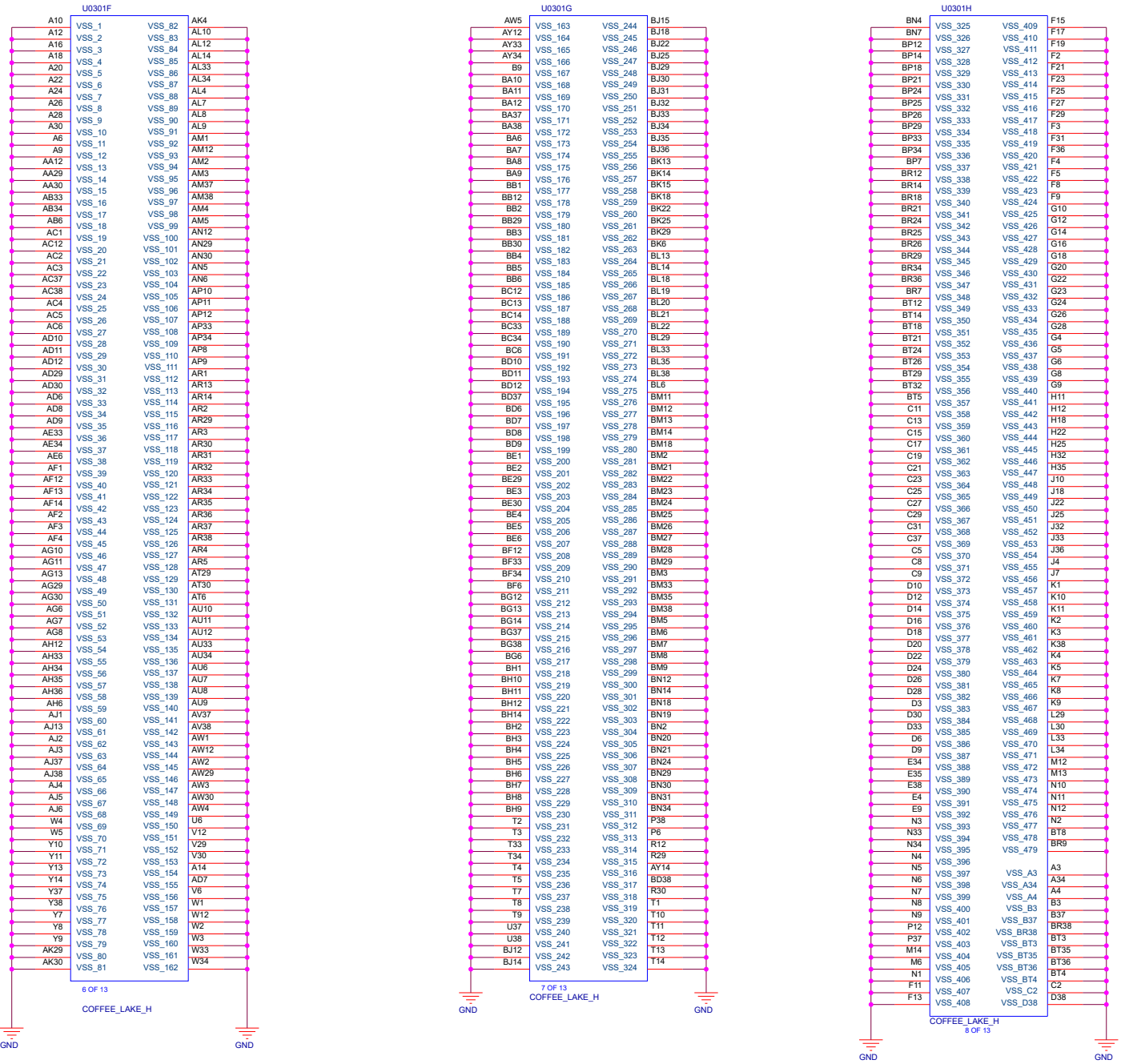


DDR4 COMPENSATION SIGNALS



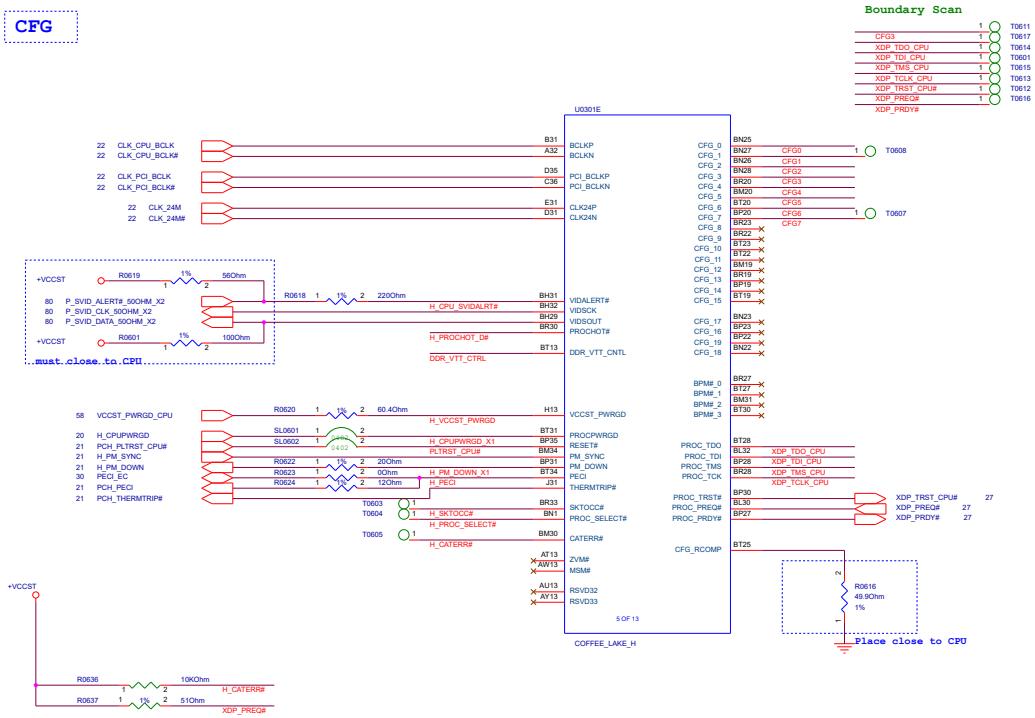
Project Name: GX701			Rev: 1.0
Title: CPU_DDR4			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 4 of 100		

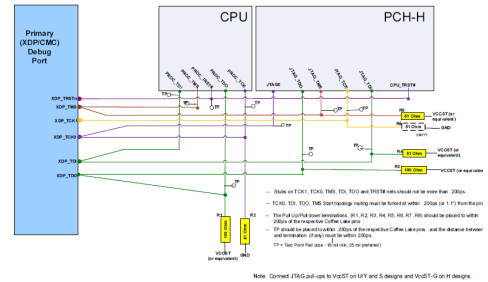
Main Board

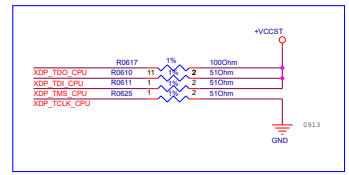


ASUS	Project Name: GX701		Rev: 1.0
Title : CPU_CFG,RSVD,GND			
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Wednesday, March 06, 2019	Sheet 5 of 100		

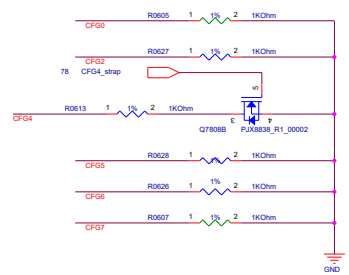
CFG







CFG Straps



CFG Straps for Processor

ref : Intel 570805_Coffeelake_EDS_Vol_1_Rev1.4 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Expres* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

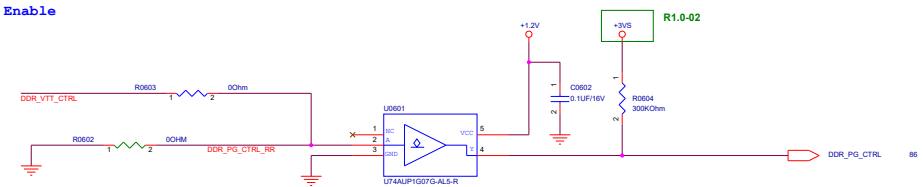
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

CFG[19:8] : Reserved Configuration Lanes

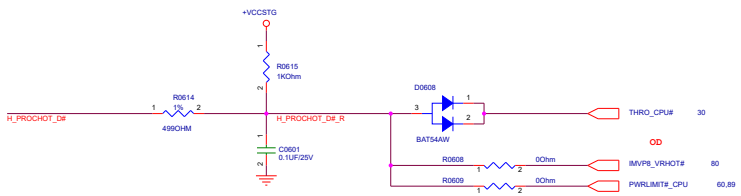
Reserved Configuration Lanes

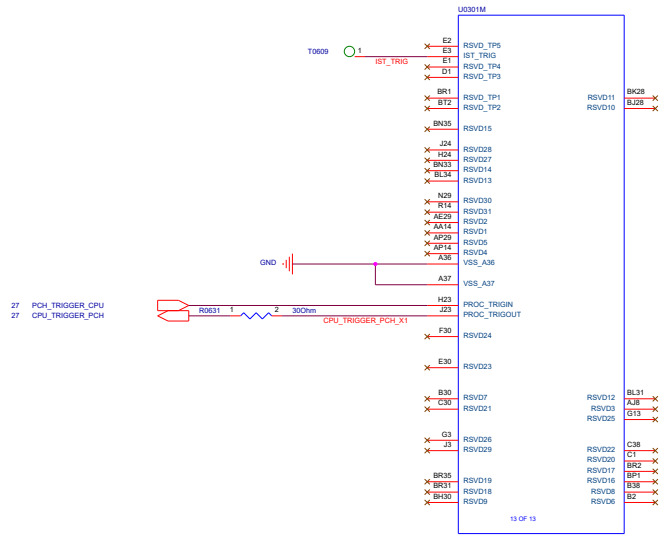
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116

VTT Enable



CPU SIDEBAND SIGNALS

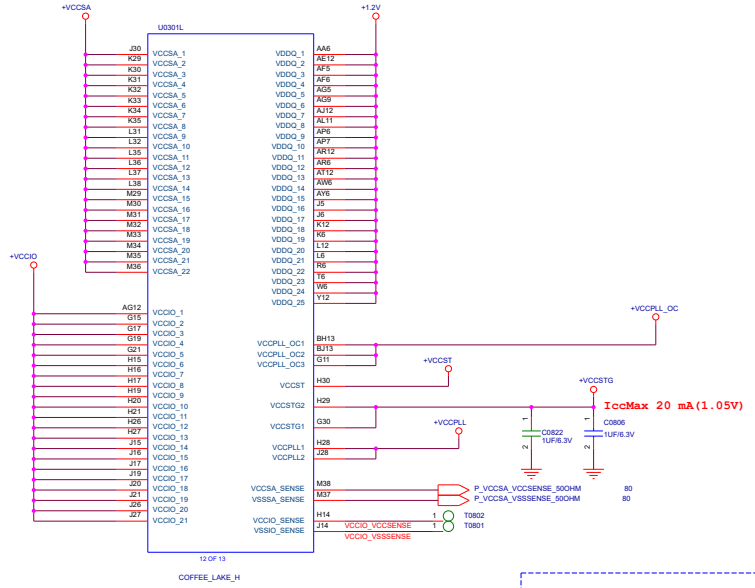




Project Name: GX701			Rev: 1.0
Title : CPU_CFG,RSVD			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 6 of 100		

CPU XDP

ASUS	Project Name: GX701	Rev: 1.0
Title : CPU XDP		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 06, 2019	Sheet 7 of 100	



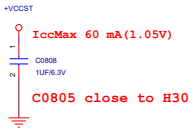
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	
		+VCCSTG	
	+1.2V	+VTT	
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO	+VCCSTG	

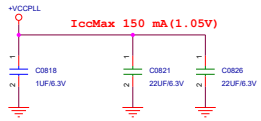
Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
VccST off in S3	On in S3	+25-30mW
VccPLL_OC off in S0/C10	On in S0/C10	+3-10mW
VccPLL_OC off in S0ix	On in S0ix	+3-10mW

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for gating off VccSTG, VccPLL_OC and VccIO (CFL-H) in the S0/C10 system state in order to save power.

+VCCST/+VCCPLL DECAPS Place Back Side (TOP)





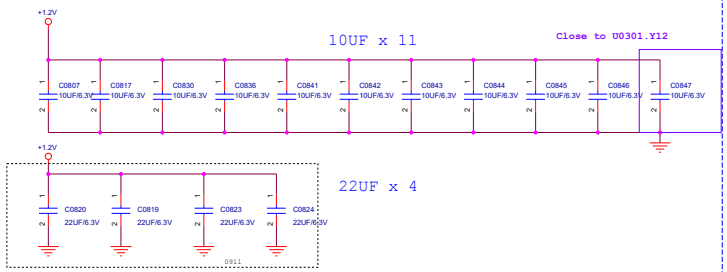
CFL U/H PDG Update for VCCPLL Power Rail Design Guidelines

Due to Display PLL lock issues observed on systems with high noise level on VCCPLL, CFL-H (BP#571391 and CFL-U (BP#571021 Platform design guidelines has been updated with new recommendation for VCCPLL power rail.

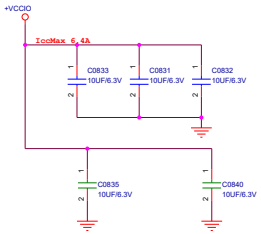
An additional capacitor 0805 size placeholder near CPU BGA ball is recommended for better power delivery, this should be stuffed when encountered a noisy VCCPLL power rail.

This new recommendation not required for systems that follows the PDG Power Integrity guidance and kept low noise level on VCCPLL.

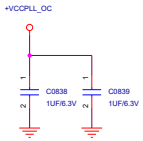
+VDDQ DECAPS Place Back Side (TOP)



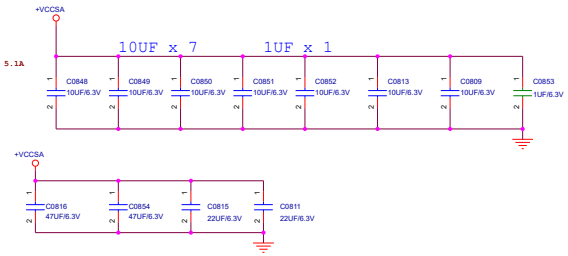
+VCCIO DECAPS Place Back Side (TOP)



+VCCPLL_OC DECAPS Place Back Side (TOP)

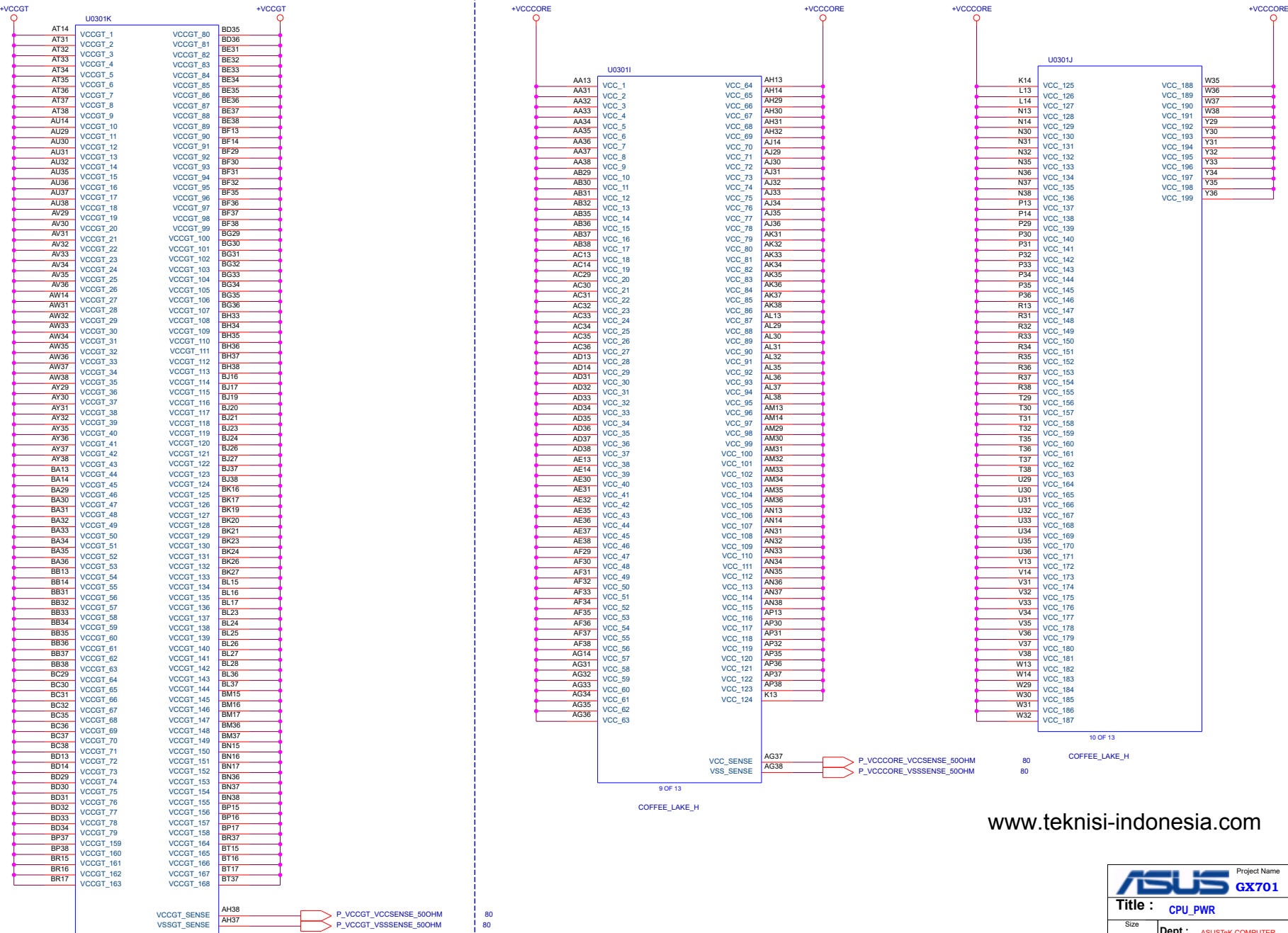


+VCCSA DECAPS Place Back Side (TOP)



+VCCSA near CPU

ASUS	Project Name: GX701		Rev: 1.0
Title : CPU_PWR			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 8 of 100		


Main Board
+VCCGT
+VCCGT
U0301K
VCCGT_1
VCCGT_2
VCCGT_3
VCCGT_4
VCCGT_5
VCCGT_6
VCCGT_7
VCCGT_8
VCCGT_9
VCCGT_10
VCCGT_11
VCCGT_12
VCCGT_13
VCCGT_14
VCCGT_15
VCCGT_16
VCCGT_17
VCCGT_18
VCCGT_19
VCCGT_20
VCCGT_21
VCCGT_22
VCCGT_23
VCCGT_24
VCCGT_25
VCCGT_26
VCCGT_27
VCCGT_28
VCCGT_29
VCCGT_30
VCCGT_31
VCCGT_32
VCCGT_33
VCCGT_34
VCCGT_35
VCCGT_36
VCCGT_37
VCCGT_38
VCCGT_39
VCCGT_40
VCCGT_41
VCCGT_42
VCCGT_43
VCCGT_44
VCCGT_45
VCCGT_46
VCCGT_47
VCCGT_48
VCCGT_49
VCCGT_50
VCCGT_51
VCCGT_52
VCCGT_53
VCCGT_54
VCCGT_55
VCCGT_56
VCCGT_57
VCCGT_58
VCCGT_59
VCCGT_60
VCCGT_61
VCCGT_62
VCCGT_63
VCCGT_64
VCCGT_65
VCCGT_66
VCCGT_67
VCCGT_68
VCCGT_69
VCCGT_70
VCCGT_71
VCCGT_72
VCCGT_73
VCCGT_74
VCCGT_75
VCCGT_76
VCCGT_77
VCCGT_78
VCCGT_79
VCCGT_159
VCCGT_160
VCCGT_161
VCCGT_162
VCCGT_163
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VCCGT_81
VCCGT_82
VCCGT_83
VCCGT_84
VCCGT_85
VCCGT_86
VCCGT_87
VCCGT_88
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VCCGT_94
VCCGT_95
VCCGT_96
VCCGT_97
VCCGT_98
VCCGT_99
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VCCGT_101
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VCCGT_134
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VCCGT_137
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VCCGT_141
VCCGT_142
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VCCGT_144
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VCCGT_147
VCCGT_148
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VCCGT_153
VCCGT_154
VCCGT_155
VCCGT_156
VCCGT_157
VCCGT_158
VCCGT_164
VCCGT_165
VCCGT_166
VCCGT_167
VCCGT_168
VCCGT_SENSE
VSSGT_SENSE
P_VCCGT_VCCSENSE_50OHM
P_VCCGT_VSSSENSE_50OHM
80
80
11 OF 13
COFFEE_LAKE_H
+VCCCORE
+VCCCORE
U0301I
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
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VCC_95
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VCC_97
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VCC_99
VCC_100
VCC_101
VCC_102
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VCC_112
VCC_113
VCC_114
VCC_115
VCC_116
VCC_117
VCC_118
VCC_119
VCC_120
VCC_121
VCC_122
VCC_123
VCC_124
VCC_SENSE
VSS_SENSE
P_VCCCORE_VCCSENSE_50OHM
P_VCCCORE_VSSSENSE_50OHM
80
80
9 OF 13
COFFEE_LAKE_H
+VCCCORE
+VCCCORE
U0301J
VCC_125
VCC_126
VCC_127
VCC_128
VCC_129
VCC_130
VCC_131
VCC_132
VCC_133
VCC_134
VCC_135
VCC_136
VCC_137
VCC_138
VCC_139
VCC_140
VCC_141
VCC_142
VCC_143
VCC_144
VCC_145
VCC_146
VCC_147
VCC_148
VCC_149
VCC_150
VCC_151
VCC_152
VCC_153
VCC_154
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VCC_172
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VCC_191
VCC_192
VCC_193
VCC_194
VCC_195
VCC_196
VCC_197
VCC_198
VCC_199
10 OF 13
COFFEE_LAKE_H
www.teknisi-indonesia.com
Project Name
GX701
Rev
1.0
Title :
CPU_PWR
Size
B
Dept.:
ASUSTeK COMPUTER
Engineer:
EE
Date:
Wednesday, March 06, 2019
Sheet
9
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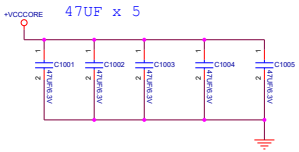
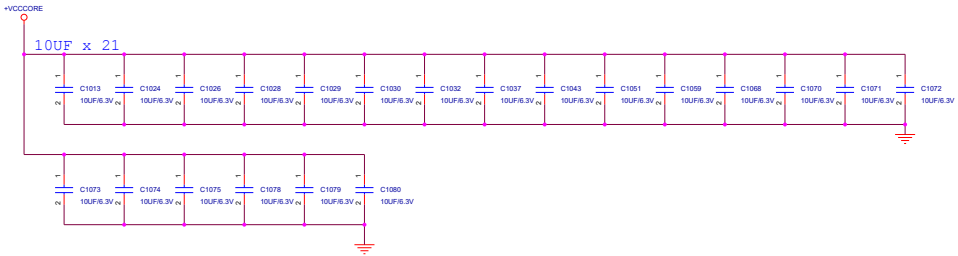
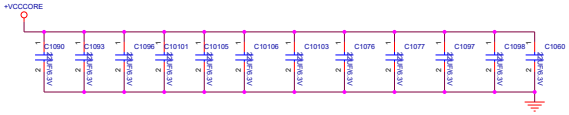
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	

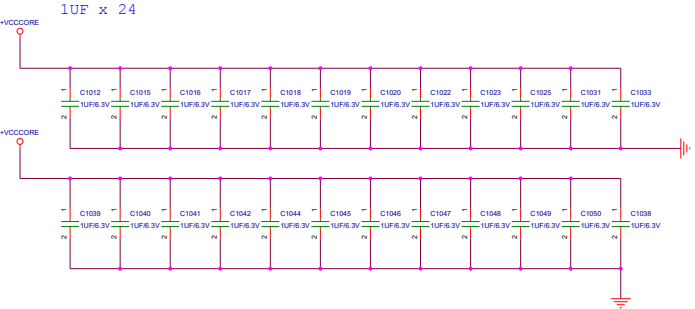
+VCCORE near CPU



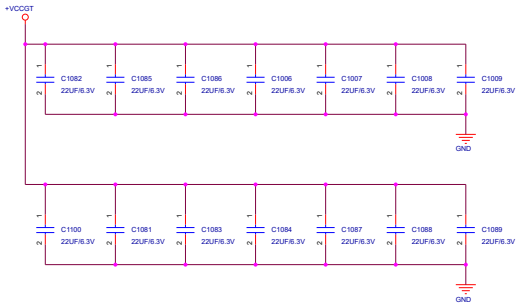
+VCCORE DECAPS Place Back Side (TOP)







+VCCGT cap near CPU **22uF x14**



ASUS	Project Name: GX701		Rev: 1.0
Title : 010_CPU_POWER_CAP			
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 10 of 100		

Project Name

GX701

Rev

R1.0

Title : TBT_Alpine-Ridge

Size	Dept.:	Engineer:
C	ASUSTeK COMPUTER INC.	EE

Date:	Sheet	of
Wednesday, March 06, 2019	11	100

	Project Name GX701GX	Rev R1.3

Title : CYPRESS CCG4

Size D	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Wednesday, March 06, 2019	Sheet 12 of 100	

<Variant Name>

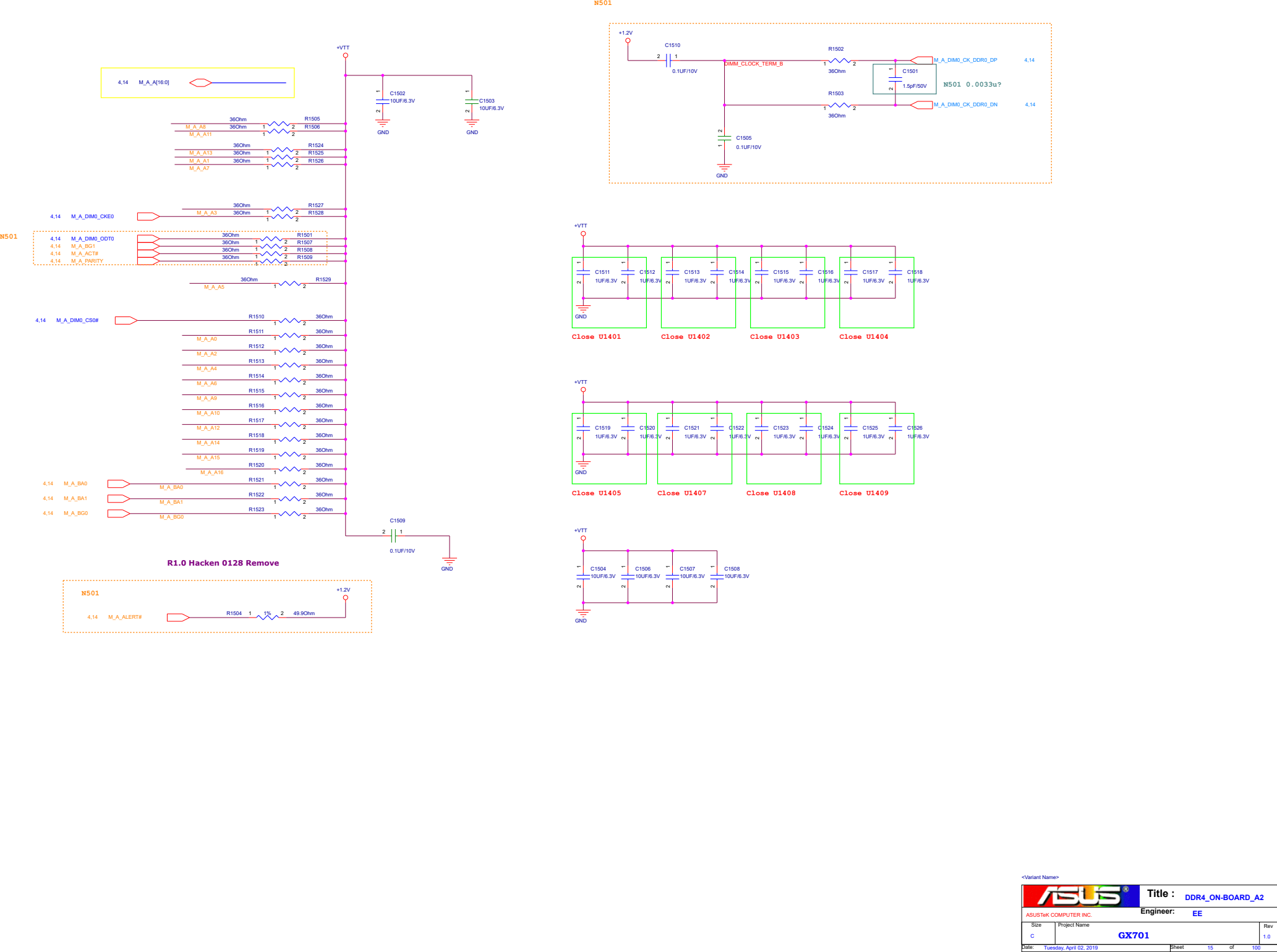
Title : DDR4_TERMINATION

ASUSTeK COMPUTER INC.

Engineer: EE

Size	Project Name	Rev
Custom	**GX701**	1.0

Date:	Wednesday, March 06, 2019	Sheet	13	of	100

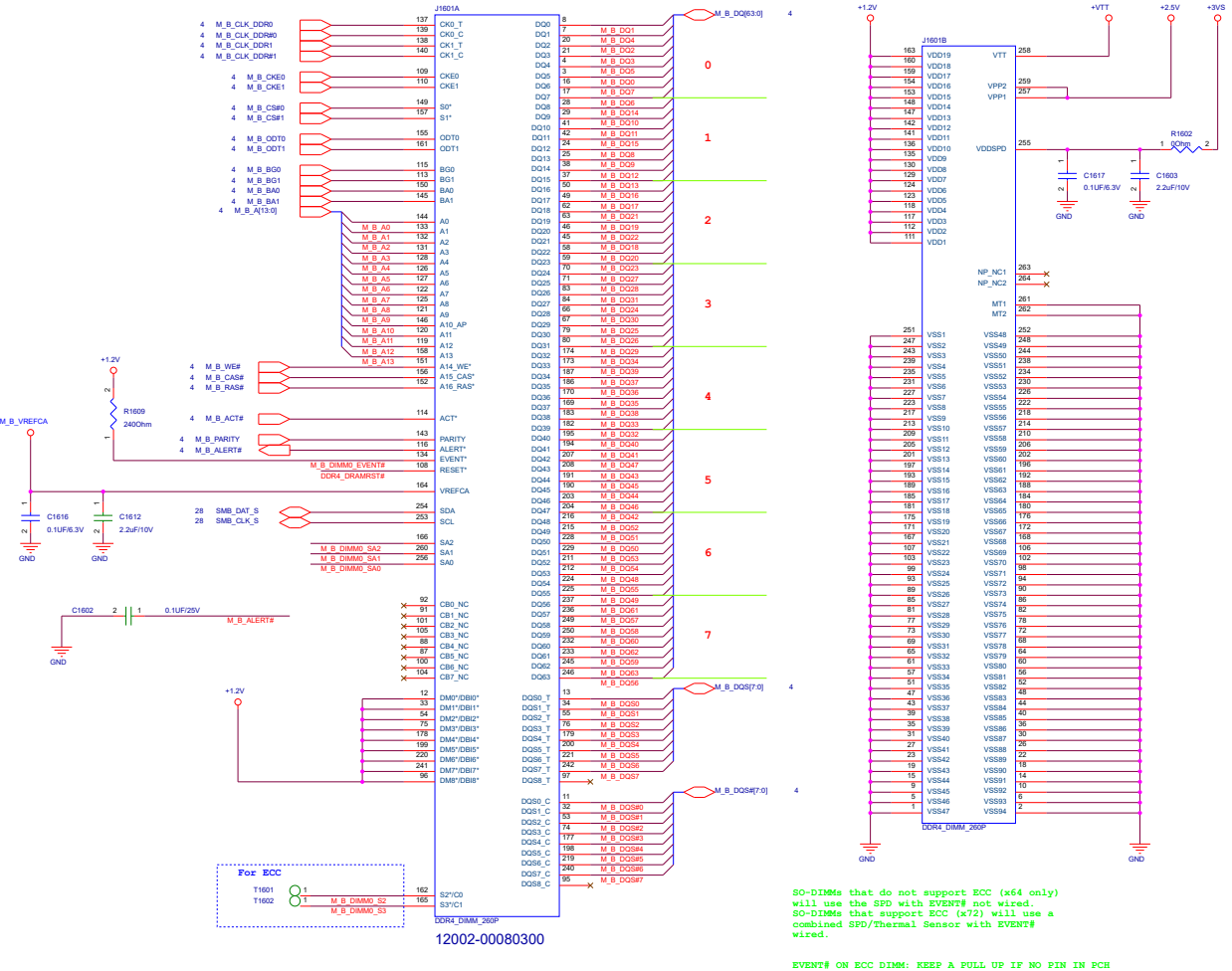


<Variant Name>

ASUSTeK COMPUTER INC.	Title : DDR4_ON-BOARD_A2	
	Engineer: EE	
Size: C	Project Name: GX701	Rev: 1.0
Date: Tuesday, April 02, 2019	Sheet 15 of 100	

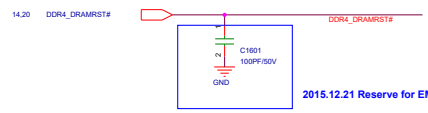
SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)

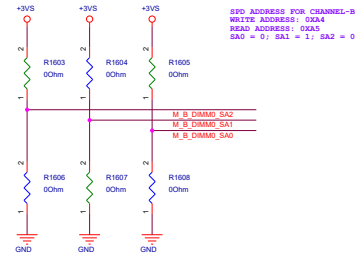
Main Board

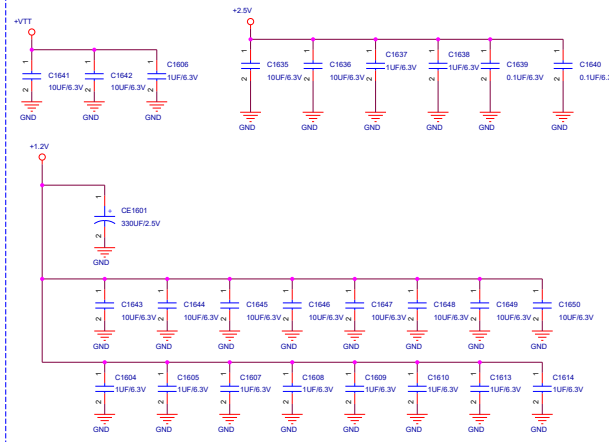


SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH







ASUS	Project Name: GX701		Rev: 1.0
Title :	DIM_DDR4 SO-DIMM B1		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 16 of 100		

<Variant Name>

Title : NB_****

ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size	Project Name	Rev
A	GX701	1.0

Date:	Wednesday, March 06, 2019	Sheet	17	of	100

Figure 4-23. CFL H DDR4 x16 Memory Down V_{REF-CA} Overview

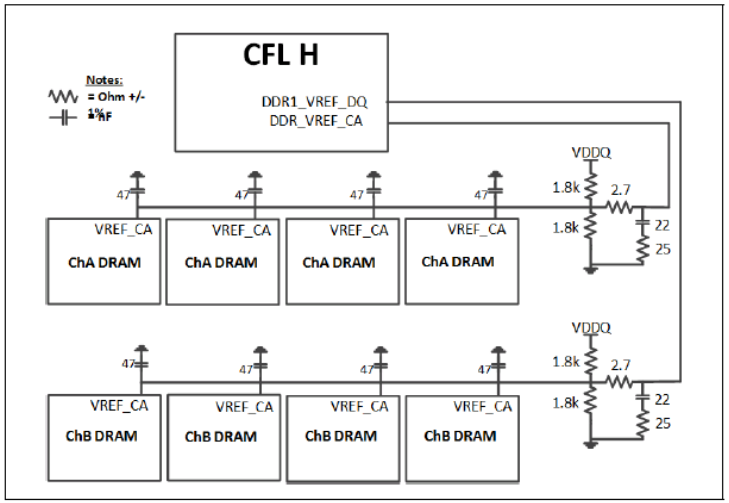
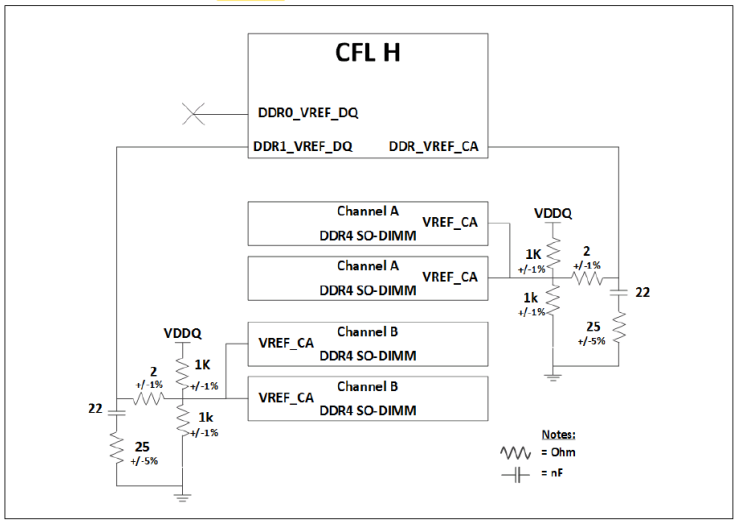
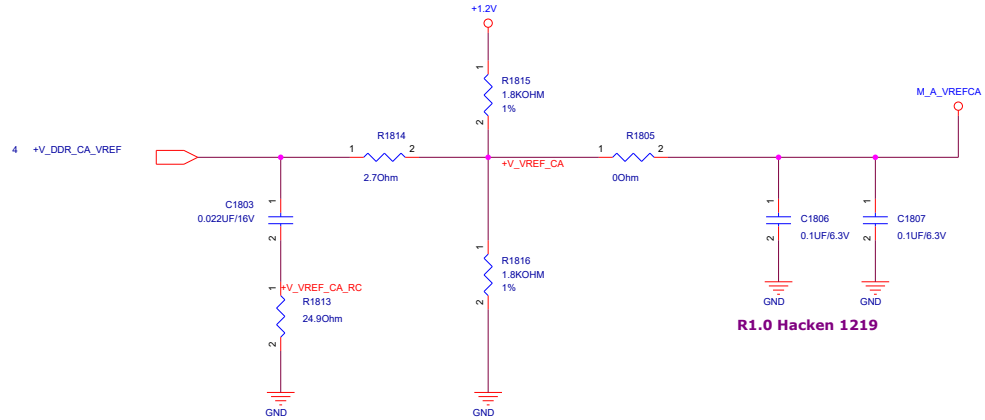


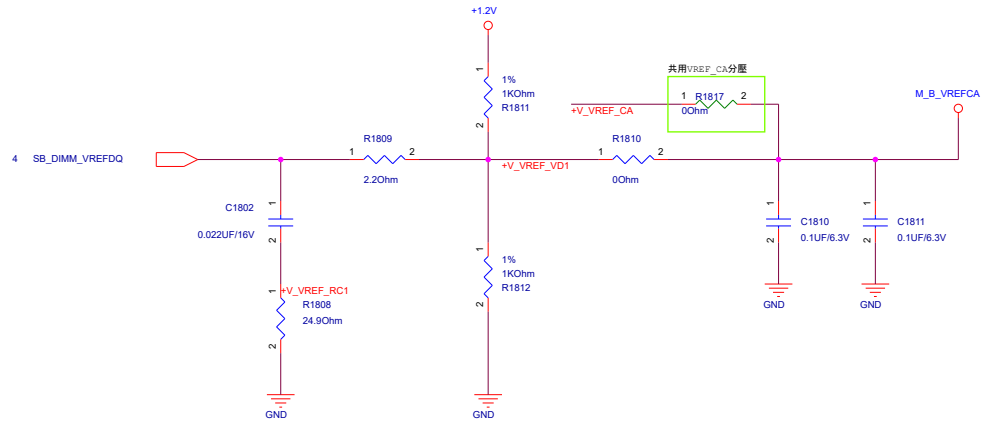
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview



Memory Down Vref



SO-DIMM1 Vref



ASUS	Project Name: GX701	Rev: 1.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Tuesday, April 02, 2019	Sheet 18 of 100	

Main Board

<Variant Name>

Title : *****

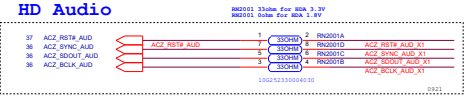
ASUSTeK COMPUTER INC. NB3

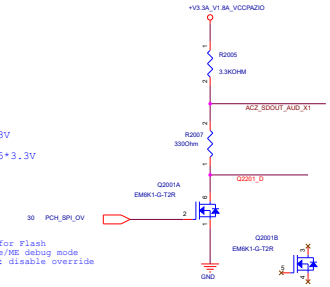
Engineer: EE

Size	Project Name	Rev
C	**GX701**	1.0

Date:	Wednesday, March 06, 2019	Sheet	19	of	100

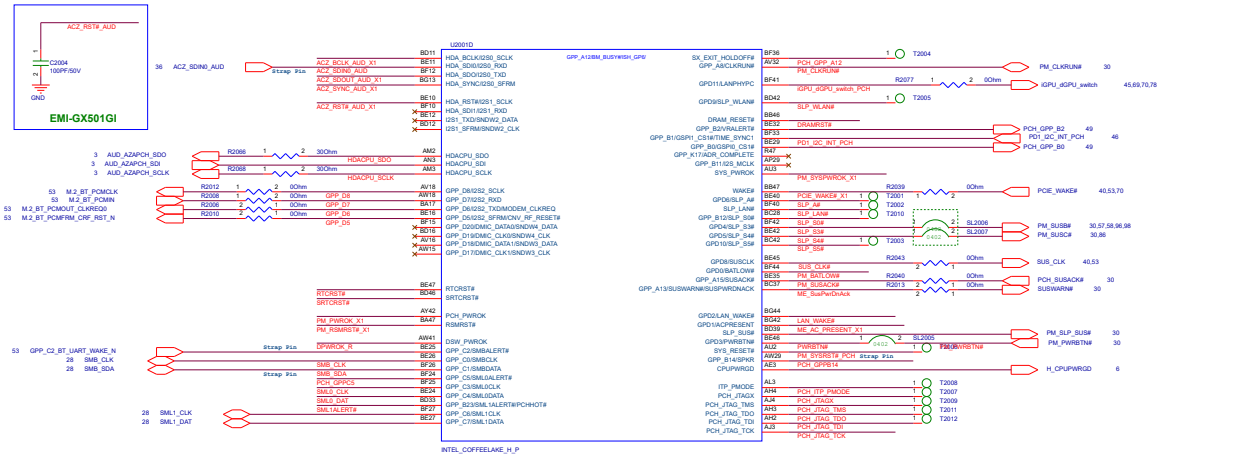
HD Audio





ACZ_SDOUT:
(1)PCH:
Internal PD 20k ohm,
VIL=0.35V,VIH=0.65~3.3V
(2)ALC269:
VIL<0.35*3.3V,VIH>0.65*3.3V

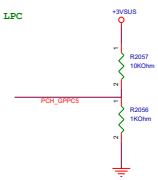
ACZ_SDOUT is a signal used for Flash Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override



Power failure solution (S0-->G3,S5-->G3):

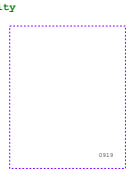
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.05VSUS	+VCCST		
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	+V3.3A_V1.8A_VCCPAZIO
		+3VS		

eSPI or LPC



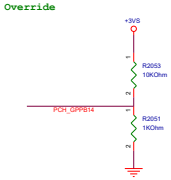
PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

TLS Confidentiality



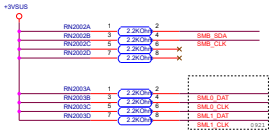
PU	Enable
PD	Disable (default)

Top Swap Override

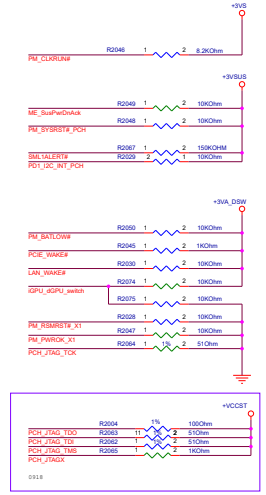


PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

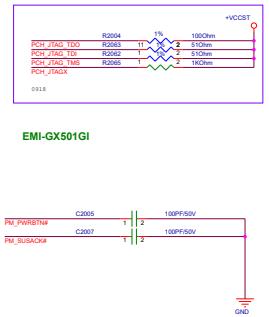
SMBUS

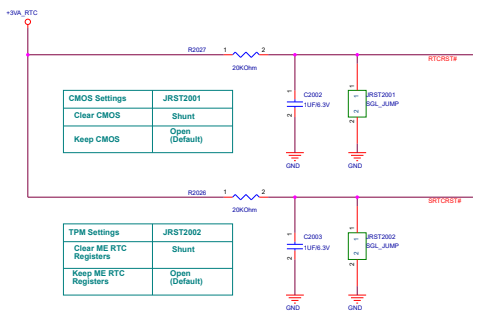


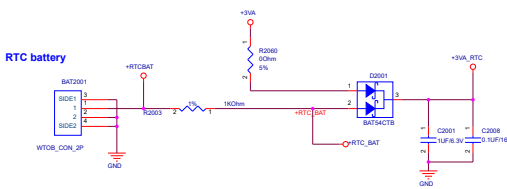
Main Board



EMI-GX501GI

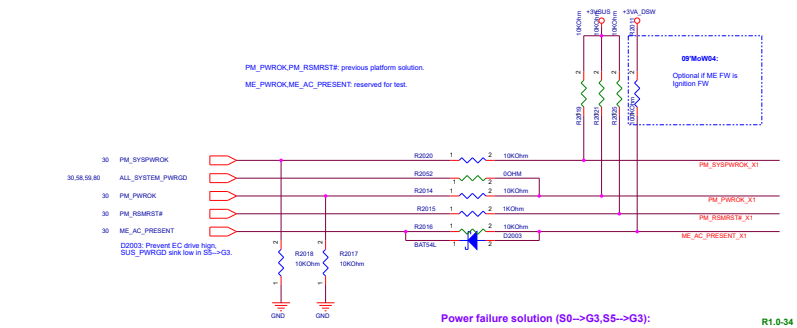






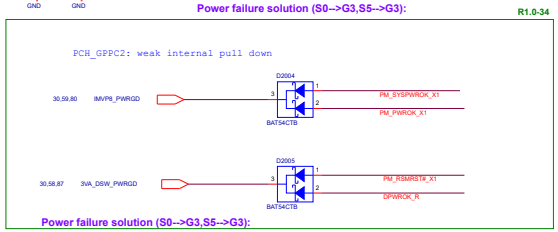
RTC battery

1st :12017-00020200
2nd :12017100002C
USE RTC Battery:
P/N: 0B100-00040500 BATT-LI CR1220 3V



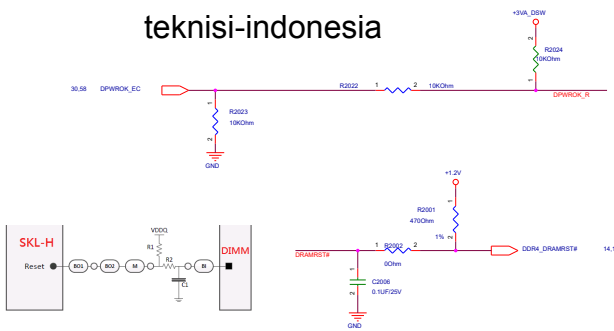
Power failure solution (S0-->G3,S5-->G3):

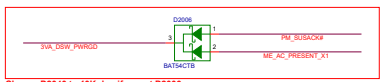
R1.0-34



Power failure solution (S0-->G3,S5-->G3):

teknisi-indonesia





R1.1-03

Change D2040 to 10Kohm if mount D2006

Deep SX discharge (S0-->DSX,S5-->DSX)

ASUS	Project Name: GX701		Rev: 1.0
Title :	PCH-CPT(1)SATA,IHDA,RTC,JTAG		
Size: Custom	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 20 of 100		

PCIE Setting

GX501GI PCIE/SATA Function define

CNL HM370

HSIO Capabilities	Function
PCIEG (From GPU)	
PCIE#01 - USB3.1#07	
PCIE#02 - USB3.1#08	
PCIE#03 - USB3.1#09	
PCIE#04 - USB3.1#10	
PCIE#05	
PCIE#06	
PCIE#07	
PCIE#08	
PCIE#09	PCIE*4 SSD
PCIE#10	
PCIE#11: SATA-0a	
PCIE#12: SATA-1a	
PCIE#13: SATA-0b	
PCIE#14: SATA-1b	
PCIE#15 / SATA#2	
PCIE#16 / SATA#3	WLAN
PCIE#17 / SATA#4	
PCIE#18 / SATA#5	
PCIE#19 / SATA#6	
PCIE#20 / SATA#6	
PCIE#21	TBT (x4)
PCIE#22	
PCIE#23	
PCIE#24	

	Function
CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	WLAN
CLKREQ-3	
CLKREQ-4	
CLKREQ-5	TBT AR
CLKREQ-6	PCIE SSD
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	

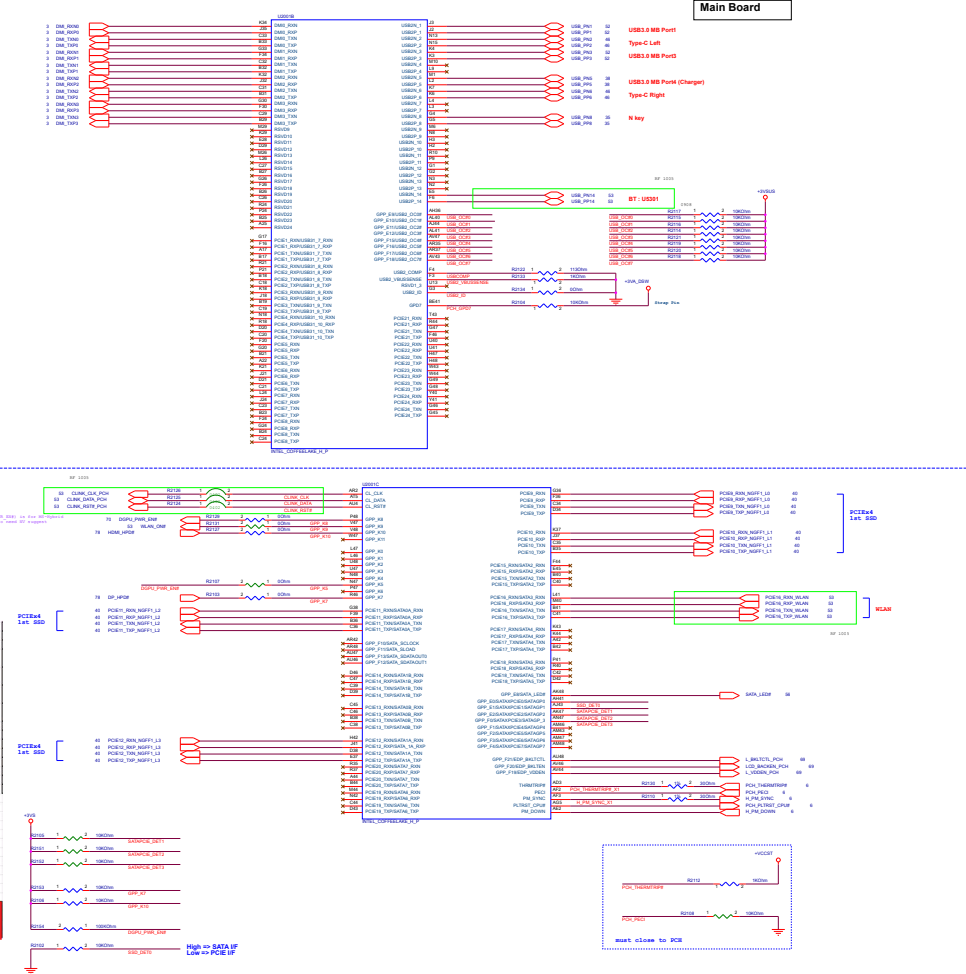
USB Setting GX501GI USB Function define CNL HM370

USB 2.0	Function
USB2_01	USB3.0 MB Port1
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4(Charger)
USB2_06	TBT
USB2_07	
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

USB 3.0	Function
USB3.1#01	USB3.1MB Port1 (Support Gen2)
USB3.1#02	USB3.0 MB Port2 (Support Gen2)
USB3.1#03	USB3.0 MB Port3 (Support Gen2)
USB3.1#04	USB3.0 MB Port4 (Support Gen2)
USB3.1#05	
USB3.1#06	
USB3.1#07	
USB3.1#08	

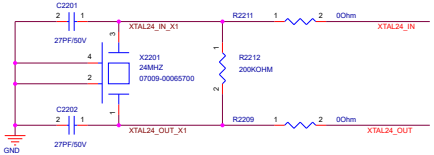
HSIO	HM370	QM370	CM246	IRST	Devices Assign
0	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1		(port1) USB3.1 Type-C
1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2		(port2) USB3.1 Type-C
2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3		(port1) USB3.0 Type-A USB3.1 Type-A
3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4		(port2) USB3.0 Type-A USB3.1 Type-A
4	USB3.1 Gen1 #5	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #5		(port3) USB3.0 Type-A USB3.1 Type-A only for QB370 / CM246
5	USB3.1 Gen1 #6	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #6		(port4) USB3.0 Type-A USB3.1 Type-A only for QB370 / CM246
6	USB3.1 Gen1 #7	USB3.1 Gen1 #7	USB3.1 Gen1 #7 PCIE #1		CR (USB3.0 / PCIE)
7	USB3.1 Gen1 #8	USB3.1 Gen1 #8	USB3.1 Gen1 #8 PCIE #2		
8	NA	USB3.1 Gen1 #9	USB3.1 Gen1 #9 PCIE #3		
9	NA	USB3.1 Gen1 #10	USB3.1 Gen1 #10 PCIE #4		
10	NA GbE	PCIE #5 GbE	PCIE #5 GbE	NO x4 x2	
11	NA	PCIE #6	PCIE #6	NO x4 x2	Thunderbolt (priority 1)
12	NA	PCIE #7	PCIE #7	NO x4 x2	
13	NA	PCIE #8	PCIE #8	NO x4 x2	
14	PCIE #9 GbE	PCIE #9 GbE	PCIE #9 GbE	x2	1st M.2 SSD (PCIE*2, optane)
15	PCIE #10	PCIE #10	PCIE #10	Yes x4 x2	(PCIE*4 / SATA#1a) (PCIE*4, optane)
16	PCIE #11 SATA #0a	PCIE #11 SATA #0a	PCIE #11 SATA #0a	x2	
17	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE	PCIE #12 SATA #1a GbE	x2	
18	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	PCIE #13 SATA #0b GbE	NO x4 x2	HDD (SATA#0b) (PCIE*4, optane)
19	PCIE #14 SATA #1b	PCIE #14 SATA #1b	PCIE #14 SATA #1b	NO x4 x2	ODD (SATA#1b)
20	PCIE #15	PCIE #15	PCIE #15 SATA #2	NO x4 x2	CLAN
21	PCIE #16	PCIE #16	PCIE #16 SATA #3	NO x4 x2	WLAN
22	PCIE #17 SATA #4	PCIE #17 SATA #4	PCIE #17 SATA #4	x2	2nd M.2 SSD (PCIE*2, optane)
23	PCIE #18 SATA #5	PCIE #18 SATA #5	PCIE #18 SATA #5	Yes x4 x2	(PCIE*4 / SATA#4) (PCIE*4, optane)
24	PCIE #19	PCIE #19	PCIE #19 SATA #6	x2	
25	PCIE #20	PCIE #20	PCIE #20 SATA #7	x2	
26	PCIE #21	PCIE #21	PCIE #21	x2	3rd M.2 SSD (PCIE*2, optane)
27	PCIE #22	PCIE #22	PCIE #22	Yes x4 x2	10G LAN (PCIE*4) optional
28	PCIE #23	PCIE #23	PCIE #23		Thunderbolt (priority 2)
29	PCIE #24	PCIE #24	PCIE #24		

Main Board

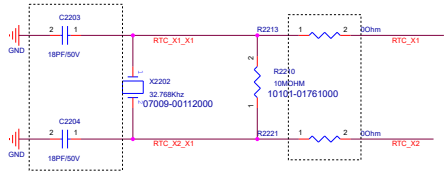


ASUS	Project Name: GX701		Rev: 1.0
Title :	PCH-CPT(2) PCIE,CLK,USB		
Size: D	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 21 of 100		

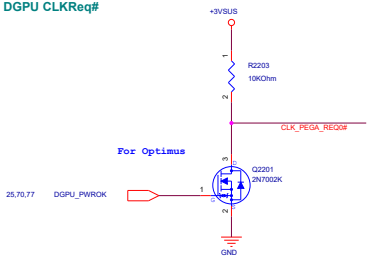
XTAL 24MHz



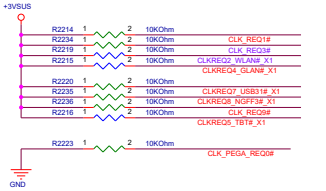
RTC CRYSTAL 32.768KHz

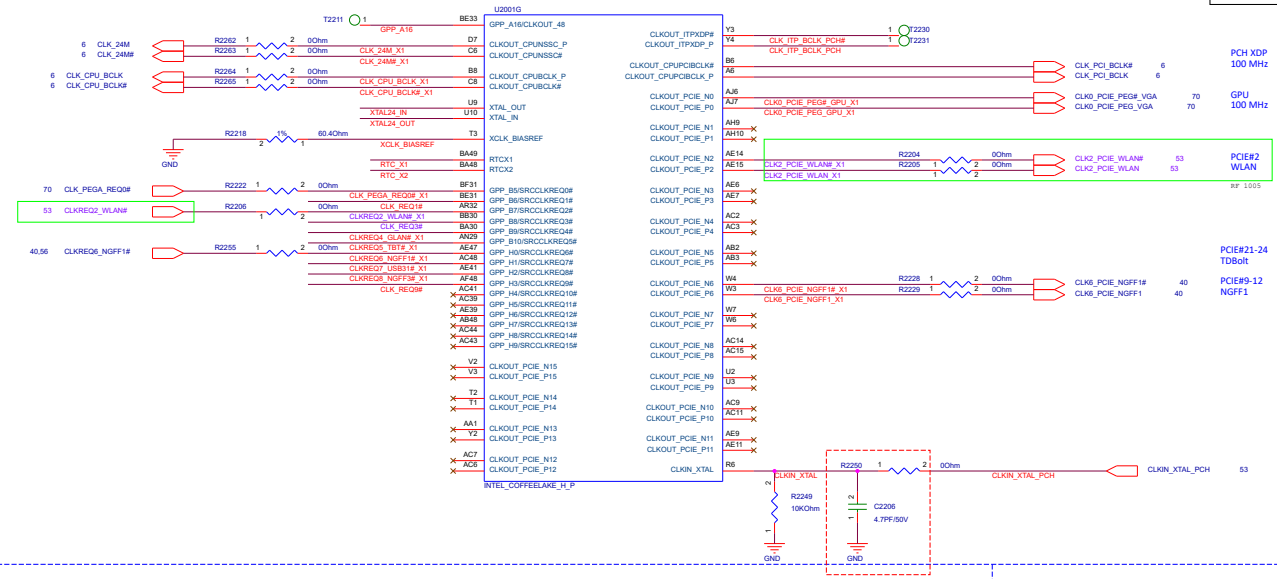


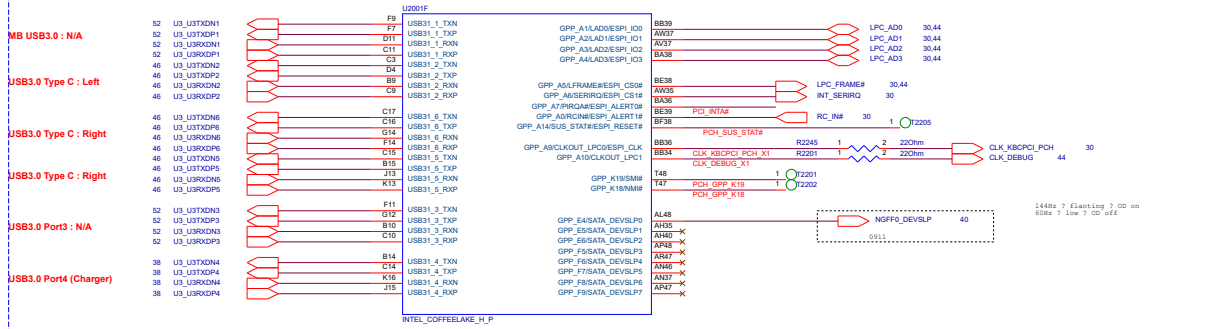
DGPU CLKReq#



PCH CLKREQ Setting:







Project Name	GX701
Rev	1.0
Title :	PCH-CPT(3)_FDI,DMI,SYS PWR
Size	Custom
Dept.:	ASUSTeK COMPUTER
Engineer:	EE
Date:	Tuesday, April 02, 2019
Sheet	22 of 100

HPD0 to DP

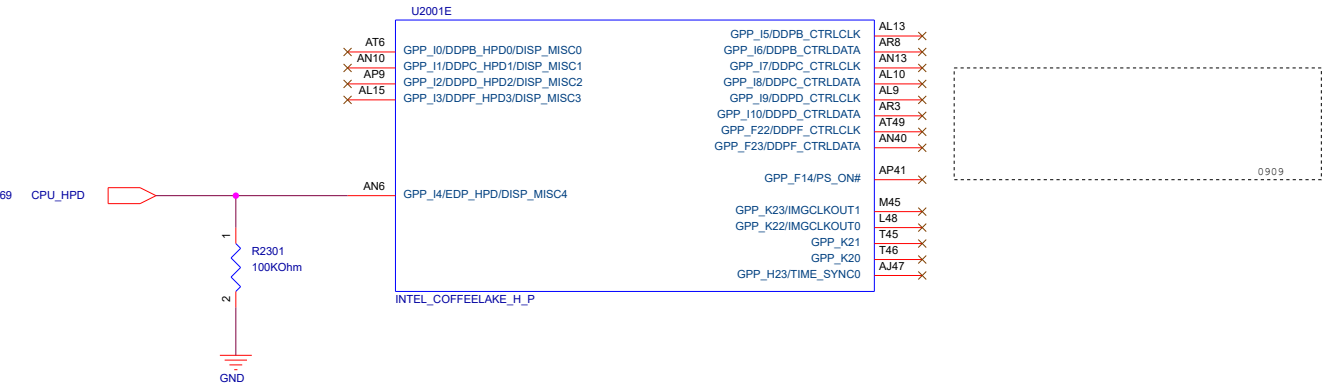
HPD1 to HDMI

HPD2 to TBT

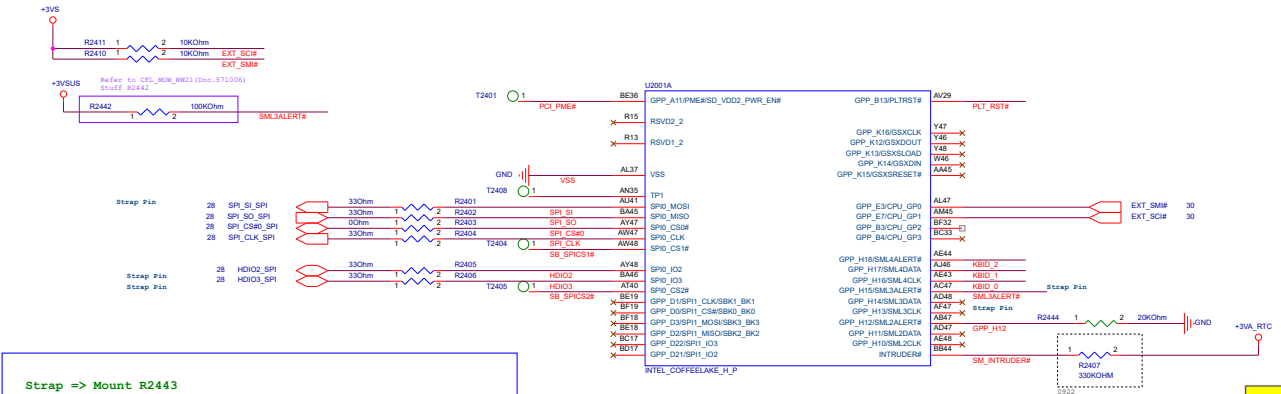
HPD3 to VGA

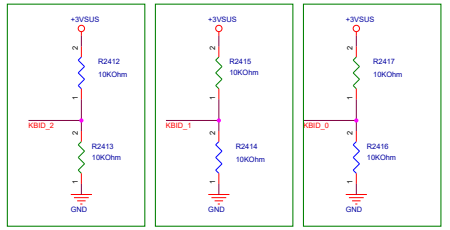
HPD4 to EDP Panel

DDP Strap Setting Update :
0 = Port is not detected (Default)
1 = Port is detected



ASUS	Project Name: GX701	Rev: 1.0
Title : PCH-CPT(4)_eDP,PCI,DP		
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 06, 2019	Sheet 23 of 100	

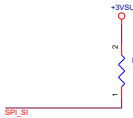




Keyboard ID : 0X03

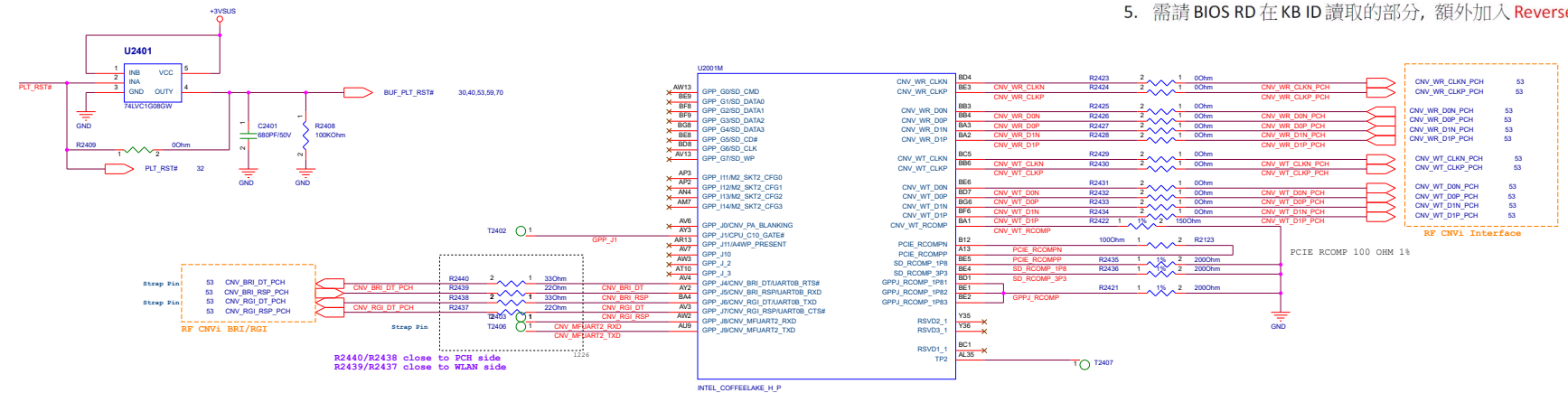
Strap => Mount R2443

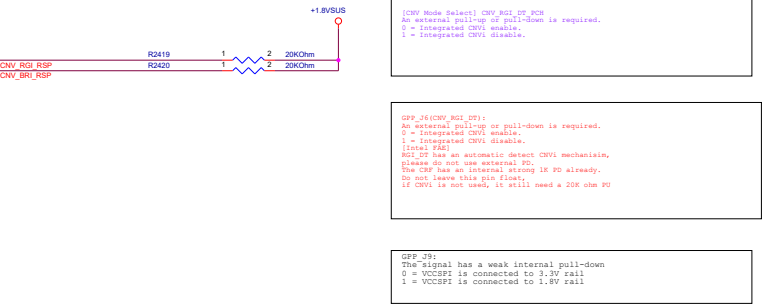
This strap should sample high,
if sample low will cause boot up fail.



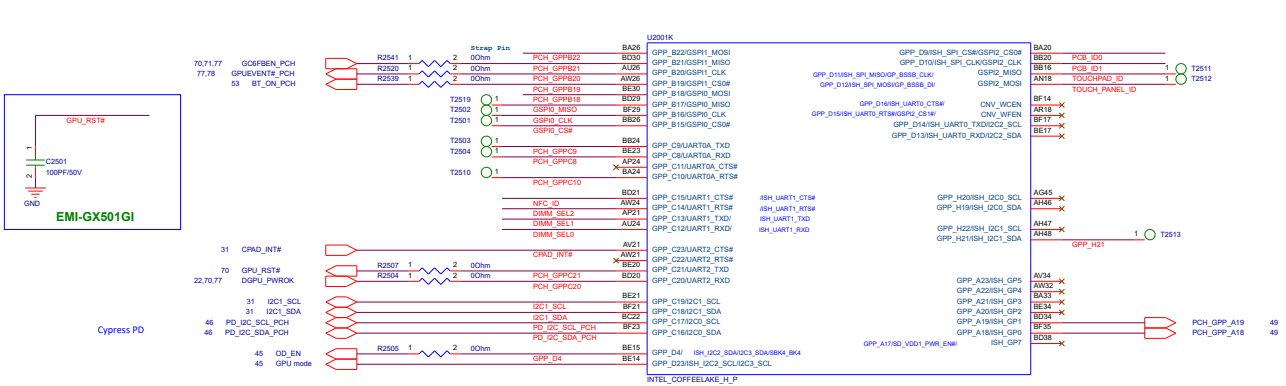
PCH Side (HW 請依照此表格做設計判斷)				
Code	ROG RGB KB Type	KBID 2 (GPP_H18)	KBID 1 (GPP_H17)	KBID 0 (GPP_H16)
0x00	Non-RGB	H	H	H
0x01	RGB per Region via QWER/WASD modes	H	H	L
0x02	RGB per Region via 4 zones	H	L	H
0x03	RGB per key	H	L	L

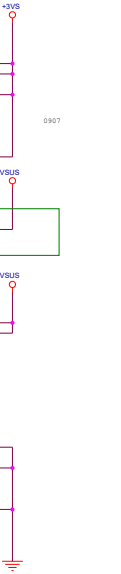
5. 需請 BIOS RD 在 KB ID 讀取的部分，額外加入 Reverse code，以符合第 1 點 table

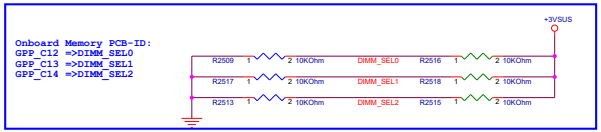




ASUS	Project Name: GX701		Rev: 1.0
Title :	PCH-CPT(5)_LPC,SPI,SMBUS		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 24 of 100		



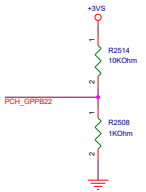




DDR4 Memory Down pool

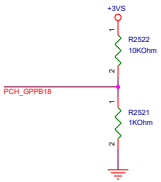
	Micron (1Rx8Gb) 03012-00030700 Micron_DDR4_2666 MT40A1G8SA-075:E	Samsung (1Rx16Gb) 03012-00060000 Samsung_DDR4_2666 K4AAG085WA-BCTD		
DIMM_SEL0	L	L		
DIMM_SEL1	L	L		
DIMM_SEL2	H	L		

Boot BIOS Strap Bit BBS



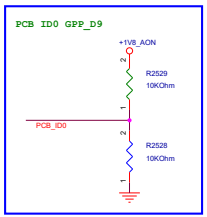
PCH_GPPB22: weal internal pull down	
PU	LPC
PD	SPI (Default)

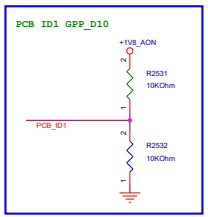
No Reboot

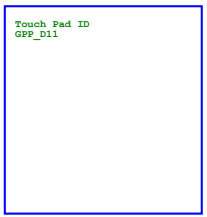


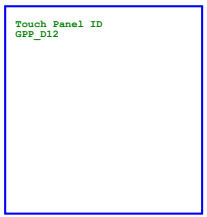
NOTE: Enable No Reboot
PCH will disable the TCO
Timer system reboot feature.
This function is useful when running ITP/XDP.

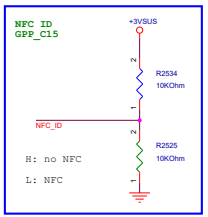
PCH_GPPB18: weak internal pull down	
PU	Enable
PD	Disable (Default)











X-tal Frequency Select

Cannon Lake PCH-LP

- XTAL_Freq_Select = GPP_H21
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

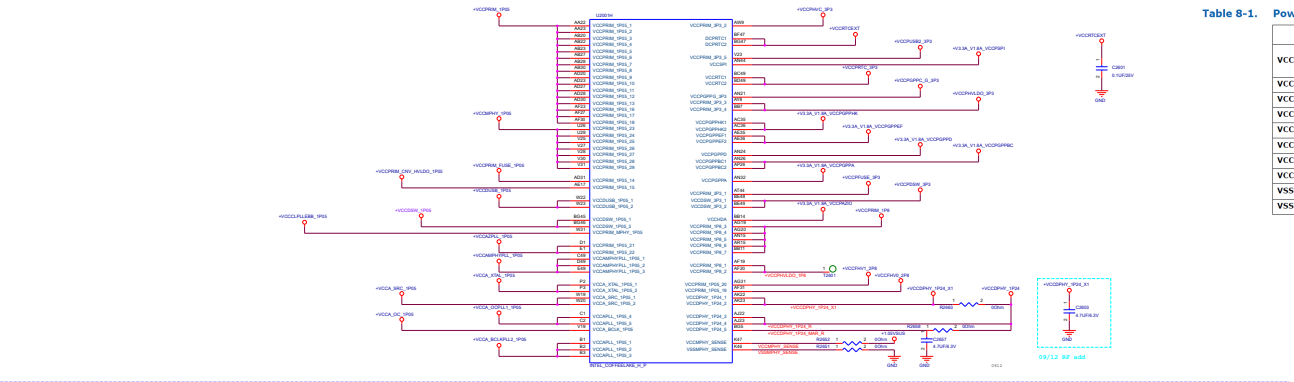
Cannon Lake PCH-H

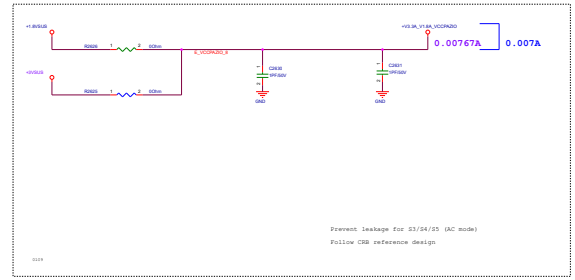
- XTAL_Freq_Select = GPP_J4
- Pin Strap for XTAL frequency selection
- An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

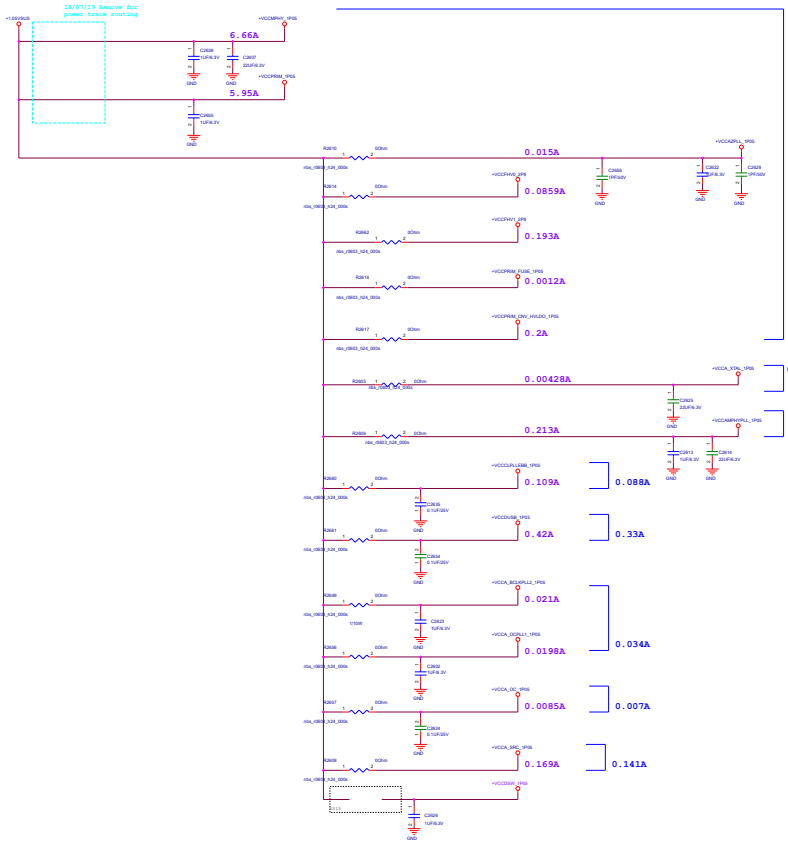
Project Name	GX701	Rev	1.0
Title :	PCH-CPT(6)_GPIO,MISC		
Size	Custom	Dept.:	ASUSTeK COMPUTER
Engineer:	EE		
Date:	Tuesday, April 02, 2019	Sheet	25 of 100

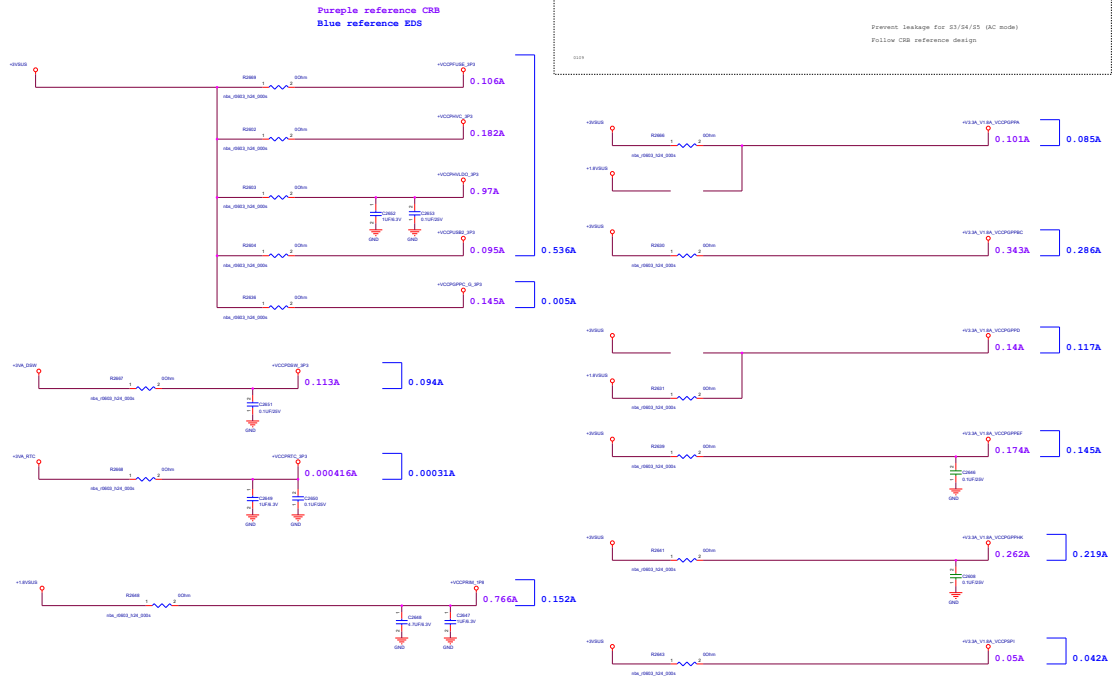
Table 8-1. Power Descriptions for PCH in CNL-H

Name	Description
VCCPHVLDO_1P8	**1.8V Primary Well.** On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	**1.8V or 3.3V for GPP_A group.**
VCCPGPPBC	**1.8V or 3.3V for GPP_B and GPP_C groups.**
VCCPGPPD	**1.8V or 3.3V for GPP_D group.**
VCCPGPPEF	**1.8V or 3.3V for GPP_E and GPP_F groups.**
VCCPGPPG_3P3	**3.3V for GPP_G group.**
VCCPGPPHK	**1.8V or 3.3V for GPP_H and GPP_K groups.**
VCCMPHY_SENSE	**1.05V Sense Line.**
VSSMPHY_SENSE	**0V (Ground) Sense Line.**
VSS	**Ground.**









ASUS	Project Name: GX701		Rev: 1.0
Title : PCH-CPT(7)_POWER,GND			
Size: D	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet: 26	of: 100	

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWANRN#	Native	ME_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	(N.C)			
GPP_A18	GPI	GPI	(N.C)			
GPP_A19	GPI	GPI	(N.C)			
GPP_A20	GPI	GPI	(N.C)			
GPP_A21	GPI	GPI	(N.C)			
GPP_A22	GPI	GPI	(N.C)			
GPP_A23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GPI	GPI	(N.C)			
GPP_B3	GPI	GPI	(N.C)			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_PEGA_REQ0#_X1		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN#_X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLKREQ4_GLAN#_X1		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_TBT#_X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MPHY_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	Native	GSPI0_CS#			
GPP_B16	GPI	Native	GSPI0_CLK			
GPP_B17	GPI	Native	GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/NV_GPU_EVENT#		PU 10K(@)	+3VSUS
GPP_B21	GPI	GPI	PCH_GPPB21/NV_GC6_FB_EN		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	GPO	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	Strap	PCH_GPPC2			
GPP_C3	SML0CLK	Native	SML0_CLK		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	PCH_GPPC8			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SEL0		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	GPO	AOAC_WLANLED		PU 10K(@)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(@)	+3VS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PD 10K(@)	
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PD 1K	
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	CIO_PLUG_EVENT		PU 10K	+VCC3V3_SX
GPP_D1	GPI	GPO	GPIO_3_FORCE_PWR		PD 10K	
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	(N.C)			
GPP_D6	GPI	GPI	(N.C)			
GPP_D7	GPI	GPO	WLAN_ON#			
GPP_D8	GPI	GPI	(N.C)			
GPP_D9	GPI	Strap	PCB_ID0		PD 10K	
GPP_D10	GPI	Strap	PCB_ID1		PD 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID			
GPP_D12	GPI	Strap	TOUCH_PANEL_ID			
GPP_D13	GPI	GPI	PCH_GPP_D13		PU 10K(@)	+3VSUS
GPP_D14	GPI	GPO	PCH_GPP_D14/WLAN_LED		PD 100K	
GPP_D15	GPI	GPO	PCH_GPP_D15/WLAN_BT_LED		PD 100K	
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	(N.C)			
GPP_D18	GPI	GPI	(N.C)			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	LED_Record			
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	SATAPCIE_DET0		PU 10K	+3VS
GPP_E1	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	GPI	SATAPCIE_DET2		PU 10K	+3VS
GPP_E3	GPI	GPI	(N.C)			
GPP_E4	GPI	Native	NGFF0_DEVSLP			
GPP_E5	GPI	Native	(N.C)			
GPP_E6	GPI	Native	NGFF2_DEVSLP			
GPP_E7	GPI	GPI	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K(@)	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	SATAPCIE_DET3		PU 10K	+3VS
GPP_F1	GPI	GPO	(N.C)			
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	(N.C)			
GPP_F6	GPI	Native	(N.C)			
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	Native	L_VDDEN_PCH_X1			
GPP_F20	GPI	Native	LCD_BACKEN_PCH_X1			
GPP_F21	GPI	Native	L_BKLTCTL_PCH_X1			
GPP_F22	GPI	GPI	(N.C)			
GPP_F23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)			
GPP_G1	GPI	GPO	SATA_ODD_PWRGT			
GPP_G2	GPI	GPI	SATA_ODD_DA#			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			
GPP_G8	FAN_PWM_0	Native	(N.C)			
GPP_G9	FAN_PWM_1	Native	(N.C)			
GPP_G10	FAN_PWM_2	Native	(N.C)			
GPP_G11	FAN_PWM_3	Native	(N.C)			
GPP_G12	GPI	GPI	(N.C)			
GPP_G13	GPI	GPI	(N.C)			
GPP_G14	GPI	GPI	(N.C)			
GPP_G15	GPI	GPI	(N.C)			
GPP_G16	GPI	GPI	(N.C)			
GPP_G17	GPI	GPI	(N.C)			
GPP_G18	GPI	GPI	PCH_GPP_G18			
GPP_G19	GPI	GPI	PCH_GPP_G19			
GPP_G20	GPI	GPI	(N.C)			
GPP_G21	GPI	GPI	(N.C)			
GPP_G22	GPI	GPI	(N.C)			
GPP_G23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ6_NGFF1#_X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLKREQ7_USB31#_X1		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H5	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H6	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H7	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H8	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H9	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	(N.C)			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPO	WLAN_WAKE_CTRL_CRB			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	Native	(N.C)		PD 100K	
GPP_I1	GPI	Native	(N.C)		PD 100K	
GPP_I2	GPI	GPI	(N.C)			
GPP_I3	GPI	Native	(N.C)			
GPP_I4	GPI	Native	GPP_I4		PD 100K	
GPP_I5	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I6	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I7	GPI	Native	(N.C)		PU 2.2K	+3VS
GPP_I8	GPO	Native	(N.C)	PD	PU 2.2K	+3VS
GPP_I9	GPI	Native	(N.C)		PU 2.2K(@)	+3VS
GPP_I10	GPO	Native	(N.C)	PD	PU 2.2K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUSB#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUSC#		PD 100K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	RSVD	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(@)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PWREN		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#	PU 10K (@)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (@)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN0_PWM		
GPA6	Alt	PWM	KB_LED_PWM		
GPA7	O	GPO	OS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	NKey_WRST	PD 10k	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (@)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K (@)	+3VSUS
GPC4	I	GPI	EC_GPC4/INTB#	PU 10K	+3VSUS
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT	PU 100K	+3VA_DSW
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN0_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	SUSWARN#_wCC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUSB#	PD 100K	
GPE6	OD	GPO	CAP_LED#		
GPE7	OD	GPO	THRO_CPU#	PU 10K(@)	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PWRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCE#/EC_SCE#_PCH		
GPG4	GPI		EC_SI/EC_SI_PCH		
GPG5	GPI		EC_SO/EC_SO_PCH		
GPG6	O	GPO	USB30_5VBUS		
GPG7	GPI		EC_SCK_PCH	PD 10K (@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K(@)	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#		
GPI1	I	GPI	3VSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PD 0	+3VACC
GPI7	Alt	AD	MB_MAX_POWER	PU 100K & PD 56K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB31_5VBUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	KB_WAKE#	PU 100K	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
on board memory CHA		
SO-DIMM B(0)	A4h	
EC Master (SMB1)	**SM-Bus Address**	
SM-Bus Device		
VGA Thermal Sensor	96h	
CPU Thermal Sensor	90h	
Power Thermal Sensor	7Eh	

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

GX501VIPCIE & USB Function define

Kabylake HM175

HSIO	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3.0 MB Port1(Charger)	
02	USB3#02 / SSIC#01	USB3.0 Port2	
03	USB3#03 / SSIC#02	USB3.0 Port3	
04	USB3#04	USB3.0 Port4	
05	USB3#05		
06	USB3#06		
07	USB3#07 / PCIE#01	CardReader_USB3(RSV)	
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE		
11	PCIE#05 / GBE	Thunderbolt	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	SATA*1 SSD port0	SRC6
16	PCIE#10 / SATA#1	PCIE*4 SSD	
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3		
23			
24			
25			
26			

USB 2.0	Function
USB2_01	USB3.0 MB Port1(Charger)
USB2_02	USB3.0 MB Port2
USB2_03	USB3.0 MB Port3
USB2_04	Camera
USB2_05	USB3.0 MB Port4
USB2_06	
USB2_07	Card Reader
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

SKL PCH-H Z170 HSIO

#	Lane			x2	x4	Function
1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7	PCIE #1		x 2	x 4	NA
8	USB3 #8	PCIE #2				
9	USB3 #9	PCIE #3		x 2		
10	USB3 #10	PCIE #4	GbE			
11	PCIE #5		GbE	x 2	x 4	NA
12	PCIE #6					
13	PCIE #7			x 2		
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23	PCIE #17	SATA #4		x 2	x 4	Intel IRST PCIE Storage Device #3
24	PCIE #18	SATA #5				
25	PCIE #19	SATA #6		x 2		
26	PCIE #20	SATA #7				

SKL PCH-H H170 HSIO

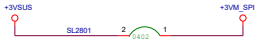
#	Lane			x2	x4	Function
1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7					
8	USB3 #8					
9	PCIE #3			x 2	NA	NA
10	PCIE #4		GbE			
11	PCIE #5		GbE	x 2	x 4	NA
12	PCIE #6					
13	PCIE #7			x 2		
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23	SATA #4			NA	NA	NA
24	SATA #5					
25	PCIE #19			x 2		
26	PCIE #20					

SKL PCH-H HM170 HSIO

#	Lane			x2	x4	Function
1	USB3 #1 (OTG)					
2	USB3 #2	SSIC #1				
3	USB3 #3	SSIC #2				
4	USB3 #4					
5	USB3 #5					
6	USB3 #6					
7	USB3 #7	PCIE #1		x 2	x 4	NA
8	USB3 #8	PCIE #2				
9	PCIE #3			x 2		
10	PCIE #4		GbE			
11	PCIE #5		GbE	x 2	x 4	NA
12	PCIE #6					
13	PCIE #7			x 2		
14	PCIE #8					
15	PCIE #9	SATA #0	GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1				
17	PCIE #11			x 2		
18	PCIE #12		GbE			
19	PCIE #13	SATA #0*	GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*				
21	PCIE #15	SATA #2		x 2		
22	PCIE #16	SATA #3				
23				NA	NA	NA
24						
25				NA		
26						

ASUS	Project Name: GX701	Rev: 1.0
Title :	PCH-CPT(8)_POWER,GND	
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 06, 2019	Sheet 27 of 100	

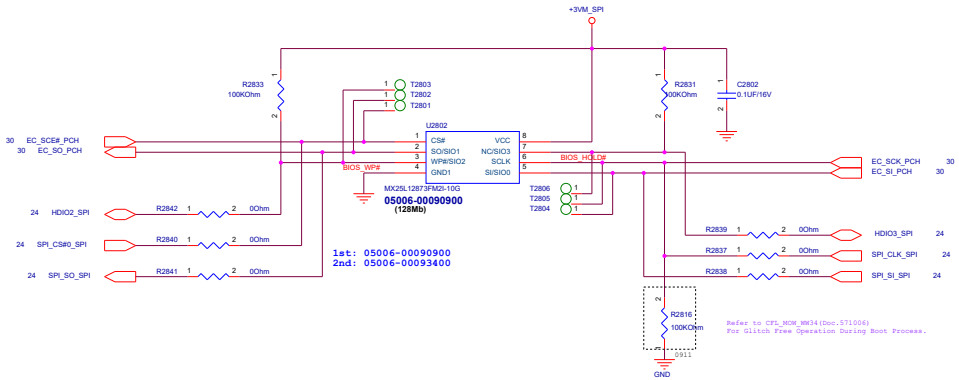
SPI Power



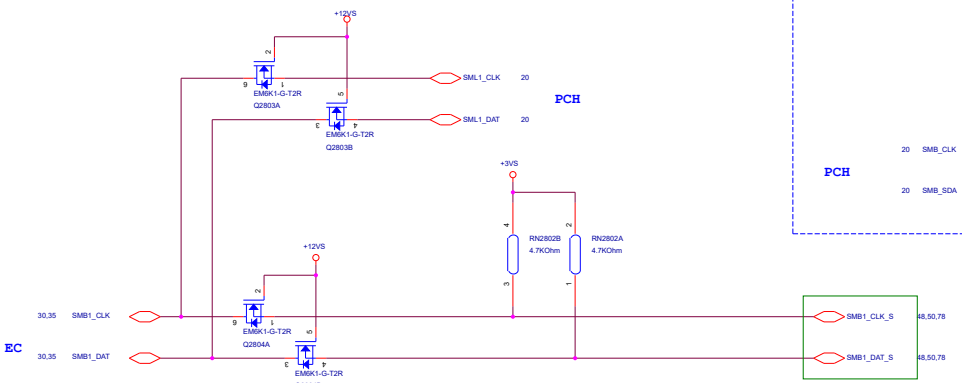
1st SPI ROM

1st: 05006-00090900 FLASH MXIC MX25L12873FM2I-10G 128M SOP-8L
2nd: 05006-00093100 FLASH GD25B127DSIGG IGADEVICE 128MB SOP8

Main Board

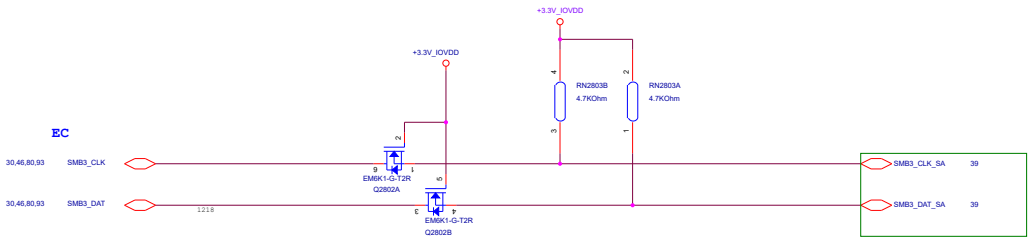


System Management Interface



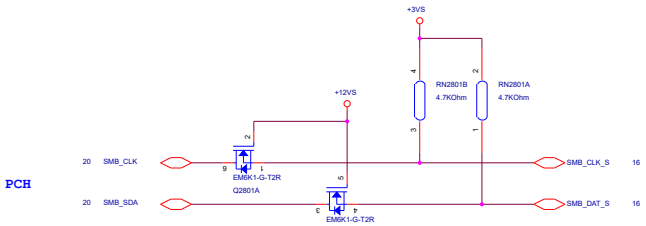
R0.1-13 R1.0-01

CPU,VGA Thermal Sensor
Power Thermal Sensor



GX501VI R1,1 for smart amp

SMBus Interface



ASUS	Project Name: GX701		Rev: 1.0
Title : PCH-SPI ROM,OTH			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 28 of 100		

ASUS	Project Name: GX701	Rev: 1.0
Title : PCH-XDP		
Size: A	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Wednesday, March 06, 2019	Sheet 29 of 100	

EC 8995

Only 3V Torlence

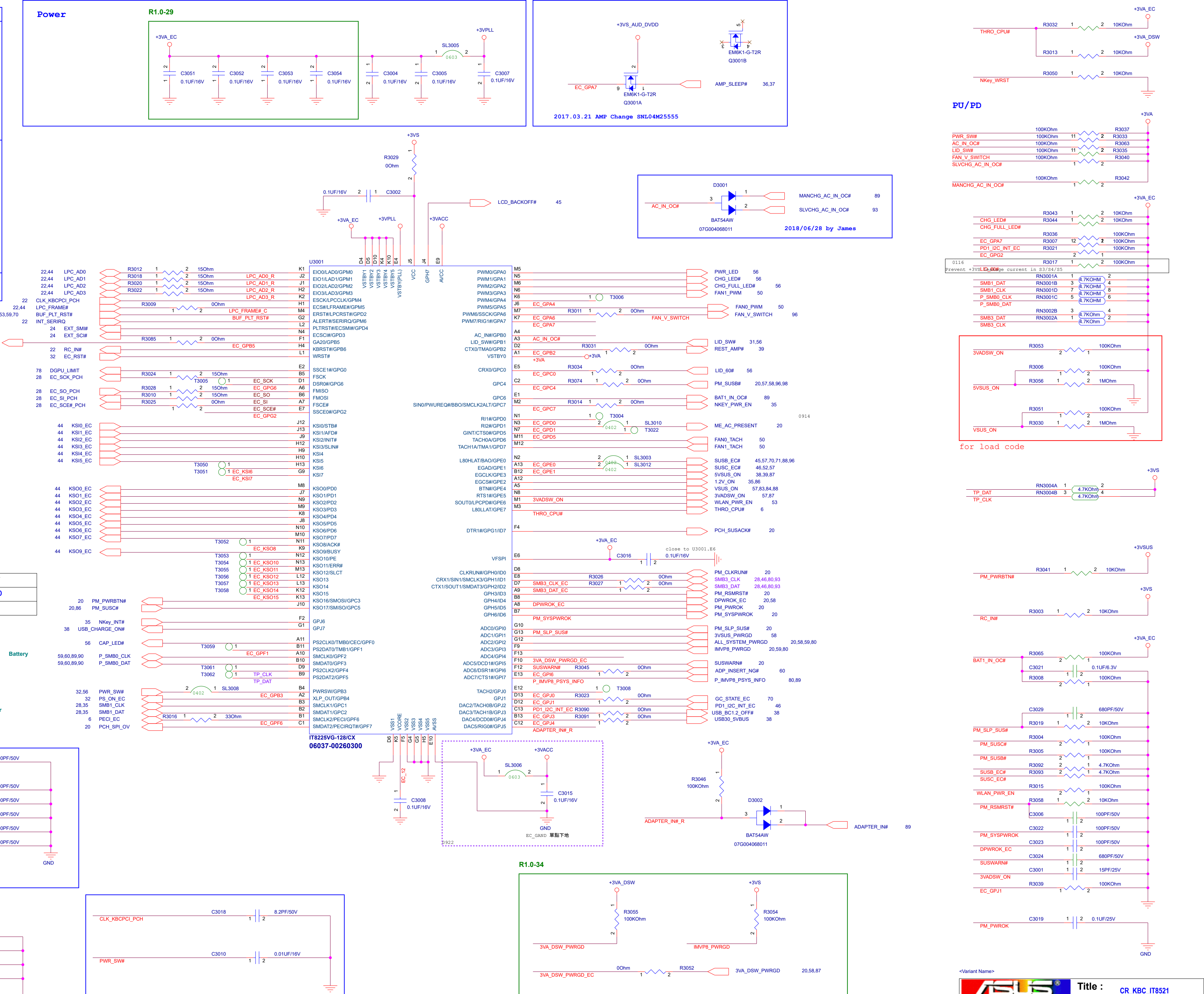
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

ITE Version	ASUS P/N
IT8225VG/BX	06037-00260000



ASUSTeK COMPUTER

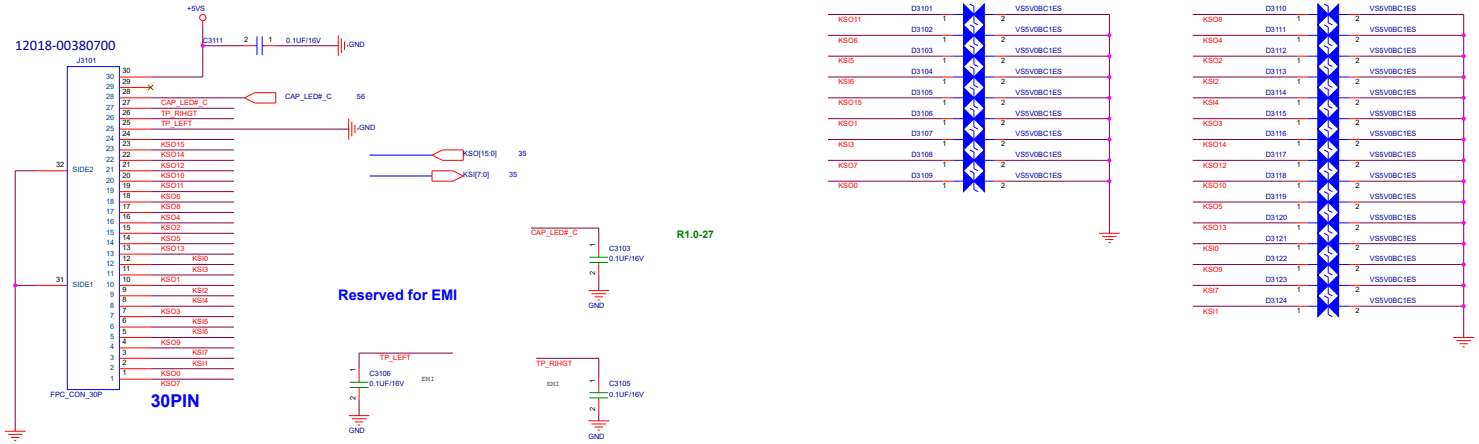
Title : CR_KBC_IT8521

Engineer: EE

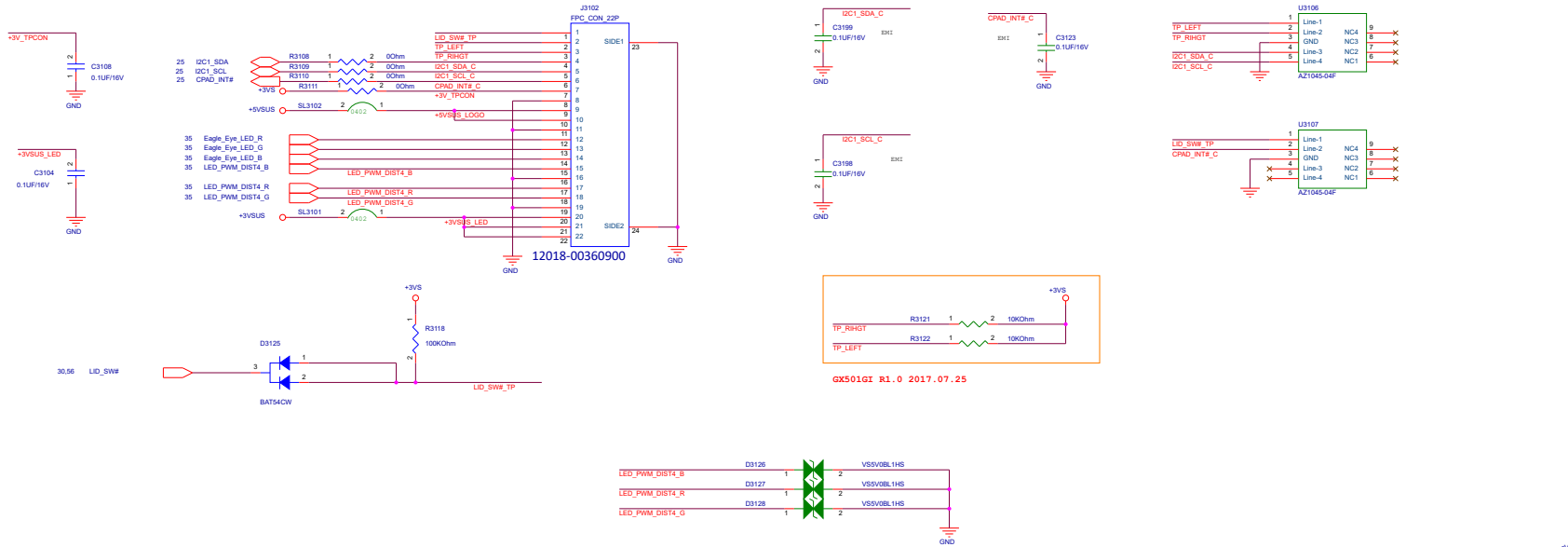
Size C | Project Name GX701 | Rev 1.0

Date: Tuesday, April 02, 2019 | Sheet 30 of 100

Keyboard Connector

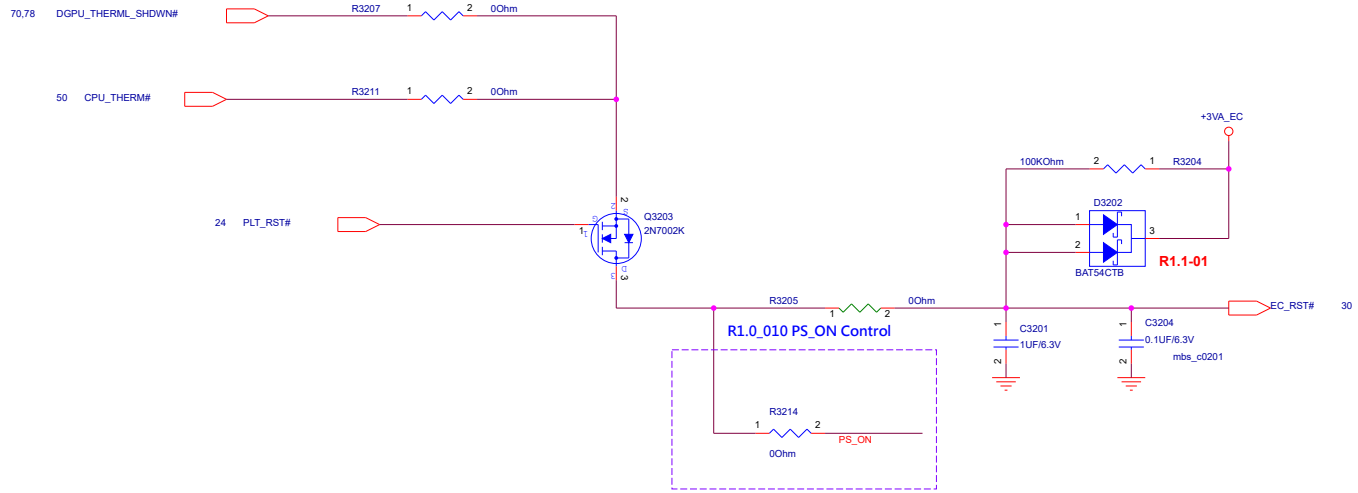


Touch Pad / Ten Keys Connector

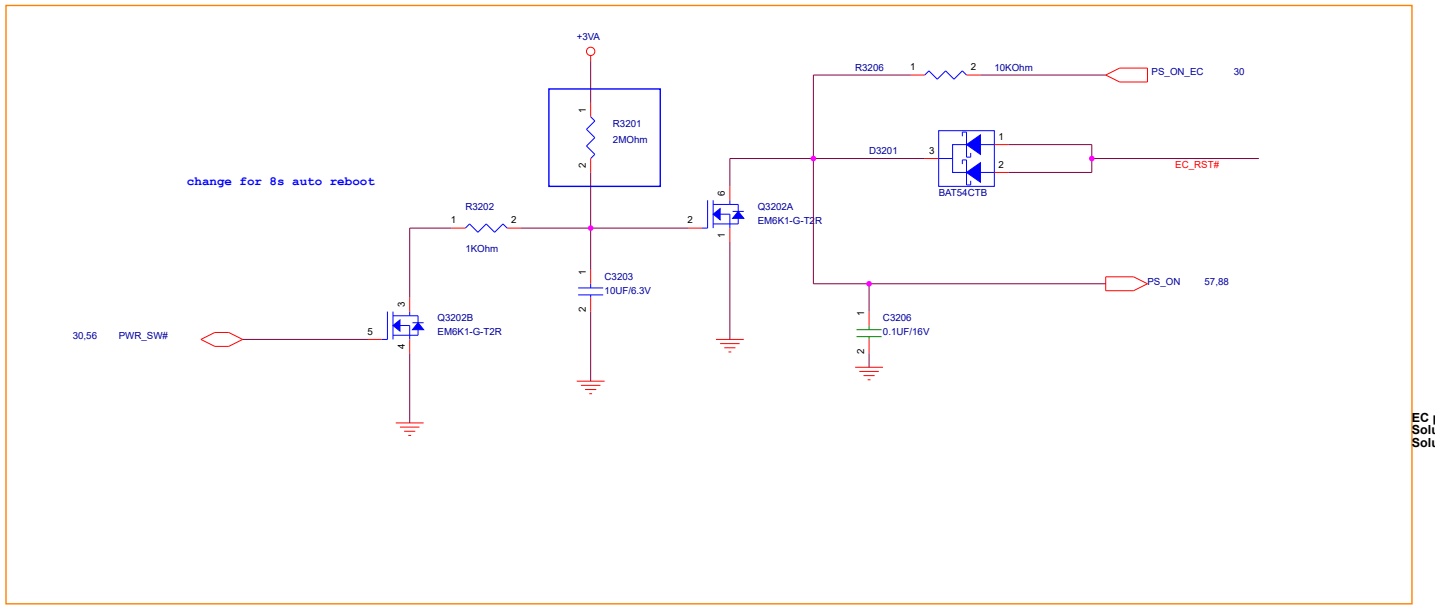


Reset Circuit

Pull up +3VSG through R7507(10kOhm=>100kOhm)
When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in parelle.
The CPU temperature point is protected ahead of time.
Increasing R7507 value can reduce to affect R5006.



Battery embedded (press pwr_sw 10sec, then reset ec)



EC power off solution:
Solution1 Mount R3206, D3201/ Unmount R3216
Solution2 Mount R3206/R3216/ Unmount D3201- for reserved 0402 footprint

R1.2-65
<Variant Name>

ASUSTeK COMPUTER	Title : RST_Reset Circuit	
	Engineer: EE	
Size: B	Project Name: GX701	Rev: 1.0
Date: Tuesday, April 02, 2019	Sheet 32 of 100	

Project Name

GX701

Rev

1.0

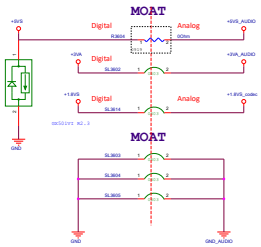
Title : LAN RTL8111GUX-CG

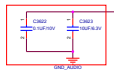
Size	Dept.:	Engineer:
B	ASUSTeK COMPUTER INC. NB1	EE

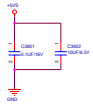
Date:	Sheet	of
Wednesday, March 06, 2019	33	100

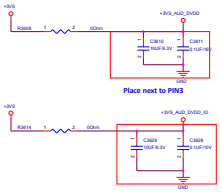
Main Board

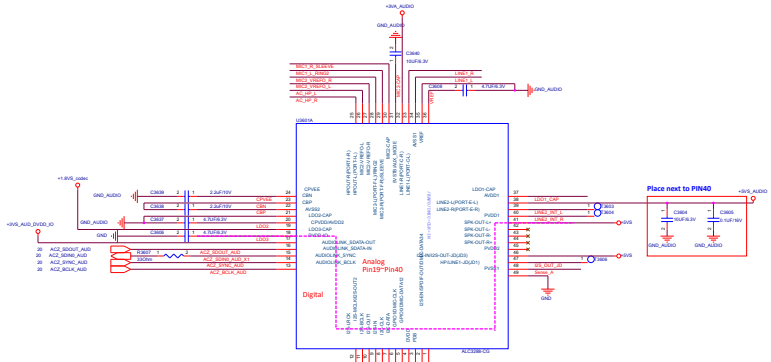
ASUS	Project Name: GX701	Rev: 1.0
Title : LAN RJ45 Conn.		
Size: B	Dept.: ASUSTeK COMPUTER INC. (I	Engineer: EE
Date: Wednesday, March 06, 2019	Sheet 34 of 100	

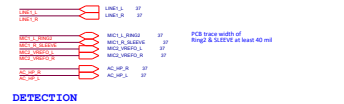


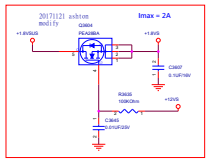


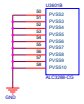


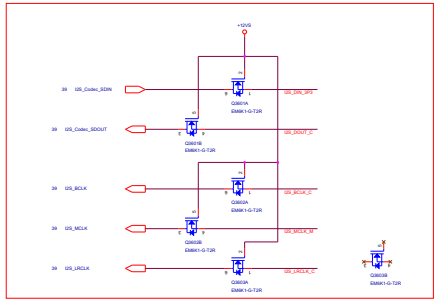


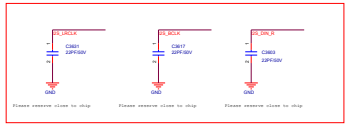




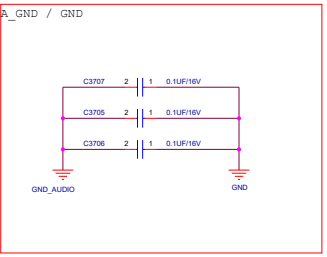


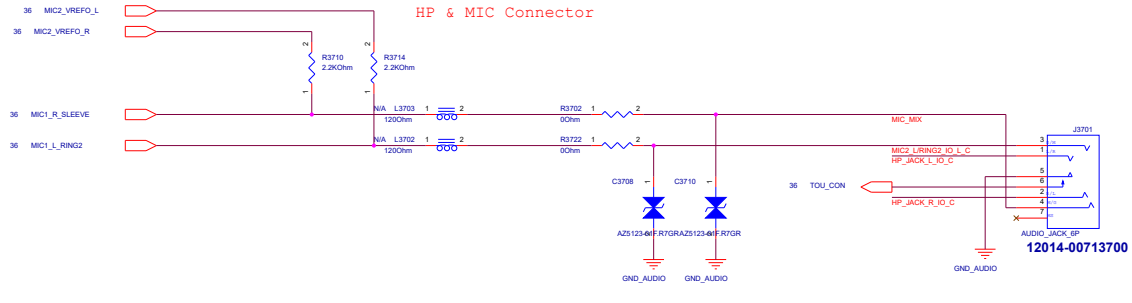




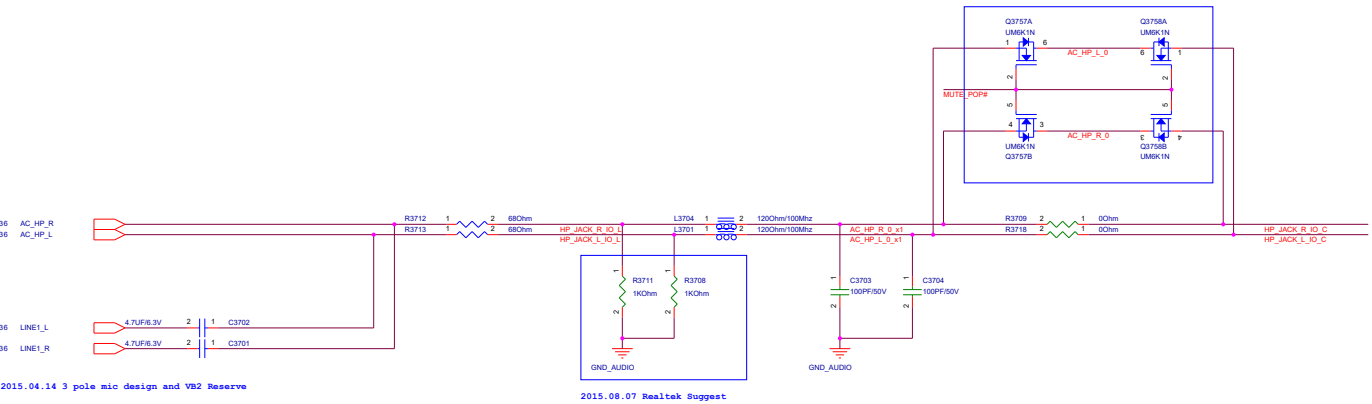


ASUS	Project Name: GX701		Rev: 1.0
Title :	AUDIO ALC3236-CG/VB2		
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet: 26	of: 100	



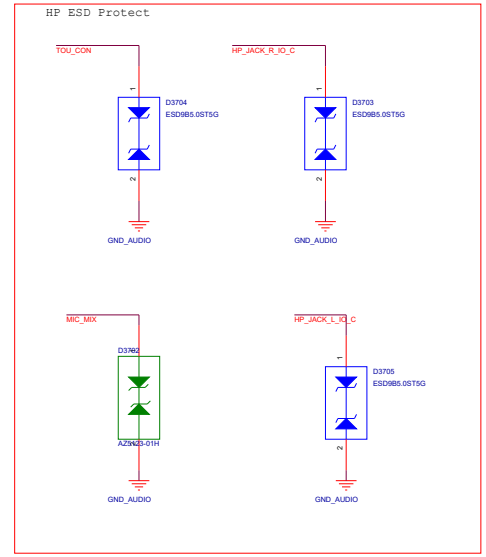


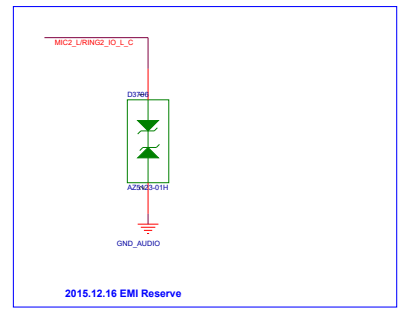
2016.09.06 Add DEPOP solution



2015.04.14 3 pole mic design and VB2 Reserve

2015.08.07 Realtek Suggest





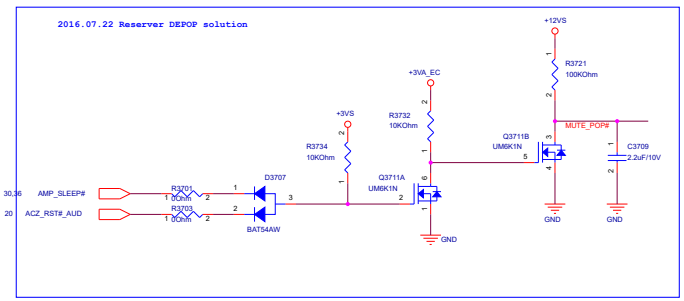
2015.12.16 EMI Reserve

MUTE CONTROL

2017.03.23 AMP Change Remove

MUTE CONTROL new solution for 1.8V HDA BUG 0318

2016.07.22 Reserver DEPOP solution



Project Name: GX701			Rev: 1.0
Title : AUDIO ALC3236-CG/VB2 Jack			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 37 of 100		

Pericom : 06113-00210000 REDRIVER IC PI3EQX1002BZLEX

Imax = 0.167A

+3VS_USB3_4

< Fine tune table for Pericom (One port Gen2) >

06113-00210100

< EQ table for Pericom 1002B >

EQ[A:B]	Gen 1 @2.5GHz(dB)	Gen 2 @5GHz(dB)
0 : 0 Ω to GND	5.1	10.9
R : Rest to GND	1.9	6.7
F : Leave Open	3.5(Default)	8.9(Default)
1 : 0 Ω to VDD	6.8	13.1

Note : With internal 100Kohm pull-up Rup and 200Kohm pull-down Rdown.
Rest = 68Kohm

< Channel / Receiver setting for Pericom 1002B >

Setting	Channel Enable [EN]	Receiver Detection [RXDET_EN]
0 : 0 Ω to GND	Disable	Disable
1 : 0 Ω to VDD	Enable(Default)	Enable(Default)
Note	Channel Enable / Receiver detection With internal 300K pull-up R.	

< FG table for Pericom 1002B >

FG[A:B]	Flat Gain (dB)
0 : 0 Ω to GND	-3.0
R : Rest to GND	-1.5
F : Leave Open	0 (Default)
1 : 0 Ω to VDD	+2.0

< SW table for Pericom 1002B >

SW[A:B]	Output Linear Swing (mV)
0 : 0 Ω to GND	800
R : Rest to GND	1200
F : Leave Open	1000 (Default)
1 : 0 Ω to VDD	1100

USB3.0_PORT4 (Support USB Charge Circuit)

J3809 USB3.0 Connector

1st Source: P/N:12013-00018300 FOXCONN/UEA1111-N40AM2-7H

2nd Source: P/N:12013-00080400 SINGATRON/2UB4006-310101F

USB3.0 Port 4

12013-00051900

06016-00810000

1st Source: P/N:06016-00510000 TPS2544RTER.

2nd Source: P/N:06016-00510000 TPS2546RTER

USB3.0 Pin define	
1	VBUS
2	D-
3	D+
4	GND
5	RX-
6	RX+
7	GND
8	TX-
9	TX+

USB Charge Circuit (For PORT 4)

EC_GPJ3

BC1.2 Charger Disable

Chief River Platform : Mount R5208

HSW, BDW Platform : Unmount R5208

CHG_CTL		TI 2544 / TI2546 [1]	[2]	[3]	
USB_CHARGER_ON#	0	0	1	1	AUTO
	1	1	1	1	CDP
USB_CHARGE_DISABLE	0	1	1	0	SDP

USB3.0_PORT4

Current Limit

TI2544 / TI2546 Mount RS314(10kohm), RS316(20kohm), RS315(10kohm)

USB3.0 ESD-Protection

1st : 07G028076030
ESD PROTECTION AZ1045-04F

2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

07024-00200200

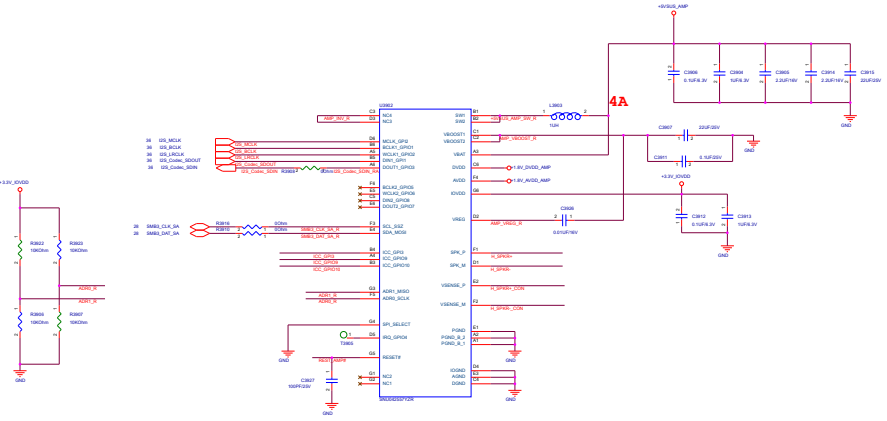
D3802 ESD Diode

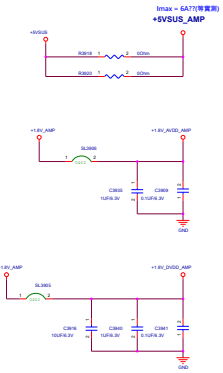
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

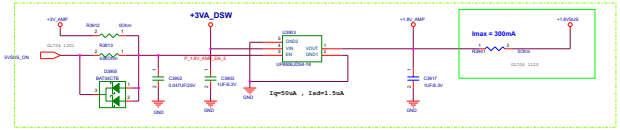
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

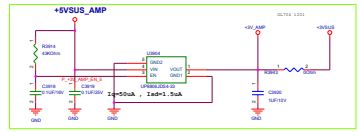
ASUSTeK COMPUTER INC. NB1	Title :	Aud_HP Jack, MIC	
	Engineer:	EE	
Size: D	Project Name:	GX701	Rev: 1.0
Date: Tuesday, April 02, 2019	Sheet	38 of	106

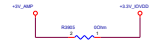
POWER











11.2 Power Supply Sequencing

The following power sequence should be followed for power up and power down. If the recommended sequence is not followed there can be large current in device due to faults in level shifters and diodes becoming forward biased. The T_{delay} between power supplies should be large enough for the power rails to settle.

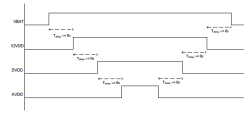


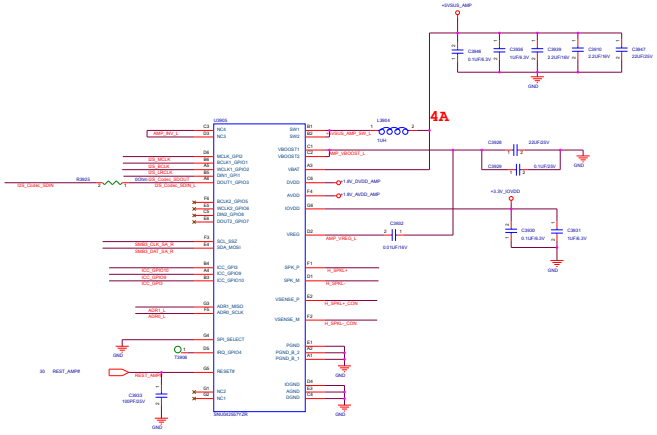
Figure 40. Power Supply Sequence for Power-Up and Power-Down

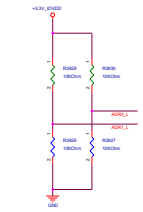
When the supplies have settled, the /RESET terminal can be set HIGH to operate the device. Additionally the /RESET pin can be tied to IOVDD and the internal DVDD POR will perform a reset of the device. After a hardware or software reset additional commands to the device should be delayed for 100uS to allow the OTP to load. The above sequence should be completed before any I²C operation.

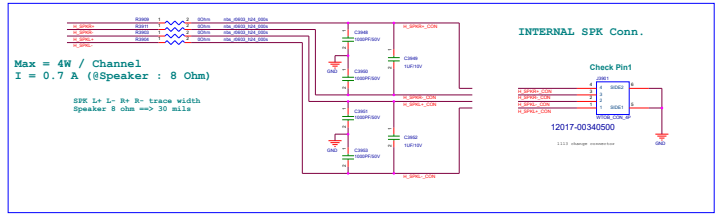
11.1 Power Supplies

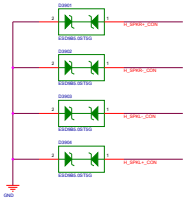
The TAS2555 requires four power supplies:

- Boost Input (terminal: VBAT)
  - Voltage: 2.9 V to 5.5 V
  - Max Current: 5 A for ILIM = 3.0 A (default)
- Analog Supply (terminal: AVDD)
  - Voltage: 1.65 V to 1.95 V
  - Max Current: 30 mA
- Digital Supply (terminal: DVDD)
  - Voltage: 1.65 V to 1.95 V
  - Max Current: TBD mA
- Digital I/O Supply (terminal: IOVDD)
  - Voltage: 1.62 V to 3.6 V
  - Max Current: 5 mA



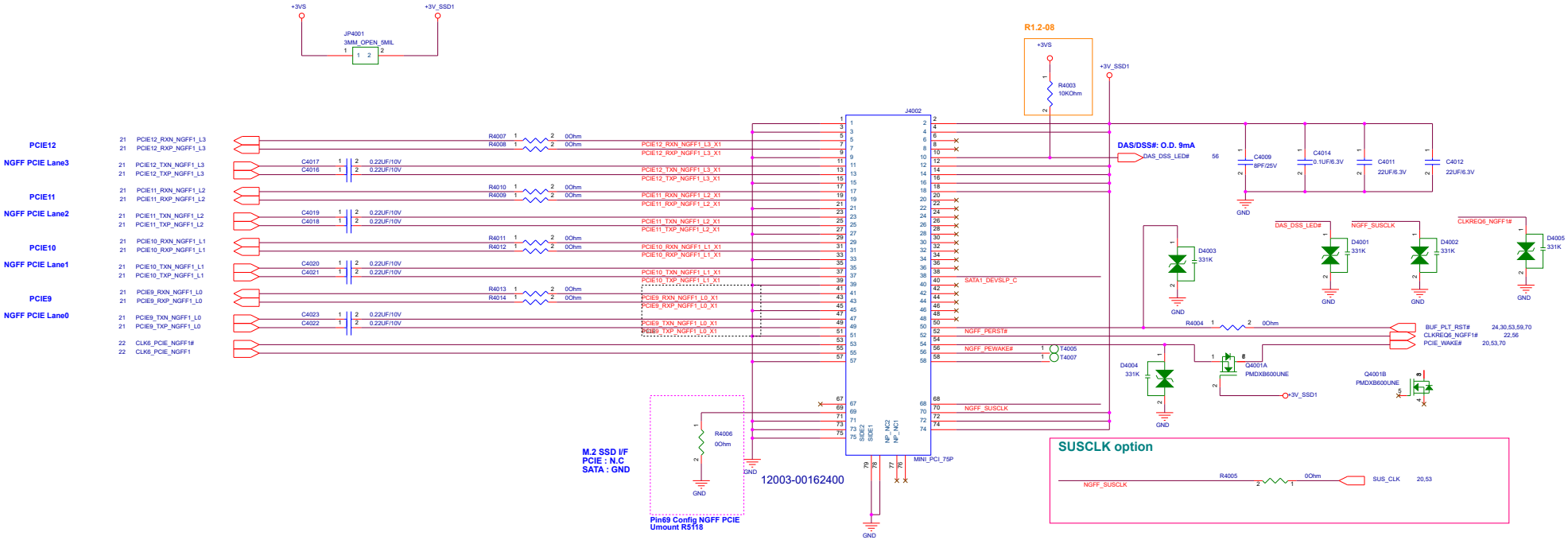






Variant Name:		
ASUSTeK COMPUTER INC.	Title :	Aud_Woofer_**
	Engineer:	EE
Size: D	Project Name: GX701	Rev: 1.0
Date: Tuesday, April 02, 2019	Sheet: 28 of 135	

KEY-M NGFF_SSD



HW Disable SSD Devslp	Mount R4002=0ohm, Unmount R4001=0ohm
HW Enable SSD Devslp	Unmount R4002=0ohm, Mount R4001=0ohm

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : MiniCard_SSD

Engineer: EE

Size	Project Name	Rev
C	GX701	1.0

Date: Tuesday, April 02, 2019 Sheet 40 of 100

<Variant Name>

Title : CB_*****

ASUSTeK COMPUTER INC. NB3

Engineer: EE

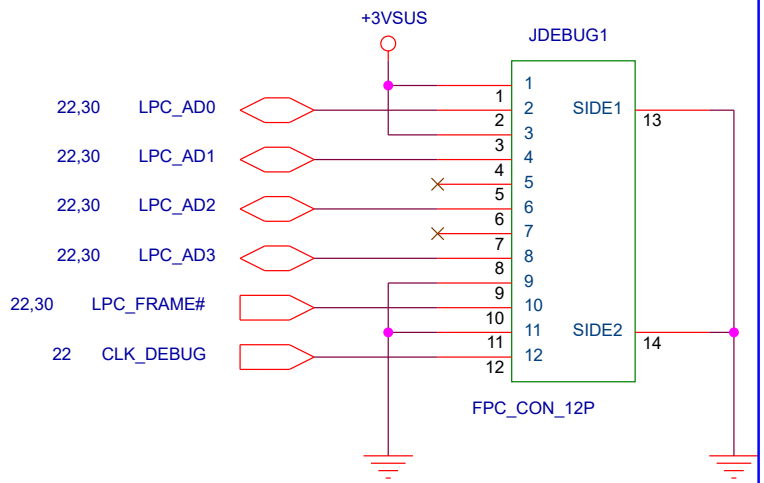
Size	Project Name	Rev
C	GX701	1.0

Date:	Wednesday, March 06, 2019	Sheet	41	of	100

ASUSTeK COMPUTER INC. NB1	Title : HDMI_DP_Switch	
	Engineer: EE	
Size: C	Project Name: GX701	Rev: 1.0
Date: Wednesday, March 06, 2019	Sheet 42 of 100	

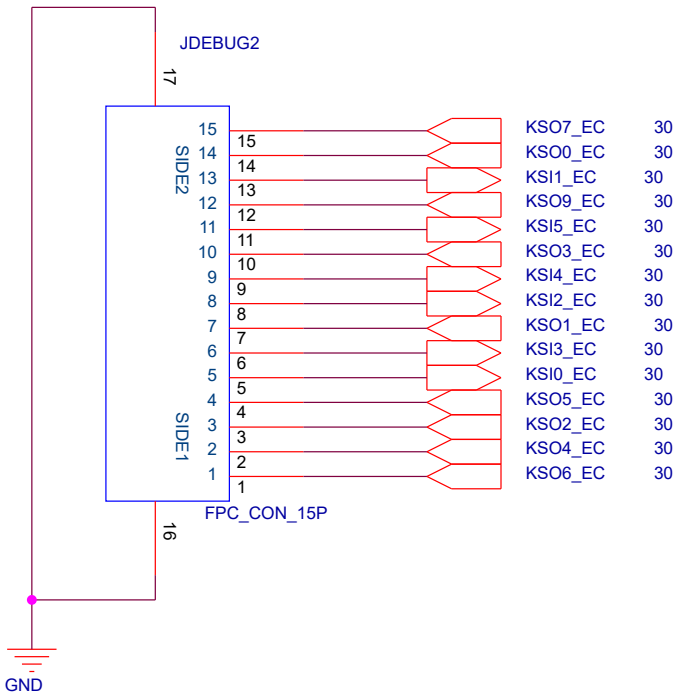
2017/11/10

LPC Debug Port



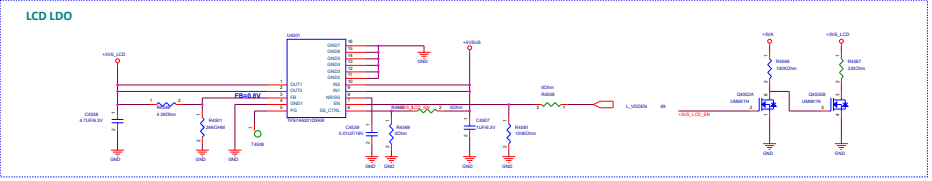
ER2 stuff

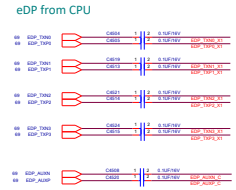
2017/11/10

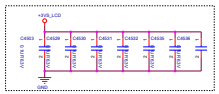


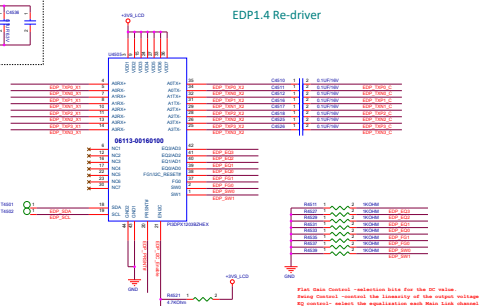
<Variant Name>

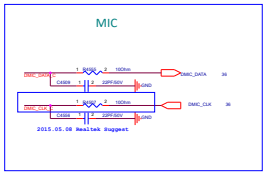
ASUSTeK COMPUTER INC. NB1	Title : DEBUG_LPC	
	Engineer: EE	
Size: A	Project Name: GX701	Rev: 1.0
Date: Tuesday, April 02, 2019	Sheet 44 of 100	

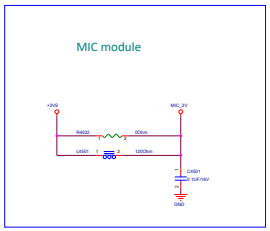


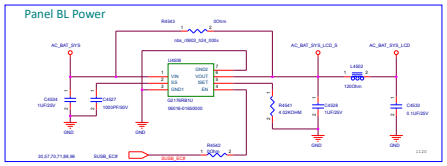


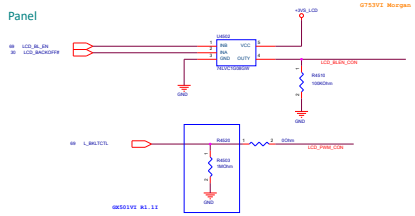


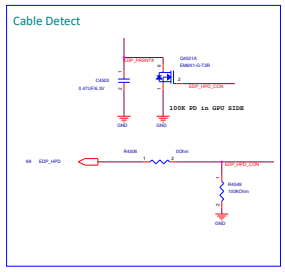


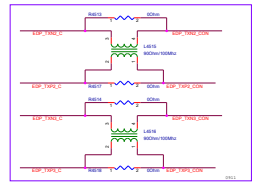


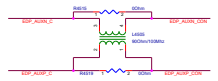


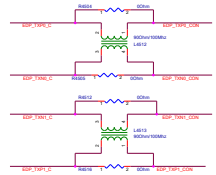


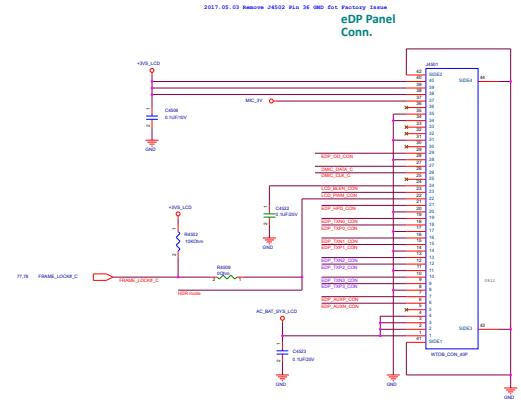


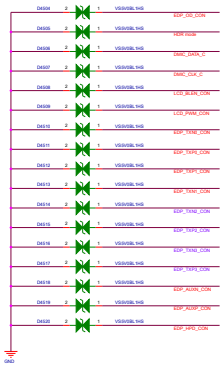


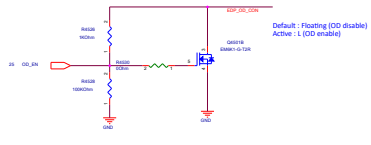


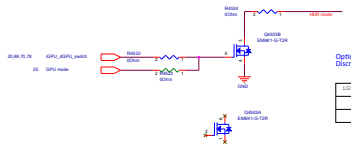












iGPU_dGPU_switch	Panel Pin34	Mode
L	Floating (default)	Optimus
H	Low	Discrete

Project Name

GX701

Rev

2.0

Title : TYPE-C USB3.1_R1.5_4

Size	Dept.:	Engineer:
D	ASUSTeK COMPUTER INC. NBT	EE

Date: Wednesday, March 06, 2019

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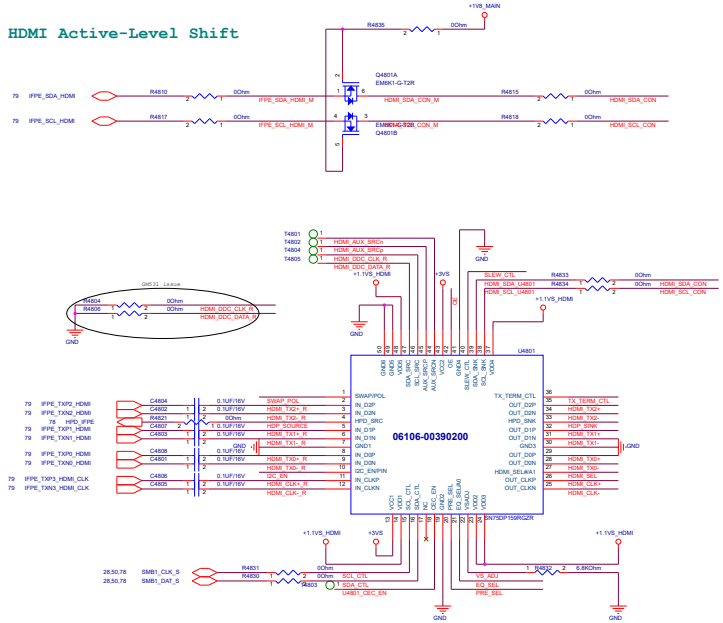
<Variant Name>

ASUS	Title :	DDR4_ON-BOARD_A1	
ASUSTeK COMPUTER INC.	Engineer:	EE	
Size: E	Project Name: GX701		Rev: 1.0
Date: Tuesday, April 02, 2019		Sheet 14 of 100	

Main Board

HDMI Active-Level Shift



Slew rate control when I2C_EN/PIN = Low.
SLEW_CTL = H, fastest data rate
SLEW_CTL = L, 5 ps slow
SLEW_CTL = No Connect, 10 ps slow

HDMI_SEL when I2C_EN/PIN = Low
HDMI_SEL = High: Device configured for DVI
HDMI_SEL = Low: Device configured for HDMI

Input Receive Equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14 dB

De-emphasis pin strap when I2C_EN/PIN = Low.
PRE_SEL = L: - 2 dB de-emphasis level
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved

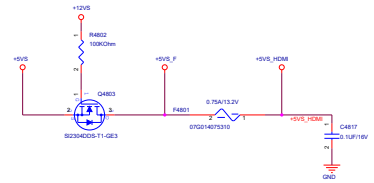
I2C_EN/PIN = High; puts device into I2C control mode
I2C_EN/PIN = Low; puts device into pin strap mode

I2C_EN/PIN = High; puts device into I2C control mode
I2C_EN/PIN = Low; puts device into pin strap mode

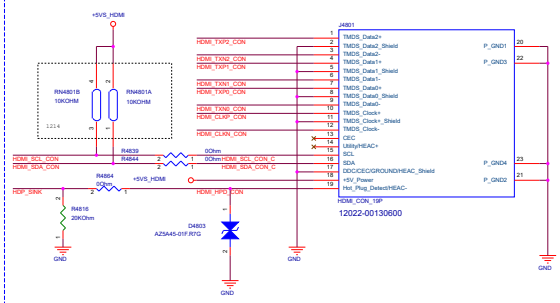
I2C_EN/PIN = High; puts device into I2C control mode
I2C_EN/PIN = Low; puts device into pin strap mode

Operation enable/reset pin
OE = L: Power-down mode OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

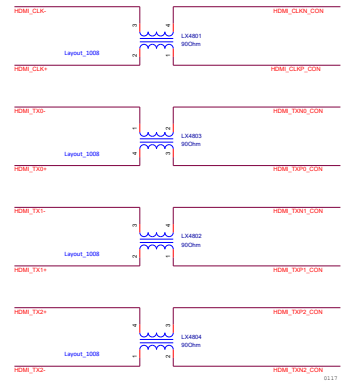
HDMI PWR_+5VS_HDMI



HDMI Conn.



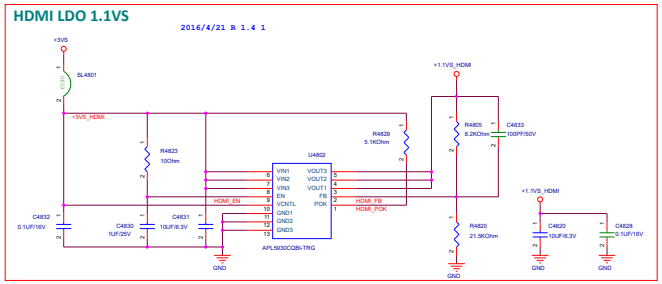
HDMI EMI

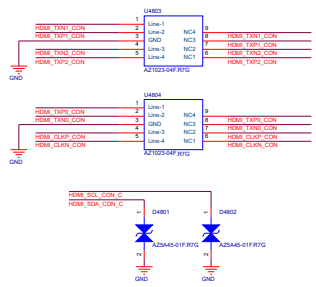


N56V C.M Choke : M 09G092090110

HDMI LDO 1.1VS

2016/4/21 R 1.4 1

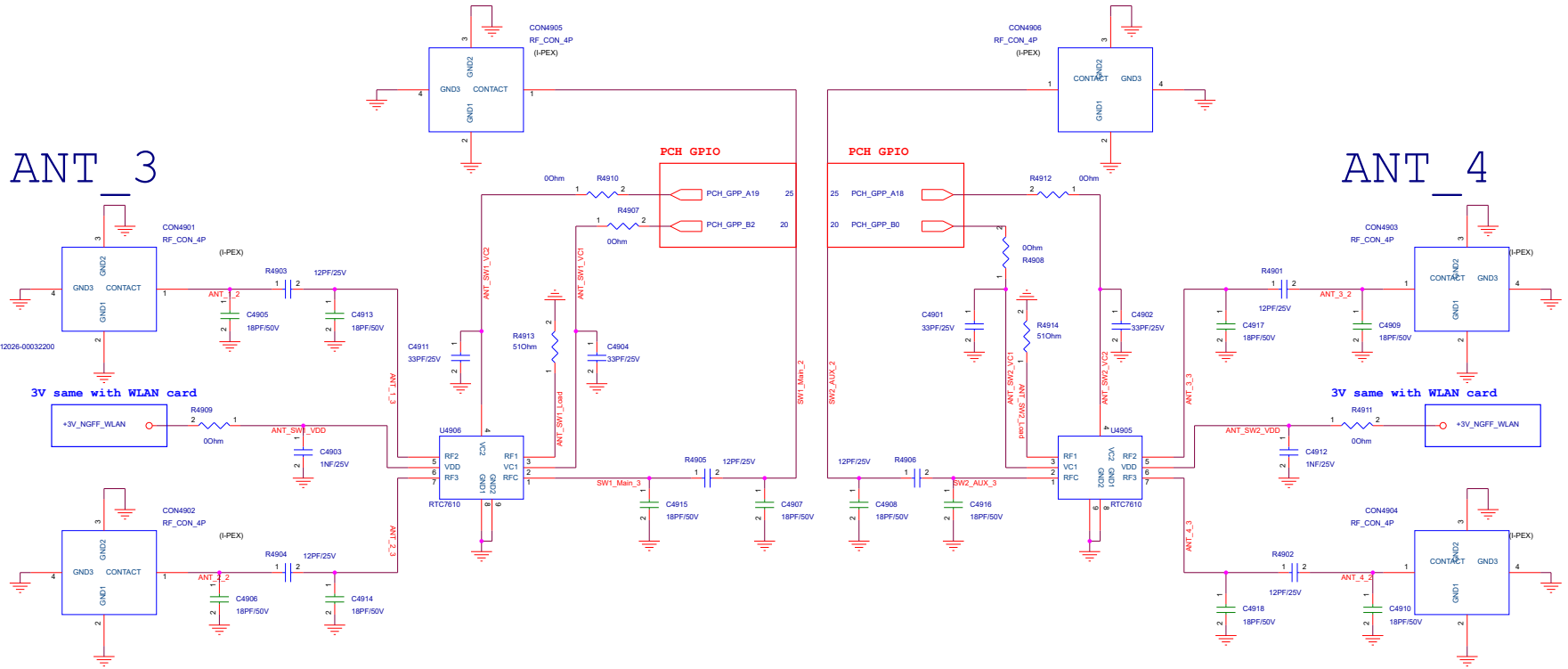




ASUS	Project Name: GX701		Rev: 1.3
Title : HDMI			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet: 48 of 100		

Module_AUX

Module_MAIN



U4906 RTC7610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Ω	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

U4905 RTC7610			
ANT	Port	VC1 GPP_B0	VC2 GPP_A18
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

<Core Design>

ASUS	Project Name: GX701	Rev: 1.0
Title : ANT		
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Tuesday, April 02, 2019	Sheet 49 of 100	

<Core Design>

Title : TYPE-C USB3.1_R1.5_4

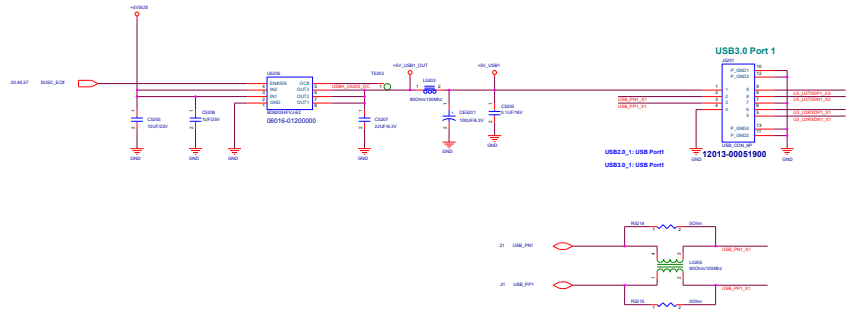
ASUSTeK COMPUTER INC. NB1

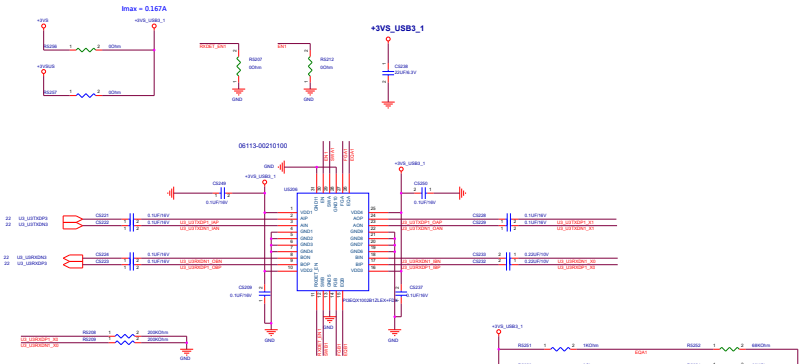
Engineer:

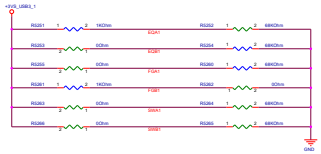
Size	Project Name	Rev
D	**GX701**	R1.5

Date:	Wednesday, March 06, 2019	Sheet	51	of	100

Main Board







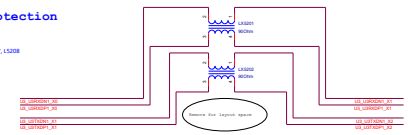
USB3.0 ESD-Protection

1st : 07G028076030
ESD PROTECTION AZ1045-04F

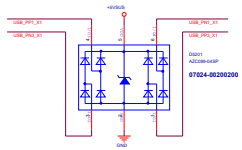
2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

USB3.0 EMI-Protection

12/10/25
LS201, LS202,LS207, LS208
09G0920090400



USB2.0 ESD-Protection



07024-00200200

D5301 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

< Channel / Receiver setting for Pericom 1002B >

Setting	Channel Enable [EN]	Receiver Detection [RXDET_EN]
0 : 0 Ω to GND	Disable	Disable
1 : 0 Ω to VDD	Enable(Default)	Enable(Default)
Note	Channel Enable / Receiver detection With internal 300K pull-up R.	

< Fine tune table for Pericom (One port Gen2) >

< SW table for Pericom 1002B >

SW[A:B]	Output Linear Swing (mV)
0 : 0 Ω to GND	800
R : Rext to GND	1200
F : Leave Open	1000 (Default)
1 : 0 Ω to VDD	1100

< FG table for Pericom 1002B >

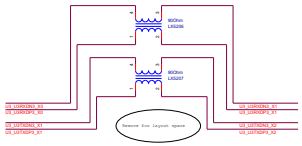
FG[A:B]	Flat Gain (dB)
0 : 0 Ω to GND	-3.0
R : Rext to GND	-1.5
F : Leave Open	0 (Default)
1 : 0 Ω to VDD	+2.0

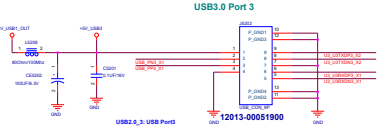
< EQ table for Pericom 1002B >

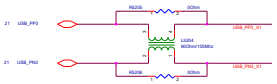
EQ[A:B]	Gen 1 @2.5GHz(dB)	Gen 2 @5GHz(dB)
0 : 0 Ω to GND	5.1	10.9
R : Rext to GND	1.9	6.7
F : Leave Open	3.5(Default)	8.9(Default)
1 : 0 Ω to VDD	6.8	13.1

Note : With internal 100Kohm pull-up Rup and 200Kohm pull-down Rdown.
Rext = 68Kohm

USB3.0_PORT3



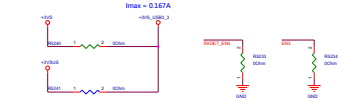


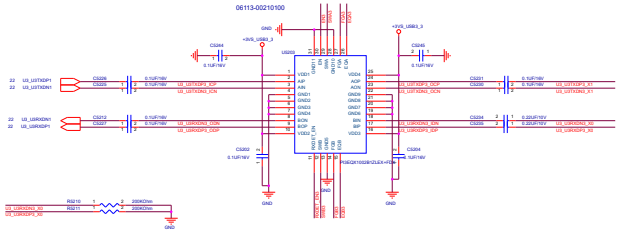


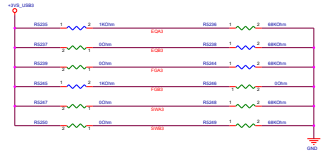
USB3.0 ESD-Protection

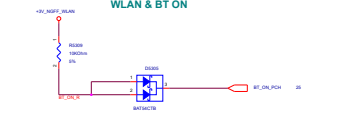
1st : 07G028076030
ESD PROTECTION AZ1045-04F

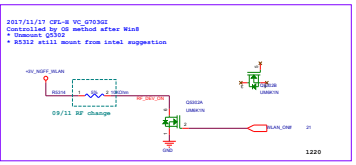
2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

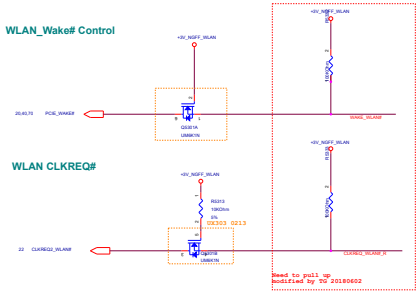


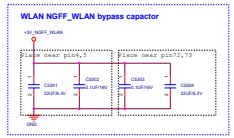


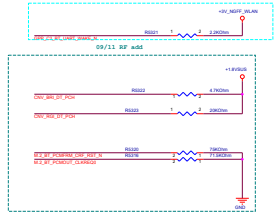


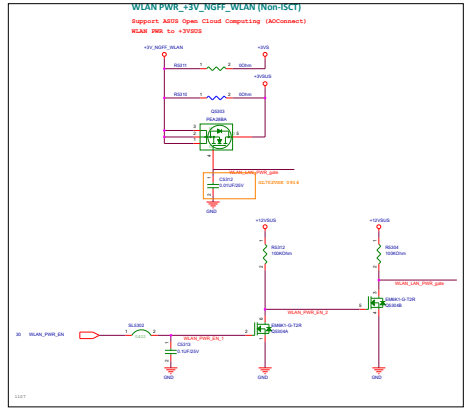






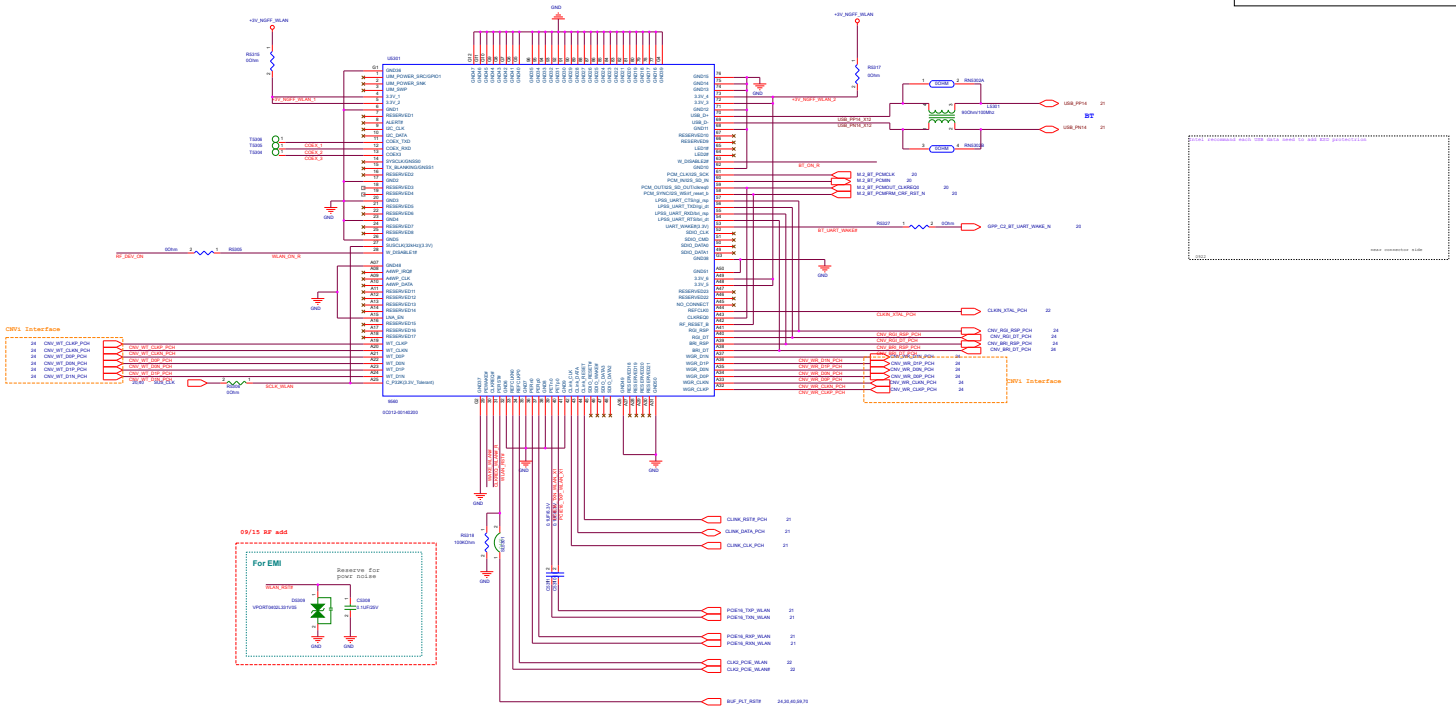






2017.03.15 Connector list update

SD-1216



<Variant Name>

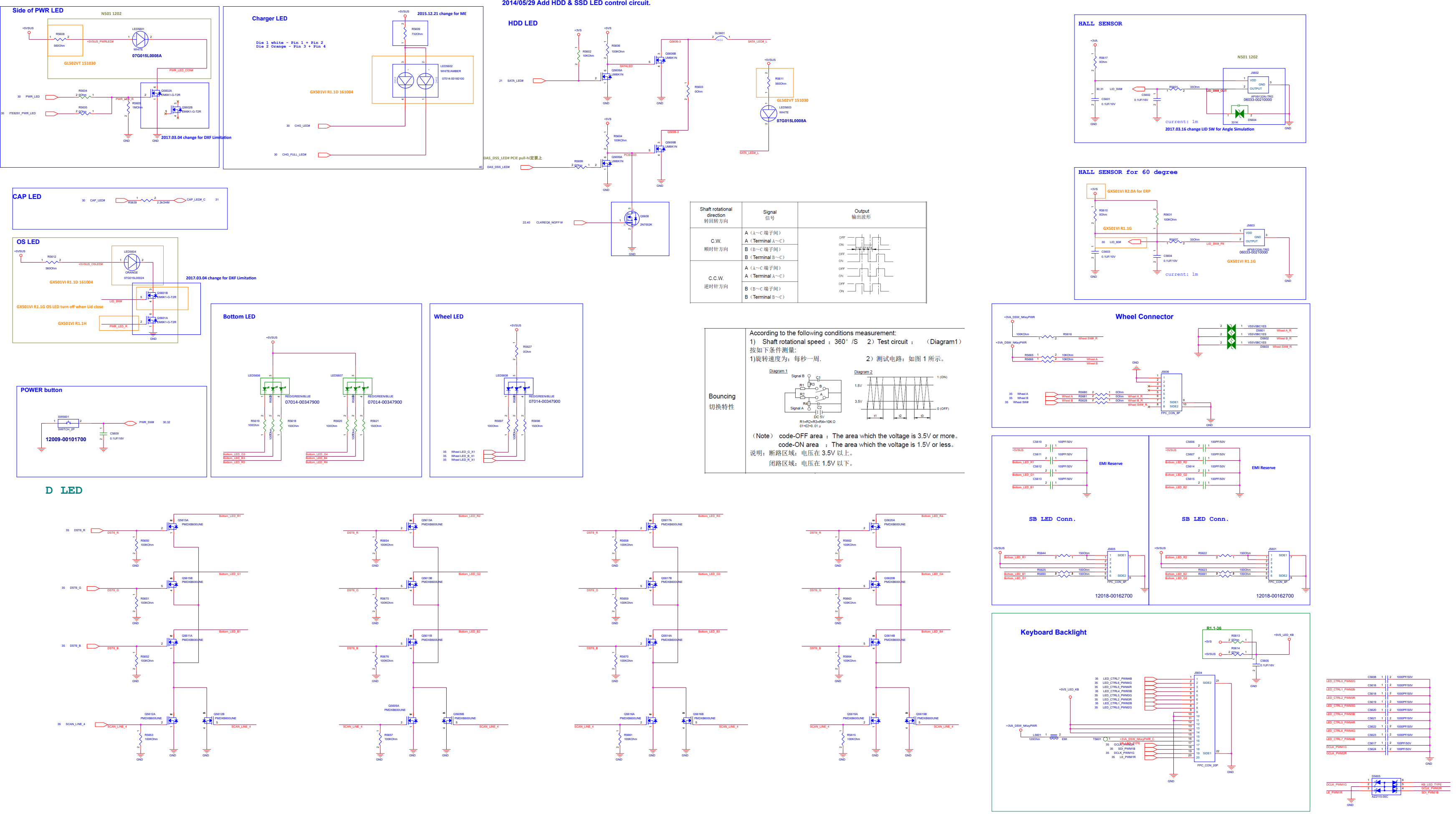
Title : IO Con. to MB

ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size	Project Name	Rev
Custom	**GX701**	1.0

Date:	Wednesday, March 06, 2019	Sheet	55	of	100



Shaft rotational direction 转回转方向	Signal 信号	Output 输出波形
C.W. 顺时针方向	A（A~C 端子间） A（Terminal A~C）	
	B（B~C 端子间） B（Terminal B~C）	
C.C.W. 逆时针方向	A（A~C 端子间） A（Terminal A~C）	
	B（B~C 端子间） B（Terminal B~C）	

Bouncing 切换特性

According to the following conditions measurement:
1) Shaft rotational speed ：360° /S 2）Test circuit ： （Diagram1）
按如下条件测量:
1)旋转速度为：每秒一周. 2）测试电路：如图 1 所示。

Diagram 1 — R1=R2=R3=R4=10KΩ, C1=C2=0.01μ

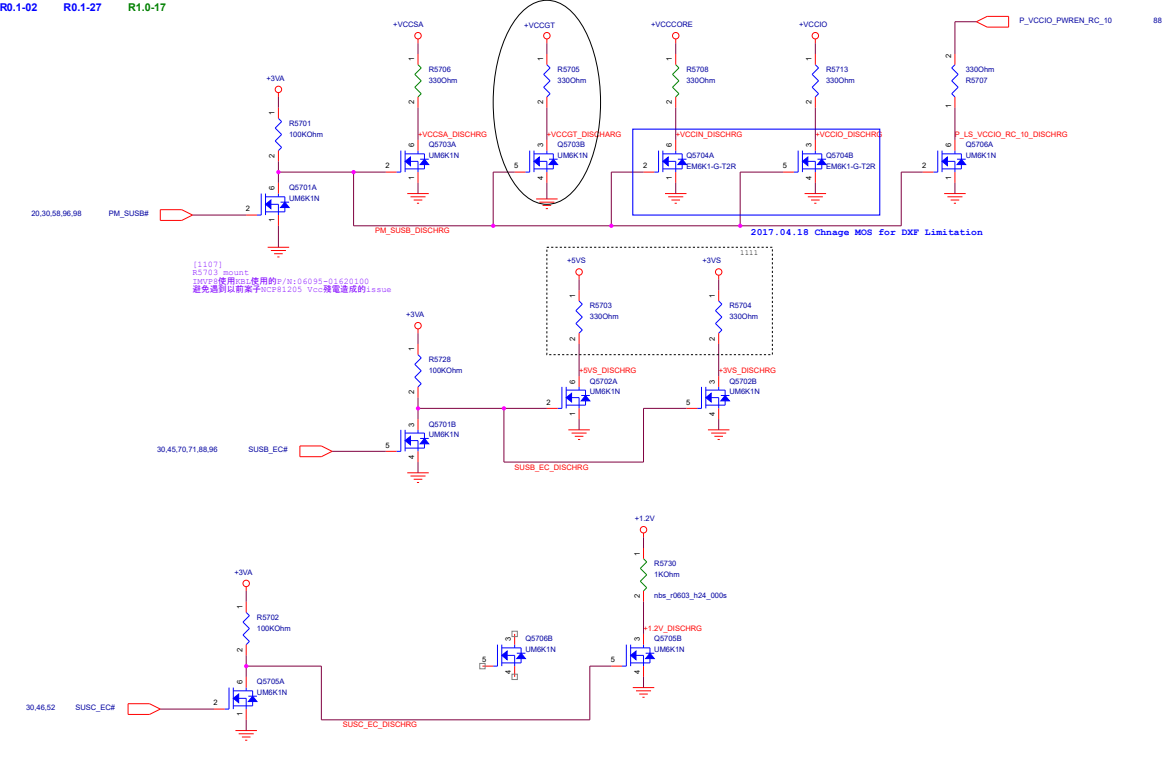
Diagram 2

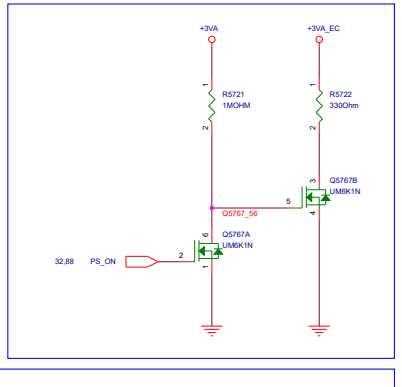
（Note） code-OFF area ：The area which the voltage is 3.5V or more。
code-ON area ：The area which the voltage is 1.5V or less。
说明：断路区域：电压在 3.5V 以上。
闭路区域：电压在 1.5V 以下。

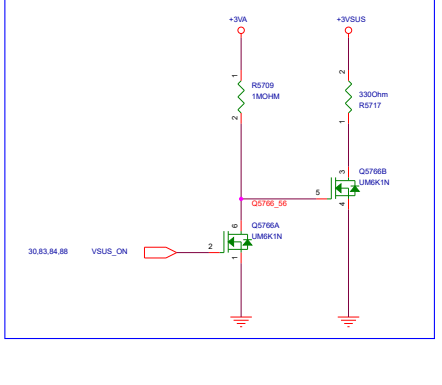
<Variant Name>

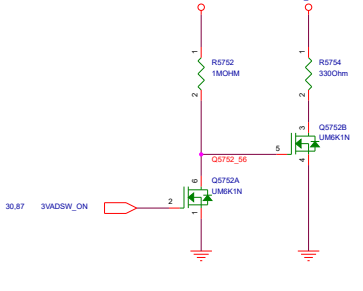
ASUSTeK COMPUTER INC. NB3	Title : LED & LID	Engineer: EE
Size: Custom	Project Name: GX701	Rev: 1.0
Date: Tuesday, April 02, 2019	Sheet 56 of 100	

R0.1-02 R0.1-27 R1.0-17



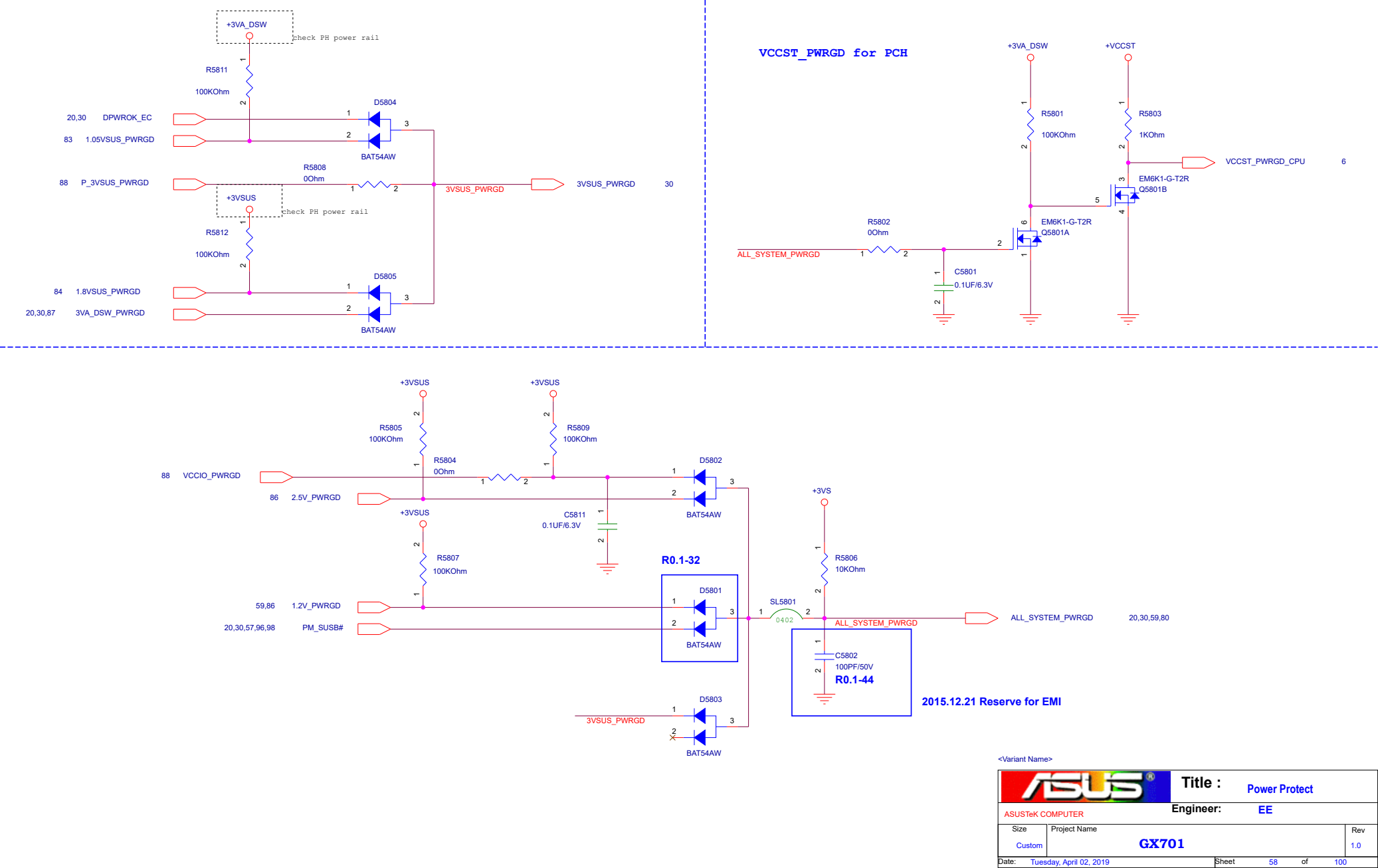






<variant_name>

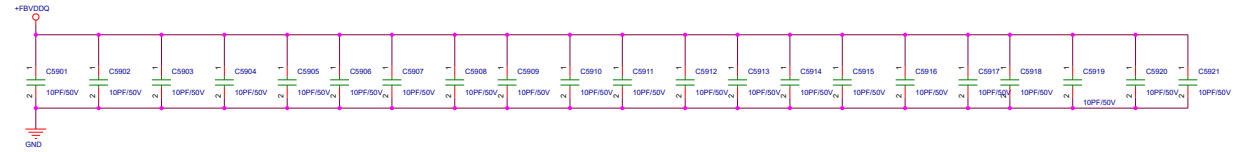
ASUSTeK COMPUTER	Title : DSG_Discharge	
	Engineer: EE	
Size: C	Project Name: GX701	Rev: 1.0
Date: Tuesday, April 02, 2019	Sheet 57 of 100	

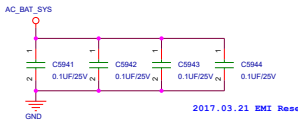


<Variant Name>

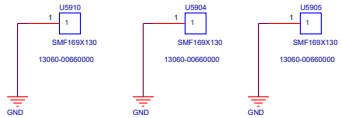
ASUSTeK COMPUTER	Title : Power Protect	
	Engineer: EE	
Size: Custom	Project Name: GX701	Rev: 1.0
Date: Tuesday, April 02, 2019	Sheet 58 of 100	

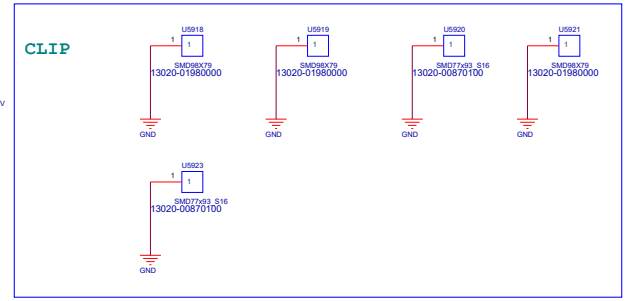
2016/06/08 EMI



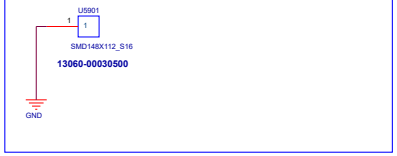


2017.03.21 EMI Reserve

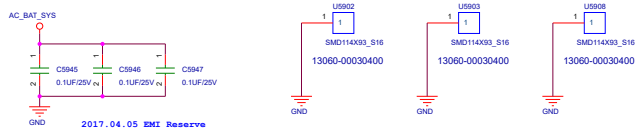




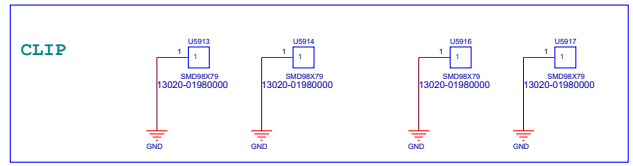
2016/08/05 EMI



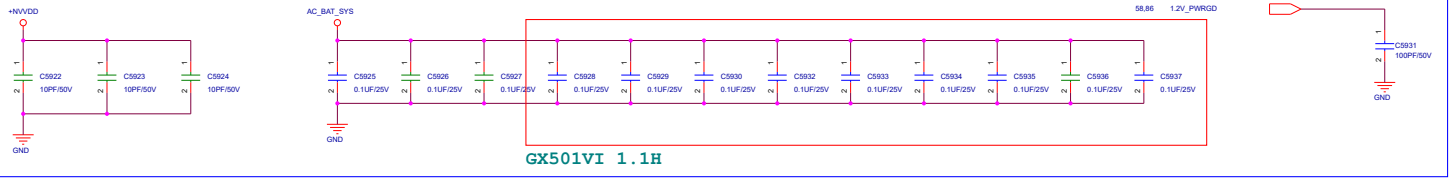
2017/04/05 EMI



2017.04.05 EMI Reserve

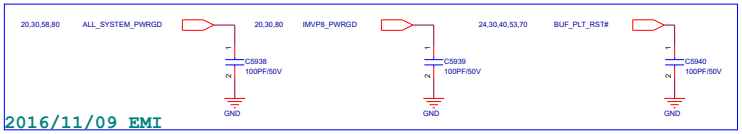


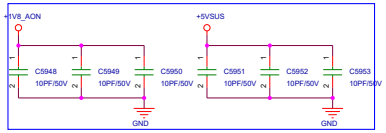
2016/07/27 EMI



GX501VI 1.1H

2016/11/09 EMI



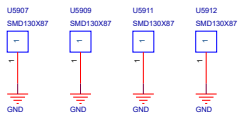


2017.05.02 EMI Reserve

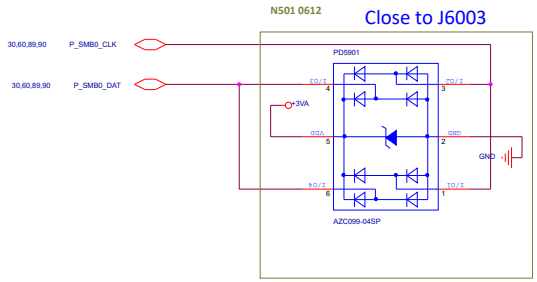
2017.05.02 EMI Reserve

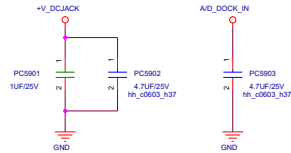
2017/12/20 EMI

Modify Footprint

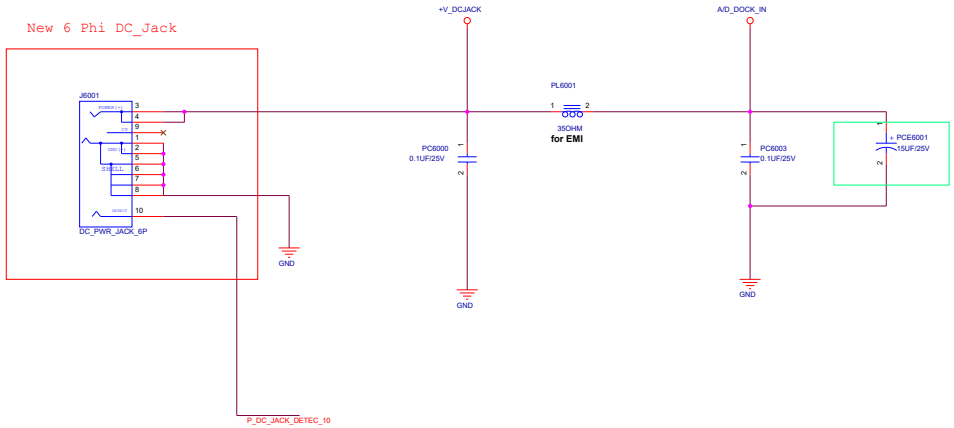


13040-00960300





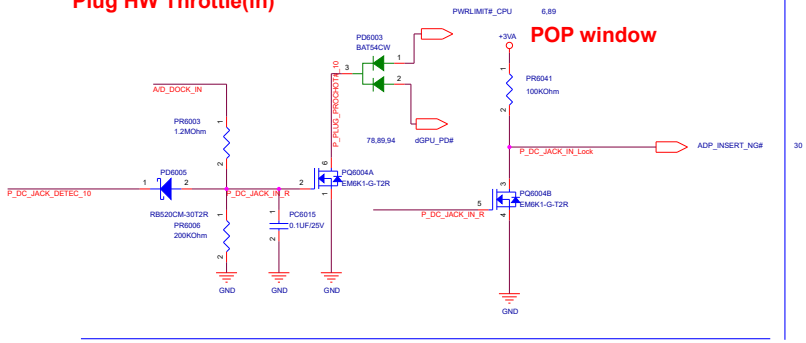
DC-IN Connector



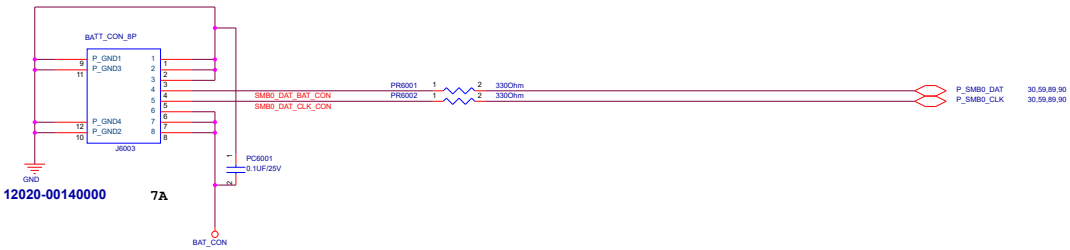
Mode	ADP_INSERT_NG#	AC_IN_OC#
AC Mode	0 (POP,throttling, stop charging)	0
	1	

Main Board

Plug HW Throttle(in)



Battery Connector



12020-00140000 7A

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : DC & BAT IN

Engineer:

Size	Project Name	Rev
C	GX701	R1.0

Date: Tuesday, April 02, 2019 Sheet 60 of 100

<Variant Name>

Title : I/O board(1-1)_CR_RTS5139

ASUSTeK COMPUTER INC. NB3

Engineer: EE

Size	Project Name	Rev
C	**GX701**	1.0

Date:	Wednesday, March 06, 2019	Sheet	62	of	100

<Variant Name>

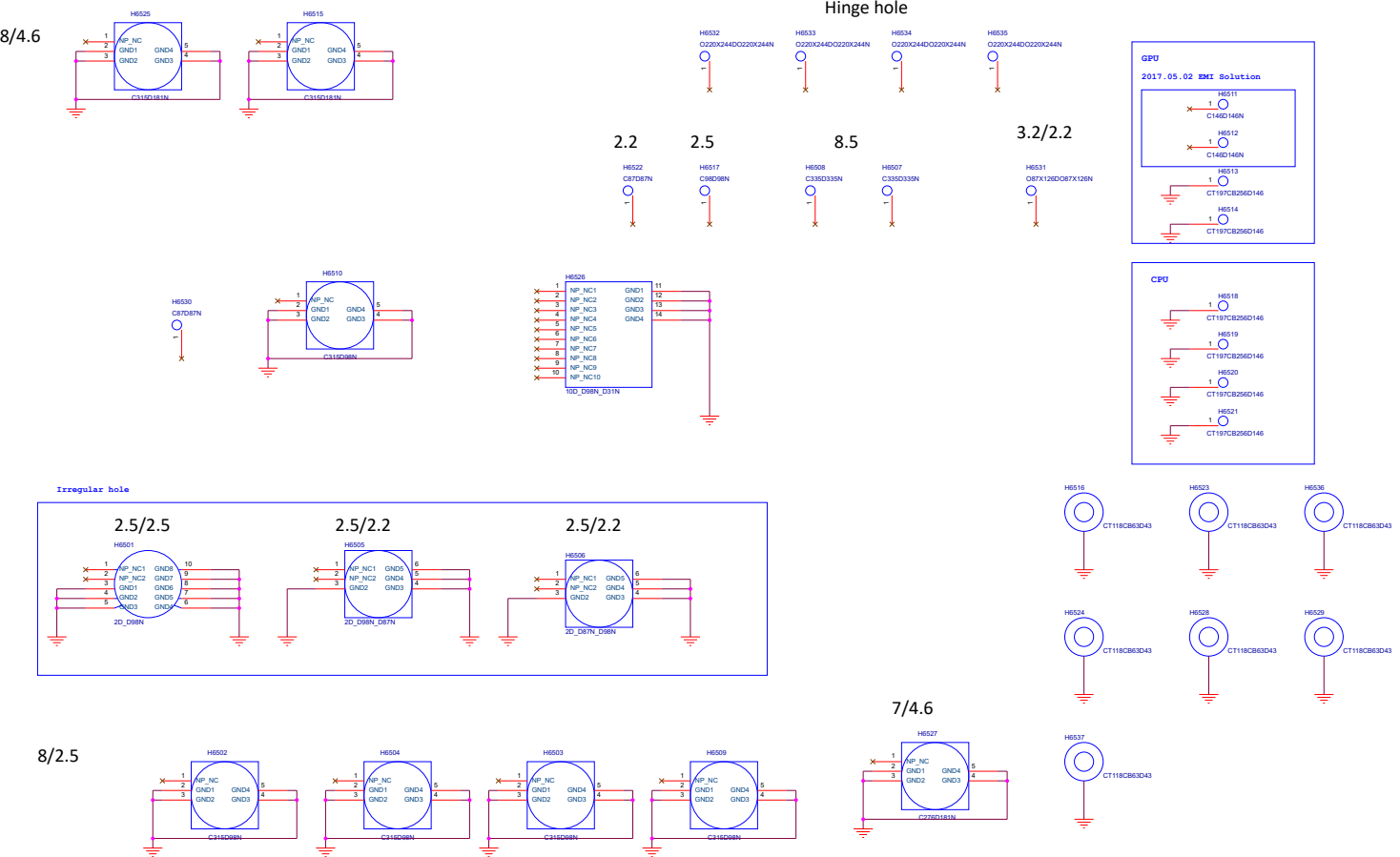
Title : USB Port

ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size	Project Name	Rev
C	**GX701**	1.0

Date:	Wednesday, March 06, 2019	Sheet	63	of	100


Hinge hole
8/4.6
H6525
H6515
NP_NC
GND1
GND2
GND3
GND4
C315D181N
H6532
H6533
H6534
H6535
O220X244DO220X244N
2.2
2.5
8.5
3.2/2.2
H6522
C87D87N
H6517
C98D98N
H6508
C335D335N
H6507
H6531
O87X126DO87X126N
GPU
2017.05.02 EMI Solution
H6511
H6512
C146D146N
H6513
H6514
CT197CB256D146
H6530
H6510
C315D98N
H6526
NP_NC1
NP_NC2
NP_NC3
NP_NC4
NP_NC5
NP_NC6
NP_NC7
NP_NC8
NP_NC9
NP_NC10
10D_D98N_D31N
CPU
H6518
H6519
H6520
H6521
Irregular hole
2.5/2.5
2.5/2.2
2.5/2.2
H6501
2D_D98N
H6505
2D_D98N_D87N
H6506
2D_D87N_D98N
H6516
H6523
H6536
H6524
H6528
H6529
CT118CB63D43
7/4.6
H6527
C276D181N
8/2.5
H6502
H6504
H6503
H6509
H6537

<Variant Name>

Title :

ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size	Project Name	Rev
D	**GX701**	1.0

Date:	Wednesday, March 06, 2019	Sheet	66	of	100

<Variant Name>

Title : I/O board FUNC key

ASUSTeK COMPUTER

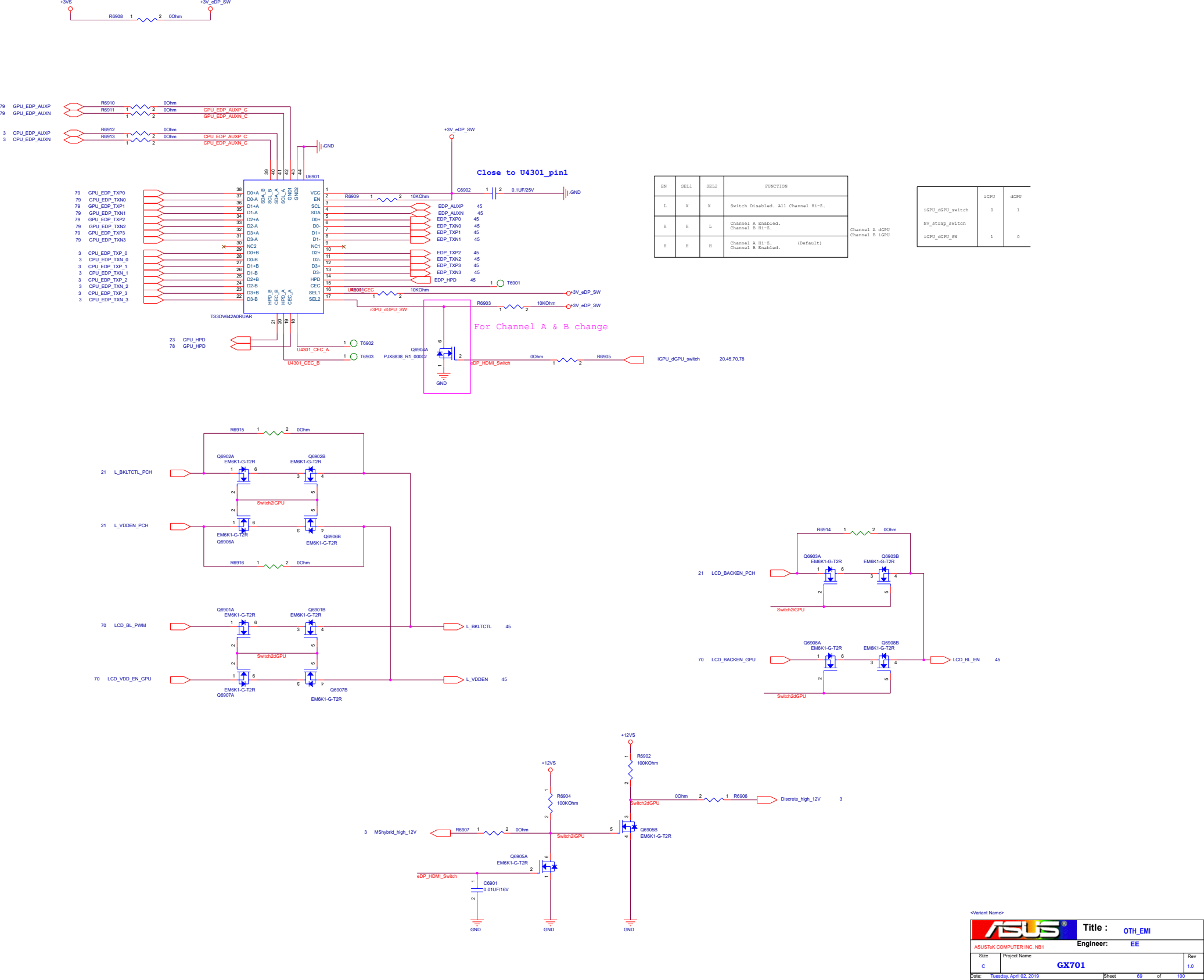
Engineer: EE

Size	Project Name	Rev
E	GX701	1.0

Date:	Wednesday, March 06, 2019	Sheet	67	of	100

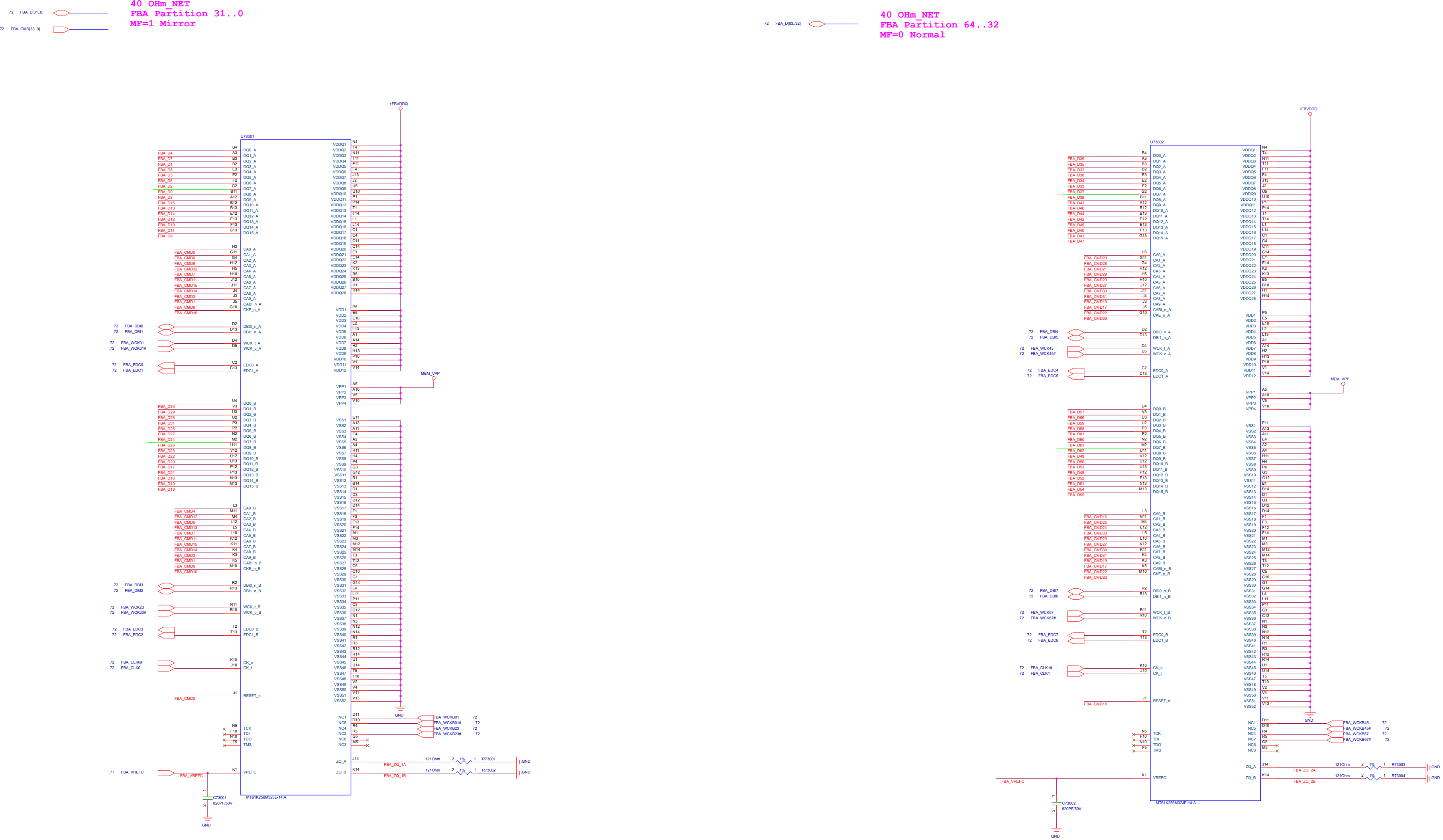
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : OTH_for test only	
	Engineer: EE	
Size: D	Project Name: GX701	Rev: 1.0
Date: Wednesday, March 06, 2019	Sheet 68 of 100	



<Variant Name>

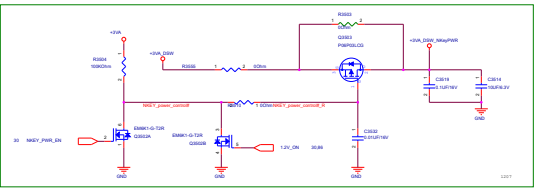
Title :	OTH_EMI
Engineer:	EE
ASUSTeK COMPUTER INC. NB1	
Size	C
Project Name	GX701
Rev	1.0
Date:	Tuesday, April 02, 2019
Sheet	69 of 100



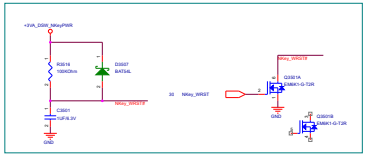
<Variant Name>

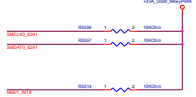
Title	<Title>	
Size A1	Document Number GX701	Rev R1.0
Date: Tuesday, April 02, 2019	Sheet 73 of 100	

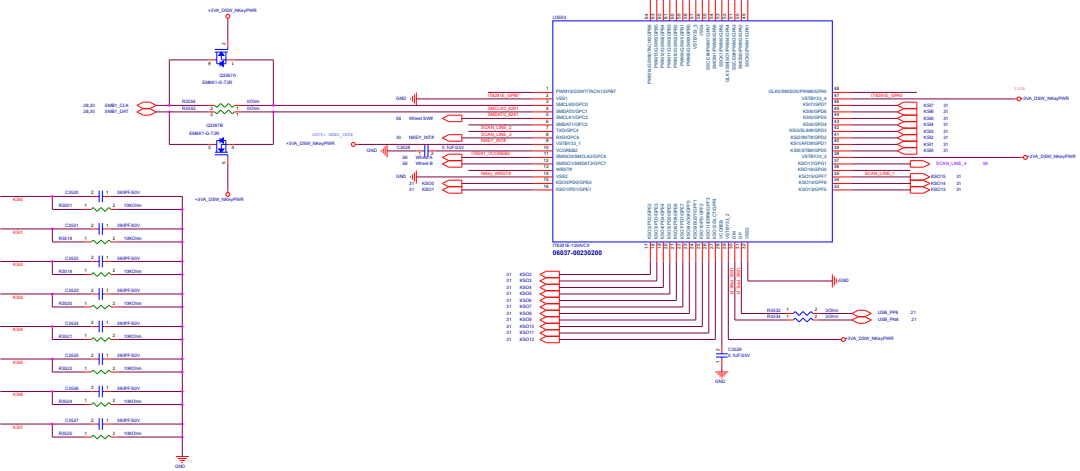
N_KEY_IT8291E



For EC Reset N_key







For DS3 wake from KB

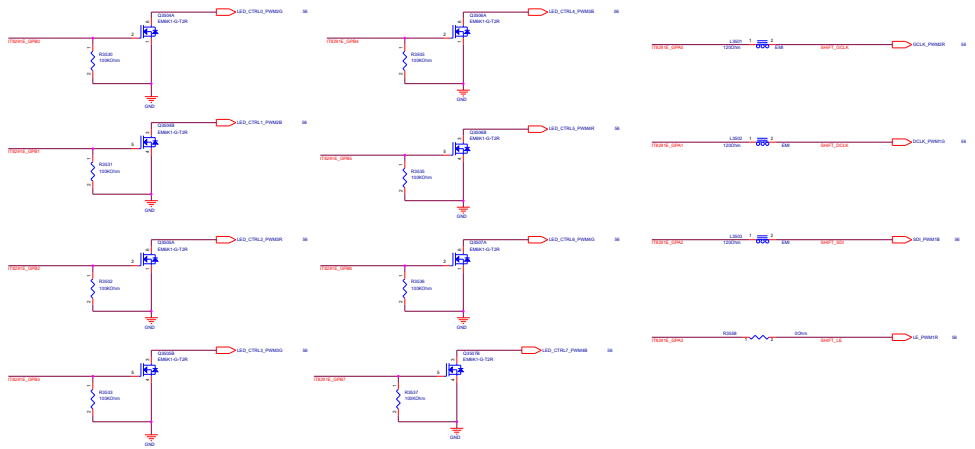
Use NEY-INT# to substitute
0920

For S4/S5 don't wake from KB

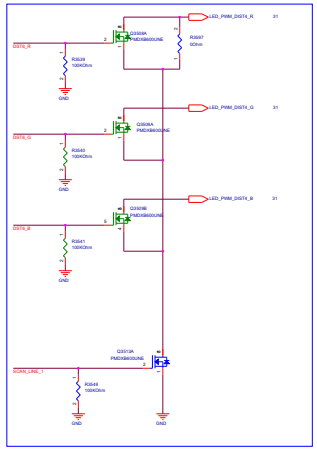
Use NEY-INT# to substitute
0920

ITE 8291 debug con

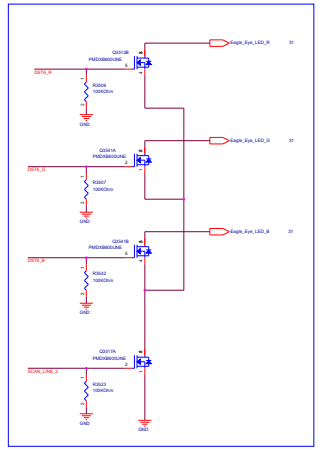
KB RGB LED



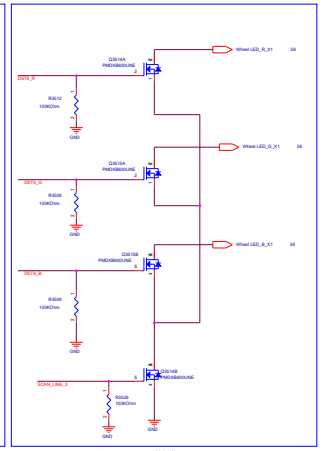
TP LED



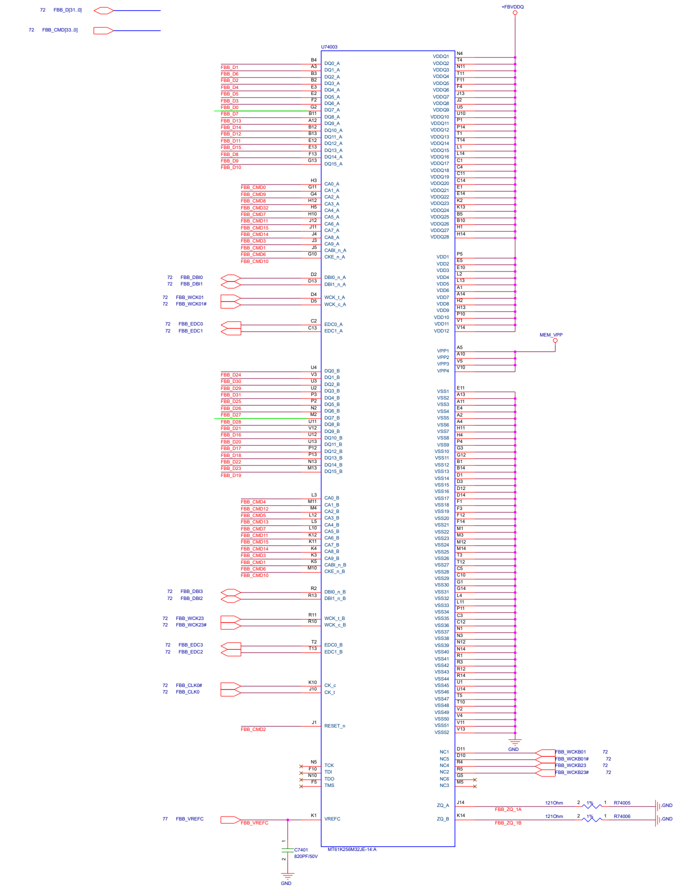
Eagle Eye LED



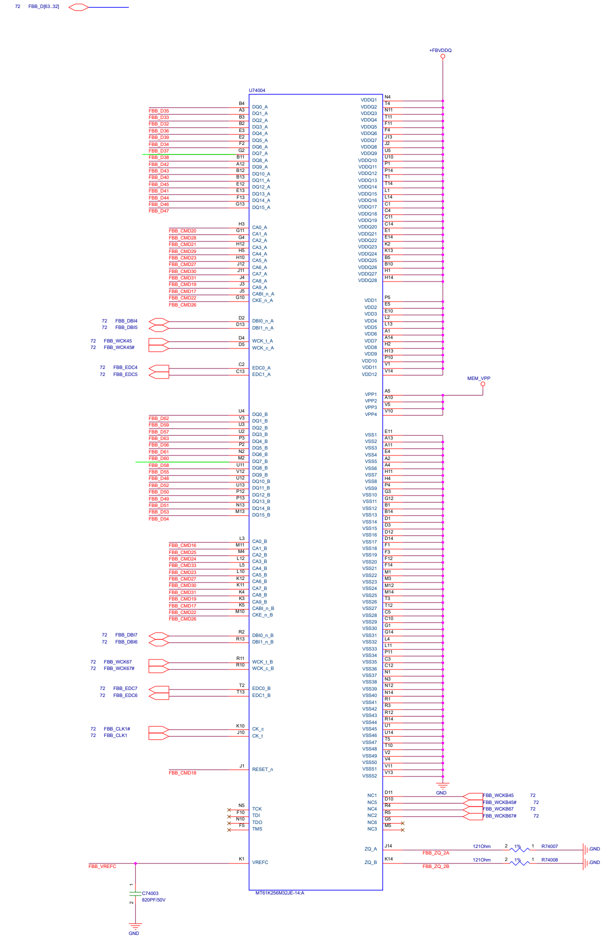
Wheel LED



40 OHm_NET
FBB Partition 31..0
MF=1 Mirror



40 OHm_NET
FBB Partition 64..32
MF=0 Normal

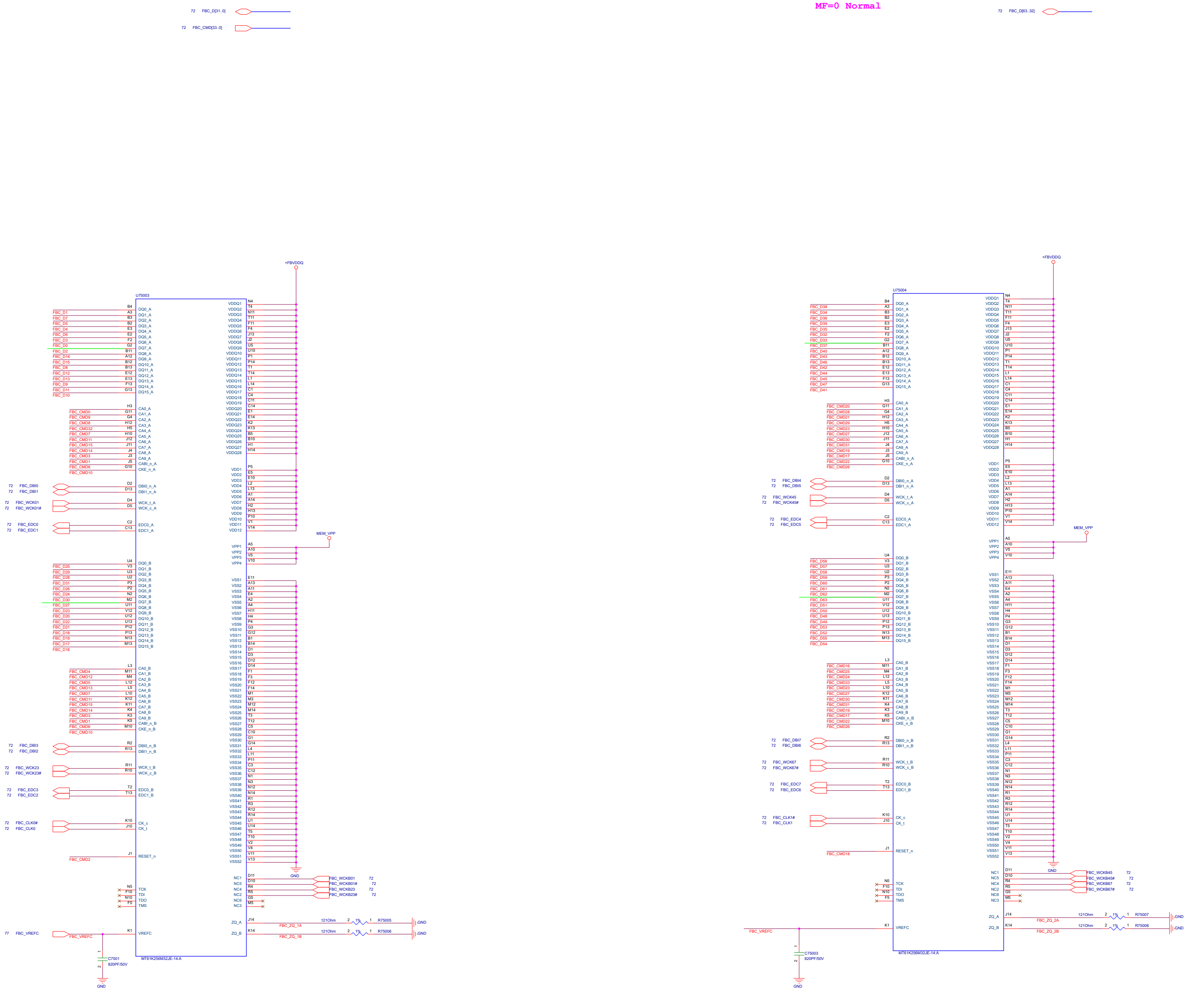


<Variant Name>

Title <Title>		
Size A1	Document Number GX701	Rev R1.0
Date: Tuesday, April 02, 2019	Sheet 74 of 100	

40 OHm_NET
FBC Partition 31..0
MF=1 Mirror

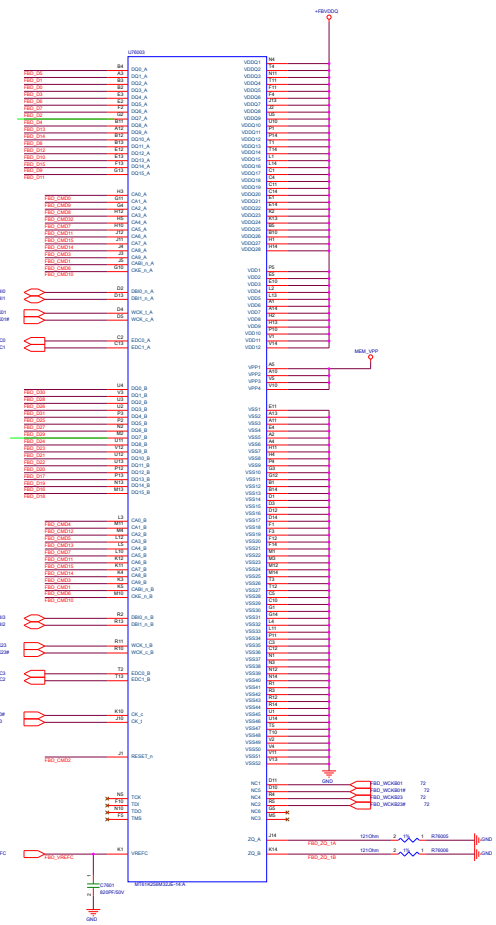
40 OHm_NET
FBC Partition 64..32
MF=0 Normal



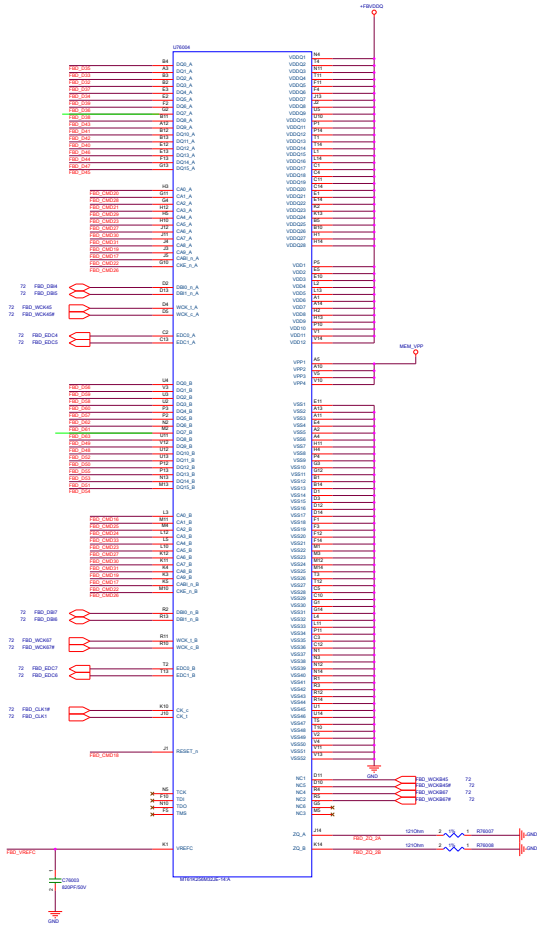
<Variant Name>

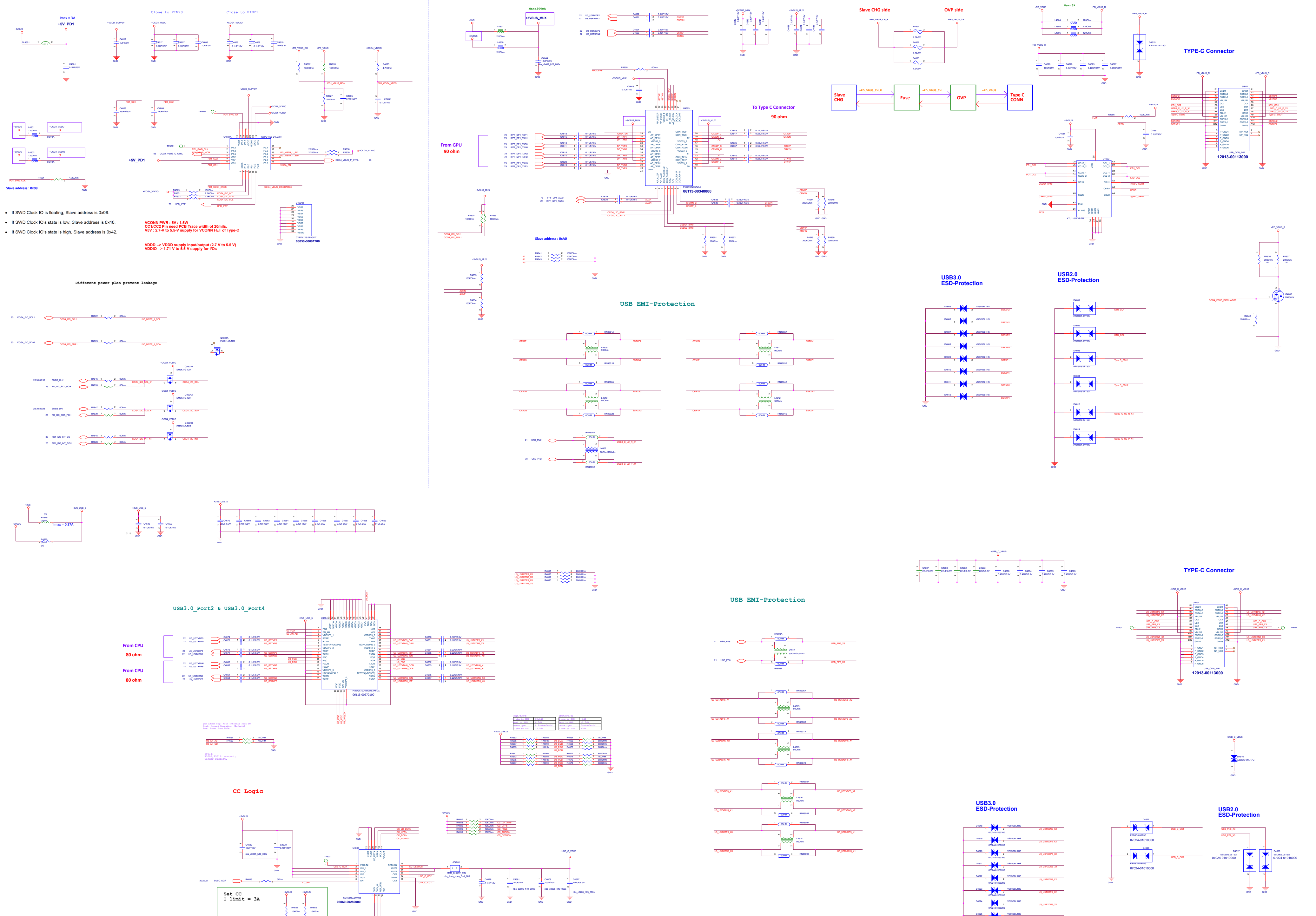
Title	<Title>	
Size A1	Document Number GX701	Rev R1.0
Date: Tuesday, April 02, 2019	Sheet 73 of 100	

40 OHm NET
FBD_Partition 31..0
MF=1 Mirror



40 OHm NET
FBDPartition 64..32
MF=0 Normal

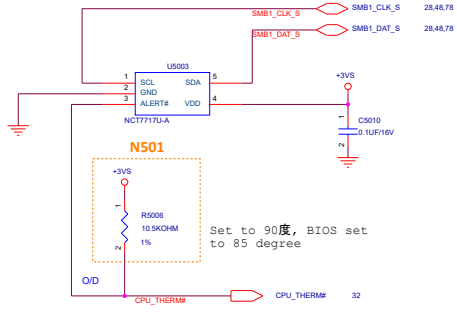




CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

Project Name: GX701
Rev: 1.0
Title : USB 3.1 ASM1142
Size: E
Dept.: ASUSTeK COMPUTER
Engineer: EE
Date: Wednesday, April 03, 2019
Sheet 46 of 100

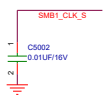
CPU Thermal Sensor

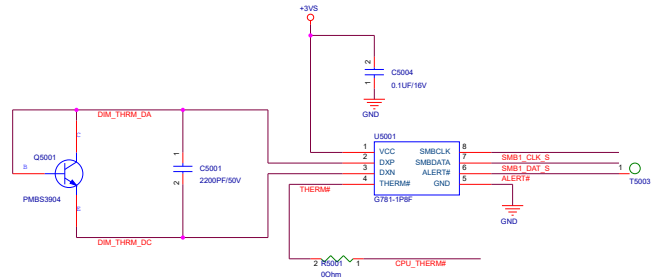


SMBUS address=10010000 (90)

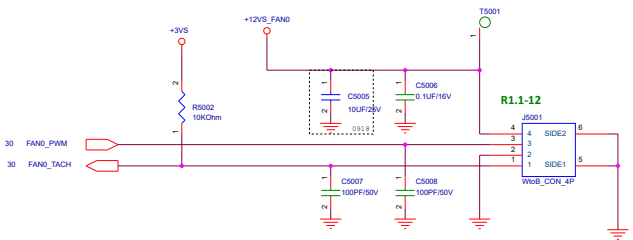
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

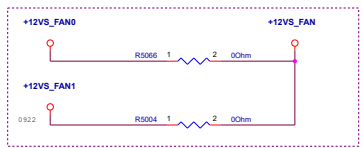
Reserve for
powr noise





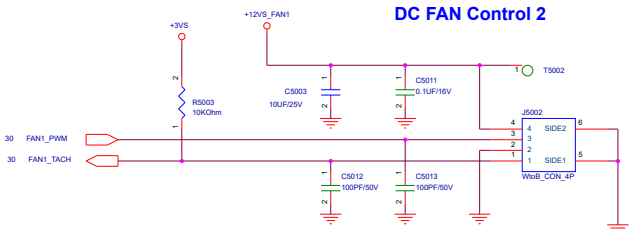
DC FAN Control 1





1st: 12017-00330300
2nd :12G171010049

DC FAN Control 2



1st: 12017-00330300
2nd :12G171010049

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : FAN_Thermal Sensor & Fan	
	Engineer: EE	
Size: C	Project Name: GX701	Rev: 1.0
Date: Tuesday, April 02, 2019	Sheet 50 of 100	

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : BT_Bluetooth	
	Engineer: EE	
Size: C	Project Name: GX701	Rev: 1.0
Date: Wednesday, March 06, 2019	Sheet 61 of 100	

Main Board

GPU POWER GOOD Signal

NVVDD POWER GOOD LOOPBACK

GPU POWER SEQUENCE CONTROL

PCI EXPRESS_Graphics

REVERSED Type PCIE X16

Reverse PCIEG x 8

teknisi-indonesia

Optimus

DGPU_PWR_EN#	FUNCTION
H	GC OFF
L	GC ON

iGPU_dGPU_switch	FUNCTION
H	dGPU Mode
L	iGPU Mode

For GC OFF & GC6 notify EC

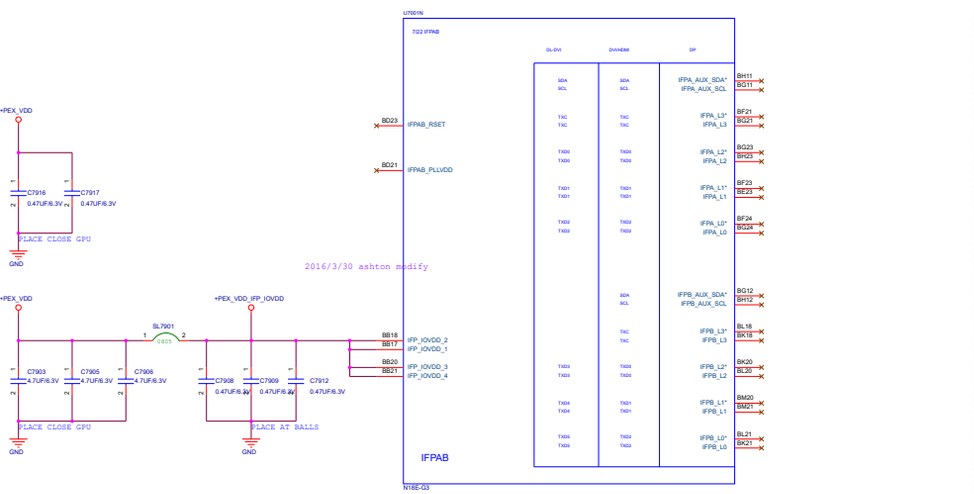
For EMI

PLACE OUTSIDE OF BGA

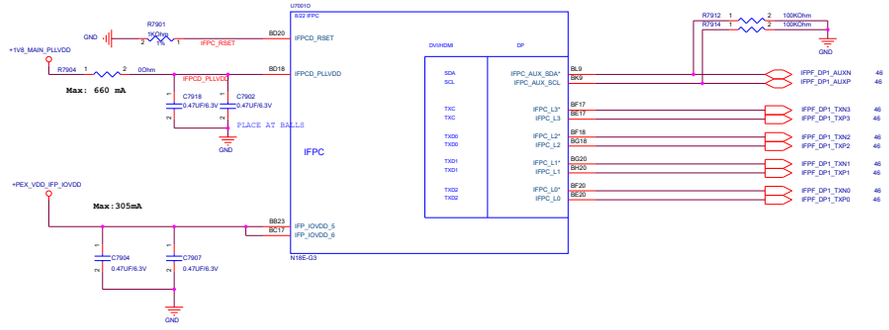
PLACE AT BALLS

Project Name	GX701
Title :	GPU_PCIE I/F
Dept.:	Engineer: EE

Main Board

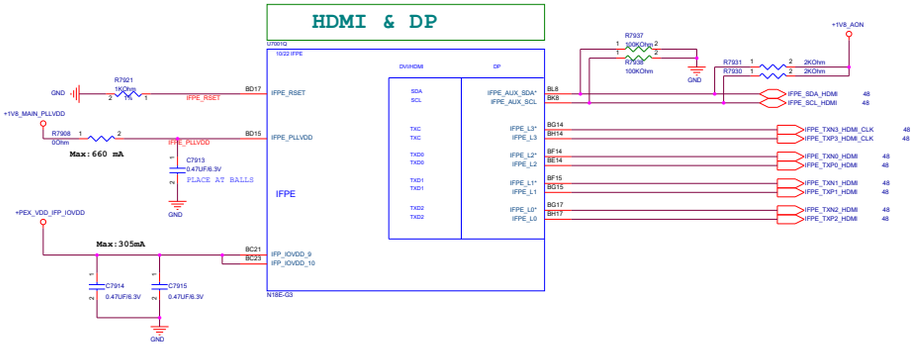


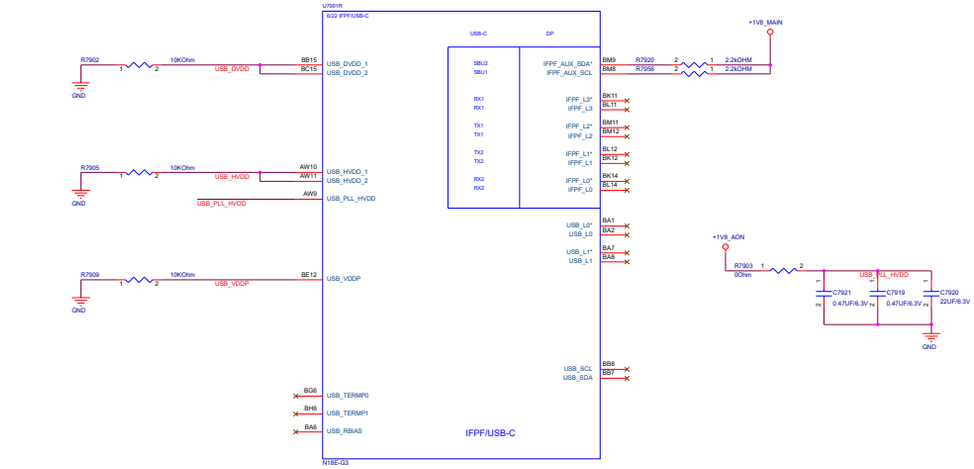
DP(Type-C)

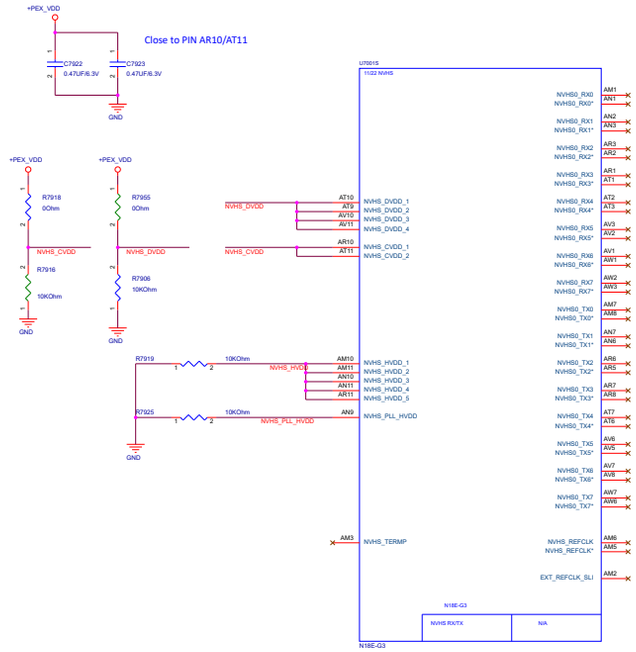


EDP(4Lane Panel)

HDMI & DP

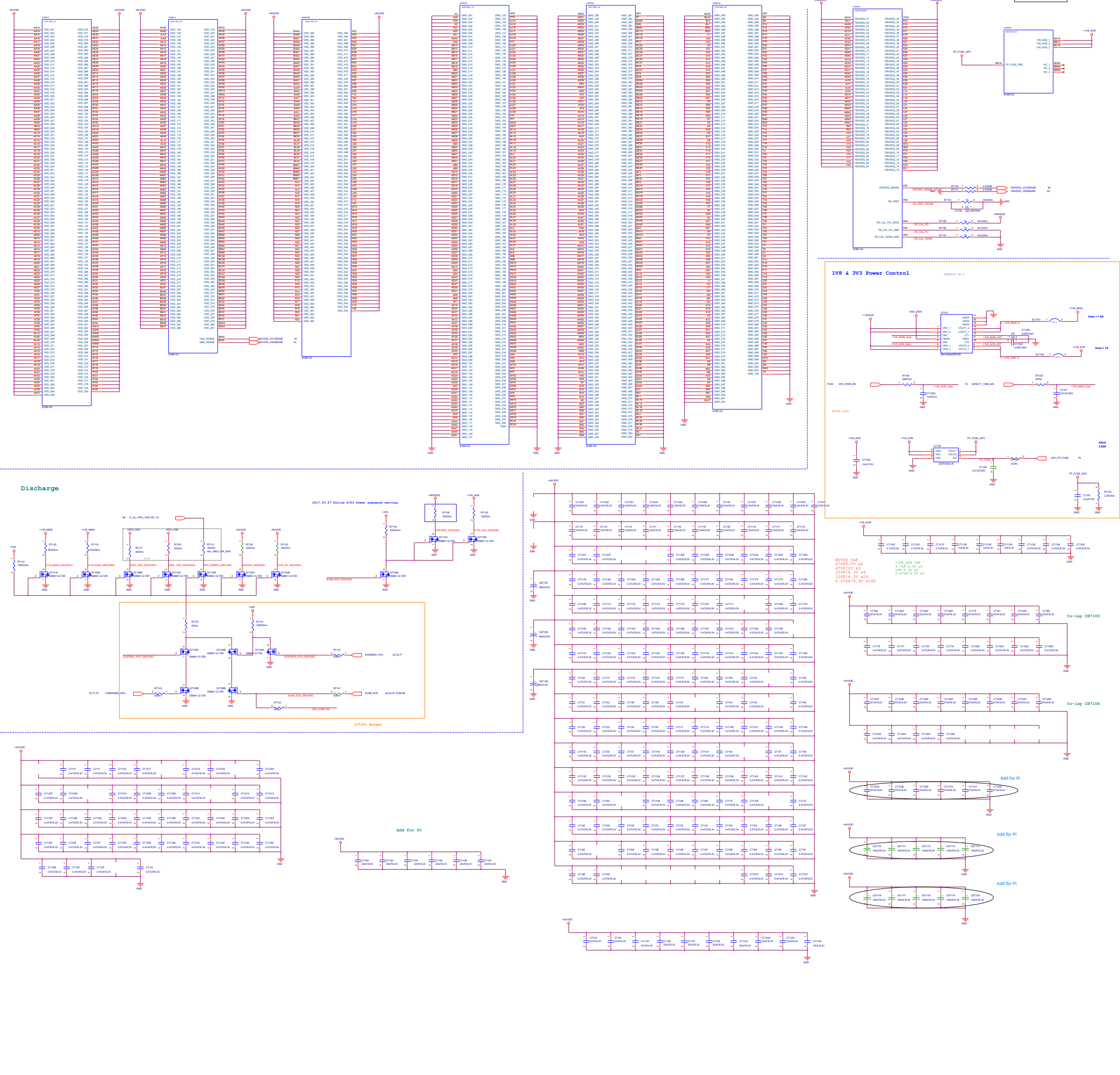






ASUS	Project Name: GX701		Rev: 2.0
Title : GPU_DP/EDP/HDMI			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet: 79	of: 100	

Main Board



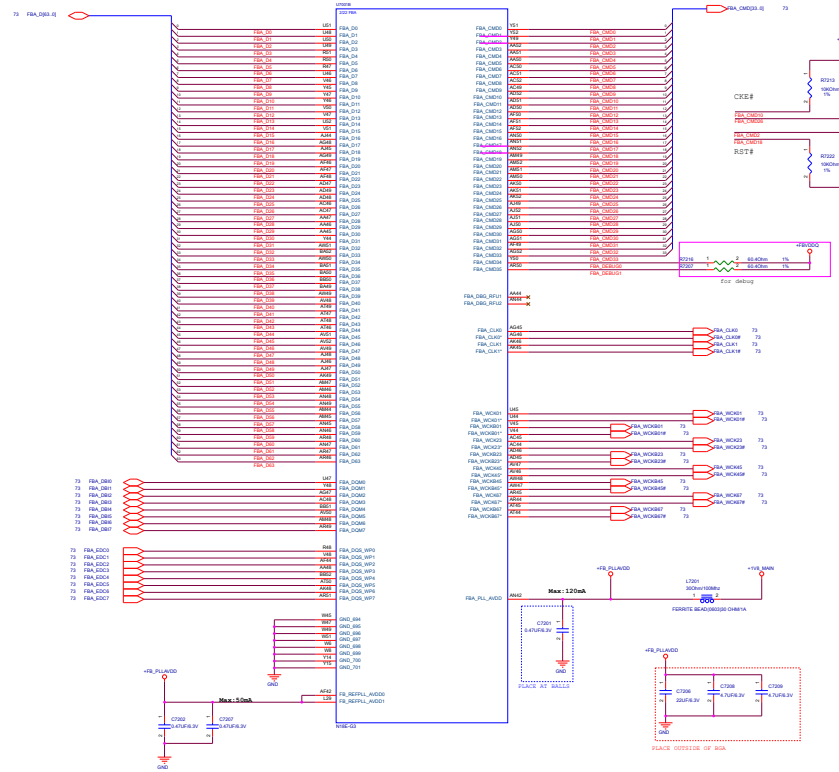
Title : GPU_POWER

Project Name: GX701

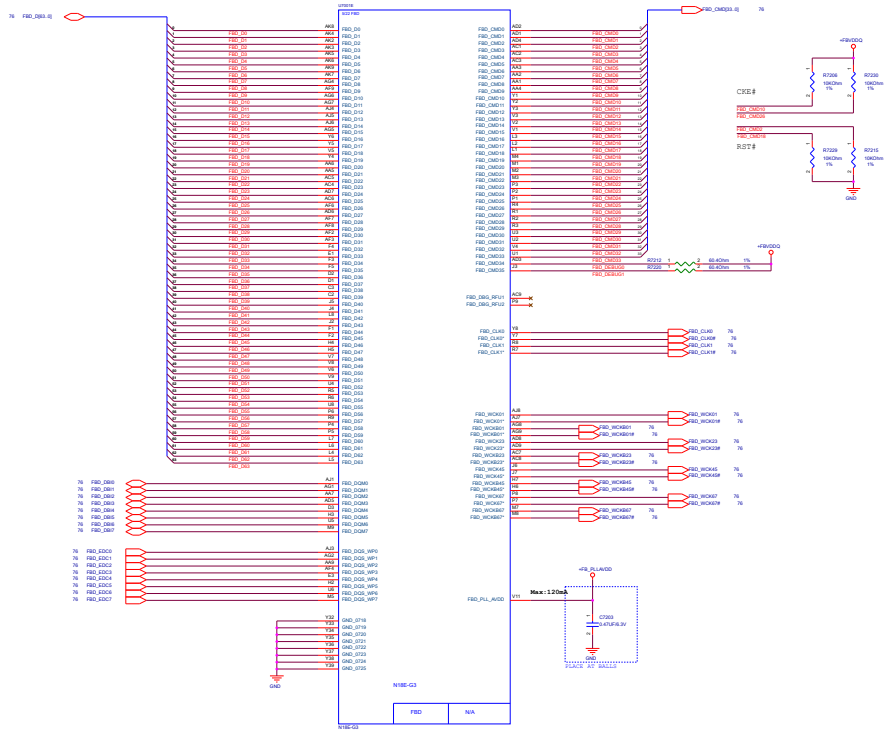
Dept.: ASUSTeK COMPUTER INC.

Engineer: EE

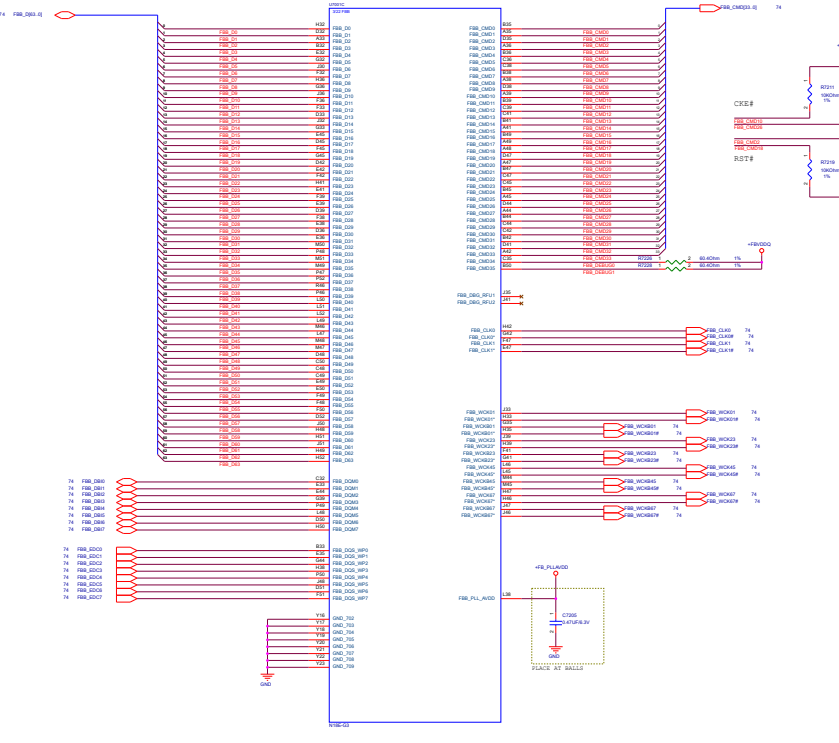
MEMORY: GPU FB Partition A



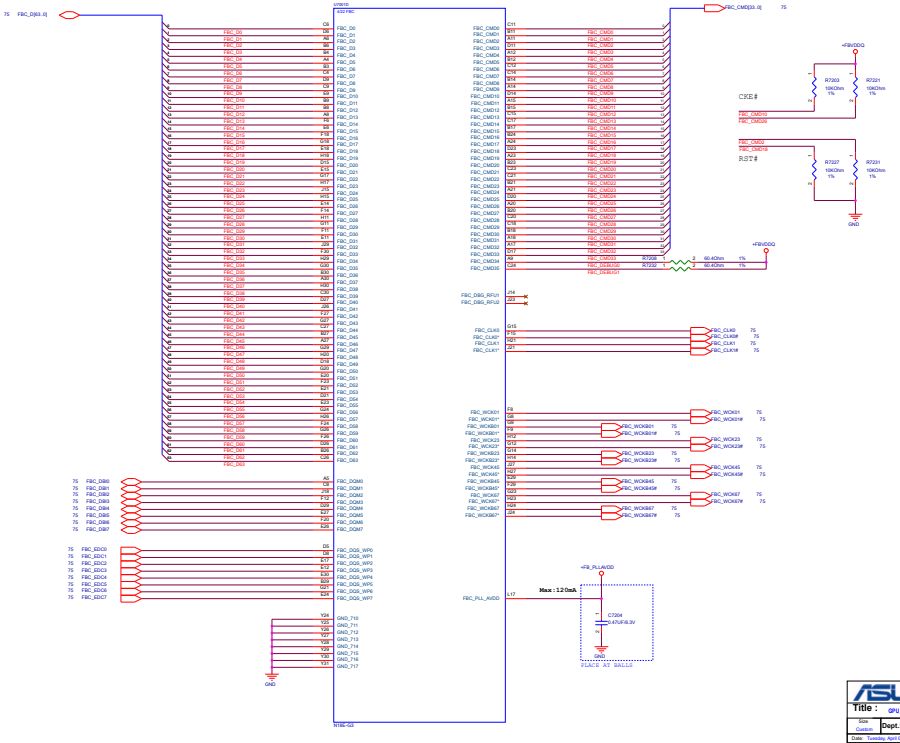
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B



MEMORY: GPU FB Partition C



ASUS	Project Name: GX701		Rev: 81.0
Title :	GPU_FRAME BUFFER		
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Tuesday, April 02, 2019	Sheet 72 of 100		

<Variant Name>

Title : <Title>

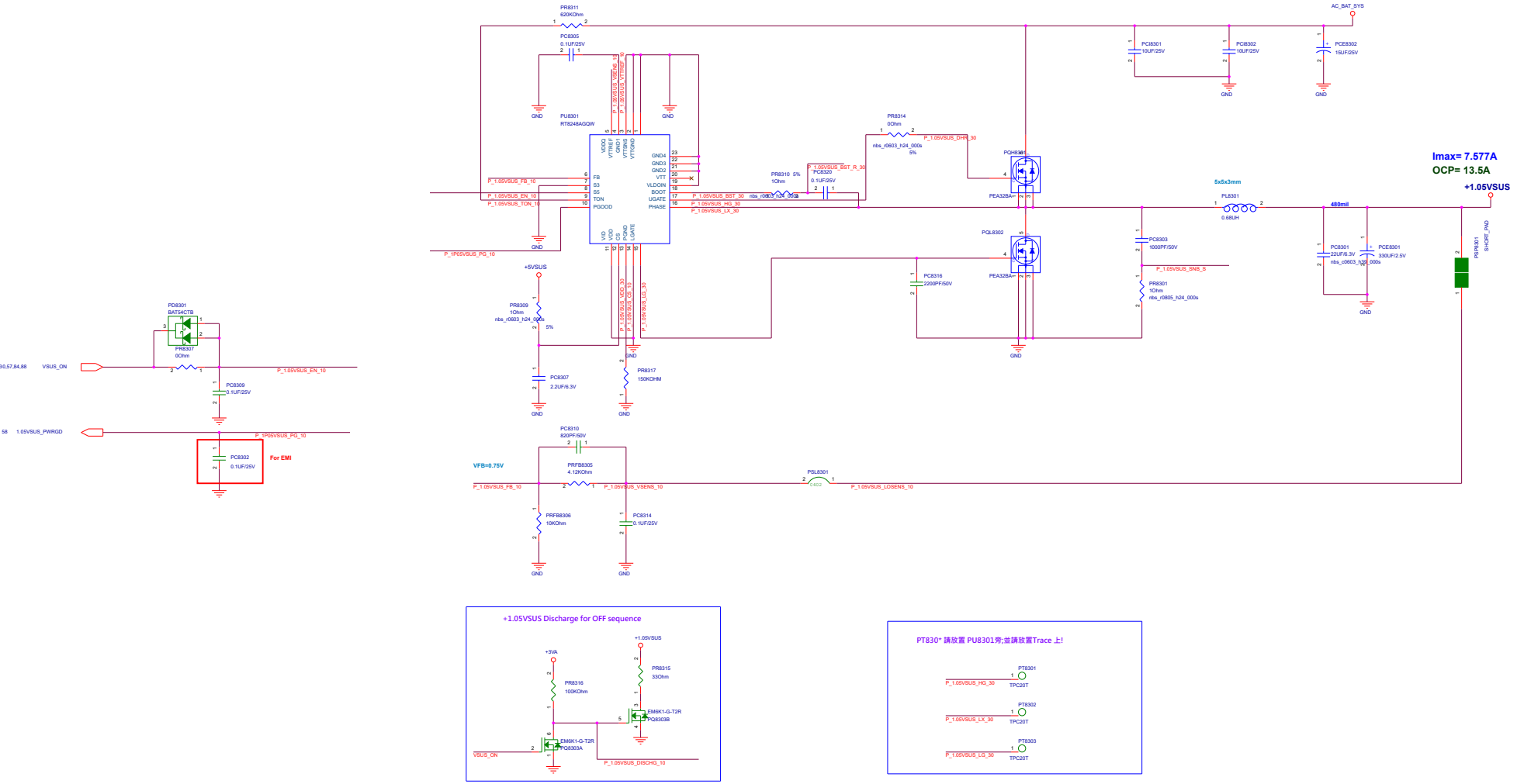
ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size	Project Name	Rev
D	GX701	1.0

Date:	Wednesday, March 06, 2019	Sheet	82	of	103

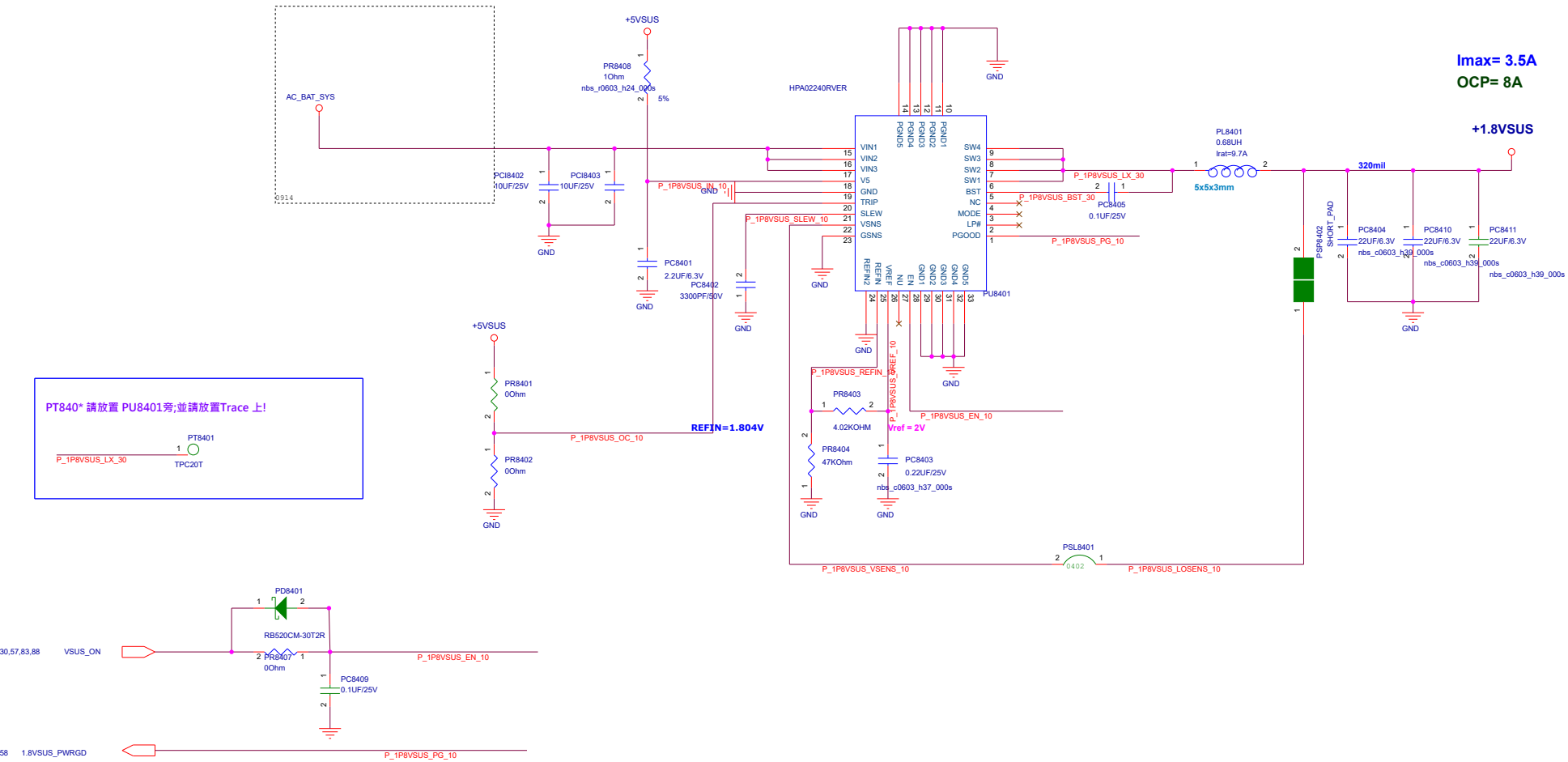
+1.05VSUS [For PCH]



<variant_name>

ASUS	Project Name: GX701		Rev: R1.0
Title : PW_+1.0VSUS			
Size: A2	Dept.: NB Power team	Engineer: Power	
Date: Tuesday, April 02, 2019	Sheet 83 of 100		

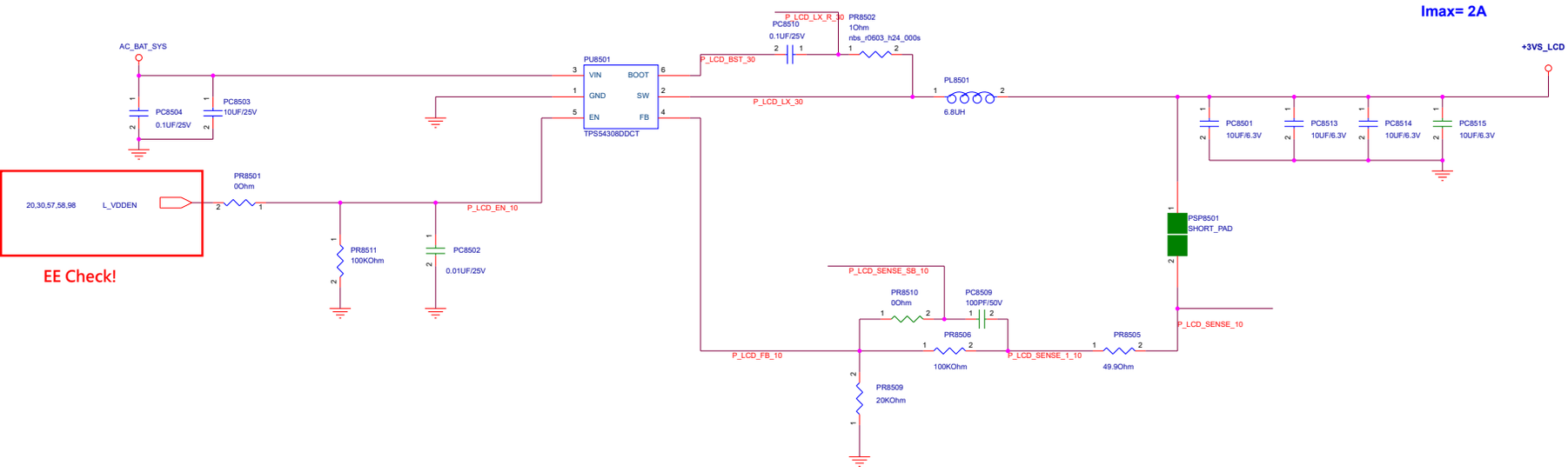
+1.8VSUS [For PCH]



<Variant Name>

ASUS	Project Name: GX701	Rev: R1.0
Title : PW_+1.8VSUS		
Size: A3	Dept.: NB Power team	Engineer: Power
Date: Tuesday, April 02, 2019	Sheet 84 of 100	

+3VS_LCD



<Variant Name>

ASUSTeK COMPUTER INC. NB1

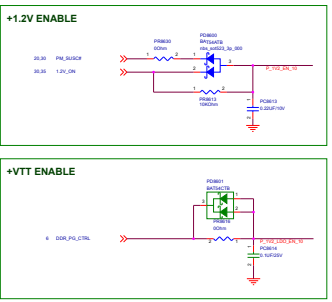
Title : <Title>

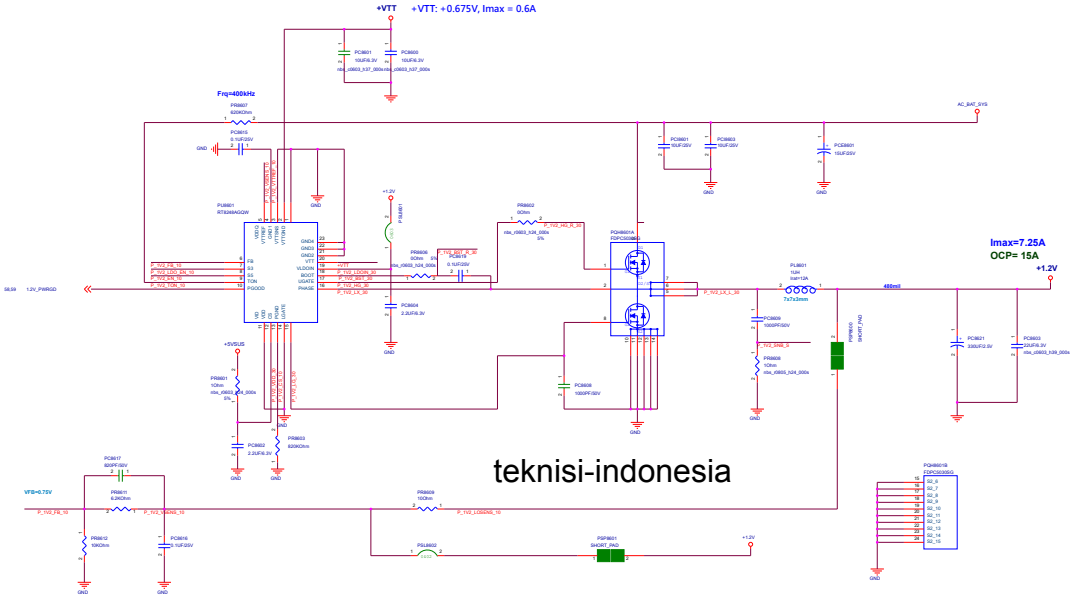
Engineer: EE

Size	Project Name	Rev
C	GX701	1.0

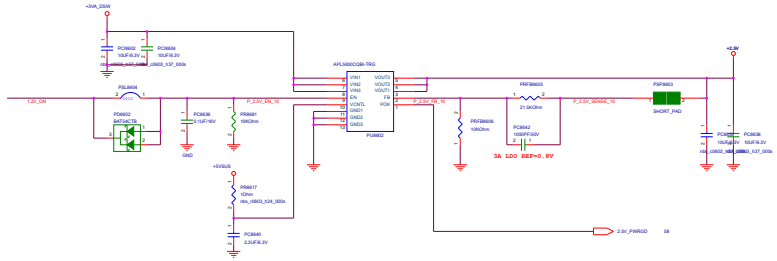
Date: Tuesday, April 02, 2019 Sheet 85 of 103

+1.2V / +VTT [For Memory]





+2.5V LDO [For Menory]



ASUS	Project Name: GX701		Rev: 1.0
Title : PW_+1.2V/+VTT/+2.5V			
Size: A3	Dept.: ASUSTeK COMPUTER INC.	Engineer: Power	
Date: Tuesday, April 02, 2019	Sheet: 46 of 150		

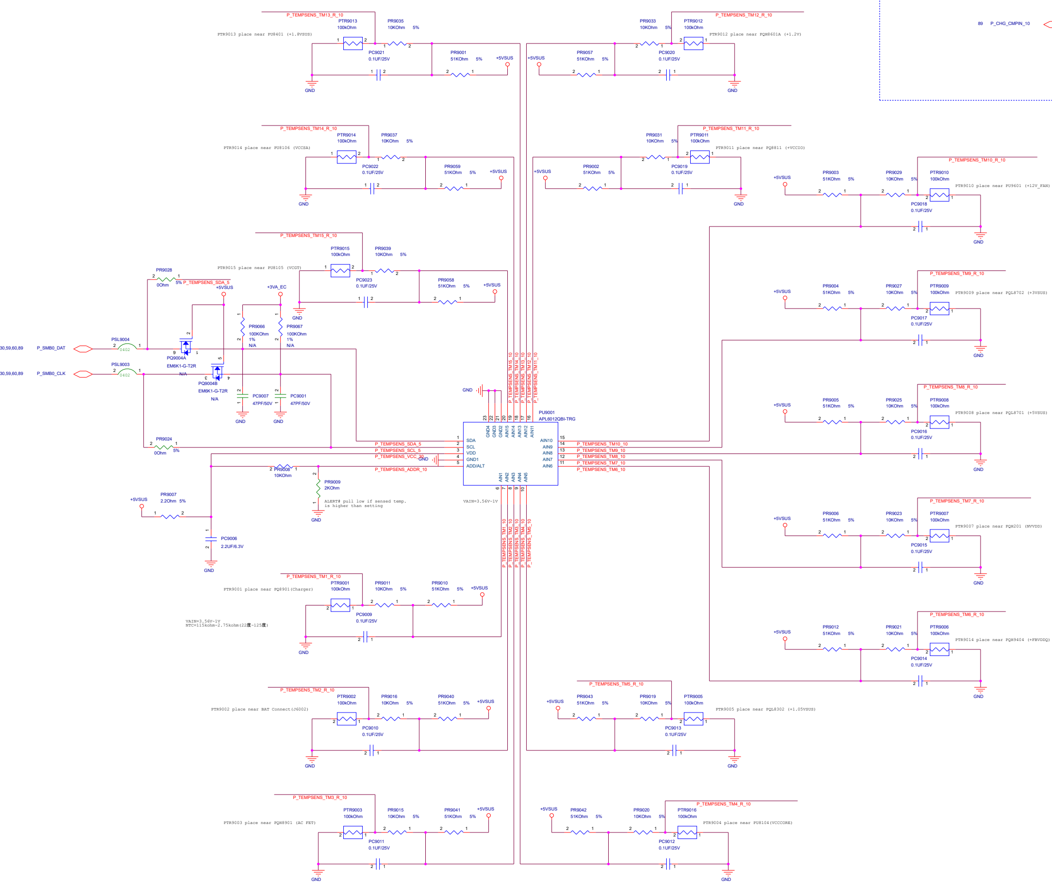
Address Selection Table

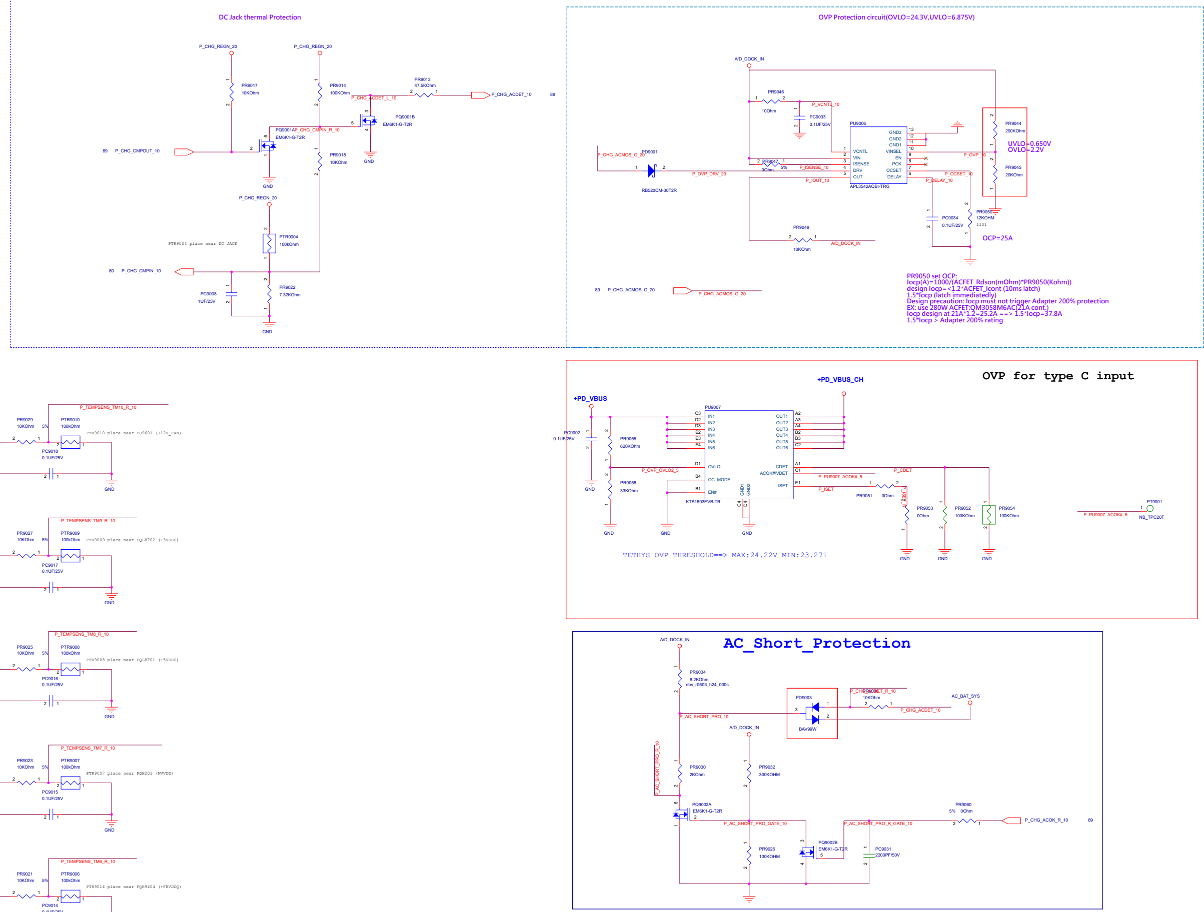
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	150k	200k	360k	390k	430k	510k	600k
PR9002	Open	820k	620k	680k	470k	360k	270k	200k

Register Address

Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

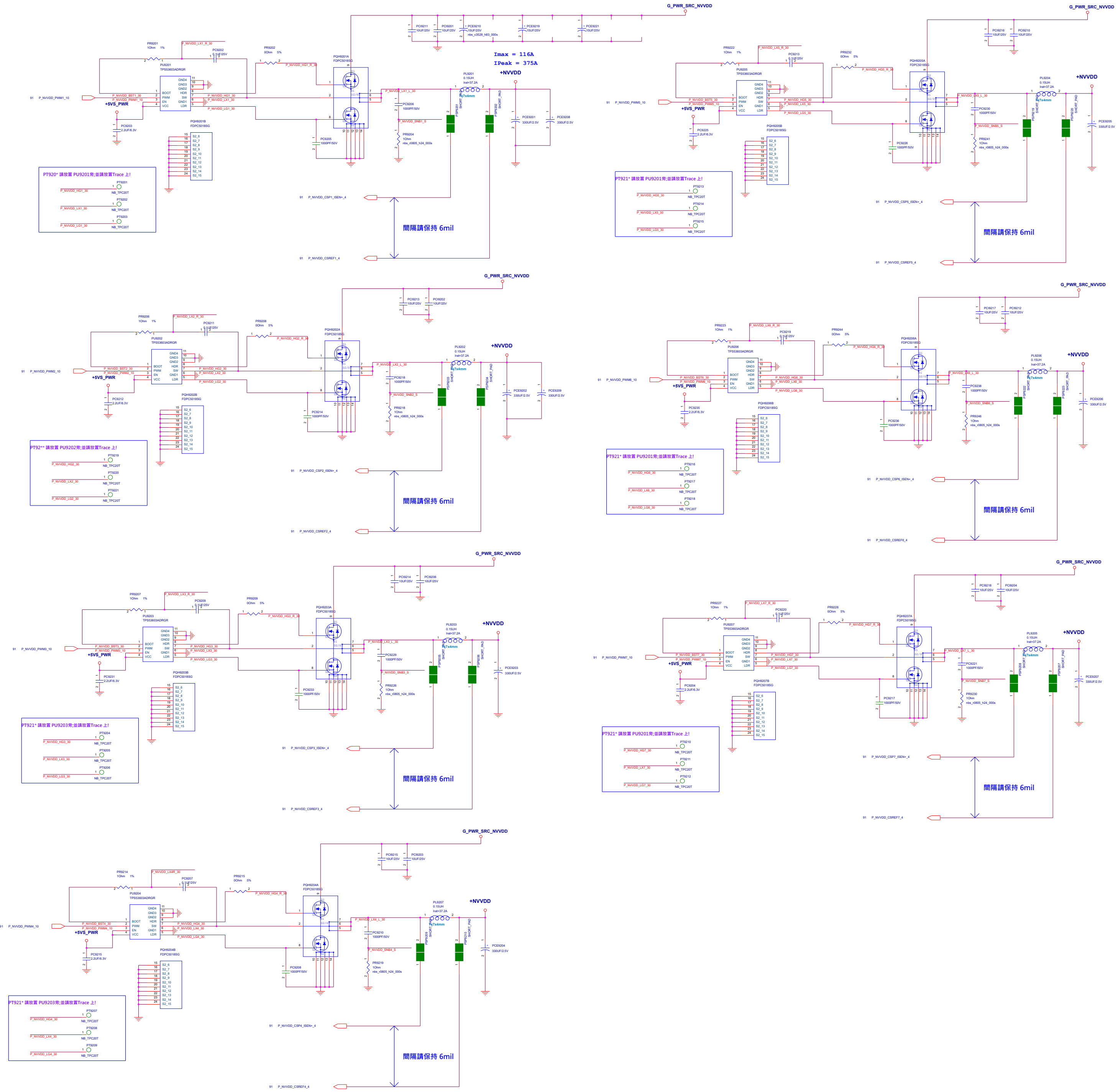
PROTECTION





DC Jack thermal Protection
PTR9004 place near DC JACK
OVP Protection circuit(OVLO=24.3V,UVLO=6.875V)
UVLO=0.650V
OVLO=2.2V
OCP=25A
PR9050 set OCP:
Iocp(A)=1000/(ACFET_Rdson(mOhm)*PR9050(Kohm))
design Iocp=<1.2*ACFET_Icont (10ms latch)
1.5*Iocp (latch immediately)
Design precaution: Iocp must not trigger Adapter 200% protection
EX: use 280W ACFET:QM3058M6AC(21A cont.)
Iocp design at 21A*1.2=25.2A ==> 1.5*Iocp=37.8A
1.5*Iocp > Adapter 200% rating
OVP for type C input
+PD_VBUS
+PD_VBUS_CH
TETHYS OVP THRESHOLD==> MAX:24.22V MIN:23.27I
AC_Short_Protection

+NVVDD [For DGPU]



<Core Design>

ASUS	Project Name: GX701	Rev: R1.0
Title : PW_+NVVDD (2)		
Size: A0	Dept.: NB Power team	Engineer: Power
Date: Tuesday, April 02, 2019	Sheet 92	of 103

+FBVDDQ [For VRAM]

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
PR9404	10KOhm	
PR9409	21.5KOhm	
PR9423	75KOhm	

PTR9401 close to PQH9401

PT940* 請放置 PU9401旁;並請放置Trace 上!

Imax= 68A
OCP= 100A

R1.1: EE request change to H = 1.5mm due to H limitation

Project Name	GX701
Title :	PW_+FBVDDQ
Dept.:	NB Power Team
Engineer:	Power

<Variant Name>

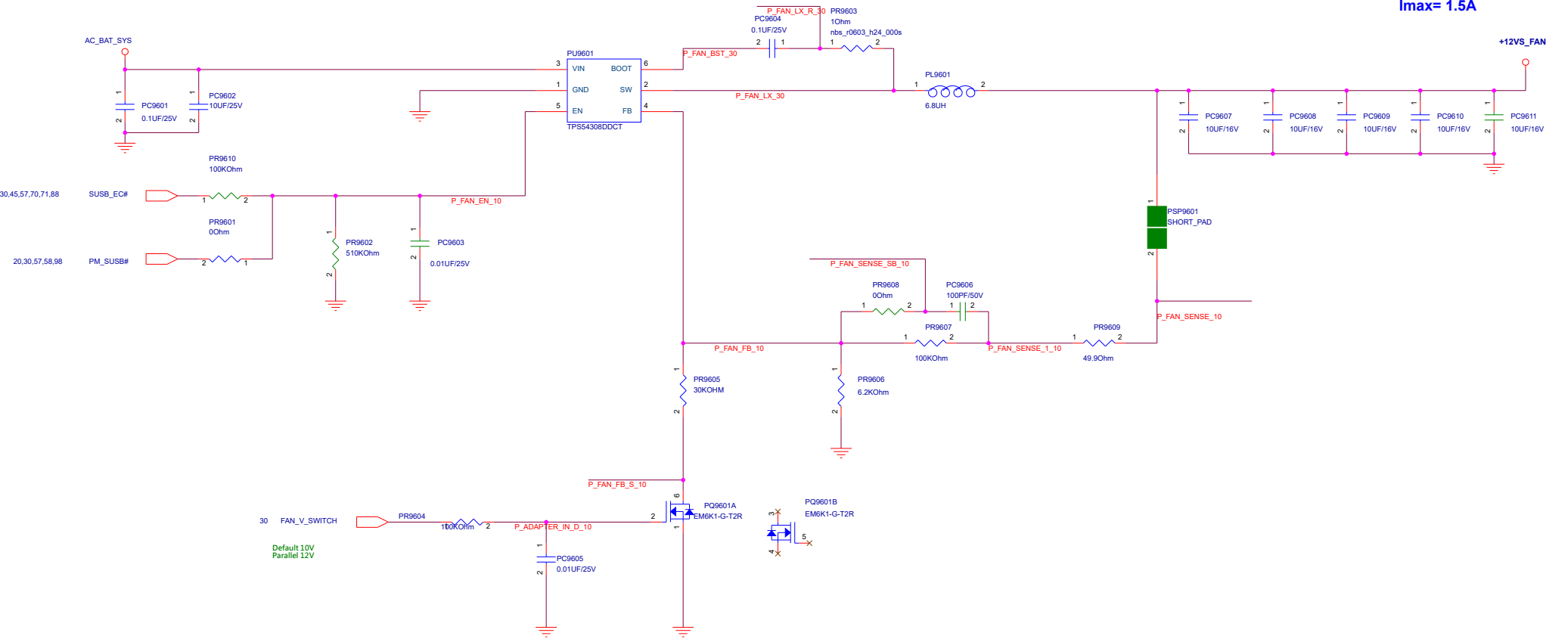
Title : <Title>

ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size	Project Name	Rev
D	**GX701**	1.0

Date:	Wednesday, March 06, 2019	Sheet	95	of	103



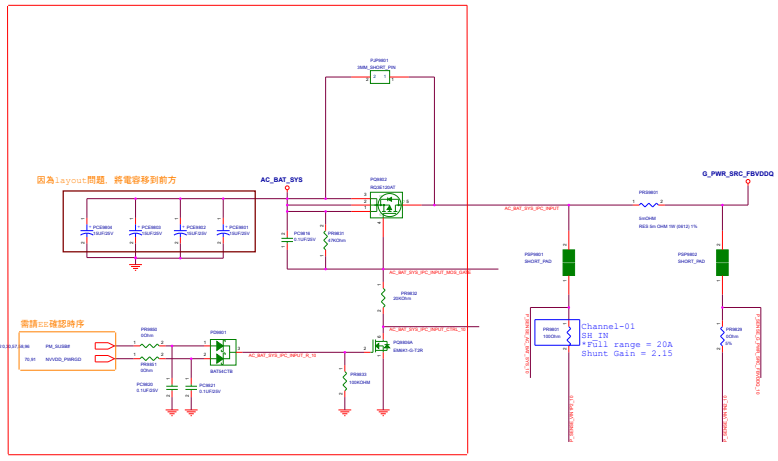
<Variant Name>

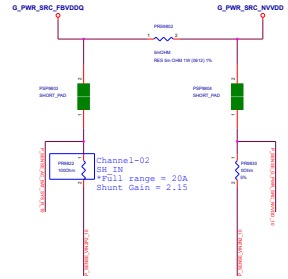
ASUS	Project Name: GX701	Rev: R1.0
Title : PW_+12VS_FAN		
Size: B	Dept.: NB Power team	Engineer: Power
Date: Tuesday, April 02, 2019	Sheet 96 of 100	

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : <Title>	
	Engineer: EE	
Size: D	Project Name: GX701	Rev: 1.0
Date: Wednesday, March 06, 2019	Sheet 97 of 103	

UPI / ON 時序Issue預留Option線路(Short Term Solution)
SS : 103us ~ 275us
OFF : 8.1ms ~ 12.4ms
Default 上short pin

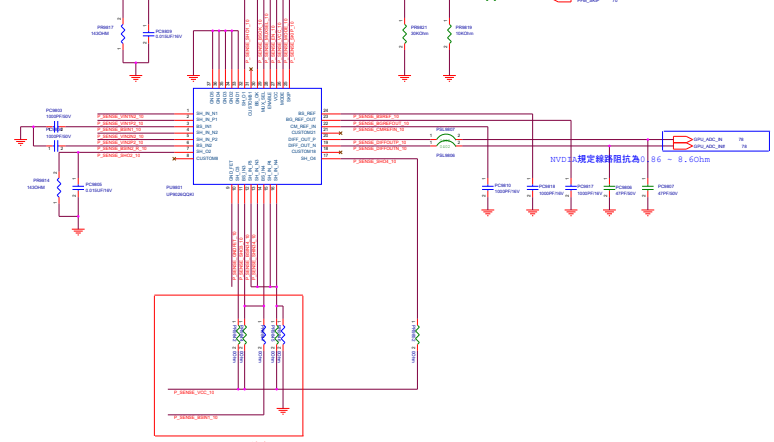




請和EE確認EE端是否有畫對應線路、pull high

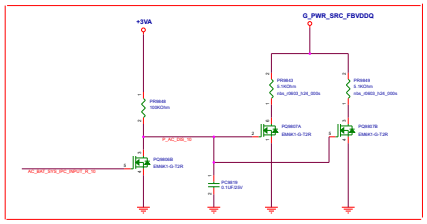
UPI / ON 時序Issue預留Option線路(Short Term Solution)

怕3VA_LDO被抽均預留線路
(PR9840上件時，PR9820需不上件)

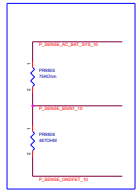


UPI / ON Co-Layout線路

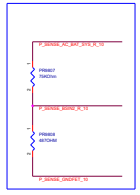
AC_BAT_SYS_Discharge線路
T-Discharge : 0.626s(Worst case 10 Phase)



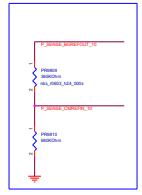
Channel-01
BS_IN
*Full range = 19V
Bus Gain = 6.4514m



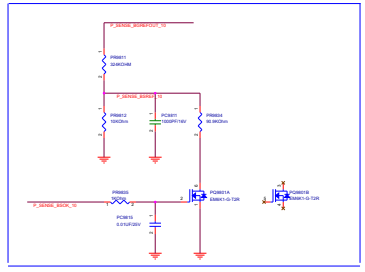
Channel-02
BS_IN
*Full range = 19V
Bus Gain = 6.4514m



CM_REF_IN
*0.85V(實際0.8459V)



BS_REF
*6.0331V、5.4514V(此值需小於19V、BAT電壓)



N18E

150W+

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100Ω(10G212100014010)	
PR9817	127Ω (10G212127014010)	169Ω (10G212169014010)
PR9822	100Ω(10G212100014010)	
PR9814	127Ω (10G212127014010)	169Ω (10G212169014010)
PR9805	75kΩ(10G212750214010)	
PR9806	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9807	75kΩ(10G212750214010)	
PR9808	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9811	324kΩ (10G212324314010)	243kΩ (10G212243314010)
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

115W ~ 130W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	143Ω (10G212143014010)	191Ω (10G212191014010)
PR9814	143Ω (10G212143014010)	191Ω (10G212191014010)

100W ~ 110W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	165Ω (10G212165014010)	221Ω (10G212221014010)
PR9822		
PR9814	165Ω (10G212165014010)	221Ω (10G212221014010)

75W ~ 90W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	215Ω (10102-00571000)	287Ω (10G212287014010)
PR9822		
PR9814	215Ω (10102-00571000)	287Ω (10G212287014010)

75W-

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9817	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9822		
PR9814	357Ω (10G212357014010)	475Ω (10G212475014010)

N18P

75W-

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	100Ω(10G212100014010)	
PR9817	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9822	100Ω(10G212100014010)	
PR9814	357Ω (10G212357014010)	475Ω (10G212475014010)
PR9805	75kΩ(10G212750214010)	
PR9806	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9807	75kΩ(10G212750214010)	
PR9808	487Ω (10G212487014010)	649Ω (10G212649014010)
PR9811	324kΩ (10G212324314010)	243kΩ (10G212243314010)
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

150w+

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G212200014010)	
PR9817	127Ω (10G212127014010)	
PR9822	200Ω(10G212200014010)	
PR9814	127Ω (10G212127014010)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

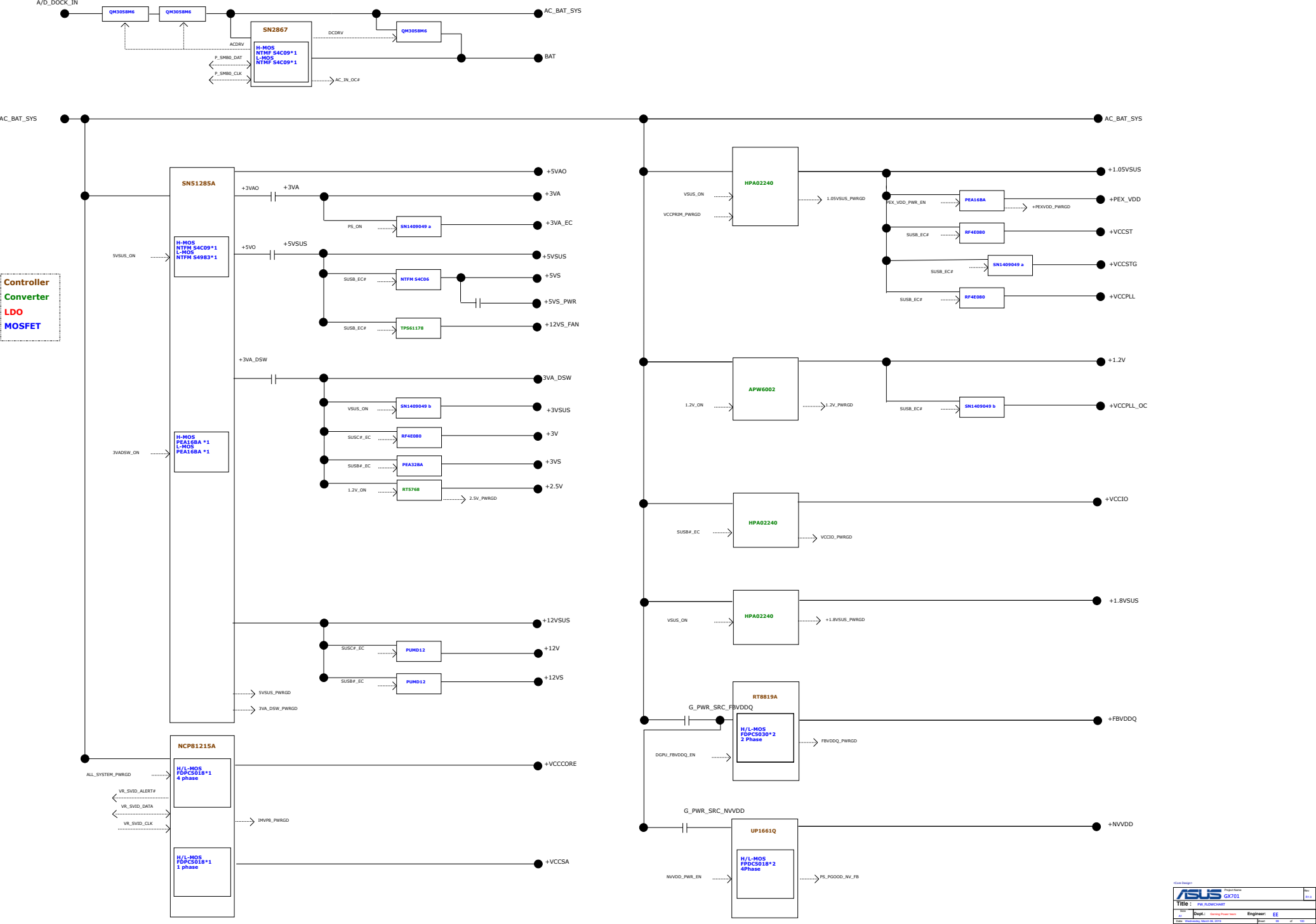
115W ~ 130W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G212200014010)	
PR9817	143Ω (10G212143014010)	
PR9822	200Ω(10G212200014010)	
PR9814	143Ω (10G212143014010)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

75W ~ 90W

	UP9026PQKI (UPI)	NCP45491 (ON)
PR9801	200Ω(10G212200014010)	
PR9817	215Ω (10102-00571000)	
PR9822	200Ω(10G212200014010)	
PR9814	215Ω (10102-00571000)	
PR9805	33kΩ (10G212330214010)	
PR9806	431Ω (10102-00581000)	
PR9807	33kΩ (10G212330214010)	
PR9808	431Ω (10102-00581000)	
PR9811	324kΩ (10G212324314010)	
PR9812	10kΩ(10G212100214010)	
PR9834	90.9kΩ(10G212909214010)	

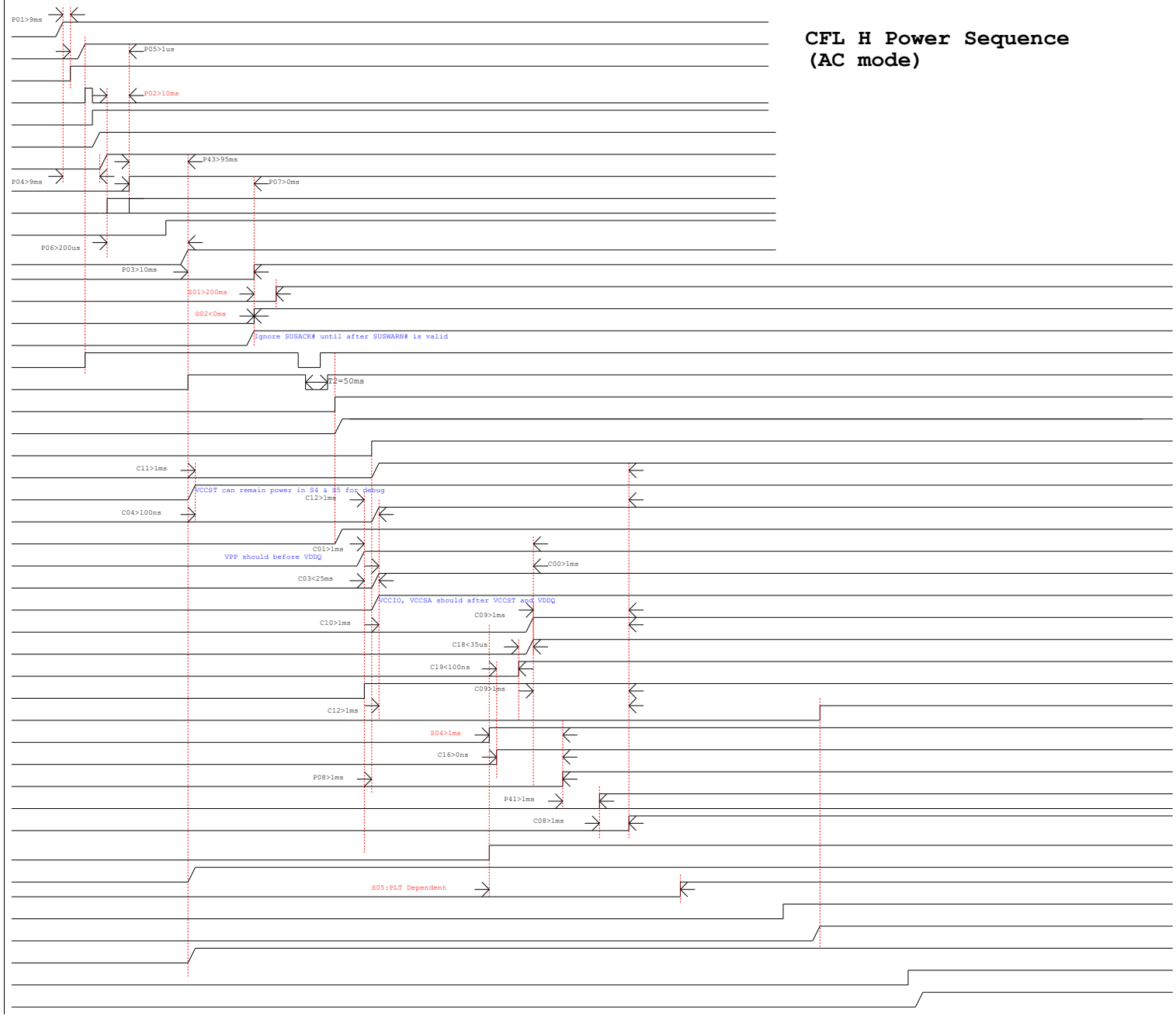
ASUS	Project Name: GX701		Rev: R1.0
Title : PW_IPC			
Size: Custom	Dept.: Power Team	Engineer: Power	
Date: Tuesday, April 02, 2019	Sheet: 98 of 102		


A/D_DOCK_IN
QM30S8M6
QM30S8M6
SN2867
H-MOS
NTMF S4C09*1
L-MOS
NTMF S4C09*1
ACDRV
DCDRV
P_SMB0_DAT
P_SMB0_CLK
AC_IN_OC#
QM30S8M6
AC_BAT_SYS
BAT
AC_BAT_SYS
SN51285A
H-MOS
NTFM S4C09*1
L-MOS
NTFM S4983*1
SVSUS_ON
H-MOS
PEA168A *1
L-MOS
PEA168A *1
3VADSW_ON
+3VAO
+3VA
+5VO
+5VSUS
+3VA_DSW
+5VAO
+3VA
PS_ON
SN1409049 a
+3VA_EC
+5VSUS
SUSB_EC#
NTFM S4C06
+5VS
+5VS_PWR
SUSB_EC#
TPS61178
+12VS_FAN
3VA_DSW
VSUS_ON
SN1409049 b
+3VSUS
SUSC#_EC
RF4E080
+3V
SUSB#_EC
PEA328A
+3VS
1.2V_ON
RT5768
2.5V_PWRGD
+2.5V
+12VSUS
SUSC#_EC
PUMD12
+12V
SUSB#_EC
PUMD12
+12VS
SVSUS_PWRGD
3VA_DSW_PWRGD
NCP81215A
H/L-MOS
FDPC5018*1
4 phase
ALL_SYSTEM_PWRGD
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
IMVP8_PWRGD
H/L-MOS
FDPC5018*1
1 phase
+VCCCORE
+VCCSA
Controller
Converter
LDO
MOSFET
AC_BAT_SYS
HPA02240
VSUS_ON
VCCPRIM_PWRGD
1.05VSUS_PWRGD
+1.05VSUS
PEX_VDD_PWR_EN
PEA168A
+PEXVDD_PWRGD
+PEX_VDD
SUSB_EC#
RF4E080
+VCCST
SUSB_EC#
SN1409049 a
+VCCSTG
SUSB_EC#
RF4E080
+VCCPLL
APW6002
1.2V_ON
1.2V_PWRGD
+1.2V
SUSB_EC#
SN1409049 b
+VCCPLL_OC
HPA02240
SUSB#_EC
VCCIO_PWRGD
+VCCIO
HPA02240
VSUS_ON
+1.8VSUS_PWRGD
+1.8VSUS
RT8819A
G_PWR_SRC_FBVDDQ
H/L-MOS
FDPC5030*2
2 Phase
FBVDDQ_PWRGD
+FBVDDQ
DGPU_FBVDDQ_EN
G_PWR_SRC_NVVDD
UP1661Q
H/L-MOS
FDPC5018*2
4Phase
NVVDD_PWR_EN
PS_PGOOD_NV_FB
+NVVDD
<Core Design>
Project Name
GX701
Title : PW_FLOWCHART
Dept.: Gaming Power team
Engineer: EE
Date: Wednesday, March 06, 2019
Sheet 90 of 100

AC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(SUSB_EC#) +1.0V_VCCST, VCCPLL
(SUSB_EC#) +VCCIO, (+12VS) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



CFL H Power Sequence (AC mode)

ASUS	Project Name: GX701		Rev: R1.0
Title : Power On Timing--AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Wednesday, March 06, 2019	Sheet 100 of 100		

Rev	Date	Description
1.0	2017.03.03	P21 Remove CN
	2017.03.04	Q5602, Q5601 change for DXF Limitation
	2017.03.10	+1V9_MAIN, +3VS_NV Follow G753 Power sequence setting
	2017.03.11	R7821 Follow GL702 GPU Power seq
	2017.03.11	+PEX_VDD GPU Sequence update
	2017.03.14	PCE8104, PCE8107, PCE8106 update Cap for DXF Limit
	2017.03.14	GX501VIK Remove useless nut in P67
	2017.03.15	J5301 Connector list update
	2017.03.15	H6716, H6706, H6724, H6723 Screw Hole update
	2017.03.16	J5602 change LID SW for Angle Simulation
	2017.03.17	EMI Reserve C5606, C5607 Cap
	2017.03.17	RM3002, L4512, L4513, L4504, L4515, L4505 SWAP for Layout
1.1	2017.03.21	P30, P37, P39 AMP Change SNL04M25555
	2017.03.21	EMI Reserve P30 C77360 Cap and P69 Caps and Spring
	2017.03.23	AMP Change Remove P37 MUTE CONTROL schematic
	2017.03.23	AMP Change Reserve Q3701
	2017.03.27	P71 +PBVDDQ Discharge setting Follow G753 Power sequence setting
	2017.03.29	P12 Remove TBT Power Low Switch for Layout
1.2	2017.03.30	Change Cap C7105, C7101 for thermal request
	2017.03.30	Thermal Request for H6728
	2017.04.05	EMI Reserve Cap and Spring in P69
	2017.04.06	Reserve C2601 for +VCCPGPP_EF Ripple
	2017.04.07	25.00MHZ Cap C1126, C1124 change for Vendor Suggest
	2017.04.07	27MHz Cap C7811, C7801 change for Vendor Suggest
2.0	2017.04.11	P48 Reserve 0 ohm for SDA and SCL
	2017.04.17	P71 Add Caps for NVVDD Ripple
	2017.04.18	Q5704 Chnage MOS for DXF Limitation
	2017.04.20	P71 Add Caps for NVVDD Ripple
	2017.04.21	P67 Screw Hole H6705 update
	2017.04.21	P71 Add Caps for NVVDD Ripple C71119~C71122
	2017.04.25	P71 C7122, C7123, C7127, C7135, C7143, C7144, C7156, C7164, C7166,, C7186, C7187 change to 10UF
	2017.04.25	P70 C7007, C7002 change to 4.7UF
	2017.04.25	P70 C7020, C7024 change to 22UF
	2017.05.02	EMI Reserve C6948, C6949, C6950, C6951, C6952, C6953, C6954 and remove U6913
	2017.05.02	H6711, H6712 change screw hole type fot EMI Solution
	2017.05.03	Remove J4502 Pin 36 GND fot Factory Issue
	2017.05.05	P88, P58 Remove VCCST_PWRGD signal
	2017.05.05	P79, P45 Remove eDP Lan2 and Lan3 Signal
	2017.08.10	P31 R3121,R3122 change to unmount

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK COMPUTER

Title : Revision History

Engineer: EE

Size: D | Project Name: GX701 | Rev: 1.0

Date: Wednesday, March 29, 2017 | Sheet 102 of 105

GX501VSK R2.0 SKU Table

			CPU	Power	DIMM	VRAM			
Option	PCB	SKU							
60NB0H10-MB1030	R2.0	GX501VSK SKU1	/I7-7700HQ	/230W	8G_Hynix	V8G_Samsung			
60NB0H10-MB2000	R2.0	GX501VSK SKU2	/I5-7300HQ	/230W	8G_Hynix	V8G_Samsung			

1. CPU: INT I7-7700HQ 2.8G/6M SR32Q BGA 01001-01380600
CPU: INT I5-7300HQ 2.5G/6M SR32S BGA 01001-01380500

2. dGPU: nVidia N17E-G2-A1 FCBGA2152 02004-00480500

4. EC: ITE IT8995VG-128/DX --06037-00050800

5.onboard menory
8G_ Hynix 03012-00030400

9. Card Reader: AU6435--02G630002400 (Page42)

10. USB Charger IC: (Page52) Silego SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011

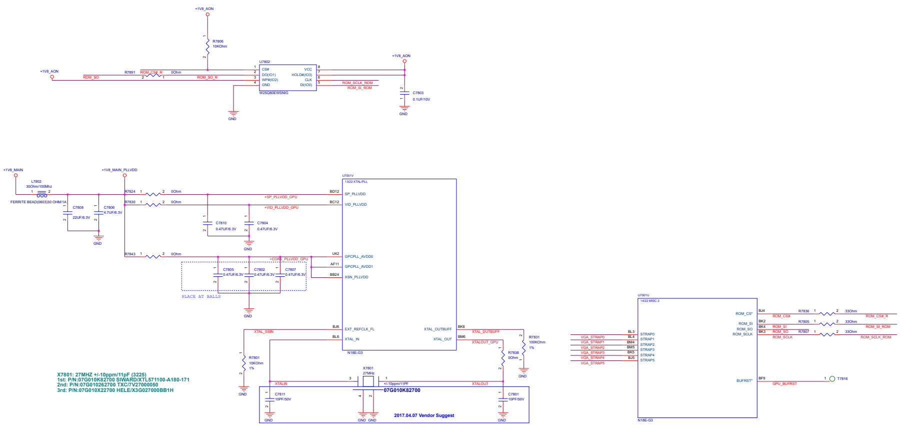
11. USB3.0 Repeater IC:(Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000

13. Audio Codec : 02043-00130000 (663-VA4)

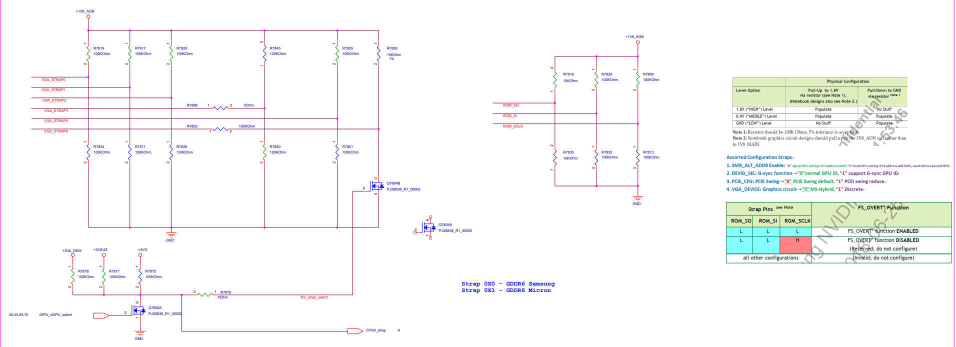
<Variant Name>

Title : UX362_SKU Table_R1.0
Engineer: EE
Size: C | Project Name: GX701 | Rev: R1.0
Date: Wednesday, March 08, 2017 | Sheet of

Channel A
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
Channel B
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
Channel C
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
Channel D
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
Close to DRAM
0.47uF x 36pcs
10uF x 4pcs
Around DRAM
22uF x 6pcs
10uF x 2pcs
Close to DRAM
0.47uF x 4pcs
4.7uF x 1pcs
VRAM PWR_FBVDDQ
Partition A
under GPU
0.47uF x 12pcs
10uF x 2pcs
Partition B
under GPU
0.47uF x 12pcs
10uF x 1pcs
Partition C
under GPU
0.47uF x 12pcs
10uF x 1pcs
Partition D
under GPU
0.47uF x 12pcs
10uF x 1pcs
Close GPU
10uF x 7pcs
22uF x 9pcs
Close GPU
Near U76001
Add for PI
For power sequence measurement
Address Selection Table
GL702VSK UP1905
移至 Page 50
GDDR5X VPP power +1.8V



STRAP PIN



Strap Pins (see Note)			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins (see Note)			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Strap Pins (See Note)			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is eDP Supported on: IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	See This Row of Table 5.4
4	4	--	--	--	15
4	3	yes	--	--	14
4	3	--	yes	--	13
4	3	--	--	yes	11
3	3	--	--	--	14
3	2	yes	--	--	12
3	2	--	yes	--	12
3	2	--	--	yes	10
2	2	--	--	--	12
2	1	yes	--	--	8
2	1	--	yes	--	8
2	1	--	--	yes	8
1	1	--	--	--	8
1	0	yes	--	--	0
1	0	--	yes	--	0
1	0	--	--	yes	0

Level Option	Physical Configuration: Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.)	Pull-Down to GND via resistor (Note 1)
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

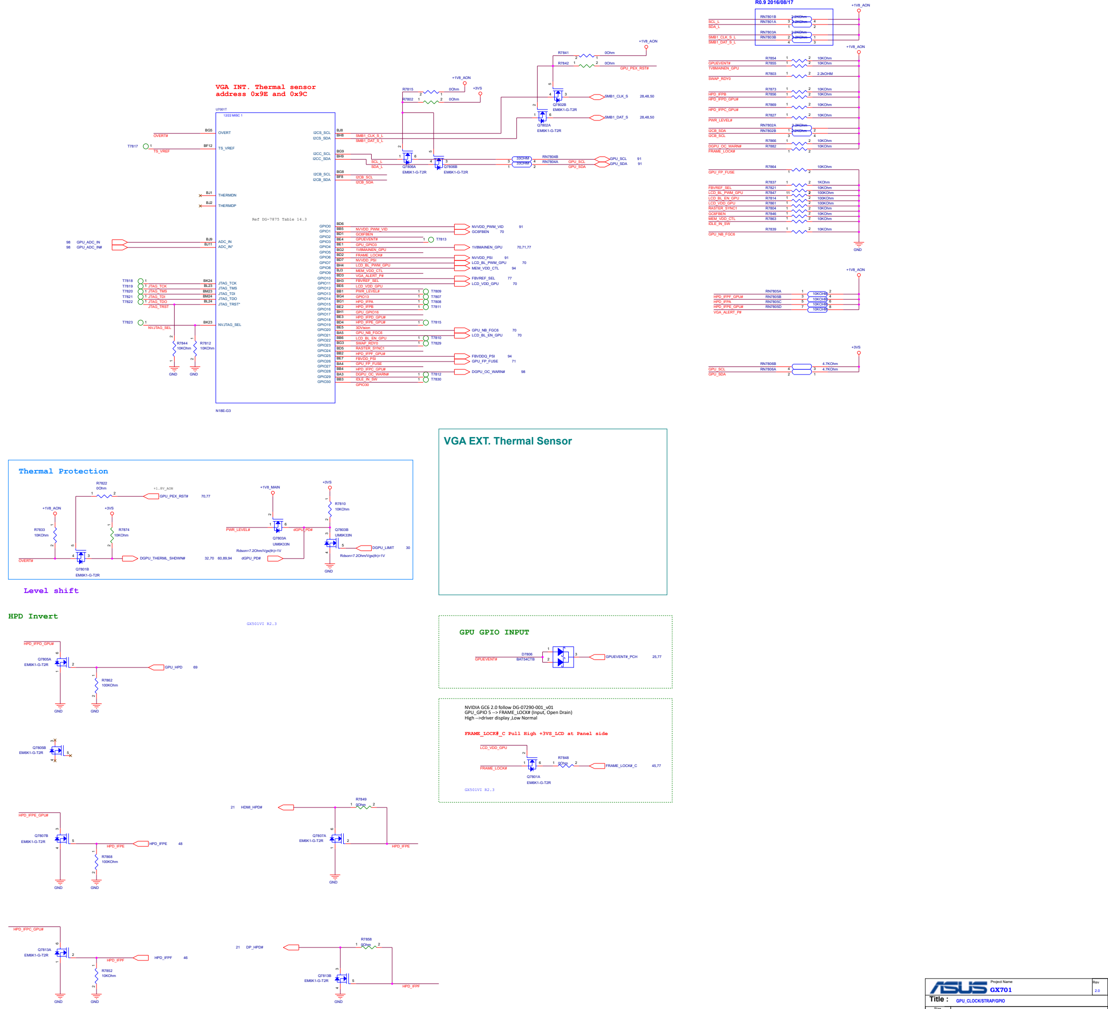
Note 1: Resistor should be 100K Ohms. 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull up to the 1V8_AON rail rather than to 1V8_MAIN.

Assorted Configuration Straps

1. SMB_ALT_ADDR Enable: "0" signal GPU setting I2CS address 0x9E, "1" Dual GPU setting I2CS address add 0x9C, used when a second GPU
2. DEVID_SEL: G-sync function→"0"normal GPU ID, "1" support G-sync GPU ID
3. PCIE_CFG: PCIE Swing→"0" PCIE Swing default, "1" PCEI swing reduce
4. VGA_DEVICE: Graphics circuit→"0" MS-Hybrid, "1" Discrete

Strap Pins (see Note)			FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

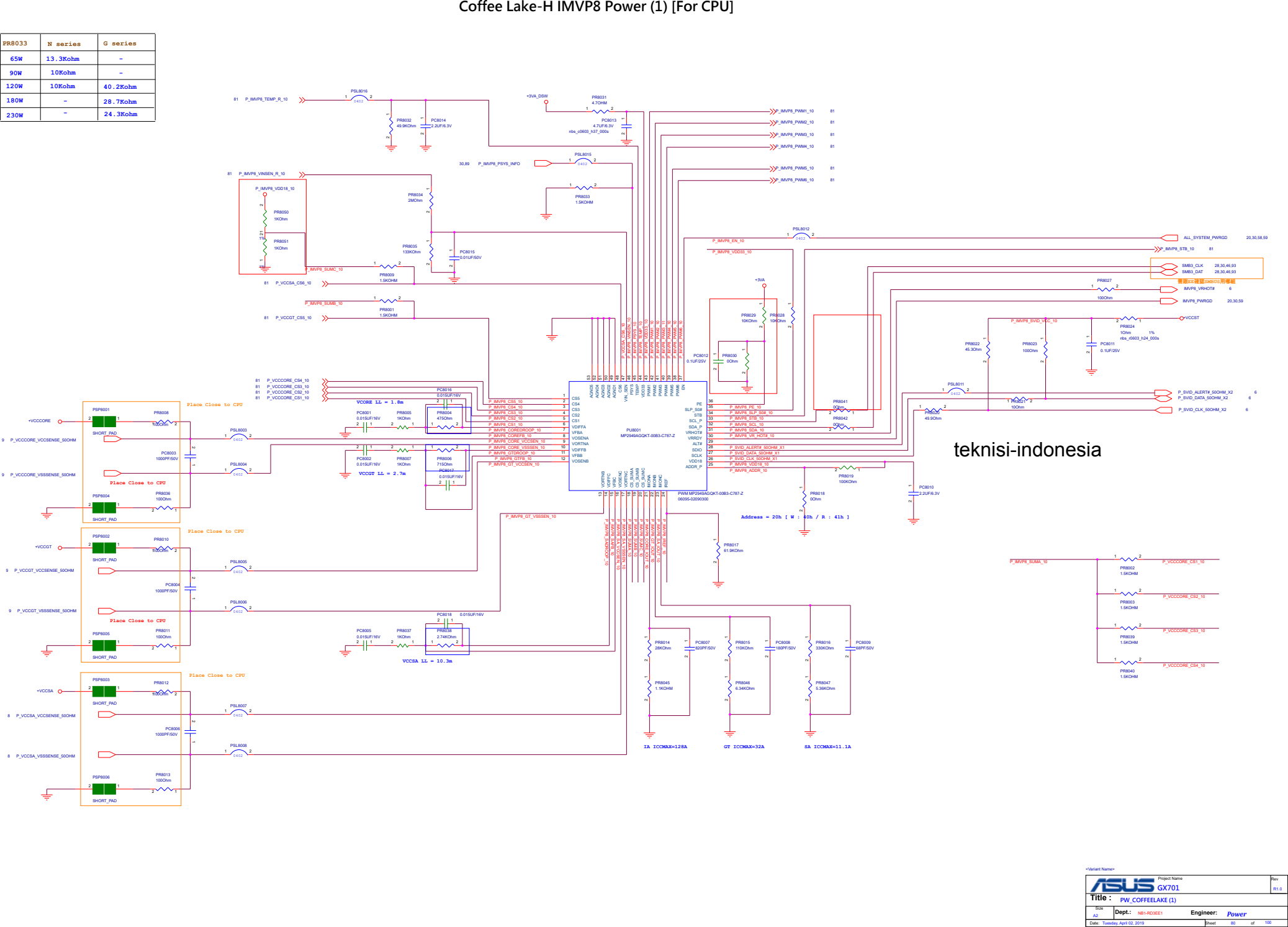
VGA INT. Thermal sensor address 0x9E and 0x9C



Title: GPU_CLOCK/STRAP/GPIO
Project Name: GX701
Dept.: ASUSTeK COMPUTER INC.
Engineer: EE
Date: Thursday, May 09, 2019

Coffee Lake-H IMVP8 Power (1) [For CPU]

PR8033	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm

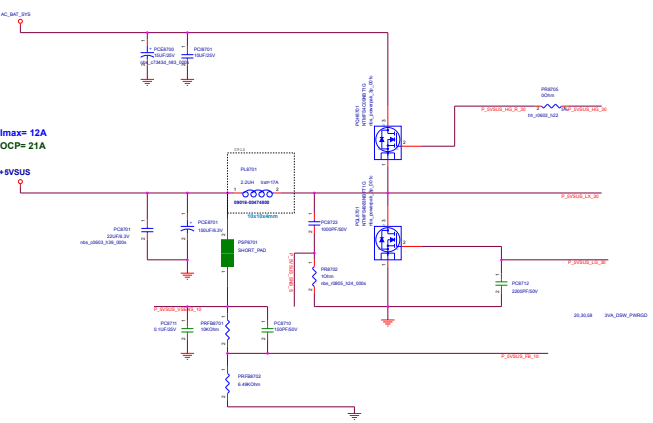


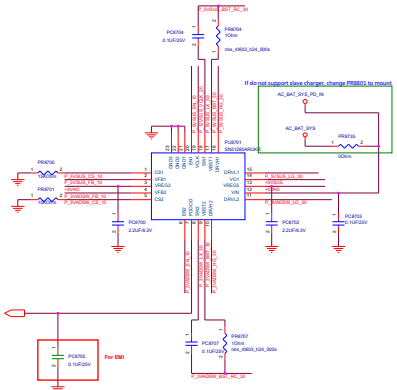
Coffee Lake-H IMVP8 Power (2) [For CPU]

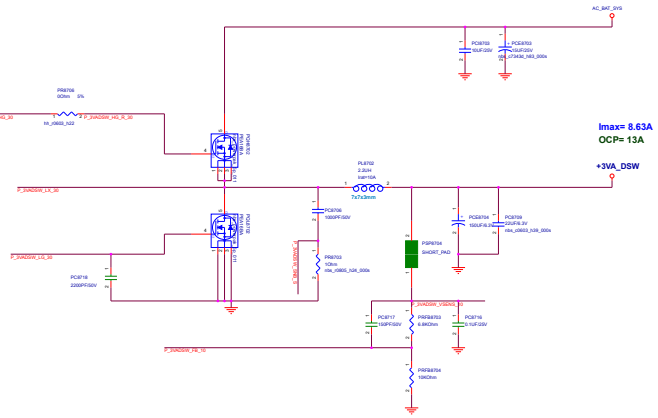
BOM

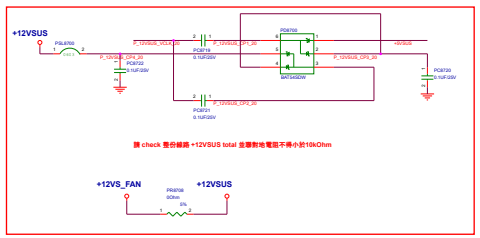
Project Name: GX701	Rev: R1.1
Title : PW_COFFEELAKE (2)	
Size: Custom	Dept.: NB1-RD3EE1 Engineer: Power
Date: Tuesday, April 02, 2019	Sheet 81 of 100

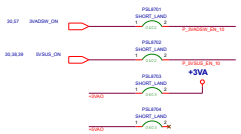
+3VA_DSW / +5VSUS [System Power]











Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

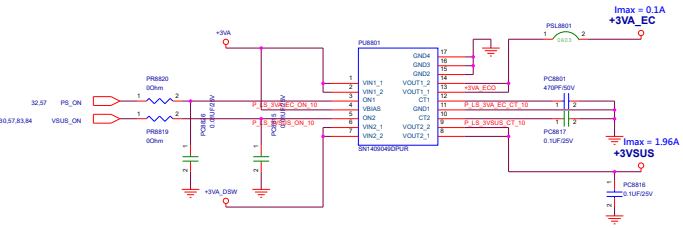
Battery Mode (IMVP8)

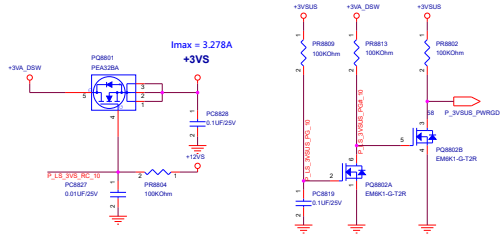
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

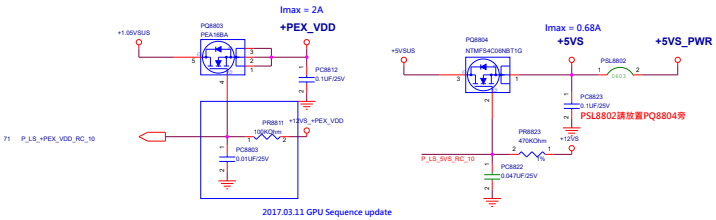
PT870* 請放置 PU8700旁坐請放置Trace 上!

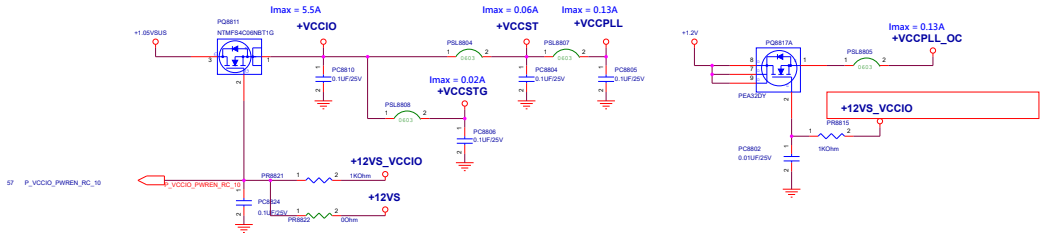
Load Switch

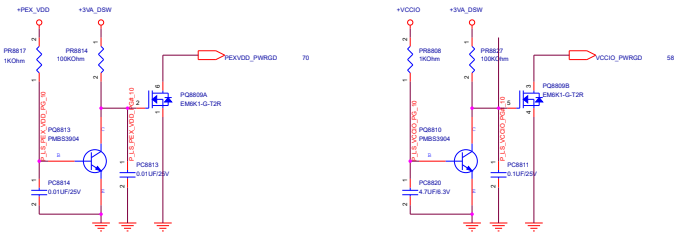
Main Board

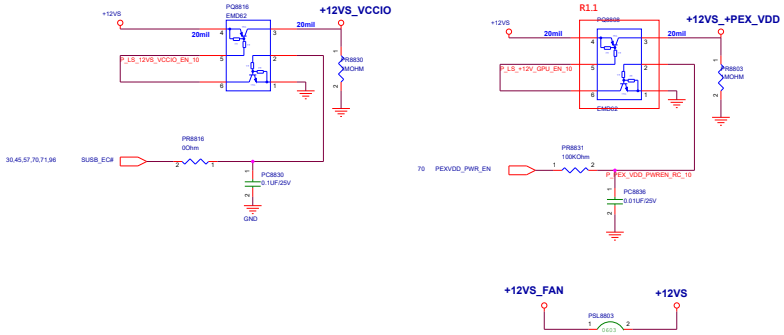










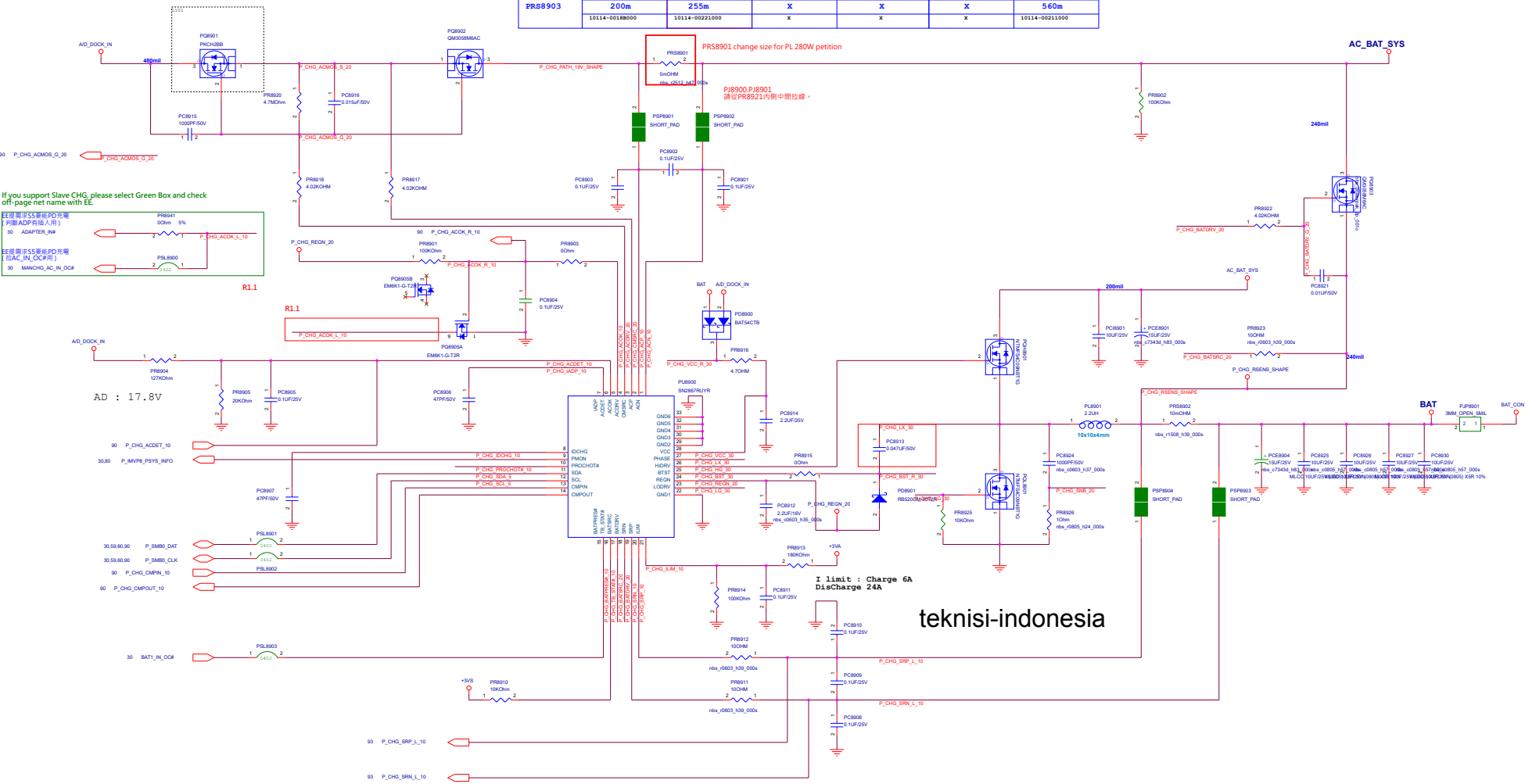


ASUS	Project Name: GX701		Rev: R1.0
Title : PW_LOAD SWITCH			
Size: A2	Dept.: NB Power team	Engineer: Power	
Date: Tuesday, April 02, 2019	Sheet: 88 of 100		

Main Board

PRS8901	ADP<120W	ADP<=230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	TBD	10125-0008B100	10108-0006B000	10108-0008B000

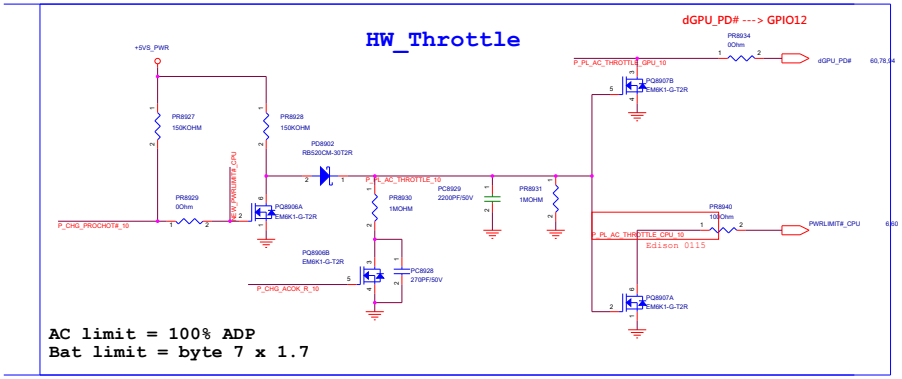
PRS8903	ADP=120W	ADP=150W	ADP=180W	ADP=230W	ADP=280W	ADP=330W
	200m	255m	X	X	X	560m
	10114-0018B000	10114-00221000	X	X	X	10114-00211000

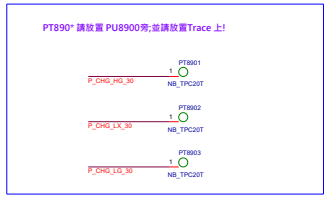


Adaptor select
total power = 90% ADP

Adaptor select

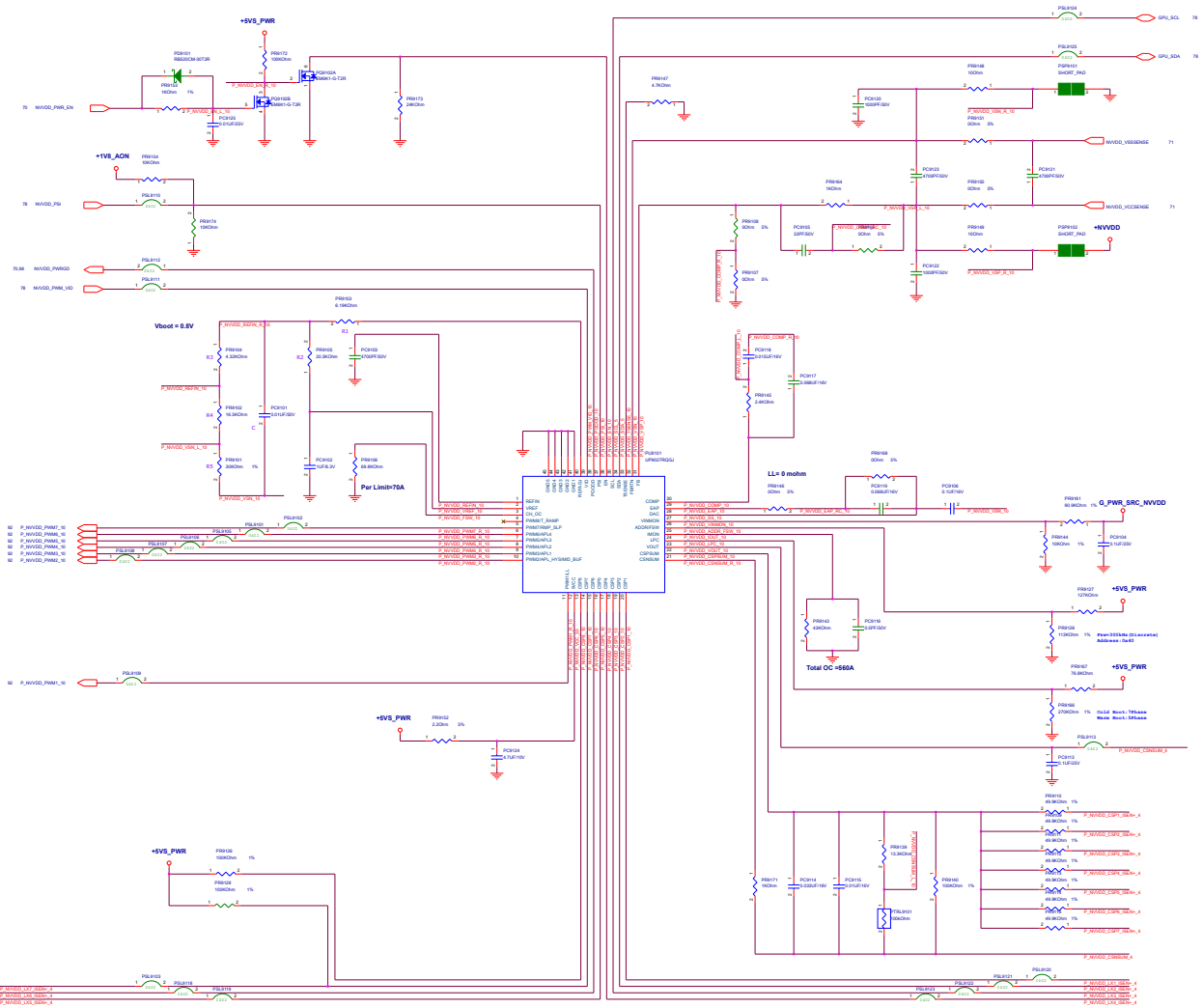
	N Series	G Series
PR8921	10m	5m
PR8936		
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	280W
270K	2.4V	90W	330W
560K	2.8V	120W	400W



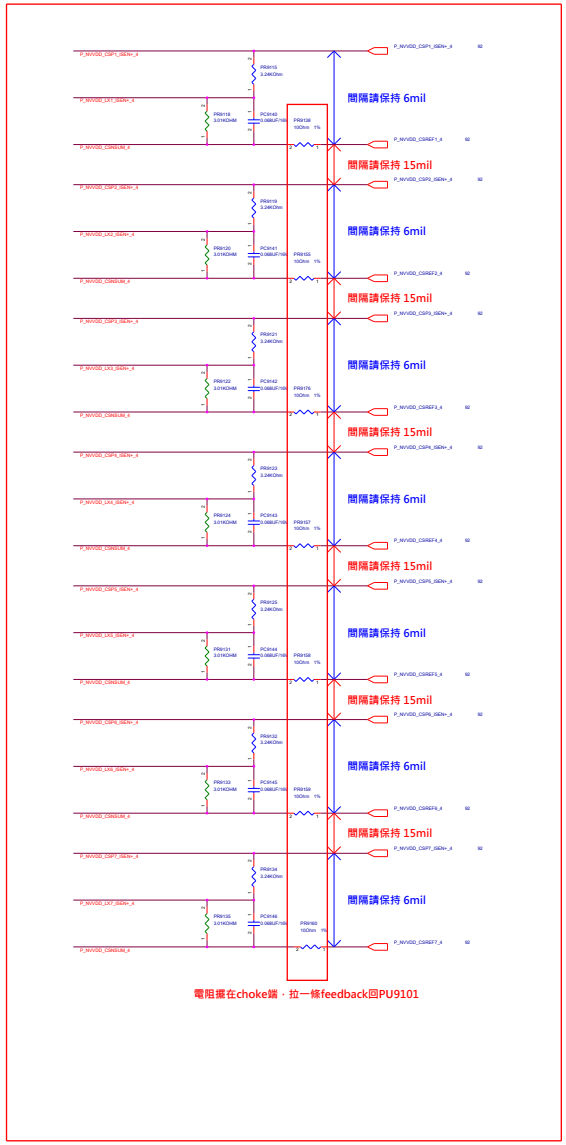


Project Name	GX701	Rev R1.0
Title :	PW_CHARGER	
Size A2	Dept.: NB Power Team	Engineer: Power
Date: Tuesday, April 02, 2019	Sheet 89 of 100	

+NVVDD [For DGPU]

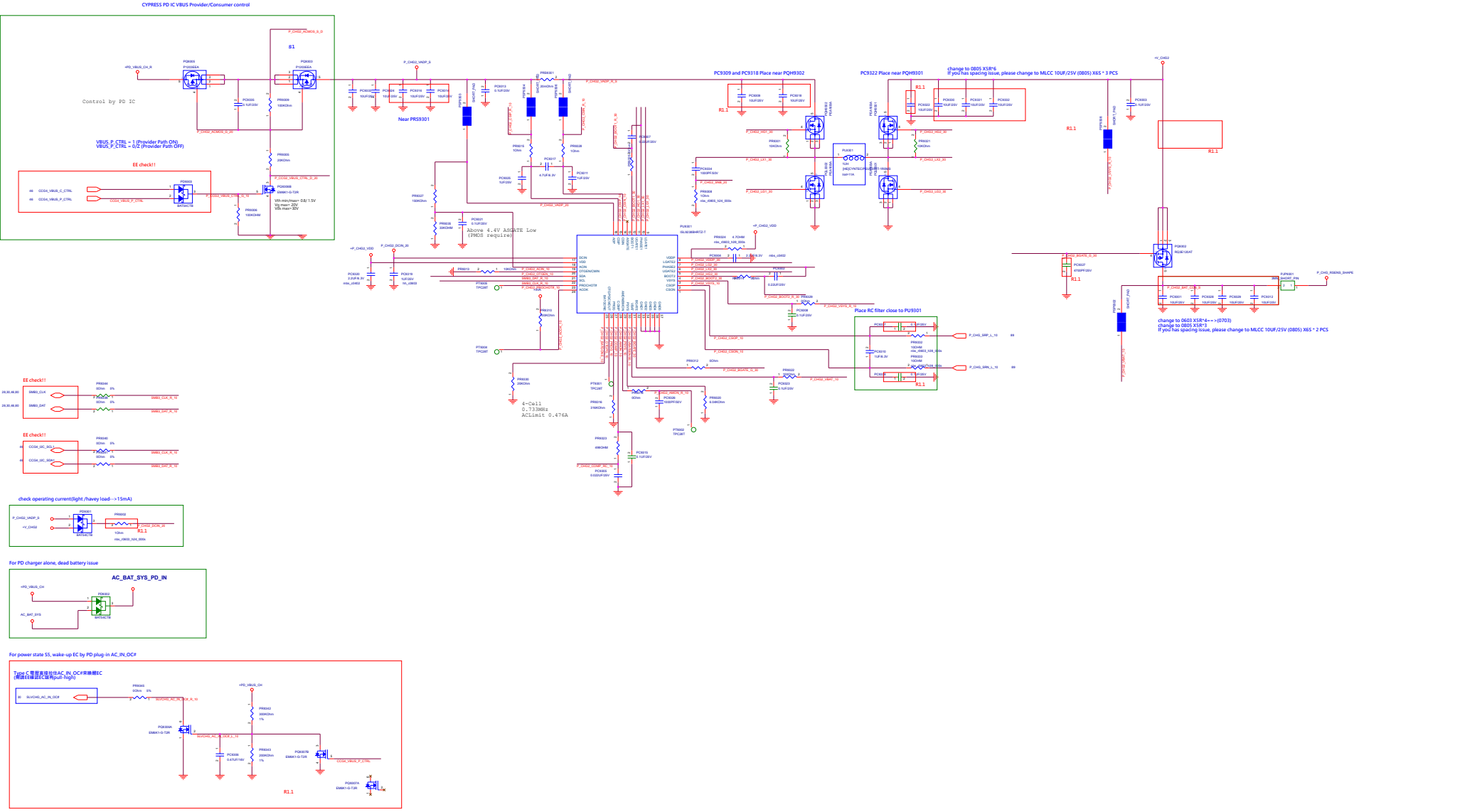


請放靠近PU9101



ASUS	Project Name: G711GW		Rev: R1.0
Title :	PW_+NVVDD (1)		
Size: A3	Dept.: NB Power team	Engineer: Neil	
Date: Tuesday, April 02, 2019	Sheet: 91	of: 100	

Charger ISL9238B (NVDC)



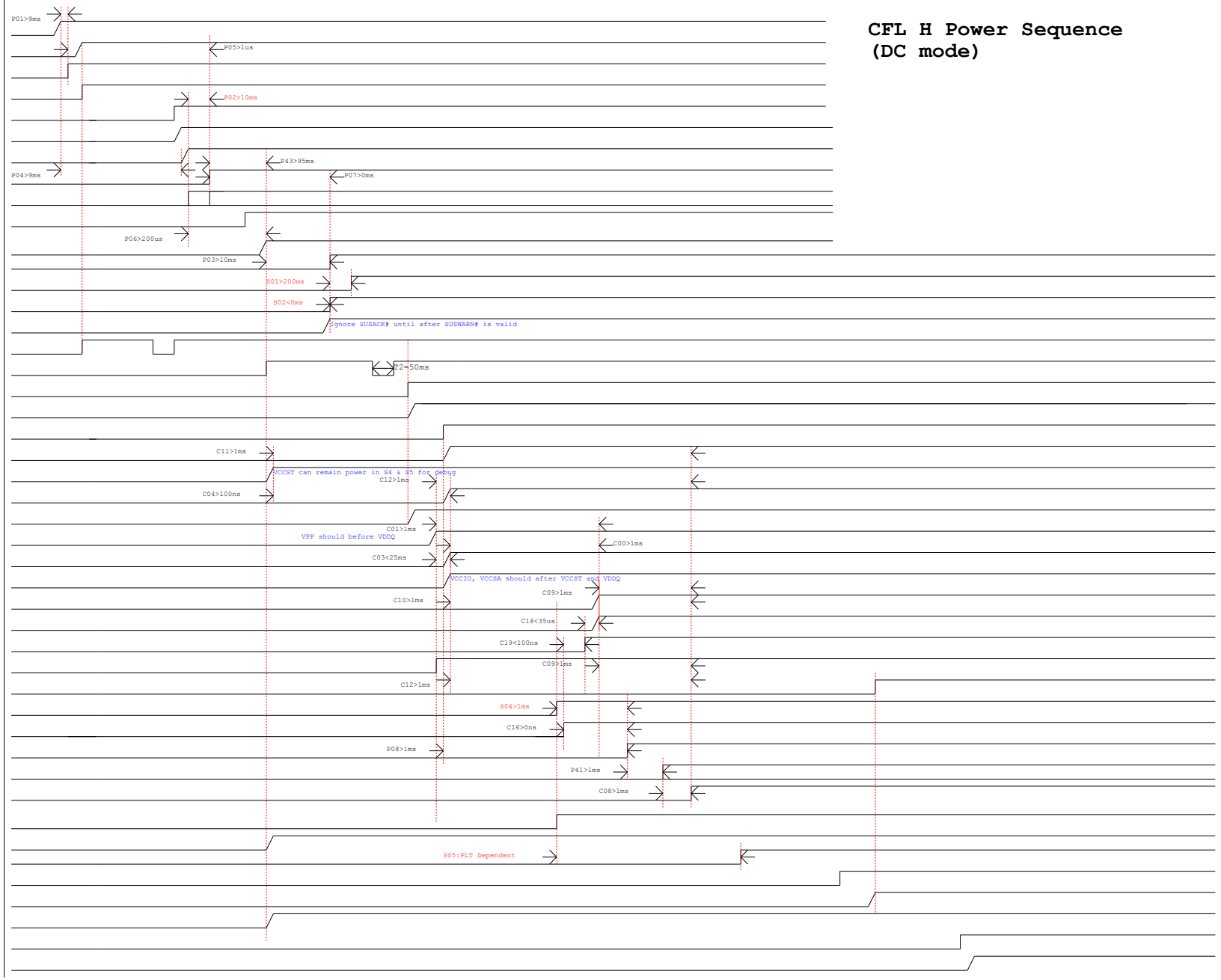
Project Name: GX701			Rev: R1.0
Title: Thunderbolt			
Size: A3	Dept.: ASUS Power Team	Engineer: Power	
Date: Tuesday, April 02, 2019	Sheet: 93	of: 100	

CFL H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



ASUS	Project Name: GX701		Rev: R1.0
Title : Power On Timing--DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Wednesday, March 06, 2019	Sheet 101 of 100		