Model Name: GA-EP45T-UD3LR REV 1.3

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02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
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06	P4_LGA775_B,D
07	P4_LGA775_C
08	P4_L775_E,F,G,H
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10	GMCH-Eaglelake_DDRII
11	GMCH-Eaglelake_PCI E, DMI
12	GMCH-Eaglelake_INT VGA
13	GMCH-Eaglelake_GND
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17	DDR3 TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH10 DMI, PCI, USB
20	ICH10 GPIO, CTRL
21	ICH10 SATA, FAN PWM
22	ICH10 VCC, GND
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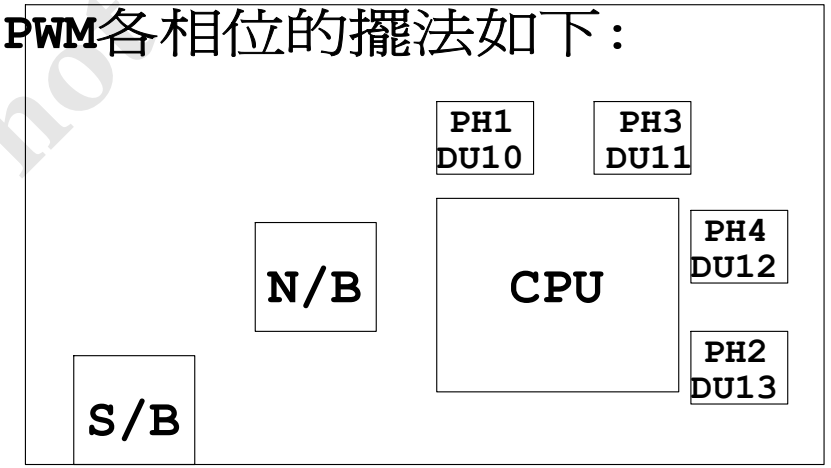
SHEET	TITLE
28	AZALIA ALC888
29	AUDIO JACK
30	VCORE PWM_ISL6334CRZ
31	DISCRETE1 POWER,FAN CTRL
32	ATX POWER
33	JMicron JMB368
34	LAN REALTEK RTL8111C
35	FRONT PANEL,FUSB,FDD
36	TPM I/F-1.2

PWM各相位的擺法如下：



Gigabyte Technology

Title	Cover Sheet	
Size: Custom	Document Number: GA-EP45T-UD3LR	Rev: 1.3
Date: Monday, April 26, 2010	Sheet 1 of 36	

Model Name: GA-EP45T-UD3LR
Rev:1.3

Component value change history

Data	Change Item	Reason
97/04/01 EBOM:01A	1. P43 CHIPSET E-BOM	
97/04/15 EBOM:02	1. 修改LED的POWER及阻值;DEL R484,DR78. ADD DR79,,R348	
	2. ADD DR80,R300 10-->49.9,C158,LBC43 0ohm-->100PF for EMI	
	3. del Q3,Q4,BC11,BC9,R42,R15,PCI_BT1,PCI_BT2,R166,R168	
97/04/28 EBOM:10A	1. DDR2 VOLTAGE 1.83 --> 1.9V --> 2.0V --> 2.1V .....-->2.5V	
97/05/09 PBOM:10B	1. DR59,DR60 14K---->549ohm,del DR69	
	2. ADD U9(uP6262),R436,BC133 FOR CPU 超頻	
97/05/21 PBOM:10C	1.ICH,MCH PCI-E ,JM368的RX,TX串電容BOM 0.1U/Y5V-->0.1U/X7R,RTC RTCVDD -->X7R	
	2.ADD U6 FOR DDR TURN ON 2.1V ISSUE	
97/06/4 PBOM:10D	1.DEL Q107,R620,ADD R621	
	2.Q49(BAT54C) 限用 DII	
97/06/18 PBOM:10E	1.ADD MB_ID R283,DEL R282,Q87,Q91,R452,R498,R499,R500 FOR VTT_GMCH 1.2V	
	2.C197 0.1U/Y5V--->X7R	
	3.R300 49.9--->100 ohm ,C158 Y5V--->X7R for USB	
	4.DC20 0.01u--->1nf FOR CPU PSI ISSUE	
97/08/07 EBOM:20A	1.CPU 改爲SMART FAN	
	2.L4,L7 CHOKE Footprint Change "CHOKE1U2-20A-1PQN"	
	3.獨立南橋1.1V 的電壓	
	4. ADD GPIO37 FOR LOAD LINE CALIBRATION	
	5.J368 改爲1.8V;R209=100 OHM, ADD R640 FOR MB_ID2	
97/08/08 EBOM:30A	1.J368 改爲1.8V;47--->44.2	
	2.TO252---改爲POWER PACK	
97/08/26 EBOM:10A	1.DDR2換成DDR3 2.換NB /SB HEAT SINK	
97/10/15 PBOM:10B	1.CHANGE SB HEAT SINK FOR DDR3專用 2.R414 102K-->105K;R384 1.27k---->1.3k for 電壓調整	
	3. FDD改爲白色	
98/02/20 PBOM:10C	1.100UF 統一料號	
98/05/18 PBOM:10D	1.Backup bios R56 pull-high 1k--->330 ohm; 移除SST BIOS	
98/06/16 PBOM:10E	1.藍、白 DIMM slot;白色IDE	
98/11/11 EBOM:11A	1.add EUP function,audio co-lay 892;change connector color	98/11/27 PBOM:11A 1.ADD package -bom
99/04/16 PBOM:13A	1.F4,F5 1.6A--->3.5A 2.R348,R86,R87,R336,R337,R338 1K--->8.2K FOR PHASE LED	
	3.U6,U9 UPI6262 10%	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
97/04/01 PCB:0.1	1.P43-DS3L	
97/04/23 PCB:1.0	1. CE3位置請移至EC24左邊	
	2. 增加 upi6262 VCC Power (R620,R621,Q107)	
	3. 增加R622,R623 FOR DDR18V_OV3	
97/07/23 PCB:2.0	1.由1.0 修改,直接改成2.0	
	2.PCIEX16 和PCIEX1_2對調位置	
	3. DDR2_1~DDR2_4往左移,盡量讓MCH的位置在DDR SLOT中間	
	4.ADD CPU SMART FAN CONTROL	
97/07/23 PCB:3.0	1.由2.0 修改	
	2. cpu Vcore MOS TO252改爲POWER PACK	
97/08/26 PCB:1.0	1.由EP45-UD3L-1.0修改;DDR2換成DDR3	
97/10/15 PCB:1.01	1.由1.0 修改字面 FOR DDR3 2200+	
98/11/04 PCB:1.1	1.add EUP function,audio co-lay 892	
99/04/15 PCB:1.3	1.FOR USB 3倍力,修改ERP READY文字面	

Gigabyte Technology		
Title: BOM & PCB MODIFY HISTORY		
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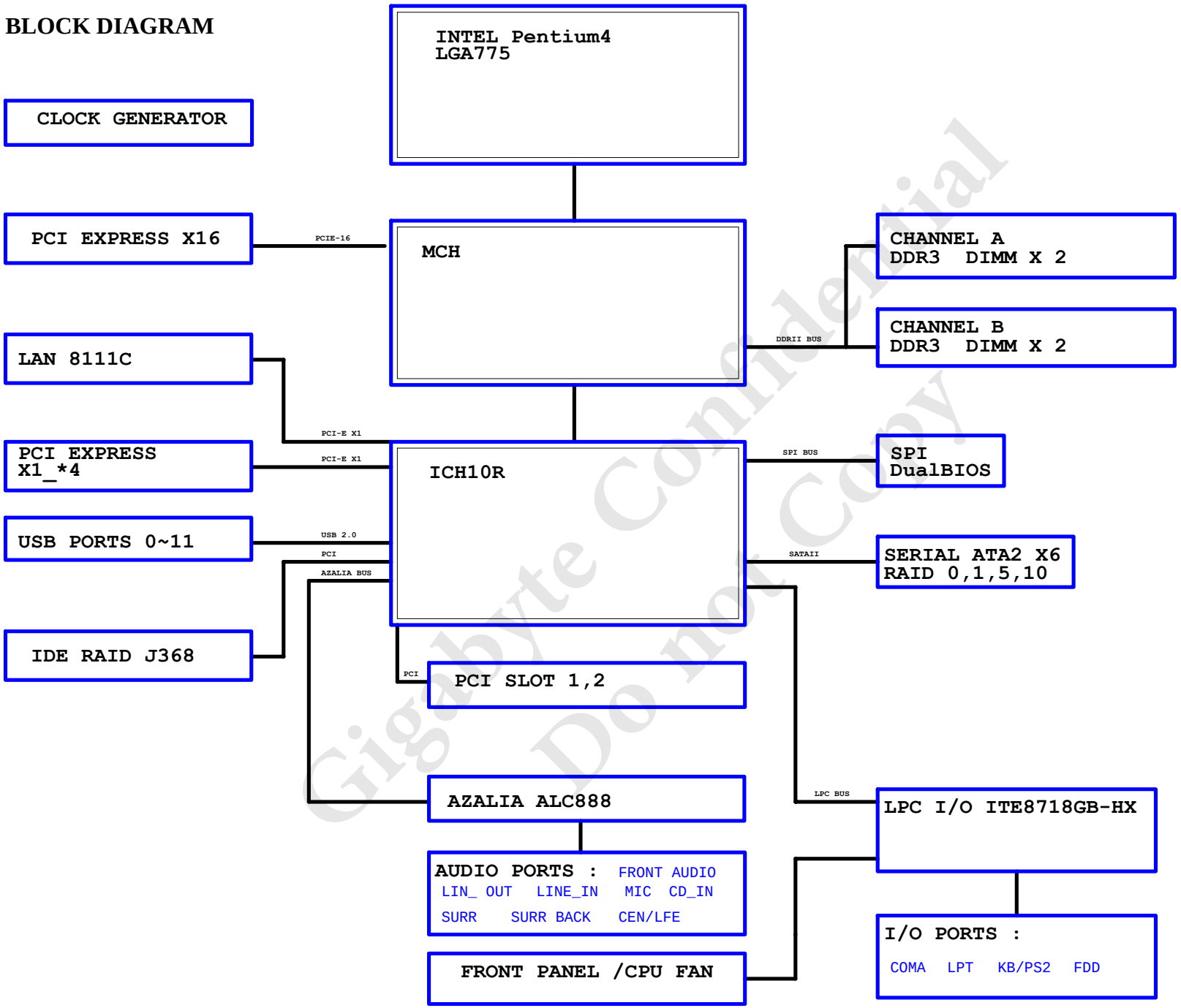
BLOCK DIAGRAM



Gigabyte Technology

Title	BLOCK DIAGRAM	
Size: Custom	Document Number: GA-EP45T-UD3LR	Rev: 1.3
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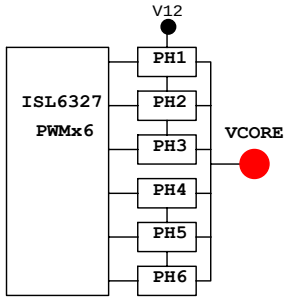
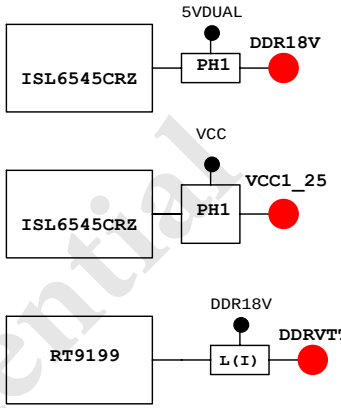
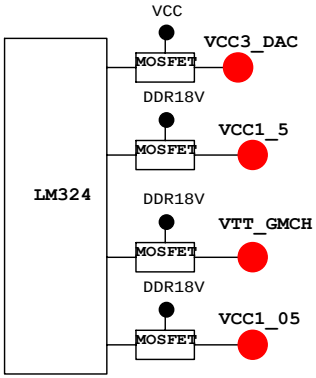
ICH8 GPIO LIST TABLE

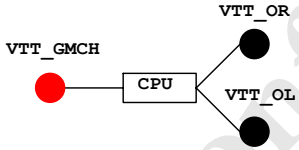
PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE(STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED(EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

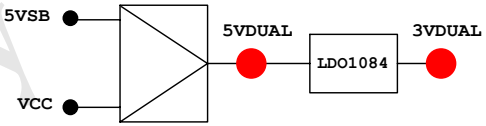
VCORE:6 PHASE PWM--ISL6327CRZ











Gigabyte Technology		
Title: TABLE LIST		
Size: B	Document Number: GA-EP45T-UD3LR	Rev: 1.3
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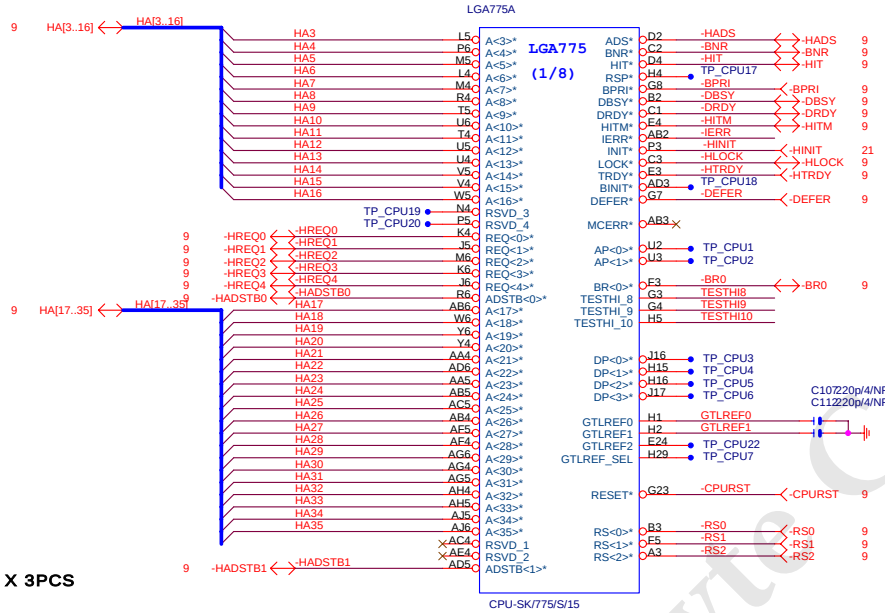
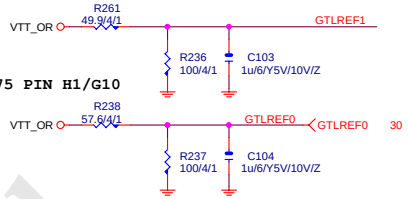
0.667 X VTT FOR LGA775 PIN H2/F2

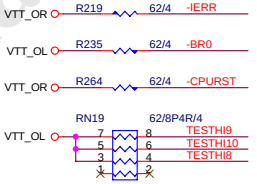
0.635 X VTT FOR LGA775 PIN H1/G10

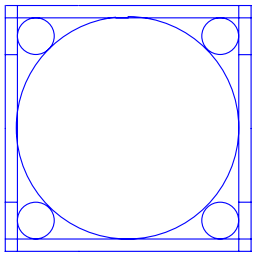
HA/REQ:50歐姆+-15% [4/11]

ADSTB:50歐姆+-15% [4/14]

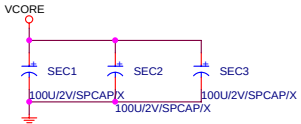




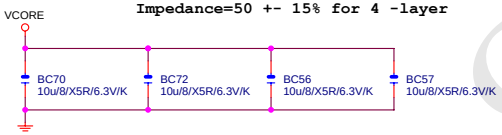


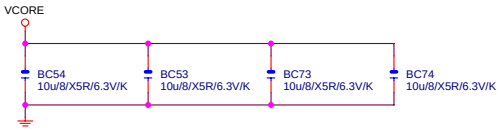


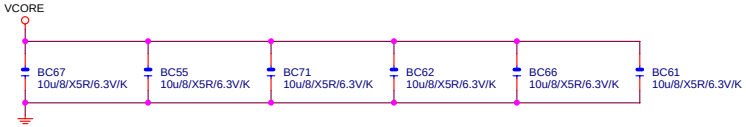
SP-CAP X 3PCS

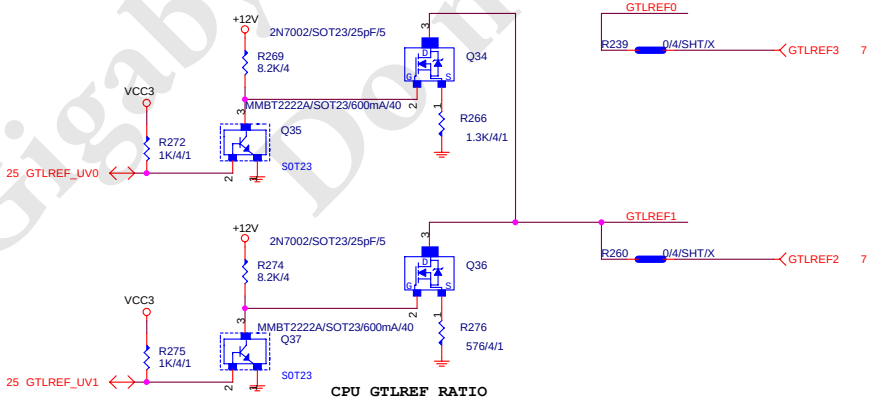


Impedance=50 +- 15% for 4 -layer









CPU GTLREF RATIO

GTLREF_UV0	GTLREF_UV1	Ratio Set
HIGH	HIGH	0.67
LOW	HIGH	0.65
HIGH	LOW	0.63
LOW	LOW	0.615

Gigabyte Technology

Title: P4_LGA775-A

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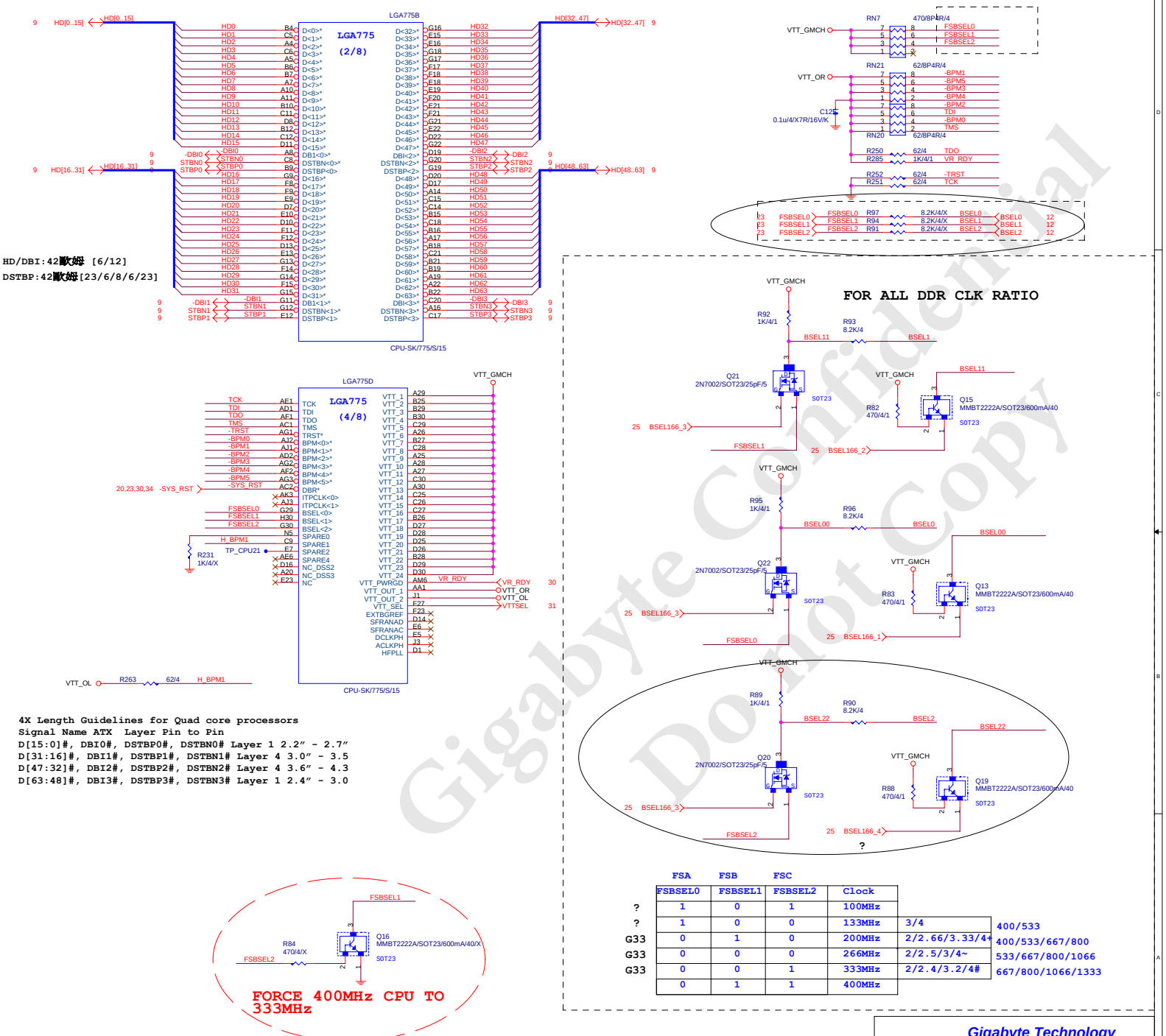
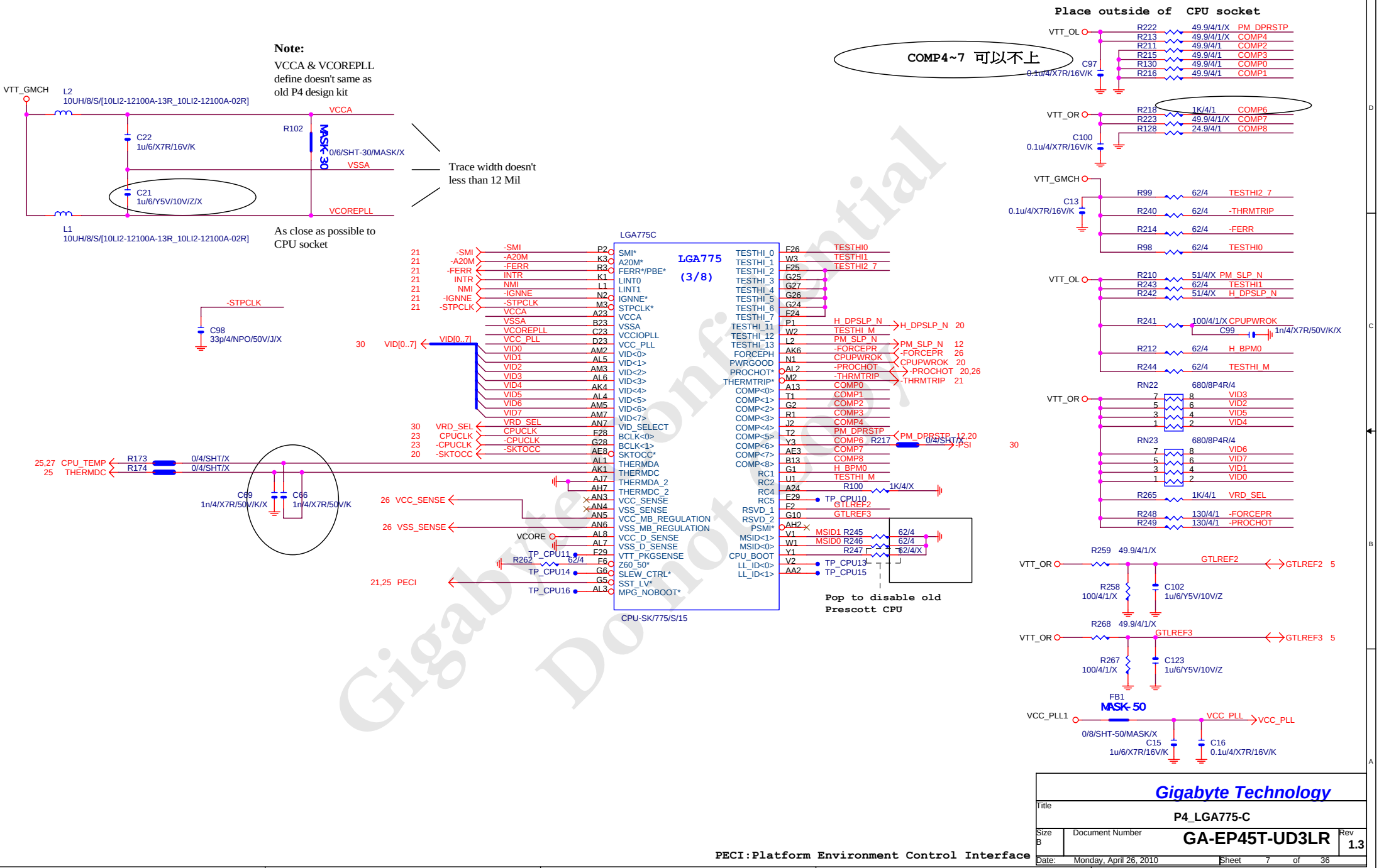


FSA	FSB	FSC			
FSBSEL0	FSBSEL1	FSBSEL2	Clock		
?	1	0	1	100MHz	
?	1	0	0	133MHz	3/4
G33	0	1	0	200MHz	2/2.66/3.33/4+
G33	0	0	0	266MHz	2/2.5/3/4~
G33	0	0	1	333MHz	2/2.4/3.2/4#
	0	1	1	400MHz	

400/533
400/533/667/800
533/667/800/1066
667/800/1066/1333

Gigabyte Technology			
Title	P4_LGA775-B,D		
Size: Custom	Document Number: GA-EP45T-UD3LR		Rev: 1.3
Date: Monday, April 26, 2010	Sheet 6 of 36		


Note:
VCCA & VCOREPLL define doesn't same as old P4 design kit
Trace width doesn't less than 12 Mil
As close as possible to CPU socket
Place outside of CPU socket
COMP4~7 可以不上
LGA775C
LGA775 (3/8)
CPU-SK/775/S/15
Pop to disable old Prescott CPU
PECI:Platform Environment Control Interface
Gigabyte Technology
P4_LGA775-C
GA-EP45T-UD3LR
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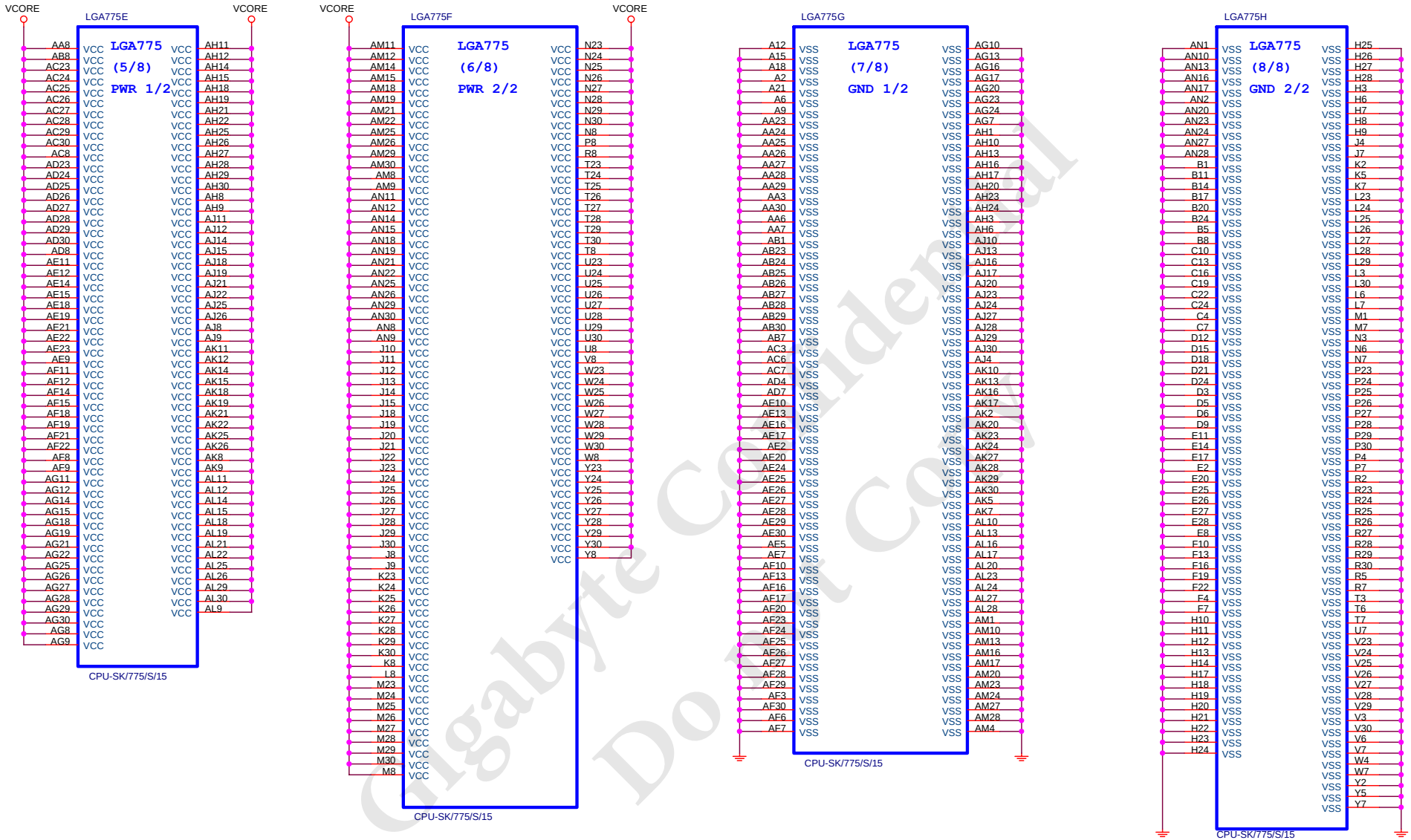
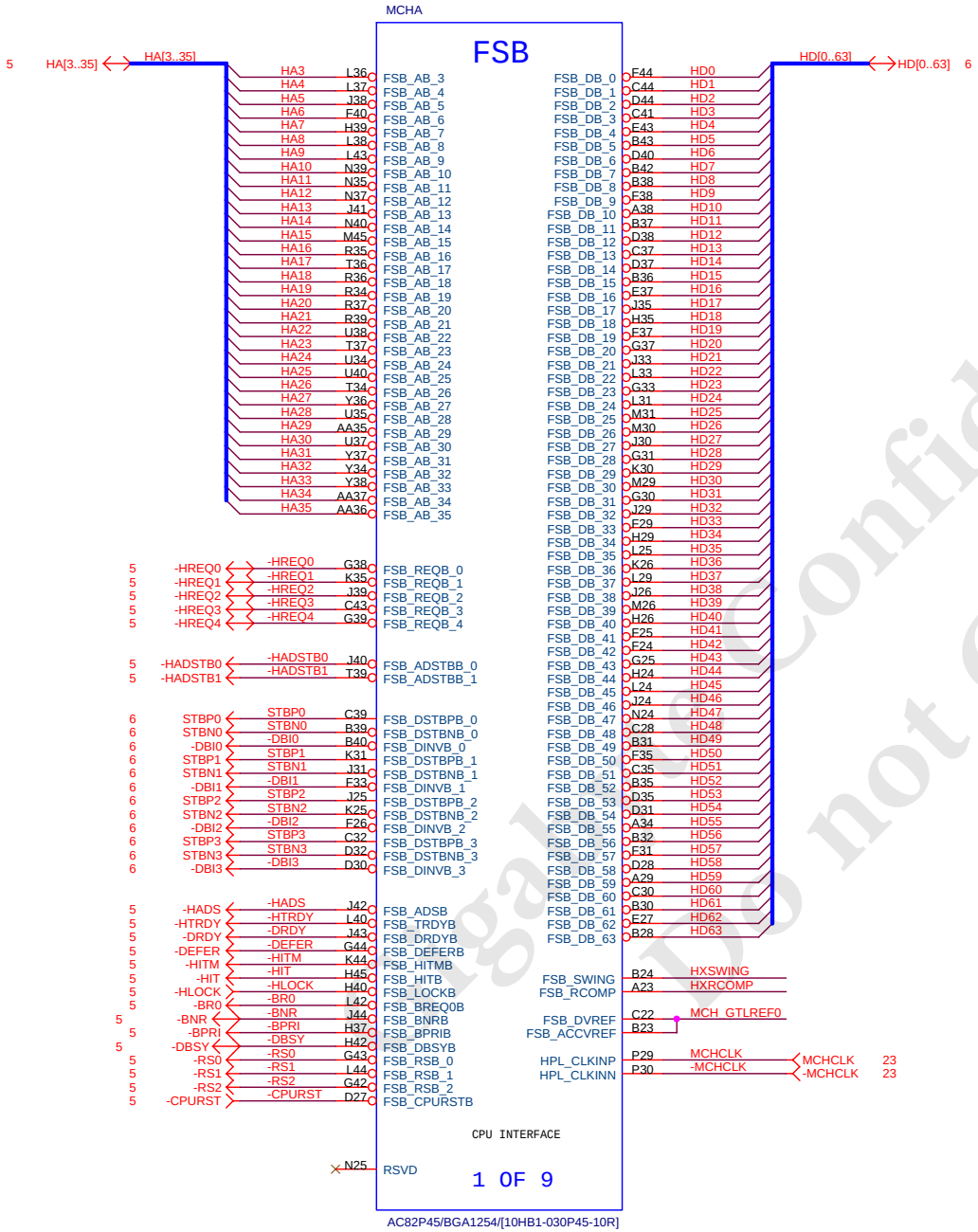
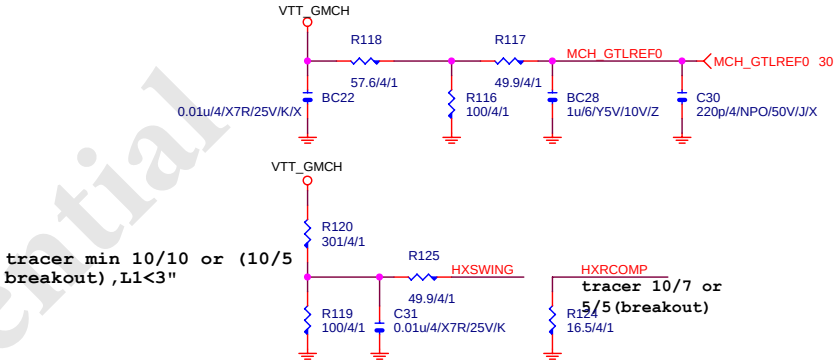


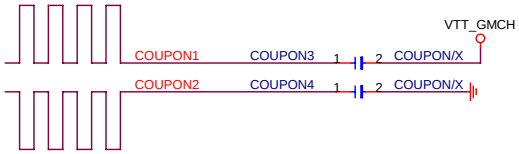
Gigabyte Technology		
Title: P4_LGA775-E,F,G,H		
Size: B	Document Number: GA-EP45T-UD3LR	Rev: 1.3
Date: Monday, April 26, 2010	Sheet 8 of 36	





tracer min 10/10 or (10/5 breakout),L1<3"

tracer 10/7 or 5/5(breakout)



Gigabyte Technology

Title: GMCH-HOST

Size: Custom | Document Number: GA-EP45T-UD3LR | Rev: 1.3

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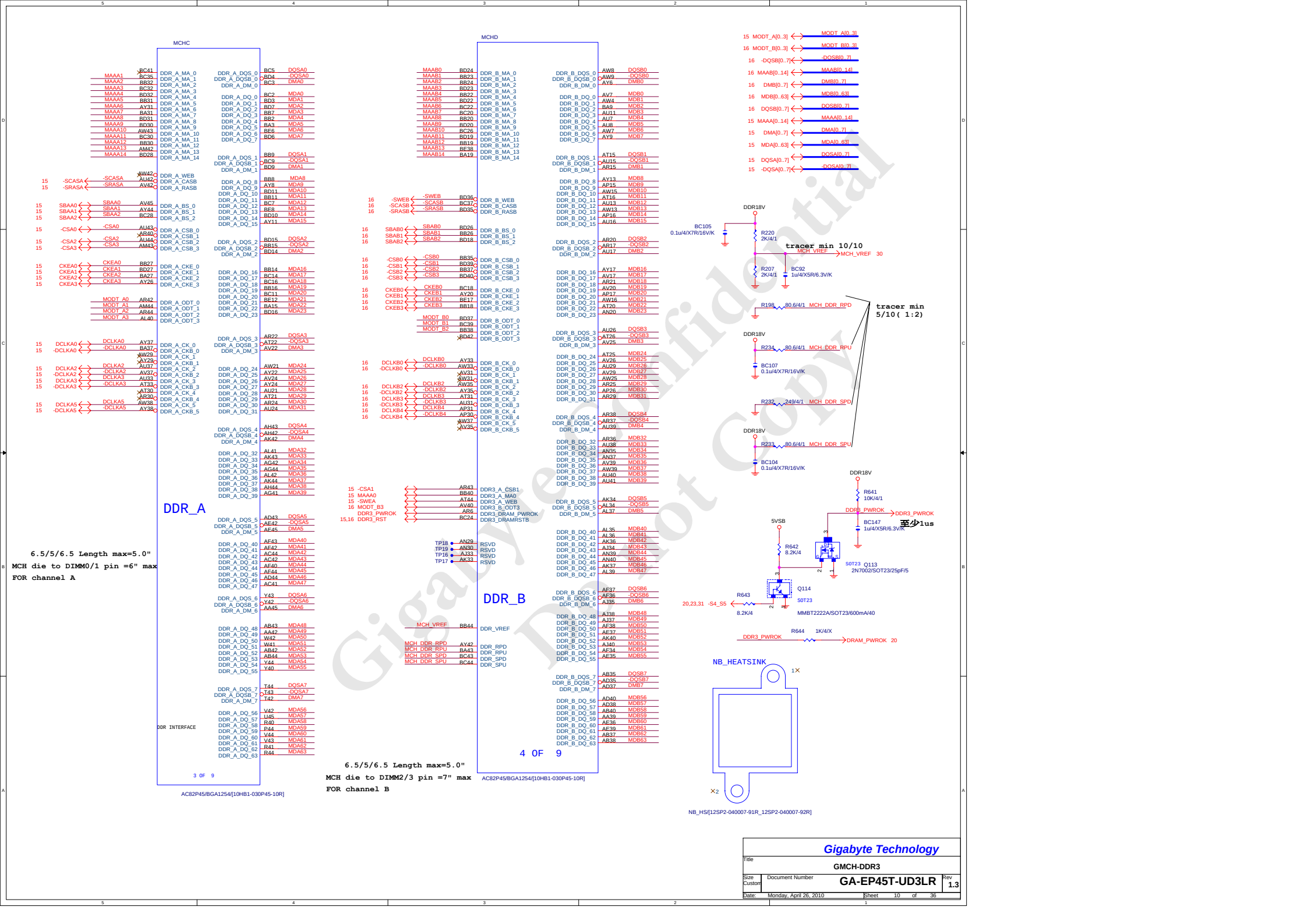
MCHC
DDR_A
DDR INTERFACE
3 OF 9
AC82P45/BGA1254/[10HB1-030P45-10R]
6.5/5/6.5 Length max=5.0"
MCH die to DIMM0/1 pin =6" max
FOR channel A
MCHD
DDR_B
4 OF 9
AC82P45/BGA1254/[10HB1-030P45-10R]
6.5/5/6.5 Length max=5.0"
MCH die to DIMM2/3 pin =7" max
FOR channel B
DDR18V
tracer min 10/10
tracer min 5/10(1:2)
NB_HEATSINK
NB_HS/[12SP2-040007-91R_12SP2-040007-92R]
Gigabyte Technology
GMCH-DDR3
GA-EP45T-UD3LR
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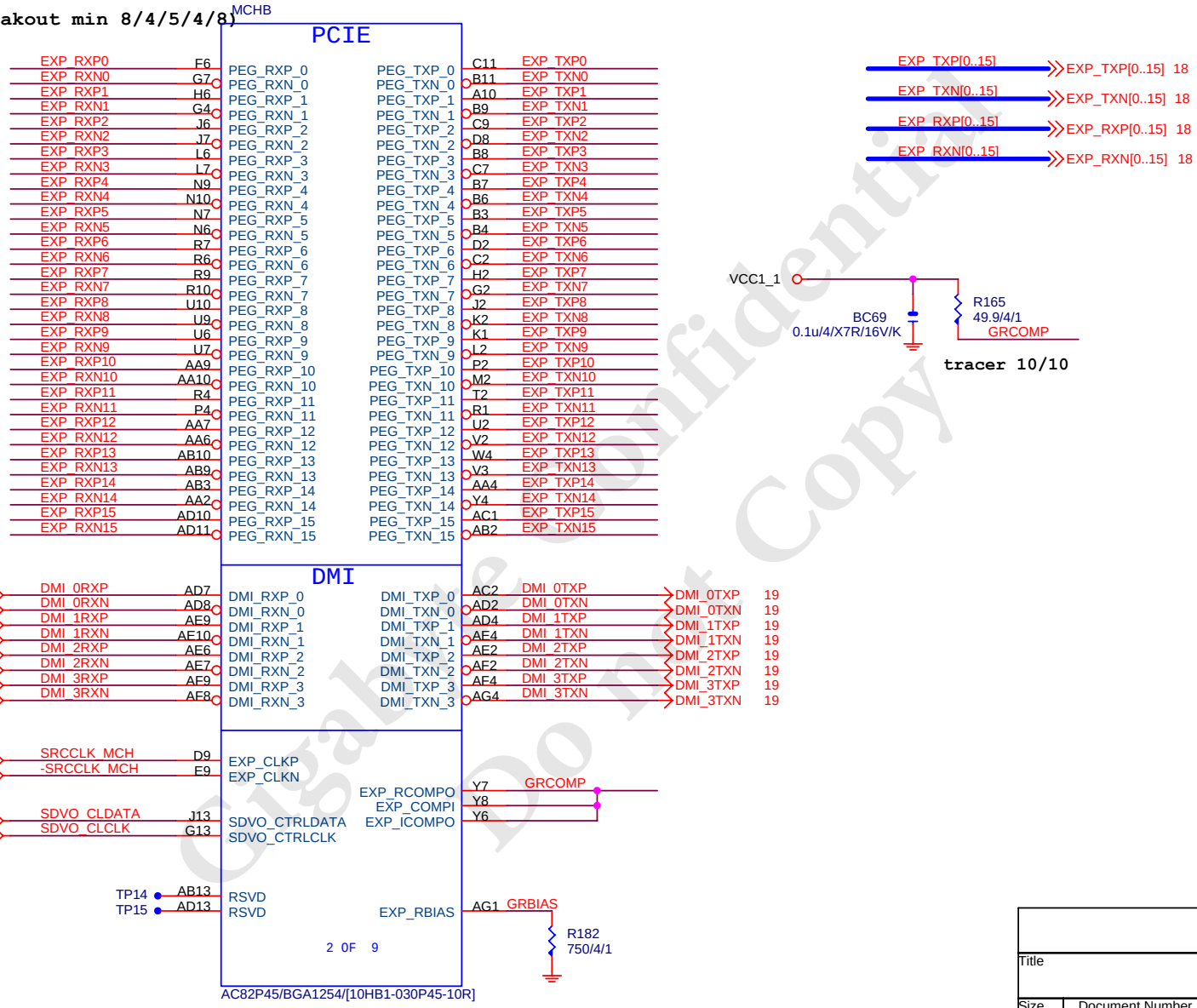
Do not Copy

PCIEX16:16/5/5/5/5/16(breakout min 8/4/5/4/8)

Impedance=85 +- 17.5%

DMI:12/4/8/4/12

Impedance=95 +- 17.5%



Gigabyte Technology		
Title: GMCH-PCI E & DMI		
Size: Custom	Document Number: GA-EP45T-UD3LR	Rev: 1.3
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EXP_SM
0:SDVO OR PCIE
1:BOTH SDVO AND PCIE

EXP_SLR:
0:BTX PCIE are reversed
1:ATX PCIE normal

ITPM:
0:ENABLE ITPM
1:DISABLE ITPM

CEN:
0:DISABLE TLS
1:ENABLE TLS

CL_VREF:4/10
0.349V

MCHE

VGA

MISC

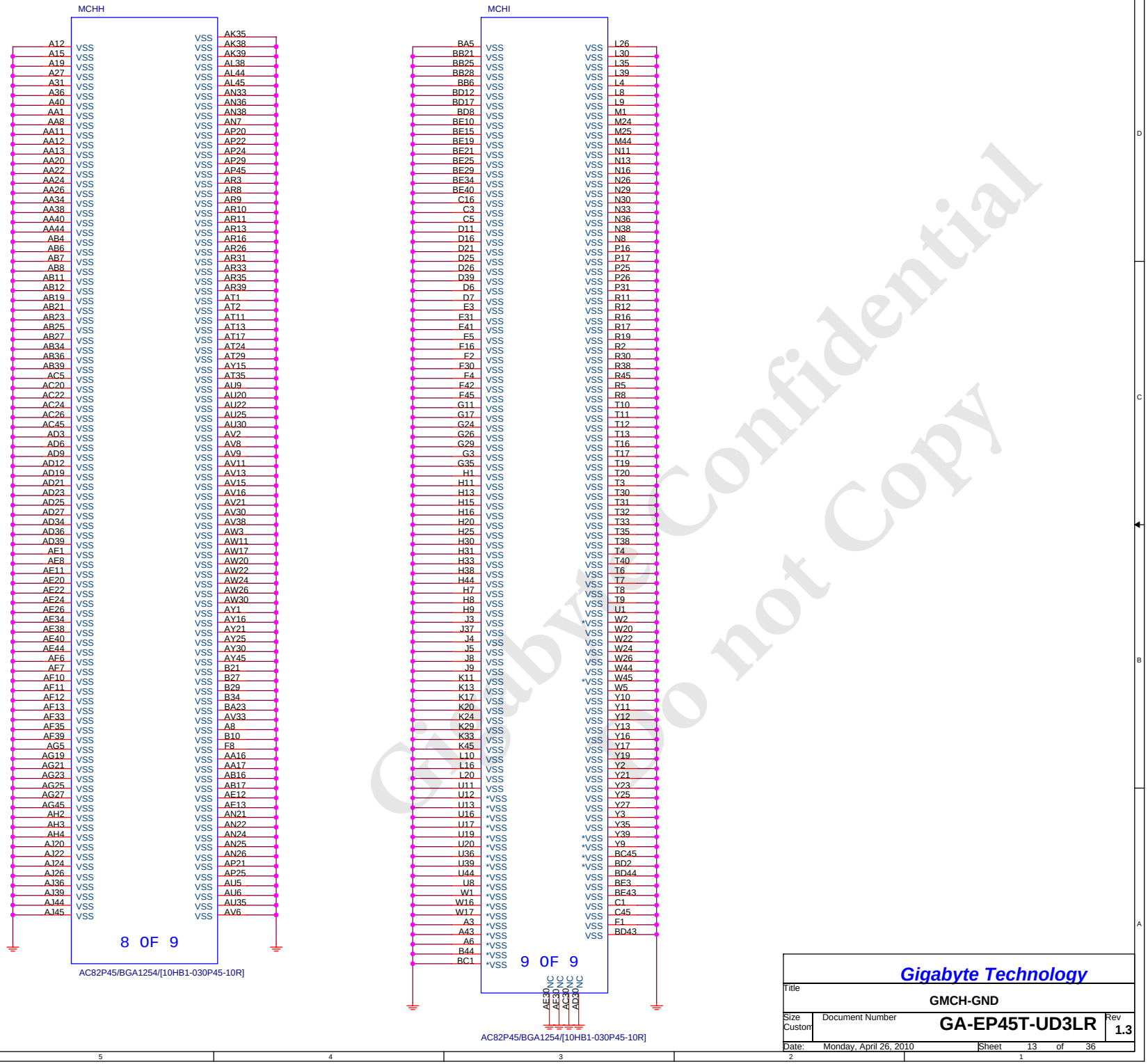
5 OF 9

AC82P45/BGA1254/[10HB1-030P45-10R]

BW+ICH8 不要上(SAMPLE)
BW+ICH7 要上

Gigabyte Technology

Title	GMCH-INTERNAL VGA		
Size: Custom	Document Number: GA-EP45T-UD3LR		Rev: 1.3
Date: Monday, April 26, 2010	Sheet 12 of 36		



Gigabyte Technology		
Title: GMCH-GND		
Size: Custom	Document Number: GA-EP45T-UD3LR	Rev: 1.3
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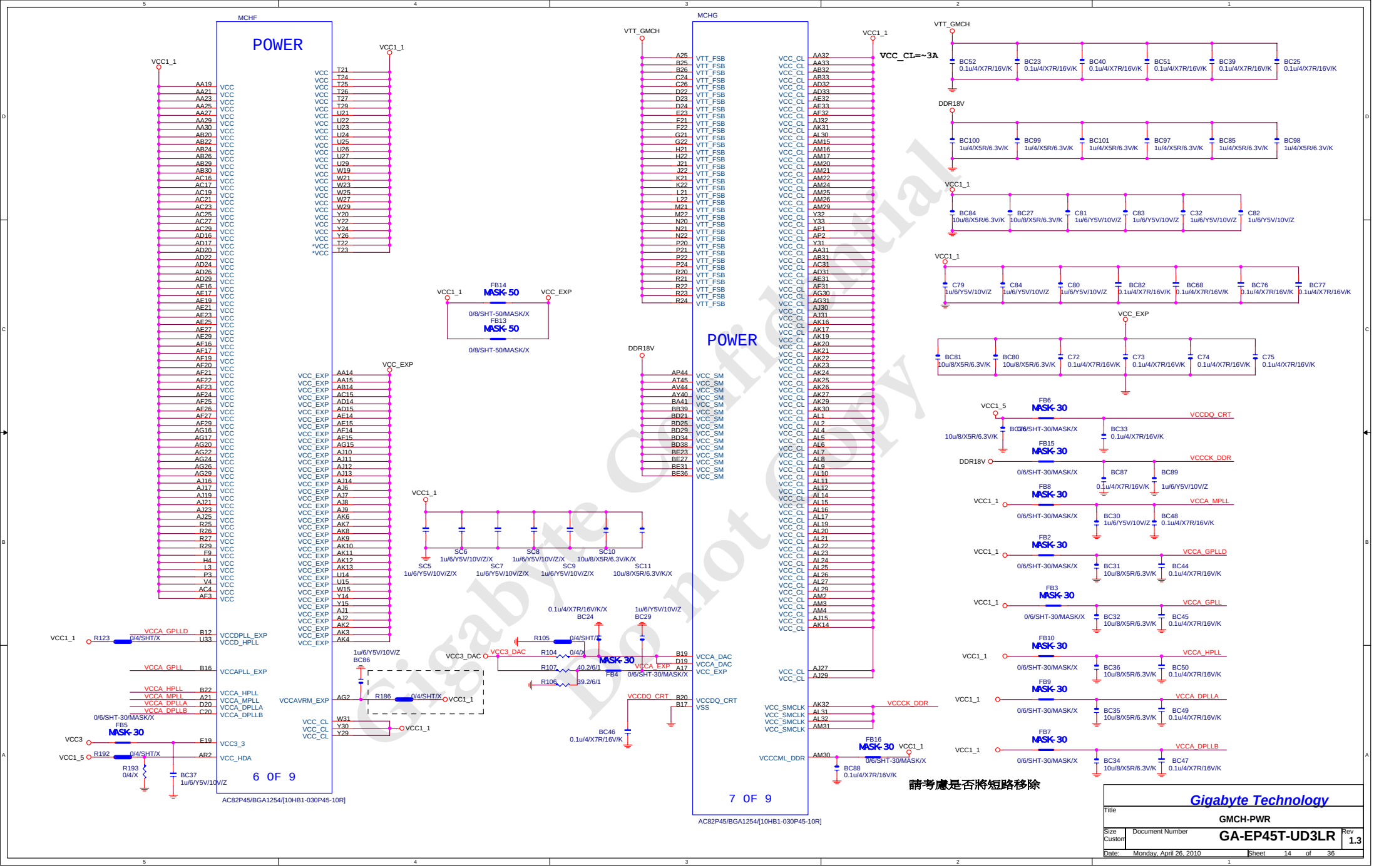
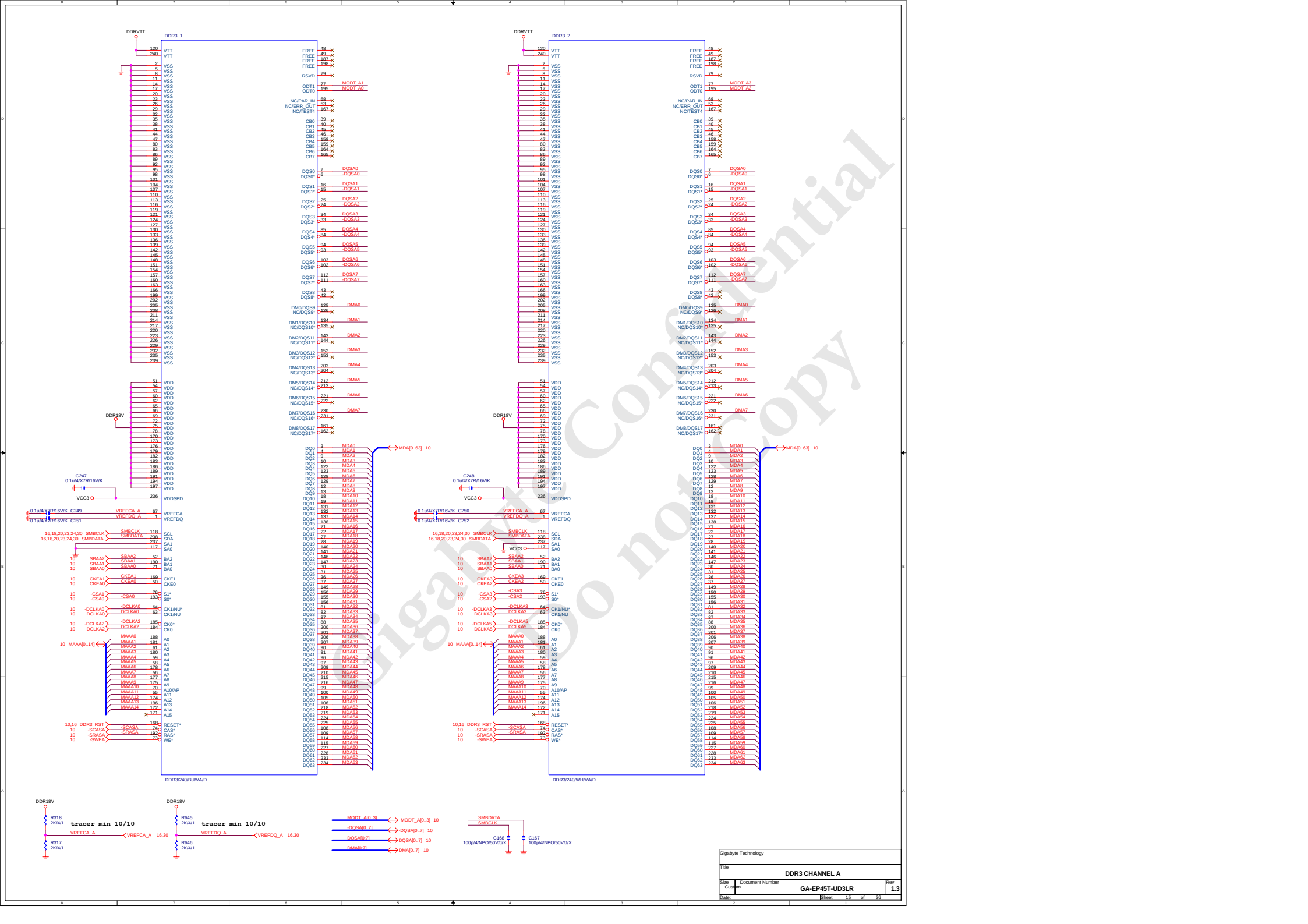
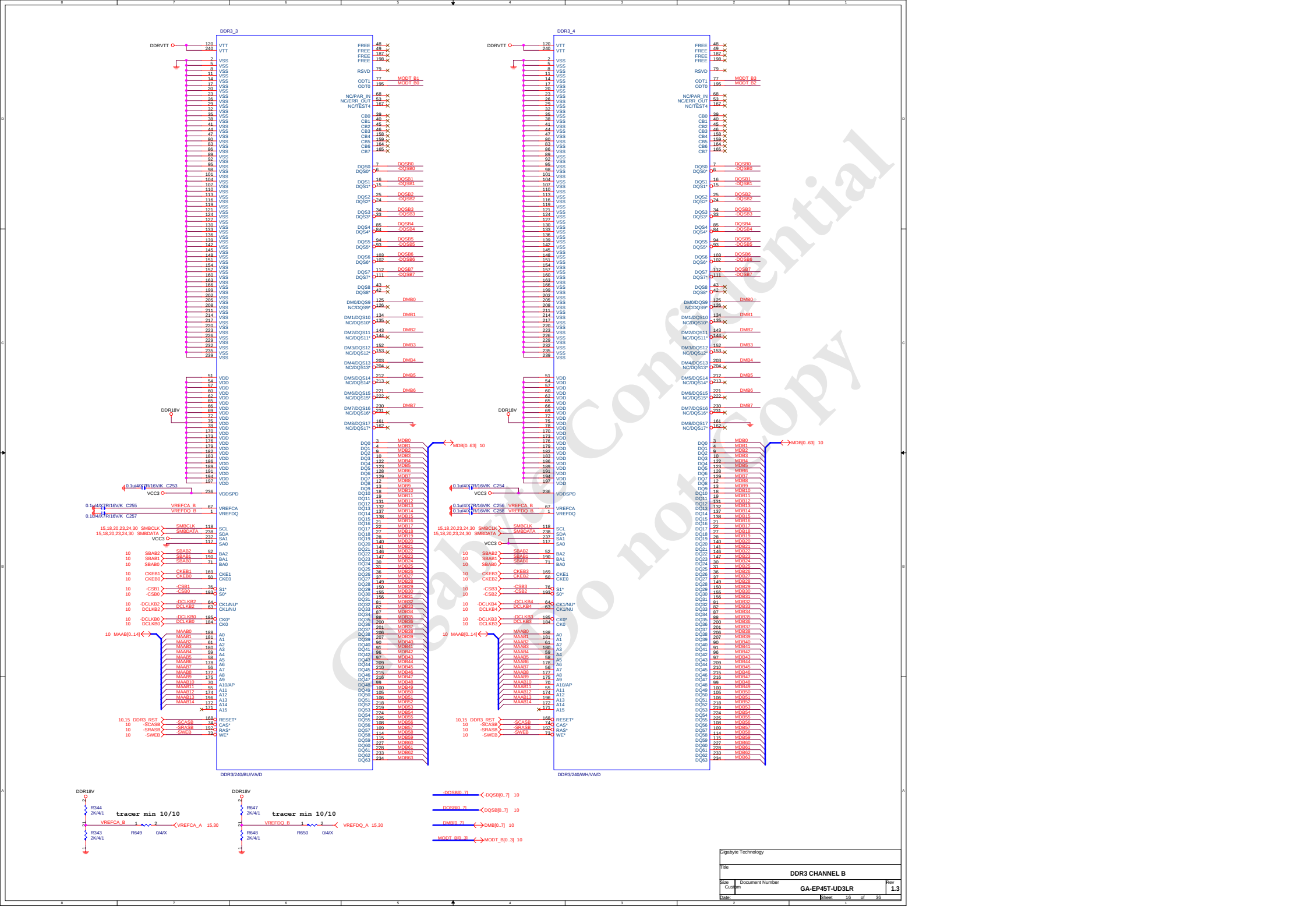
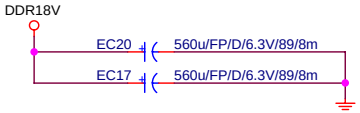

MCHF
POWER
6 OF 9
AC82P45/BGA1254/[10HB1-030P45-10R]
MCHG
POWER
7 OF 9
AC82P45/BGA1254/[10HB1-030P45-10R]
VCC_CL=~3A
請考慮是否將短路移除
Gigabyte Technology
Title
GMCH-PWR
Size
Custom
Document Number
GA-EP45T-UD3LR
Rev
1.3
Date: Monday, April 26, 2010
Sheet 14 of 36

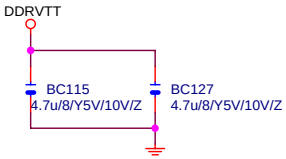




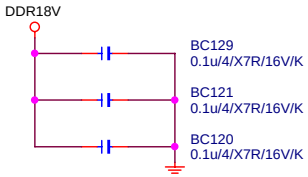
DDR TERMINATION CHANNEL A

DDRVTT Decouple

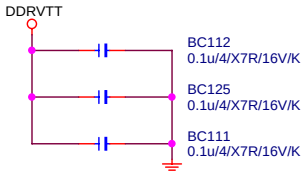


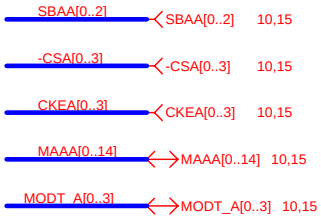


DDR18V Decouple



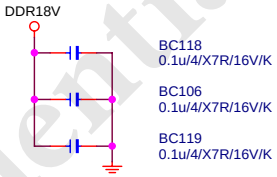
DDRVTT Decouple



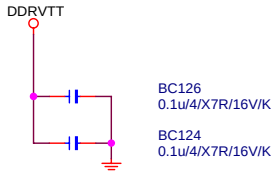


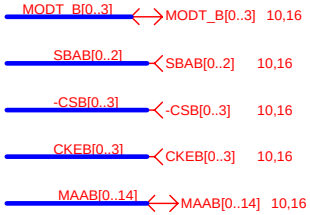
DDR TERMINATION CHANNEL B

DDR18V Decouple



DDRVTT Decouple





Gigabyte Technology

Title: DDR3 TERMINATOR

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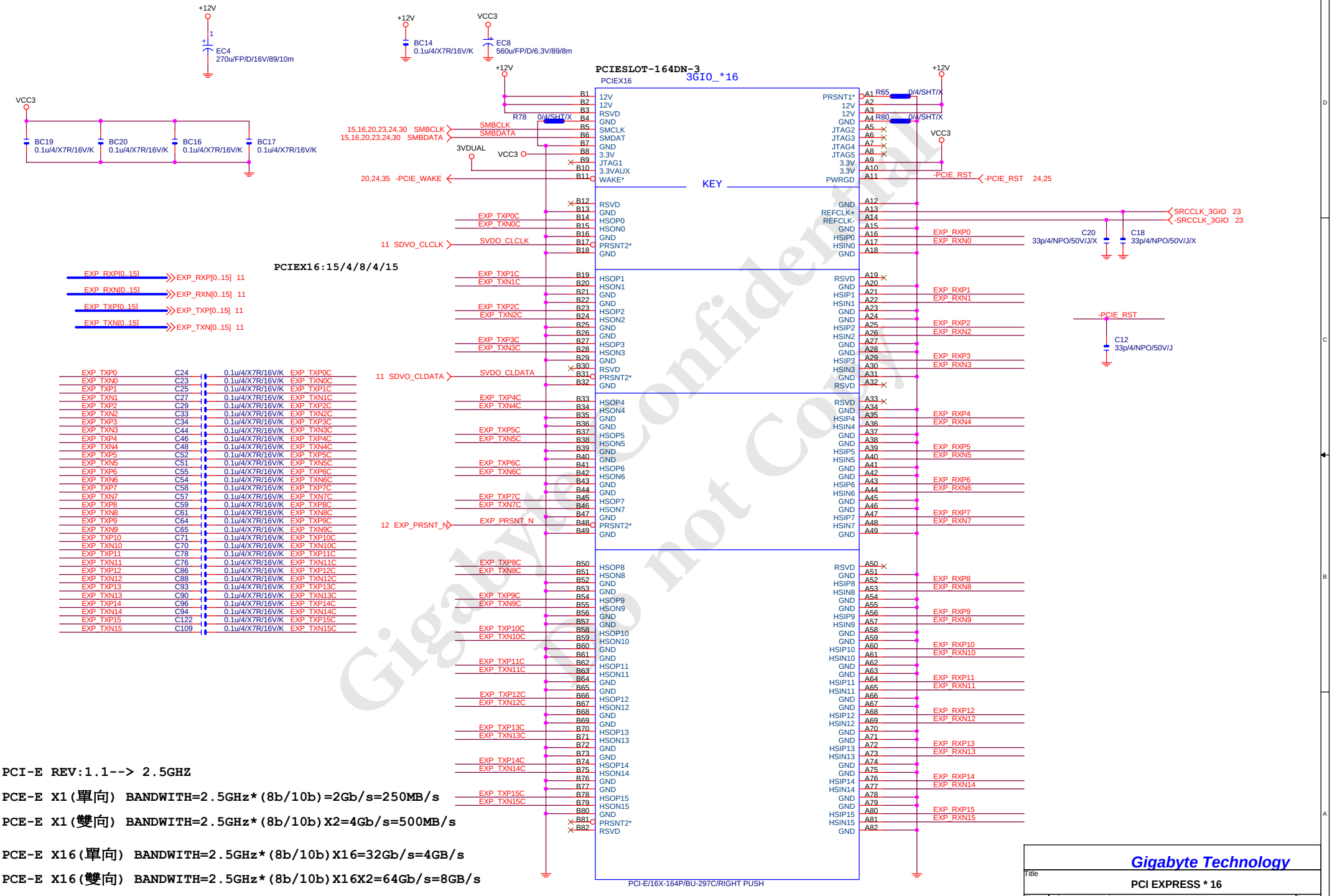

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

Gigabyte Technology		
Title	PCI EXPRESS * 16	
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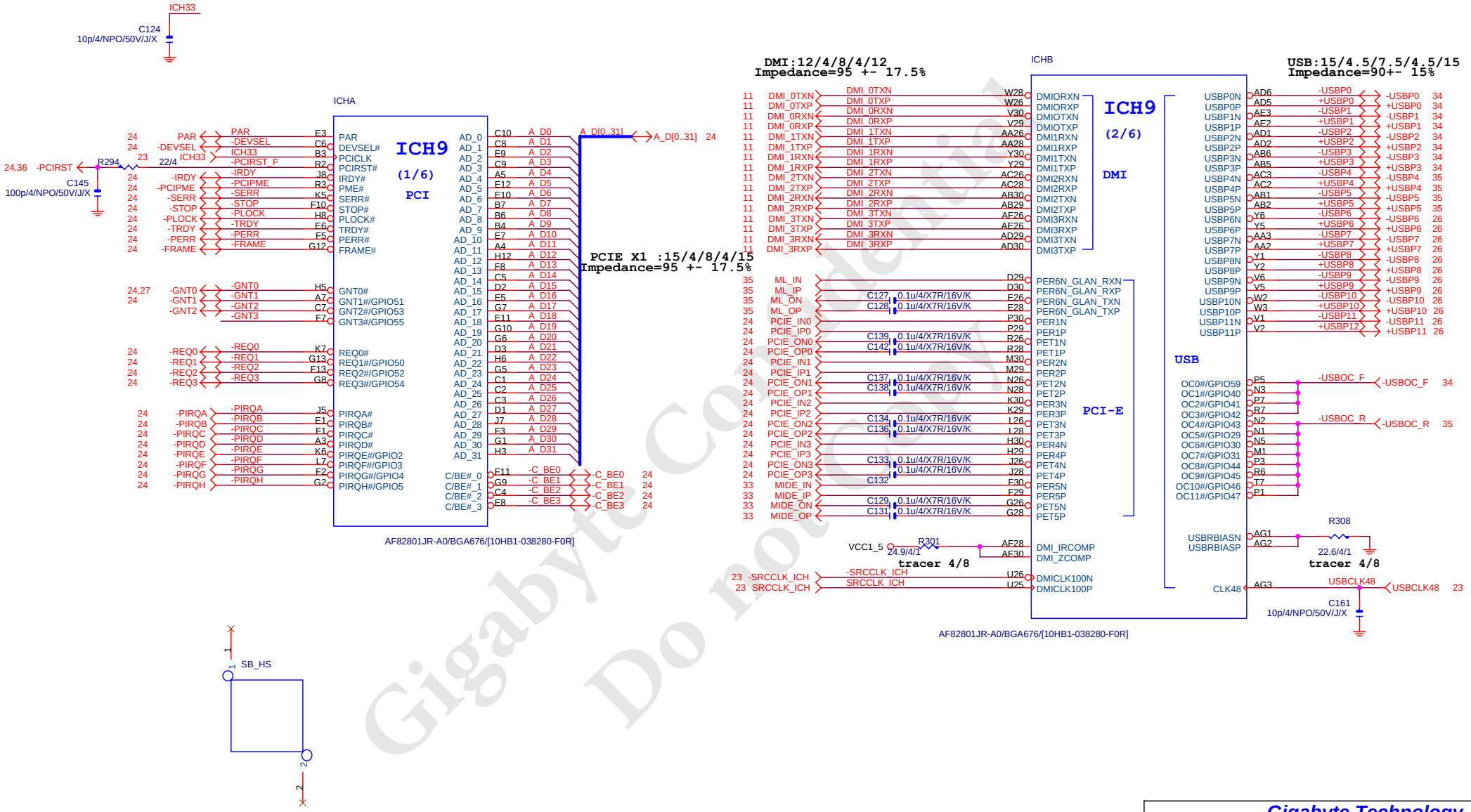

Gigabyte Technology		
Title	ICH9-PCI, DMI, LAN, USB	
Size B	Document Number GA-EP45T-UD3LR	Rev 1.3
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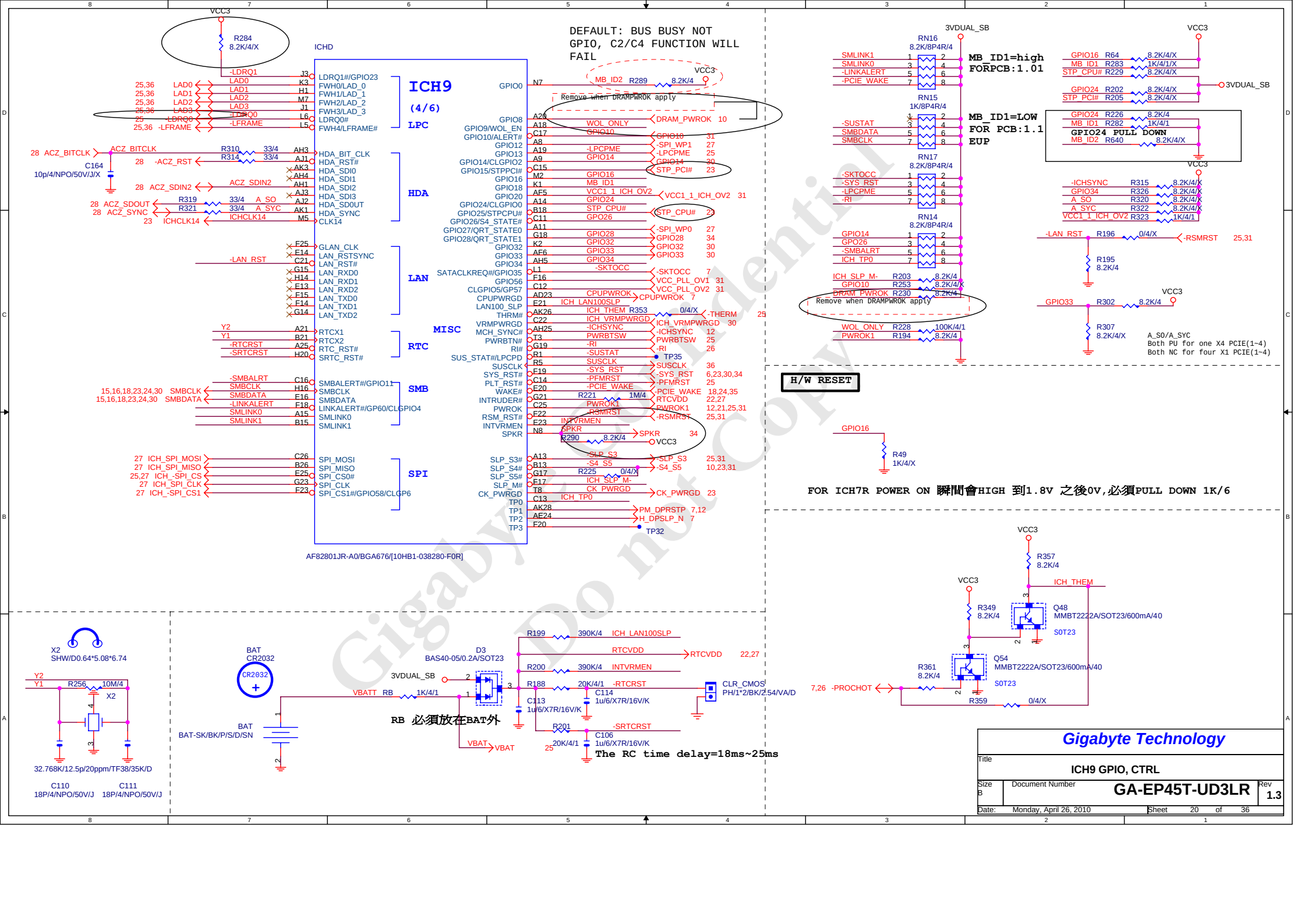

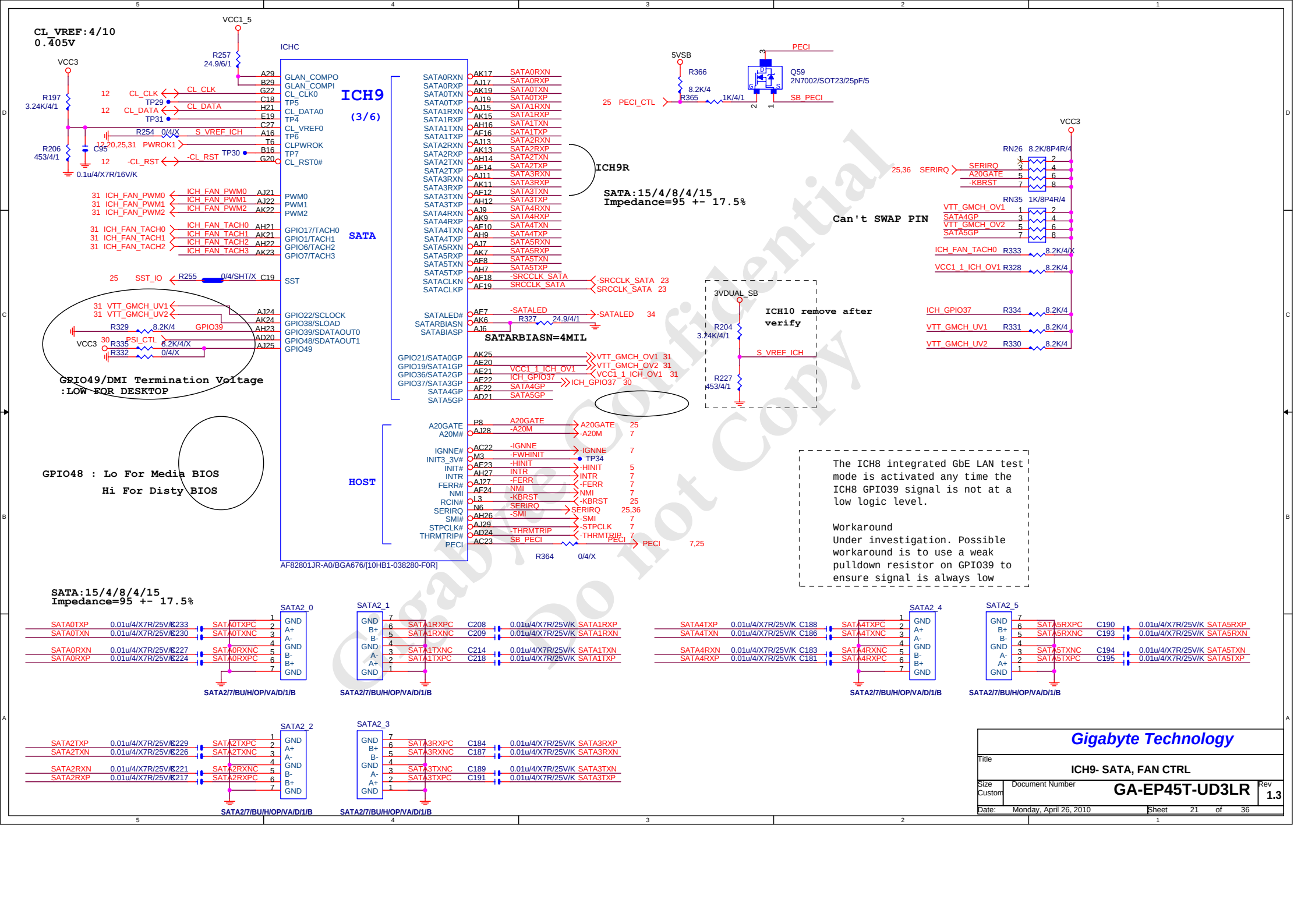

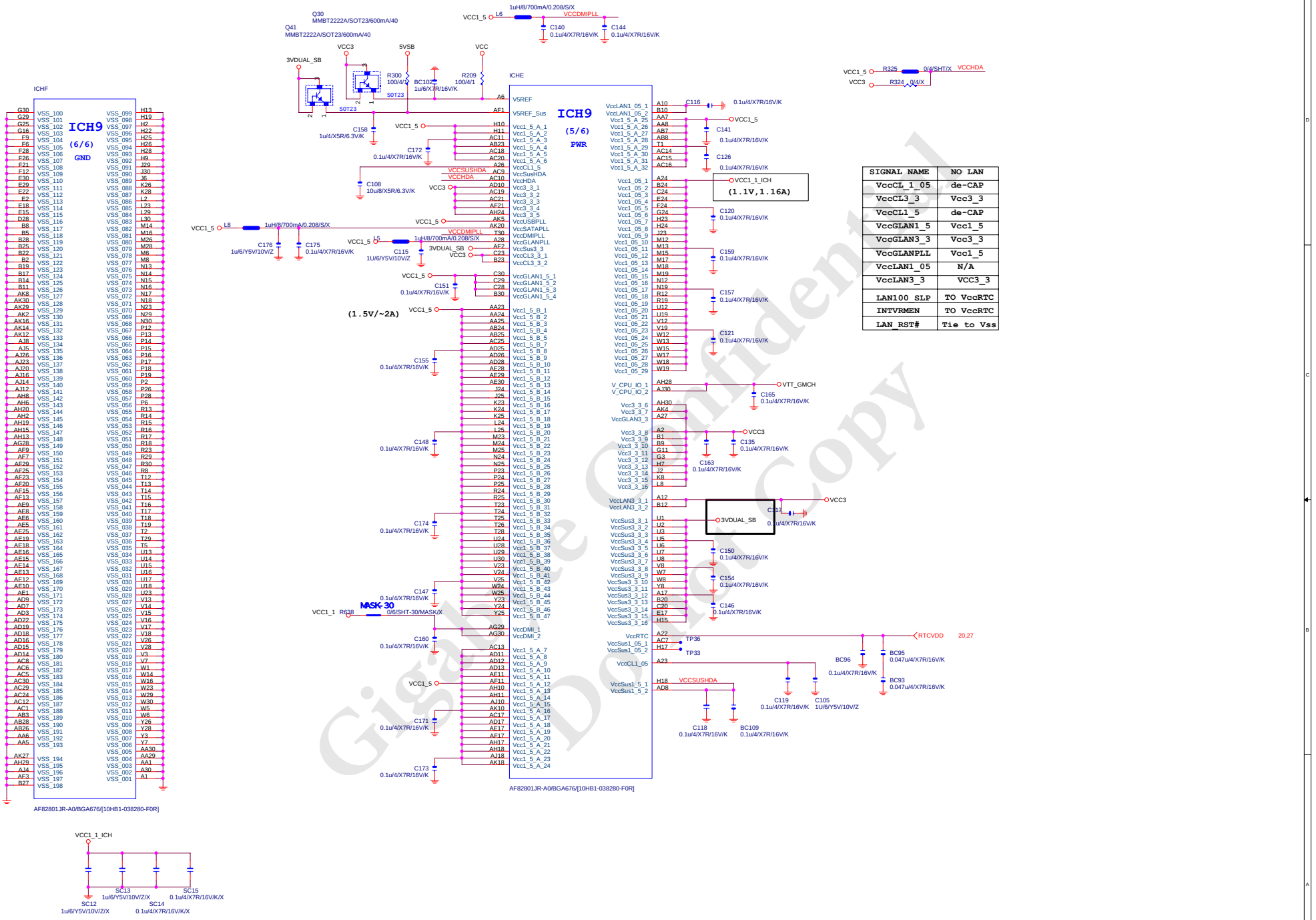

SIGNAL NAME	NO LAN
VccCL1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	VCC3_3
LAN100_SLP	TO VccRTC
INTVRMEN	TO VccRTC
LAN_RST#	Tie to Vss

Gigabyte Technology		
Title: ICH9-PWR & GND		
Size: C	Document Number: GA-EP45T-UD3LR	Rev: 1.3
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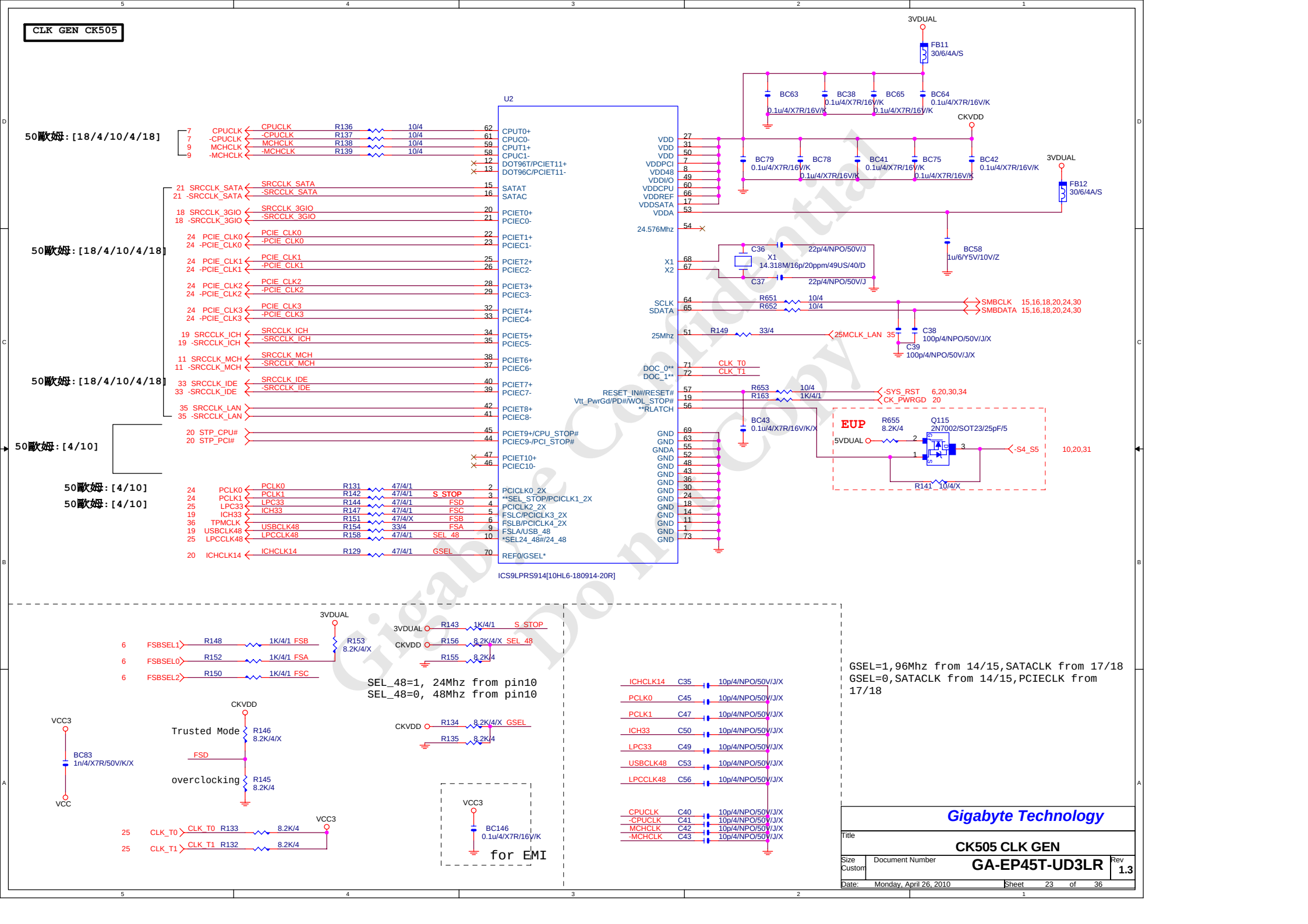

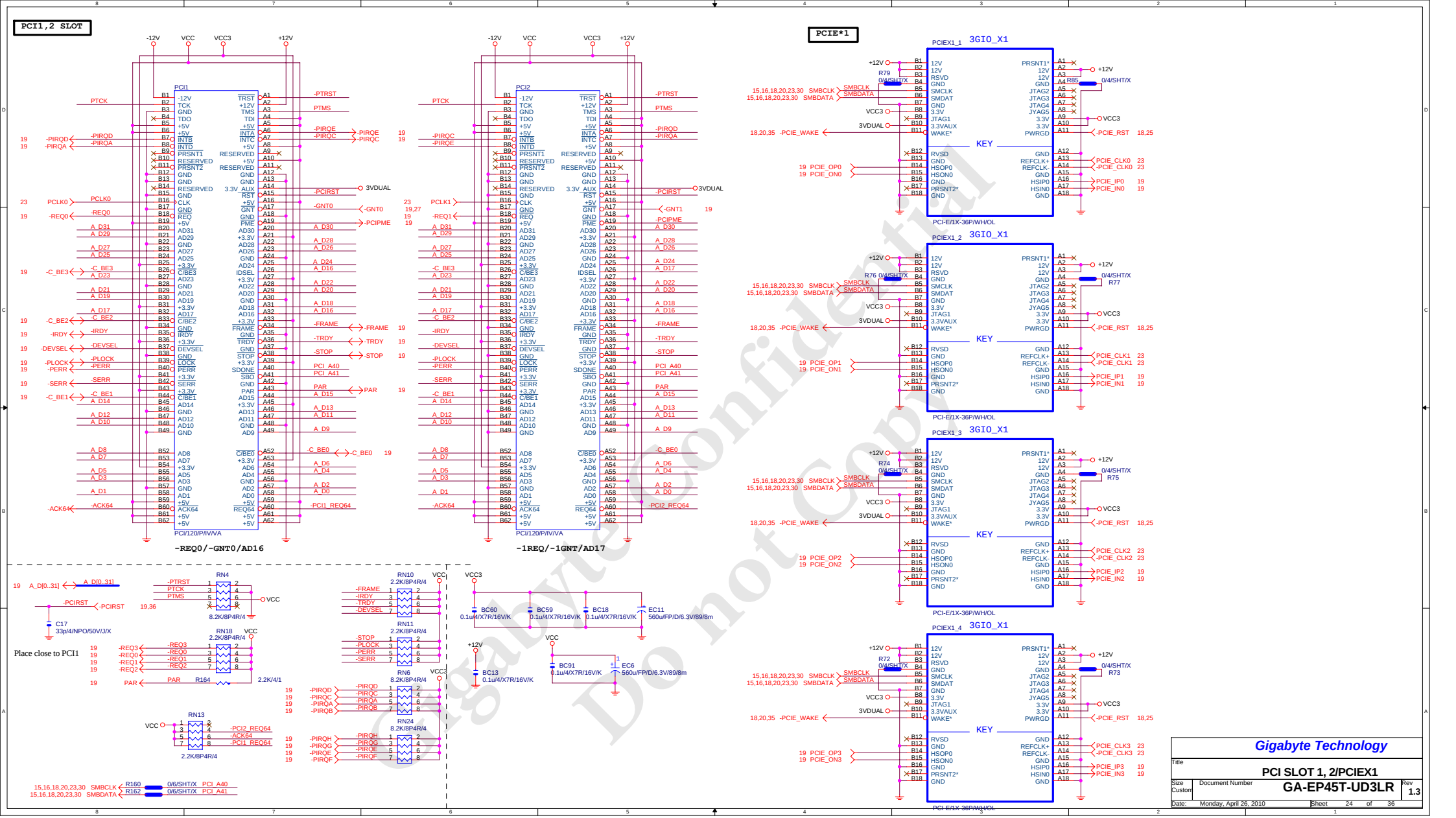
PCI1,2 SLOT
PCI1
PCI2
PCI120/P/IV/VA
-REQ0/-GNT0/AD16
-1REQ/-1GNT/AD17
PCIE*1
PCIEX1_1 3GIO_X1
PCIEX1_2 3GIO_X1
PCIEX1_3 3GIO_X1
PCIEX1_4 3GIO_X1
KEY
PCI-E/1X-36P/WH/OL
Place close to PCI1
Gigabyte Technology
PCI SLOT 1, 2/PCIEX1
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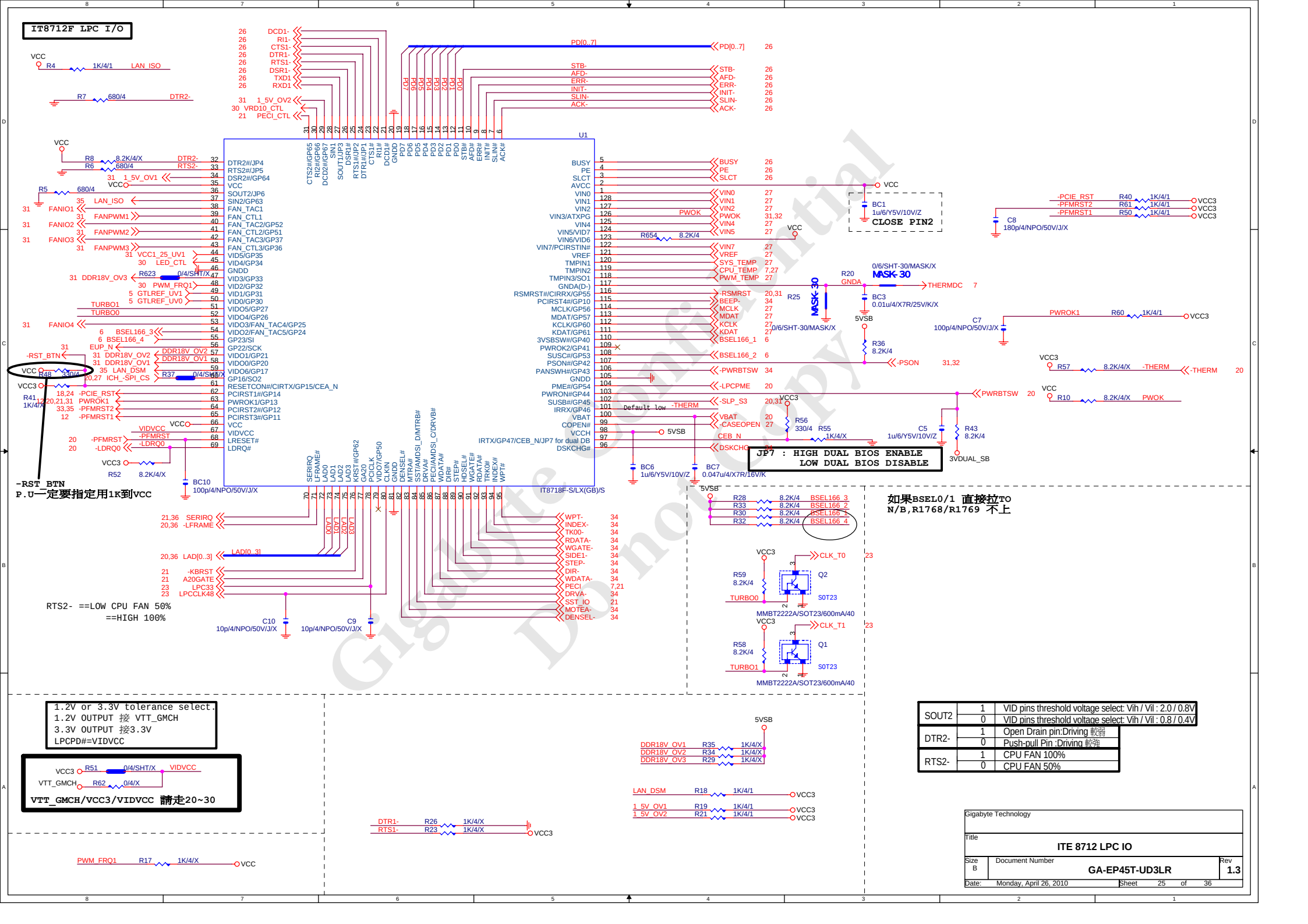
Gigabyte Confidential
Do not Copy


IT8712F LPC I/O
U1
IT8718F-S/LX(GB)/S
-RST_BTN
P.U一定要指定用1K到VCC
JP7 : HIGH DUAL BIOS ENABLE
LOW DUAL BIOS DISABLE
如果BSEL0/1 直接拉TO
N/B,R1768/R1769 不上
RTS2- ==LOW CPU FAN 50%
==HIGH 100%
1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接3.3V
LPCPD#=VIDVCC
VTT_GMCH/VCC3/VIDVCC 請走20~30
CLOSE PIN2
MASK-30
MMBT2222A/SOT23/600mA/40
SOUT2
DTR2-
RTS2-
VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V
Open Drain pin:Driving 較弱
Push-pull Pin :Driving 較強
CPU FAN 100%
CPU FAN 50%
Gigabyte Technology
ITE 8712 LPC IO
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1.3
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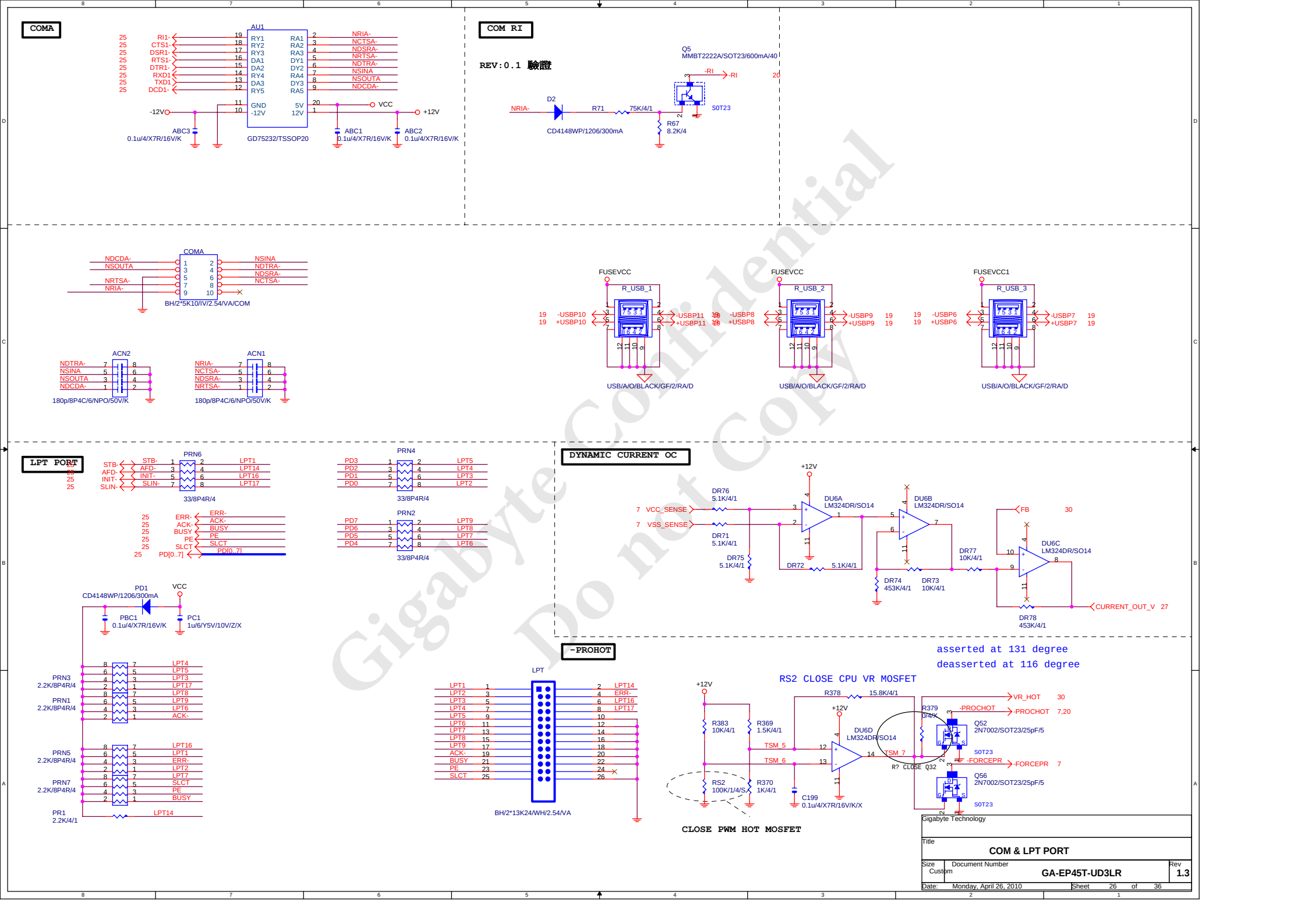
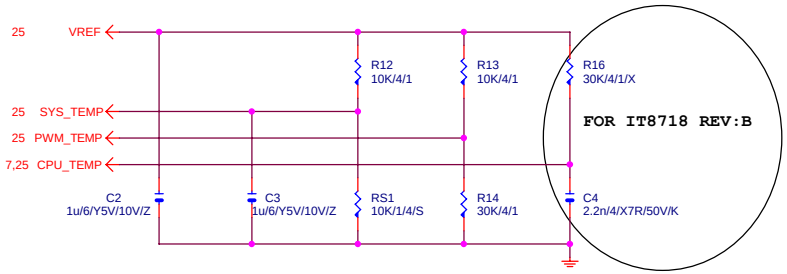
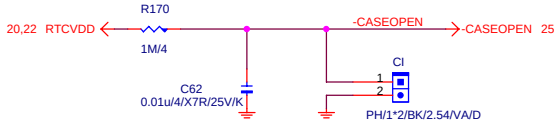
Do not Copy



TEMP H/W MONITOR

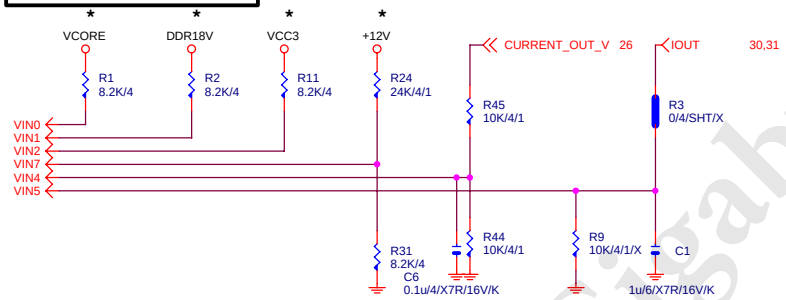


CASE OPEN

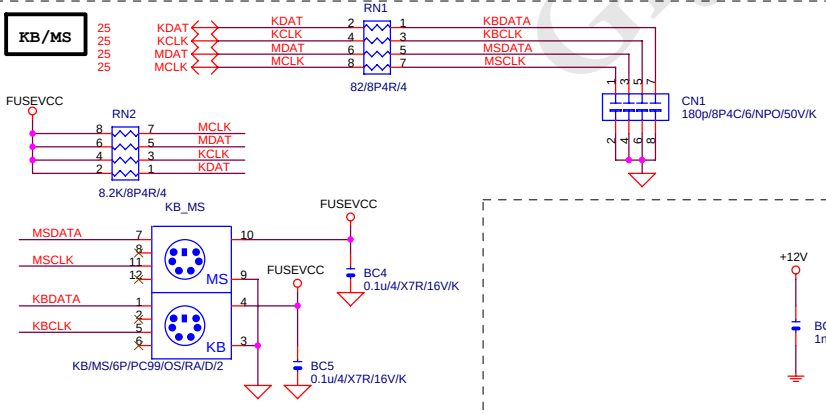


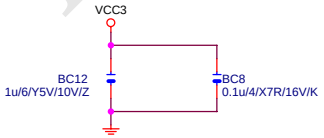
Case Open Circuits

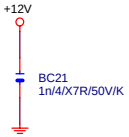
VOLTAGE-- H/W MONITOR

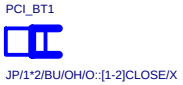


KB/MS









Gigabyte Technology		
Title: BIOS/HW-MONITOR/CI/KB/MS		
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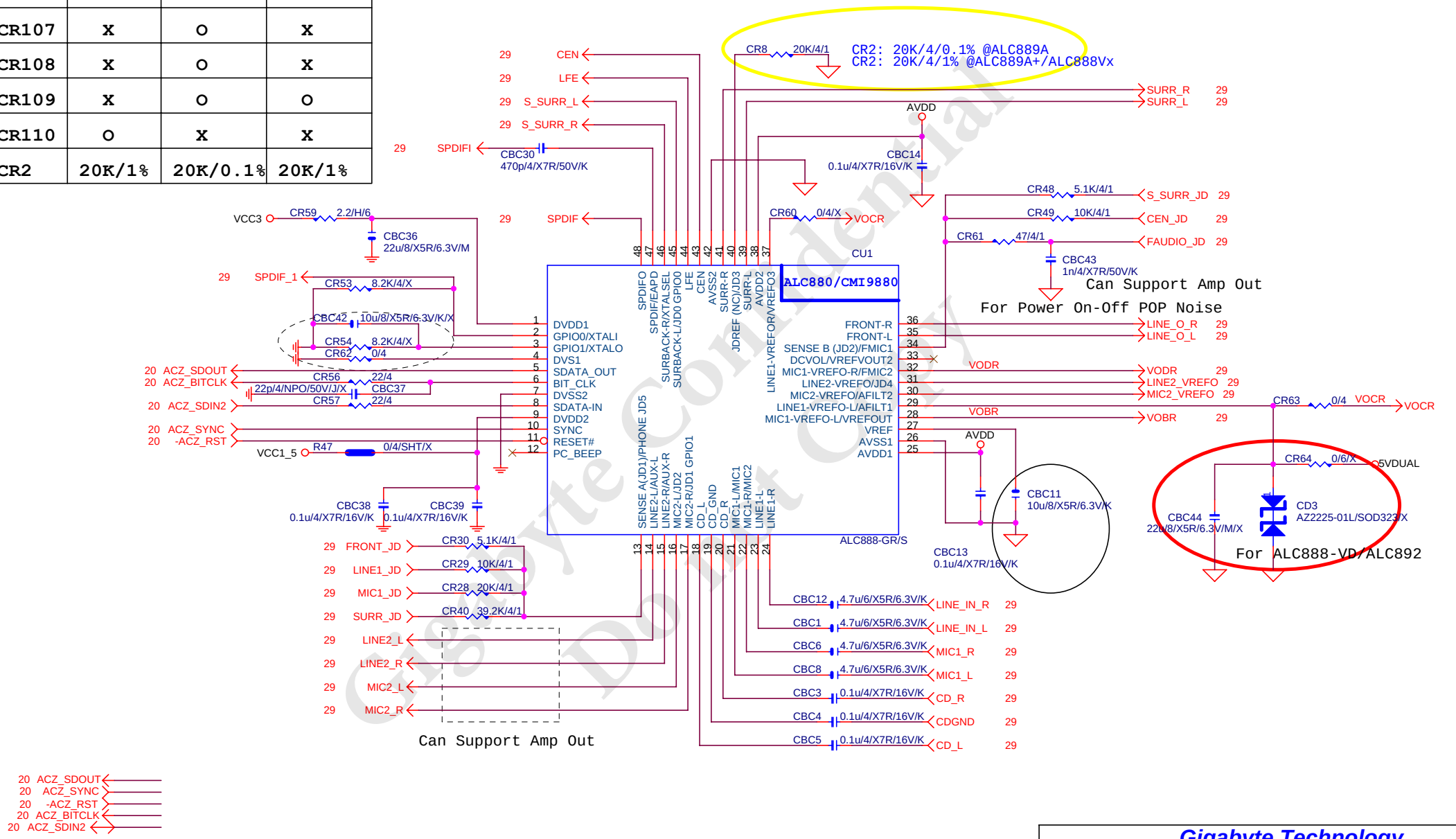
AZALIA CODEC *ALC889A+/ALC889A/ALC888Vx Colay*

	ALC889A+	ALC889A	ALC888Vx
CR107	X	O	X
CR108	X	O	X
CR109	X	O	O
CR110	O	X	X
CR2	20K/1%	20K/0.1%	20K/1%



Title	ALC888
Size / Custom	Document Number: GA-EP45T-UD3LR
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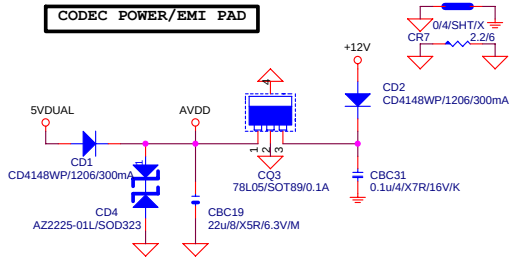
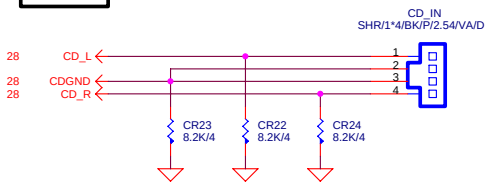
Gigabyte Technology

CODEC POWER/EMI PAD

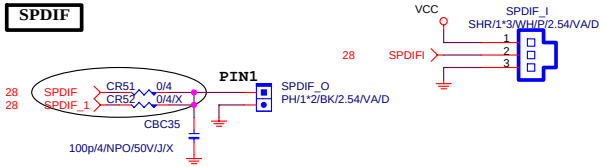


CO-LAYOUT

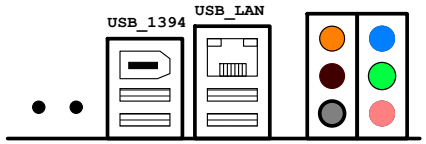
CD IN

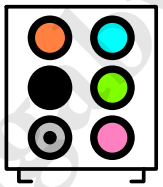


SPDIF



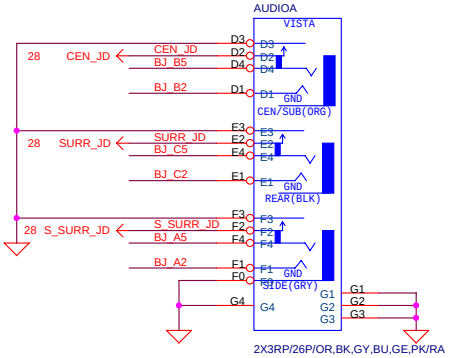
AZALIA JACK

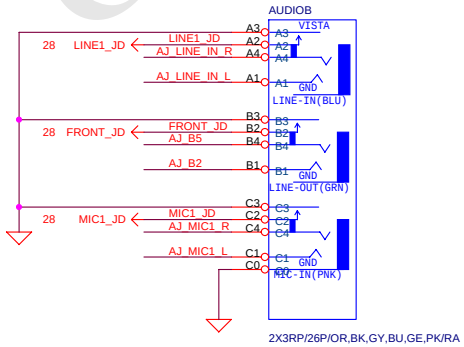




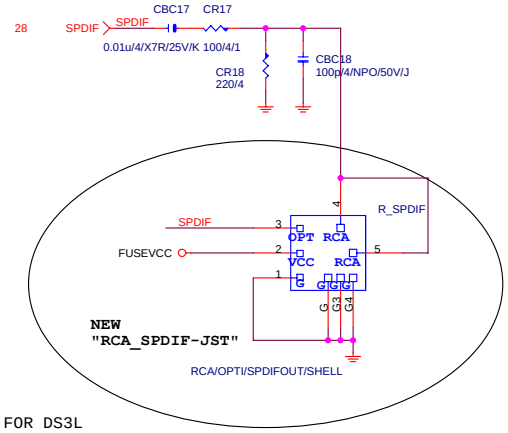
3RP/26P/OR,BK,GY,BU,GE,PK/RA/D/1/B

VISTA規範:REAR-->BLK,CEN/SUB-->ORG





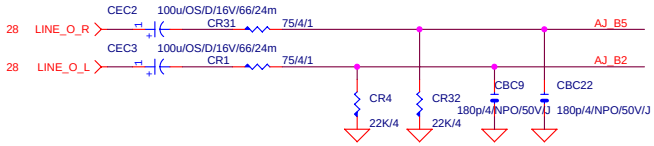
Fpr
EMI



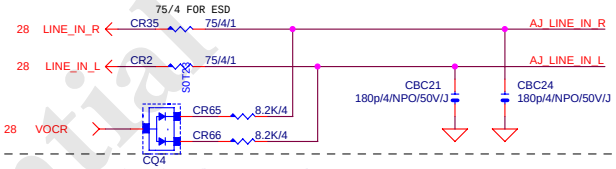
FOR DS3L
11NR6-402030-41R(無鐵殼)11NR6-402030-51R/52R(鐵殼)

FOR S3L 11NR6-501004-G1R ONLY support RCA

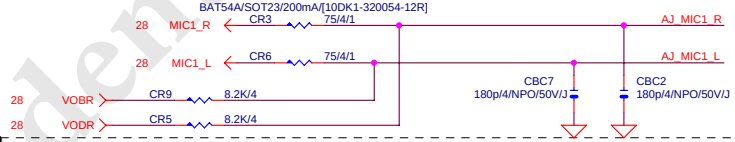
LINE-OUT



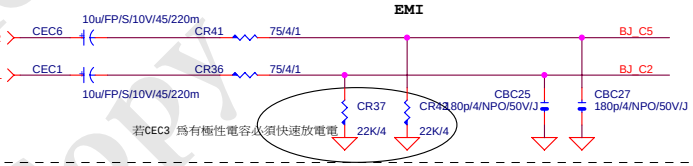
LINE-IN



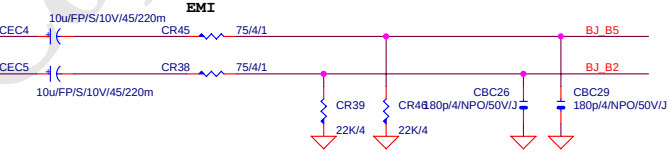
MIC-IN



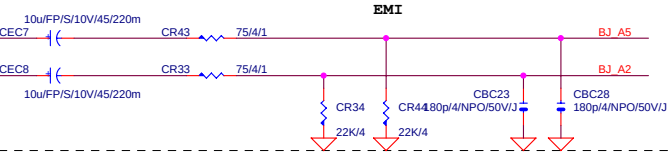
SURROUND



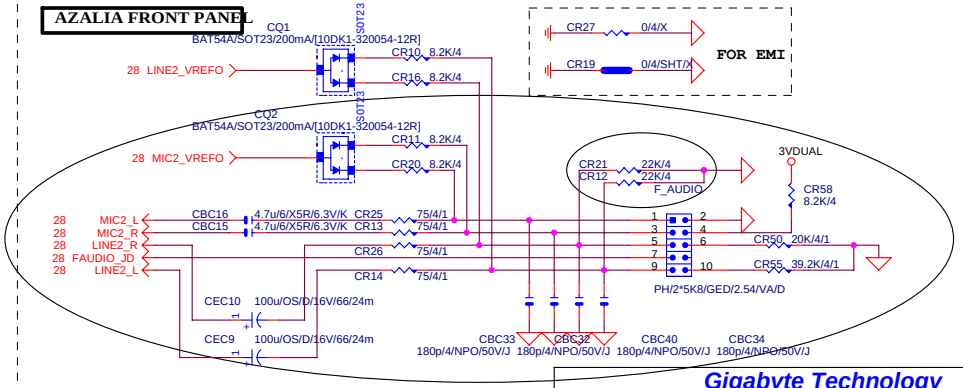
CEN/LFE



SURR BACK



AZALIA FRONT PANEL



Gigabyte Technology

Title: AUDIO JACK

Size: Custom | Document Number: GA-EP45T-UD3LR | Rev: 1.3

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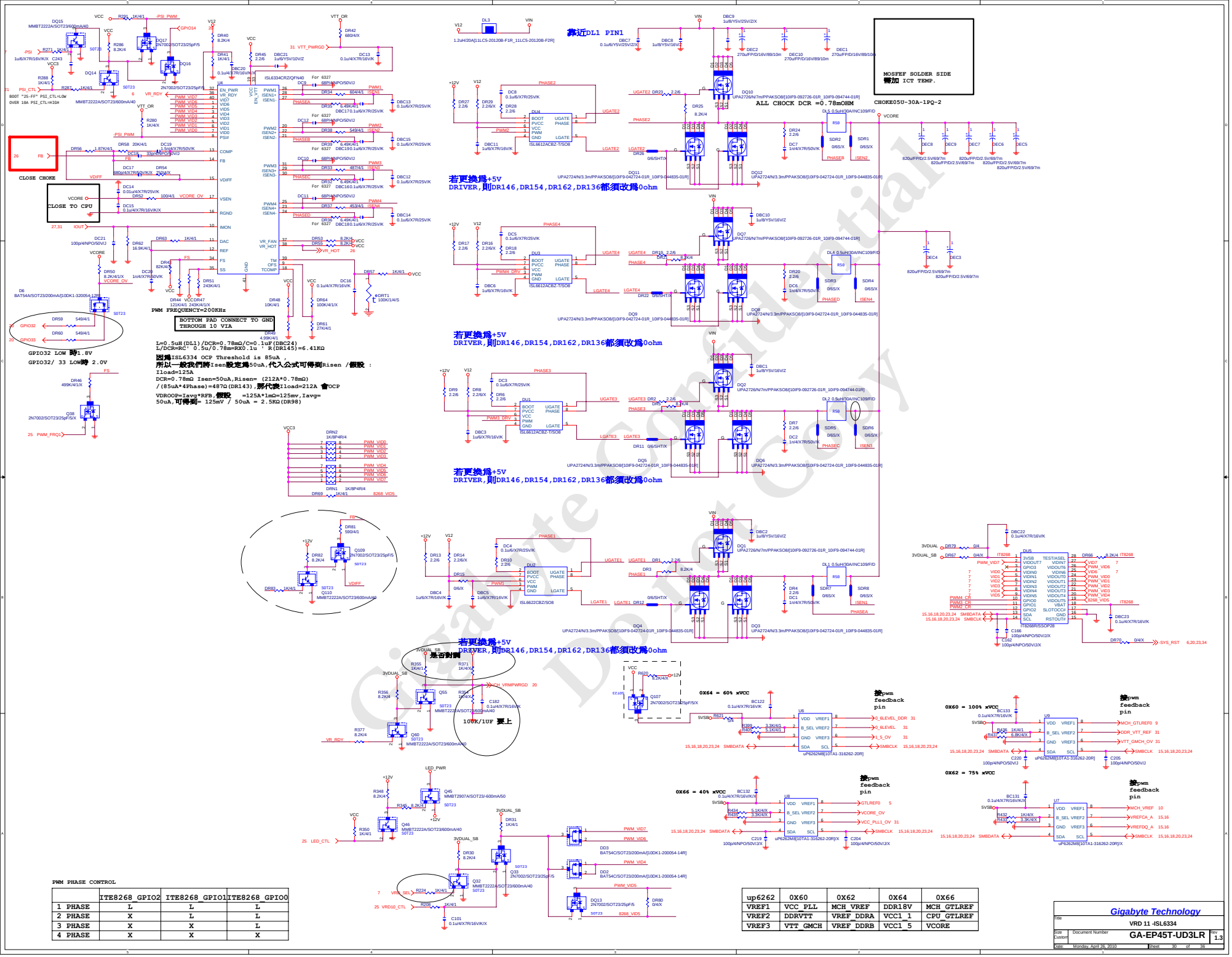
靠近DL1 PIN1
MOSFET SOLDER SIDE
需加 ICT TEMP.
CHOKE05U-30A-1PQ-2
ALL CHOCK DCR =0.78mOHM
若更換爲+5V DRIVER,則DR146,DR154,DR162,DR136都須改爲0ohm
CLOSE CHOKE
CLOSE TO CPU
BOTTOM PAD CONNECT TO GND THROUGH 10 VIA
PWM FREQUENCY=200KHz
GPIO32 LOW 時1.8V
GPIO32/ 33 LOW時 2.0V
L=0.5uH(DL1)/DCR=0.78mΩ/C=0 1uF(DBC24)
L/DCR=RC' 0.5u/0.78m=RX0.1u ' R(DR145)=6.41KΩ
因爲ISL6334 OCP Threshold is 85uA ,
所以一般我們將Isen設定爲50uA,代入公式可得到Risen /設設 :
Iload=125A
DCR=0.78mΩ Isen=50uA,Risen= (212A*0.78mΩ)
/(85uA*4Phase)=487Ω(DR143),那代表Iload=212A 會OCP
VDROOP=Iavg*RFB, 假設 =125A*1mΩ=125mv,Iavg=
50uA,可得到= 125mV / 50uA = 2.5KΩ(DR98)
是否對調
100K/10F 要上
0X64 = 60% xVCC
0X60 = 100% xVCC
0X62 = 75% xVCC
0X66 = 40% xVCC
接pwm feedback pin
PWM PHASE CONTROL
ITE8268_GPIO2 ITE8268_GPIO1 ITE8268_GPIO0
1 PHASE L L L
2 PHASE X L L
3 PHASE X X L
4 PHASE X X X
up6262 0X60 0X62 0X64 0X66
VREF1 VCC_PLL MCH_VREF DDR18V MCH_GTLREF
VREF2 DDRVTT VREF_DDRA VCC1_1 CPU_GTLREF
VREF3 VTT_GMCH VREF_DDRB VCC1_5 VCORE
Gigabyte Technology
VRD 11 -ISL6334
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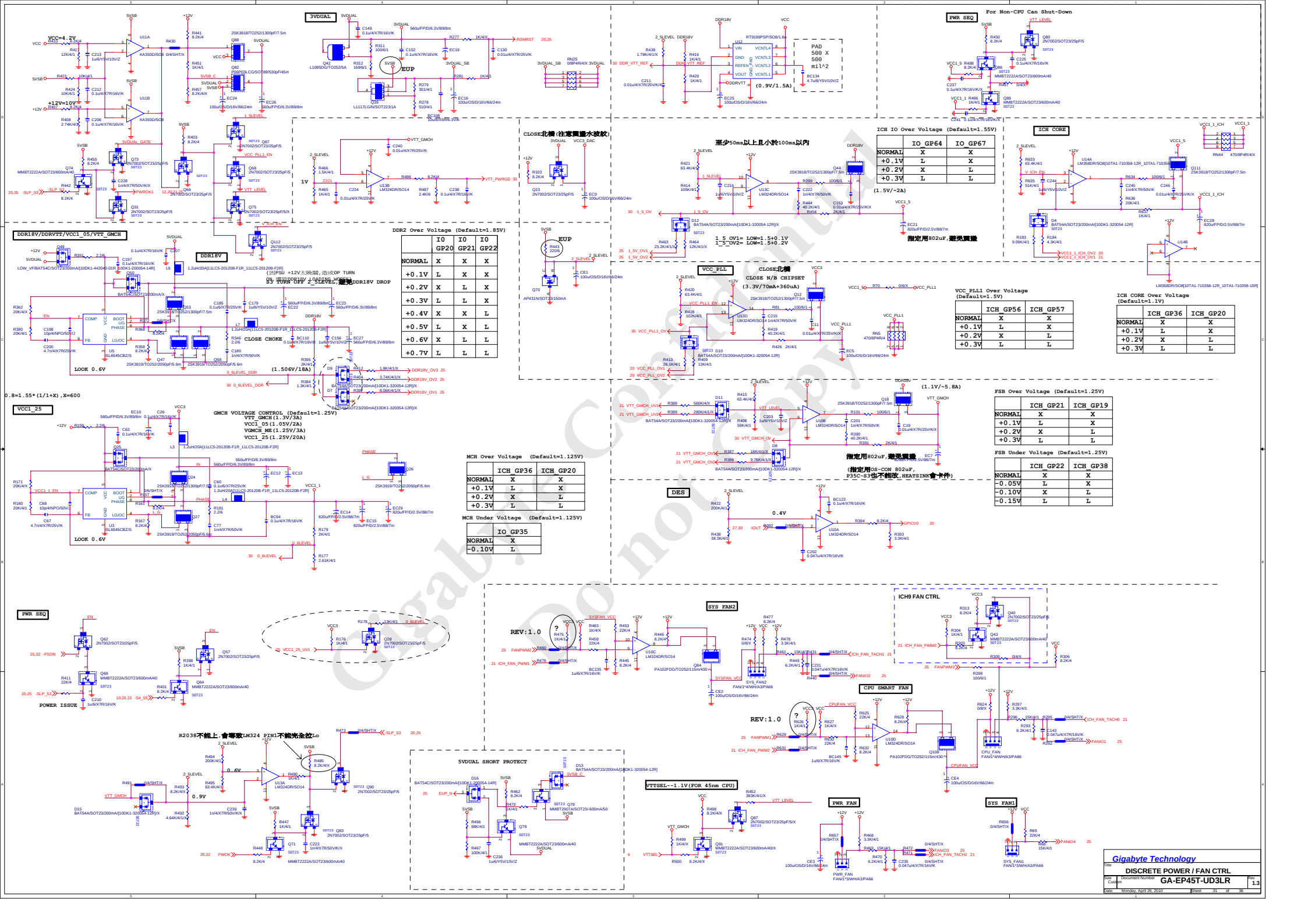
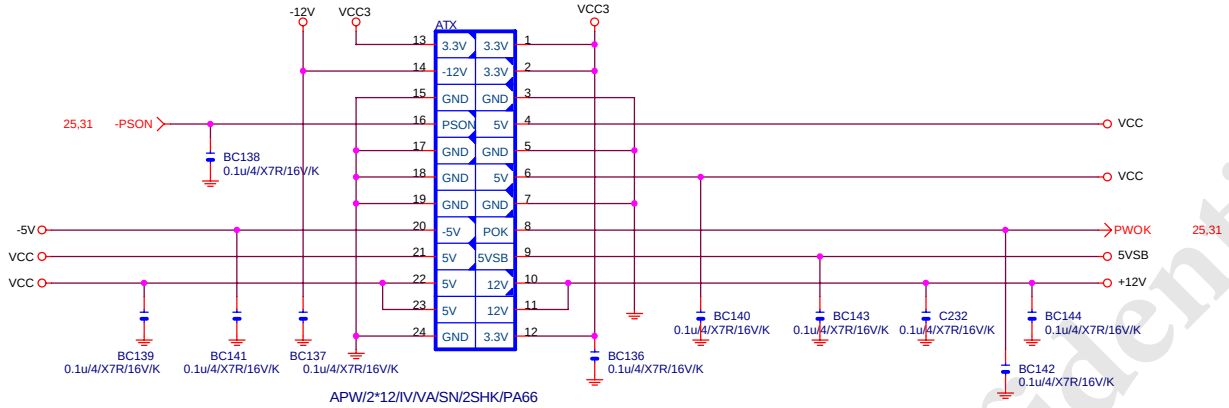
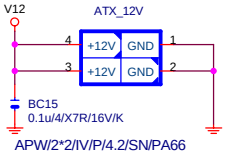
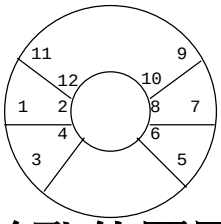
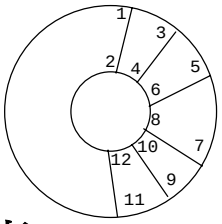


ATX POWER CONNECTOR

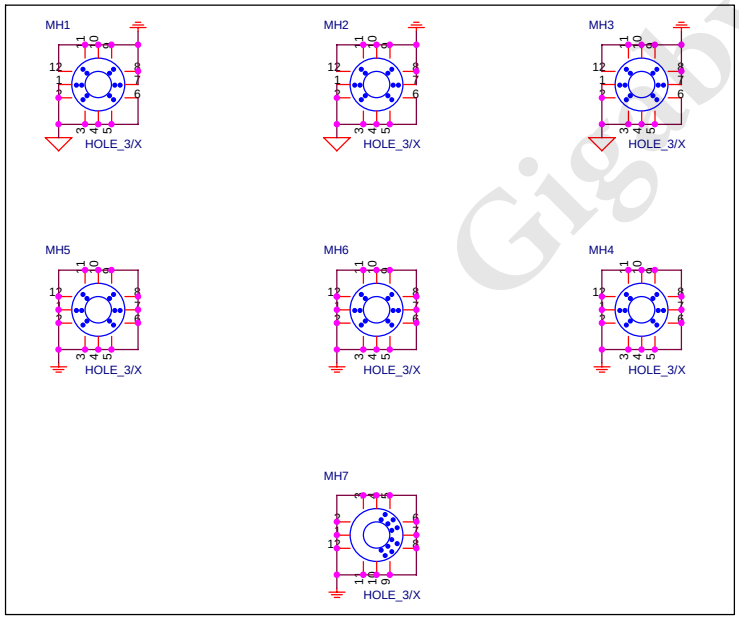


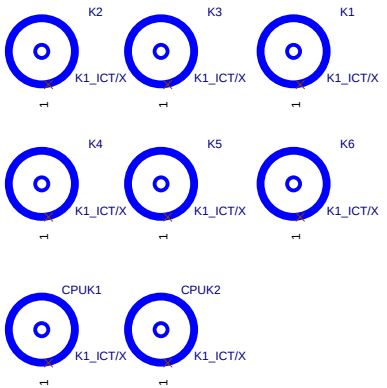


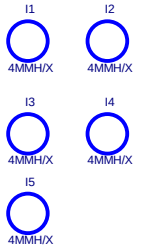




螺絲孔位置圖 (注意Footprint不同)







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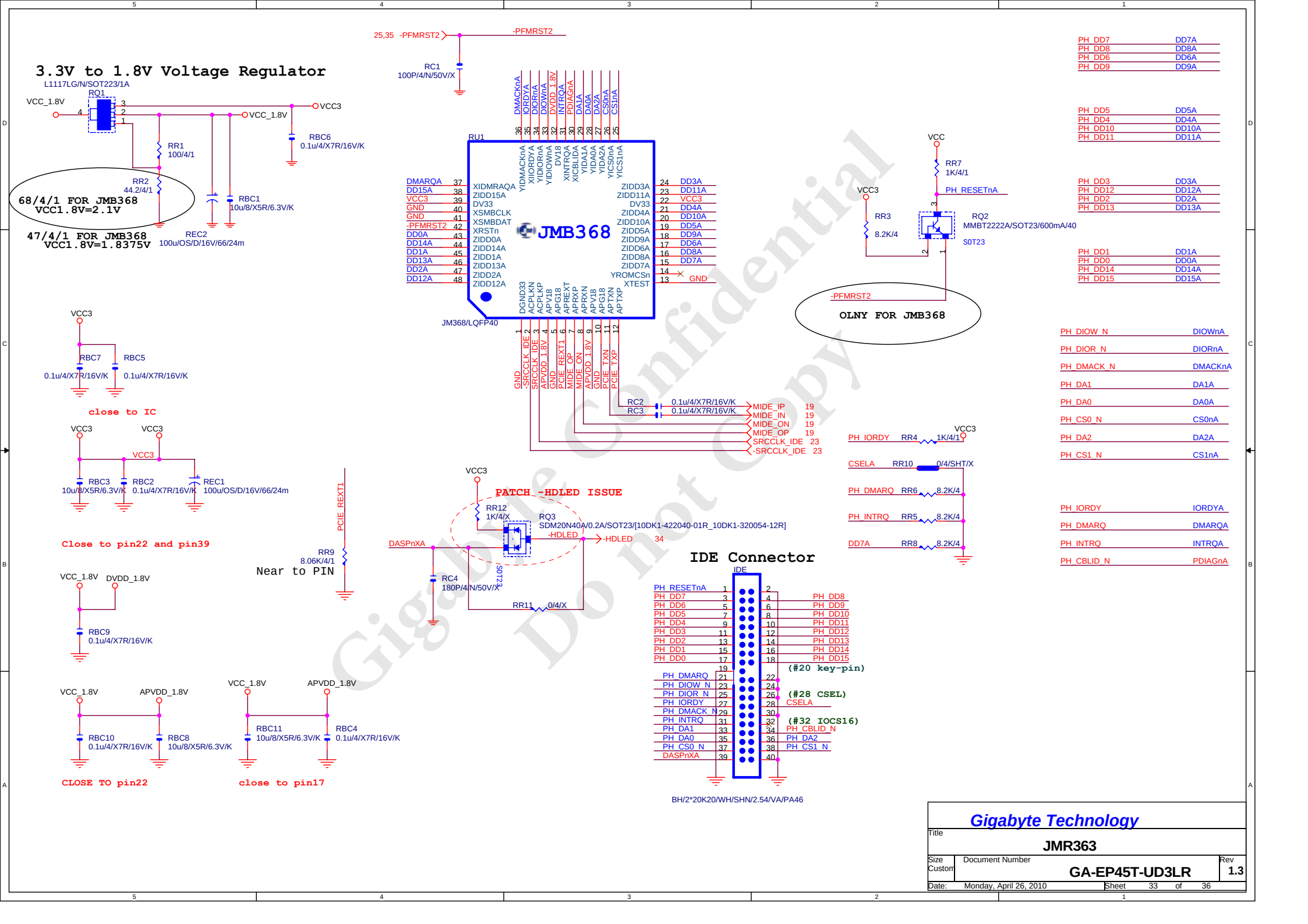

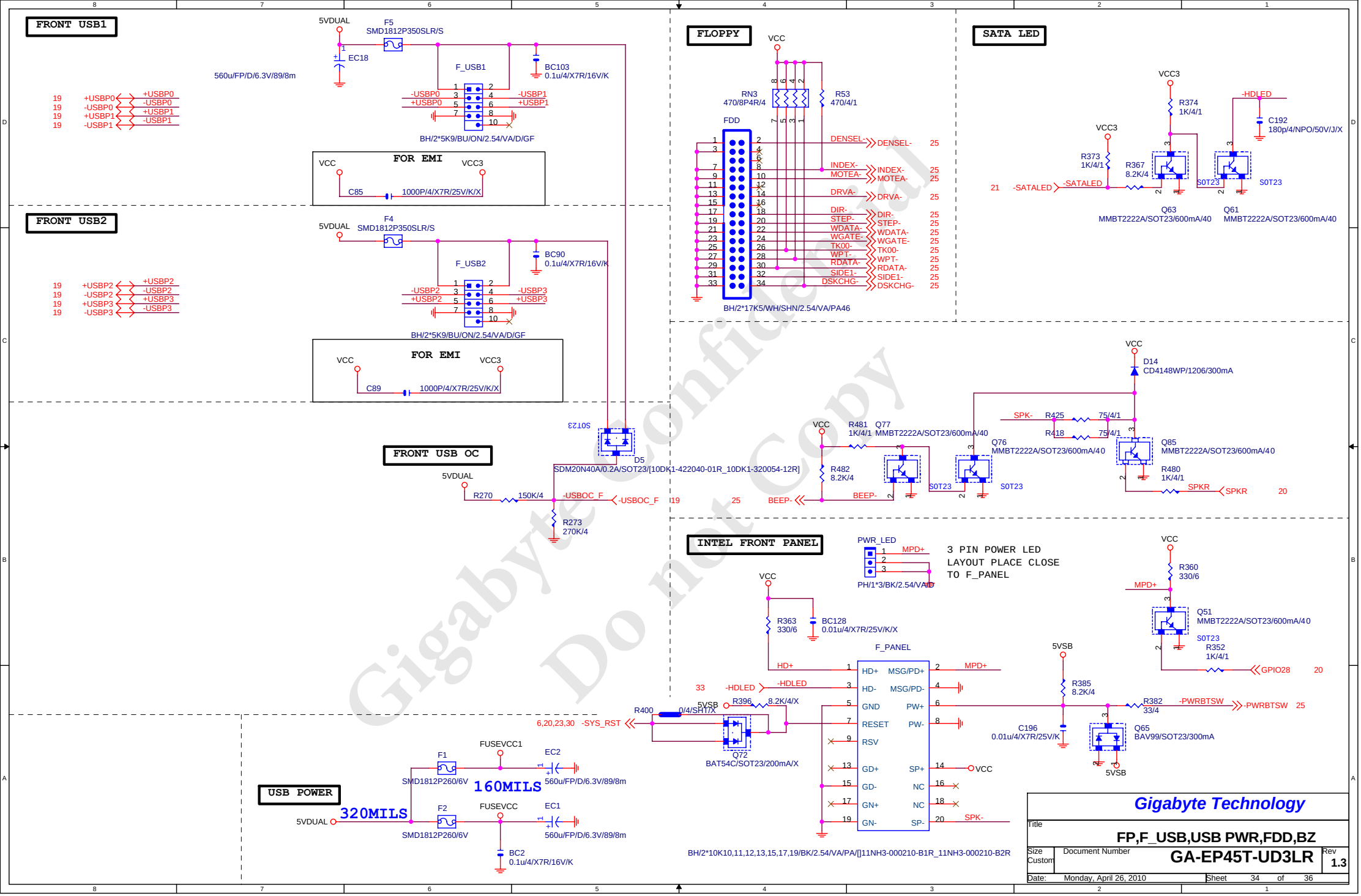

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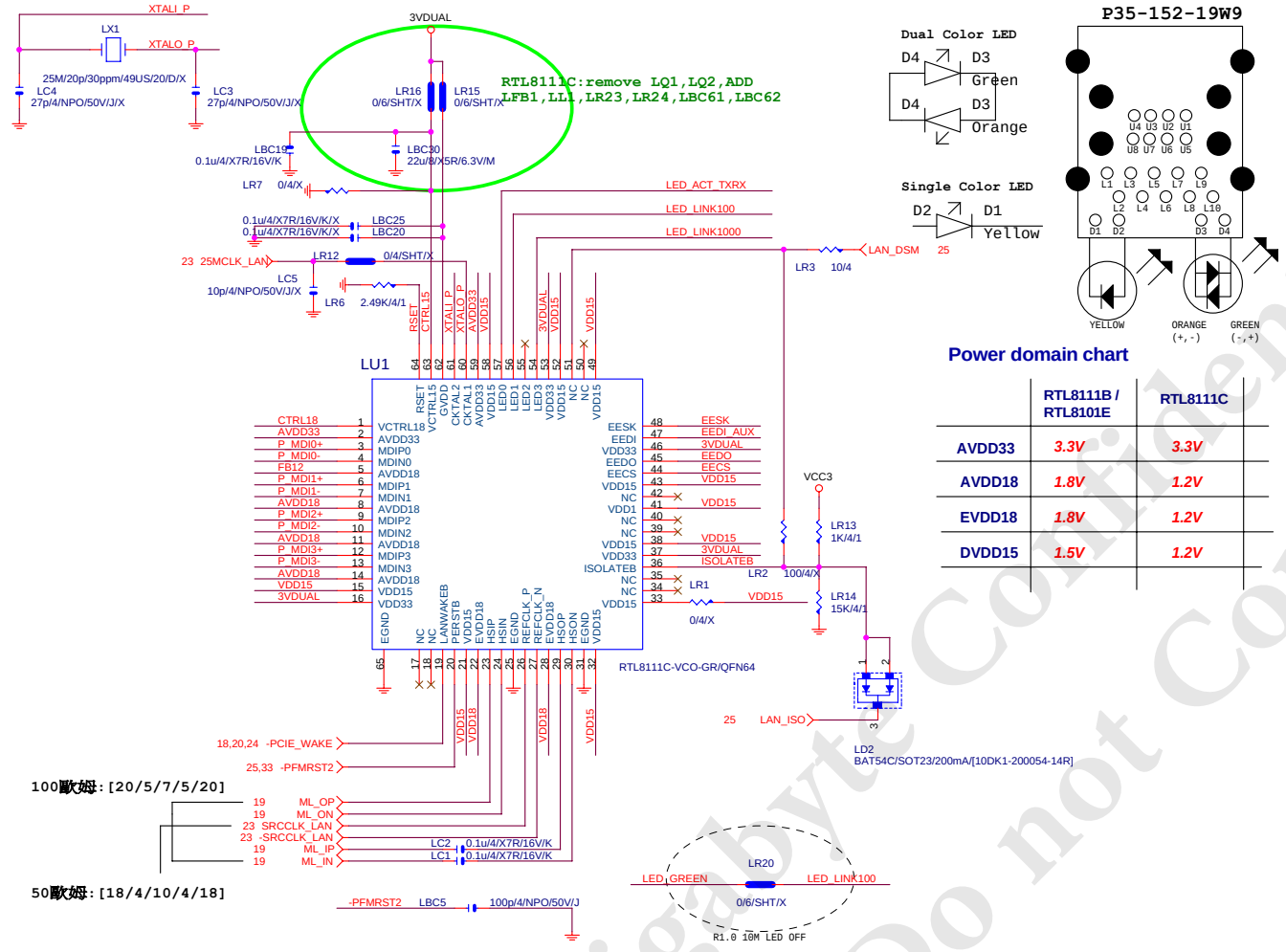


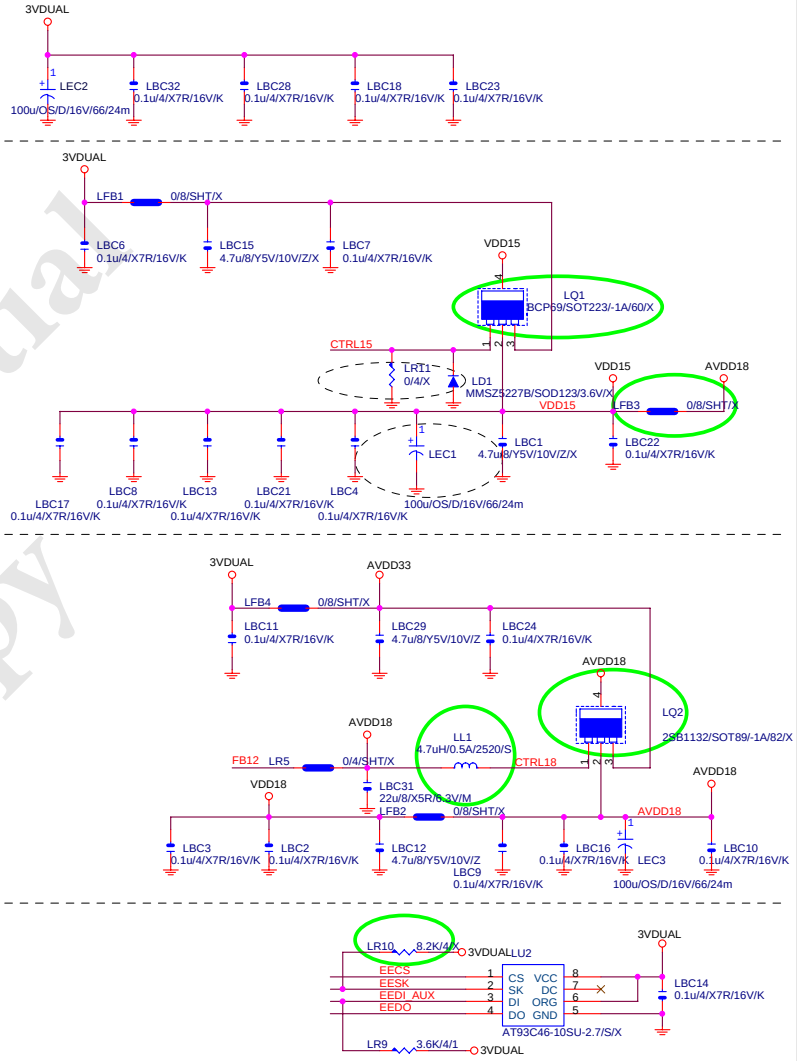
Dual Color LED

Single Color LED

P35-152-19W9

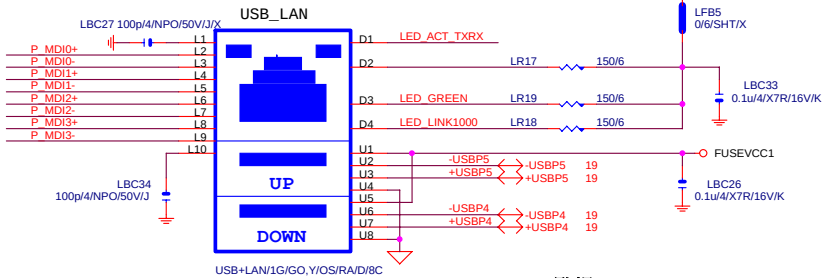
Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V



USB_LAN CONNECTOR

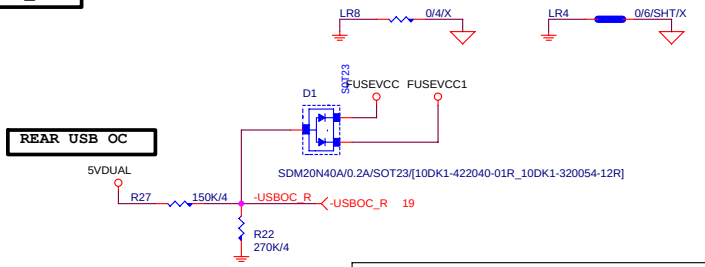
LAN 100歐姆:[30/4/8/4/30] FOR B 製程



USB POWER

90歐姆:[15/4.5/7.5/4.5/15]

USB_LAN



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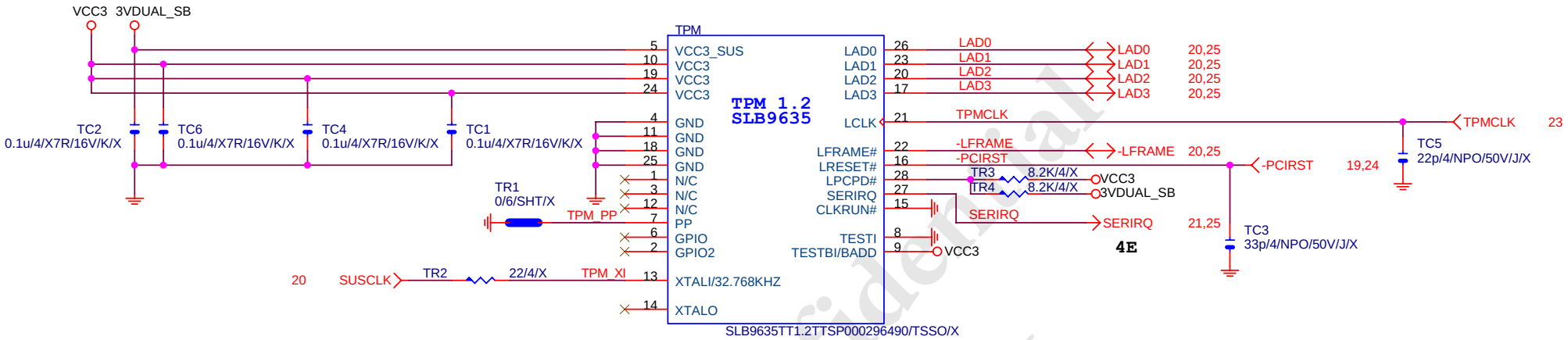

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