Bumblebee (LBB-2)
Cometlake-U Schematics

Project Code: 4PD0JH010001
PCB(Raw Card): 19733-1

2020-03-03

Properties of DUMMY: (BOM Control Parts)

Value	Description
(No Value)	ASM, assemble
DY	DUMMY, NOT ASM, not assemble
ZZ (No Need to Display)	ZZ parts for testpoint / shortpad / hole
PCBID	PCB ID for SW Team (PCB number)
SKUID	SKU ID for SW Team (CPU Type: non-vPro / vPro)
MEM_IDx_0 / MEM_IDx_1 (x = 0~4)	Memory ID for SW Team (0 = Low / 1 = High Level)
DDR4_CTRL	Memory Packaging Technology setting (SDP / DDP)
SDP / DDP	Number of identical die in package (1 = SDP, 2 = DDP)
APS / ISH / LPC / XDP	Debug Connectors (Assemble in 1st build only)
EMC	Follow EMC Team requested
NON_PSL / PSL	Support / Non Support KBC Power Switched Logic
WLAN_PCIe / WLAN_CNVi	Support WLAN type (PCIe or CNVi interface)
CHARGER_HS / CHARGER_LS	Charger High / Low Side MOSFET
VCCSA_HS / VCCSA_LS	VCCSA High / Low Side MOSFET

LBB-2

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Title: **COVER PAGE**		
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Bumblebee-2 Cometlake Block Diagram

Project Code: 4PD0JH010001
PCB(Raw Card): 19733-1

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DESCRIPTION

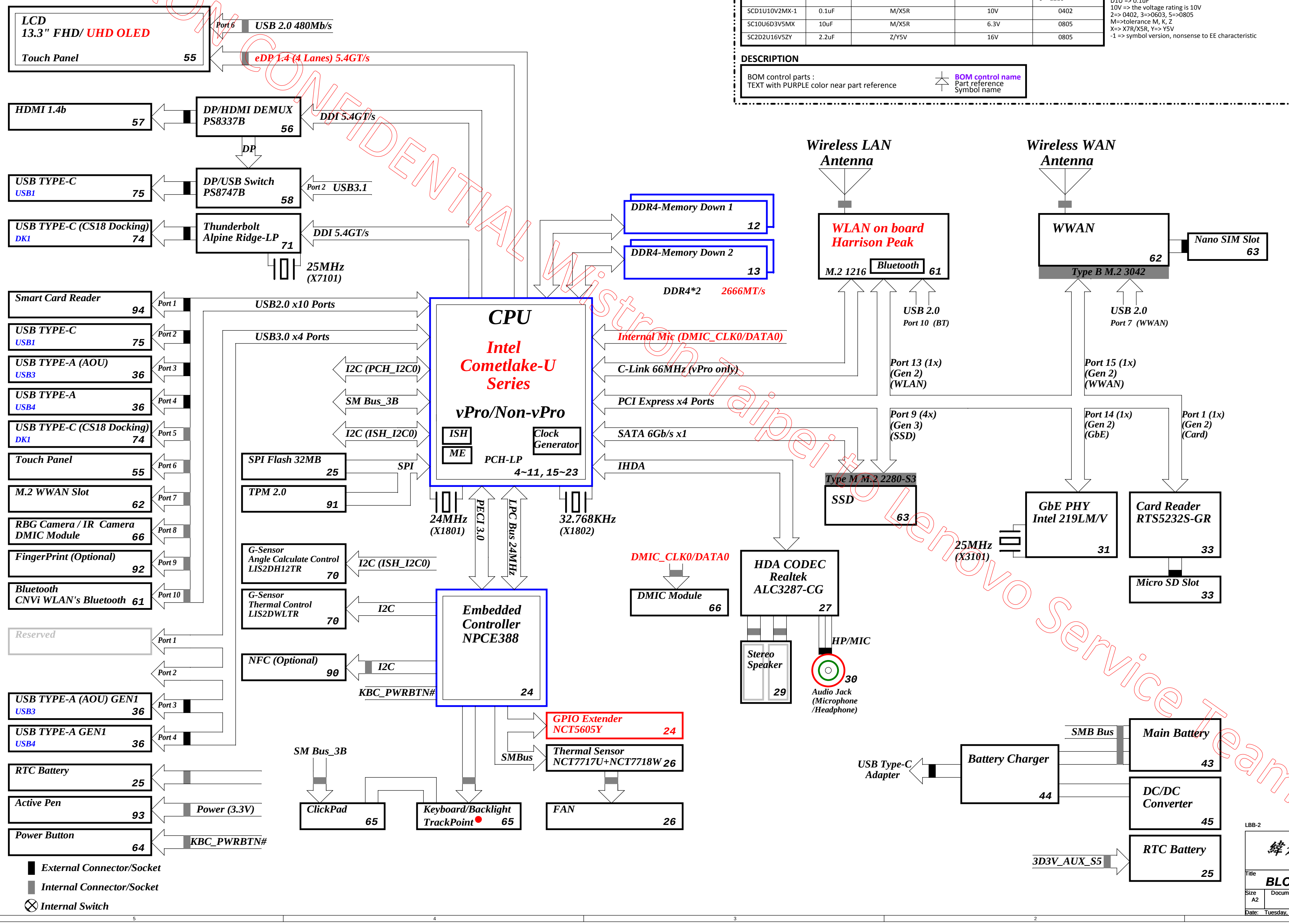
BOM control parts :
TEXT with PURPLE color near part reference

BOM control name
Part reference
Symbol name

PCB Layer Stackup

L1:Component
L2:GND
L3:Signal 1
L4:VCC
L5:Signal 2
L6:Signal 3
L7:GND
L8:Signal 4
L9:GND
L10:Component

Battery Charger/Selector BQ25700ARSNR 44	
VINT20_IN	19V_DCBATOUT BT+
System DC/DC TPS51285B 45	
19V_DCBATOUT	5V_S5 3D3V_S5
DC/DC IMVP8 NCP81218PMNTXG 46	
DC/DC VCCCPUCORE NCP302045LMNTXG 47	
19V_DCBATOUT	1V_CPU_CORE
DC/DC VCCGT NCP302045LMNTXG 48	
19V_DCBATOUT	1V_VCCGT
DC/DC VCCSA NCP81253MNTBG 50	
19V_DCBATOUT	1V_VCCSA
DC/DC 1D2V_S3 NB687GQ-C669-Z 51	
19V_DCBATOUT	1D2V_S3
DC/DC 0D6V_VREF_S0 NB687GQ-C669-Z 51	
1D2V_S3	0D6V_VREF_S0
DC/DC 2D5V_S3 NB687GQ-C669-Z 51	
3D3V_S5	2D5V_S3
DC/DC 1D05V_SUS RT8237CZQW 52	
19V_DCBATOUT	1D05V_SUS
DC/DC 1D8V_SUS RT5797ALGQW 53	
3D3V_S5	1D8V_SUS



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Title			
BLOCK DIAGRAM			
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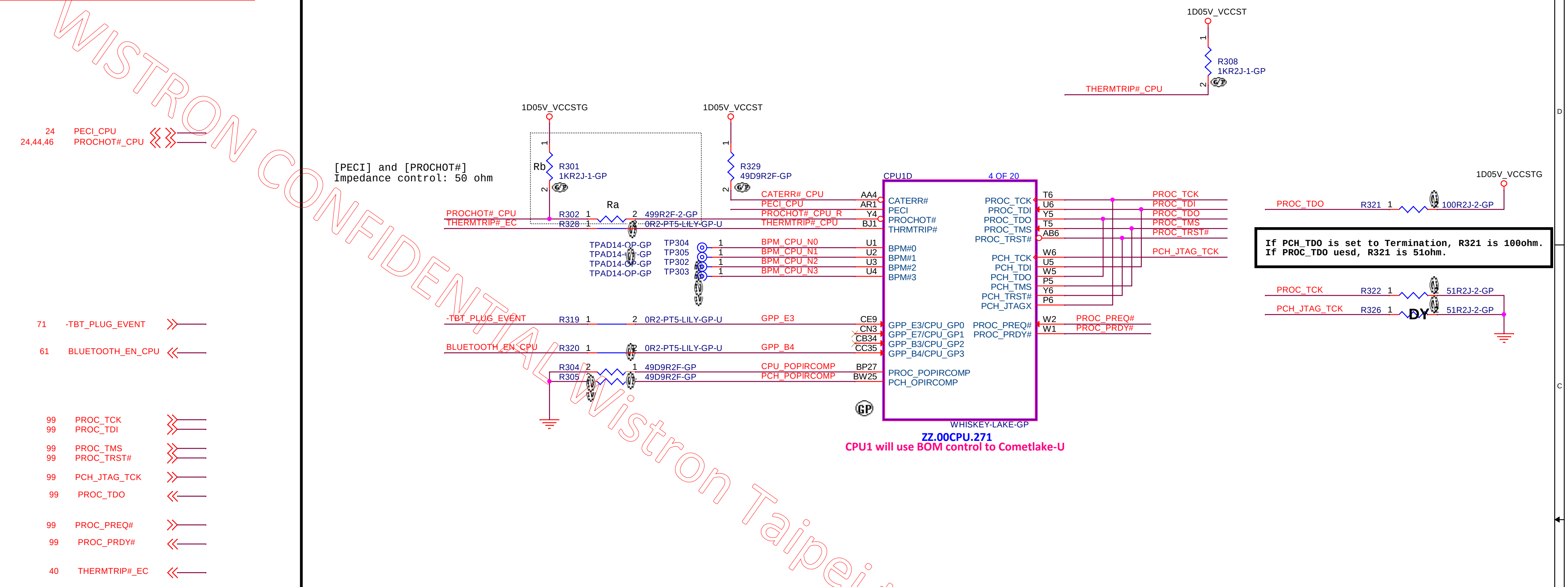
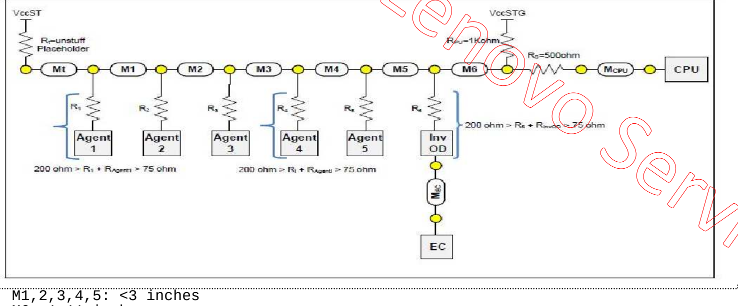
Main Func = CPU



(#543016) PROCHOT# Routing Guidelines

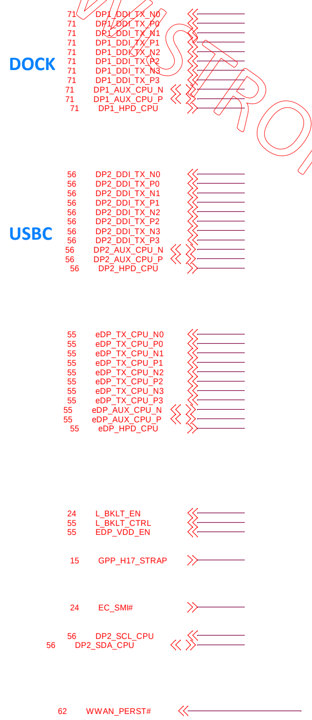
Figure 10-1. Routing Illustration for PROCHOT# Topology

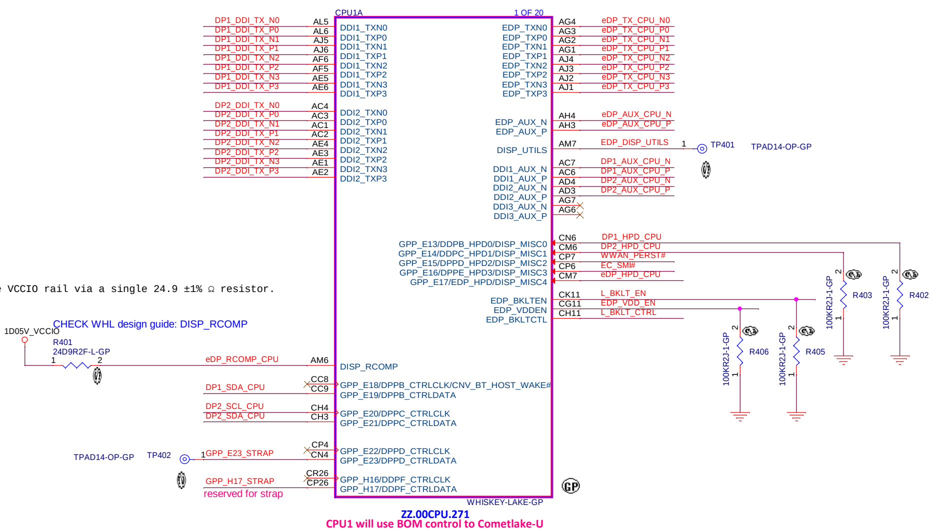


M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

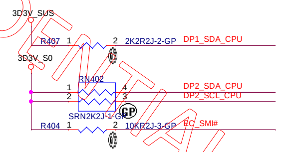
LBB-2

Main Func = CPU





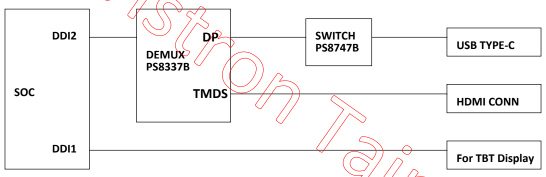
Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.



Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

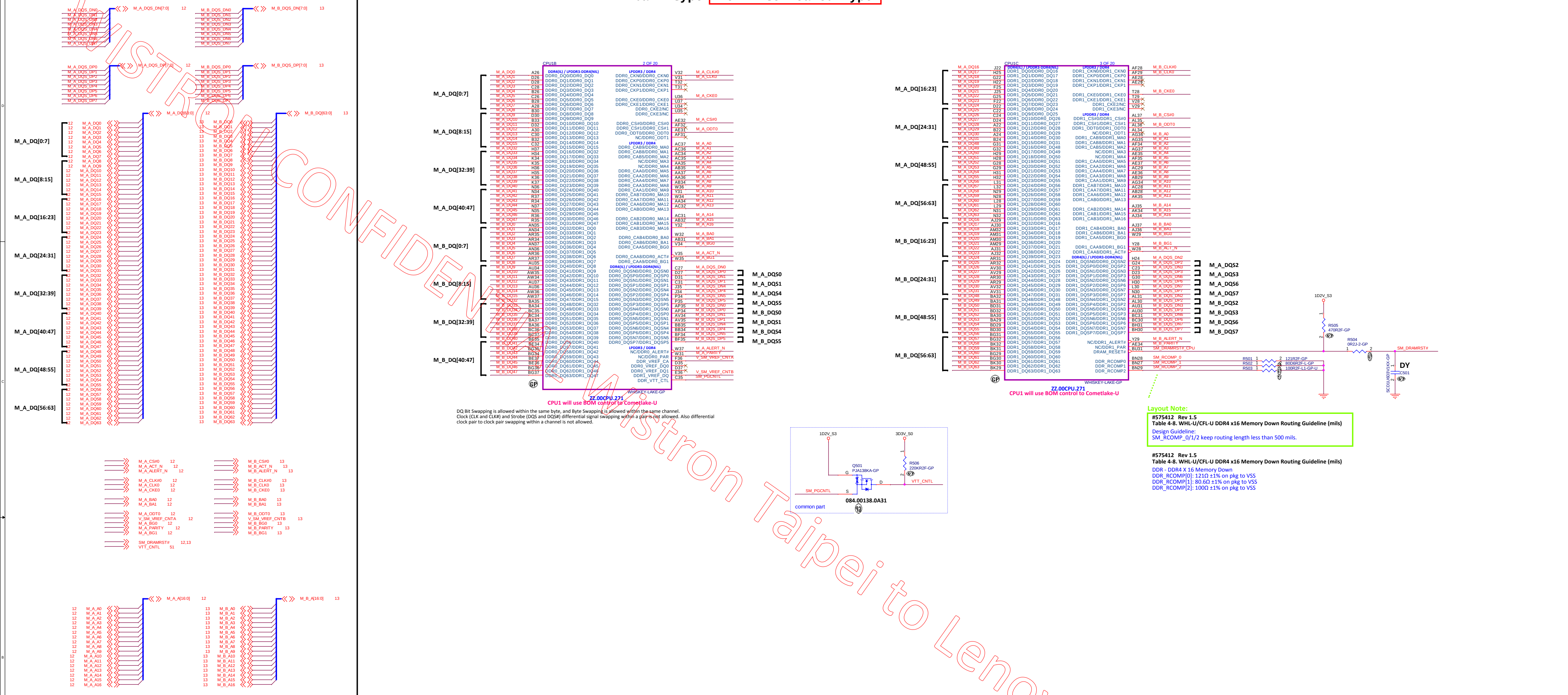
TABLE: Functional Strap

DDPB_CTRLDATA	
HIGH	Port B is detected.
LOW	Port B is not detected.
DDPC_CTRLDATA	
HIGH	Port C is detected.
LOW	Port C is not detected.



Main Func = CPU

DDR4 ball type: Non-Interleaved Type



CPU1 will use BOM control to Cometlake-U

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

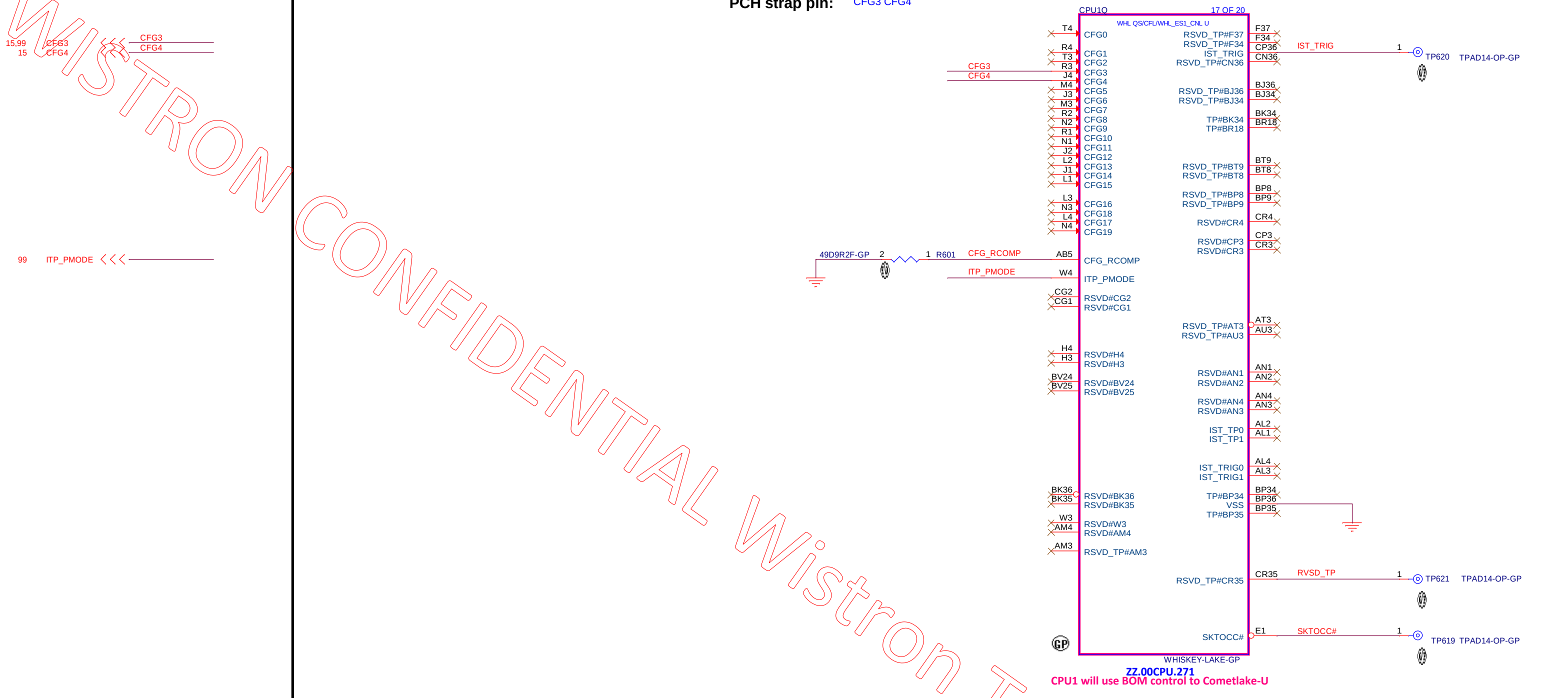
Layout Note:

#575412 Rev 1.5
Table 4-8. WHL-U/CFL-U DDR4 x16 Memory Down Routing Guideline (mils)
Design Guideline:
SM_RCOMP_0/1/2 keep routing length less than 500 mils.

#575412 Rev 1.5
Table 4-8. WHL-U/CFL-U DDR4 x16 Memory Down Routing Guideline (mils)
DDR - DDR4 X 16 Memory Down
DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS
DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS
DDR_RCOMP[2]: 100Ω ±1% on pkg to VSS

Main Func = CPU

PCH strap pin: CFG3 CFG4



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Title	CPU(CFG/IST)	
Size A2	Document Number Bumblebee-2	Rev 1
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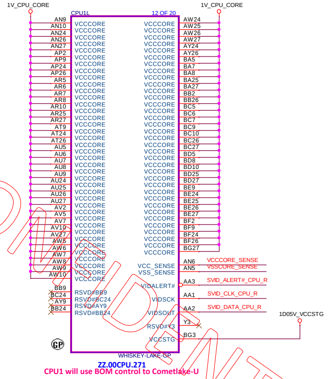
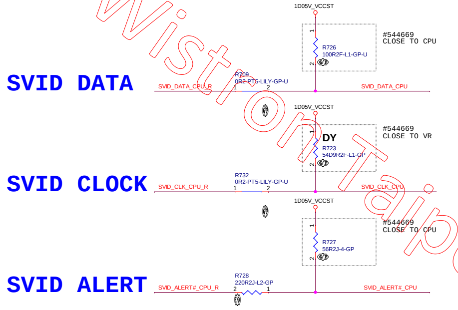
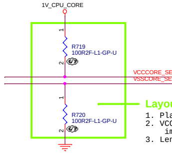
Main Func = CPU



Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.





Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Figure 10-7. Routing Illustration for SVID Topology

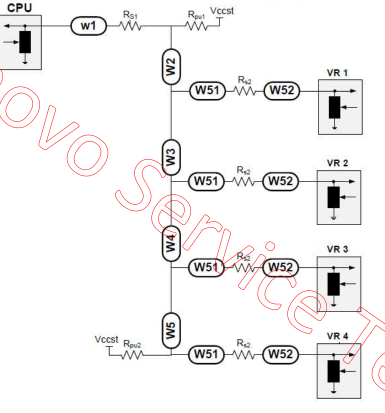


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

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Title	CPU(VCC_CORE)
Size A1	Document Number Bumblebee-2 — Rev 1
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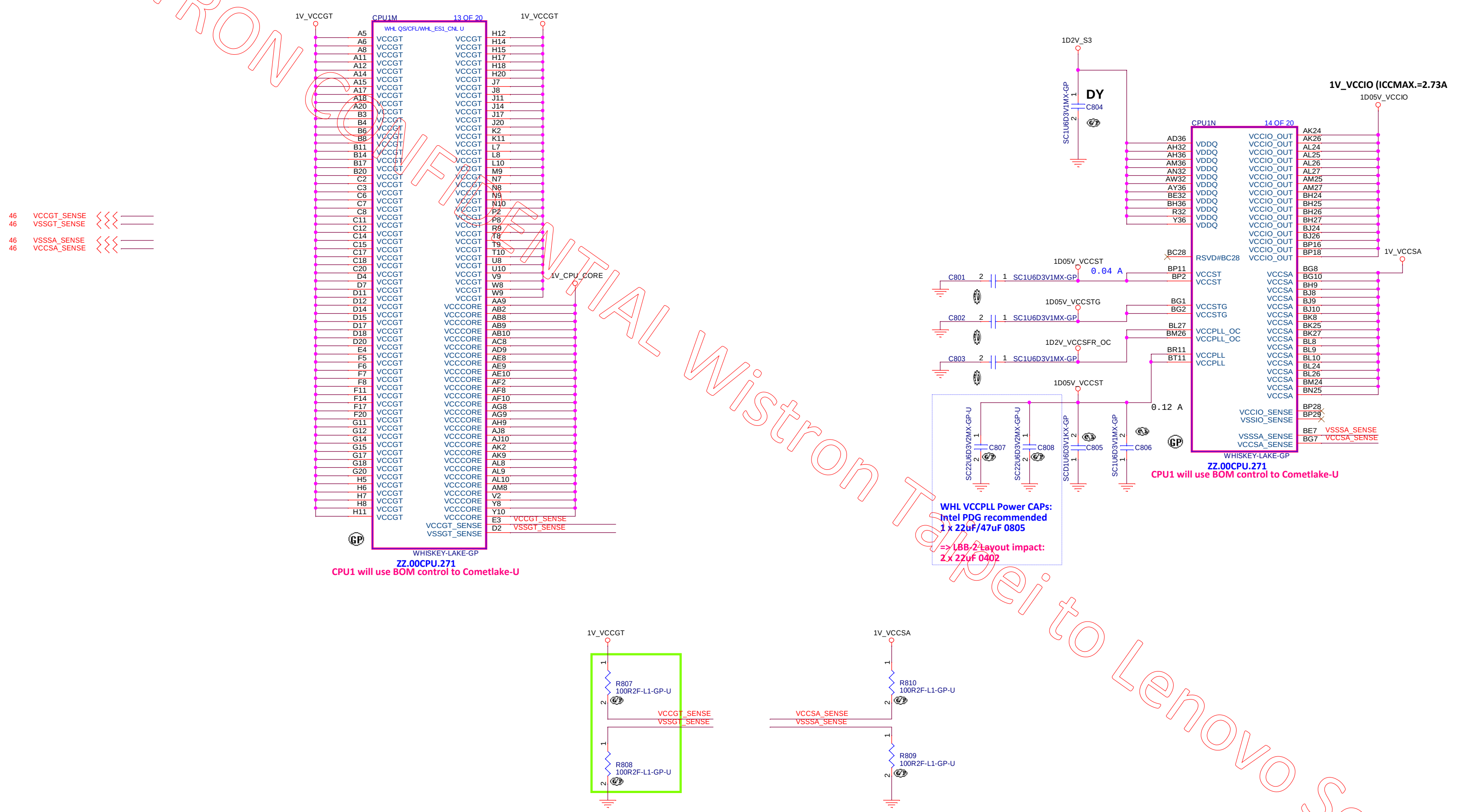
Main Func = CPU



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Title: CPU(VDDQ/VCC/VCCST/VCCSTG)

Size	Document Number	Rev
A2	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 8 of 106

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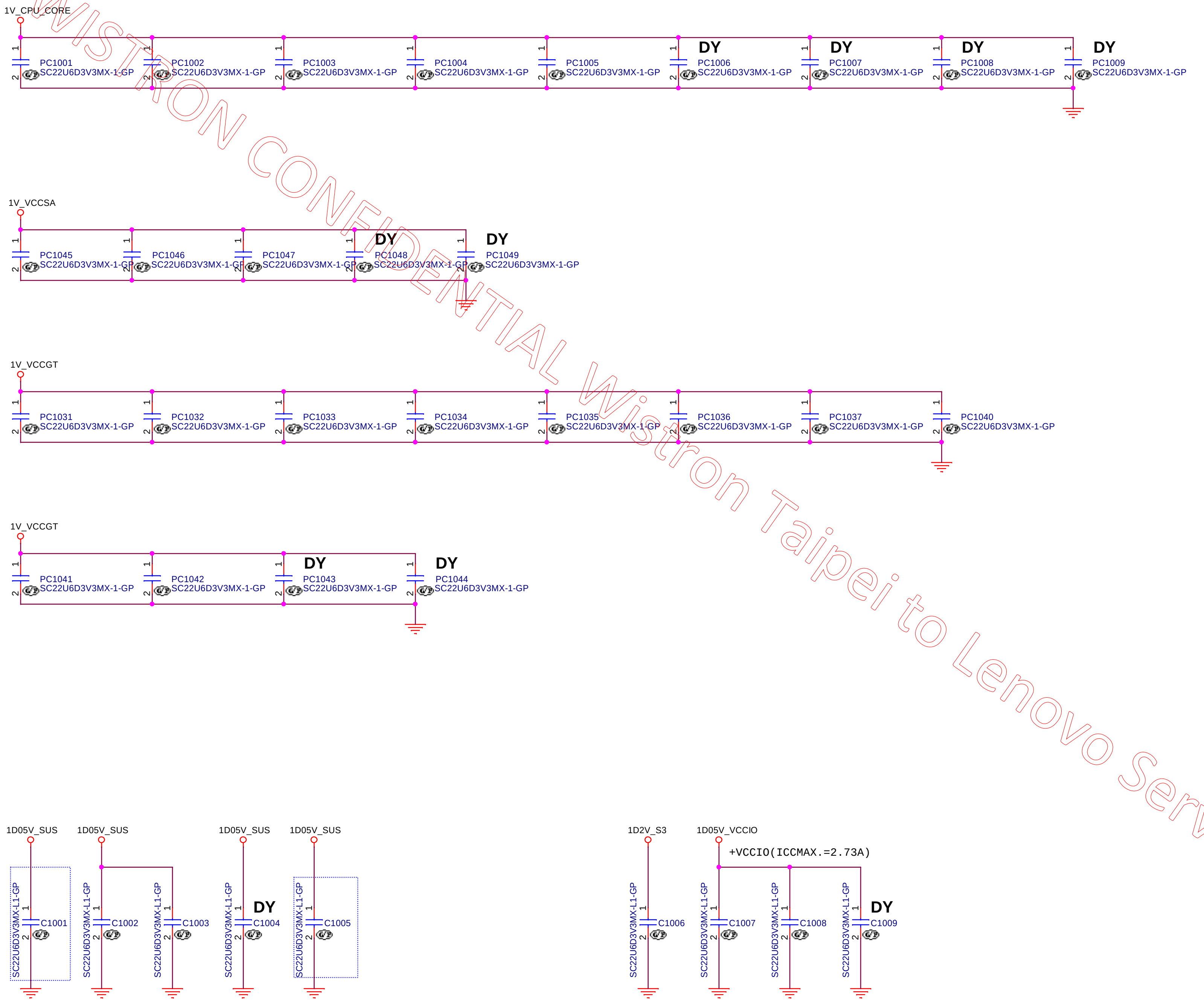
Main Func = CPU



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Title: CPU (POWER CAP1)		
Size: A3	Document Number: Bumblebee-2	Rev: 1
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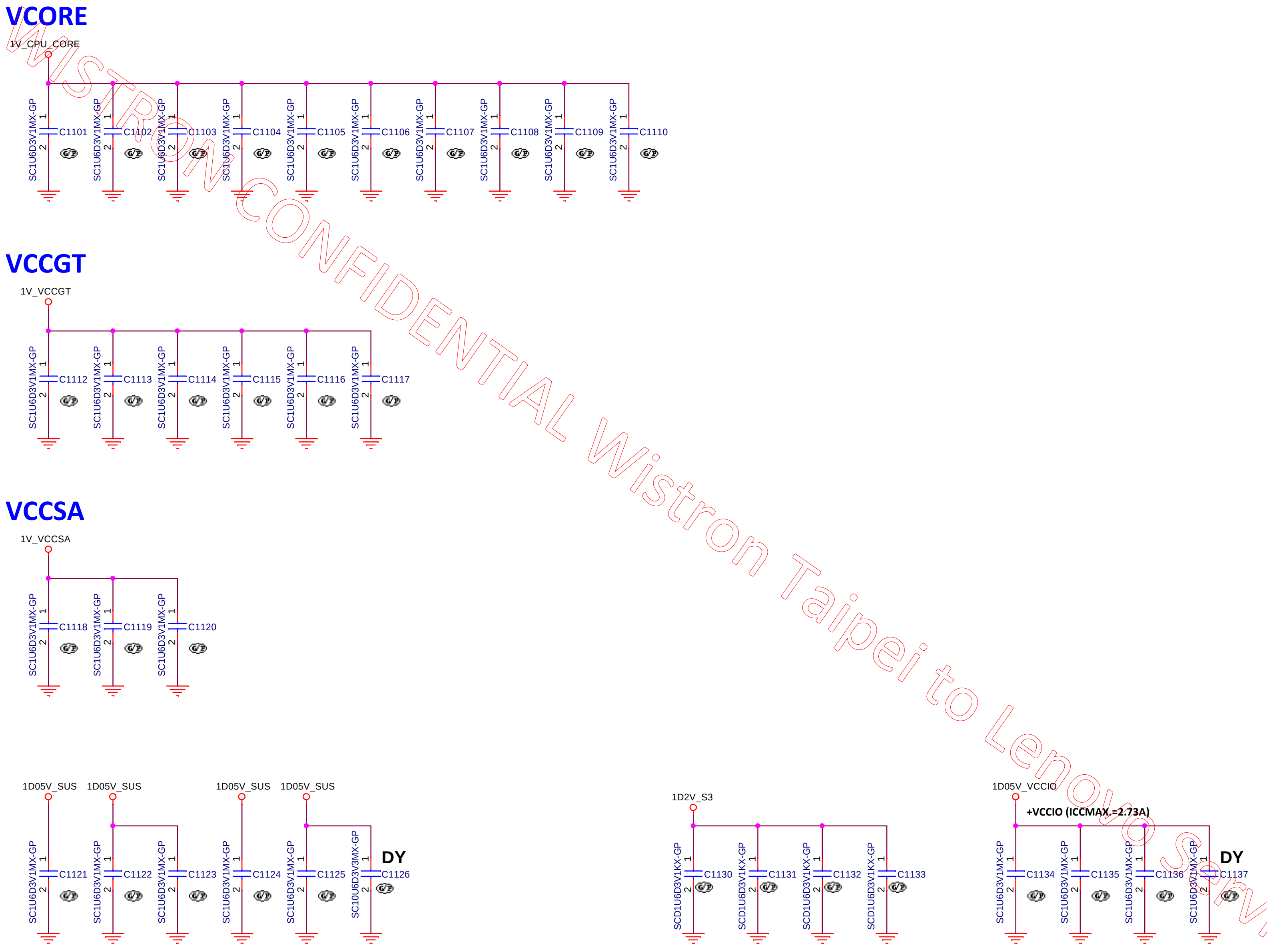

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Title: CPU (POWER CAP2)

Size: A3 | Document Number: Bumblebee-2 | Rev: 1

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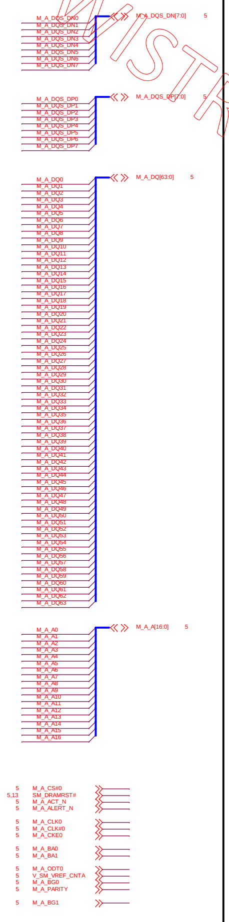
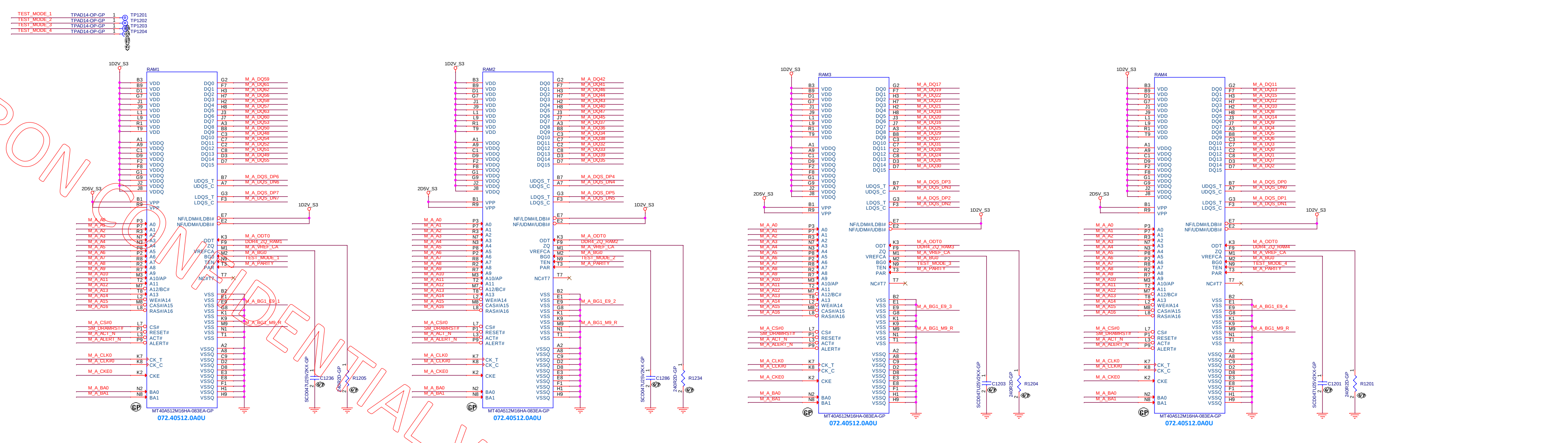
Main Func = DIMM1

BB2_EVT_MAIN_W024
BB2_FVT_MAIN_W011





SDP & DDP SETTING

R1212~R1215:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)

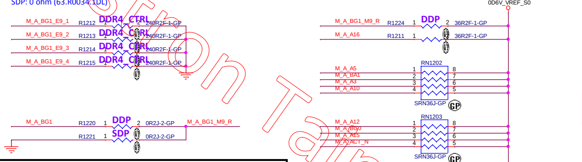
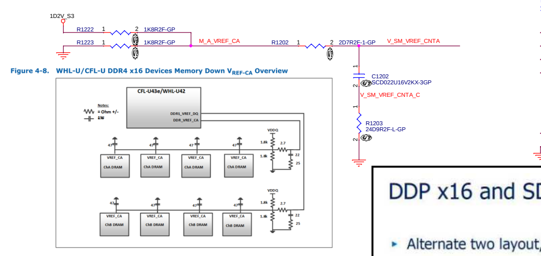
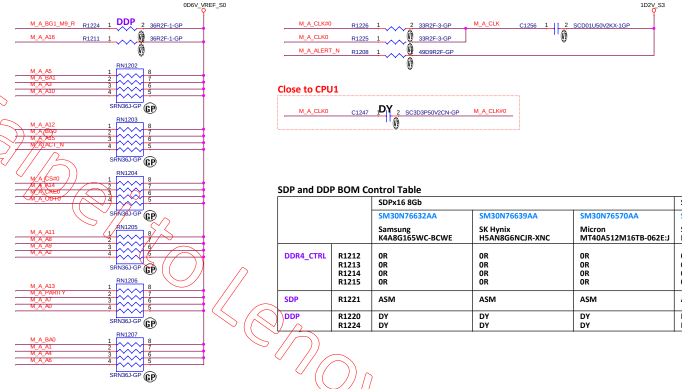
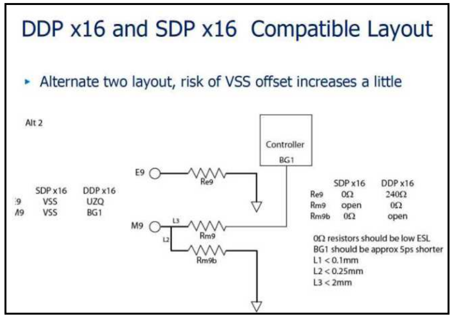


Figure 4-8. WHL-U/CFL-U DDR4 x16 Devices Memory Down V_{REF-CA} Overview



Close to CPU1





SDP and DDP BOM Control Table

		SDPx16 8Gb			SDPx16 16Gb	DDPx16 16Gb	SDPx16 16Gb
		SM30N76632AA Samsung K4A8G165WC-BCWE	SM30N76639AA SK Hynix H5AN8G6NCJR-XNC	SM30N76570AA Micron MT40A512M16TB-062E:J	SM30N76633AA Samsung K4AAG165WA-BCWE	SM30N76640AA SK Hynix H5ANAG6NCMR-XNC	SM30N76641AA Micron MT40A1G16KD-062E:E
DDR4_CTRL	R1212 R1213 R1214 R1215	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	240R 1% 240R 1% 240R 1% 240R 1%	0R 0R 0R 0R
SDP	R1221	ASM	ASM	ASM	ASM	DY	ASM
DDP	R1220 R1224	DY DY	DY DY	DY DY	DY DY	ASM ASM	DY DY

VDDQ/VDD 1uF x16

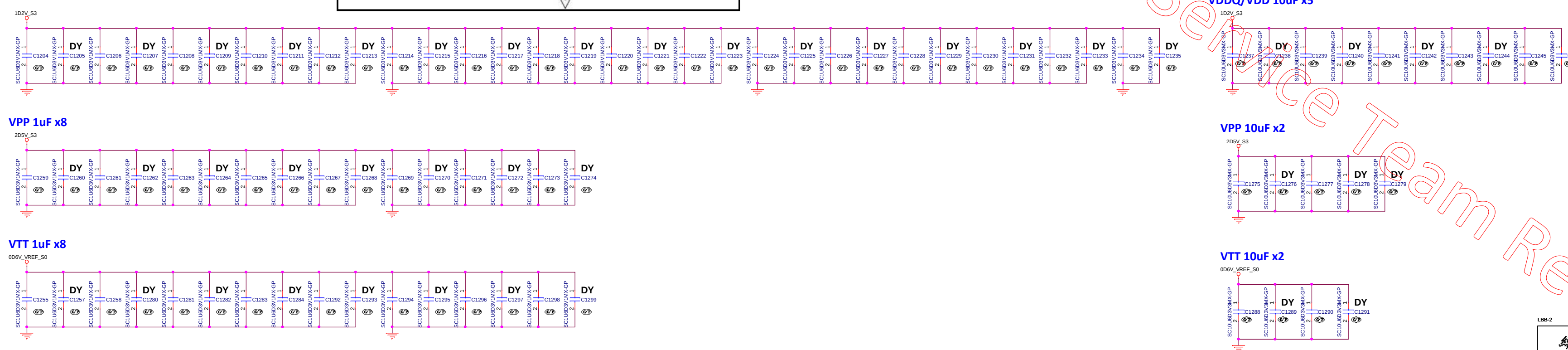
VDDQ/VDD 10uF x5

VPP 1uF x8

VPP 10uF x2

VTT 1uF x8

VTT 10uF x2



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Title	DDR (DDR4-CHA)
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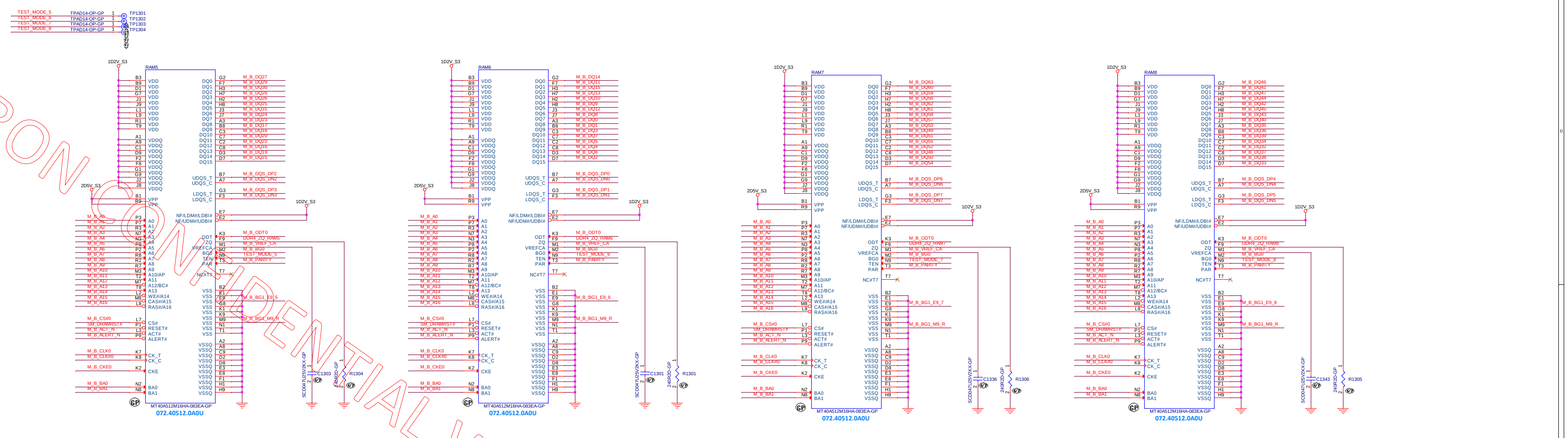
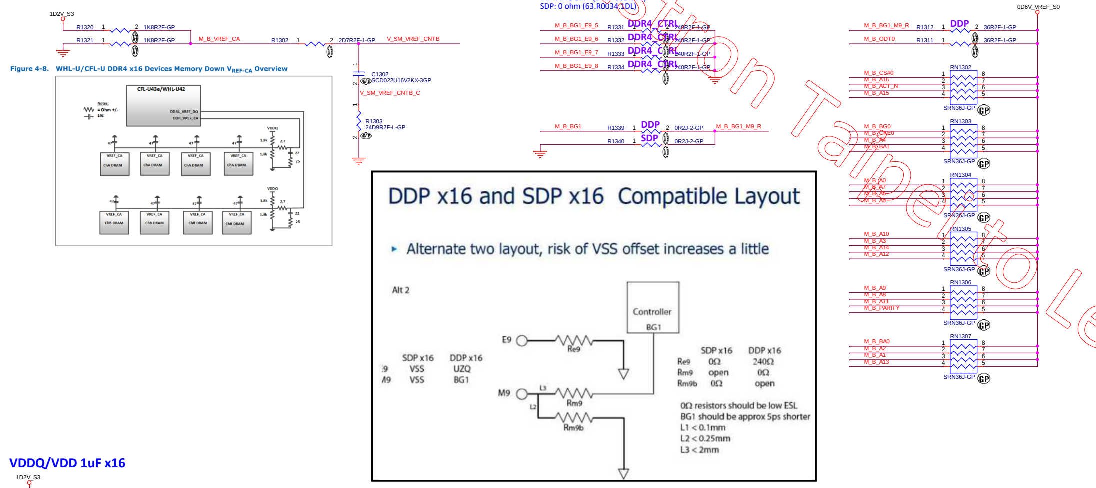
Main Func = DIMM2

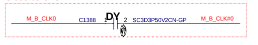
BB2_EVT_MAIN_W024
BB2_FVT_MAIN_W011



SDP & DDP SETTING

R1331~R1334:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)





SDP and DDP BOM Control Table

		SDPx16 8Gb			SDPx16 16Gb	DDPx16 16Gb	SDPx16 16Gb
		SM30N76632AA Samsung K4A8G165WC-BCWE	SM30N76639AA SK Hynix H5AN8G6NCJR-XNC	SM30N76570AA Micron MT40A512M16TB-062E:J	SM30N76633AA Samsung K4AAG165WA-BCWE	SM30N76640AA SK Hynix H5ANAG6NCMR-XNC	SM30N76641AA Micron MT40A1G16KD-062E:E
DDR4_CTRL	R1331 R1332 R1333 R1334	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	240R 1% 240R 1% 240R 1% 240R 1%	0R 0R 0R 0R
SDP	R1340	ASM	ASM	ASM	ASM	DY	ASM
DDP	R1339 R1312	DY DY	DY DY	DY DY	DY DY	ASM ASM	DY DY

VDDQ/VDD 1uF x16

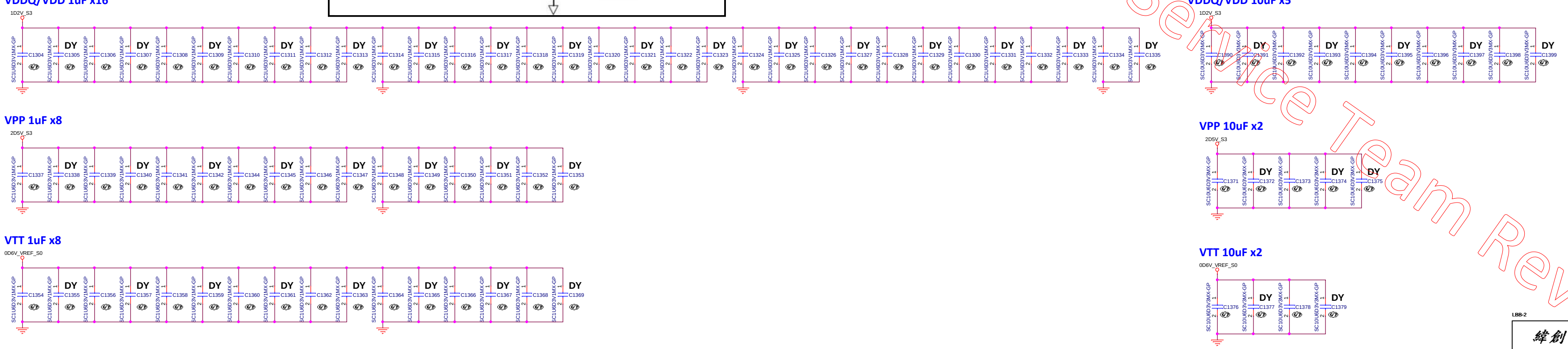
VDDQ/VDD 10uF x5

VPP 1uF x8

VPP 10uF x2

VTT 1uF x8

VTT 10uF x2



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Title	DDR (DDR4-CHB)	
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Title	*DDR (RSVD)*
Size A4	Document Number **Bumblebee-2** Rev **1**
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Main Func = PCH

HW Strap

GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

GPP_B14

GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_B18

GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_C2

GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). Bit 6 — Boot BIOS Destination 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

GPP_B22

GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the e*SPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**

GPP_C5

LBB-2 uses LPC interface

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_MOSI

GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_D12

RVP 20K PH; #566439 EDS 100K

GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.

GPP_B23

SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2

SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3

HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_R2 / HDA_SDO / I2S0_TXD / HDACPU_SDO

GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

on page 71

GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

on page 4

GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on the PCH. This strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_H21

GPP_F6 / CNV_RGI_DT	M.2 CNVi Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

GPP_F6 / CNV_RGI_DT / UART0_TXD

INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.

GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

PDG datasheet. #575418

PCH strap pin:

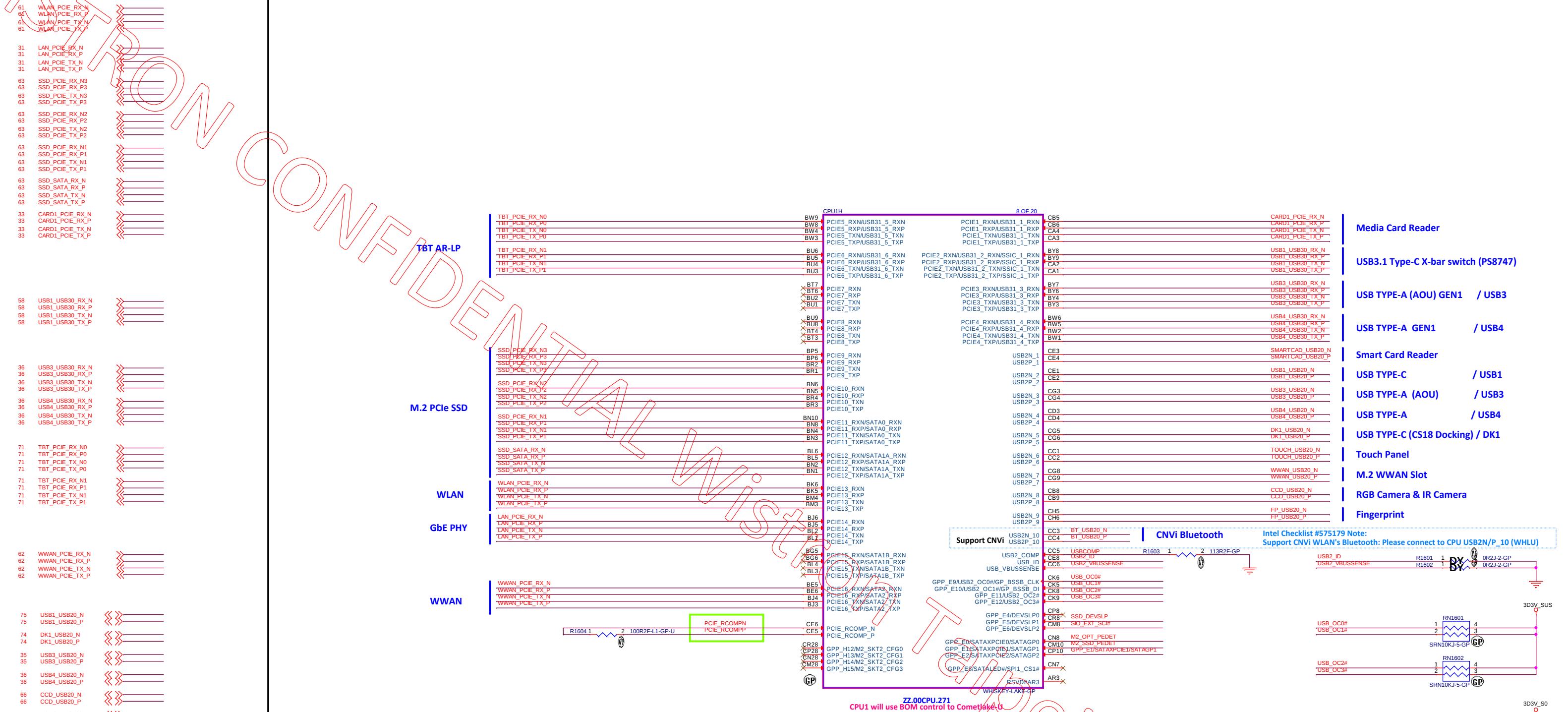
DISPLAY PORT PRESENCE STRAP

Wistron Corporation

CPU(STRAP)

Bumblebee-2

Main Func = PCH



Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

SATA Configuration

Pair	Device
0	NC
1A	M.2 SATA SSD
1B	NC
2	NC

PCIe Configuration

Pair	Device
1	Media Card Reader
2	NC
3	NC
4	NC
5	TBT (AR-LP)
6	TBT (AR-LP)
7	NC
8	NC
9	M.2 PCIe SSD
10	M.2 PCIe SSD
11	M.2 PCIe SSD
12	M.2 PCIe SSD
13	WLAN
14	GbE
15	NC
16	WWAN

USB3.0 Configuration

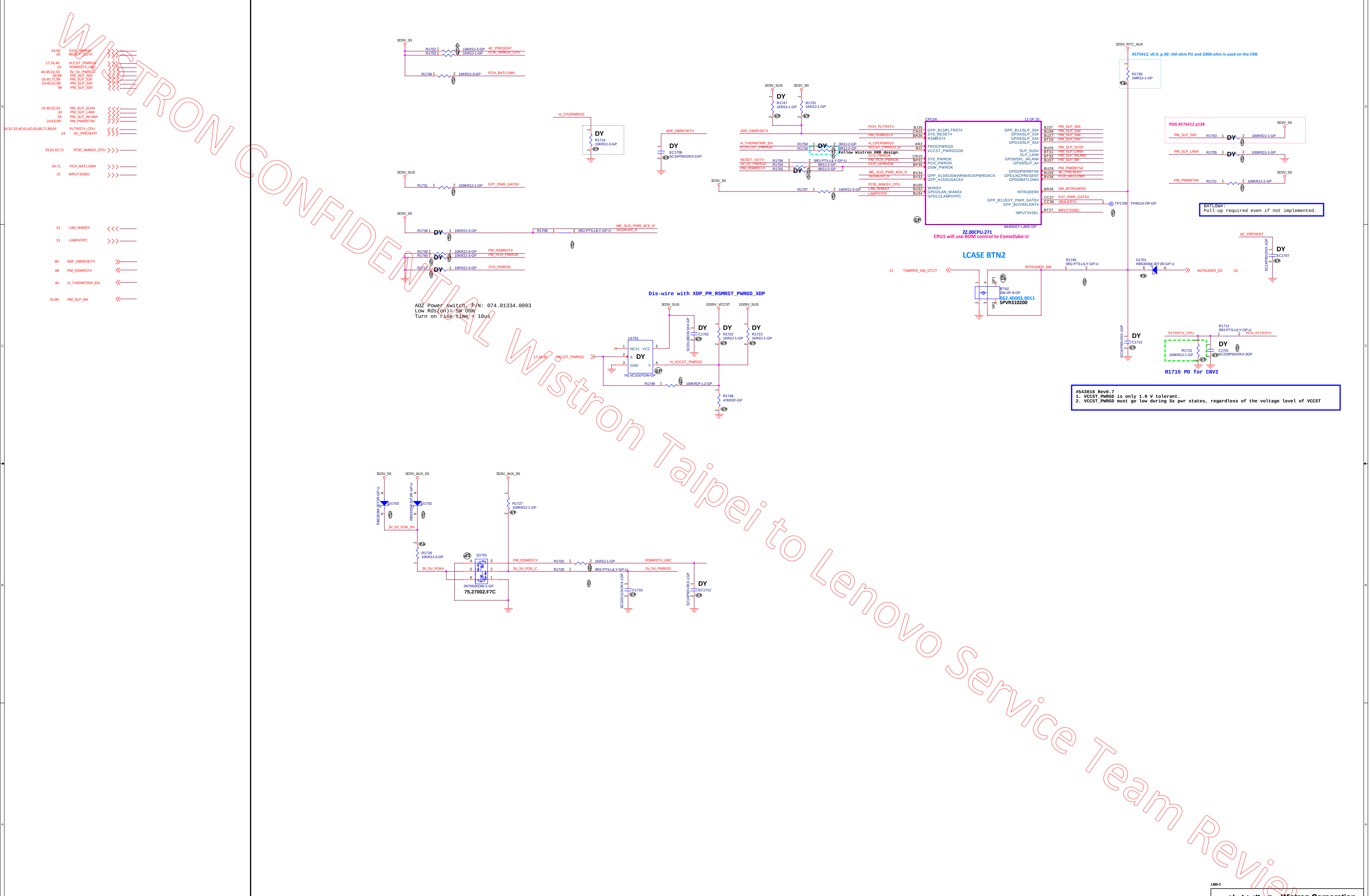
Pair	Device
1	NC
2	USB3 Type-C Port1
3	USB3 Type-A Port3 (AOU)
4	USB3 Type-A Port4
5	NC
6	NC

USB2.0 Configuration

Pair	Device
1	Smart Card Reader
2	USB3 Type-C Port1
3	USB3 Type-A Port3 (AOU)
4	USB3 Type-A Port4
5	USB3 Type-C (CS18 Docking) Port2 / DK1
6	Touch Screen
7	WWAN Card
8	RGB/IR Hybrid Camera
9	Fingerprint
10	Bluetooth (CNVi)

Main Func = PCH

BB2_SVT_MAIN_W003

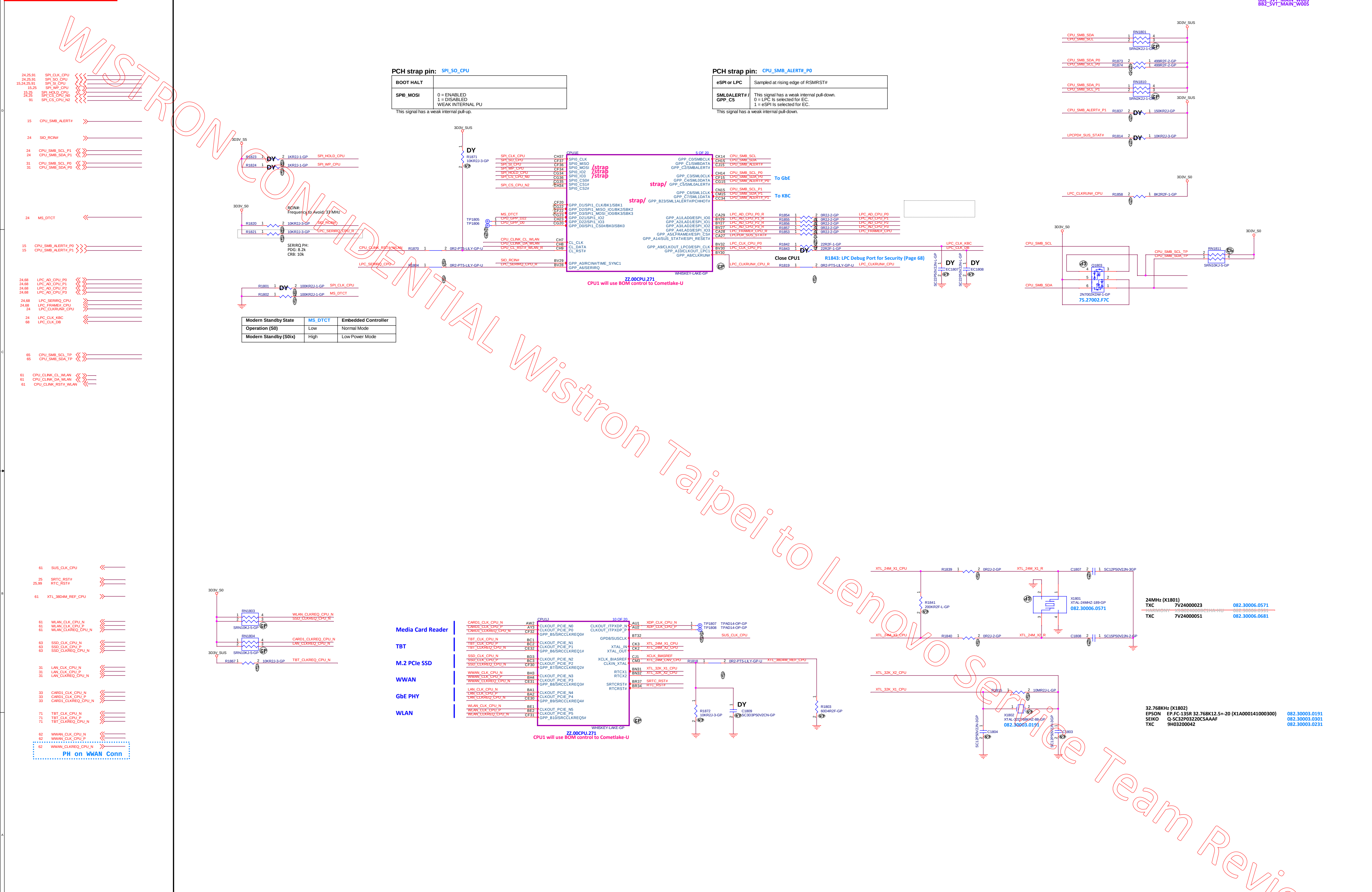


LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (PMU)
Size	A1
Document Number	Bumblebee-2
Rev	1
Date	Tuesday, March 03, 2020
Sheet	17 of 106

Main Func = PCH



PCH strap pin: SPI_SO_CPU

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PCH strap pin: CPU_SMB_ALERT#_P0

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

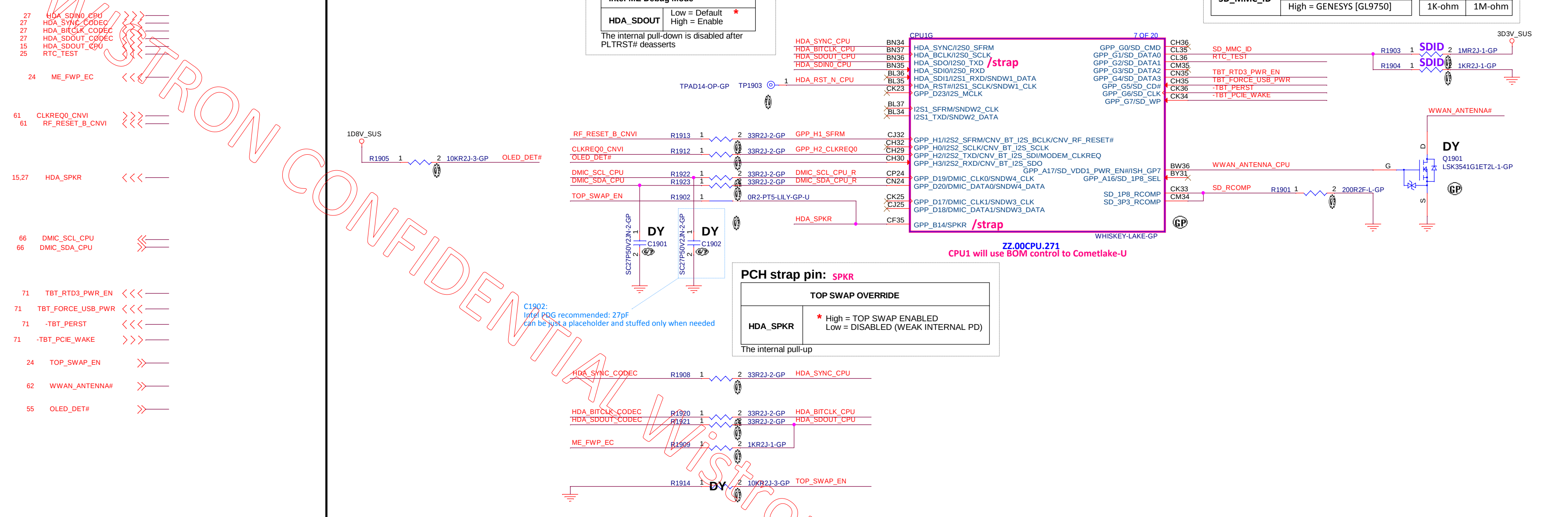
Modern Standby State	MS_DTCT	Embedded Controller
Operation (S0)	Low	Normal Mode
Modern Standby (S0ix)	High	Low Power Mode

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_(SPI/ESPI/SMBUS/XTAL/CLK)	
Size A1	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 18 of 106	

Main Func = PCH



PCH strap pin: HDA_SDOUT_CPU

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

SW Control : GPP_G1 — **HW Control :** *

		R1903	R1904
SD_MMC_ID	Low = REALTEK [RTS5232S]	1M-ohm	1K-ohm
	High = GENESYS [GL9750]	1K-ohm	1M-ohm

<-- Default

PCH strap pin: SPKR

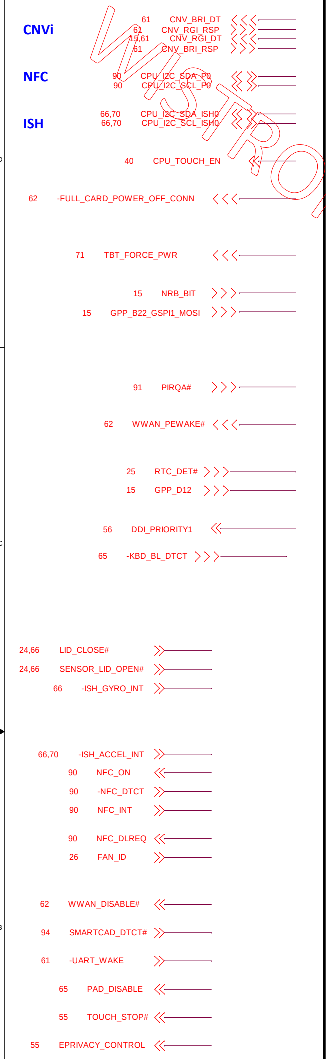
TOP SWAP OVERRIDE	
HDA_SPKR	* High = TOP SWAP ENABLED Low = DISABLED (WEAK INTERNAL PD)

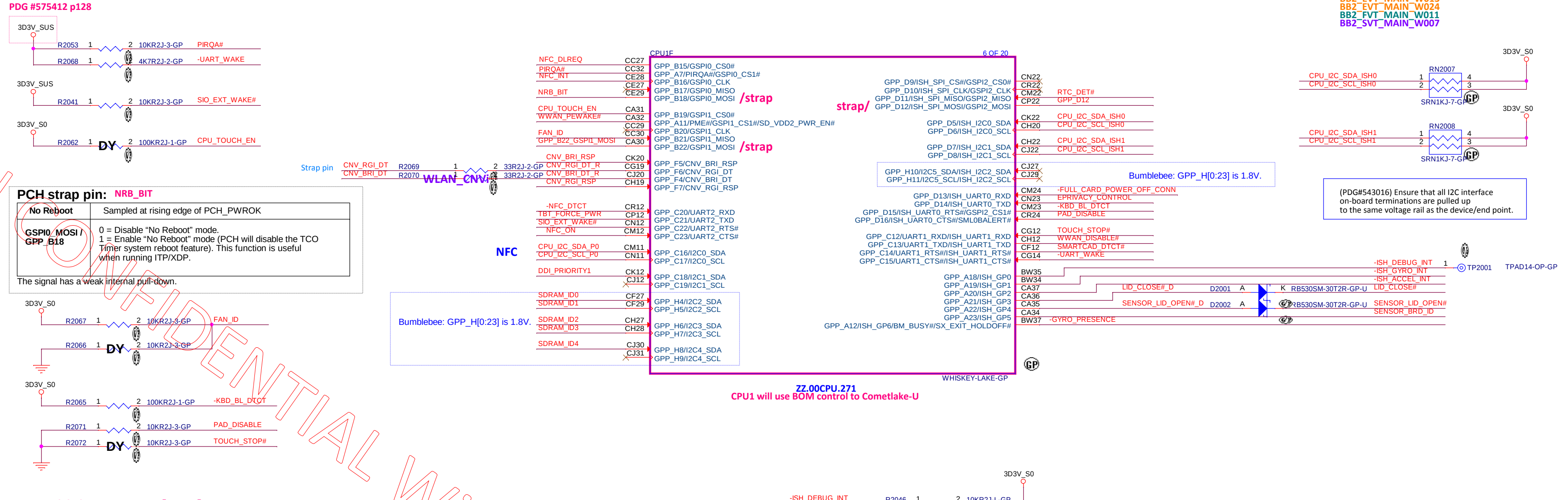
The internal pull-up

BB2_EVT_MAIN_W002
BB2_EVT_MAIN_W017
BB2_EVT_MAIN_W018
BB2_SVT_MAIN_W003
BB2_FVT_MAIN_L001

LBB-2

Main Func = PCH





PCH strap pin: NRB_BIT

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

Bumblebee: GPP_H[0:23] is 1.8V.

Memory Configuration	Memory Supplier	Die Revision
00: 8Gb 01: 4Gb (Reserve) 10: 16Gb 11: 32Gb (Reserve)	00: Samsung 01: Micron 10: SK Hynix 11: (Reserve)	

GPP_H8	GPP_H7	GPP_H6	GPP_H5	GPP_H4				
SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Memory ID	Supplier	Density	Vendor PN
0	0	0	0	0	0	SAMSUNG	8GB (8Gb*8)	K4A8G165WC-BCWE
0	1	0	0	0	8			
1	0	0	0	0	16	SAMSUNG	16GB (16Gb*8)	K4AAG165WA-BCWE
1	1	0	0	0	24			
0	0	0	1	0	2	MICRON	8GB (8Gb*8)	MT40A512M16TB-062E:J
0	1	0	1	0	10			
1	0	0	1	0	18	MICRON	16GB (16Gb*8)	MT40A1G16KD-062E:E
1	1	0	1	0	26			
0	0	1	0	0	4	SK HYNIX	8GB (8Gb*8)	H5AN8G6NCJR-XNC
0	1	1	0	0	12			
1	0	1	0	0	20	SK HYNIX	16GB (16Gb*8)	H5ANAG6NCMR-XNC
1	1	1	0	0	28			

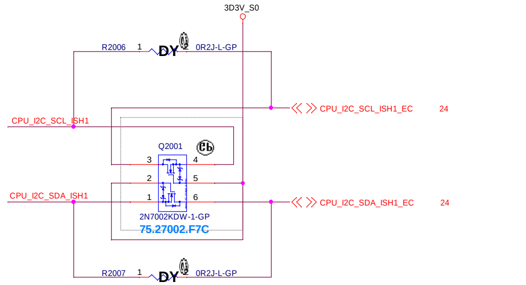
0=L, 1=H

SDRAM_ID4 R2073 R2074	SDRAM_ID3 R2011 R2012	SDRAM_ID2 R2022 R2029	SDRAM_ID1 R2017 R2018	SDRAM_ID0 R2015 R2016	Memory ID	Supplier	Density	Vendor PN
DY 10K	DY 10K	DY 10K	DY 10K	DY 10K	0	SAMSUNG	8GB (8Gb*8)	K4A8G165WC-BCWE
10K DY	DY 10K	DY 10K	DY 10K	DY 10K	16	SAMSUNG	16GB (16Gb*8)	K4AAG165WA-BCWE
DY 10K	DY 10K	DY 10K	10K DY	DY 10K	2	MICRON	8GB (8Gb*8)	MT40A512M16TB-062E:J
10K DY	DY 10K	DY 10K	10K DY	DY 10K	18	MICRON	16GB (16Gb*8)	MT40A1G16KD-062E:E
DY 10K	DY 10K	10K DY	DY 10K	DY 10K	4	SK HYNIX	8GB (8Gb*8)	H5AN8G6NCJR-XNC
10K DY	DY 10K	10K DY	DY 10K	DY 10K	20	SK HYNIX	16GB (16Gb*8)	H5ANAG6NCMR-XNC

Sensors Debug Hooks_543016:

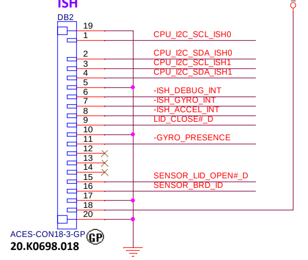
Table 31-3. 18-pin ZIF Connector Pinout

Pin	Pin function	Description
1	ISH_I2C0_SCL	Clock line for the I2C0
2	ISH_I2C0_SDA	Data line for the I2C0
3	ISH_I2C1_SCL	Clock line for the I2C1
4	ISH_I2C1_SDA	Data line for the I2C1
5	GND	System Ground
6	GPIOa (1)	Connect here one of the GPIOs in use
7	GPIOb (1)	Connect here one of the GPIOs in use
8	GPIOc (1)	Connect here one of the GPIOs in use
9	GPIOd (1)	Connect here one of the GPIOs in use
10	GND	System Ground
11	Reserved by Intel	Do not use
12	Reserved by Intel	Do not use
13	Reserved by Intel	Do not use
14	Reserved by Intel	Do not use
15	Reserved by Intel	Do not use
16	Reserved by Intel	Do not use
17	GND	System Ground
18	Vio	Sensors Reference Voltage

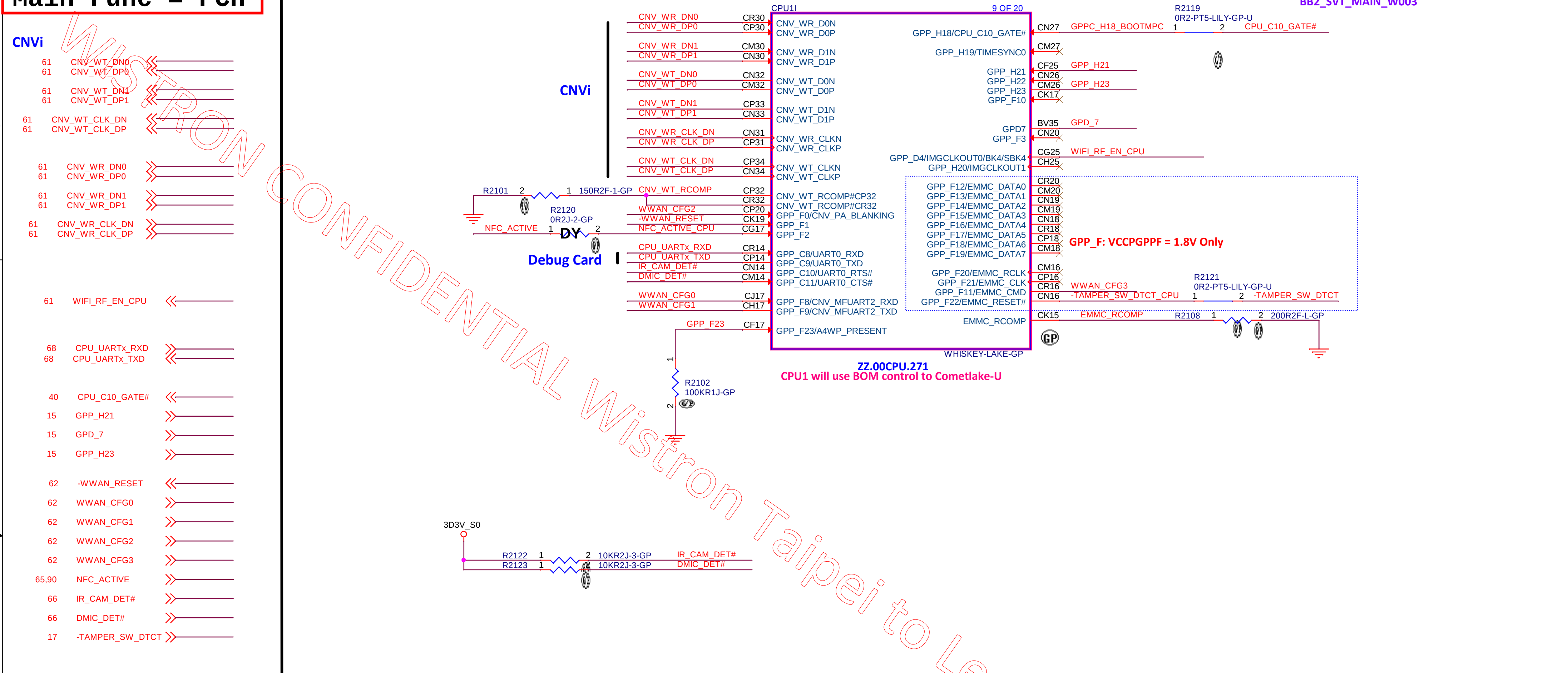


Sensors Debug Hooks

ISH



Main Func = PCH



LBB-2

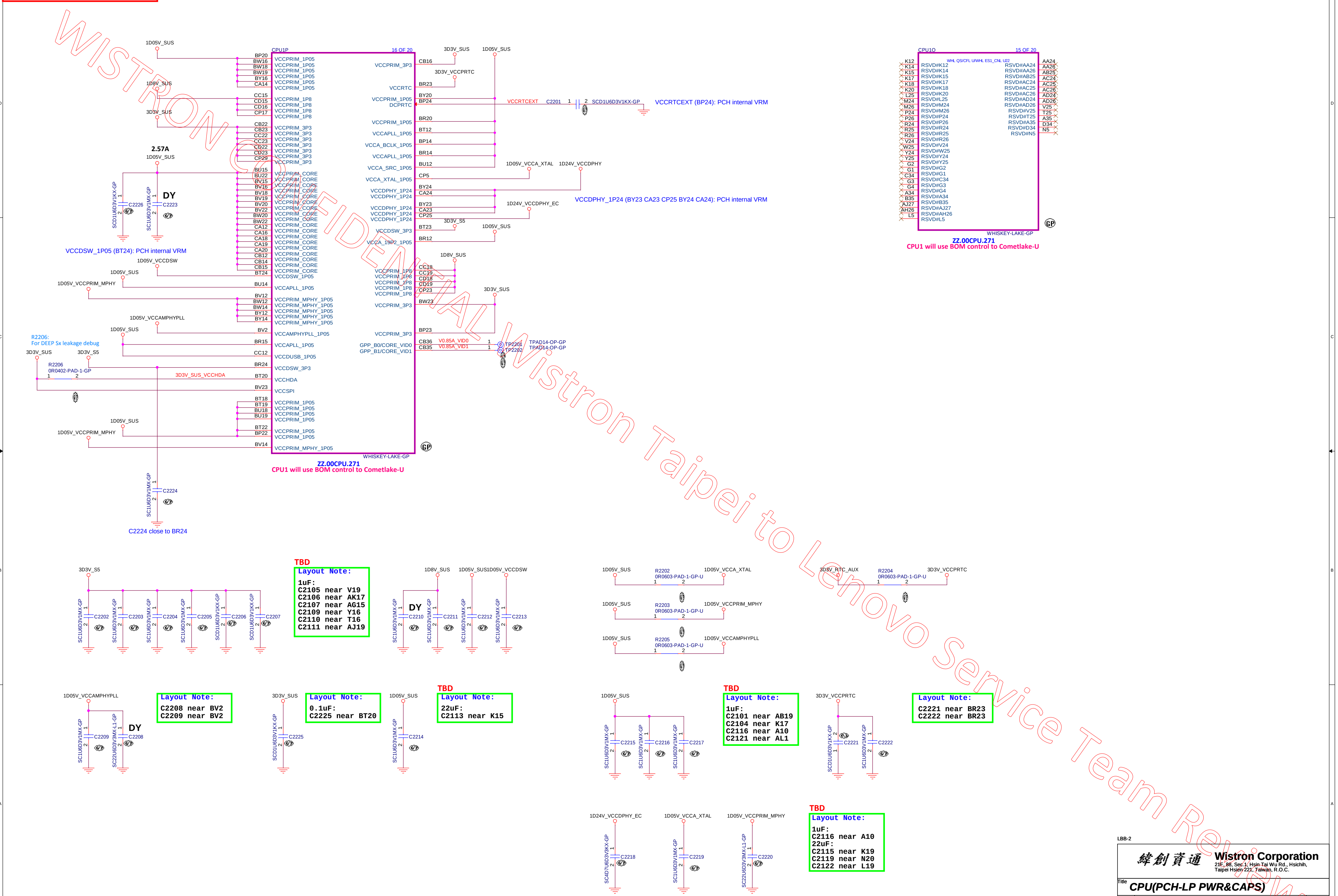
緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_(CSI/EMMC/CNVI)	
Size A3	Document Number: Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 21 of 106	

Main Func = PCH

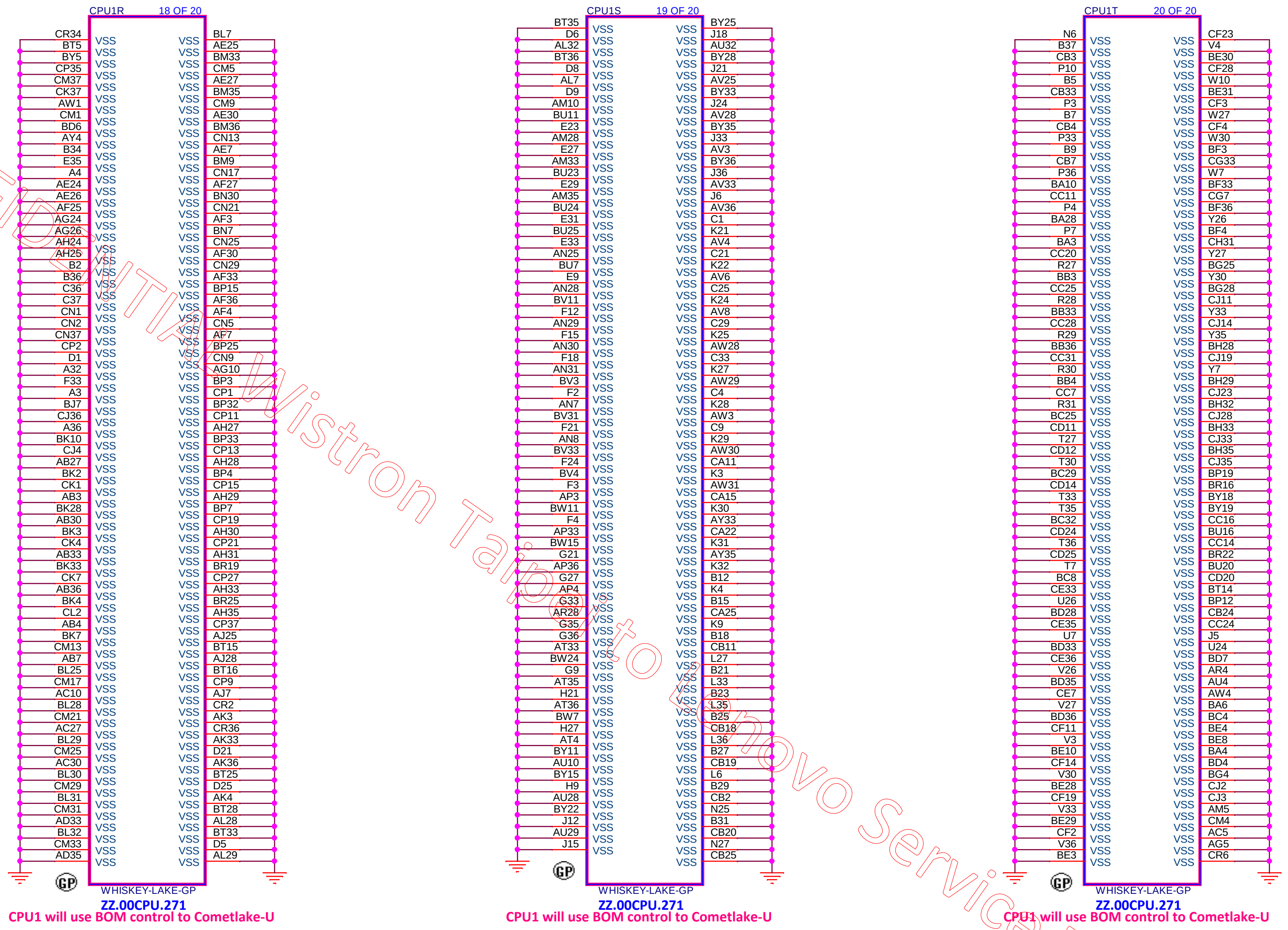
BB2_SVT_MAIN_W003



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU(PCH-LP PWR&CAPS)	
Size A2	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 22 of 106	

Main Func = PCH

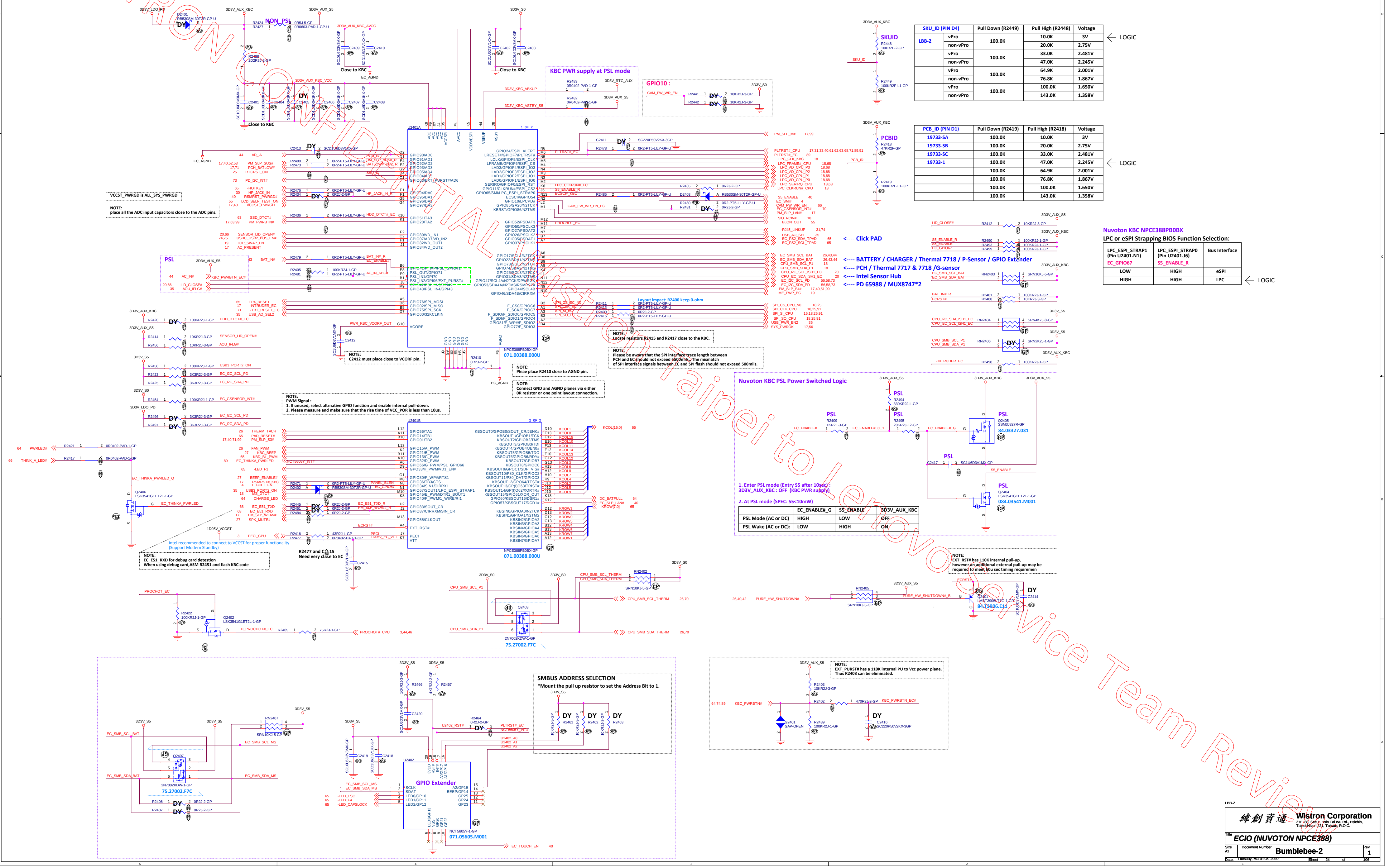


LBB-2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU_(VSS)***
Size A3	Document Number **Bumblebee-2** — Rev **1**
Date: Tuesday, March 03, 2020	Sheet 23 of 106

Main Func = KBC

BB2_EVT_MAIN_W003
BB2_EVT_MAIN_W004
BB2_EVT_MAIN_W015
BB2_EVT_MAIN_W021
BB2_EVT_MAIN_W022
BB2_FVT_MAIN_W001
BB2_FVT_MAIN_W005
BB2_FVT_MAIN_W007
BB2_FVT_MAIN_W017
BB2_SIT_MAIN_W002
BB2_SIT_MAIN_W004
BB2_SVT_MAIN_W001
BB2_SVT_MAIN_W003



SKU_ID (PIN D4)		Pull Down (R2449)	Pull High (R2448)	Voltage
LBB-2	vPro	100.0K	10.0K	3V
	non-vPro		20.0K	2.75V
	vPro	100.0K	33.0K	2.481V
	non-vPro		47.0K	2.245V
	vPro	100.0K	64.9K	2.001V
	non-vPro		76.8K	1.867V
	vPro	100.0K	100.0K	1.650V
	non-vPro		143.0K	1.358V

PCB_ID (PIN D1)	Pull Down (R2419)	Pull High (R2418)	Voltage
19733-SA	100.0K	10.0K	3V
19733-SB	100.0K	20.0K	2.75V
19733-SC	100.0K	33.0K	2.481V
19733-1	100.0K	47.0K	2.245V
	100.0K	64.9K	2.001V
	100.0K	76.8K	1.867V
	100.0K	100.0K	1.650V
	100.0K	143.0K	1.358V

Nuvoton KBC NPCE388PB0BX

LPC or eSPI Strapping BIOS Function Selection:

LPC_ESPI_STRAP1 (Pin U2401.N1) EC_GPIO67	LPC_ESPI_STRAP0 (Pin U2401.J6) S5_ENABLE_R	Bus Interface
LOW	HIGH	eSPI
HIGH	HIGH	LPC

<---- Click PAD
<---- BATTERY / CHARGER / Thermal 7718 / P-Sensor / GPIO Extender
<---- PCH / Thermal 7717 & 7718 /G-sensor
<---- Intel Sensor Hub
<---- PD 65988 / MUX8747*2

KBC PWR supply at PSL mode

GPIO10 :

VCCST_PWRGD is ALL_SYS_PWRGD

NOTE:
place all the ADC input capacitors close to the ADC pins.

NOTE:
C2412 must place close to VCORF pin.

NOTE:
Please place R2410 close to AGND pin.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

NOTE:
PWM Signal :
1. If unused, select altrnative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_POR is less than 10us.

Layout impact: R2400 keep 0-ohm

NOTE:
Locate resistors R2415 and R2417 close to the KBC.

NOTE:
Please be aware that the SPI interface trace length between PCH and EC should not exceed 6500mils . The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

Nuvoton KBC PSL Power Switched Logic

1. Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)

2. At PSL mode (SPEC: S5<10mW)

	EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
PSL Mode (AC or DC)	HIGH	LOW	OFF
PSL Wake (AC or DC)	LOW	HIGH	ON

Intel recommended to connect to VCCST for proper functionality (Support Modern Standby)

NOTE:
EC_E51_RXD for debug card detection
When using debug card,ASM R2451 and flash KBC code

R2477 and C2415 Need very close to EC

NOTE:
EXT_RST# has 110K internal pull-up, however an additional external pull-up may be required to meet 60u sec timing requiremen

SMBUS ADDRESS SELECTION
*Mount the pull up resistor to set the Address Bit to 1.

GPIO Extender

NOTE:
EXT_PURST# has a 110K internal PU to Vcc power plane. Thus R2403 can be eliminated.

LBB-2

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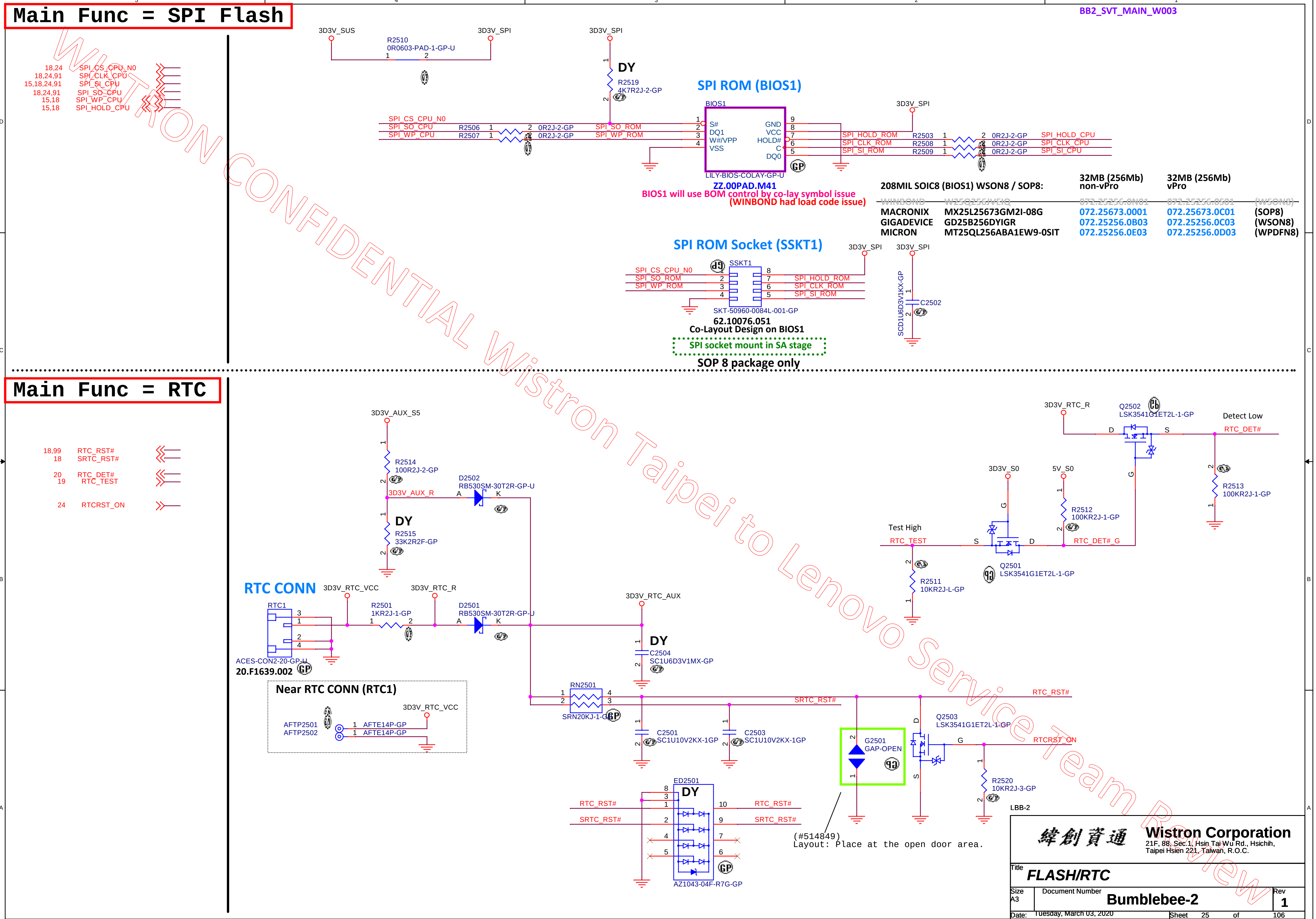
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ECIO (NUVOTON NPCE388)
Size: A1 | Document Number: Bumblebee-2 | Rev: 1
Date: Tuesday, March 03, 2020 | Sheet 24 of 106



208MIL SOIC8 (BIOS1) WSON8 / SOP8:		32MB (256Mb) non-vPro	32MB (256Mb) vPro	
~~WINBOND~~	~~W25Q256JVEIQ~~	~~072.25256.0N01~~	~~072.25256.0S01~~	~~(WSON8)~~
MACRONIX	MX25L25673GM2I-08G	072.25673.0001	072.25673.0C01	(SOP8)
GIGADEVICE	GD25B256DYIGR	072.25256.0B03	072.25256.0C03	(WSON8)
MICRON	MT25QL256ABA1EW9-0SIT	072.25256.0E03	072.25256.0D03	(WPDFN8)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

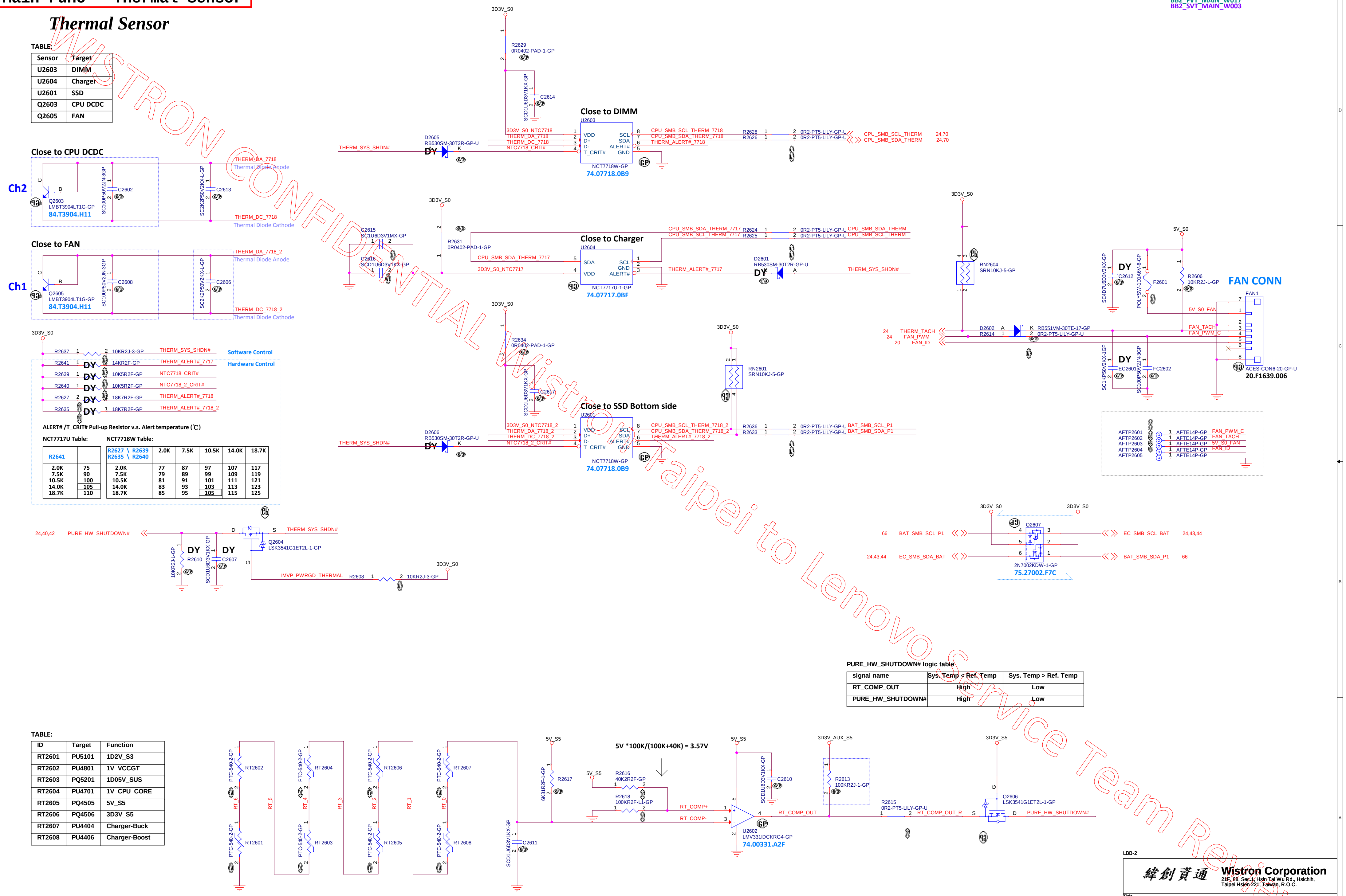
Title: FLASH/RTC
Size: A3 | Document Number: Bumblebee-2 | Rev: 1
Date: Tuesday, March 03, 2020 | Sheet 25 of 106

Main Func = Thermal Sensor

Thermal Sensor

TABLE:

Sensor	Target
U2603	DIMM
U2604	Charger
U2601	SSD
Q2603	CPU DCDC
Q2605	FAN



ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)

NCT7717U Table:

R2641	
2.0K	75
7.5K	90
10.5K	100
14.0K	105
18.7K	110

NCT7718W Table:

R2627 \ R2639 R2635 \ R2640	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125

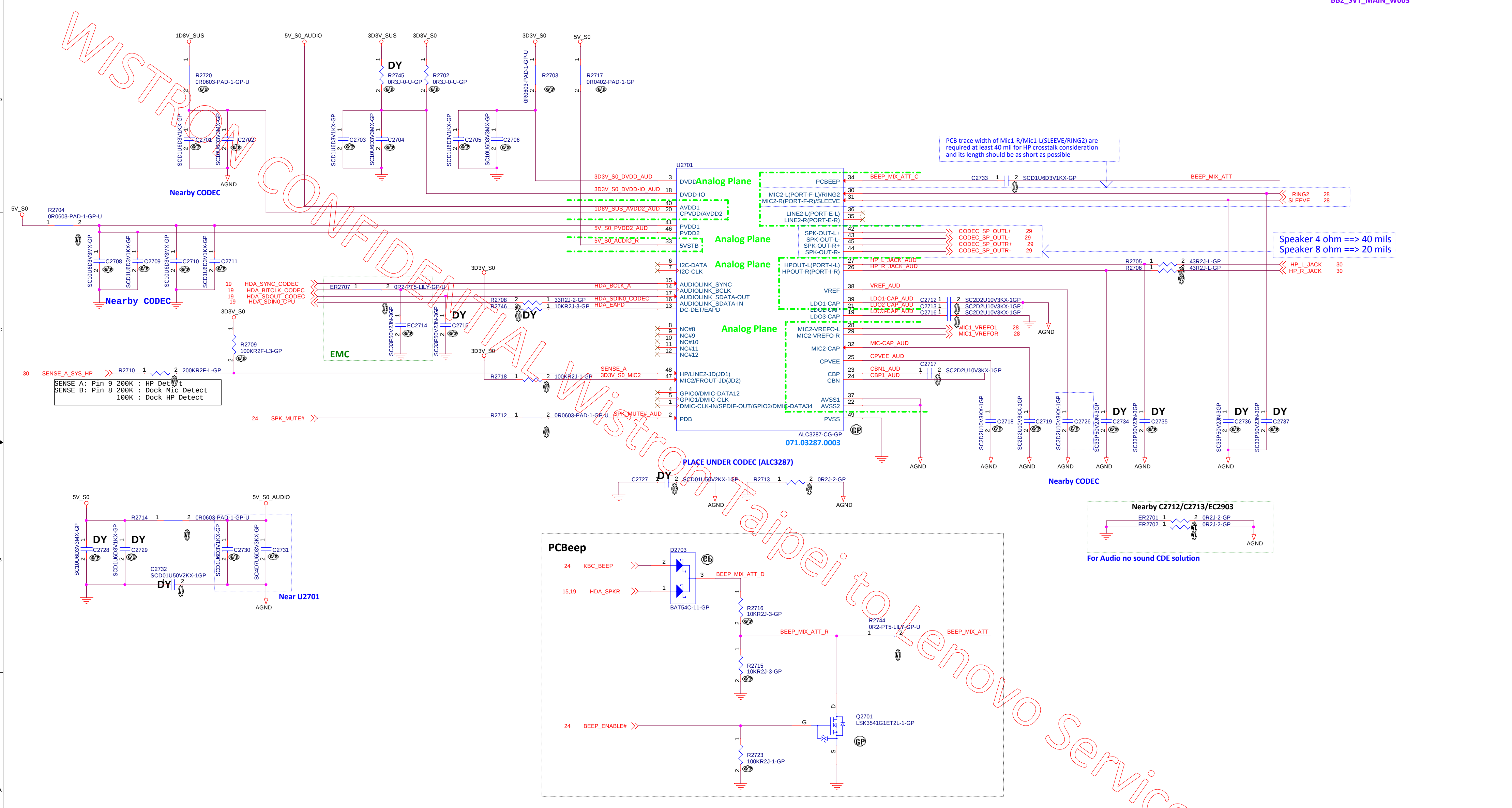
PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

TABLE:

ID	Target	Function
RT2601	PU5101	1D2V_S3
RT2602	PU4801	1V_VCCGT
RT2603	PQ5201	1D05V_SUS
RT2604	PU4701	1V_CPU_CORE
RT2605	PQ4505	5V_S5
RT2606	PQ4506	3D3V_S5
RT2607	PU4404	Charger-Buck
RT2608	PU4406	Charger-Boost

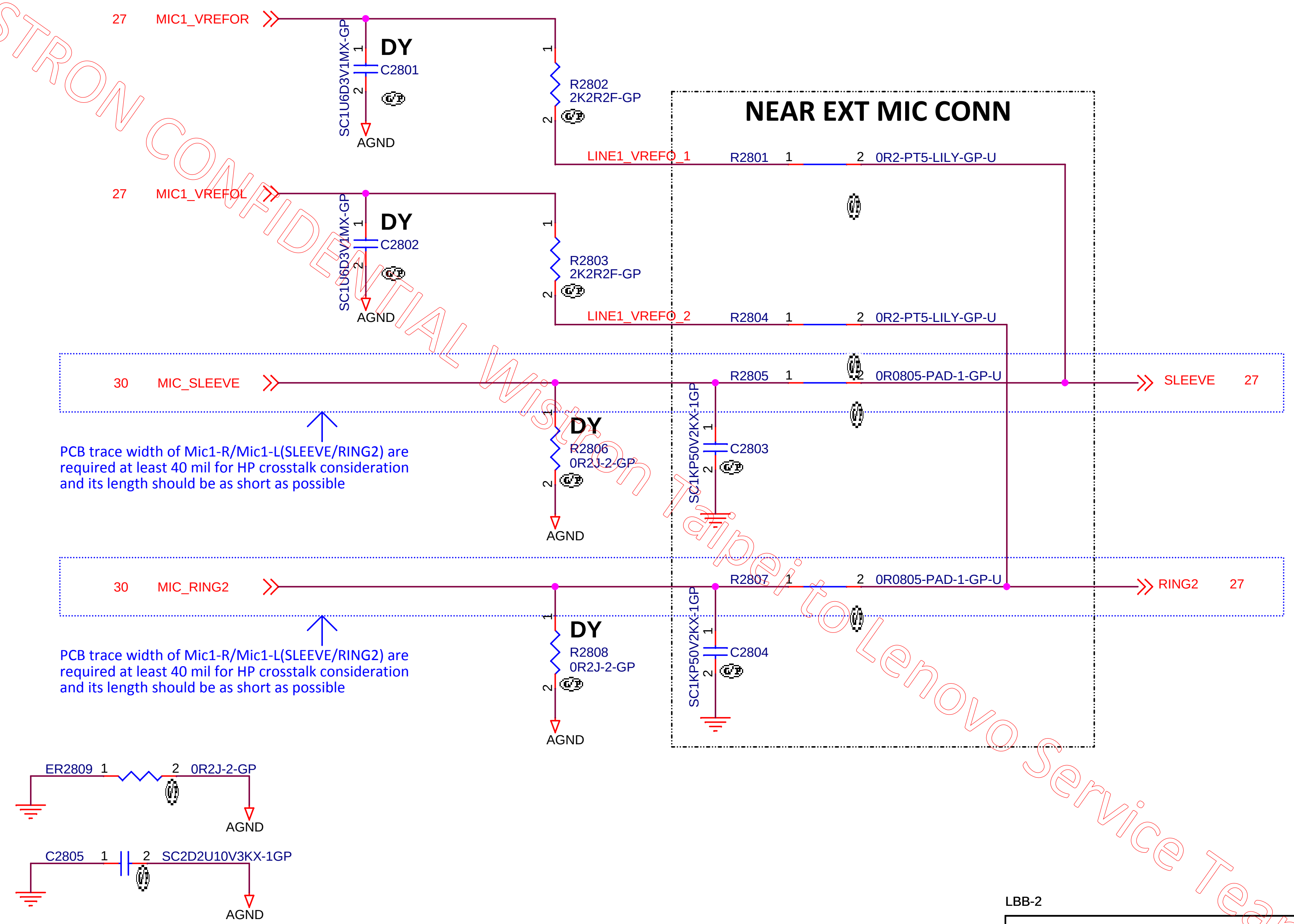
BB2_EVT_MAIN_W002
BB2_SVT_MAIN_W002
BB2_SVT_MAIN_W003



LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO (CODEC ALC3287)		
Size: Custom	Document Number: Bumblebee-2		Rev: 1
Date: Tuesday, March 03, 2020	Sheet 27 of 106		



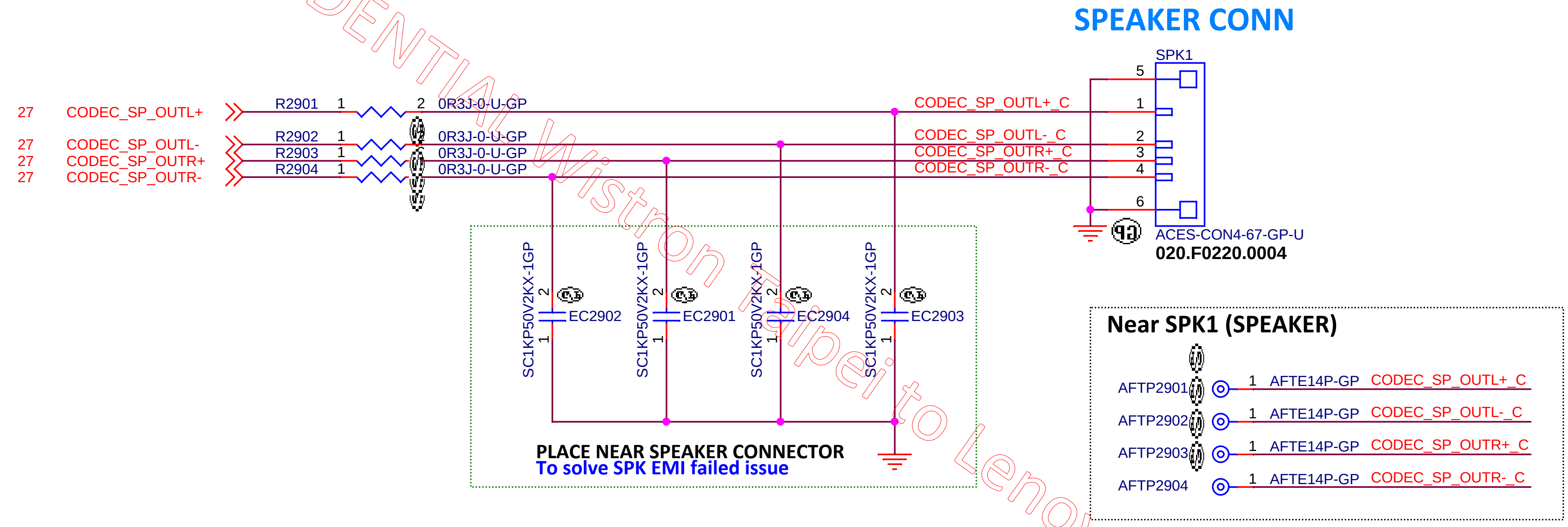
LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**AUDIO (MIC I/F)**	
Size A4	Document Number **Bumblebee-2**	Rev **1**
Date: Tuesday, March 03, 2020	Sheet 28 of 106	

Main Func = AUDIO

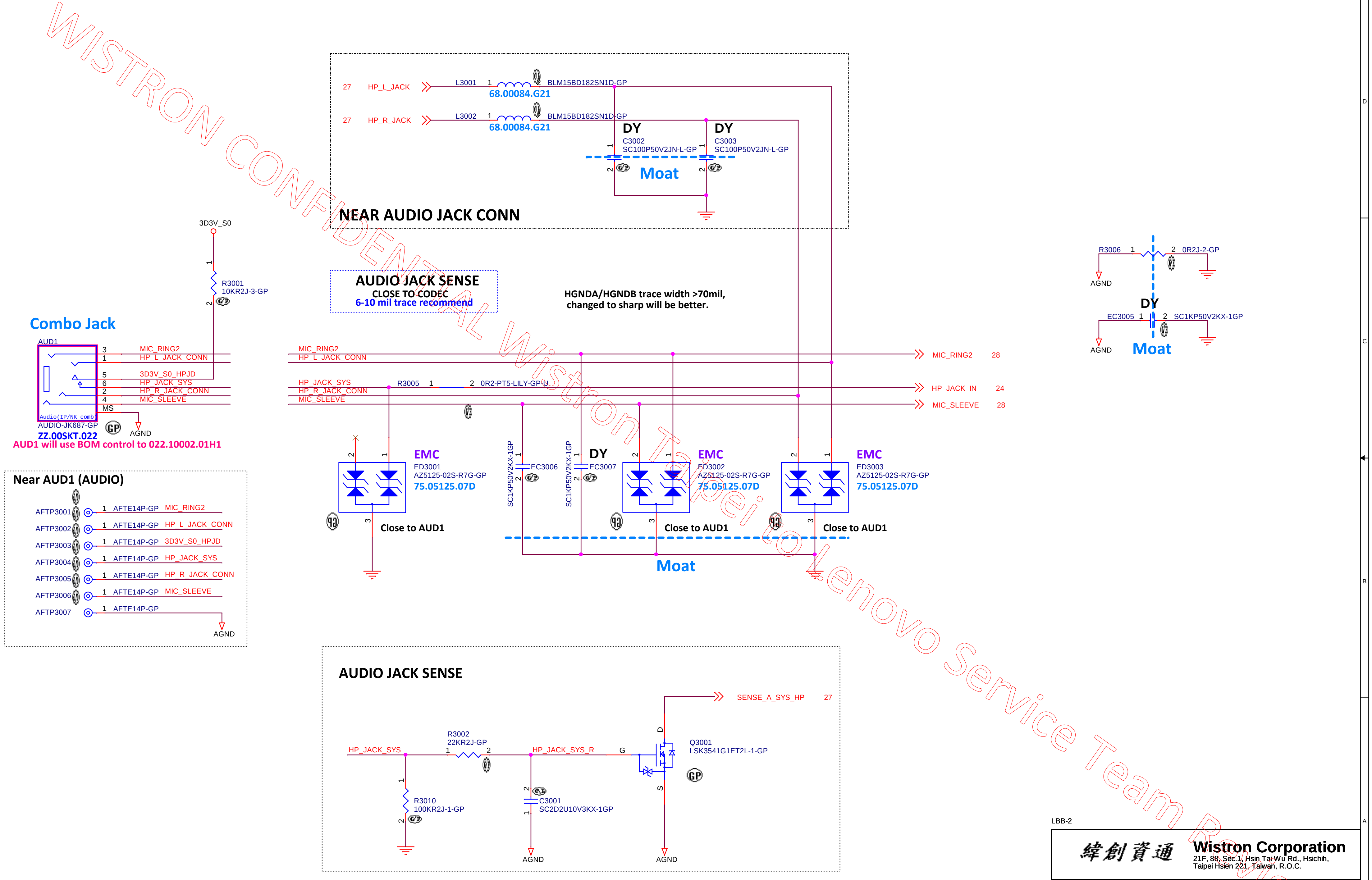
BB2_SVT_MAIN_W003



LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

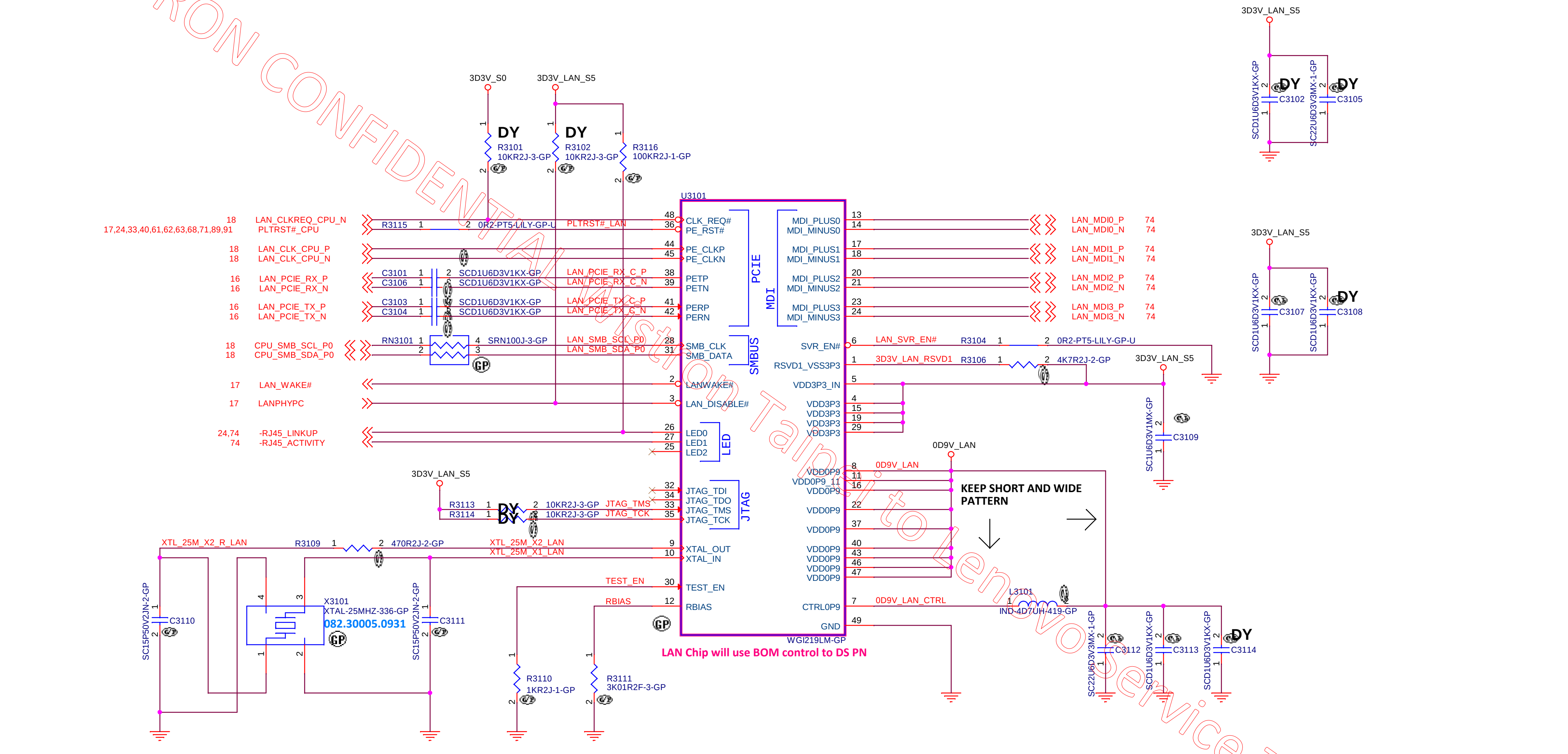
Title	AUDIO (SPEAKER)	
Size A4	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 29 of 106	



LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO (AUDIO JACK)	
Size A3	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 30 of 106	



25MHz (X3101)

TXC	7R25000008	082.30005.0931
HARMONY	X2V025000DC1H-HU	082.30005.0A81
MURATA	XRCGB25M000F2P40R0	082.30005.0911

LBB-2

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN (GIGA_WGI219LM)*

Size: A3 | Document Number: **Bumblebee-2** | Rev: 1

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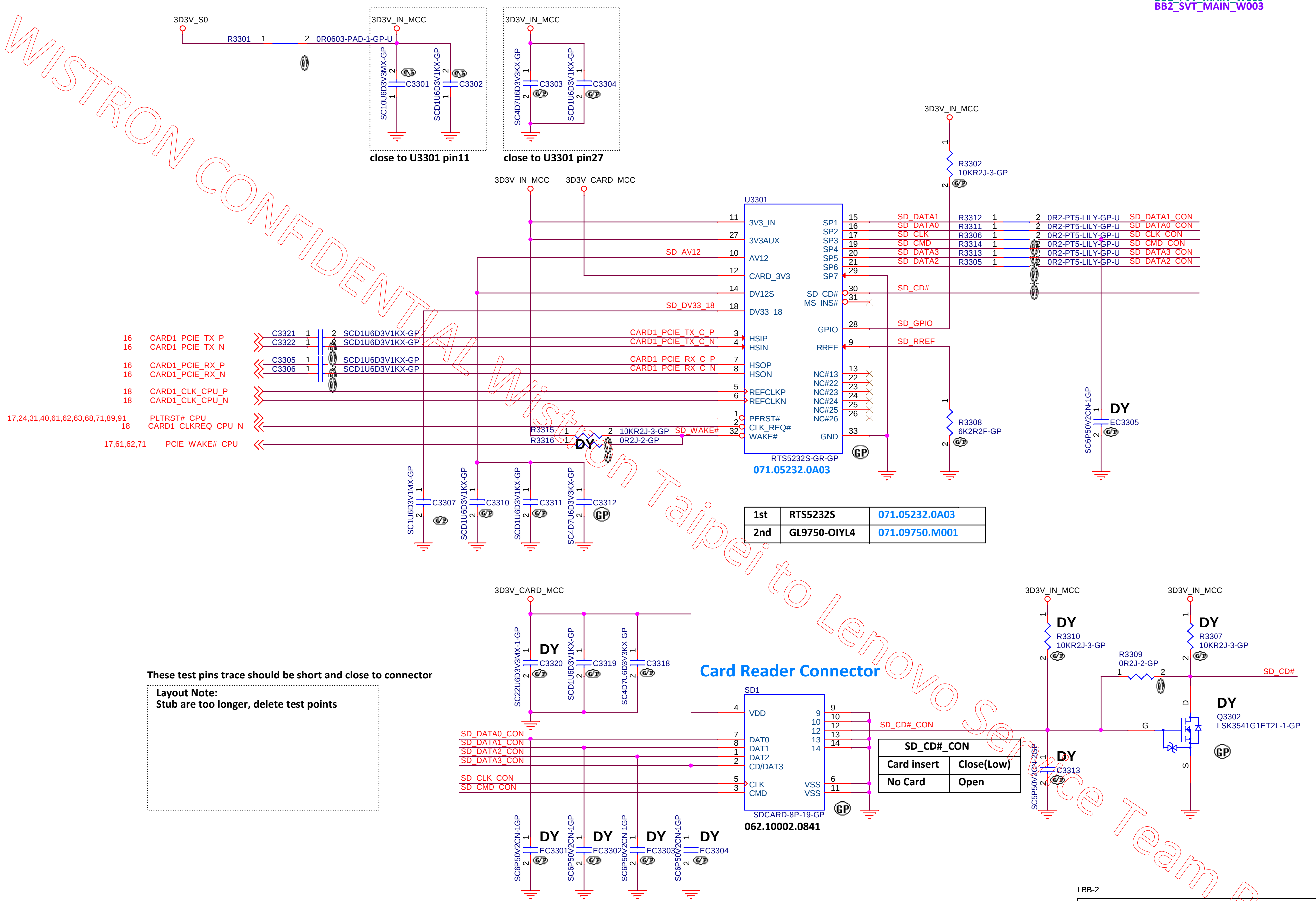
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN (RSVD)**		
Size: A4	Document Number: **Bumblebee-2**	Rev: **1**
Date: Tuesday, March 03, 2020	Sheet 32 of 106	

BB2_FVT_MAIN_W009
BB2_SVT_MAIN_W003



1st	RTS5232S	071.05232.0A03
2nd	GL9750-OIYL4	071.09750.M001

SD_CD#_CON	
Card insert	Close(Low)
No Card	Open

These test pins trace should be short and close to connector

Layout Note:
Stub are too longer, delete test points

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD READER (SDIO/CONN)

Size: A3 | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020 | Sheet 33 of 106

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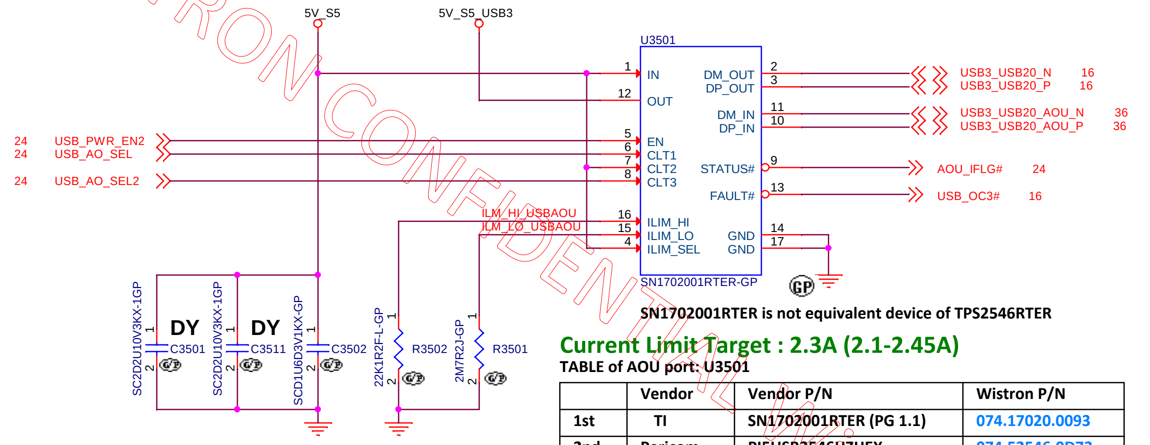
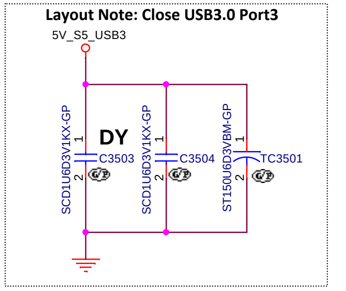
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB (RSVD)	
Size A4	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 34 of 106	

Main Func = USB Charger

For USB3.0 System Port3 (For AOU)





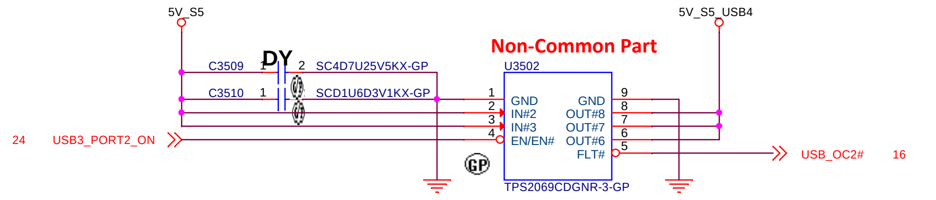
SN1702001RTER is not equivalent device of TPS2546RTER

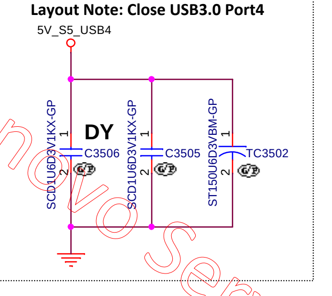
Current Limit Target : 2.3A (2.1-2.45A)

TABLE of AOU port: U3501

	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER (PG 1.1)	074.17020.0093
2nd	Pericom	PI5USB2546HZHEX	074.52546.0D73

For USB3.0 System Port4





Continous Current Limit 1.5A

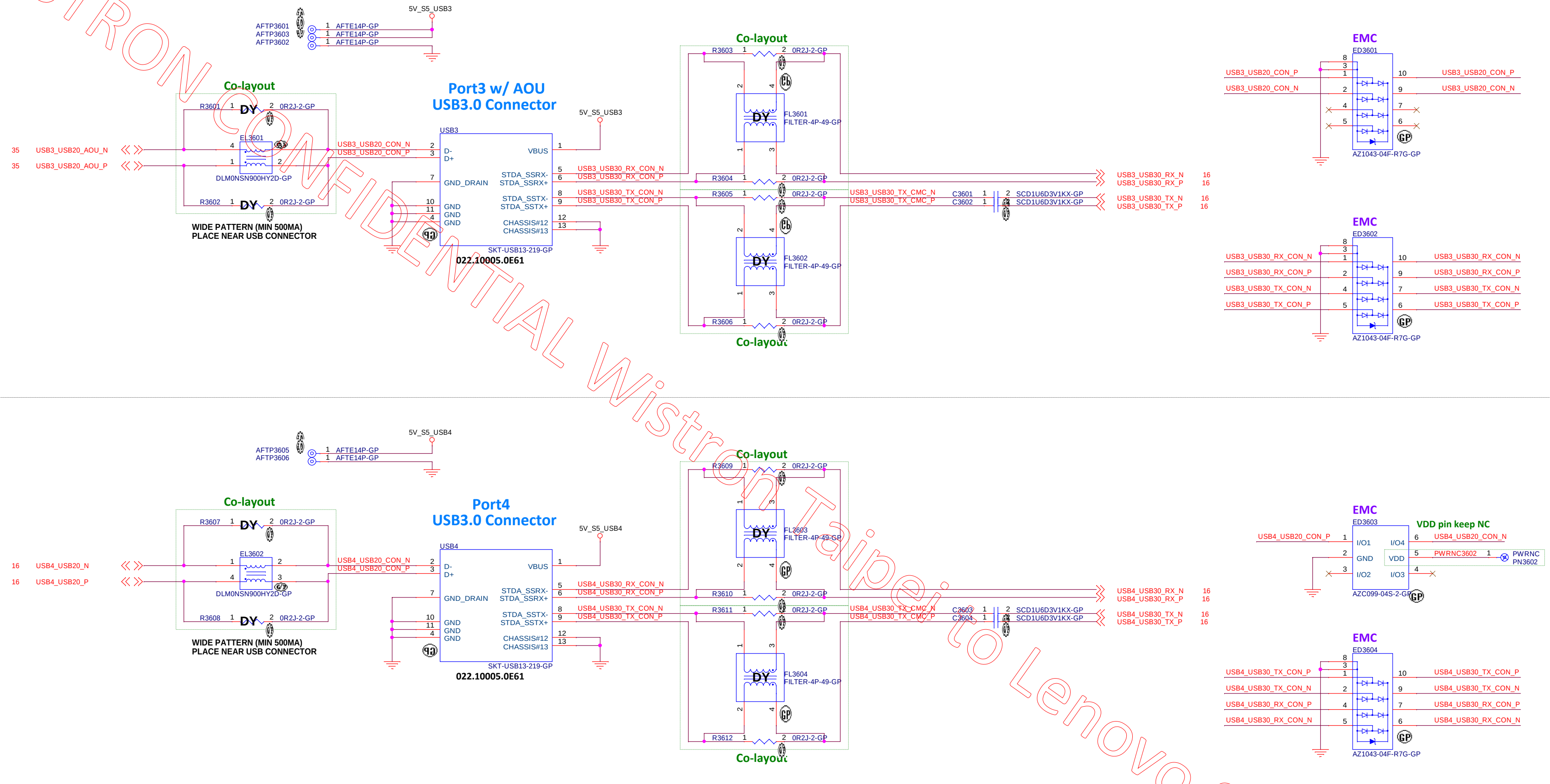
TABLE of USB 3.0 port: U3502

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGNR	074.02069.M001
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G

LBB-2

Main Func = USB3.0 Port3 w/ AOU

Main Func = USB3.0 Port4



LBB-2

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	USB (USB3.0 CONN)
Size A2	Document Number: Bumblebee-2
Rev	1
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5 4 3 2 1

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***USB (RSVD)***
Size A4	Document Number **Bumblebee-2** Rev **1**
Date: Tuesday, March 03, 2020	Sheet 37 of 106

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SEQUENCE (RSVD)***	
Size A4	Document Number **Bumblebee-2**	Rev **1**
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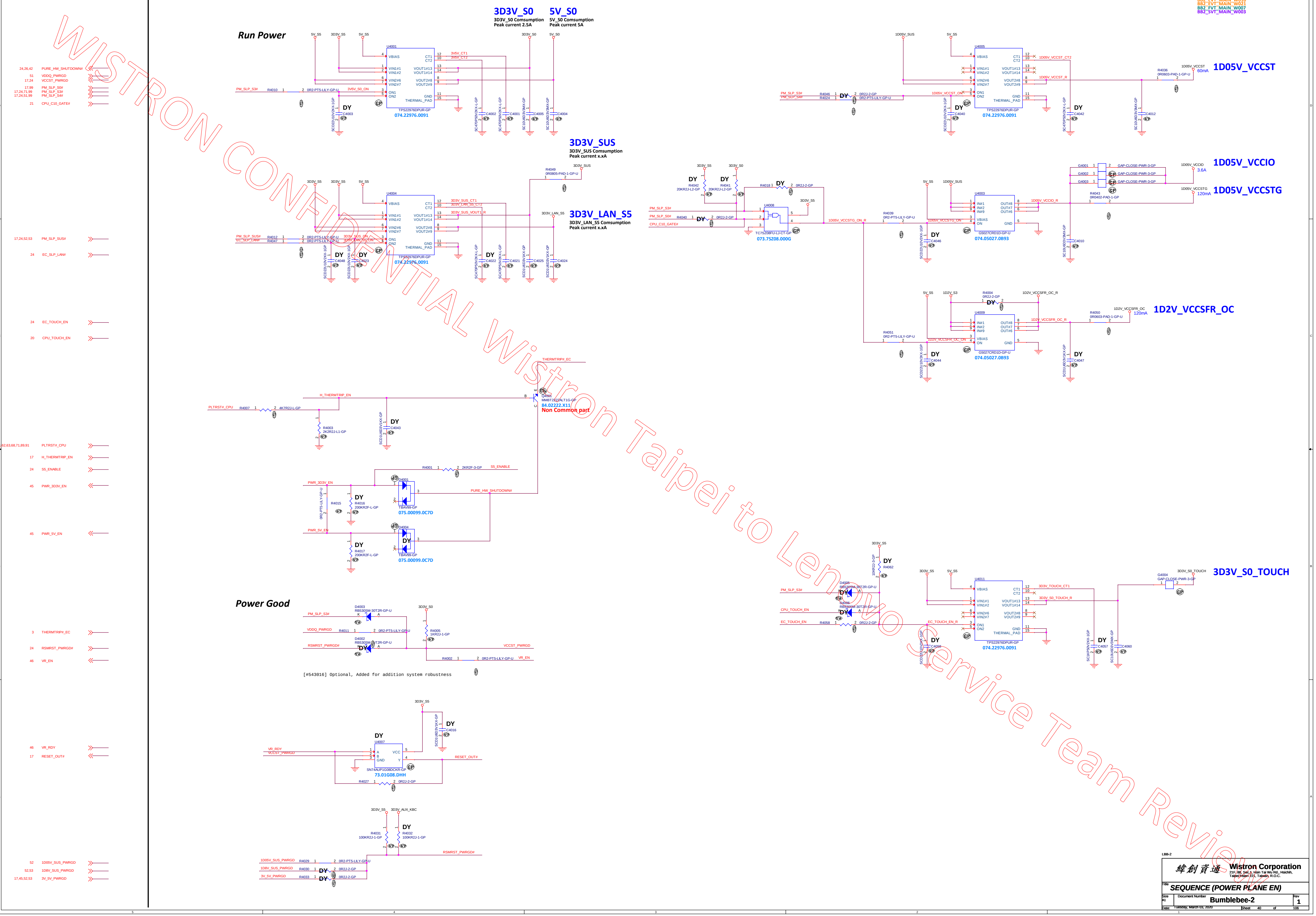
Power Plane & Sequence



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LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
SEQUENCE (RSVD)		
Size: A4	Document Number: **Bumblebee-2**	Rev: **1**
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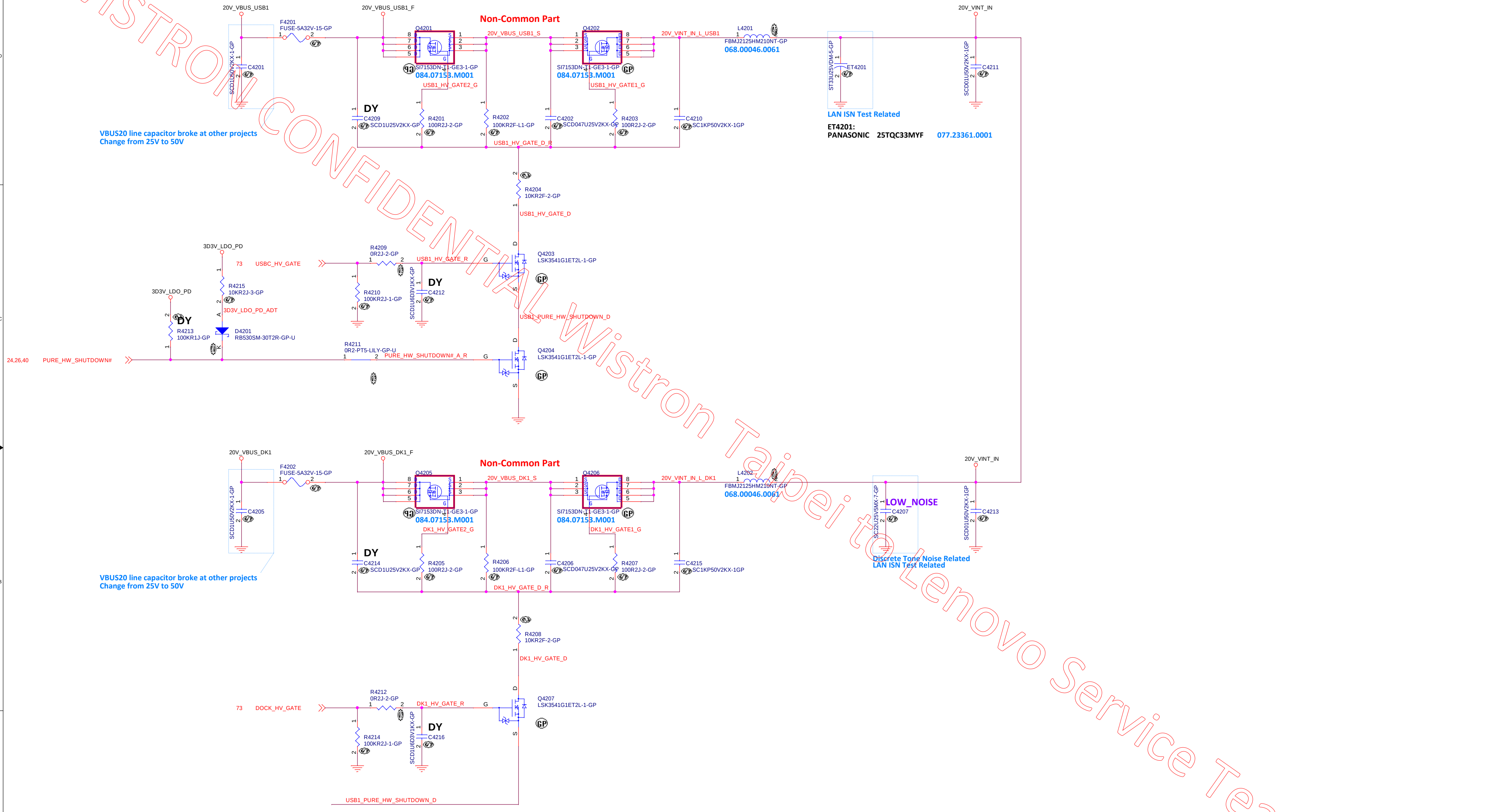
BB2_EVT_MAIN_W006
BB2_EVT_MAIN_W008
BB2_SIT_MAIN_W012
BB2_SVT_MAIN_W003

Q4201, Q4202, Q4205, Q4206

1st	VISHAY	SI7153DN-T1-GE3	084.07153.M001
2nd	AOS	AONR21357	084.21357.0A37
~~	~~AOS~~	~~AON7409~~	~~084.07409.M001~~
~~	~~FAIRCHILD~~	~~FDMC6679AZ~~	~~084.06679.M001~~

EOL soon
had supply issue (OBS part)



LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	INT IO (DC-IN)	
Size A2	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 42 of 106	

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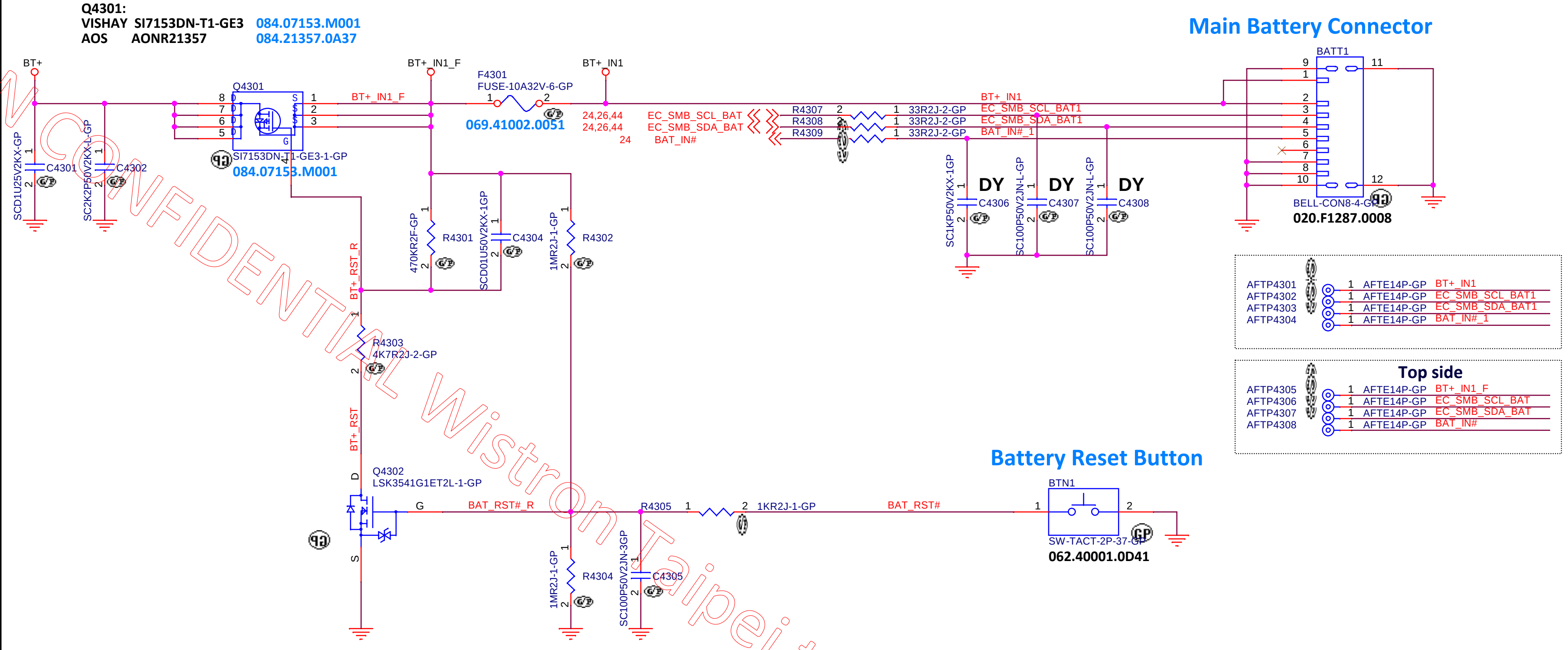

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (BATT CONN)

Size: A3 | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020

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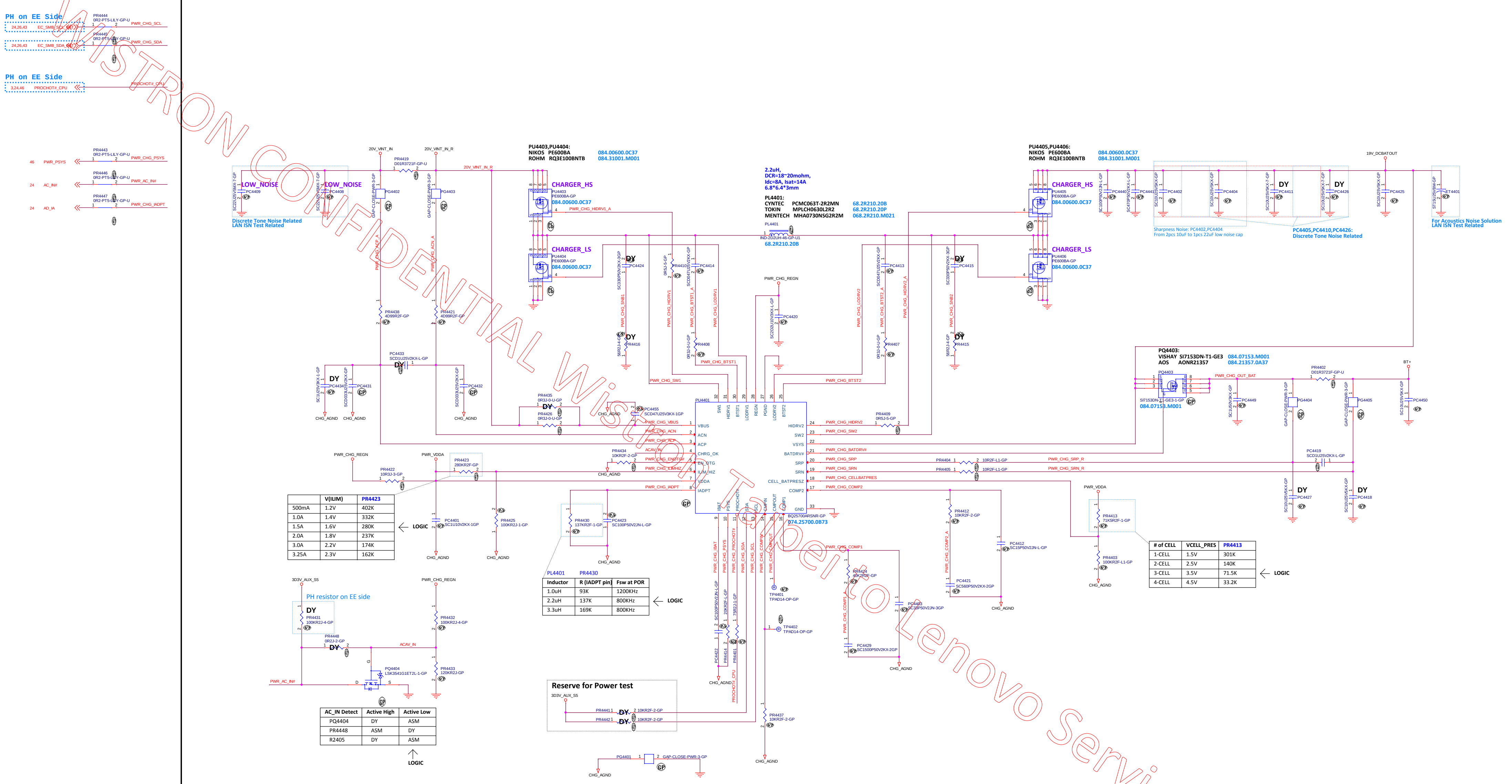


	V(ILIM)	PR4423
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

LOGIC

PL4401 PR4430

Inductor	R (IADPT pin)	Fsw at POR
1.0uH	93K	1200KHz
2.2uH	137K	800KHz
3.3uH	169K	800KHz

LOGIC

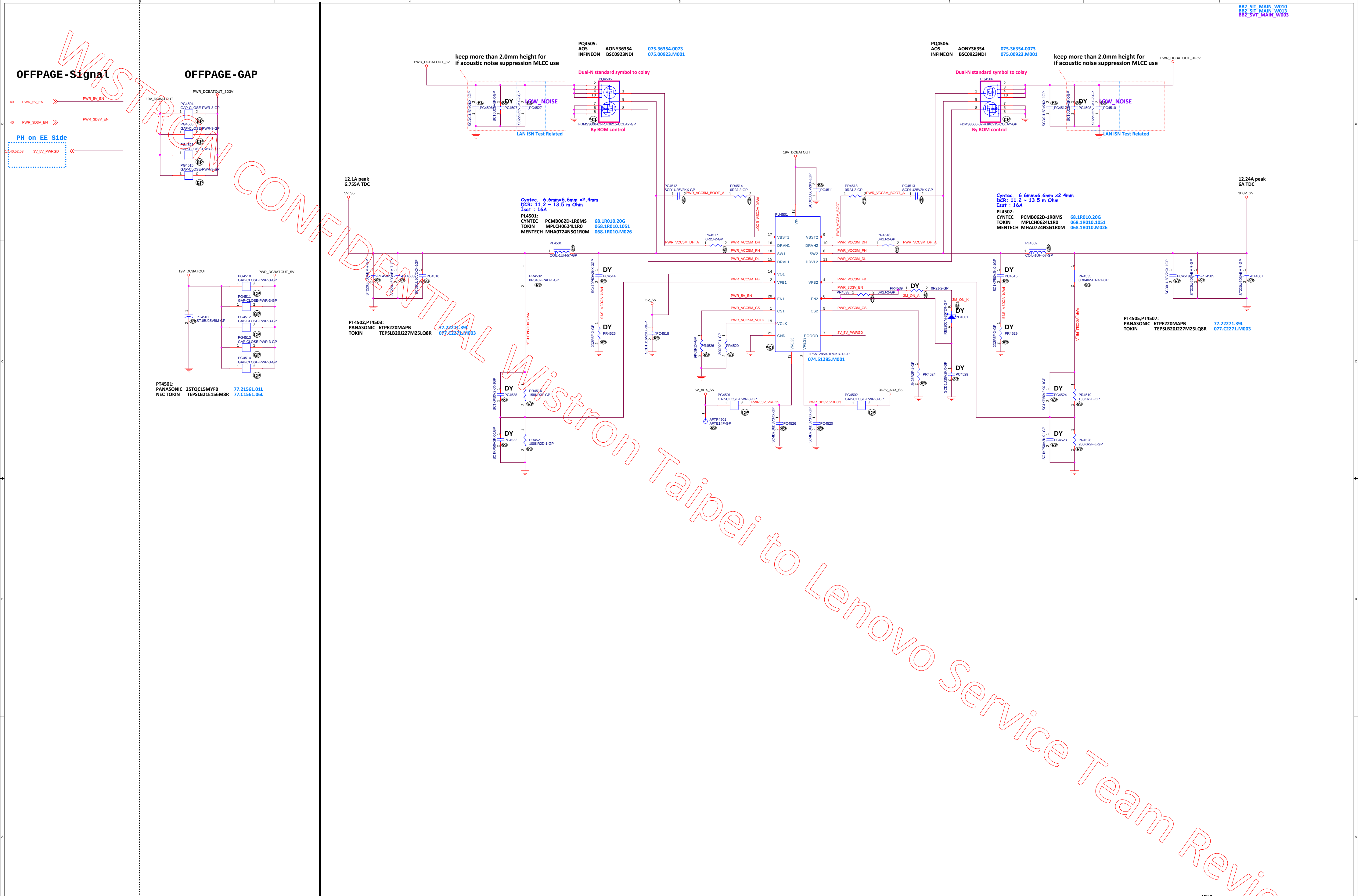
AC_IN Detect	Active High	Active Low
PQ4404	DY	ASM
PR4448	ASM	DY
R2405	DY	ASM

LOGIC

# of CELL	VCELL_PRES	PR4413
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

LOGIC

LBB-2



LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER (TPS51285B_5V/3D3V)**

Size: A1 | Document Number: **Bumblebee-2** | Rev: 1

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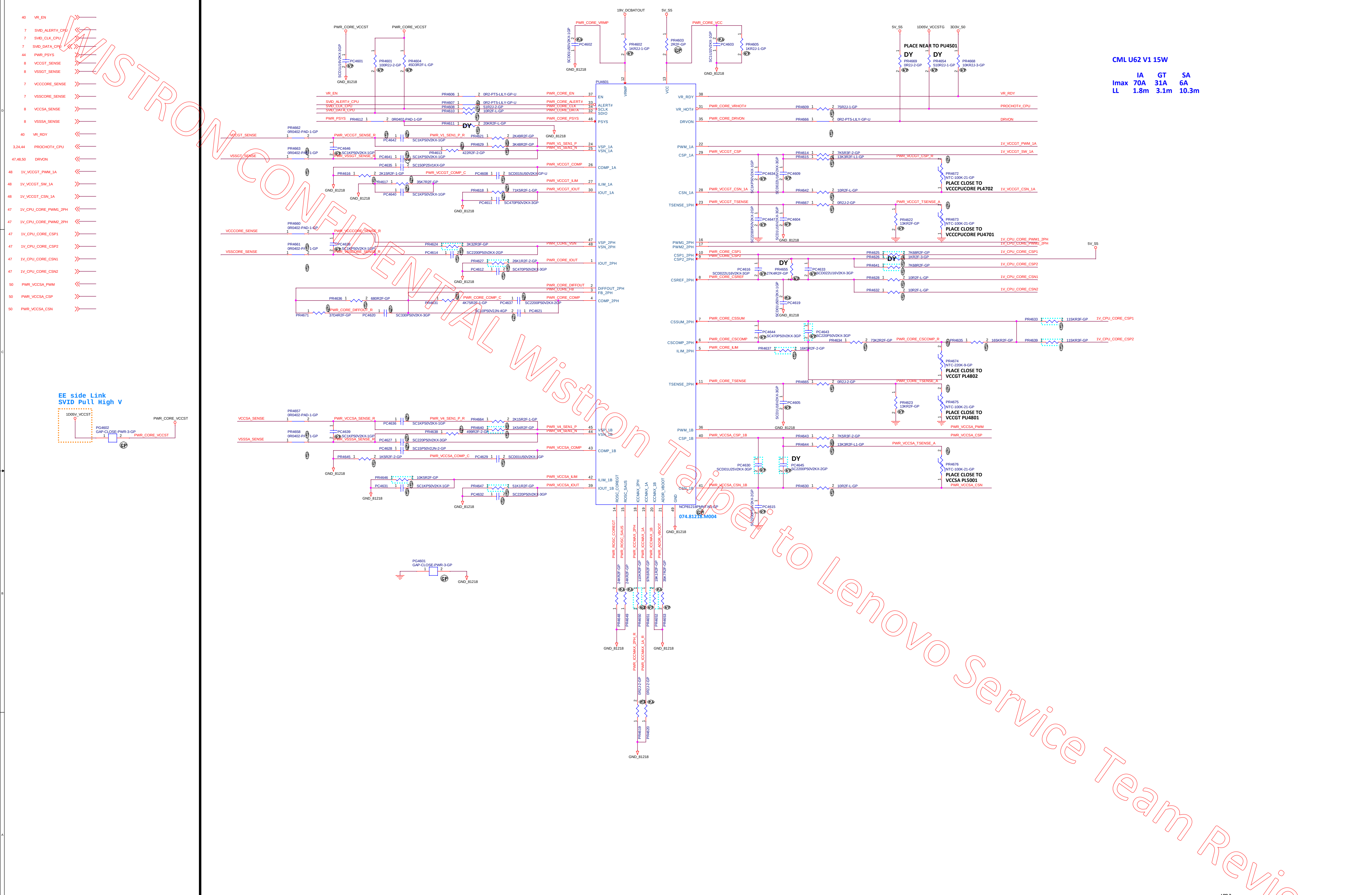


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

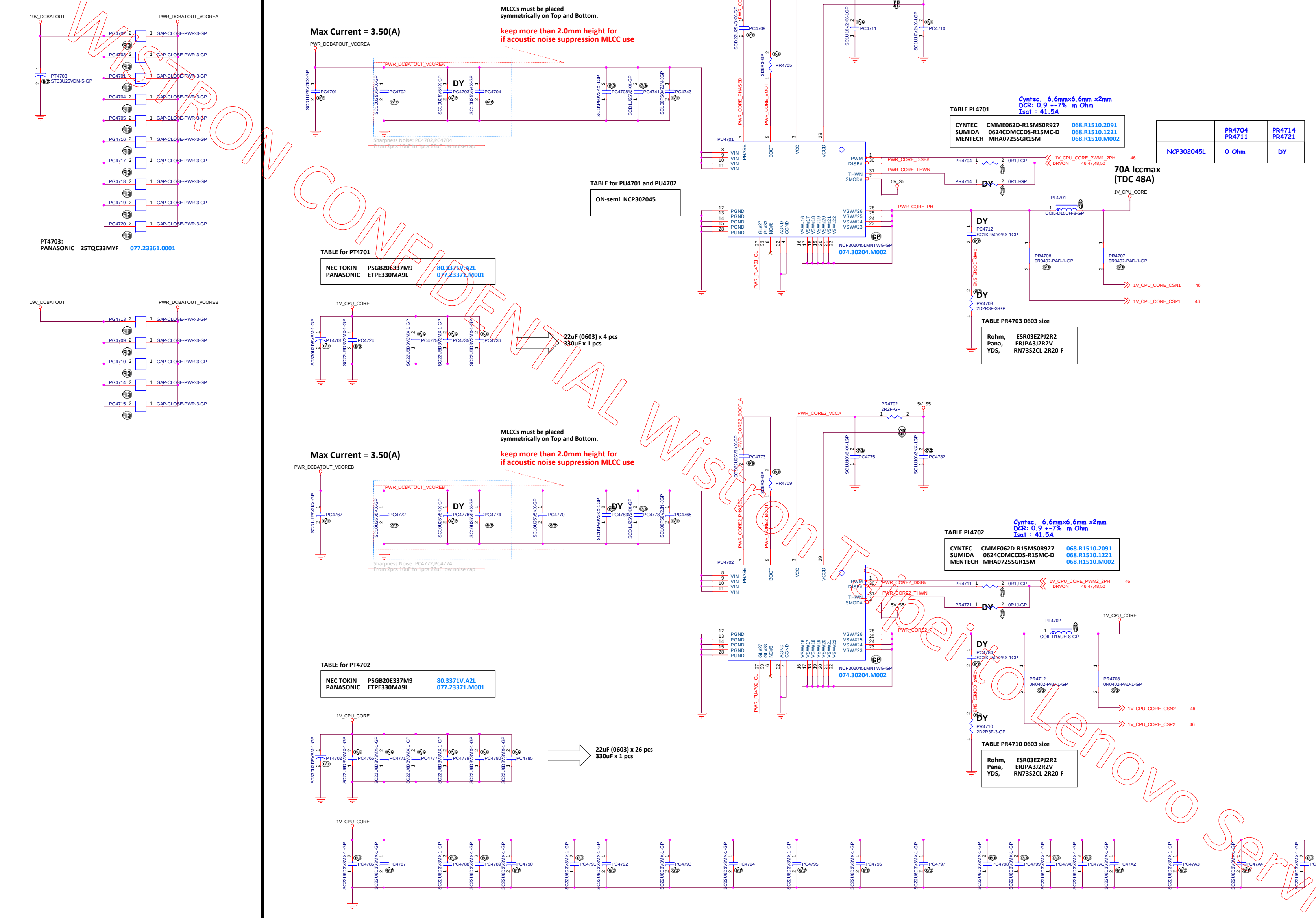
Title: POWER (NCP81218P_IMVP8)

Size: A1 | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020 | Sheet 46 of 106

Main Func = CPU_CORE

OFFPAGE



PT4703:
PANASONIC 25TQC33MYF 077.23361.0001

TABLE for PU4701 and PU4702

ON-semi	NCP302045

TABLE for PT4701

NEC TOKIN	PSGB20E337M9	80.3371V.A2L
PANASONIC	ETPE330MA9L	077.23371.M001

TABLE for PT4702

NEC TOKIN	PSGB20E337M9	80.3371V.A2L
PANASONIC	ETPE330MA9L	077.23371.M001

TABLE PL4701

Cyntec. 6.6mmx6.6mm x2mm
DCR: 0.9 +-7% m Ohm
Isat : 41.5A

CYNTEC	CMME062D-R15MS0R927	068.R1510.2091
SUMIDA	0624CDMCCDS-R15MC-D	068.R1510.1221
MENTECH	MHA0725SGR15M	068.R1510.M002

	PR4704 PR4711	PR4714 PR4721
NCP302045L	0 Ohm	DY

TABLE PL4702

Cyntec. 6.6mmx6.6mm x2mm
DCR: 0.9 +-7% m Ohm
Isat : 41.5A

CYNTEC	CMME062D-R15MS0R927	068.R1510.2091
SUMIDA	0624CDMCCDS-R15MC-D	068.R1510.1221
MENTECH	MHA0725SGR15M	068.R1510.M002

TABLE PR4703 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

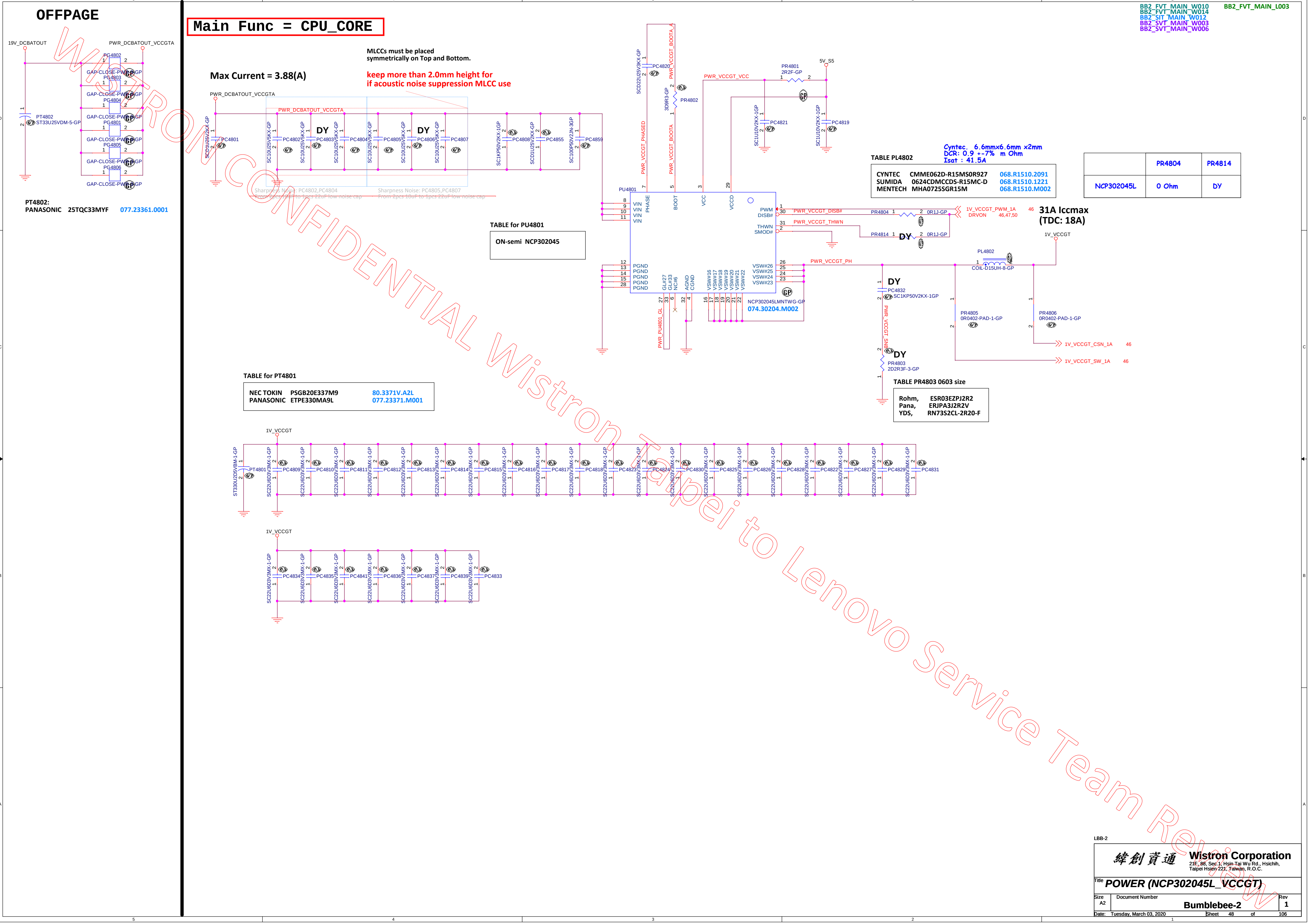
TABLE PR4710 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

OFFPAGE

Main Func = CPU_CORE

BB2_FVT_MAIN_W010
BB2_FVT_MAIN_W014
BB2_SIT_MAIN_W012
BB2_SVT_MAIN_W003
BB2_SVT_MAIN_W006
BB2_FVT_MAIN_L003



PT4802:
PANASONIC 25TQC33MYF 077.23361.0001

TABLE for PU4801

ON-semi NCP302045

TABLE PL4802

CYNTEC	CMME062D-R15MS0R927	068.R1510.2091
SUMIDA	0624CDMCCDS-R15MC-D	068.R1510.1221
MENTECH	MHA0725SGR15M	068.R1510.M002

	PR4804	PR4814
NCP302045L	0 Ohm	DY

TABLE for PT4801

NEC TOKIN	PSGB20E337M9	80.3371V.A2L
PANASONIC	ETPE330MA9L	077.23371.M001

TABLE PR4803 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (NCP302045L_VCCGT)

Size A2 | Document Number: Bumblebee-2 | Rev 1

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Main Func = CPU_CORE

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LBB-2

Main Func = CPU_CORE

BB2_FVT_MAIN_W010
BB2_SVT_MAIN_W006

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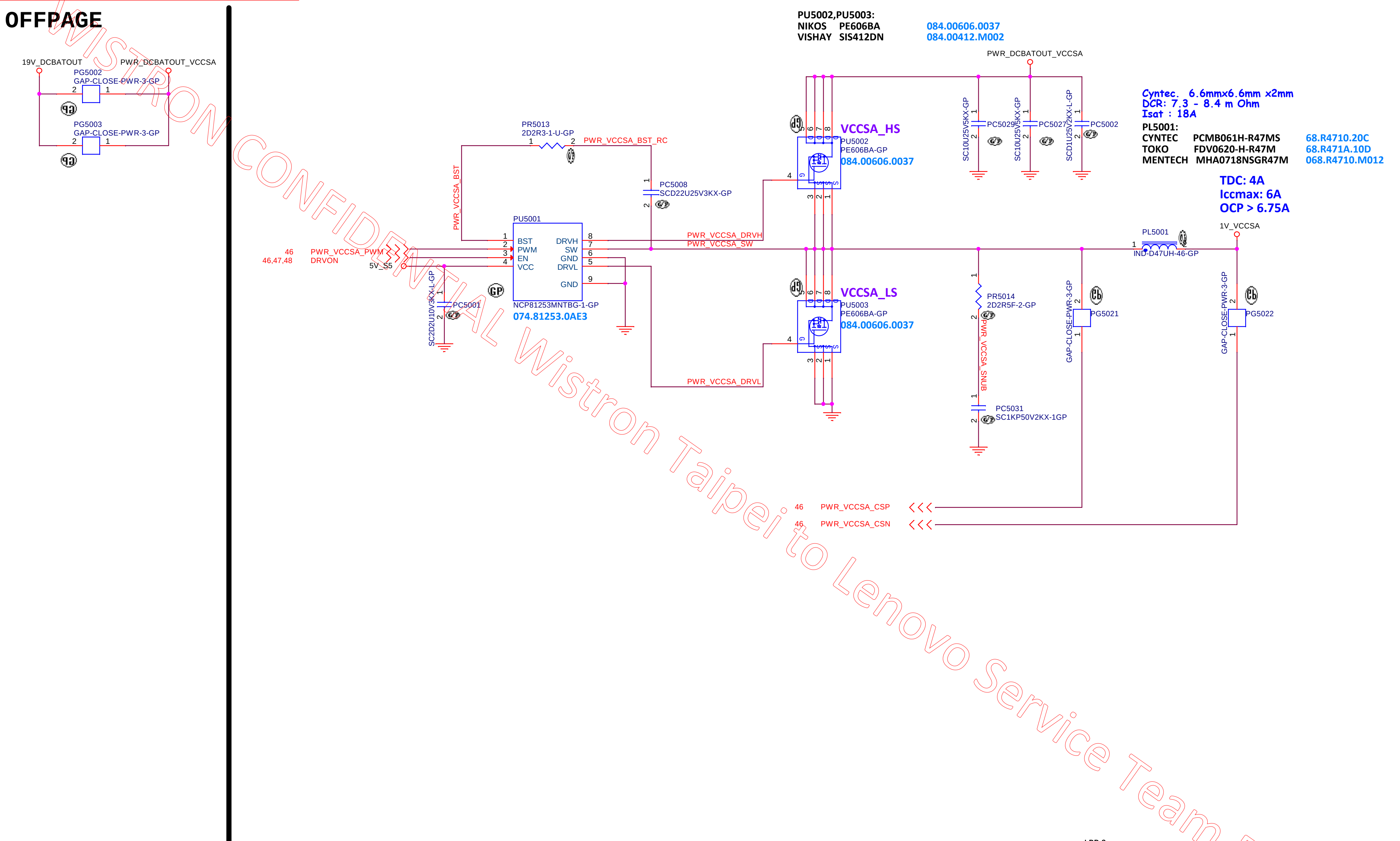
PU5002,PU5003:
NIKOS PE606BA 084.00606.0037
VISHAY SIS412DN 084.00412.M002

Cyntec. 6.6mmx6.6mm x2mm
DCR: 7.3 - 8.4 m Ohm
Isat : 18A

PL5001:
CYNTEC PCMB061H-R47MS 68.R4710.20C
TOKO FDV0620-H-R47M 68.R471A.10D
MENTECH MHA0718NSGR47M 068.R4710.M012

TDC: 4A
Iccmax: 6A
OCP > 6.75A



LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (NCP81253MN_VCCSA)		
Size A3	Document Number: Bumblebee-2		Rev 1
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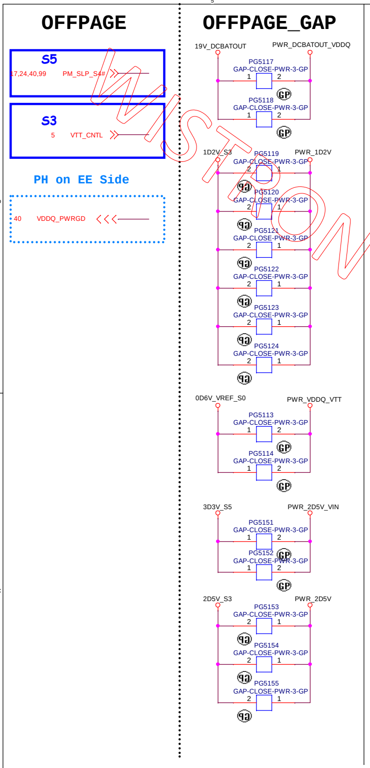

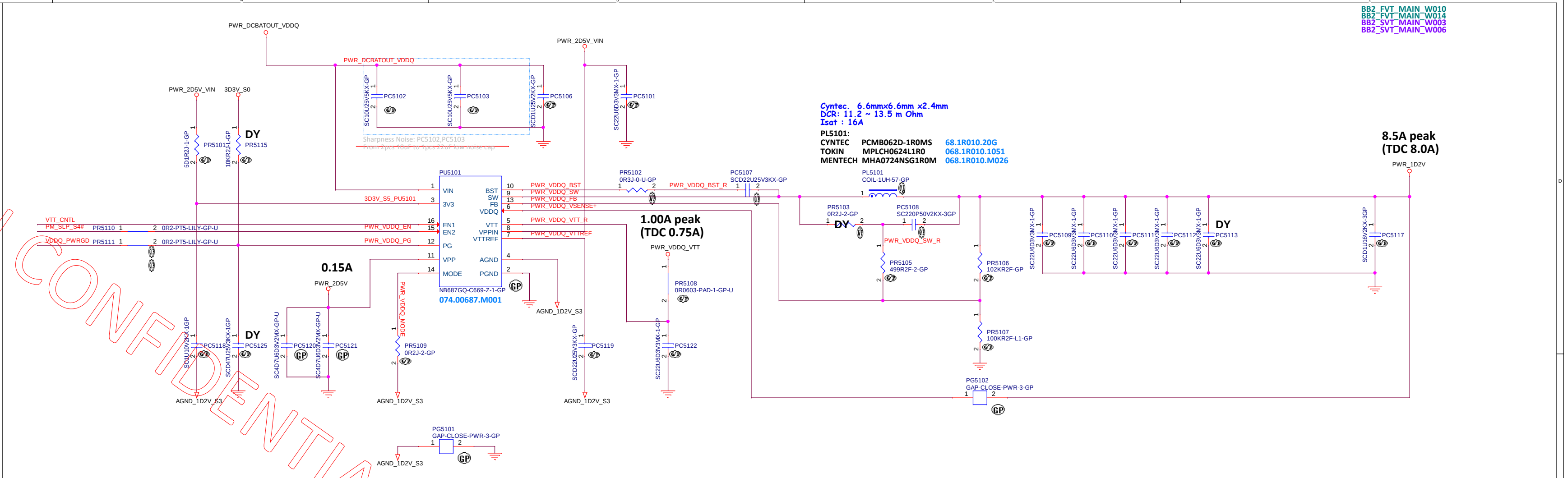

Table 1: EN1/EN2 Control

State	EN1	EN2	VDDQ	VPP	VTT REF	VTT
S0	High	High	On	On	On	On
S3	Low	High	On	On	On	Off (Hi-Z)
S4/S5	Low	Low	Off	Off	Off	Off
Others	High	Low	Off	Off	Off	Off

Table 2: Mode Selection

State	USM	Fs	Resistor to GND
M1	No	700kHz	0Ω
M2	Yes	700kHz	90kΩ
M3	No	500kHz	150kΩ
M4	Yes	500kHz	>230kΩ or float

LB8-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (NB687_1D2V/2D5V/0D6V

Size: Custom | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020 |

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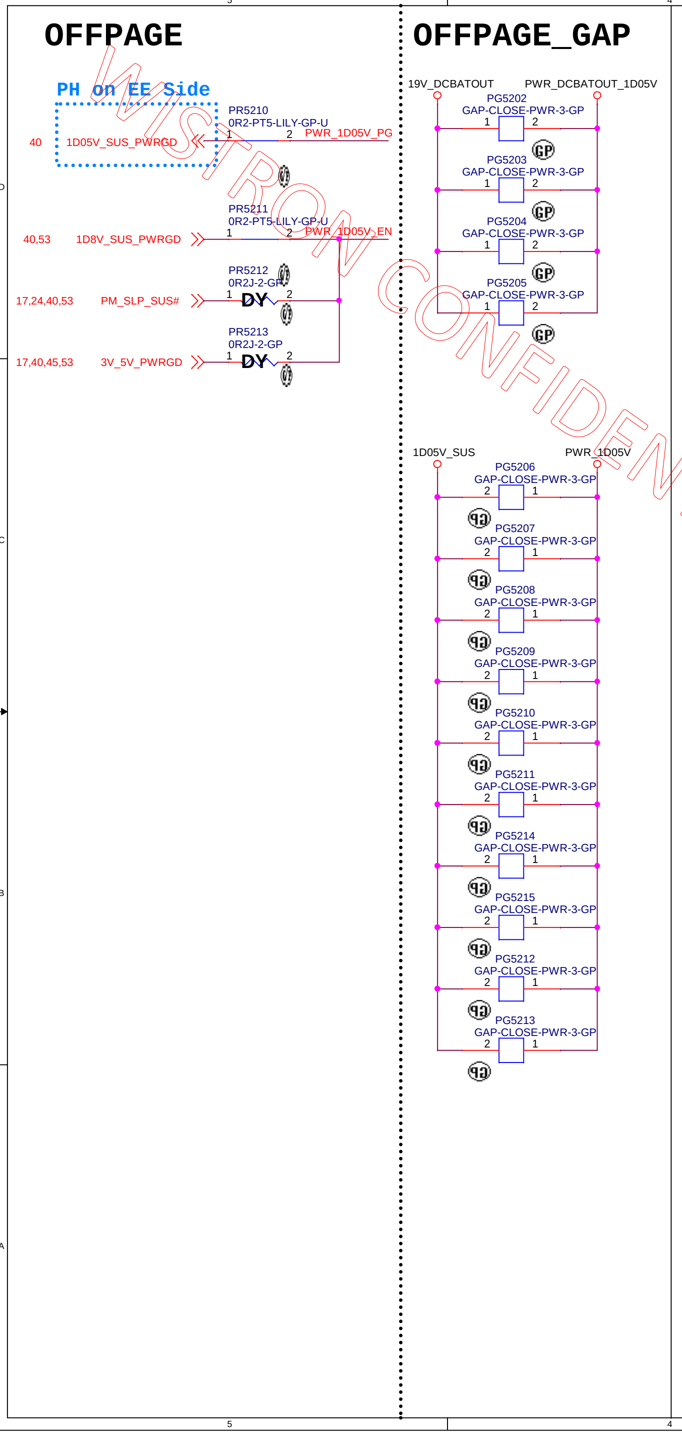
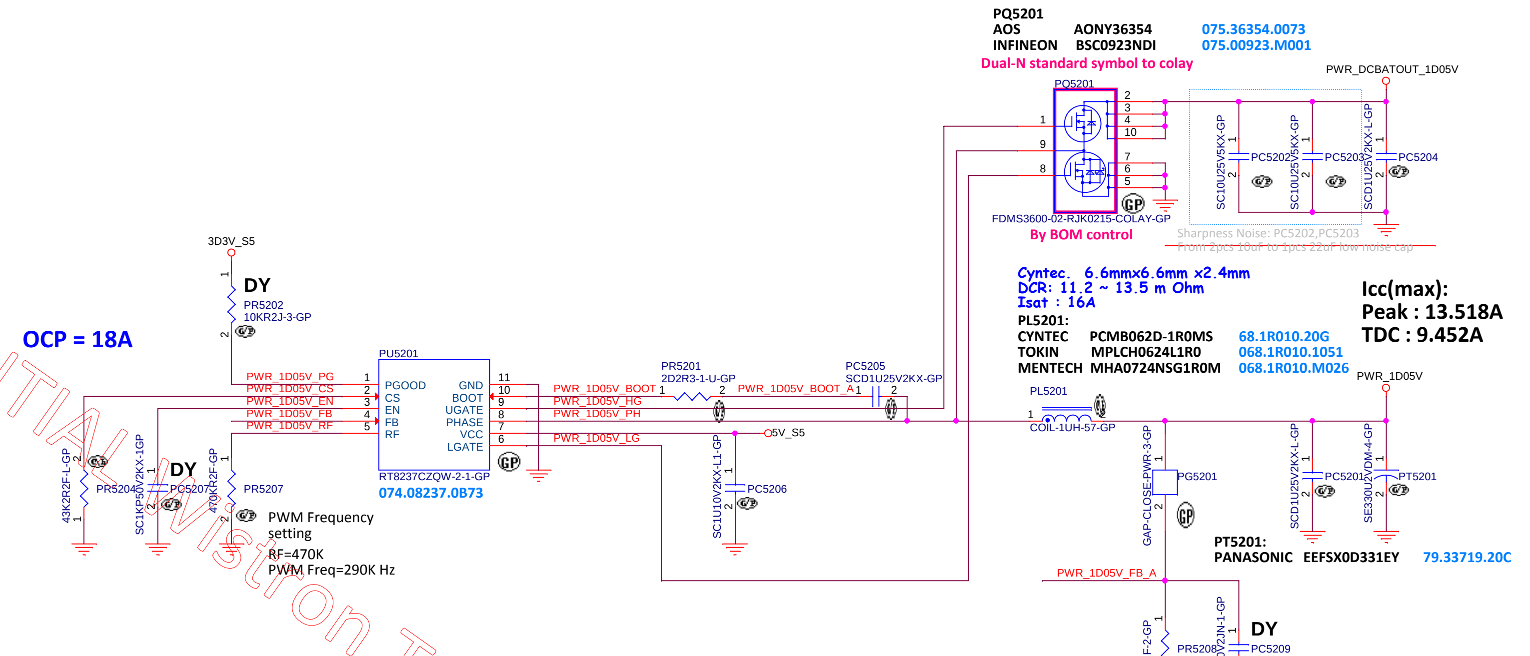


BB2_FVT_MAIN_W010
BB2_FVT_MAIN_W014
BB2_SIT_MAIN_W010
BB2_SIT_MAIN_W012
BB2_SVT_MAIN_W003
BB2_SVT_MAIN_W006



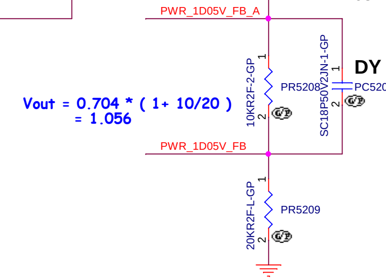


Table 1. RF Connection and Switching Frequency

R_{RF} (kΩ)	Switching Frequency (kHz)
470kΩ	290
200kΩ	340
100kΩ	380
39kΩ	430

<--- LOGIC

Note : For DEM, connect R_{RF} to GND; for CCM, connect R_{RF} to PGOOD.

$$V_{OUT} = V_{REF} \times \left(1+\frac{R1}{R2}\right)$$

where V_{REF} is 0.704V (typ.).

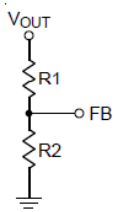


Figure 4. Setting V_{OUT} with a Resistive Voltage Divider

LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (RT8237C_1D05V)	
Size Custom	Document Number Bumblebee-2	Rev 1
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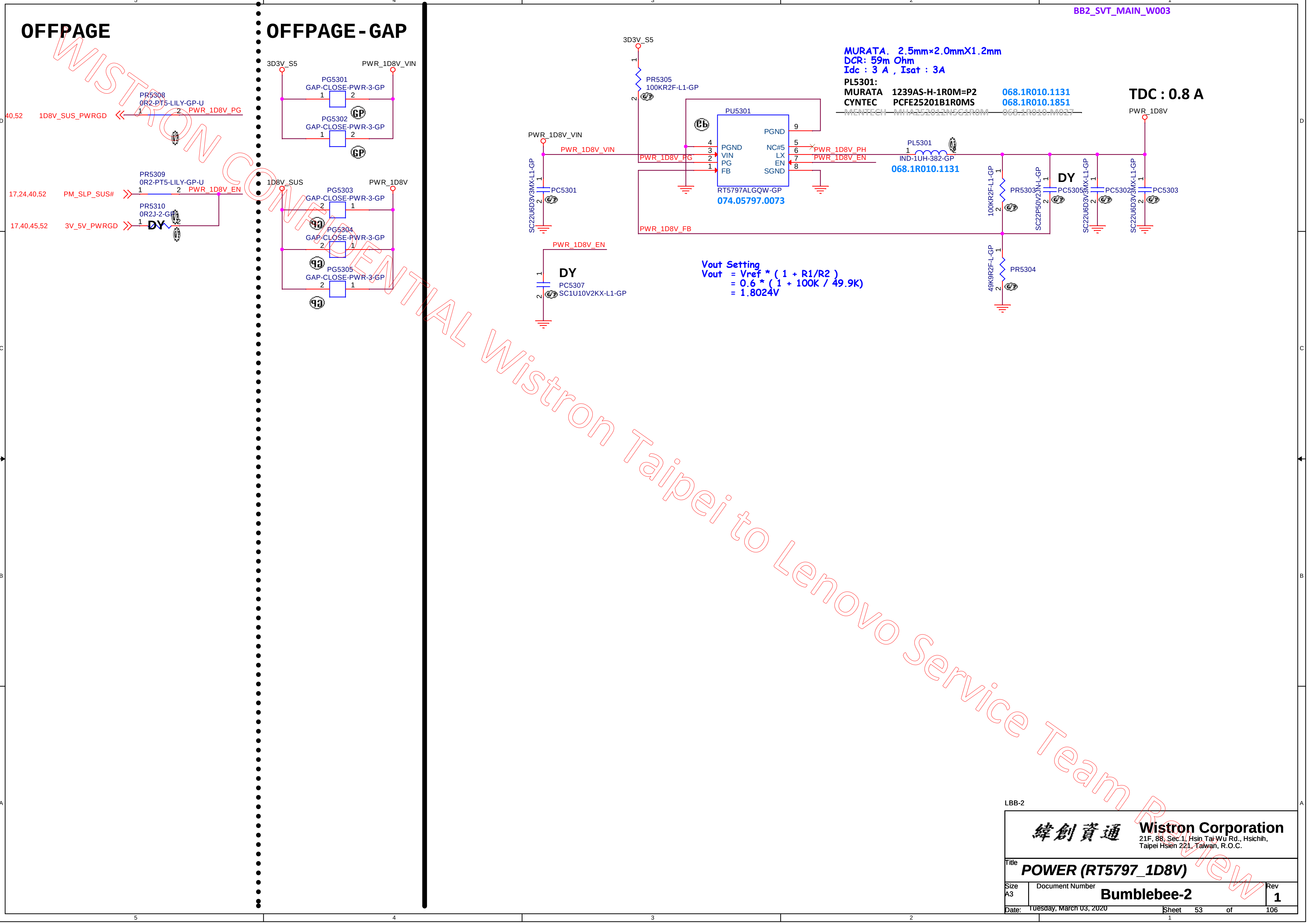

LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (RT5797_1D8V)	
Size A3	Document Number: Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 53 of 106	

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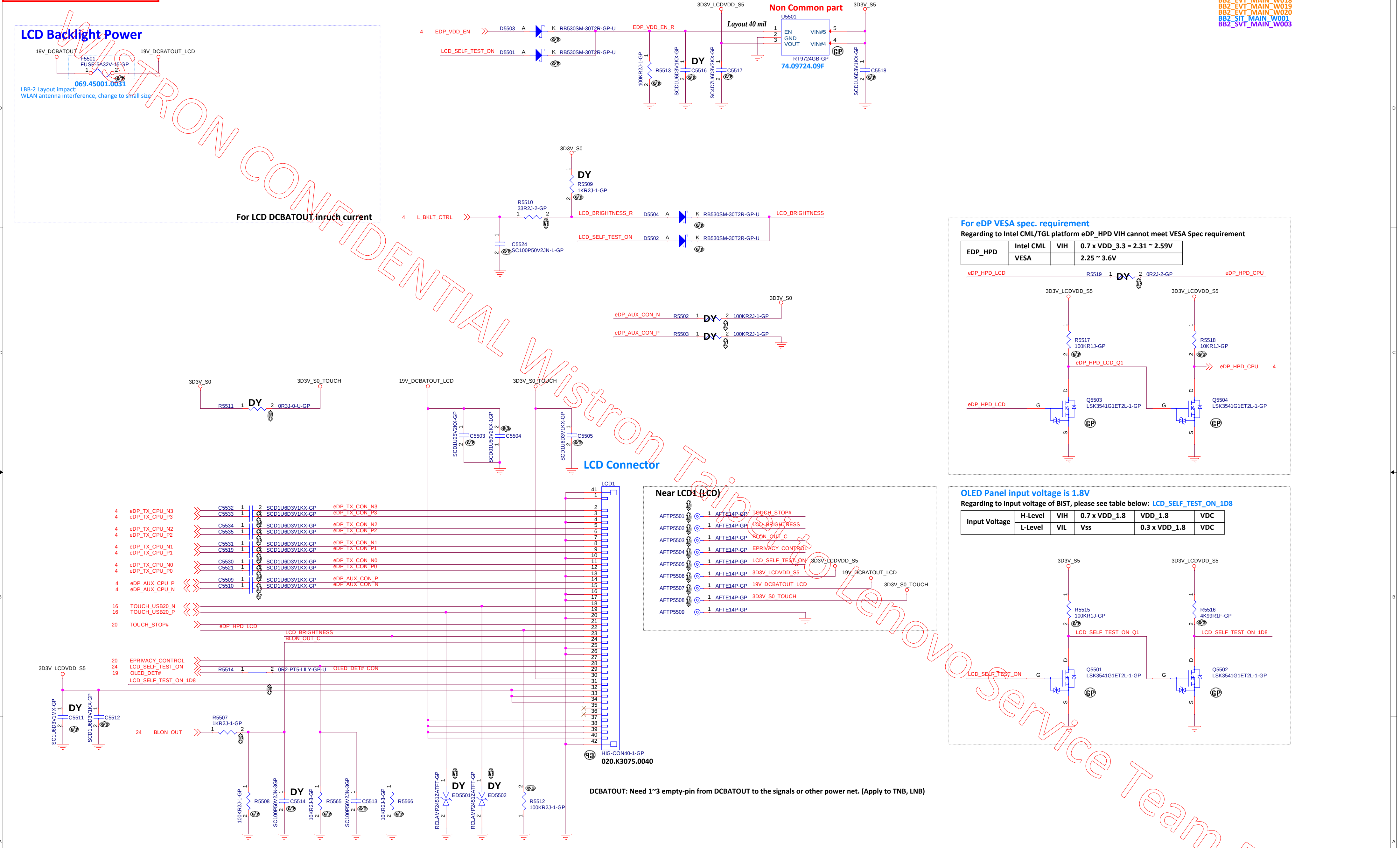
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER (RSVD)	
Size A4	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 54 of 106	

Main Func = LCD



LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DISPLAY (LCD/CAM/TOUCH)***

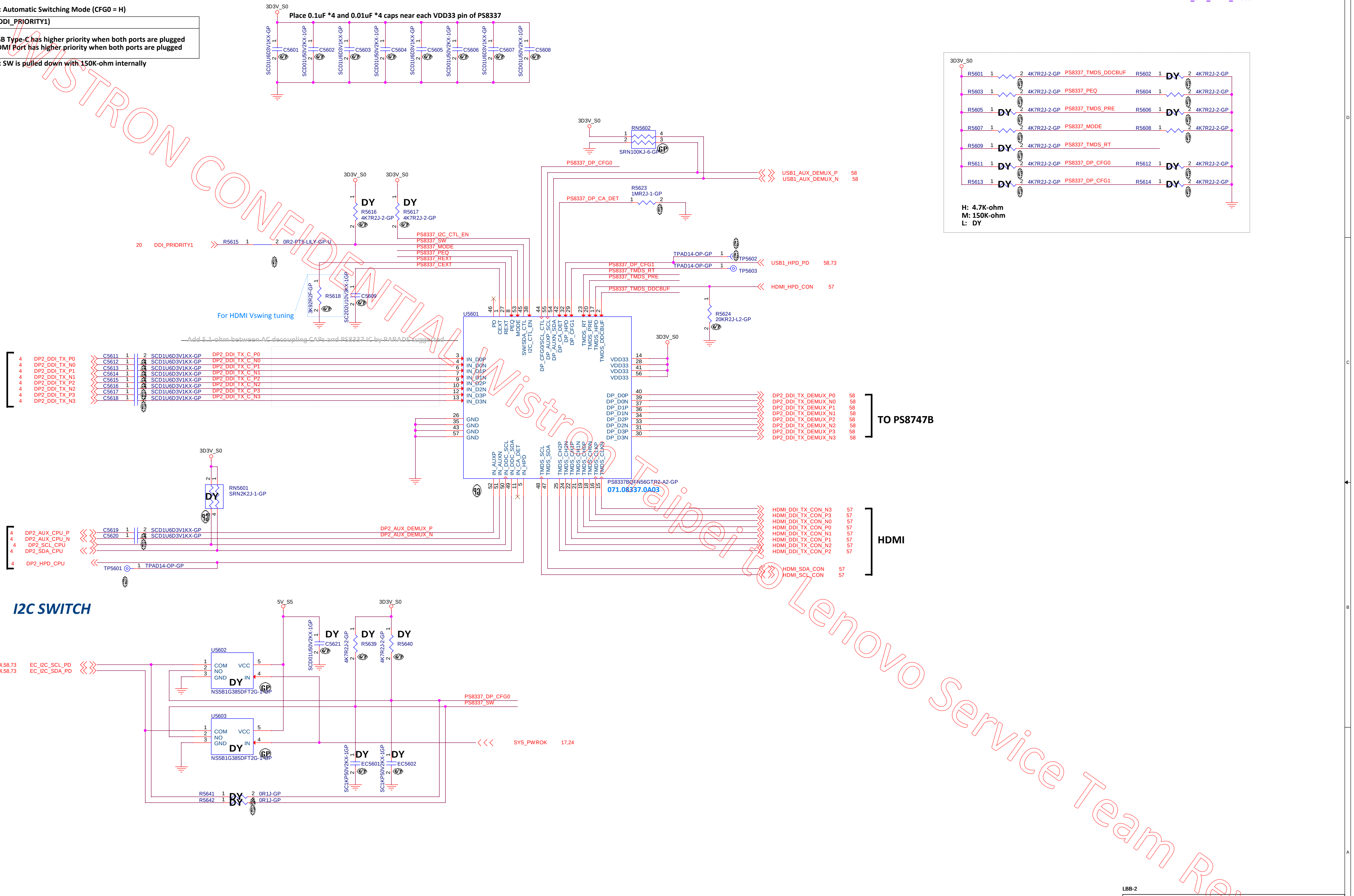
Size	Document Number	Rev
A2	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 55 of 106

TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY1)
L: USB Type-C has higher priority when both ports are plugged H: HDMI Port has higher priority when both ports are plugged

Note: SW is pulled down with 150K-ohm internally



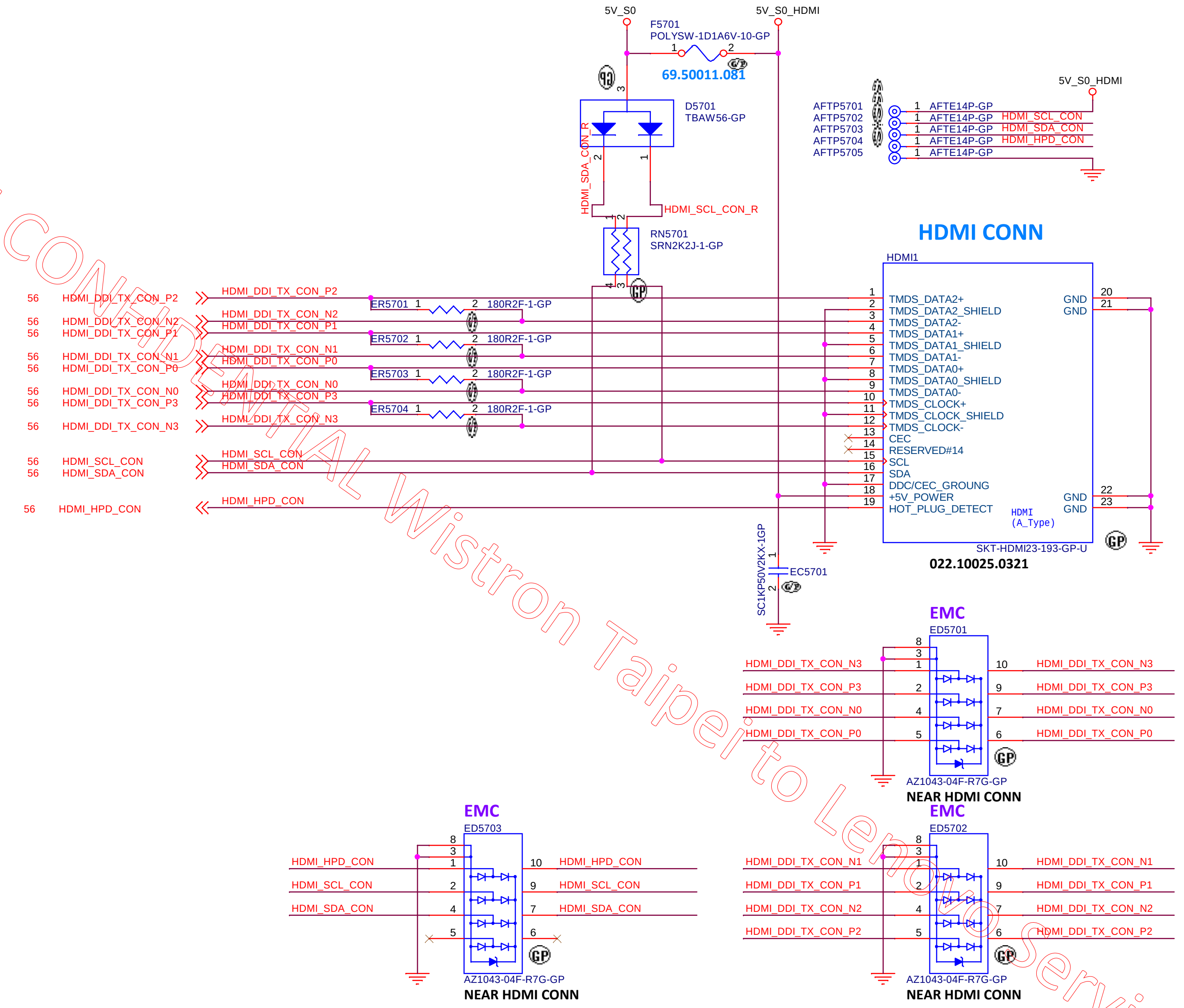
LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title DDI DEMULTIPLEXER (PS8337B)

Size A2 | Document Number Bumblebee-2 | Rev 1

Date: Tuesday, March 03, 2020



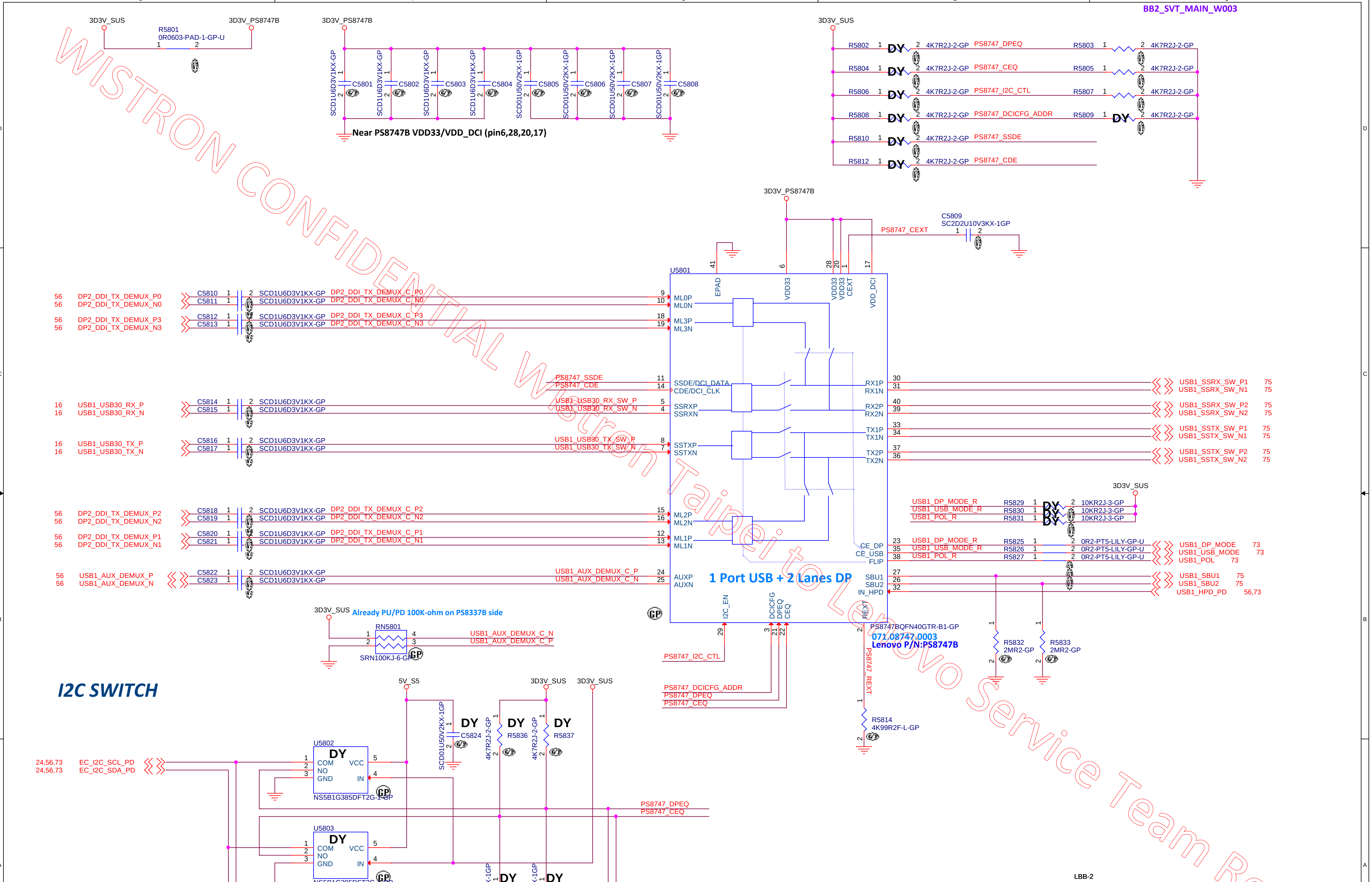
LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **DISPLAY (HDMI CONN)**

Size	Document Number		Rev
A3		Bumblebee-2	1

Date: Tuesday, March 03, 2020 — Sheet 57 of 106



LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	DISPLAY (DPUSB3 SW PS8747B))	
Size: Custom	Document Number: Bumblebee-2	Rev: 1
Date: Tuesday, March 03, 2020	Sheet 58 of 106	

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***INT IO (RSVD)***
Size A4	Document Number **Bumblebee-2** Rev **1**
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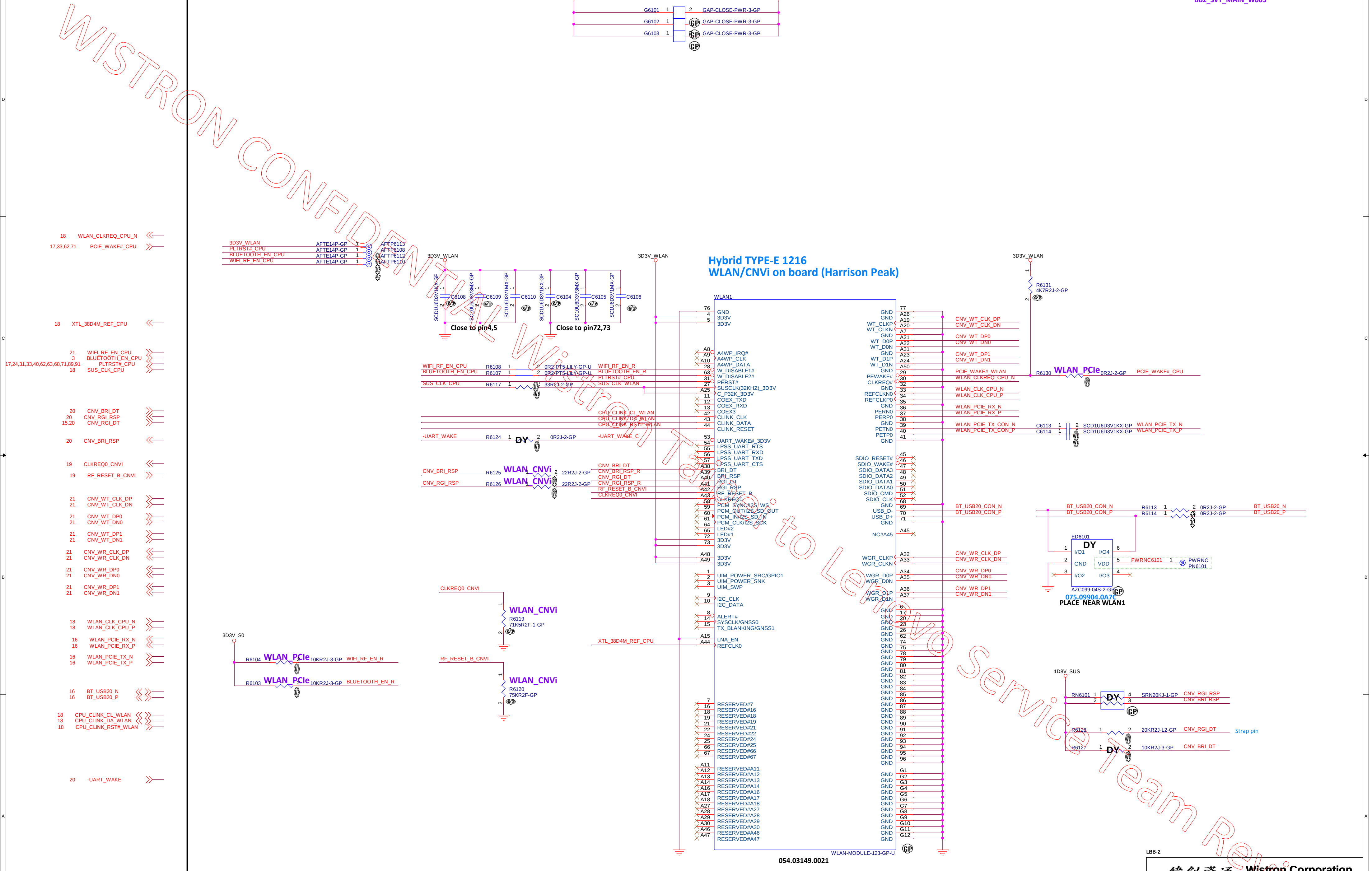
Main Func = WLAN

BB2_EVT_MAIN_W003
BB2_EVT_MAIN_W003
BB2_FVT_MAIN_W007
BB2_SVT_MAIN_W003



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	INT IO (WLAN /CNVi)		
Size A2	Document Number	Bumblebee-2	Rev 1
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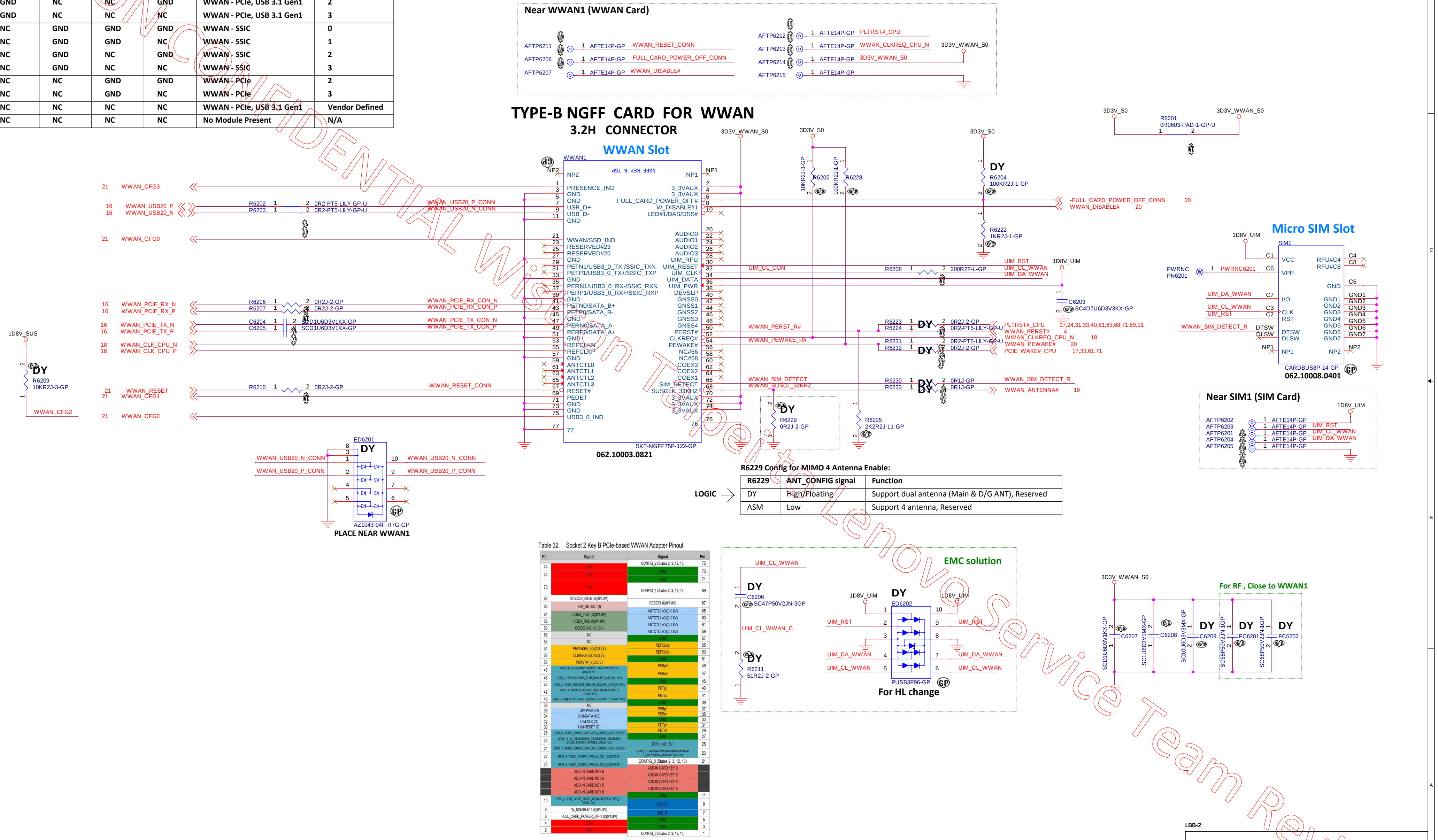
BB2_EVT_MAIN_W003
BB2_FVT_MAIN_W007
BB2_FVT_MAIN_W008
BB2_FVT_MAIN_W012
BB2_SVT_MAIN_W003

TABLE:

State #	Module Configuration Decodes: CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)	Module Type & Main Host Interface	Port Configuration
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined
15	NC	NC	NC	NC	No Module Present	N/A

TABLE:

Module	Module Configuration Decodes: CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)
Fibocom L850-GL	GND	NC	GND	GND
Fibocom L860-GL	NC	NC	NC	GND



R6229 Config for MIMO 4 Antenna Enable:

LOGIC

R6229	ANT_CONFIG signal	Function
DY	High/Floating	Support dual antenna (Main & D/G ANT), Reserved
ASM	Low	Support 4 antenna, Reserved

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **M.2 SOCKET 2 MODULE I/F**

Size A2 | Document Number **Bumblebee-2** | Rev 1

Date: Tuesday, March 03, 2020 | Sheet 62 of 106

TYPE-M M.2 CARD FOR SSD

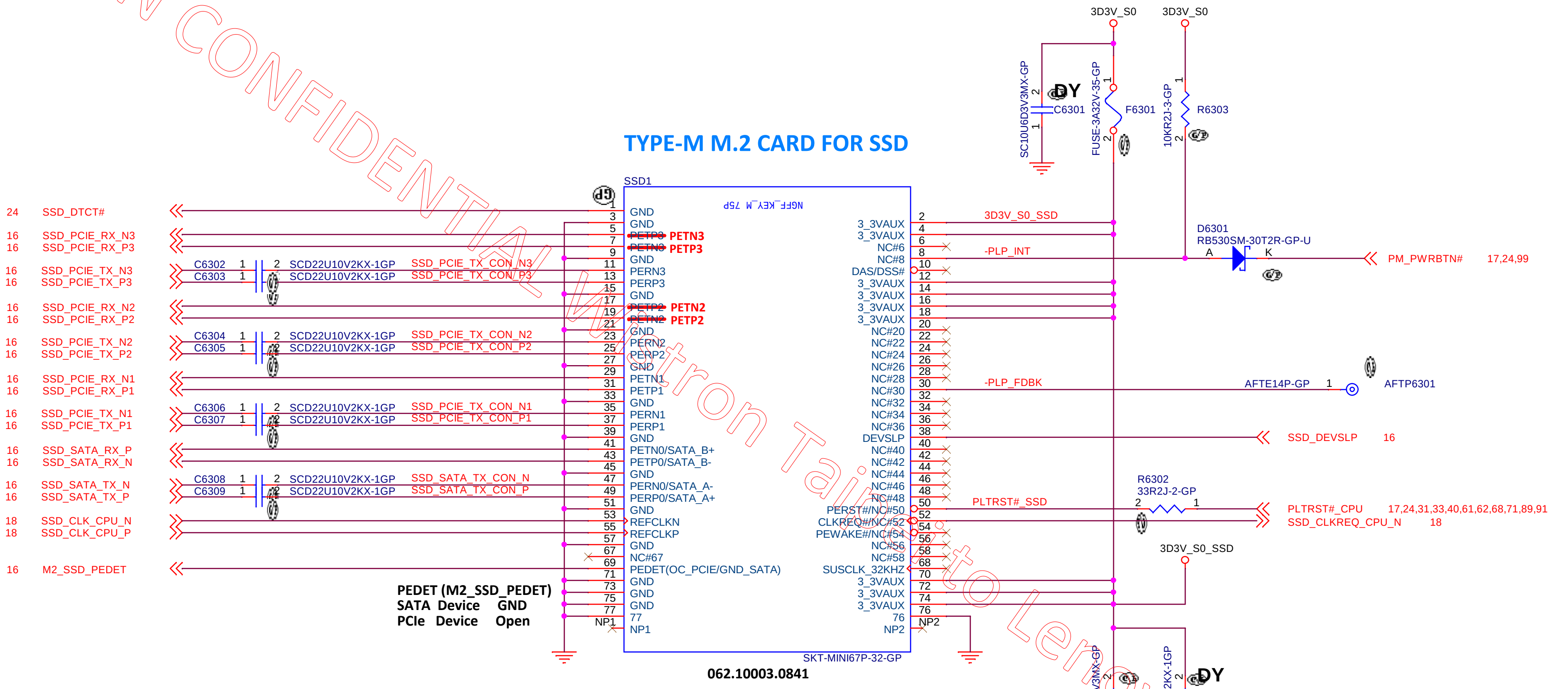
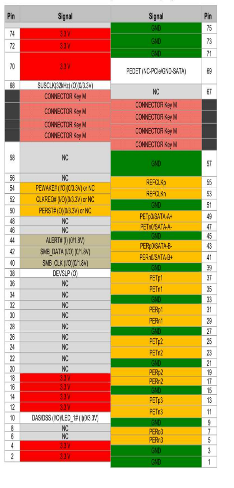


Table 54. Socket 3 SSD Pinout (Mechanical Key M) On Platform



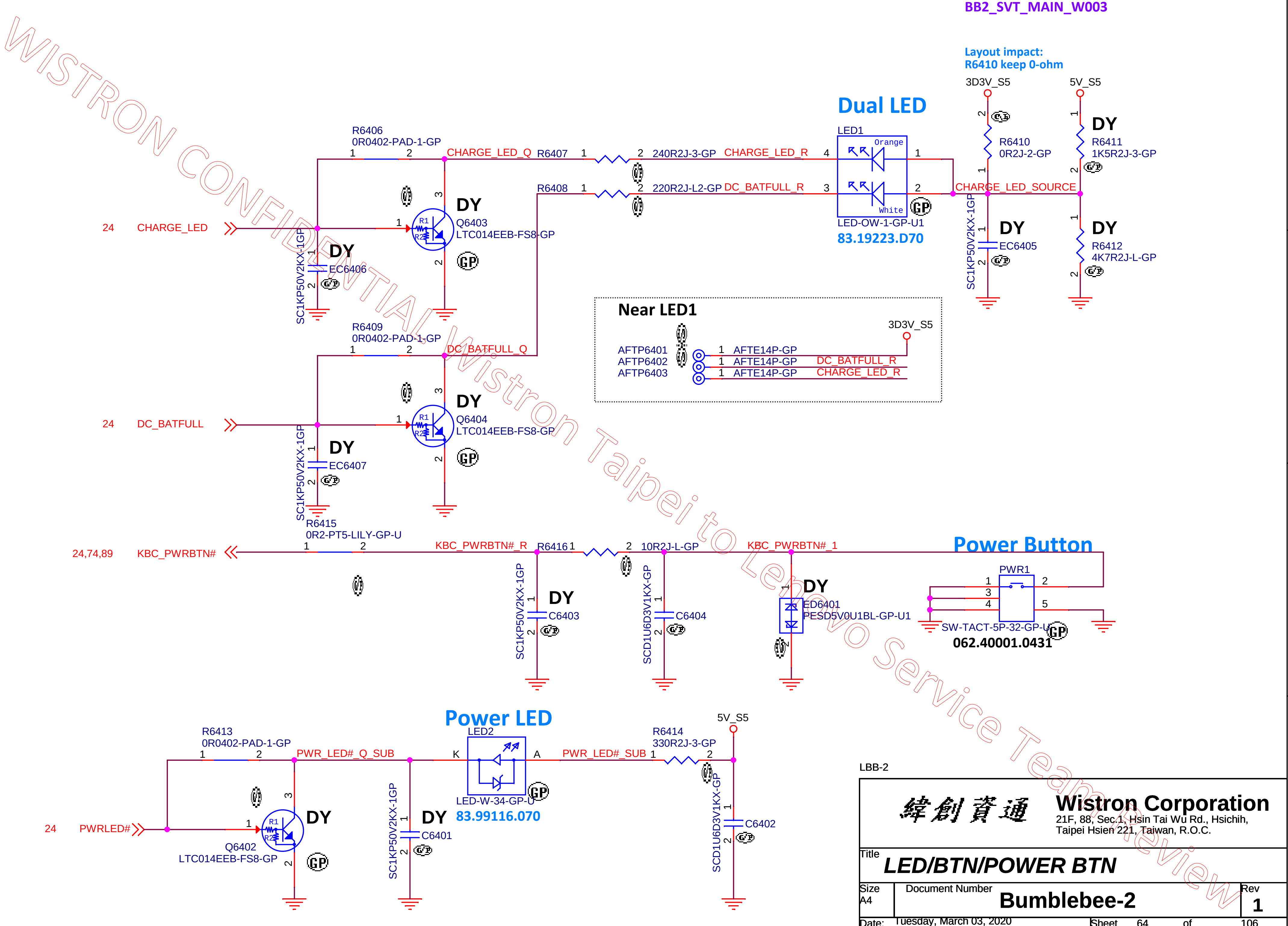
LBB-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD M.2)

Size: A3 | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020 | Sheet 63 of 106



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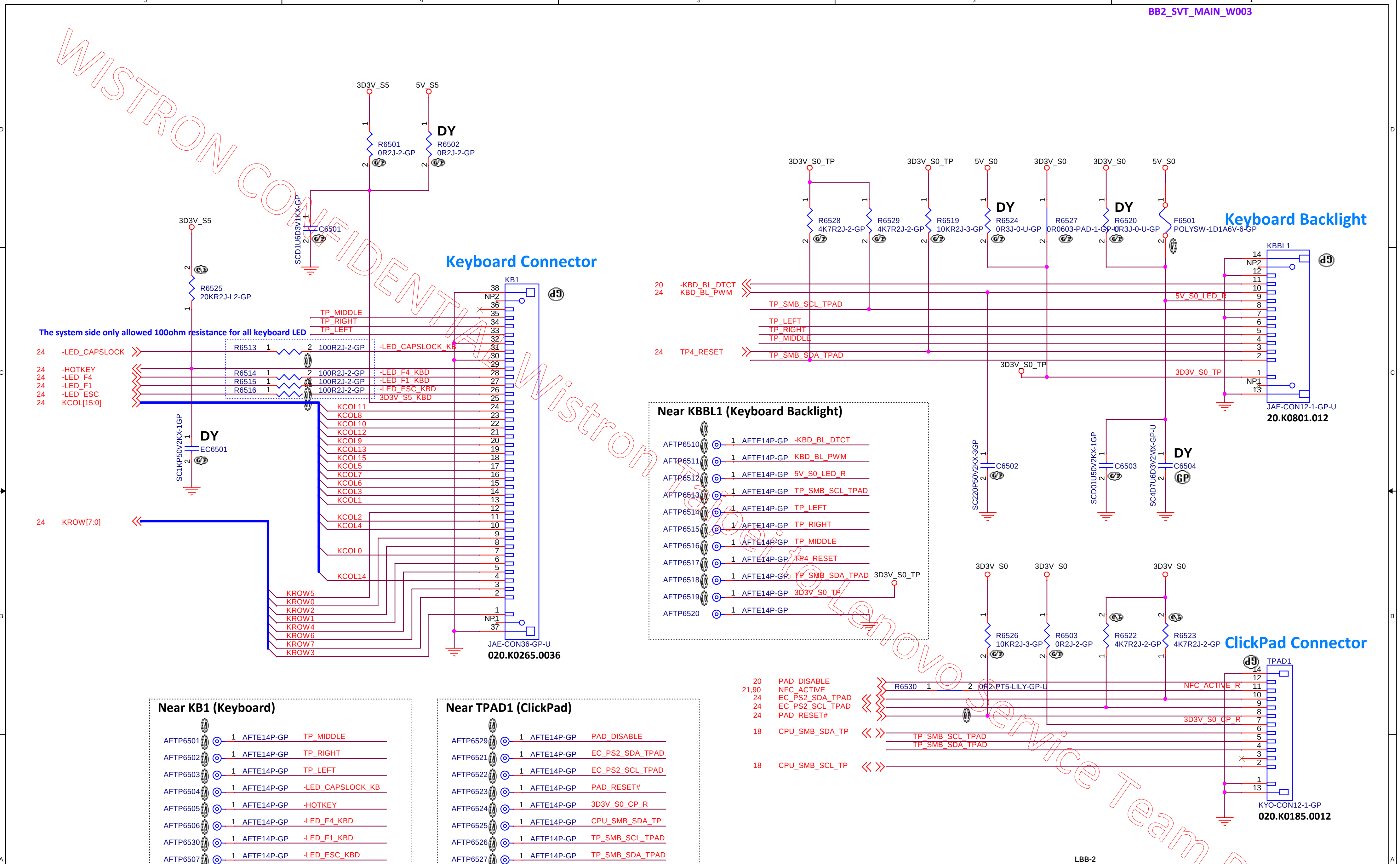
緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LED/BTN/POWER BTN**

Size: A4 | Document Number: **Bumblebee-2** | Rev: 1

Date: Tuesday, March 03, 2020 | Sheet 64 of 106



LBB-2

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	INT IO (KB/CP/TP)
Size A3	Document Number: Bumblebee-2
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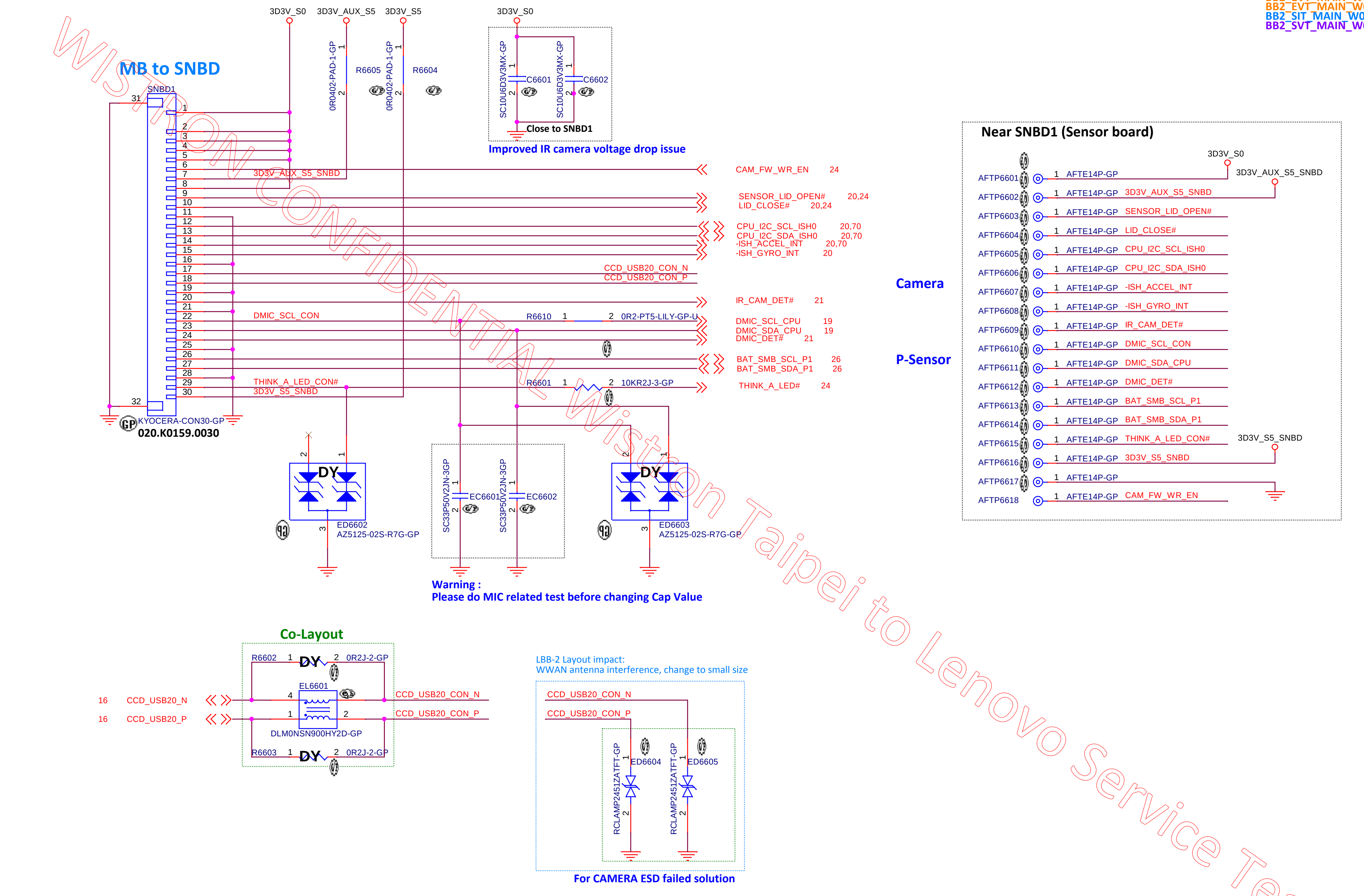
BB2_EVT_MAIN_W002
BB2_EVT_MAIN_W017
BB2_SIT_MAIN_W006
BB2_SVT_MAIN_W003



LBB-2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	IO BOARD CONN
Size A3	Document Number: Bumblebee-2 — Rev 1
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **SENSOR (RSVD)**

Size	Document Number	Rev
A4	**Bumblebee-2**	**1**

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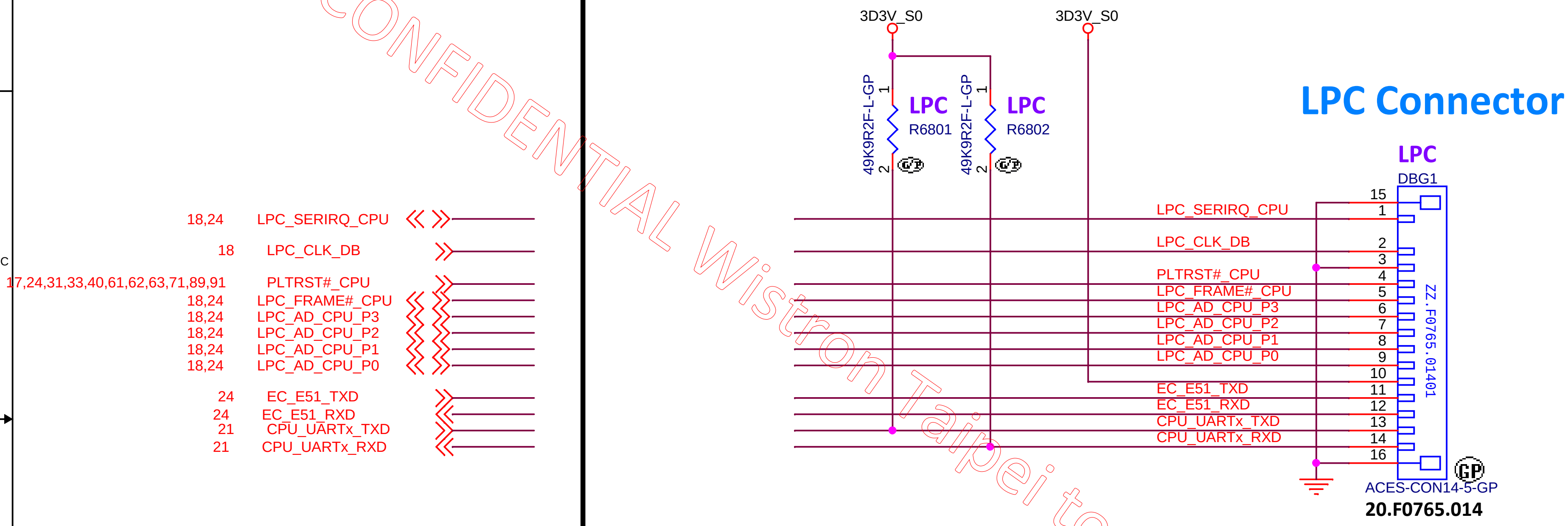
Main Func = Debug



LBB-2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**DEBUG (LPC DEBUG)**
Size A4	Document Number **Bumblebee-2** Rev **1**
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***SENSOR (RSVD)***	
Size A4	Document Number **Bumblebee-2**	Rev **1**
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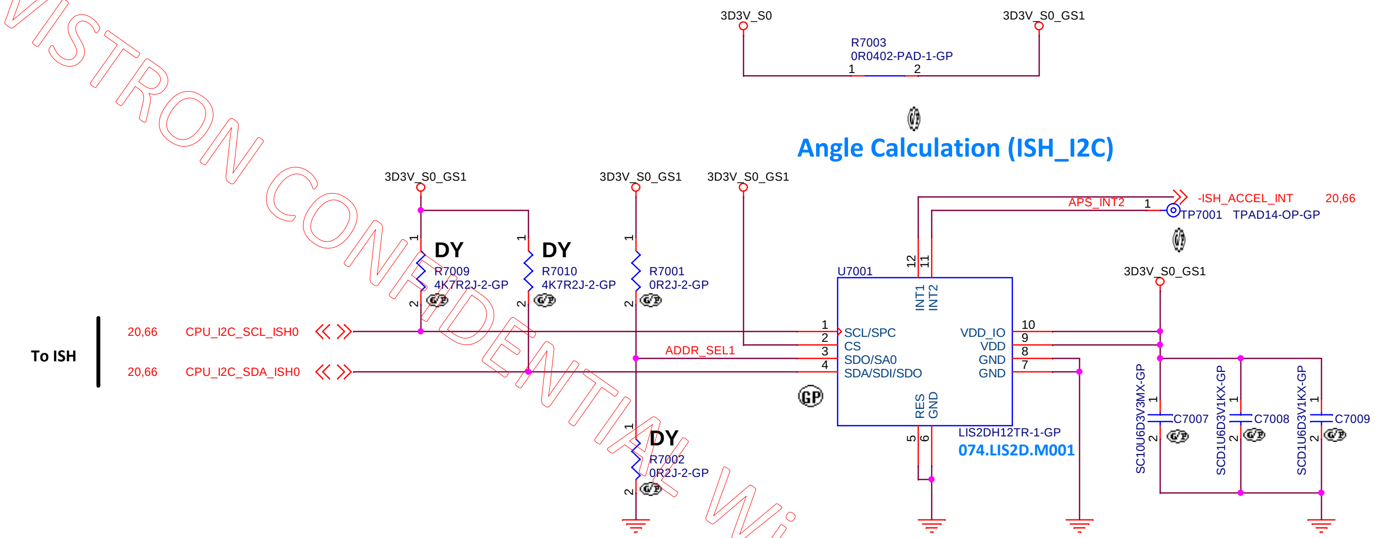
Angle Calculation (ISH_I2C)



TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

TABLE for Angle Detection (U7001): Tri-axis Digital Accelerometer

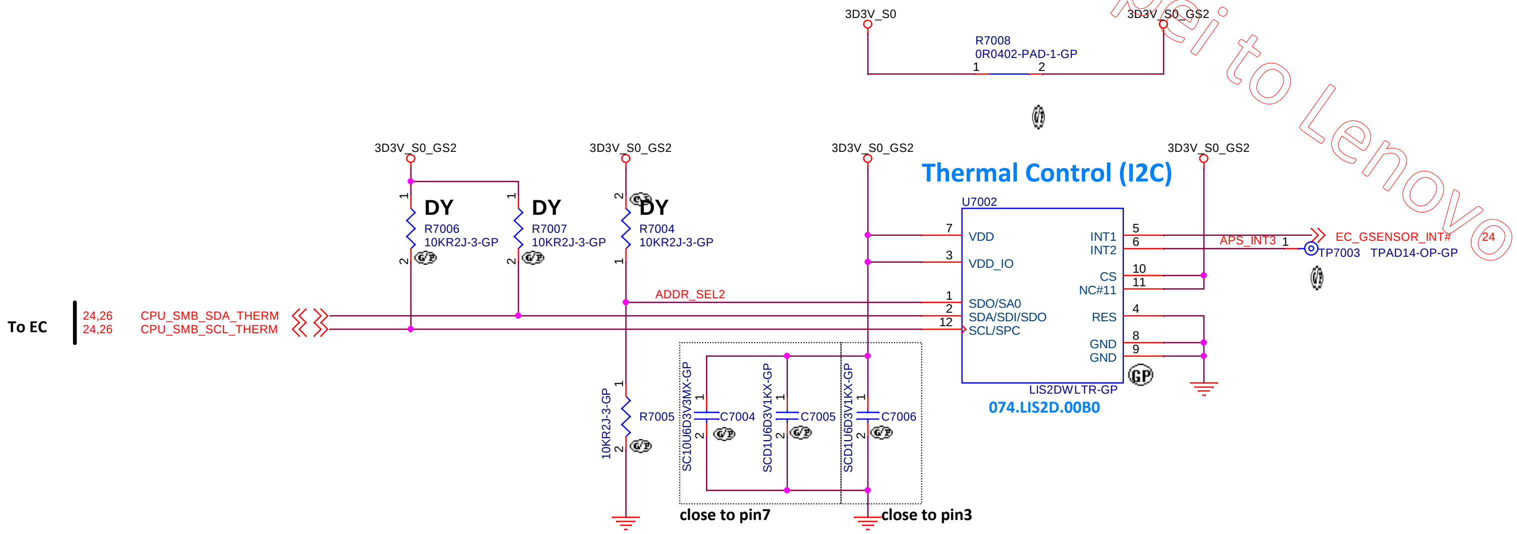
P/N	ADDR_SEL1	Address
LIS2DH12TR	H L	32h(W) & 33h(R) 30h(W) & 31h(R)

← Logic

TABLE of G-Sensor (U7001)

Vendor	P/N	Wistron P/N
ST	LIS2DH12TR	074.LIS2D.M001

Thermal Control (I2C)



TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

TABLE for Angle Detection (U7002): Tri-axis Digital Accelerometer

P/N	ADDR_SEL2	Address
BMA280	H L	32h(W) & 33h(R) 30h(W) & 31h(R)
LIS2DWLTR	H L	32h(W) & 33h(R) 30h(W) & 31h(R)

← Logic

TABLE of G-Sensor(U7002)

Vendor	P/N	Wistron P/N
BOSCH	BMA280	074.00280.0AB0
ST	LIS2DWLTR	074.LIS2D.00B0

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Title		
SENSOR (G-SENSOR)		
Size A3	Document Number **Bumblebee-2**	Rev **1**
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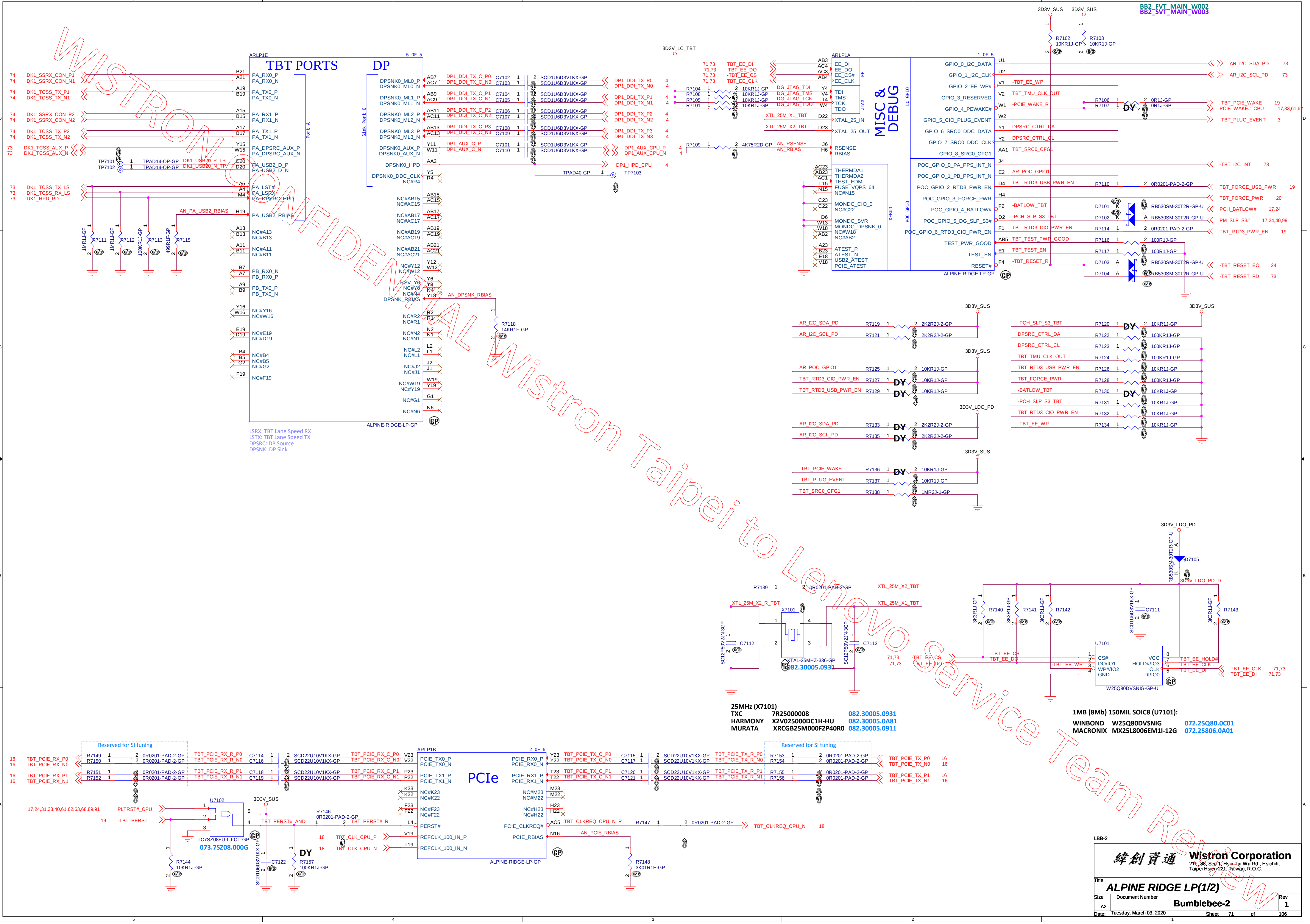


25MHz (X7101)

TXC	7R25000008	082.30005.0931
HARMONY	X2V025000DC1H-HU	082.30005.0A81
MURATA	XRCGB25M000F2P40R0	082.30005.0911

1MB (8Mb) 150MIL SOIC8 (U7101):

WINBOND	W25Q80DVSNIG	072.25Q80.0C01
MACRONIX	MX25L8006EM1I-12G	072.25806.0A01

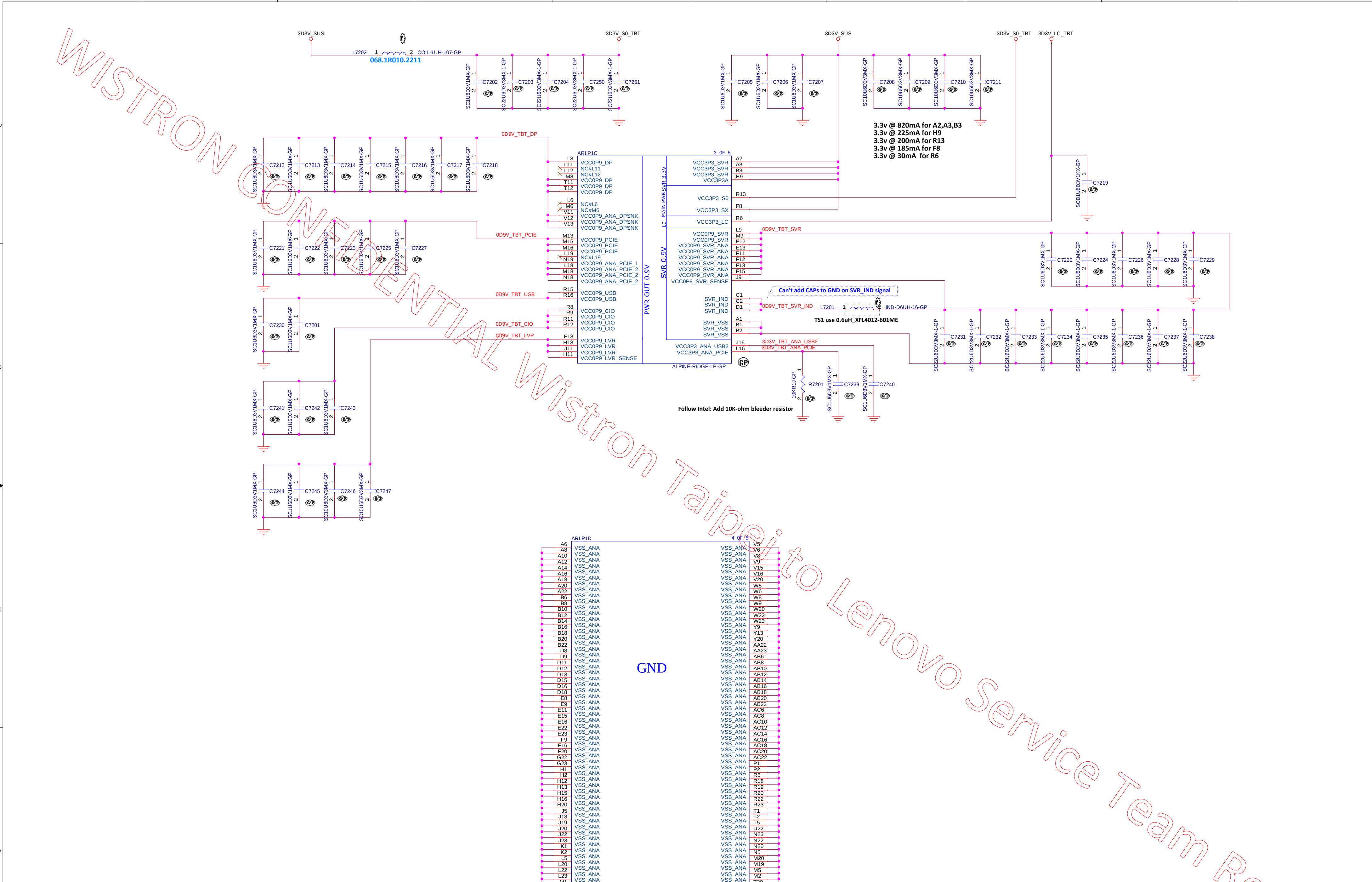
LBB-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ALPINE RIDGE LP(1/2)**

Size: A2 | Document Number: **Bumblebee-2** | Rev: 1

Date: Tuesday, March 03, 2020 | Sheet 71 of 106



LBB-2

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	ALPINE RIDGE LP(2/2)	
Size A2	Document Number Bumblebee-2	Rev 1
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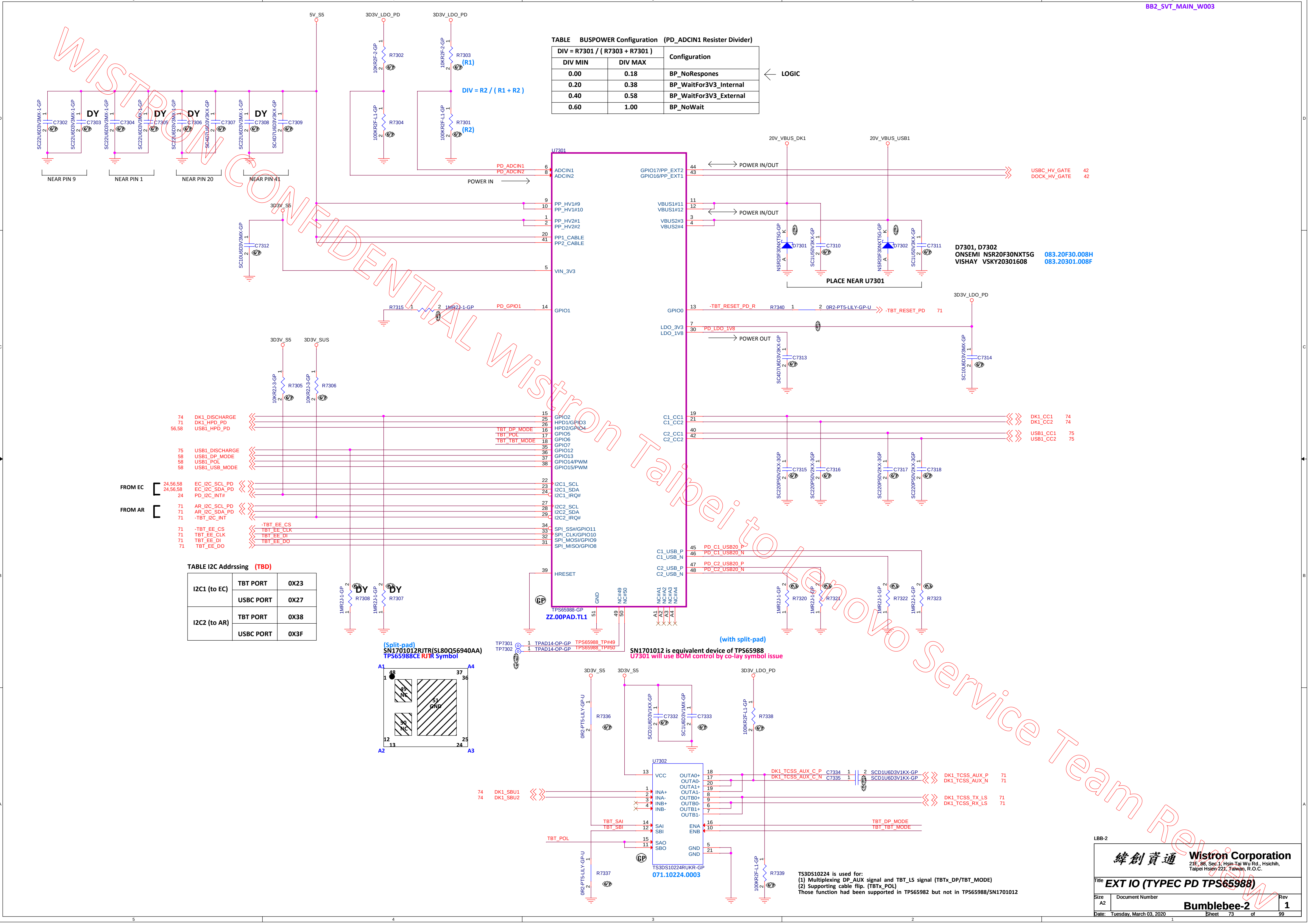


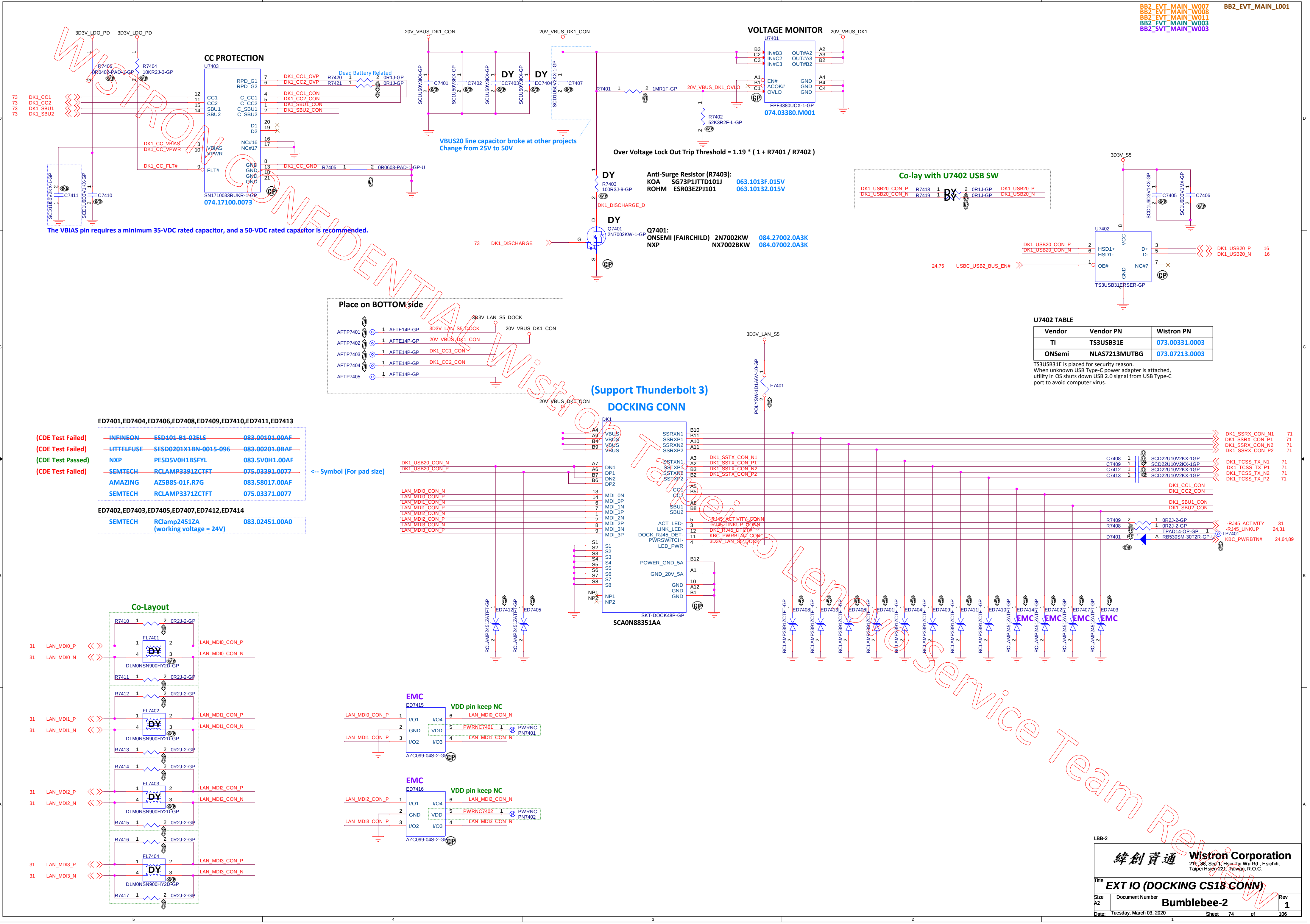
TABLE BUSPOWER Configuration (PD_ADCIN1 Resister Divider)

DIV = R7301 / (R7303 + R7301)		Configuration
DIV MIN	DIV MAX	
0.00	0.18	BP_NoRespones
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

TABLE I2C Addrssing (TBD)

I2C1 (to EC)	TBT PORT	0X23
	USBC PORT	0X27
I2C2 (to AR)	TBT PORT	0X38
	USBC PORT	0X3F

TS3DS10224 is used for:
(1) Multiplexing DP_AUX signal and TBT_LS signal (TBTx_DP/TBT_MODE)
(2) Supporting cable flip. (TBTx_POL)
Those function had been supported in TPS65982 but not in TPS65988/SN1701012



ED7401,ED7404,ED7406,ED7408,ED7409,ED7410,ED7411,ED7413

(CDE Test Failed)	~~INFINEON~~	~~ESD101-B1-02ELS~~	~~083.00101.00AF~~	
(CDE Test Failed)	~~LITTELFUSE~~	~~SESD0201X1BN-0015-096~~	~~083.00201.0BAF~~	
(CDE Test Passed)	NXP	PESD5V0H1BSFYL	083.5V0H1.00AF	
(CDE Test Failed)	~~SEMTECH~~	~~RCLAMP3391ZCTFT~~	~~075.03391.0077~~	<-- Symbol (for pad size)
	AMAZING	AZ5B8S-01F.R7G	083.58017.00AF	
	SEMTECH	RCLAMP3371ZCTFT	075.03371.0077	

ED7402,ED7403,ED7405,ED7407,ED7412,ED7414

SEMTECH	RClamp2451ZA (working voltage = 24V)	083.02451.00A0

U7402 TABLE

Vendor	Vendor PN	Wistron PN
TI	TS3USB31E	073.00331.0003
ONSemi	NLAS7213MUTBG	073.07213.0003

TS3USB31E is placed for security reason.
When unknown USB Type-C power adapter is attached, utility in OS shuts down USB 2.0 signal from USB Type-C port to avoid computer virus.

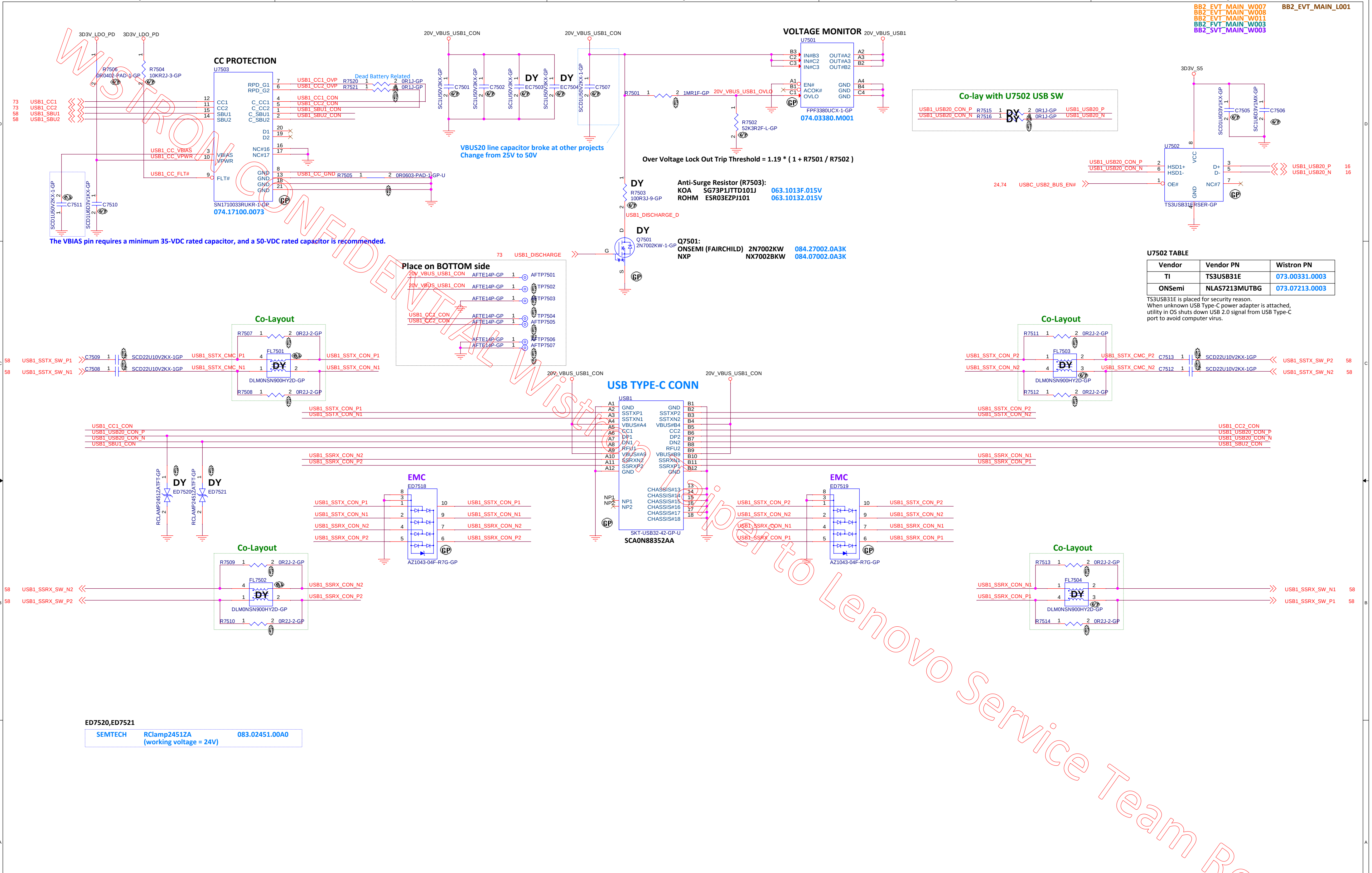
LBB-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (DOCKING CS18 CONN)

Size: A2 | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020 | Sheet 74 of 106



U7502 TABLE

Vendor	Vendor PN	Wistron PN
TI	TS3USB31E	073.00331.0003
ONSemi	NLAS7213MUTBG	073.07213.0003

TS3USB31E is placed for security reason.
When unknown USB Type-C power adapter is attached, utility in OS shuts down USB 2.0 signal from USB Type-C port to avoid computer virus.

ED7520,ED7521

SEMTECH	RClamp2451ZA (working voltage = 24V)	083.02451.00A0

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (TYPEC CONN)

Size	Document Number	Rev
A2	Bumblebee-2	1

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緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)		
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU (RSVD)	
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU (RSVD)***		
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: GPU (RSVD)		
Size: A4	Document Number: Bumblebee-2	Rev: 1
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*GPU (RSVD)*	
Size A4	Document Number **Bumblebee-2**	Rev **1**
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size: A4 | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)		
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU (RSVD)***	
Size A4	Document Number **Bumblebee-2**	Rev **1**
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU (RSVD)***	
Size A4	Document Number **Bumblebee-2**	Rev **1**
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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	GPU (RSVD)		
Size A4	Document Number Bumblebee-2		Rev 1
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緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*GPU (RSVD)*	
Size A4	Document Number **Bumblebee-2**	Rev **1**
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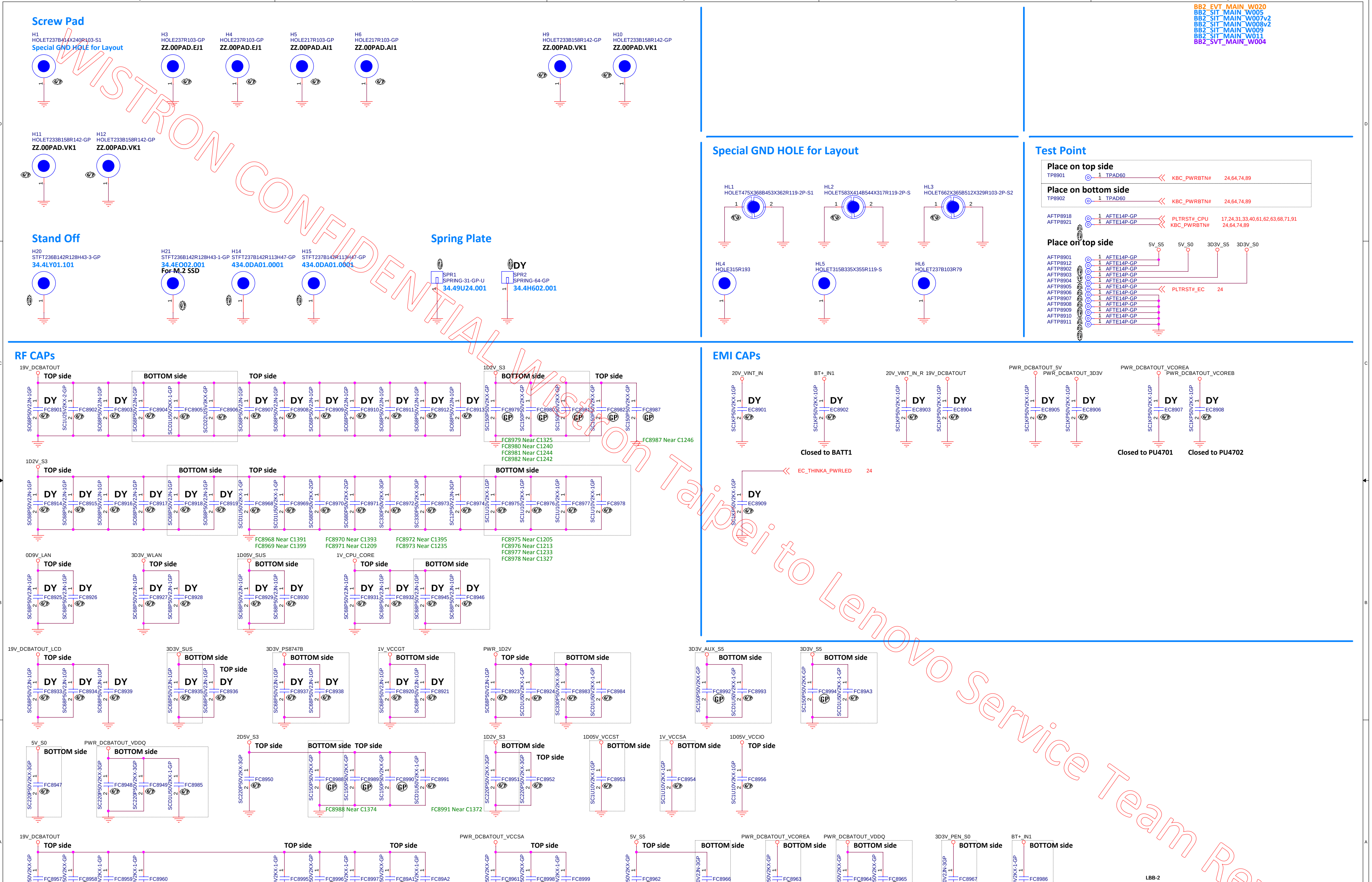

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

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Title	UNUSED PARTS (ME/RF/EMI)		
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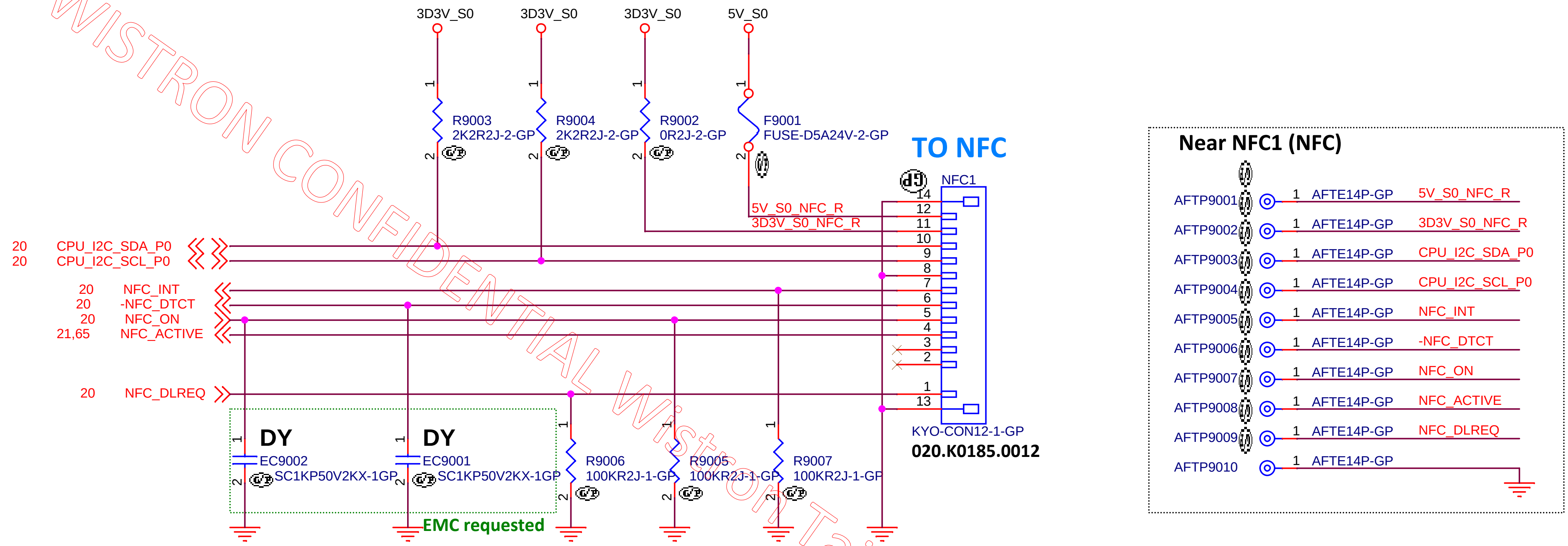
BB2_SVT_MAIN_W003



Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C_SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

Remark: P = power supply, G = ground, I = input, O = output, I/O = input/output

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (NFC)

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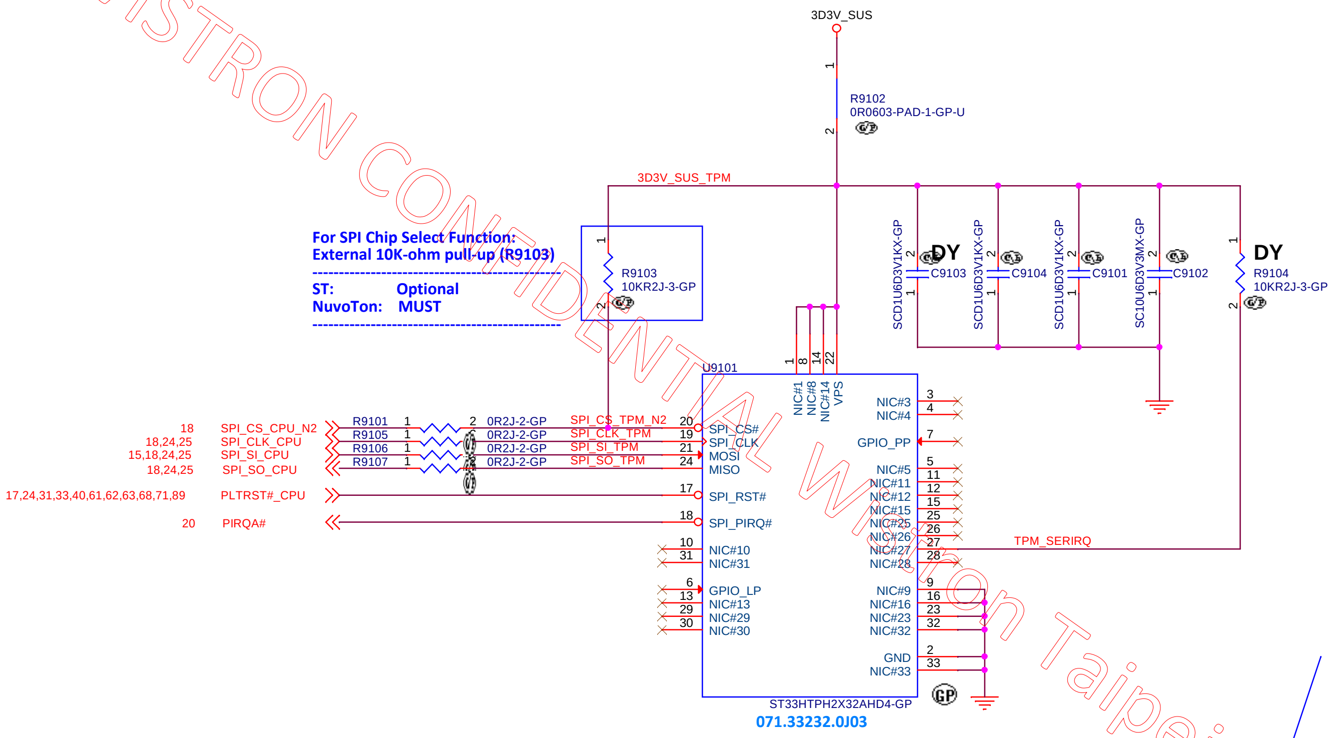

SPI Chip Select Pin:
ST (SPI_CS#) Internal pull-up
NuvoTon (SCS#) Internal pull-up is disabled if the pin is part of the recognized host interface

TABLE

	TPM2.0	EVT		FVT		SIT and beyond	
1st	ST	ST33HTPH2E32AHC0	071.33232.0H03	ST33HTPH2X32AHC4	071.33232.0I03	ST33HTPH2X32AHD4	071.33232.0J03
2nd	NuvoTon	NPCT750LABYX	071.00750.0D03	NPCT750LABYX	071.00750.0D03	NPCT750LABYX	071.00750.0D03

TABLE

Pin No	TCG PTP Spec(V38)	NuvoTon NPCT750LABYX (071.00750.0D03)	ST Micro ST33HTPH2X32AHD4 (071.33232.0J03)	Infineon SLB9670VQ2.0 FW7.63 (~~071.09670.0I03~~)
1	VDD	VSB	NC	VDD
2	GND	NC	GND	GND
3	NC	NC	NC	NC
4	GPIO	GPIO/PP	PP	NC
5	NC	NC	NC	NC
6	GPIO	GPIO3	NC	GPIO
7	GPIO	NC	GPIO	PP
8	VDD	VHIO	NC	VDD
9	NC	NC	NC	GND
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	GPIO4	NC	NC
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	GND	NC	NC
17	SPI_RST#	RST#	SPI_RST#	RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#	PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#	CS#
21	MOSI	MOSI/GPIO7	MOSI	MOSI
22	VDD	VHIO	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO0	NC	NC
30	SCL/GPIO0	SCL/GPIO1	NC	NC
31	NC	NC	NC	NC
32	NC	NC	NC	GND

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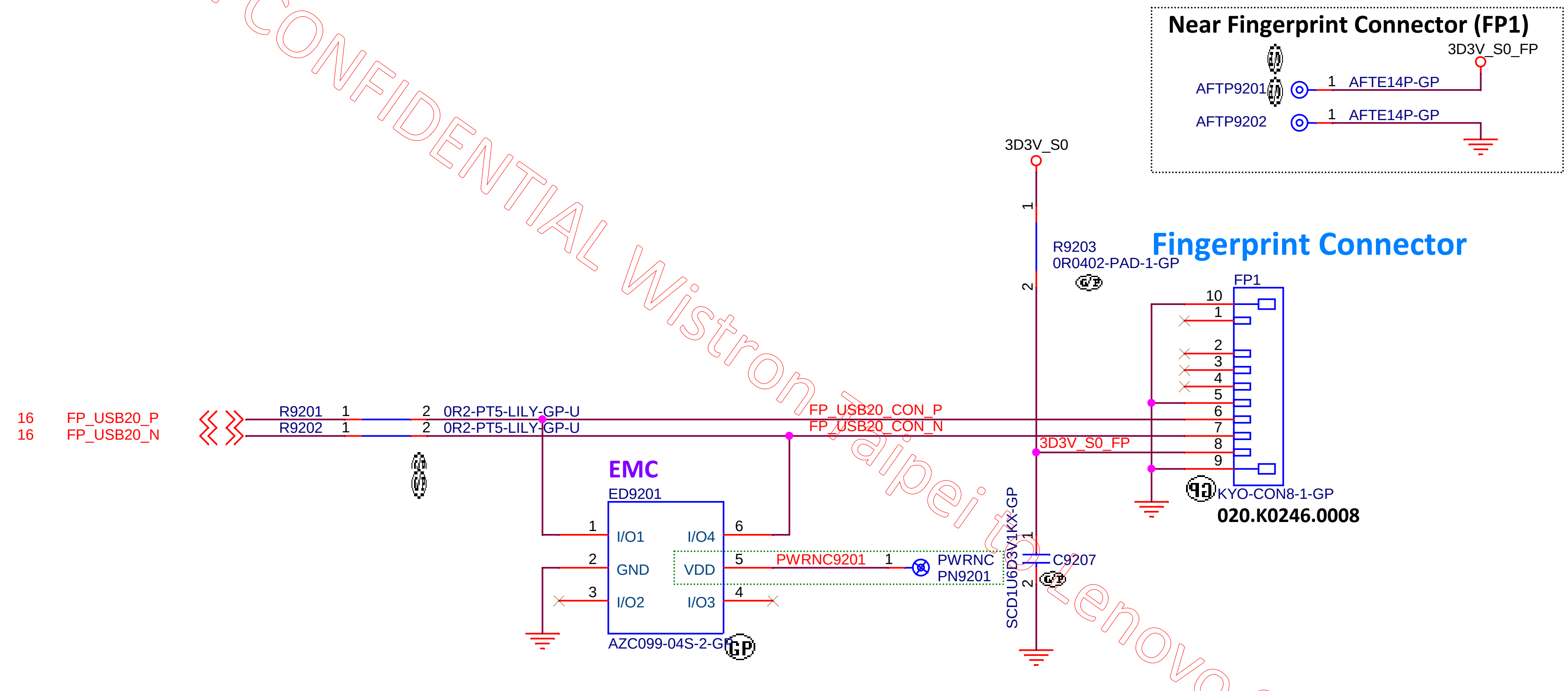
BB2_EVT_MAIN_W003
BB2_FVT_MAIN_W007
BB2_SVT_MAIN_W003



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緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	INT IO (FINGERPRINT)	
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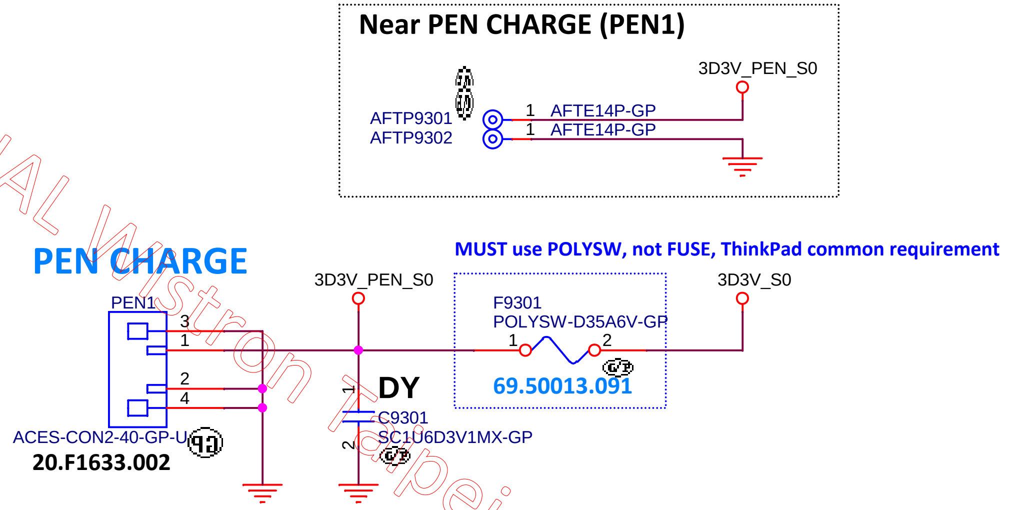

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	EXT IO (ACTIVE PEN)	
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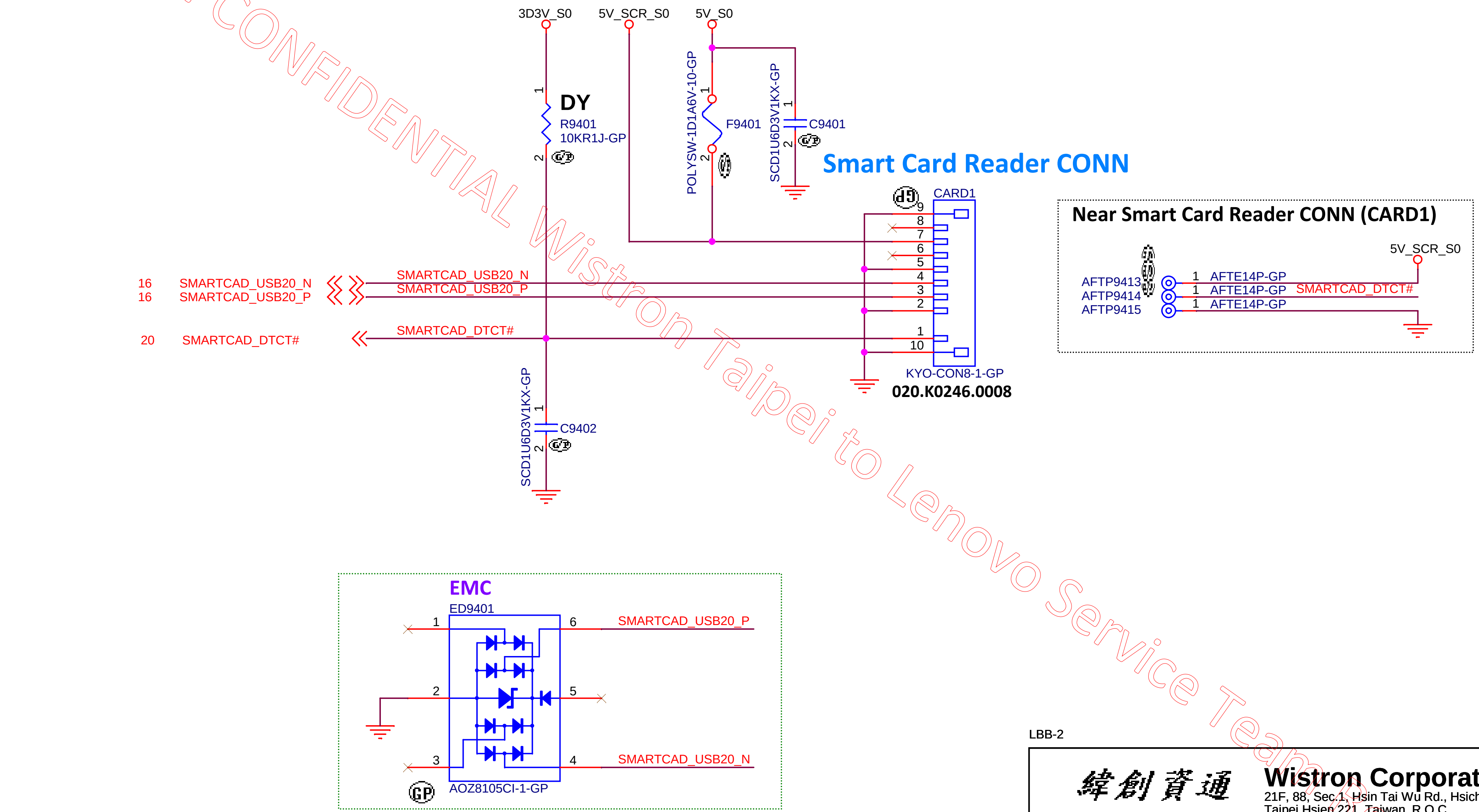

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Title: EXT IO (SMART CARD)		
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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***EXT IO (RSVD)***		
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Title	COMMERCIAL (RSVD)	
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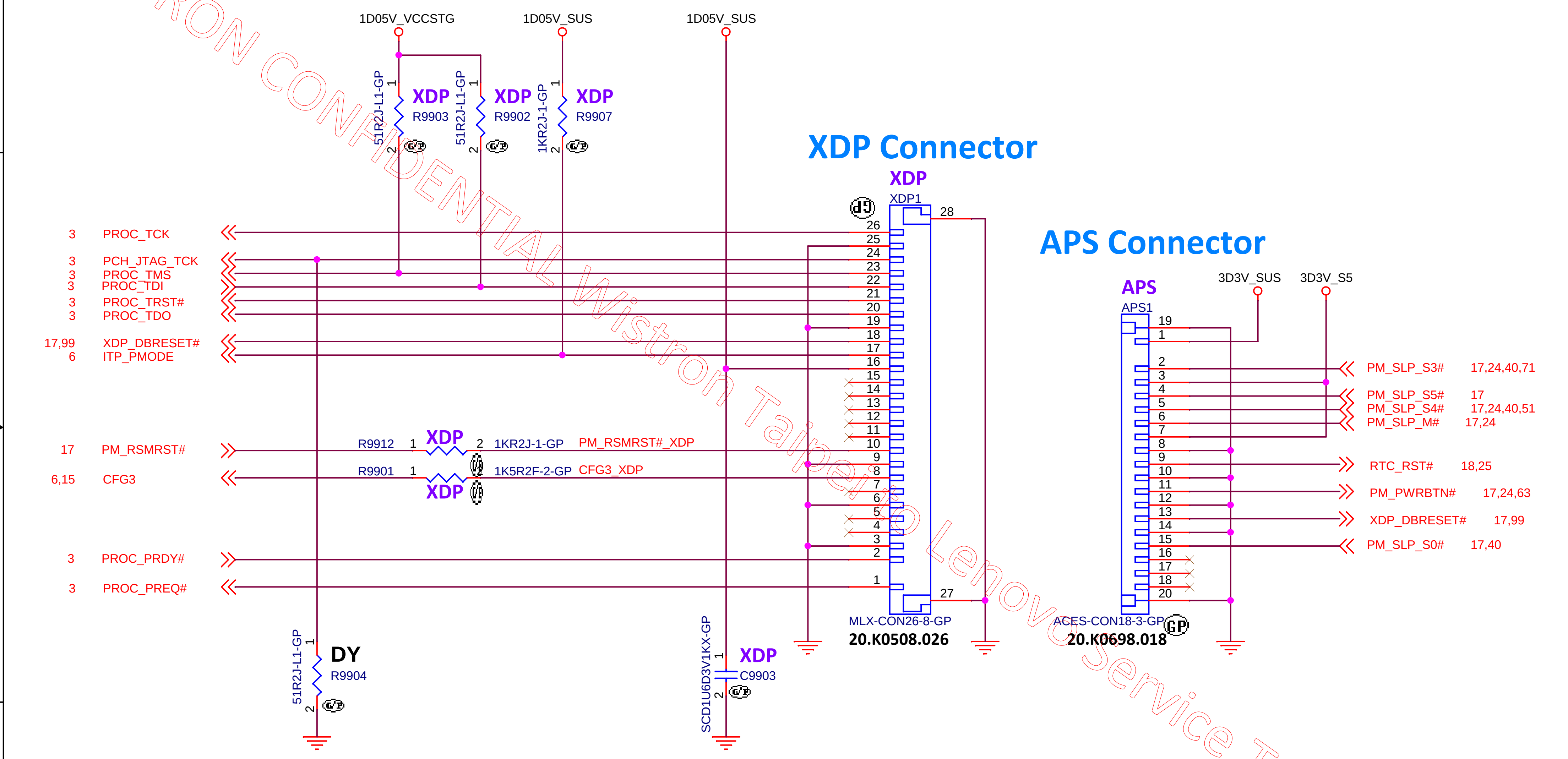
Main Func = Debug



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緯創資通 Wistron Corporation
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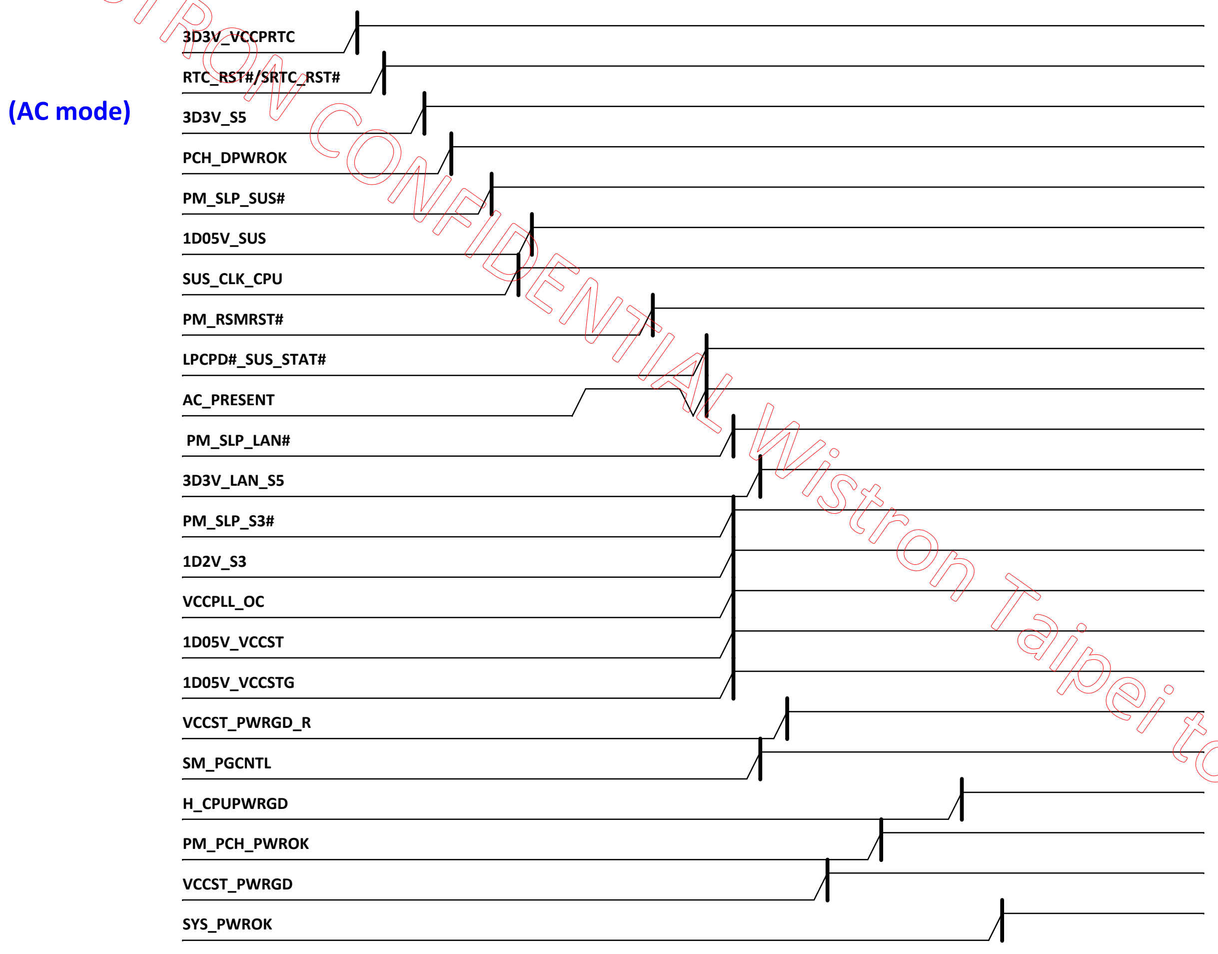
Intel-Power Up Sequence

#607109_CML_U_PDG_Rev1p2_P.629



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緯創資通 **Wistron Corporation**
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Title	POWER SEQUENCE	
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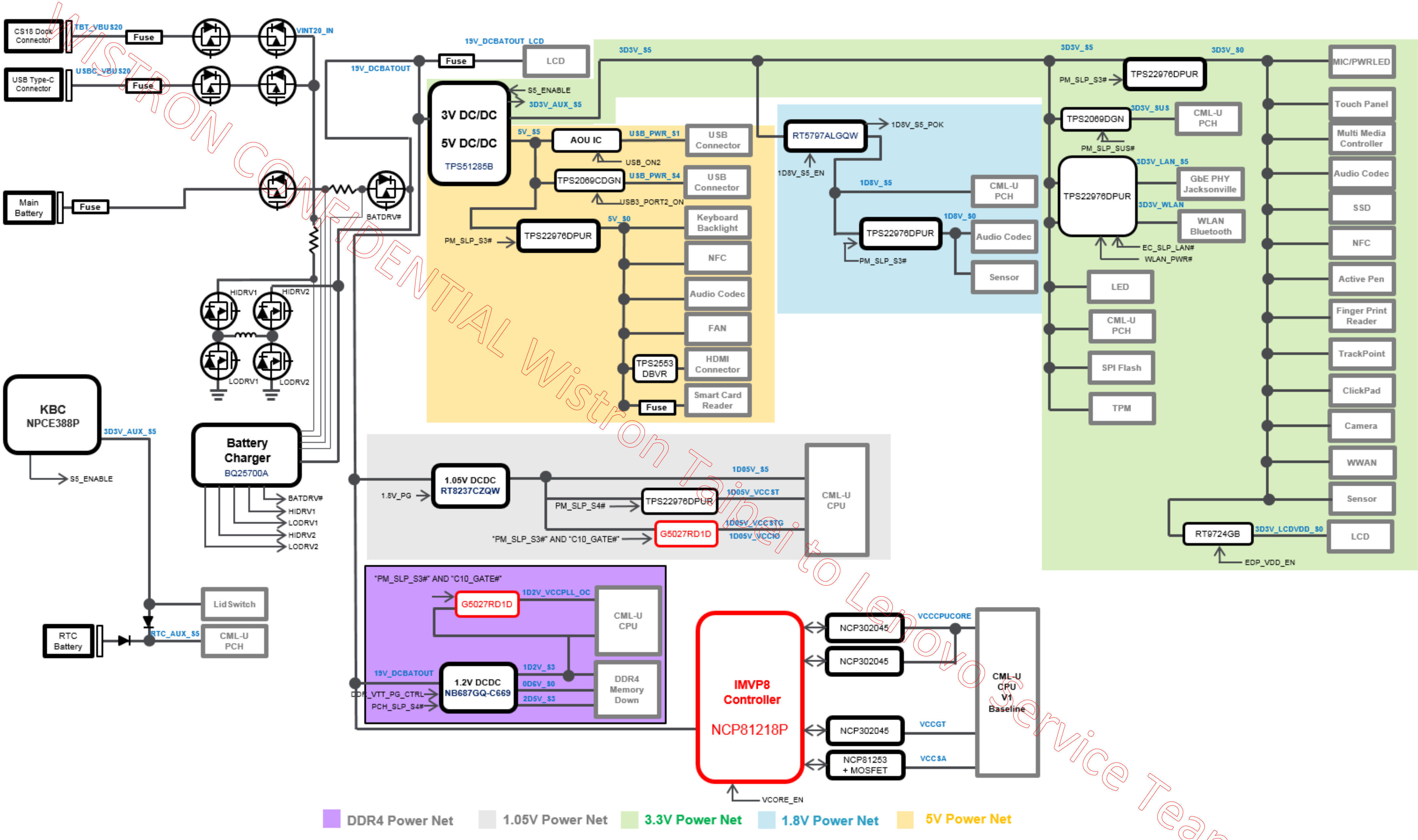

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Title	**POWER BLOCK DIAGRAM**
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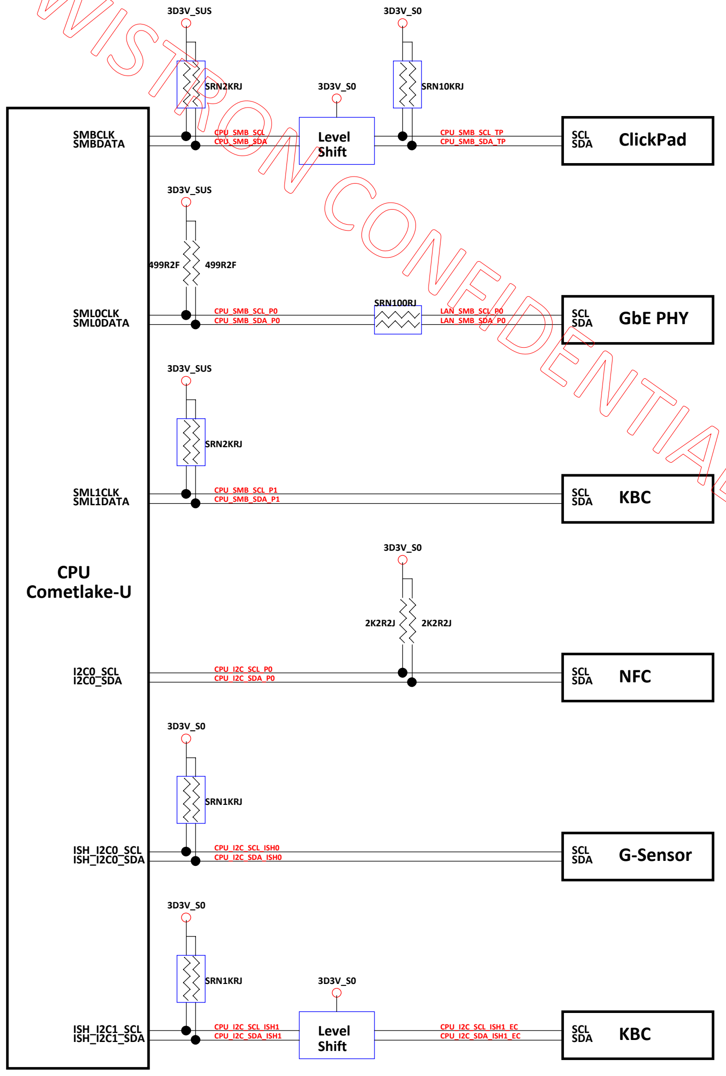
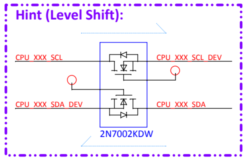
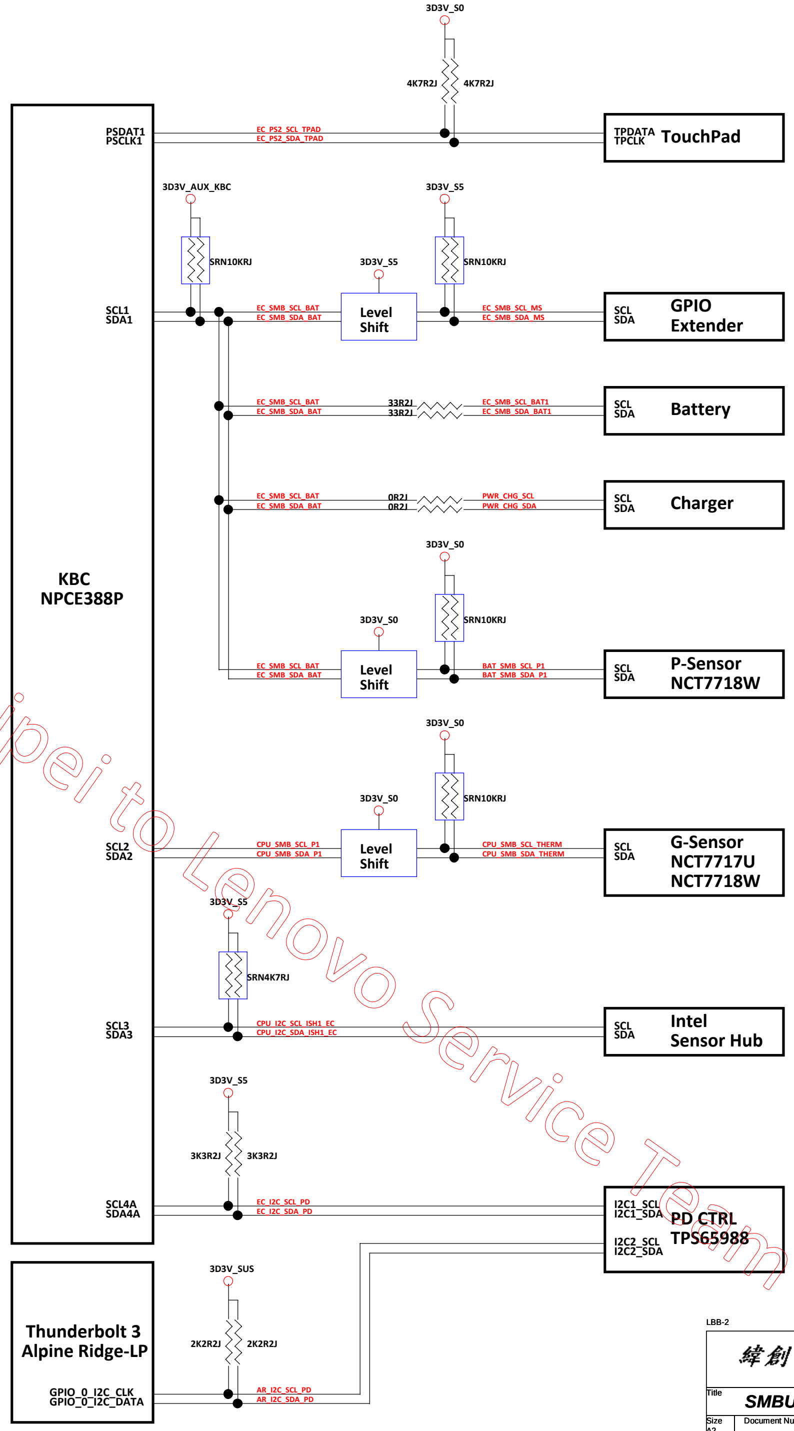
PCH SMBus/I2C Block Diagram





KBC SMBus/I2C Block Diagram



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Title	SMBUS/I2C BLOCK DIAGRAM		
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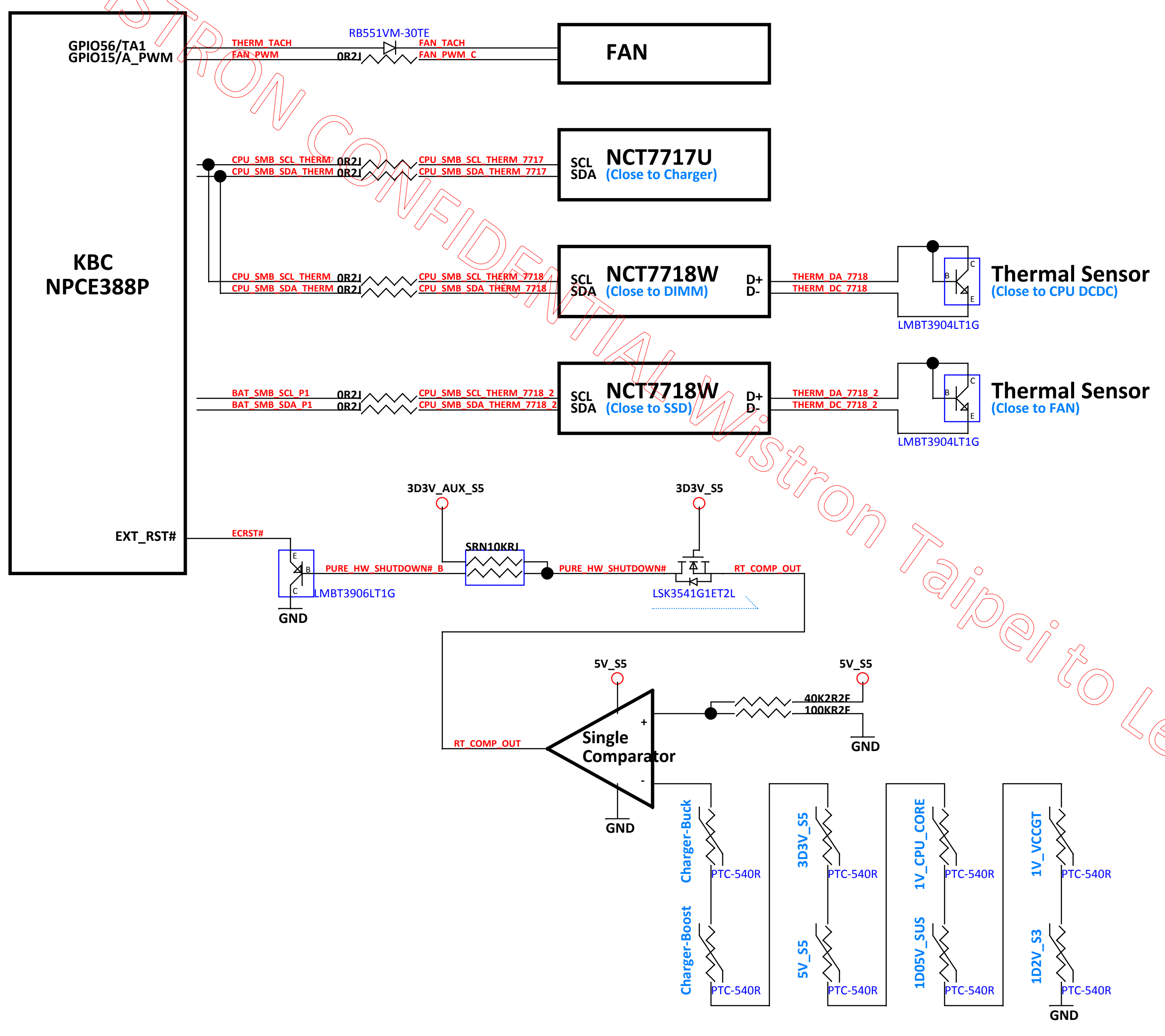
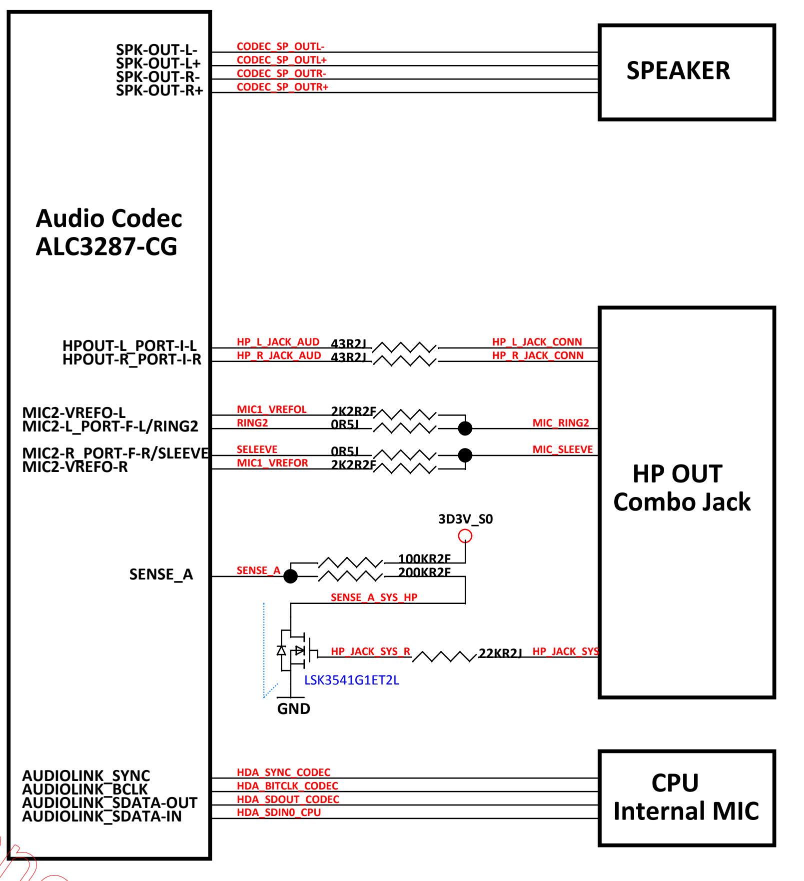
Thermal Block Diagram



Audio Block Diagram



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Title	THERMAL/AUDIO BLOCK DIAGRAM	
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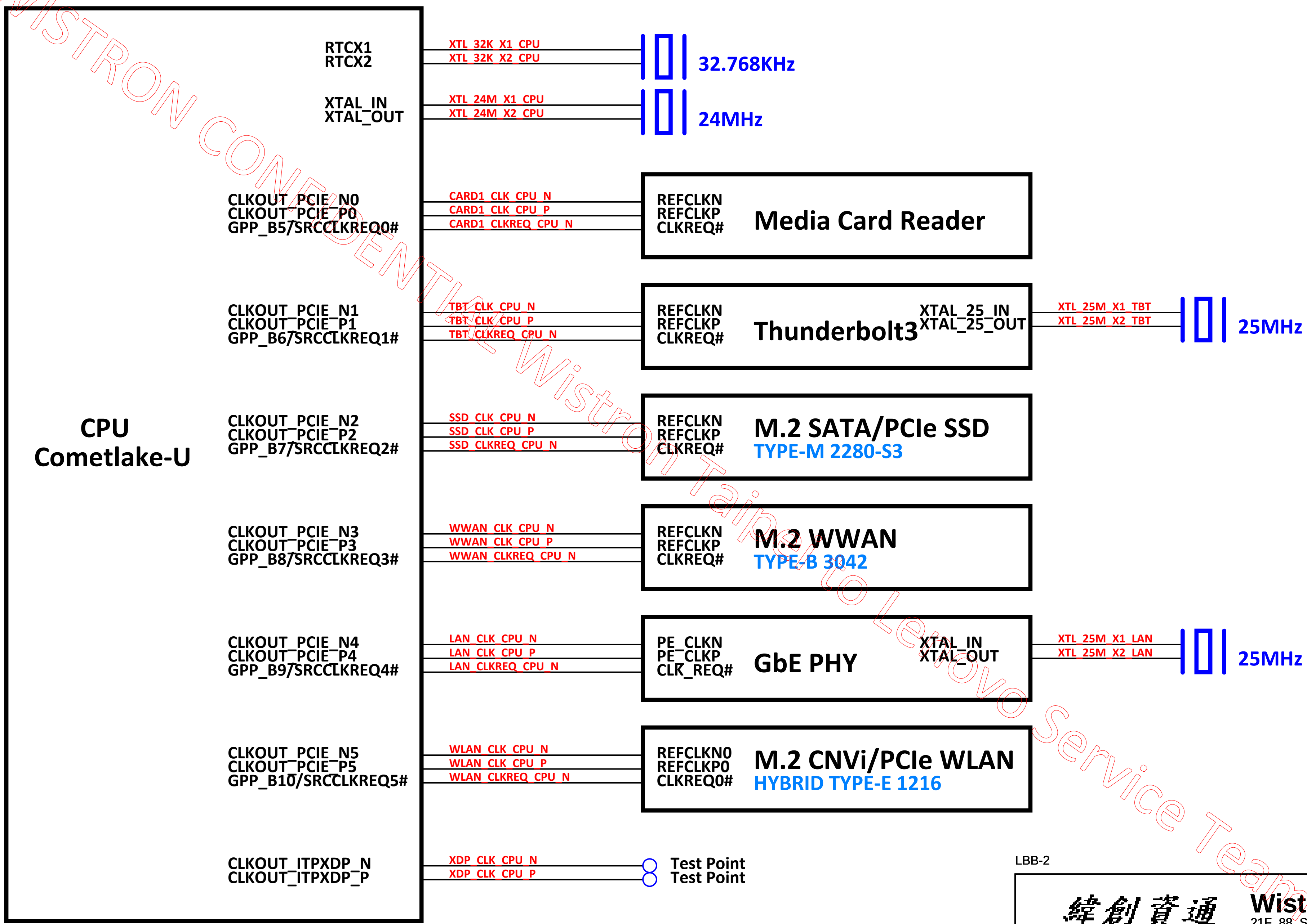

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Title

CLK BLOCK DIAGRAM

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