Bumblebee (LBB-2)
Cometlake-U Schematics

Project Code: 4PD0JH010001
PCB(Raw Card): 19733-1

2020-03-03

Properties of DUMMY: (BOM Control Parts)

Value	Description
(No Value)	ASM, assemble
DY	DUMMY, NOT ASM, not assemble
ZZ (No Need to Display)	ZZ parts for testpoint / shortpad / hole
PCBID	PCB ID for SW Team (PCB number)
SKUID	SKU ID for SW Team (CPU Type: non-vPro / vPro)
MEM_IDx_0 / MEM_IDx_1 (x = 0~4)	Memory ID for SW Team (0 = Low / 1 = High Level)
DDR4_CTRL	Memory Packaging Technology setting (SDP / DDP)
SDP / DDP	Number of identical die in package (1 = SDP, 2 = DDP)
APS / ISH / LPC / XDP	Debug Connectors (Assemble in 1st build only)
EMC	Follow EMC Team requested
NON_PSL / PSL	Support / Non Support KBC Power Switched Logic
WLAN_PCIe / WLAN_CNVi	Support WLAN type (PCIe or CNVi interface)
CHARGER_HS / CHARGER_LS	Charger High / Low Side MOSFET
VCCSA_HS / VCCSA_LS	VCCSA High / Low Side MOSFET

LBB-2

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Title: COVER PAGE

Size	Document Number	Rev
A4	Bumblebee-2	1

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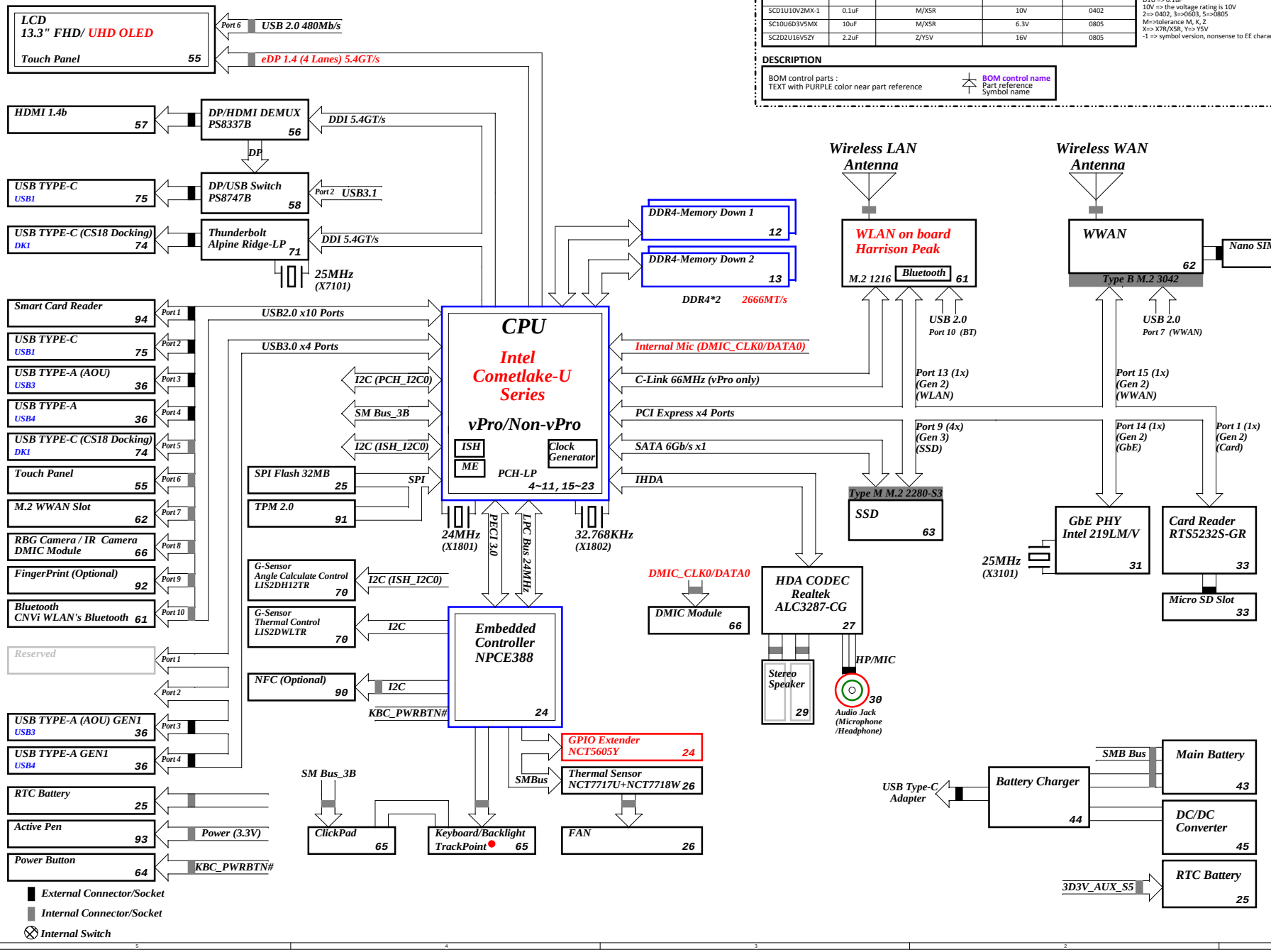
Bumblebee-2 Cometlake Block Diagram

Project Code: 4PD0JH010001
PCB(Raw Card): 19733-1



RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating	Size
10KR3	10K Ohm	If no letter, it means J: 5%	0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DESCRIPTION

BOM control parts :
TEXT with PURPLE color near part reference

BOM control name
Part reference
Symbol name

PCB Layer Stackup

L1:Component
L2:GND
L3:Signal 1
L4:VCC
L5:Signal 2
L6:Signal 3
L7:GND
L8:Signal 4
L9:GND
L10:Component

Battery Charger/Selector BQ25700ARSNR 44	
VINT20_IN	19V_DCBATOUT BT+
System DC/DC TPS51285B 45	
19V_DCBATOUT	5V_S5 3D3V_S5
DC/DC IMVP8 NCP81218PMNTXG 46	
DC/DC VCCCPUCORE NCP302045LMNTXG 47	
19V_DCBATOUT	1V_CPU_CORE
DC/DC VCCGT NCP302045LMNTXG 48	
19V_DCBATOUT	1V_VCCGT
DC/DC VCCSA NCP81253MNTBG 50	
19V_DCBATOUT	1V_VCCSA
DC/DC 1D2V_S3 NB687GQ-C669-Z 51	
19V_DCBATOUT	1D2V_S3
DC/DC 0D6V_VREF_S0 NB687GQ-C669-Z 51	
1D2V_S3	0D6V_VREF_S0
DC/DC 2D5V_S3 NB687GQ-C669-Z 51	
3D3V_S5	2D5V_S3
DC/DC 1D05V_SUS RT8237CZQW 52	
19V_DCBATOUT	1D05V_SUS
DC/DC 1D8V_SUS RT5797ALGQW 53	
3D3V_S5	1D8V_SUS

LBB-2

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Title: **BLOCK DIAGRAM**

Size	Document Number	Rev
A2	Bumblebee-2	1

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Main Func = CPU

24 PECI_CPU
24,44,46 PROCHOT#_CPU

71 -TBT_PLUG_EVENT

61 BLUETOOTH_EN_CPU

99 PROC_TCK
99 PROC_TDI
99 PROC_TMS
99 PROC_TRST#
99 PCH_JTAG_TCK
99 PROC_TDO
99 PROC_PREQ#
99 PROC_PRDY#
40 THERMTRIP#_EC

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

1D05V_VCCSTG
1D05V_VCCST
Rb R301 1KR2J-1-GP
Ra
R329 49D9R2F-GP
R302 499R2F-2-GP
R328 0R2-PT5-LILY-GP-U
TPAD14-OP-GP TP304
TPAD14-OP-GP TP305
TPAD14-OP-GP TP302
TPAD14-OP-GP TP303
R319 0R2-PT5-LILY-GP-U
R320 0R2-PT5-LILY-GP-U
R304 49D9R2F-GP
R305 49D9R2F-GP

CPU1D 4 OF 20

CATERR# CPU	AA4	CATERR#	
PECI CPU	AR1	PECI	
PROCHOT# CPU R	Y4	PROCHOT#	
THERMTRIP# CPU	BJ1	THRMTRIP#	
BPM CPU N0	U1	BPM#0	
BPM CPU N1	U2	BPM#1	
BPM CPU N2	U3	BPM#2	
BPM CPU N3	U4	BPM#3	
GPP E3	CE9	GPP_E3/CPU_GP0	
	CN3	GPP_E7/CPU_GP1	
	CB34	GPP_B3/CPU_GP2	
GPP B4	CC35	GPP_B4/CPU_GP3	
CPU POPIRCOMP	BP27	PROC_POPIRCOMP	
PCH POPIRCOMP	BW25	PCH_OPIRCOMP	

PROC_TCK	T6	PROC_TCK
PROC_TDI	U6	PROC_TDI
PROC_TDO	Y5	PROC_TDO
PROC_TMS	T5	PROC_TMS
PROC_TRST#	AB6	PROC_TRST#
PCH_TCK	W6	PCH_JTAG_TCK
PCH_TDI	U5	
PCH_TDO	W5	
PCH_TMS	P5	
PCH_TRST#	Y6	
PCH_JTAGX	P6	
PROC_PREQ#	W2	PROC_PREQ#
PROC_PRDY#	W1	PROC_PRDY#

WHISKEY-LAKE-GP

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CPU1 will use BOM control to Cometlake-U

1D05V_VCCST
R308 1KR2J-1-GP
THERMTRIP#_CPU

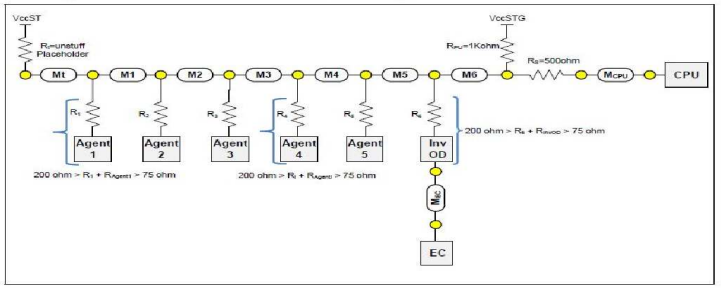
1D05V_VCCSTG
PROC_TDO R321 100R2J-2-GP

If PCH_TDO is set to Termination, R321 is 100ohm.
If PROC_TDO uesd, R321 is 51ohm.

PROC_TCK R322 51R2J-2-GP
PCH_JTAG_TCK R326 51R2J-2-GP
DY

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

LBB-2

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Title: CPU (THML/JTAG)
Size: A3 | Document Number: Bumblebee-2 | Rev: 1
Date: Tuesday, March 03, 2020 | Sheet 3 of 106

Main Func = CPU

DOCK

71 DP1_DDI_TX_N0
71 DP1_DDI_TX_P0
71 DP1_DDI_TX_N1
71 DP1_DDI_TX_P1
71 DP1_DDI_TX_N2
71 DP1_DDI_TX_P2
71 DP1_DDI_TX_N3
71 DP1_DDI_TX_P3
71 DP1_AUX_CPU_N
71 DP1_AUX_CPU_P
71 DP1_HPD_CPU

USBC

56 DP2_DDI_TX_N0
56 DP2_DDI_TX_P0
56 DP2_DDI_TX_N1
56 DP2_DDI_TX_P1
56 DP2_DDI_TX_N2
56 DP2_DDI_TX_P2
56 DP2_DDI_TX_N3
56 DP2_DDI_TX_P3
56 DP2_AUX_CPU_N
56 DP2_AUX_CPU_P
56 DP2_HPD_CPU

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 eDP_HPD_CPU

24 L_BKLT_EN
55 L_BKLT_CTRL
55 EDP_VDD_EN

15 GPP_H17_STRAP

24 EC_SMI#

56 DP2_SCL_CPU
56 DP2_SDA_CPU

62 WWAN_PERST#

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

CHECK WHL design guide: DISP_RCOMP

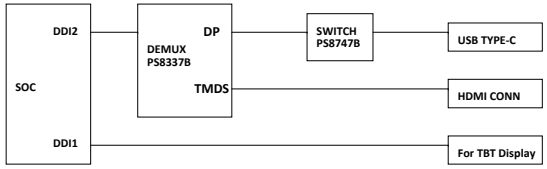
1D05V_VCCIO
R401 24D9R2F-L-GP
eDP_RCOMP_CPU → AM6 DISP_RCOMP

3D3V_SUS
R407 2K2R2J-2-GP DP1_SDA_CPU
3D3V_S0
RN402 SRN2K2J-1-GP
DP2_SDA_CPU
DP2_SCL_CPU
R404 10KR2J-3-GP EC_SMI#

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

TABLE: Functional Strap

DDPB_CTRLDATA **HIGH Port B is detected.** **LOW Port B is not detected.**
DDPC_CTRLDATA **HIGH Port C is detected.** **LOW Port C is not detected.**



CPU1A — 1 OF 20

DP1_DDI_TX_N0 AL5 DDI1_TXN0
DP1_DDI_TX_P0 AL6 DDI1_TXP0
DP1_DDI_TX_N1 AJ5 DDI1_TXN1
DP1_DDI_TX_P1 AJ6 DDI1_TXP1
DP1_DDI_TX_N2 AF6 DDI1_TXN2
DP1_DDI_TX_P2 AF5 DDI1_TXP2
DP1_DDI_TX_N3 AE5 DDI1_TXN3
DP1_DDI_TX_P3 AE6 DDI1_TXP3
DP2_DDI_TX_N0 AC4 DDI2_TXN0
DP2_DDI_TX_P0 AC3 DDI2_TXP0
DP2_DDI_TX_N1 AC1 DDI2_TXN1
DP2_DDI_TX_P1 AC2 DDI2_TXP1
DP2_DDI_TX_N2 AE4 DDI2_TXN2
DP2_DDI_TX_P2 AE3 DDI2_TXP2
DP2_DDI_TX_N3 AE1 DDI2_TXN3
DP2_DDI_TX_P3 AE2 DDI2_TXP3

EDP_TXN0 AG4 eDP_TX_CPU_N0
EDP_TXP0 AG3 eDP_TX_CPU_P0
EDP_TXN1 AG2 eDP_TX_CPU_N1
EDP_TXP1 AG1 eDP_TX_CPU_P1
EDP_TXN2 AJ4 eDP_TX_CPU_N2
EDP_TXP2 AJ3 eDP_TX_CPU_P2
EDP_TXN3 AJ2 eDP_TX_CPU_N3
EDP_TXP3 AJ1 eDP_TX_CPU_P3
EDP_AUX_N AH4 eDP_AUX_CPU_N
EDP_AUX_P AH3 eDP_AUX_CPU_P
DISP_UTILS AM7 EDP_DISP_UTILS — TP401 TPAD14-OP-GP
DDI1_AUX_N AC7 DP1_AUX_CPU_N
DDI1_AUX_P AC6 DP1_AUX_CPU_P
DDI2_AUX_N AD4 DP2_AUX_CPU_N
DDI2_AUX_P AD3 DP2_AUX_CPU_P
DDI3_AUX_N AG7
DDI3_AUX_P AG6

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 DP1_HPD_CPU
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6 DP2_HPD_CPU
GPP_E15/DDPD_HPD2/DISP_MISC2 CP7 WWAN_PERST#
GPP_E16/DDPE_HPD3/DISP_MISC3 CP6 EC_SMI#
GPP_E17/EDP_HPD/DISP_MISC4 CM7 EDP_HPD_CPU
EDP_BKLTEN CK11 L_BKLT_EN
EDP_VDDEN CG11 EDP_VDD_EN
EDP_BKLTCTL CH11 L_BKLT_CTRL

R403 10KR2J-1-GP
R402 10KR2J-1-GP
R406 10KR2J-1-GP
R405 10KR2J-1-GP

DP1_SDA_CPU → CC8 CC9 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE# GPP_E19/DPPB_CTRLDATA
DP2_SCL_CPU → CH4 GPP_E20/DPPC_CTRLCLK
DP2_SDA_CPU → CH3 GPP_E21/DPPC_CTRLDATA
TPAD14-OP-GP TP402 GPP_E23_STRAP → CP4 CN4 GPP_E22/DPPD_CTRLCLK GPP_E23/DPPD_CTRLDATA
GPP_H17_STRAP → CR26 CP26 GPP_H16/DDPF_CTRLCLK GPP_H17/DDPF_CTRLDATA
reserved for strap

WHISKEY-LAKE-GP

ZZ.00CPU.271
CPU1 will use BOM control to Cometlake-U

LBB-2

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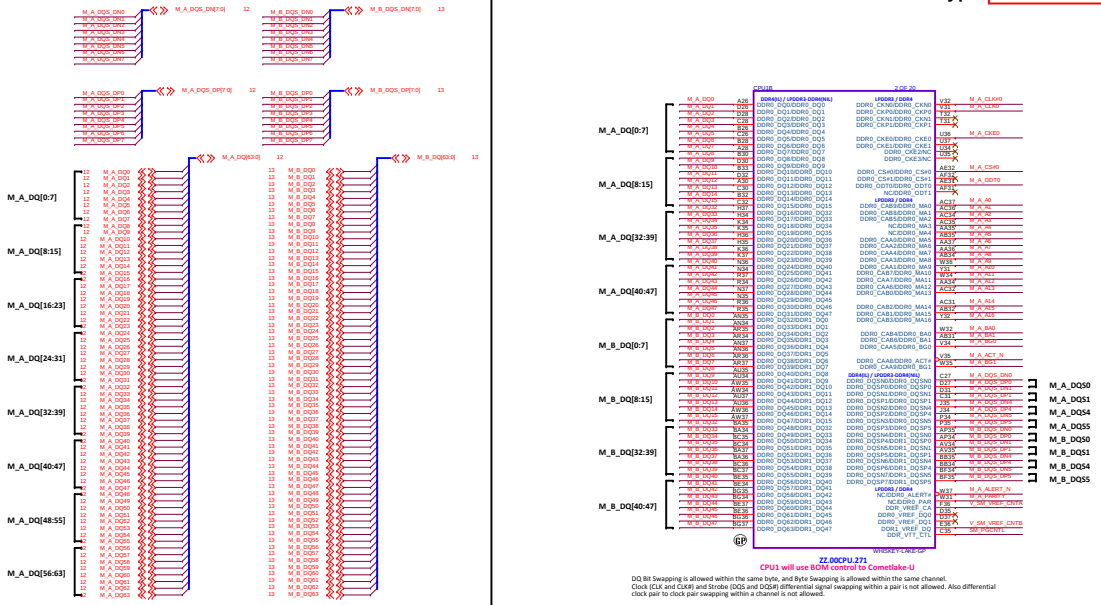
Title: **CPU (DDI/EDP)**

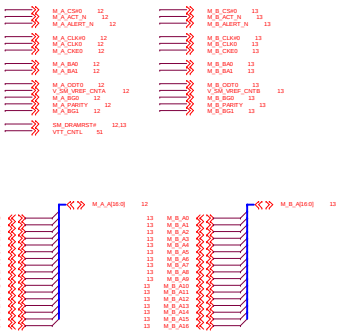
Size	Document Number	Rev
A2	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 4 of 106

Main Func = CPU

DDR4 ball type: Non-Interleaved Type





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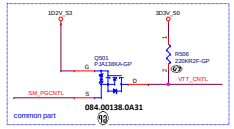
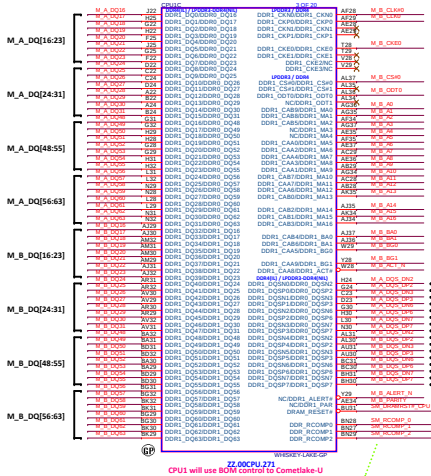
CPU1 will use BOM control to Cometlake-U

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.





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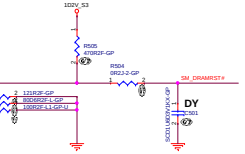
CPU1 will use BOM control to Cometlake-U



Layout Note:

#575412 Rev 1.5
Table 4-8. WHL-U/CFL-U DDR4 x16 Memory Down Routing Guideline (mils)

Design Guideline:
SM_RCOMP_0/1/2 keep routing length less than 500 mils.

#575412 Rev 1.5
Table 4-8. WHL-U/CFL-U DDR4 x16 Memory Down Routing Guideline (mils)

DDR - DDR4 X 16 Memory Down
DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS
DDR_RCOMP[1]: 80.6Ω ±1% on pkg to VSS
DDR_RCOMP[2]: 100Ω ±1% on pkg to VSS

LBB-2

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Title: CPU(CFG/IST)

Size	Document Number	Rev
A1	Bumblebee-2	1

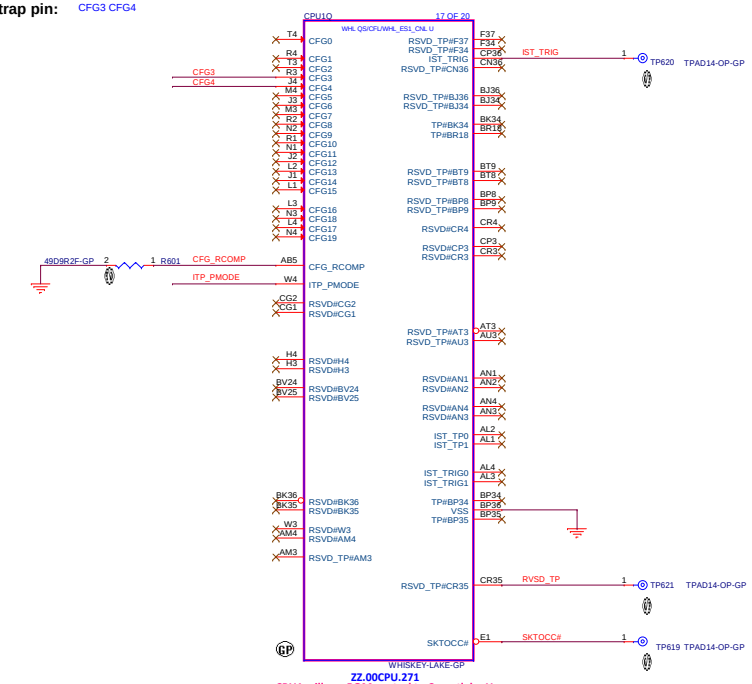
Date: Tuesday, March 01, 2022 Sheet 5 of 105

Main Func = CPU

15,99 CFG3
15 CFG4

99 ITP_PMODE

PCH strap pin: CFG3 CFG4



ZZ.00CPU.271
CPU1 will use BOM control to Cometlake-U

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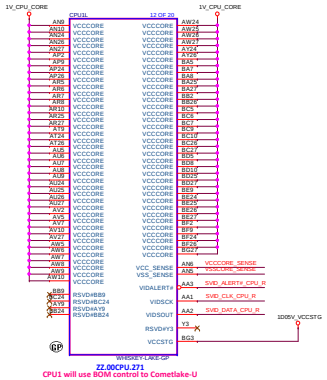
Title: CPU(CFG/IST)

Size: A2 | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020 | Sheet 6 of 106

46 VCCCORE_SENSE
46 VSSCORE_SENSE

46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU



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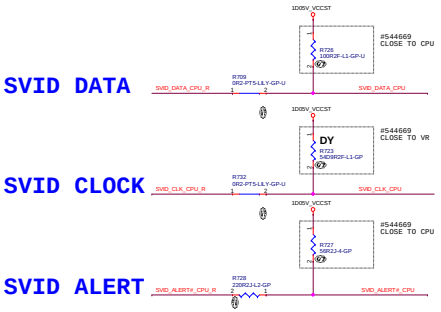
CPU1 will use BOM control to Cometlake-U

Layout Note:
The total length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



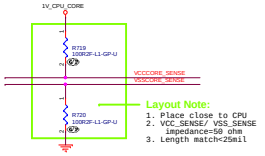


Figure 10-7. Routing Illustration for SVID Topology

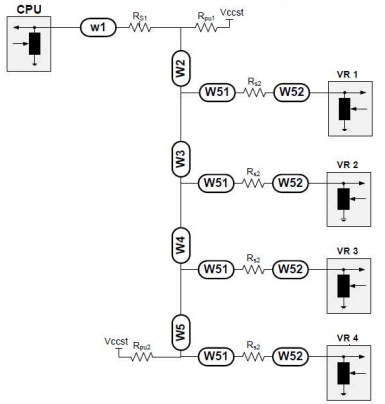


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{pu} [Ω]	R_{pu2} [Ω]	R_{s1} [Ω]	R_{s2} [Ω]	VCCgt [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

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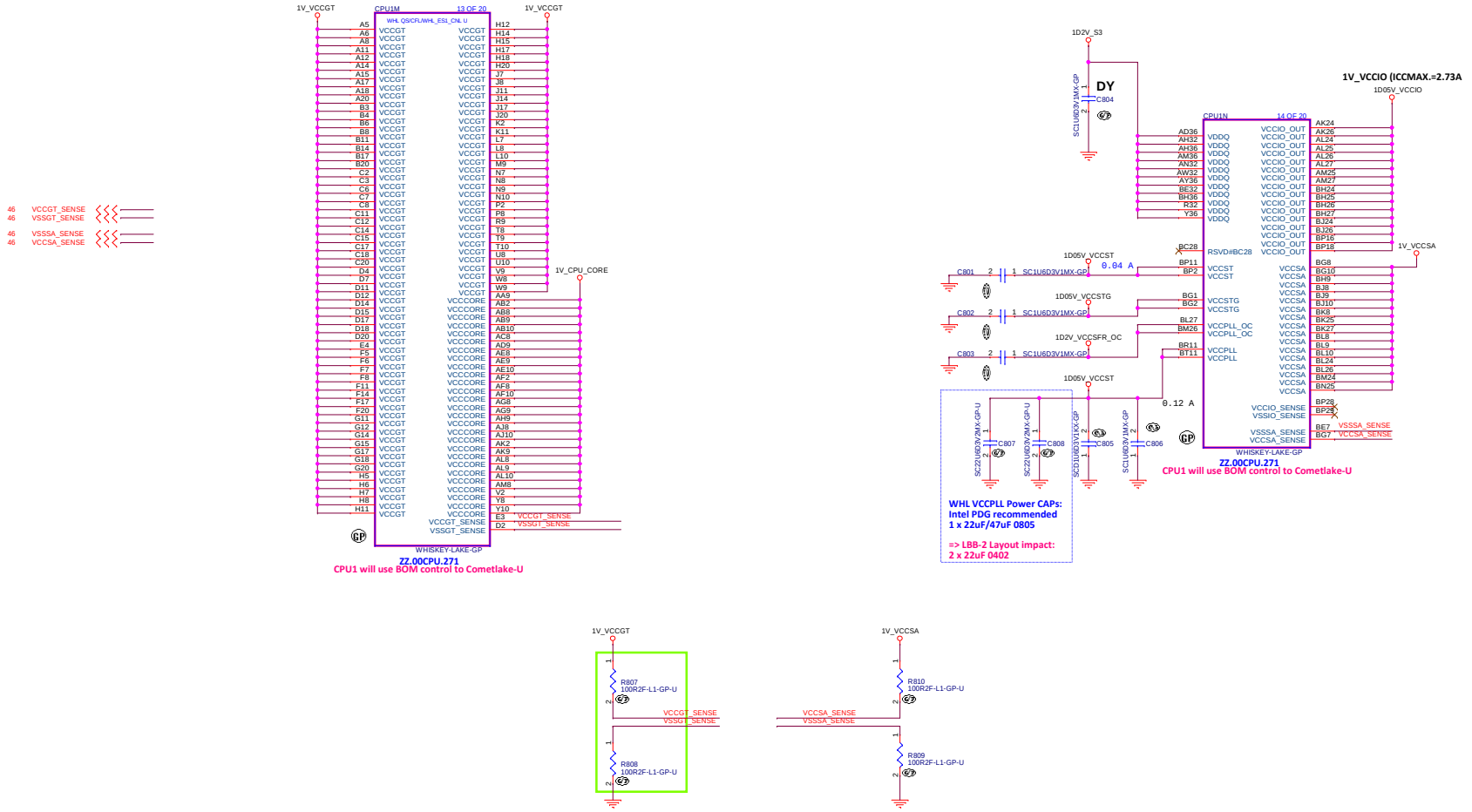
Title: CPU(VCC_CORE)
Size: A1 | Document Number: Bumblebee-2 | Rev: 1
Date: Tuesday, March 03, 2020 | Sheet 7 of 105

Main Func = CPU



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(VDDQ/VCC/VCCST/VCCSTG)**

Size	Document Number	Rev
A2	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 8 of 106

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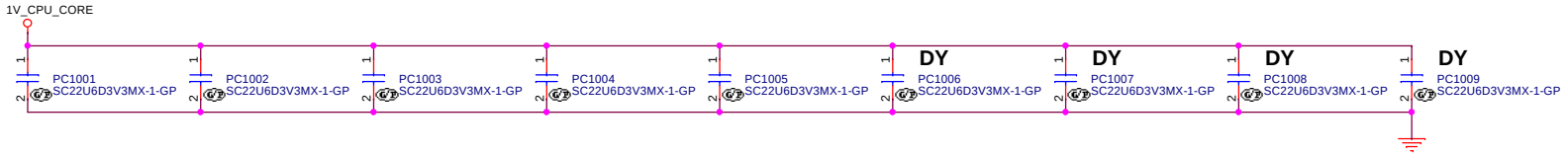
Taipei Hsien 221, Taiwan, R.O.C.

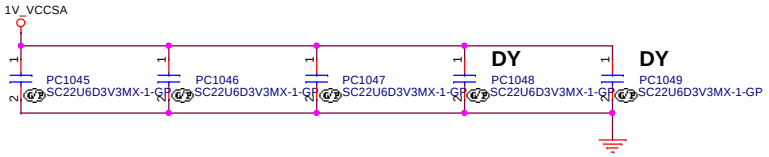
Title: ***CPU (RSVD)***

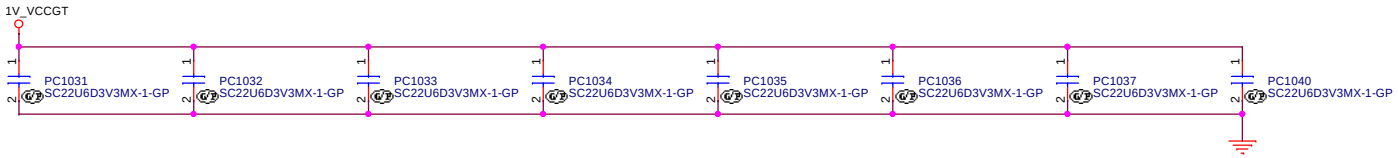
Size	Document Number	Rev
A4	**Bumblebee-2**	**1**

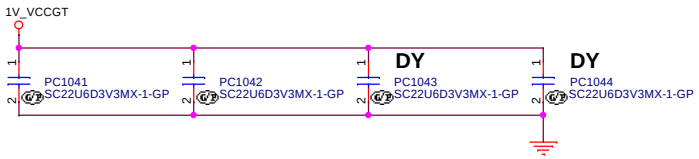
Date: Tuesday, March 03, 2020 Sheet 9 of 106

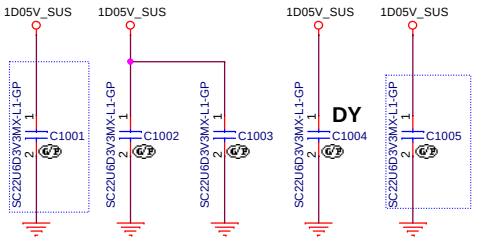
Main Func = CPU

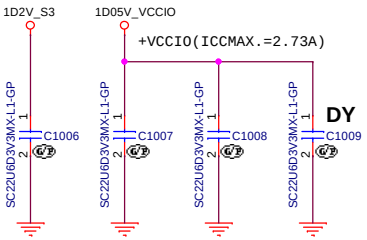












LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (POWER CAP1)*		
Size: A3	Document Number: **Bumblebee-2**	Rev: **1**
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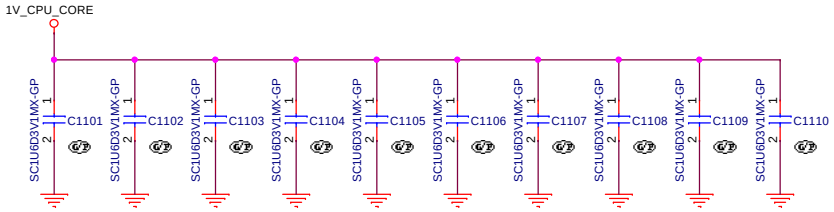
VCORE



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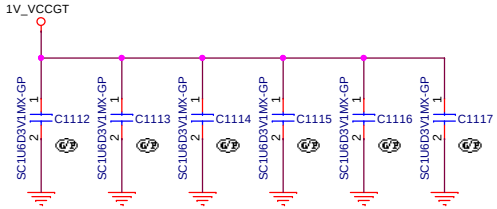
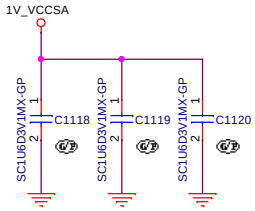
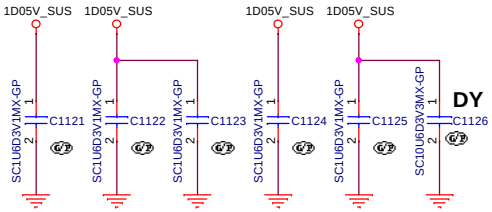
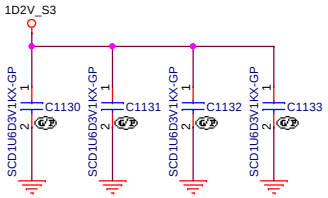
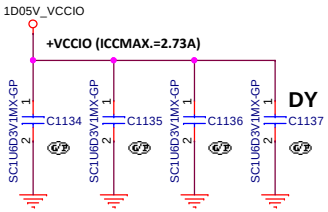


VCCSA









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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (POWER CAP2)*		
Size: A3	Document Number: **Bumblebee-2**	Rev: 1
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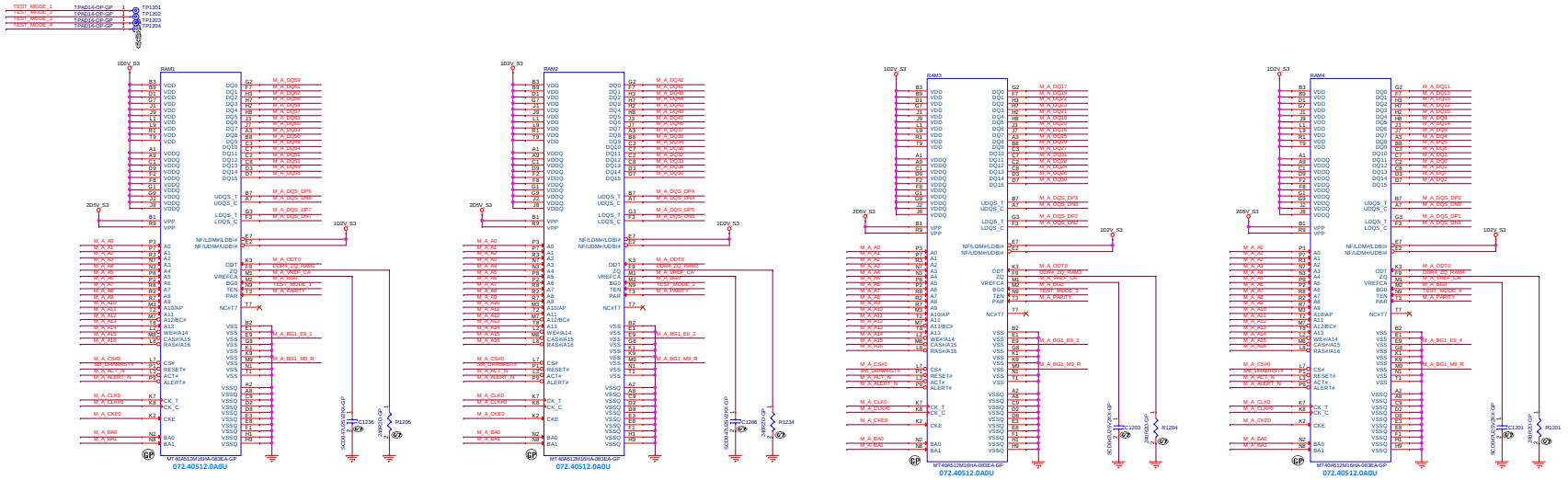
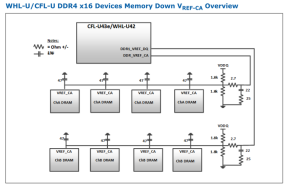
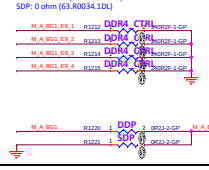


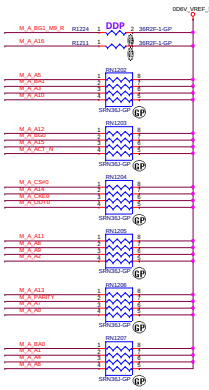
Figure 4-8. WHL-U/CFL-U DDR4 x16 Devices Memory Down V_{REF-CA} Overview

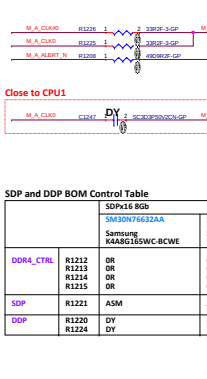


SDP & DDP SETTING

R1212~R1215:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)







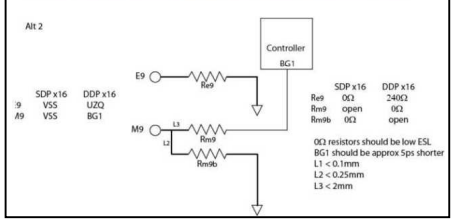
Close to CPU1

SDP and DDP BOM Control Table

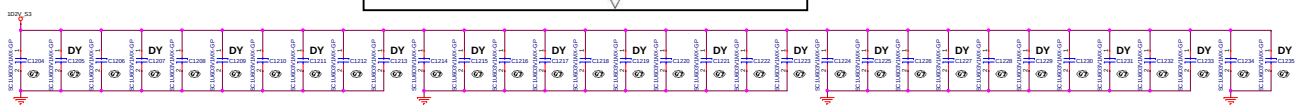
		SDPx16 8Gb		SDPx16 16Gb	DDPx16 16Gb	SDPx16 16Gb
		SM30N76632AA	SM30N76639AA	SM30N76570AA	SM30N76633AA	SM30N76640AA	SM30N76641AA
		Samsung K4A8G165WC-BCWE	SK Hynix H5AN8G6NCJR-XNC	Micron MT40A512M16TB-062E:J	Samsung K4AAG165WA-BCWE	SK Hynix H5ANAG6NCMR-XNC	Micron MT40A1G16KD-062E:E
DDR4_CTRL	R1212	0R	0R	0R	0R	240R 1%	0R
	R1213	0R	0R	0R	0R	240R 1%	0R
	R1214	0R	0R	0R	0R	240R 1%	0R
	R1215	0R	0R	0R	0R	240R 1%	0R
SDP	R1221	ASM	ASM	ASM	ASM	DY	ASM
DDP	R1220	DY	DY	DY	DY	ASM	DY
	R1224	DY	DY	DY	DY	ASM	DY

DDP x16 and SDP x16 Compatible Layout

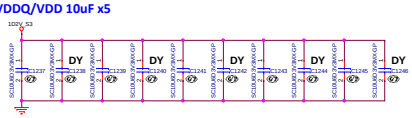
- Alternate two layout, risk of VSS offset increases a little



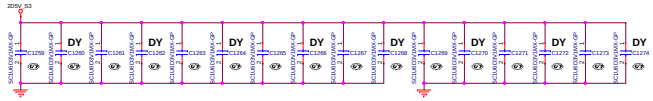
VDDQ/VDD 1uF x16



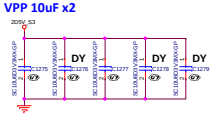
VDDQ/VDD 10uF x5



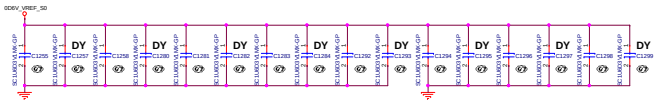
VPP 1uF x8



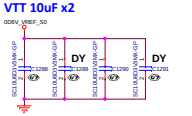
VPP 10uF x2



VTT 1uF x8



VTT 10uF x2



LBB-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHA)

Size	Document Number	Rev
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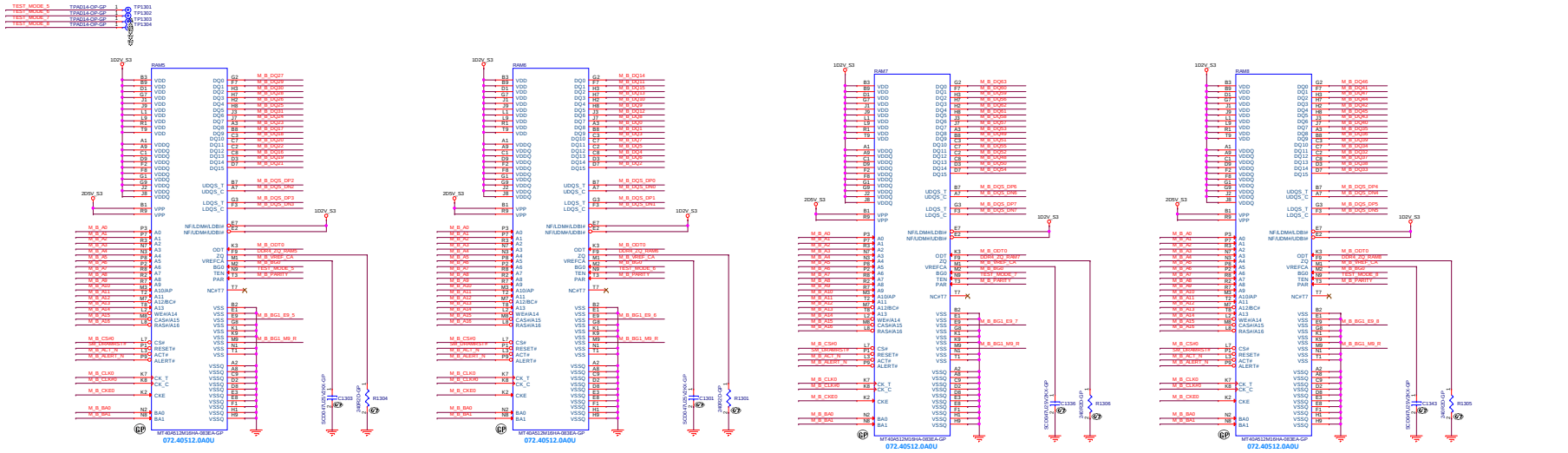
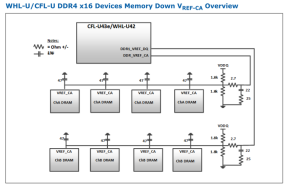
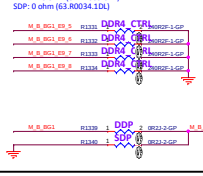
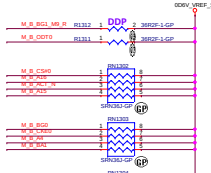
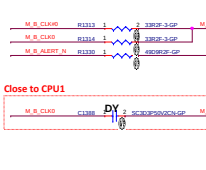


Figure 4-8. WHL-U/CFL-U DDR4 x16 Devices Memory Down V_{REF-CA} Overview



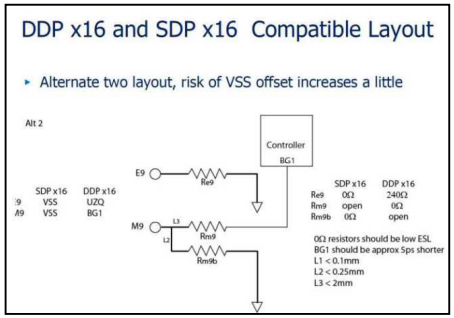






SDP & DDP SETTING

R1331~R1334:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)

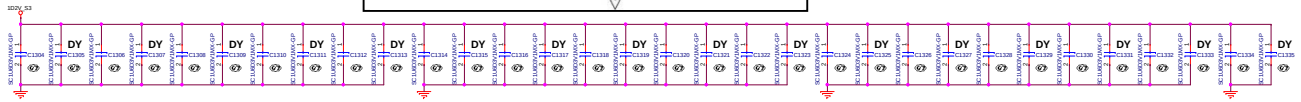


Close to CPU1

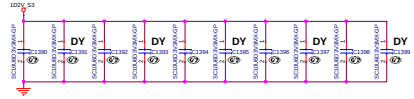
SDP and DDP BOM Control Table

		SDPx16 8Gb		SDPx16 16Gb	DDPx16 16Gb	SDPx16 16Gb
		SM30N76632AA	SM30N76639AA	SM30N76570AA	SM30N76633AA	SM30N76640AA	SM30N76641AA
		Samsung K4A8G165WC-BCWE	SK Hynix H5AN8G6NCJR-XNC	Micron MT40A512M16TB-062E:J	Samsung K4AAG165WA-BCWE	SK Hynix H5ANAG6NCMR-XNC	Micron MT40A1G16KD-062E:E
DDR4_CTRL	R1331	0R	0R	0R	0R	240R 1%	0R
	R1332	0R	0R	0R	0R	240R 1%	0R
	R1333	0R	0R	0R	0R	240R 1%	0R
	R1334	0R	0R	0R	0R	240R 1%	0R
SDP	R1340	ASM	ASM	ASM	ASM	DY	ASM
DDP	R1339	DY	DY	DY	DY	ASM	DY
	R1312	DY	DY	DY	DY	ASM	DY

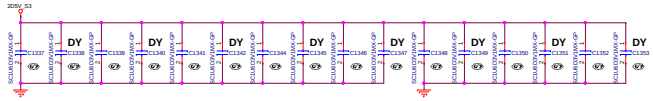
VDDQ/VDD 1uF x16



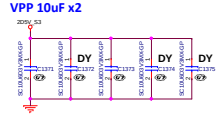
VDDQ/VDD 10uF x5



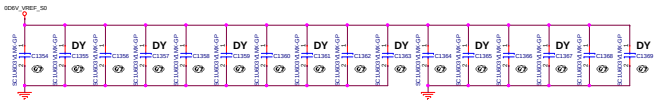
VPP 1uF x8



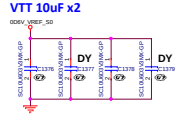
VPP 10uF x2



VTT 1uF x8



VTT 10uF x2



LBB-2
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHB)

Size	Document Number	Rev
A1	Bumblebee-2	1

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***DDR (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-2**	**1**

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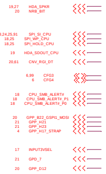
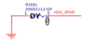
Main Func = PCH

HW Strap



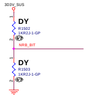
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

GPP_B14



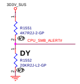
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_B18



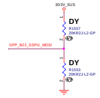
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_C2



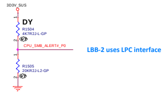
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6** — **Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

GPP_B22



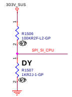
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the e*SPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**

GPP_C5



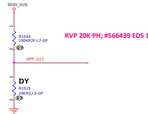
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_MOSI



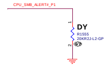
GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_D12



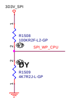
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.

GPP_B23



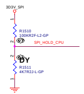
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2



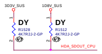
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3



HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_R2 / HDA_SDO / I2S0_TXD / HDACPU_SDO



GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

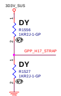
on page 71

GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

on page 4

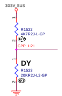
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



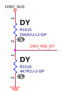
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_H21

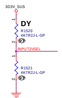


GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

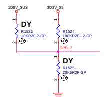
GPP_F6 / CNV_RGI_DT / UART0_TXD



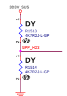
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.



GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

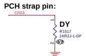


GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

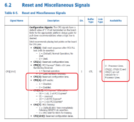


[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

PCH strap pin:

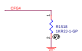


PDG datasheet. #575418



(#543016)

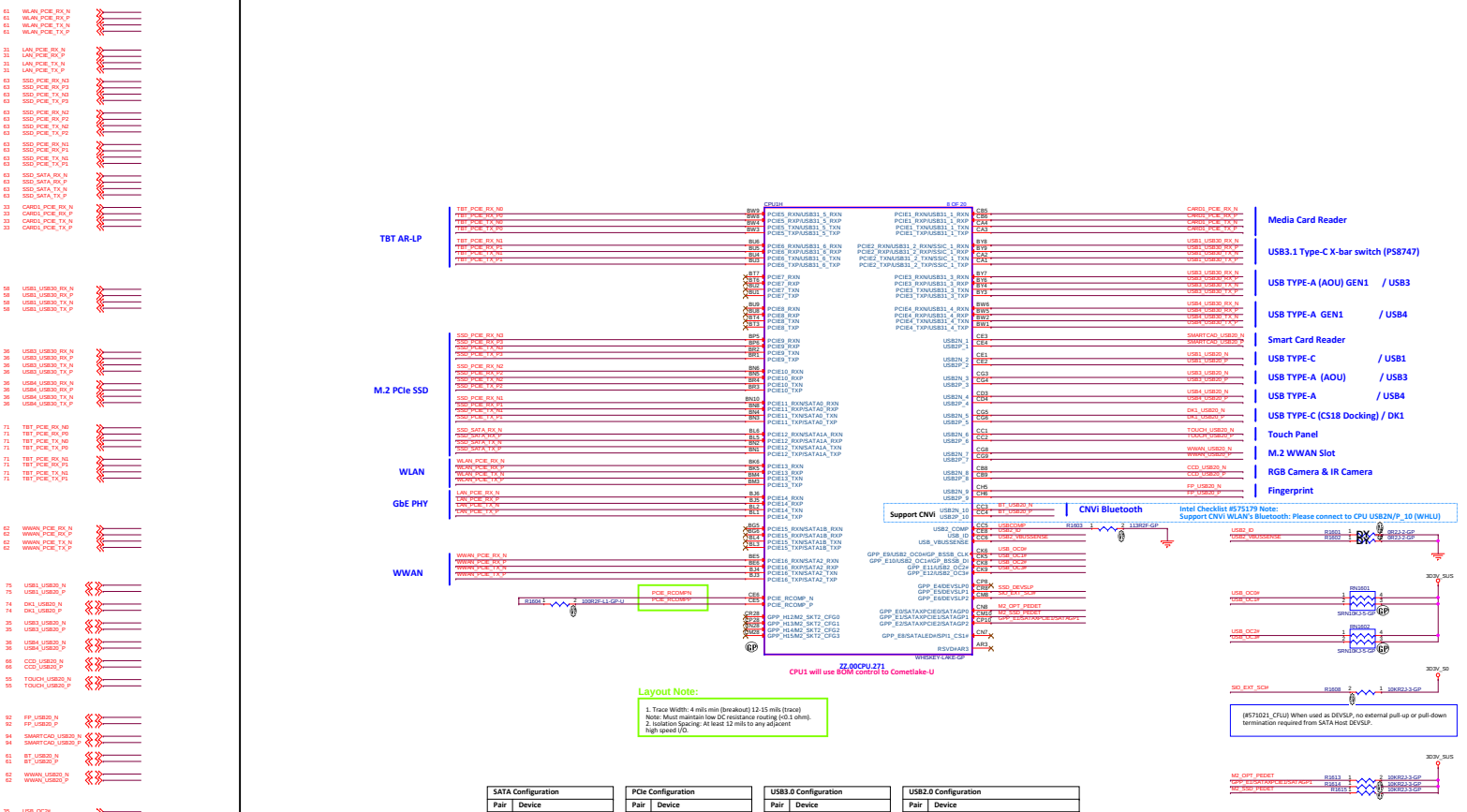
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.



LBB-2

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU(STRAP)	
Size A0	Document Number Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 15 of 106	

Main Func = PCH



SATA Configuration	
Pair	Device
0	NC
1A	M.2 SATA SSD
1B	NC
2	NC

PCIe Configuration	
Pair	Device
1	Media Card Reader
2	NC
3	NC
4	NC
5	TBT (AR-LP)
6	TBT (AR-LP)
7	NC
8	NC
9	M.2 PCIe SSD
10	M.2 PCIe SSD
11	M.2 PCIe SSD
12	M.2 PCIe SSD
13	WLAN
14	GbE
15	NC
16	WWAN

USB3.0 Configuration	
Pair	Device
1	NC
2	USB3 Type-C Port1
3	USB3 Type-A Port3 (AOU)
4	USB3 Type-A Port4
5	NC
6	NC

USB2.0 Configuration	
Pair	Device
1	Smart Card Reader
2	USB3 Type-C Port1
3	USB3 Type-A Port3 (AOU)
4	USB3 Type-A Port4
5	USB3 Type-C (CS18 Docking) Port2 / DK1
6	Touch Screen
7	WWAN Card
8	RGB/IR Hybrid Camera
9	Fingerprint
10	Bluetooth (CNVi)

LBB-2

緯創資通	Wistron Corporation	
	21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU (PCIE/SATA/USB)		
Size: A1	Document Number: Bumblebee-2	Rev: 1
Date: Tuesday, March 03, 2020	Sheet 16 of 105	

Main Func = PCH

24,56 SYS_PWROK
40 RESET_OUT#

17,24,40 VCCST_PWRGD
24 RSMRST#_KBC
40,45,52,53 3V_5V_PWRGD
40,89 PM_SLP_S0#
24,40,71,99 PM_SLP_S3#
24,40,51,99 PM_SLP_S4#
99 PM_SLP_S5#

24,40,52,53 PM_SLP_SUS#
24 PM_SLP_LAN#
24 PM_SLP_WLAN#
24,63,99 PM_PWRBTN#
4,31,33,40,61,62,63,68,71,89,91 PLTRST#_CPU
24 AC_PRESENT

33,61,62,71 PCIE_WAKE#_CPU

24,71 PCH_BATLOW#
15 INPUT3VSEL

31 LAN_WAKE#
31 LANPHYPC

99 XDP_DBRESET#
99 PM_RSMRST#
40 H_THERMTRIP_EN
24,99 PM_SLP_M#

3D3V_S5
R1752 1 2 10KR22-3-GP AC_PRESENT
R1753 1 2 10KR22-3-GP PCIE_WAKE#_CPU
R1746 1 2 10KR22-3-GP PCH_BATLOW#

H_CPUPWRGD
DY R1714 10KR22-3-GP
XDP_DBRESET#
DY EC1706 SC1KP50V2KX-1GP

3D3V_SUS
R1731 1 2 100KR22-1-GP EXT_PWR_GATE#

3D3V_S5
R1738 1 DY 2 10KR22-3-GP
R1708 1 2 0R2-PTS-LILY-GP-U ME_SUS_PWR_ACK_R
SUSACK#_R
R1739 1 2 10KR22-3-GP PM_RSMRST#
R1740 2 DY 1 10KR22-3-GP PM_PCH_PWROK
R1717 2 DY 1 10KR22-3-GP SYS_PWROK

3D3V_SUS 3D3V_S0
DY R1747 1KR22-1-GP
R1701 1KR21-1-GP
XDP_DBRESET#
H_THERMTRIP_EN
H_VCCST_PWRGD
RESET_OUT#
3V_5V_PWRGD
PM_RSMRST#
R1750 1 2 0R2-2-GP
R1751 1 2 0R2-2-GP
R1706 1 2 0R2-PTS-LILY-GP-U
R1704 1 2 0R2-2-GP
R1755 1 2 0R2-2-GP
DY
Follow wistron ORS design.
H_CPUPWRGD
VCCST_PWRGOOD
SYS_PWROK
PCH_PWROK
SSW_PWROK
ME_SUS_PWR_ACK_R
SUSACK#_R
PCIE_WAKE#_CPU
LAN_WAKE#
LANPHYPC
PCH_PLTRST#
PM_RSMRST#
H_CPUPWRGD
VCCST_PWRGOOD
SYS_PWROK
PCH_PWROK
SSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDACK
GPP_A15/SUSACK#
WAKE#
GPD0/LAN_WAKE#
GPD1/LANPHYPC
3D3V_S5
R1707 1 2 10KR22-3-GP

CPU1K
GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGOOD
SYS_PWROK
PCH_PWROK
SSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDACK
GPP_A15/SUSACK#
WAKE#
GPD0/LAN_WAKE#
GPD1/LANPHYPC
11 OF 20
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD5/SPI_WLAN#
GPD6/SLP_A#
GPD1/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
INPUT3VSEL
WHSKEY-LX6Z-GP
22.00CPU.271
CPU1 will use BOM control to Cometlake-U

3D3V_RTC_AUX
#575412, v0.9, p.30: 1M-ohm PU and 330K-ohm is used on the CRB
R1730 1MR22-1-GP

PDG #575412 p128
3D3V_S5
PM_SLP_S0# R1703 DY 100KR22-1-GP
PM_SLP_LAN# R1705 DY 100KR22-1-GP
PM_PWRBTN# R1721 100KR22-1-GP

BATLOW#:
Pull-up required even if not implemented.

AC_PRESENT
DY SC1KP50V2KX-1GP EC1707

LCASE BTN2
TAMPER_SW_DTCT
INTRUDER_SW
R1745 0R2-PTS-LILY-GP-U
D1701 RB520S30M-30T2R-GP-U
INTRUDER_EC
SW1 BTN2 SW-4P-9-GP
PCB 40003-0011 REV:A
SPVR310Z00

TP1708 TPAD14-OP-GP

PLTRST#_CPU
R1713 0R2-PTS-LILY-GP-U PCH_PLTRST#
R1715 100KR22-1-GP
DY C1701 SC220P50V2KX-3GP
R1715 PD for CNVI

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us

Dis-wire with XDP_PM_RSMRST_PWRGD_XDP

3D3V_SUS 1D05V_VCCST 1D05V_SUS
DY EC1702 SCD1U16V2KX-GP
DY R1722 1KR22-1-GP
DY R1723 1KR22-1-GP
U1701 74LVC1G07GW-GP
17,24,40 VCCST_PWRGD
H_VCCST_PWRGD
R1749 100KR2F-L2-GP
R1748 47KR2F-GP

3D3V_S5 3D3V_AUX_S5
RB520S30M-30T2R-GP-U D1703
RB520S30M-30T2R-GP-U D1702
3V_5V_PCH_EN
R1726 10KR23-3-GP
3V_5V_PCH#
Q1701 2N7002KDW2-1-GP 75.27002.F7C
PM_RSMRST#
3V_5V_PCH_C
R1702 1KR22-1-GP
R1728 0R2-PTS-LILY-GP-U
RSMRST#_KBC
3V_5V_PWRGD
3D3V_AUX_S5
R1727 100KR22-1-GP
DY EC1710 SCD22U10V2KX-GP
DY EC1712 SC1U25V2KX-1GP

LBB-2

緯創資通	Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: PCH (PMU)		
Size: A1	Document Number: Bumblebee-2	Rev: 1
Date: Tuesday, March 03, 2020	Sheet 17 of 105	

Main Func = PCH

BB2_EVT_MAIN_W022
BB2_EVT_MAIN_W002
BB2_SVT_MAIN_W003
BB2_SVT_MAIN_W005

PCH strap pin: SPI_SO_CPU

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PCH strap pin: CPU_SMB_ALERT#_P0

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.

Modern Standby State	MS_DTCT	Embedded Controller
Operation (S0)	Low	Normal Mode
Modern Standby (S0ix)	High	Low Power Mode

Media Card Reader
TBT
M.2 PCIe SSD
WWAN
GbE PHY
WLAN

PH on WWAN Conn

ZZ.00CPU.271
CPU1 will use BOM control to Cometlake-U

Close CPU1

R1843: LPC Debug Port for Security (Page 68)

24MHz (X1801)
TXC 7V24000023 082.30006.0571
TXC 7V24000051 082.30006.0681

32.768KHz (X1802)
EPSON EP.FC-135R 32.768K12.5+-20 (X1A000141000300) 082.30003.0191
SEIKO Q-SC32P0322DC5AAAF 082.30003.0301
TXC 9H03200042 082.30003.0231

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU_(SPI/ESPI/SMBUS/XTAL/CLK)	
Size: A1	Document Number: Bumblebee-2
Rev: 1	
Date: Tuesday, March 01, 2022	Sheet 18 of 105

Main Func = PCH

BB2_EVT_MAIN_W002 BB2_EVT_MAIN_W017 BB2_EVT_MAIN_W018 BB2_SVT_MAIN_W003 BB2_FVT_MAIN_L001

27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC
15 HDA_SDOUT_CPU
25 RTC_TEST

24 ME_FWP_EC

61 CLKREQ0_CNVI
61 RF_RESET_B_CNVI

15,27 HDA_SPKR

66 DMIC_SCL_CPU
66 DMIC_SDA_CPU

71 TBT_RTD3_PWR_EN
71 TBT_FORCE_USB_PWR
71 -TBT_PERST
71 -TBT_PCIE_WAKE

24 TOP_SWAP_EN

62 WWAN_ANTENNA#

55 OLED_DET#

PCH strap pin: HDA_SDOUT_CPU

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deassers

SW Control :

GPP_G1	
SD_MMC_ID	Low = REALTEK [RTS5232S]
	High = GENESYS [GL9750]

HW Control : *

R1903	R1904
1M-ohm	1K-ohm
1K-ohm	1M-ohm

<-- Default

CPU1G 7 OF 20

HDA_SYNC_CPU BN34 HDA_SYNC/I2S0_SFRM
HDA_BITCLK_CPU BN37 HDA_BCLK/I2S0_SCLK
HDA_SDOUT_CPU BN36 HDA_SDO/I2S0_TXD /strap
HDA_SDIN0_CPU BN35 HDA_SDI0/I2S0_RXD
BL36 HDA_SDI1/I2S1_RXD/SNDW1_DATA
TPAD14-OP-GP TP1903 1 HDA_RST_N_CPU BL35 HDA_RST#/I2S1_SCLK/SNDW1_CLK
CK23 GPP_D23/I2S_MCLK
BL37
BL34 I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA

GPP_G0/SD_CMD CH36
GPP_G1/SD_DATA0 CL38 SD_MMC_ID
GPP_G2/SD_DATA1 CL36 RTC_TEST
GPP_G3/SD_DATA2 CM35
GPP_G4/SD_DATA3 CN36 TBT_RTD3_PWR_EN
GPP_G5/SD_CD# CM35 TBT_FORCE_USB_PWR
GPP_G6/SD_CLK CK36 -TBT_PERST
GPP_G7/SD_WP CK34 -TBT_PCIE_WAKE

3D3V_SUS
R1903 1 SDID 2 1MR2J-1-GP
R1904 1 SDID 2 1KR2J-1-GP

RF_RESET_B_CNVI R1913 1 2 33R2J-2-GP GPP_H1_SFRM CJ32 GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
CLKREQ0_CNVI R1912 1 2 33R2J-2-GP GPP_H2_CLKREQ0 CH29 GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
OLED_DET# CH30 GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
DMIC_SCL_CPU R1922 1 2 33R2J-2-GP DMIC_SCL_CPU_R CP24 GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
DMIC_SDA_CPU R1923 1 2 33R2J-2-GP DMIC_SDA_CPU_R CN24 GPP_D19/DMIC_CLK0/SNDW4_CLK GPP_A16/SD_1P8_SEL
GPP_D20/DMIC_DATA0/SNDW4_DATA
TOP_SWAP_EN R1902 1 2 0R2-PT5-LILY-GP-U CK25 GPP_D17/DMIC_CLK1/SNDW3_CLK SD_1P8_RCOMP
C125 GPP_D18/DMIC_DATA1/SNDW3_DATA SD_3P3_RCOMP
HDA_SPKR CF35 GPP_B14/SPKR /strap

WHISKEY-LAKE-GP

1D8V_SUS
R1905 1 2 10KR2J-3-GP OLED_DET#

DY C1901 SC27P50V2JN-2-GP
DY C1902 SC27P50V2JN-2-GP

C1902:
Intel PDG recommended: 27pF
can be just a placeholder and stuffed only when needed

ZZ.00CPU.271
CPU1 will use BOM control to Cometlake-U

PCH strap pin: SPKR

TOP SWAP OVERRIDE	
HDA_SPKR	* High = TOP SWAP ENABLED Low = DISABLED (WEAK INTERNAL PD)

The internal pull-up

WWAN_ANTENNA# WWAN_ANTENNA_CPU BW36 BY33
SD_RCOMP R1901 1 2 200R2F-L-GP CK33 CM34
DY Q1901 LSK3541G1ET2L-1-GP

HDA_SYNC_CODEC R1908 1 2 33R2J-2-GP HDA_SYNC_CPU
HDA_BITCLK_CODEC R1920 1 2 33R2J-2-GP HDA_BITCLK_CPU
HDA_SDOUT_CODEC R1921 1 2 33R2J-2-GP HDA_SDOUT_CPU
ME_FWP_EC R1909 1 2 1KR2J-1-GP
R1914 1 DY 2 10KR2J-3-GP TOP_SWAP_EN

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(HDA/I2S/SD/DMIC)
Size: A2 | Document Number: Bumblebee-2 | Rev: 1
Date: Tuesday, March 03, 2020 | Sheet 19 of 106

Main Func = PCH

BB2_EVT_MAIN_W003
BB2_EVT_MAIN_W010
BB2_EVT_MAIN_W013
BB2_EVT_MAIN_W024
BB2_EVT_MAIN_W011
BB2_SVT_MAIN_W007

PDG #575412 p128

PCH strap pin: NRB_BIT

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

Strap pin

Bumblebee: GPP_H[0:23] is 1.8V.

Bumblebee: GPP_H[0:23] is 1.8V.

ZZ.00CPU.271
CPU1 will use BOM control to Cometlake-U

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

Sensors Debug Hooks_543016:

Table 31-3. 18-pin ZIF Connector Pinout

Pin	Pin function	Description
1	ISH_I2C0_SCL	Clock line for the I2C0
2	ISH_I2C0_SDA	Data line for the I2C0
3	ISH_I2C1_SCL	Clock line for the I2C1
4	ISH_I2C1_SDA	Data line for the I2C1
5	GND	System Ground
6	GPIOb (1)	Connect here one of the GPIOs in use
7	GPIOb (1)	Connect here one of the GPIOs in use
8	GPIOc (1)	Connect here one of the GPIOs in use
9	GPIOd (1)	Connect here one of the GPIOs in use
10	GND	System Ground
11	Reserved by Intel	Do not use
12	Reserved by Intel	Do not use
13	Reserved by Intel	Do not use
14	Reserved by Intel	Do not use
15	Reserved by Intel	Do not use
16	Reserved by Intel	Do not use
17	GND	System Ground
18	Vio	Sensors Reference Voltage

Sensors Debug Hooks

ISH

ACES-CON18-3-GP
20.K0698.018

Memory Configuration	Memory Supplier	Die Revision
00: 8Gb 01: 4Gb (Reserve) 10: 16Gb 11: 32Gb (Reserve)	00: Samsung 01: Micron 10: SK Hynix 11: (Reserve)	

GPP_H8	GPP_H7	GPP_H6	GPP_H5	GPP_H4				
SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Memory ID	Supplier	Density	Vendor PN
0	0	0	0	0	0	SAMSUNG	8GB (8Gb*8)	K4A8G165WC-BCWE
X	X	X	X	X	X			
1	0	0	0	0	16	SAMSUNG	16GB (16Gb*8)	K4AAG165WA-BCWE
X	X	X	X	X	X			
0	0	0	1	0	2	MICRON	8GB (8Gb*8)	MT40A512M16TB-062E:J
X	X	X	X	X	X			
1	0	0	1	0	18	MICRON	16GB (16Gb*8)	MT40A1G16KD-062E:E
X	X	X	X	X	X			
0	0	1	0	0	4	SK HYNIX	8GB (8Gb*8)	H5AN8G6NCJR-XNC
X	X	X	X	X	X			
1	0	1	0	0	20	SK HYNIX	16GB (16Gb*8)	H5ANAG6NCMR-XNC
X	X	X	X	X	X			

0=L, 1=H

SDRAM_ID4 R2073 R2074	SDRAM_ID3 R2011 R2012	SDRAM_ID2 R2022 R2029	SDRAM_ID1 R2017 R2018	SDRAM_ID0 R2015 R2016	Memory ID	Supplier	Density	Vendor PN
DY 10K	DY 10K	DY 10K	DY 10K	DY 10K	0	SAMSUNG	8GB (8Gb*8)	K4A8G165WC-BCWE
10K DY	DY 10K	DY 10K	DY 10K	DY 10K	16	SAMSUNG	16GB (16Gb*8)	K4AAG165WA-BCWE
DY 10K	DY 10K	DY 10K	10K DY	DY 10K	2	MICRON	8GB (8Gb*8)	MT40A512M16TB-062E:J
10K DY	DY 10K	DY 10K	10K DY	DY 10K	18	MICRON	16GB (16Gb*8)	MT40A1G16KD-062E:E
DY 10K	DY 10K	10K DY	DY 10K	DY 10K	4	SK HYNIX	8GB (8Gb*8)	H5AN8G6NCJR-XNC
10K DY	DY 10K	10K DY	DY 10K	DY 10K	20	SK HYNIX	16GB (16Gb*8)	H5ANAG6NCMR-XNC

LBB-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(UART/I2C/ISH)
Size: A2
Document Number: Bumblebee-2
Rev: 1
Date: Tuesday, March 03, 2020
Sheet 20 of 106

Main Func = PCH

BB2_EVT_MAIN_W016
BB2_SVT_MAIN_W003

CNVi

61 CNV_WT_DN0
61 CNV_WT_DP0
61 CNV_WT_DN1
61 CNV_WT_DP1
61 CNV_WT_CLK_DN
61 CNV_WT_CLK_DP
61 CNV_WR_DN0
61 CNV_WR_DP0
61 CNV_WR_DN1
61 CNV_WR_DP1
61 CNV_WR_CLK_DN
61 CNV_WR_CLK_DP
61 WIFI_RF_EN_CPU
68 CPU_UARTx_RXD
68 CPU_UARTx_TXD
40 CPU_C10_GATE#
15 GPP_H21
15 GPD_7
15 GPP_H23
62 -WWAN_RESET
62 WWAN_CFG0
62 WWAN_CFG1
62 WWAN_CFG2
62 WWAN_CFG3
65,90 NFC_ACTIVE
66 IR_CAM_DET#
66 DMIC_DET#
17 -TAMPER_SW_DTCT

CPU1I — 9 OF 20

CNVi

CNV_WR_DN0 CR30 CNV_WR_D0N
CNV_WR_DP0 CP30 CNV_WR_D0P
CNV_WR_DN1 CM30 CNV_WR_D1N
CNV_WR_DP1 CN30 CNV_WR_D1P
CNV_WT_DN0 CN32 CNV_WT_D0N
CNV_WT_DP0 CM32 CNV_WT_D0P
CNV_WT_DN1 CP33 CNV_WT_D1N
CNV_WT_DP1 CN33 CNV_WT_D1P
CNV_WR_CLK_DN CN31 CNV_WR_CLKN
CNV_WR_CLK_DP CP31 CNV_WR_CLKP
CNV_WT_CLK_DN CP34 CNV_WT_CLKN
CNV_WT_CLK_DP CN34 CNV_WT_CLKP

R2101 2 — 1 150R2F-1-GP CNV_WT_RCOMP CP32 CNV_WT_RCOMP#CP32
CR32 CNV_WT_RCOMP#CR32
R2120 0R2J-2-GP
WWAN_CFG2 CP20 GPP_F0/CNV_PA_BLANKING
-WWAN_RESET CK19 GPP_F1
NFC_ACTIVE 1 — 2 NFC_ACTIVE_CPU CG17 GPP_F2
DY
Debug Card
CPU_UARTx_RXD CR14 GPP_C8/UART0_RXD
CPU_UARTx_TXD CP14 GPP_C9/UART0_TXD
IR_CAM_DET# CN14 GPP_C10/UART0_RTS#
DMIC_DET# CM14 GPP_C11/UART0_CTS#
WWAN_CFG0 CJ17 GPP_F8/CNV_MFUART2_RXD
WWAN_CFG1 CH17 GPP_F9/CNV_MFUART2_TXD
GPP_F23 CF17 GPP_F23/A4WP_PRESENT

R2102 100KR1J-GP

3D3V_S0
R2122 1 — 2 10KR2J-3-GP IR_CAM_DET#
R2123 1 — 2 10KR2J-3-GP DMIC_DET#

GPP_H18/CPU_C10_GATE# CN27 GPPC_H18_BOOTMPC
GPP_H19/TIMESYNC0 CM27
GPP_H21 CF25 GPP_H21
GPP_H22 CN26
GPP_H23 CM26 GPP_H23
GPP_F10 CK17
GPD7 BV35 GPD_7
GPP_F3 CN20
GPP_D4/IMGCLKOUT0/BK4/SBK4 CG25 WIFI_RF_EN_CPU
GPP_H20/IMGCLKOUT1 CH25
GPP_F12/EMMC_DATA0 CR20
GPP_F13/EMMC_DATA1 CM20
GPP_F14/EMMC_DATA2 CN19
GPP_F15/EMMC_DATA3 CM19
GPP_F16/EMMC_DATA4 CN18
GPP_F17/EMMC_DATA5 CR18
GPP_F18/EMMC_DATA6 CP18
GPP_F19/EMMC_DATA7 CM18
GPP_F: VCCPGPPF = 1.8V Only
GPP_F20/EMMC_RCLK CM16
GPP_F21/EMMC_CLK CP16
GPP_F11/EMMC_CMD CR16 WWAN_CFG3
GPP_F22/EMMC_RESET# CN16 -TAMPER_SW_DTCT_CPU
EMMC_RCOMP CK15 EMMC_RCOMP

R2119 0R2-PT5-LILY-GP-U 1 — 2 CPU_C10_GATE#
R2121 0R2-PT5-LILY-GP-U 1 — 2 -TAMPER_SW_DTCT
R2108 1 — 2 200R2F-L-GP

WHISKEY-LAKE-GP

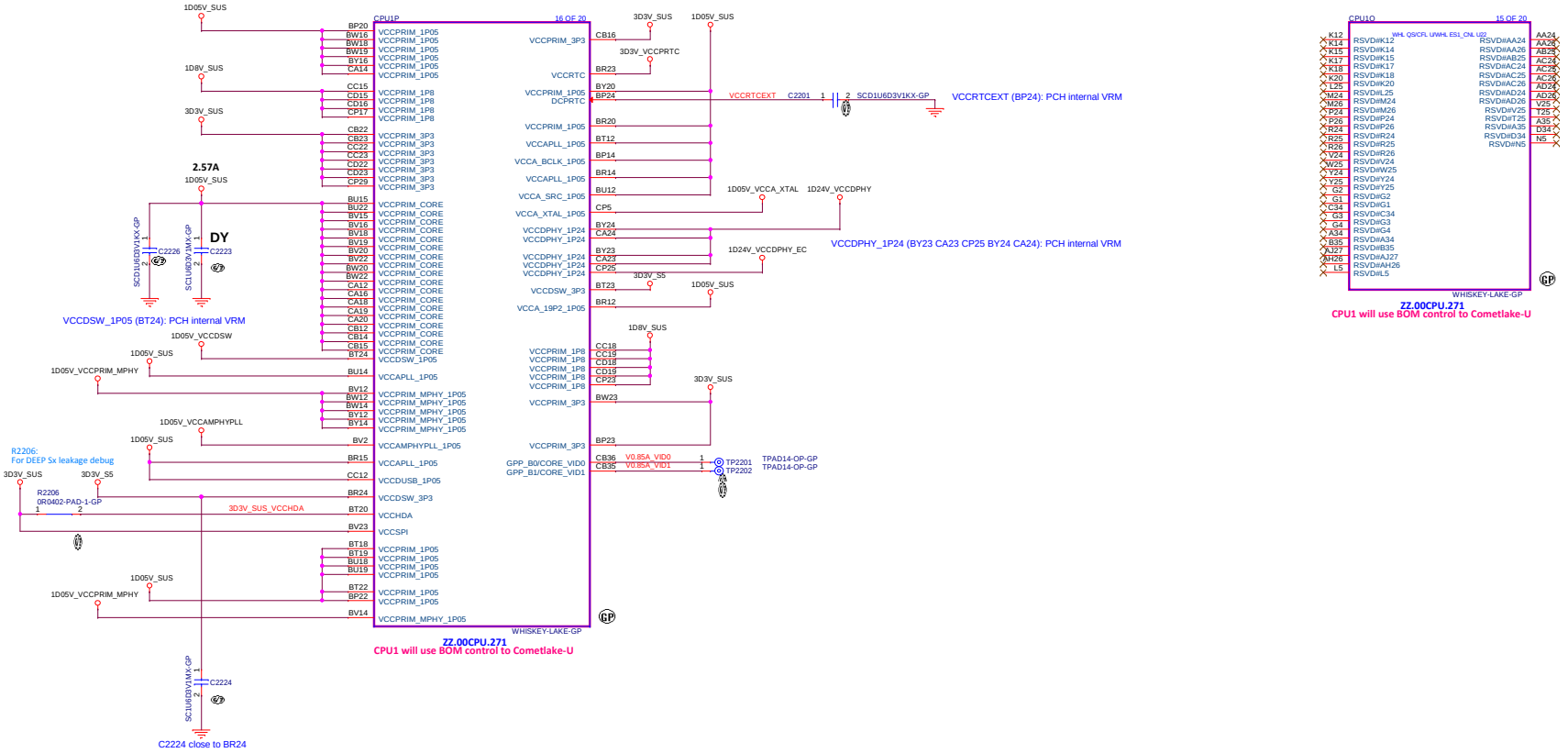
ZZ.00CPU.271
CPU1 will use BOM control to Cometlake-U

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(CSI/EMMC/CNVI)
Size: A3 | Document Number: Bumblebee-2 | Rev: 1
Date: Tuesday, March 03, 2020 | Sheet 21 of 106

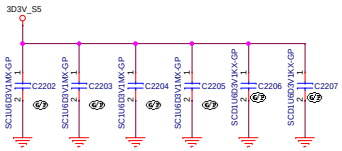
Main Func = PCH

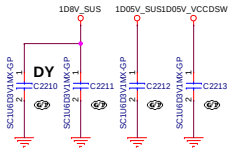


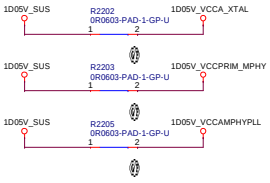
TBD

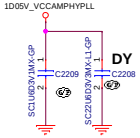
Layout Note:

1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19



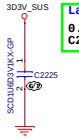






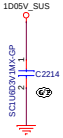
Layout Note:

C2208 near BV2
C2209 near BV2



Layout Note:

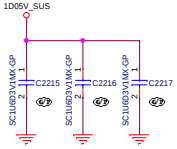
0.1uF:
C2225 near BT20



TBD

Layout Note:

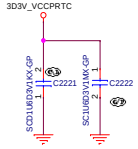
22uF:
C2113 near K15



TBD

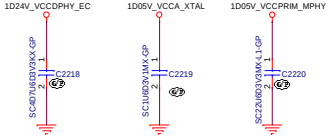
Layout Note:

1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1



Layout Note:

C2221 near BR23
C2222 near BR23



TBD

Layout Note:

1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

LBB-2

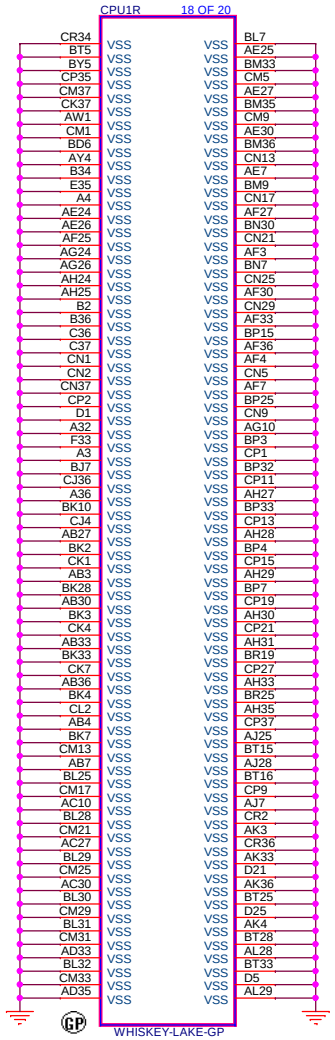
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(PCH-LP PWR&CAPS)**

Size: A2 | Document Number: **Bumblebee-2** | Rev: **1**

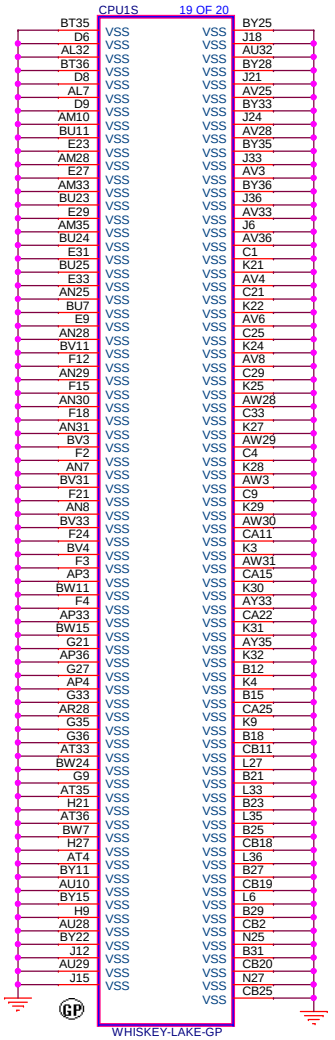
Date: Tuesday, March 03, 2020 | Sheet 22 of 106

Main Func = PCH



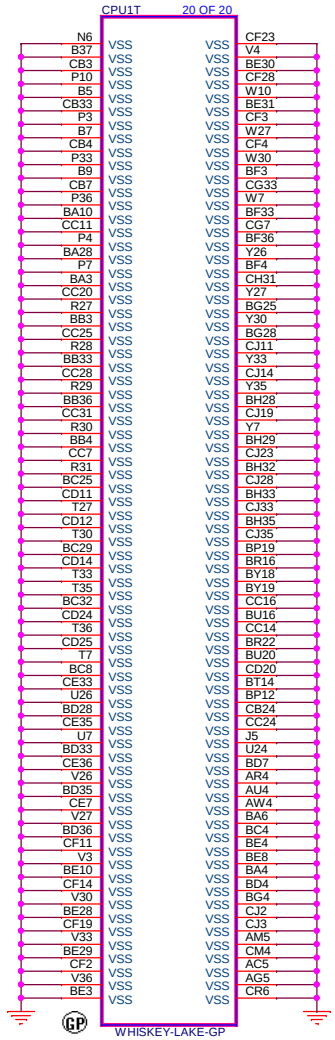
ZZ.00CPU.271

CPU1 will use BOM control to Cometlake-U



ZZ.00CPU.271

CPU1 will use BOM control to Cometlake-U



ZZ.00CPU.271

CPU1 will use BOM control to Cometlake-U

LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

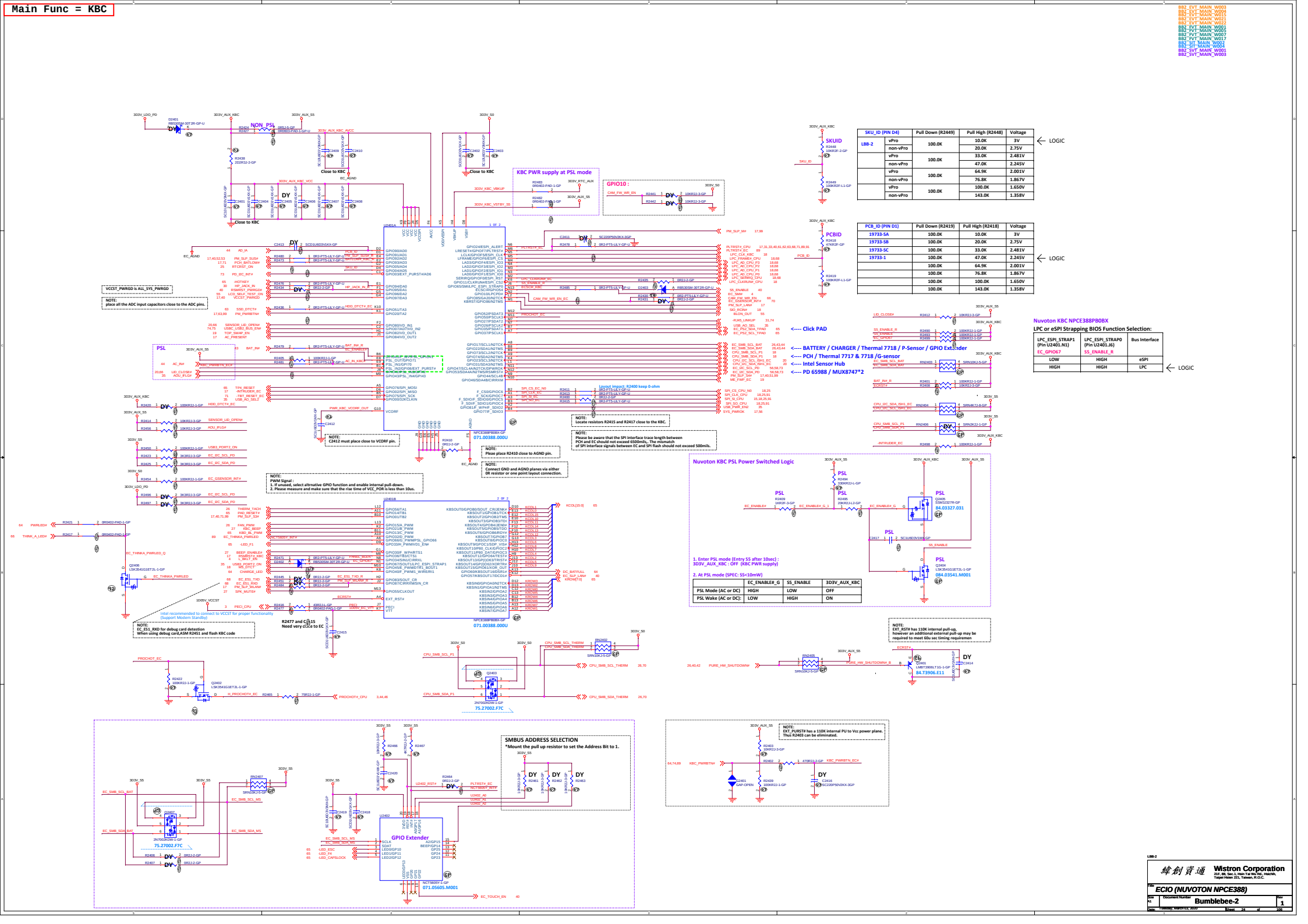
Title: **CPU_(VSS)**

Size	Document Number	Rev
A3	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 23 of 106

Main Func = KBC

B82_EVT_MAIN_W003
B82_EVT_MAIN_W004
B82_EVT_MAIN_W015
B82_EVT_MAIN_W021
B82_EVT_MAIN_W022
B82_PVT_MAIN_W001
B82_PVT_MAIN_W005
B82_PVT_MAIN_W007
B82_PVT_MAIN_W017
B82_SIT_MAIN_W002
B82_SIT_MAIN_W004
B82_SVT_MAIN_W001
B82_SVT_MAIN_W003



Main Func = SPI Flash

18,24 SPI_CS_CPU_N0
18,24,91 SPI_CLK_CPU
15,18,24,91 SPI_SI_CPU
18,24,91 SPI_SO_CPU
15,18 SPI_WP_CPU
15,18 SPI_HOLD_CPU

3D3V_SUS — R2510 0R0603-PAD-1-GP-U — 3D3V_SPI

3D3V_SPI — DY R2519 4K7R2J-2-GP

SPI ROM (BIOS1)

BIOS1 — LILY-BIOS-COLAY-GP-U

SPI_CS_CPU_N0		S#	
SPI_SO_CPU	R2506 0R2J-2-GP	DQ1	SPI_SO_ROM
SPI_WP_CPU	R2507 0R2J-2-GP	W#/VPP	SPI_WP_ROM
		VSS	
		GND	
		VCC	
SPI_HOLD_ROM	R2503 0R2J-2-GP	HOLD#	SPI_HOLD_CPU
SPI_CLK_ROM	R2508 0R2J-2-GP	C	SPI_CLK_CPU
SPI_SI_ROM	R2509 0R2J-2-GP	DQ0	SPI_SI_CPU

ZZ.00PAD.M41

BIOS1 will use BOM control by co-lay symbol issue (WINBOND had load code issue)

208MIL SOIC8 (BIOS1) WSON8 / SOP8:

		32MB (256Mb) non-vPro	32MB (256Mb) vPro	
~~WINBOND~~	~~W25Q256JVEIQ~~	~~072.25256.0N01~~	~~072.25256.0P01~~	~~(W5QN8)~~
MACRONIX	MX25L25673GM2I-08G	072.25673.0001	072.25673.0C01	(SOP8)
GIGADEVICE	GD25B256DYIGR	072.25256.0B03	072.25256.0C03	(WSON8)
MICRON	MT25QL256ABA1EW9-0SIT	072.25256.0E03	072.25256.0D03	(WPDFN8)

SPI ROM Socket (SSKT1)

SSKT1 — SKT-50960-0084L-001-GP

SPI_CS_CPU_N0	1	8	SPI_HOLD_ROM
SPI_SO_ROM	2	7	SPI_CLK_ROM
SPI_WP_ROM	3	6	SPI_SI_ROM
	4	5	

3D3V_SPI — C2502 SCD1U6D3V1KX-GP

62.10076.051
Co-Layout Design on BIOS1
SPI socket mount in SA stage
SOP 8 package only

Main Func = RTC

18,99 RTC_RST#
18 SRTC_RST#
20 RTC_DET#
19 RTC_TEST
24 RTCRST_ON

3D3V_AUX_S5 — R2514 100R2J-2-GP — 3D3V_AUX_R — D2502 RB530SM-30T2R-GP-U — DY R2515 33K2R2F-GP

RTC CONN

RTC1 — ACES-CON2-20-GP-U
20.F1639.002

3D3V_RTC_VCC — R2501 1KR2J-1-GP — 3D3V_RTC_R — D2501 RB530SM-30T2R-GP-U

3D3V_RTC_AUX — DY C2504 SC1U6D3V1MX-GP

RN2501 SRN20KJ-1-GP

C2501 SC1U10V2KX-1GP
C2503 SC1U10V2KX-1GP

SRTC_RST# — RTC_RST#

G2501 GAP-OPEN

Q2503 LSK3541G1ET2L-1-GP — RTCRST_ON — R2520 10KR2J-3-GP

ED2501 DY — AZ1043-04F-R7G-GP

RTC_RST#	8	10	RTC_RST#
SRTC_RST#	2	9	SRTC_RST#
	4	7	
	5	6	

Near RTC CONN (RTC1)

3D3V_RTC_VCC — AFTP2501 AFTE14P-GP — AFTP2502 AFTE14P-GP

(#514849)
Layout: Place at the open door area.

3D3V_RTC_R — Q2502 LSK3541G1ET2L-1-GP — Detect Low — RTC_DET# — R2513 100KR2J-1-GP

3D3V_S0 — R2512 100KR2J-1-GP — 5V_S0

Test High — RTC_TEST — Q2501 LSK3541G1ET2L-1-GP — RTC_DET#_G — R2511 10KR2J-L-GP

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	FLASH/RTC		
Size A3	Document Number Bumblebee-2		Rev 1
Date: Tuesday, March 03, 2020	Sheet 25 of 106		

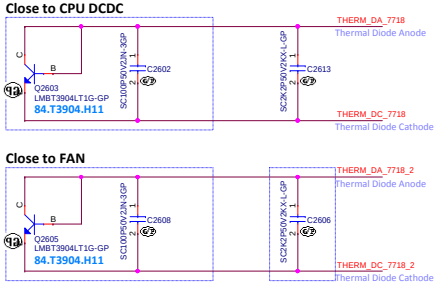
Main Func = Thermal Sensor

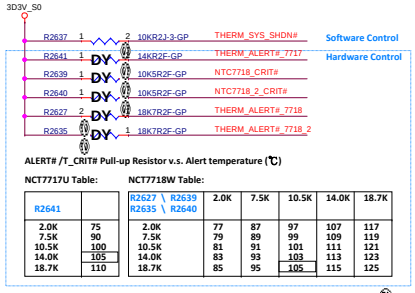
Thermal Sensor

BB2_EVT_MAIN_W016
BB2_EVT_MAIN_W017
BB2_SVT_MAIN_W003

TABLE:

Sensor	Target
U2603	DIMM
U2604	Charger
U2601	SSD
Q2603	CPU DCDC
Q2605	FAN





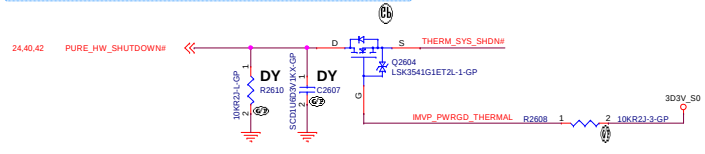
ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)

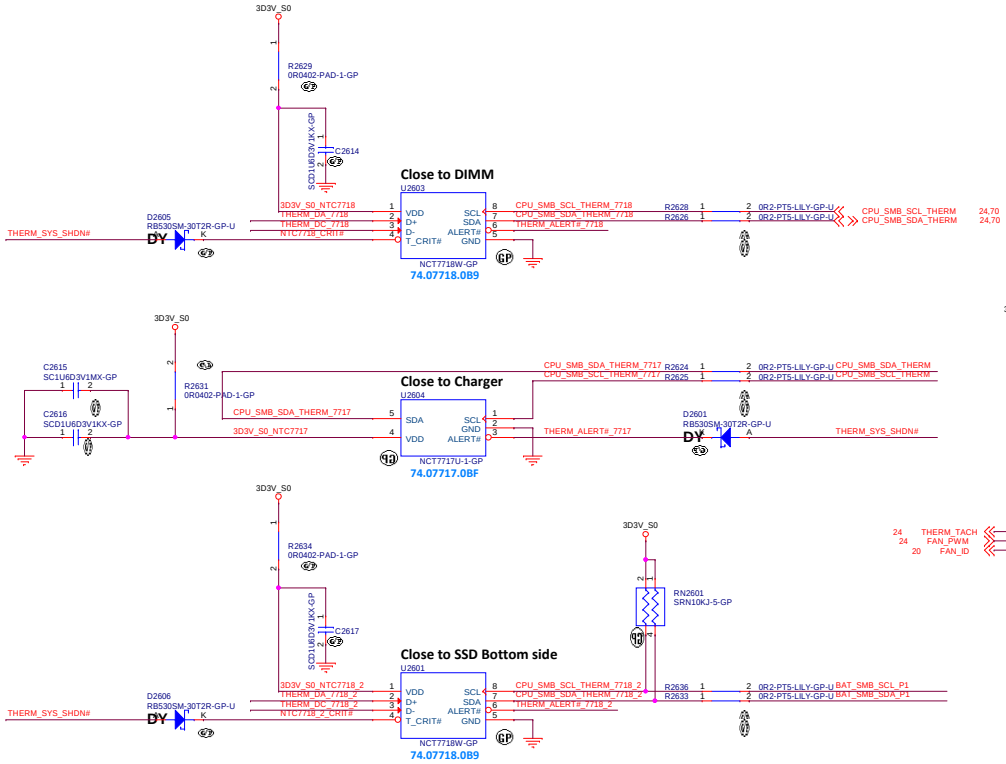
NCT7717U Table:

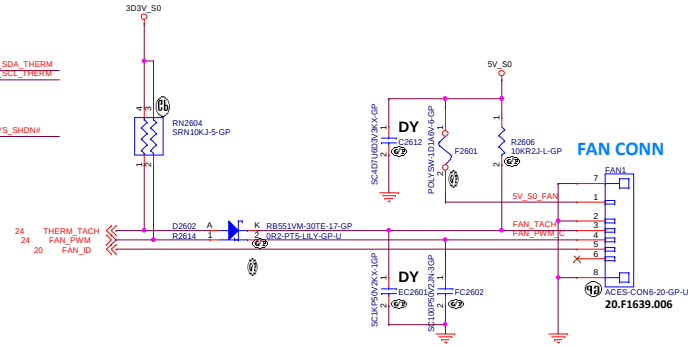
R2641	
2.0K	75
7.5K	90
10.5K	100
14.0K	105
18.7K	110

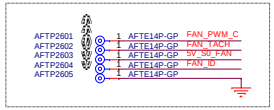
NCT7718W Table:

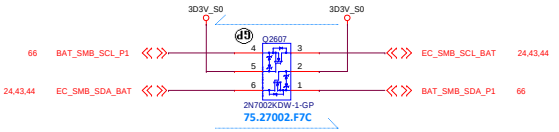
R2627 \ R2639 R2635 \ R2640	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125









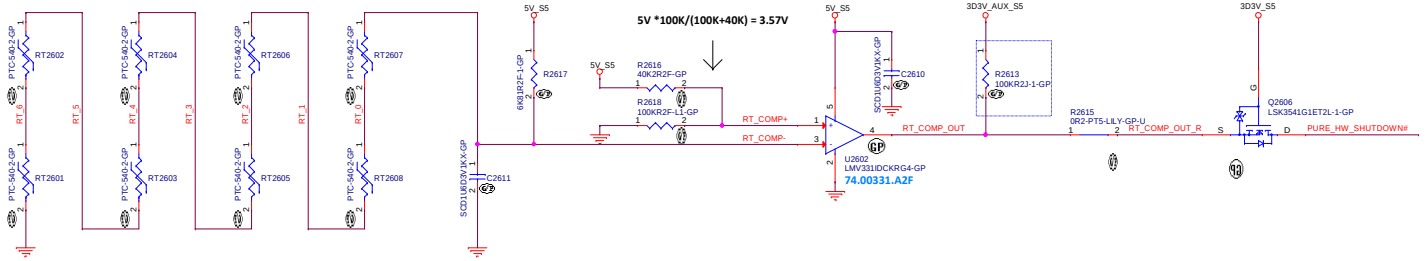


PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

TABLE:

ID	Target	Function
RT2601	PU5101	1D2V_S3
RT2602	PU4801	1V_VCCGT
RT2603	PQ5201	1D05V_SUS
RT2604	PU4701	1V_CPU_CORE
RT2605	PQ4505	5V_S5
RT2606	PQ4506	3D3V_S5
RT2607	PU4404	Charger-Buck
RT2608	PU4406	Charger-Boost



LBB-2

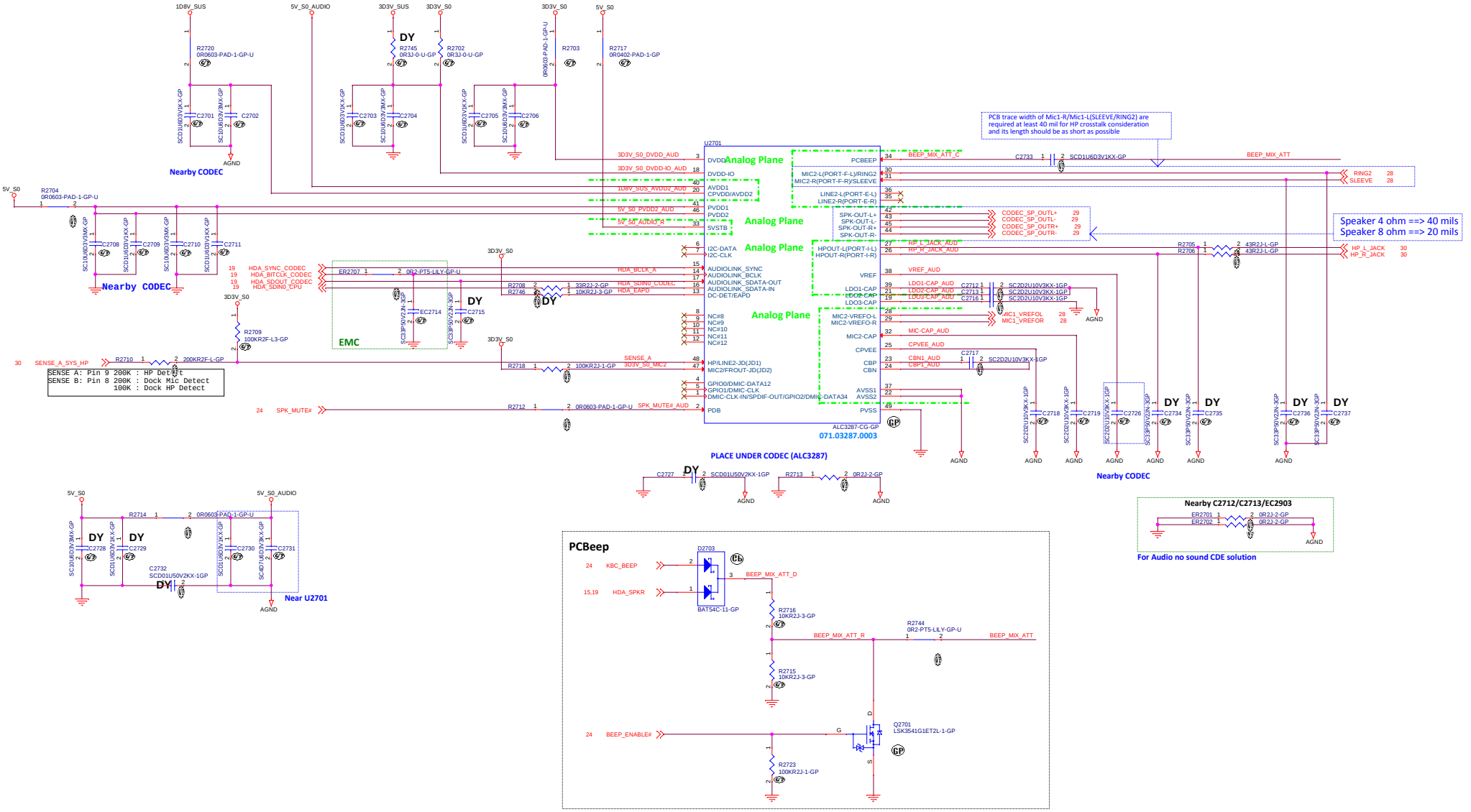
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **INT IO (THERMAL/FAN)**

Size: A2 | Document Number: **Bumblebee-2** | Rev: 1

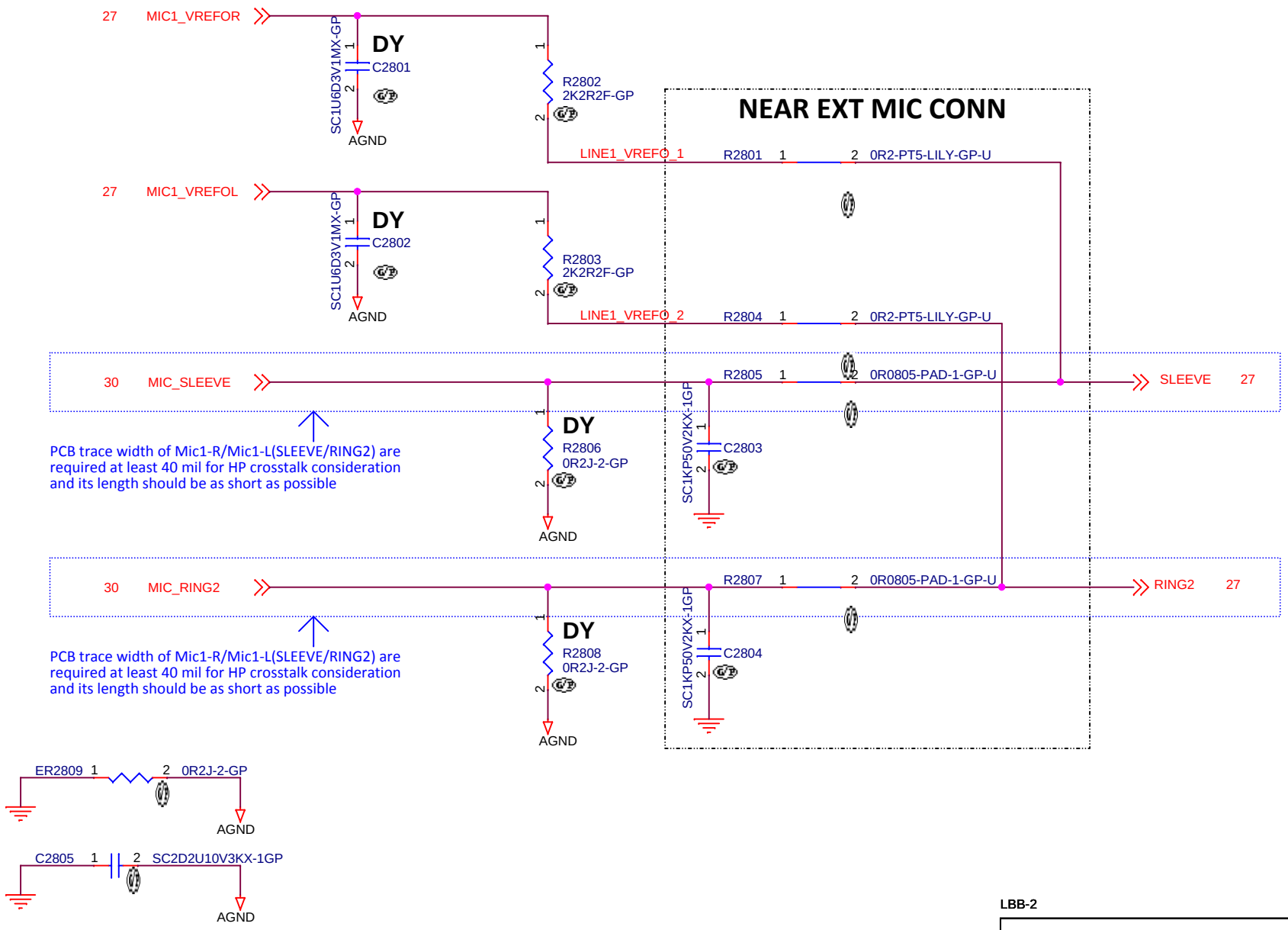
Date: Tuesday, March 03, 2020 | Sheet 26 of 106

BB2_EVT_MAIN_W002
BB2_SVT_MAIN_W002
BB2_SVT_MAIN_W003



LBB-2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO (CODEC ALC3287)		
Size: Custom	Document Number: Bumblebee-2	Rev: 1
Date: Tuesday, March 03, 2020	Sheet 27 of 106	



LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

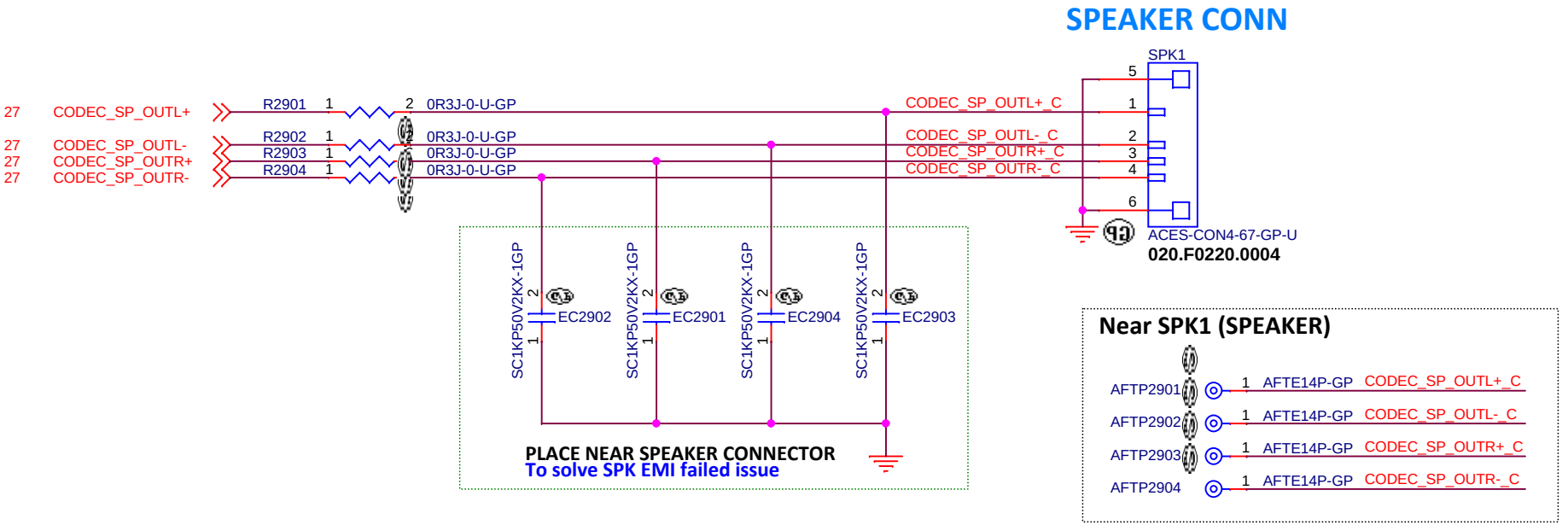
Title: ***AUDIO (MIC I/F)***

Size	Document Number	Rev
A4	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 28 of 106

Main Func = AUDIO

BB2_SVT_MAIN_W003



LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (SPEAKER)***

Size	Document Number	Rev
A4	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 29 of 106

BB2_EVT_MAIN_W005
BB2_SVT_MAIN_W003

NEAR AUDIO JACK CONN

27 HP_L_JACK → L3001 1 BLM15BD182SN1D-GP 68.00084.G21
27 HP_R_JACK → L3002 1 BLM15BD182SN1D-GP 68.00084.G21
DY C3002 SC100P50V2JN-L-GP
DY C3003 SC100P50V2JN-L-GP
Moat

AUDIO JACK SENSE
CLOSE TO CODEC
6-10 mil trace recommend

HGNDA/HGNDB trace width >70mil, changed to sharp will be better.

3D3V_S0 → R3001 10KR2J-3-GP

Combo Jack
AUD1
3 MIC_RING2
1 HP_L_JACK_CONN
5 3D3V_S0_HPJD
6 HP_JACK_SYS
2 HP_R_JACK_CONN
4 MIC_SLEEVE
MS
Audio(IP/NK_comb)
AUDIO-JK687-GP
ZZ.00SKT.022
AGND
AUD1 will use BOM control to 022.10002.01H1

MIC_RING2 → MIC_RING2 28
HP_L_JACK_CONN
HP_JACK_SYS → R3005 1 2 0R2-PT5-LILY-GP-U → HP_JACK_IN 24
HP_R_JACK_CONN
MIC_SLEEVE → MIC_SLEEVE 28

EMC ED3001 AZ5125-02S-R7G-GP 75.05125.07D Close to AUD1
SC1KP50V2KX-1GP EC3006
DY SC1KP50V2KX-1GP EC3007
EMC ED3002 AZ5125-02S-R7G-GP 75.05125.07D Close to AUD1
EMC ED3003 AZ5125-02S-R7G-GP 75.05125.07D Close to AUD1
Moat

R3006 1 2 0R2J-2-GP
AGND
DY
EC3005 1 2 SC1KP50V2KX-1GP
AGND
Moat

Near AUD1 (AUDIO)

AFTP3001 1 AFTE14P-GP MIC_RING2
AFTP3002 1 AFTE14P-GP HP_L_JACK_CONN
AFTP3003 1 AFTE14P-GP 3D3V_S0_HPJD
AFTP3004 1 AFTE14P-GP HP_JACK_SYS
AFTP3005 1 AFTE14P-GP HP_R_JACK_CONN
AFTP3006 1 AFTE14P-GP MIC_SLEEVE
AFTP3007 1 AFTE14P-GP
AGND

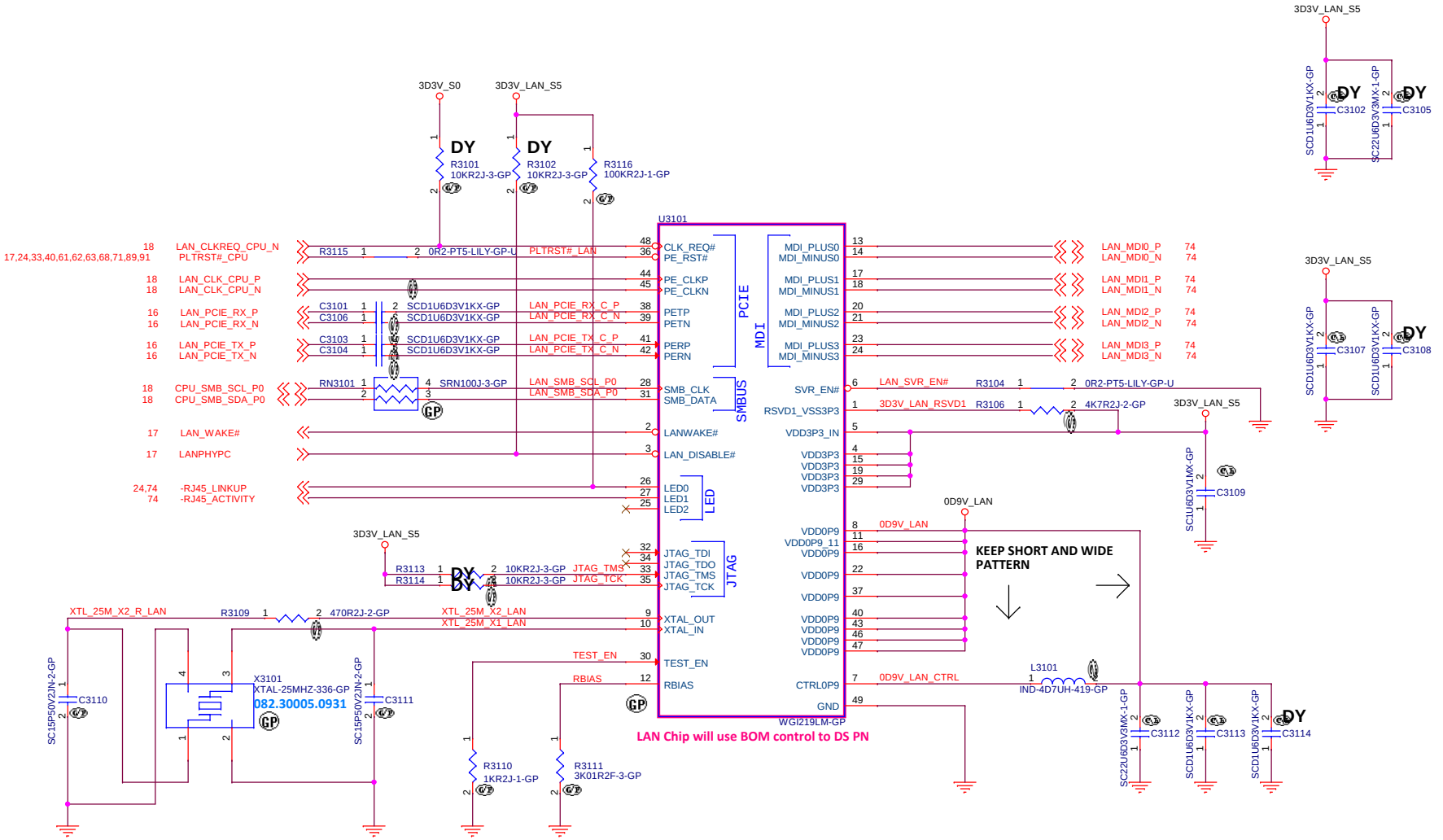
AUDIO JACK SENSE

SENSE_A_SYS_HP 27
HP_JACK_SYS → R3002 22KR2J-GP 1 2 → HP_JACK_SYS_R
Q3001 LSK3541G1ET2L-1-GP (G, D, S)
R3010 100KR2J-1-GP
C3001 SC2D2U10V3KX-1GP
AGND
AGND

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO (AUDIO JACK)
Size: A3 | Document Number: Bumblebee-2 | Rev: 1
Date: Tuesday, March 03, 2020 | Sheet 30 of 106



25MHz (X3101)

TXC	7R25000008	082.30005.0931
HARMONY	X2V025000DC1H-HU	082.30005.0A81
MURATA	XRCGB25M000F2P40R0	082.30005.0911

LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN (GIGA_WGI219LM)***

Size	Document Number	Rev
A3	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 31 of 106

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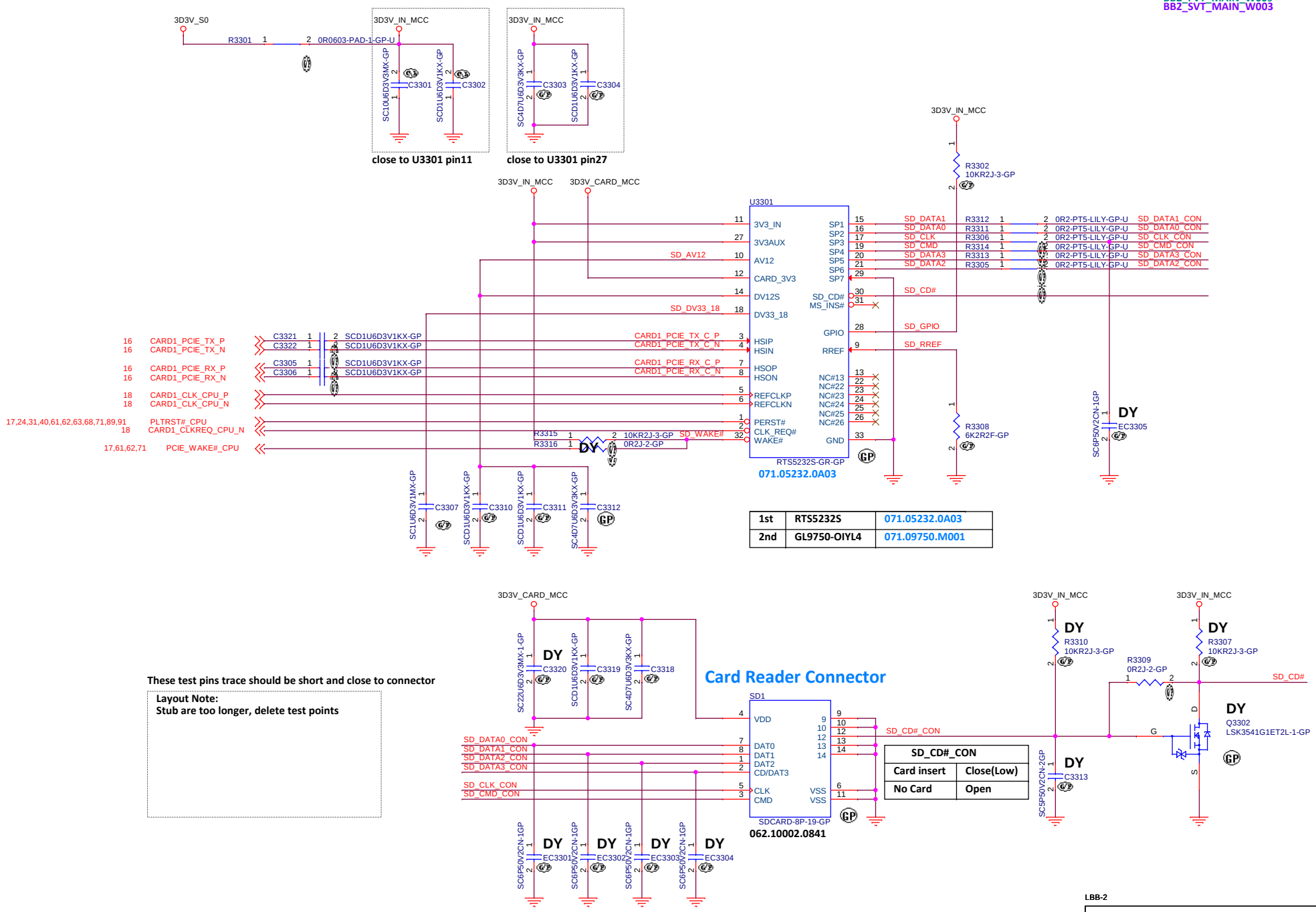
LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***LAN (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 32 of 106



1st	RTS5232S	071.05232.0A03
2nd	GL9750-OIYL4	071.09750.M001

These test pins trace should be short and close to connector

Layout Note:
Stub are too longer, delete test points

SD_CD#_CON	
Card insert	Close(Low)
No Card	Open

LBB-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD READER (SDIO/CONN)**

Size	Document Number	Rev
A3	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 33 of 106

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LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

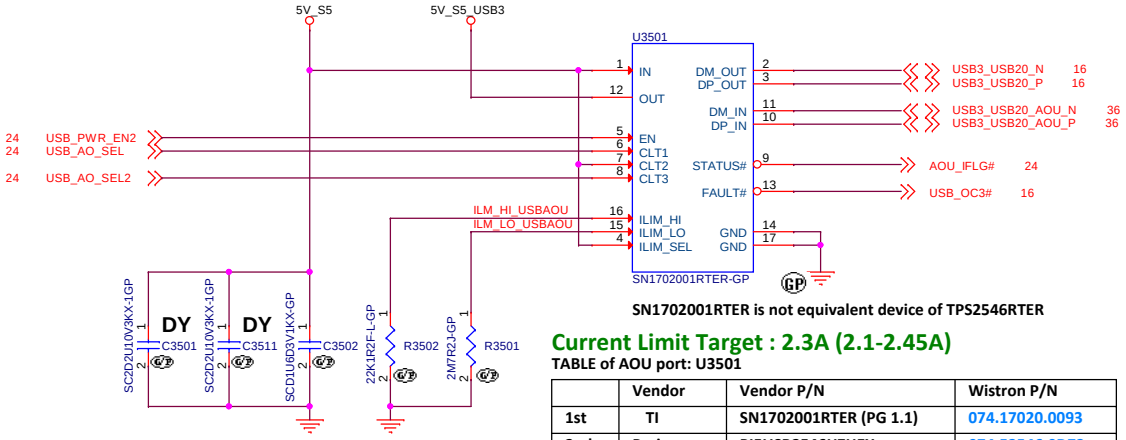
Title: ***USB (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 34 of 106

Main Func = USB Charger

For USB3.0 System Port3 (For AOU)



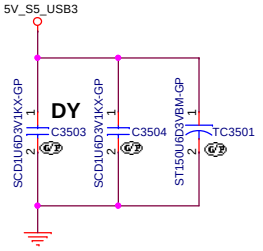
SN1702001RTER is not equivalent device of TPS2546RTER

Current Limit Target : 2.3A (2.1-2.45A)

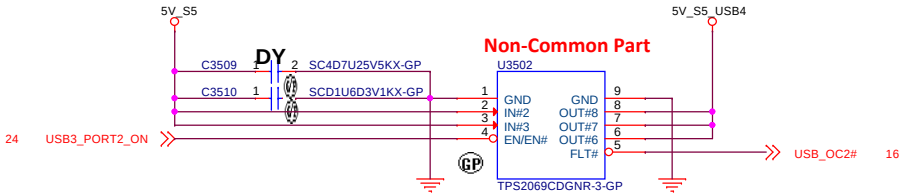
TABLE of AOU port: U3501

	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER (PG 1.1)	074.17020.0093
2nd	Pericom	PI5USB2546HZHEX	074.52546.0D73

Layout Note: Close USB3.0 Port3



For USB3.0 System Port4

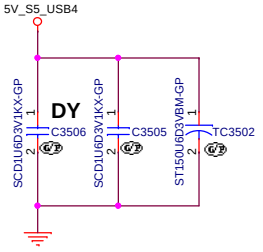


Continous Current Limit 1.5A

TABLE of USB 3.0 port: U3502

	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGNR	074.02069.M001
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G

Layout Note: Close USB3.0 Port4



LBB-2

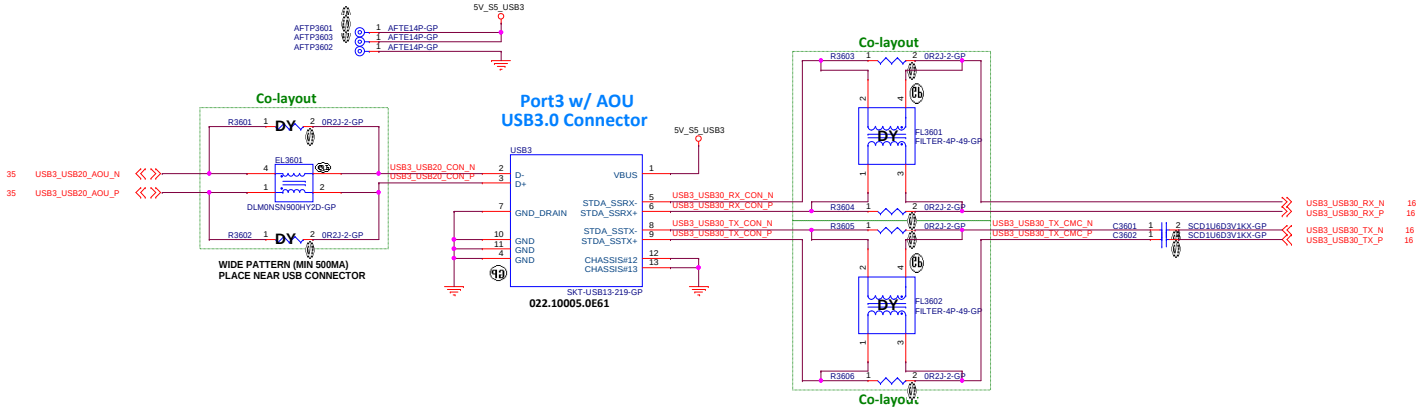
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

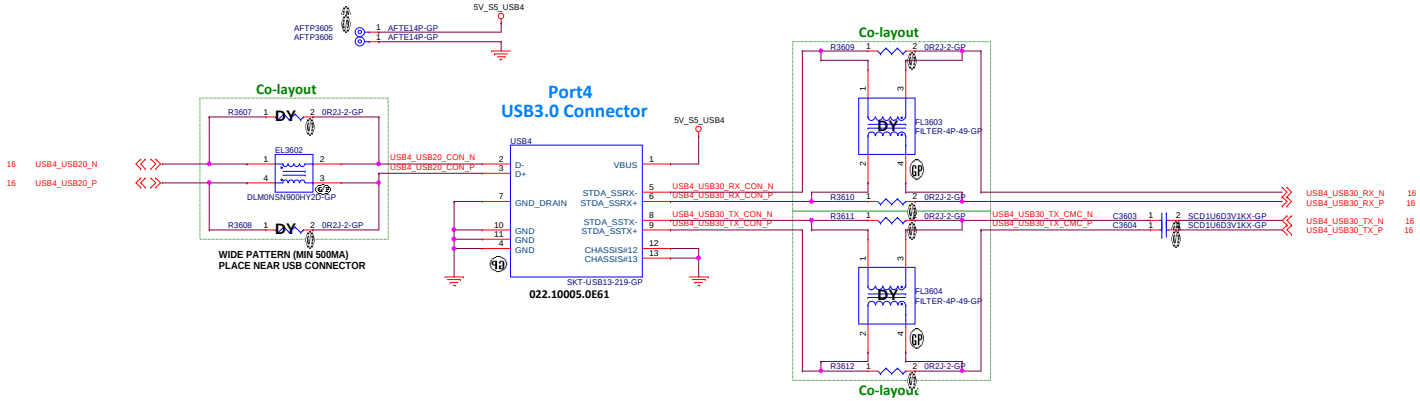
Title: USB (CHARGER/SWITCH)

Size	Document Number	Rev
A3	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 35 of 106

Main Func = USB3.0 Port3 w/ AOU
Main Func = USB3.0 Port4





LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB (USB3.0 CONN)**

Size	Document Number	Rev
A2	Bumblebee-2	1

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 37 of 106

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LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 38 of 106

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LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SEQUENCE (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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BB2_EVT_MAIN_W003
BB2_EVT_MAIN_W009
BB2_EVT_MAIN_W010
BB2_EVT_MAIN_W021
BB2_EVT_MAIN_W007
BB2_SVT_MAIN_W003

Run Power

3D3V_S0 — 3D3V_S0 Comsumption — Peak current 2.5A
5V_S0 — 5V_S0 Comsumption — Peak current 5A

3D3V_SUS — 3D3V_SUS Comsumption — Peak current x.xA

3D3V_LAN_S5 — 3D3V_LAN_S5 Comsumption — Peak current x.xA

1D05V_VCCST — 60mA
1D05V_VCCIO — 3.6A
1D05V_VCCSTG — 120mA
1D2V_VCCSFR_OC — 120mA

Power Good

[#543016] Optional, Added for addition system robustness

3D3V_S0_TOUCH

24,26,42 PURE_HW_SHUTDOWN#
51 VDDQ_PWRGD
17,24 VCCST_PWRGD
17,99 PM_SLP_S0#
17,24,71,99 PM_SLP_S3#
17,24,51,99 PM_SLP_S4#
21 CPU_C10_GATE#
17,24,52,53 PM_SLP_SUS#
24 EC_SLP_LAN#
24 EC_TOUCH_EN
20 CPU_TOUCH_EN
3,62,63,68,71,89,91 PLTRST#_CPU
17 H_THERMTRIP_EN
24 S5_ENABLE
45 PWR_3D3V_EN
45 PWR_5V_EN
3 THERMTRIP#_EC
24 RSMRST_PWRGD#
46 VR_EN
46 VR_RDY
17 RESET_OUT#
52 1D05V_SUS_PWRGD
52,53 1D8V_SUS_PWRGD
17,45,52,53 3V_5V_PWRGD

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LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***SEQUENCE (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-2**	**1**

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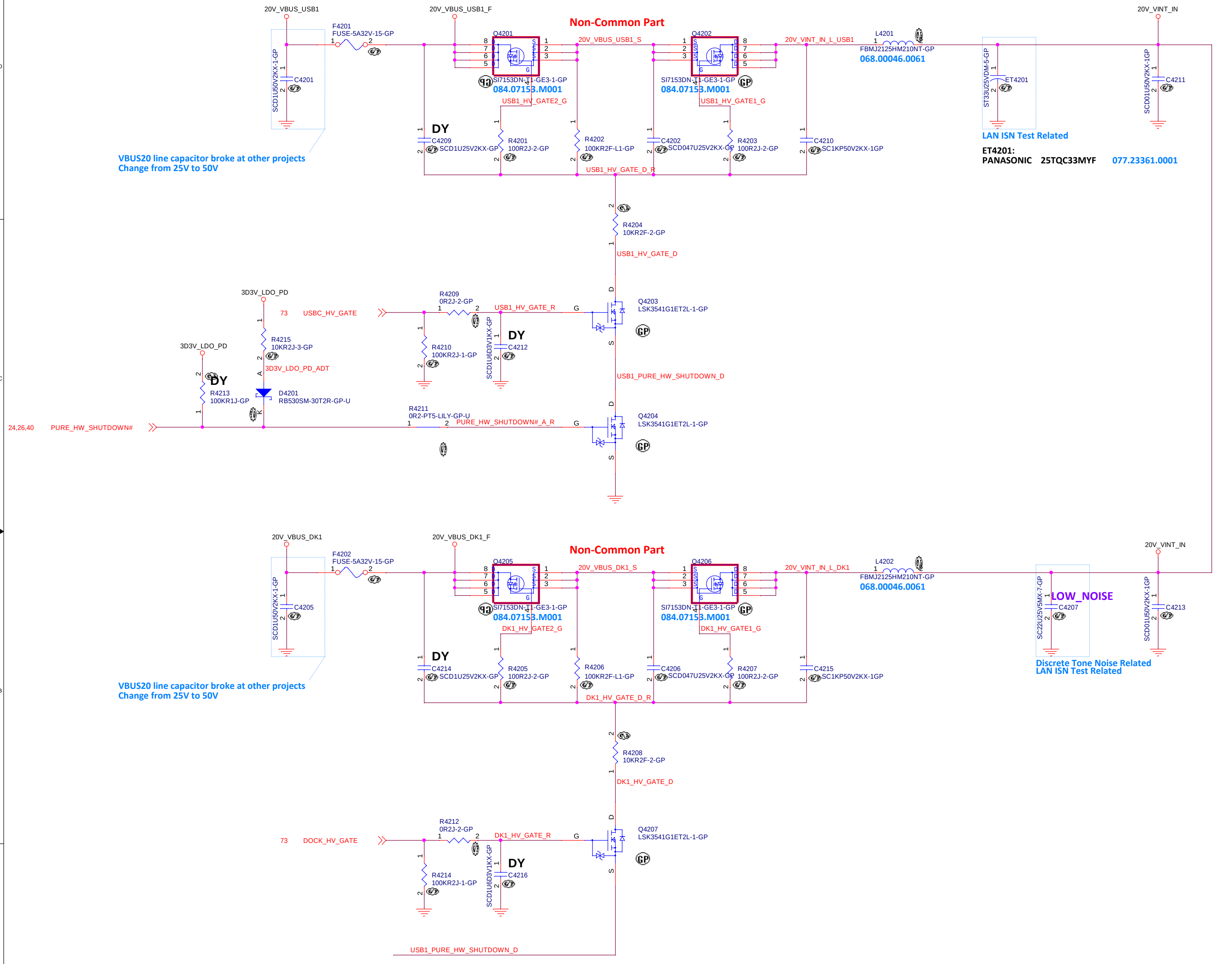
Q4201, Q4202, Q4205, Q4206

1st	VISHAY	SI7153DN-T1-GE3	084.07153.M001	
2nd	AOS	AONR21357	084.21357.0A37	
	~~AOS~~	~~AON7409~~	~~084.07409.M001~~	EOL soon
	~~FAIRCHILD~~	~~FDMC6679AZ~~	~~084.06679.M001~~	had supply issue (OBS part)


Non-Common Part
20V_VBUS_USB1
20V_VBUS_USB1_F
F4201
FUSE-5A32V-15-GP
C4201
SCD1U50V2KX-1-GP
Q4201
SI7153DN-T1-GE3-1-GP
084.07153.M001
20V_VBUS_USB1_S
Q4202
SI7153DN-T1-GE3-1-GP
084.07153.M001
20V_VINT_IN_L_USB1
L4201
FBMJ2125HM210NT-GP
068.00046.0061
20V_VINT_IN
USB1_HV_GATE2_G
USB1_HV_GATE1_G
DY
C4209
SCD1U25V2KX-GP
R4201
100R2J-2-GP
R4202
100KR2F-L1-GP
C4202
SCD047U25V2KX-GP
R4203
100R2J-2-GP
C4210
SC1KP50V2KX-1GP
USB1_HV_GATE_D_R
ET4201
ST33U25VDM-5-GP
C4211
SCD01U50V2KX-1GP
LAN ISN Test Related
ET4201:
PANASONIC 25TQC33MYF 077.23361.0001
VBUS20 line capacitor broke at other projects
Change from 25V to 50V
R4204
10KR2F-2-GP
USB1_HV_GATE_D
3D3V_LDO_PD
73 USBC_HV_GATE
R4209
0R2J-2-GP
USB1_HV_GATE_R
Q4203
LSK3541G1ET2L-1-GP
R4215
10KR2J-3-GP
R4210
100KR2J-1-GP
C4212
SCD1U6D3V1KX-GP
3D3V_LDO_PD_ADT
D4201
RB530SM-30T2R-GP-U
R4213
100KR1J-GP
USB1_PURE_HW_SHUTDOWN_D
R4211
0R2-PT5-LILY-GP-U
24,26,40 PURE_HW_SHUTDOWN#
PURE_HW_SHUTDOWN#_A_R
Q4204
LSK3541G1ET2L-1-GP
20V_VBUS_DK1
20V_VBUS_DK1_F
F4202
FUSE-5A32V-15-GP
C4205
SCD1U50V2KX-1-GP
Q4205
SI7153DN-T1-GE3-1-GP
084.07153.M001
20V_VBUS_DK1_S
Q4206
SI7153DN-T1-GE3-1-GP
084.07153.M001
20V_VINT_IN_L_DK1
L4202
FBMJ2125HM210NT-GP
068.00046.0061
C4207
SC22U25V5MX-7-GP
LOW_NOISE
C4213
SCD01U50V2KX-1GP
Discrete Tone Noise Related
LAN ISN Test Related
DK1_HV_GATE2_G
DK1_HV_GATE1_G
C4214
SCD1U25V2KX-GP
R4205
100R2J-2-GP
R4206
100KR2F-L1-GP
C4206
SCD047U25V2KX-GP
R4207
100R2J-2-GP
C4215
SC1KP50V2KX-1GP
DK1_HV_GATE_D_R
R4208
10KR2F-2-GP
DK1_HV_GATE_D
73 DOCK_HV_GATE
R4212
0R2J-2-GP
DK1_HV_GATE_R
Q4207
LSK3541G1ET2L-1-GP
R4214
100KR2J-1-GP
C4216
SCD1U6D3V1KX-GP
USB1_PURE_HW_SHUTDOWN_D

LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	INT IO (DC-IN)	
Size A2	Document Number: Bumblebee-2	Rev 1
Date: Tuesday, March 03, 2020	Sheet 42 of 106	

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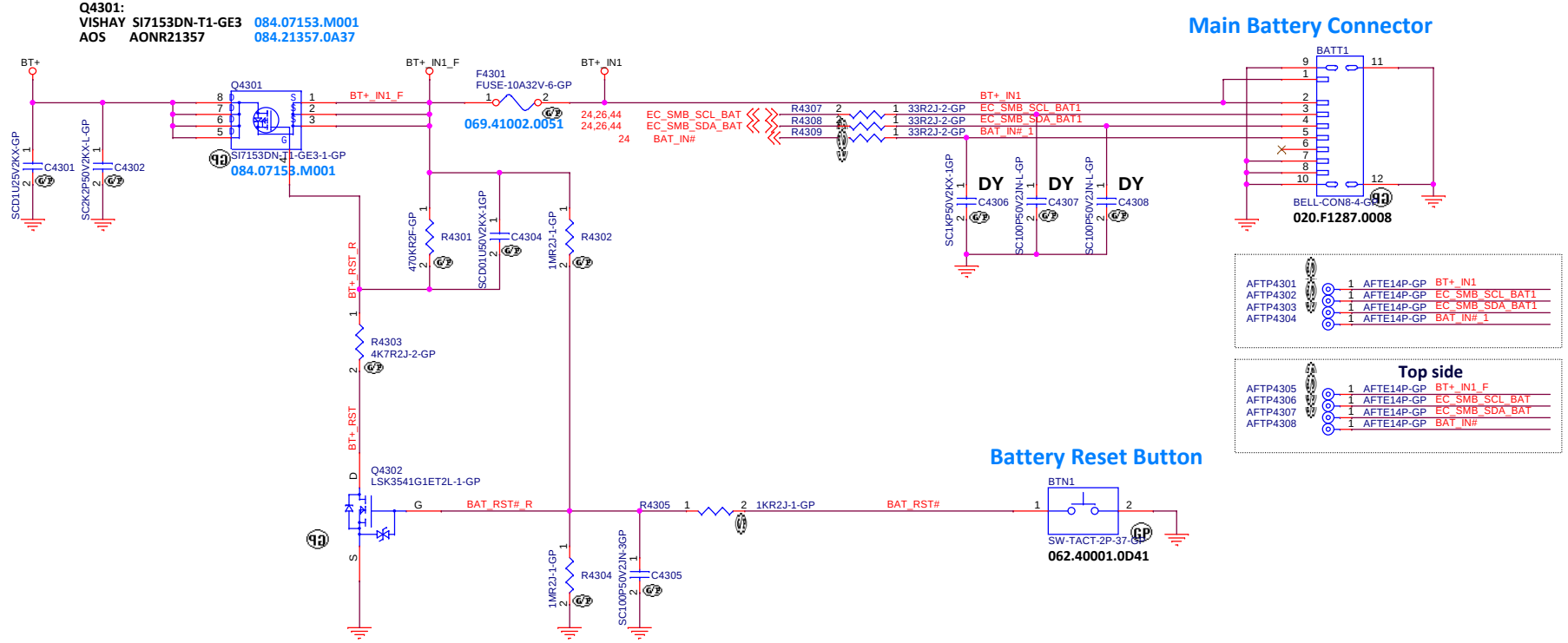

LBB-2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: INT IO (BATT CONN)		
Size: A3	Document Number: Bumblebee-2	Rev: 1
Date: Tuesday, March 03, 2020	Sheet 43 of 106	

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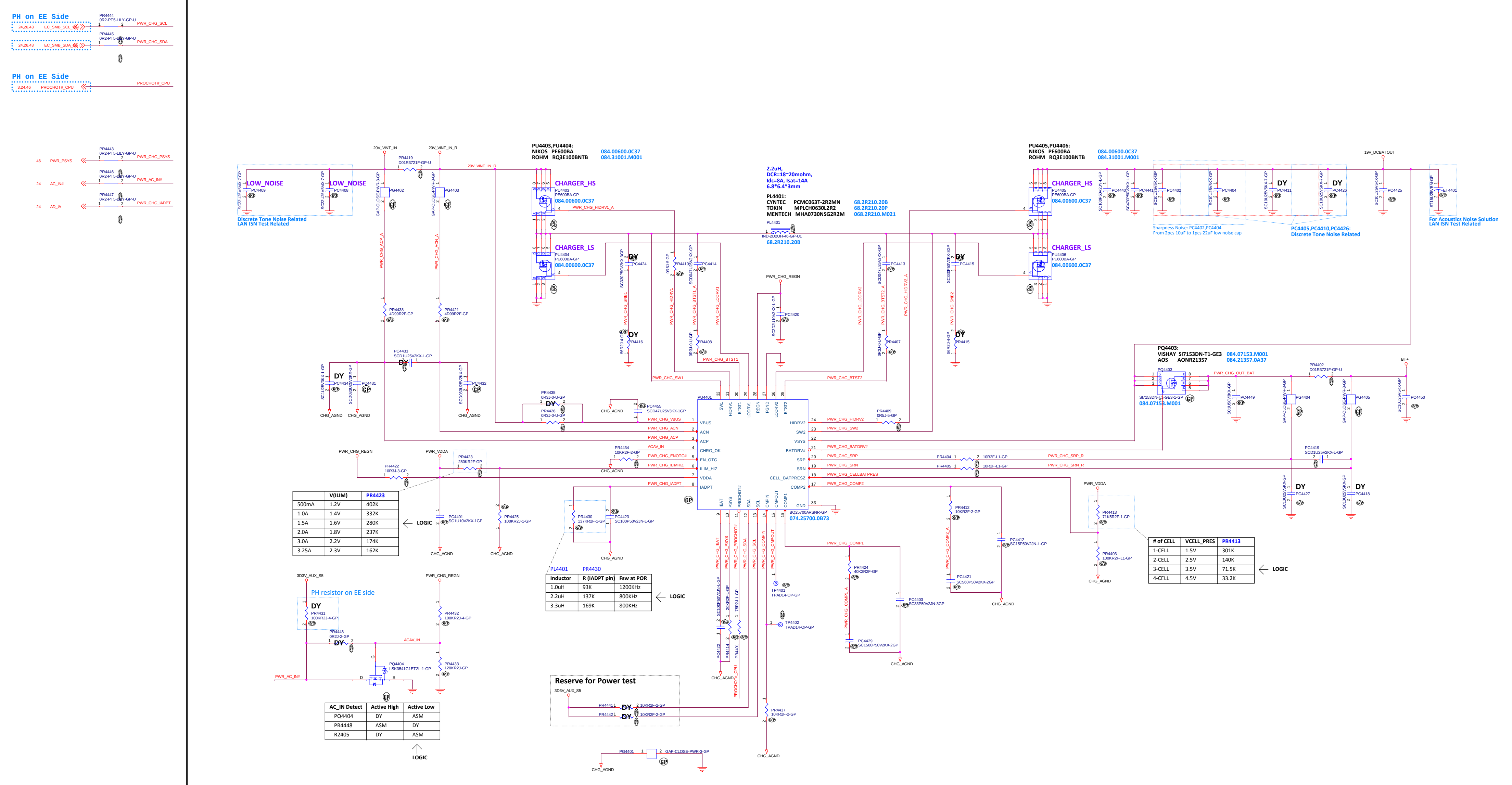


BB2_FVT_MAIN_W010
BB2_FVT_MAIN_W014
BB2_FVT_MAIN_W015
BB2_SIT_MAIN_W010
BB2_SVT_MAIN_W003
BB2_SVT_MAIN_W006
PH on EE Side
EC_SMB_SCL_EC
EC_SMB_SDA_EC
PWR_CHG_SCL
PWR_CHG_SDA
PH on EE Side
PROCHOT#_CPU
PWR_PSYS
AC_IN#
AD_IA
PWR_CHG_PSYS
PWR_AC_IN#
PWR_CHG_IADPT
LOW_NOISE
LOW_NOISE
Discrete Tone Noise Related
LAN ISN Test Related
20V_VINT_IN
20V_VINT_IN_R
PU4403,PU4404:
NIKOS PE600BA 084.00600.0C37
ROHM RQ3E100BNTB 084.31001.M001
CHARGER_HS
CHARGER_LS
2.2uH,
DCR=18~20mohm,
Idc=8A, Isat=14A
6.8*6.4*3mm
PL4401:
CYNTEC PCMC063T-2R2MN 68.2R210.20B
TOKIN MPLCH0630L2R2 68.2R210.20P
MENTECH MHA0730NSG2R2M 068.2R210.M021
PU4405,PU4406:
NIKOS PE600BA 084.00600.0C37
ROHM RQ3E100BNTB 084.31001.M001
19V_DCBATOUT
Sharpness Noise: PC4402,PC4404
From 2pcs 10uF to 1pcs 22uF low noise cap
PC4405,PC4410,PC4426:
Discrete Tone Noise Related
For Acoustics Noise Solution
LAN ISN Test Related
PQ4403:
VISHAY SI7153DN-T1-GE3 084.07153.M001
AOS AONR21357 084.21357.0A37
BT+
PU4401
BQ25700ARSNR-GP
074.25700.0B73
PH resistor on EE side
Reserve for Power test
3D3V_AUX_S5
LOGIC

	V(ILIM)	PR4423
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

LOGIC

PL4401 PR4430

Inductor	R (IADPT pin)	Fsw at POR
1.0uH	93K	1200KHz
2.2uH	137K	800KHz
3.3uH	169K	800KHz

LOGIC

# of CELL	VCELL_PRES	PR4413
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

LOGIC

AC_IN Detect	Active High	Active Low
PQ4404	DY	ASM
PR4448	ASM	DY
R2405	DY	ASM

LOGIC

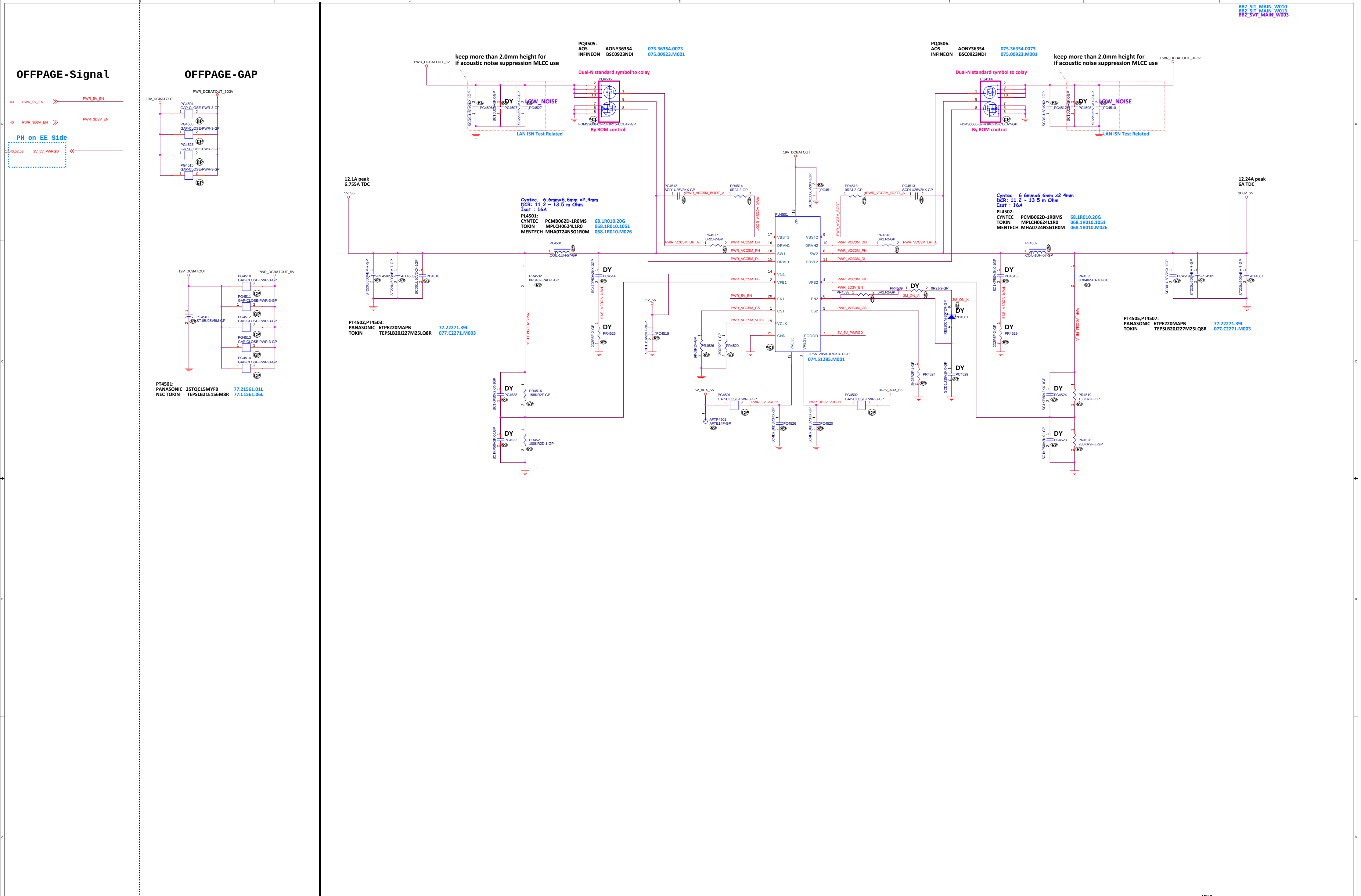
LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER (CHARGER_BQ25700ARSNR)**

Size A1 | Document Number: **Bumblebee-2** | Rev 1

Date: Tuesday, March 03, 2020 | Sheet 44 of 106



BB2_SIT_MAIN_W010
BB2_SIT_MAIN_W013
BB2_SVT_MAIN_W003
OFFPAGE-Signal
PWR_5V_EN
PWR_3D3V_EN
PH on EE Side
3V_5V_PWRGD
OFFPAGE-GAP
19V_DCBATOUT
PWR_DCBATOUT_3D3V
PWR_DCBATOUT_5V
GAP-CLOSE-PWR-3-GP
PT4501:
PANASONIC 25TQC15MYFB 77.21561.01L
NEC TOKIN TEPSLB21E156M8R 77.C1561.06L
PQ4505:
AOS AONY36354 075.36354.0073
INFINEON BSC0923NDI 075.00923.M001
keep more than 2.0mm height for
if acoustic noise suppression MLCC use
Dual-N standard symbol to colay
LOW_NOISE
LAN ISN Test Related
FDMS3600-02-RJK0215-COLAY-GP
By BOM control
PQ4506:
AOS AONY36354 075.36354.0073
INFINEON BSC0923NDI 075.00923.M001
12.1A peak
6.755A TDC
5V_S5
Cyntec. 6.6mmx6.6mm x2.4mm
DCR: 11.2 ~ 13.5 m Ohm
Isat : 16A
PL4501:
CYNTEC PCMB062D-1R0MS 68.1R010.20G
TOKIN MPLCH0624L1R0 068.1R010.1051
MENTECH MHA0724NSG1R0M 068.1R010.M026
PT4502,PT4503:
PANASONIC 6TPE220MAPB 77.22271.39L
TOKIN TEPSLB20J227M25LQ8R 077.C2271.M003
12.24A peak
6A TDC
3D3V_S5
Cyntec. 6.6mmx6.6mm x2.4mm
DCR: 11.2 ~ 13.5 m Ohm
Isat : 16A
PL4502:
CYNTEC PCMB062D-1R0MS 68.1R010.20G
TOKIN MPLCH0624L1R0 068.1R010.1051
MENTECH MHA0724NSG1R0M 068.1R010.M026
PT4505,PT4507:
PANASONIC 6TPE220MAPB 77.22271.39L
TOKIN TEPSLB20J227M25LQ8R 077.C2271.M003
PU4501
TPS51285B-1RUKR-1-GP
074.51285.M001
VBST1 DRVH1 SW1 DRVL1 VO1 VFB1 EN1 CS1 VCLK GND VIN VBST2 DRVH2 SW2 DRVL2 VFB2 EN2 CS2 PGOOD VREG5 VREG3
5V_AUX_S5
3D3V_AUX_S5
PWR_5V_VREG5
PWR_3D3V_VREG3
AFTP4501
DY

LBB-2

Wistron Corporation
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Title	POWER (TPS51285B_5V/3D3V)
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OFFPAGE

40 VR_EN
7 SVID_ALERT#_CPU
7 SVID_CLK_CPU
7 SVID_DATA_CPU
44 PWR_PSYS
8 VCCGT_SENSE
8 VSSGT_SENSE
7 VCCCORE_SENSE
7 VSSCORE_SENSE
8 VCCSA_SENSE
8 VSSSA_SENSE
40 VR_RDY
3,24,44 PROCHOT#_CPU
47,48,50 DRVON
48 1V_VCCGT_PWM_1A
48 1V_VCCGT_SW_1A
48 1V_VCCGT_CSN_1A
47 1V_CPU_CORE_PWM1_2PH
47 1V_CPU_CORE_PWM2_2PH
47 1V_CPU_CORE_CSP1
47 1V_CPU_CORE_CSP2
47 1V_CPU_CORE_CSN1
47 1V_CPU_CORE_CSN2
50 PWR_VCCSA_PWM
50 PWR_VCCSA_CSP
50 PWR_VCCSA_CSN

EE side Link
SVID Pull High V

1D05V_VCCST — PG4602 GAP-CLOSE-PWR-3-GP — PWR_CORE_VCCST

CML U62 V1 15W

	IA	GT	SA
Imax	70A	31A	6A
LL	1.8m	3.1m	10.3m

PLACE NEAR TO PU4501

PLACE CLOSE TO VCCPUCORE PL4702

PLACE CLOSE TO VCCPUCORE PU4701

PLACE CLOSE TO VCCGT PL4802

PLACE CLOSE TO VCCGT PU4801

PLACE CLOSE TO VCCSA PL5001

NCP81218PMNTXG-GP 074.81218.M004

LBB-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (NCP81218P_IMVP8)

Size: A1 | Document Number: Bumblebee-2 | Rev: 1

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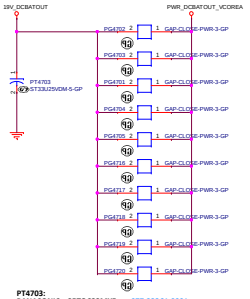
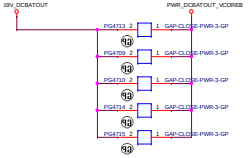


PT4703:
PANASONIC 25TQC33MYF 077.23361.0001



Main Func = CPU_CORE

MLCCs must be placed symmetrically on Top and Bottom.

keep more than 2.0mm height for if acoustic noise suppression MLCC use

Max Current = 3.50(A)

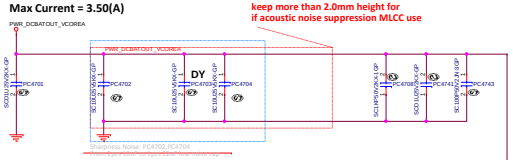
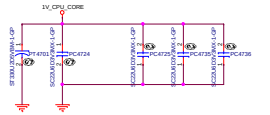


TABLE for PU4701 and PU4702

ON-semi NCP302045

TABLE for PT4701

NEC TOKIN	PSGB20E337M9	80.3371V.A2L
PANASONIC	ETPE330MA9L	077.23371.M001



22uF (0603) x 4 pcs
330uF x 1 pcs

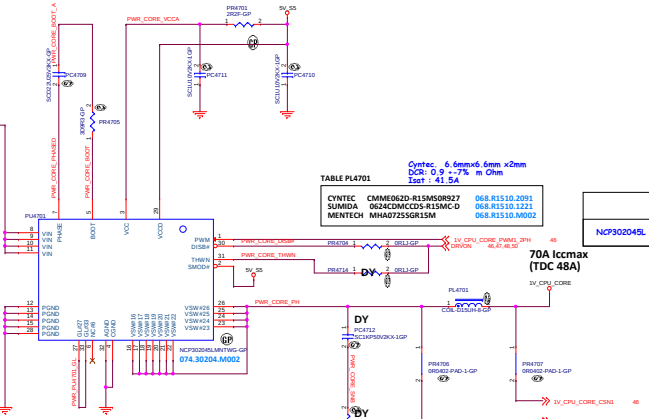


TABLE PL4701

CYNTEC	CMME062D-R15MS0R927	068.R1510.2091
SUMIDA	0624CDMCCDS-R15MC-D	068.R1510.1221
MENTECH	MHA07255GR15M	068.R1510.M002

Cyntec 6.6mmx6.6mm x2mm
DCR: 0.9 +-7% m Ohm
Isat : 41.5A

	PR4704 PR4711	PR4714 PR4721
NCP302045L	0 Ohm	DY

70A Iccmax (TDC 48A)

TABLE PR4703 0603 size

Rohm,	ESR03EZPJ2R2	
Pana,	ERJPA3J2R2V	
YDS,	RN73S2CL-2R20-F	

MLCCs must be placed symmetrically on Top and Bottom.

keep more than 2.0mm height for if acoustic noise suppression MLCC use

Max Current = 3.50(A)

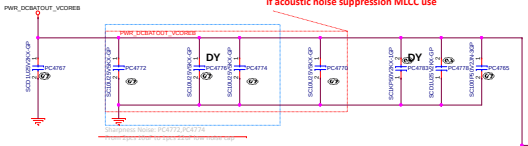
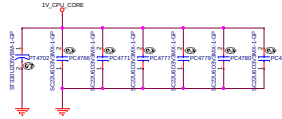


TABLE for PT4702

NEC TOKIN	PSGB20E337M9	80.3371V.A2L
PANASONIC	ETPE330MA9L	077.23371.M001



22uF (0603) x 26 pcs
330uF x 1 pcs

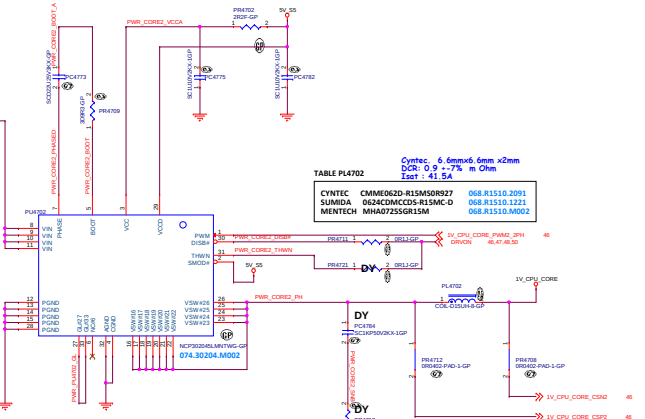


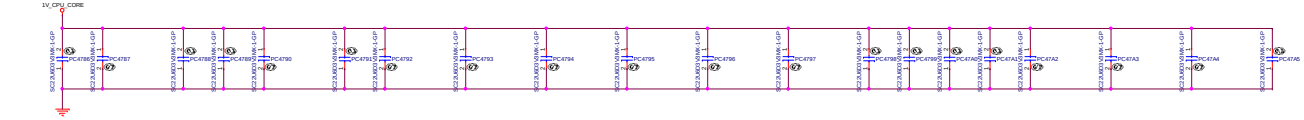
TABLE PL4702

CYNTEC	CMME062D-R15MS0R927	068.R1510.2091
SUMIDA	0624CDMCCDS-R15MC-D	068.R1510.1221
MENTECH	MHA07255GR15M	068.R1510.M002

Cyntec 6.6mmx6.6mm x2mm
DCR: 0.9 +-7% m Ohm
Isat : 41.5A

TABLE PR4710 0603 size

Rohm,	ESR03EZPJ2R2	
Pana,	ERJPA3J2R2V	
YDS,	RN73S2CL-2R20-F	



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Title: POWER (NCP302045L_CPUCORE)

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BB2_FVT_MAIN_W010 BB2_FVT_MAIN_L003
BB2_FVT_MAIN_W014
BB2_SIT_MAIN_W012
BB2_SVT_MAIN_W003
BB2_SVT_MAIN_W006

OFFPAGE

19V_DCBATOUT PWR_DCBATOUT_VCCGTA

PT4802
PANASONIC 25TQC33MYF 077.23361.0001

Main Func = CPU_CORE

MLCCs must be placed symmetrically on Top and Bottom.

Max Current = 3.88(A)

keep more than 2.0mm height for if acoustic noise suppression MLCC use

PWR_DCBATOUT_VCCGTA

DY

Sharpness Noise: PC4802,PC4804 From 2pcs 10uF to 1pcs 22uF low noise cap

Sharpness Noise: PC4805,PC4807 From 2pcs 10uF to 1pcs 22uF low noise cap

PU4801

TABLE for PU4801

ON-semi NCP302045

Cyntec 6.6mmx6.6mm x2mm
DCR: 0.9 +-7% m Ohm
Isat : 41.5A

TABLE PL4802

CYNTEC	CMME062D-R15MS0R927	068.R1510.2091
SUMIDA	0624CDMCCDS-R15MC-D	068.R1510.1221
MENTECH	MHA0725SGR15M	068.R1510.M002

	PR4804	PR4814
NCP302045L	0 Ohm	DY

31A Iccmax (TDC: 18A)

TABLE for PT4801

NEC TOKIN	PSGB20E337M9	80.3371V.A2L
PANASONIC	ETPE330MA9L	077.23371.M001

TABLE PR4803 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

1V_VCCGT

LBB-2

緯創資通 Wistron Corporation
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Title: POWER (NCP302045L_VCCGT)

Size	Document Number	Rev
A2	Bumblebee-2	1

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Main Func = CPU_CORE

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LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 49 of 106

Main Func = CPU_CORE

BB2_FVT_MAIN_W010
BB2_SVT_MAIN_W006

OFFPAGE

19V_DCBATOUT
PWR_DCBATOUT_VCCSA
PG5002 GAP-CLOSE-PWR-3-GP
PG5003 GAP-CLOSE-PWR-3-GP

PU5002,PU5003:
NIKOS PE606BA 084.00606.0037
VISHAY SIS412DN 084.00412.M002

PWR_DCBATOUT_VCCSA
PC5029 SC10U25V5KX-GP
PC5027 SC10U25V5KX-GP
PC5002 SCD1U25V2KX-L-GP

Cyntec 6.6mmx6.6mm x2mm
DCR: 7.3 - 8.4 m Ohm
Isat : 18A
PL5001:
CYNTEC PCMB061H-R47MS 68.R4710.20C
TOKO FDV0620-H-R47M 68.R471A.10D
MENTECH MHA0718NSGR47M 068.R4710.M012

TDC: 4A
Iccmax: 6A
OCP > 6.75A

PR5013 2D2R3-1-U-GP
PWR_VCCSA_BST_RC
PWR_VCCSA_BST
PC5008 SCD22U25V3KX-GP

VCCSA_HS
PU5002 PE606BA-GP 084.00606.0037

PU5001
46 PWR_VCCSA_PWM
46,47,48 DRVON
5V_S5
BST DRVH
PWM SW
EN GND
VCC DRVL
GND
NCP81253MNTBG-1-GP 074.81253.0AE3
PWR_VCCSA_DRVH
PWR_VCCSA_SW
PWR_VCCSA_DRVL
PC5001 SC2D2U10V3KX-L-GP

VCCSA_LS
PU5003 PE606BA-GP 084.00606.0037

PR5014 2D2R5F-2-GP
PWR_VCCSA_SNUB
PC5031 SC1KP50V2KX-1GP
PG5021 GAP-CLOSE-PWR-3-GP

PL5001 IND-D47UH-46-GP
1V_VCCSA
PG5022 GAP-CLOSE-PWR-3-GP

46 PWR_VCCSA_CSP
46 PWR_VCCSA_CSN

LBB-2

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (NCP81253MN_VCCSA)
Size: A3
Document Number: Bumblebee-2
Rev: 1
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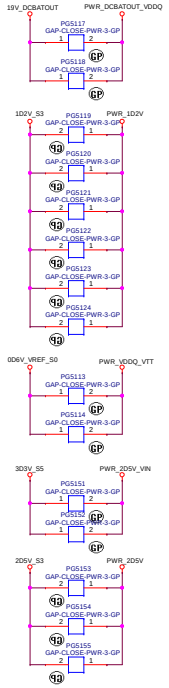
OFFPAGE

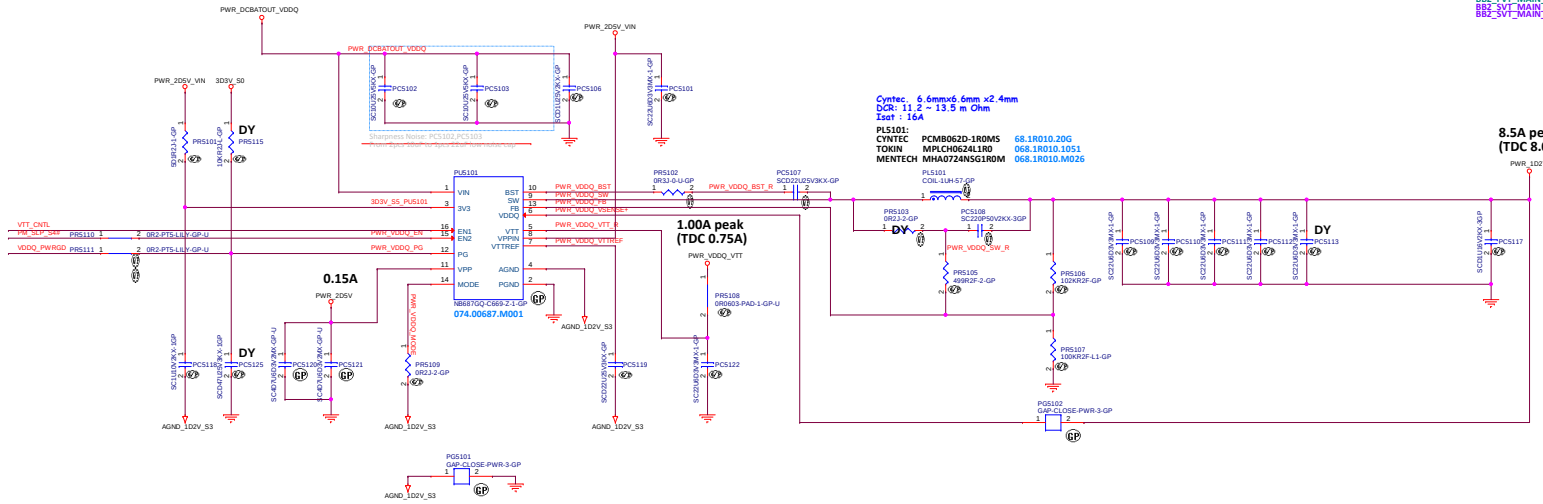
S5
7,24,40,99 PM_SLP_S4#

S3
S VTT_CNTL

PH on EE Side
40 VDDQ_PWRGD

OFFPAGE_GAP





BB2_FVT_MAIN_W010
BB2_FVT_MAIN_W014
BB2_SVT_MAIN_W003
BB2_SVT_MAIN_W006

Table 1: EN1/EN2 Control

State	EN1	EN2	VDDQ	VPP	VTT REF	VTT
S0	High	High	On	On	On	On
S3	Low	High	On	On	On	Off (Hi-Z)
S4/S5	Low	Low	Off	Off	Off	Off
Others	High	Low	Off	Off	Off	Off

Table 2: Mode Selection

State	USM	Fs	Resistor to GND
M1	No	700kHz	0Ω
M2	Yes	700kHz	90kΩ
M3	No	500kHz	150kΩ
M4	Yes	500kHz	>230kΩ or float

LBB-2

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Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (NB687_1D2V/2D5V/0D6V

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Custom	Bumblebee-2	1

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BB2_FVT_MAIN_W010
BB2_FVT_MAIN_W014
BB2_SIT_MAIN_W010
BB2_SIT_MAIN_W012
BB2_SVT_MAIN_W003
BB2_SVT_MAIN_W006

OFFPAGE

PH on EE Side

40 1D05V_SUS_PWRGD — PR5210 0R2-PT5-LILY-GP-U — PWR_1D05V_PG

40,53 1D8V_SUS_PWRGD — PR5211 0R2-PT5-LILY-GP-U — PWR_1D05V_EN

17,24,40,53 PM_SLP_SUS# — PR5212 0R2J-2-GP DY

17,40,45,53 3V_5V_PWRGD — PR5213 0R2J-2-GP DY

OFFPAGE_GAP

19V_DCBATOUT — PWR_DCBATOUT_1D05V

PG5202 GAP-CLOSE-PWR-3-GP
PG5203 GAP-CLOSE-PWR-3-GP
PG5204 GAP-CLOSE-PWR-3-GP
PG5205 GAP-CLOSE-PWR-3-GP

1D05V_SUS — PWR_1D05V

PG5206 GAP-CLOSE-PWR-3-GP
PG5207 GAP-CLOSE-PWR-3-GP
PG5208 GAP-CLOSE-PWR-3-GP
PG5209 GAP-CLOSE-PWR-3-GP
PG5210 GAP-CLOSE-PWR-3-GP
PG5211 GAP-CLOSE-PWR-3-GP
PG5214 GAP-CLOSE-PWR-3-GP
PG5215 GAP-CLOSE-PWR-3-GP
PG5212 GAP-CLOSE-PWR-3-GP
PG5213 GAP-CLOSE-PWR-3-GP

OCP = 18A

3D3V_S5 — PR5202 10KR2J-3-GP DY

PU5201 RT8237CZQW-2-1-GP 074.08237.0B73

PGOOD, CS, EN, FB, RF, GND, BOOT, UGATE, PHASE, VCC, LGATE

PWR_1D05V_PG, PWR_1D05V_CS, PWR_1D05V_EN, PWR_1D05V_FB, PWR_1D05V_RF, PWR_1D05V_BOOT, PWR_1D05V_HG, PWR_1D05V_PH, PWR_1D05V_LG

PR5204 43K2R2F-L-GP
PC5202 SC1K5V2KX-1GP DY
PR5207 470KR2F-GP
PC5206 SC1U10V2KX-L1-GP
PR5201 2D2R3-1-U-GP
PC5205 SCD1U25V2KX-GP
5V_S5

PWM Frequency setting
RF=470K
PWM Freq=290K Hz

R_{RF} (kΩ)	Switching Frequency (kHz)
470kΩ	290
200kΩ	340
100kΩ	380
39kΩ	430

<--- LOGIC

Note : For DEM, connect R_{RF} to GND; for CCM, connect R_{RF} to PGOOD.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is 0.704V (typ.).

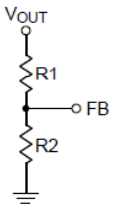

Figure 4. Setting V_{OUT} with a Resistive Voltage Divider

PQ5201
AOS AONY36354 075.36354.0073
INFINEON BSC0923NDI 075.00923.M001
Dual-N standard symbol to colay

PQ5201 — FDMS3600-02-RJK0215-COLAY-GP
By BOM control

PWR_DCBATOUT_1D05V
PC5202 SC10U25V5KX-GP
PC5203 SC10U25V5KX-GP
PC5204 SCD1U25V2KX-L-GP
Sharpness Noise: PC5202,PC5203
From 2pcs 10uF to 1pcs 22uF low noise cap

Cyntec. 6.6mmx6.6mm x2.4mm
DCR: 11.2 ~ 13.5 m Ohm
Isat : 16A

PL5201:
CYNTEC PCMB062D-1R0MS 68.1R010.20G
TOKIN MPLCH0624L1R0 068.1R010.1051
MENTECH MHA0724NSG1R0M 068.1R010.M026

Icc(max):
Peak : 13.518A
TDC : 9.452A

PL5201 COIL-1UH-57-GP

PWR_1D05V
PG5201 GAP-CLOSE-PWR-3-GP
PC5201 SCD1U25V2KX-L-GP
PT5201 SE330U2VDM-4-GP

PT5201:
PANASONIC EEFSX0D331EY 79.33719.20C

PWR_1D05V_FB_A
PR5208 10KR2F-2-GP
PC5209 SC18P50V2JN-1-GP DY
PWR_1D05V_FB
PR5209 20KR2F-L-GP

Vout = 0.704 * (1+ 10/20)
= 1.056

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RT8237C_1D05V)
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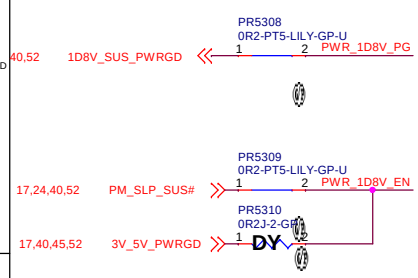
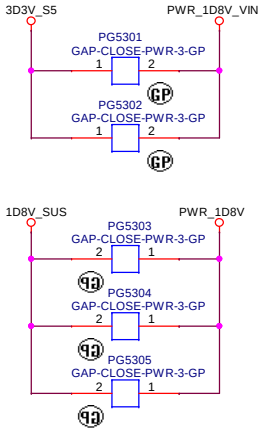
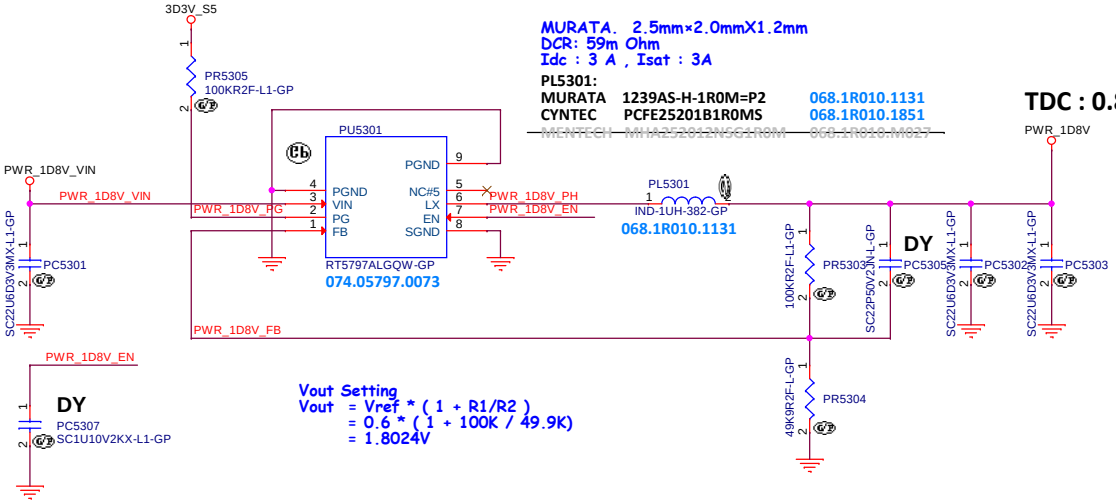


OFFPAGE - GAP





LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER (RT5797_1D8V)**

Size	Document Number	Rev
A3	Bumblebee-2	1

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LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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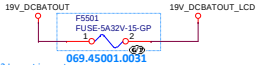
Main Func = LCD

BB2_EVT_MAIN_W001
BB2_EVT_MAIN_W003
BB2_EVT_MAIN_W018
BB2_EVT_MAIN_W019
BB2_EVT_MAIN_W020
BB2_SIT_MAIN_W001
BB2_SVT_MAIN_W003

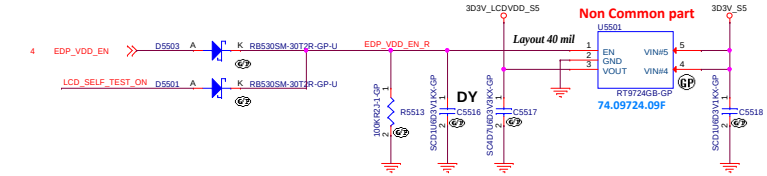
BB2_SIT_MAIN_L002

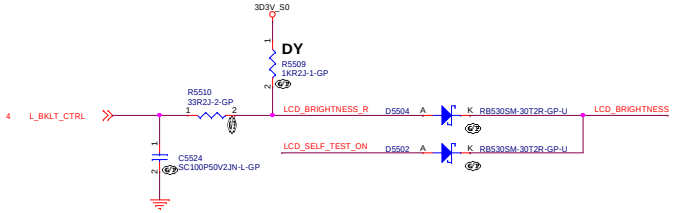
LCD Backlight Power

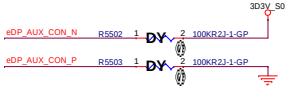


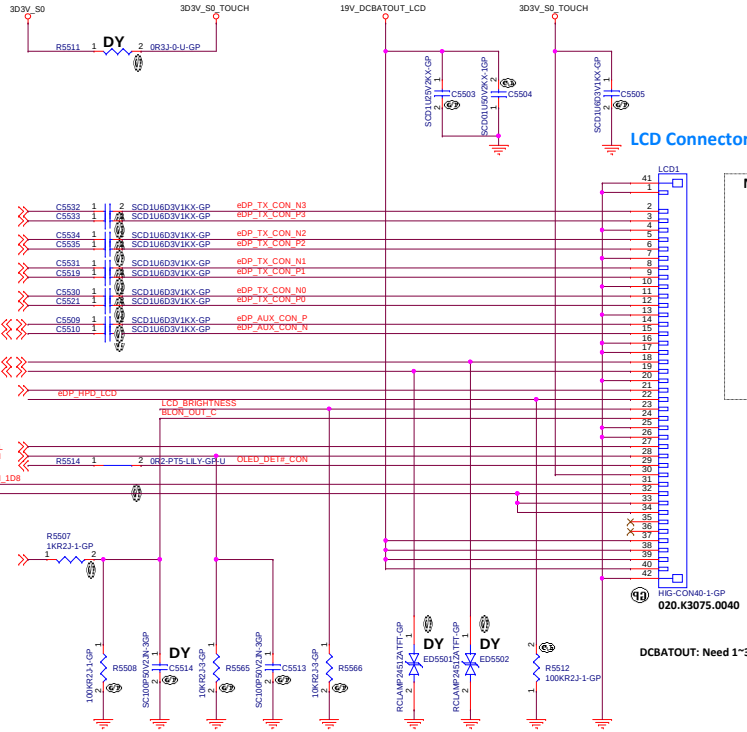
LBB-2 Layout impact:
WLAN antenna interference, change to small size

For LCD DCBATOUT inruch current



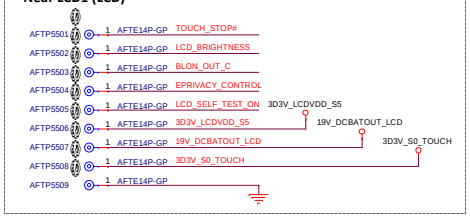






DCBATOUT: Need 1~3 empty-pin from DCBATOUT to the signals or other power net. (Apply to TNB, LNB)

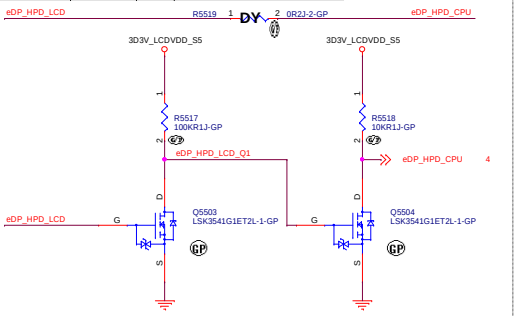
Near LCD1 (LCD)



For eDP VESA spec. requirement

Regarding to Intel CML/TGL platform eDP_HPD VIH cannot meet VESA Spec requirement

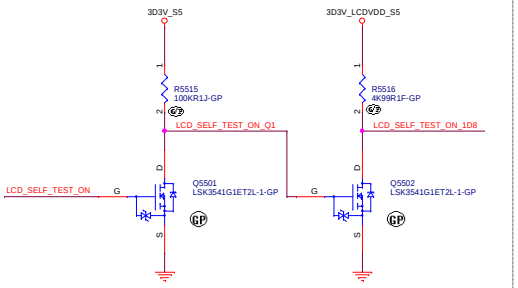
EDP_HPD	Intel CML	VIH	0.7 x VDD_3.3 = 2.31 ~ 2.59V
	VESA		2.25 ~ 3.6V



OLED Panel input voltage is 1.8V

Regarding to input voltage of BIST, please see table below: LCD_SELF_TEST_ON_1D8

Input Voltage	H-Level	VIH	0.7 x VDD_1.8	VDD_1.8	VDC
	L-Level	VIL	Vss	0.3 x VDD_1.8	VDC



LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DISPLAY (LCD/CAM/TOUCH)
Size: A2
Document Number: Bumblebee-2
Rev: 1
Date: Tuesday, March 03, 2020
Sheet 55 of 106

TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY1)
L: USB Type-C has higher priority when both ports are plugged H: HDMI Port has higher priority when both ports are plugged

Note: SW is pulled down with 150K-ohm internally

Place 0.1uF *4 and 0.01uF *4 caps near each VDD33 pin of PS8337

H: 4.7K-ohm
M: 150K-ohm
L: DY

CML DDI

TO PS8747B

CML DDI

HDMI

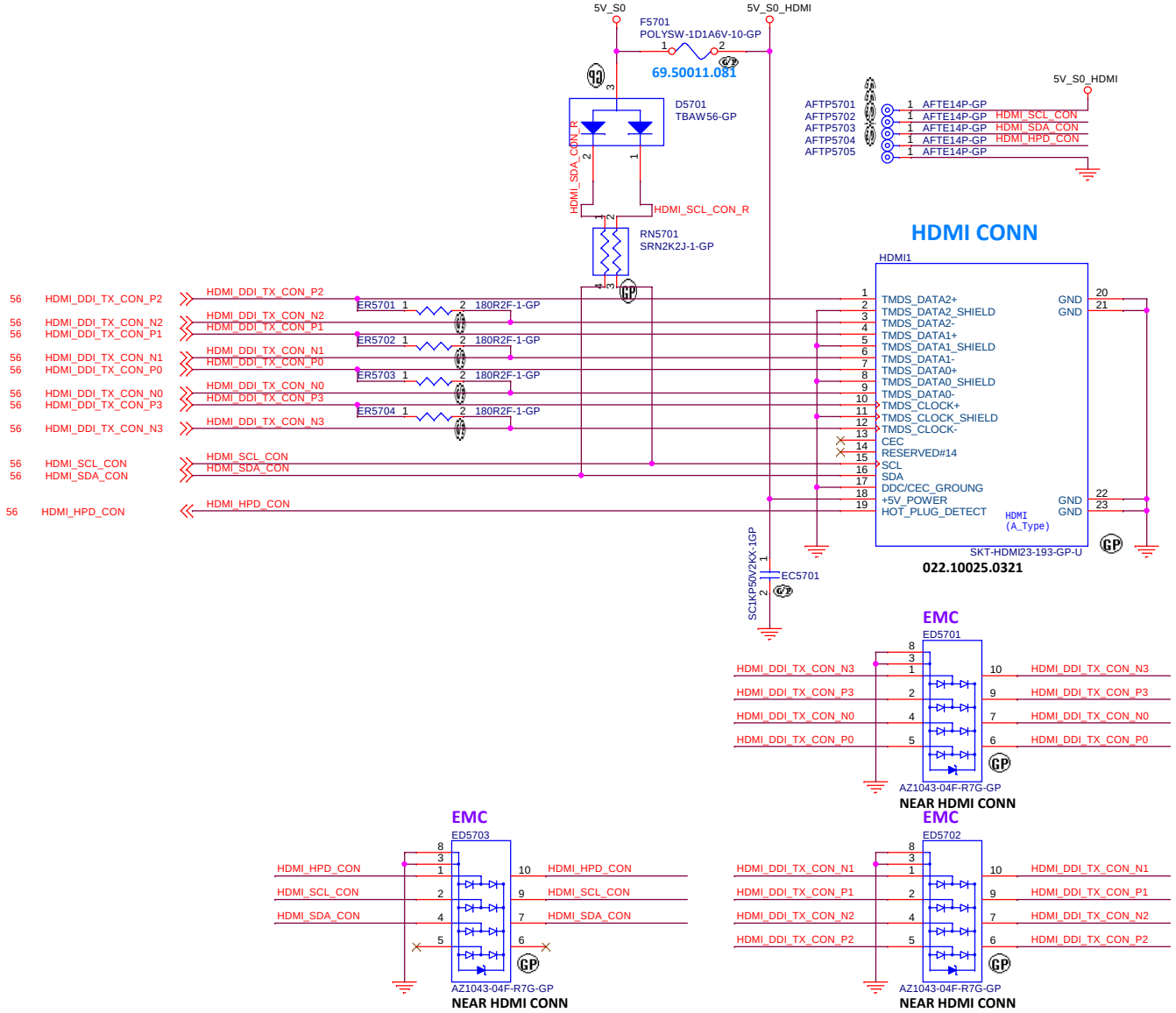
I2C SWITCH

LBB-2
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDI DEMULTIPLEXER (PS8337B)

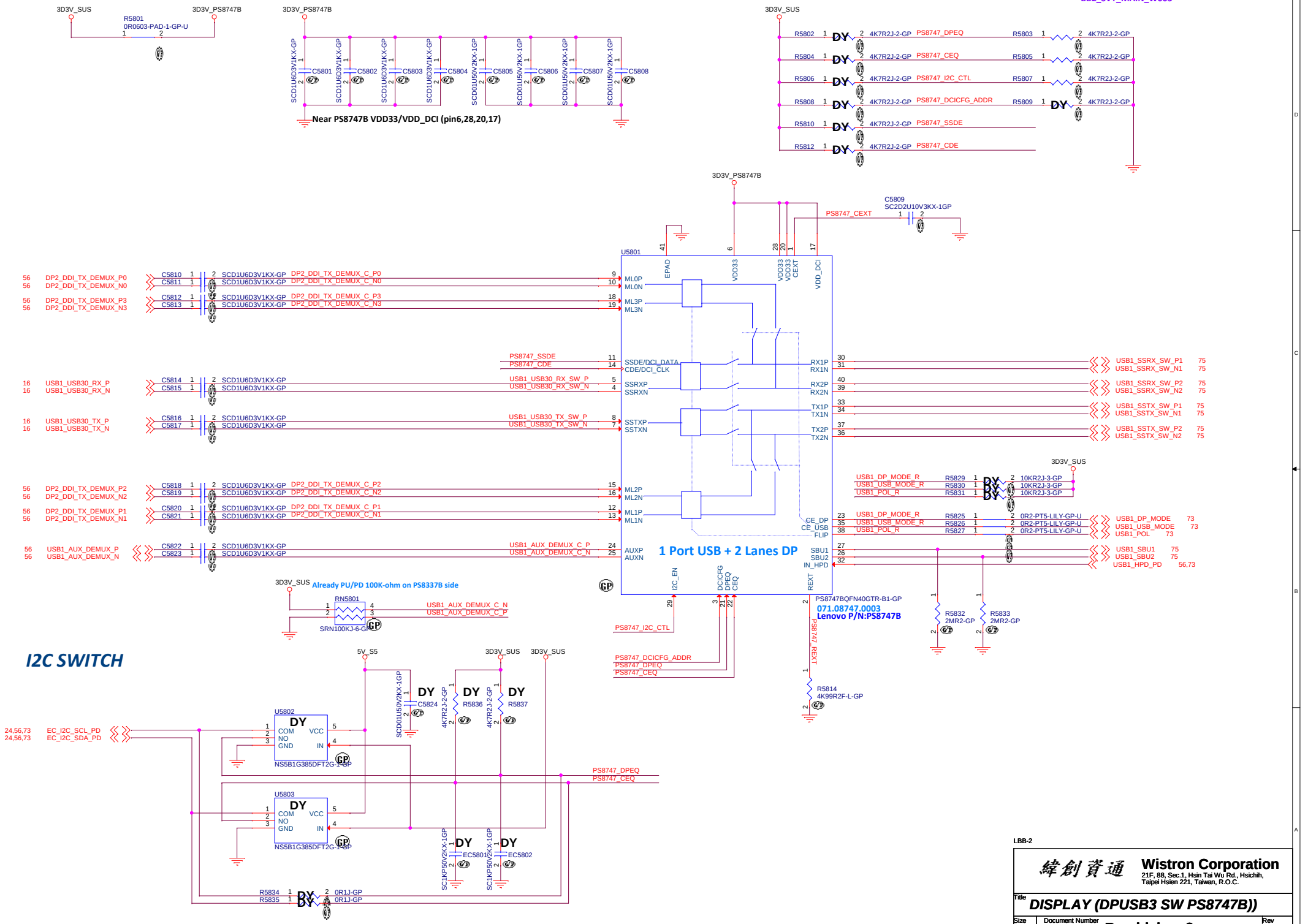
Size	Document Number	Rev
A2	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 56 of 106



LBB-2

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DISPLAY (HDMI CONN)		
Size: A3	Document Number: Bumblebee-2	Rev: 1
Date: Tuesday, March 03, 2020	Sheet 57 of 106	



LBB-2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DISPLAY (DPUSB3 SW PS8747B))		
Size: Custom	Document Number: Bumblebee-2	Rev: 1
Date: Tuesday, March 03, 2020	Sheet 58 of 106	

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LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DISPLAY (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-2**	**1**

Date: Tuesday, March 03, 2020 Sheet 59 of 106

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LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 60 of 106

Main Func = WLAN

BB2_EVT_MAIN_W003
BB2_EVT_MAIN_W023
BB2_EVT_MAIN_W007
BB2_SVT_MAIN_W003

Hybrid TYPE-E 1216
WLAN/CNVi on board (Harrison Peak)

Close to pin4,5

Close to pin72,73

WLAN1

WLAN-MODULE-123-GP-U

054.03149.0021

075.09904.0A7

PLACE NEAR WLAN1

Strap pin

LBB-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WLAN /CNVi)

Size: A2 | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020 | Sheet 61 of 106

BB2_EVT_MAIN_W003
BB2_FVT_MAIN_W007
BB2_FVT_MAIN_W008
BB2_FVT_MAIN_W012
BB2_SVT_MAIN_W003

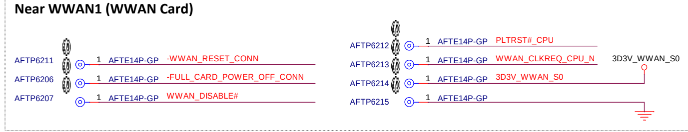
TABLE:

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)	Module Type & Main Host Interface	Port Configuration
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined
15	NC	NC	NC	NC	No Module Present	N/A

TABLE:

Module	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)	
Fibocom L850-GL	GND	NC	GND	GND	
Fibocom L860-GL	NC	NC	NC	GND	

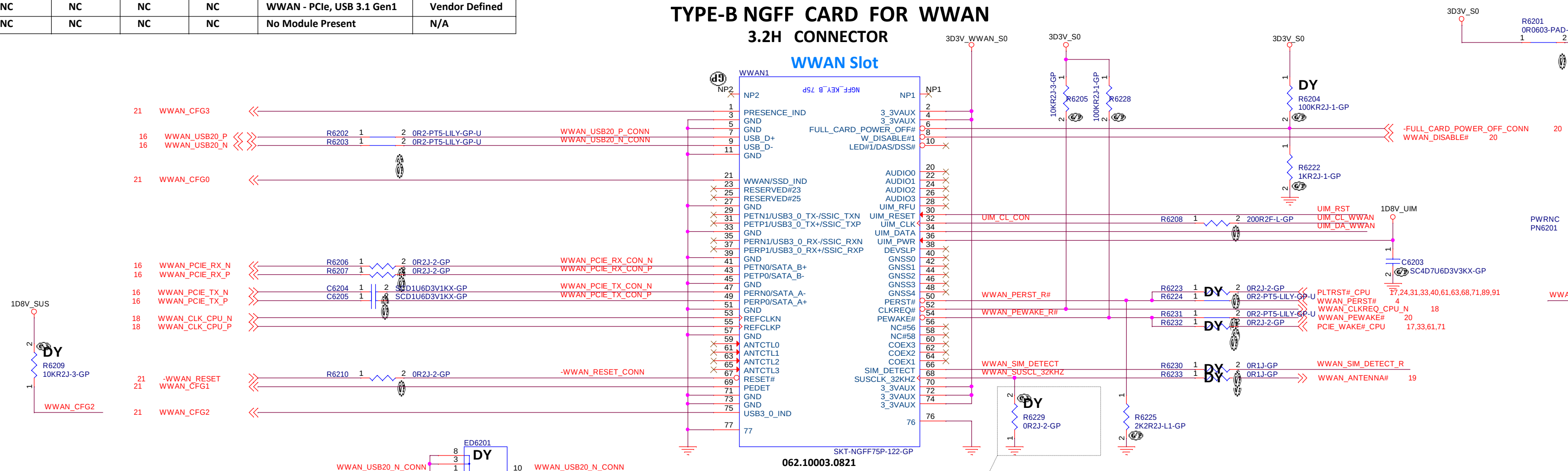
Near WWAN1 (WWAN Card)



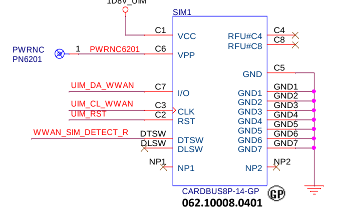
TYPE-B NGFF CARD FOR WWAN

3.2H CONNECTOR

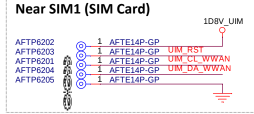
WWAN Slot

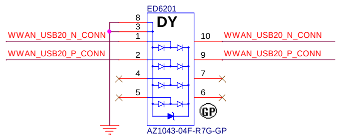


Micro SIM Slot



Near SIM1 (SIM Card)





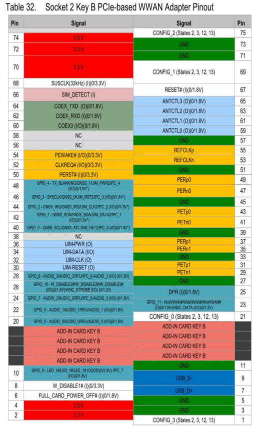
PLACE NEAR WWAN1

R6229 Config for MIMO 4 Antenna Enable:

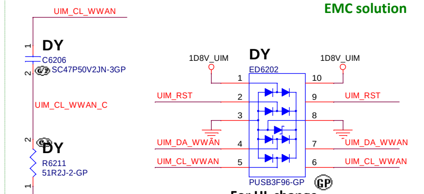
LOGIC →

R6229	ANT_CONFIG signal	Function
DY	High/Floating	Support dual antenna (Main & D/G ANT), Reserved
ASM	Low	Support 4 antenna, Reserved

Table 32. Socket 2 Key B PCIe-based WWAN Adapter Pinout

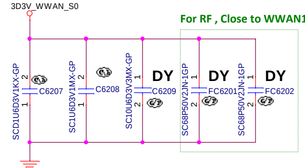


EMC solution



For HL change

For RF , Close to WWAN1



LBB-2

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	M.2 SOCKET 2 MODULE I/F
Size A2	Document Number Bumblebee-2 — Rev 1
Date: Tuesday, March 03, 2020	Sheet 62 of 106

TYPE-M M.2 CARD FOR SSD

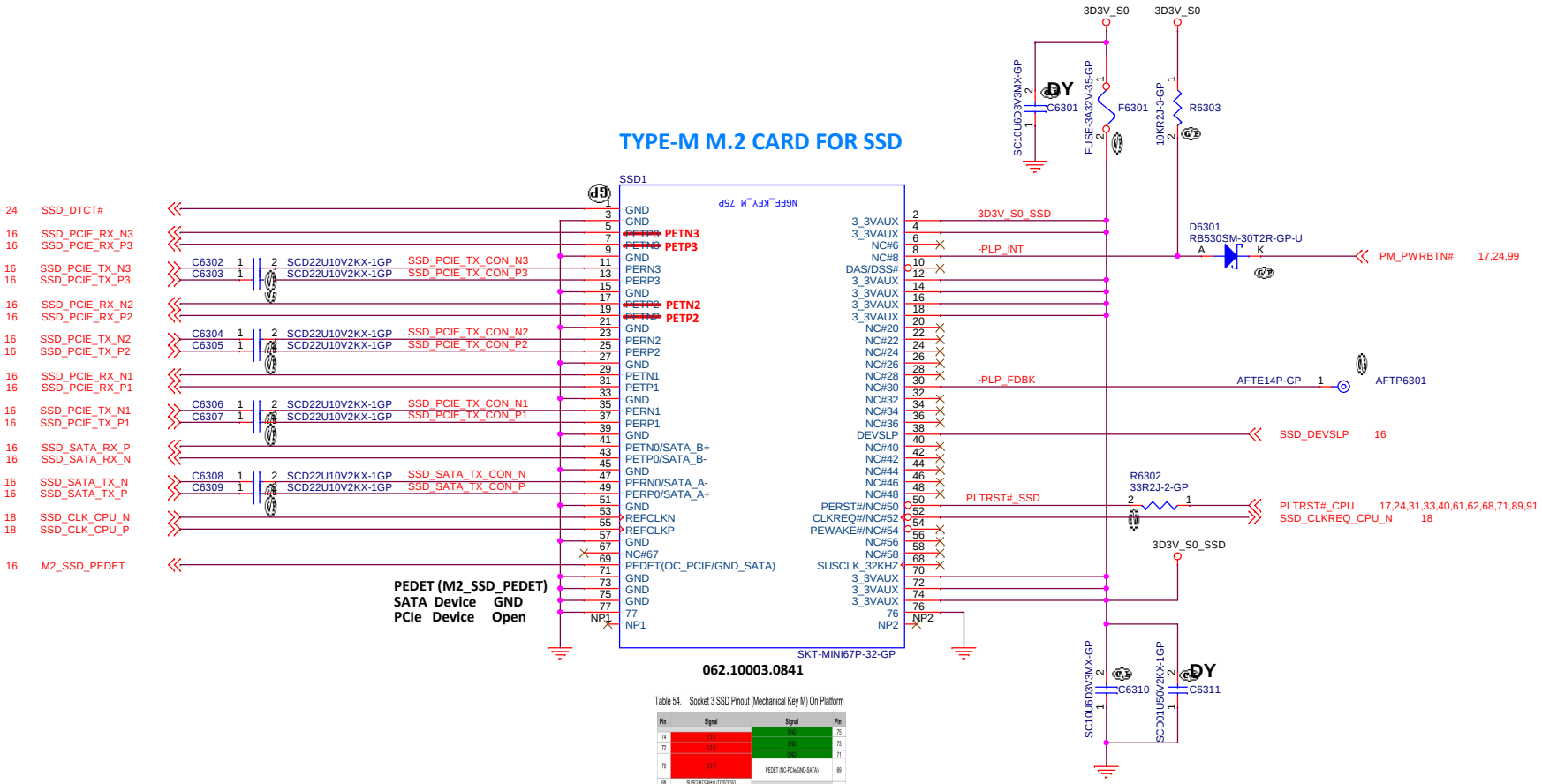
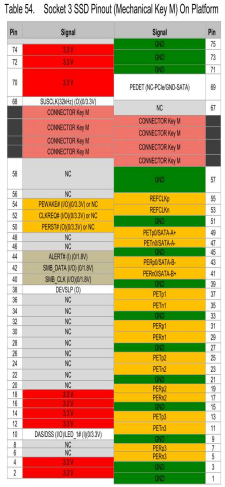


Table 54. Socket 3 SSD Pinout (Mechanical Key M) On Platform



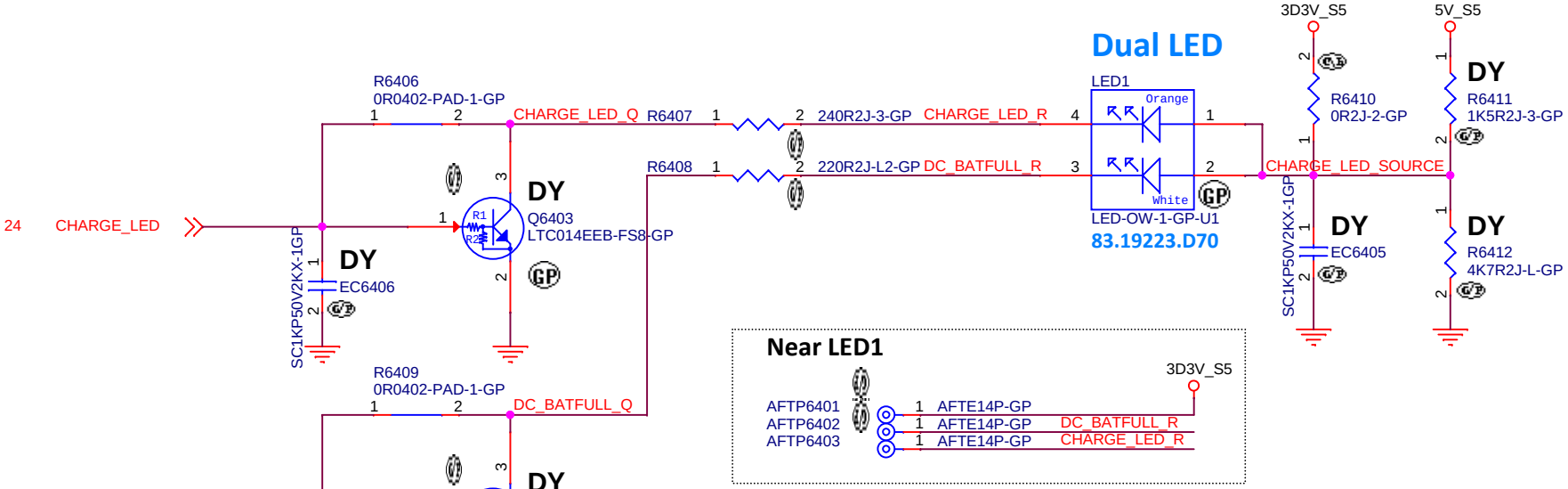
LBB-2

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: INT IO (SSD M.2)		
Size: A3	Document Number: Bumblebee-2	Rev: 1
Date: Tuesday, March 03, 2020	Sheet 63 of 106	

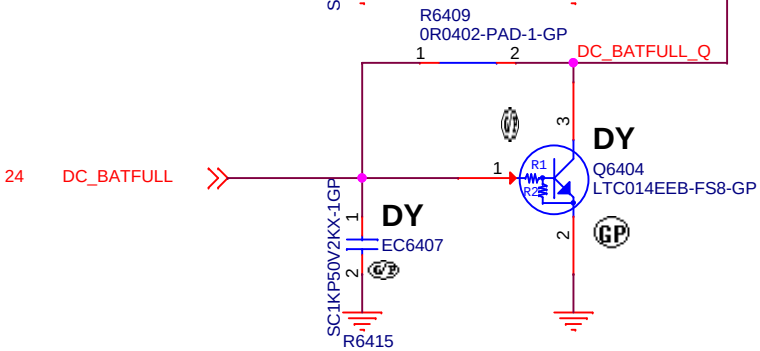
BB2_SVT_MAIN_W003

Layout impact:
R6410 keep 0-ohm

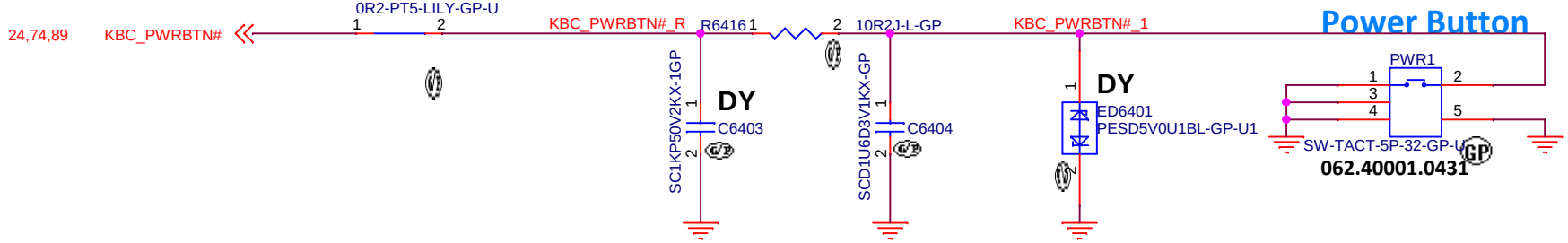
Dual LED



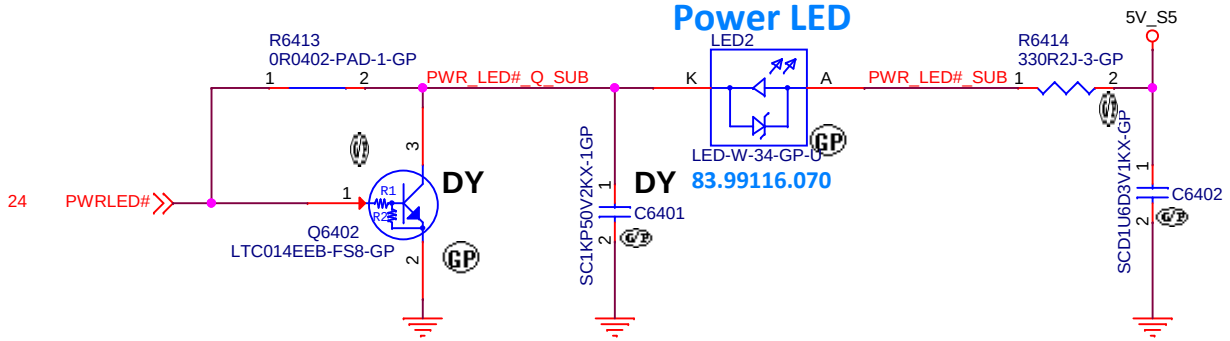
Near LED1



Power Button



Power LED



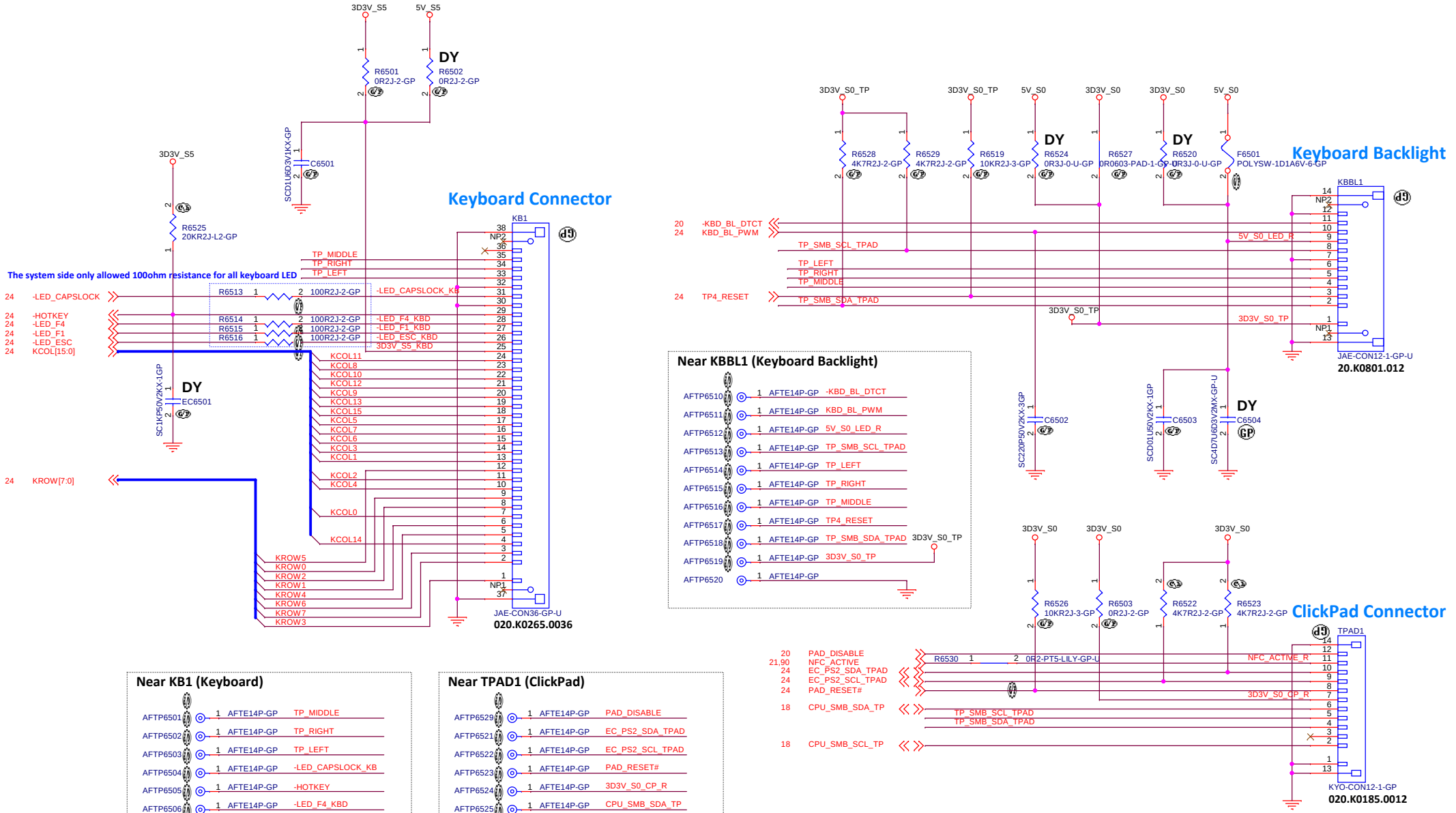
LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LED/BTN/POWER BTN**

Size	Document Number	Rev
A4	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 64 of 106

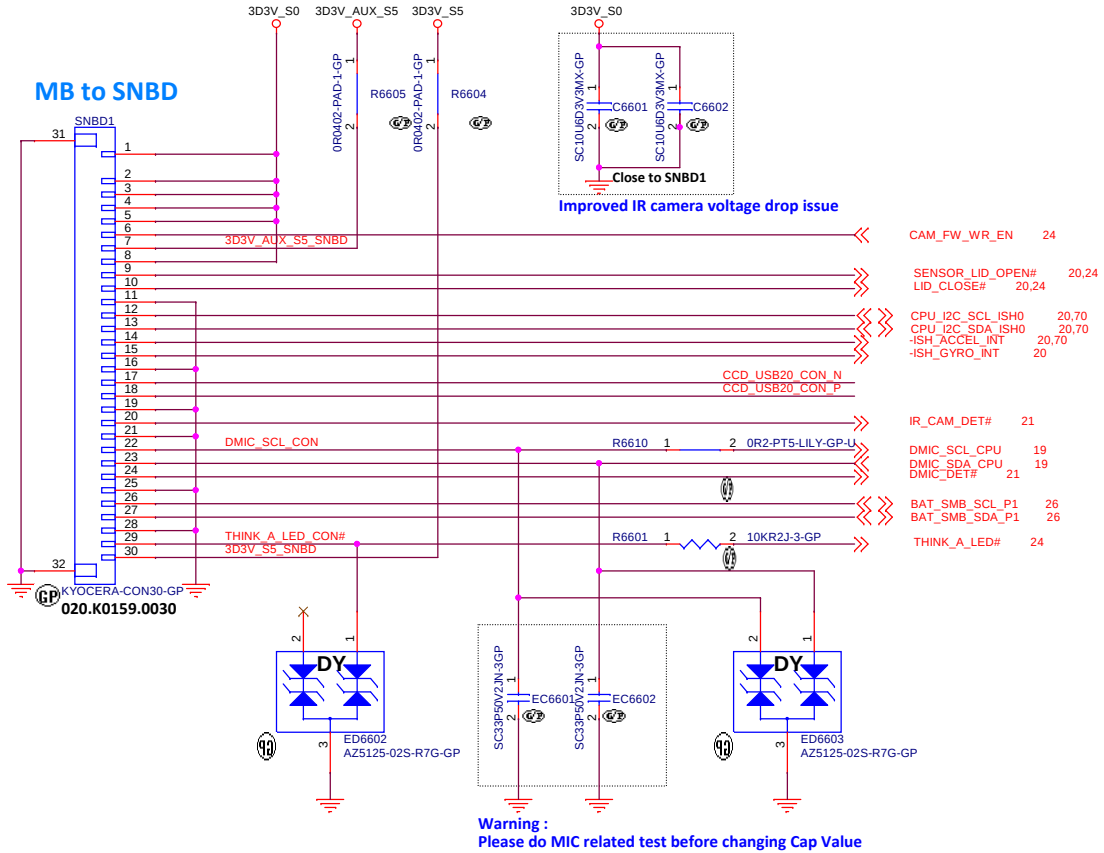


LBB-2

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: INT IO (KB/CP/TP)		
Size: A3	Document Number: Bumblebee-2	Rev: 1
Date: Tuesday, March 03, 2020	Sheet 65 of 106	

BB2_EVT_MAIN_W002
BB2_EVT_MAIN_W017
BB2_SIT_MAIN_W006
BB2_SVT_MAIN_W003

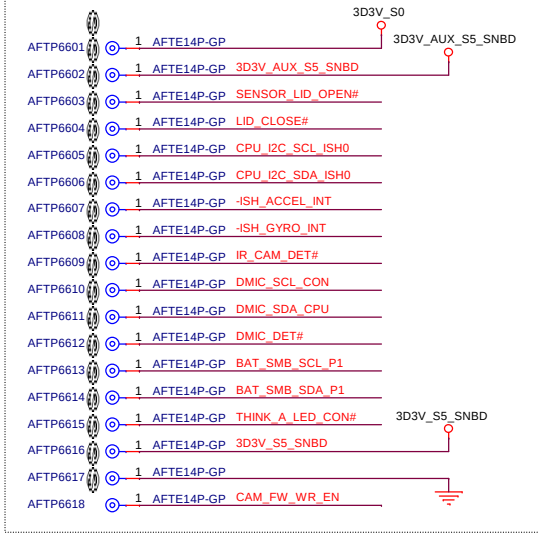
MB to SNBD



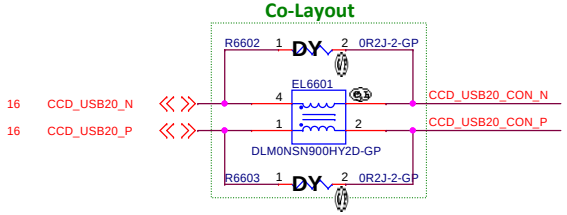
Camera

P-Sensor

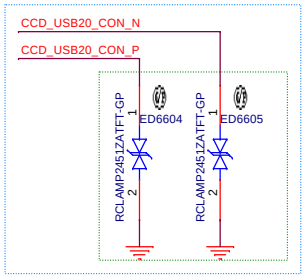
Near SNBD1 (Sensor board)



Co-Layout



LBB-2 Layout impact:
WWAN antenna interference, change to small size



For CAMERA ESD failed solution

LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO BOARD CONN

Size	Document Number	Rev
A3	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 66 of 106

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LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

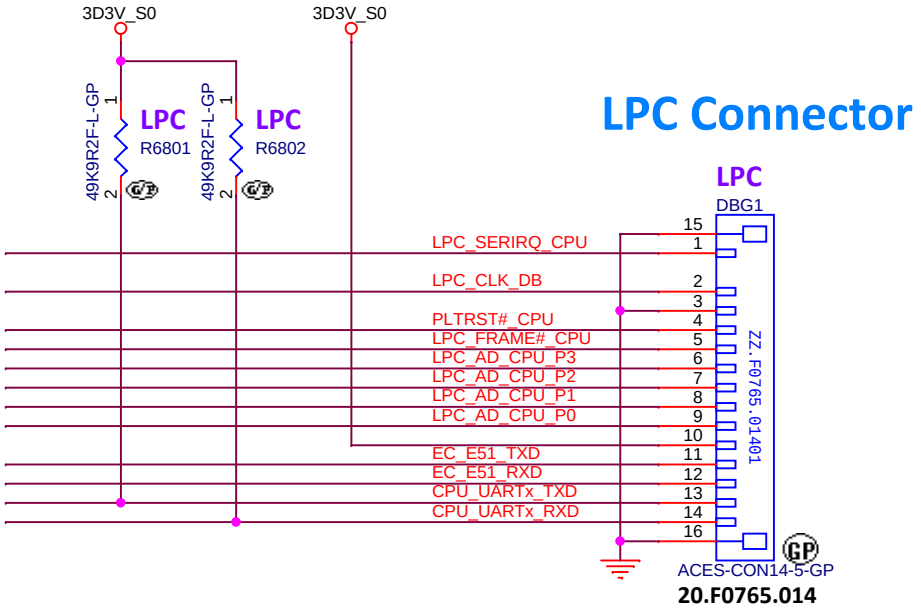
Title ***SENSOR (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-2**	**1**

Date: Tuesday, March 03, 2020 Sheet 67 of 106

Main Func = Debug

18,24 LPC_SERIRQ_CPU
18 LPC_CLK_DB
17,24,31,33,40,61,62,63,71,89,91 PLTRST#_CPU
18,24 LPC_FRAME#_CPU
18,24 LPC_AD_CPU_P3
18,24 LPC_AD_CPU_P2
18,24 LPC_AD_CPU_P1
18,24 LPC_AD_CPU_P0
24 EC_E51_TXD
24 EC_E51_RXD
21 CPU_UARTx_TXD
21 CPU_UARTx_RXD



LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DEBUG (LPC DEBUG)***

Size	Document Number	Rev
A4	**Bumblebee-2**	1

Date: Tuesday, March 03, 2020 Sheet 68 of 106

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LBB-2

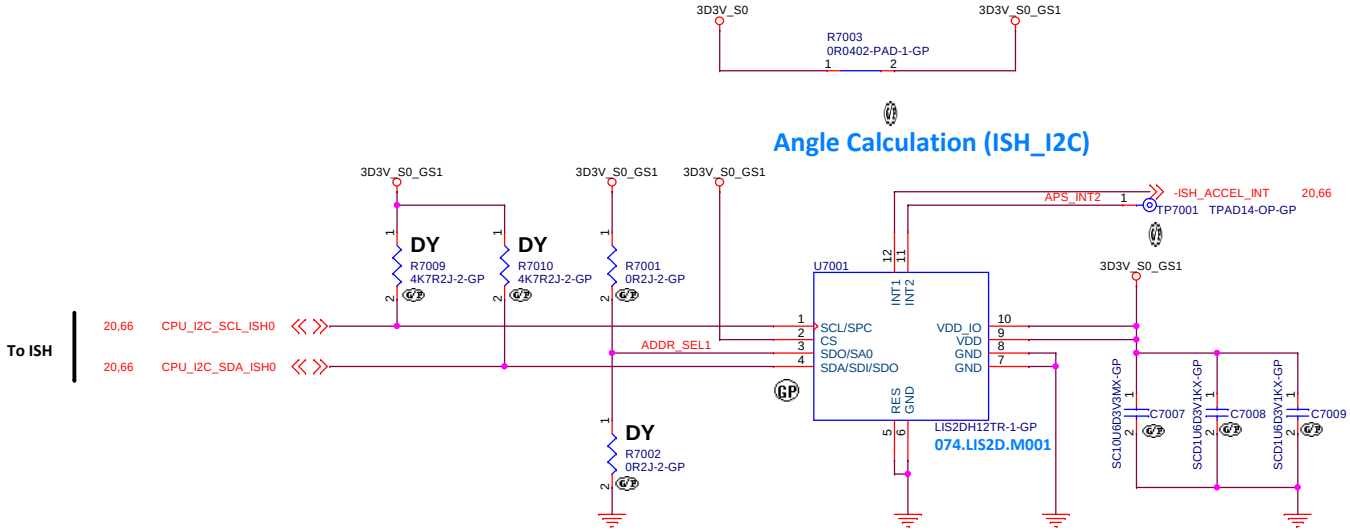
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SENSOR (RSVD)***

Size	Document Number	Rev
A4	**Bumblebee-2**	**1**

Date: Tuesday, March 03, 2020 Sheet 69 of 106



TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

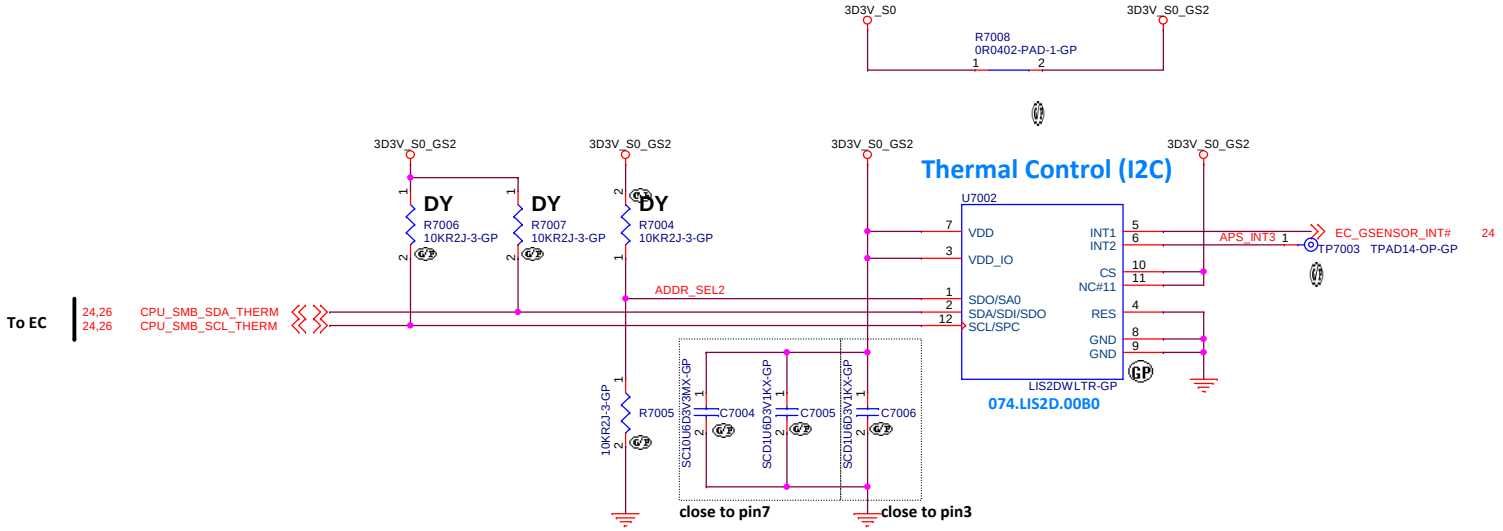
TABLE for Angle Detection (U7001): Tri-axis Digital Accelerometer

P/N	ADDR_SEL1	Address
LIS2DH12TR	H	32h(W) & 33h(R)
	L	30h(W) & 31h(R)

← Logic

TABLE of G-Sensor (U7001)

Vendor	P/N	Wistron P/N
ST	LIS2DH12TR	074.LIS2D.M001



TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

← Logic

TABLE for Angle Detection (U7002): Tri-axis Digital Accelerometer

P/N	ADDR_SEL2	Address
BMA280	H	32h(W) & 33h(R)
	L	30h(W) & 31h(R)
LIS2DWLTR	H	32h(W) & 33h(R)
	L	30h(W) & 31h(R)

← Logic

TABLE of G-Sensor(U7002)

Vendor	P/N	Wistron P/N
BOSCH	BMA280	074.00280.0AB0
ST	LIS2DWLTR	074.LIS2D.00B0

LBB-2

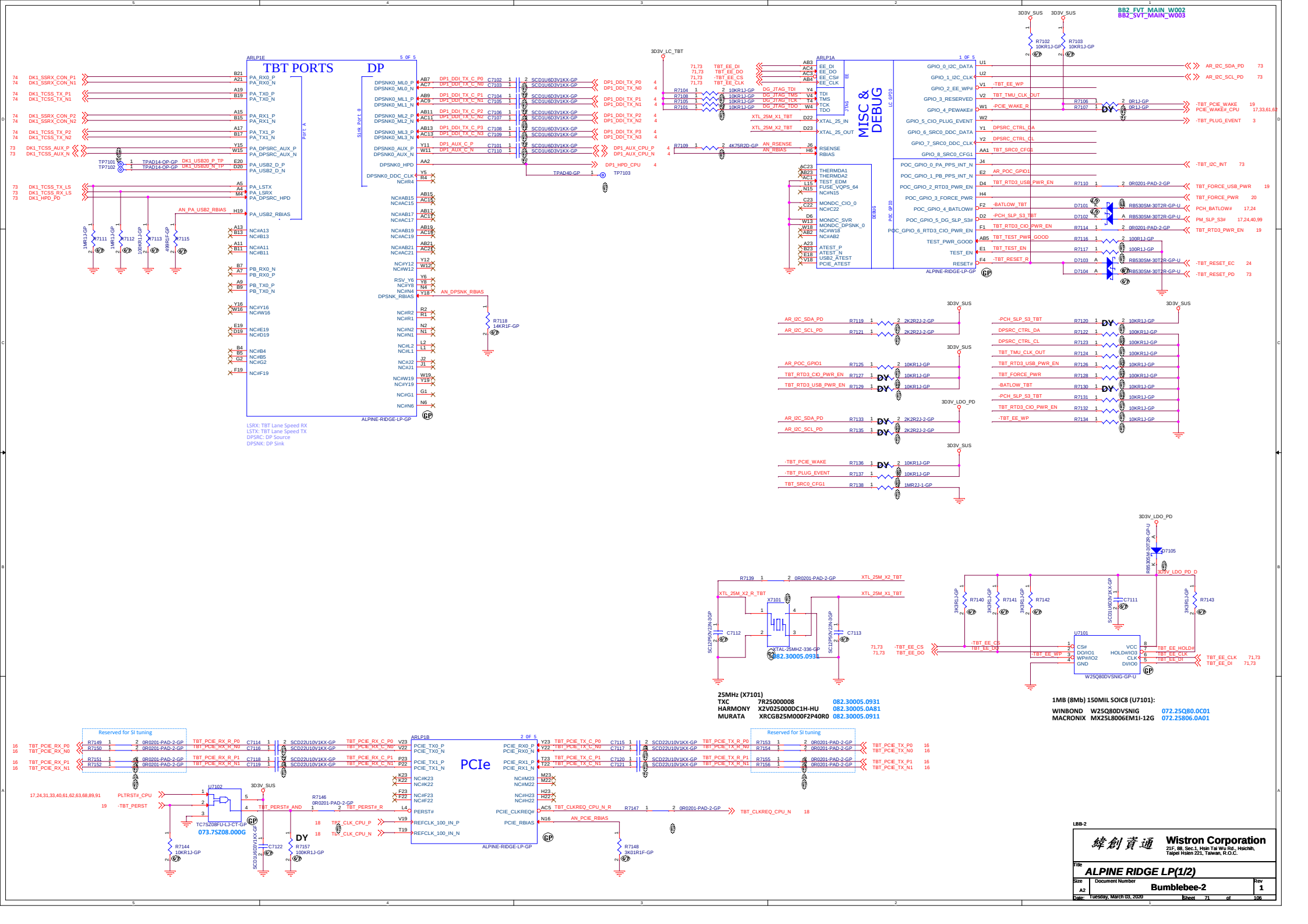
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

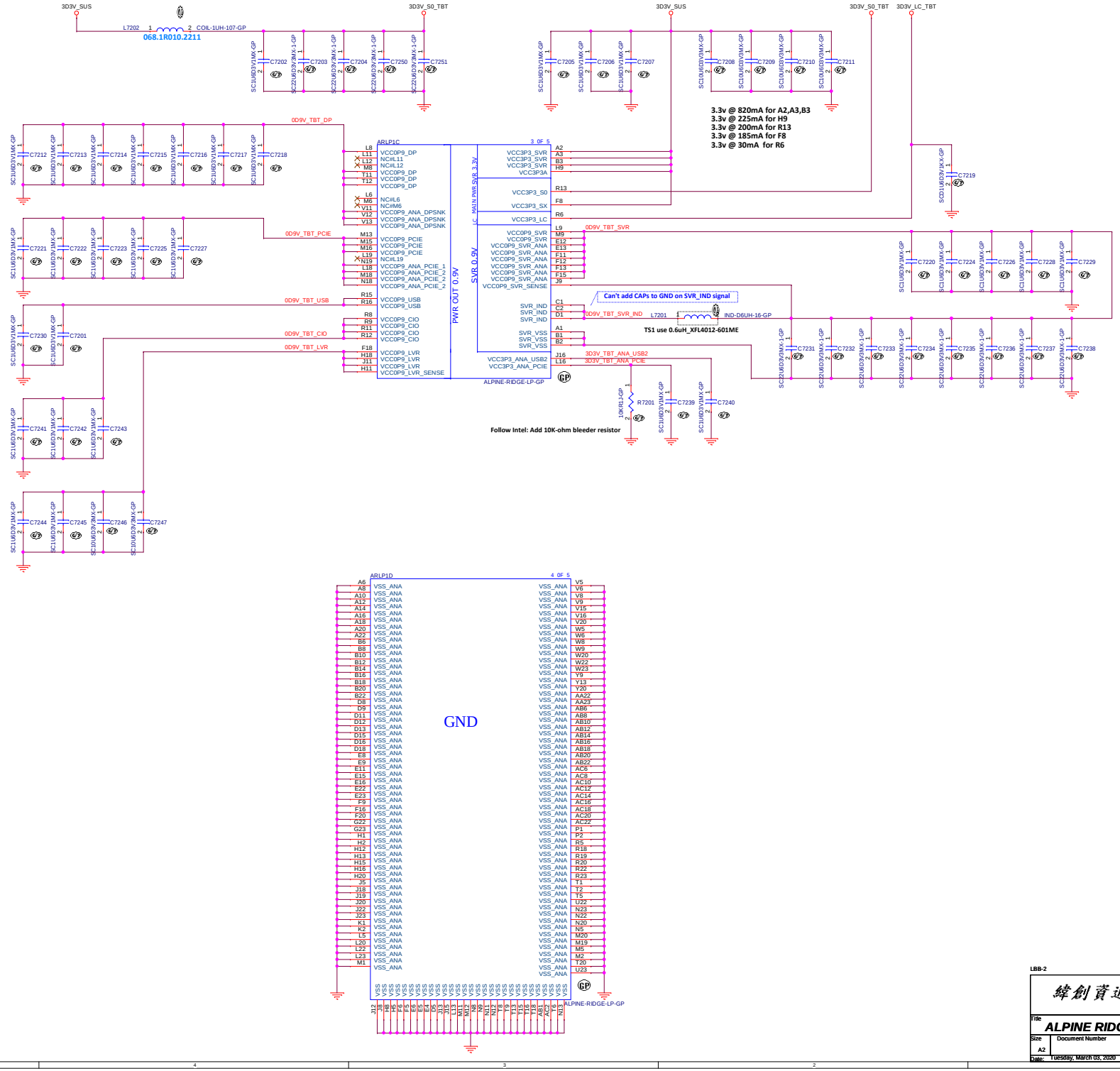
Title: ***SENSOR (G-SENSOR)***

Size	Document Number	Rev
A3	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 70 of 106

BB2_FVT_MAIN_W002
BB2_SVT_MAIN_W003





LBB-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ALPINE RIDGE LP(2/2)**

Size	Document Number	Rev
A2	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 72 of 106

TABLE BUSPOWER Configuration (PD_ADCIN1 Resister Divider)

DIV = R7301 / (R7303 + R7301)		Configuration
DIV MIN	DIV MAX	
0.00	0.18	BP_NoRespones
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

LOGIC

DIV = R2 / (R1 + R2)

(R1)

(R2)

POWER IN

POWER IN/OUT

POWER OUT

PLACE NEAR U7301

D7301, D7302
ONSEMI NSR20F30NXT5G 083.20F30.008H
VISHAY VSKY20301608 083.20301.008F

FROM EC

FROM AR

TABLE I2C Addrssing (TBD)

I2C1 (to EC)	TBT PORT	0X23
	USBC PORT	0X27
I2C2 (to AR)	TBT PORT	0X38
	USBC PORT	0X3F

(Split-pad)
SN1701012RJTR(SL80Q56940AA)
TPS65988CE RJTR Symbol

(with split-pad)
SN1701012 is equivalent device of TPS65988
U7301 will use BOM control by co-lay symbol issue

TS3DS10224 is used for:
(1) Multiplexing DP_AUX signal and TBT_LS signal (TBTx_DP/TBT_MODE)
(2) Supporting cable flip (TBTx_POL)
Those function had been supported in TPS65982 but not in TPS65988/SN1701012

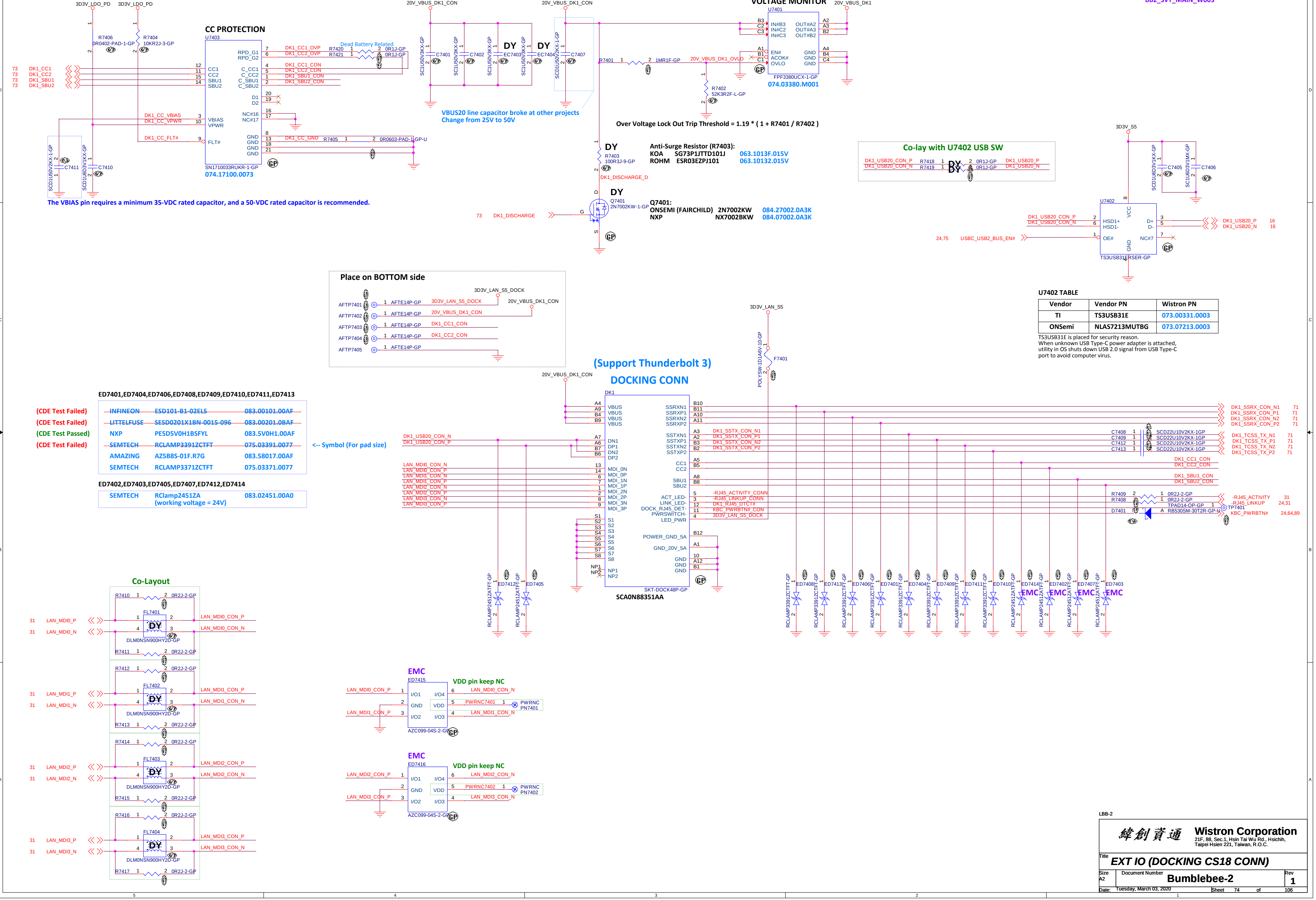
LBB-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (TYPEC PD TPS65988)

Size: A2 | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020 | Sheet 73 of 99


CC PROTECTION
U7403
SN1710033RUKR-1-GP
074.17100.0073
Dead Battery Related
VOLTAGE MONITOR
U7401
FPF3380UCX-1-GP
074.03380.M001
VBUS20 line capacitor broke at other projects
Change from 25V to 50V
Over Voltage Lock Out Trip Threshold = 1.19 * (1 + R7401 / R7402)
Anti-Surge Resistor (R7403):
KOA SG73P1JTTD101J 063.1013F.015V
ROHM ESR03EZPJ101 063.10132.015V
Q7401:
ONSEMI (FAIRCHILD) 2N7002KW 084.27002.0A3K
NXP NX7002BKW 084.07002.0A3K
Co-lay with U7402 USB SW
U7402
TS3USB31ERSER-GP
The VBIAS pin requires a minimum 35-VDC rated capacitor, and a 50-VDC rated capacitor is recommended.
Place on BOTTOM side
(Support Thunderbolt 3)
DOCKING CONN
DK1
SKT-DOCK48P-GP
SCA0N88351AA
<-- Symbol (For pad size)
Co-Layout
FL7401
FL7402
FL7403
FL7404
DLM0NSN900HY2D-GP
EMC
ED7415
ED7416
AZC099-04S-2-GP
VDD pin keep NC

U7402 TABLE

Vendor	Vendor PN	Wistron PN
TI	TS3USB31E	073.00331.0003
ONSemi	NLAS7213MUTBG	073.07213.0003

TS3USB31E is placed for security reason.
When unknown USB Type-C power adapter is attached, utility in OS shuts down USB 2.0 signal from USB Type-C port to avoid computer virus.

ED7401,ED7404,ED7406,ED7408,ED7409,ED7410,ED7411,ED7413

Test result	Vendor	Vendor PN	Wistron PN
(CDE Test Failed)	~~INFINEON~~	~~ESD101-B1-02ELS~~	~~083.00101.00AF~~
(CDE Test Failed)	~~LITTELFUSE~~	~~SESD0201X1BN-0015-096~~	~~083.00201.0BAF~~
(CDE Test Passed)	NXP	PESD5V0H1BSFYL	083.5V0H1.00AF
(CDE Test Failed)	~~SEMTECH~~	~~RCLAMP3391ZCTFT~~	~~075.03391.0077~~
	AMAZING	AZ5B8S-01F.R7G	083.58017.00AF
	SEMTECH	RCLAMP3371ZCTFT	075.03371.0077

ED7402,ED7403,ED7405,ED7407,ED7412,ED7414

Vendor	Vendor PN	Wistron PN
SEMTECH	RClamp2451ZA (working voltage = 24V)	083.02451.00A0

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Title: *EXT IO (DOCKING CS18 CONN)*

Size: A2 | Document Number: **Bumblebee-2** | Rev: 1

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BB2_EVT_MAIN_W007
BB2_EVT_MAIN_W008
BB2_EVT_MAIN_W011
BB2_EVT_MAIN_W003
BB2_SVT_MAIN_W003

BB2_EVT_MAIN_L001

CC PROTECTION

U7503

SN1710033RUKR-1-GP

074.17100.0073

The VBIAS pin requires a minimum 35-VDC rated capacitor, and a 50-VDC rated capacitor is recommended.

VOLTAGE MONITOR

U7501

FPF3380UCX-1-GP

074.03380.M001

VBUS20 line capacitor broke at other projects
Change from 25V to 50V

Over Voltage Lock Out Trip Threshold = 1.19 * (1 + R7501 / R7502)

Anti-Surge Resistor (R7503):

KOA	SG73P1JTTD101J	063.1013F.015V
ROHM	ESR03EZPJ101	063.10132.015V

Q7501:

ONSEMI (FAIRCHILD)	2N7002KW	084.27002.0A3K
NXP	NX7002BKW	084.07002.0A3K

Co-lay with U7502 USB SW

U7502

TS3USB31ERSER-GP

U7502 TABLE

Vendor	Vendor PN	Wistron PN
TI	TS3USB31E	073.00331.0003
ONSemi	NLAS7213MUTBG	073.07213.0003

TS3USB31E is placed for security reason.
When unknown USB Type-C power adapter is attached, utility in OS shuts down USB 2.0 signal from USB Type-C port to avoid computer virus.

Place on BOTTOM side

Co-Layout

USB TYPE-C CONN

USB1

SKT-USB32-42-GP-U

SCA0N88352AA

EMC

ED7518

ED7519

AZ1043-04F-R7G-GP

ED7520,ED7521

SEMTECH	RClamp2451ZA (working voltage = 24V)	083.02451.00A0

LBB-2

緯創資通 Wistron Corporation
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Title: EXT IO (TYPEC CONN)

Size	Document Number	Rev
A2	Bumblebee-2	1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 77 of 106

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 82 of 106

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 83 of 106

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 87 of 106

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RSVD)

Size	Document Number	Rev
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BB2_EVT_MAIN_W020
BB2_SIT_MAIN_W005
BB2_SIT_MAIN_W007v2
BB2_SIT_MAIN_W008v2
BB2_SIT_MAIN_W009
BB2_SIT_MAIN_W011
BB2_SVT_MAIN_W004

Screw Pad

H1 HOLET237B414X240R103-S1 — Special GND HOLE for Layout
H3 HOLE237R103-GP — ZZ.00PAD.EJ1
H4 HOLE237R103-GP — ZZ.00PAD.EJ1
H5 HOLE217R103-GP — ZZ.00PAD.AI1
H6 HOLE217R103-GP — ZZ.00PAD.AI1
H9 HOLET233B158R142-GP — ZZ.00PAD.VK1
H10 HOLET233B158R142-GP — ZZ.00PAD.VK1
H11 HOLET233B158R142-GP — ZZ.00PAD.VK1
H12 HOLET233B158R142-GP — ZZ.00PAD.VK1

Stand Off

H20 STFT236B142R128H43-3-GP — 34.4LY01.101
H21 STFT236B142R128H43-1-GP — 34.4EO02.001 — For M.2 SSD
H14 STFT237B142R113H47-GP — 434.0DA01.0001
H15 STFT237B142R113H47-GP — 434.0DA01.0001

Spring Plate

SPR1 SPRING-31-GP-U — 34.49U24.001
SPR2 SPRING-64-GP — 34.4H602.001

Special GND HOLE for Layout

HL1 HOLET475X368B453X362R119-2P-S1
HL2 HOLET583X414B544X317R119-2P-S
HL3 HOLET662X365B512X329R103-2P-S2
HL4 HOLE315R193
HL5 HOLET315B335X355R119-S
HL6 HOLET237B103R79

Test Point

Place on top side
TP8901 TPAD60 — KBC_PWRBTN# — 24,64,74,89

Place on bottom side
TP8902 TPAD60 — KBC_PWRBTN# — 24,64,74,89

AFTP8918 AFTE14P-GP — PLTRST#_CPU — 17,24,31,33,40,61,62,63,68,71,91
AFTP8921 AFTE14P-GP — KBC_PWRBTN# — 24,64,74,89

Place on top side
5V_S5 5V_S0 3D3V_S5 3D3V_S0
AFTP8901 AFTE14P-GP
AFTP8912 AFTE14P-GP
AFTP8902 AFTE14P-GP
AFTP8903 AFTE14P-GP
AFTP8904 AFTE14P-GP
AFTP8905 AFTE14P-GP
AFTP8906 AFTE14P-GP — PLTRST#_EC — 24
AFTP8907 AFTE14P-GP
AFTP8908 AFTE14P-GP
AFTP8909 AFTE14P-GP
AFTP8910 AFTE14P-GP
AFTP8911 AFTE14P-GP

RF CAPs

19V_DCBATOUT: TOP side | BOTTOM side | TOP side
1D2V_S3: BOTTOM side | TOP side
FC8979 Near C1325
FC8980 Near C1240
FC8981 Near C1244
FC8982 Near C1242
FC8987 Near C1246

1D2V_S3: TOP side | BOTTOM side | TOP side | BOTTOM side
FC8968 Near C1391
FC8969 Near C1399
FC8970 Near C1393
FC8971 Near C1209
FC8972 Near C1395
FC8973 Near C1235
FC8975 Near C1205
FC8976 Near C1213
FC8977 Near C1233
FC8978 Near C1327

0D9V_LAN: TOP side
3D3V_WLAN: TOP side
1D05V_SUS: BOTTOM side
1V_CPU_CORE: TOP side | BOTTOM side

19V_DCBATOUT_LCD: TOP side
3D3V_SUS: BOTTOM side | TOP side
3D3V_PS8747B: BOTTOM side
1V_VCCGT: BOTTOM side
PWR_1D2V: TOP side | BOTTOM side
3D3V_AUX_S5: BOTTOM side
3D3V_S5: BOTTOM side

5V_S0: BOTTOM side
PWR_DCBATOUT_VDDQ: BOTTOM side
2D5V_S3: TOP side | BOTTOM side | TOP side
FC8988 Near C1374
FC8991 Near C1372
1D2V_S3: BOTTOM side | TOP side
1D05V_VCCST: BOTTOM side
1V_VCCSA: BOTTOM side
1D05V_VCCIO: TOP side

19V_DCBATOUT: TOP side | TOP side | TOP side
PWR_DCBATOUT_VCCSA: TOP side
5V_S5: TOP side | BOTTOM side
PWR_DCBATOUT_VCOREA: BOTTOM side
PWR_DCBATOUT_VDDQ: BOTTOM side
3D3V_PEN_S0: BOTTOM side
BT+_IN1: BOTTOM side

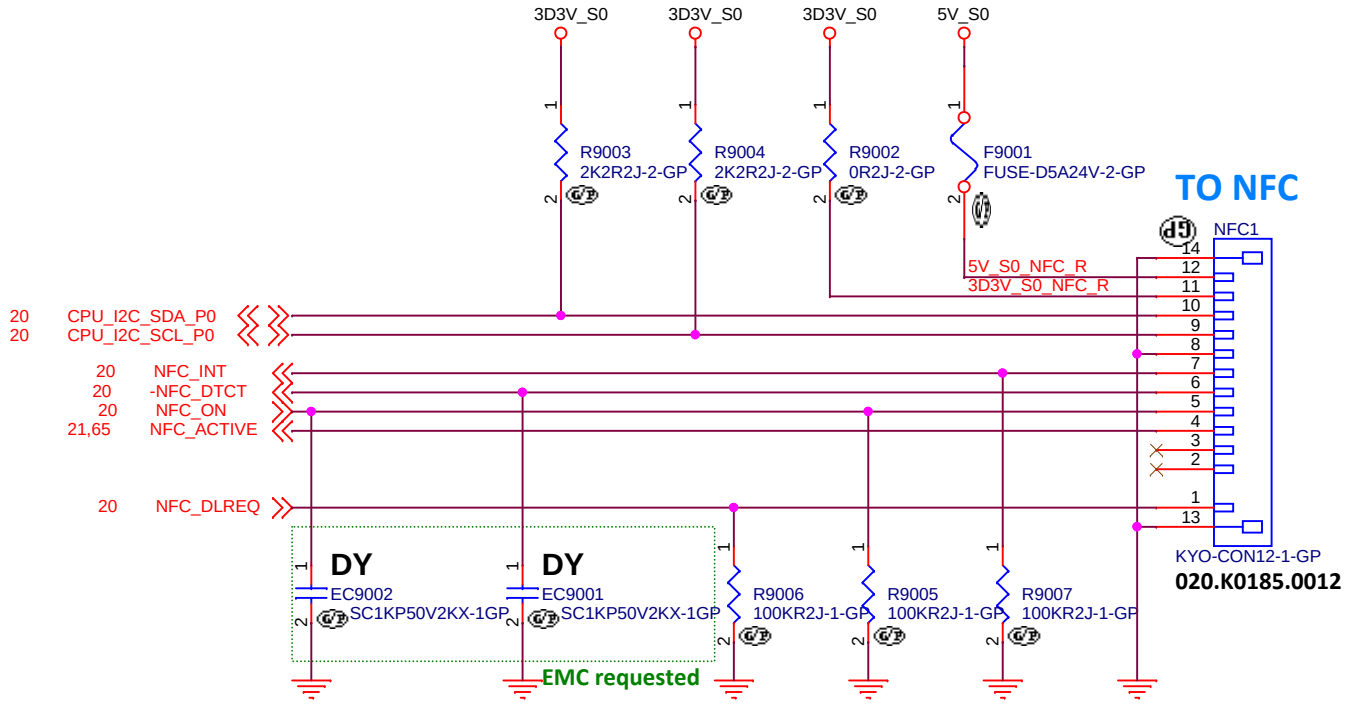
EMI CAPs

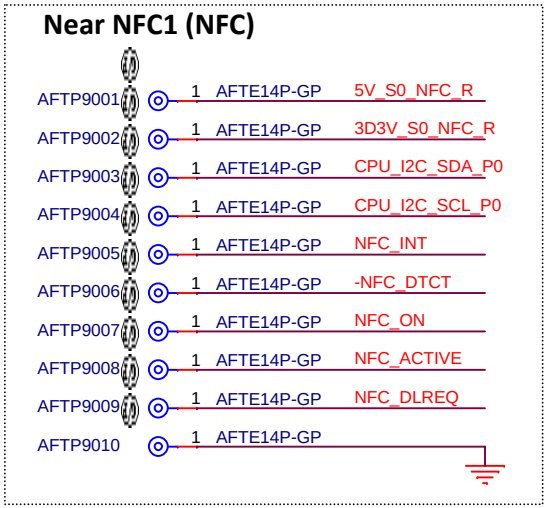
20V_VINT_IN
BT+_IN1 — Closed to BATT1
20V_VINT_IN_R
19V_DCBATOUT
PWR_DCBATOUT_5V
PWR_DCBATOUT_3D3V — Closed to PU4701
PWR_DCBATOUT_VCOREA
PWR_DCBATOUT_VCOREB — Closed to PU4702
EC_THINKA_PWRLED 24

LBB-2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS (ME/RF/EMI)
Size: A2 | Document Number: Bumblebee-2 | Rev: 1
Date: Tuesday, March 03, 2020 | Sheet 89 of 106





Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C _SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

Remark: P – power supply, G – ground, I – input, O – output, I/O – input/output

LBB-2

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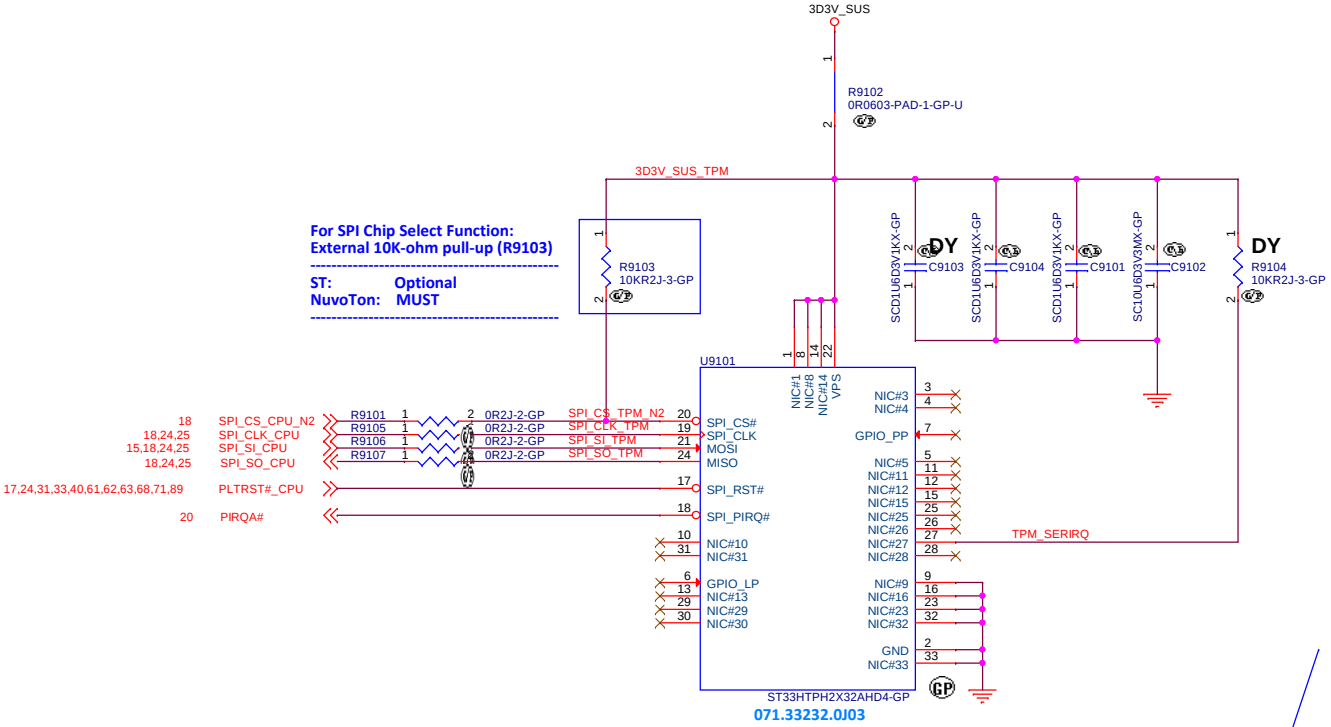
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (NFC)

Size: A4 | Document Number: Bumblebee-2 | Rev: 1

Date: Tuesday, March 03, 2020 | Sheet 90 of 106



SPI Chip Select Pin:
ST (SPI_CS#) Internal pull-up
NuvoTon (SCS#) Internal pull-up is disabled if the pin is part of the recognized host interface

TABLE

	TPM2.0	EVT		FVT		SIT and beyond	
1st	ST	ST33HTPH2E32AHC0	071.33232.0H03	ST33HTPH2X32AHC4	071.33232.0I03	ST33HTPH2X32AHD4	071.33232.0J03
2nd	NuvoTon	NPCT750LABYX	071.00750.0D03	NPCT750LABYX	071.00750.0D03	NPCT750LABYX	071.00750.0D03

TABLE 071.00750.0D03 071.33232.0J03 ~~071.09670.0I03~~

Pin No	TCG PTP Spec(V38)	NuvoTon NPCT750LABYX	ST Micro ST33HTPH2X32AHD4	Infineon SLB9670VQ2.0 FW7.63
1	VDD	VSB	NC	VDD
2	GND	NC	GND	GND
3	NC	NC	NC	NC
4	GPIO	GPIO/PP	PP	NC
5	NC	NC	NC	NC
6	GPIO	GPIO3	NC	GPIO
7	GPIO	NC	GPIO	PP
8	VDD	VHIO	NC	VDD
9	NC	NC	NC	GND
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	GPIO4	NC	NC
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	GND	NC	NC
17	SPI_RST#	RST#	SPI_RST#	RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#	PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#	CS#
21	MOSI	MOSI/GPIO7	MOSI	MOSI
22	VDD	VHIO	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO0	NC	NC
30	SCL/GPIO0	SCL/GPIO1	NC	NC
31	NC	NC	NC	NC
32	NC	NC	NC	GND

LBB-2

緯創資通 Wistron Corporation
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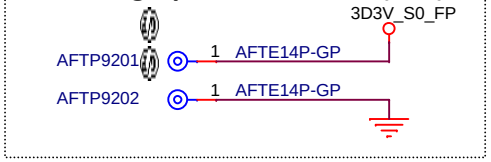
Title: INT IO (TPM 2.0)

Size: A3 | Document Number: Bumblebee-2 | Rev: 1

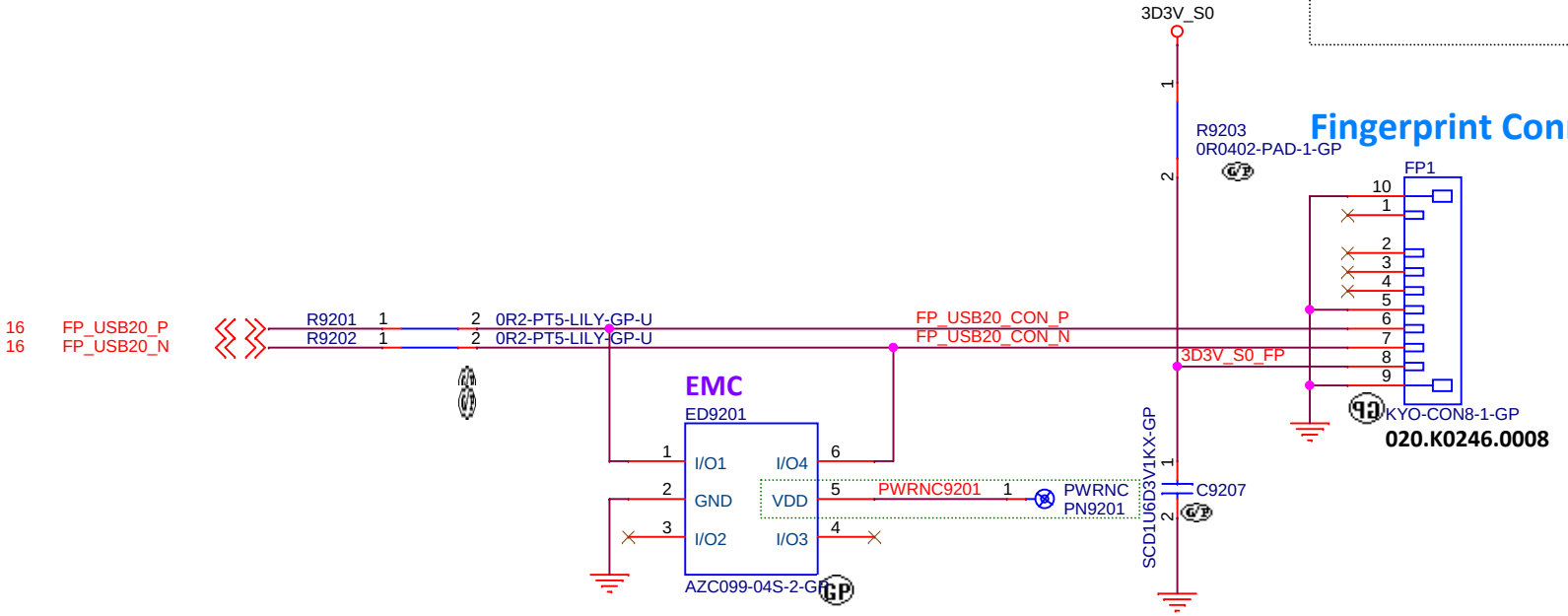
Date: Tuesday, March 03, 2020 | Sheet 91 of 106

BB2_EVT_MAIN_W003
BB2_FVT_MAIN_W007
BB2_SVT_MAIN_W003

Near Fingerprint Connector (FP1)

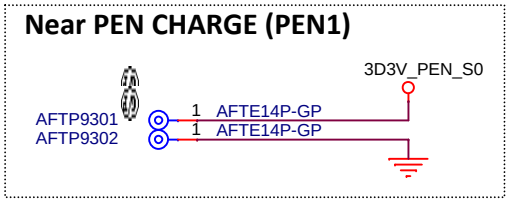


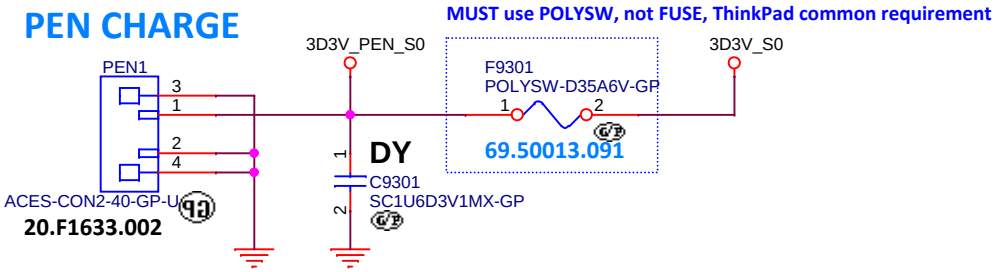
Fingerprint Connector



LBB-2

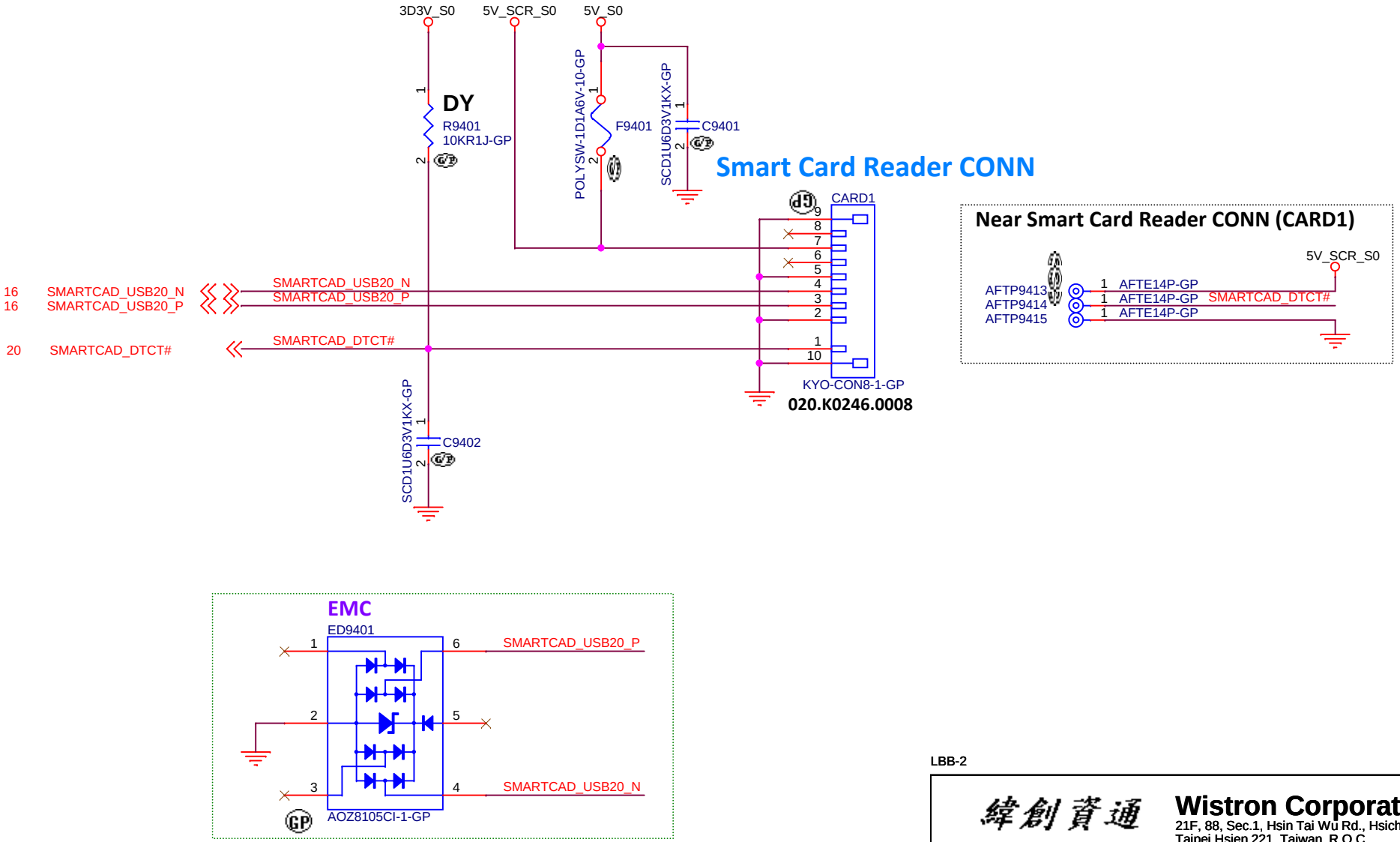
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *INT IO (FINGERPRINT)*		
Size: A4	Document Number: **Bumblebee-2**	Rev: **1**
Date: Tuesday, March 03, 2020	Sheet 92 of 106	





LBB-2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *EXT IO (ACTIVE PEN)*		
Size: A4	Document Number: **Bumblebee-2**	Rev: **1**
Date: Tuesday, March 03, 2020	Sheet 93 of 106	



LBB-2

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

EXT IO (SMART CARD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

EXT IO (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

Date: Tuesday, March 03, 2020 Sheet 95 of 106

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: COMMERCIAL (RSVD)

Size	Document Number	Rev
A4	Bumblebee-2	1

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Title: COMMERCIAL (RSVD)

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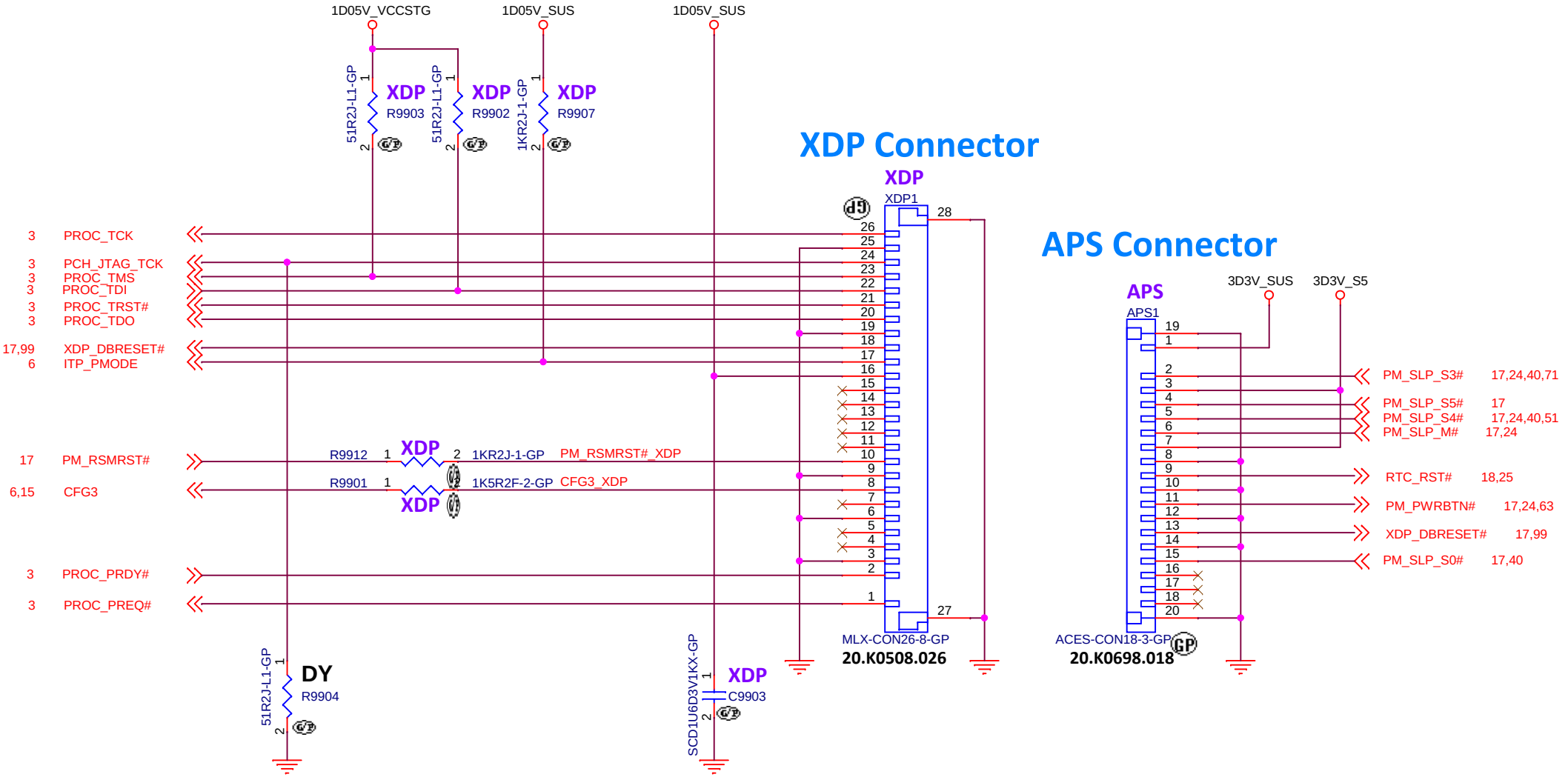
Main Func = Debug



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Title: ***DEBUG (XDP/APS)***

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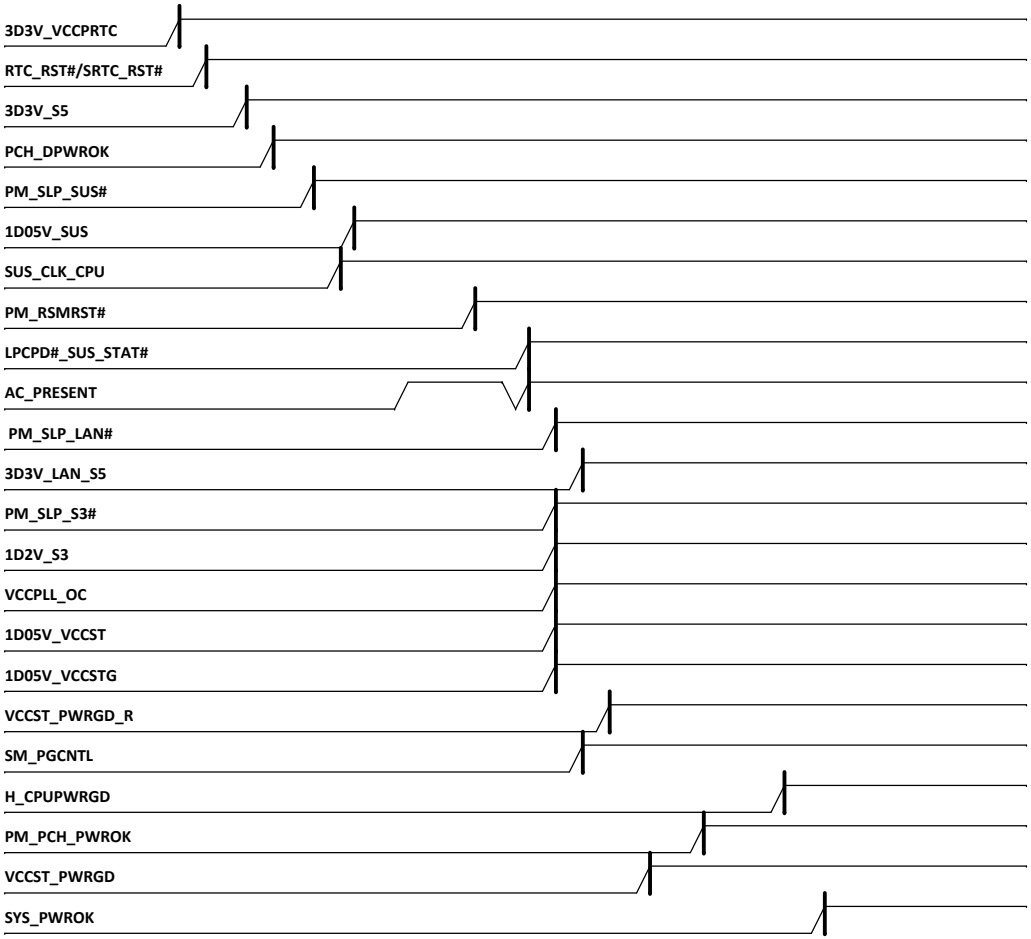
Intel-Power Up Sequence

#607109_CML_U_PDG_Rev1p2_P.629

(AC mode)



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Title: ***POWER SEQUENCE***		
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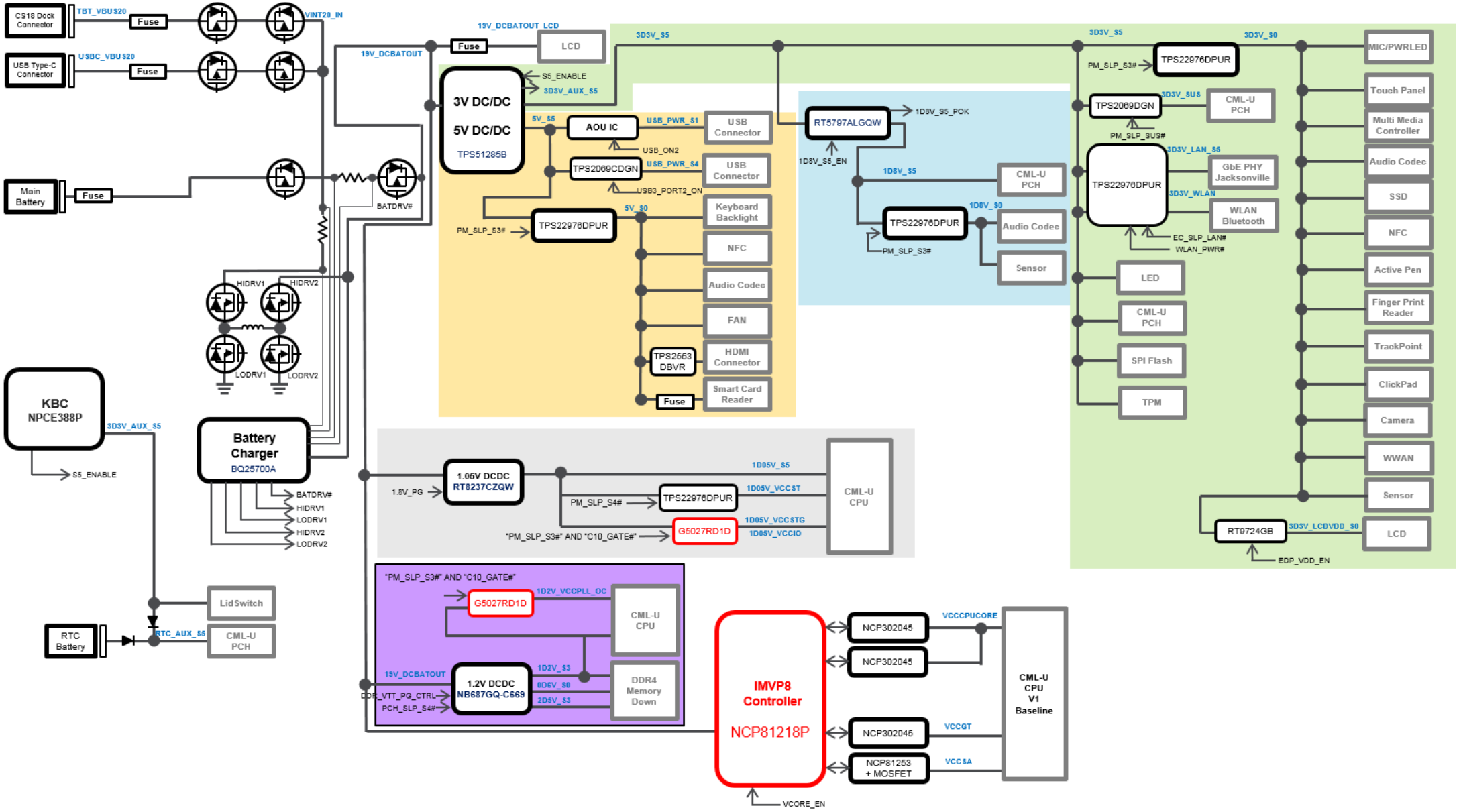

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Title: **POWER BLOCK DIAGRAM**

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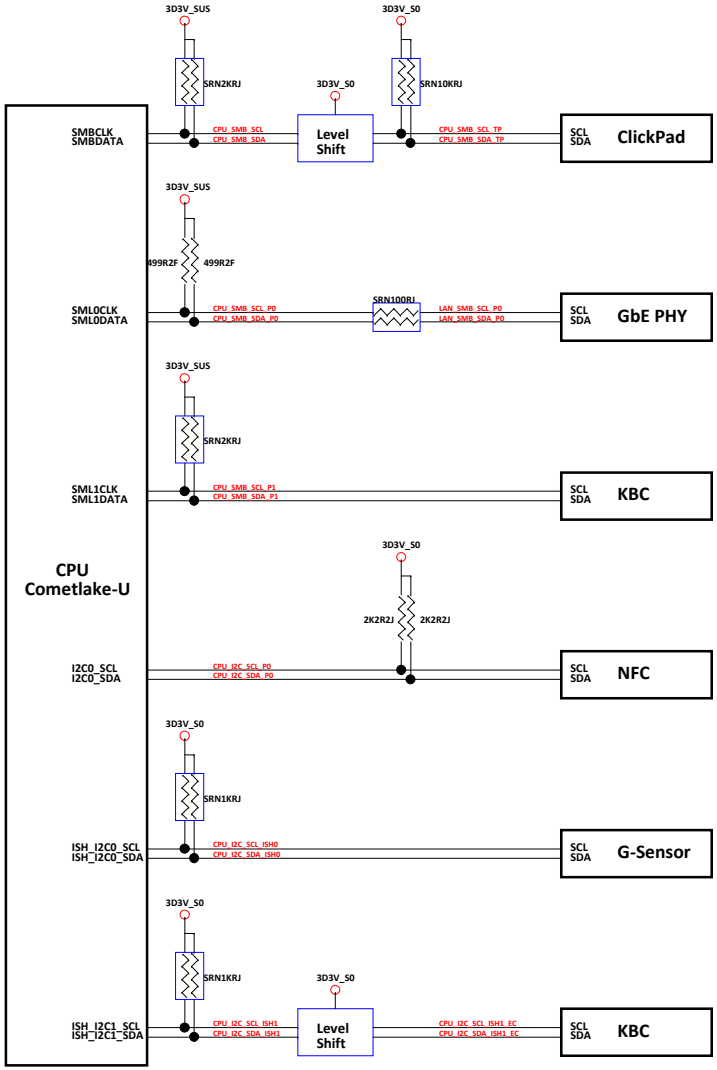
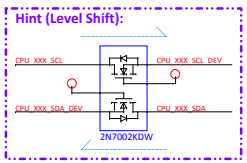
PCH SMBus/I2C Block Diagram





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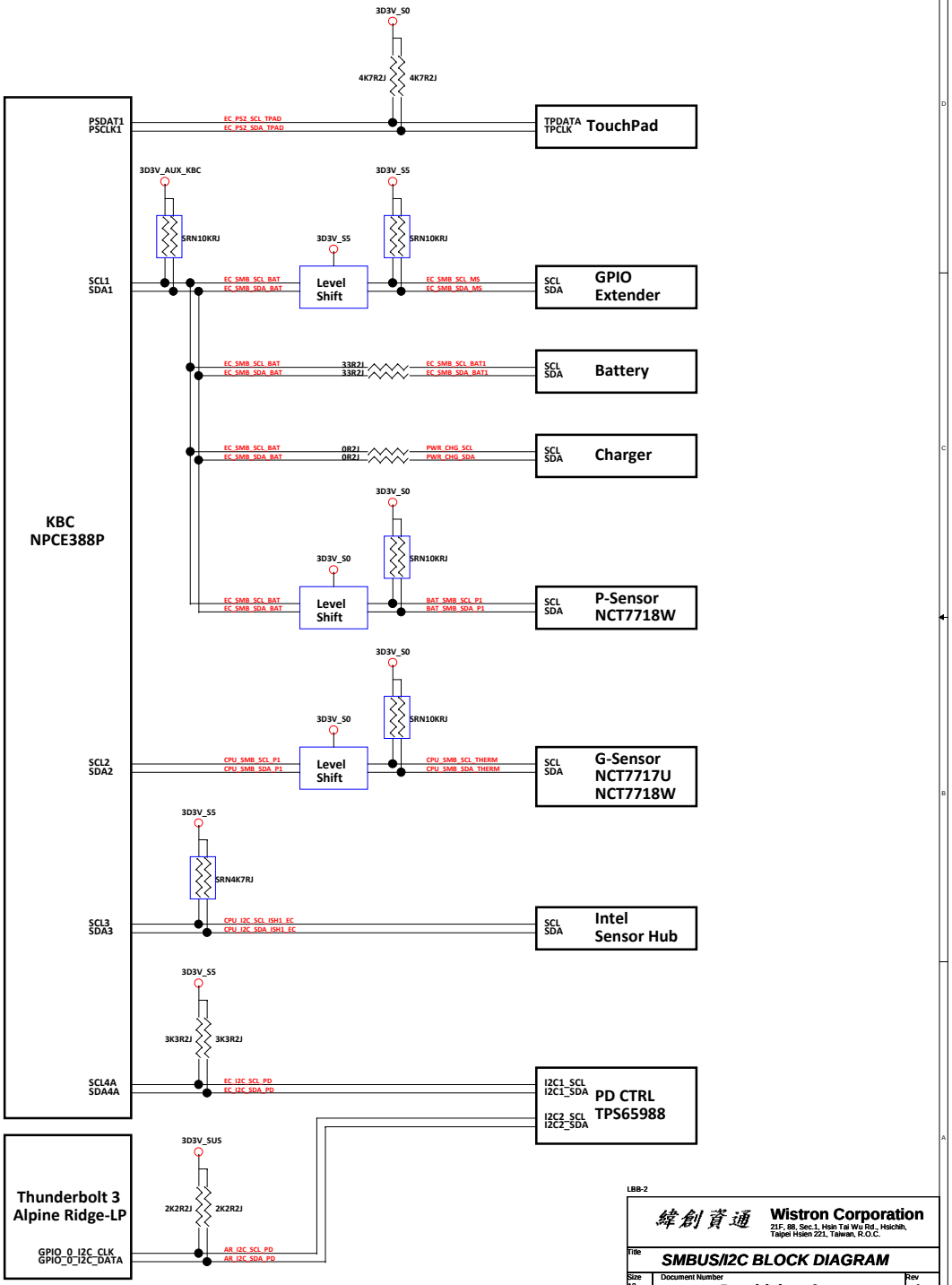

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Title: SMBUS/I2C BLOCK DIAGRAM

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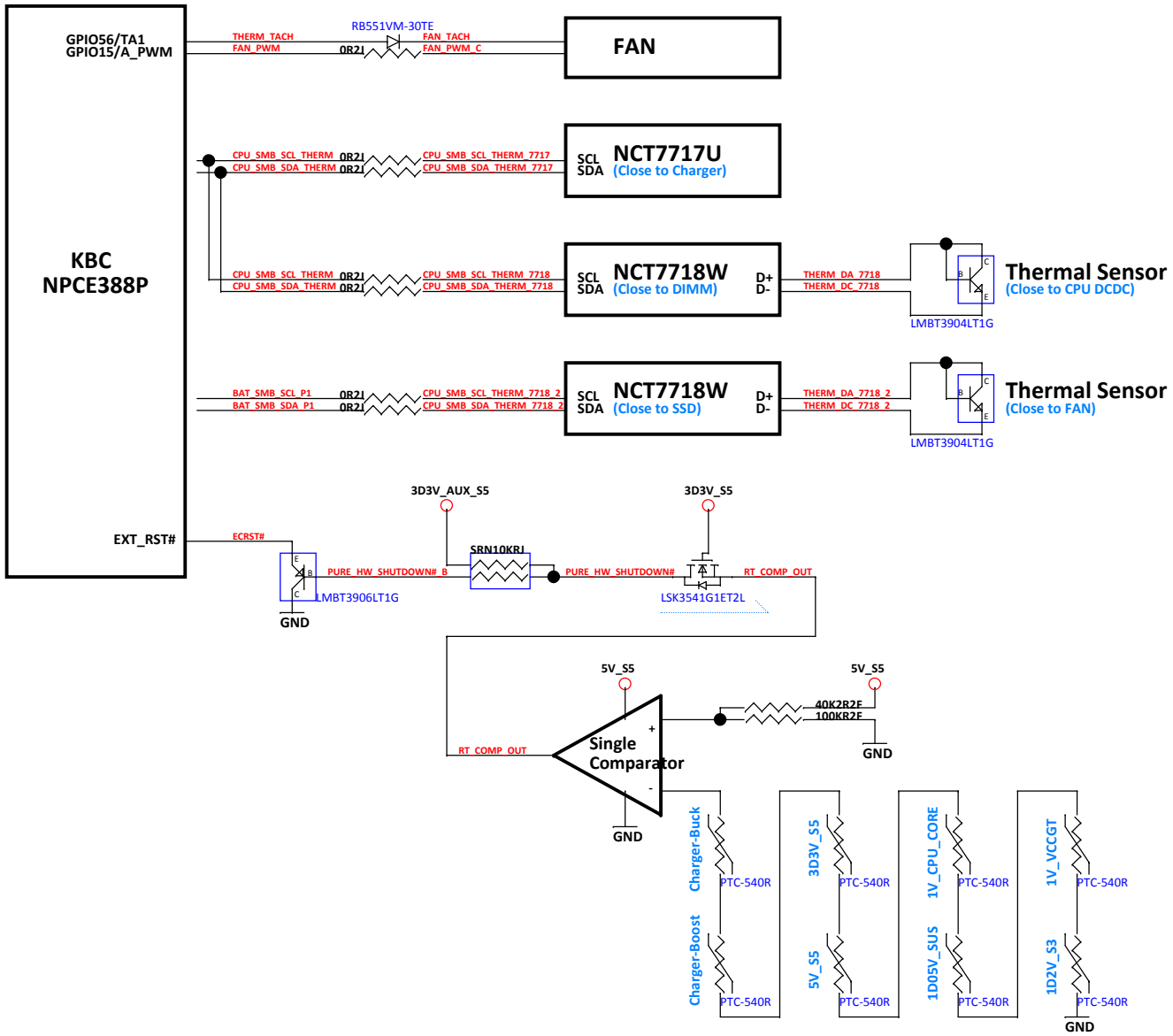
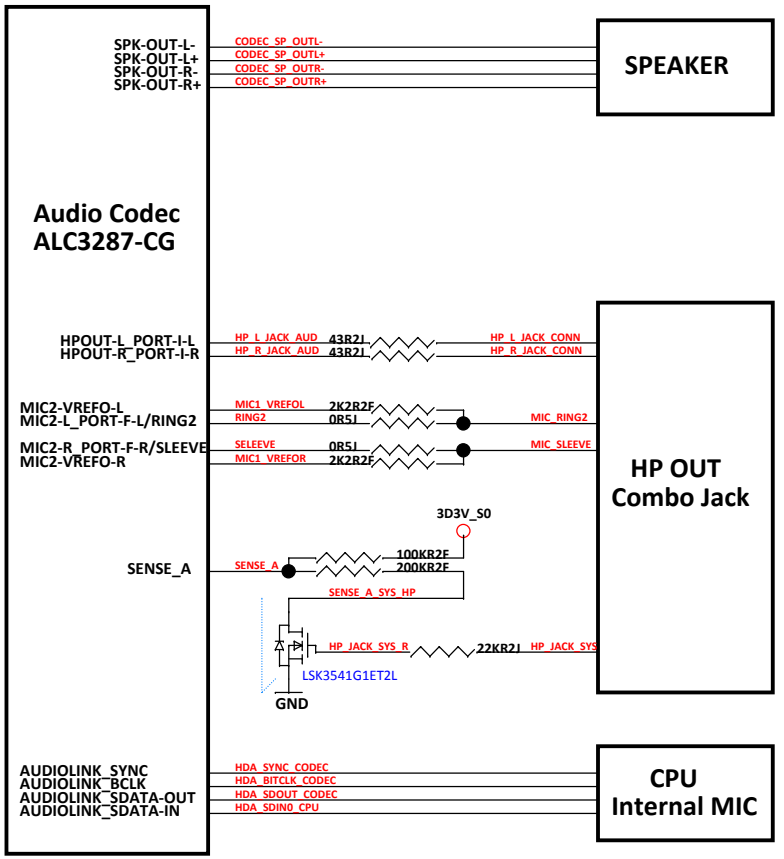
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM		
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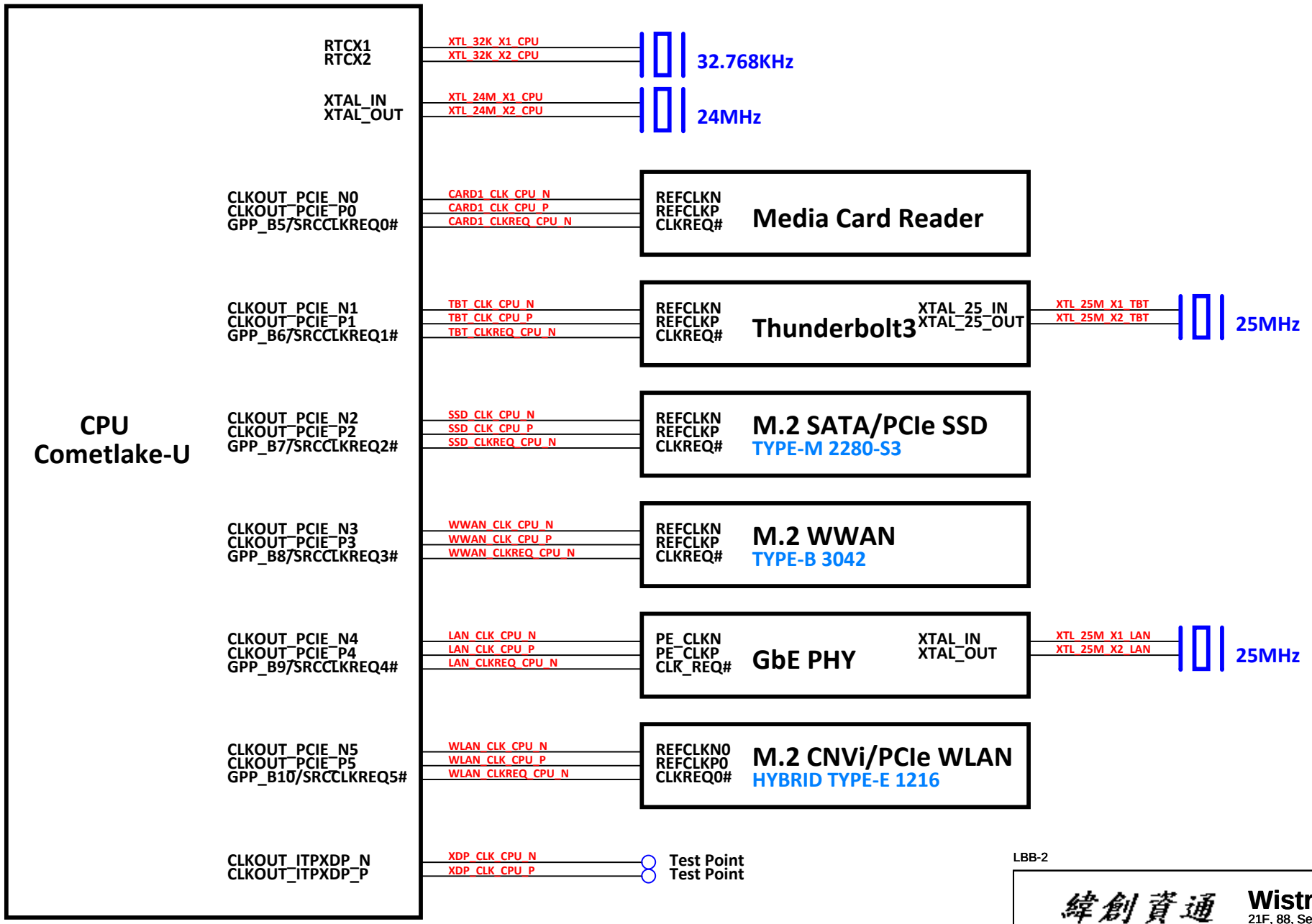

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Title: ***CLK BLOCK DIAGRAM***

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