FP8_GARNETT Block Diagram

PCB STACK UP 8L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : In2
- LAYER 5 : SVCC
- LAYER 7 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT

Max 4GB

DDR3 SO-DIMM Page:16 — DDR3 800MHz
DDR3 8x1Rx8 1G Page:17~19 — DDR3 800MHz

AMDGENEVA CPU
ASB2 PACKAGE
27 x 27mm 812 Balls
TDP~15W
Page:3~6

HyperTransport Link 16x16(HT_LINK)
Remove

11.6" LED Panel Page:21 — LVDS
CRT Page:25 — RGB
HDMI Page:24 — HDMI

AMD RS880M
21 x 21 mm
FCBGA 528 Balls
TDP~7.5W
Page: 7~10

G sensor

PCIE → 10/100M LAN RTL8103EL 23

PCIEx4(A_LINK)

32.768KHz 25MHz

USB CONN X 3 27 — Port0,1,2 — USB
CCD CONN 21 — Port3
BT CONN 28 — Port6
Card Reader RTS5159 25 — Port7
SIM Card 26 — WWAN 26 — Port4

AMD SB820
23 x 23 mm
FCBGA 605 Balls
TDP~4W
Page: 11~15

PCIE

USB Port5 → WLAN 26
SATA0 → 2.5"HDD&SSD 24
HDA → AUDIO CODEC IDT 92HD80 20

32.768KHz
LPC
EC KB3926 D2 29

HP/MIC COMBO JACK 20
MIC Digital 20
Int SPK 20

K/B Con. 28
Touch Pad Con. 28
SPI Flash 29

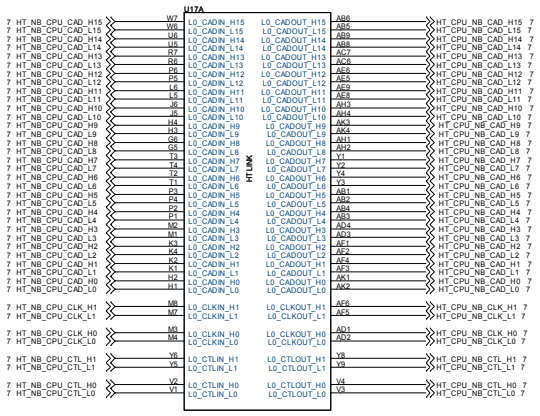
Quanta Computer Inc.
PROJECT : FP8
Size: Document Number: BLOCK DIAGRAM — Rev 1A
Date: Thursday, February 11, 2010 Sheet 1 of 41

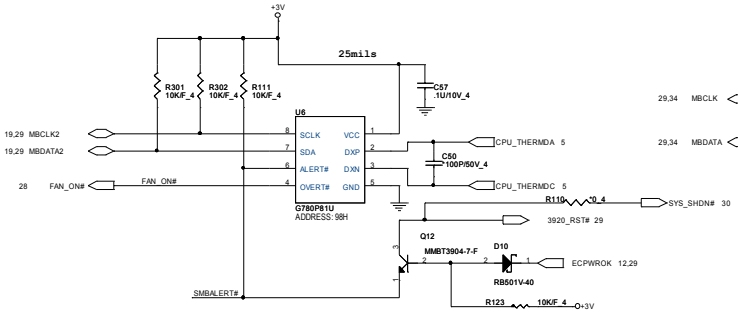
Quanta Computer Inc.

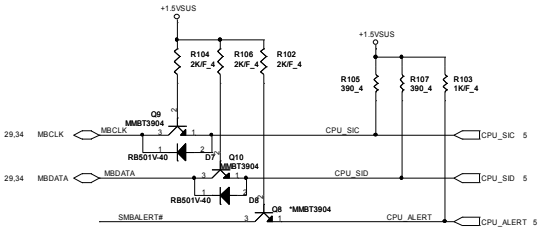
PROJECT : FP8

Size	Document Number	Rev
	Index	1A

Date: Thursday, February 11, 2010 Sheet 2 of 41







Quanta Computer Inc.

PROJECT : FP8

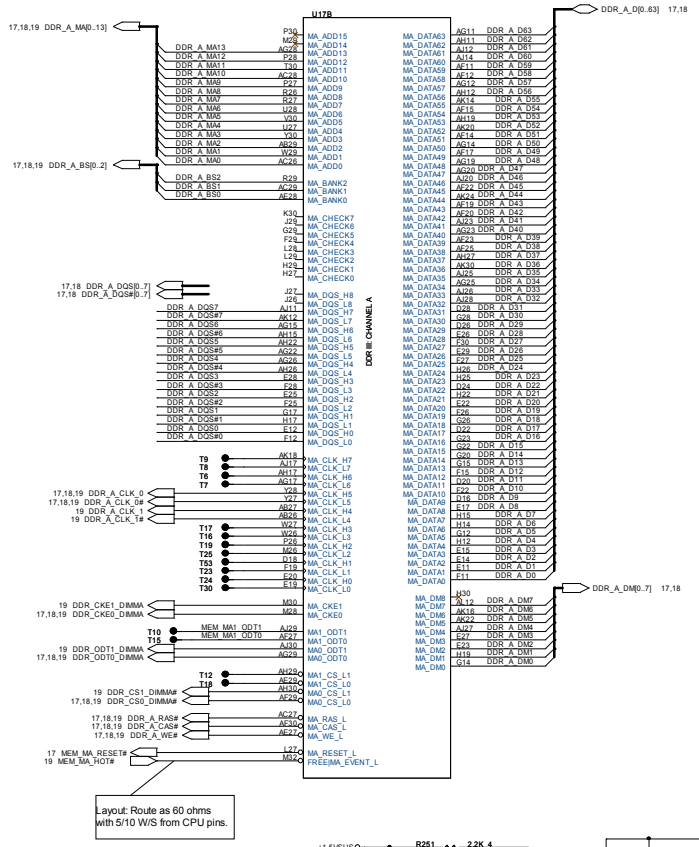
Size	Document Number	Rev
	AMD ASB2 HT LINK/THERMAL	1A

Date: Thursday, February 11, 2010 Sheet 3 of 41

AMD Processor DDR3 Memory Interface

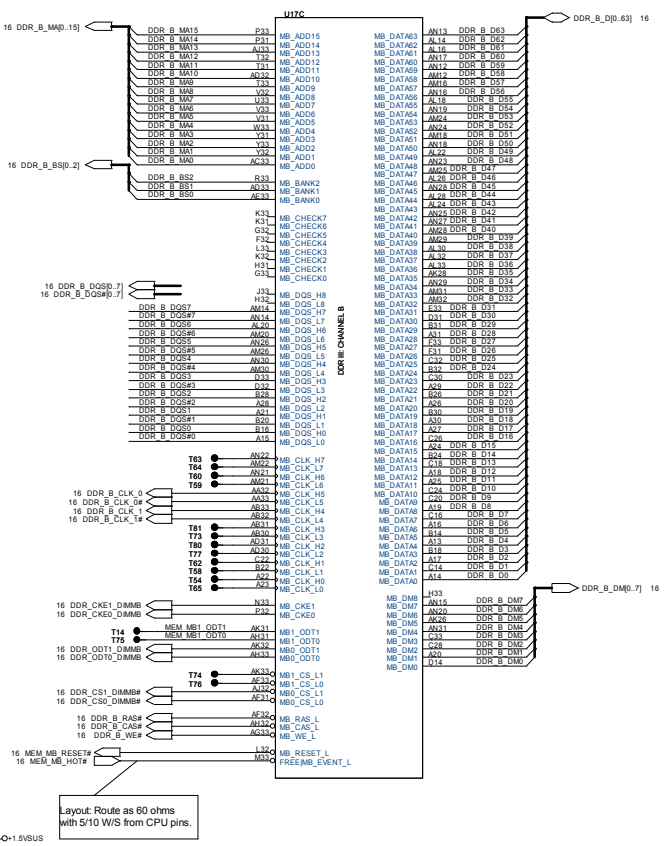
04

Channel-A to Solderdown MEM

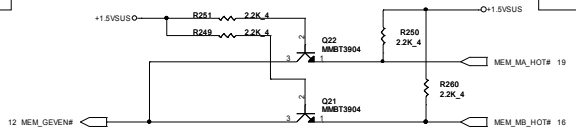


Layout: Route as 60 ohms with 5/10 W/S from CPU pins.

Channel-B to SODIMM Connector

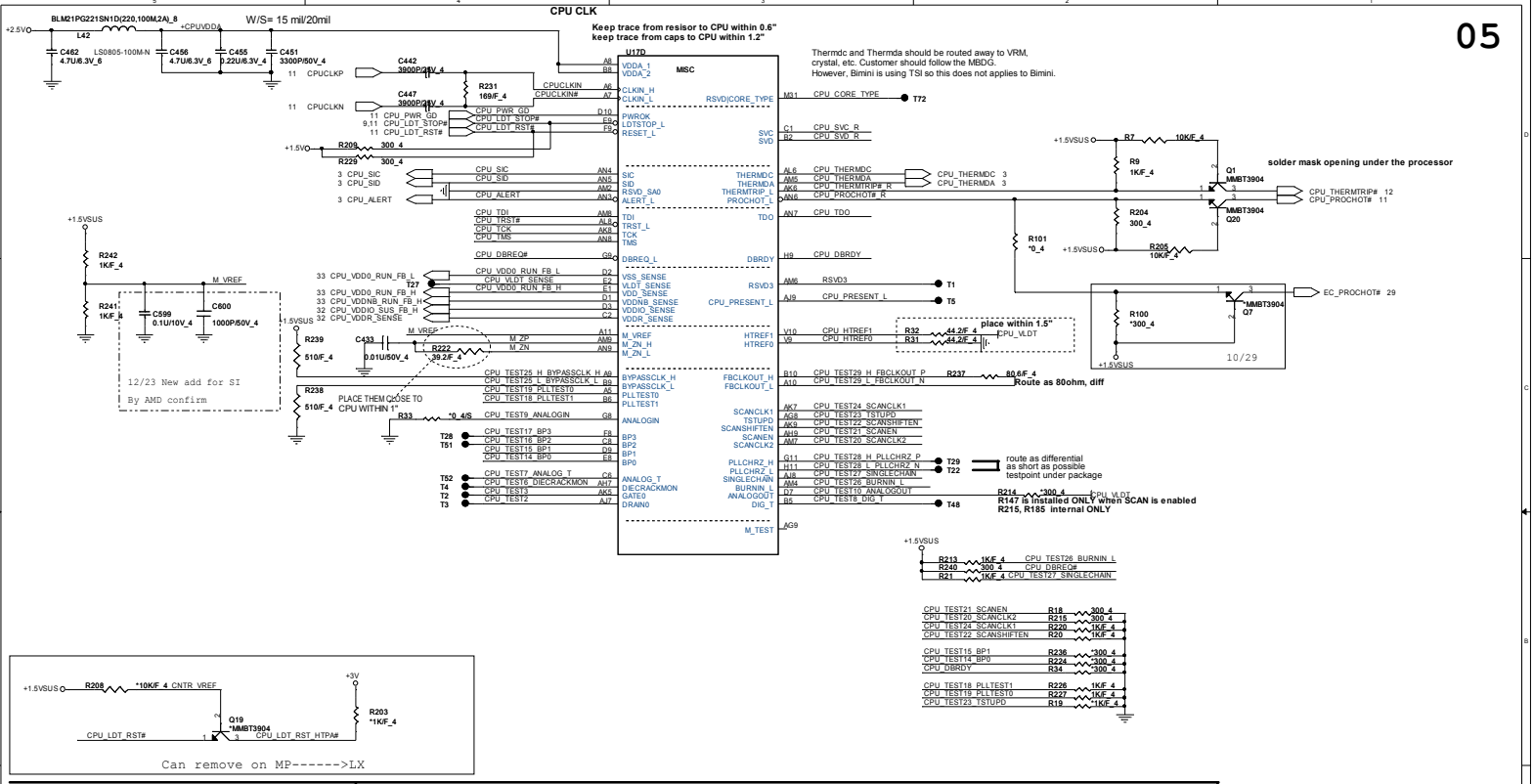


Layout: Route as 60 ohms with 5/10 W/S from CPU pins.

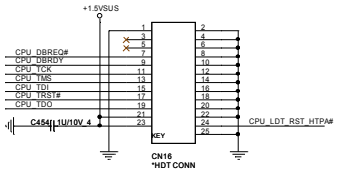


Quanta Computer Inc.		
PROJECT : FP8		
Size	Document Number: AMD ASB2 CPU(DDR3 MEM I/F)	Rev: 1A
Date: Thursday, February 11, 2010	Sheet 4 of 41	

CPU CLK



HDT Connector

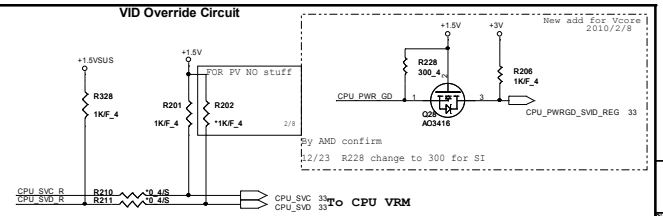


VID Override Circuit

Note:
To override VID,
Remove R192, R194, R196, install R165
set VID via SW100

SVC	SVD	BOOT VOLTAGE(VDD) (CPU/VRM_PRO# = VCC/GND)	(CPU/VRM_PRO# = OPEN)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

VID OVERIDE TABLE (VDD)

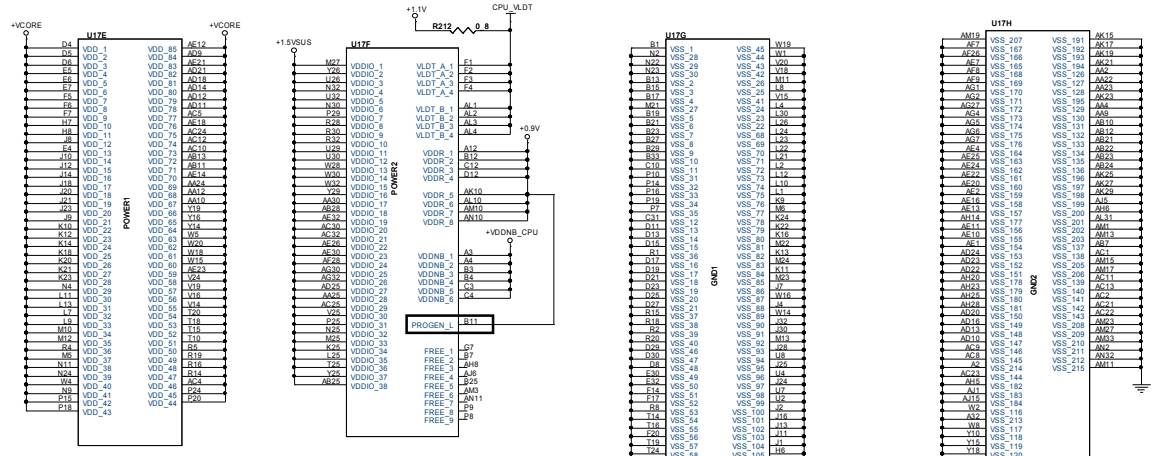


Quanta Computer Inc.

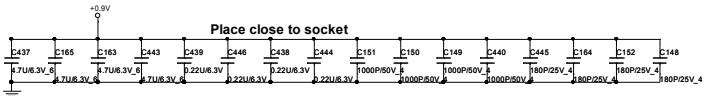
PROJECT : FP8

Size	Document Number	Rev
	AMD ASB2 CPU(CTRL&DEBUG)	1A

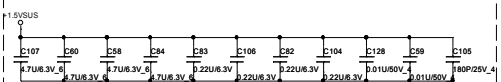
Date: Thursday, February 11, 2010 Sheet 5 of 41



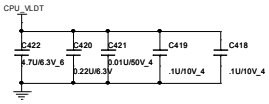
+1.1V or +1.2V => CPU_VLDT
+0.9V => CPU_VDDR
+1.5V_SUS => CPU_VDDIO_SUS
CPU_VCORE => CPU_VDD_RUN



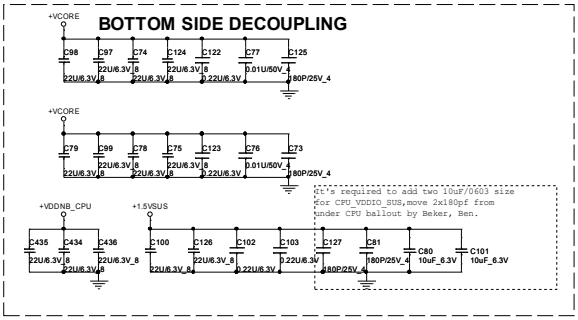
DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



PROCESSOR POWER AND GROUND



BOTTOM SIDE DECOUPLING



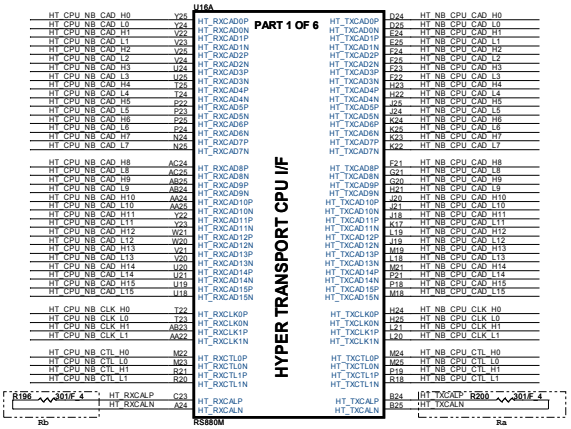
Quanta Computer Inc.
PROJECT : FP8

Size	Document Number	Rev
	AMD ASB2 CPU(PWR&GND)	1A

Date: Thursday, February 11, 2010 Sheet 6 of 41

+1.8V 9,10,12,22,35
+1.1V 6,8,9,10,14,22,31

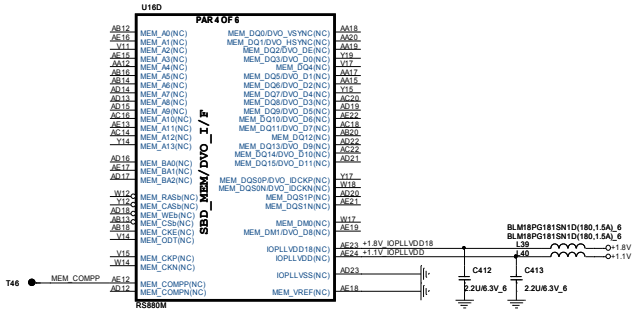
HT_CPU_NB_CAD_H[15..0]	HT_CPU_NB_CAD_H[15..0]	3
HT_CPU_NB_CAD_L[15..0]	HT_CPU_NB_CAD_L[15..0]	3
HT_CPU_NB_CLK_H[1..0]	HT_CPU_NB_CLK_H[1..0]	3
HT_CPU_NB_CLK_L[1..0]	HT_CPU_NB_CLK_L[1..0]	3
HT_CPU_NB_CTL_H[1..0]	HT_CPU_NB_CTL_H[1..0]	3
HT_CPU_NB_CTL_L[1..0]	HT_CPU_NB_CTL_L[1..0]	3
HT_NB_CPU_CAD_H[15..0]	HT_NB_CPU_CAD_H[15..0]	3
HT_NB_CPU_CAD_L[15..0]	HT_NB_CPU_CAD_L[15..0]	3
HT_NB_CPU_CLK_H[1..0]	HT_NB_CPU_CLK_H[1..0]	3
HT_NB_CPU_CLK_L[1..0]	HT_NB_CPU_CLK_L[1..0]	3
HT_NB_CPU_CTL_H[1..0]	HT_NB_CPU_CTL_H[1..0]	3
HT_NB_CPU_CTL_L[1..0]	HT_NB_CPU_CTL_L[1..0]	3



10/22

If the side-port memory interface is not used, make sure that:
- The memory interface I/O power (VDD_MEM) is connected to GND.
- The memory interface I/O transform power (VDD18_MEM) is connected to GND plane (preferred) or connected to 1.8 V.
- The memory interface compensation pins (MEM_COMPP, MEM_COMPN) for N and P channel devices are left not connected.
- The memory interface reference voltage MEM_VREF is connected to GND or left not connected.
- The memory interface PLL power IOPLLVDD18 is connected to 1.8 V and IOPLLVDD is connected to 1.1 V.
- The memory interface enable strap HSYNC is not connected to GND.

This block is for UMA only , DIS can remove all component



Modify as below:

page 10:

1.VDD_MEM connected to gnd

2.VDD18_MEM connected to gnd

Page 7

1.MEM_COMPP, MEM_COMPN are left not connected

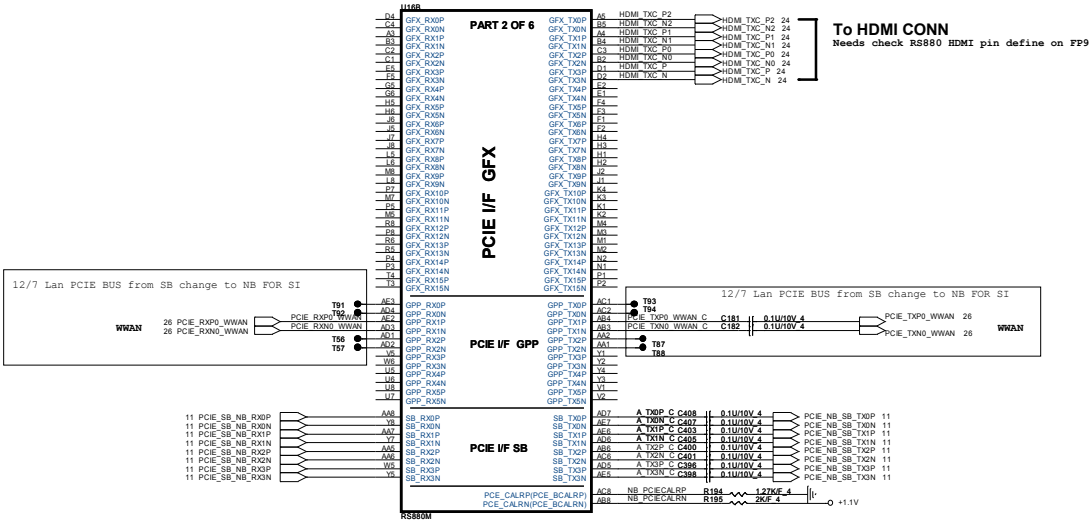
2.MEM_VREF is connected to GND or left not connected.

3.IOPLLVDD18 is connected to 1.8 V and IOPLLVDD is connected to 1.1 V.

Page 9

1.HSYNC_COM connected to pull high +3V

Quanta Computer Inc.			
PROJECT : FP8			
Size	Document Number: RS880M HT IF/SIDE PORT		Rev: 1A
Date: Thursday, February 11, 2010	Sheet 7 of 41		



RS880 Display Port Support (muxed on GFX)

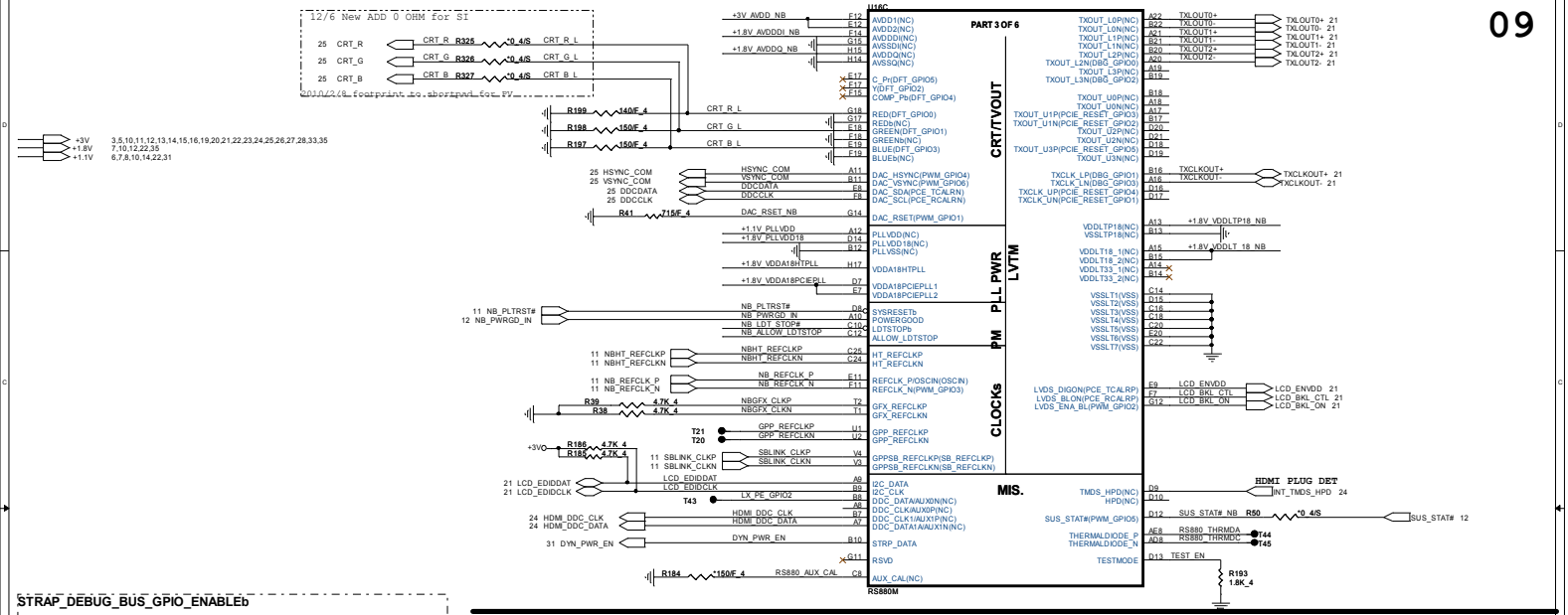
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

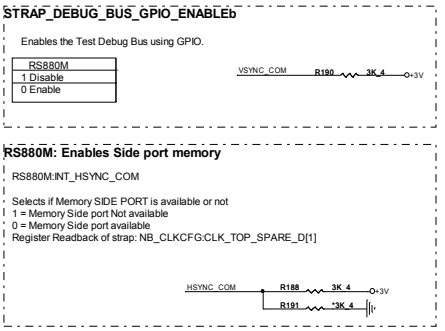
Quanta Computer Inc.

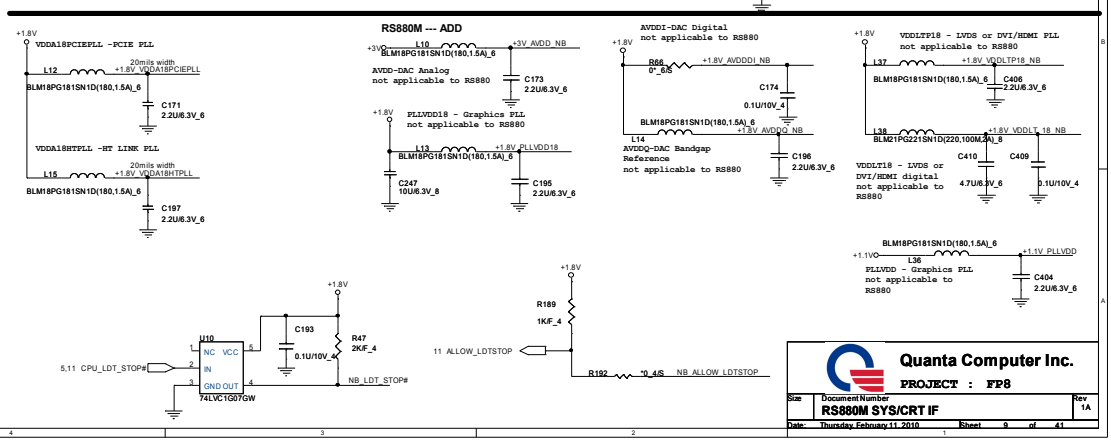
PROJECT : FP8

Size	Document Number	Rev
	RS880M PCIE	1A

Date: Thursday, February 11, 2010 Sheet 8 of 41





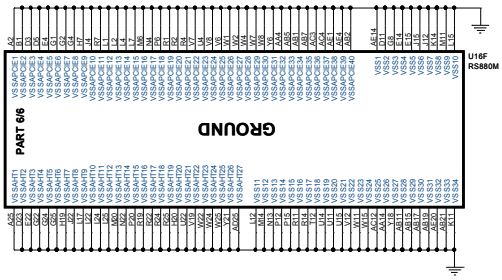


Quanta Computer Inc.

PROJECT : FP8

Size	Document Number	Rev
	RS880M SYS/CRT IF	1A

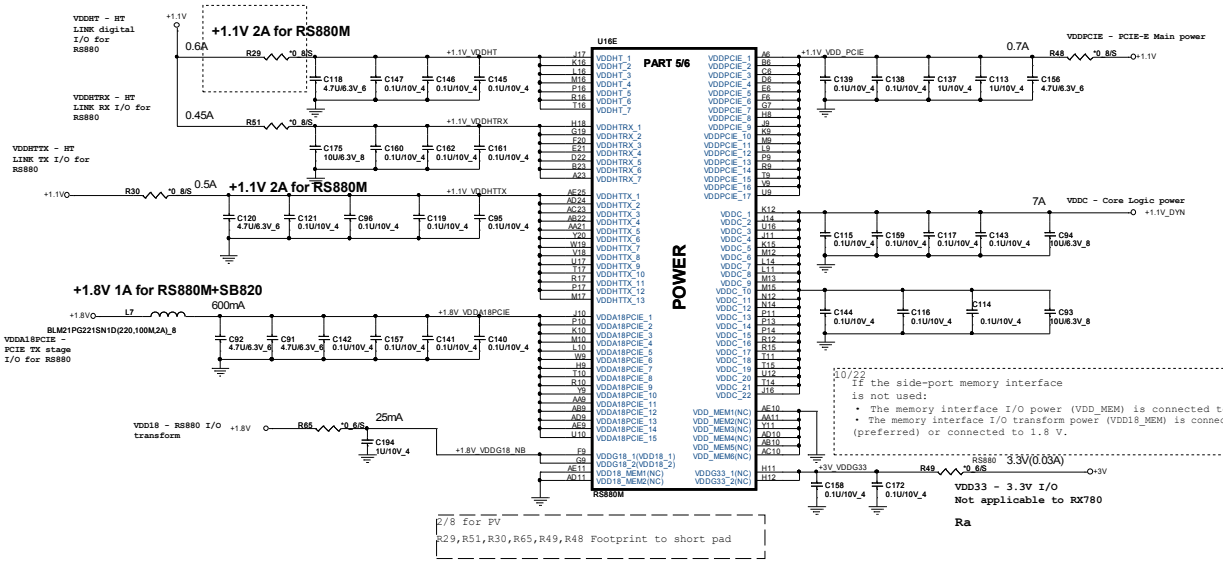
Date: Thursday, February 11, 2010 Sheet 9 of 41



RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

+1.1V_DYN 31
+3V 3,5,9,11,12,13,14,15,16,19,20,21,22,23,24,25,26,27,28,33,35
+1.1V 6,7,8,9,14,22,31
+1.8V 7,9,12,22,35



Quanta Computer Inc.			
PROJECT : FP8			
Size	Document Number		Rev
	RS880M PWR		1A
Date: Thursday, February 11, 2010		Sheet 10 of 41	

+1.1V_PCIE_VDDR 14

+3VS5 12,13,14,15,29,35
+3VPCU 21,22,25,26,27,28,29,30,31,34,35

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U7007

To RS880

U18A

SB800 Part 1 of 5

PCI EXPRESS INTERFACES

PCIE_RST# A_RST#

NB_PLTRST# R234 33_4 A_RST#

PCIE_SB_NB_RX0P	C417	0.1U/10V_4	A_RX0P_C	AD26
PCIE_SB_NB_RX0N	C416	0.1U/10V_4	A_RX0N_C	AD27
PCIE_SB_NB_RX1P	C426	0.1U/10V_4	A_RX1P_C	AC26
PCIE_SB_NB_RX1N	C425	0.1U/10V_4	A_RX1N_C	AC29
PCIE_SB_NB_RX2P	C414	0.1U/10V_4	A_RX2P_C	AB29
PCIE_SB_NB_RX2N	C415	0.1U/10V_4	A_RX2N_C	AB28
PCIE_SB_NB_RX3P	C423	0.1U/10V_4	A_RX3P_C	AB26
PCIE_SB_NB_RX3N	C424	0.1U/10V_4	A_RX3N_C	AB27

PCIE_NB_SB_TX0P	AE24	A_RX0P
PCIE_NB_SB_TX0N	AE23	A_RX0N
PCIE_NB_SB_TX1P	AD25	A_RX1P
PCIE_NB_SB_TX1N	AD24	A_RX1N
PCIE_NB_SB_TX2P	AC24	A_RX2P
PCIE_NB_SB_TX2N	AC25	A_RX2N
PCIE_NB_SB_TX3P	AB25	A_RX3P
PCIE_NB_SB_TX3N	AB24	A_RX3N

+1.1V_PCIE_VDDR — R67 590/F_4 — R68 2.0K/F_4 — PCIE_CALRP_SB AD29 — PCIE_CALRP — PCIE_CALRN AB29 — PCIE_CALRN

LAN / WLAN

23 PCIE_TXP2_LAN	C310	0.1U/10V_4	PCIE_TXP2_LAN_C	AA28
23 PCIE_TXN2_LAN	C309	0.1U/10V_4	PCIE_TXN2_LAN_C	AA29
26 PCIE_TXP1_WLAN	C187	0.1U/10V_4	PCIE_TXP1_WLAN_C	Y29
26 PCIE_TXN1_WLAN	C188	0.1U/10V_4	PCIE_TXN1_WLAN_C	Y28

GPP_TX0P	Y26	PCIE_RXP2_LAN	23 PCIE_RXP2_LAN
GPP_TX0N	Y27	PCIE_RXN2_LAN	23 PCIE_RXN2_LAN
GPP_TX1P	W28	PCIE_RXP1_WLAN	26 PCIE_RXP1_WLAN
GPP_TX1N	W29	PCIE_RXN1_WLAN	26 PCIE_RXN1_WLAN
GPP_TX2P			
GPP_TX2N			
GPP_TX3P			
GPP_TX3N			

LAN / WLAN

GPP_RX0P	AA22	PCIE_RXP2_LAN
GPP_RX0N	Y21	PCIE_RXN2_LAN
GPP_RX1P	AA25	PCIE_RXP1_WLAN
GPP_RX1N	AA24	PCIE_RXN1_WLAN
GPP_RX2P	W23	
GPP_RX2N	Y24	
GPP_RX3P	W24	
GPP_RX3N	W25	

PCI CLKS

PCICLK0	W2	PCI_CLK0	T49 PCI_CLK_TPM 15
PCICLK1/GPO36	W1	PCI_CLK_TPM	
PCICLK2/GPO37	W3	PCI_CLK2	PCI_CLK2 15
PCICLK3/GPO38	W4	PCI_CLK3	PCI_CLK3 15
PCICLK4/14M_OSC/GPO39	Y1	PCI_CLK4	PCI_CLK4 15

STRAP Function

PCIRST# V2 PCIRST#_L R233 33_4 PCIRST# PCIRST# 26,29 To EC

C441 150P/50V_4

Debug STRAPs

AD0/GPIO0	AA1		
AD1/GPIO1	AA4		
AD2/GPIO2	AA3		
AD3/GPIO3	AB1		
AD4/GPIO4	AA5		
AD5/GPIO5	AB2		
AD6/GPIO6	AB5		
AD7/GPIO7	AA6		
AD8/GPIO8	AC2		
AD9/GPIO9	AC3		
AD10/GPIO10	AC4		
AD11/GPIO11	AC1		
AD12/GPIO12	AD1		
AD13/GPIO13	AD2		
AD14/GPIO14	AC6		
AD15/GPIO15	AE2		
AD16/GPIO16	AE1		
AD17/GPIO17	AF8		
AD18/GPIO18	AE3		
AD19/GPIO19	AF1		
AD20/GPIO20	AG1		
AD21/GPIO21	AF2		
AD22/GPIO22	AE9	AD23	AD23 15
AD23/GPIO23	AD9	AD24	AD24 15
AD24/GPIO24	AC11	AD25	AD25 15
AD25/GPIO25	AF6	AD26	AD26 15
AD26/GPIO26	AF4	AD27	AD27 15
AD27/GPIO27	AF3		
AD28/GPIO28	AH2		
AD29/GPIO29	AG2		
AD30/GPIO30	AH3		
AD31/GPIO31	AA8		

PCI INTERFACE

All the PCI bus has build-in Pull-UP/Down resistors

CBE0#	AD5		
CBE1#	AD8		
CBE2#	AA10		
CBE3#	AC8		
FRAME#	AB9		
DEVSEL#	AJ3		
IRDY#	AC7		
TRDY#	AC5		
PAR	AF5		
STOP#	AE6		
PERR#	AE4	SERR#	SERR# 29
SERR#	AE11		
REQ0#	AH5		
REQ1#/GPIO40	AH4		
REQ2#/CLK_REQ8#/GPIO41	AC12	SB_GPIO42	T33
REQ3#/CLK_REQ5#/GPIO42	AD12		
GNT0#	AJ5		
GNT1#/GPO44	AH6		
GNT2#/GPO45	AB12		
GNT3#/CLK_REQ7#/GPIO46	AB11	CLKRUN#	CLKRUN# 29
CLKRUN#	AD7	LOCK#	T47
LOCK#			
INTE#/GPIO32	AJ6		
INTF#/GPIO33	AG6		
INTG#/GPIO34	AG4		
INTH#/GPIO35	AJ4	INTG#	24

CLOCK GENERATOR

SBLINK_CLKP	M23	SBLINK_CLKP	9 SBLINK_CLKP
SBLINK_CLKN	P23	SBLINK_CLKN	9 SBLINK_CLKN
PCIE_RCLKP/NB_LNK_CLKP			
PCIE_RCLKN/NB_LNK_CLKN			
NB_DISP_CLKP	U29	NB_REFCLK_P	9 NB_REFCLK_P
NB_DISP_CLKN	U28	NB_REFCLK_N	9 NB_REFCLK_N
NB_HT_CLKP	T26	NBHT_REFCLKP	9 NBHT_REFCLKP
NB_HT_CLKN	T27	NBHT_REFCLKN	9 NBHT_REFCLKN
CPU_HT_CLKP	V21	CPUCLKP	5 CPUCLKP
CPU_HT_CLKN	T21	CPUCLKN	5 CPUCLKN
SLT_GFX_CLKP	V23		
SLT_GFX_CLKN	T23		
GPP_CLK0P	L29	CLK_PCIE_WLAN_0P	26 CLK_PCIE_WLAN_0P
GPP_CLK0N	L28	CLK_PCIE_WLAN#_0N	26 CLK_PCIE_WLAN#_0N
GPP_CLK1P	N29		
GPP_CLK1N	N28		
GPP_CLK2P	M29		
GPP_CLK2N	M28		
GPP_CLK3P	T25	CLK_PCIE_LAN	23 CLK_PCIE_LAN
GPP_CLK3N	V25	CLK_PCIE_LAN#	23 CLK_PCIE_LAN#
GPP_CLK4P	L24	CLK_PCIE_WWAN_4P	26 CLK_PCIE_WWAN_4P
GPP_CLK4N	L23	CLK_PCIE_WWAN#_4N	26 CLK_PCIE_WWAN#_4N
GPP_CLK5P	P25		
GPP_CLK5N	M25		
GPP_CLK6P	P29		
GPP_CLK6N	P28		
GPP_CLK7P	N26		
GPP_CLK7N	N27		
GPP_CLK8P	T29		
GPP_CLK8N	T28		

To RS880M / To RS880M / CPU_CLK / To WLAN Connector / To LAN Controller / To WWAN Connector

OSCCLK T31 L25 14M_25M_48M_OSC

25M_X1_1 — Y5 25MHz — C457 10P/50V_4 — C458 10P/50V_4 — R243 *0_4/S — R244 1M/F_4 — 25M_X1 L26 25M_X1 — 25M_X2 L27 25M_X2

LPC

LPCCLK0	H24	LPC_CLK0	LPC_CLK0 15
LPCCLK1	H26	LPC_CLK1	LPC_CLK1 15 To STRAPs Page
LAD0	J27	LPC_LAD0	LPC_LAD0 26,29
LAD1	J26	LPC_LAD1	LPC_LAD1 26,29
LAD2	H29	LPC_LAD2	LPC_LAD2 26,29
LAD3	H28	LPC_LAD3	LPC_LAD3 26,29
LFRAME#	G28	LPC_LFRAME#	LPC_LFRAME# 26,29
LDRQ0#	F26	LDRQ0#_SB	T32
LDRQ1#/CLK_REQ6#/GPIO49	AA18		
SERIRQ/GPIO48	AB19	LPC_SERIRQ	LPC_SERIRQ 29

R274 22_4 — R269 22_4 — PCLK_LPC_KB3920 29 — PCLK_LPC_DEBUG 26

C485 5.6P/50V_6 — C487 22P/50V_4

CPU

ALLOW_LDTSTP/DMA_ACTIVE#	G21	ALLOW_LDTSTOP	ALLOW_LDTSTOP_9
PROCHOT#	H21	CPU_PROCHOT#	CPU_PROCHOT# 5
LDT_PG	K19	CPU_PWR_GD	CPU_PWR_GD 5
LDT_STP#	G22	CPU_LDT_STOP#	CPU_LDT_STOP# 5,9
LDT_RST#	C24	CPU_LDT_RST#	CPU_LDT_RST# 5

R96 10K/F_4 +3VS5

RTC

32K_X1	C1	RTC_X1	RTC_X1
32K_X2	C2	RTC_X2	RTC_X2
RTCCLK	D2	RTC_CLK	R136 *10K/F_4 +3VS5
INTRUDER_ALERT#	B2	INTRUDER_ALERT#	T71
VDDBT_RTC_G	B1	+AVBAT	

R245 20M_6

RTC_CLK must ready refore RSMRST#

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

SB800 A11

+AVBAT — 20MIL — R98 499/F_4 — +3VRTC_1 — R99 10_4 — +3VRTC — 20MIL — 20MIL — C282 1U/10V_4

D5 RB500V-40 — D6 RB500V-40 — +3VPCU — +VCCRTC_2 — 20MIL — R86 1K/F_4 — +BAT

+AVBAT — 20MIL — G2 *SHORT_PAD1 — C467 0.1U/10V_4

CN17 RTC CONN

SMT request CN17 footprint change to 88266-020L-2P-R-SMT 12/17

+3V — C304 0.1U/10V_4 — U11 TC7SH08FU

23 LAN_PLTRST# — R117 33_4
26 MINI_PLTRST# — R116 33_4 — A_RST# R_4 — A_RST# — SB_GPIO_RST# 12

Add AND gate to reset all PCIE devices by AMD recommand

2/6/2010 Change to 10ppm for PV

Y4 32.768KHZ — C460 18P/50V — C459 18P/50V

Quanta Computer Inc.

PROJECT : FP8

Size	Document Number	Rev
	SB820 PCIE/LPC/CPU	1A

Date: Thursday, February 11, 2010 Sheet 11 of 41

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
Clock gen/Robson/TV tuner /DDR3/DDR3 thermal/Accelerometer
R81 2.2K_4 PCLK_SMB
R80 2.2K_4 PDAT_SMB

12/16 BIOS Request for SI
R329 *10K/F_4
23 LAN_Cable_detect
LAN_Cable_detect

12/16 New add for SI
R311 10K/F_4 SYS_RST#
R313 *10K/F_4 MCP_A20GATE
By AMD confirm

SB800 SB_TEST0,SB_TEST1,SB_TEST2 has internal 10K PD.

Add SB_GPIO_RST# form AMD recommand

SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R139 10K/F_4 SB_SMBCLK1
R137 10K/F_4 SB_SMBDATA1
R91 *10K/F_4

R92 300_4
9 NB_PWRGD_IN
R93 *0_4/S
WD_PWRGD

R135 2.2K_4 DNBSWON#
R138 4.7K_4 SUS_STAT#

R140 *10K/F_4
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

To Azalia
HD audio interface is 3.385 voltage

20 HDA_BITCLK
15 ACZ_SDOUT
20 HDA_SDATA_OUT
20 ACZ_SDATA_IN
20 HDA_SYNC
20 HDA_RESET#

C314 10P/50V_4
R131 33_4 ACZ_BCLK
R130 33_4 ACZ_SDOUT
C315 *10P/50V_4
R127 33_4 ACZ_SYNC
R128 33_4 ACZ_RST#

R141 10K/F_4 SB_PWRGD_IN
C317 *2.2U/6.3V_6
33 CPU_VRM8380_PG
3,29 ECPWROK
D12 BAT54A
NB/SB POWER GOOD CIRCUIT

+3V +3VS5 3,5,9,10,11,13,14,15,16,19,20,21,22,23,24,25,26,27,28,33,35
11,13,14,15,29,35

R315 10K/F_4 GBE_COL
R316 10K/F_4 GBE_CRS
R314 10K/F_4 GBE_MDIO
R317 10K/F_4 GBE_RXERR
R318 10K/F_4 GBE_PHY_INTR
12/16 AMD Datasheet definr it for SI

T70 SB_GPIO187
T69 SB_GPIO188
T79 SB_GPIO166
T78 SB_GPIO160

CN18 SB JTAG
C474 68p/50V_4 2010/2/11 BF For PV
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

U18D SB800 Part 4 of 5 SB800 A11

MEM_GEVEN# R#
SPI_CS3# SUS8#
SUS#
DNBSWON#
SB_PWRGD_IN
SUS_STAT#
SB_TEST0
SB_TEST1
SB_TEST2
MCP_A20GATE RCIN#
LAN_Cable_detect
SIO_EXT_SMI#
SIO_EXT_SCI#
SYS_RST#
PCIE_WAKE#
CPU_THERMTRIP#
WD_PWRGD
RSMRST#
WWAN_CLKREQ@#4
LAN_DISABLE#_SB
SB_GPIO_RST#
ACCLED_EN
ACZ_SPKR
PCLK_SMB
PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
WLAN_CLKREQ@#2
LX_VGA_REQ_R
WWAN_OFF#

PCI_PME#/GEVENT4#
R#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO90
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPIO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC
USB_RCOMP
CLK_48M_USB
USB_RCOMP_SB R85 11.8K/F_4
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
T68 T95 T96 T89 T90
USBP7+ 25 USBP7- 25 Card reader
USBP6+ 28 USBP6- 28 BLUETOOTH
USBP5+ 26 USBP5- 26 WLAN Min-Card
USBP4+ 26 USBP4- 26 WWAN CARD
USBP3+ 21 USBP3- 21 WEBCAM
USBP2+ 25 USBP2- 25
USBP1+ 25 USBP1- 25
USBP0+ 27 USBP0- 27
Right Side Conn.
Left Side Conn.
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it

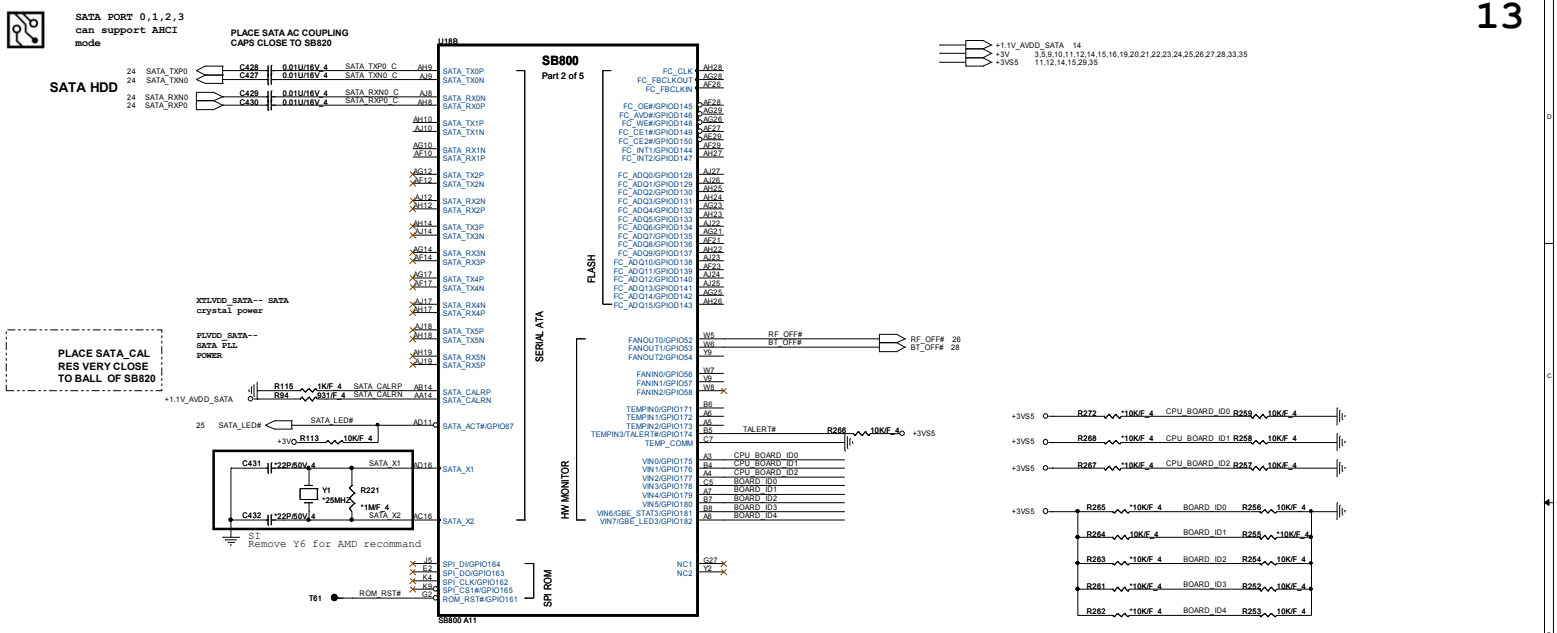
SCL2/GPIO193
SDA2/GPIO194
SCL3_LVGPIO195
SDA3_LVGPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
SB_SCLK2 R270 10K/F_4 +3VS5
SB_SDATA2 R83 10K/F_4
SB_SCLK3 R248 10K/F_4 +3VS5
SB_SDATA3 R246 10K/F_4
SB_GPIO199 R84 10K/F_4
SB_GPIO200 R271 2.2K_4 +3VS5

GPIO200 GPIO199
H,H = Reserved
H,L = SPI ROM
L,H = LPC ROM (Default)
L,L = FWH ROM

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226

SB_SCLK2 R320 *2.2K_4
SB_SDATA2 R319 *2.2K_4
SB_SCLK3 R322 *2.2K_4
SB_SDATA3 R321 *2.2K_4
SB_SMBCLK1 R324 *2.2K_4
SB_SMBDATA1 R323 *2.2K_4
12/16 reserve Pull down R for SI

Quanta Computer Inc.
PROJECT : FP8
Size Document Number SB820 ACPI/GPIO/USB Rev 1A
Date: Thursday, February 11, 2010 Sheet 12 of 41



BOARD ID Configuration

BOARD ID_[2:0]	
No on board MEM	0 0 0
Hynix 1333	0 0 1
Samsung 1333	0 1 0
Micron 1333	0 1 1
reserve	1 0 0
reserve	1 0 1
reserve	1 1 0
reserve	1 1 1

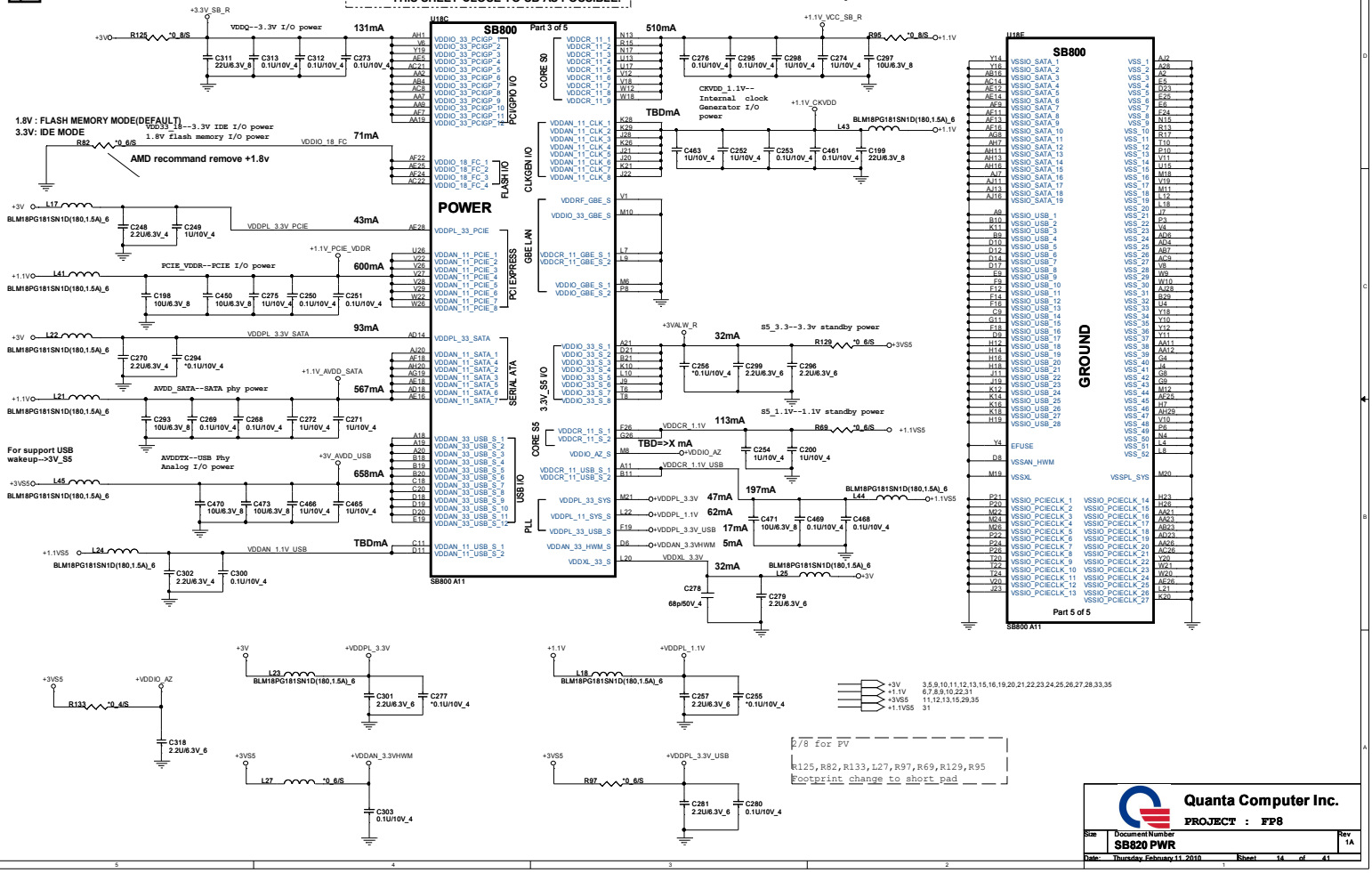
CPU_BOARD_ID_[2:0]	
reserve	0 0 0
reserve	0 0 1
reserve	0 1 0
reserve	0 1 1
reserve	1 0 0

BOARD ID_[4:3]	
FP8 1.0	0 0
FP8 1.1	0 1

Samsung 1333 128Mx8	Micron 1333 128Mx8	Hynix 1333 128Mx8
K4B1G0846E-HCH9	MT41J128M8JP-15E	H5TQ1G83BFR-H9C
573005-941	573005-641	573005-341
QCI:AKD5LZET501	QCI: AKD5LZSTL06	QCI: AKD5LZQTW00
TOP:AKD5LZET502	TOP:AKD5LZSTL05	TOP: AKD5LZQTW01

Quanta Computer Inc.
PROJECT : FP8
Size: Document Number: SB820 SATA/IDE/SPI/HWM
Rev: 1A
Date: Thursday, February 11, 2010 Sheet 13 of 41

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

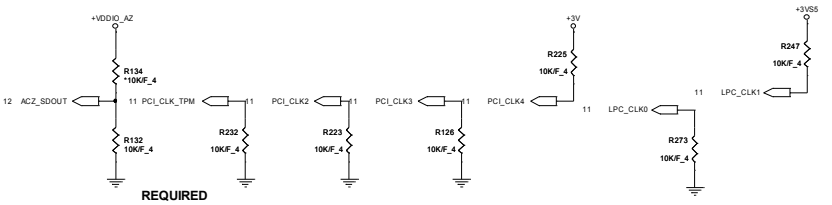


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need

+VDDIO_AZ 14
+3V 3,5,9,10,11,12,13,14,16,19,20,21,22,23,24,25,26,27,28,33,35
+3VS5 11,12,13,14,29,35

REQUIRED STRAPS

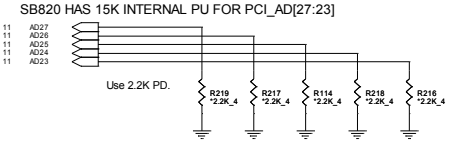


REQUIRED STRAPS

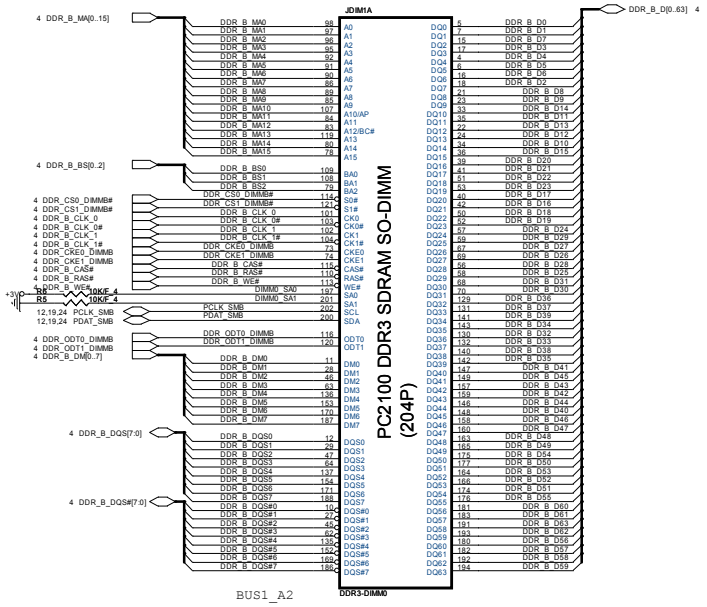
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM

DEBUG STRAPS

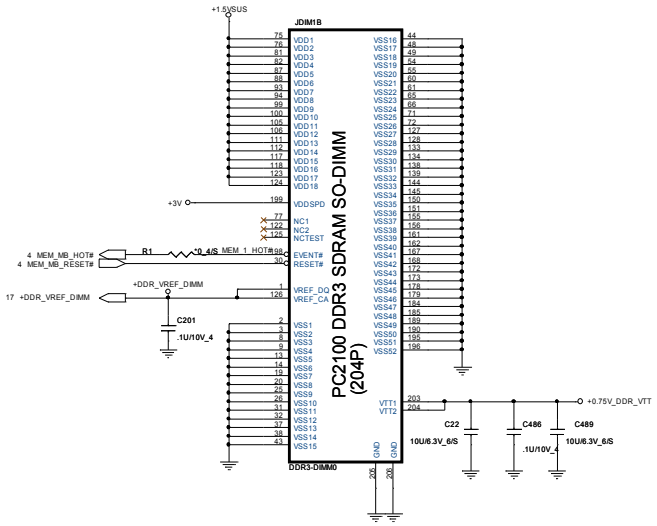
SB820 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

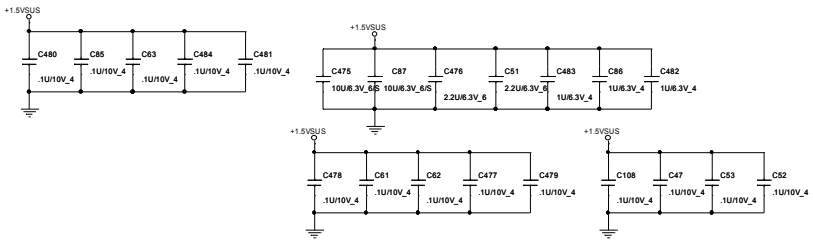


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

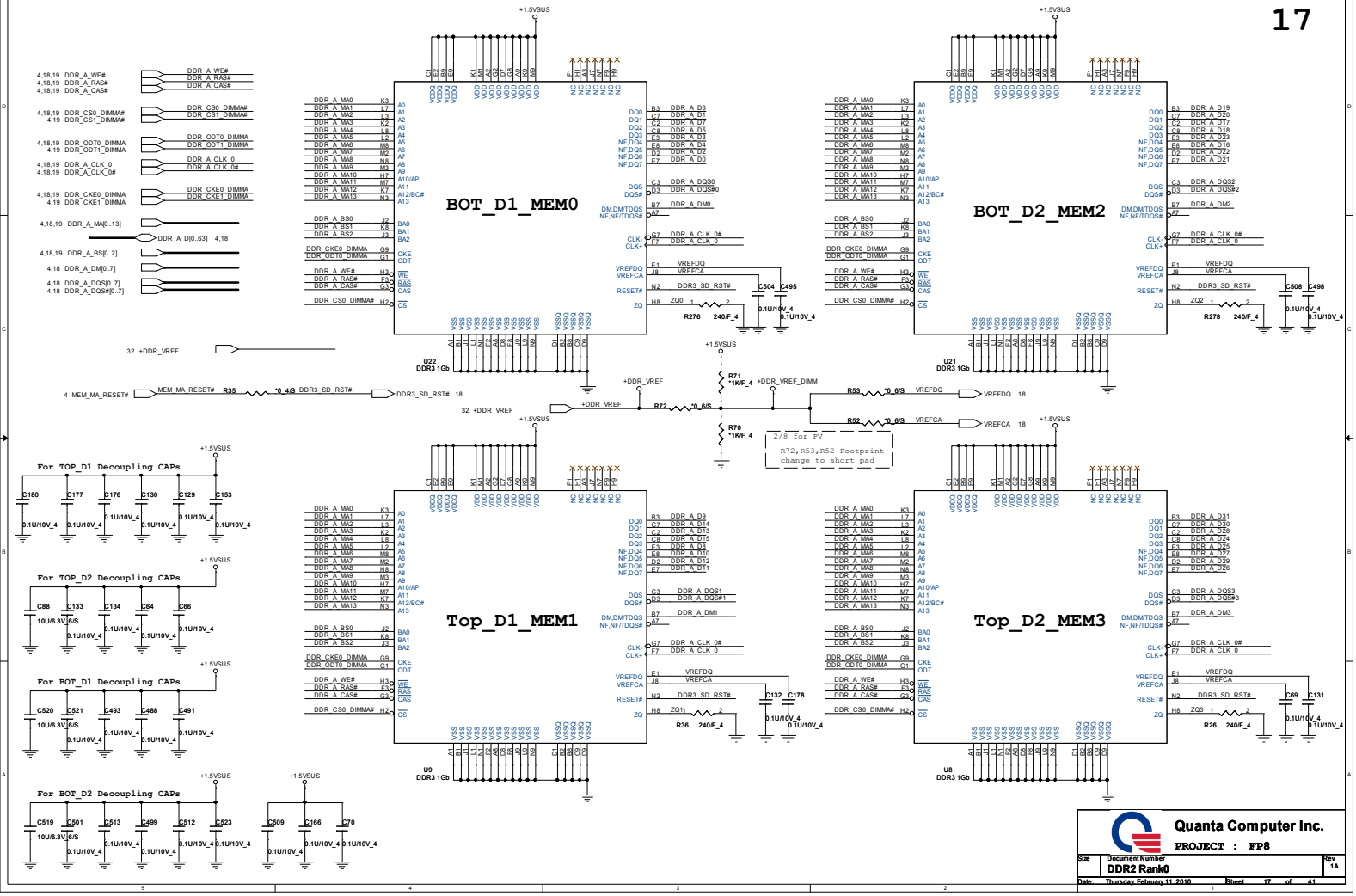


SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001





Quanta Computer Inc.		
PROJECT : FP8		
Size	Document Number: DDR2 SO-DIMM(200P)	Rev: 1A
Date: Thursday, February 11, 2010	Sheet 16 of 41	

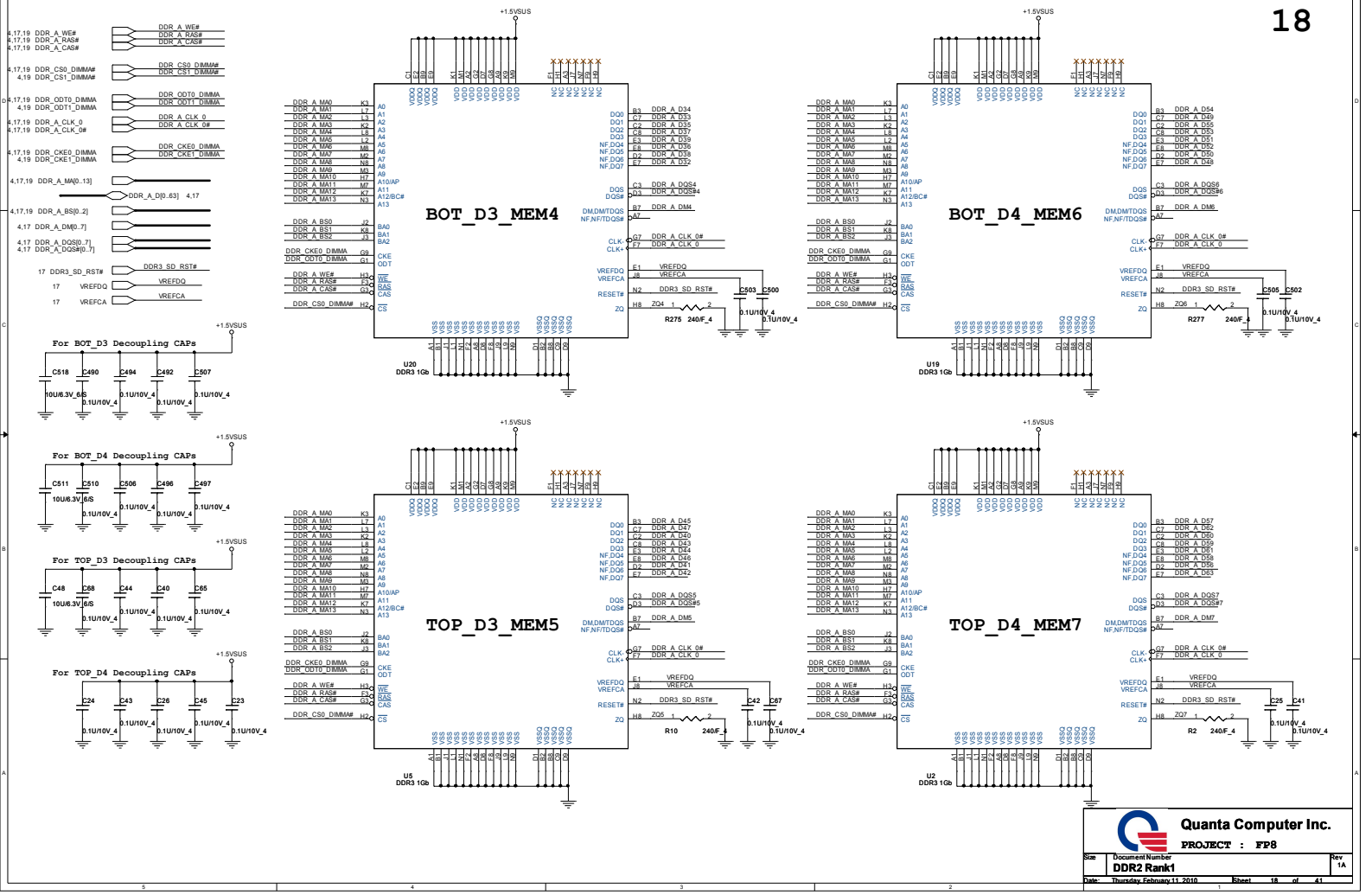


Quanta Computer Inc.

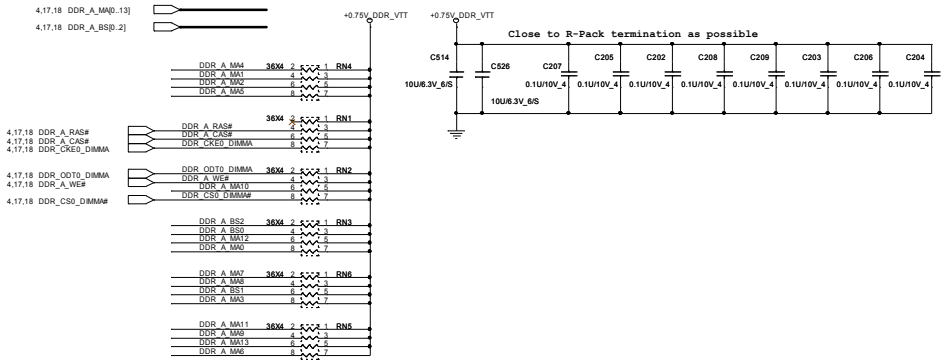
PROJECT : FP8

Size	Document Number	Rev
	DDR2 Rank0	1A

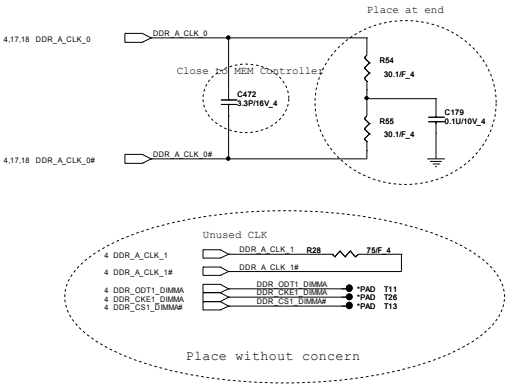
Date: Thursday, February 11, 2010 Sheet 17 of 41



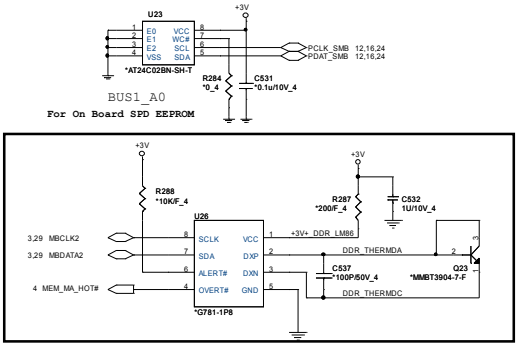
Quanta Computer Inc.			
PROJECT : FP8			
Size	Document Number		Rev
	DDR2 Rank1		1A
Date: Thursday, February 11, 2010		Sheet 18 of 41	



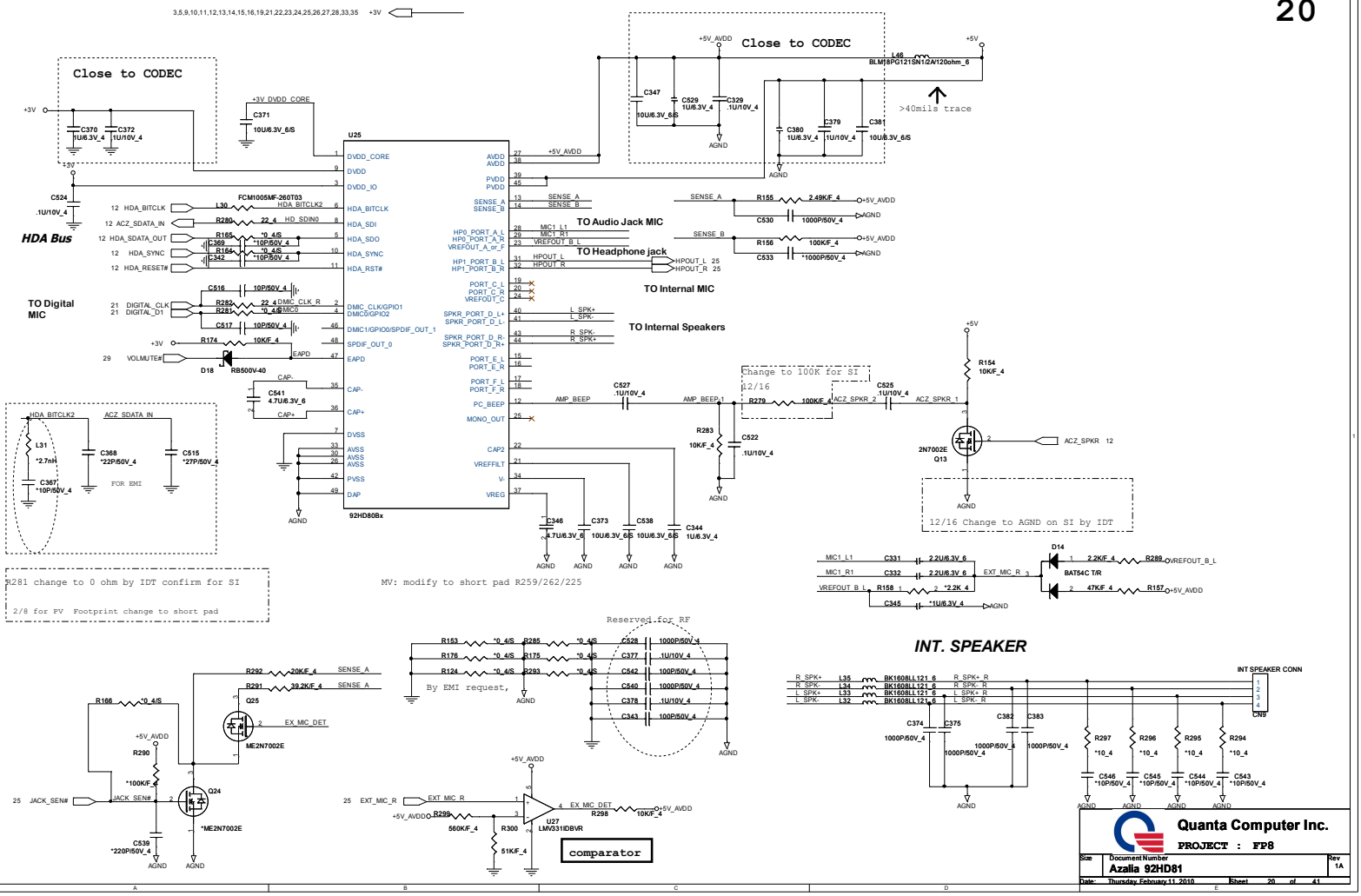
change RN1~RN6 footprint from 8p4r-0402 to 8p4r-0402-smt for pv



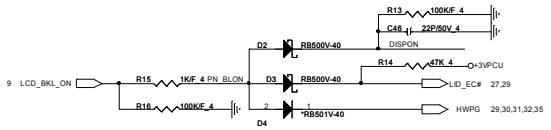
Solder Down SPD ROM



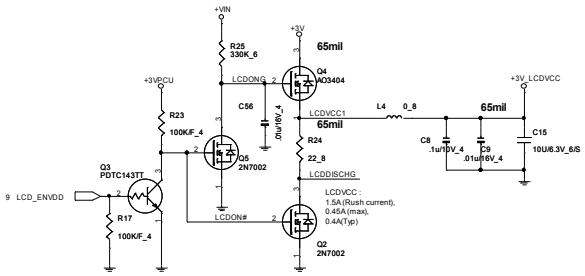
Quanta Computer Inc.		
PROJECT : FP8		
Size	Document Number: DDR2 Ter RES	Rev: 1A
Date: Thursday, February 11, 2010	Sheet 19 of 41	

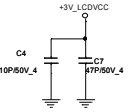

Close to CODEC
Close to CODEC
HDA Bus
TO Digital MIC
TO Audio Jack MIC
TO Headphone jack
TO Internal MIC
TO Internal Speakers
92HD80Bx
U25
Change to 100K for SI 12/16
12/16 Change to AGND on SI by IDT
R281 change to 0 ohm by IDT confirm for SI
2/8 for PV Footprint change to short pad
MV: modify to short pad R259/262/225
Reserved for RF
By EMI request,
INT. SPEAKER
INT SPEAKER CONN
comparator

Backlight Control(LDS)

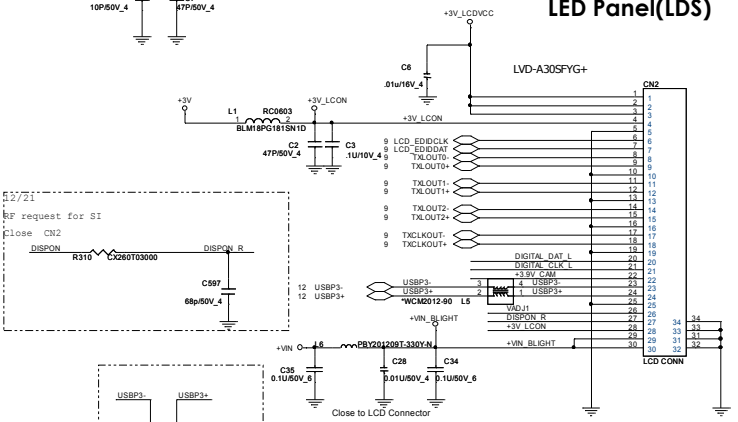


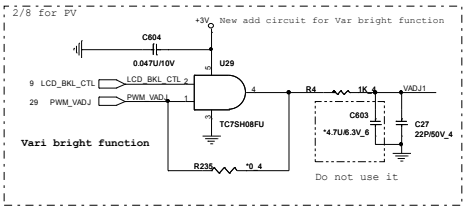
LCD POWER SWITCH



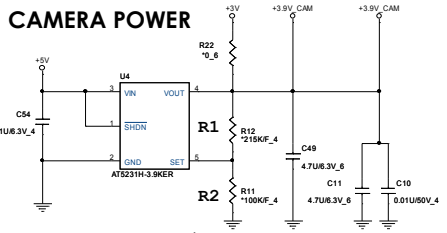


LED Panel(LDS)





CAMERA POWER



Quanta Computer Inc.		
PROJECT : FP8		
Size	Document Number: LED PANEL/CCD MODULE	Rev: 1A
Date: Friday, February 12, 2010	Sheet 21 of 41	

EMI Request

Stitchinf CAPs calose to CN8 for +5VPCU and GND Plane

by EMI request

+3V C210 1U/10V_4
+3VPCU C155 .1U/10V_4
+3VPCU C5 .1U/10V_4
+3VPCU C237 .1U/10V_4
+3VLANVCC C567 .1U/10V_4

+VIN C14 .1U/25V_4
+VIN C36 .1U/25V_4
+VA_AC C402 .1U/25V_4
+VA_AC C1 .1U/25V_4
+5V C330 .1U/10V_4
+5VPCU C571 .1U/10V_4
+5VPCU C573 .1U/10V_4
+5VPCU C325 .1U/10V_4

+1.5VSUS PC203 1000P/25V_4
+1.0VCU PC202 1000P/25V_4
+1.0VCC PC201 1000P/25V_4
+3VPCU PC200 1000P/25V_4
+5VPCU C550 .1U/10V_4

12/17 EMI Request for SI

+1.5VSUS PC205 1000P/25V_4
12/17 EMI Request for SI

+0.75V_DDR_VTT PC204 1000P/25V_4
+1.1V PC199 1000P/25V_4
12/17 EMI Request for SI

+5VPCU C384 68p/50V_4
+5VPCU C376 68p/50V_4
2010/2/11 RF For PV

Close to PQ34 11/13 RF Request
+VIN C464 470P/50V_4

12/21 RF Request change to 1u
+1.5VSUS_1 C341 1U/10V_4
+0.9V C292 1U/10V_4
+VCORE C37 1U/10V_4
+1.5VSUS_1 C596 1U/10V_4
+1.8V_L C397 1U/10V_4
close PR142

+1.5V PC193 1U/10V_4
+1.5VSUS PC194 1U/10V_4
+1.5VSUS PC206 1U/10V_4
+1.8V C136 1U/10V_4
+1.8V C246 1U/10V_4
+VIN PC207 1U/35V_6
PC206 close PC100
+3V PC128 1U/10V_4
12/21 RF Request change to 1u
+3V C598 *.1U/10V_4

PCB Screws

H1 *O-FP8-3
H2 MBIM3001
H3 *H-C275D90
H4 *H-C315D90
H5 *O-FP8-1
H6 *H-TC275BC220D181
H7 *O-FP8-2
H8 MBIM3001
H9 MBIM3001
H10 *H-C315D90
H11 *H-C394D275
H12 *H-C315D90
H13 *H-TC275BC220D181
H14 *H-TC275BC220D181
H15 *H-C394D275
H16 *H-C197D90
H17 MBFP8001
H18 *H-C79D79N
H19 *H-C79D79N
H20 *H-C394D110
H21 *H-C79D79N
H22 *H-C315D110
H23 *O-FP8-4
H24 *spad-re124x78np
H25 *spad-re124x78np

FAN Hole
CPU BRAKET

Close to PQ26 11/13 RF Request
+VIN C387 470P/50V_4
C388 33P/50V_4
PC115 0.1U/25V_4

Close to PQ23 11/13 RF Request
+VIN C390 470P/50V_4
C389 33P/50V_4
PC119 0.1U/25V_4

Close to PQ43 11/13 RF Request
+VIN C392 470P/50V_4
C393 33P/50V_4
PC125 0.1U/25V_4

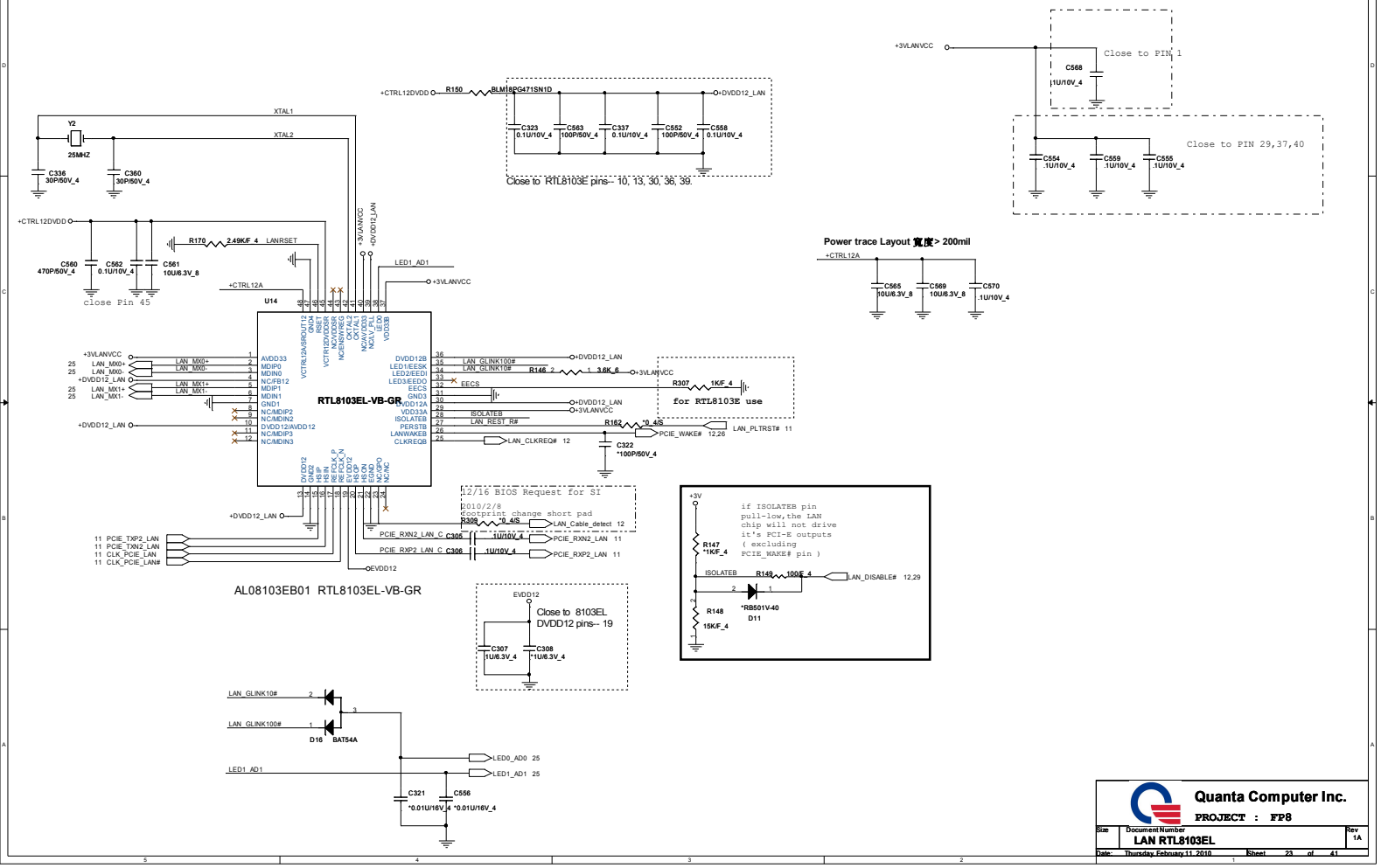
Close to PQ61 11/13 RF Request
+VIN C328 470P/50V_4
C411 33P/50V_4
PC79 0.1U/25V_4

Close to PQ49 11/13 RF Request
+VIN C453 470P/50V_4
C452 33P/50V_4
PC163 0.1U/25V_4

Close to PQ52 11/13 RF Request
+VIN C448 470P/50V_4
C449 33P/50V_4
PC162 0.1U/25V_4

Close to PQ41 11/13 RF Request
+VIN C19 470P/50V_4
C18 33P/50V_4
PC25 0.1U/25V_4

Quanta Computer Inc.
PROJECT : FP8
Size: Document Number: PCB SCREWs Rev: 1A
Date: Thursday, February 11, 2010 Sheet 22 of 41



Quanta Computer Inc.

PROJECT : FP8

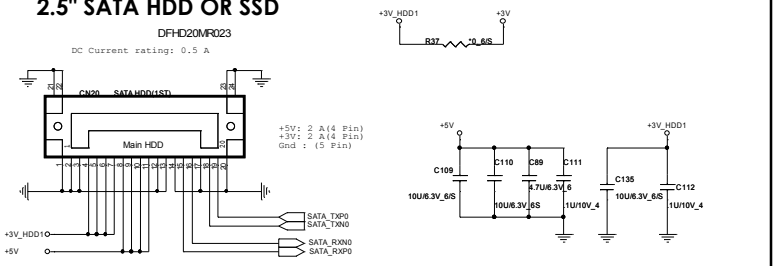
Size	Document Number	Rev
	LAN RTL8103EL	1A

Date: Thursday, February 11, 2010 Sheet 23 of 41

2.5" SATA HDD OR SSD

DFHD20MR023

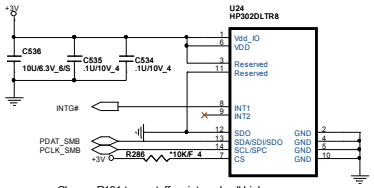
DC Current rating: 0.5 A



Accelerometer Sensor

1116 New add for HD protect

SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



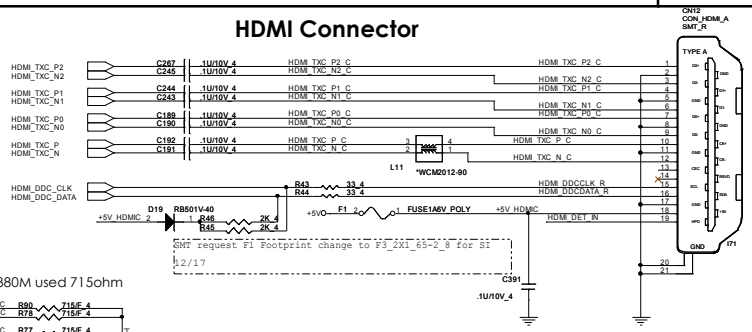
Change R181 to no stuff as internal pull high

Change footprint from sensor-3-8-14p to SENSOR-3-8-14P-smt for PV 2/8

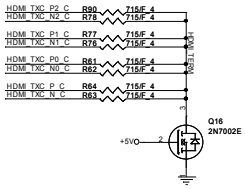
Pin 12: Low 38hex

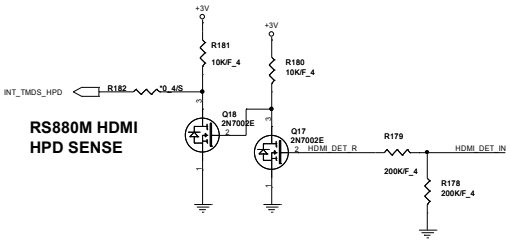
Pin 12: unconnected/floating 3Ahex

HDMI Connector



For RS880M used 715ohm





RS880M HDMI HPD SENSE

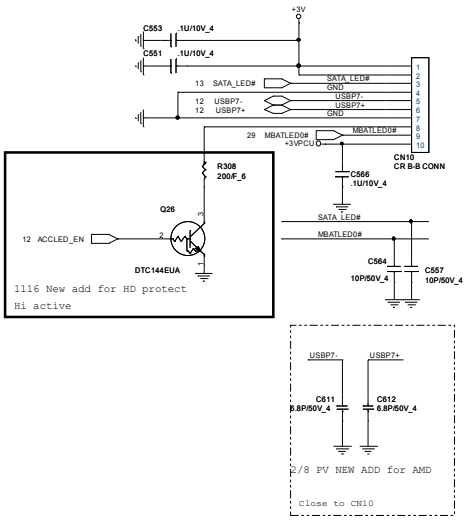
Quanta Computer Inc.

PROJECT : FP8

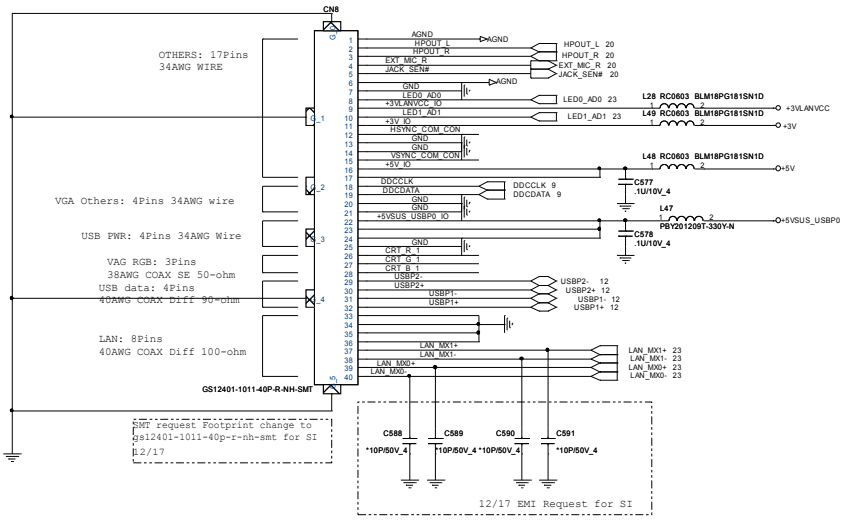
Size	Document Number	Rev
	HDD/HDMI	1A

Date: Thursday, February 11, 2010 Sheet 24 of 41

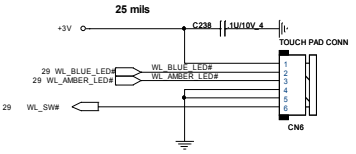
CardReader CONN.

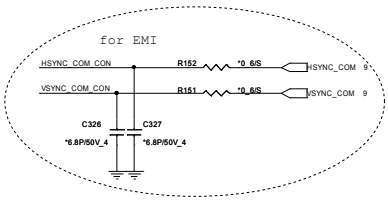


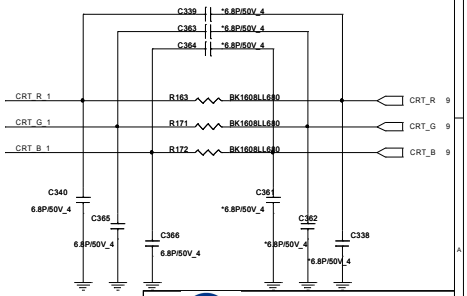
I/O Board CONN.



WL CTRL CONN.



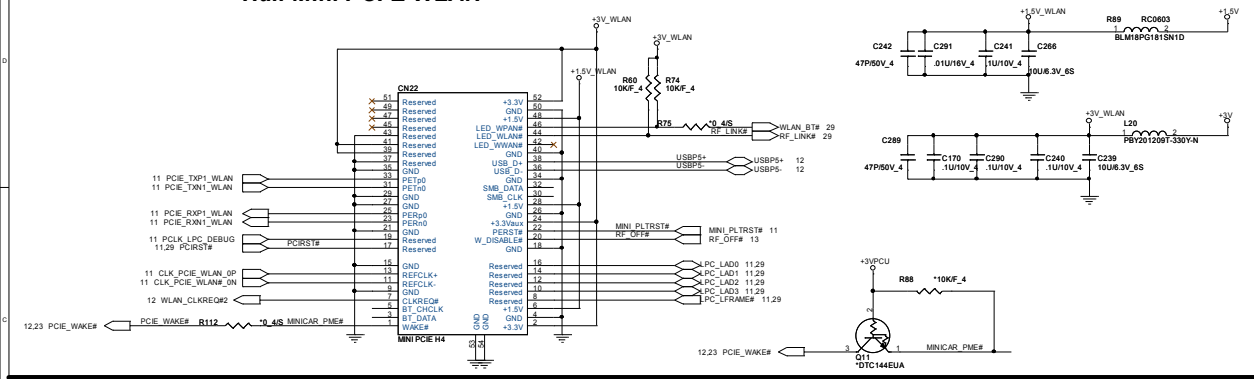




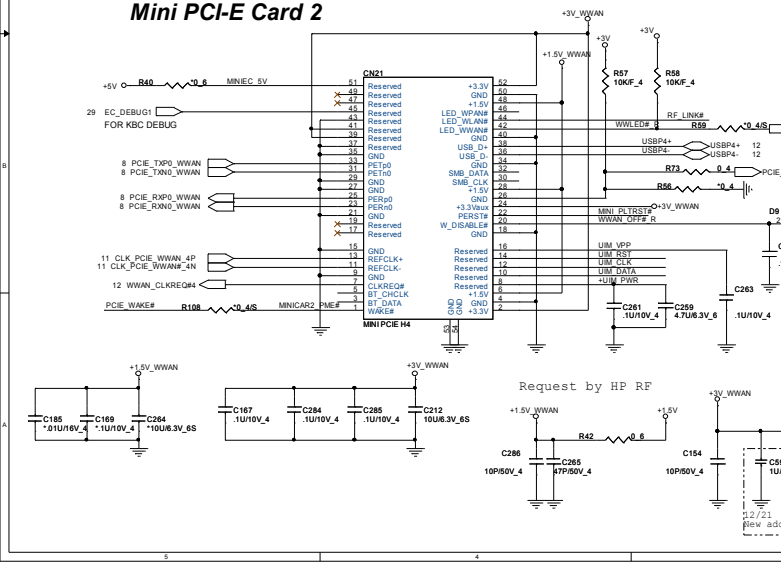
Quanta Computer Inc.
PROJECT : FP8
Size: Document Number: DB connectors
Rev: 1A
Date: Thursday, February 11, 2010
Sheet 25 of 41

Mini PCI-E Card 1
Half Mini PCI-E WLAN

The value of the capacitor is suggest by Siemens HQ expert.
For against 900Mhz RF interference. The value of capacitor is 27pF.
For against 1800Mhz RF interference. The value of capacitor is 10pF.
1nF/10nF value capacitor use for against ESD purpose.

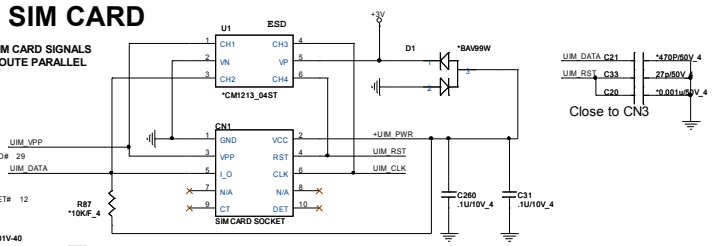


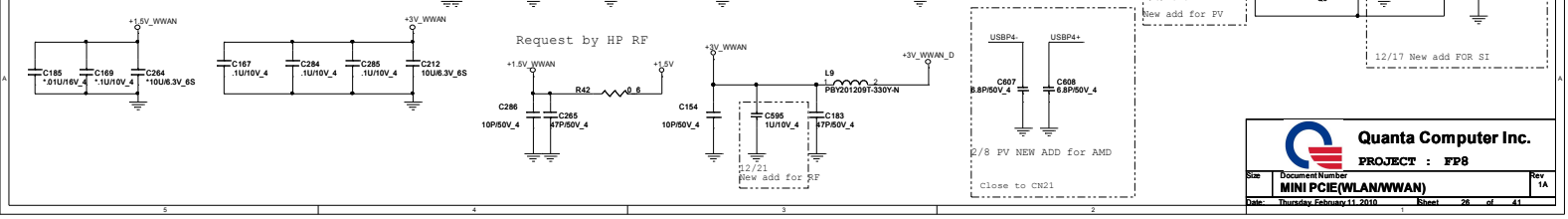
Full mini PCIE for WWAN
Mini PCI-E Card 2



SIM CARD

SIM CARD SIGNALS
ROUTE PARALLEL

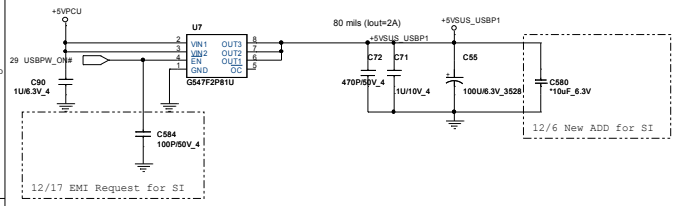


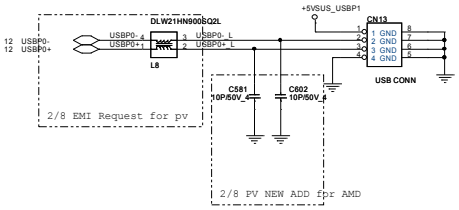


Quanta Computer Inc.
PROJECT : FP8

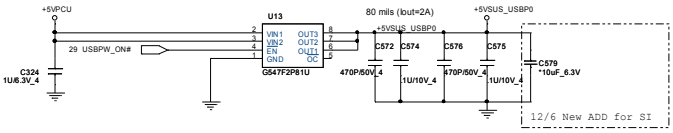
Size	Document Number	Rev
	MINI PCIE(WLAN/WWAN)	1A
Date: Thursday, February 11, 2010	Sheet 26 of 41	

1x Left side USB PORT

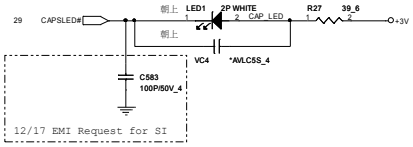




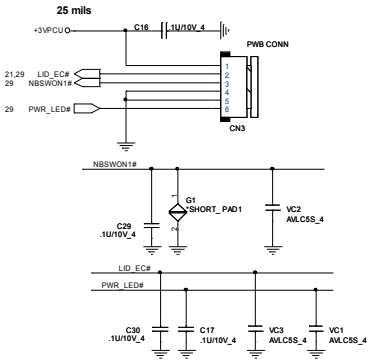
For Right 2xUSB Ports PWR



CAPS LEDs



PWR BT CONN.



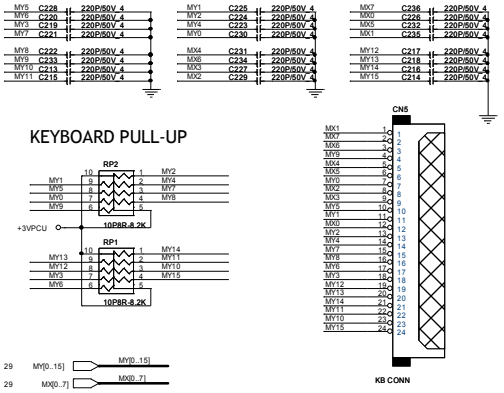
Quanta Computer Inc.

PROJECT : FP8

Size	Document Number	Rev
	USB Connectors/LED/PWR BT	1A

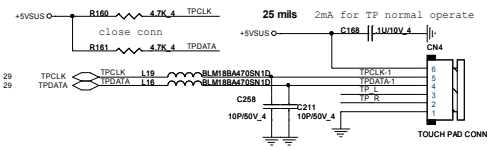
Date: Thursday, February 11, 2010 Sheet 27 of 41

Keyboard(KBC)

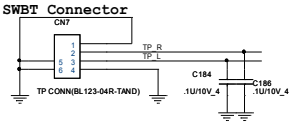


KEYBOARD PULL-UP

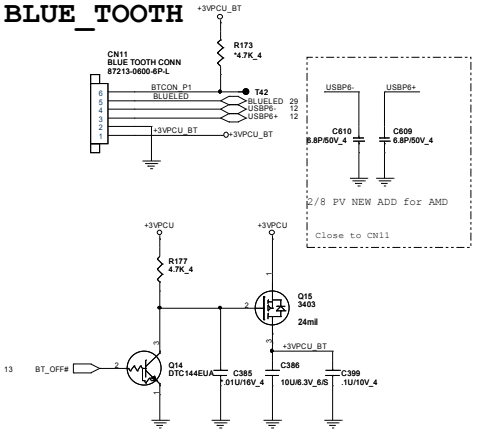
Touch Pad CONNECTOR(TBD)



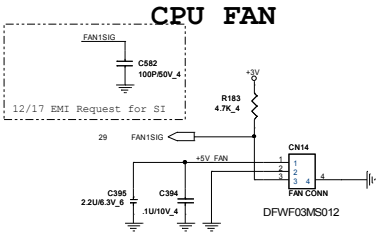
SWBT Connector

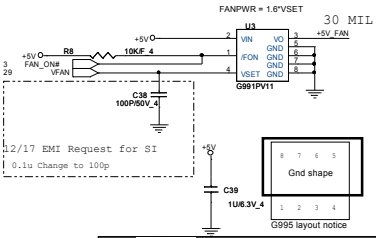


BLUE_TOOTH

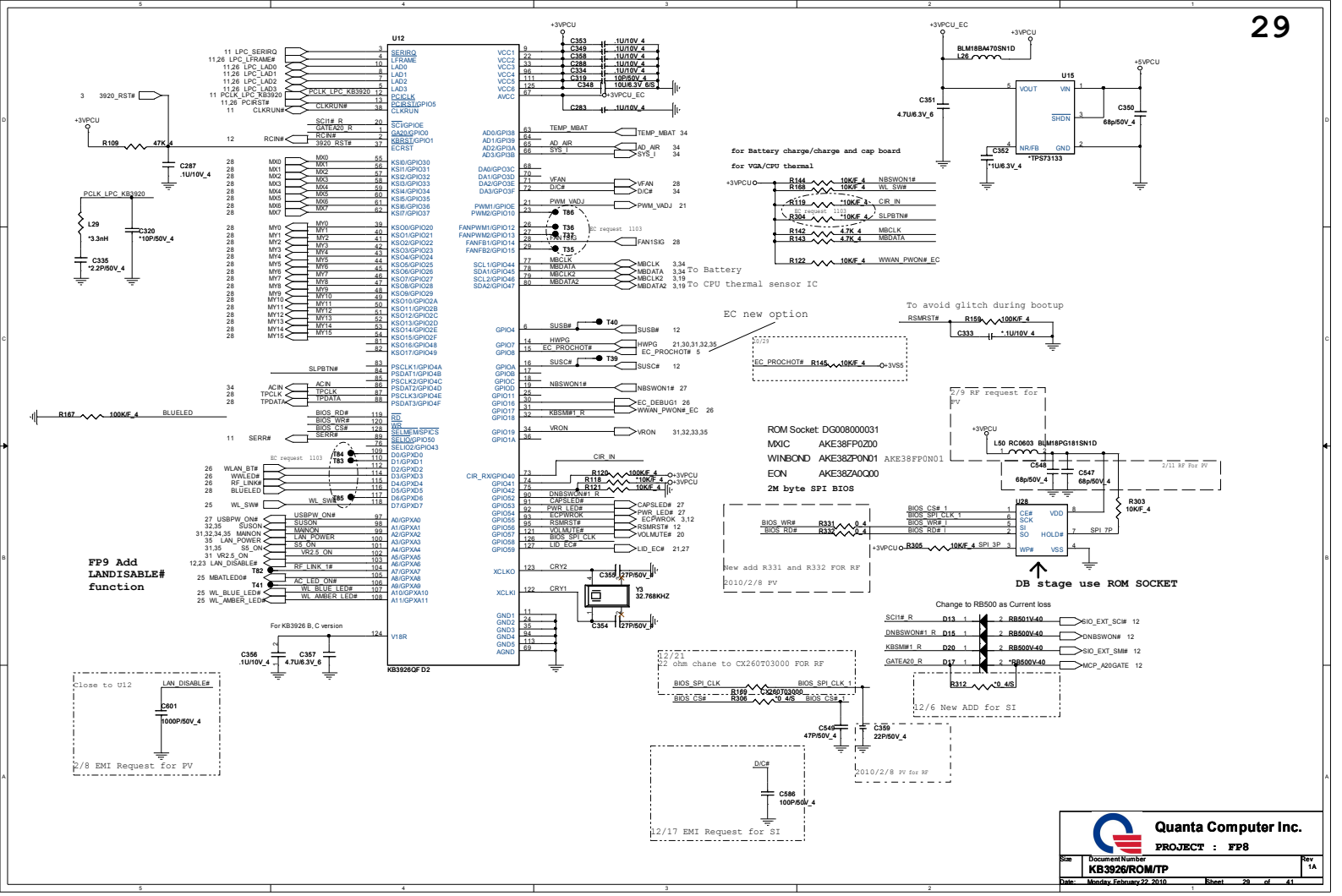


CPU FAN





Quanta Computer Inc.			
PROJECT : FP8			
Size	Document Number		Rev
	KB/BT/TP/CPU FAN		1A
Date: Thursday, February 11, 2010		Sheet 28 of 41	



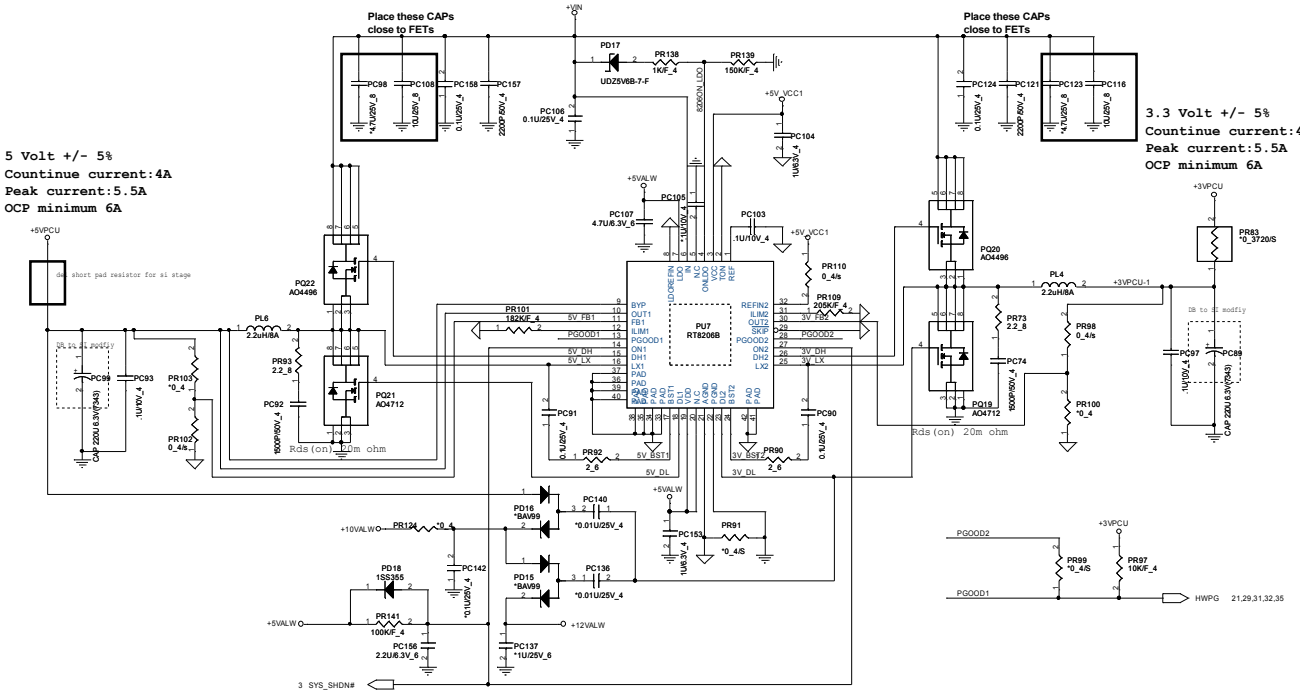
Quanta Computer Inc.

PROJECT : FP8

Size	Document Number	Rev
	KB3926/ROM/TP	1A

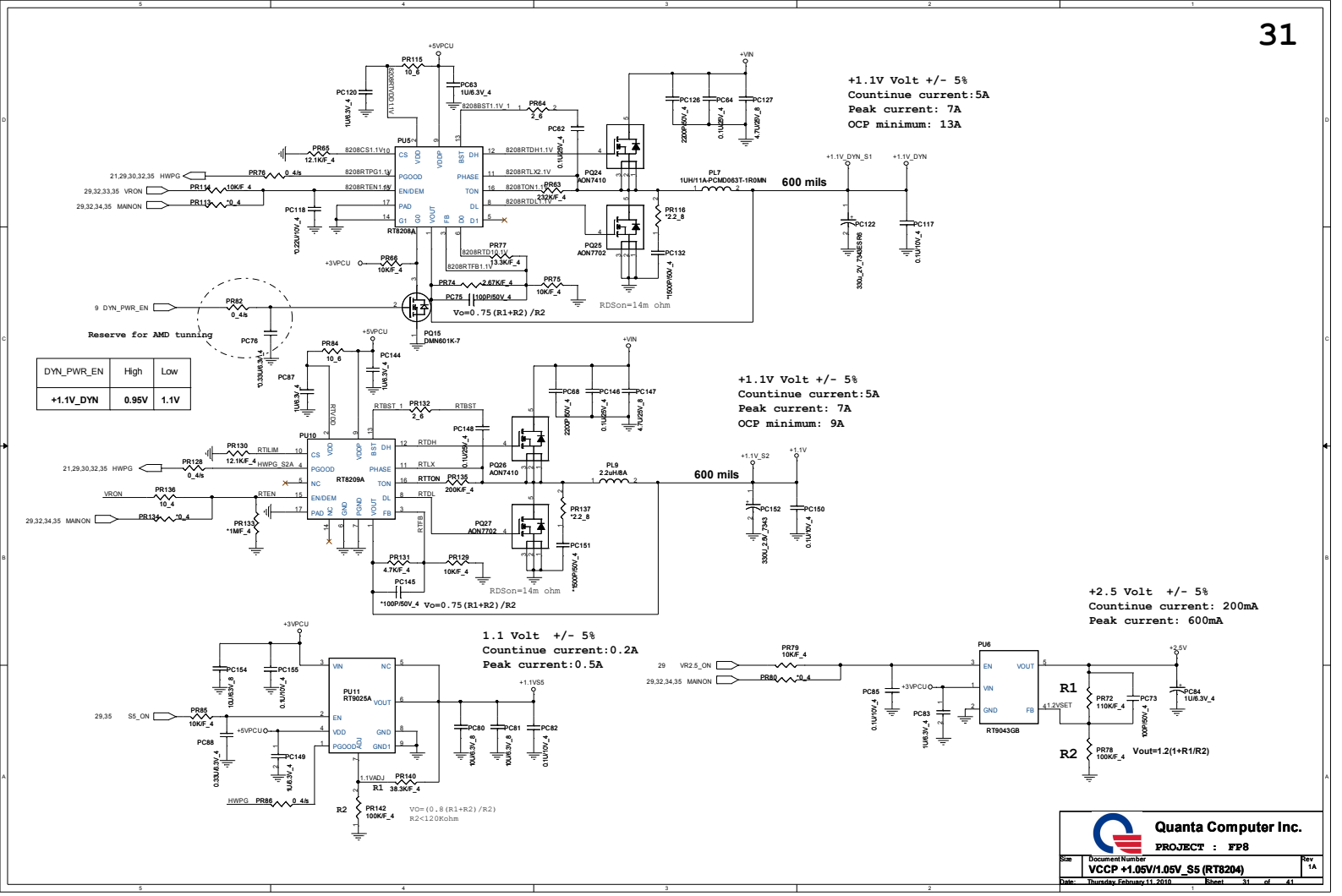
Date: Monday, February 22, 2010 Sheet 29 of 41

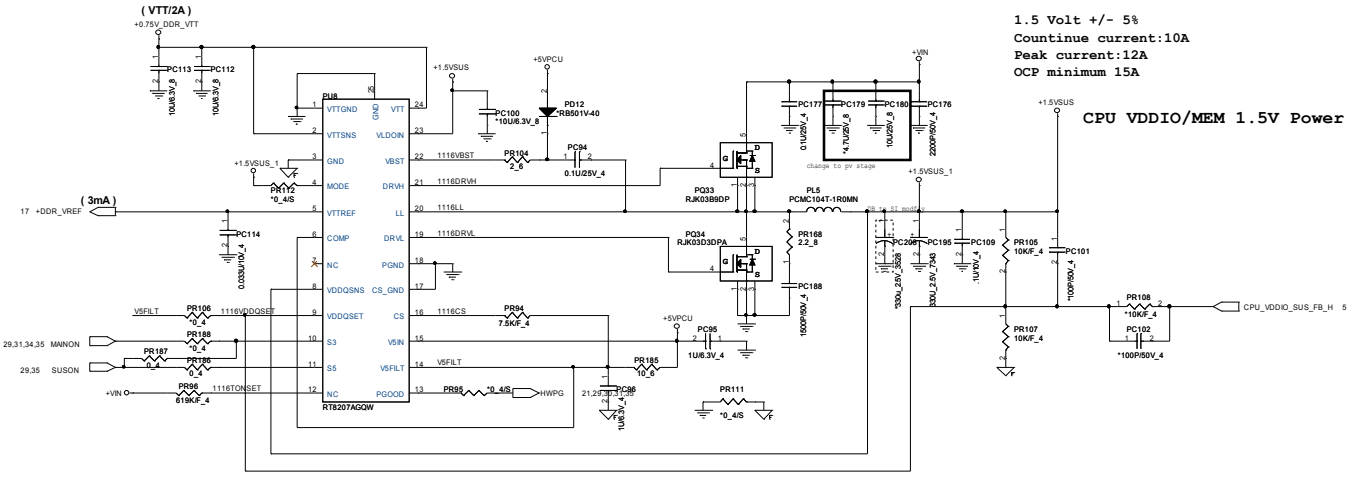
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

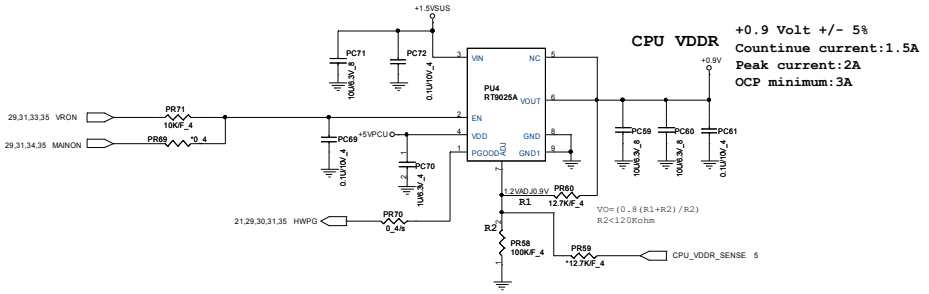


Quanta Computer Inc.		
PROJECT : FP8		
Size	Document Number: SYSTEM 5V/3V (RT8206B)	Rev 1A
Date: Thursday, February 11, 2010	Sheet 30 of 41	

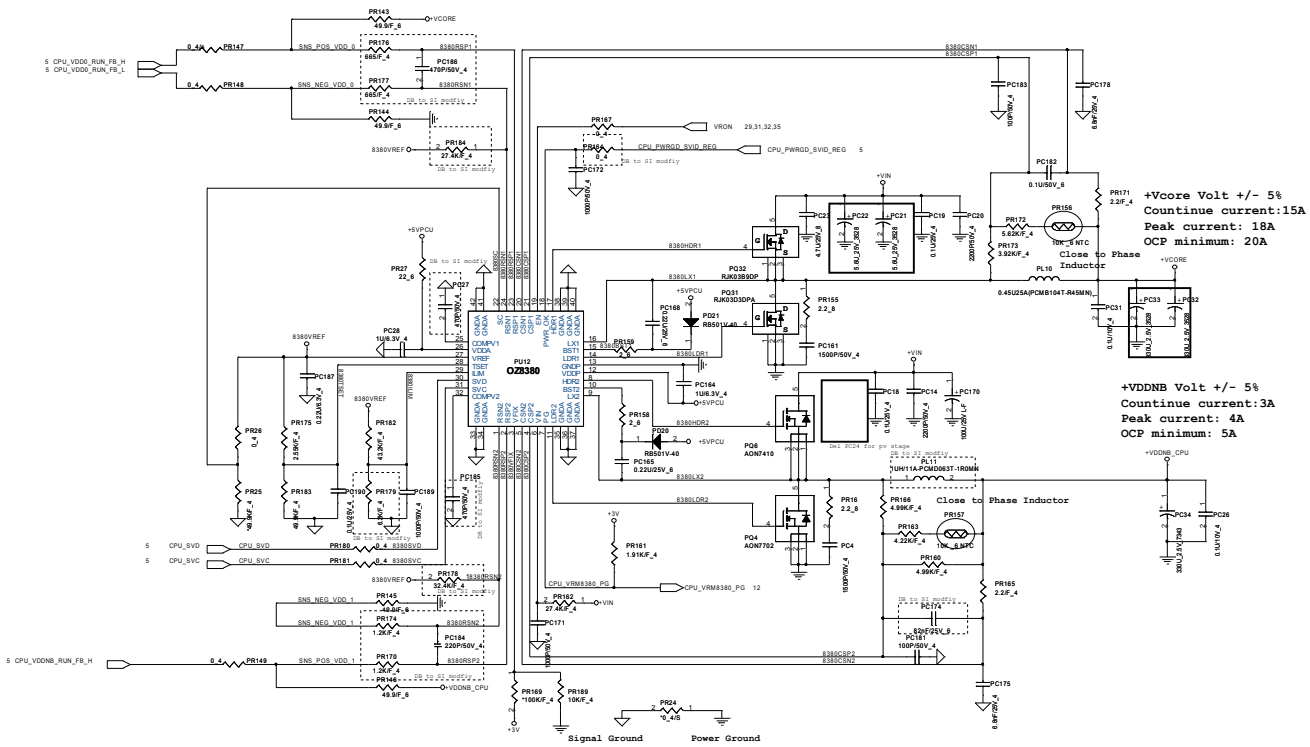
PROJECT : ZU1
Quanta Computer Inc.


+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 7A
OCP minimum: 13A
600 mils
Reserve for AMD tunning
DYN_PWR_EN | High | Low
+1.1V_DYN | 0.95V | 1.1V
+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 9A
OCP minimum: 9A
600 mils
1.1 Volt +/- 5%
Countinue current:0.2A
Peak current:0.5A
+2.5 Volt +/- 5%
Countinue current: 200mA
Peak current: 600mA
Vout=1.2(1+R1/R2)
Quanta Computer Inc.
PROJECT : FP8
VCCP +1.05V/1.05V_S5 (RT8204)
Thursday, February 11, 2010

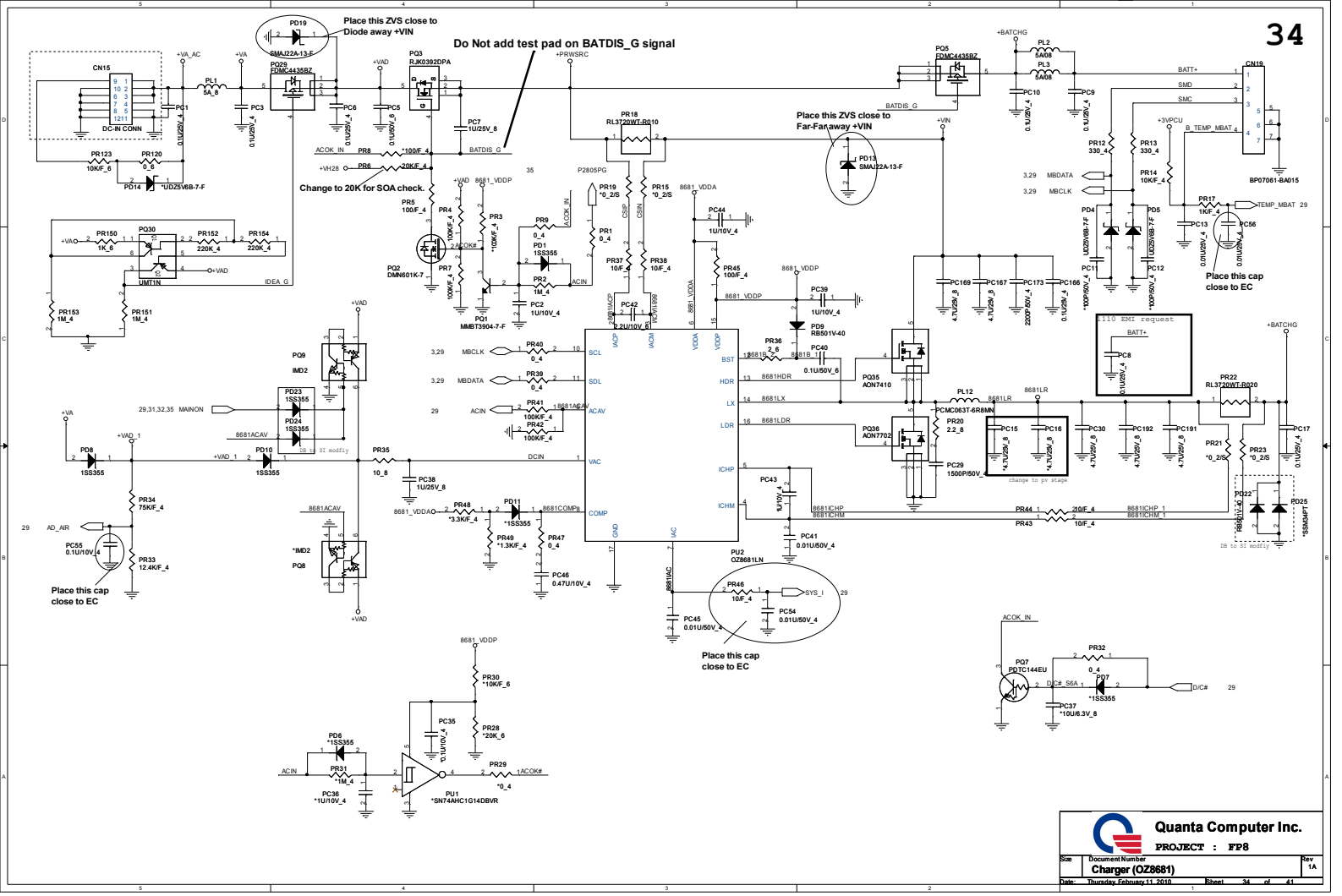


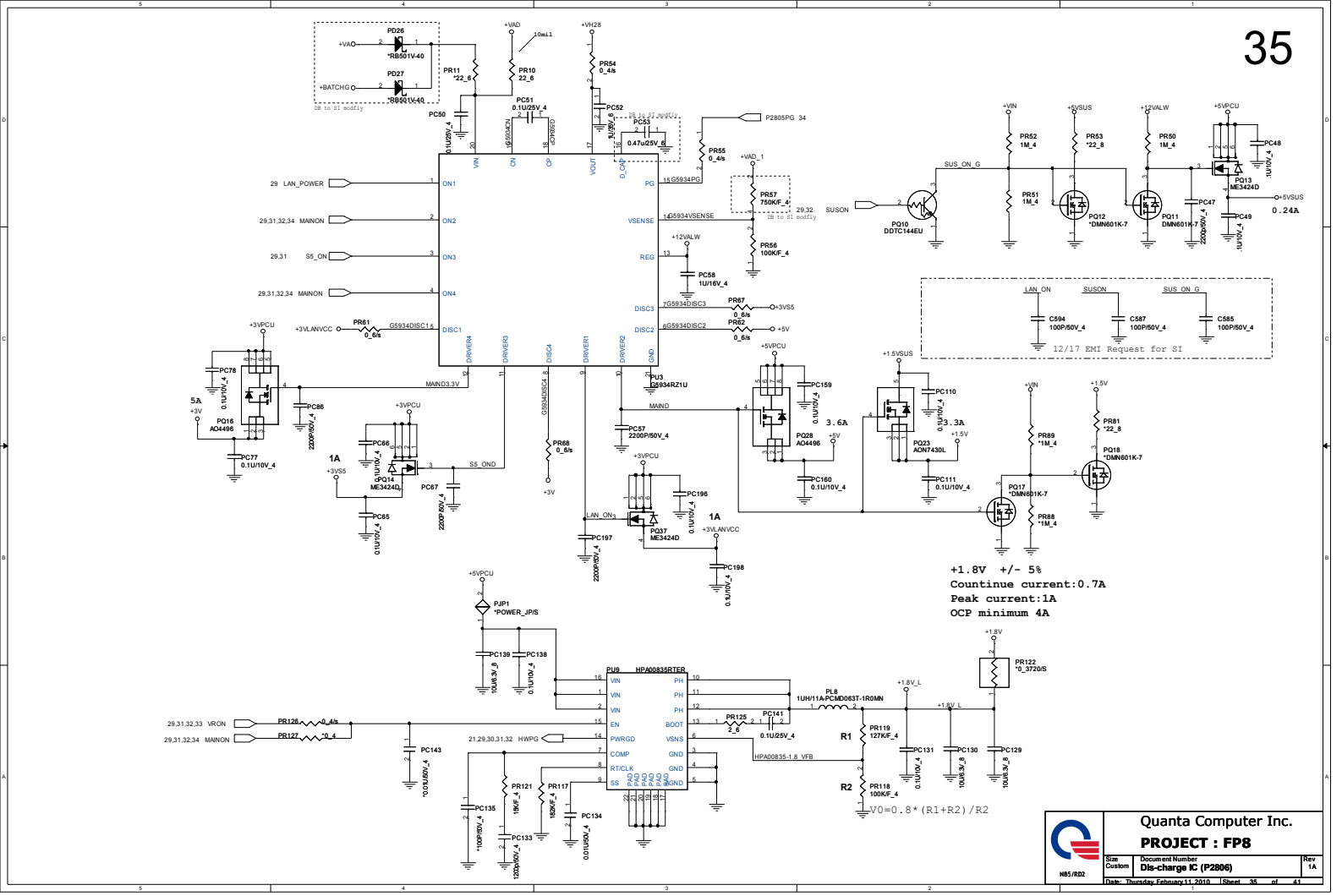


Quanta Computer Inc.		
PROJECT : FP8		
Size	Document Number: DDR3 +1.5VSUS (RT8207)	Rev: 1A
Date: Thursday, February 11, 2010	Sheet 32 of 41	



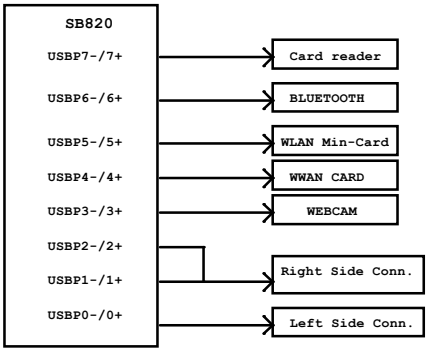
Quanta Computer Inc.	
PROJECT : FP8	
Size	Document Number: VCORE (OZ8380) — Rev: 1A
Date: Thursday, February 11, 2010	Sheet 33 of 41


Place this ZVS close to Diode away +VIN
Do Not add test pad on BATDIS_G signal
Place this ZVS close to Far-Faraway +VIN
Change to 20K for SOA check.
Place this cap close to EC
Place this cap close to EC
Place this cap close to EC
DC-IN CONN
SMAJ22A-13-F
FDMC4435BZ
RJK0392DPA
RL3720WT-R010
SMAJ22A-13-F
FDMC4435BZ
AON7410
PCMC063T-6R8MN
AON7702
OZ8681LN
PDTC144EU
UMT1N
DMN601K-7
MMBT3904-7-F
RB501V-40
1SS355
UDZ5V6B-7-F
SN74AHC1G14DBVR
BP07061-BA015
RL3720WT-R020
PCMC063T-6R8MN
Quanta Computer Inc.
PROJECT : FP8
Charger (OZ8681)
Thursday, February 11, 2010
Sheet 34 of 41



Quanta Computer Inc.			
PROJECT : FP8			
Size: Custom	Document Number: Dis-charge IC (P2806)		Rev: 1A
NB5/RD2	Date: Thursday, February 11, 2010	Sheet 35 of 41	

USB GUIDE

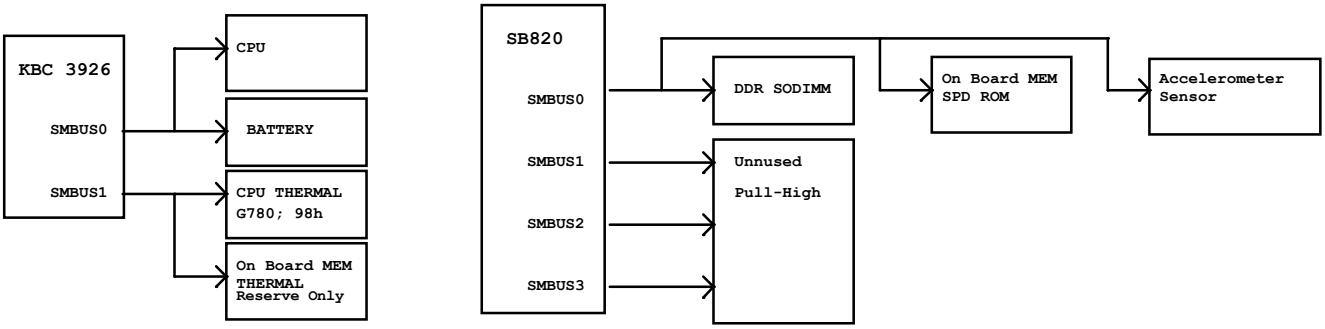


Quanta Computer Inc.
PROJECT : FP8

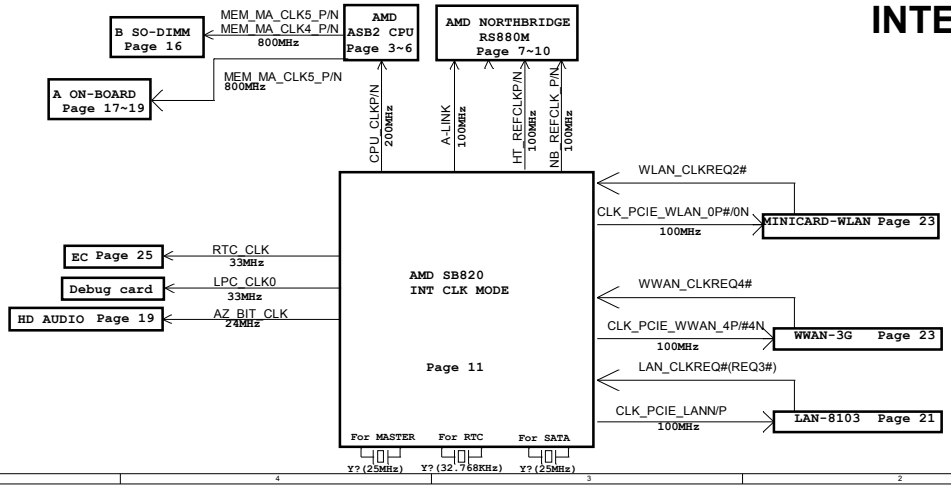
Size	Document Number	Rev
	SB CLKs Routing	1A

Date: Thursday, February 11, 2010 Sheet 36 of 41

SYSTEM SMBUS GUIDE



INTERNAL CLOCK MODE

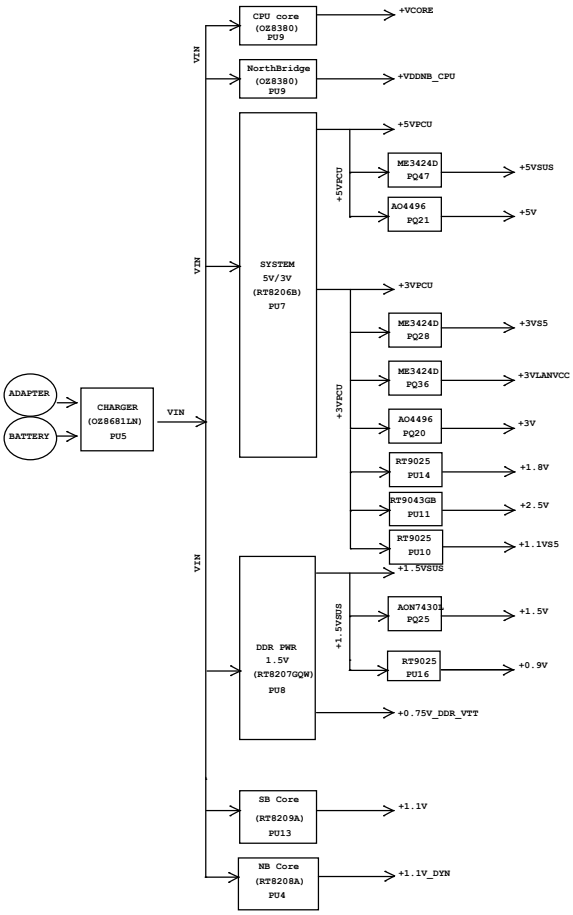


Quanta Computer Inc.

PROJECT : FP8

Size	Document Number	Rev
	Clock Distribution Diagram	1A

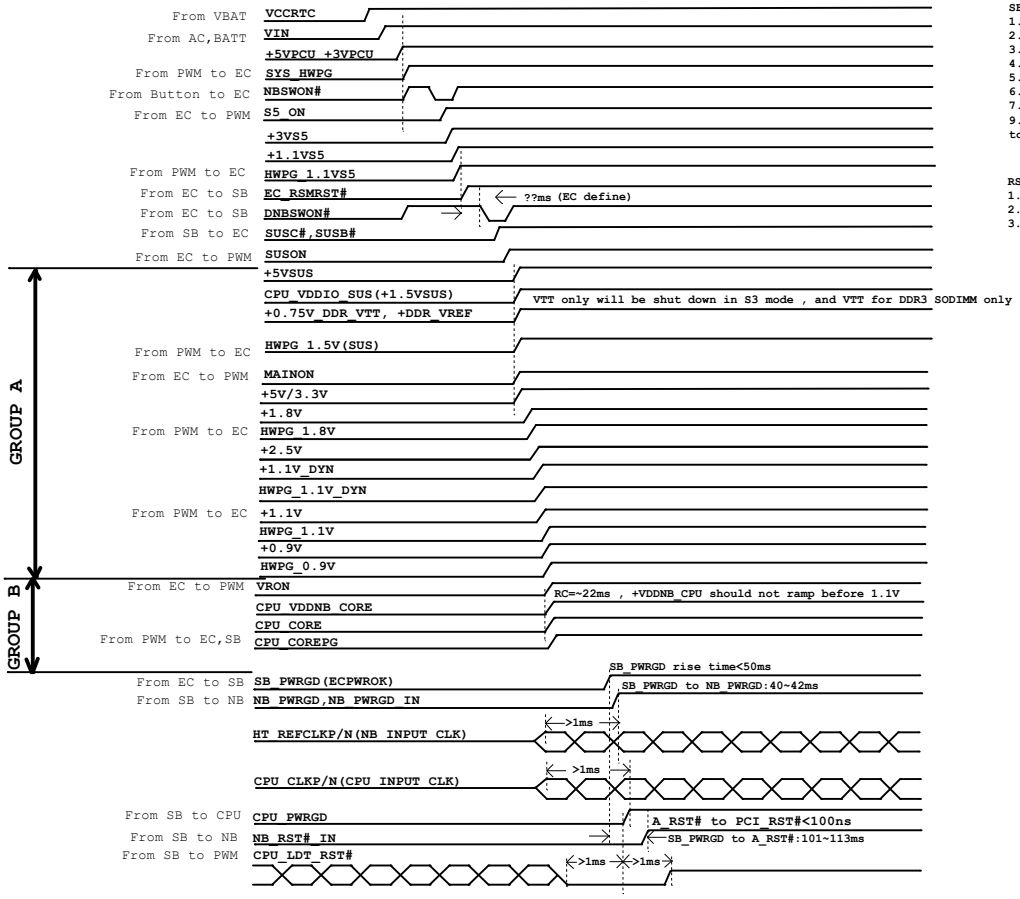
Date: Thursday, February 11, 2010 Sheet 37 of 41



POWER	Distribution
VIN	LCD Backlight, CPU_CORE,NB_CORE, +5VPCU, +3VPCU, +1.5VSUS, +1.1V, +1.1V_DYN
+VCORE	CPU
+VDDNB_CPU	power supply for on-die NorthBridge
+1.1V	NorthBridge power supply
+1.1_DYN	power supply for on-die NorthBridge
+5VPCU	USB Connecter
+5VSUS	Touch Pad
+5V	CRT, Audio codec, SATA
+3VPCU	KeyBoard, EC, BIOS
+3VS5	SouthBridge
+3VLANVCC	LAN
+3V	thermal Sensor, NB, SB, EEPROM, Audio codec, Card Reader, WLAN, WWAN, FAN, LED, BT
+1.8V	NB, SB
+1.5VSUS	CPU, DDR3
+1.5V	WLAN
+0.9V	CPU
+0.75V_DDR_VTT	DDR3
+2.5V	CPU
+1.1VS5	SB

Quanta Computer Inc.
PROJECT : F9S
Power Tree

Nile Power On Sequence



Power on sequence required:

SB800:
1.+3VS5 ramp before +1.1S5
2.+3V ramp before +1.8V
3.+1.8V ramp before +1.1V
4.+3.3V ramp before +1.1V
5.+3VS5 ramping down time>300us
6.50us<=all power rails rise time except +3VS5<=40ms
7.100us<=+3VS5 rise time<=40ms
9.VBAT (VCCRTC) must ramp at least 5 seconds before the S5 rails to allow start time for the internal RTC

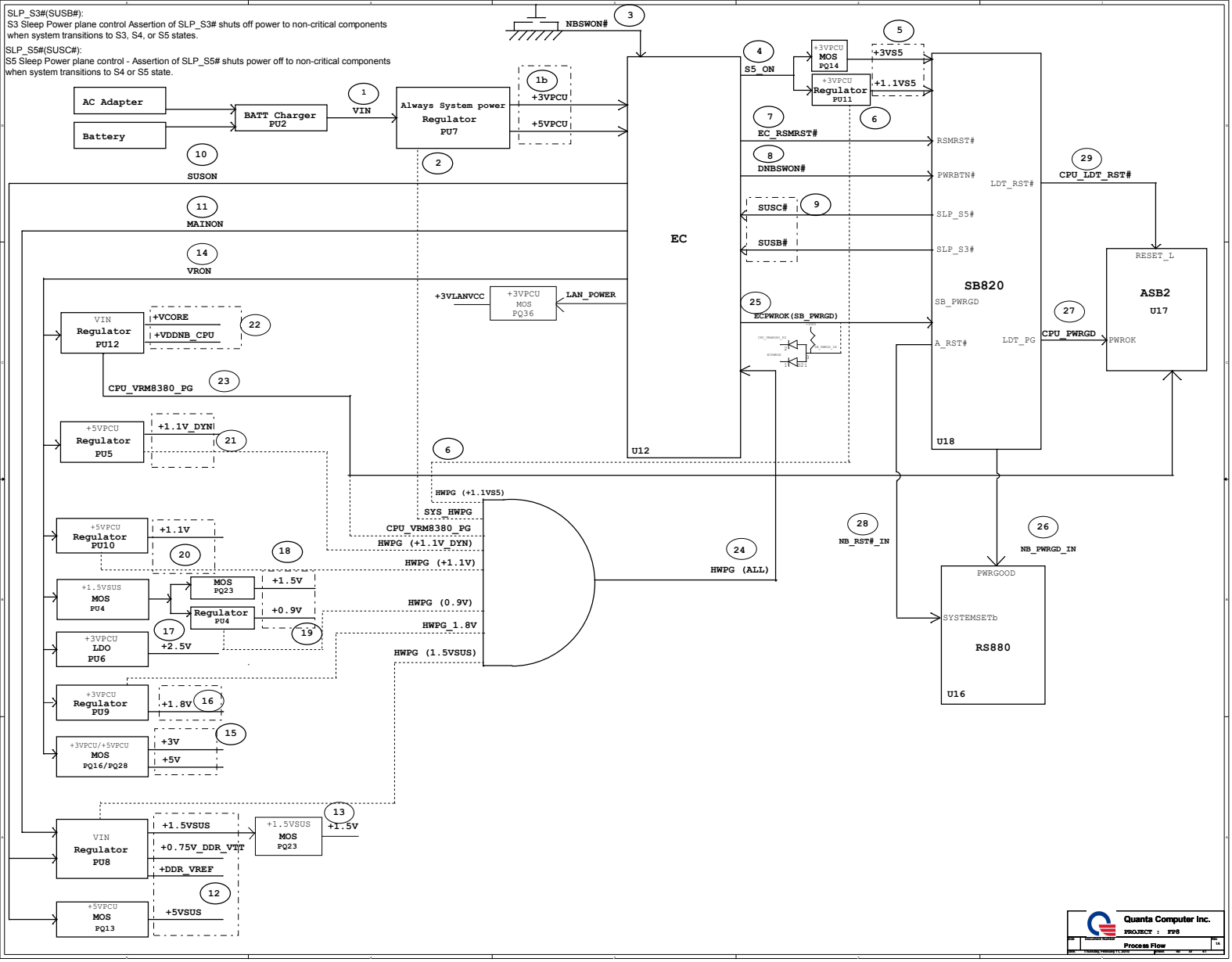
RS880:
1.0<(+3.3V)-(+1.8V)<2.1
2.+1.8V ramp before +1.1V
3.+1.1V ramp before +VDDNB_CPU

Notice:
1.CPU_LDT_RST# msut be asserted a minimum of 1ms prior to the assertion of CPU_PWRGD
2.CPU_CLKP/N must be within specification a minimum of 1ms prior to the assertion of CPU_PWRGD
3.CPU_PWRGD remains deasserted at least 1ms after both CPU_CLKP/N and all voltages to the processor are within specification for operation
4.all NB power rails(1.8V/1.2V/1.1V) valid before NB_PWRGD at least 1ms
5.stable input clocks from CLKGEN(HT_REFCLKP/N) to NB before NB_PWRGD at least 1ms

Quanta Computer Inc.
PROJECT : FP8
Size | Document Number | Rev 1A
Power Sequence
Date: Thursday, February 11, 2010 | Sheet 39 of 41

SLP_S3#(SUSB#):
S3 Sleep Power plane control Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states.

SLP_S5#(SUSC#):
S5 Sleep Power plane control - Assertion of SLP_S5# shuts power off to non-critical components when system transitions to S4 or S5 state.



Quanta Computer Inc.
PROJECT : FP8
Process Flow