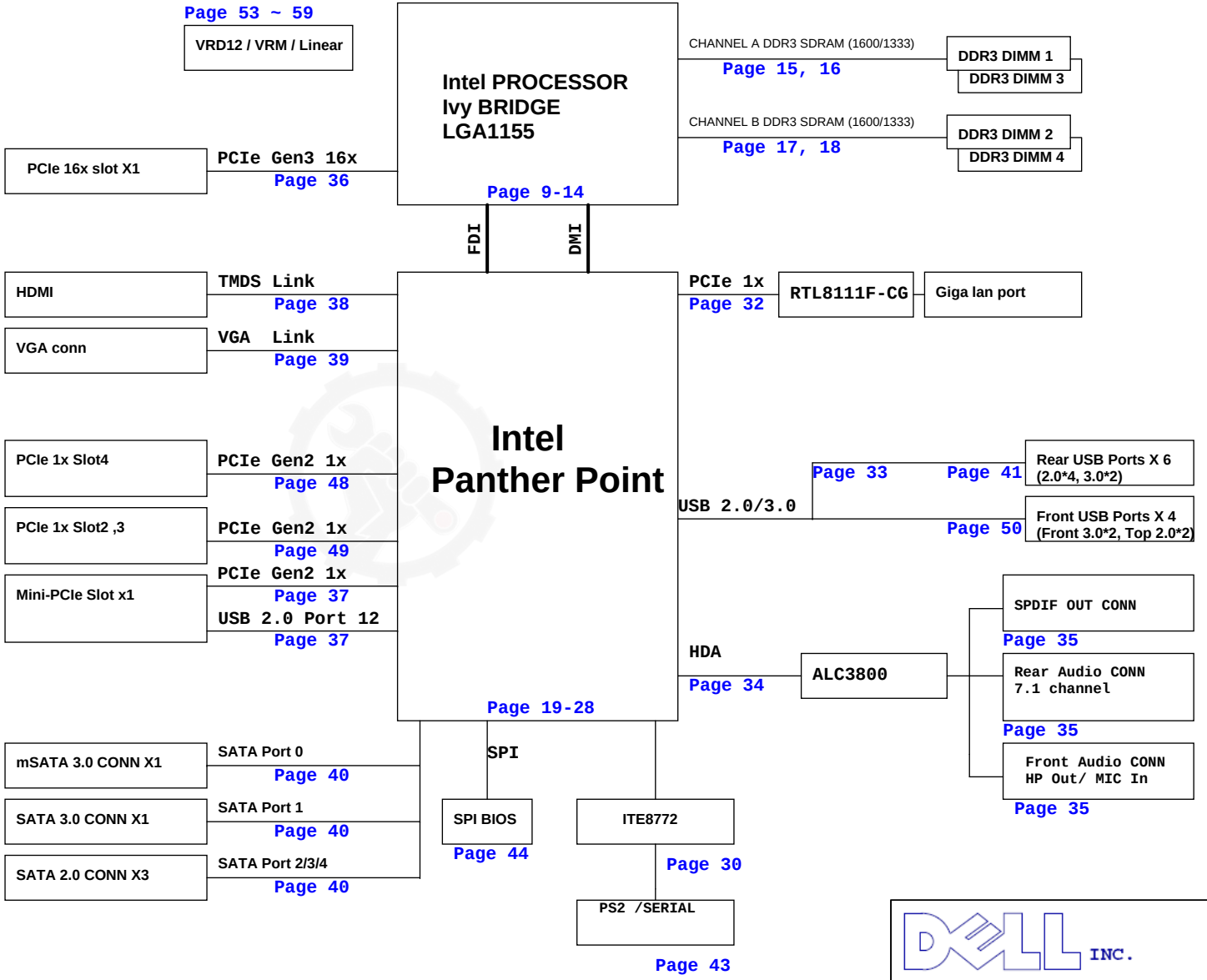
Cyperss point Diagram



DELL INC.

Title: BLOCK DIAGRAM

DWG NO: Cyperss point

Rev: A00

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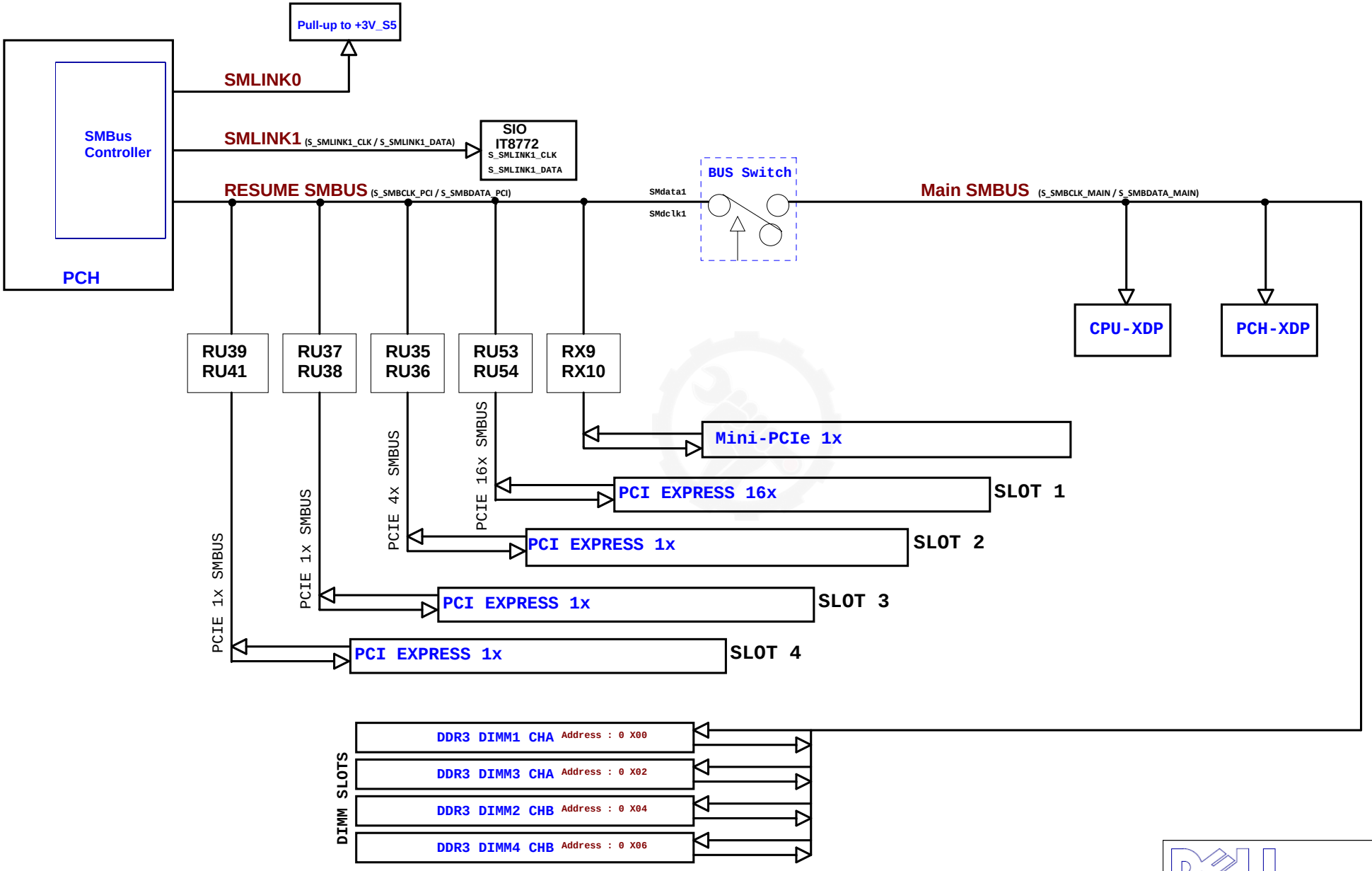
SMBUS DIAGRAM



DELL INC.

Title: SMBus MAP

DWG NO: Cyperss point

Rev: A00

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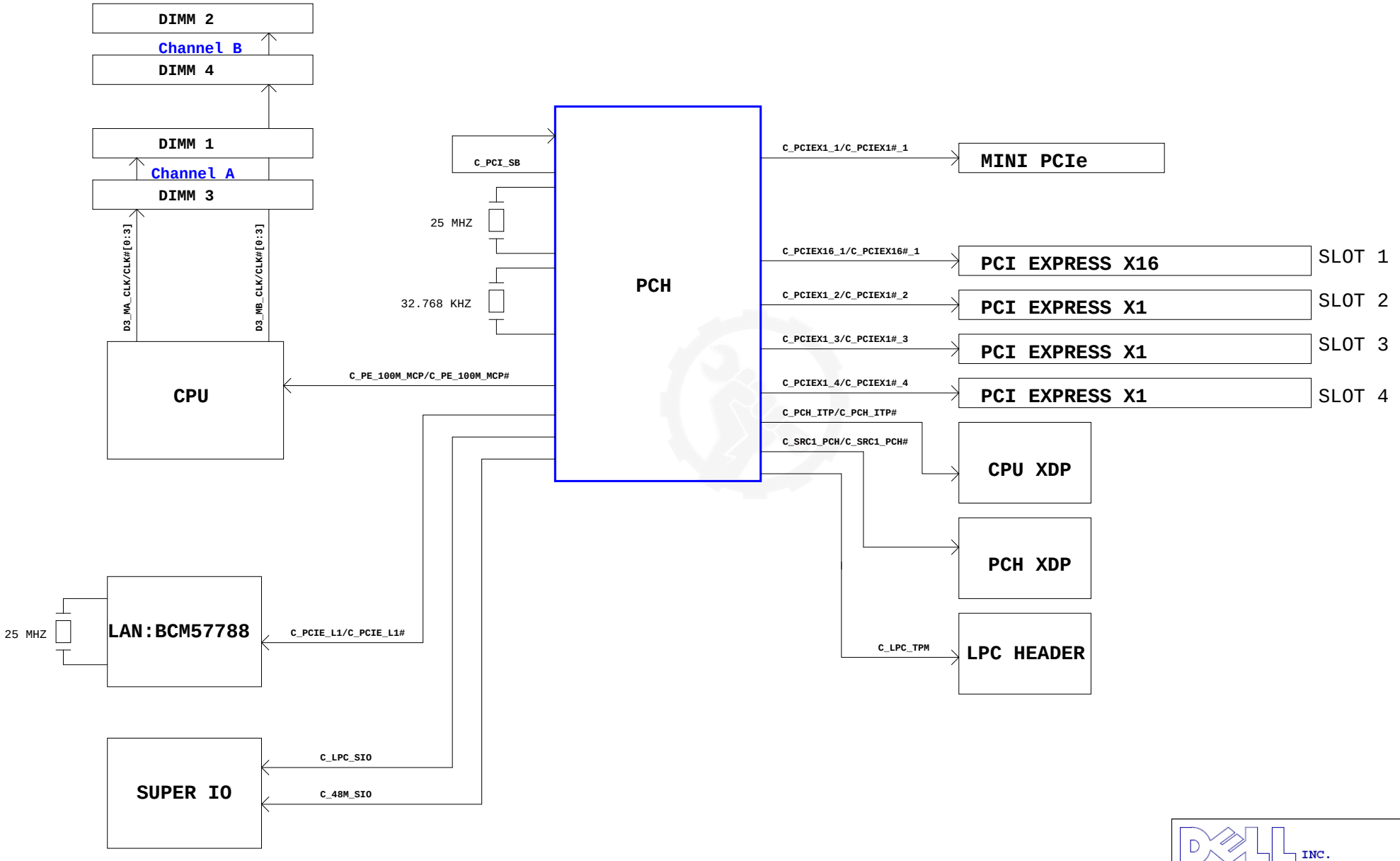

DELL INC.

Title: Clock Distribution

DWG NO: Cyperss point

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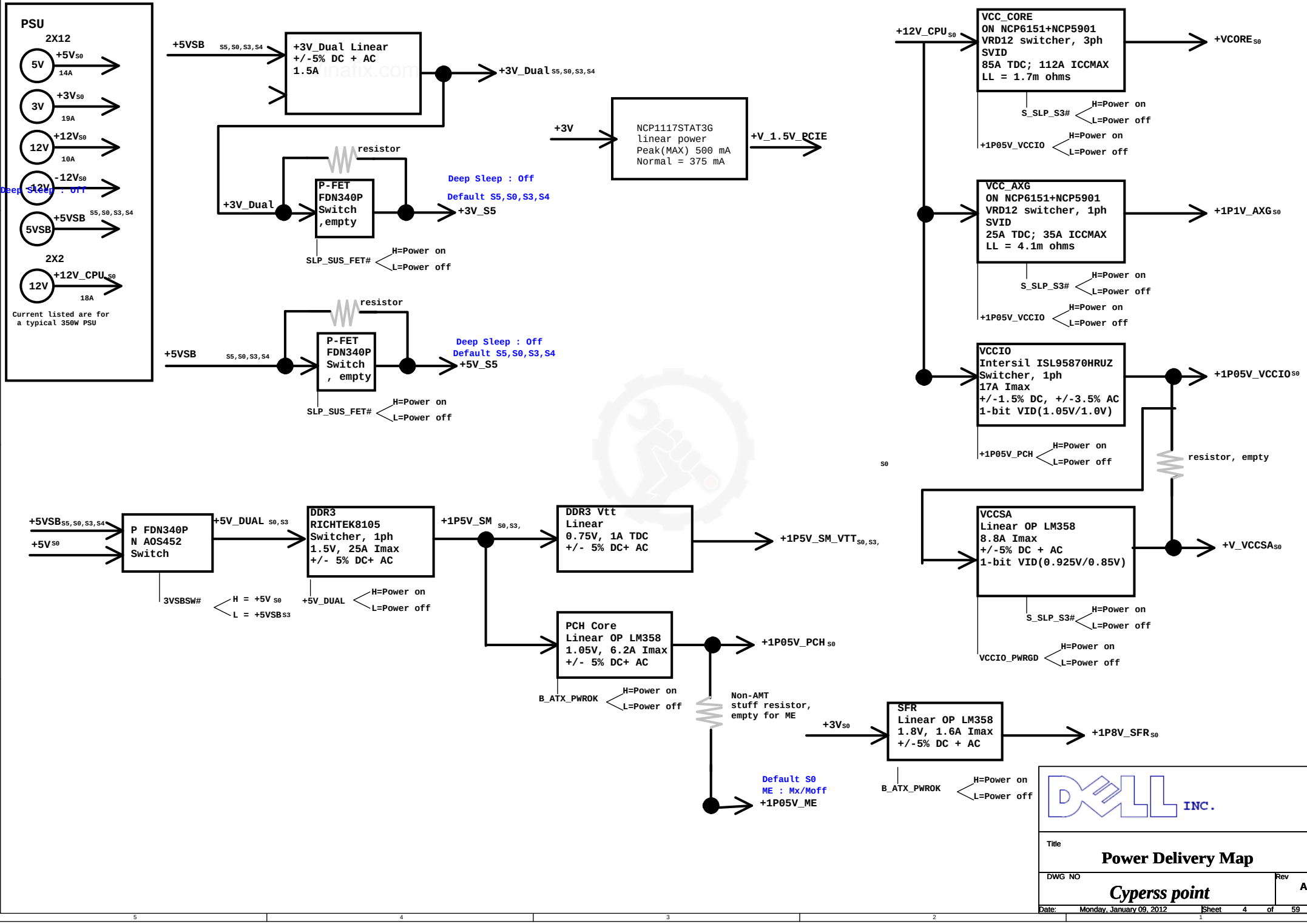
POWER DELIVERY MAP



DELL INC.

Title

Power Delivery Map

DWG NO

Cyperss point

Rev A00

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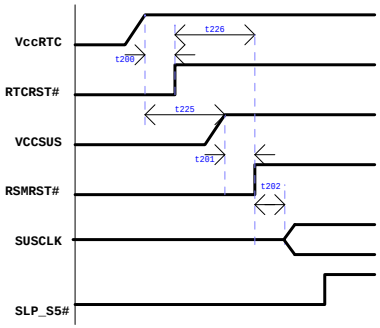
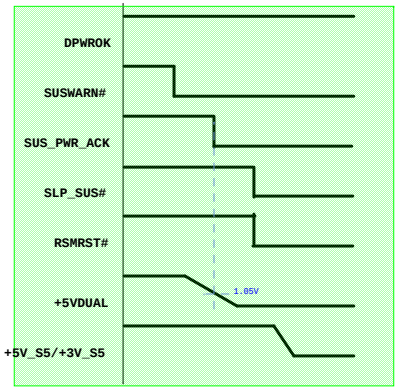
POWER ON Timing Diagram

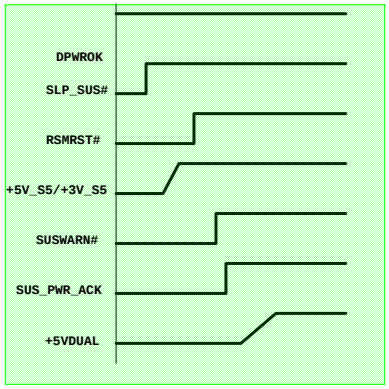
G3 to S4/S5 Timing Diagram

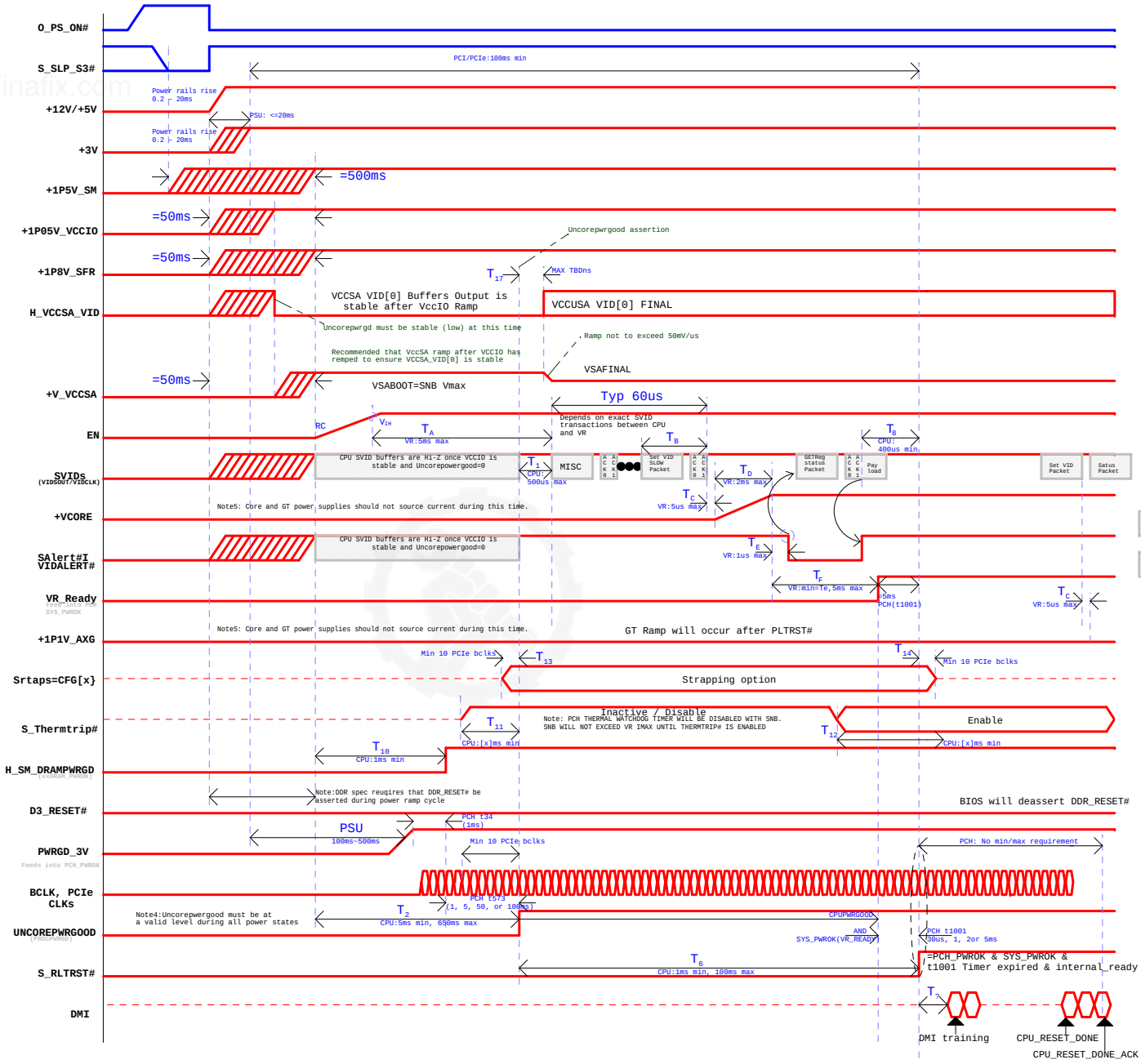


Deep Sleep Entry



Deep Sleep Exit





Title	Power On Sequence
DWG NO	Cyperss point
Rev	A00
Date:	Monday, January 09, 2012
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RESET / Power Good MAP

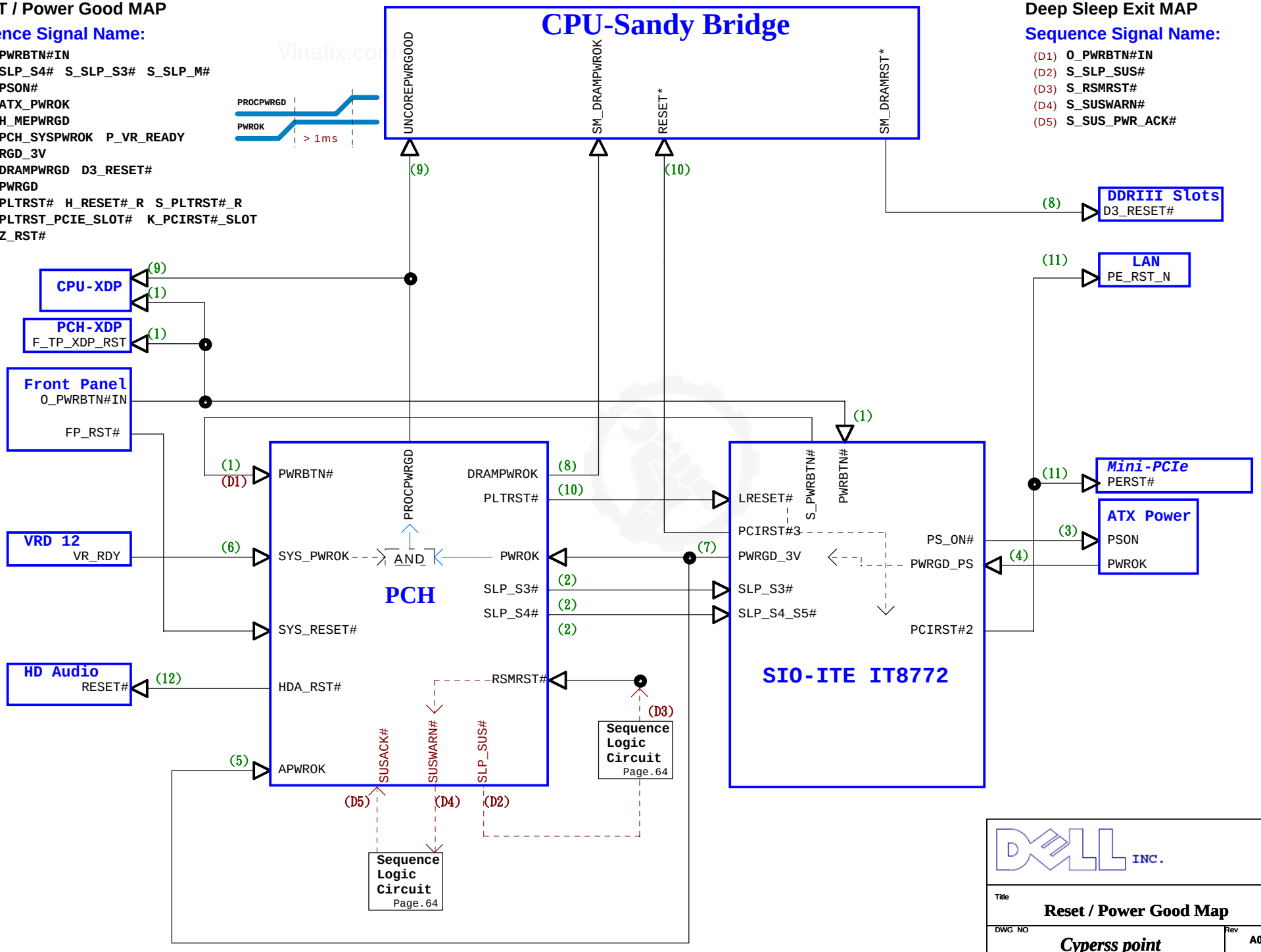
Sequence Signal Name:

(1) O_PWRBTN#IN
(2) S_SLP_S4# S_SLP_S3# S_SLP_M#
(3) O_PSON#
(4) B_ATX_PWROK
(5) PCH_MEPWRGD
(6) S_PCH_SYSPWROK P_VR_READY
(7) PWRGD_3V
(8) H_DRAMPWRGD D3_RESET#
(9) H_PWRGD
(10) S_PLTRST# H_RESET#_R S_PLTRST#_R
(11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
(12) A_Z_RST#

Deep Sleep Exit MAP

Sequence Signal Name:

(D1) O_PWRBTN#IN
(D2) S_SLP_SUS#
(D3) S_RSMRST#
(D4) S_SUSWARN#
(D5) S_SUS_PWR_ACK#



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Title: Reset / Power Good Map

DWG NO: Cyperss point

Rev: A00

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IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot3	C	D	A	B	18	0	0

STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

Clock Gen.

FREQ	C_CK_BSEL0	C_CK_BSEL1	C_CK_BSEL2
100	1	0	1
133	1	0	0

Default

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	C_CK505_33M_PCI2	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI4/SRC5_EN (PIN6)	C_CK505_33M_PCI4	1	SRC5 DEFAULT
		0	CPU_STOP# and PCI_STOP#
PCIF5/ITP_EN (PIN7)	C_CK505_33M_PCI5	1	CPU_ITP
		0	SRC8 DEFAULT
PCI3/CFGP (PIN5)	C_CK505_33M_PCI3	Low	See CFG Table DEFAULT (Set SATA and SRC come from PLL4)
		Mid	See CFG Table
		High	See CFG Table

PCH

On-Die PLL Voltage Regulator Voltage Select

HDA_SYNC	Description
High	1.5V
Low	1.8V DEFAULT

On-Die PLL Voltage Regulator

GPIO28 (IN-PU)	Description
High	Regulator is enabled. DEFAULT
Low	Regulator is disabled.

Topblock Swap Mode

GNT3#/GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable DEFAULT
Low	Topblock swap mode: Enable

No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable DEFAULT

Integrated 1.05V VRM

INTVRMEN	Description
High	Integrated 1.05V VRM: Enable DEFAULT
Low	Integrated 1.05V VRM: Disable

TLS Confidentiality

GPIO15 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality DEFAULT

Flash Descriptor Override Strap

HDA_SDO	Description
High	Flash descriptor security will be override
Low	Disable ME in Manufacturing Mode DEFAULT

DMI Rx Termination Voltage

SPI_MOSI (IN-PD)	Description
Low	DMI Rx Termination Voltage DEFAULT

DMI Termination Voltage

NV_CLE (IN-PU)	Description
High	DMI and FDI Tx/Rx Termination Voltage DEFAULT

Boot BIOS Destination Selection

GNT1# (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
Low	High	Flash cycle routed to NAND
High	High	Flash cycle routed to SPI DEFAULT

Deep S4/S5 Well on-die Voltage Regulator Enable

DSWVRMEN	Description
High	Enable DEFAULT
Low	Disable

Digital Port C Strap

DDPC_CTRLDATA	Description
High	Configure Port C DEFAULT
Low	Disable

DELL INC.

Title: **GPIO/IRQ/IDSEL Table**

DWG NO: *Cyperss point*

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PCH GPIO table

PCH GPIO Summary

GPIO	Mult Function Pin	PIN OUT	Type	Power Well	Default	Signal Name	IN PU/PD	EX PU/PD	*Current Usage (GAUN advertising setting)	Programming Function	Estimated result	Test Result
GPIO[0]	BMBUSY#GPIO0	AH55	I/O	Core	GPI	S_GPI_CHASSIS_LID1	–	10k pull-up to +3V	I	NU		
GPIO[1]	TACH1/GPIO1	BR19	I/O	Core	GPI	S_SEN_CHARAN	20K IN-PU (only on TACH0)	8.2k pull-up to +3V		NU	N/A	
GPIO[2]	PIRQB#/GPIO2	BH9	I/OD	Core	GPI	V_NTSW	–	8.2k pull-up to +3V		NU	N/A	
GPIO[3]	PIRQC#/GPIO3	AU9	I/OD	Core	GPI	V_HDMI_HPD	–	–		I	I: V_HDMI_HPD unuged O: V_HDMI_HPD plugged	D0 V_HDMI_HPD unuged
GPIO[4]	PIRQD#/GPIO4	BT15	I/OD	Core	GPI	V_GPU_VGA_DEN_DETW	–	8.2k pull-up to +3V		I	I: VGA cable unplugged O: VGA cable plugged	D5 VGA cable unplugged
GPIO[5]	PIRQE#/GPIO5	BP4	I/OD	Core	GPI	V_WLAN_DETECTB	–	8.2k pull-up to +3V		I	I: WLAN card unplugged O: WLAN card plugged	D5 WLAN card unplugged
GPIO[6]	TACH2/GPIO6	BA20	I/O	Core	GPI	S_GPI_PCH_HS_DETW	20K IN-PU (only on TACH0)	8.2k pull-up to +3V		I	I: PCH HS unplugged O: PCH HS plugged	D5 PCH HS unplugged
GPIO[7]	TACH3/GPIO7	BR18	I/O	Core	GPI	S_GPI_SYLC	20K IN-PU (only on TACH0)	10k pull-up to +3V (dummy) 330 pull-down to GND		I	reserve for SKU ID	
GPIO[8]	GPIO8	BP21	I/O	Suspend	GPO	S_LCC_EN#		10K IN-PU		NU	N/A pull-down to GND (dummy)	
GPIO[9]	OD3M/GPIO9	Bu41	I/O	Suspend	Native	V_USB_OC_N_45	–	8.2k pull-up to +3V_S5 (dummy)		Native	N/A	
GPIO[10]	OD6M/GPIO10	BT45	I/O	Suspend	Native	V_USB_OC_N_89	–	8.2k pull-up to +3V_S5 (dummy)		NU	N/A	
GPIO[11]	SMBALERT#/GPIO11	BH40	I/O	Suspend	Native	V_I_S_WAKE#	–	10k pull-up to +3V_S5		NU	N/A	
GPIO[12]	SLP_LAN#/GPIO12	BH30	I/O	Suspend	Native	V_LAN_ENABLEM	–			O	I: LAN enable (default) O: LAN disable	LAN enable LAN disable
GPIO[13]	GPIO13	BA35	I/O	Suspend	GPI	GPIO_SW_RELEASE_ENABLEM	–	10k pull-up to +3V_PCH_AUX		O	I: ENABLE ISLAN (DEFAULT) O: DISABLE ISLAN	enable ISLAN Disable ISLAN
GPIO[14]	DSTB/GPIO14	BM45	I/O	Suspend	Native	V_USB_OC_N_67	–	8.2k pull-up to +3V_S5		NU	N/A	
GPIO[15]	GPIO15	BM55	I/O	Suspend	GPO	S_PCH_GPI15	20K IN-PD	10k pull-to +3V_S5		NU	N/A	
GPIO[16]	SATA4GP/GPIO16	AL59	I/O	Core	GPI	S_GPI_BAD_RS1#0	–	10k pull-up to +3V (dummy) 10k pull-down to GND		NU	N/A	
GPIO[17]	TACH4/GPIO17	BT17	I/O	Core	GPI	S_GPI_CHASSIS_LID1	20K IN-PU (only on TACH0)	10k pull-up to +3V (dummy) 10k pull-down to GND		I		
GPIO[18]	SATA1GP/GPIO21	AY52	I/O	Core	GPI	S_SATA1GP	20K IN-PU	10k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	Stragping	N/A	Boot from SPI	
GPIO[20]	PCIECLKRQ2B#/GPIO20	AU43	I/O	Core	Native	S_PCH_GPIO20_PU	–	10k pull-up to +3V 10k pull-down to GND (dummy)	NU	N/A		
GPIO[21]	SATA0GP/GPIO21	BG34	I/O	Core	GPI	S_GPI_BRD_REV0	–	10k pull-up to +3V (dummy) 10k pull-down to GND	I		Default	

BOARD ID

Rev1	Rev0	Type
0	0	Default
0	1	Reserved
1	0	Reserved
1	1	Reserved

GPIO[22]	SCLOCK/GPIO22	BA43	I/O	Core	GPI	S_PCH_CONFIG_JUMPER	–	1k pull-up to +3V 4.7k pull-down to GND (dummy)	NU	N/A	
GPIO[23]	LDRQ1#/GPIO23	BA20	I/O	Core	Native	S_DRQ1#	20K IN-PU	10k pull-up to +3V (dummy)	I	For PLIS test point	
GPIO[24]	MEM_LED/GPIO24	BP63	I/O	Suspend	GPO	M_NTTOCC#	–	10K pull-up to +3V_S5	I	0: default O: CPU present	CPU not present CPU present
GPIO[27]	GPIO27	Bu43	I/O	Deep Sleep	GPI	S_GPI27_PD	20K IN-PU	10k pull-up to +3V_DUAL 10k pull-down to GND (dummy)	NU	N/A	
GPIO[28]	GPIO28	BJ35	I/O	Suspend	GPO	S_PCH_GPI28_PU	20K IN-PU	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	Stragping	N/A	
GPIO[29]	SLP_LAN#/GPIO29	BH49	I/O	Suspend	Native	S_SLP_LAN#	–	1k pull-up to +3V_S5 (dummy)	Native	N/A	
GPIO[30]	SUSCLK/GPIO30	BU46	I/O	Deep Sleep	Native	S_SUSCLK#GPI	–	10k pull-up to +3V_DUAL (dummy)	Native	N/A	
GPIO[31]	GPIO31	BG43	I/O	Deep Sleep	GPI	S_PRWD_CLR	TBD IN-PD	8.2k pull-up to +3V_DUAL	I	I: Clear Password O: normal (default)	clear password default

SKU ID

SKU1E	SKU0E	Type
0	0	TPM
0	1	TCM
1	0	NO TPM/NO TCM
1	1	Reserved

GPIO[32]	CLKRUN#/GPIO32	BG55	I/O	Core	GPO	S_GPI_SKU0	–	10k pull-up to +3V (dummy) 330 pull-down to GND	I		TPM/NO TPM_NO TCM TCM Reserved
GPIO[33]	HAD_DOCK_ENB#/GPIO33	BC28	I/O	Core	GPO	–	–	–	NU	N/A	
GPIO[34]	STP_PCI#/GPIO34	BJ36	I/O	Core	GPI	S_GPI_CHASSIS_EO	–	10k pull-up to +3V 10k pull-down to GND (dummy)	I		
GPIO[35]	GPIO35	BJ37	I/O	Core	GPO	S_GPI_SKU1	–	10k pull-up to +3V (dummy) 330 pull-down to GND	I		TPM/TCM NO TPM_NO TCM Reserved
GPIO[36]	SATA2GP/GPIO36	BB55	I/O	Core	GPI	GPIO36	20K IN-PD	–	NU		
GPIO[37]	SATA3GP/GPIO37	BG63	I/O	Core	GPI	GPIO37	20K IN-PD	–	NU		
GPIO[38]	SLOAD/GPIO38	BB54	I/O	Core	GPI	M1537-O	–	10k pull-up to +3V (dummy) 10k pull-down to GND	I		
GPIO[39]	SDATAOUT0/GPIO39	BP55	I/O	Core	GPI	A_PA_PRSM	–	10k pull-up to +3V	I	I: Front Audio cable unplugged O: Front Audio cable plugged	Front Audio cable unplugged Front Audio cable plugged
GPIO[40]	OC1#/GPIO40	BG41	I/O	Suspend	Native	V_USB_OC_N_A#	–	10k pull-up to +3V_DUAL and 15k pull-down to GND		Native	For Over current function	Lees as USB OC default
GPIO[41]	OC2#/GPIO41	BG41	I/O	Suspend	Native	V_USB_OC_N_B#	–	10k pull-up to +3V_DUAL and 15k pull-down to GND		Native	For Over current function	Lees as USB OC default
GPIO[42]	OC3#/GPIO42	BG43	I/O	Suspend	Native	V_USB_OC_N_C#	–	10k pull-up to +3V_DUAL and 15k pull-down to GND		Native	For Over current function	Lees as USB OC default

GPIO[32]	SCLOCK/GPIO22	BA43	I/O	Core	GPI	S_PCH_CONFIG_JUMPER	–	1k pull-up to +3V 4.7k pull-down to GND (dummy)	NU	N/A	
GPIO[33]	LDRQ1#/GPIO23	BA20	I/O	Core	Native	S_DRQ1#	20K IN-PU	10k pull-up to +3V (dummy)	I	For PLIS test point	
GPIO[24]	MEM_LED/GPIO24	BP63	I/O	Suspend	GPO	M_NTTOCC#	–	10K pull-up to +3V_S5	I	0: default O: CPU present	CPU not present CPU present
GPIO[27]	GPIO27	Bu43	I/O	Deep Sleep	GPI	S_GPI27_PD	20K IN-PU	10k pull-up to +3V_DUAL 10k pull-down to GND (dummy)	NU	N/A	
GPIO[28]	GPIO28	BJ35	I/O	Suspend	GPO	S_PCH_GPI28_PU	20K IN-PU	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	Stragping	N/A	
GPIO[29]	SLP_LAN#/GPIO29	BH49	I/O	Suspend	Native	V_SLP_LAN#	–	1k pull-up to +3V_S5 (dummy)	Native	N/A	
GPIO[30]	SUSCLK/GPIO30	BU46	I/O	Deep Sleep	Native	S_SUSCLK#GPI	–	10k pull-up to +3V_DUAL (dummy)	Native	N/A	
GPIO[31]	GPIO31	BG43	I/O	Deep Sleep	GPI	S_PRWD_CLR	TBD IN-PD	8.2k pull-up to +3V_DUAL	I	I: Clear Password O: normal (default)	clear password default

SKU ID

SKU1E	SKU0E	Type
0	0	TPM
0	1	TCM
1	0	NO TPM/NO TCM
1	1	Reserved

GPIO[32]	CLKRUN#/GPIO32	BG55	I/O	Core	GPO	S_GPI_SKU0	–	10k pull-up to +3V (dummy) 330 pull-down to GND	I		TPM/NO TPM_NO TCM TCM Reserved
GPIO[33]	HAD_DOCK_ENB#/GPIO33	BC28	I/O	Core	GPO	–	–	–	NU	N/A	
GPIO[34]	STP_PCI#/GPIO34	BJ36	I/O	Core	GPI	S_GPI_CHASSIS_EO	–	10k pull-up to +3V 10k pull-down to GND (dummy)	I		
GPIO[35]	GPIO35	BJ37	I/O	Core	GPO	S_GPI_SKU1	–	10k pull-up to +3V (dummy) 330 pull-down to GND	I		TPM/TCM NO TPM_NO TCM Reserved
GPIO[36]	SATA2GP/GPIO36	BB55	I/O	Core	GPI	GPIO36	20K IN-PD	–	NU		
GPIO[37]	SATA3GP/GPIO37	BG63	I/O	Core	GPI	GPIO37	20K IN-PD	–	NU		
GPIO[38]	SLOAD/GPIO38	BB54	I/O	Core	GPI	M1537-O	–	10k pull-up to +3V (dummy) 10k pull-down to GND	I		
GPIO[39]	SDATAOUT0/GPIO39	BP55	I/O	Core	GPI	A_PA_PRSM	–	10k pull-up to +3V	I	I: Front Audio cable unplugged O: Front Audio cable plugged	Front Audio cable unplugged Front Audio cable plugged
GPIO[40]	OC1#/GPIO40	BG41	I/O	Suspend	Native	V_USB_OC_N_A#	–	10k pull-up to +3V_DUAL and 15k pull-down to GND		Native	For Over current function	Lees as USB OC default
GPIO[41]	OC2#/GPIO41	BG41	I/O	Suspend	Native	V_USB_OC_N_B#	–	10k pull-up to +3V_DUAL and 15k pull-down to GND		Native	For Over current function	Lees as USB OC default
GPIO[42]	OC3#/GPIO42	BG43	I/O	Suspend	Native	V_USB_OC_N_C#	–	10k pull-up to +3V_DUAL and 15k pull-down to GND		Native	For Over current function	Lees as USB OC default

GPIO[43]	OC4#/GPIO43	BP43	I/O	Suspend	Native	V_USB_OC_N_44	–	10k pull-up to +3V_DUAL and 15k pull-down to GND	NU	For Over current function	
GPIO[44]	PCIECLKRQ0B#/GPIO44	BL54	I/O	Suspend	Native	V_PWRLID_ISB_DETW	20K IN-PU	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	I	I: Chassis lid cover cable unplugged O: Chassis lid cover cable plugged	lid cover cable unplugged lid cover cable plugged
GPIO[45]	PCIECLKRQ6B#/GPIO45	AV44	I/O	Suspend	Native	V_CLOCK_SMRY_DETW	–	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	I	I: serial port 1 cable unplugged O: serial port 1 cable plugged	serial port 1 cable unplugged serial port 1 cable plugged
GPIO[46]	PCIECLKRQ7B#/GPIO46	BP55	I/O	Suspend	Native	V_GPI_BRD_REV1	20K IN-PU	10k pull-up to +3V_S5 (dummy) 10k pull-down to GND	I		Default
GPIO[49]	SDATAOUT1/GPIO49	AS63	I/O	Core	GPI	P_USB_DETECT1	–	10k pull-up to +3V	I	For USB port 9 I: Front USB cable unplugged O: Front USB cable plugged	internal USB cable unplugged internal USB cable plugged
GPIO[48]	SATA5GP/GPIO48	BA55	I/O	Core	GPI	P_USB_DETECT3	–	10k pull-up to +3V	I	For USB port 8/9 I: Front USB cable unplugged O: Front USB cable plugged	internal USB cable unplugged internal USB cable plugged
GPIO[50]	REQ1#/GPIO50	BT5	I/O	Core	Native	N_REQ#1	–	8.2k pull-up to +3V	NU	N/A	
GPIO[51]	GNT1#GPIO51	AU8	I/O	Core	Native	N_GNT#1	20K IN-PU	1k pull-up to +3V (dummy) 1k pull-down to GND (dummy)	Stragping	N/A	Boot from SPI
GPIO[52]	REQ3#/GPIO52	BH8	I/O	Core	Native	N_REQ#3	–	8.2k pull-up to +3V	NU	N/A	
GPIO[53]	GNT3#GPIO53	BU12	I/O	Core	Native	N_GNT#3	20K IN-PU	1k pull-down to GND (dummy)	Stragping	N/A	
GPIO[54]	REQ2#/GPIO54	AU11	I/O	Core	Native	N_REQ#2	–	8.2k pull-up to +3V	NU	N/A	
GPIO[55]	GNT2#/GPIO55	BB2	I/O	Core	Native	N_GNT#2	20K IN-PU	1k pull-down to GND (dummy)	Stragping	N/A	
GPIO[57]	GPIO57	BT53	I/O	Suspend	GPI	S_GPI1267_PD	–	10k pull-up to +3V_S5 (dummy) 47k pull-down to GND	NU	N/A	
GPIO[59]	SMLI1/GPIO59	Bu46	I/O	Suspend	Native	S_SMLI1_CLK	–	10k pull-up to +3V_S5	Native	N/A	Lees as S_SMLI1_CLK
GPIO[58]	OD5M/GPIO58	BN43	I/O	Suspend	Native	V_USB_OC_N_45	–	10k pull-up to +3V_DUAL and 15k pull-down to GND	Native	For Over current function	Lees as USB OC default
GPIO[60]	SMLI0ALERT#/GPIO60	BU40	I/O	Suspend	Native	V_I_N_HLOWER	–	10k pull-up to +3V_S5	I	For suspend load I: default O: HLAN wake up event	default HLAN wake up event
GPIO[61]	SLI_GTX/GPIO61	BH54	I/O	Suspend	Native	S_LPCPDN	–	8.2k pull-up to +3V_S5 (dummy)	Native	N/A	Lees as S_LPCPDN
GPIO[62]	SLI/GPIO62	BN7	I/O	Suspend	Native	–	–	–	Native	N/A	
GPIO[63]	SLP_S5#/GPIO63	BH50	I/O	Suspend	Native	S_PCH_ALW_GATE	–	10k pull-up to +3V_S5	O	I: VR_RTCALW gate control (default) O: VR_RTCALW off	default VR_RTCALW off
GPIO[64]	CLK01_TPU_EN1/GPIO64	AT9	I/O	Core	Native	S_TP_CLK01_TPU_EN1	20K IN-PD	–	NU	N/A	
GPIO[65]	CLK01_TPU_EO1/GPIO65	BP8	I/O	Core	Native	S_48G_EO	20K IN-PD	–	Native	48 MHz to EC	Lees as 48MHz to EC
GPIO[66]	CLK01_TPU_EO2/GPIO66	AW8	I/O	Core	Native	S_TP_CLK01_TPU_EO2	20K IN-PD	–	NU	N/A	
GPIO[67]	CLK01_TPU_EO3/GPIO67	BA2	I/O	Core	Native	–	20K IN-PD	–	NU	N/A	
GPIO[68]	TACH5/GPIO68	BU16	I/O	Core	GPI	S_GPI_SKU3	20K IN-PU (only on TACH0)	10k pull-up to +3V 330 pull-down to GND (dummy)	I	reserve for SKU ID	
GPIO[69]	TACH6/GPIO69	BW16	I/O	Core	GPI	INT_USB_DETECT1	20K IN-PU (only on TACH0)	10k pull-up to +3V	I	For USB port 5/11 I: internal USB cable unplugged O: internal USB cable plugged	internal USB cable unplugged internal USB cable plugged
GPIO[70]	TACH7/GPIO70	BN17	I/O	Core	Native	INT_USB_DETECT0	20K IN-PU (only on TACH0)	8.2k pull-up to +3V	I	For USB port 10/11 I: internal USB cable unplugged O: internal USB cable plugged	internal USB cable unplugged internal USB cable plugged
GPIO[71]	TACH8/GPIO71	BP15	I/O	Core	Native	–	20K IN-PU (only on TACH0)	10k pull-up to +3V	NU	N/A	
GPIO[72]	SATLED#/GPIO72	AU45	I/O	Suspend	Native/ Active	S_PCH_GPI72_PU	–	10k pull-up to +3V_S5	NU	N/A	
GPIO[74]	SLI_MUX#/GPIO74	BP45	I/O	Suspend	Native	S_GPI_MUX_EN	–	10k pull-up to +3V_S5 (dummy)	O	I: Enter MFG Mode O: Disable	Enter MFG Mode Disable
GPIO[76]	SMLI2C#/GPI76	BN45	I/O	Suspend	Native	S_SMLI1_CLK1	–	10k pull-up to +3V_S5	Native	N/A	Lees as S_SMLI1_CLK1

*Current Usage
Initialize
1 used as GPI
O: used as GPO
NU: are used
Native: used as native function
Stragping: used as strapping

SIO GPIO table

SIO_8771 GPIO Summary

PIN	GPIO	PIN NAME	Power well	Buffer Type	Signal Name	EX PU/PD	Current Usage	Notes
1	GP10	nSMI_1/GA20IN	AVCC3	OD08	S_SMI_1#/A20	With a pull-down RX120 470Ohm and pull-up with R2120 2.2K ohm to +3V and pull-down to GND via R2122 470Ohm	NU	
2	GP11	nSMI_2/CLKRUN	AVCC3	OD08	S_SMI2#_PME		NU	
3	GP12	nSMI_3/LPCPD#	AVCC3	OD08	S_SMI3#_PME	With a pull-down RX130 470Ohm and pull-up with R2119 2.2K ohm to +3V and pull-down to GND via R2127 470Ohm	NU	
4	GP13	nSMI_4/SCI#	AVCC3	OD08	S_SMI_PME		NU	
5	GP20	nRI1/GPIO20	AVCC3	OD08	S_RI1#_PME	Pull-up to +3V	NU	
6	GP21	nRI2/GPIO21	AVCC3	OD08	S_RI2#_PME	Pull-up to +3V	NU	
7	GP22	CPU_PWRGD	AVCC3	OD08	S_PWRGD	Pull-up to +3V_DUAL	LED	Note1 1: Enable 0: disable
8	GP23	nPCI_RST	AVCC3	OD08	S_PCIRST_PCIB_EC#_R	Pull-up to +3V	NU	
9	GP24	nSCI/SWI/IRQ	AVCC3	OD08	S_SCI_EC#	Pull-up to +3V	NU	
10	GP25	nSMI/SWI/IRQ/PS2	AVCC3	OD08	S_SMI_EC#	Pull-up to +3V_DUAL	NU	
11	GP26	PS2DAT/IRQ	AVCC3	OD08	S_PS2DAT	Pull-up to +3V_S5	NU	
12	GP27	PS2CLK/IRQ	AVCC3	OD08	S_PS2CLK	Pull-up to +3V_S5	NU	
13	GP30	nRI3/GPIO30	AVCC3	OD08	S_RI3#_PME	Pull-up to +3V_DUAL	NU	
14	GP31	nRI4/GPIO31	AVCC3	OD08	S_RI4#_PME	Pull-up to +3V_DUAL	NU	
15	GP32	nDCD1/GPIO32	AVCC3	OD08	S_DCD1#	Pull-up to +3V_DUAL	NU	
16	GP33	nDSR1/GPIO33	AVCC3	OD08	S_DSR1#	Pull-up to +3V_DUAL	NU	
17	GP34	nRTS1/GPIO34	AVCC3	OD08	S_RTS1#	Pull-up to +3V_DUAL	NU	
18	GP35	nDTR1/GPIO35	AVCC3	OD08	S_DTR1#	Pull-up to +3V_DUAL	NU	
19	GP36	nCTS1/GPIO36	AVCC3	OD08	S_CTS1#	Pull-up to +3V_DUAL	NU	
20	GP37	nDCD2/GPIO37	AVCC3	OD08	S_DCD2#	With a pull-down RX85 10ohm and pull-up with R2083 330 ohm to +3V and pull-down to GND via R2082 1210ohm	NU	
21	GP40	nDSR2/GPIO40	AVCC3	OD08	S_DSR2#	Pull-up to +3V_DUAL	NU	
22	GP41	nRTS2/GPIO41	AVCC3	OD08	S_RTS2#	Pull-up to +3V_DUAL	NU	
23	GP42	nDTR2/GPIO42	AVCC3	OD08	S_DTR2#	Pull-up to +3V_DUAL	NU	
24	GP43	nCTS2/GPIO43	AVCC3	OD08	S_CTS2#	Pull-up to +3V_DUAL	NU	

*Current Usage definitionen:
1: used as GPO
O: used as GPO
NU: are used
Native: used as native function
Stragping: used as strapping

Note1: Please follow below table Function Table (Based on your BOM PN)

Common Chip	as GPI LED Chain	Function
GPI (SW01)	Power LED ON	Common is either as built GPI (SW01, Mechanical GPI SW), or Support to Dock (SW).
as GPI (SW)	Power LED Solid Amber	Common is as a Windows Quality Power State, Power LED Solid Amber, Power LED Blinking Amber, Power LED Solid White, Power LED Blinking White, Power LED Off.
Follow as PIN27	Power LED Blinking Amber	Common is as a Windows Quality Power State, Power LED Solid Amber, Power LED Blinking Amber, Power LED Solid White, Power LED Blinking White, Power LED Off.
Via PIN27	Power LED Solid Amber	When GPO does not blink and write, display is PIN27 should change Power LED from White to Amber. When GPO does not blink and write, display is common, write PIN27 as 1/0 (Whatever is opposite).
Reversed Operations, as GPI (SW)	Power LED Solid White	Common has reversed(By hardware) as opposite operation.

Title	GPIO Table	
DWG NO	Cyperss point	Rev A00
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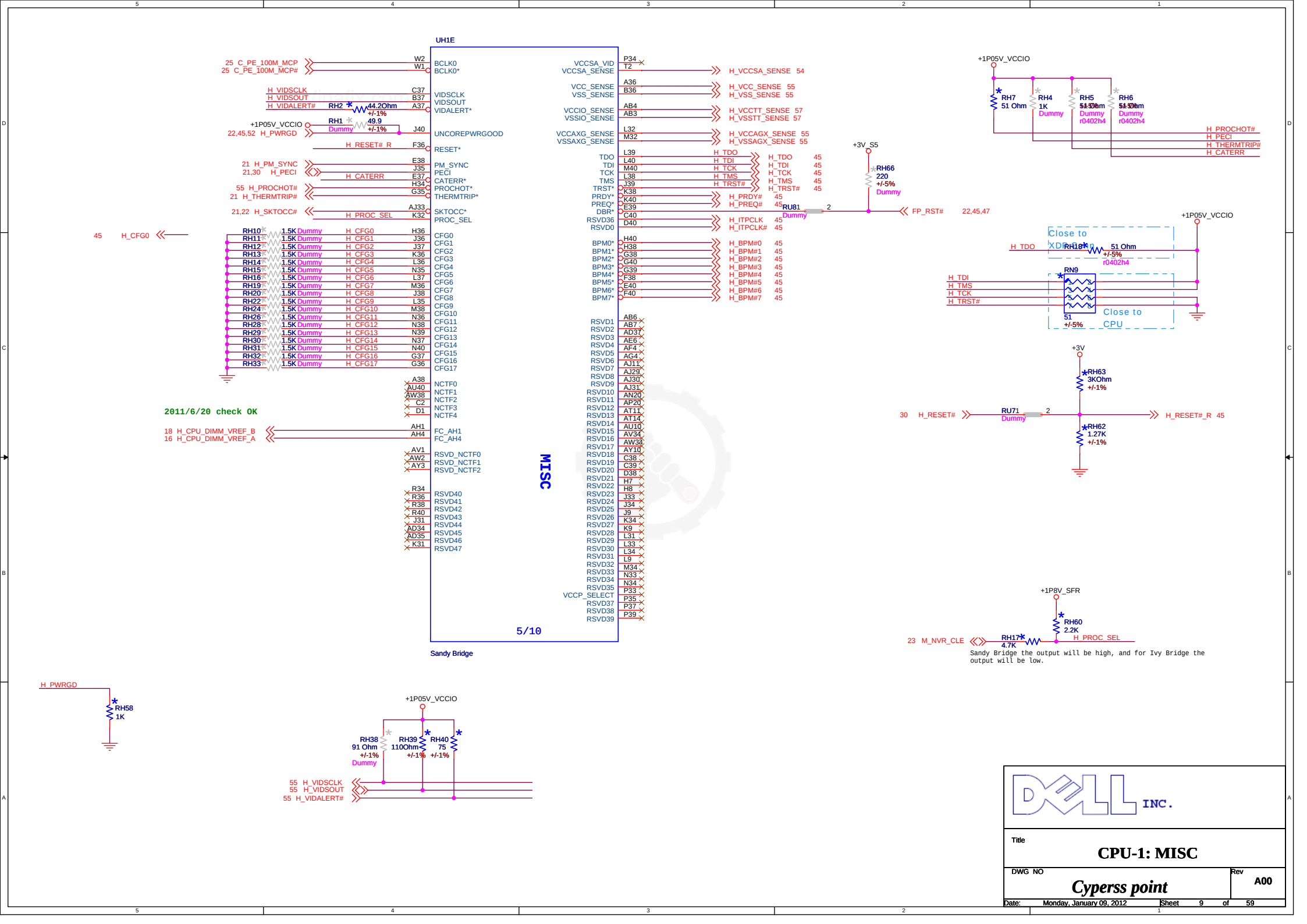
UH1E
MISC
5/10
Sandy Bridge
2011/6/20 check OK
Close to XDP Probe
Close to CPU
Sandy Bridge the output will be high, and for Ivy Bridge the output will be low.
DELL INC.
Title
CPU-1: MISC
DWG NO
Cyperss point
Rev
A00
Date: Monday, January 09, 2012
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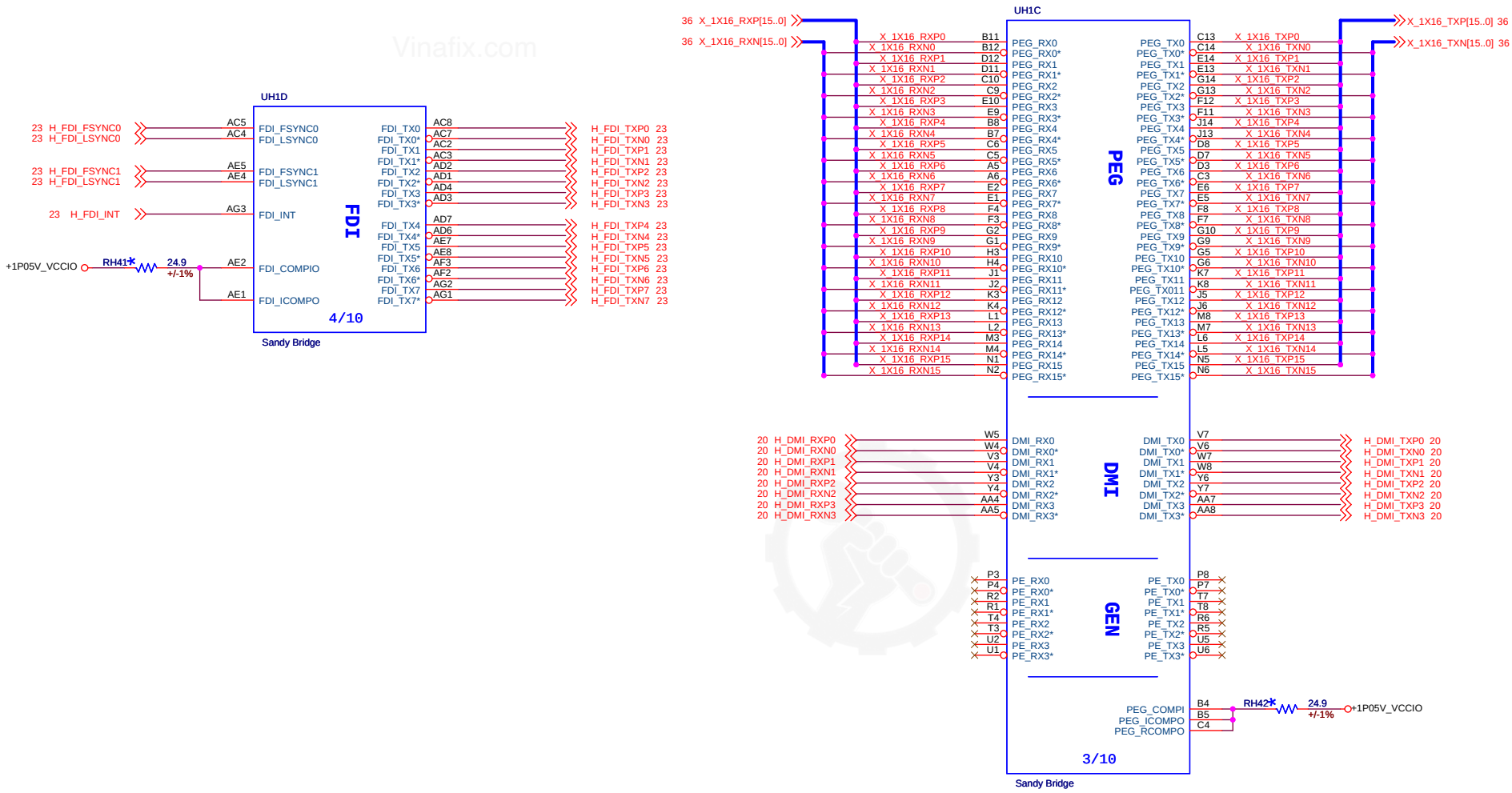


DELL INC.

Title

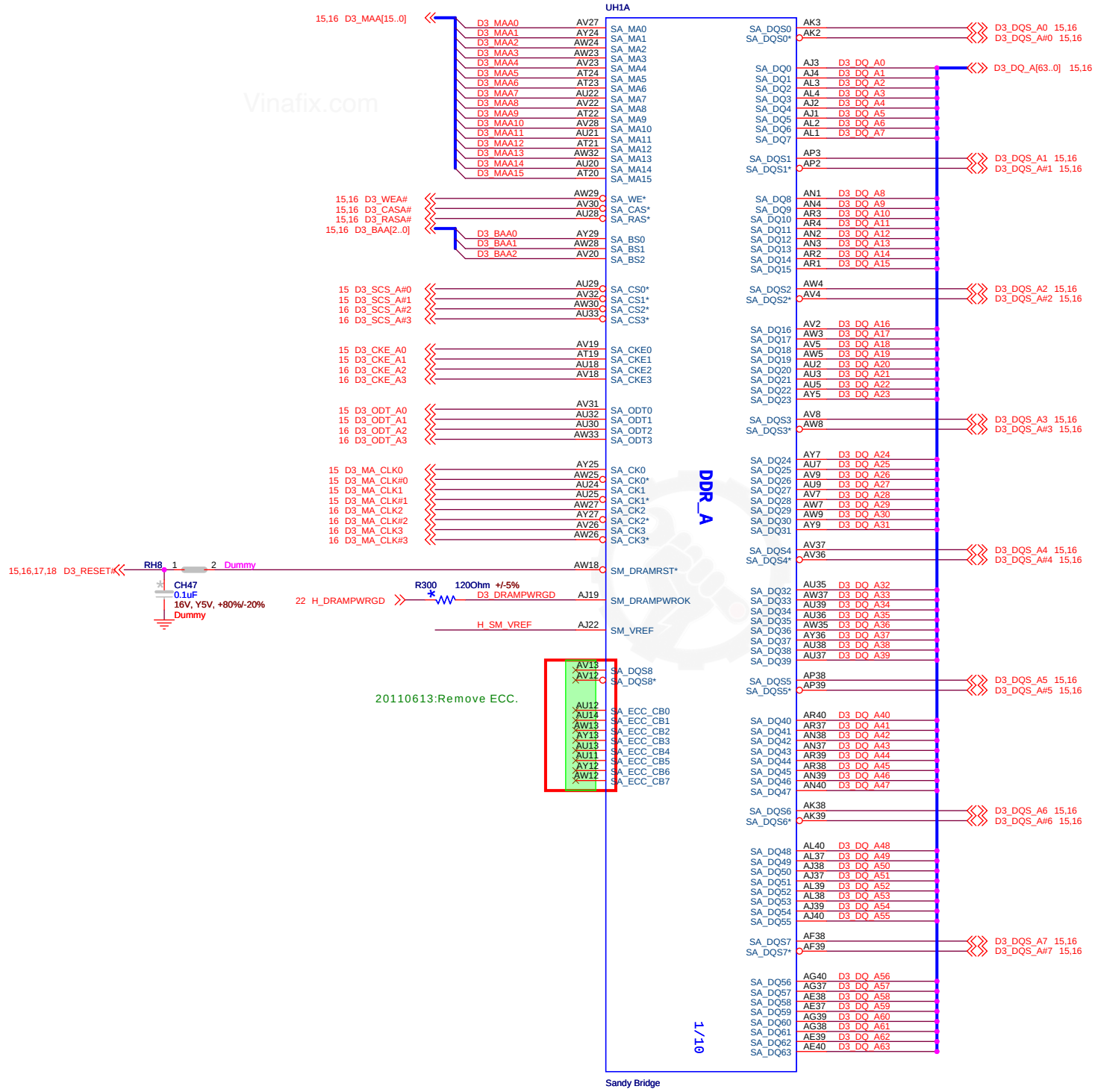
CPU-2: FDI/PCIe/DMI

DWG NO

Cyperss point

Rev A00

Date: Thursday, March 22, 2012 Sheet 10 of 59



DELL INC.

Title

CPU-3: DDR3_CHA

DWG NO

Cyperss point

Rev A00

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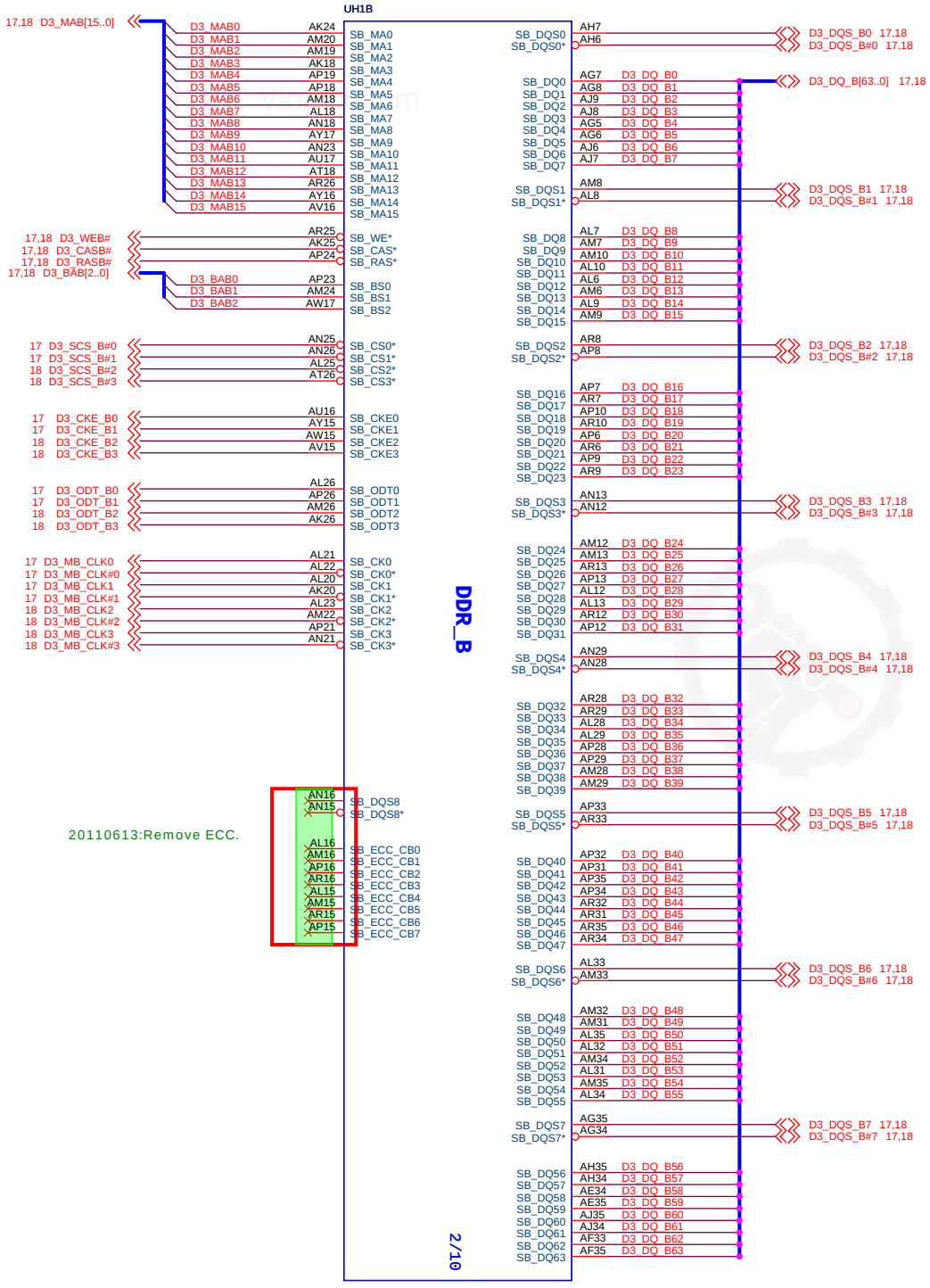

DELL INC.

Title

CPU-4: DDR3_CHB

DWG NO

Cyperss point

Rev A00

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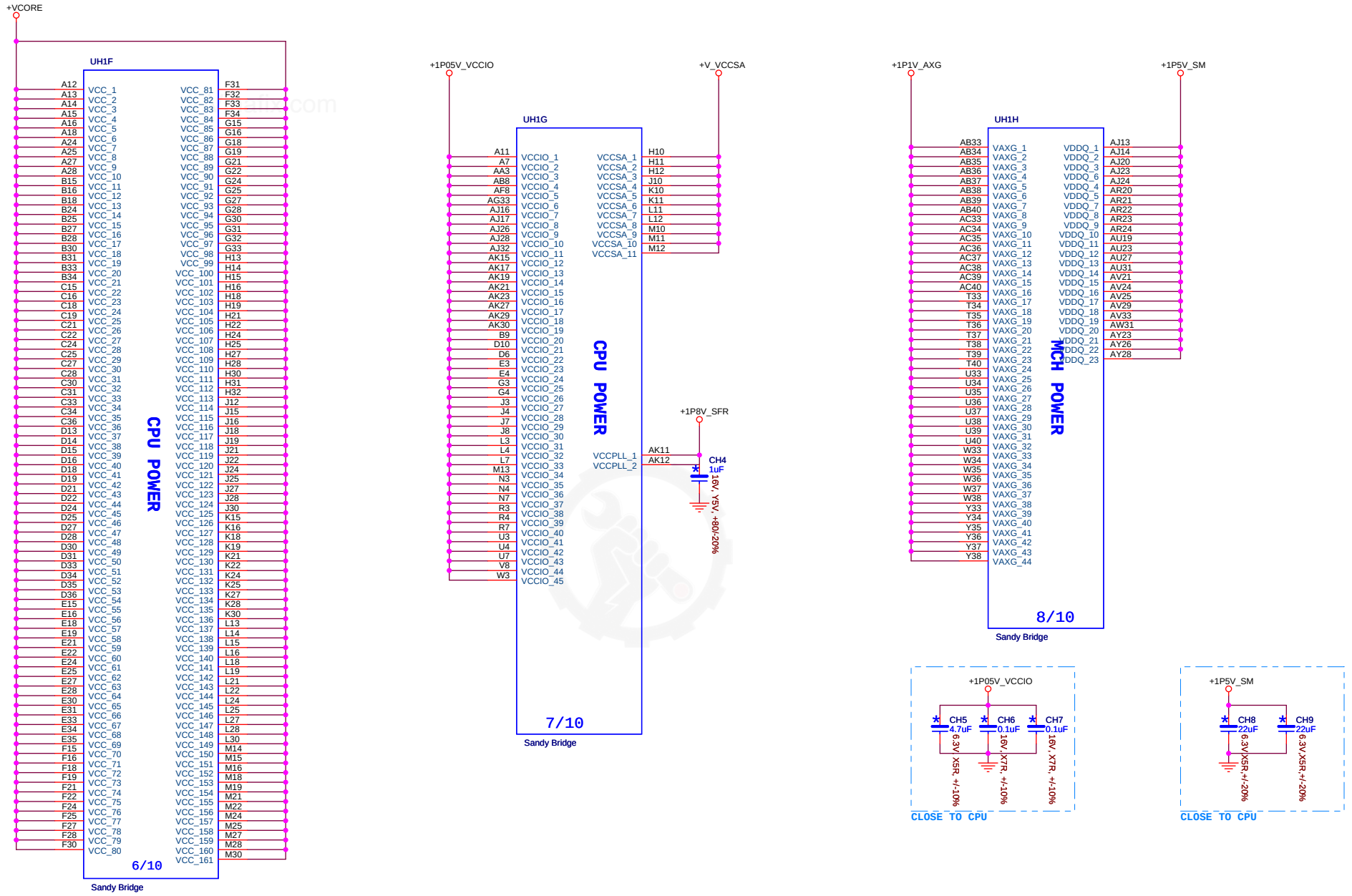

DELL INC.

Title

CPU-5: Power

DWG NO

Cyperss point

Rev A00

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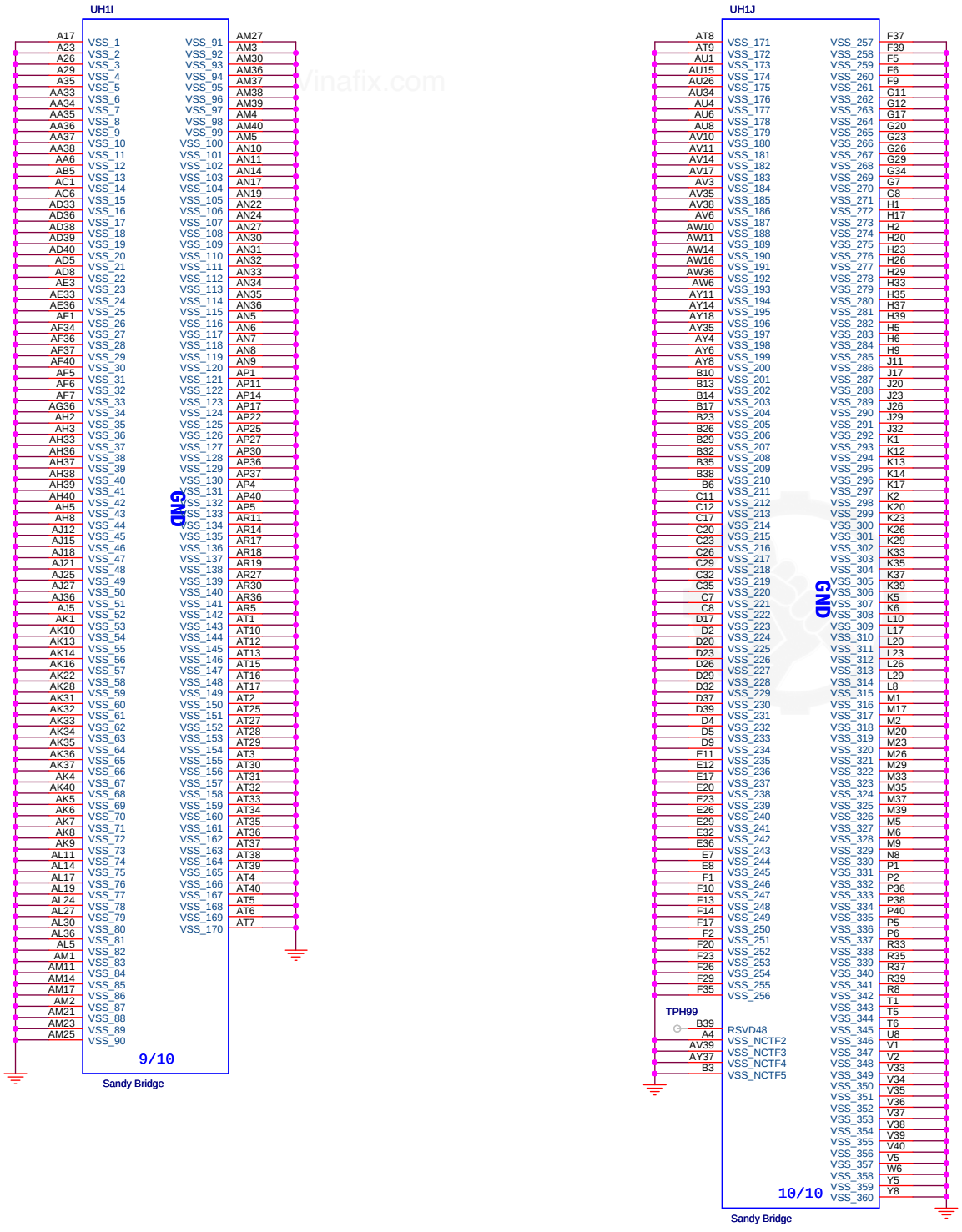


DELL INC.

Title

CPU-6: GND

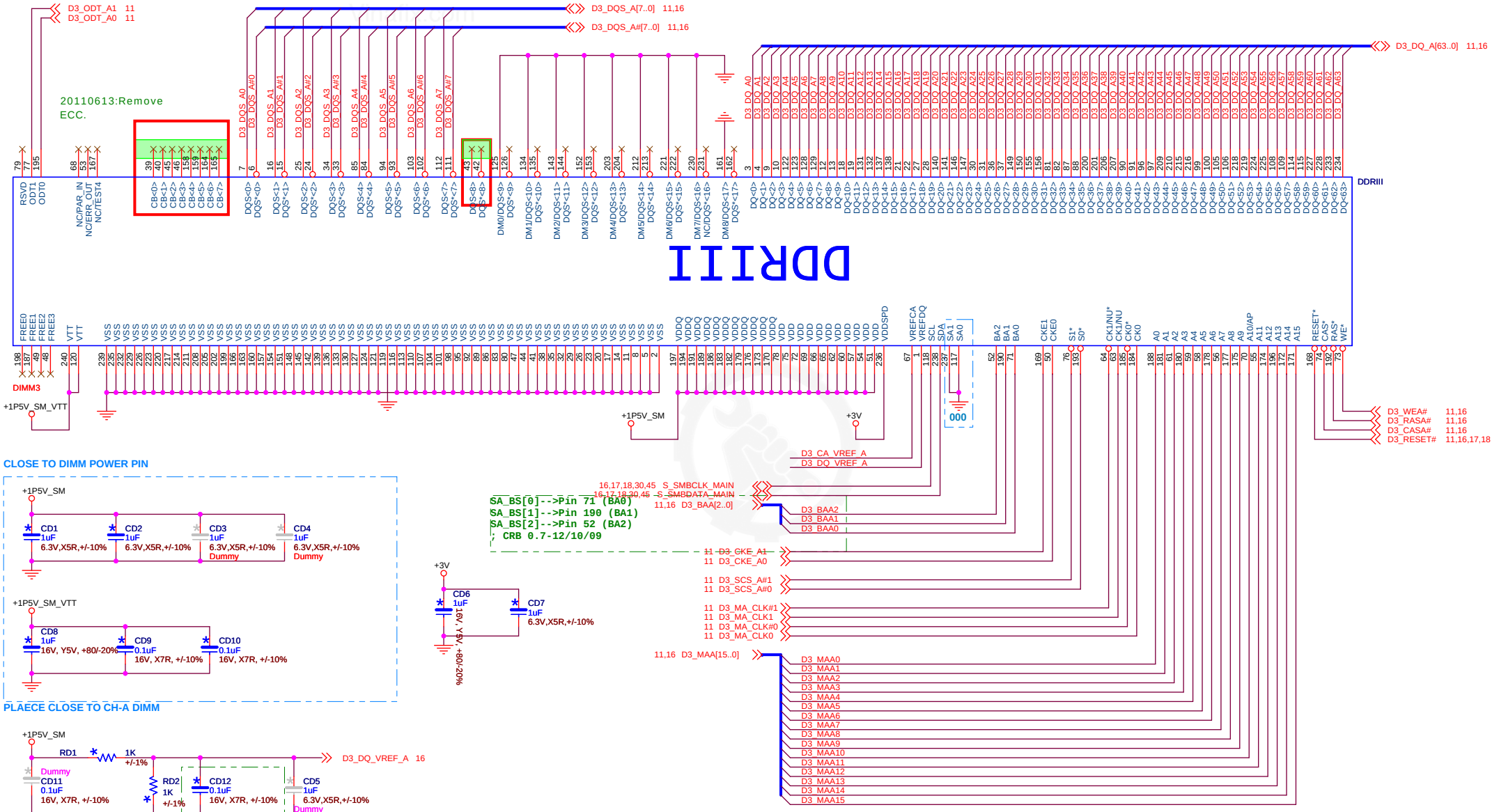
DWG NO

Cyperss point

Rev A00

Date: Monday, January 09, 2012 Sheet 14 of 59

CHANNEL A BANK 1
SMB ADDRESS:000



DELL INC.

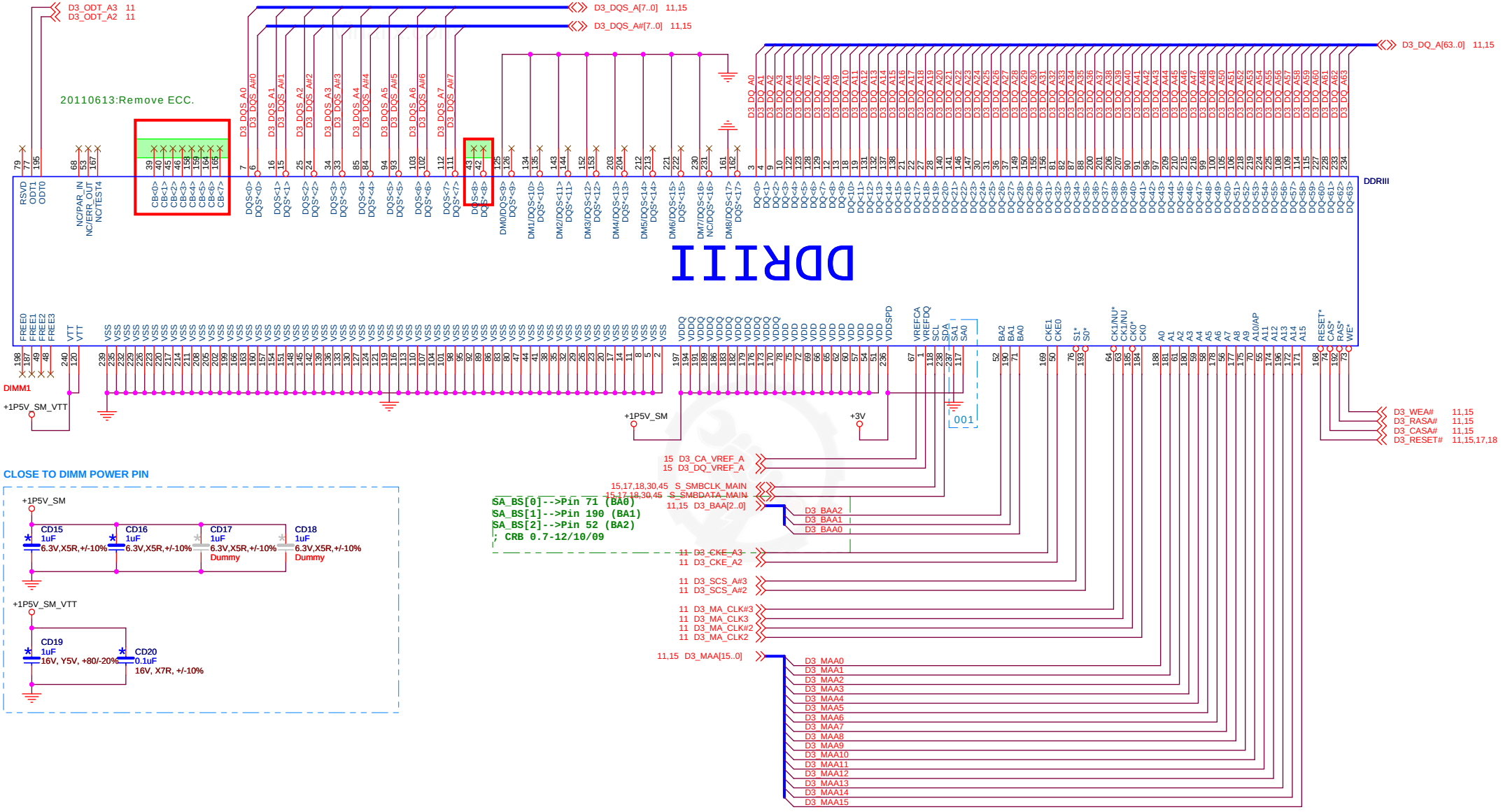
Title
DDR3 Conn: CHA_1 (DIMM3)

DWG NO
Cyperss point

Rev
A00

Date: Monday, January 09, 2012 Sheet 15 of 59

CHANNEL A BANK 2
SMB ADDRESS:001



DELL INC.

Title
DDR3 Conn: CHA_2 (DIMM1)

DWG NO
Cyperss point

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A00

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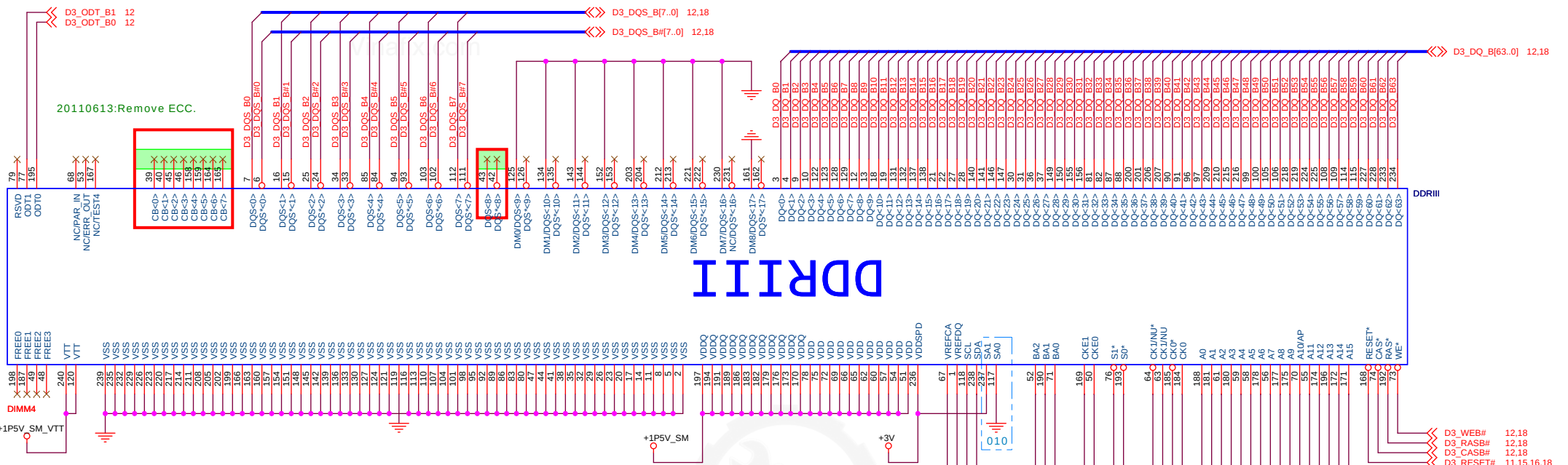
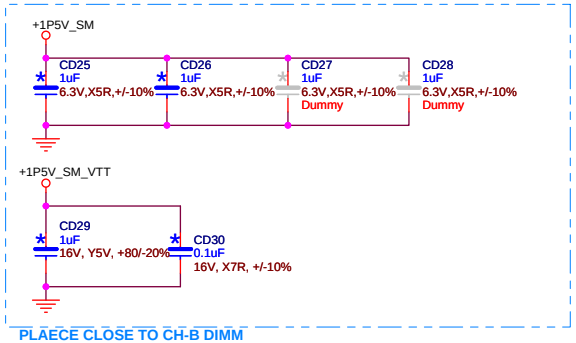
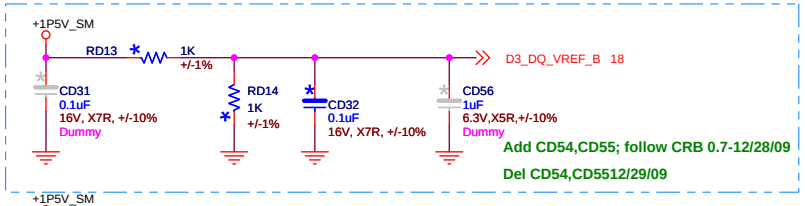
CHANNEL B BANK 1
SMB ADDRESS:010

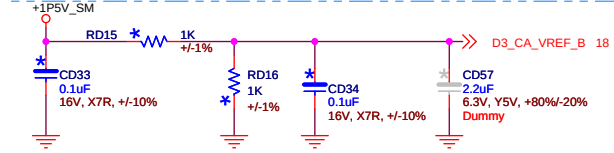


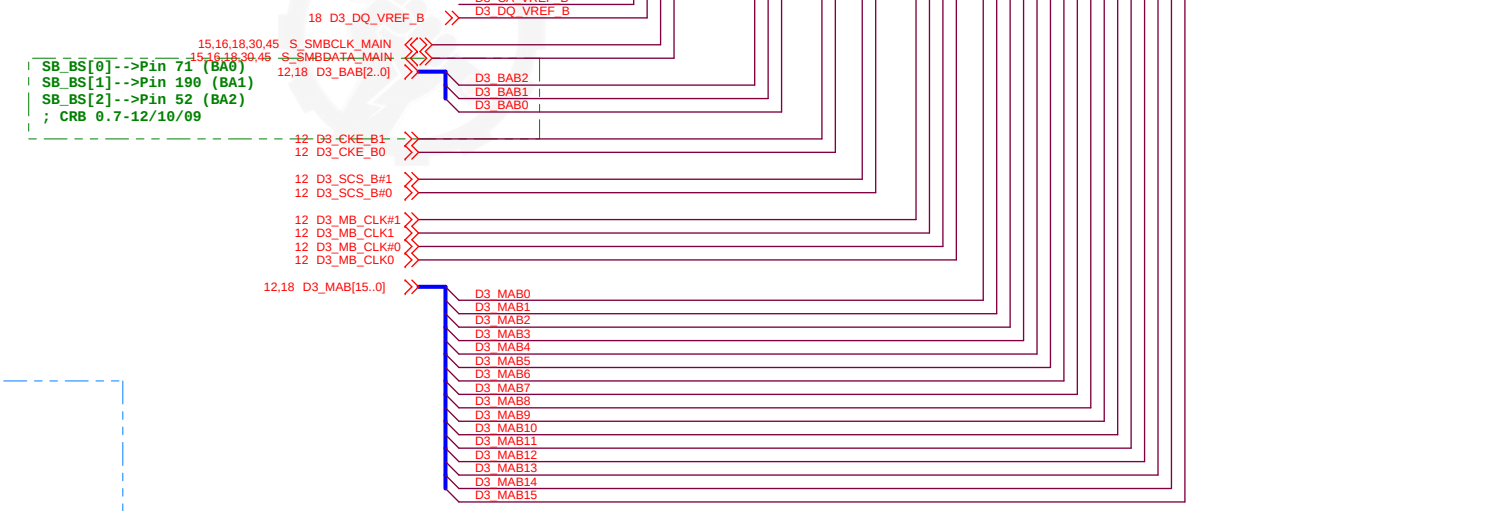
CLOSE TO DIMM POWER PIN



PLAECE CLOSE TO CH-B DIMM







DELL INC.

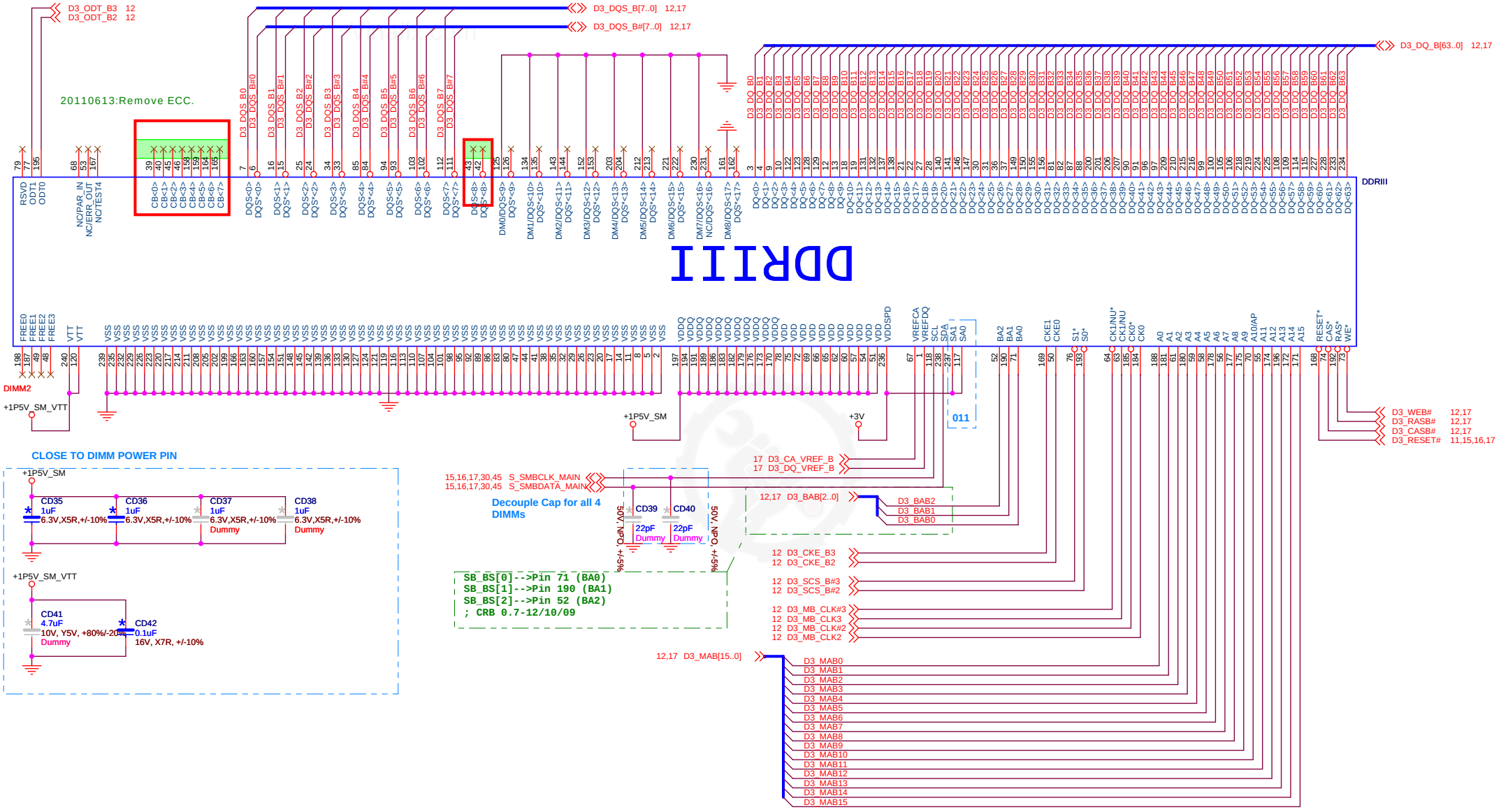
Title
DDR3 Conn: CHB_1 (DIMM4)

DWG NO
Cyperss point

Rev
A00

Date: Monday, January 09, 2012 Sheet 17 of 59

CHANNEL B BANK 2
SMB ADDRESS:011



DELL INC.

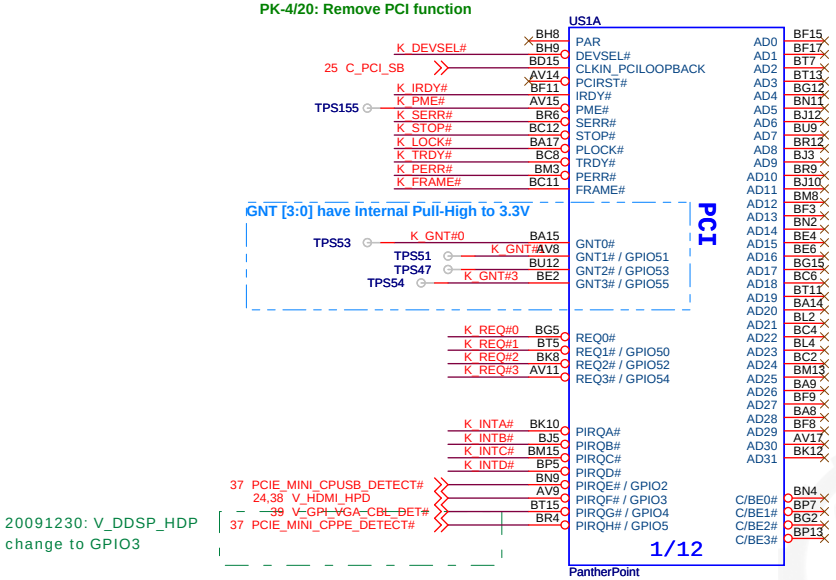
Title
DDR3 Conn: CHB_2 (DIMM2)

DWG NO
Cyperss point

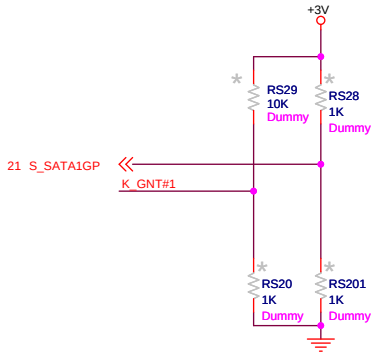
Rev
A00

Date: Monday, January 09, 2012 Sheet 18 of 59

PK-4/20: Remove PCI function

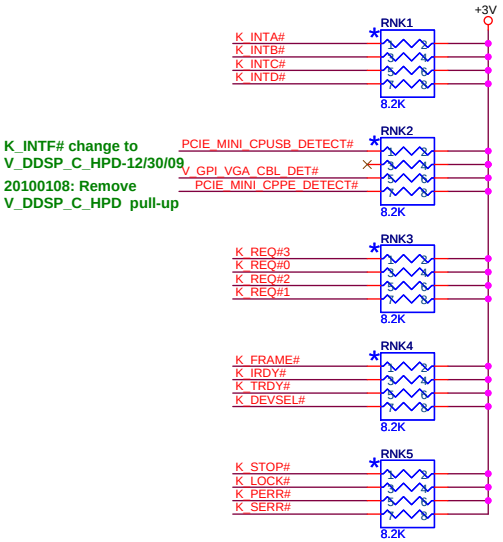


20091230: V_DDSP_HDP change to GPIO3



K_INTF# change to V_DDSP_C_HPD-12/30/09

20100108: Remove V_DDSP_C_HPD pull-up



DELL INC.

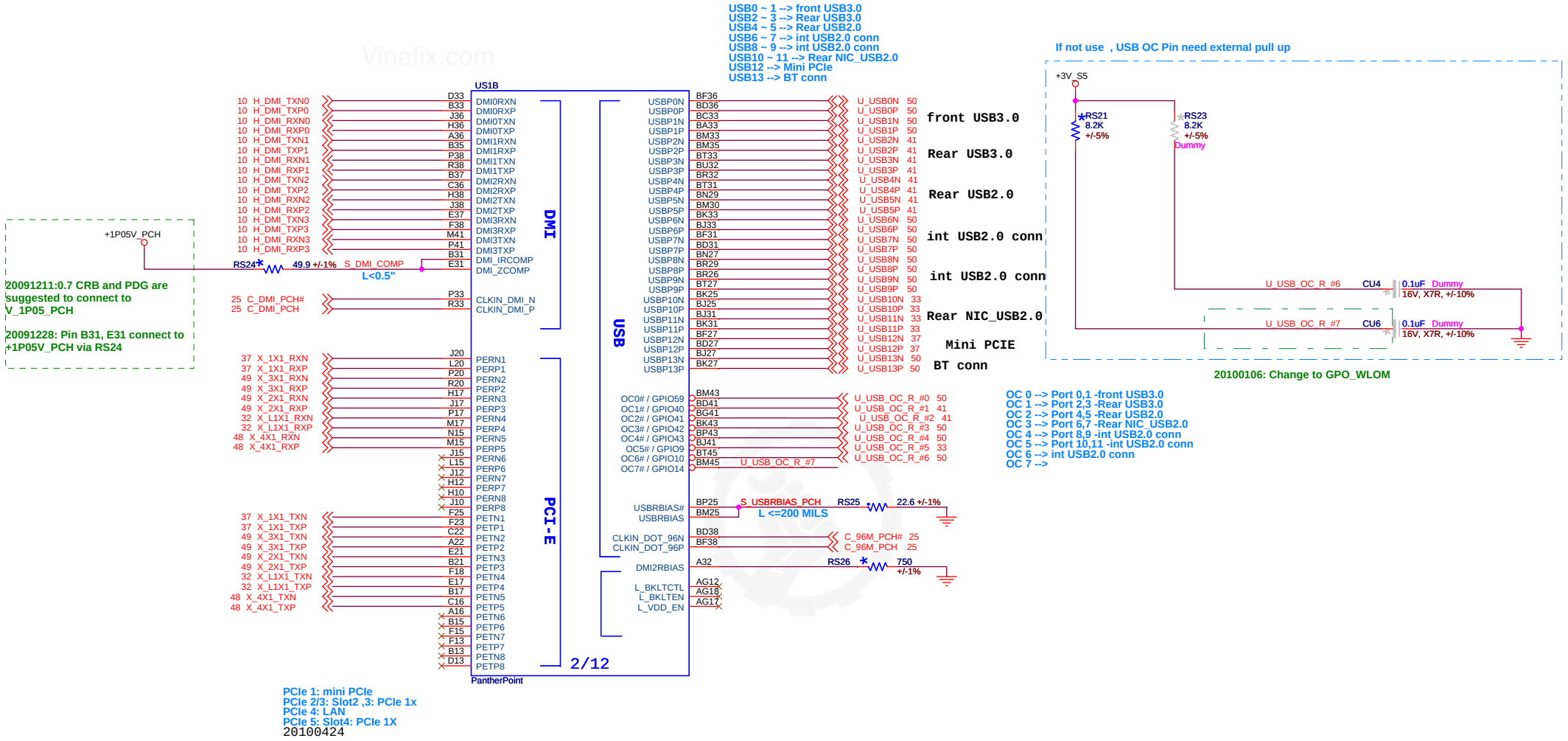
Title

PCH-1: PCI

DWG NO *Cyperss point*

Rev A00

Date: Friday, March 16, 2012 Sheet 19 of 59



DELL INC.

Title

PCH-2: DMI/PCIe/USB

DWG NO

Cyperss point

Rev A00

Date: Thursday, March 22, 2012 Sheet 20 of 59

Add CLINK to PCI-ex1; Follow CRB 0.7-12/03/09

20100107:Remove test points

20100105:Remove Test Point

20100107: Remove RS47, RS48 and connect S_PCH_MEPWROK_R to S_PCH_MEPWROK directly

20100104: Add TPS23,TPS25 and remove RS29,RS30,RS33, RS34 since useless this function

Add RS 144 and pull-up to +3V; CRB 0.7-12/07/09

FAN control from SMSC 5544 without using SST

20091221: RS35 stuffed for meet CRB0.7

20100107:Remove test points

Dummy RS39; SMSC suggestion-12/08/09

20100107: Remove RS47, RS48 and connect S_PCH_MEPWROK_R to S_PCH_MEPWROK directly

STUFF RS57 FOR ME ON CPU PRESENT DETECTION

PCH_CONFIG

US1C

CLINK

SATA

FAN

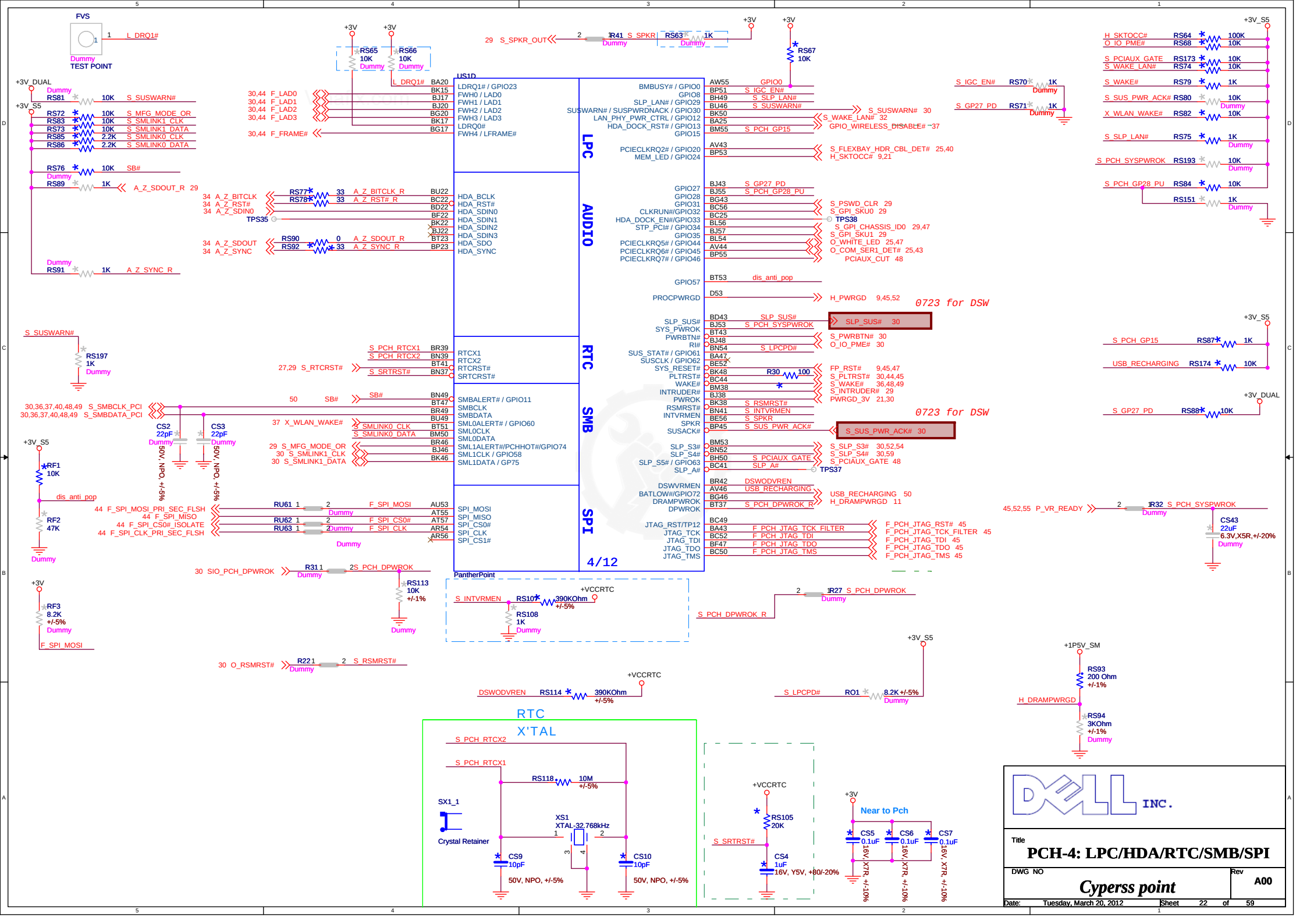
GPIO

HOST

3/12

PantherPoint

Title	PCH-3: SATA/HOST/FAN
DWG NO	Cyperss point
Rev	A00
Date:	Monday, January 09, 2012
Sheet	21 of 59


FVS
L_DRQ1#
Dummy
TEST POINT
+3V
+3V_S5
+3V_DUAL
US1D
LDRQ1# / GPIO23
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
LDRQ0#
FWH4 / LFRAME#
LPC
HDA_BCLK
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_SYNC
AUDIO
RTCX1
RTCX2
RTCRST#
SRTCRST#
RTC
SMBALERT# / GPIO11
SMBCLK
SMBDATA
SML0ALERT# / GPIO60
SML0CLK
SML0DATA
SML1ALERT#/PCHHOT#/GPIO74
SML1CLK / GPIO58
SML1DATA / GP75
SMB
SPI_MOSI
SPI_MISO
SPI_CS0#
SPI_CLK
SPI_CS1#
SPI
4/12
PantherPoint
BMBUSY# / GPIO0
GPIO8
SLP_LAN# / GPIO29
SUSWARN# / SUSPWRDNACK / GPIO30
LAN_PHY_PWR_CTRL / GPIO12
HDA_DOCK_RST# / GPIO13
GPIO15
PCIECLKRQ2# / GPIO20
MEM_LED / GPIO24
GPIO27
GPIO28
GPIO31
CLKRUN#/GPIO32
HDA_DOCK_EN#/GPIO33
STP_PCI# / GPIO34
GPIO35
PCIECLKRQ5# / GPIO44
PCIECLKRQ6# / GPIO45
PCIECLKRQ7# / GPIO46
GPIO57
PROCPWRGD
SLP_SUS#
SYS_PWROK
PWRBTN#
RI#
SUS_STAT# / GPIO61
SUSCLK / GPIO62
SYS_RESET#
PLTRST#
WAKE#
INTRUDER#
PWROK
RSMRST#
INTVRMEN
SPKR
SUSACK#
SLP_S3#
SLP_S4#
SLP_S5# / GPIO63
SLP_A#
DSWVRMEN
BATLOW#/GPIO72
DRAMPWROK
DPWROK
JTAG_RST/TP12
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
RTC X'TAL
Crystal Retainer
XS1
XTAL-32.768kHz
Near to Pch
Dell Inc.
Title
PCH-4: LPC/HDA/RTC/SMB/SPI
DWG NO
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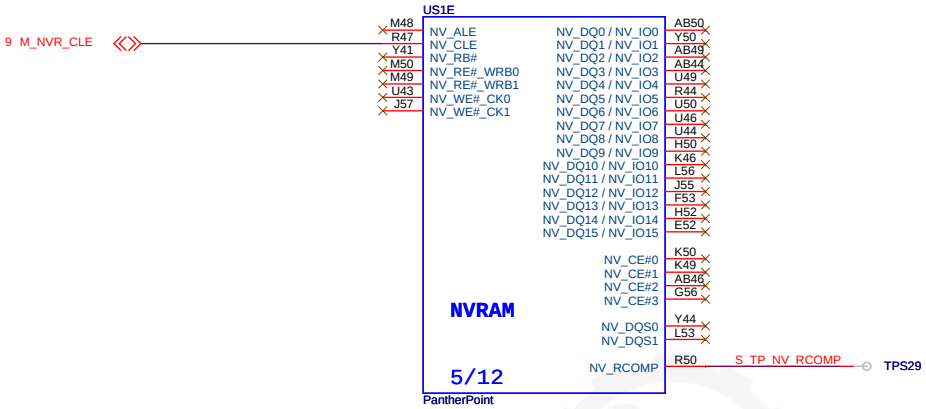
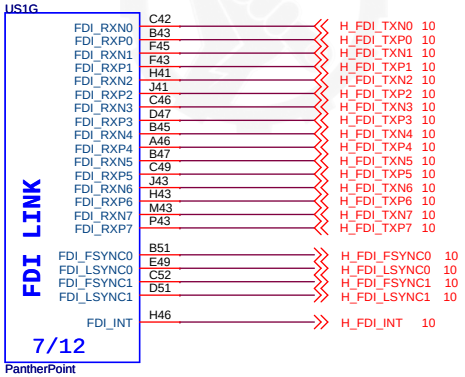
S_NVR_CLE internal pull-down.





DELL INC.

Title
PCH-5/7: NVRAM/FDI

DWG NO
Cyperss point

Rev
A00

Date: Monday, January 09, 2012 Sheet 23 of 59

20100108: Dummy RS128,RS129: CRB 0.7

20100107: Correct pin T1 and M1 net name to S_DDPB_HPD_PD and S_DDPD_HPD_PD

20100420: Del DVI

RS167 1K+/-1% Dummy
RS129 1K+/-1% Dummy
S_DDPD_HPC_PD
19,38 V_HDMI_HPD

US1F

T1 DDPB_HPD
N2 DDPC_HPD
M1 DDPD_HPD
R8 DDPB_AUXP
R9 DDPB_AUXN
U14 DDPC_AUXP
U12 DDPC_AUXN
N6 DDPD_AUXP
R6 DDPD_AUXN

CRT_HSYNC AR4 V_HSYNC
CRT_VSYNC AR2 V_VSYNC
CRT_RED AN6 V_RED 39
CRT_GREEN AN2 V_GREEN 39
CRT_BLUE AM1 V_BLUE 39
CRT_IRTN AM6
CRT_DDC_DATA AW1 V_DDCA_DATA 39
CRT_DDC_CLK AW3 V_DDCA_CLK 39
DAC_IREF AT3 V_DACREFSET RS130 1K +/-0.5%
L<500 MILS
NON-Graphic sku : Change to O ohm

20100420: Del DVI

TPS77 TP_DDPB_3P
TPS67 TP_DDPB_3N

R14 DDPB_0P
R12 DDPB_0N
M11 DDPB_1P
M12 DDPB_1N
H8 DDPB_2P
K8 DDPB_2N
L5 DDPB_3P
M3 DDPB_3N
L2 DDPB_3N
J3 DDPC_0P
G2 DDPC_0N
G4 DDPC_1P
F3 DDPC_1N
F5 DDPC_2P
E4 DDPC_2N
E2 DDPC_3P
D5 DDPC_3N
B5 DDPD_0P
C6 DDPD_0N
D7 DDPD_1P
B7 DDPD_1N
C9 DDPD_2P
E11 DDPD_2N
B11 DDPD_3P
DDPD_3N

PORT C : Display port

38 V_DDSP_C_HDMI_0_DP
38 V_DDSP_C_HDMI_0_DN
38 V_DDSP_C_HDMI_1_DP
38 V_DDSP_C_HDMI_1_DN
38 V_DDSP_C_HDMI_2_DP
38 V_DDSP_C_HDMI_2_DN
38 V_DDSP_C_HDMI_3_DP
38 V_DDSP_C_HDMI_3_DN

DISPLAY

DDPC_CTRLCLK AL12
DDPC_CTRLDATA AL14
DDPD_CTRLCLK AL9 V_DDP_HDMI_CTRL_CLK 38
DDPD_CTRLDATA AL8 V_DDP_HDMI_CTRL_DATA 38
SDVO_CTRLCLK AL15
SDVO_CTRLDATA AL17

U2 SDVO_INTP
T3 SDVO_INTN
W3 SDVO_STALLP
U5 SDVO_STALLN
U8 SDVO_TVCLKINP
U9 SDVO_TVCLKINN

6/12
PantherPoint

V_RED
V_GREEN
V_BLUE
RS133 150 +/ -1%
RS134 150 +/ -1%
RS135 150 +/ -1%
CLOSE TO PCH: L<250 MILS

NON-Graphic sku : Change to O ohm
V_HSYNC SR110 33 V_HSYNC_3V 39
V_VSYNC SR111 33 V_VSYNC_3V 39
L<750 MILS
NON-Graphic sku : Stuff O ohm

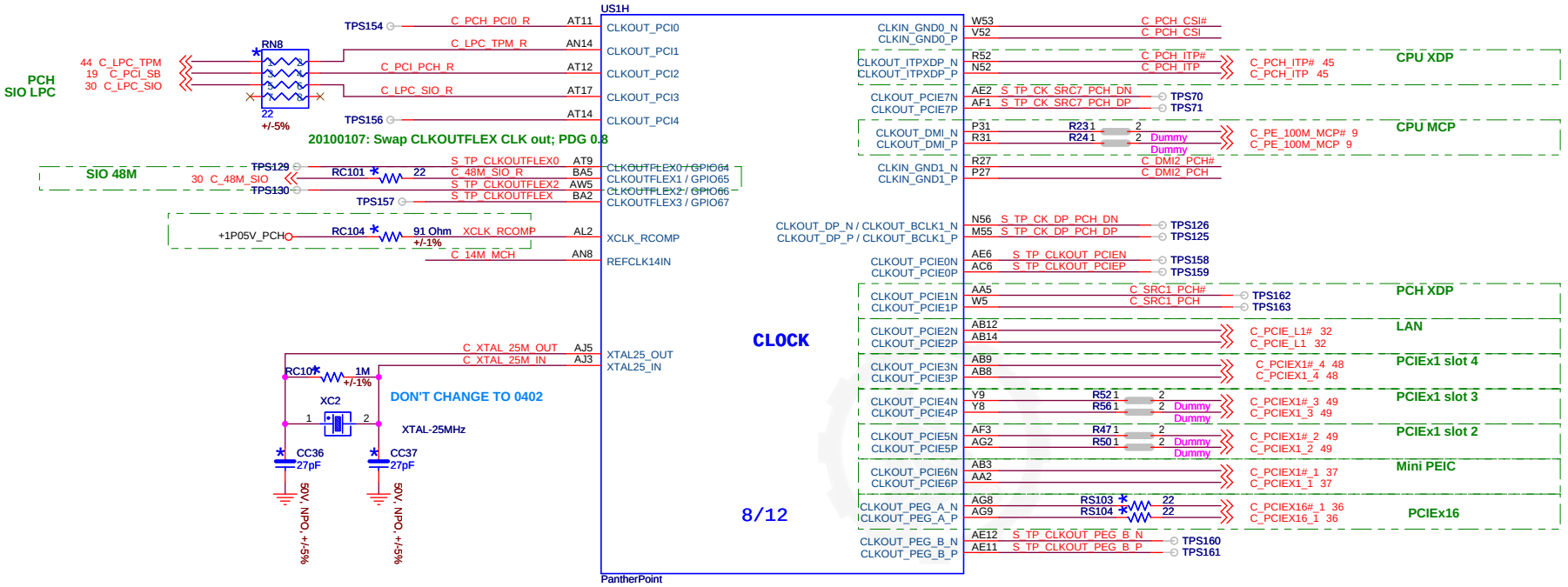
DELL INC.

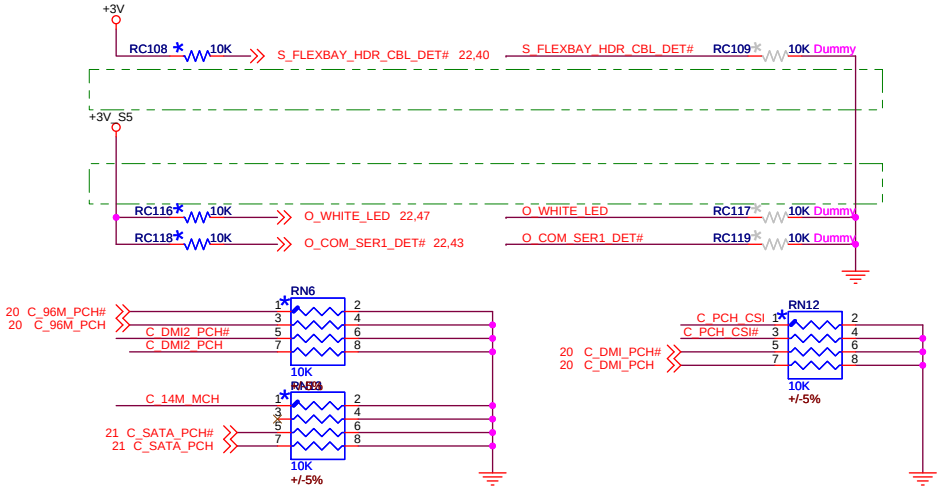
Title
PCH-6: Display

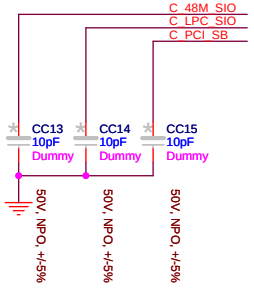
DWG NO
Cyperss point

Rev
A00

Date: Monday, January 09, 2012 Sheet 24 of 59







DELL INC.

Title

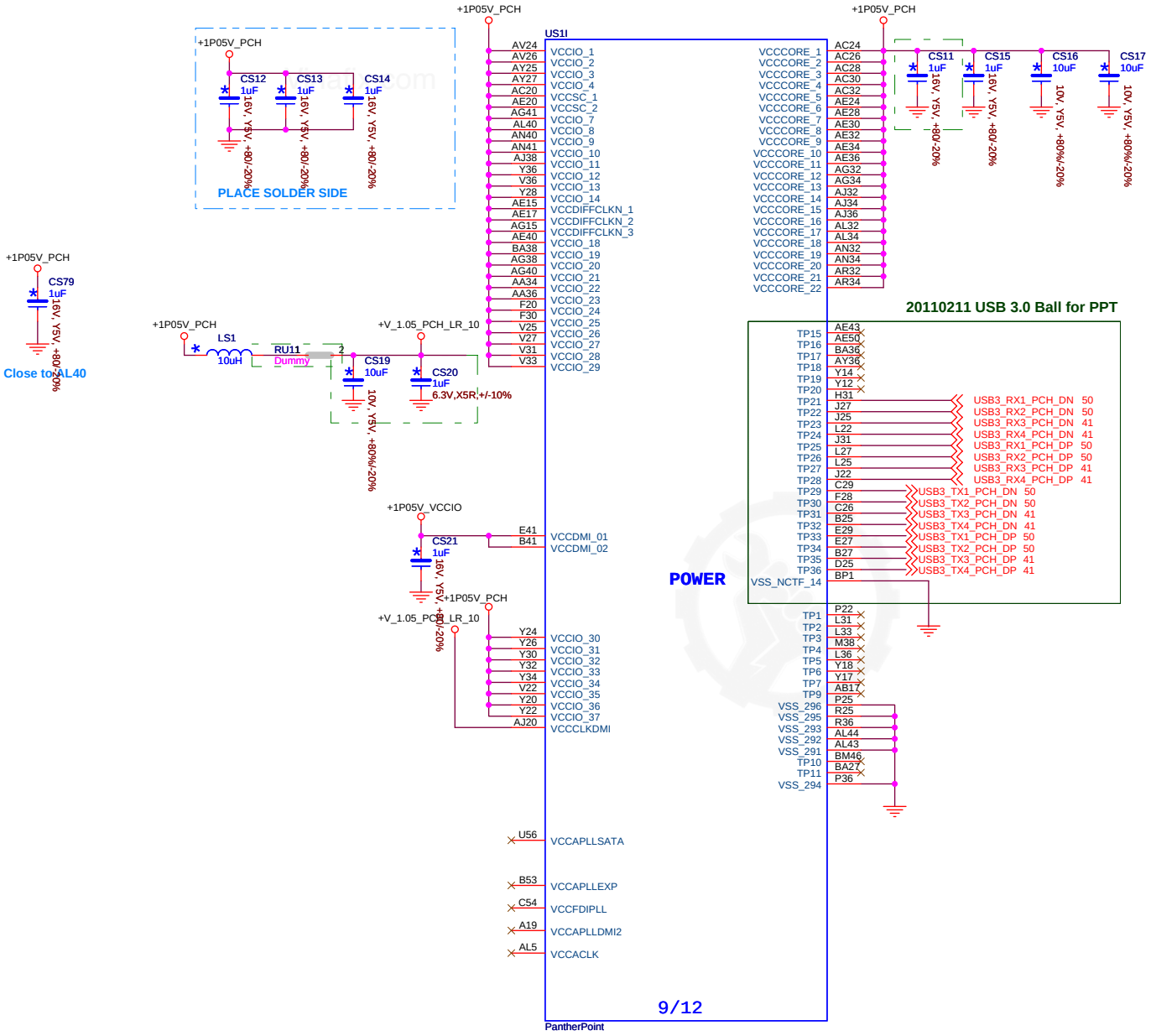
PCH-8: Clock

DWG NO

Cyperss point

Rev A00

Date: Thursday, March 22, 2012 Sheet 25 of 59



USB 3.0 Ball for PPT	
J34	USB3Tp4
B27	USB3Tp3
E27	USB3Tp2
E29	USB3Tp1
B25	USB3Tn4
C26	USB3Tn3
F28	USB3Tn2
C29	USB3Tn1
J22	USB3Rp4
L25	USB3Rp3
L27	USB3Rp2
J31	USB3Rp1
L22	USB3Rn4
J25	USB3Rn3
J27	USB3Rn2
H31	USB3Rn1

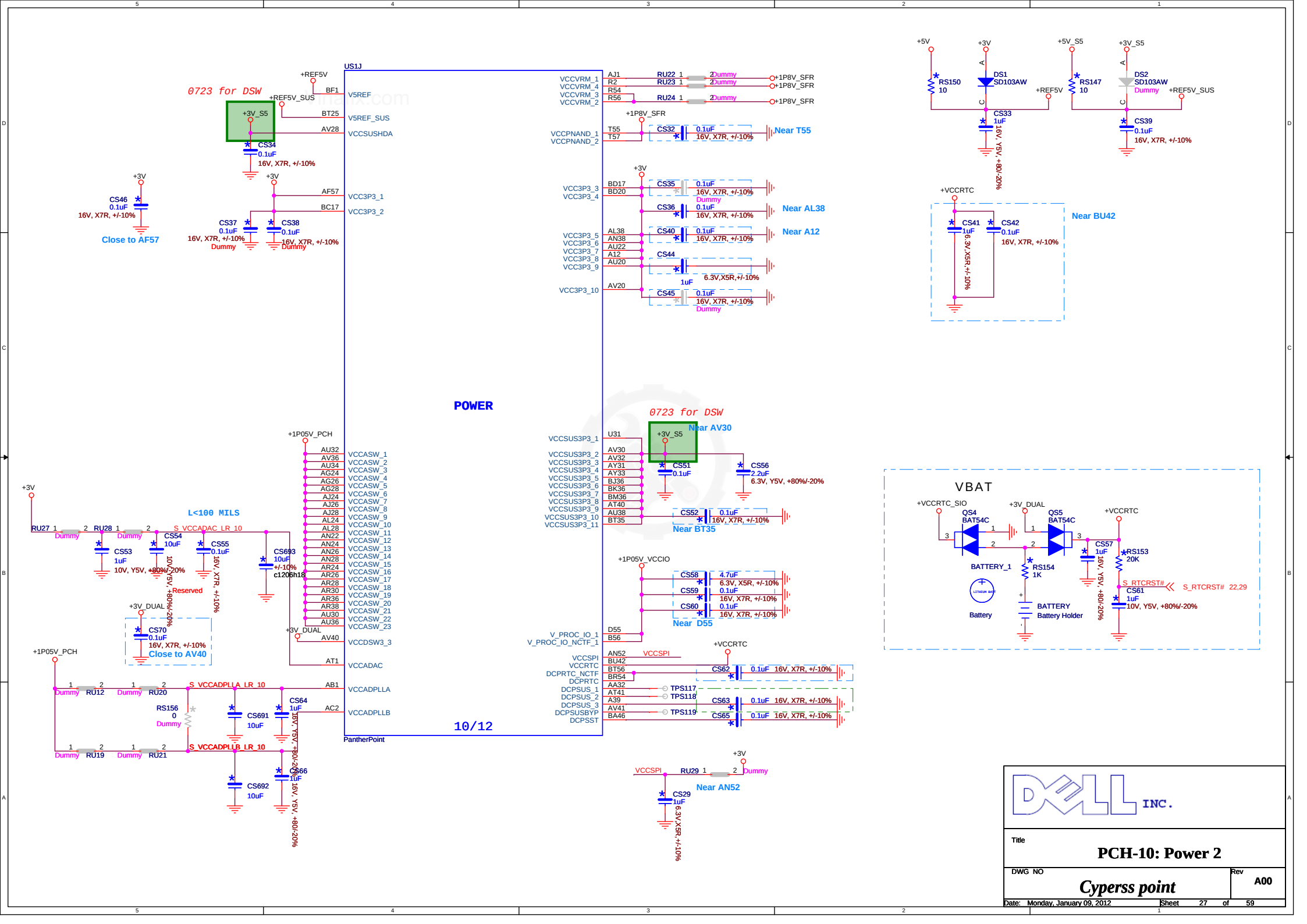
DELL INC.

Title: **PCH-9: Power 1**

DWG NO: *Cyperss point*

Rev: A00

Date: Monday, January 09, 2012 Sheet 26 of 59


POWER
US1J
PantherPoint
10/12
0723 for DSW
Near AV30
Near T55
Near AL38
Near A12
Near BU42
Near BT35
Near D55
Near AN52
Close to AF57
Close to AV40
L<100 MILS
VBAT
Battery
BATTERY
Battery Holder
Cypress point
PCH-10: Power 2
DELL INC.
DWG NO
Rev
A00
Date: Monday, January 09, 2012
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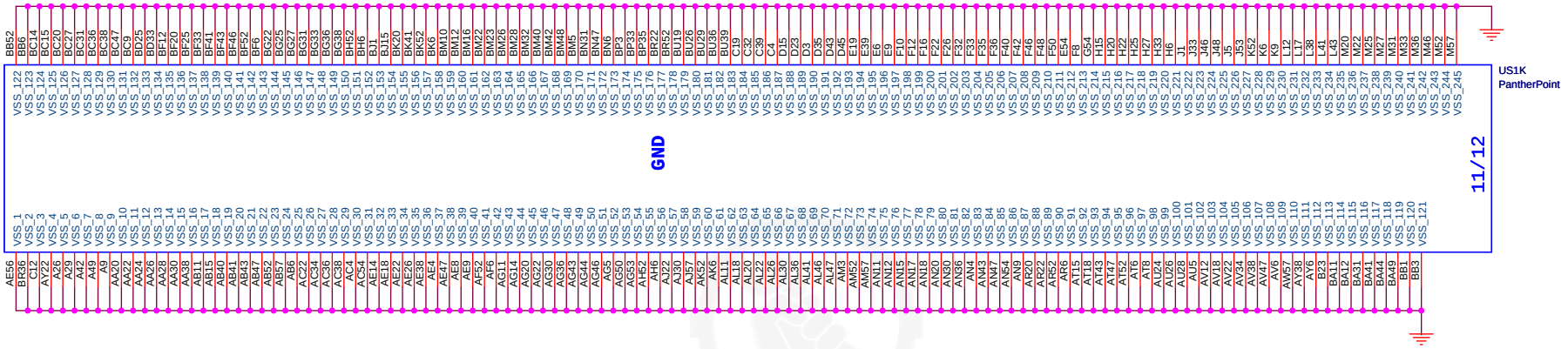
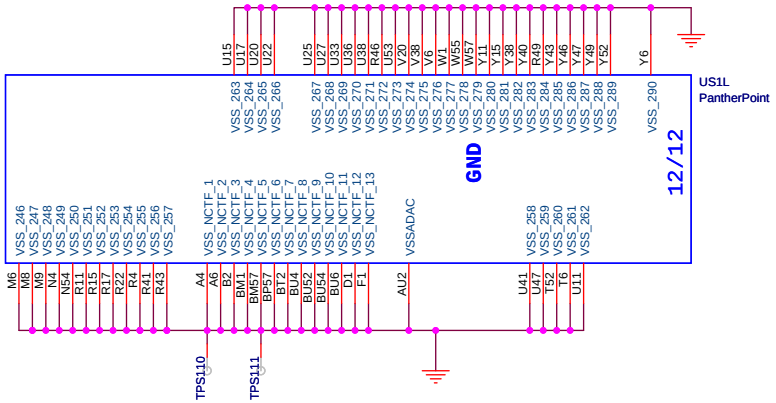
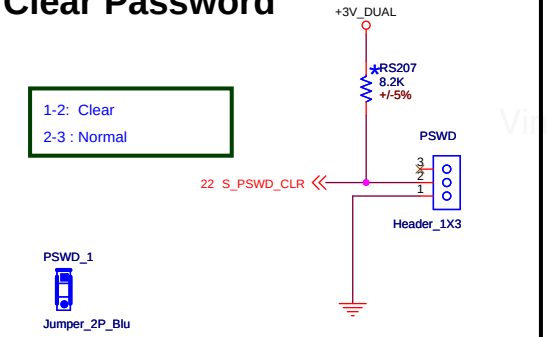


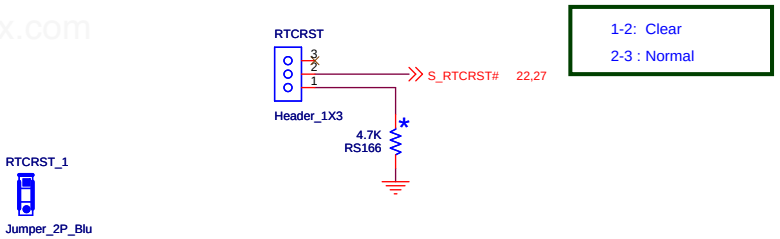


Title	**PCH-11: GND**
DWG NO	*Cyperss point*
Rev	A00
Date: Monday, January 09, 2012	Sheet 28 of 59

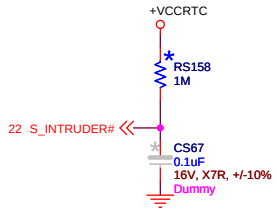
Clear Password



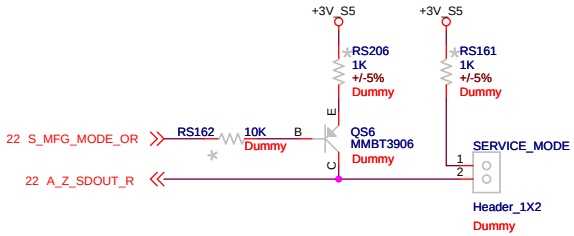
CLR_CMOS



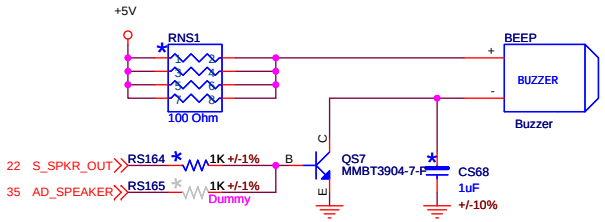
Chassis Intruder



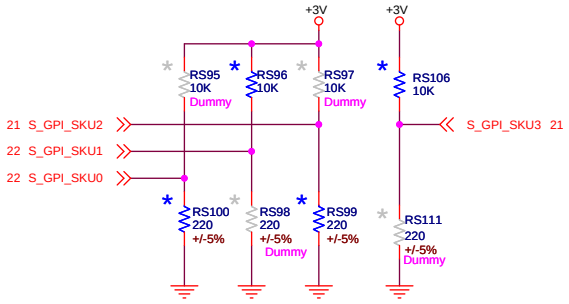
SERVICE_MODE



BEEP



SKU ID



SKU ID

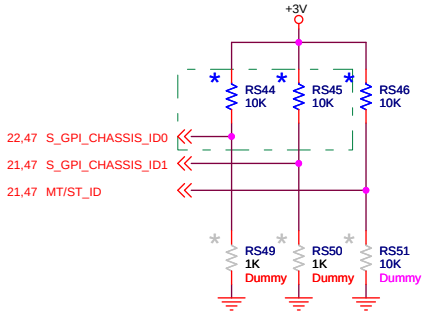
SKU1	SKU0	Type
0	0	Reserved
0	1	Reserved
1	0	Reserved
1	1	Reserved

Chassis ID

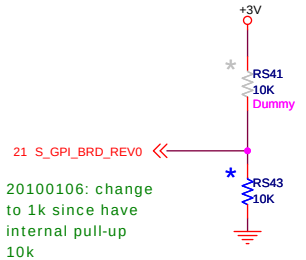
Chassis ID1	Chassis ID0	MT/ST ID	Description
L	L	L	Reserved
L	L	H	Reserved
L	H	L	Cosumer MT
L	H	H	Cosumer ST
H	L	L	SMB MT
H	L	H	SMB ST
H	H	L	reserved
H	H	H	CBL detect

Turnberry

Riviera



BOARD ID



20100106: change to 1k since have internal pull-up 10k

Rev0	Type
0	Default
1	Reserved
0	Reserved
1	Reserved

DELL INC.

Title

PCH MISC Conn/BUZ/ID

DWG NO

Cyperss point

Rev A00

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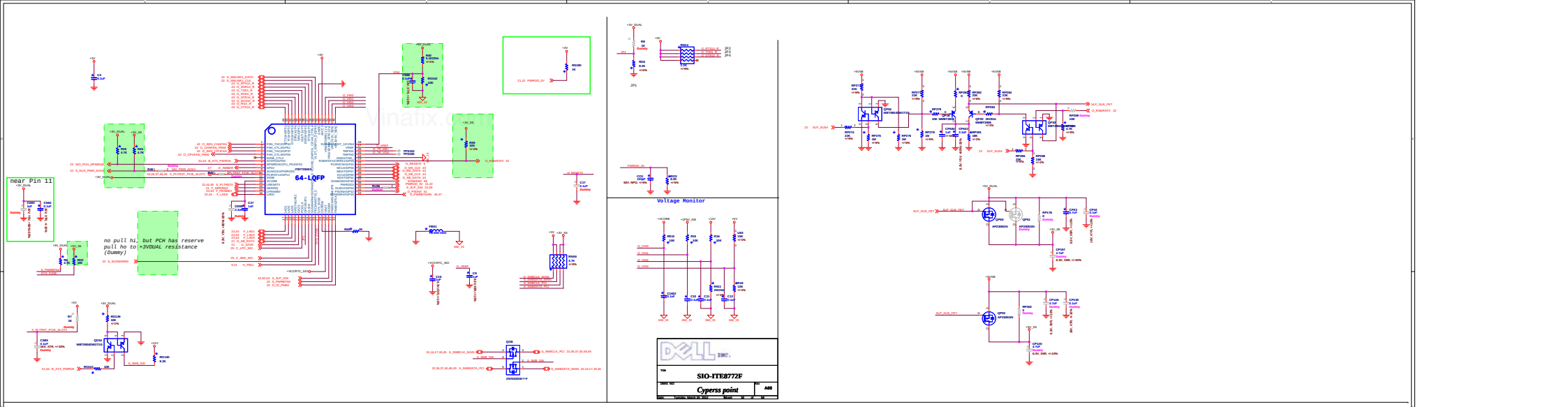
near Pin 11
64-LQFP
no pull hi, but PCH has reserve
pull ho to +3VDUAL resistance
(Dummy)
Voltage Monitor
SIO-ITE8772F
Cypress point

IT8772 Power On Strapping Options

Symbol		value	Description
JP4 Pin 61	K8PWR_EN	1	Disable K8 power sequence function
		0	Enable K8 power sequence function
JP3 & JP5 Pin 59 & 21	FAN_CTL_SEL	11	The default value of EC Index 63h/6Bh/73h is 80h
		10	The default value of EC Index 63h/6Bh/73h is FFh
		01	The default value of EC Index 63h/6Bh/73h is 00h
		00	The default value of EC Index 63h/6Bh/73h is 40h

DELL INC.

Title: SIO-ITE8772F (MISC)

DWG NO: Cyperss point

Rev: A00

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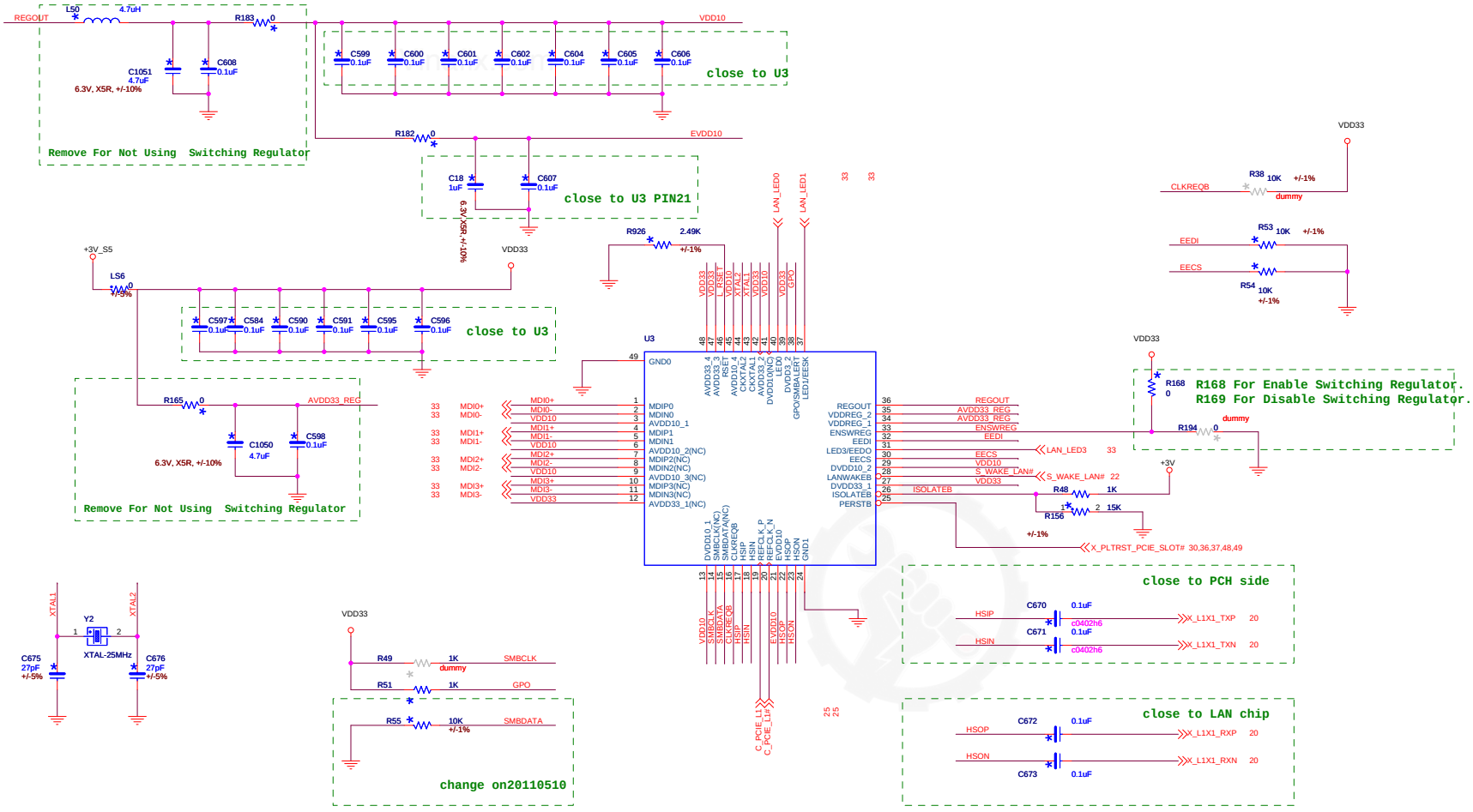
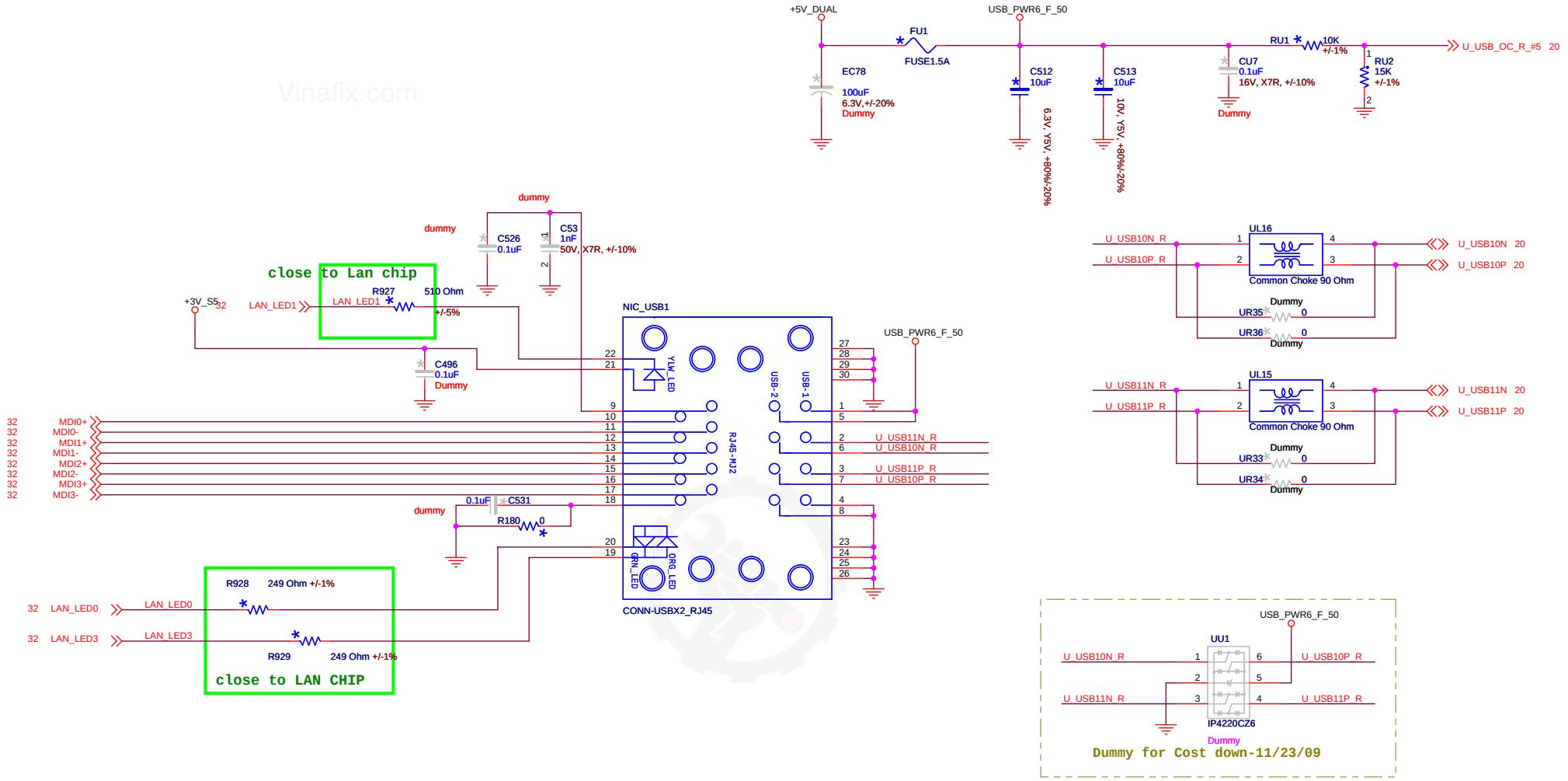


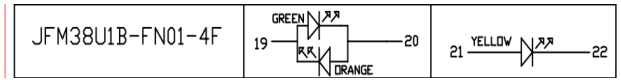
FOXCONN®

FOXCONN PCEG

Title	BCM57788		
Size	Document Number	Cyperss point	Rev A00
Date: Wednesday, March 21, 2012	Sheet 32 of 59		



SPEED LED	
LINK 10M	GREEN
LINK 100M	
LINK 1000M	ORANGE



ACTIVE LED

YELLOW = LINK UP
BLINKING = TX/RX ACTIVITY

When implementing customized LEDs:

Configure IO register offset 18h~19h to support your own LED signals. For example, if the value in the IO offset 0x18 is 0x0CA9h (0000110010101001b), the LED actions are:

- LED 0: On only in 10M mode, with blinking during TX/RX
- LED 1: On only in 100M mode, with blinking during TX/RX
- LED 3: On only in 1000M mode, with blinking during TX/RX

DELL INC.

Title: **LAN Power & LAN/USB Conn**

DWG NO: *Cyperss point*

Rev: A00

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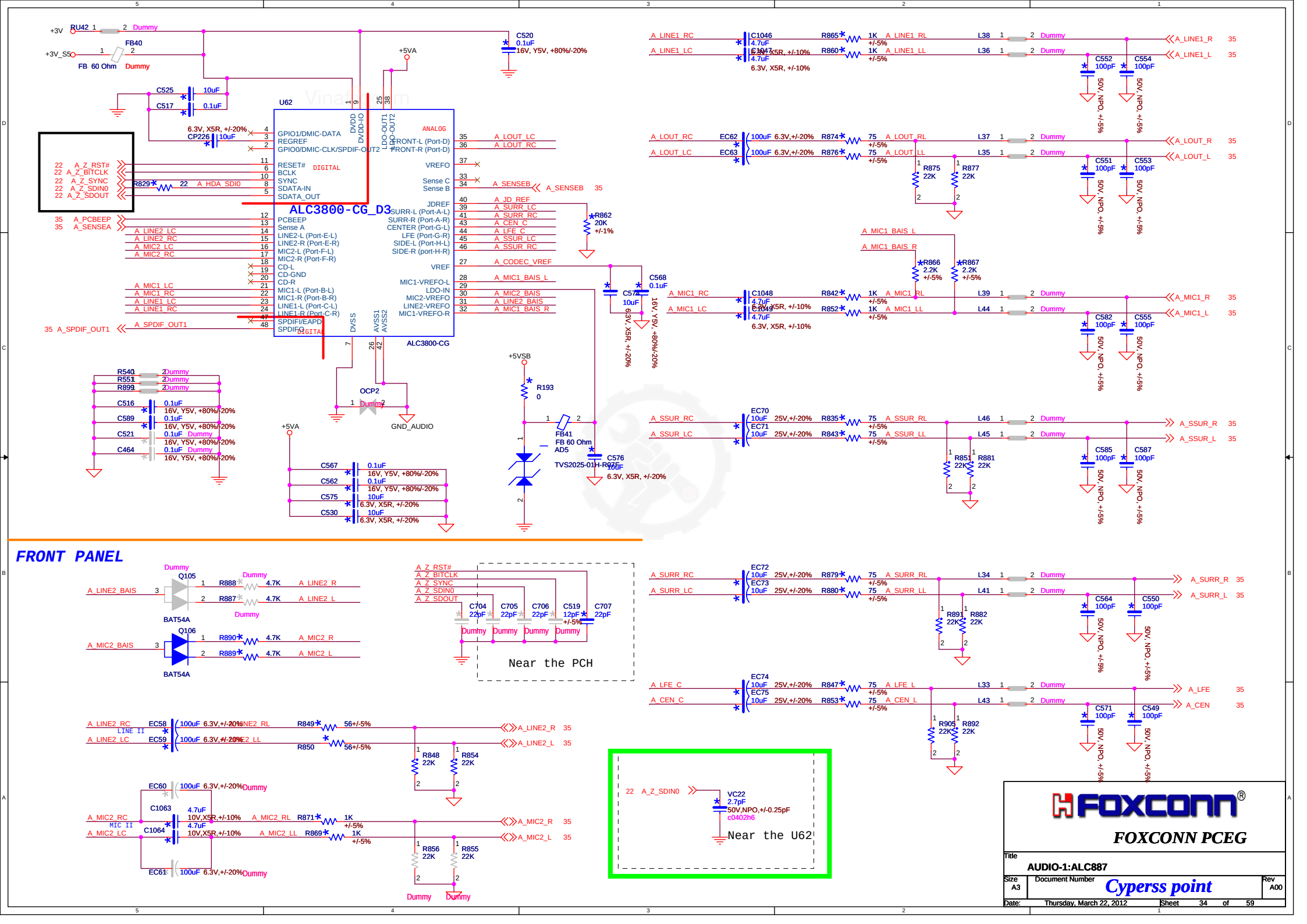
ALC3800-CG_D3
ALC3800-CG
FRONT PANEL
Near the PCH
Near the U62
FOXCONN PCEG
AUDIO-1:ALC887
Cyperss point
Thursday, March 22, 2012
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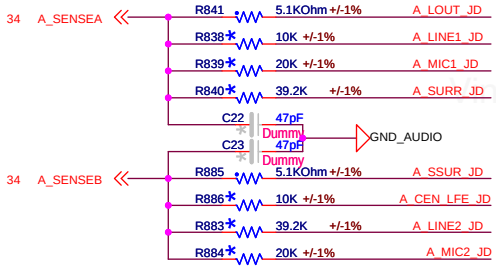
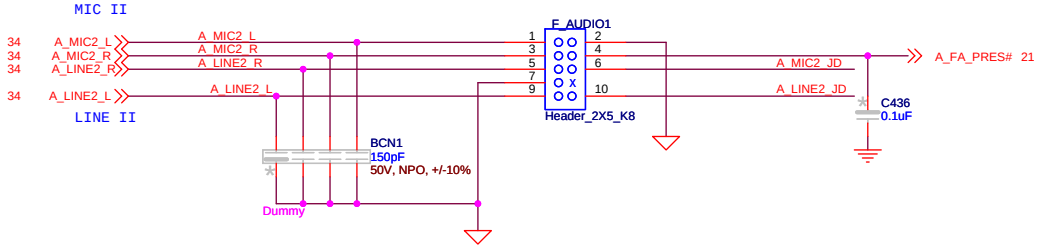
JACK SENSE



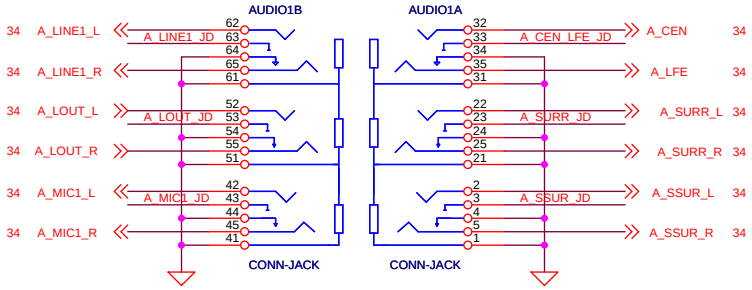
Front_Audio



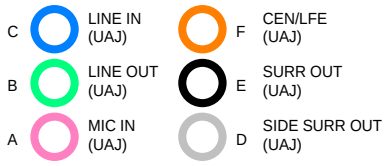
+5VA for AUDIO

SPDIF OUT Header

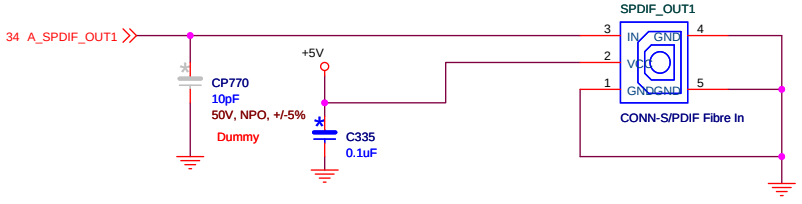
Audio Jack



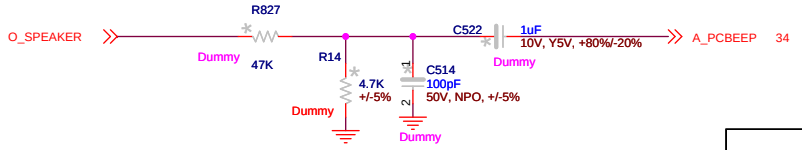
Audio Jack



SPDIF OUT



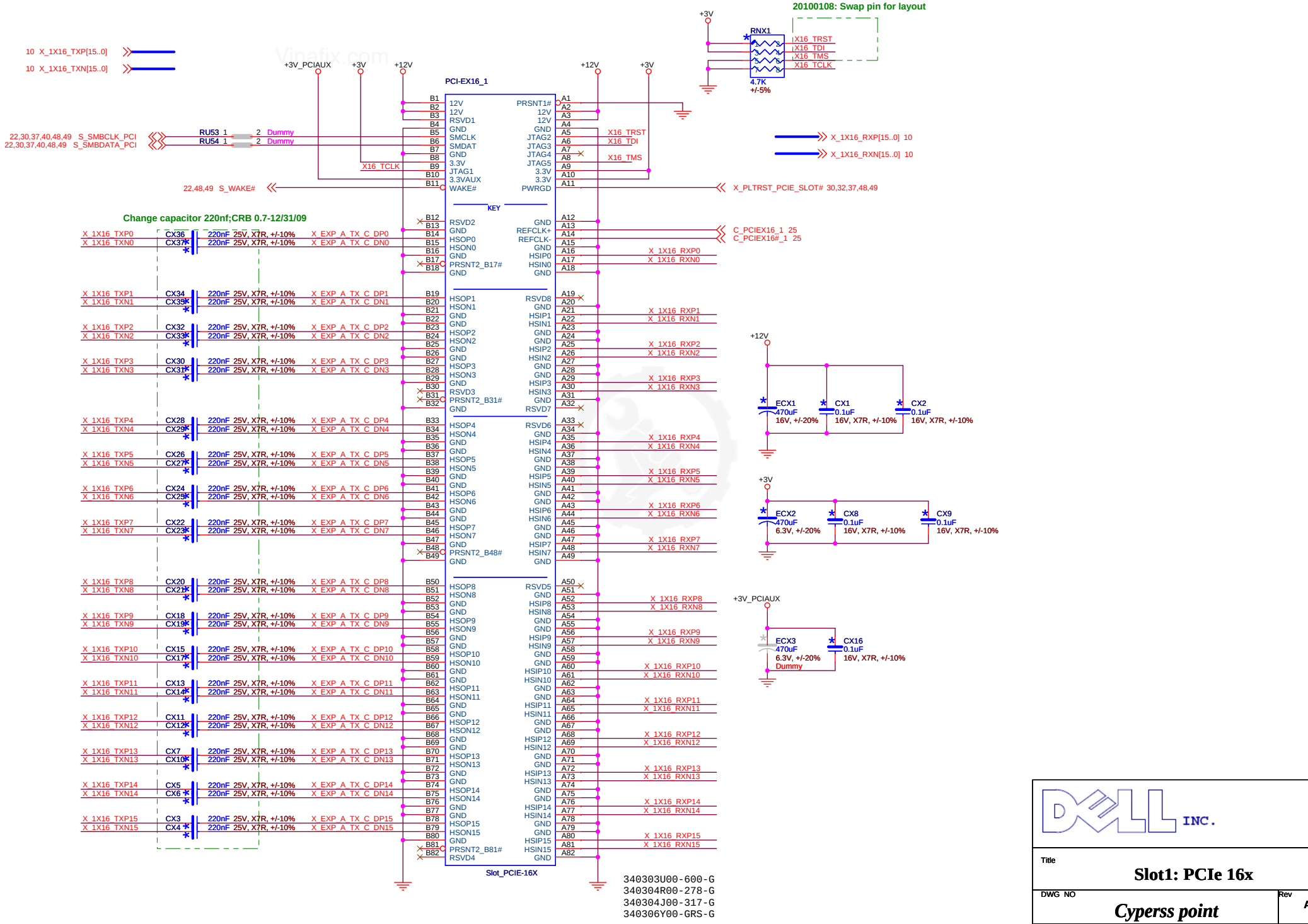
PC BEEP



FOXCONN®

FOXCONN PCEG

Title: AUDIO-2:CONNECTOR		
Size: A3	Document Number: Cyperss point	Rev: A00
Date: Thursday, March 22, 2012	Sheet 35 of 59	



DELL INC.

Title

Slot1: PCIe 16x

DWG NO

Cyperss point

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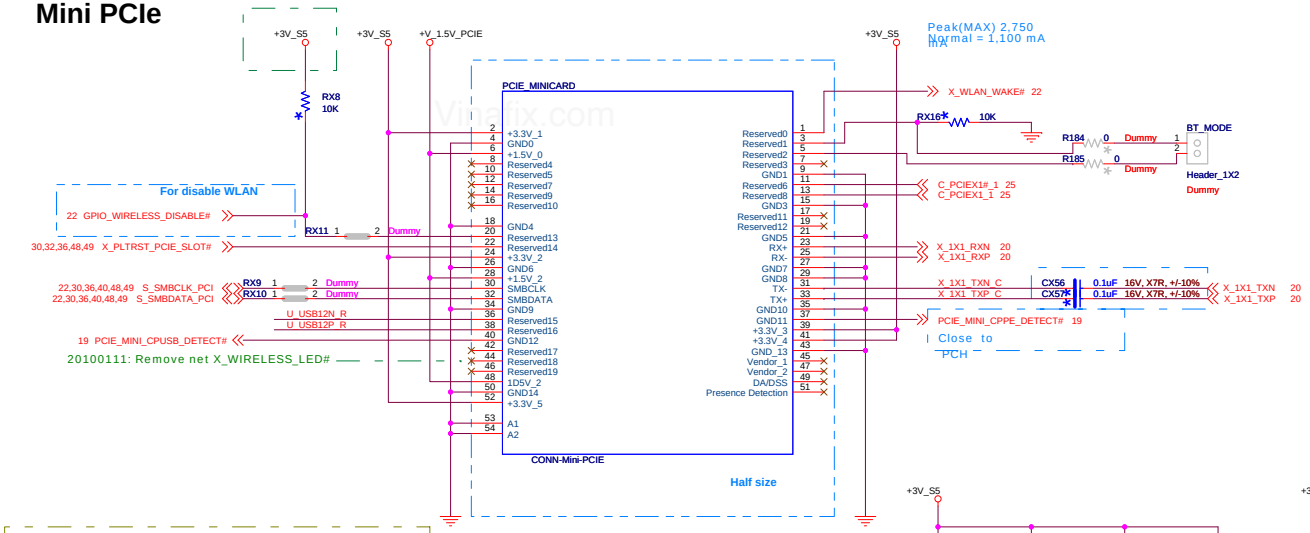
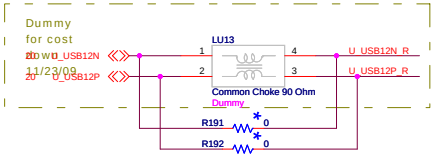
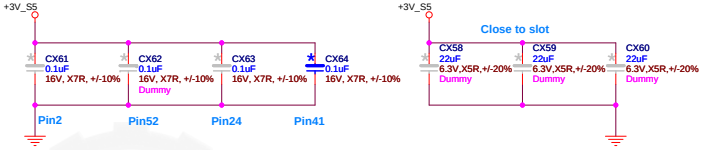
Mini PCIe

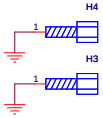


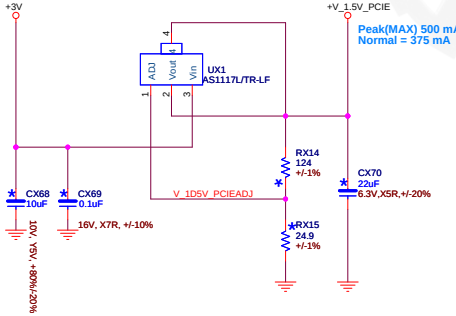


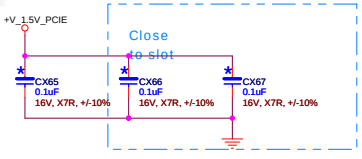


Latch

+V_1.5V_PCIE







DELL INC.

Title: **Mini PCIe**

DWG NO: ***Cyperss point***

Rev: **A00**

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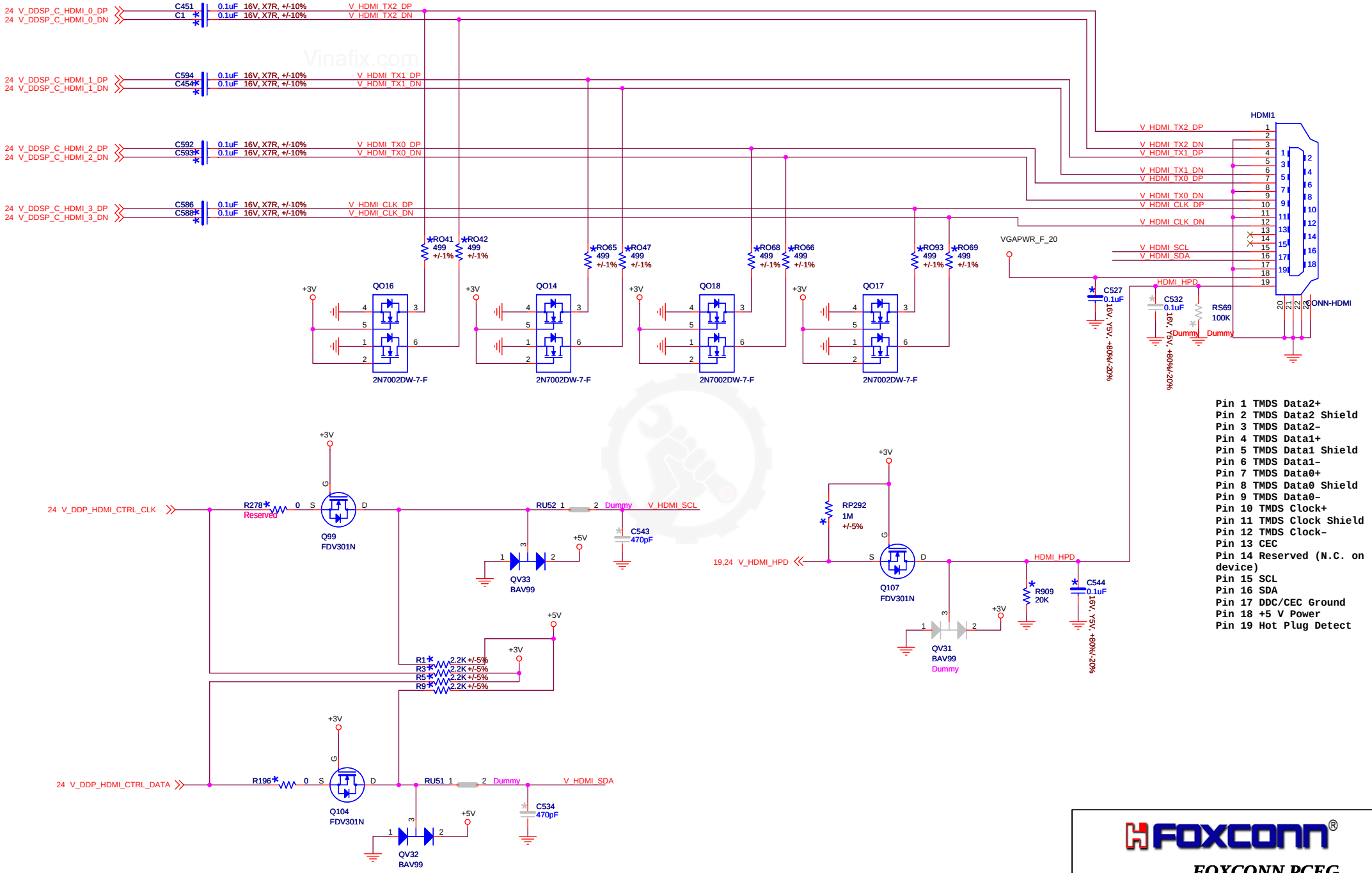
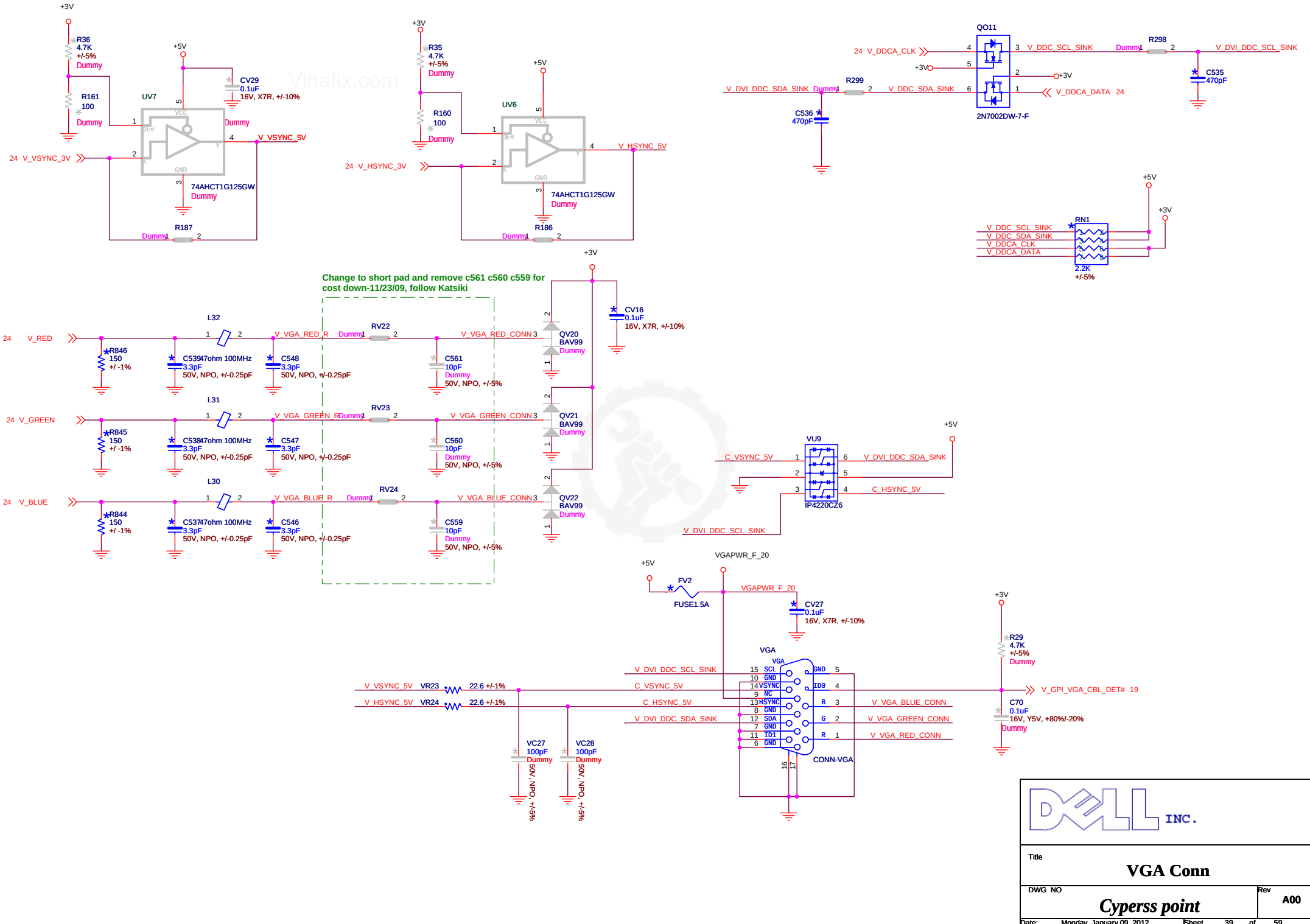


FOXCONN®

FOXCONN PCEG

Title	HDMI	
Size A3	Document Number Cyperss point	Rev A00
Date: Monday, January 09, 2012	Sheet 38 of 59	


+3V
R36
4.7K
+/-5%
Dummy
R161
100
Dummy
UV7
+5V
CV29
0.1uF
16V, X7R, +/-10%
Dummy
V_VSYNC_5V
24 V_VSYNC_3V
74AHCT1G125GW
Dummy
R187
R35
4.7K
+/-5%
Dummy
R160
100
Dummy
UV6
V_HSYNC_5V
24 V_HSYNC_3V
74AHCT1G125GW
Dummy
R186
QO11
24 V_DDCA_CLK
V_DDC_SCL_SINK
R298
V_DVI_DDC_SCL_SINK
C535
470pF
+3V
V_DDCA_DATA 24
V_DVI_DDC_SDA_SINK
R299
V_DDC_SDA_SINK
C536
470pF
2N7002DW-7-F
RN1
V_DDC_SCL_SINK
V_DDC_SDA_SINK
V_DDCA_CLK
V_DDCA_DATA
2.2K
+/-5%
Change to short pad and remove c561 c560 c559 for
cost down-11/23/09, follow Katsiki
L32
L31
L30
24 V_RED
24 V_GREEN
24 V_BLUE
R846
R845
R844
150
+/ -1%
C539 47ohm 100MHz
C538 47ohm 100MHz
C537 47ohm 100MHz
C548
C547
C546
3.3pF
50V, NPO, +/-0.25pF
C561
C560
C559
10pF
Dummy
50V, NPO, +/-5%
RV22
RV23
RV24
V_VGA_RED_R
V_VGA_GREEN_R
V_VGA_BLUE_R
V_VGA_RED_CONN
V_VGA_GREEN_CONN
V_VGA_BLUE_CONN
QV20
QV21
QV22
BAV99
Dummy
CV16
0.1uF
16V, X7R, +/-10%
VU9
IP4220CZ6
C_VSYNC_5V
C_HSYNC_5V
V_DVI_DDC_SDA_SINK
V_DVI_DDC_SCL_SINK
FV2
FUSE1.5A
VGAPWR_F_20
CV27
0.1uF
16V, X7R, +/-10%
VGA
VR23
VR24
22.6 +/-1%
VC27
VC28
100pF
Dummy
50V, NPO, +/-5%
CONN-VGA
R29
4.7K
+/-5%
Dummy
V_GPI_VGA_CBL_DET# 19
C70
0.1uF
16V, Y5V, +80%/-20%
Dummy
DELL INC.
Title
VGA Conn
DWG NO
Cyperss point
Rev
A00
Date: Monday, January 09, 2012
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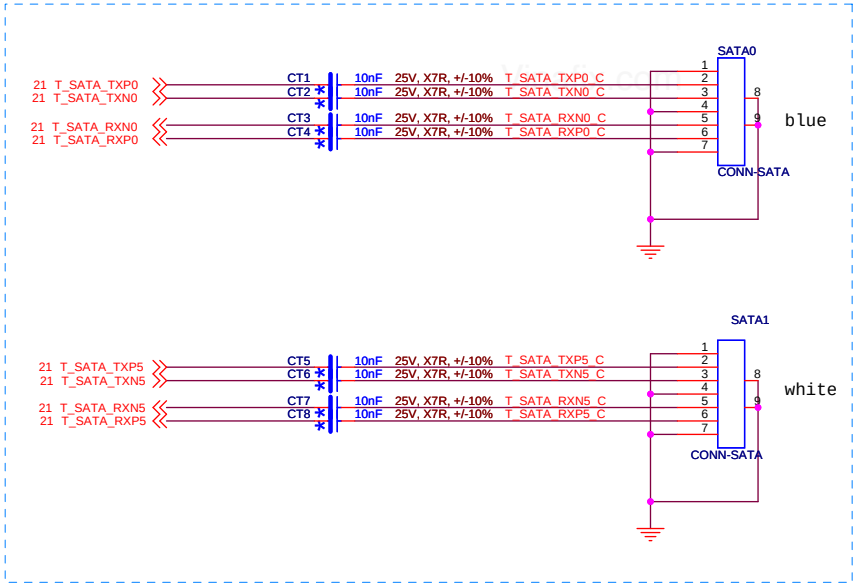
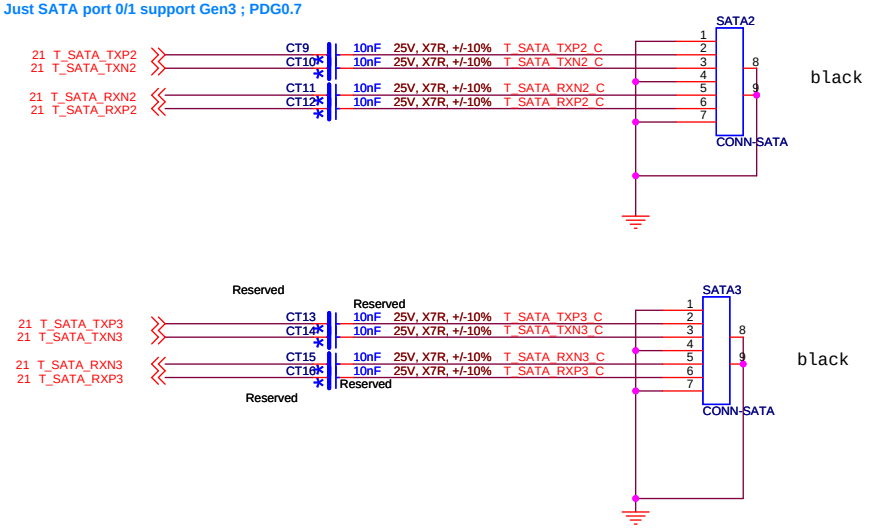
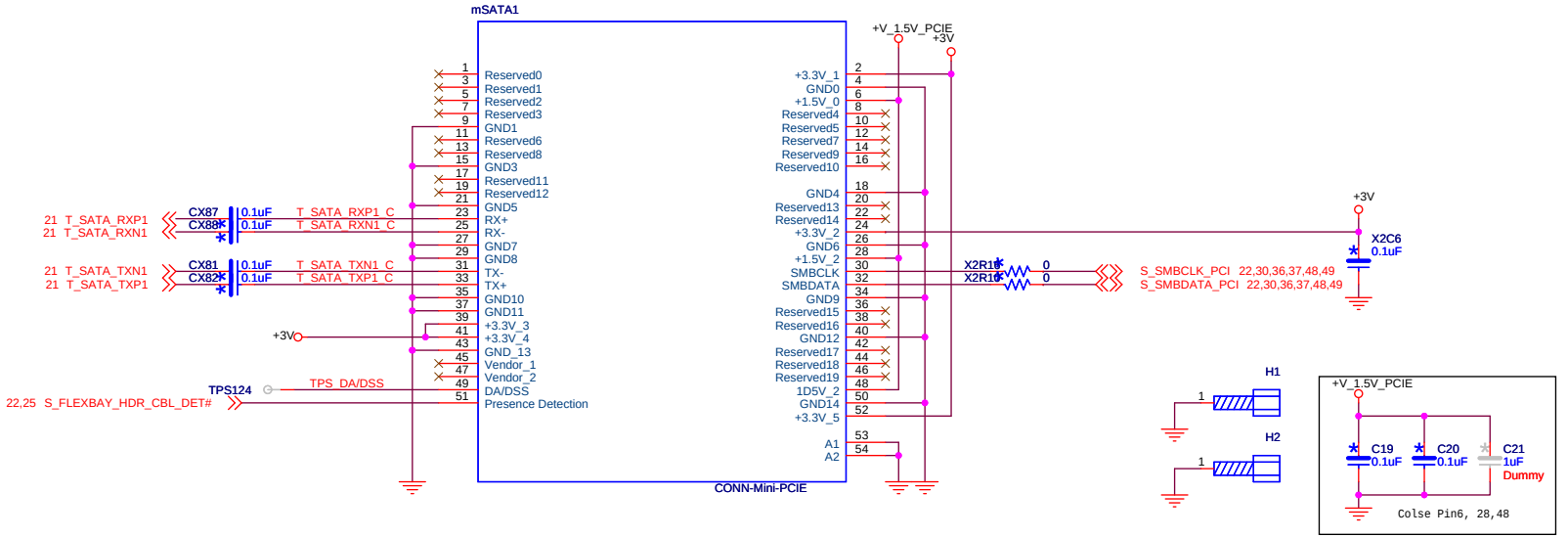
SATA x 4



Just SATA port 0/1 support Gen3 ; PDG0.7





DELL INC.

Title: **SATA Conn**

DWG NO: *Cyperss point*

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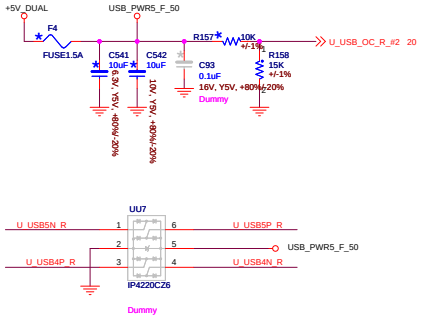
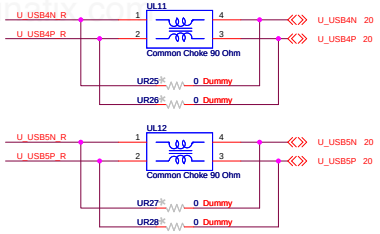
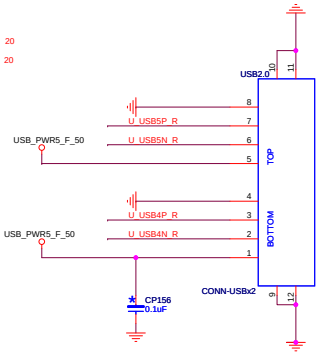
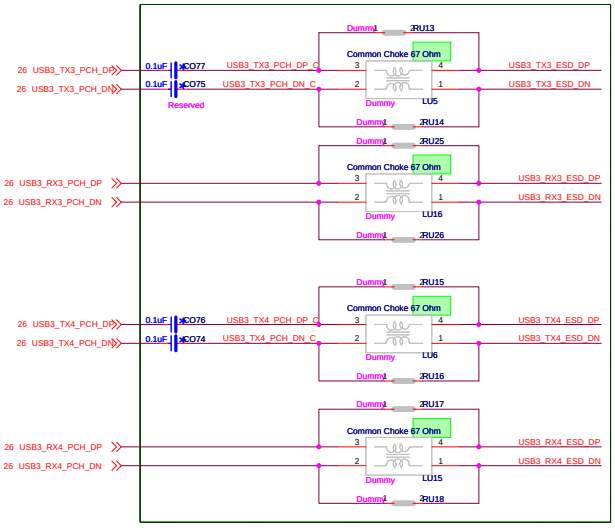
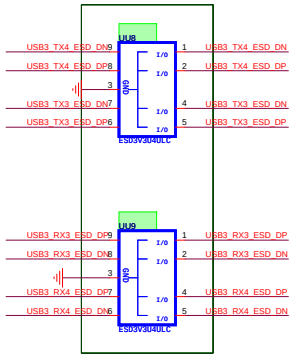
Rear USB3.0

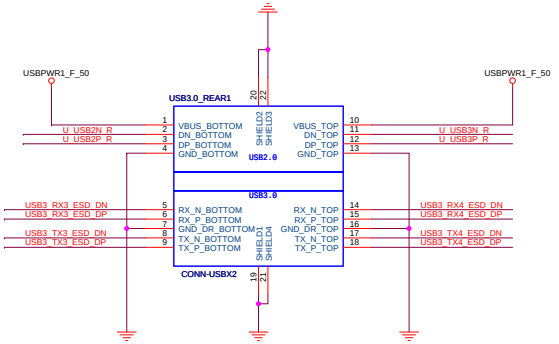




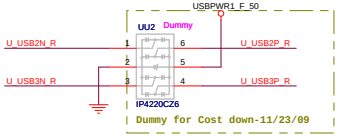


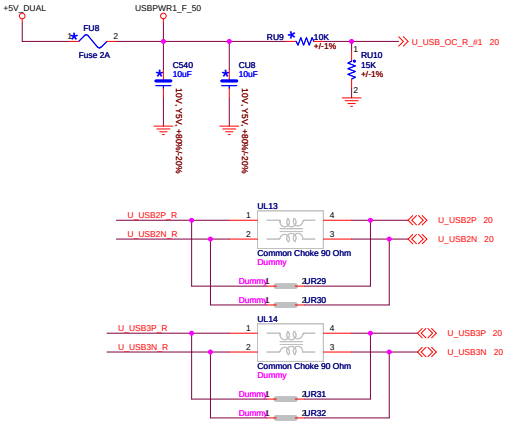






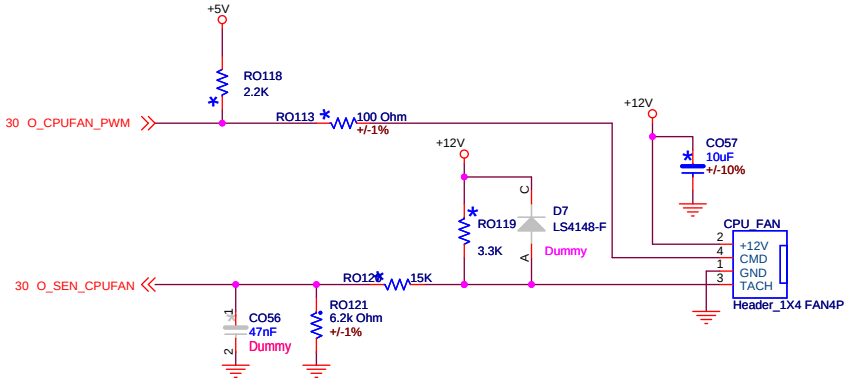
Follow Little Sur USB3.0
Jock 0818

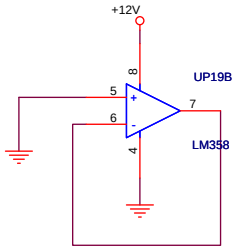




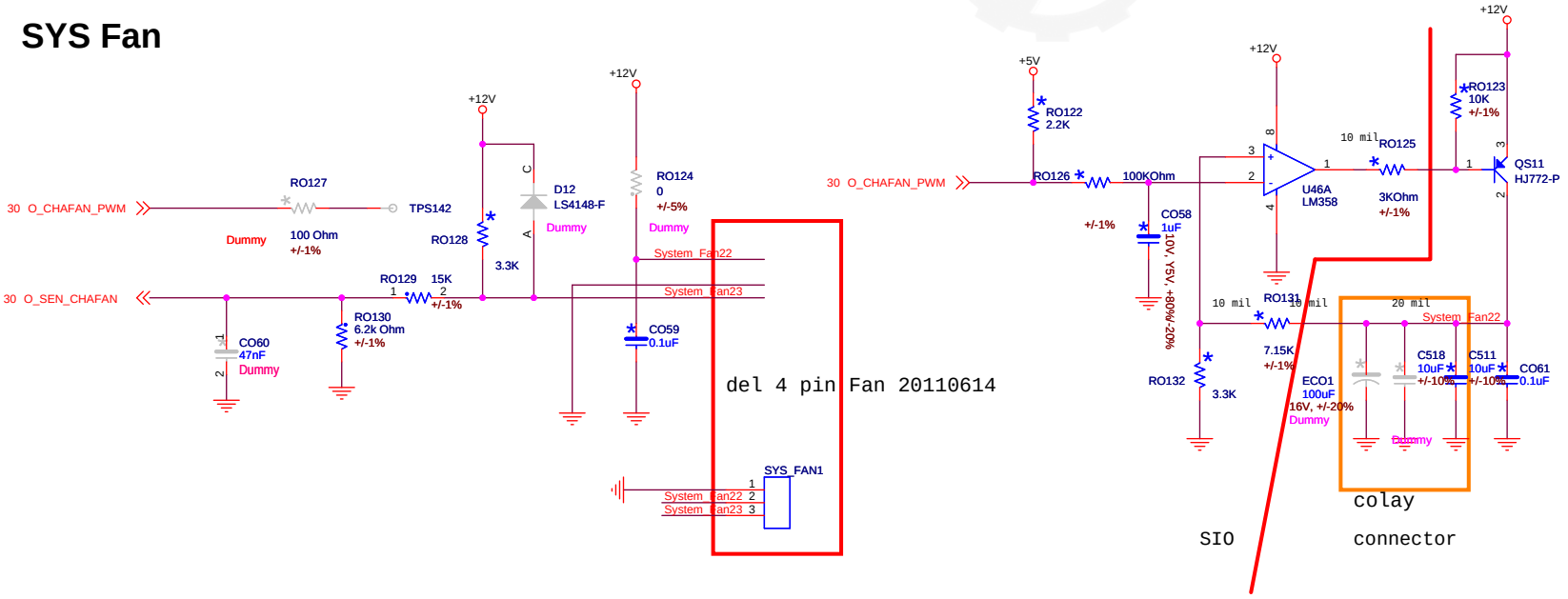
DELL INC.	
Title	eSATA Conn
DWG NO	Cyperss point
Rev	A00
Date: Monday, January 09, 2012	Sheet 41 of 59

CPU Fan





SYS Fan



DELL INC.

Title

FAN

DWG NO

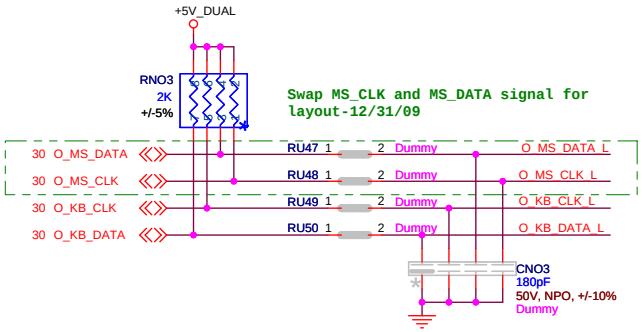
Cyperss point

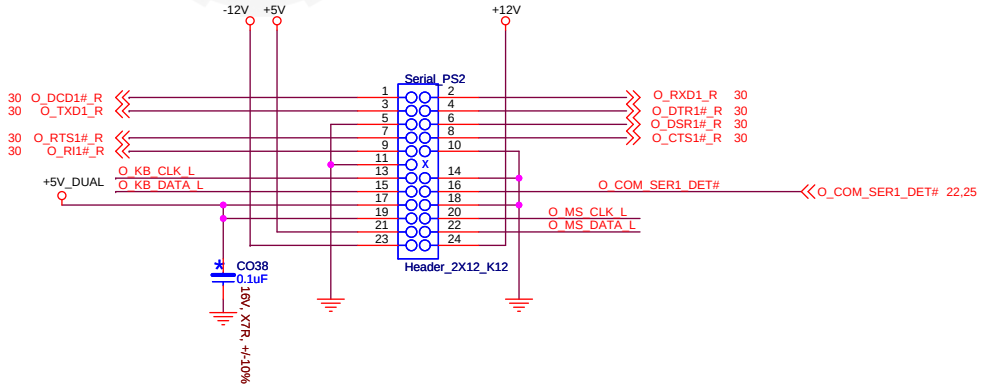
Rev A00

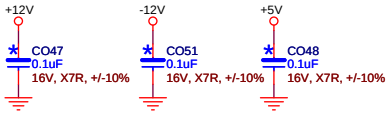
Date: Monday, January 09, 2012 Sheet 42 of 59

Serial

PS2 port







DELL INC.

Title

Serial / PS2 port

DWG NO

Cyperss point

Rev A00

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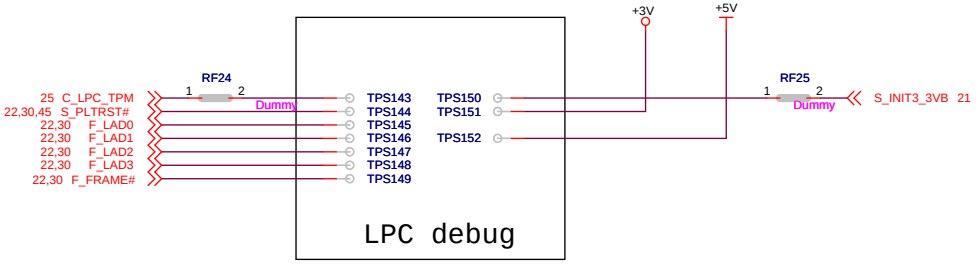
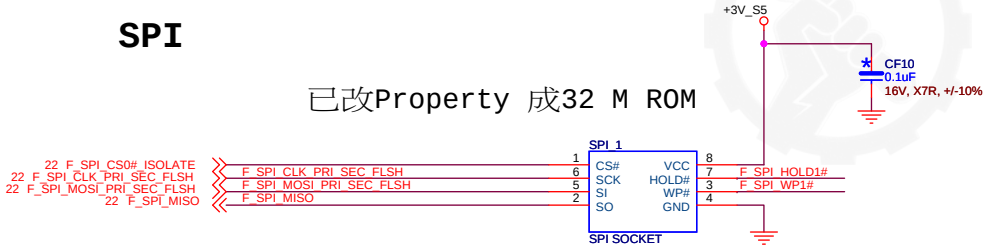
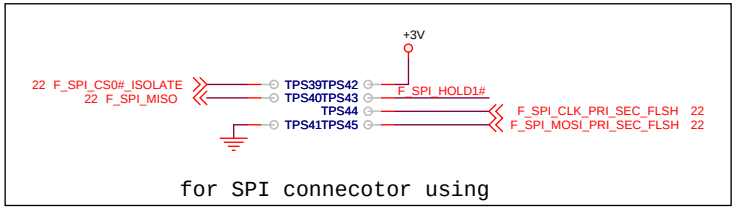
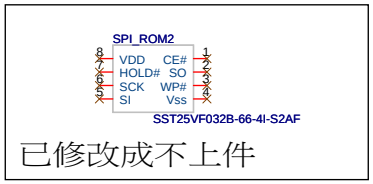


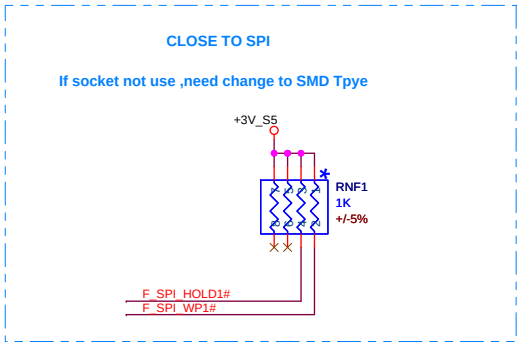
SPI

已改Property 成32 M ROM









<LBL>
Label for 686BIOS AMI
<Tolerance>
BIOS_Lable

<LBL>
Lable
<Tolerance>
2D_Lable

DELL INC.

Title
SPI/LPC DBG

DWG NO
Cyperss point

Rev
A00

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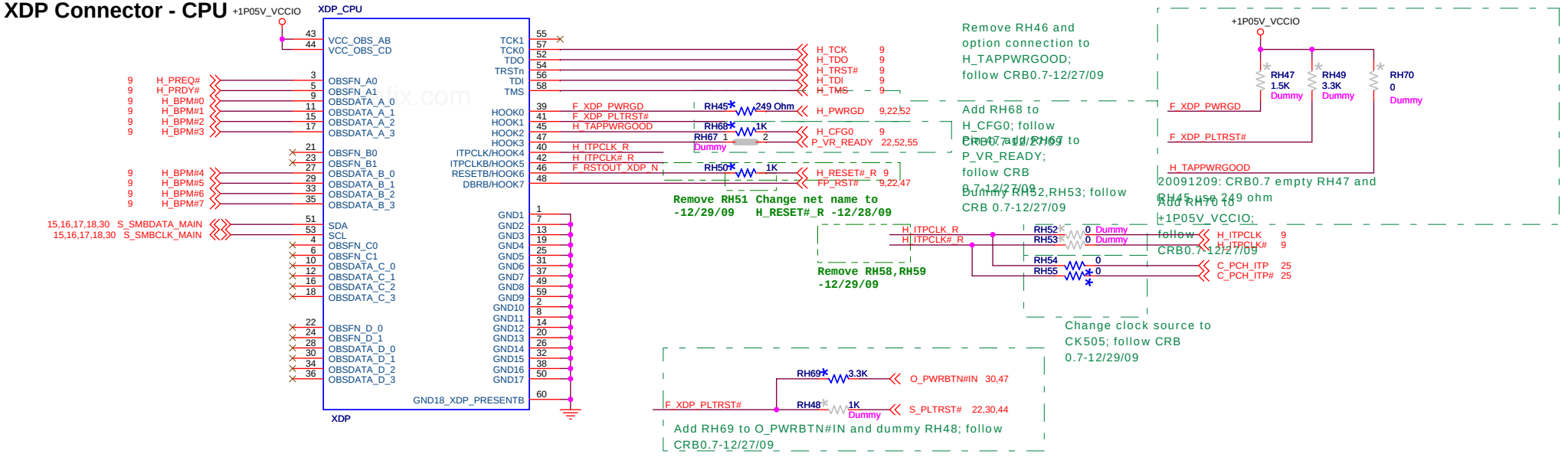
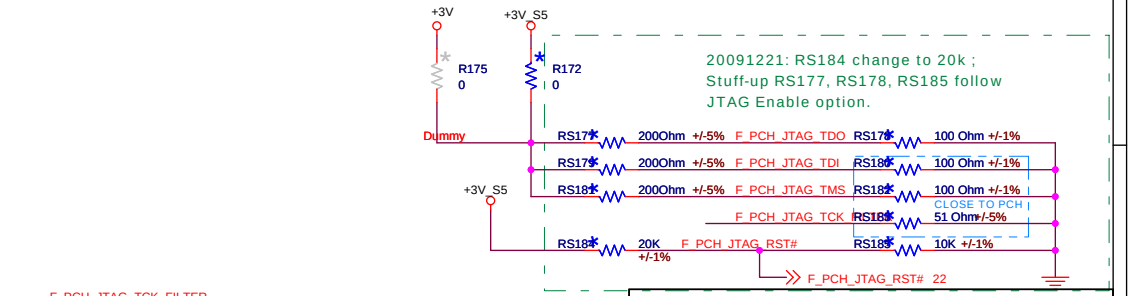
XDP Connector - CPU



2009/12/21 Update JTAG Table		PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
F_PCH_JTAG_TDO	RS177	No Stff	200 Ohms[1]	No Stuff	No Stuff
	RS178	No Stff	100 Ohms[1]	No Stuff	No Stuff
F_PCH_JTAG_TMS	RS179	200 Ohms	200 Ohms	No Stuff	No Stuff
	RS180	100 Ohms	100 Ohms	No Stuff	No Stuff
F_PCH_JTAG_TDI	RS181	200 Ohms	200 Ohms	20K Ohms	No Stuff
	RS182	100 Ohms	100 Ohms	10K Ohms	No Stuff
F_PCH_FILTER_TCK	RS183	51 Ohms	51 Ohms	51 Ohms	51 Ohms
F_PCH_JTAG_RST#	RS184	20K Ohms	20K Ohms	No Stuff	No Stuff
	RS185	10K Ohms	10K Ohms	No Stuff	No Stuff

20091221: updated JTAG stuffing table



F_PCH_JTAG_TCK_FILTER → F_PCH_JTAG_TCK_FILTER 22
F_PCH_JTAG_TDI → F_PCH_JTAG_TDI 22
F_PCH_JTAG_TDO → F_PCH_JTAG_TDO 22
F_PCH_JTAG_TMS → F_PCH_JTAG_TMS 22

DELL INC.

Title: XDP

DWG NO: Cyperss point

Rev: A00

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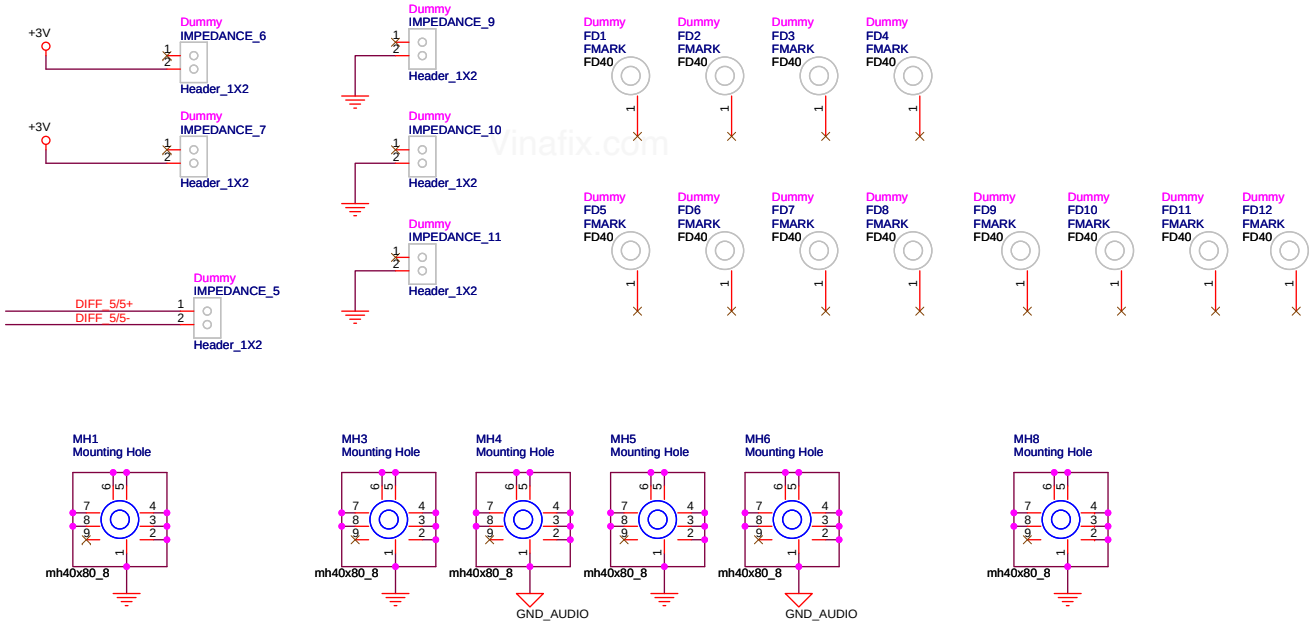
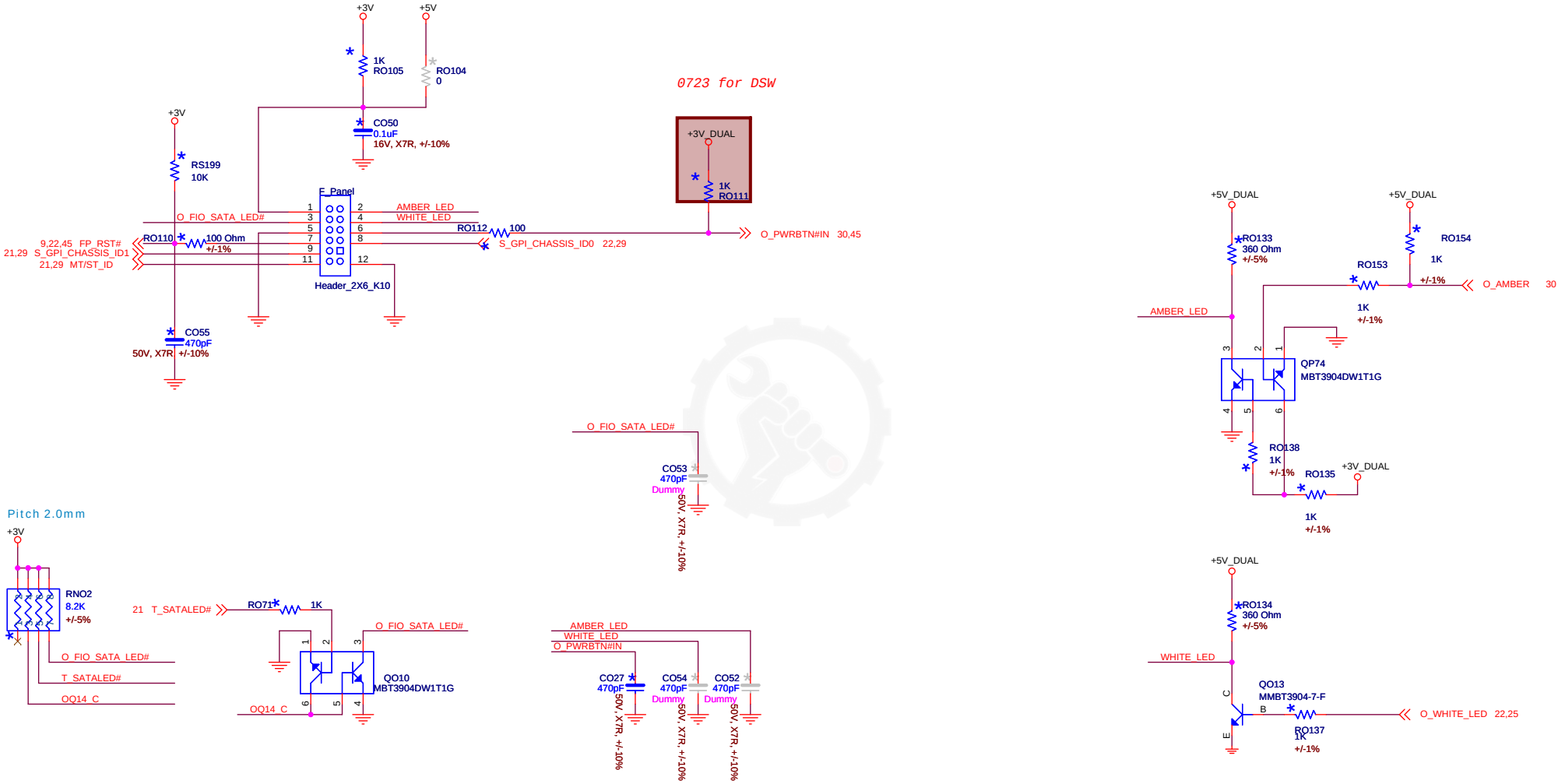


20100108: Add for EMI

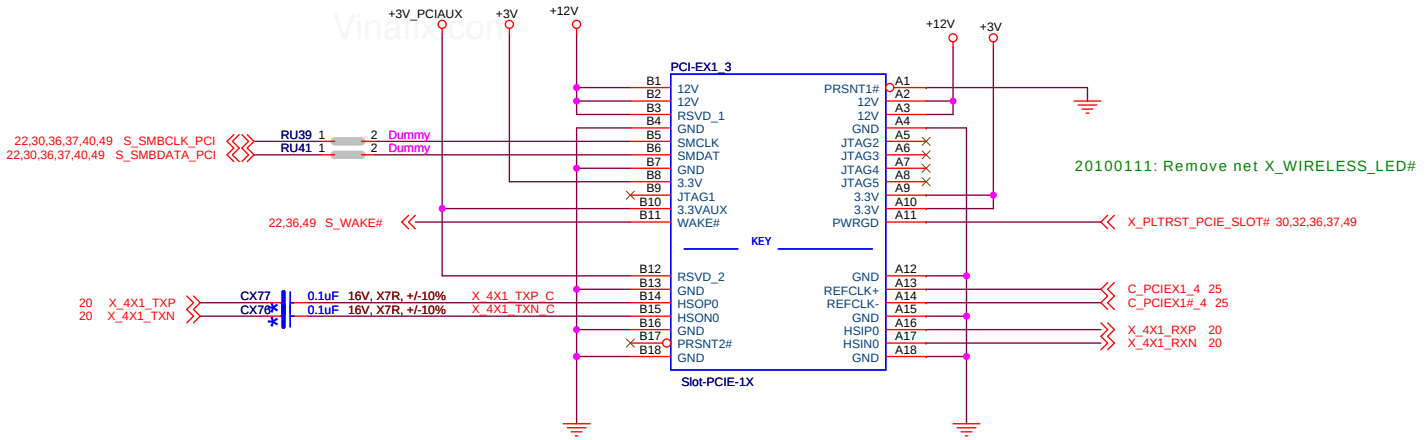
DELL INC.		
Title: **EMI**		
DWG NO: ***Cyperss point***		Rev: **A00**
Date: Monday, January 09, 2012	Sheet 46 of 59	

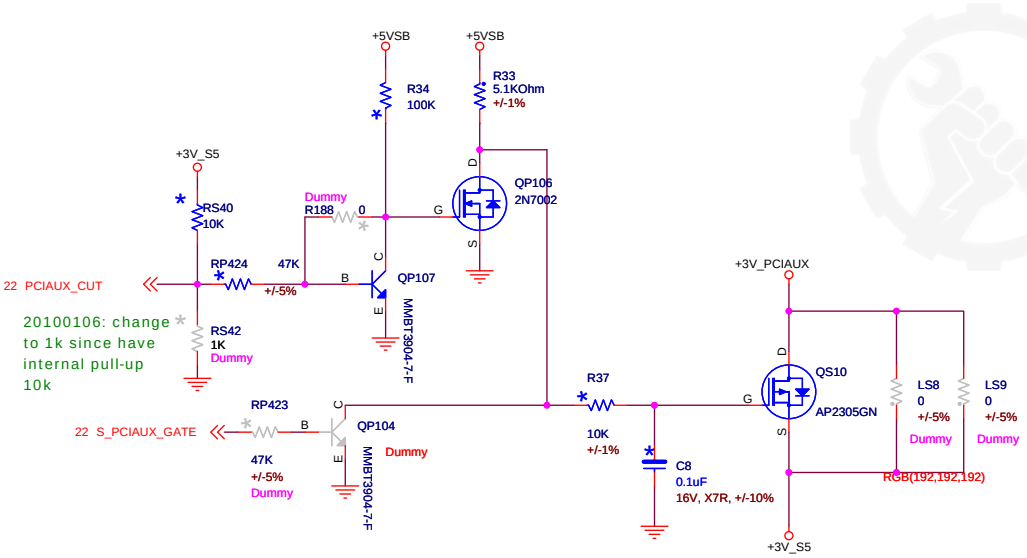
Front_IO Header



DELL INC.

Title	**Front_Panel**
DWG NO	***Cyperss point***
Rev	**A00**
Date: Thursday, March 22, 2012	Sheet 47 of 59





DELL INC.

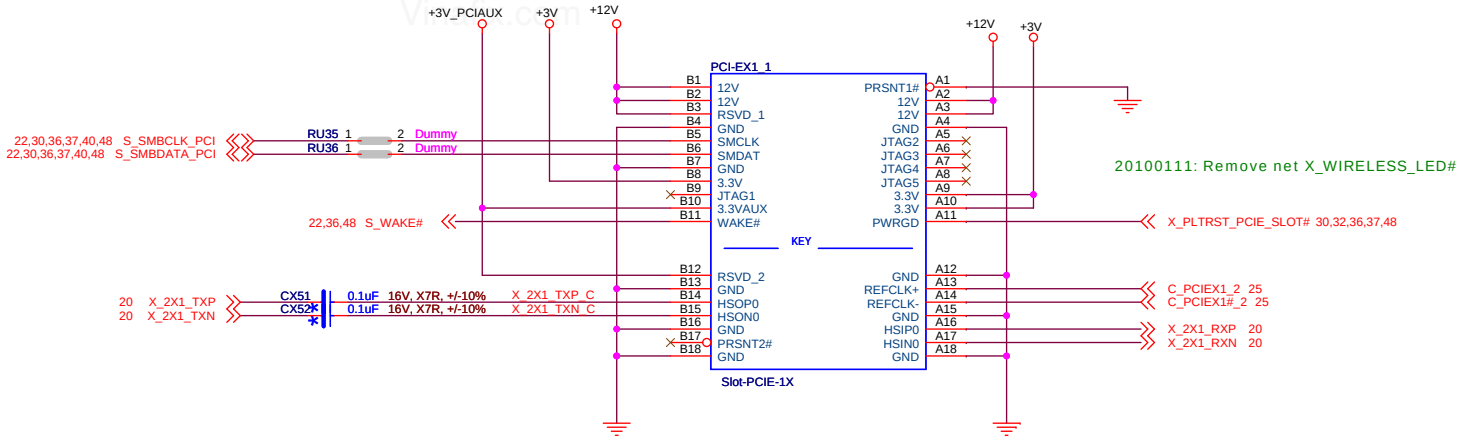
Title

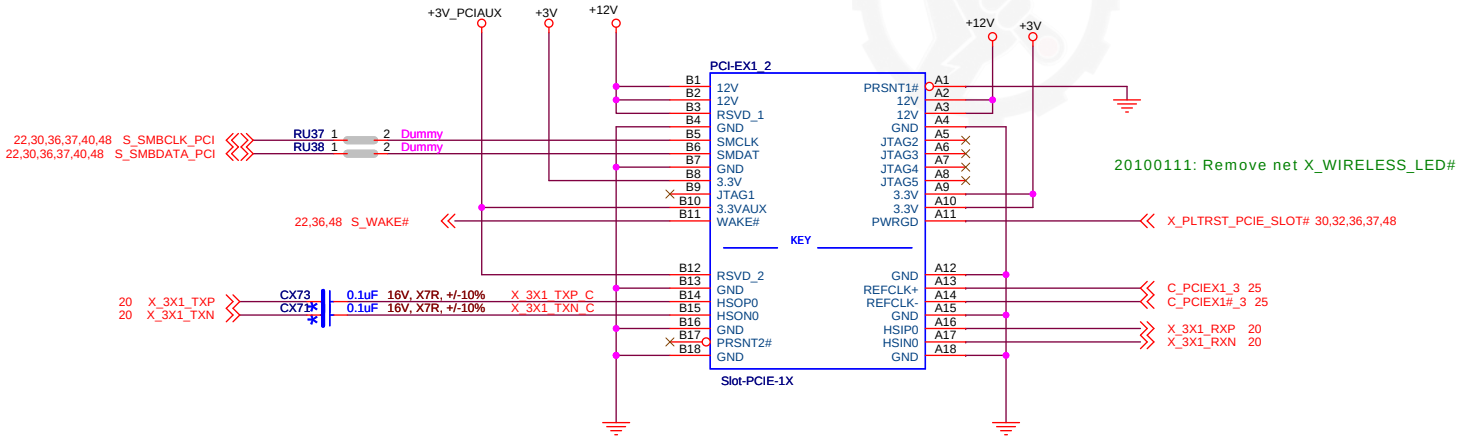
Slot4: PCIEx1

DWG NO *Cyperss point*

Rev A00

Date: Monday, January 09, 2012 Sheet 48 of 59





DELL INC.

Title

Slot2.3: PCIe 1x

DWG NO

Cyperss point

Rev **A00**

Date: Monday, January 09, 2012 Sheet 49 of 59

INT USB

Black card reader

white TOP_USB

BT orange

GPIO
Hi : SDP only
Lo :DCP, apple only

stuff R198
dummy R190

K/M wake up
Hi : enable
Lo :disable

USB3.0

Place ESD Close to Header

Front
Light blue

CRB both Dummy

Change 2.6A DCR 47m ohm for IR Drop.

Dummy for Cost down-11/23/09

DELL INC.

Title: Front USB

DWG NO: Cyperss point

Rev: A00

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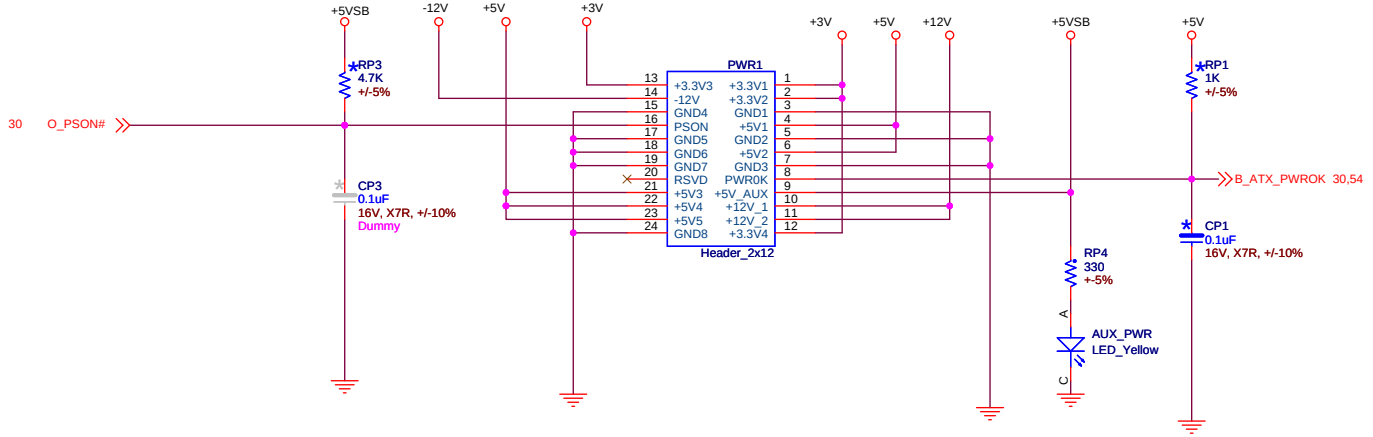
ATX POWER CONNECTOR



for plane stable

+3V CP34 0.1uF 16V, X7R, +/-10%

+3V CP35 0.1uF 16V, X7R, +/-10%

USB3.0

+1P05V_PCH CP45 0.1uF 16V, X7R, +/-10%

+1P05V_PCH CP47 0.1uF 16V, X7R, +/-10%

O_RXD1_R

+5V CP18 +5V_DUAL

0.1uF Dummy 16V, X7R, +/-10%

C_PCIEX16#_1

+3V CP19 +12V

0.1uF Dummy 16V, X7R, +/-10%

+3V CP20 +12V

0.1uF Dummy 16V, X7R, +/-10%

USB3_RX2_PCH_DN

+3V CP22 +1P05V_PCH

0.1uF 16V, X7R, +/-10%

+1P05V_PCH CP21 +12V

0.1uF Dummy 16V, X7R, +/-10%

+3V C_96M_PCH# CP24 0.1uF 16V, X7R, +/-10% Dummy	+3V C_PCIEX16_1 CP29 0.1uF 16V, X7R, +/-10% Dummy	+3V CP30 0.1uF 16V, X7R, +/-10% Dummy	+1P05V_VCCIO H_DMI_RXN2 CP36 0.1uF 16V, X7R, +/-10% Dummy	+1P05V_VCCIO H_DMI_RXN2 CP37 0.1uF 16V, X7R, +/-10% Dummy	+1P05V_VCCIO H_DMI_RXN2 CP38 0.1uF 16V, X7R, +/-10% Dummy	
HDMI +1P05V_PCH CP25 0.1uF 16V, X7R, +/-10% Dummy	+3V C_14M_MCH CP26 0.1uF 16V, X7R, +/-10% Dummy	+5V_DUAL C_48M_SIO CP31 0.1uF 16V, X7R, +/-10% Dummy	+5V_DUAL A_Z_BITCLK CP33 0.1uF 16V, X7R, +/-10% Dummy	+3V C_14M_MCH CP39 0.1uF 16V, X7R, +/-10% Dummy	+3V SPI CP40 0.1uF 16V, X7R, +/-10% Dummy	+1P05V_PCH HDMI CP48 0.1uF 16V, X7R, +/-10% Dummy

DELL INC.

Title: **Power Conn**

DWG NO: ***Cyperss point***

Rev: **A00**

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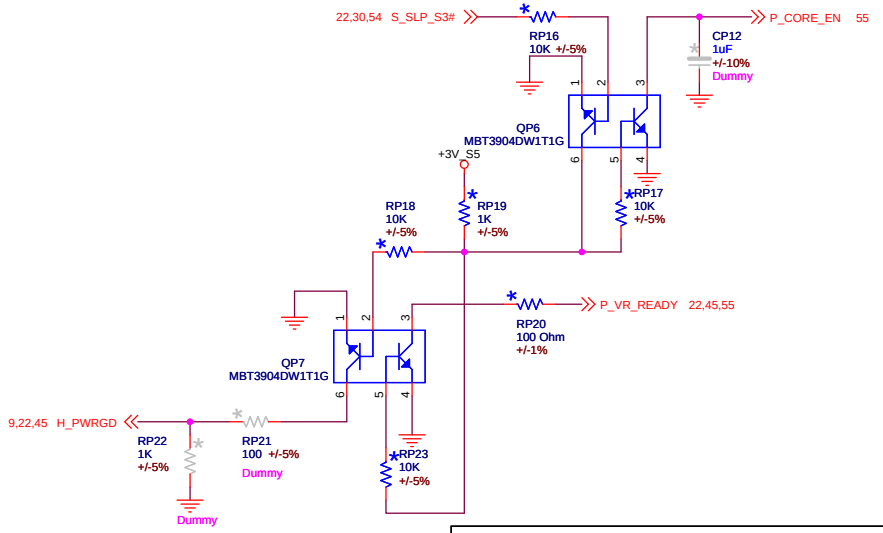
For Deep Sleep

RESUME RESET Logic

VR_READY DEFENSIVE



DELL INC.

Title

Power Sequence

DWG NO

Cyperss point

Rev A00

Date: Monday, January 09, 2012 Sheet 52 of 59

0602 Del sequence control circuit.

0602 Del sequence control circuit.

DELL INC.

Title

Power-1:Linear Power-1

DWG NO

Cyperss point

Rev **A00**

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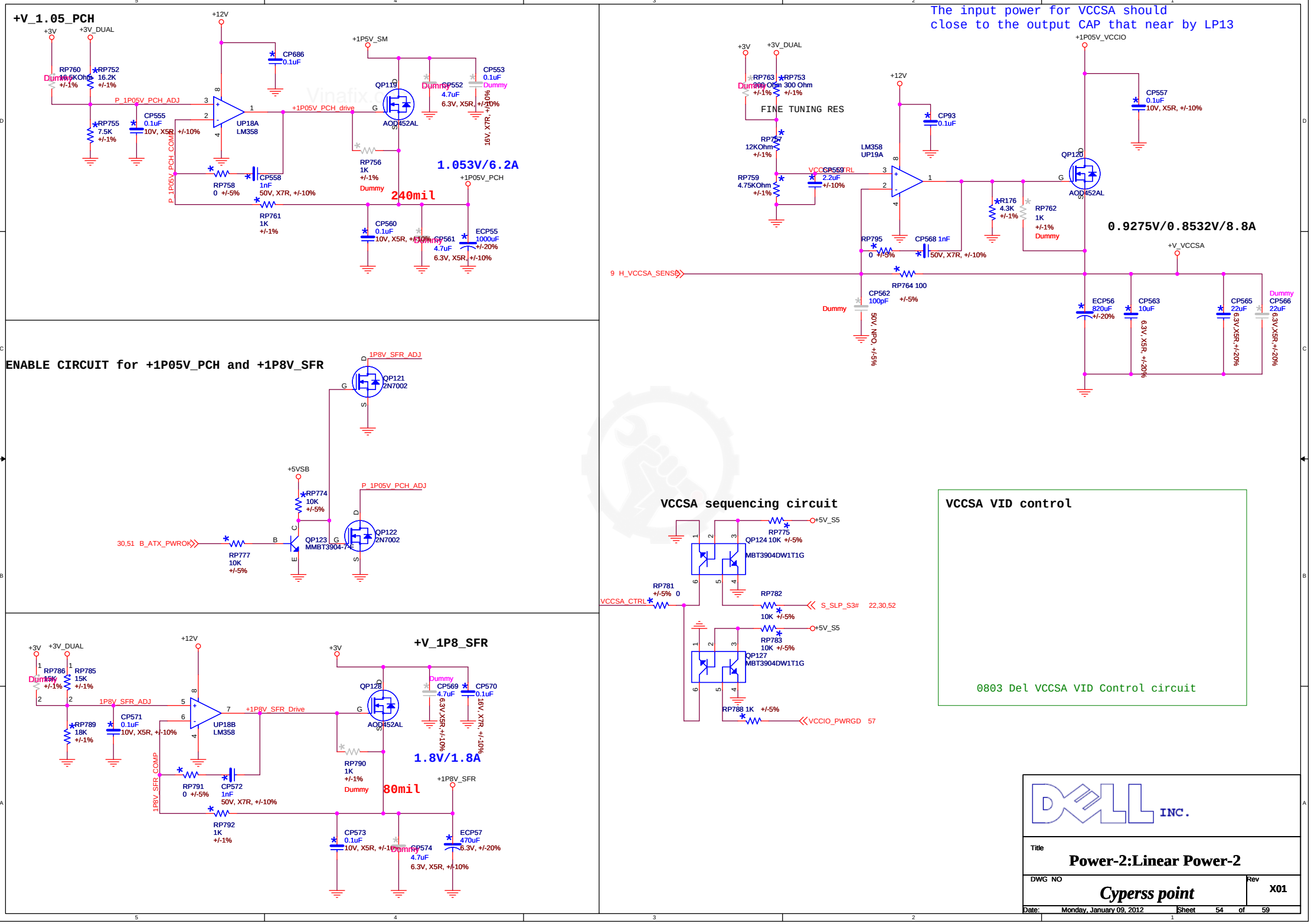
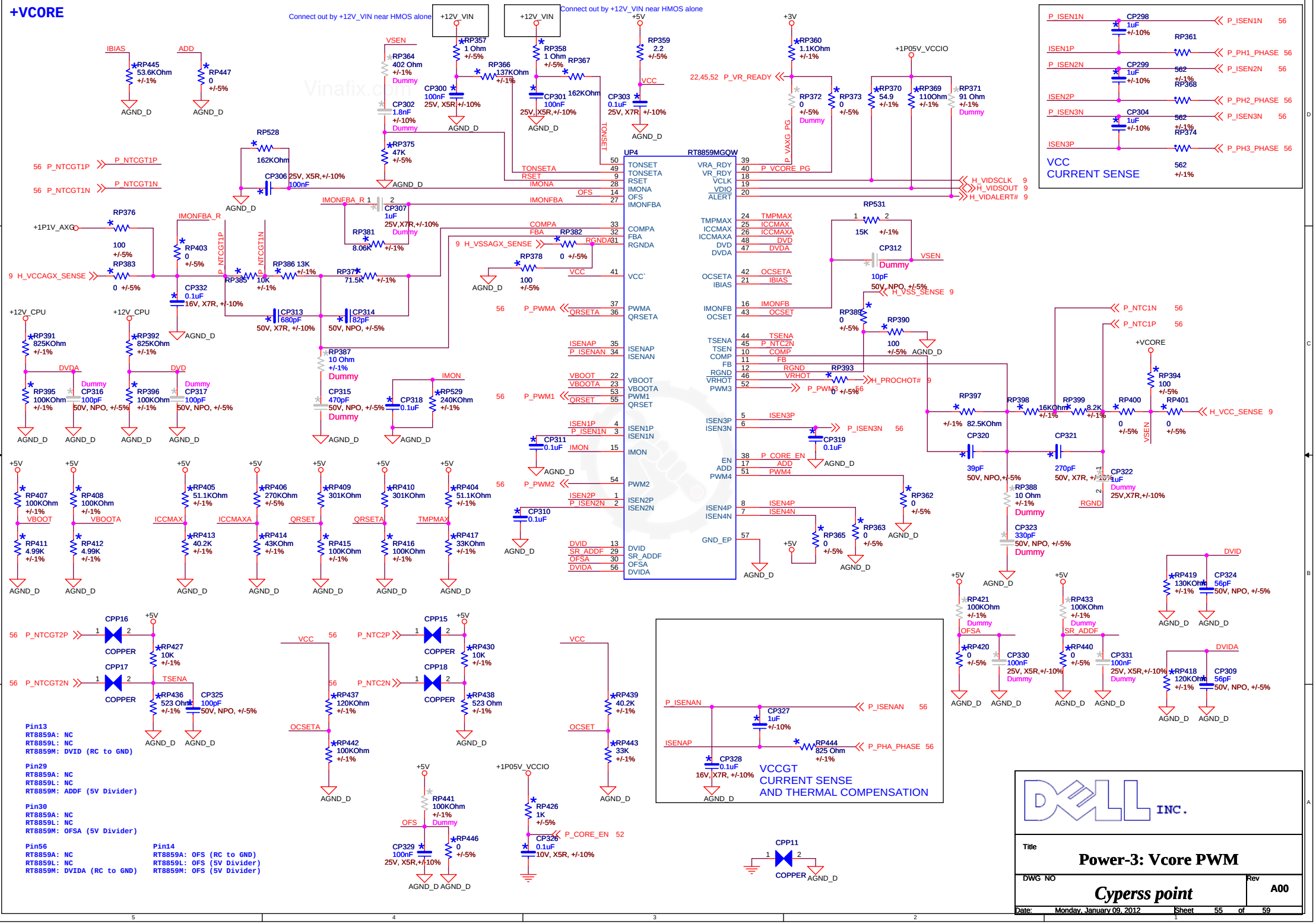
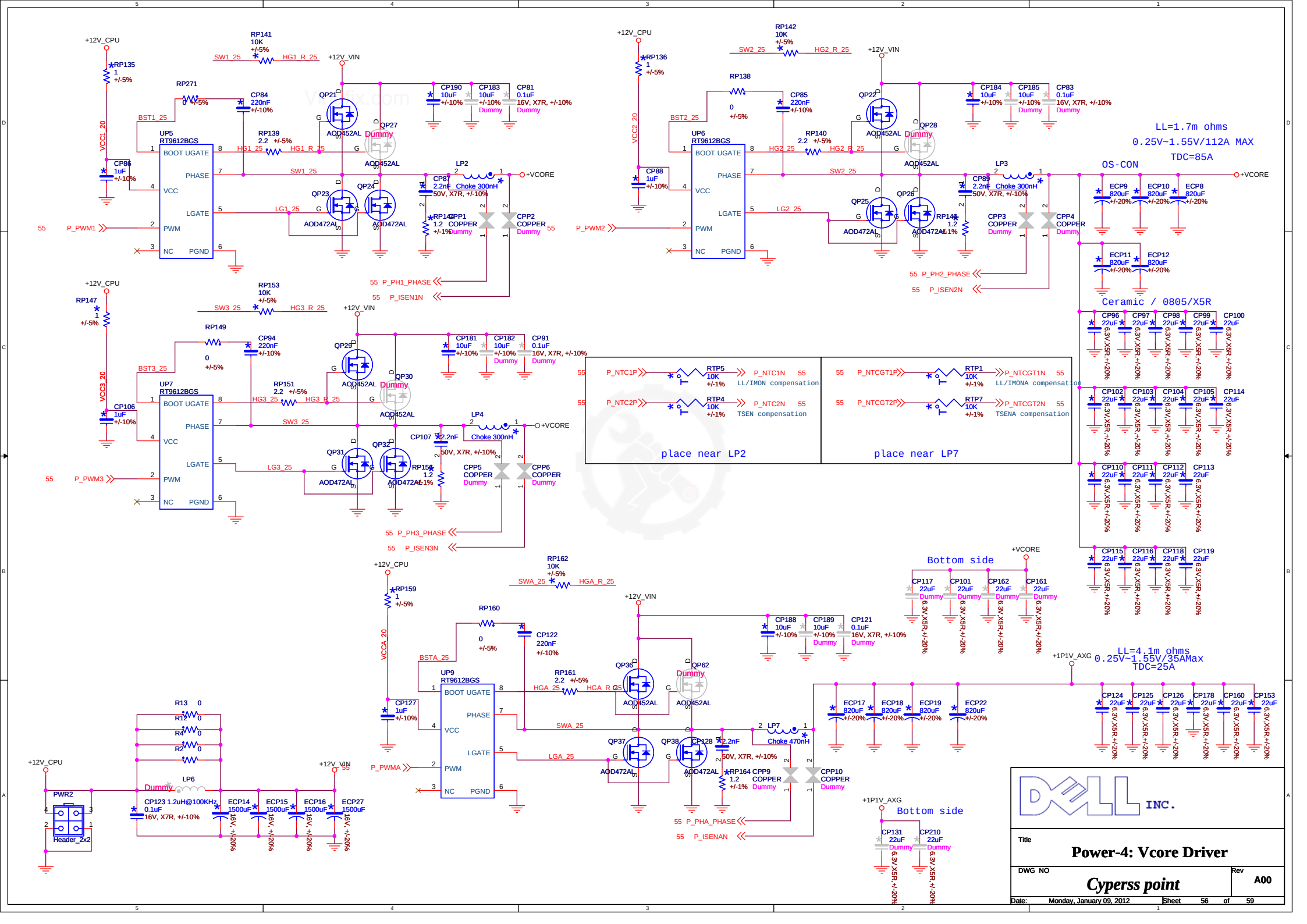

+V_1.05_PCH
+3V
+3V_DUAL
+12V
RP760 16.5KOhm +/-1%
RP752 16.2K +/-1%
RP755 7.5K +/-1%
CP555 0.1uF 10V, X5R +/-10%
P_1P05V_PCH_ADJ
P_1P05V_PCH_COMP
UP18A LM358
CP686 0.1uF
+1P05V_PCH_drive
+1P5V_SM
QP119 AOD452AL
CP552 4.7uF 6.3V, X5R, +/-10%
CP553 0.1uF Dummy
16V, X7R, +/-10%
RP756 1K +/-1% Dummy
1.053V/6.2A
RP758 0 +/-5%
CP558 1nF 50V, X7R, +/-10%
240mil
+1P05V_PCH
RP761 1K +/-1%
CP560 0.1uF 10V, X5R, +/-10%
CP561 4.7uF 6.3V, X5R, +/-10%
ECP55 1000uF +/-20%
The input power for VCCSA should close to the output CAP that near by LP13
+1P05V_VCCIO
RP763 300 Ohm +/-1%
RP753 300 Ohm +/-1%
FINE TUNING RES
RP757 12KOhm +/-1%
RP759 4.75KOhm +/-1%
LM358 UP19A
CP93 0.1uF
CP557 0.1uF 10V, X5R, +/-10%
QP120 AOD452AL
VCCSA_SENSE
CP559 2.2uF +/-10%
R176 4.3K +/-1%
RP762 1K +/-1%
Dummy
0.9275V/0.8532V/8.8A
RP795 0 +/-5%
CP568 1nF 50V, X7R, +/-10%
+V_VCCSA
9 H_VCCSA_SENSE
RP764 100
CP562 100pF +/-5%
50V, NPO, +/-5%
ECP56 820uF +/-20%
CP563 10uF 6.3V, X5R, +/-20%
CP565 22uF 6.3V, X5R, +/-20%
CP566 22uF 6.3V, X5R, +/-20%
ENABLE CIRCUIT for +1P05V_PCH and +1P8V_SFR
1P8V_SFR_ADJ
QP121 2N7002
+5VSB
RP774 10K +/-5%
P_1P05V_PCH_ADJ
30,51 B_ATX_PWROK
RP777 10K +/-5%
QP123 MMBT3904-7-F
QP122 2N7002
VCCSA sequencing circuit
+5V_S5
RP775 10K +/-5%
QP124 MBT3904DW1T1G
RP781 +/-5% 0
VCCSA_CTRL
RP782 10K +/-5%
S_SLP_S3# 22,30,52
QP127 MBT3904DW1T1G
RP783 10K +/-5%
RP788 1K +/-5%
VCCIO_PWRGD 57
VCCSA VID control
0803 Del VCCSA VID Control circuit
+V_1P8_SFR
RP786 15K +/-1%
RP785 15K +/-1%
RP789 18K +/-1%
CP571 0.1uF 10V, X5R, +/-10%
1P8V_SFR_ADJ
UP18B LM358
+1P8V_SFR_Drive
QP128 AOD452AL
CP569 4.7uF 6.3V, X5R, +/-10%
CP570 0.1uF 16V, X7R, +/-10%
1.8V/1.8A
RP790 1K +/-1% Dummy
80mil
+1P8V_SFR
RP791 0 +/-5%
CP572 1nF 50V, X7R, +/-10%
1P8V_SFR_COMP
RP792 1K +/-1%
CP573 0.1uF 10V, X5R, +/-10%
CP574 4.7uF 6.3V, X5R, +/-10%
ECP57 470uF 6.3V, +/-20%
DELL INC.
Title
Power-2:Linear Power-2
DWG NO
Cyperss point
Rev
X01
Date: Monday, January 09, 2012
Sheet 54 of 59

+VCORE



Title	Power-3: Vcore PWM
DWG NO	Cyperss point
Rev	A00
Date:	Monday, January 09, 2012
Sheet	55 of 59


+12V_CPU
+12V_VIN
+VCORE
UP5 RT9612BGS
UP6 RT9612BGS
UP7 RT9612BGS
UP9 RT9612BGS
BOOT UGATE
PHASE
VCC
LGATE
PWM
NC PGND
P_PWM1
P_PWM2
P_PWM3
P_PWMA
P_PH1_PHASE
P_PH2_PHASE
P_PH3_PHASE
P_PHA_PHASE
P_ISEN1N
P_ISEN2N
P_ISEN3N
P_ISENAN
LL=1.7m ohms
0.25V~1.55V/112A MAX
TDC=85A
OS-CON
Ceramic / 0805/X5R
LL=4.1m ohms
0.25V~1.55V/35AMax
TDC=25A
Bottom side
place near LP2
place near LP7
LL/IMON compensation
LL/IMONA compensation
TSEN compensation
TSENA compensation
AOD452AL
AOD472AL
Dummy
Header_2x2
DELL INC.
Title
Power-4: Vcore Driver
DWG NO
Cyperss point
Rev
A00
Date: Monday, January 09, 2012
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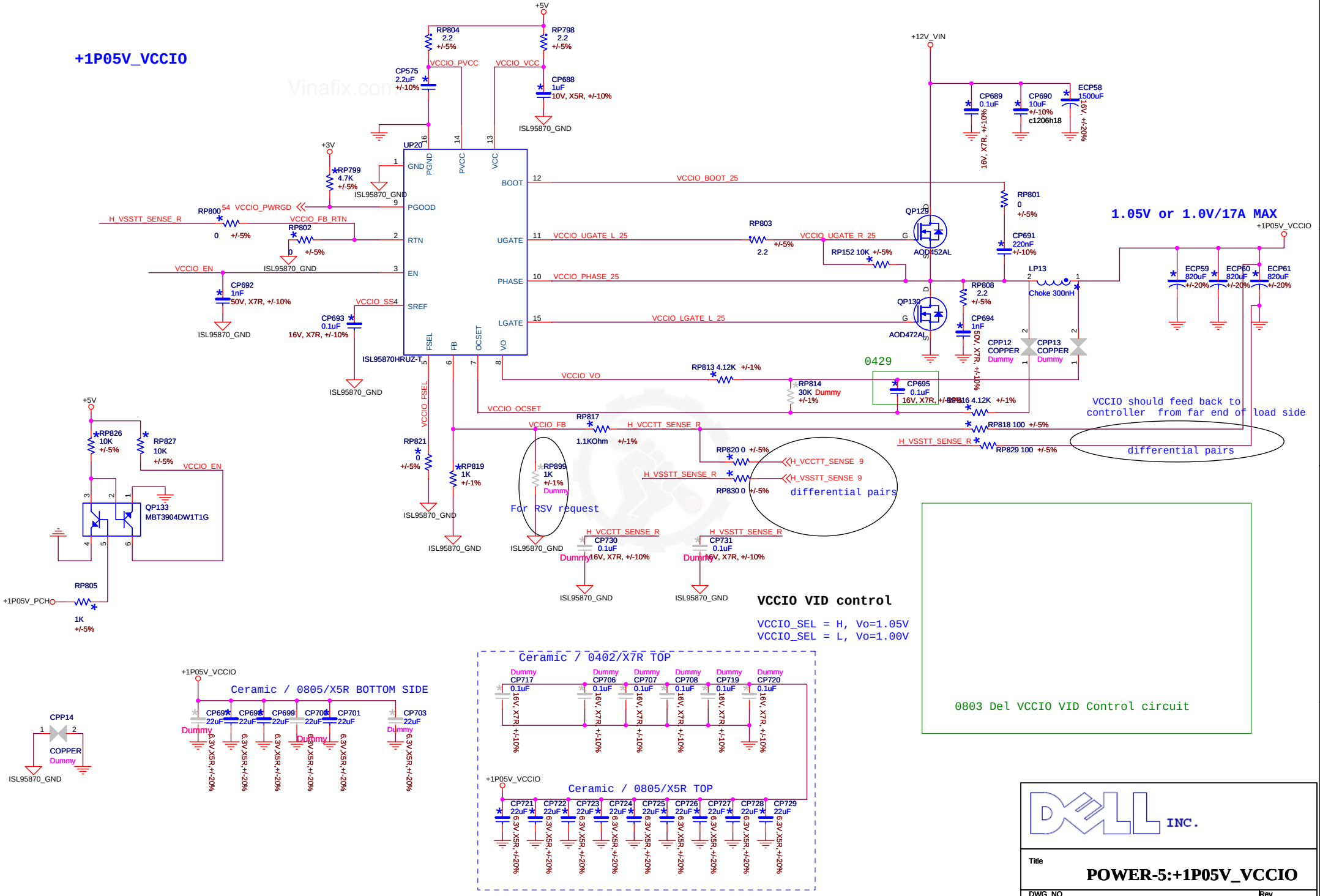
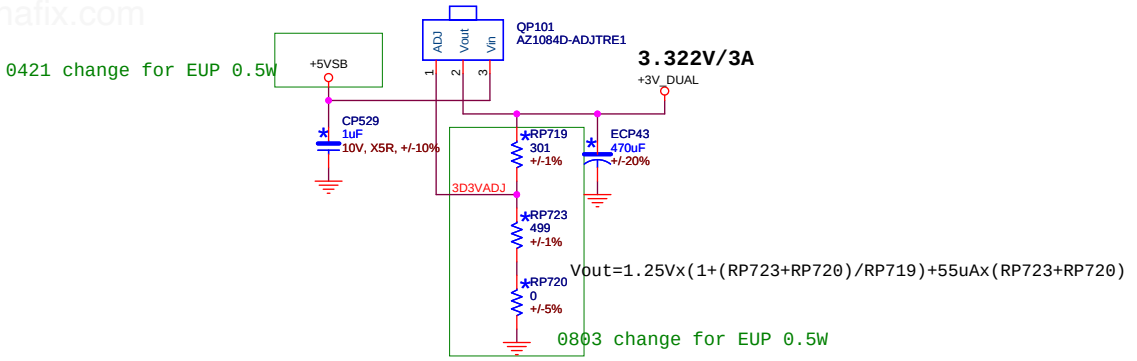
+1P05V_VCCIO

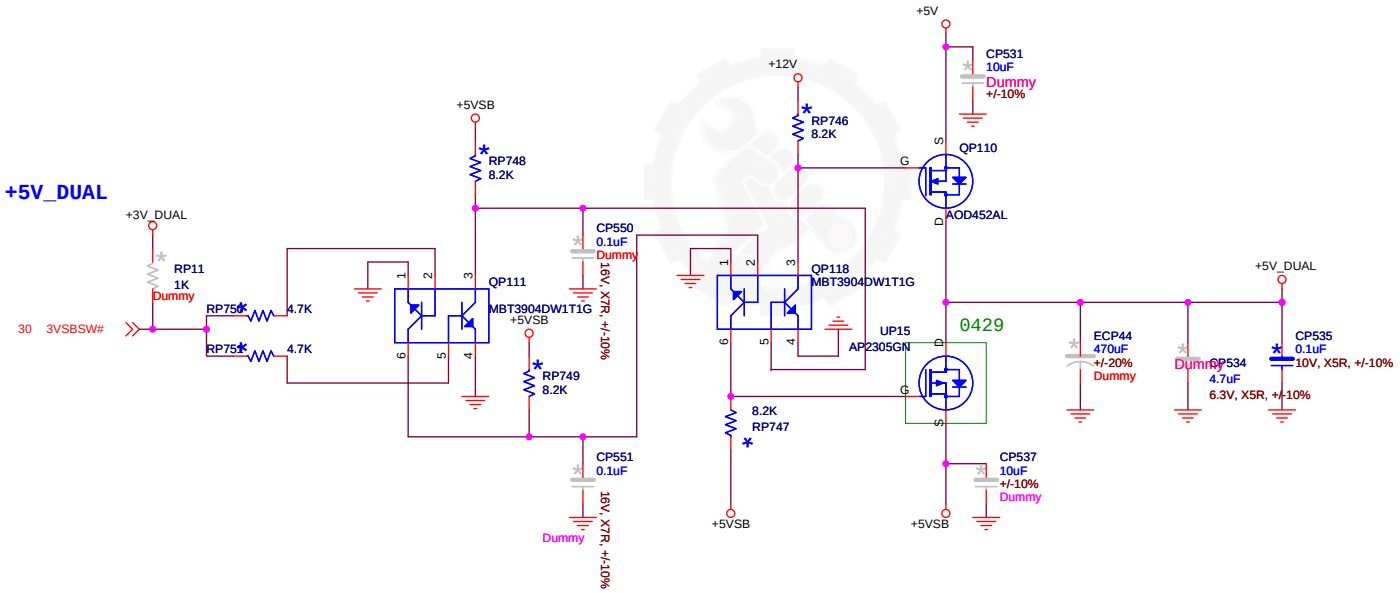


Title	POWER-5:+1P05V_VCCIO
DWG NO	Cyperss point
Rev	X01
Date:	Monday, January 09, 2012
Sheet	57 of 59

+3V_DUAL



+5V_DUAL



DELL INC.

Title: +5V_DUAL/+3V_DUAL

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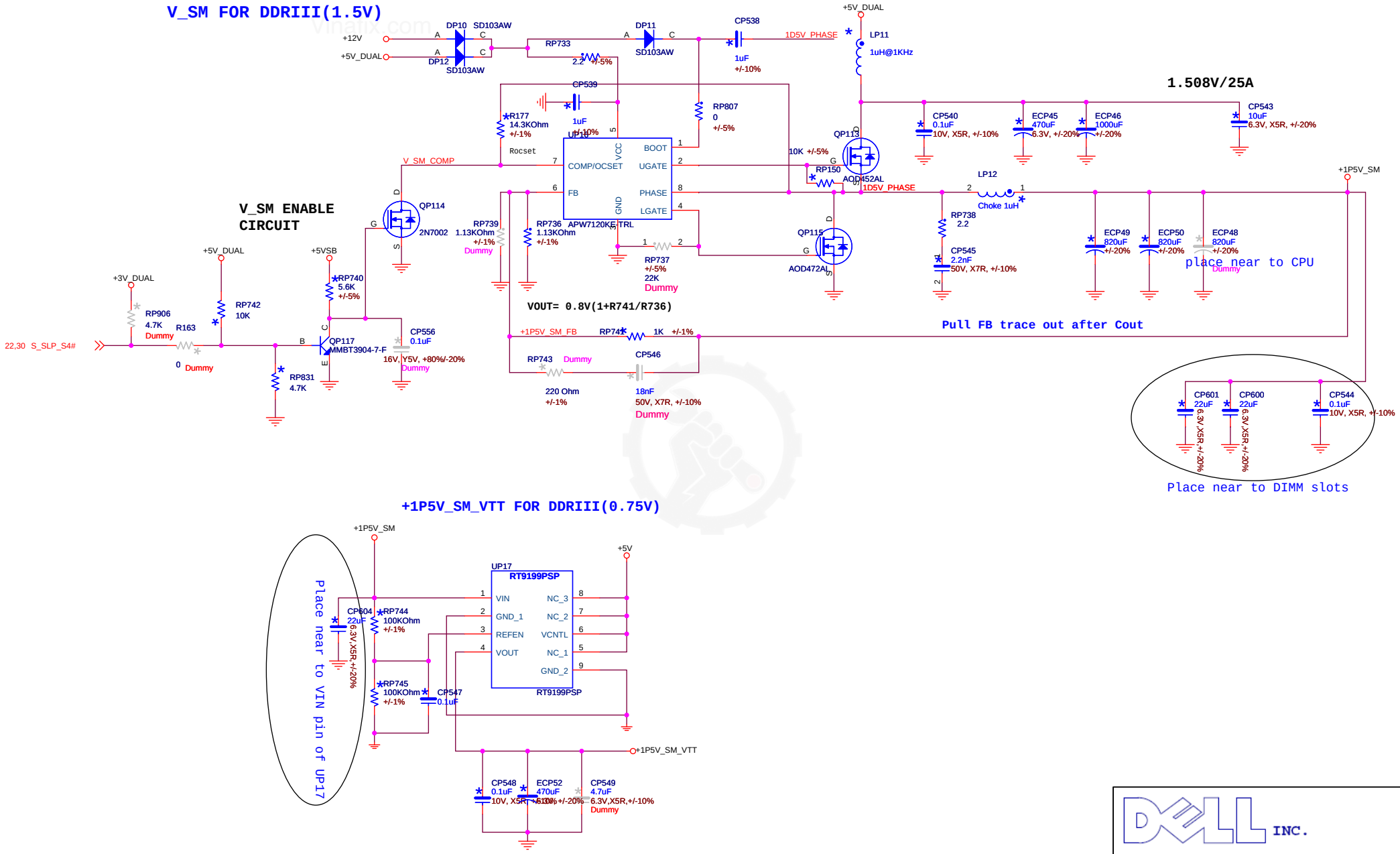

Title	POWER-5:VTT/V_SM
DWG NO	Cyperss point
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