TWK Shark Bay DIAGRAM

01

+3V/+5V S5 PG.33

+1.05V PG.34

CPU Core PG.37~38

DDR3L PG.35

Charge PG.32

Dis-Charge PG.36

+VGACORE PG.39

+1.5V_GFX PG.40

+1.05V_GFX/3V_GFX PG.41

SODIMM1 Max. 4GB PG.12 — 1600MT/s DDR3 L Channel A

SODIMM2 Max. 4GB PG.13 — 1600MT/s DDR3 L Channel B

INTEL Haswell
Processor : Quad Core
Power : 47 (Watt)
Package : rPGA947
Size : 37.5 x 37.5 (mm)
PG.2~5

PCI-E x8 — nVIDIA N15P-GX(GT 860M)
GB4128
FCBGA908
29mm X 29mm
PG.14~18

eDP (5.4Gb/s)

DDI (5.4Gb/s)

DDR3 900MHz — VRAM 1024MB GDDR5B x32 PG.19~20

FDI DMI

HDD PG.30 — SATA0 6GB/s SATA0

ODD PG.30 — SATA4 3GB/s SATA4

mSATA PG.30 — SATA1 6GB/s SATA1

INTEL PCH
Lynx Point
Power : 3.5 Watt
Package : FCBGA695
Size : 20 x 20 (mm)
PG.6~11

eDP — RTD 2136S DP to LVDS Converter PAGE 22 — LVDS Interface — LVDS PG.23

DP Port B — HDMI PG.21

PCI-E x 1 LANE2 LANE1

LAN RTL8111GS-CG GbE PG.27

WLAN BT COMBO PG.26 — USB 2.0 PORT10

PCI-E x 1 LANE3

Card Reader 5227-GRT PG.24

LPC

KBC IT8528E PG.31

KB PG.26 | TP PG.28 | ROM PG.31 | FAN PG.30

USB 3.0 PORT1 — USB3.0 Ports PG.28 — USB Charge X1 SLG55583A PG.28

USB 3.0 PORT2 — USB3.0 Ports PG.28

USB 2.0 PORT2,9 — USB2.0 Ports X2 PG.26

PORT1 PORT0 PORT3 — Webcam PG.23

AUDIO CODEC ALC282-CG PG.25

Speaker PG.25

HP/MIC PG.25

Analog MIC PG.25

Stackup

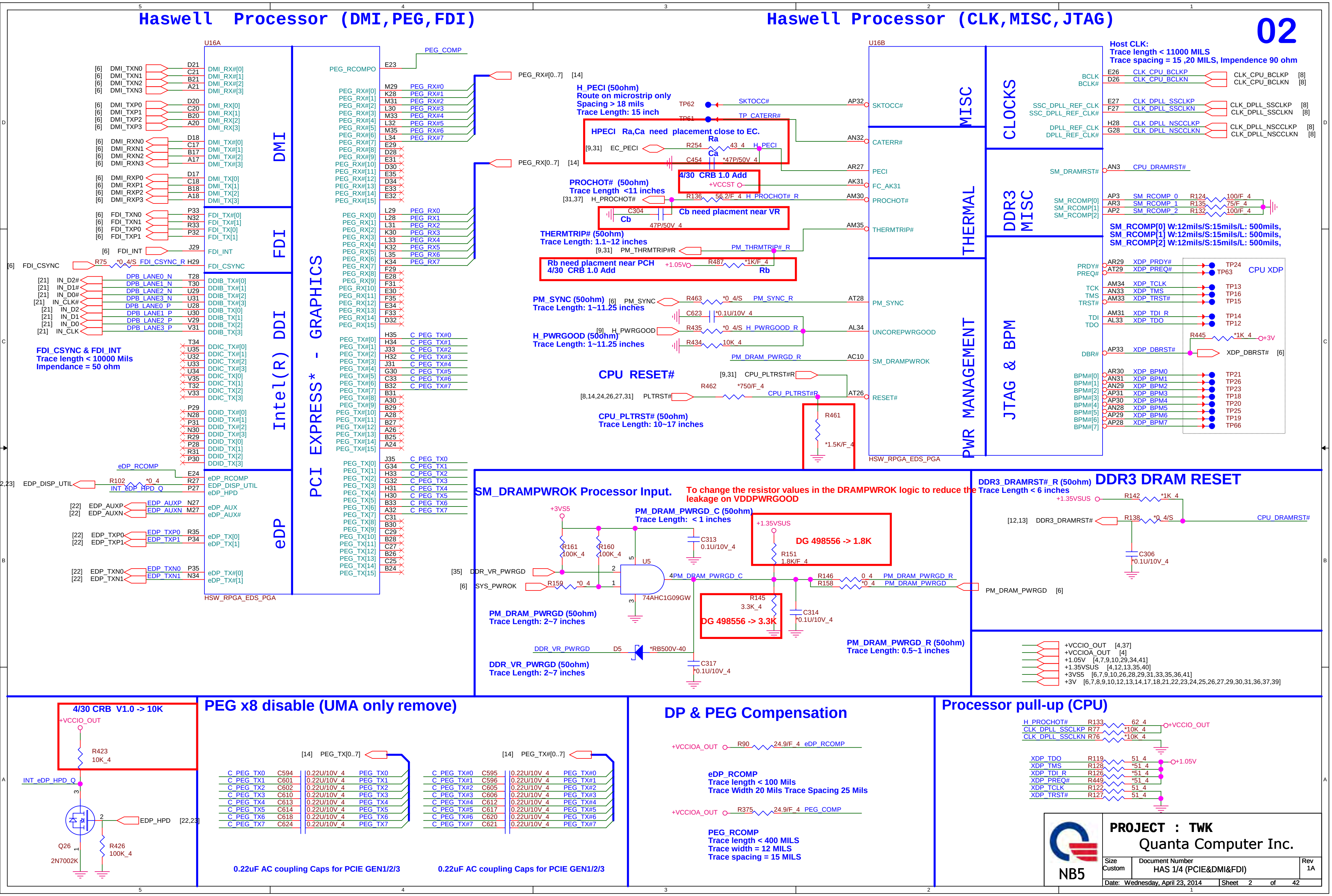
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT

NB5

PROJECT : TWK
Quanta Computer Inc.

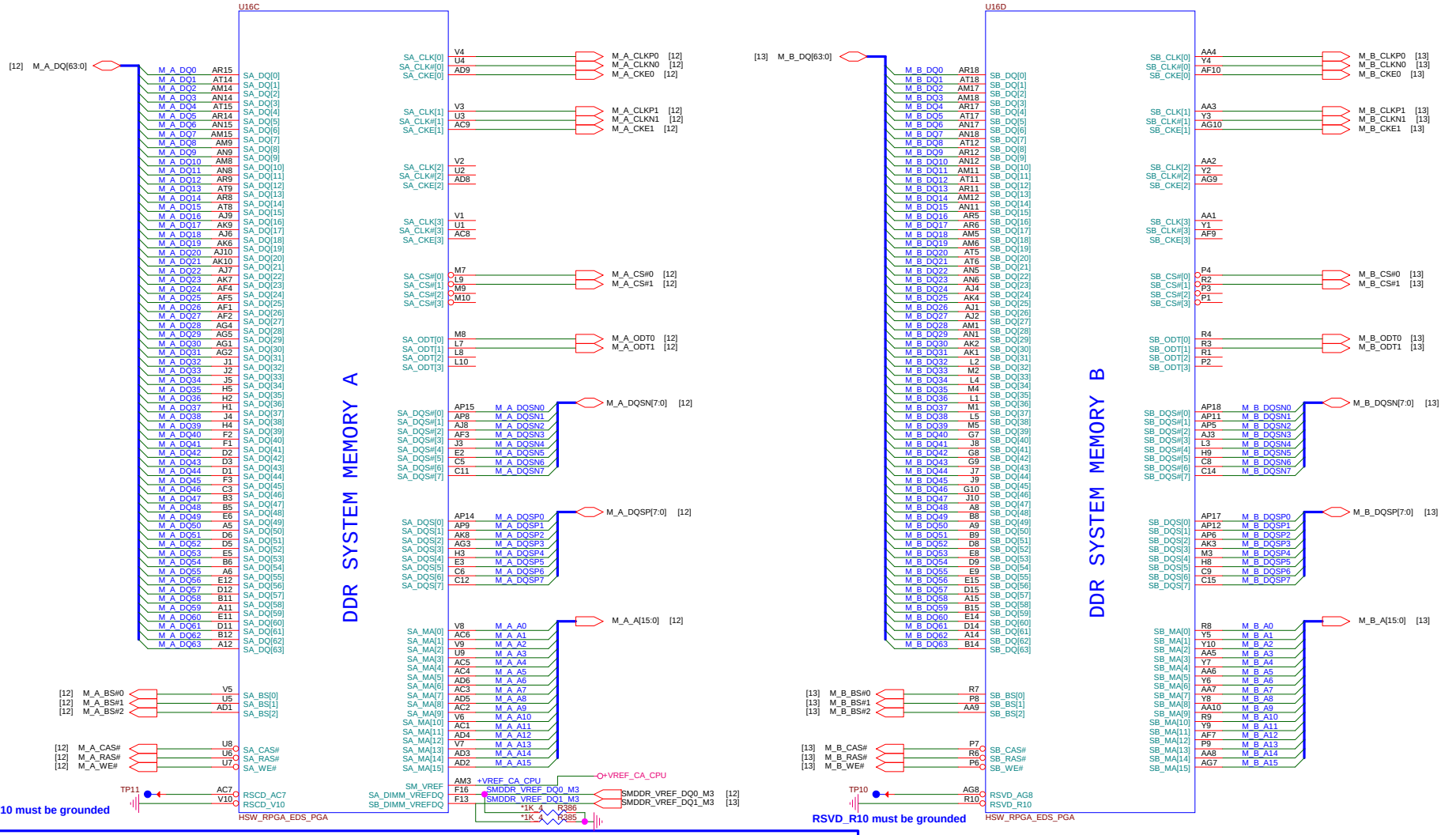
Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Wednesday, April 23, 2014 Sheet 1 of 42


Haswell Processor (DMI,PEG,FDI)
Haswell Processor (CLK,MISC,JTAG)
02
U16A
DMI
FDI
Intel(R) DDI
eDP
PCI EXPRESS* - GRAPHICS
HSW_RPGA_EDS_PGA
DMI_TXN0
DMI_TXN1
DMI_TXN2
DMI_TXN3
DMI_TXP0
DMI_TXP1
DMI_TXP2
DMI_TXP3
DMI_RXN0
DMI_RXN1
DMI_RXN2
DMI_RXN3
DMI_RXP0
DMI_RXP1
DMI_RXP2
DMI_RXP3
FDI_TXN0
FDI_TXN1
FDI_TXP0
FDI_TXP1
FDI_INT
FDI_CSYNC
IN_D2#
IN_D1#
IN_D0#
IN_CLK#
IN_D2
IN_D1
IN_D0
IN_CLK
DPB_LANE0_N
DPB_LANE1_N
DPB_LANE2_N
DPB_LANE3_N
DPB_LANE0_P
DPB_LANE1_P
DPB_LANE2_P
DPB_LANE3_P
FDI_CSYNC & FDI_INT
Trace length < 10000 Mils
Impendance = 50 ohm
eDP_RCOMP
EDP_DISP_UTIL
INT_eDP_HPD_Q
EDP_AUXP
EDP_AUXN
EDP_TXP0
EDP_TXP1
EDP_TXN0
EDP_TXN1
PEG_COMP
PEG_RCOMPO
PEG_RX#[0..7]
PEG_RX[0..7]
C_PEG_TX#0
C_PEG_TX0
U16B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 90 ohm
CLK_CPU_BCLKP
CLK_CPU_BCLKN
CLK_DPLL_SSCLKP
CLK_DPLL_SSCLKN
CLK_DPLL_NSCCLKP
CLK_DPLL_NSCCLKN
H_PECI (50ohm)
Route on microstrip only
Spacing > 18 mils
Trace Length: 15 inch
SKTOCC#
TP_CATERR#
HPECI Ra,Ca need placement close to EC.
EC_PECI
H_PECI
4/30 CRB 1.0 Add
PROCHOT# (50ohm)
Trace Length <11 inches
H_PROCHOT#
H_PROCHOT#_R
Cb need placment near VR
THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
PM_THRMTRIP#R
Rb need placment near PCH
4/30 CRB 1.0 Add
CPU_DRAMRST#
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
SM_RCOMP[0] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[1] W:12mils/S:15mils/L: 500mils,
SM_RCOMP[2] W:12mils/S:15mils/L: 500mils,
CPU XDP
PM_SYNC (50ohm)
Trace Length: 1~11.25 inches
PM_SYNC
H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches
H_PWRGOOD
PM_DRAM_PWRGD_R
CPU RESET#
CPU_PLTRST#R
PLTRST#
CPU_PLTRST#R
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches
XDP_DBRST#
XDP_PRDY#
XDP_PREQ#
XDP_TCLK
XDP_TMS
XDP_TRST#
XDP_TDI_R
XDP_TDO
XDP_BPM0
XDP_BPM1
XDP_BPM2
XDP_BPM3
XDP_BPM4
XDP_BPM5
XDP_BPM6
XDP_BPM7
SM_DRAMPWROK Processor Input.
To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD
PM_DRAM_PWRGD_C (50ohm)
Trace Length: < 1 inches
DG 498556 -> 1.8K
DG 498556 -> 3.3K
DDR_VR_PWRGD
SYS_PWROK
74AHC1G09GW
PM_DRAM_PWRGD (50ohm)
Trace Length: 2~7 inches
DDR_VR_PWRGD (50ohm)
Trace Length: 2~7 inches
PM_DRAM_PWRGD_R (50ohm)
Trace Length: 0.5~1 inches
PM_DRAM_PWRGD
DDR3_DRAMRST#_R (50ohm)
Trace Length < 6 inches
DDR3 DRAM RESET
DDR3_DRAMRST#
CPU_DRAMRST#
+VCCIO_OUT [4,37]
+VCCIOA_OUT [4]
+1.05V [4,7,9,10,29,34,41]
+1.35VSUS [4,12,13,35,40]
+3VS5 [6,7,9,10,26,28,29,31,33,35,36,41]
+3V [6,7,8,9,10,12,13,14,17,18,21,22,23,24,25,26,27,29,30,31,36,37,39]
4/30 CRB V1.0 -> 10K
INT_eDP_HPD_Q
EDP_HPD
Q26
2N7002K
PEG x8 disable (UMA only remove)
PEG_TX[0..7]
PEG_TX#[0..7]
0.22uF AC coupling Caps for PCIE GEN1/2/3
0.22uF AC coupling Caps for PCIE GEN1/2/3
DP & PEG Compensation
eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils
PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS
Processor pull-up (CPU)
PROJECT : TWK
Quanta Computer Inc.
NB5
Size Custom
Document Number
HAS 1/4 (PCIE&DMI&FDI)
Rev 1A
Date: Wednesday, April 23, 2014
Sheet 2 of 42

Haswell Processor (DDR3)

03



PROJECT :	TWK
	Quanta Computer Inc.
Size: Custom	Document Number: HAS 2/4 (DDR3 I/F) Rev: 1A
Date: Wednesday, April 23, 2014	Sheet 3 of 42

NB5

Haswell Processor (POWER)

POWER

04

+VCCIN 95A

U16F

+VCC_CORE

C221 22U/6.3VS_6 C590 22U/6.3VS_6 C166 22U/6.3VS_6
C607 22U/6.3VS_6 C585 22U/6.3VS_6 C151 22U/6.3VS_6
C584 22U/6.3VS_6 C608 22U/6.3VS_6 C589 22U/6.3VS_6
C563 22U/6.3VS_6 C220 22U/6.3VS_6 C152 22U/6.3VS_6
C598 22U/6.3VS_6 C574 22U/6.3VS_6 C597 22U/6.3VS_6
C575 22U/6.3VS_6 C196 22U/6.3VS_6 C165 22U/6.3VS_6
C197 22U/6.3VS_6 C599 22U/6.3VS_6 C222 22U/6.3VS_6
C576 *22U/6.3VS_6 C179 *22U/6.3VS_6 C588 22U/6.3VS_6
C564 22U/6.3VS_6 C583 22U/6.3VS_6 C609 10U/6.3V_6
C562 10U/6.3V_6 C140 10U/6.3V_6 C168 10U/6.3V_6

AA26 AA28 AA34 AA30 AA32 AB26 AB29 AB25 AB27 AB28 AB30 AB31 AB33 AB34 AB32 AC26 AB35 AC28 AD25 AC30 AD28 AC32 AD31 AC34 AD34 AD26 AD27 AD29 AD30 AD32 AD33 AD35 AE26 AE32 AE28 AE30 AG28 AG34 AE34 AF25 AF26 AF27 AF28 AF29 AF30 AF31 AF32 AF33 AF34 AF35 AG26 AH26 AH29 AG30 AG32 AH32 AH35 AH25 AH27 AH28 AH30 AH31 AH33 AH34 AJ25 AJ26 AJ27 AJ28 AJ29 AJ30 AJ31 AJ32 AJ33 AJ34 AJ35 G25 H25 J25 K25 L25 M25 N25 P25 R25 T25 U25 U26 V25 V26 W26 W27 Y25 Y26 Y27 Y28 Y29 Y30 Y31 Y32 Y33 Y34 Y35 K26 F25

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100 VCC101 VCC102 VCC103 VCC104

HSW_RPGA_EDS_PGA

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

+1.35VSUS 4.2A

+1.35VSUS

VDDQ1 AB11
VDDQ2 AB2
VDDQ3 AB5
VDDQ4 AB8
VDDQ5 AE11
VDDQ6 AE2
VDDQ7 AE5
VDDQ8 AE8
VDDQ9 AH11
VDDQ10 K11
VDDQ11 N11
VDDQ12 N8
VDDQ13 T11
VDDQ14 T2
VDDQ15 T5
VDDQ16 T8
VDDQ17 W11
VDDQ18 W2
VDDQ19 W5
VDDQ20 W8

C170 22U/6.3VS_6 C147 22U/6.3VS_6 C586 22U/6.3VS_6
C577 22U/6.3VS_6 C158 22U/6.3VS_6 C600 22U/6.3VS_6
C582 22U/6.3VS_6 C142 22U/6.3VS_6 C579 22U/6.3VS_6
C604 22U/6.3VS_6 C180 22U/6.3VS_6 C202 10U/6.3V_6
C587 10U/6.3V_6 C611 10U/6.3V_6 C215 10U/6.3V_6
C181 10U/6.3V_6 C592 10U/6.3V_6 C223 10U/6.3V_6
C167 10U/6.3V_6 C593 10U/6.3V_6 C150 10U/6.3V_6 + C154 *330U/2V_7343

RSVD K27
RSVD L27
RSVD T27
RSVD V27
RSVD N26
RSVD AL27
RSVD AK27
RSVD E17
RSVD W32
RSVD AL16
RSVD AL13
RSVD J27

VCCIO_OUT AN35 +VCCIO_OUT_R *0_1206/S R439 +VCCIO_OUT 300mA
VCCIO2PCH A23 +VCCIO_PCH_R *0.002/F_1206 R373 +VCCIO_PCH 300mA
VCOMP_OUT F22 +VCCIOA_OUT_R *0_1206/S R374 +VCCIOA_OUT
VSS_AP35 AP35

VIDALERT# AM28 H_CPU_SVIDALRT#
VIDSCLK AM29 H_CPU_SVIDCLK
VIDSOUT AL28 H_CPU_SVIDDAT
PWR_DEBUG H27 PWR_DEBUG_R TP3
0_4 R442

VSS AP34 AT34 AL22 AT33 AM21 AM25 AM22 AM20 AM24 AL19 AM23 AT32 AT35

RSVD_TP AM35 AR35 AR32 AL26

VCC_SENSE AL35 VCC_SENSE [37]
VSS_SENSE AK35 VSS_SENSE [37]
R431 100_4 +VCC_CORE
R429 100_4

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

+VCCIOA_OUT [2]
+VCCIO_OUT [2,37]
+VCCIO_PCH [10]
+1.5V [6,7,8,10,25,26,29,30,35]
+1.05V [2,7,9,10,29,34,41]
+VCC_CORE [37,38]
+VCCST [2]
+1.35VSUS [2,12,13,35,40]

HW Thrm Protect

+3VPCU

For 65 degree, 1.8v limit, (SW)

R377 20K/F_4

For 75 degree, 1.2v limit, (HW)

THRM_MOINTOR1 [31]

R376 100K_6 NTC

+1.05V +VCCST
R115 *0_8
C259 *10U/6.3V_6 C258 *10U/6.3V_6

+VCC_CORE
C2003 0.1U/10V_4 C2004 0.1U/10V_4

Add 0.1u for EMI request 0223 (PV)

Power Test Propose

+1.05V
R74 150/F_4
PWR_DEBUG_R
R71 *10K_4

+1.05V +VCCIO_OUT
R129 *0_8
C310 *4.7U/6.3V_6

+1.05V +VCCIO_PCH
R185 0_6
CRB 1.0 stuff
C367 *4.7U/6.3V_6

CPU VDDQ

Layout note: It is recommended to shield VIDSOUT signal by routing it in between the VIDSCLK and VIDALERT# signals.

SVID CLK

H_CPU_SVIDCLK VR_SVID_CLK [37]

SVID DATA

+VCCIO_OUT
Place PU resistor close to CPU
R143 130/F_4
H_CPU_SVIDDAT VR_SVID_DATA [37]

DG V0.7 -> 110 Ohm
SCH V0.7 -> 130 Ohm

Place PU resistor close to CPU
The VIDALERT# signal must have a damping resistor to prevent overshoot

SVID ALERT

C305 *0.1U/10V_4
+VCCIO_OUT R140 75/F_4
H_CPU_SVIDALRT# R141 43_4 VR_SVID_ALERT# [37]

DG V0.7 -> 44 Ohm
SCH V0.7 -> 43 Ohm

NB5

PROJECT : TWK
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HAS 3/4 (POWER)	1A

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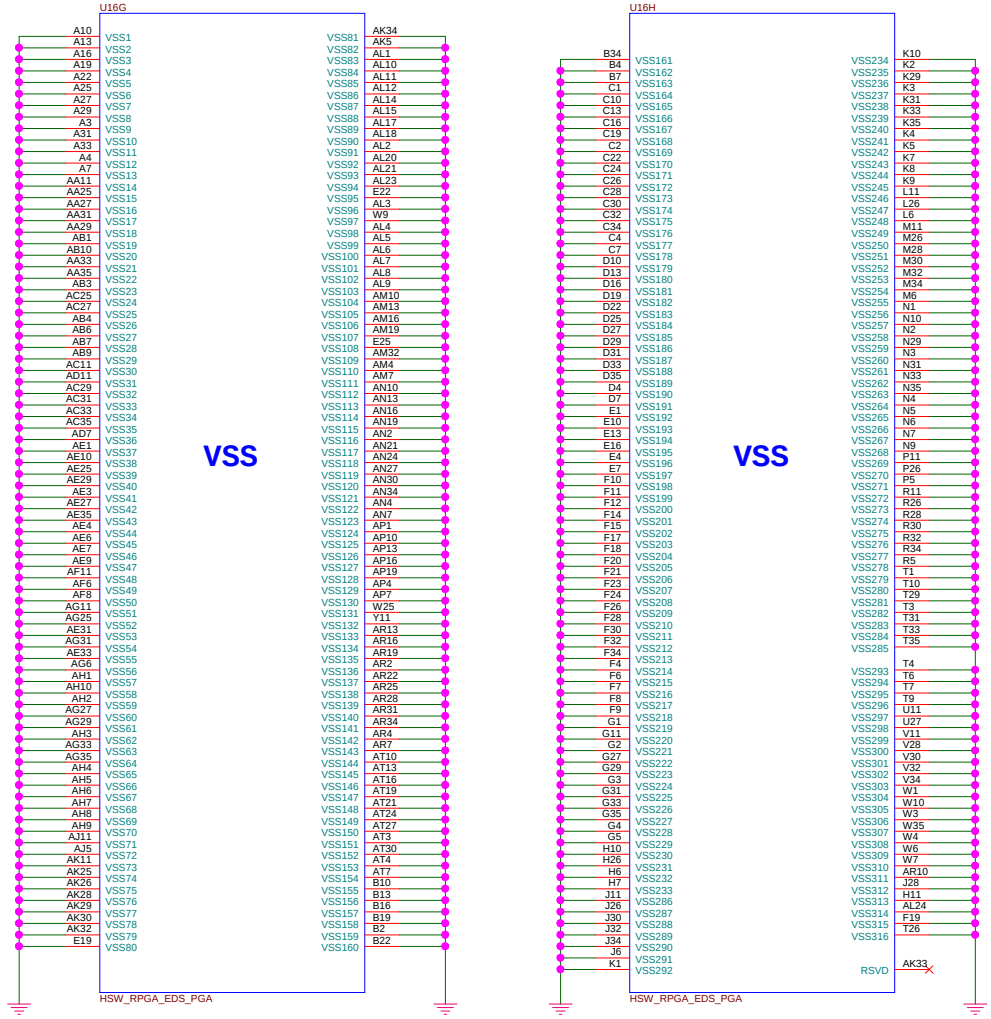
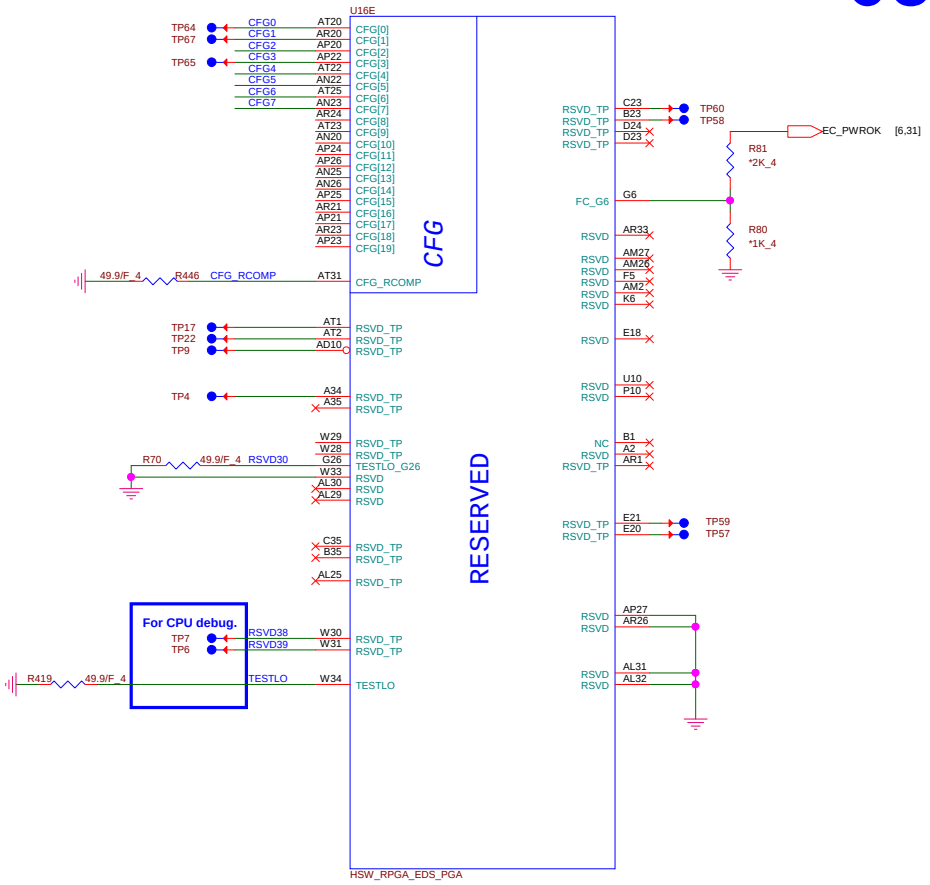
Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



05

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

CFG3 R458 *1K_4

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG2 R456 *1K_4
CFG4 R457 1K_4
CFG7 R460 *1K_4
CFG5 R459 1K_4
CFG6 R466 *1K_4

PROJECT : TWK
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	HAS 4/4 (GND)	1A

Date: Wednesday, April 23, 2014 Sheet 5 of 42

Lynx Point (DMI,FDI,PM)

U21C

DMI

FDI

System Power Management

LPT_PCH_M_EDS/BGA

5/16 for DS3

for DS3

DG V0.7 -> 33 ohm
SCH V0.7 -> 0 ohm

Reserve for power on sequence

Lynx Point (DDI)

U21D

LVDS

CRT

Digital Display Interface

INT. HDMI

PD Res place close to PCH

PCH to Res routeing 37.5 ohm Impedance.
Res to connector filter routeing 50ohm Impedance.

DAC_IREF (50ohm)
Trace length < 500 MILS
Trace spacing = 30 MILS

LPT_PCH_M_EDS/BGA

PCH Nut: QCI P/N: MBUL1001010 (Location:H13,H14)

PCH Pull-high/low(CLG)

for DS3

EDS V0.7 -> BATLOW# is in SUS well
SCH V0.7 -> BATLOW# pull up to DS3 power

DG V0.7 say that PWRBTN# is internal pulled-up in PCH to 3.3 V DSW through a weak pull-up resistor (24 kΩ nominal)

On Die DSW VR Enable

High = Enable (Default)
Low = Disable

System PWR_OK(CLG)

PROJECT	TWK
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: PCH 1/6 (DMI/FDI/VIDEO)
Rev: 1A	
Date: Wednesday, April 23, 2014	Sheet 6 of 42

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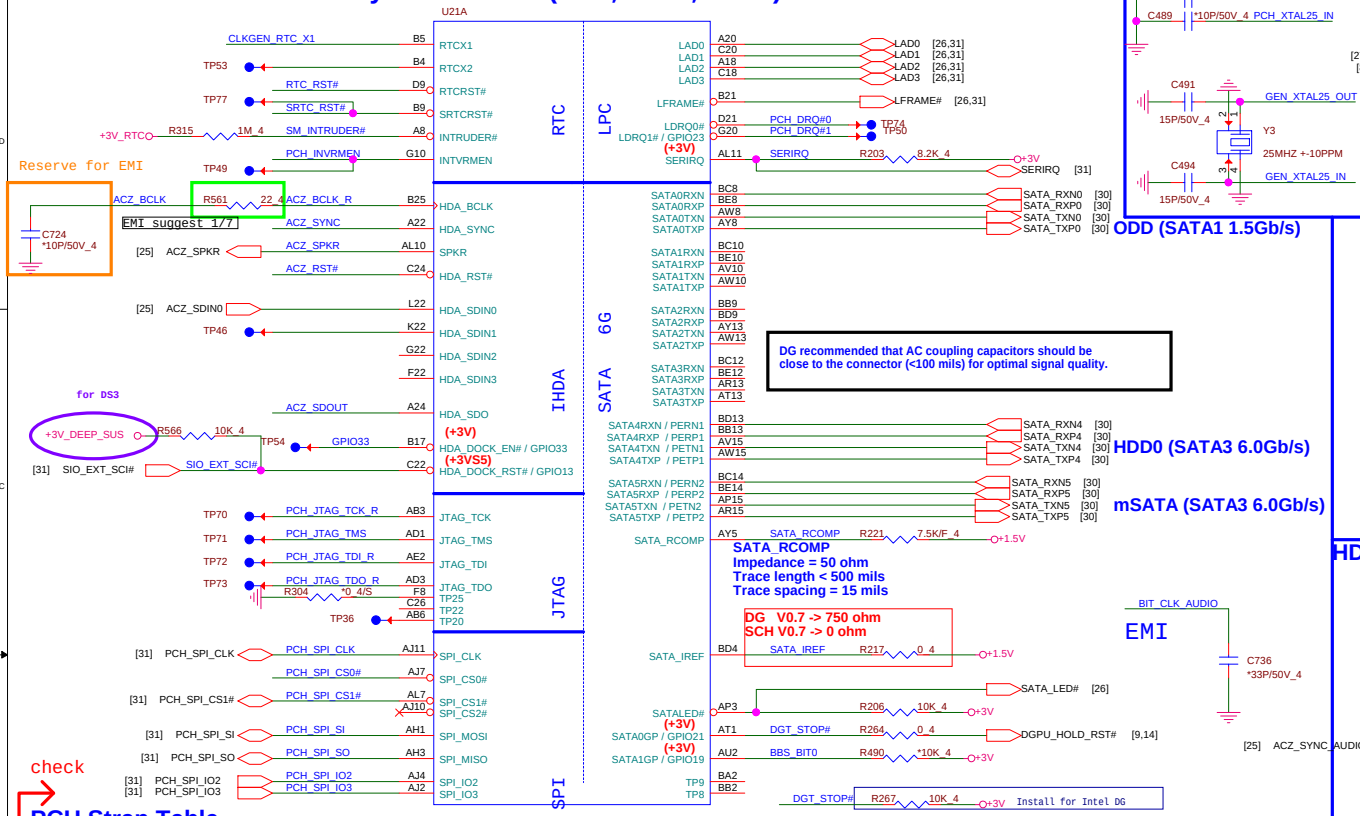
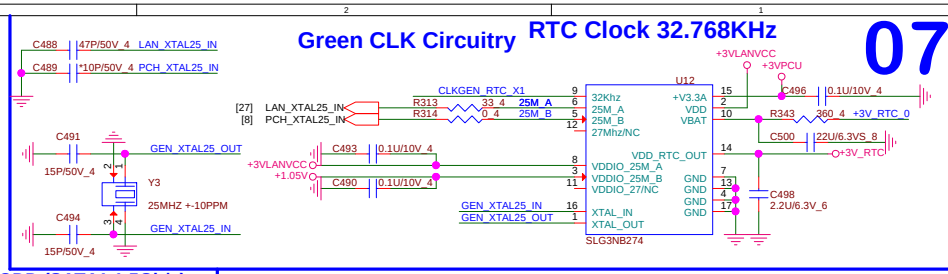
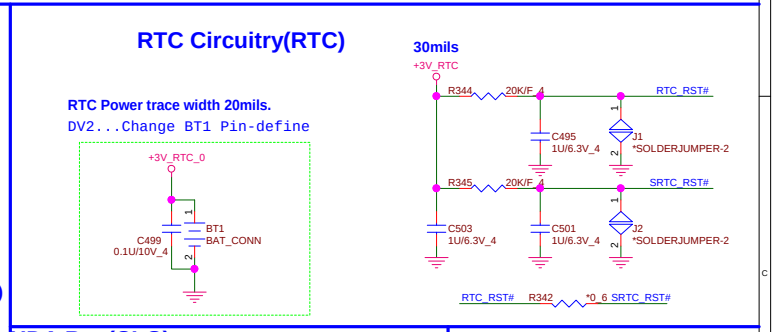
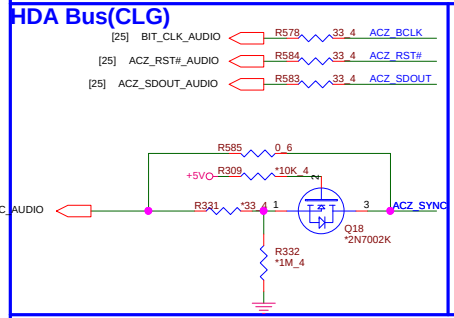
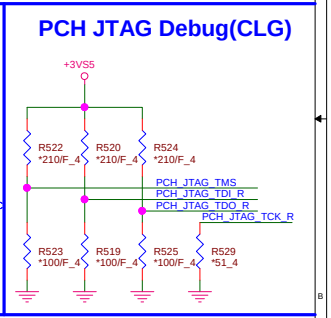
Lynx Point (HDA, JTAG, SATA)

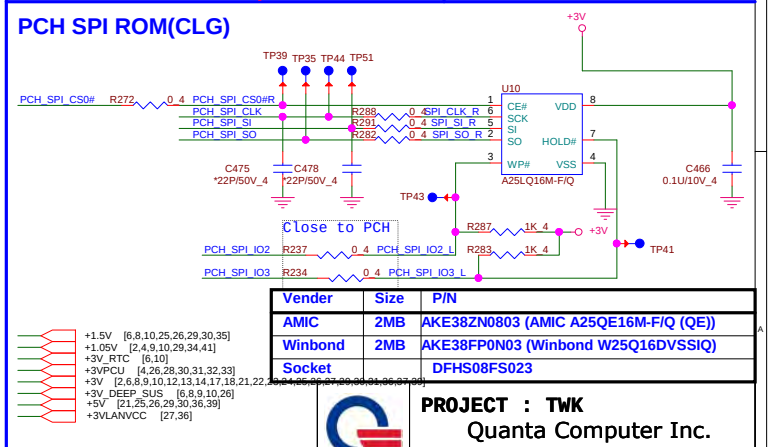












Vender	Size	P/N
AMIC	2MB	AKE38ZN0803 (AMIC A25QE16M-F/Q (QE))
Winbond	2MB	AKE38FP0N03 (Winbond W25Q16DVSSIQ)
Socket		DFHS08FS023

check

PCH Strap Table

LPT_PCH_M_EDS/BGA

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R227 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)	R241 *1K_4 PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable	PCH_INVRMEN R300 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 1 SPI; 0 0 LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R481 *1K_4 BBS_BIT0 R565 *1K_4 BBS_BIT1 [8]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R567 *1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overridden	[31] GPIO33_E ACZ_SDOUT R562 *1K_4 +VCC_HDA_IO
GPIO8	RSVD	RSMRST#	Internel PU	R531 *1K_4 BT_OFF# [9,26]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Int PU)	R536 *1K_4 PLL_ODVR_EN [9]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R231 *1K_4 +3V
SUSCLK / GPIO62	On-die PLL Voltage Regulator	PWROK	0 = Disable 1 = Enable (Int PU)	[6] PCH_SUSCLK_L R280 *1K_4 R274 *1K_4 +3V

NB5	PROJECT : TWK Quanta Computer Inc.		
Size: Custom	Document Number: PCH 2/6 (SATA/HDA/SPI)		Rev: 1A
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Lynx Point (PCI,USB,NVRAM)

Lynx Point (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

USB3.0

check

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

PCIE Clock

SMBus/Pull-up(CLG)

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

PROJECT :	TWK
	Quanta Computer Inc.
Size: Custom	Document Number: PCH 3/6 (PCIE/USB/CLK)
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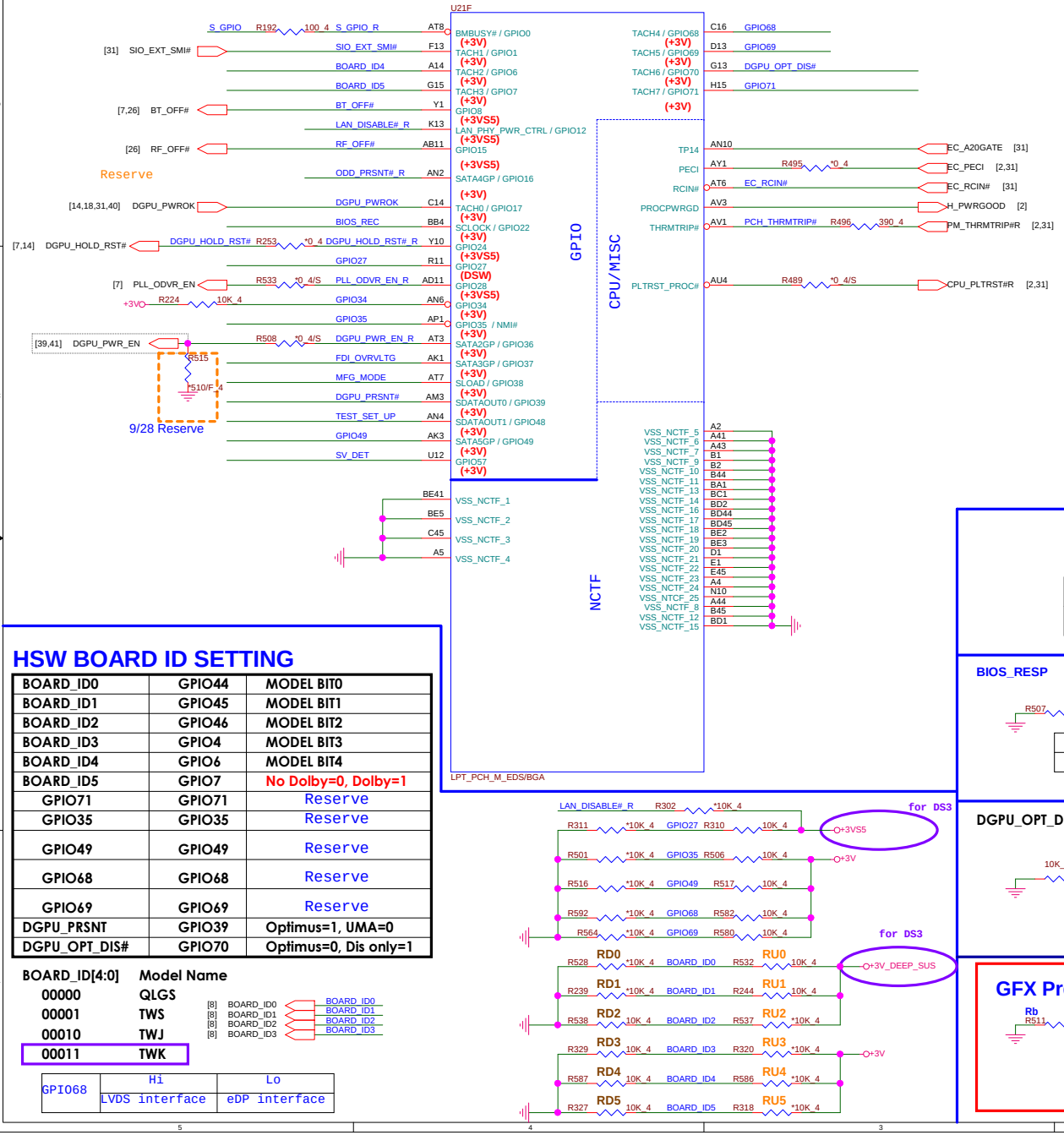
NB5

Lynx Point (GPIO,VSS_NCTF,RSVD)



HSW BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO45	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO4	MODEL BIT3
BOARD_ID4	GPIO6	MODEL BIT4
BOARD_ID5	GPIO7	No Dolby=0, Dolby=1
GPIO71	GPIO71	Reserve
GPIO35	GPIO35	Reserve
GPIO49	GPIO49	Reserve
GPIO68	GPIO68	Reserve
GPIO69	GPIO69	Reserve
DGPU_PRSNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

BOARD_ID[4:0]	Model Name
00000	QLGS
00001	TWS
00010	TWJ
00011	TWK

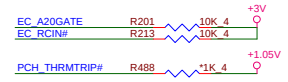
[8] BOARD_ID0 BOARD_ID0
[8] BOARD_ID1 BOARD_ID1
[8] BOARD_ID2 BOARD_ID2
[8] BOARD_ID3 BOARD_ID3

GPIO68	Hi	Lo
	LVDS interface	eDP interface

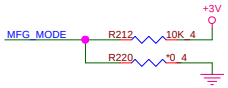
09

+3V_DEEP_SUS [6,7,8,10,26]
+3VS5 [2,6,7,10,26,28,29,31,33,35,36,41]
+3V [2,6,7,8,10,12,13,14,17,18,21,22,23,24,25,26,27,29,30,31,36,37,39]
+5VS5 [25,28,29,33,34,35,36,37,38,39,40]

PCH MISC PU /PD

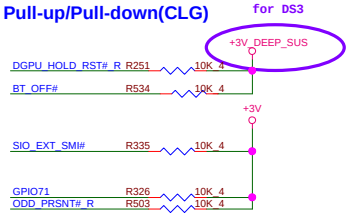


MFG-TEST



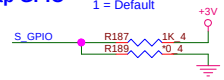
GPIO Pull-up/Pull-down(CLG)

for DS3

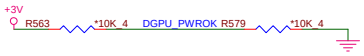


Swap GPIO

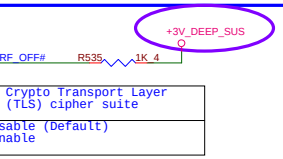
0 = SGPIO
1 = Default

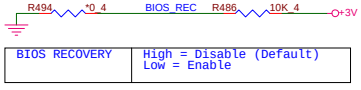


DGPU_PWROK UMA=0

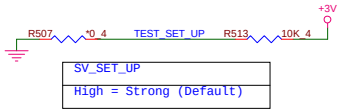


for DS3



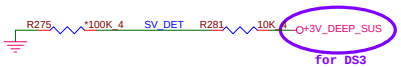


BIOS_RESP

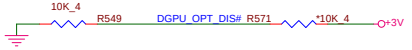


SV Detect

0 = SV Detect
1 = Default

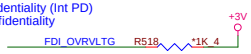


DGPU_OPT_DIS# GPIO70 Optimus=0, Dis only=1

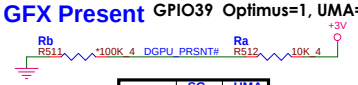


SATA3GP/GPIO37 TLS Confidentiality

0 = TLS no confidentiality (Int PD)
1 = TLS with confidentiality

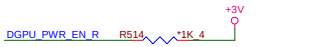


GFX Present GPIO39 Optimus=1, UMA=0



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

GPIO36 Internal PD



NB5

PROJECT : TWK
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
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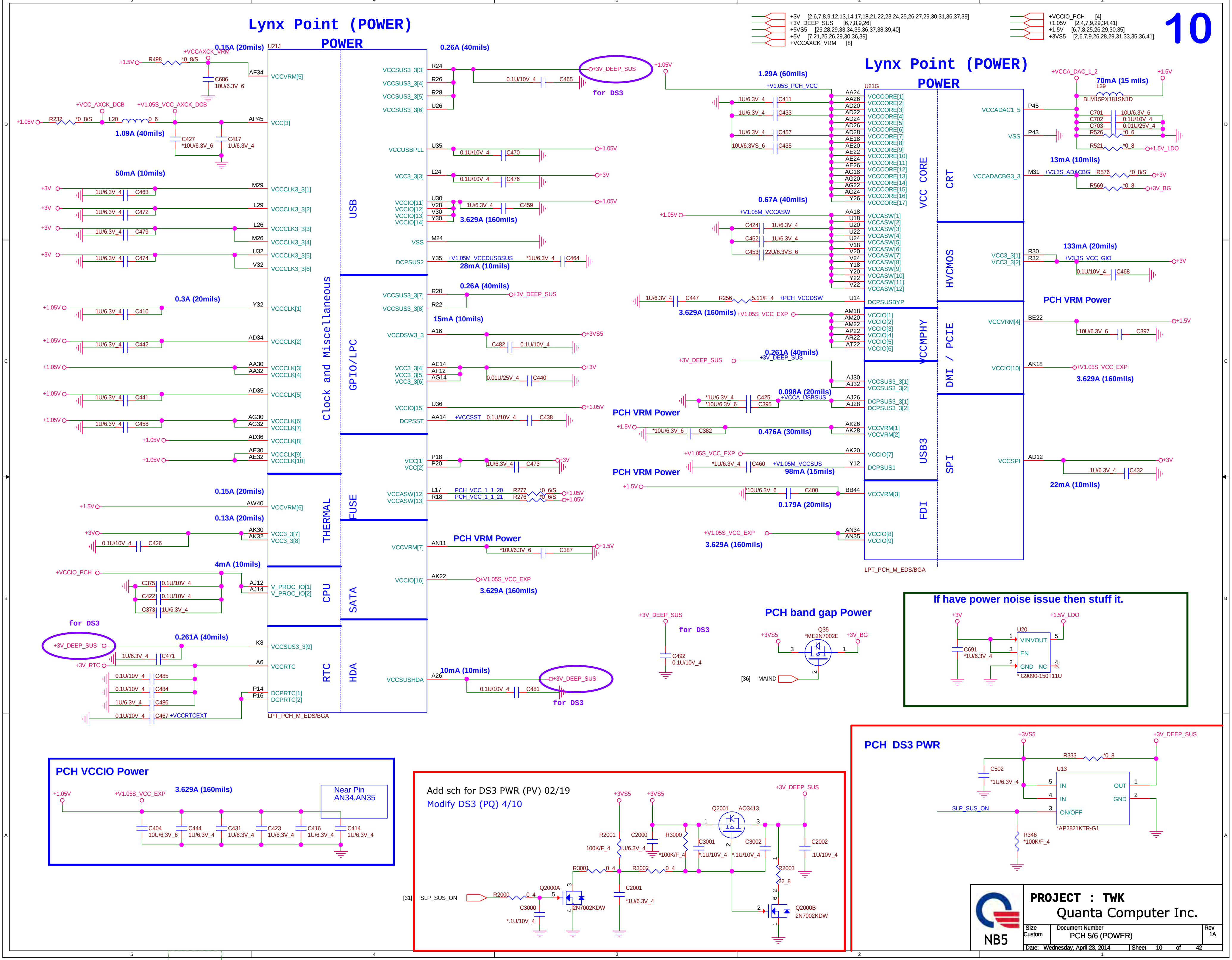
10
Lynx Point (POWER)
POWER
U21J
+3V [2,6,7,8,9,12,13,14,17,18,21,22,23,24,25,26,27,29,30,31,36,37,39]
+3V_DEEP_SUS [6,7,8,9,26]
+5VS5 [25,28,29,33,34,35,36,37,38,39,40]
+5V [7,21,25,26,29,30,36,39]
+VCCAXCK_VRM [8]
+VCCIO_PCH [4]
+1.05V [2,4,7,9,29,34,41]
+1.5V [6,7,8,25,26,29,30,35]
+3VS5 [2,6,7,9,26,28,29,31,33,35,36,41]
Clock and Miscellaneous
USB
GPIO/LPC
FUSE
THERMAL
SATA
CPU
RTC
HDA
U21G
VCC CORE
CRT
HVCMOS
VCCMPHY
DMI / PCIE
USB3
SPI
FDI
PCH VRM Power
PCH band gap Power
If have power noise issue then stuff it.
for DS3
LPT_PCH_M_EDS/BGA
PCH VCCIO Power
3.629A (160mils)
Near Pin AN34,AN35
Add sch for DS3 PWR (PV) 02/19
Modify DS3 (PQ) 4/10
PCH DS3 PWR
SLP_SUS_ON
*AP2821KTR-G1
*G9090-150T11U
AO3413
2N7002KDW
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Quanta Computer Inc.
NB5
Size Custom
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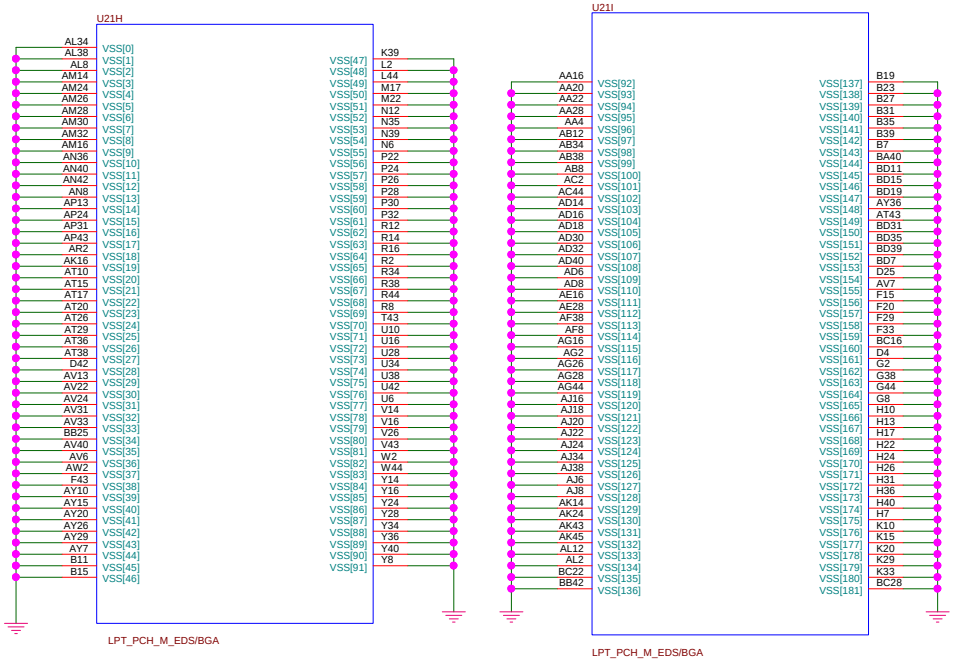
Lynx Point (GND)



PROJECT : TWK

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

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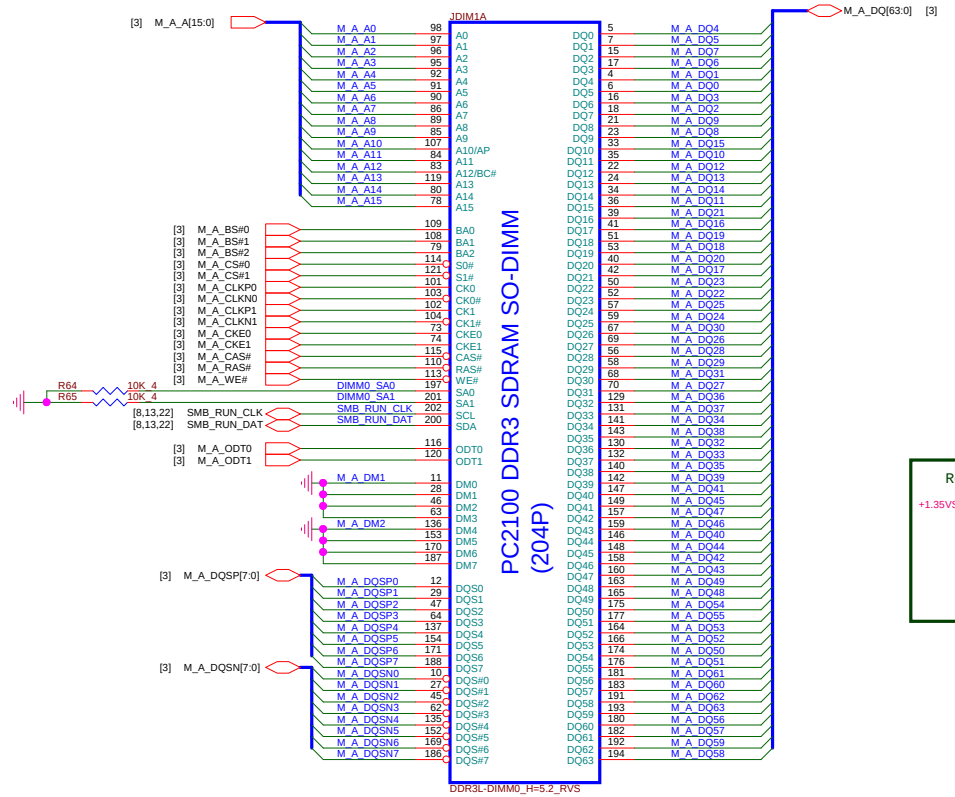
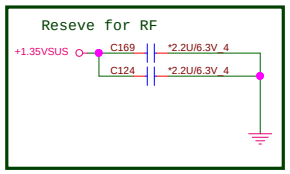
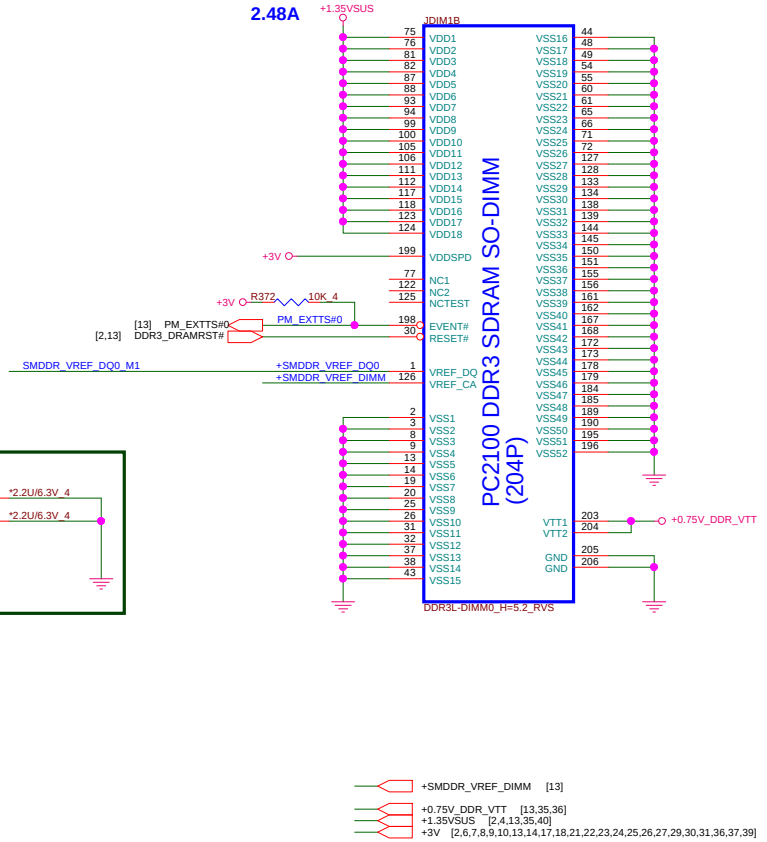
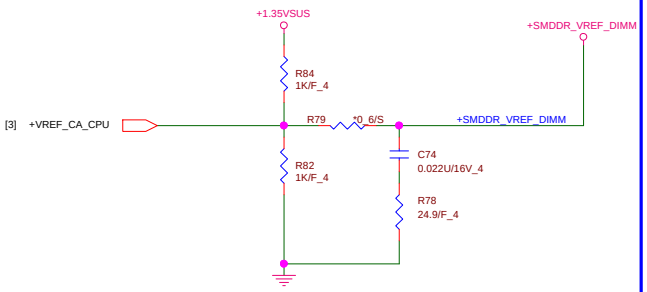




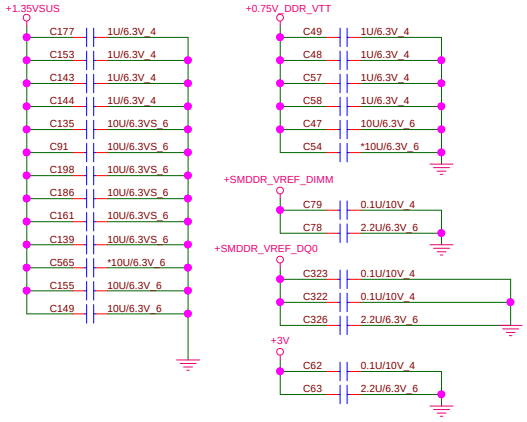
2.48A



10/4 : INTEL suggestion



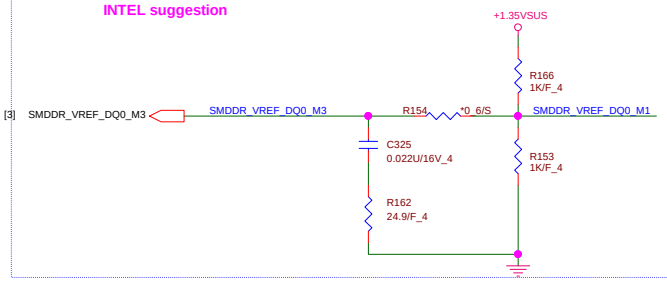
Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution

Place these Caps near So-Dimm0.

INTEL suggestion



NB5

PROJECT : TWK

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

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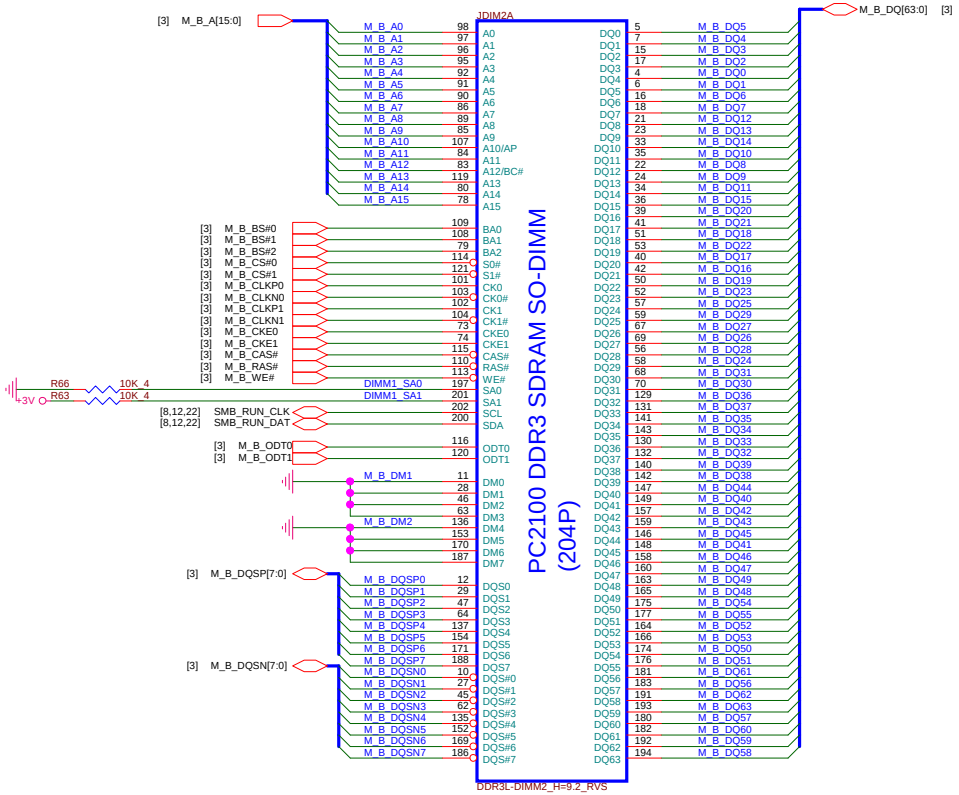
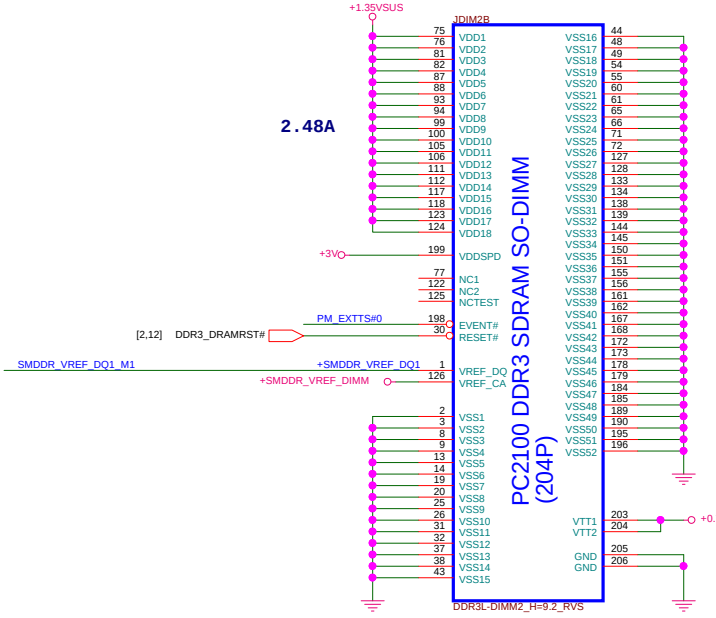
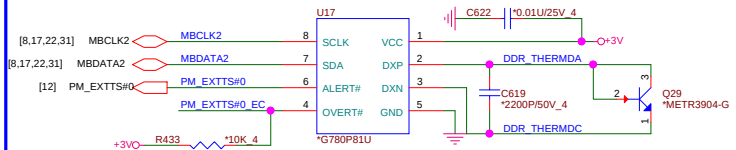


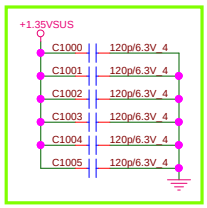


+0.75V_DDR_VTT [12,35,36]
+1.35VSUS [2,4,12,35,40]
+3V [2,6,7,8,9,10,12,14,17,18,21,22,23,24,25,26,27,29,30,31,36,37,39]
+SMDDR_VREF_DIMM [12]

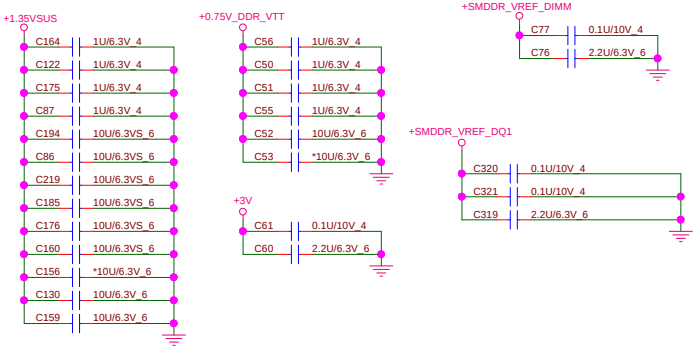
DDR3 Thermal Sensor



EMI add C1000~C1005 for b stage 1/3



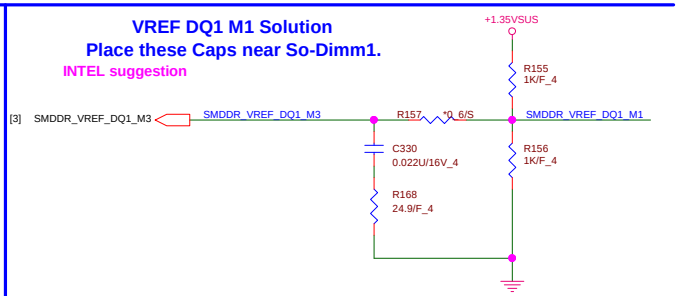
Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution

Place these Caps near So-Dimm1.

INTEL suggestion



PROJECT : TWK

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	DDR3L DIMM1-RVS (9.2H)	1A

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U18A
N15P-GX

PEX_IOVDD/Q : 3300mA
+1.05V_GFX
To be placed no further from the GPU than bewteen the PS and GPU
C282 22U/6.3VS_6
C295 22U/6.3VS_6
C630 22U/6.3VS_6
C293 22U/6.3VS_6
C229 10U/6.3VS_6
C228 10U/6.3VS_6
C294 10U/6.3VS_6
C634 10U/6.3VS_6
PLACE NEAR BALLS
C288 1U/6.3V_4
C629 1U/6.3V_4
C633 1U/6.3V_4
C267 1U/6.3V_4
PLACE UNDER BGA
C276 4.7U/6.3V_6
C251 4.7U/6.3V_6

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6
AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

[PEG Interface]

PEX_RX0 AN12 PEG_TX0 [2]
PEX_RX0_N AM12 PEG_TX#0 [2]
PEX_RX1 AN14 PEG_TX1 [2]
PEX_RX1_N AM14 PEG_TX#1 [2]
PEX_RX2 AP14 PEG_TX2 [2]
PEX_RX2_N AP15 PEG_TX#2 [2]
PEX_RX3 AN15 PEG_TX3 [2]
PEX_RX3_N AM15 PEG_TX#3 [2]
PEX_RX4 AN17 PEG_TX4 [2]
PEX_RX4_N AM17 PEG_TX#4 [2]
PEX_RX5 AP17 PEG_TX5 [2]
PEX_RX5_N AP18 PEG_TX#5 [2]
PEX_RX6 AN18 PEG_TX6 [2]
PEX_RX6_N AM18 PEG_TX#6 [2]
PEX_RX7 AN20 PEG_TX7 [2]
PEX_RX7_N AM20 PEG_TX#7 [2]
PEX_RX8 AP20
PEX_RX8_N AP21
PEX_RX9 AN21
PEX_RX9_N AM21
PEX_RX10 AN23
PEX_RX10_N AM23
PEX_RX11 AP23
PEX_RX11_N AP24
PEX_RX12 AN24
PEX_RX12_N AM24
PEX_RX13 AN26
PEX_RX13_N AM26
PEX_RX14 AP26
PEX_RX14_N AP27
PEX_RX15 AN27
PEX_RX15_N AM27

PEX_TX0 AK14 C_PEG_RX0 C210 0.22U/10V_4 PEG_RX0 [2]
PEX_TX0_N AJ14 C_PEG_RX#0 C204 0.22U/10V_4 PEG_RX#0 [2]
PEX_TX1 AH14 C_PEG_RX1 C201 0.22U/10V_4 PEG_RX1 [2]
PEX_TX1_N AG14 C_PEG_RX#1 C190 0.22U/10V_4 PEG_RX#1 [2]
PEX_TX2 AK15 C_PEG_RX2 C226 0.22U/10V_4 PEG_RX2 [2]
PEX_TX2_N AJ15 C_PEG_RX#2 C234 0.22U/10V_4 PEG_RX#2 [2]
PEX_TX3 AL16 C_PEG_RX3 C224 0.22U/10V_4 PEG_RX3 [2]
PEX_TX3_N AK16 C_PEG_RX#3 C214 0.22U/10V_4 PEG_RX#3 [2]
PEX_TX4 AK17 C_PEG_RX4 C253 0.22U/10V_4 PEG_RX4 [2]
PEX_TX4_N AJ17 C_PEG_RX#4 C266 0.22U/10V_4 PEG_RX#4 [2]
PEX_TX5 AH17 C_PEG_RX5 C236 0.22U/10V_4 PEG_RX5 [2]
PEX_TX5_N AG17 C_PEG_RX#5 C250 0.22U/10V_4 PEG_RX#5 [2]
PEX_TX6 AK18 C_PEG_RX6 C278 0.22U/10V_4 PEG_RX6 [2]
PEX_TX6_N AJ18 C_PEG_RX#6 C283 0.22U/10V_4 PEG_RX#6 [2]
PEX_TX7 AL19 C_PEG_RX7 C271 0.22U/10V_4 PEG_RX7 [2]
PEX_TX7_N AK19 C_PEG_RX#7 C277 0.22U/10V_4 PEG_RX#7 [2]
PEX_TX8 AK20
PEX_TX8_N AJ20
PEX_TX9 AH20
PEX_TX9_N AG20
PEX_TX10 AK21
PEX_TX10_N AJ21
PEX_TX11 AL22
PEX_TX11_N AK22
PEX_TX12 AK23
PEX_TX12_N AJ23
PEX_TX13 AH23
PEX_TX13_N AG23
PEX_TX14 AK24
PEX_TX14_N AJ24
PEX_TX15 AL25
PEX_TX15_N AK25

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

PEX_REFCLK AL13 CLK_PCIE_VGA [8]
PEX_REFCLK_N AK13 CLK_PCIE_VGA# [8]

PEX_TSTCLK_OUT AJ26 PEX_TSTCLK R440 *200_4
PEX_TSTCLK_OUT_N AK26 PEX_TSTCLK#

PEX_WAKE AJ11
PEX_RST_N AJ12 VGA_RST# R417 *0_4/S PEGX_RST#

PEX_CLKREQ_N AK12 PEX_CLKREQ# R428 10K_4 +3V_GFX

PEX_TERMP AP29 PEX_TERMP R464 2.49K/F_4

TESTMODE AK11 TESTMODE R418 10K_4

PEX_PLLVDD AG26 PEX_PLLVDD PEX_PLLVDD : 150mA
PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
PEX_SVDD_3V3 : 210mA
0.1U/10V_4 C209
4.7U/6.3V_6 C217
4.7U/6.3V_6 C131
PLACE NEAR BGA
+3V_GFX

3.3V_AUX_NC P8

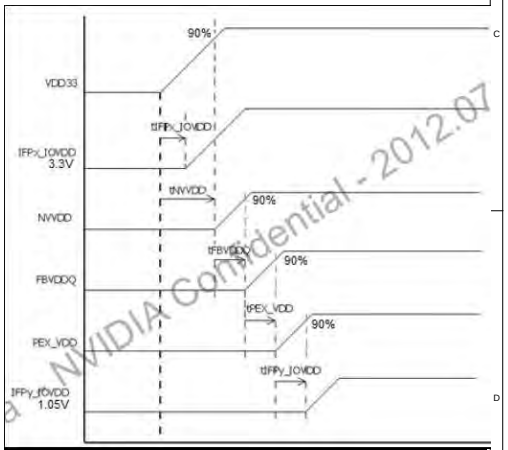
VDD_SENSE L4 VGPU_CORE_SENSE [39]

GND_SENSE L5 VSS_GPU_SENSE [39]

+1.05V_GFX
R134 *0_6
L15 BLM15PX330SN1D
C307 4.7U/6.3V_6
C309 1U/6.3V_4
C308 0.1U/10V_4
PLACE NEAR BGA CLOSE TO CAPS
PLACE UNDER BGA
PLACE NEAR BALLS

VDD33 : 85mA
+3V_GFX
J8 VDD33_1
K8 VDD33_2
L8 VDD33_3
M8 VDD33_4
PLACE CLOSE TO BGA
C207 4.7U/6.3V_6
C187 2.2U/6.3V_4
PLACE CLOSE TO GPU BALLS
C188 1U/6.3V_4
C191 0.1U/10V_4
C189 0.1U/10V_4
C208 0.1U/10V_4

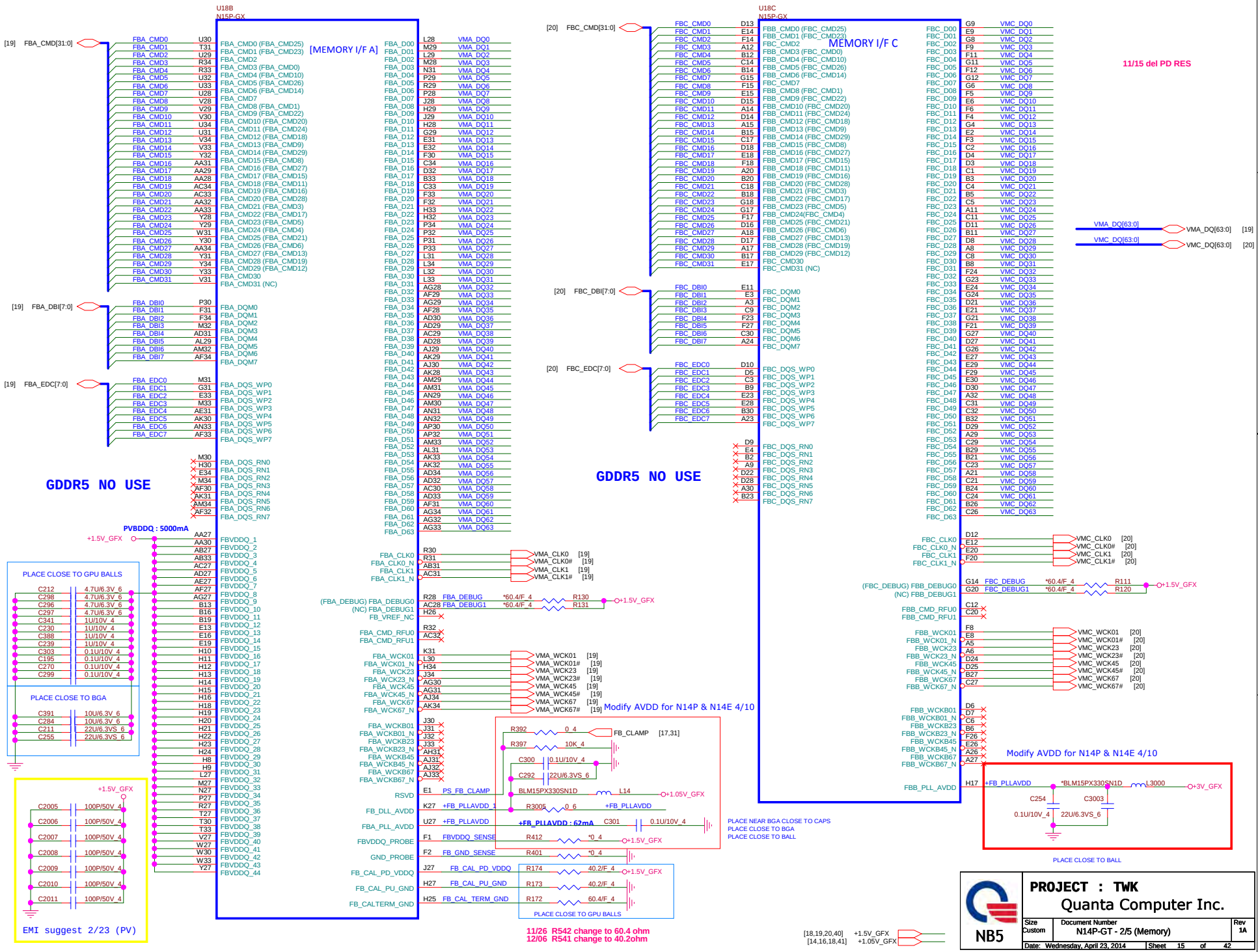
+3V_GFX R427 4.7K_4
[9,18,31,40] DGPU_PWROK
Q27 DTC144EUA
PEX_CLKREQ# Q28 *DTC144EUA
CLK_PEGA_REQ# [8]
+3V
U4 MC74VHC1G08DFT2G
C273 0.1U/10V_4
[2,8,24,26,27,31] PLTRST#
[7,9] DGPU_HOLD_RST#
PEGX_RST# [17]
R114 100K_4

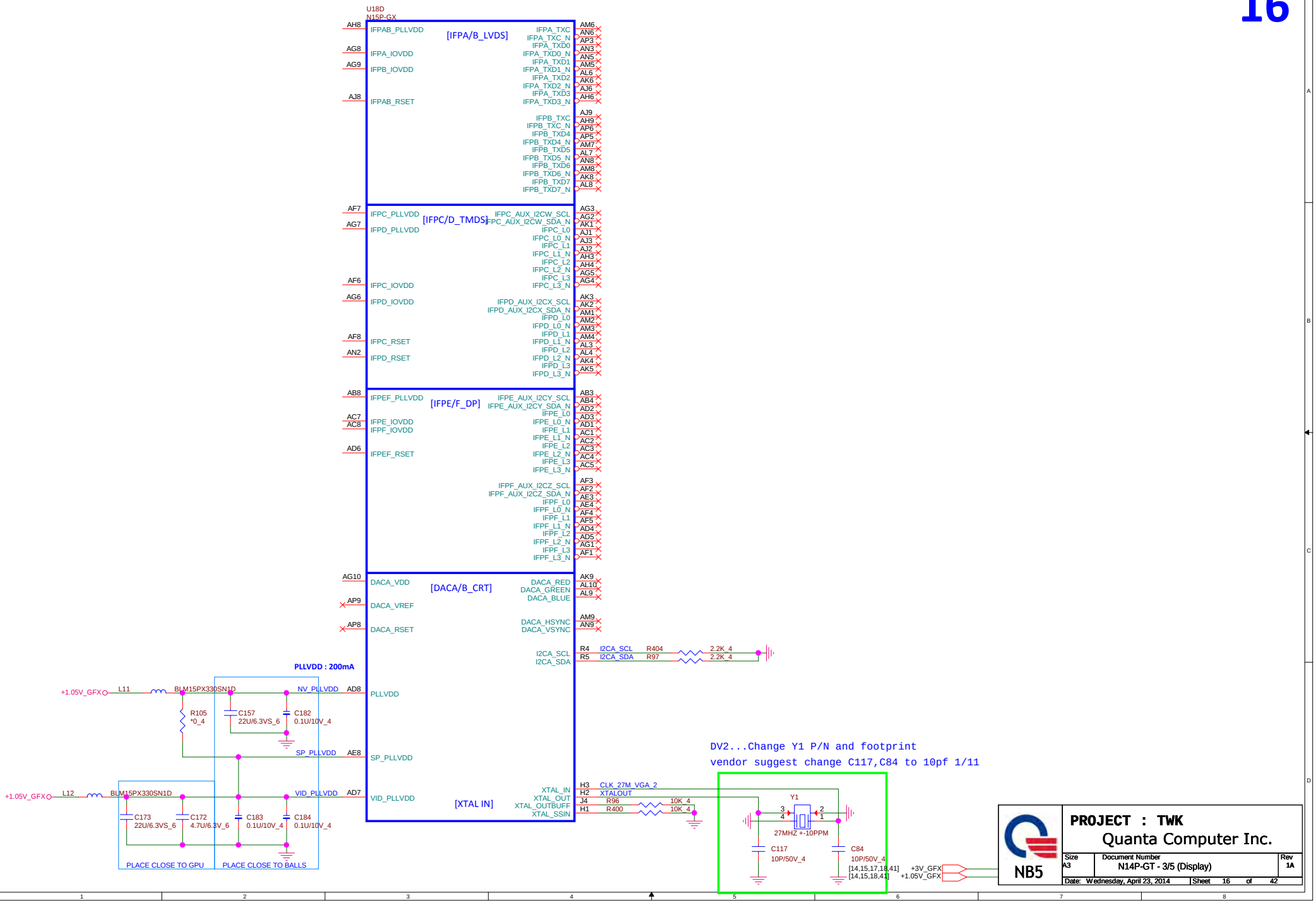


[15,17,18,41] +3V_GFX
[15,18,19,20,40] +1.5V_GFX
[15,16,18,41] +1.05V_GFX
[2,6,7,8,9,10,12,13,17,18,21,22,23,24,25,26,27,29,30,31,36,37,39] +3V

NB5

PROJECT : TWK
Quanta Computer Inc.
Size A3 | Document Number N14P-GT - 1/5 (PCIE) | Rev 1A
Date: Wednesday, April 23, 2014 | Sheet 14 of 42


U18B
N15P-GX
[MEMORY I/F A]
GDDR5 NO USE
PVBDDQ : 5000mA
PLACE CLOSE TO GPU BALLS
PLACE CLOSE TO BGA
EMI suggest 2/23 (PV)
U18C
N15P-GX
MEMORY I/F C
GDDR5 NO USE
11/15 del PD RES
Modify AVDD for N14P & N14E 4/10
PLACE NEAR BGA CLOSE TO CAPS
PLACE CLOSE TO BGA
PLACE CLOSE TO BALL
PLACE CLOSE TO GPU BALLS
11/26 R542 change to 60.4 ohm
12/06 R541 change to 40.2ohm
PROJECT : TWK
Quanta Computer Inc.
NB5
N14P-GT - 2/5 (Memory)
Wednesday, April 23, 2014


U18D
N15P-GX
[IFPA/B_LVDS]
IFPAB_PLLVDD
IFPA_IOVDD
IFPB_IOVDD
IFPAB_RSET
IFPA_TXC
IFPA_TXC_N
IFPA_TXD0
IFPA_TXD0_N
IFPA_TXD1
IFPA_TXD1_N
IFPA_TXD2
IFPA_TXD2_N
IFPA_TXD3
IFPA_TXD3_N
IFPB_TXC
IFPB_TXC_N
IFPB_TXD4
IFPB_TXD4_N
IFPB_TXD5
IFPB_TXD5_N
IFPB_TXD6
IFPB_TXD6_N
IFPB_TXD7
IFPB_TXD7_N
[IFPC/D_TMDS]
IFPC_PLLVDD
IFPD_PLLVDD
IFPC_IOVDD
IFPD_IOVDD
IFPC_RSET
IFPD_RSET
IFPC_AUX_I2CW_SCL
IFPC_AUX_I2CW_SDA_N
IFPC_L0
IFPC_L0_N
IFPC_L1
IFPC_L1_N
IFPC_L2
IFPC_L2_N
IFPC_L3
IFPC_L3_N
IFPD_AUX_I2CX_SCL
IFPD_AUX_I2CX_SDA_N
IFPD_L0
IFPD_L0_N
IFPD_L1
IFPD_L1_N
IFPD_L2
IFPD_L2_N
IFPD_L3
IFPD_L3_N
[IFPE/F_DP]
IFPEF_PLLVDD
IFPE_IOVDD
IFPF_IOVDD
IFPEF_RSET
IFPE_AUX_I2CY_SCL
IFPE_AUX_I2CY_SDA_N
IFPE_L0
IFPE_L0_N
IFPE_L1
IFPE_L1_N
IFPE_L2
IFPE_L2_N
IFPE_L3
IFPE_L3_N
IFPF_AUX_I2CZ_SCL
IFPF_AUX_I2CZ_SDA_N
IFPF_L0
IFPF_L0_N
IFPF_L1
IFPF_L1_N
IFPF_L2
IFPF_L2_N
IFPF_L3
IFPF_L3_N
[DACA/B_CRT]
DACA_VDD
DACA_VREF
DACA_RSET
DACA_RED
DACA_GREEN
DACA_BLUE
DACA_HSYNC
DACA_VSYNC
I2CA_SCL
I2CA_SDA
R4 I2CA_SCL R404 2.2K_4
R5 I2CA_SDA R97 2.2K_4
PLLVDD : 200mA
+1.05V_GFX
L11 BLM15PX330SN1D
NV_PLLVDD
PLLVDD
R105 *0_4
C157 22U/6.3VS_6
C182 0.1U/10V_4
SP_PLLVDD
L12 BLM15PX330SN1D
VID_PLLVDD
C173 22U/6.3VS_6
C172 4.7U/6.3V_6
C183 0.1U/10V_4
C184 0.1U/10V_4
PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS
[XTAL IN]
XTAL_IN
XTAL_OUT
XTAL_OUTBUFF
XTAL_SSIN
CLK_27M_VGA_2
XTALOUT
R96 10K_4
R400 10K_4
DV2...Change Y1 P/N and footprint
vendor suggest change C117,C84 to 10pf 1/11
Y1
27MHZ +-10PPM
C117 10P/50V_4
C84 10P/50V_4
[14,15,17,18,41] +3V_GFX
[14,15,18,41] +1.05V_GFX
NB5
PROJECT : TWK
Quanta Computer Inc.
Size A3
Document Number N14P-GT - 3/5 (Display)
Rev 1A
Date: Wednesday, April 23, 2014
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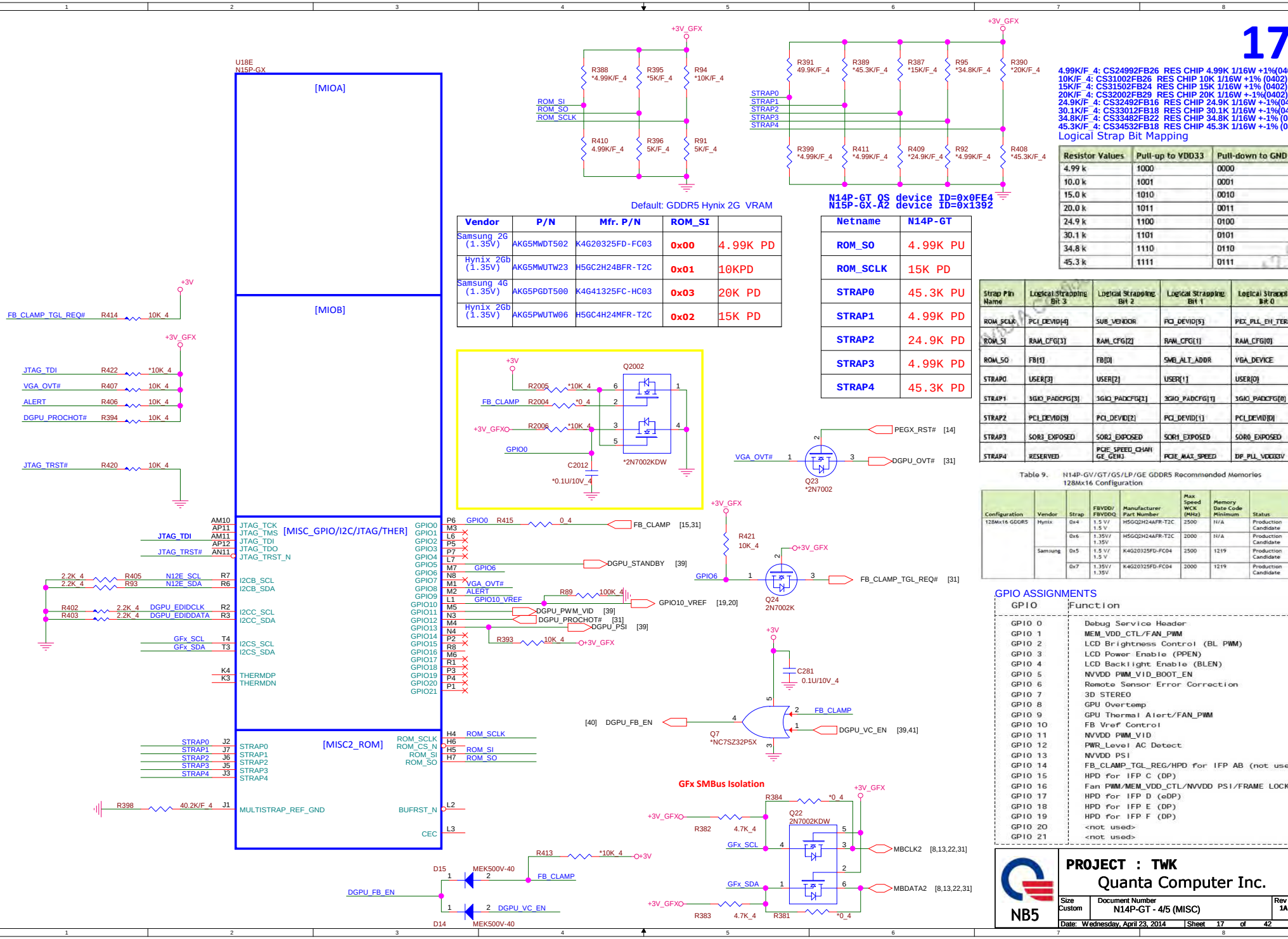

Vendor	P/N	Mfr. P/N	ROM_SI	
Samsung 2G (1.35V)	AKG5MWDT502	K4G20325FD-FC03	0x00	4.99K PD
Hynix 2Gb (1.35V)	AKG5MWUTW23	H5GC2H24BFR-T2C	0x01	10KPD
Samsung 4G (1.35V)	AKG5PGDT500	K4G41325FC-HC03	0x03	20K PD
Hynix 2Gb (1.35V)	AKG5PWUTW06	H5GC4H24MFR-T2C	0x02	15K PD

Netname	N14P-GT
ROM_SO	4.99K PU
ROM_SCLK	15K PD
STRAP0	45.3K PU
STRAP1	4.99K PD
STRAP2	24.9K PD
STRAP3	4.99K PD
STRAP4	45.3K PD

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EH_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHAN GE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Table 9. N14P-GV/GT/GS/LP/GE GDDR5 Recommended Memories
128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x4	1.5 V/ 1.5 V	H5GQ2H24AFR-T2C	2500	N/A	Production Candidate
		0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	K4G20325FD-FC04	2500	1219	Production Candidate
		0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Production Candidate

GPIO ASSIGNMENTS

GPIO	Function
GPIO 0	Debug Service Header
GPIO 1	MEM_VDD_CTL/FAN_PWM
GPIO 2	LCD Brightness Control (BL PWM)
GPIO 3	LCD Power Enable (PPEN)
GPIO 4	LCD Backlight Enable (BLEN)
GPIO 5	NVVDD PWM_VID_BOOT_EN
GPIO 6	Remote Sensor Error Correction
GPIO 7	3D STEREO
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert/FAN_PWM
GPIO 10	FB Vref Control
GPIO 11	NVVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	NVVDD PSI
GPIO 14	FB_CLAMP_TGL_REG/HPD for IFP AB (not used)
GPIO 15	HPD for IFP C (DP)
GPIO 16	Fan PWM/MEM_VDD_CTL/NVVDD PSI/FRAME LOCK
GPIO 17	HPD for IFP D (eDP)
GPIO 18	HPD for IFP E (DP)
GPIO 19	HPD for IFP F (DP)
GPIO 20	<not used>
GPIO 21	<not used>

NB5

PROJECT : TWK
Quanta Computer Inc.

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Custom	N14P-GT - 4/5 (MISC)	1A
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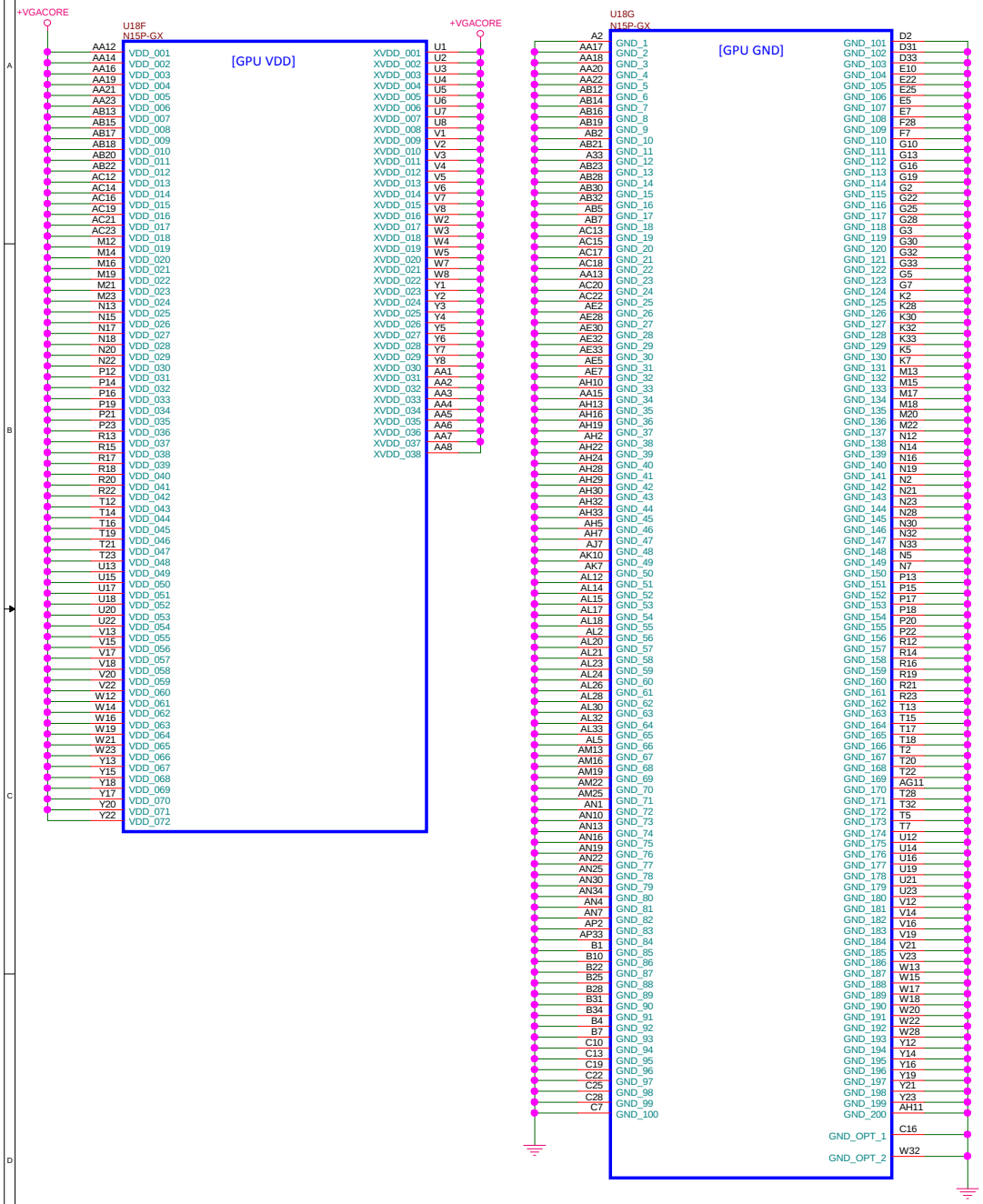
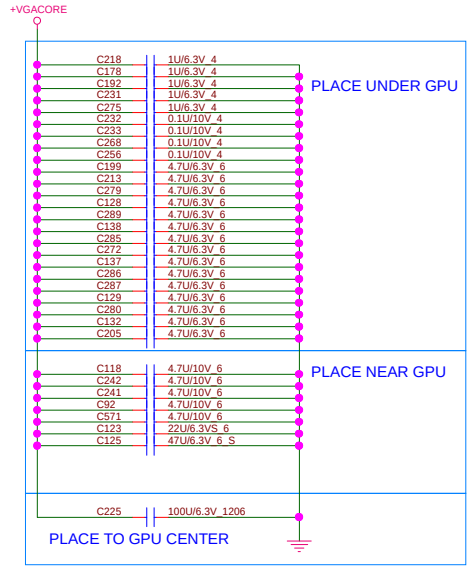
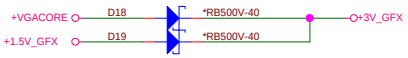
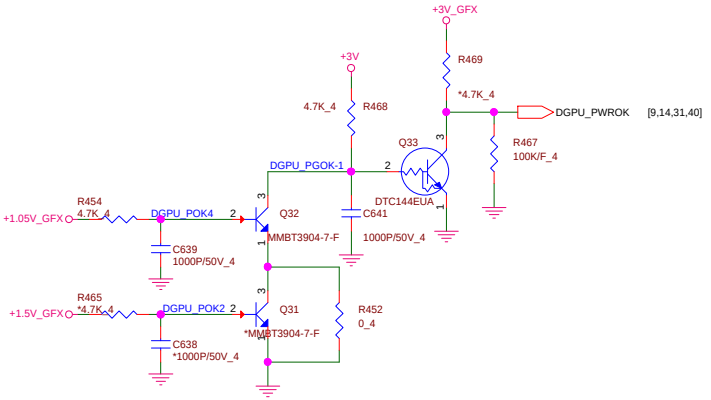
VDD/XVDD : 25.72A





for meet Power down sequence for +3V_GFX





[39] +VGACORE
[14,15,16,41] +1.05V_GFX
[15,19,20,40] +1.5V_GFX
[14,15,17,41] +3V_GFX
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,29,30,31,36,37,39] +3V

NB5

PROJECT : TWK

Quanta Computer Inc.

Size	Document Number	Rev
Custom	N14P-GT - 5/5 (Power)	1A

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CHANNEL A: 1024MB GDDR5x32

[15] VMA_DQ[63..0] — VMA_DQ[63..0]
[15] FBA_CMD[31:0] — FBA_CMD[31:0]
[15] FBA_DBI[7..0] — FBA_DBI[7..0]
[15] FBA_EDC[7..0] — FBA_EDC[7..0]

Channel 0 <0-31>
MF=0 Non-mirrored

QD16~23

QD0~7

Channel 0 <32-63>
MF=1 Mirrored

QD8~15

QD24~31

Channel 1 <0-31>
MF=0 Non-mirrored

QD48~55

QD32~39

Channel 1 <32-63>
MF=1 Mirrored

QD40~47

QD56~63

VREFD_VMA1 0.4MM=16mils
VREFC_VMA1 0.4MM=16mils
VREFD_VMA2 0.4MM=16mils
VREFC_VMA2 0.4MM=16mils

11/26 change to 100U_1206 *2

FBVDDQ_MEM
1 X 10uF
4 X 1uF
6 X 0.1uF

FBVDD
1 X 10uF
4 X 1uF

CKE* is strap pin to set ODT value of memory chip

RST PD place @ the end of daisy-chain.

GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A8_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

NB5

PROJECT : TWK
Quanta Computer Inc.
Size: Custom | Document Number: N14P-GT GDDR5 VRAM 1/2 | Rev: 1A
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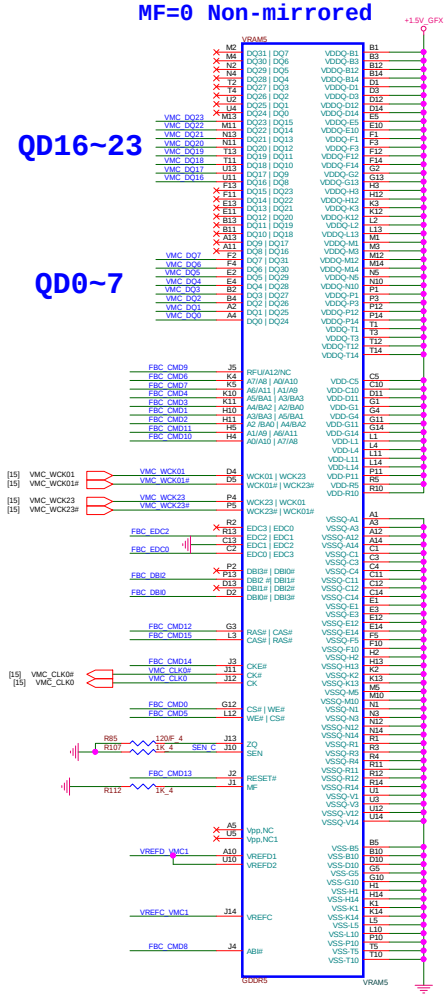
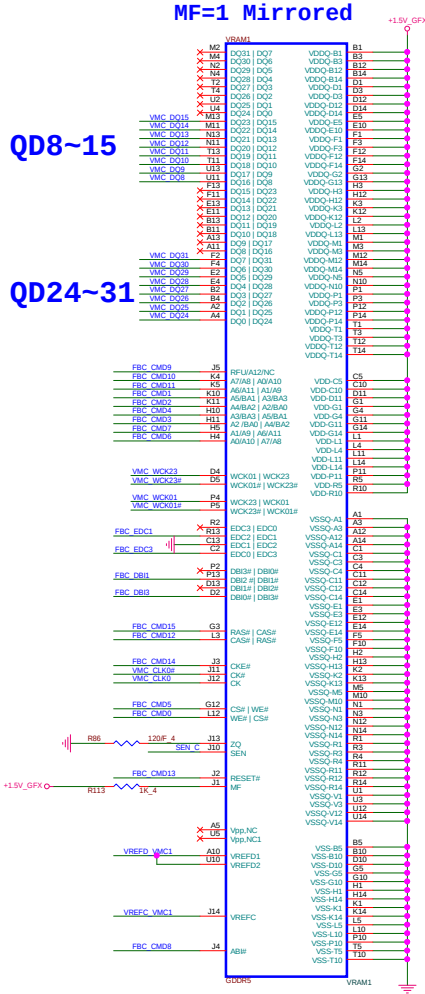
CHANNEL B: 1024MB GDDR5x32

[15] VMC_DQ[63..0] — VMC_DQ[63..0]
[15] FBC_CMD[31:0] — FBC_DBI[7..0]
[15] FBC_DBI[7..0] — FBC_EDC[7..0]
[15] FBC_EDC[7..0]

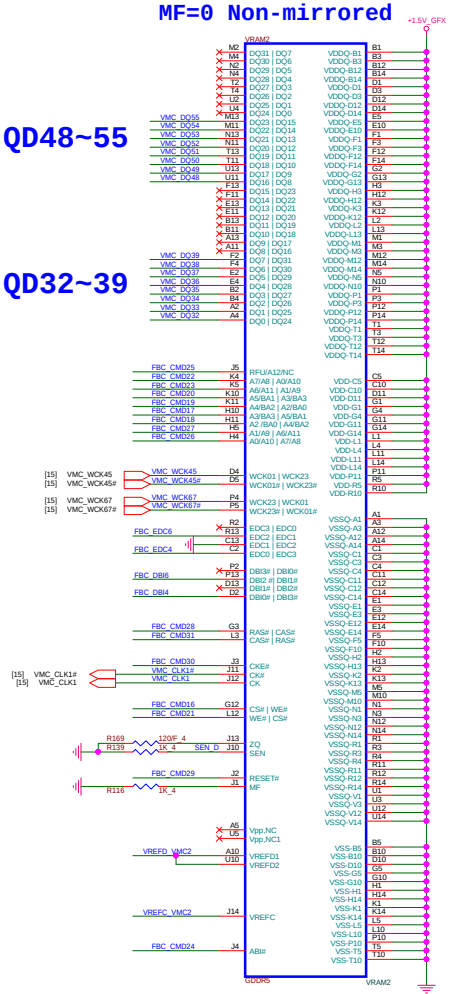
Channel 0 <0-31> MF=0 Non-mirrored — QD16~23, QD0~7



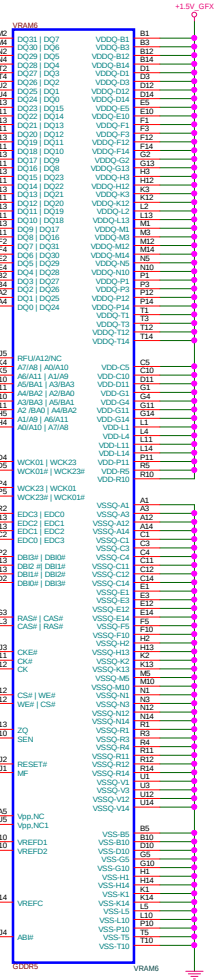
Channel 0 <32-63> MF=1 Mirrored — QD8~15, QD24~31

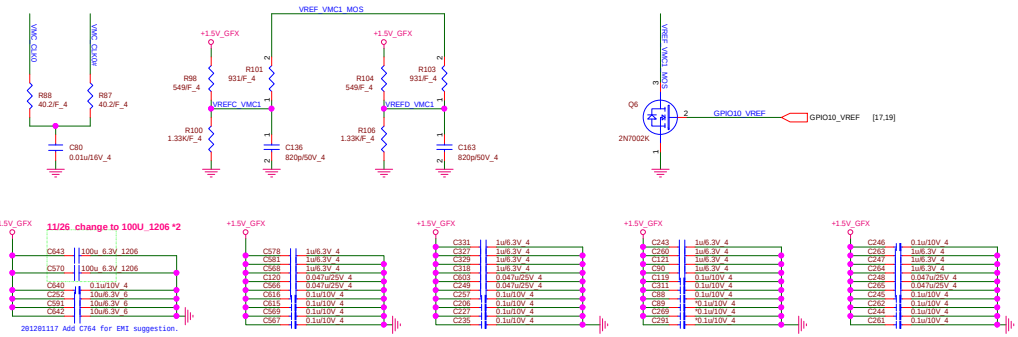


Channel 1 <0-31> MF=0 Non-mirrored — QD48~55, QD32~39



Channel 1 <32-63> MF=1 Mirrored — QD40~47, QD56~63





FBC_CMD14 R109 10K_4
FBC_CMD30 R125 10K_4

CKE* is strap pin to set ODT value of memory chip

FBC_CMD13 R110 10K_4
FBC_CMD29 R123 10K_4

RST PD place @ the end of daisy-chain.

GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CMD0	CMD16	CS*
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE*
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI*
CMD9	CMD25	A12_RFU
CMD10	CMD26	A9_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS*
CMD13	CMD29	RST*
CMD14	CMD30	CKE*
CMD15	CMD31	CAS*

NB5

PROJECT : TWK
Quanta Computer Inc.

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Custom	N14P-GT GDDR5 VRAM 2/2	1A

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CRT PORT

21

HDMI PORT

close to HDMI conn

[2] IN_CLK#
[2] IN_CLK
[2] IN_D0#
[2] IN_D0
[2] IN_D1#
[2] IN_D1
[2] IN_D2#
[2] IN_D2

IN_CLK# C625 0.1U/10V_4 C_TXC_HDMI-
IN_CLK C626 0.1U/10V_4 C_TXC_HDMI+
IN_D0# C631 0.1U/10V_4 C_TX0_HDMI-
IN_D0 C632 0.1U/10V_4 C_TX0_HDMI+
IN_D1# C627 0.1U/10V_4 C_TX1_HDMI-
IN_D1 C628 0.1U/10V_4 C_TX1_HDMI+
IN_D2# C635 0.1U/10V_4 C_TX2_HDMI-
IN_D2 C637 0.1U/10V_4 C_TX2_HDMI+

[6] SDVO_CLK — SDVO_CLK
[6] SDVO_DATA — SDVO_DATA
[6] HDMI_HPD_CON — HDMI_HPD_CON

Close to HDMI Connector

+3V R117 2.2K_4 — SDVO_CLK — HDMI_SCLK
+3V R118 2.2K_4 — SDVO_DATA — HDMI_SDATA
Q8 2N7002KDW

EMI request

C_TX2_HDMI+ R453 150/F_4 C_TX2_HDMI-
C_TX1_HDMI+ R443 150/F_4 C_TX1_HDMI-
C_TX0_HDMI+ R448 150/F_4 C_TX0_HDMI-
C_TXC_HDMI+ R437 150/F_4 C_TXC_HDMI-

JHDMI1

C_TX2_HDMI+ 1 — D2+ — SHELL1 20
C_TX2_HDMI- 3 — D2- — SHELL2 21
C_TX1_HDMI+ 4 — D1+ — SHELL2 22
C_TX1_HDMI- 6 — D1- — SHELL2 23
C_TX0_HDMI+ 7 — D0+
C_TX0_HDMI- 9 — D0-
D2 Shield 2
D1 Shield 5
D0 Shield 8
C_TXC_HDMI+ 10 — CK+ — CK Shield 11
C_TXC_HDMI- 12 — CK- — GND 17
HDMI_SCLK 15 — DDC CLK — CE Remote 13
HDMI_SDATA 16 — DDC DATA — NC 14
+5V 18
HP DET 19
HDMI CONN

1A +5V_HDMIC
KMC3S110RY F1
+5V
VC1 TVM0G5R5M220R
HDMI_HPD — L13 0_6 — HDMI_HPD_L
C216 220P/50V_4
VC2 *TVM0G5R5M220R

+5V_HDMIC D17 MEK500V-40 — R430 2.2K_4 — HDMI_SCLK
+5V_HDMIC D16 MEK500V-40 — R432 2.2K_4 — HDMI_SDATA

EMI request

+5V_HDMIC C238 0.1U/10V_4
+5V_HDMIC C237 220P/50V_4
+3V C274 0.1U/10V_4

+5V VC3 *TVM0G5R5M220R
R163 *0_4/S Q11 2N7002K
R152 100K_4 C324 0.01U/16V_4

R455 510/F_4 C_TX2_HDMI+
R451 510/F_4 C_TX2_HDMI-
R444 510/F_4 C_TX1_HDMI+
R441 510/F_4 C_TX1_HDMI-
R450 510/F_4 C_TX0_HDMI+
R447 510/F_4 C_TX0_HDMI-
R438 510/F_4 C_TXC_HDMI+
R436 510/F_4 C_TXC_HDMI-

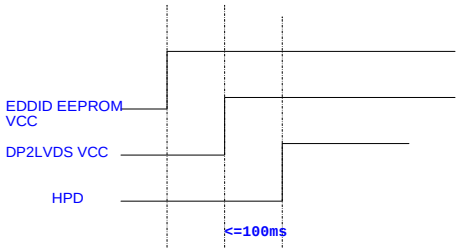
+3V R150 1M_4
HDMI_HPD_CON — Q10 ME2N7002E — HDMI_HPD
R137 20K/F_4

[7,25,26,29,30,36,39] +5V
[2,6,7,8,9,10,12,13,14,17,18,22,23,24,25,26,27,29,30,31,36,37,39] +3V
[25,28,29,33,34,35,36,37,38,39,40] +5VS5

NB5

PROJECT : TWK
Quanta Computer Inc.
Size Custom | Document Number CRT,Hole | Rev 1A
Date: Wednesday, April 23, 2014 | Sheet 21 of 42

RTD2136S Power Up Sequence 22



Reserve for co layout EDP CON, EDP only please stuff

RTD2136 Dual Channel only

Pine 18: keep 80 Mile Trace

IC body need GND pad

Use 1% Res on R7034

Default

Reserve

Reserve

Reserve

keep 80 Mile Trace

L7: need use CV-4709MN00 for Vendor suggestion

	PIN 47	
	0	1
PIN 48 0	X	EP mode
PIN 48 1	ROM	EEPROM

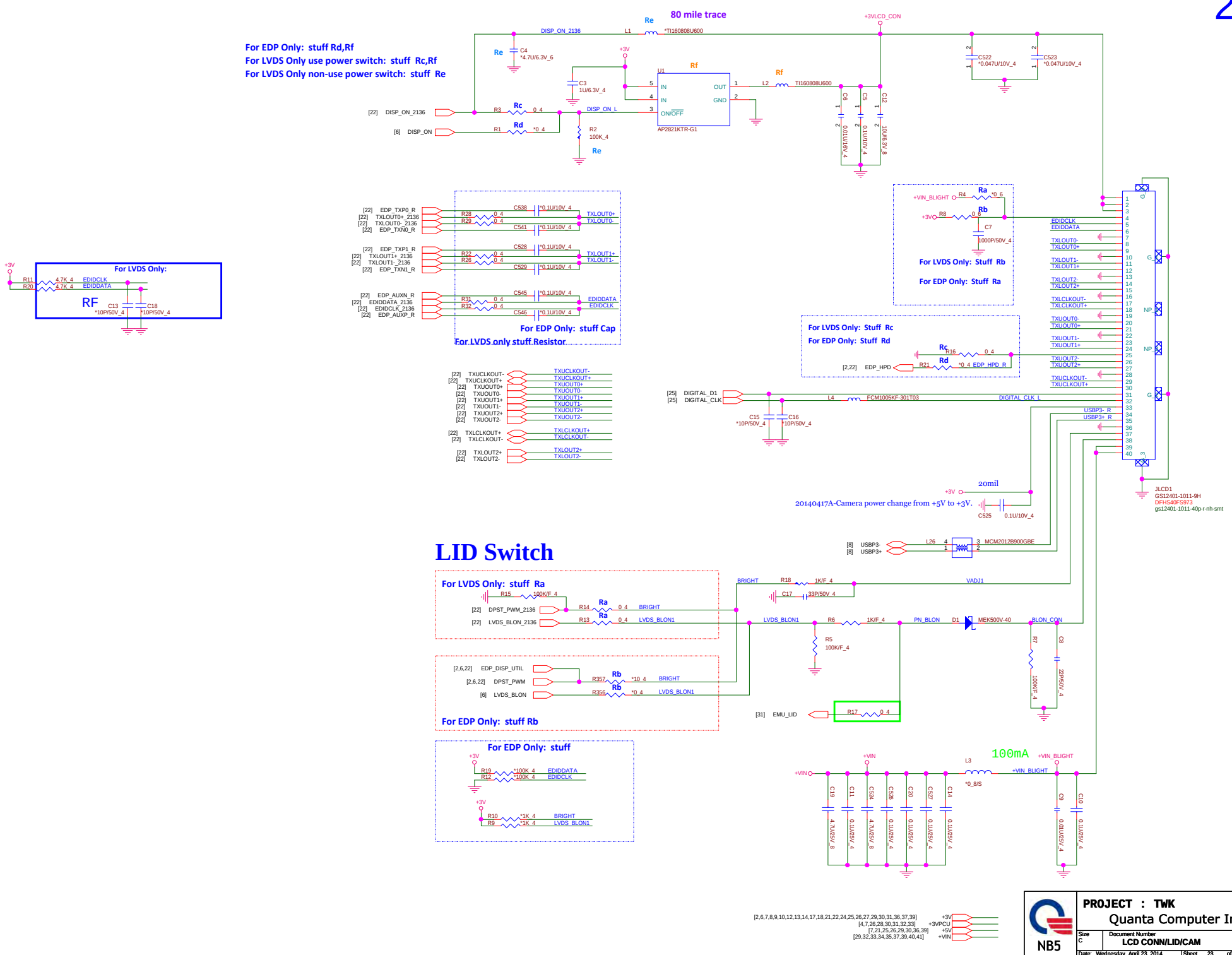
SWR MODE	LDO MODE
Stuff L69	Stuff R9095

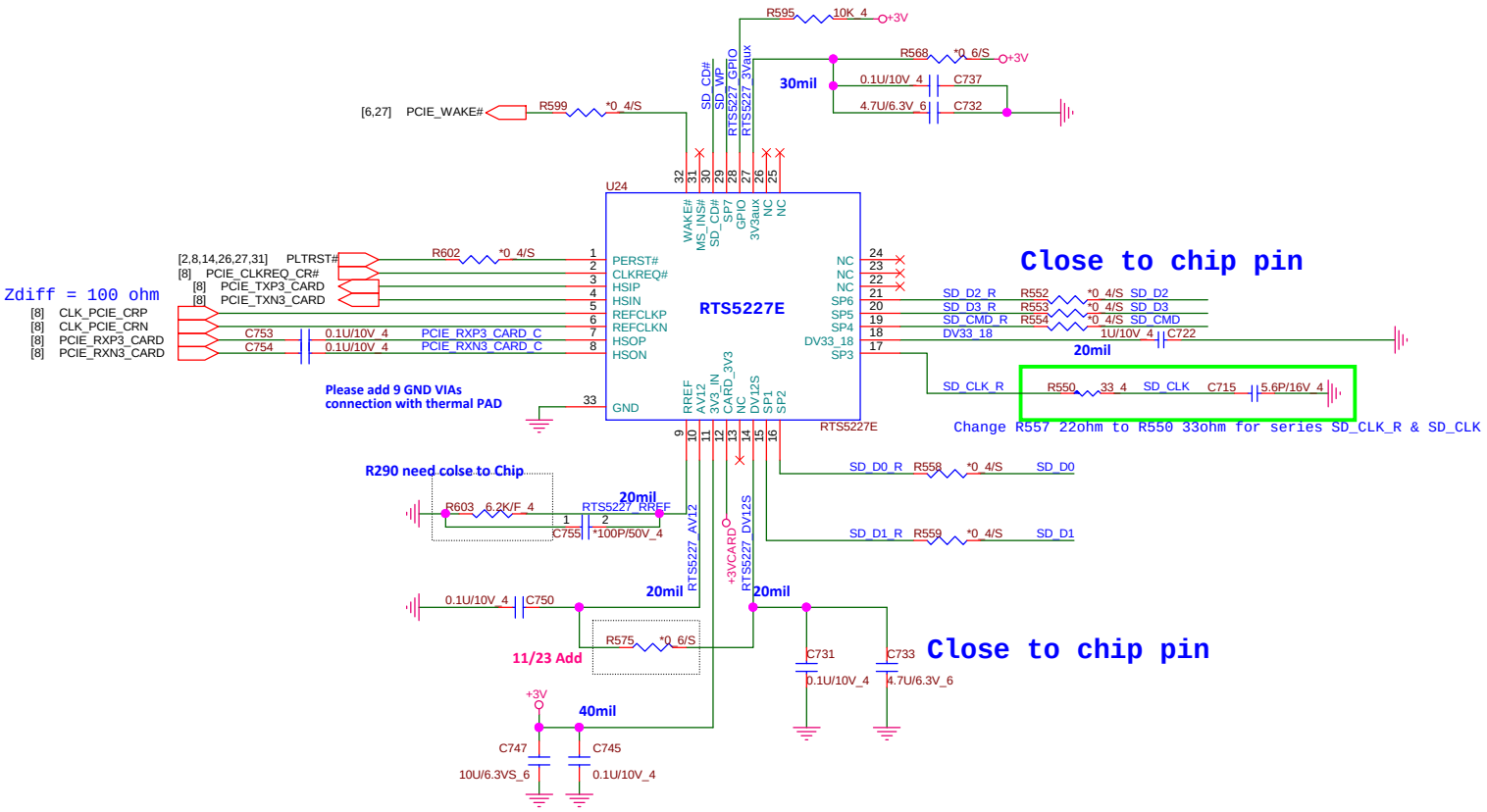
PROJECT : TWK
Quanta Computer Inc.

NB5

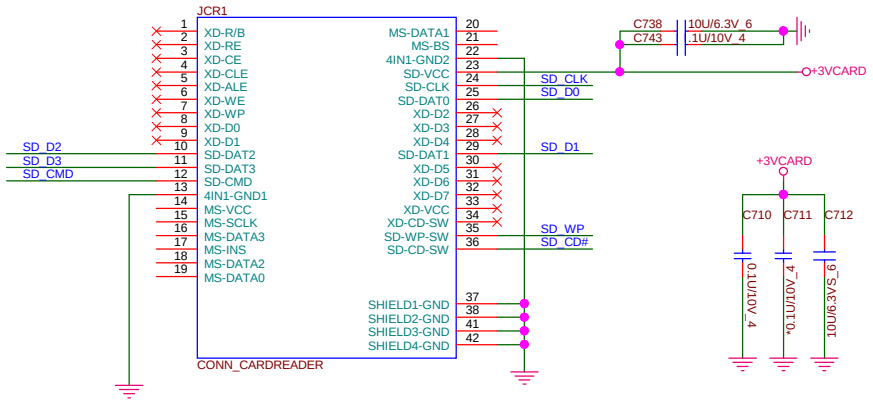
Size: Custom | Document Number: RTD2136S | Rev: 1A

Date: Wednesday, April 23, 2014 | Sheet 22 of 42

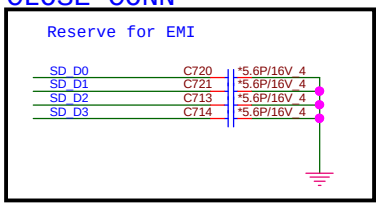

For EDP Only: stuff Rd,Rf
For LVDS Only use power switch: stuff Rc,Rf
For LVDS Only non-use power switch: stuff Re
80 mile trace
DISP_ON_2136
L1 *TI160808U600
+3VLCD_CON
C4 *4.7U/6.3V_6
C3 1U/6.3V_4
U1
AP2821KTR-G1
IN
OUT
GND
ON/OFF
L2 TI160808U600
C522 *0.047U/10V_4
C523 *0.047U/10V_4
C6 *0.01U/16V_4
C5 0.1U/10V_4
C12 10U/6.3V_8
[22] DISP_ON_2136
[6] DISP_ON
R3 0_4
R1 *0_4
R2 100K_4
DISP_ON_L
For LVDS Only: stuff Cap
For LVDS only stuff Resistor
For LVDS Only: stuff Ra
For EDP Only: Stuff Rb
For LVDS Only: Stuff Rc
For EDP Only: Stuff Rd
[2,22] EDP_HPD
R16 0_4
R21 *0_4 EDP_HPD_R
[25] DIGITAL_D1
[25] DIGITAL_CLK
L4 FCM1005KF-301T03
C15 *10P/50V_4
C16 *10P/50V_4
20mil
20140417A-Camera power change from +5V to +3V.
C525 0.1U/10V_4
JLCD1
GS12401-1011-9H
DFHS40FS973
gs12401-1011-40p-r-nh-smt
[8] USBP3-
[8] USBP3+
L26 MCM2012B900GBE
USBP3-_R
USBP3+_R
LID Switch
For LVDS Only: stuff Ra
For EDP Only: stuff Rb
For EDP Only: stuff
[2,6,22] EDP_DISP_UTIL
[2,6,22] DPST_PWM
[6] LVDS_BLON
[22] DPST_PWM_2136
[22] LVDS_BLON_2136
BRIGHT
LVDS_BLON1
R18 1K/F_4
C17 33P/50V_4
R6 1K/F_4
R5 100K/F_4
PN_BLON
D1 MEK500V-40
BLON_CON
R7 100K/F_4
C3 2200P/50V_4
[31] EMU_LID
R17 0_4
VADJ1
100mA
+VIN
+VIN_BLIGHT
L3 *0_8/S
C19 4.7U/25V_8
C11 0.1U/25V_4
C524 4.7U/25V_8
C526 0.1U/25V_4
C20 0.1U/25V_4
C527 0.1U/25V_4
C14 0.1U/25V_4
C3 0.01U/25V_4
C10 0.1U/25V_4
[2,6,7,8,9,10,12,13,14,17,18,21,22,24,25,26,27,29,30,31,36,37,39]
[4,7,26,28,30,31,32,33]
[7,21,25,26,29,30,36,39]
[29,32,33,34,35,37,39,40,41]
+3V
+3VPCU
+5V
+VIN
PROJECT : TWK
Quanta Computer Inc.
NB5
Size C
Document Number LCD CONN/LID/CAM
Rev 1A
Date: Wednesday, April 23, 2014
Sheet 23 of 42



SD / MMC CARD READER

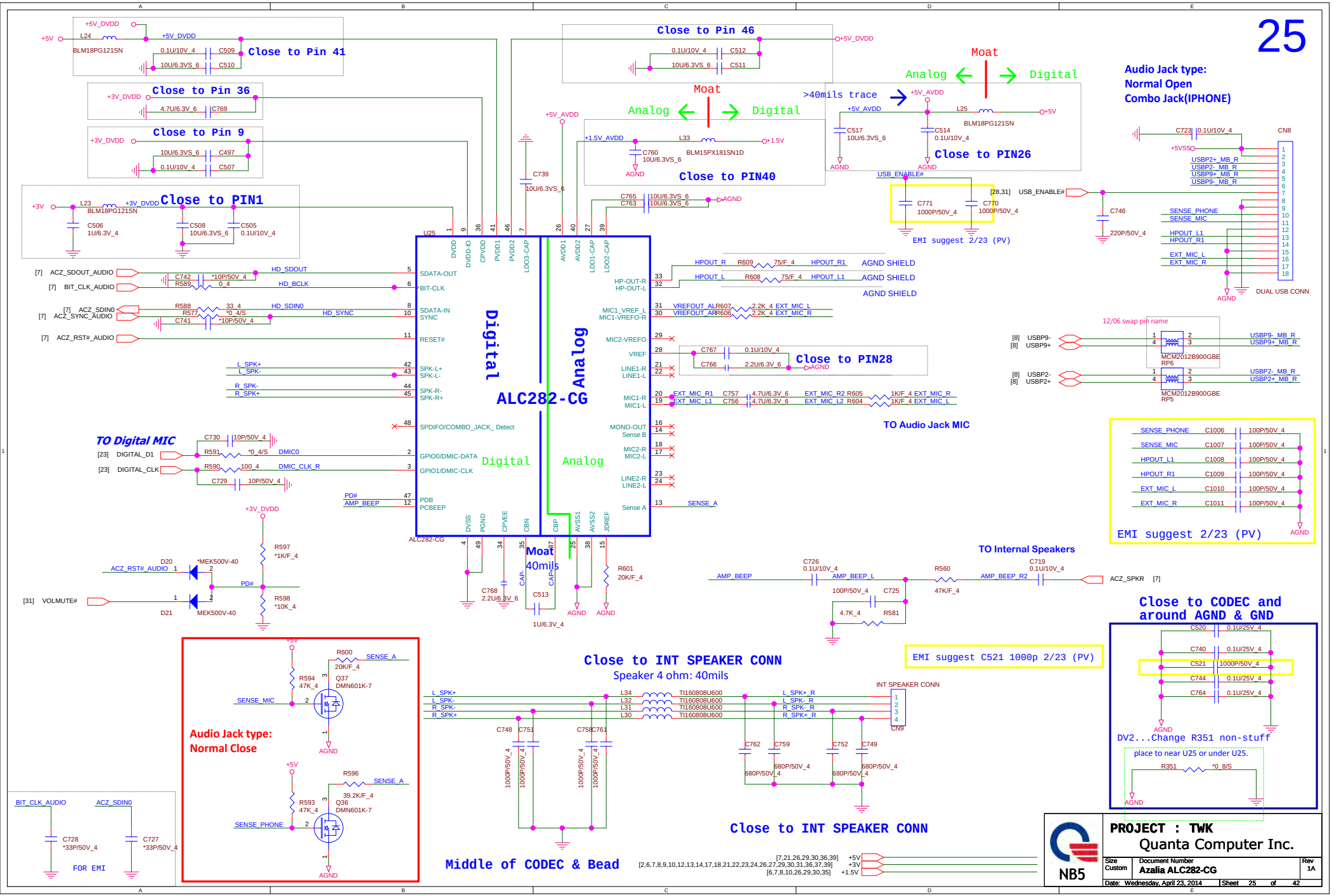


CLOSE CONN



[2,6,7,9,10,26,28,29,31,33,35,36,41] +3VS5
[2,6,7,8,9,10,12,13,14,17,18,21,22,23,25,26,27,29,30,31,36,37,39] +3V

NB5	PROJECT : TWK Quanta Computer Inc.	
Size: Custom	Document Number: RTS5227 & CR SOCKET	Rev: 1A
Date: Wednesday, April 23, 2014	Sheet 24 of 42	



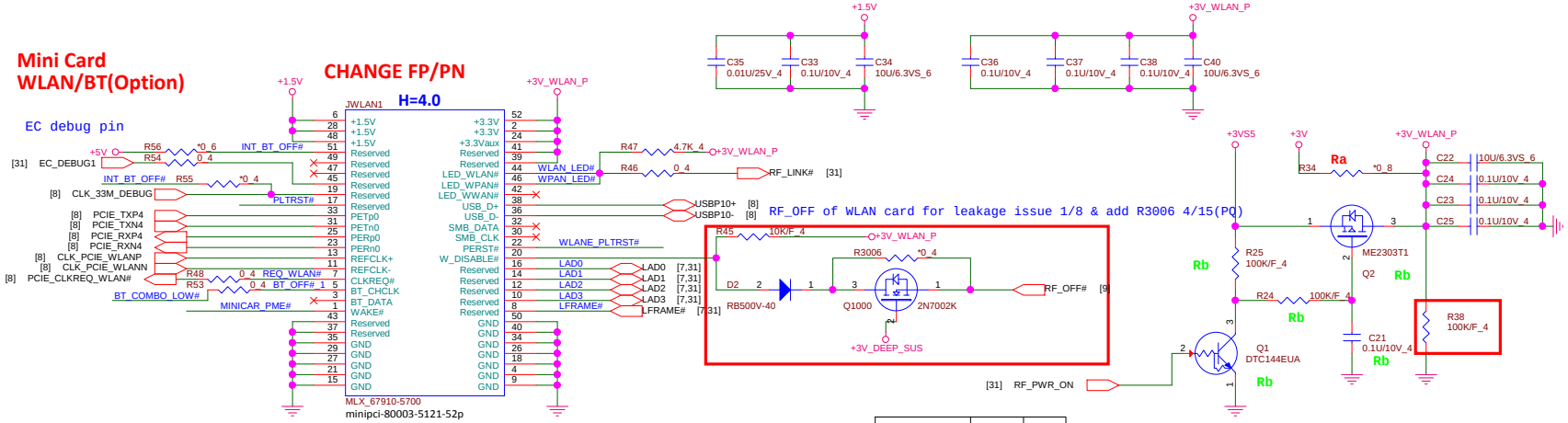
PROJECT :	TWK
	Quanta Computer Inc.
NB5	
Size: Custom	Document Number: Azalia ALC282-CG
Rev: 1A	
Date: Wednesday, April 23, 2014	Sheet 25 of 42

Mini Card WLAN/BT(Option)

CHANGE FP/PN

H=4.0

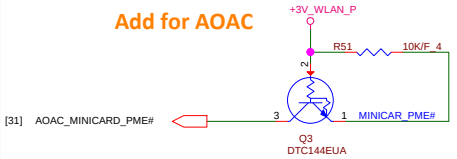
EC debug pin



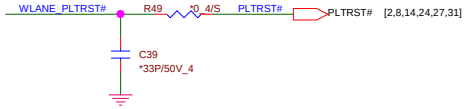
non-AOAC	LG	Ra
AOAC	CB	Rb

Support Wake Function(Reserve)

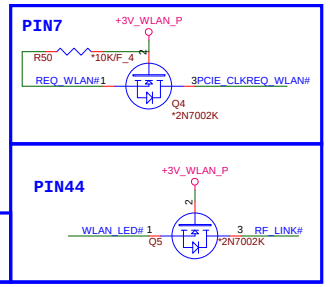
Add for AOAC



Mini Card Reset



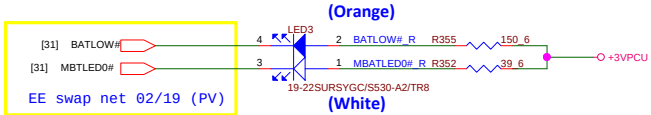
Avoid leakage issue

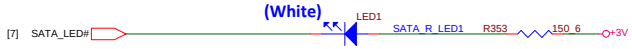


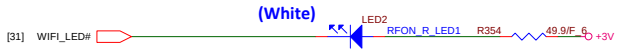
For EMI Suggestion

CLK_33M_DEBUG — R52 *0_4 — C41 *33P/50V_4

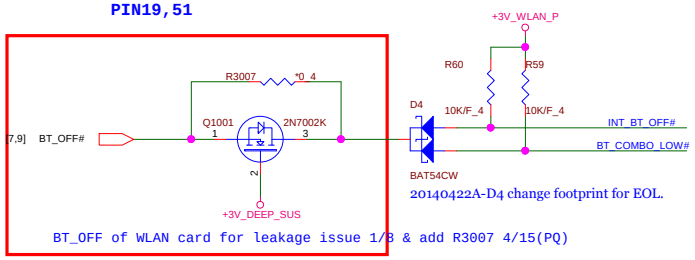
LED Status







PIN19, 51



9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

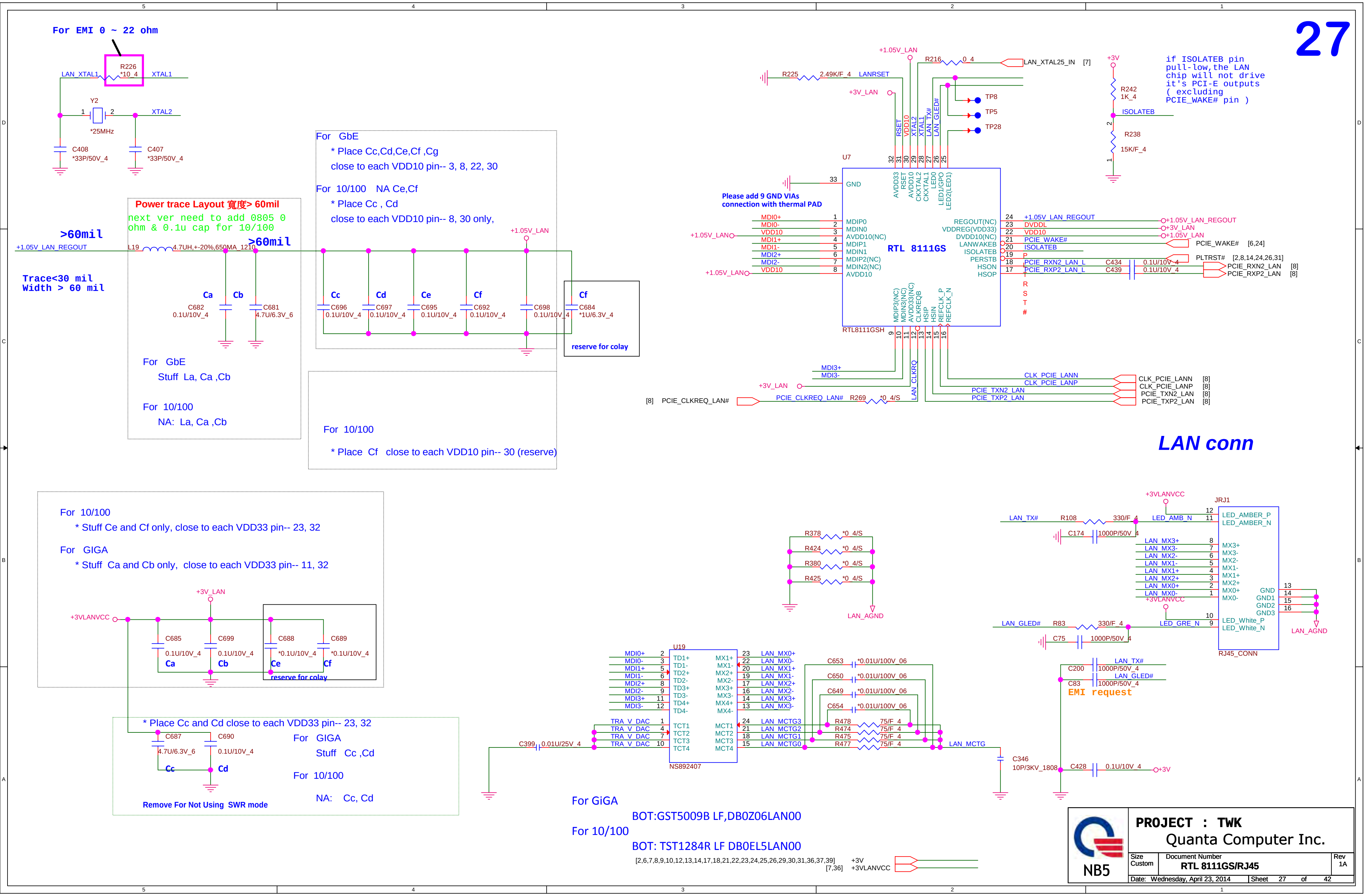
[2,6,7,8,9,10,12,13,14,17,18,21,22,23,24,25,27,29,30,31,36,37,39] +3V
[7,21,25,29,30,36,39] +5V
[4,7,28,30,31,32,33] +3VPCU
[6,7,8,10,25,29,30,35] +1.5V

NB5

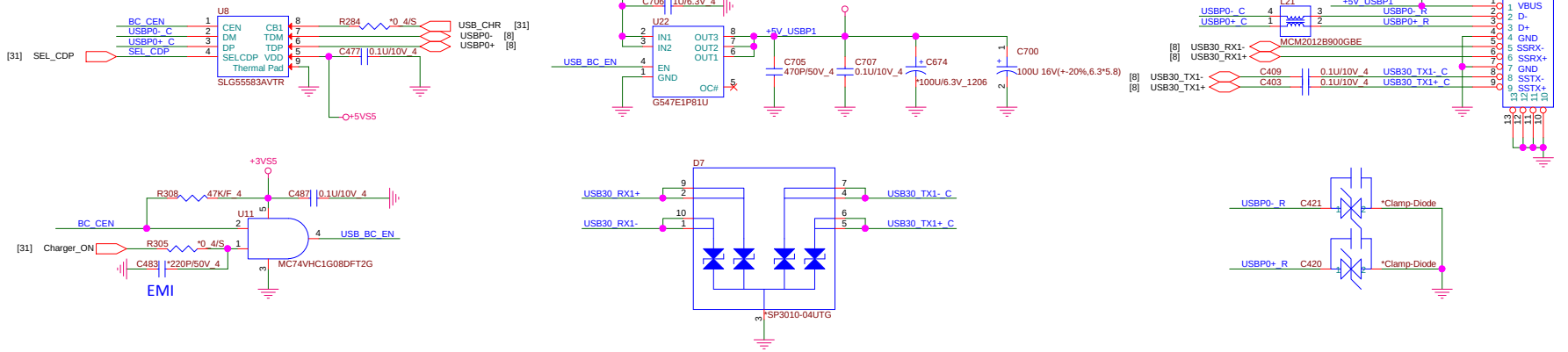
PROJECT : TWK
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN & LED	1A

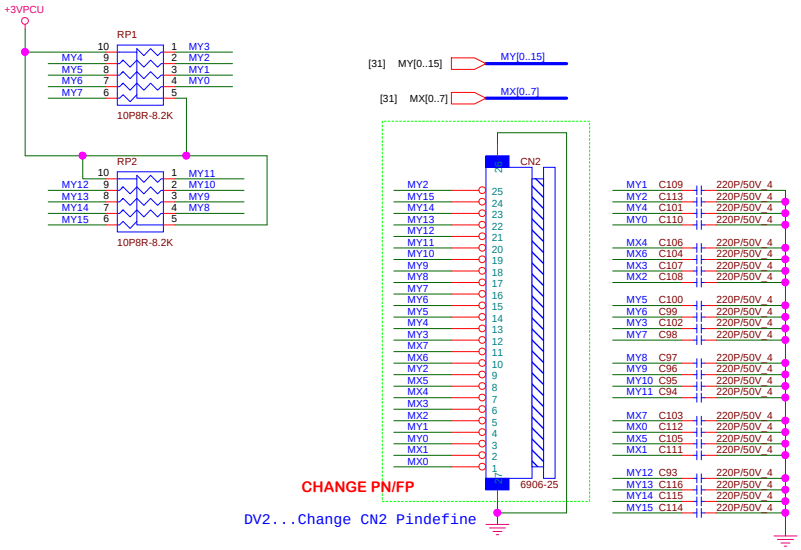
Date: Wednesday, April 23, 2014 Sheet 26 of 42


27
For EMI 0 ~ 22 ohm
R226
*10_4
LAN_XTAL1
XTAL1
XTAL2
Y2
*25MHz
C408
*33P/50V_4
C407
*33P/50V_4
Power trace Layout 寬度> 60mil
next ver need to add 0805 0 ohm & 0.1u cap for 10/100
>60mil
+1.05V_LAN_REGOUT
L19
4.7UH,+-20%,650MA_1210
Trace<30 mil
Width > 60 mil
Ca
Cb
C682
0.1U/10V_4
C681
4.7U/6.3V_6
For GbE
Stuff La, Ca ,Cb
For 10/100
NA: La, Ca ,Cb
For GbE
* Place Cc,Cd,Ce,Cf ,Cg
close to each VDD10 pin-- 3, 8, 22, 30
For 10/100 NA Ce,Cf
* Place Cc , Cd
close to each VDD10 pin-- 8, 30 only,
+1.05V_LAN
Cc
Cd
Ce
Cf
C696
C697
C695
C692
C698
C684
*1U/6.3V_4
reserve for colay
For 10/100
* Place Cf close to each VDD10 pin-- 30 (reserve)
R225
2.49K/F_4
LANRSET
+1.05V_LAN
R216
0_4
LAN_XTAL25_IN [7]
+3V_LAN
TP8
TP5
TP28
U7
Please add 9 GND VIAs
connection with thermal PAD
RTL 8111GS
RTL8111GSH
MDI0+
MDI0-
VDD10
MDI1+
MDI1-
MDI2+
MDI2-
+1.05V_LAN_REGOUT
DVDDL
PCIE_WAKE#
ISOLATEB
PCIE_RXN2_LAN_L
PCIE_RXP2_LAN_L
C434
C439
0.1U/10V_4
PCIE_WAKE# [6,24]
PLTRST# [2,8,14,24,26,31]
PCIE_RXN2_LAN [8]
PCIE_RXP2_LAN [8]
+3V
R242
1K_4
ISOLATEB
R238
15K/F_4
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)
MDI3+
MDI3-
CLK_PCIE_LANN
CLK_PCIE_LANP
PCIE_TXN2_LAN
PCIE_TXP2_LAN
CLK_PCIE_LANN [8]
CLK_PCIE_LANP [8]
PCIE_TXN2_LAN [8]
PCIE_TXP2_LAN [8]
[8] PCIE_CLKREQ_LAN#
R269
*0_4/S
LAN conn
For 10/100
* Stuff Ce and Cf only, close to each VDD33 pin-- 23, 32
For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32
+3V_LAN
+3VLANVCC
C685
C699
C688
C689
0.1U/10V_4
*0.1U/10V_4
reserve for colay
* Place Cc and Cd close to each VDD33 pin-- 23, 32
C687
4.7U/6.3V_6
C690
0.1U/10V_4
For GIGA
Stuff Cc ,Cd
For 10/100
NA: Cc, Cd
Remove For Not Using SWR mode
R378
R424
R380
R425
*0_4/S
LAN_AGND
U19
NS892407
TRA_V_DAC
C399
0.01U/25V_4
LAN_MX0+
LAN_MX0-
LAN_MX1+
LAN_MX1-
LAN_MX2+
LAN_MX2-
LAN_MX3+
LAN_MX3-
LAN_MCTG3
LAN_MCTG2
LAN_MCTG1
LAN_MCTG0
C653
C650
C649
C654
*0.01U/100V_06
R478
R474
R475
R477
75/F_4
LAN_MCTG
C346
10P/3KV_1808
C428
0.1U/10V_4
+3VLANVCC
JRJ1
LAN_TX#
R108
330/F_4
LED_AMB_N
C174
1000P/50V_4
LAN_GLED#
R83
330/F_4
LED_GRE_N
C75
1000P/50V_4
RJ45_CONN
C200
C83
1000P/50V_4
EMI request
For GiGA
BOT:GST5009B LF,DB0Z06LAN00
For 10/100
BOT: TST1284R LF DB0EL5LAN00
[2,6,7,8,9,10,12,13,14,17,18,21,22,23,24,25,26,29,30,31,36,37,39] +3V
[7,36] +3VLANVCC
PROJECT : TWK
Quanta Computer Inc.
NB5
Size Custom
Document Number RTL 8111GS/RJ45
Rev 1A
Date: Wednesday, April 23, 2014
Sheet 27 of 42

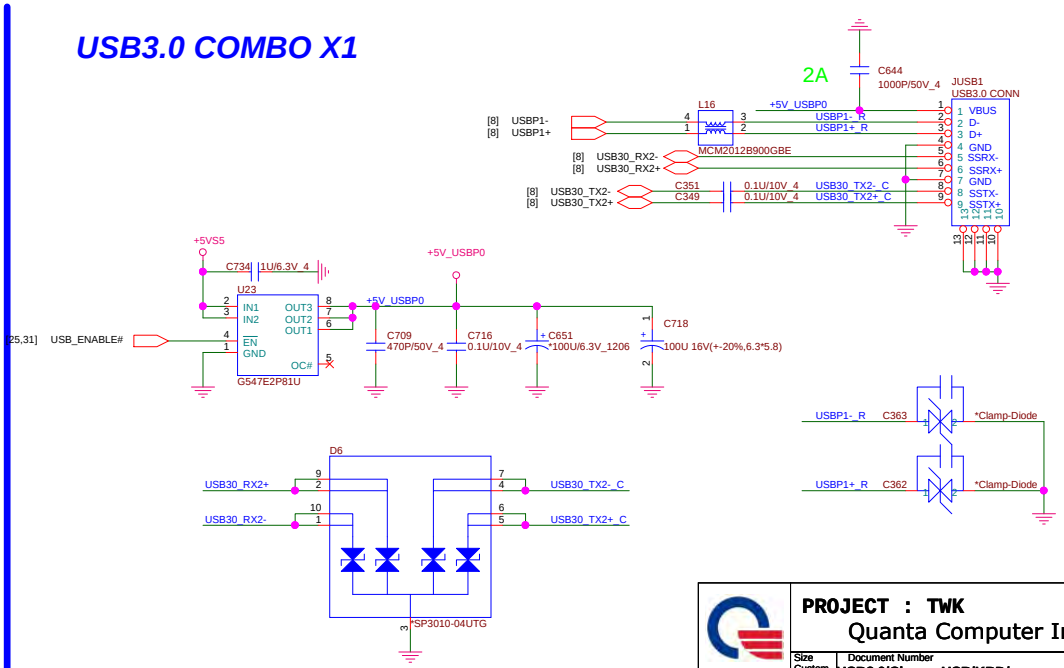
Charge USB/USB3.0 COMBO X1



Keyboard Connector



USB3.0 COMBO X1



NB5	PROJECT : TWK Quanta Computer Inc.	
	Size: Custom	Document Number: USB3.0/Charge USB/KBD/ Rev: 1A
	Date: Wednesday, April 23, 2014	Sheet 28 of 42

CPU Bracket

HC1 *H-TC276BC197D150P2
HC2 *H-TC276BC197D150P2
HC3 *H-TC276BC197D150P2
HC4 *H-TC276BC197D150P2

GPU Bracket

HG1 *H-TC276BC197D150P2
HG3 *H-TC276BC197D150P2
HG4 *H-TC276BC197D150P2
HG2 *H-TC276BC197D150P2

PCH NU Screw Hold

NP2 H-C256D122P2
NP1 H-C256D122P2
NS1 *H-C256D67P2
NL1 H-C256D161P2

System Screw Hold

HS1 *H-C315D110P2
HS2 *H-C315D110P2
HS3 *H-C236D110P2
HS4 *O-TWH-4
HS7 *h-tc472bc315d110p2
HS5 *H-C315D110P2
HS6 *h-tc472bc315d110p2
HL1 *H-C394D157P2
H10 *H-TS394BC315D110P2
H8 *H-TS394BC315D110P2
H9 *H-TS394BC315D110P2
H3 *h-tr315x295br394x295d110p2
H12 *O-TWH-2
H13 *H-C110D110N
H6 *H-C110D110N
H15 *O-TWH-3

System Pad(Top)

P1 P2 P3 P4 P5 P6 P13 P7 B1
H14 *O-TWH-3
H16 *O-TWH-3
H11 *h-c197d91p2
H7 *h-c197d91p2

System Pad(Button)

P12 P8 P9 P11 P10 B2

Define to GND for EMI request 4/10

EMI CAP

+3V: C59 0.1U/10V_4, C312 0.1U/10V_4, C708 0.1U/10V_4, C735 0.1U/10V_4
+1.05V: C240 0.1U/10V_4, C302 0.1U/10V_4
+3VS5: C554 0.1U/10V_4, C504 0.1U/10V_4, C704 0.1U/10V_4, C70 0.1U/10V_4, C531 0.1U/10V_4
+1.5V: C396 0.1U/10V_4, C376 0.1U/10V_4, C390 0.1U/10V_4
+5VS5: C69 0.1U/10V_4, C338 0.1U/10V_4, C515 0.1U/10V_4, C518 0.1U/10V_4, C772 0.1U/10V_4
+VIN: C2 0.1U/25V_4, C315 0.1U/25V_4, C1 0.1U/25V_4, C32 0.1U/25V_4
+5V: C516 1000P/50V_4, C519 1000P/50V_4

KB LIGHT

+VIN, +5V
R3008 *1M_4
Q2003 *AO3404
[31] LED_ON
Q2004 *2N7002
R3009 *2M_4
+5V_LED_KBLIGHT
C3004 *0.1U/10V_4
C3005 *0.1U/10V_4
CN10 *KB_LIGHT_CONN_15"

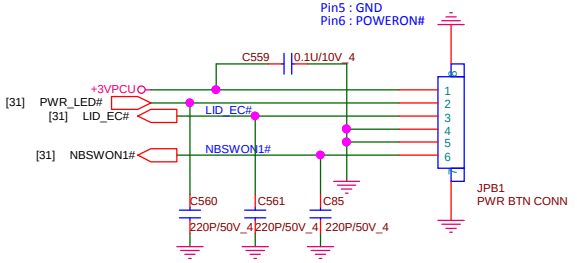
[2,6,7,8,9,10,12,13,14,17,18,21,22,23,24,25,26,27,30,31,36,37,39] +3V
[25,28,33,34,35,36,37,38,39,40] +5VS5
[2,6,7,9,10,26,28,31,33,35,36,41] +3VS5
[23,32,33,34,35,37,39,40,41] +VIN
[2,4,7,9,10,34,41] +1.05V
[7,21,25,26,30,36,39] +5V
[6,7,8,10,25,26,30,35] +1.5V

NB5

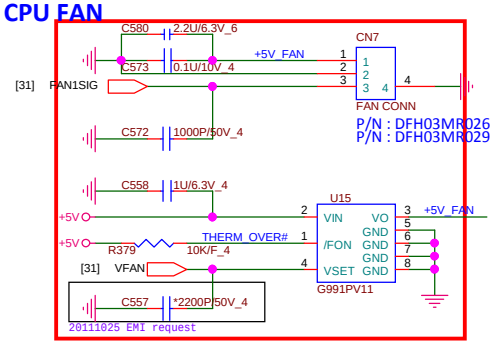
PROJECT : TWK
Quanta Computer Inc.
Size: Custom | Document Number: Hole / EMI Cap | Rev: 1A
Date: Wednesday, April 23, 2014 | Sheet 29 of 42

Power Botton Connector

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

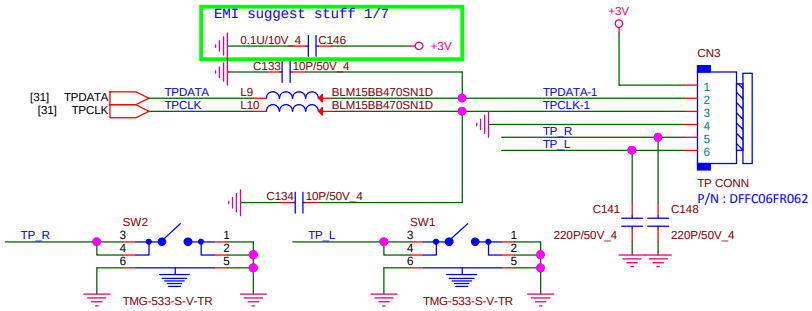


CPU FAN

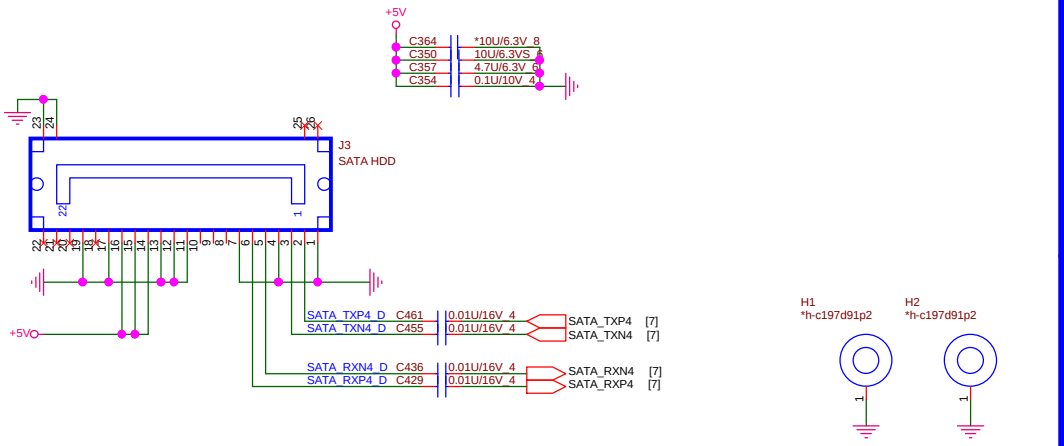


Touch Pad Connector

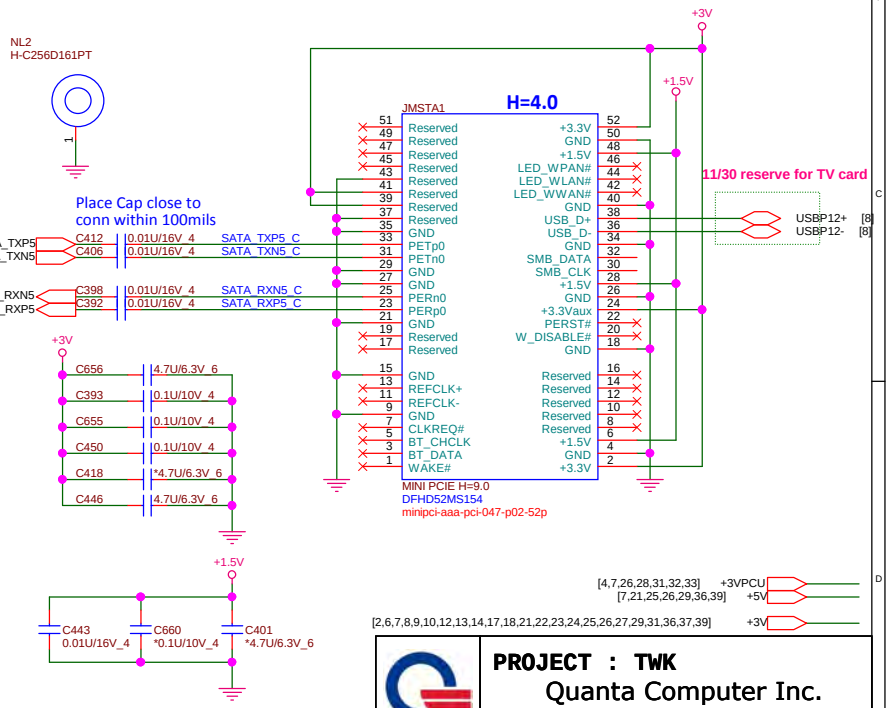
B-stage change footprint to 88513-0601-6p-l-smt



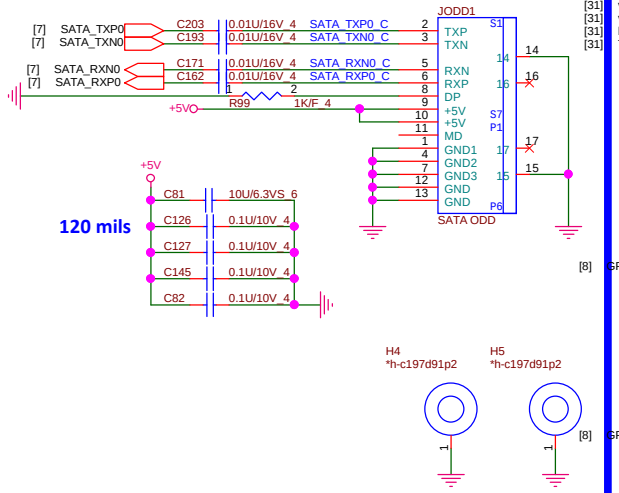
SATA HDD CONNECTOR



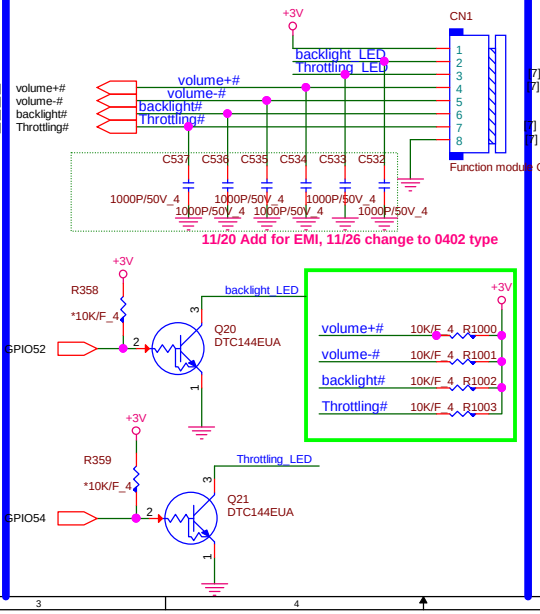
MINISATA



SATA ODD Connector



Function Module connector



[4,7,26,28,31,32,33] +3VPCU
[7,21,25,26,29,36,39] +5V
[2,6,7,8,9,10,12,13,14,17,18,21,22,23,24,25,26,27,29,31,36,37,39] +3V

NB5

PROJECT : TWK
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SW/TP/FAN/HDD/ODD/mSATA	1A

Date: Wednesday, April 23, 2014 | Sheet 30 of 42

IT8528E/AX

Layout Note:
Place all capacitors close to IT8502N.

12 MILS

C693 0.1U/10V_4 C663 0.1U/10V_4 C683 0.1U/10V_4 C380 0.1U/10V_4 C672 0.1U/10V_4 C694 0.1U/10V_4

DV2...Q12 pin2 change Net to "PWR_LED"

DV2...Q17 pin5 change Net to "BATLOW"

2N7002KDW

For Battery charge

For PCH SMB/DDR Thermal IC/VGA and Cap board

11/14 add

11/14 add
20140417A-Pin-30 LED_ON for TWK K/B backlight control.

stuff R228,R233 for touch pad function 1/7

thermal shutdown circuit

Open Drain need pu high

Close to EC
EMI request

Q19 place close to CPU

11/20 move to EC side

Vender	Size	P/N
AMIC	4MB	AKE39ZN0800 (AMIC A25QE32M-F (QE))
Winbond	4MB	AKE39FN0N01 (Winbond W25Q32FVSSIQ (QE))
Socket		DFHS08FS023

Socket: DG008000031

Select Pin

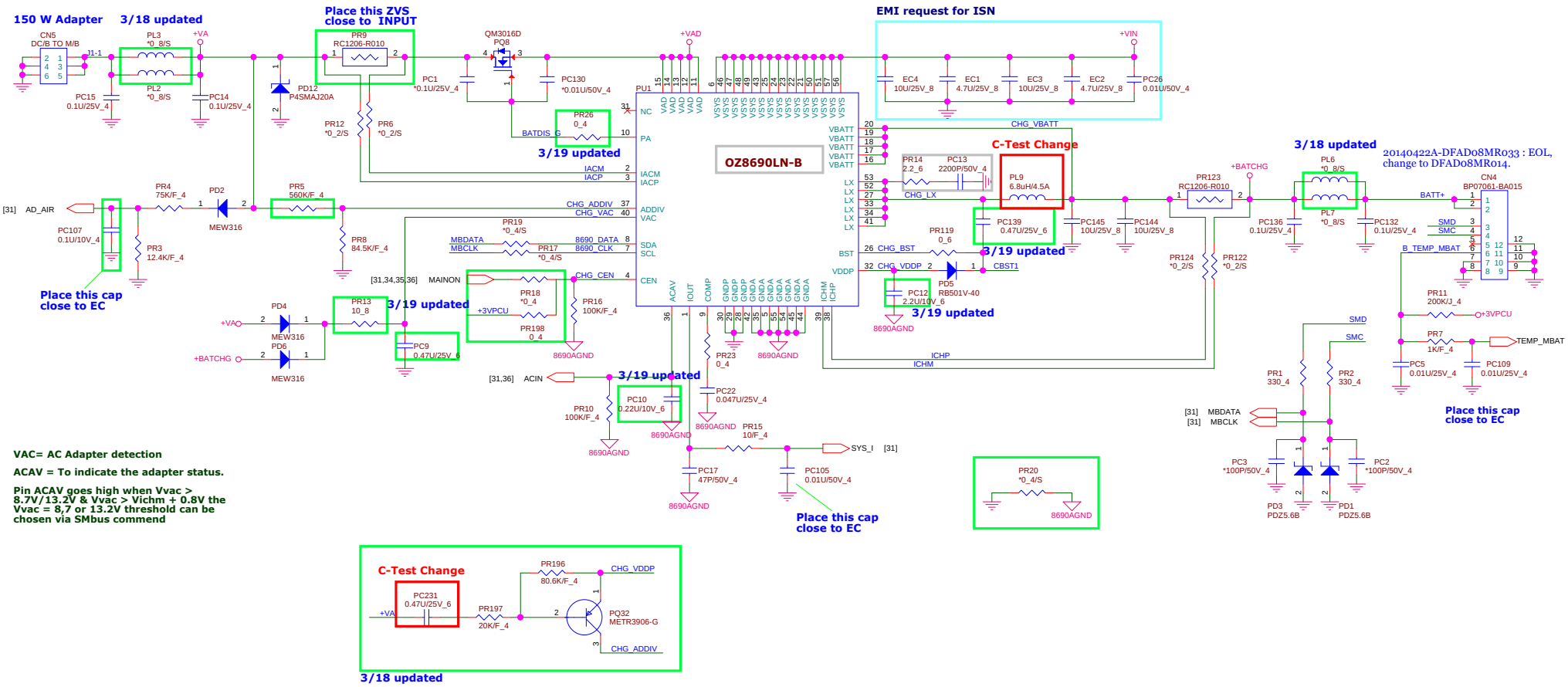
	CB/LG Select
QLGS	Ra
TWS	Rb
TWJ/TWK	Ra+Rb

NB5

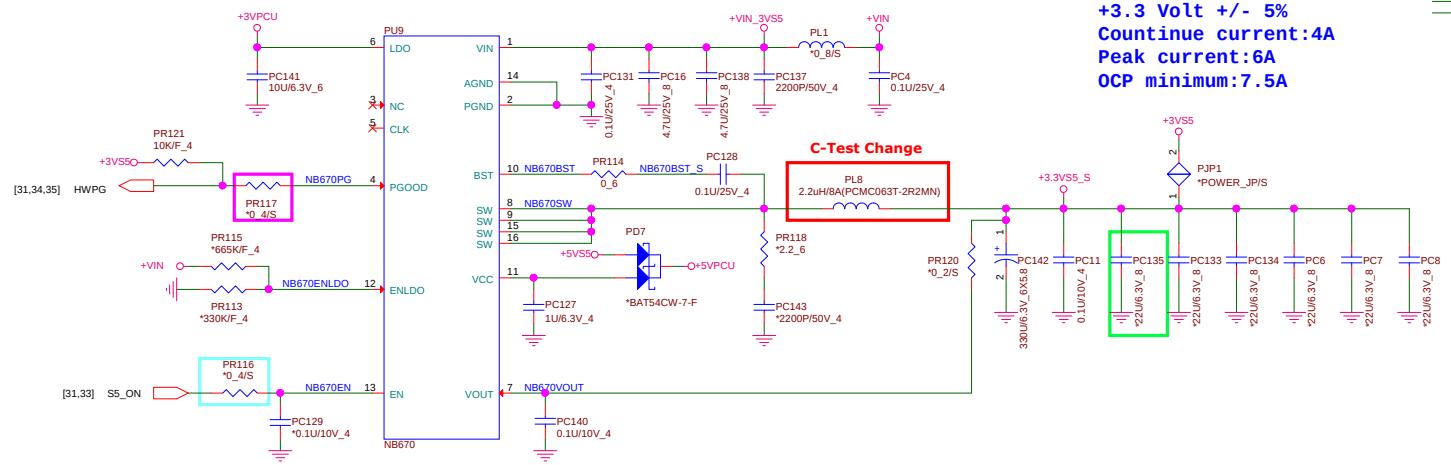
PROJECT : TWK
Quanta Computer Inc.

Size	Document Number	Rev
C	EC (ITE8258E)/ROM	1A

Date: Wednesday, April 23, 2014 Sheet 31 of 42

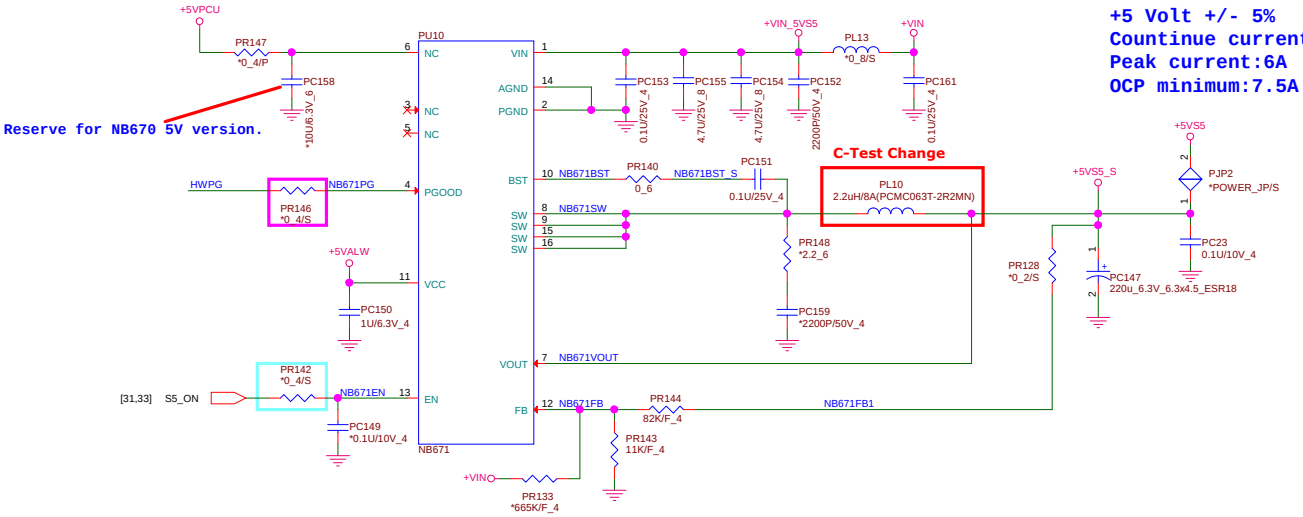

150 W Adapter
3/18 updated
Place this ZVS close to INPUT
EMI request for ISN
OZ8690LN-B
C-Test Change
3/19 updated
3/18 updated
20140422A-DFAD08MR033 : EOL, change to DFAD08MR014.
Place this cap close to EC
VAC= AC Adapter detection
ACAV = To indicate the adapter status.
Pin ACAV goes high when Vvac > 8.7V/13.2V & Vvac > Vichm + 0.8V the Vvac = 8,7 or 13.2V threshold can be chosen via SMbus commend
PROJECT : TWK
Quanta Computer Inc.
NB5
Charger (OZ8681)
Wednesday, April 23, 2014

DC/DC +3VS5/+5VS5



+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3VS5 [2,6,7,9,10,26,28,29,31,35,36,41]
+5VS5 [25,28,29,34,35,36,37,38,39,40]



Reserve for NB670 5V version.

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

NB5	PROJECT : TWK Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VPCU(RT8243A)	Rev: 1A
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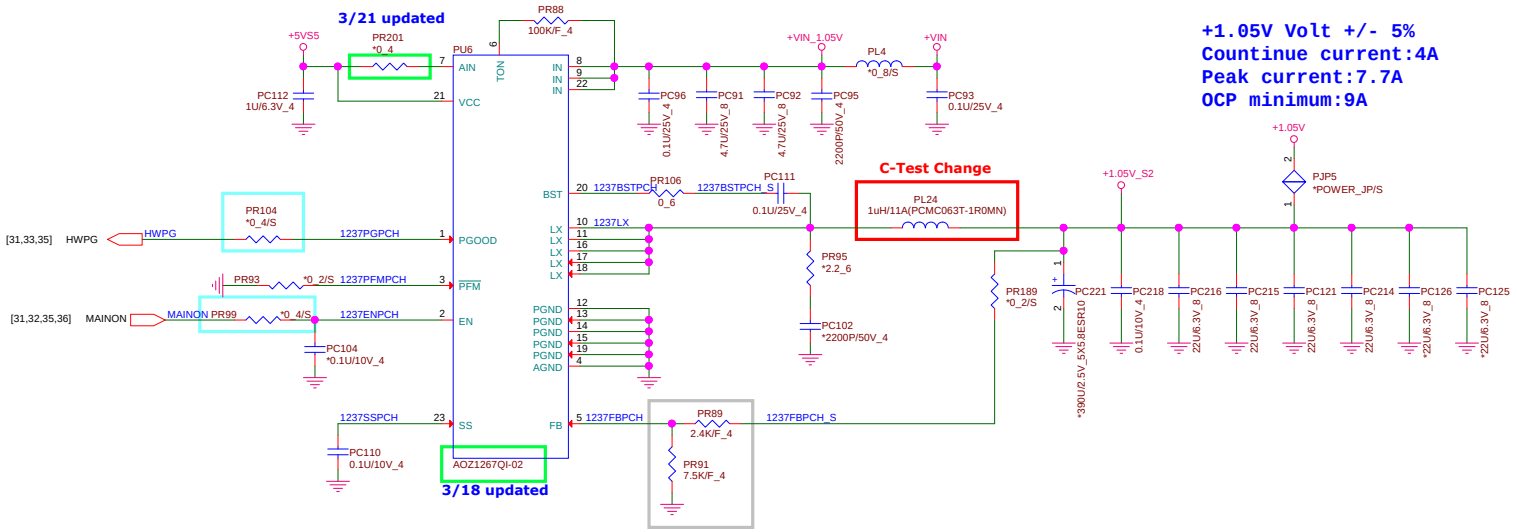

+1.05V [2,4,7,9,10,29,41]

NB5

PROJECT : TWK

Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.05V(RT8228BZ)	1A

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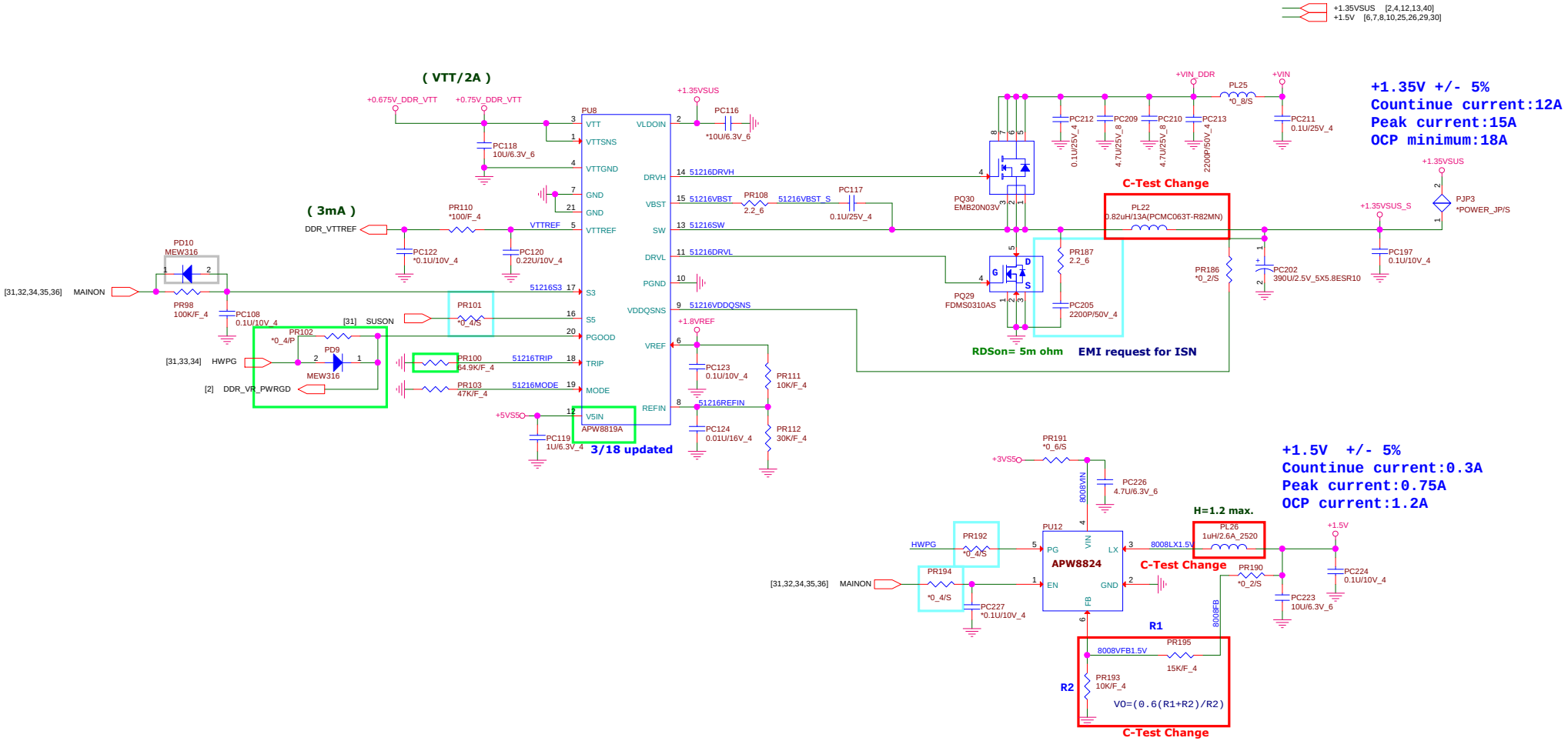

NB5	PROJECT : TWK Quanta Computer Inc.	
	Size: Custom Document Number: DDR3L(APW8819)	Rev: 1A
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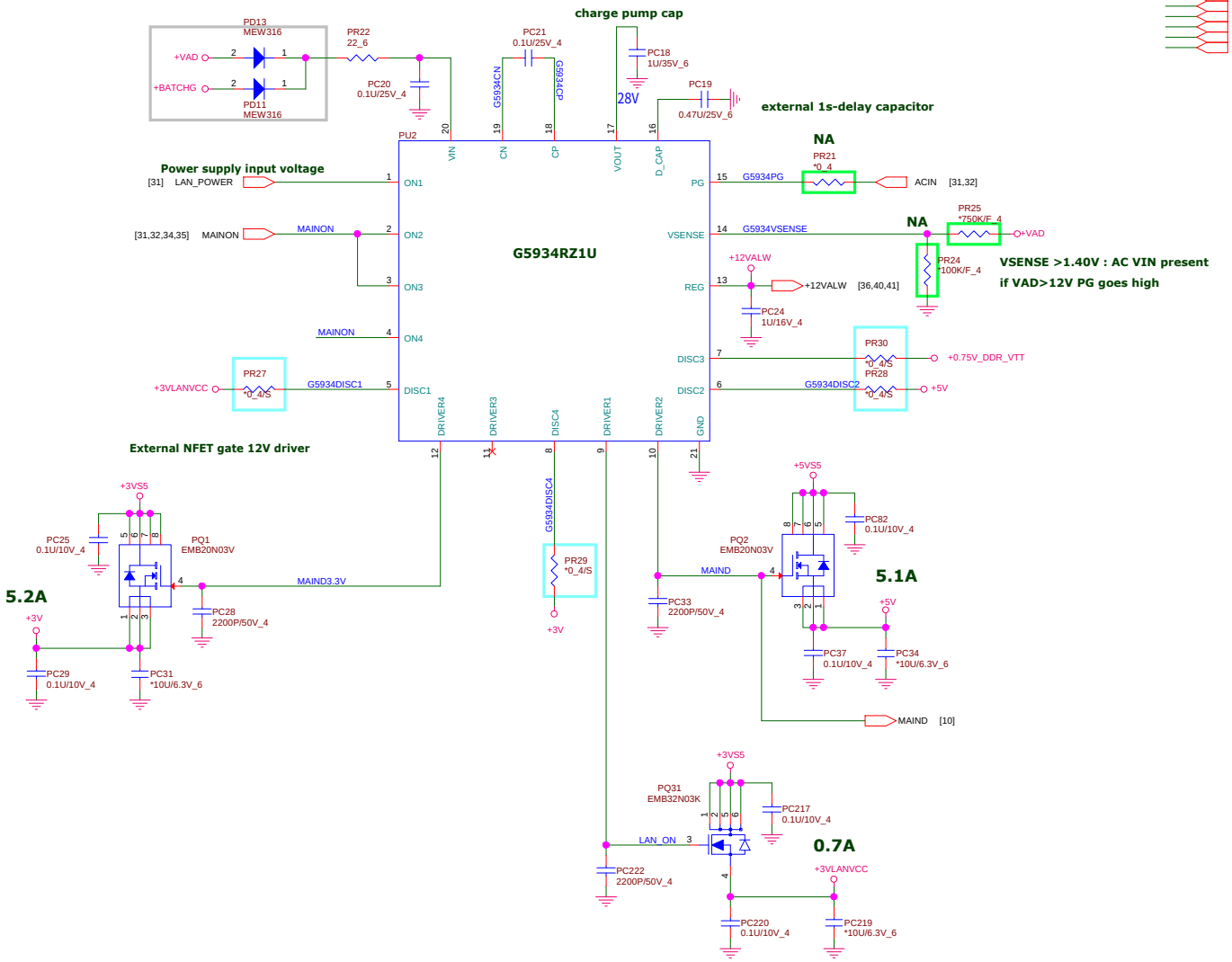
+5V [7,21,25,26,29,30,39]
+VIN [23,29,32,33,34,35,37,39,40,41]
+1.5V [6,7,8,10,25,26,29,30,35]
+3VS5 [2,6,7,9,10,26,28,29,31,33,35,41]
+5VS5 [25,28,29,33,34,35,37,38,39,40]
+VAD [32]
+12VALW [36,40,41]
+3VLANVCC [7,27]
+0.75V_DDR_VTT [12,13,35]



0/P will be change to shaort pad before PV

NB5	PROJECT : TWK Quanta Computer Inc.	
Size: Custom	Document Number: Dis-charge IC (G5934)	Rev: 1A
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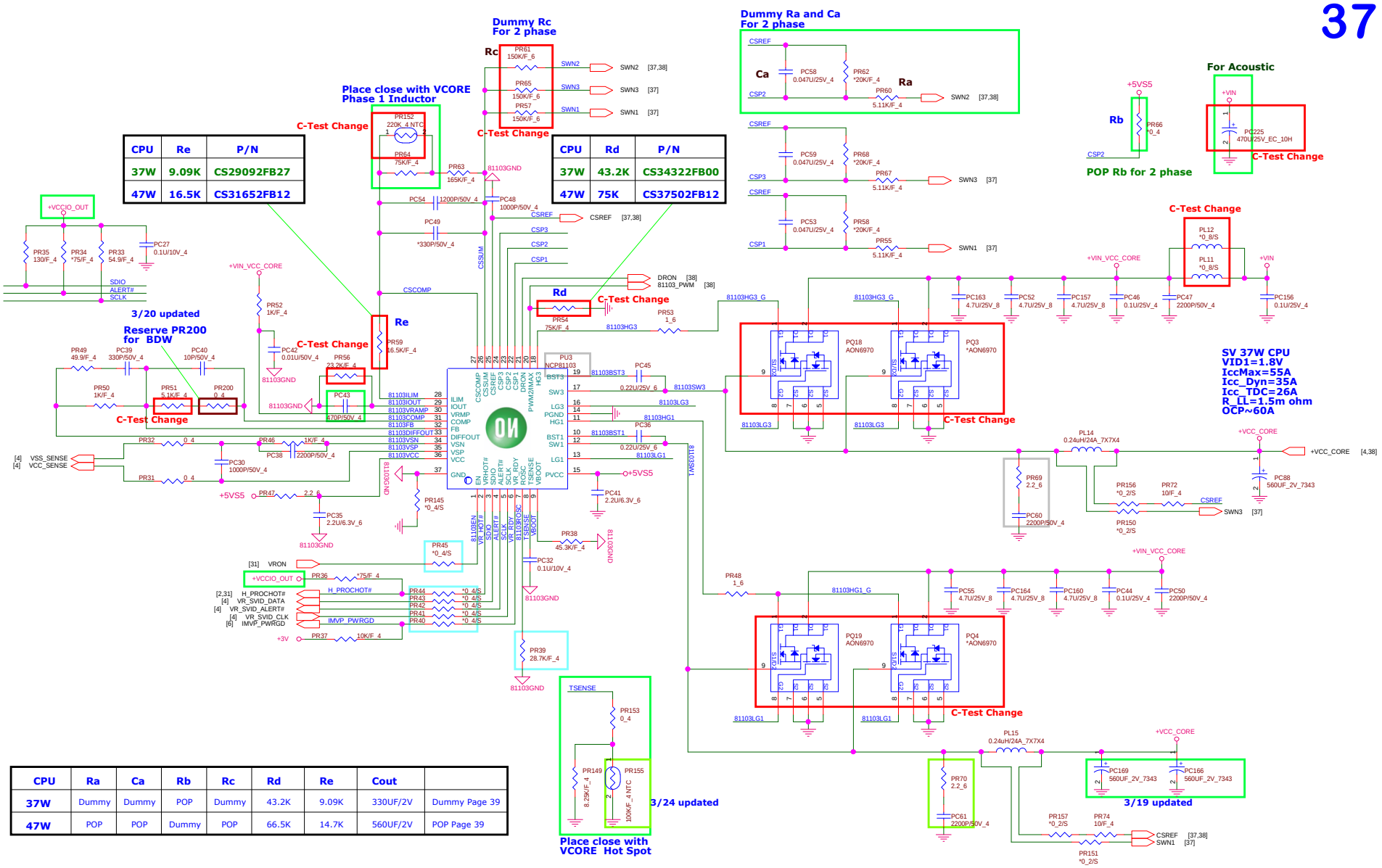
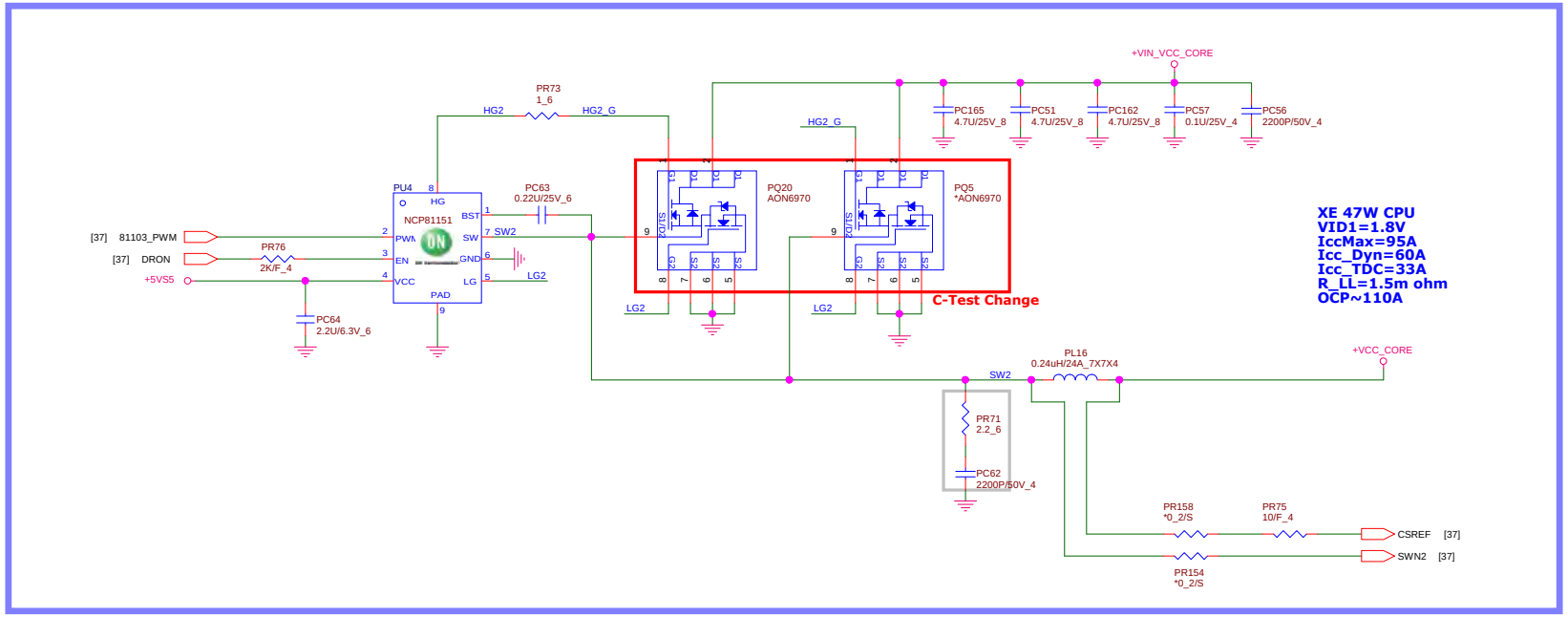


CPU	Re	P/N
37W	9.09K	CS29092FB27
47W	16.5K	CS31652FB12

CPU	Rd	P/N
37W	43.2K	CS34322FB00
47W	75K	CS37502FB12

CPU	Ra	Ca	Rb	Rc	Rd	Re	Cout	
37W	Dummy	Dummy	POP	Dummy	43.2K	9.09K	330UF/2V	Dummy Page 39
47W	POP	POP	Dummy	POP	66.5K	14.7K	560UF/2V	POP Page 39

NB5	PROJECT : TWK Quanta Computer Inc.		
	Size: C	Document Number: Dis-charge IC (G5934)	Rev: 1A
	Date: Wednesday, April 23, 2014	Sheet 37 of 42	



NB5	PROJECT : TWK Quanta Computer Inc.	
Size: Custom	Document Number: NCP81151	Rev: 1A
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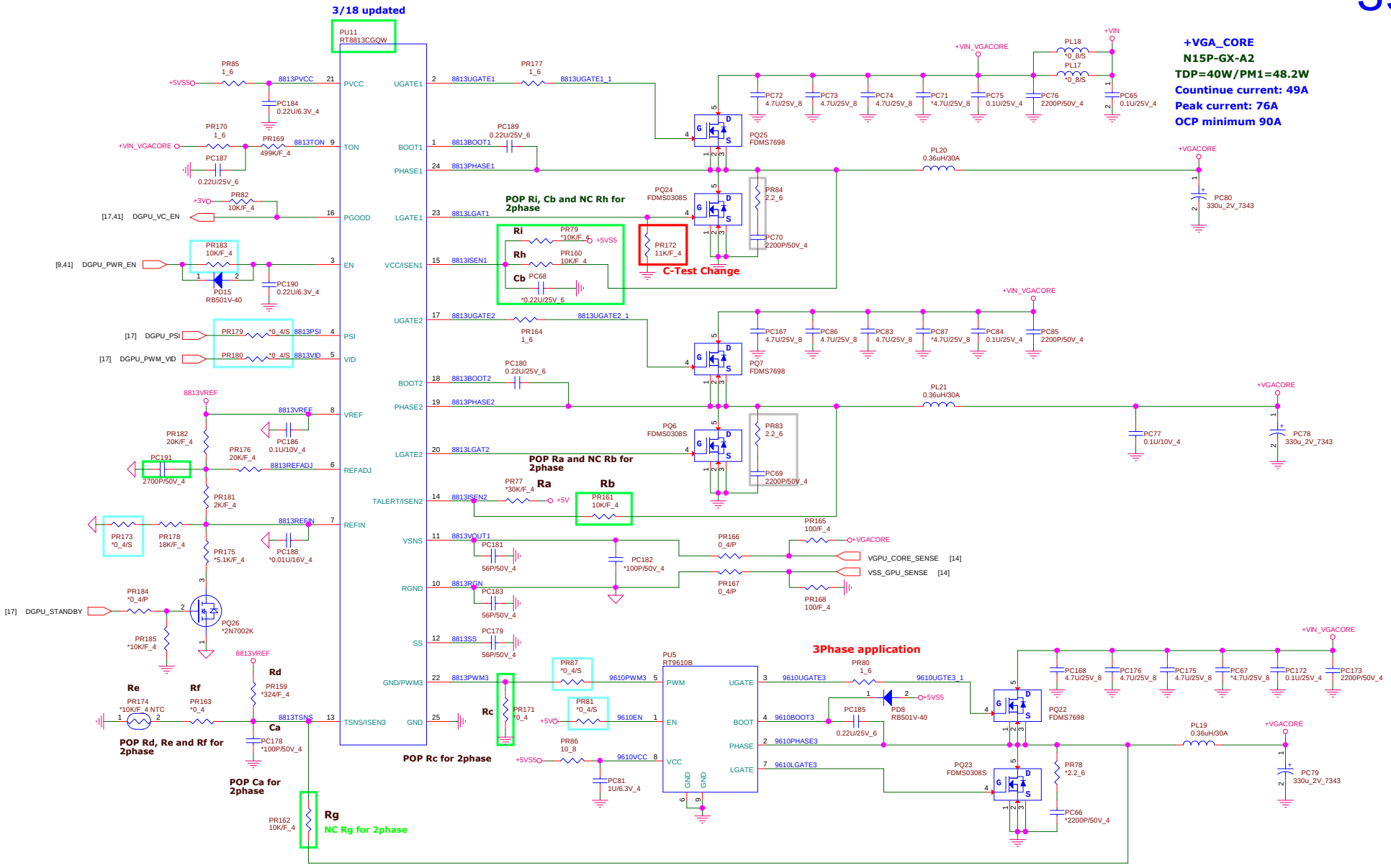
3/18 updated
PU11
RT8813CGQW
+VGA_CORE
N15P-GX-A2
TDP=40W/PM1=48.2W
Countinue current: 49A
Peak current: 76A
OCP minimum 90A
POP Ri, Cb and NC Rh for 2phase
C-Test Change
POP Ra and NC Rb for 2phase
POP Rc for 2phase
POP Rd, Re and Rf for 2phase
POP Ca for 2phase
NC Rg for 2phase
3Phase application
PU5
RT9610B
PQ25 FDMS7698
PQ24 FDMS0308S
PQ7 FDMS7698
PQ6 FDMS0308S
PQ22 FDMS7698
PQ23 FDMS0308S
PQ26 *2N7002K
PD15 RB501V-40
PD8 RB501V-40
PL18 *0_8/S
PL17 *0_8/S
PL20 0.36uH/30A
PL21 0.36uH/30A
PL19 0.36uH/30A
PC80 330u_2V_7343
PC78 330u_2V_7343
PC79 330u_2V_7343
VGPU_CORE_SENSE [14]
VSS_GPU_SENSE [14]
PROJECT : TWK
Quanta Computer Inc.
NB5
+VGA CORE (NCP3218G)
Wednesday, April 23, 2014
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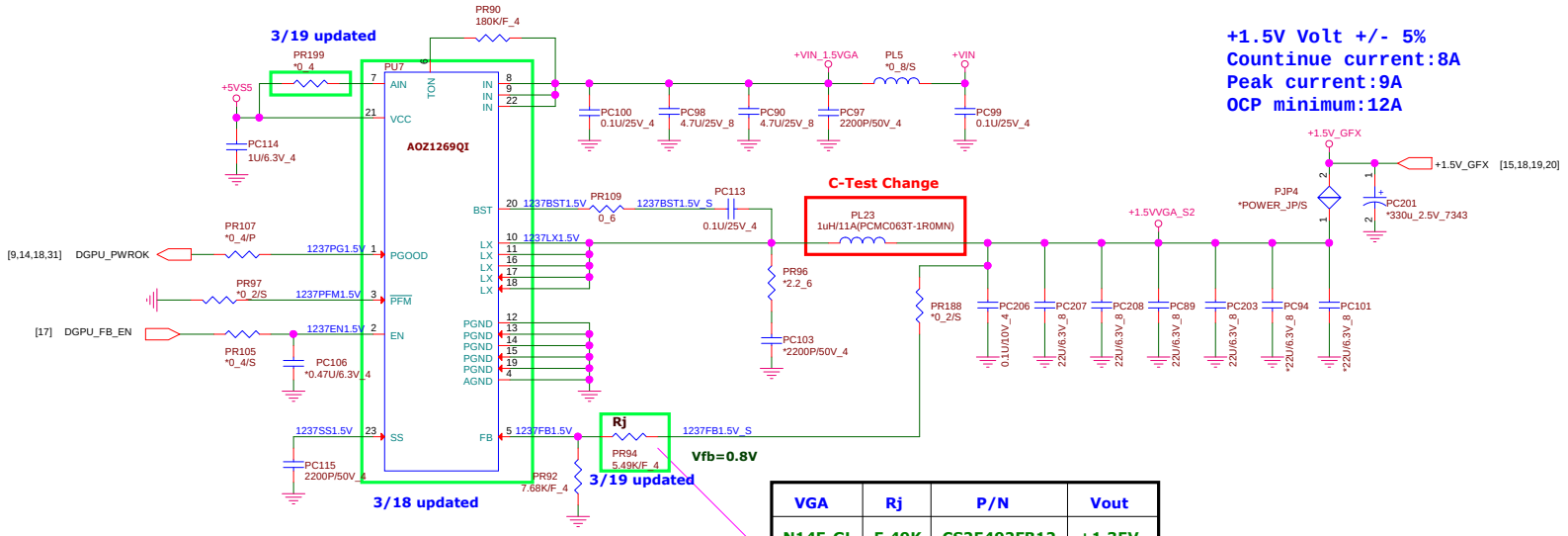
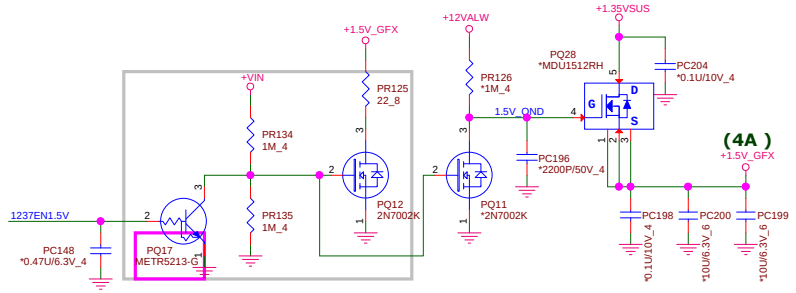


VGA	Rj	P/N	Vout
N14E-GL	5.49K	CS25492FB12	+1.35V
N14P-GT	6.98K	CS26982FB01	+1.5V



NB5	PROJECT : TWK Quanta Computer Inc.	
	Size: Custom Document Number: +VGA POWER	Rev: A
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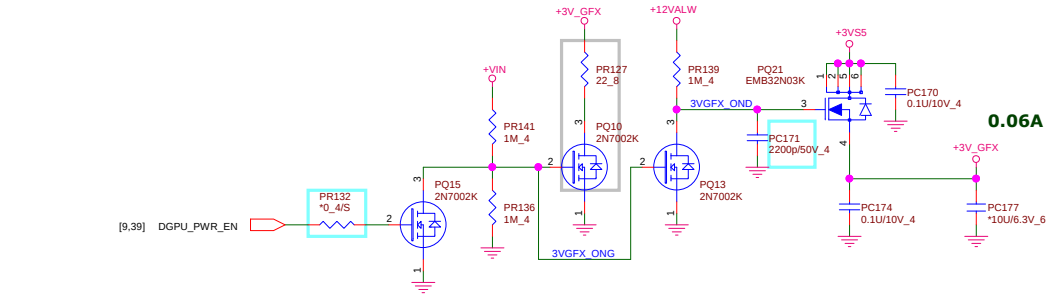

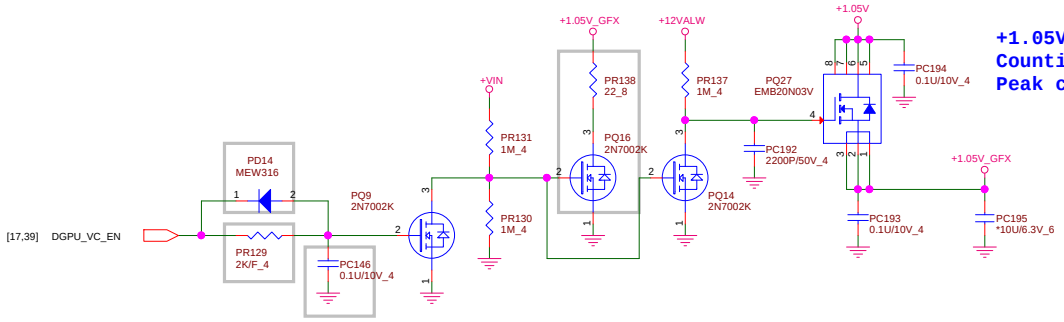

NB5	PROJECT : TWK Quanta Computer Inc.	
Size: Custom	Document Number: +VGACORE (RT8208/1.8V)	Rev: 1A
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