Ares-2 (LAR-2)
Tigerlake-UP3 Schematics

Project Code : 4PD0LL010001
PCB(Raw Card) : 19837-1

2020-08-01

DY	DUMMY
PCBID	PCB NO. control for SW
SKUID	CPU Type change for SW
MEM_ID	Memory ID for SW
DDR4_CTRL	SDP DDP setting
SDP/DDP	Select single DIE (SDP) Dual DIE(DDP)
APS/ISH/LPC/XDP	Debug Connectors
EMC	For EMC test request
NON_PSL/PSL	KBC PSL model control
CHARGER_HS/CHARGER_LS	Charger High/Low side MOSFET
VCCSA_HS/VCCSA_LS	VCCSA High/Low Side MOSFET
YOGA	YOGA model setting
ZZ	For Test Piont /Hole /ShortPad

LAR-2

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Title: COVER PAGE

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 1 of 106

Ares-2 Tigerlake-UP3 Block Diagram

Project Code: 4PD0LL010001
PCB(Raw Card): 19837-SB

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating	Size
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

0402=> 1/16W, 25V
0603 => 1/16W, 75V
0805 => 1/10W, 100V

2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DESCRIPTION

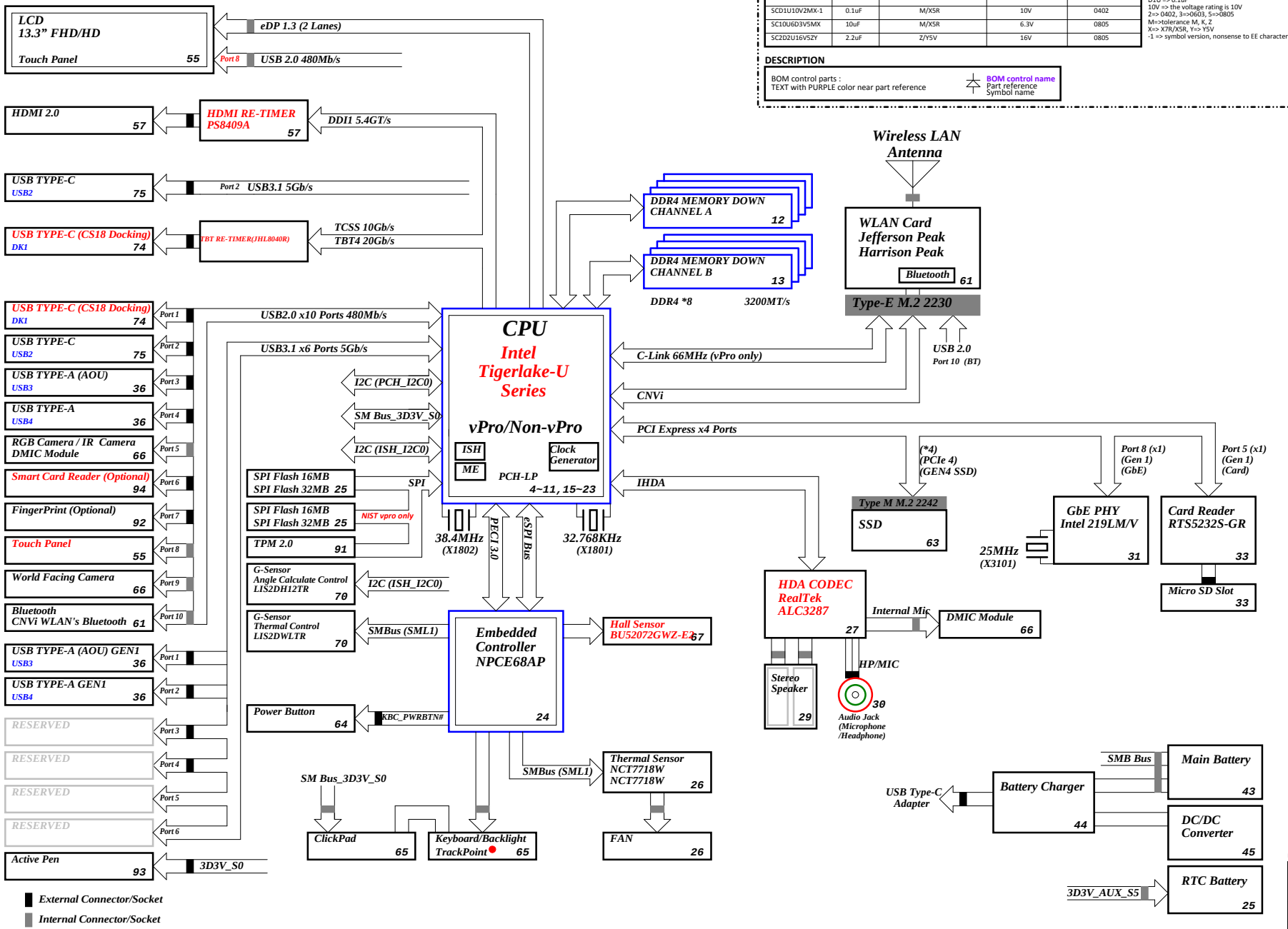
BOM control parts :
TEXT with PURPLE color near part reference

BOM control name
Part reference
Symbol name

PCB Layer Stackup

8 Layers FR4 (8-1.0-15L)
L1: Component (TOP)
L2: Signal / GND / POWER
L3: Signal / GND / POWER
L4: Signal / GND / POWER
L5: Signal / GND / POWER
L6: Signal
L7: GND / POWER
L8:Component (BOTTOM)

Battery Charger/Selector BQ25710ARSNR 44	
20V_VINT_IN	19V_DCBATOUT BT+
System DC/DC 5V TPS51395RJER 45	
19V_DCBATOUT	5V_S5
System DC/DC 3D3V TPS51393RJER 45	
19V_DCBATOUT	3D3V_S5
DC/DC IMVP8 NCP81218MNTXG 46	
DC/DC VCCCPUCORE NCP302045LMNTWG 47	
19V_DCBATOUT	1V_CPU_CORE
DC/DC VCCGT NCP302035LMNTWG 48	
19V_DCBATOUT	1V_VCCGT
DC/DC VCCSA NCP81253MNTBG 50	
19V_DCBATOUT	1V_VCCSA
DC/DC DDR4 VDDQ TPS51486RJER 51	
19V_DCBATOUT	1D2V_S3
DC/DC DDR4 VTT TPS51486RJER 51	
1D2V_S3	0D6V_VREF_S0
DC/DC DDR4 VPP TPS51486RJER 51	
5V_S5	2D5V_S3
DC/DC 1D05V_SUS TPS51396RJER 52	
19V_DCBATOUT	1D05V_SUS
DC/DC 1D8V_SUS RT5797ALGQW 53	
3D3V_S5	1D8V_SUS



LAR-2

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Title: **BLOCK DIAGRAM**

Size	Document Number	Rev
A2	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 2 of 106

24 PECI_CPU
15,99 DBG_PMODE
24,44,46,73 PROCHOT_CPU_N
40 THERMTRIP_CPU_N

61 CNV_UART_WAKE
61 BLUETOOTH_EN_CPU

CPU1U

CPU_CATERR M7 CATERR#
PECI_CPU BK9 PECI
PROCHOT_CPU_R_N E2 PROCHOT#
THERMTRIP_CPU_N M5 THRMTRIP#

CPU_POPI_RCOMP CT39 PROC_POPIRCOMP
PCH_OPI_RCOMP CB9 PCH_OPIRCOMP
CW12 TP#CW12
CM39 TP#CM39

DBG_PMODE DF4 DBG_PMODE

BLUETOOTH_EN_CPU DB42 GPP_B4/CPU_GP3
DB41 GPP_B3/CPU_GP2
DF8 GPP_E7/CPU_GP1
DU5 GPP_E3/CPU_GP0

DF31 GPP_H2
DV32 GPP_H1
DW32 GPP_H0

CNV_UART_WAKE DJ27 GPP_H19/TIME_SYNC0

TGL-U-1-GP-U2

ZZ.00CPU.481

21 0F 21

PROC_TRST# K4 PROC_TRST_N
PROC_TMS B9 PROC_TMS
PROC_TDO D12 PROC_TDO
PROC_TDI A12 PROC_TDI
PROC_TCK B6 PROC_TCK

PCH_JTAGX D8
PCH_TMS A9
PCH_TDO E12
PCH_TDI B12
PCH_TCK A7 PCH_JTAG_TCK
PCH_TRST# H4

PROC_PREQ# C11 PROC_PREQ_N
PROC_PRDY# D11 PROC_PRDY_N

EAR_N/EAR_N_TEST_NCTF G1 CPU_EAR

GPP_F7 DT15
GPP_F9 DR15
GPP_F10 DT14

PROC_TRST_N 99
PROC_TMS 99
PROC_TDO 99
PROC_TDI 99
PROC_TCK 99
PCH_JTAG_TCK 99
PROC_PREQ_N 99
PROC_PRDY_N 99
CPU_EAR 99

3D3V_SUS
R314 1 2 10KR2J-3-GP CNV_UART_WAKE

1D05V_VCCSTG_TERM
DY R308 1 2 51R2J-2-GP PROC_PREQ_N
XDP R311 1 2 51R2J-2-GP PROC_TDI
XDP R312 1 2 51R2J-2-GP PROC_TMS
DCI XDP R309 1 2 51R2J-2-GP PROC_TDO
DCI XDP R310 1 2 51R2J-2-GP PROC_TCK
DY RN304 SRN51J-GP
1 4 PROC_TRST_N
2 3 PCH_JTAG_TCK
R305 1 2 49D9R2F-GP CPU_POPI_RCOMP
R306 1 2 49D9R2F-GP PCH_OPI_RCOMP

1D05V_VCCSTG_TERM
R302 1KR2J-1-GP
PROCHOT_CPU_N
R303 1 2 499R2F-GP PROCHOT_CPU_R_N

1D05V_VCCST
R304 1 2 1KR2J-1-GP THERMTRIP_CPU_N
R307 1 2 1KR2J-1-GP CPU_CATERR

1D05V_VCCSTG
R313 1 2 1KR2J-1-GP CPU_EAR

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Title: CPU (THML/JTAG)

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 3 of 106

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
24 eDP_BLEN_CPU
55 EDP_VDD_EN
55 L_BKLT_CTRL
55 eDP_HPD_CPU

DK1

71 DK1_TCSS_TX_N0
71 DK1_TCSS_TX_P0
71 DK1_TCSS_TX_N1
71 DK1_TCSS_TX_P1
71 DK1_TCSS_RX_N0
71 DK1_TCSS_RX_P0
71 DK1_TCSS_RX_N1
71 DK1_TCSS_RX_P1
71 DK1_TCSS_AUX_N
71 DK1_TCSS_AUX_P
71 DK1_TCSS_TX_LSX2
15,71 DK1_TCSS_RX_LSX2

USB-C

75 USB2_TCSS_TX_N0
75 USB2_TCSS_TX_P0
75 USB2_TCSS_TX_N1
75 USB2_TCSS_TX_P1
75 USB2_TCSS_RX_N0
75 USB2_TCSS_RX_P0
75 USB2_TCSS_RX_N1
75 USB2_TCSS_RX_P1
75 USB2_TCSS_AUX_N
75 USB2_TCSS_AUX_P
75 USB2_TCSS_AUX_CR_N
75 USB2_TCSS_AUX_CR_P

HDMI

57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_SCL_CPU
57 HDMI_SDA_CPU
57 HDMI_HPD_CPU

Others

15 TBT_LSX3_VCC_CONFIG
15 TBT_LSX1_VCC_CONFIG
73 USB_TCSS_OC1_N
73 USB_TCSS_OC2_N

NOTE:
"eDP_HPD_CPU"
"eDP_VDDEN_CPU"
"eDP_BLEN_CPU"
PD 100K to LCD side

3D3V_S0 — R403 2K2R2J-L1-GP — EDP_SDA

TP401 TP402 — 1DDI_AUX_P / 1DDI_AUX_N

CPU1A — 1 OF 21

AC2	DDIA_TXP3	
AC1	DDIA_TXN3	
AD2	DDIA_TXP2	
AD1	DDIA_TXN2	
AF1	DDIA_TXP1	eDP_TX_CPU_P1
AF2	DDIA_TXN1	eDP_TX_CPU_N1
AG2	DDIA_TXP0	eDP_TX_CPU_P0
AG1	DDIA_TXN0	eDP_TX_CPU_N0
AJ2	DDIA_AUX_P	eDP_AUX_CPU_P
AJ1	DDIA_AUX_N	eDP_AUX_CPU_N
DN4	GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD	
DT6	GPP_E23/DDPA_CTRLDATA	EDP_SDA
DR5	GPP_E14/DDSP_HPDA/DISP_MISCA	eDP_HPD_CPU
T12	DDIB_TXP3	HDMI_DDI_TX_P3
T11	DDIB_TXN3	HDMI_DDI_TX_N3
Y11	DDIB_TXP2	HDMI_DDI_TX_P2
Y9	DDIB_TXN2	HDMI_DDI_TX_N2
T9	DDIB_TXP1	HDMI_DDI_TX_P1
P9	DDIB_TXN1	HDMI_DDI_TX_N1
V11	DDIB_TXP0	HDMI_DDI_TX_P0
V9	DDIB_TXN0	HDMI_DDI_TX_N0
AB9	DDIB_AUX_P	1DDI_AUX_P
AD9	DDIB_AUX_N	1DDI_AUX_N
DM29	GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN	HDMI_SCL_CPU
DK27	GPP_H17/DDPB_CTRLDATA	HDMI_SDA_CPU
DG43	GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD	HDMI_HPD_CPU
DG47	GPP_A21/DDPC_CTRLCLK/I2S5_TXD	
DJ47	GPP_A22/DDPC_CTRLDATA/I2S5_RXD	
DU8	GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD	USB2_TCSS_AUX_CR_N
DV8	GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD	USB2_TCSS_AUX_CR_P
DF6	GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD	
DD6	GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD	TBT_LSX1_VCC_CONFIG
DN23	GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#	DK1_TCSS_TX_LSX2
DM23	GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK	DK1_TCSS_RX_LSX2
DK23	GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO	
DN21	GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI	TBT_LSX3_VCC_CONFIG
DF43	GPP_A17/DISP_MISCC/I2S4_TXD	
DF45	GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK	
DF47	GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM	
DH52	GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1	USB_TCSS_OC1_N
DK45	GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK	USB_TCSS_OC2_N
DM8	EDP_VDDEN	EDP_VDD_EN
DN8	EDP_BKLTEN	eDP_BLEN_CPU
DG10	EDP_BKLTCTL	L_BKLT_CTRL

TGL-U-1-GP-U2

AY2	USB2_TCSS_RX_P1	TCP0_TXRX_P1
AY1	USB2_TCSS_RX_N1	TCP0_TXRX_N1
BB1	USB2_TCSS_RX_P0	TCP0_TXRX_P0
BB2	USB2_TCSS_RX_N0	TCP0_TXRX_N0
AM5	USB2_TCSS_TX_P1	TCP0_TX_P1
AM7	USB2_TCSS_TX_N1	TCP0_TX_N1
AT7	USB2_TCSS_TX_P0	TCP0_TX_P0
AT5	USB2_TCSS_TX_N0	TCP0_TX_N0
AP7	USB2_TCSS_AUX_P	TCP0_AUX_P
AP5	USB2_TCSS_AUX_N	TCP0_AUX_N
AT2		TCP1_TXRX_P1
AT1		TCP1_TXRX_N1
AU1		TCP1_TXRX_P0
AU2		TCP1_TXRX_N0
AD5		TCP1_TX_P1
AD7		TCP1_TX_N1
AH7		TCP1_TX_P0
AH5		TCP1_TX_N0
AF7		TCP1_AUX_P
AF5		TCP1_AUX_N
BF1	DK1_TCSS_RX_P1	TCP2_TXRX_P1
BF2	DK1_TCSS_RX_N1	TCP2_TXRX_N1
BE2	DK1_TCSS_RX_P0	TCP2_TXRX_P0
BE1	DK1_TCSS_RX_N0	TCP2_TXRX_N0
BD7	DK1_TCSS_TX_P1	TCP2_TX_P1
BD5	DK1_TCSS_TX_N1	TCP2_TX_N1
AY5	DK1_TCSS_TX_P0	TCP2_TX_P0
AY7	DK1_TCSS_TX_N0	TCP2_TX_N0
BB5	DK1_TCSS_AUX_P	TCP2_AUX_P
BB7	DK1_TCSS_AUX_N	TCP2_AUX_N
BK1		TCP3_TXRX_P1
BK2		TCP3_TXRX_N1
BJ2		TCP3_TXRX_P0
BJ1		TCP3_TXRX_N0
BM7		TCP3_TX_P1
BM5		TCP3_TX_N1
BH5		TCP3_TX_P0
BH7		TCP3_TX_N0
BK5		TCP3_AUX_P
BK7		TCP3_AUX_N
AN2	TCSS_RCOMP_P	TC_RCOMP_P
AN1	TCSS_RCOMP_N	TC_RCOMP_N
M8		DSI_DE_TE_2
AB1	DISP_RCOMP	DDI_RCOMP
CE4		DISP_UTILS/DSI_DE_TE_1

R402 150R2F-4-L-GP
R401 150R2F-1-GP

LAR-2

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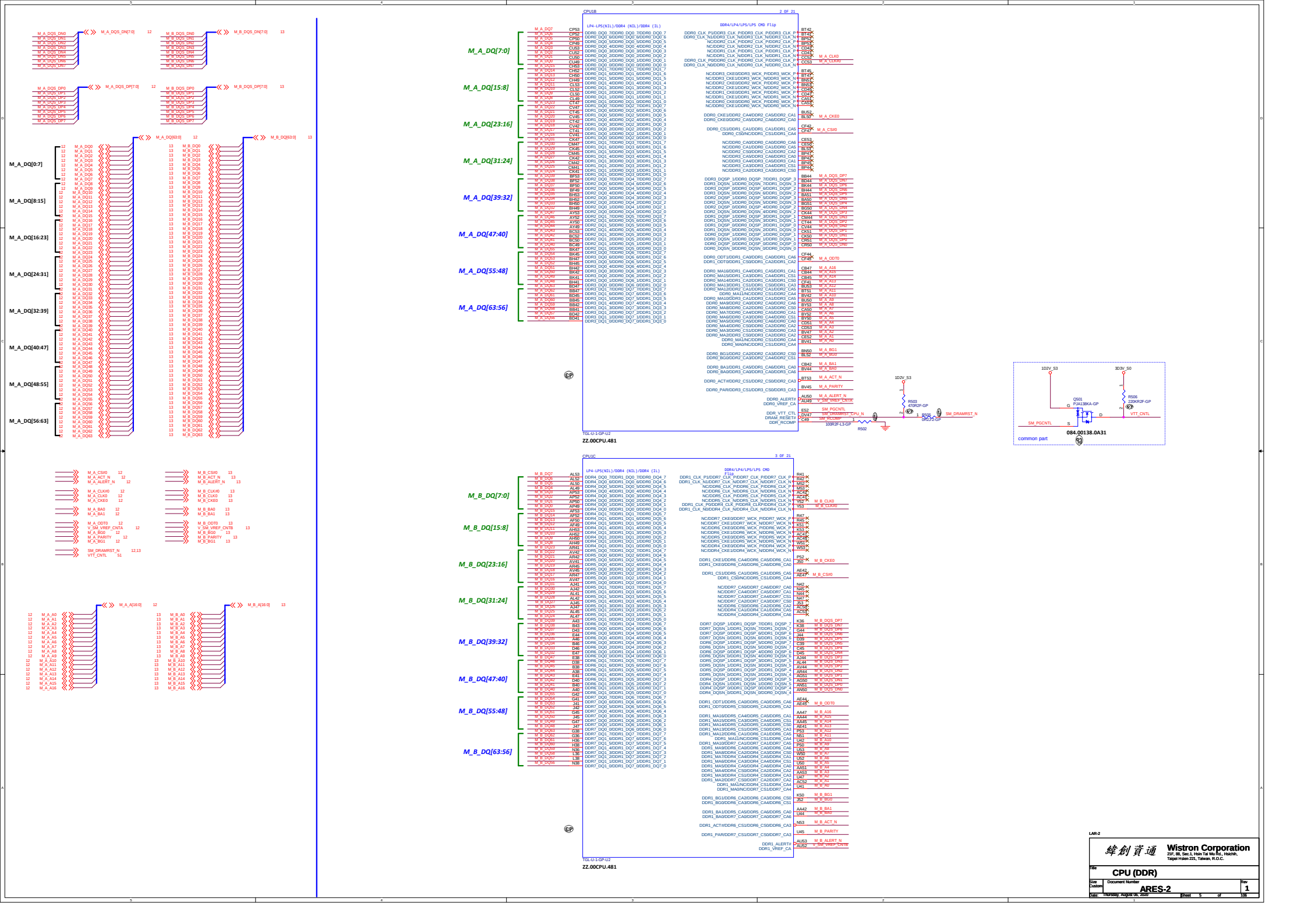
Title: **CPU (DDI/EDP/TBT/TPC/)**

Size	Document Number	Rev
A3	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 4 of 106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M_A_DQ[40:47]
M_A_DQ[48:55]
M_A_DQ[56:63]
M_B_DQ[0:7]
M_B_DQ[8:15]
M_B_DQ[16:23]
M_B_DQ[24:31]
M_B_DQ[32:39]
M_B_DQ[40:47]
M_B_DQ[48:55]
M_B_DQ[56:63]
CPU1B
2 OF 21
CPU1C
3 OF 21
TGL-U-1-GP-U2
ZZ.00CPU.481
common part
084.00138.0A31
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CPU (DDR)
ARES-2
LAR-2

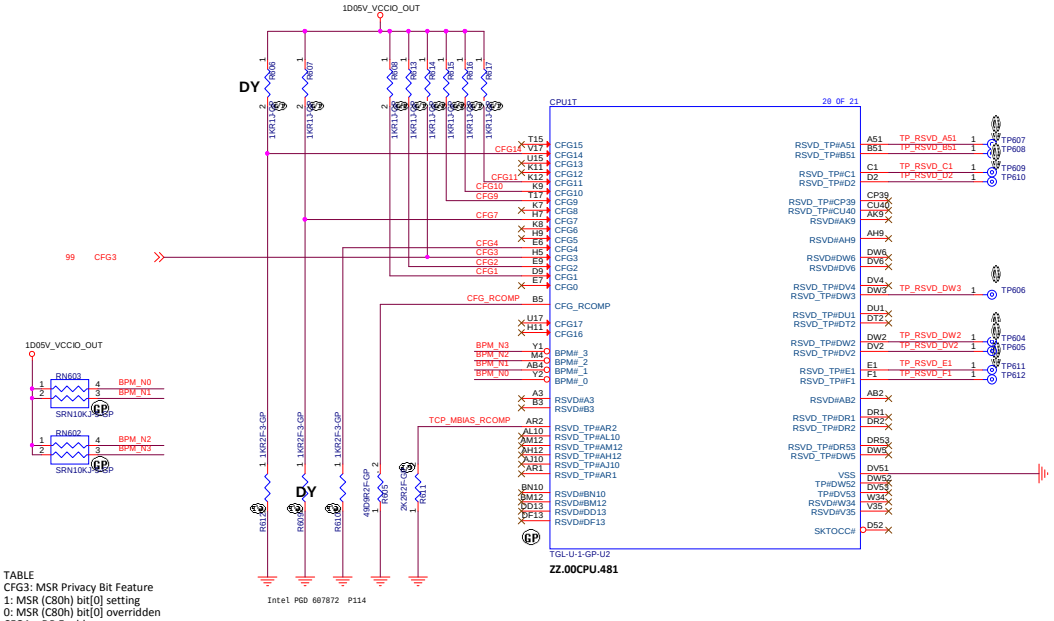

TABLE
CFG3: MSR Privacy Bit Feature
1: MSR (C80h) bit[0] setting
0: MSR (C80h) bit[0] overridden
CFG4: eDP Enable
1:Disabled
0:Enabled
CFG9: SVID Bus Communication
1:Enabled
0:Disabled
CFG14: PEG60 Lane Reversal
1:Normal
0:Reversed

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Title: CPU (CFG/IST)

Size: A2 | Document Number: ARES-2 | Rev: 1

Date: Thursday, August 06, 2020 | Sheet 6 of 106

46 VCCCORE_SENSE
46 VSSCORE_SENSE
46 SVID_ALERT_CPU_N
46 SVID_CLK_CPU
46 SVID_DATA_CPU

1V_CPU_CORE

CPU1M

13 0F 21

1V_CPU_CORE

A24 A26 A29 A30 A33 A35 AY39 B24 B26 B29 B30 B33 B35 BA10 BA40 BB39 BB9 BC10 BC40 BD39 BD9 BE10 BE40 BF9 BG10 BG40 BH12 BH39 BH9 BJ10 BJ40 BK39 BL10 BL40 BM39 BN40 BP12 BP39 BR10 BR40 BT12 BT39 BU10 BU40 BV12 BY12 CA10 CB12 D24 D26 D29 D30 D33 D35 E24 E26 E27 E29 E30 E32 E33 G2 G24 G26 G30 — VCCIN

G32 H24 H26 H30 H32 J1 J2 K1 K2 K24 K26 K30 K32 L24 L26 L30 L32 N24 N26 N30 N32 P24 P26 P28 P30 P32 T21 T23 T25 T27 T31 U23 U27 U29 U31 U33 V23 V25 V27 V29 V31 V33 W22 W24 W28 W32 — VCCIN

VCCIN_SENSE — R38 — VCCCORE_SENSE
VSSIN_SENSE — R37 — VSSCORE_SENSE

VIDSOUT — M12 — SVID_DATA_CPU
VIDSCK — M11 — SVID_CLK_CPU
VIDALERT# — P12 — SVID_ALERT_CPU_R_N

TGL-U-1-GP-U2

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SVID DATA

1D05V_VCCST

1 R703 2 SVID_DATA_CPU
100R2F-L1-GP-U

SVID ALERT

1D05V_VCCST

R701
56R2J-4-GP

SVID_ALERT_CPU_N — 1 R706 2 — SVID_ALERT_CPU_R_N
0R402-DB-GP-U

Layout note:
3.Length matchin 25mil, and close SOC in 2inch "

1V_CPU_CORE

R704 1 2 VCCCORE_SENSE
100R2F-L1-GP-U

R705 1 2 VSSCORE_SENSE
100R2F-L1-GP-U

Layout Note:

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

LAR-2

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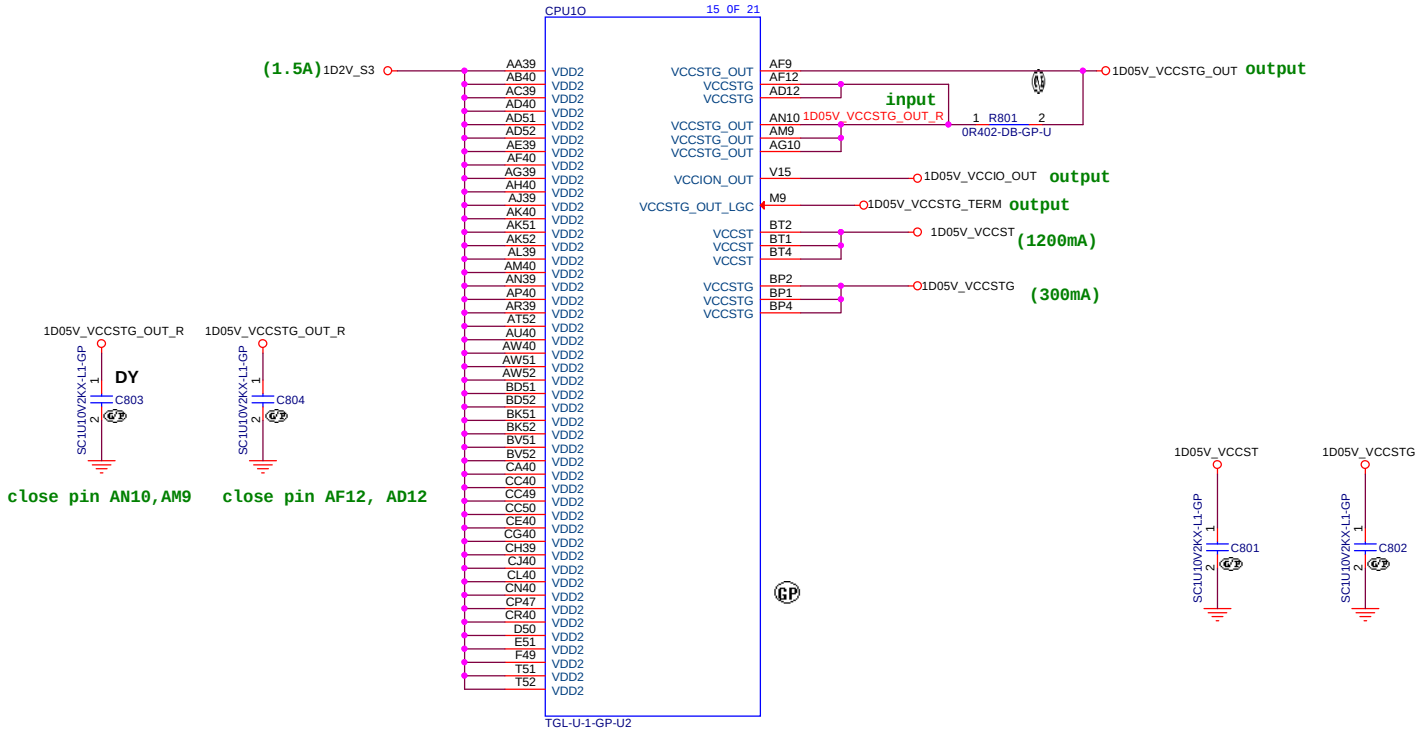
Title: **CPU (VCCIN/VID)**

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 7 of 106



ZZ.00CPU.481

Lack of VCCPLL_OC / VCC1P8A / VCCPLL

LAR-2

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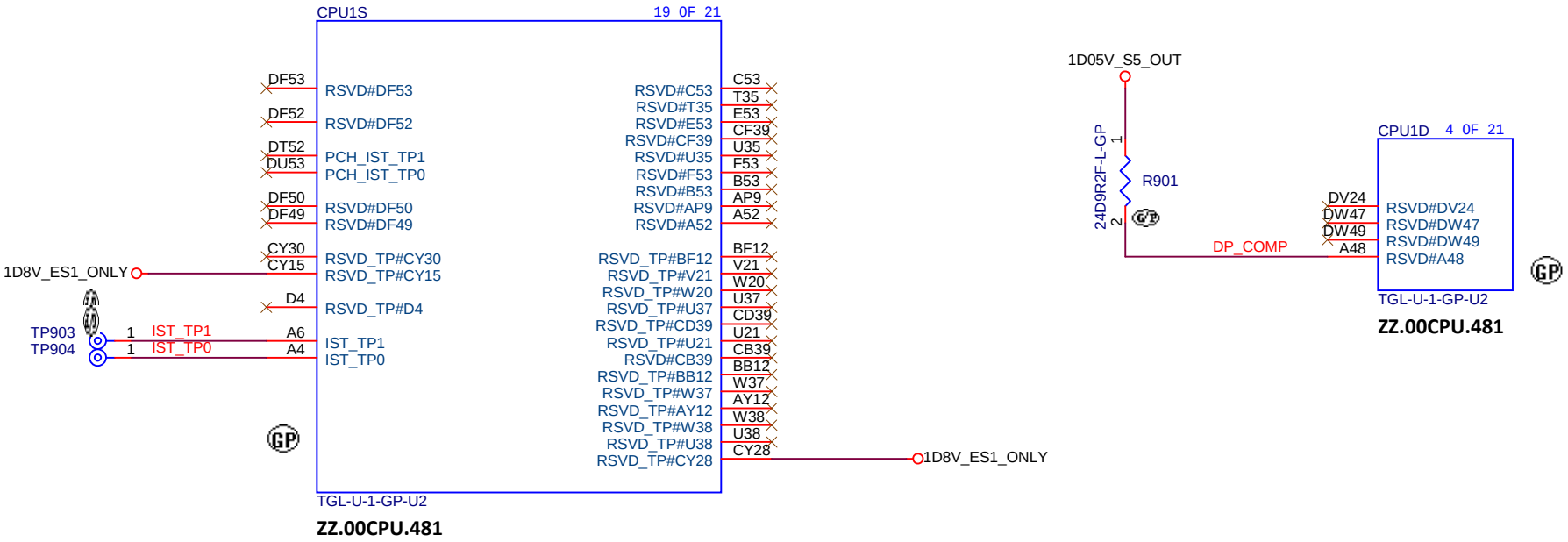
Title: **CPU (VDDQ/VCC/VCCST)**

Size	Document Number	Rev
A3	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 8 of 106



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Title: **CPU (RSVD)**

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 9 of 106

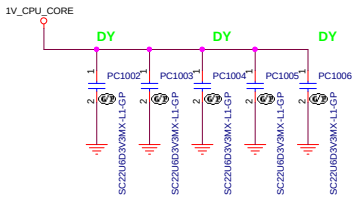
Main Func = CPU

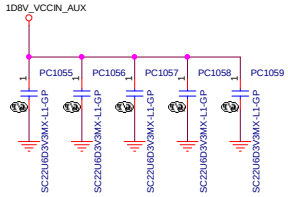
VCORE

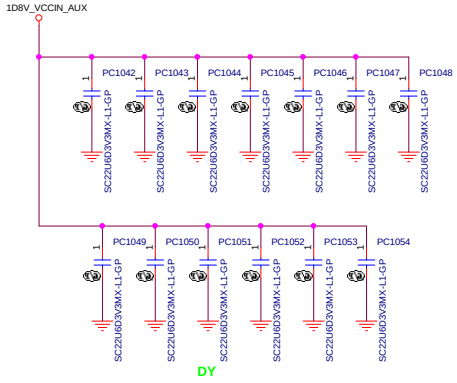
ICL_U42

U42
IccMax current-10ms max = 70 A

22uF	PCS	Cap
U42	15	330uF*1



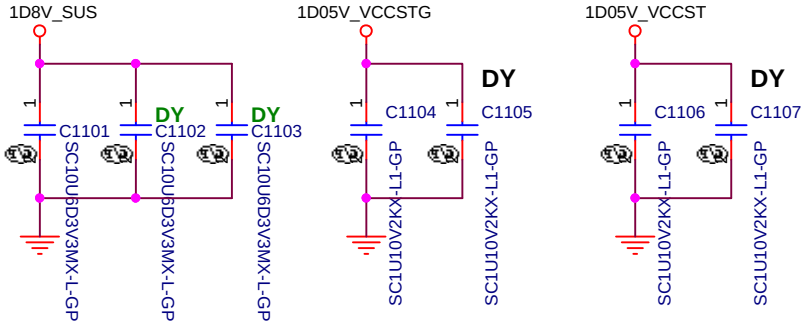




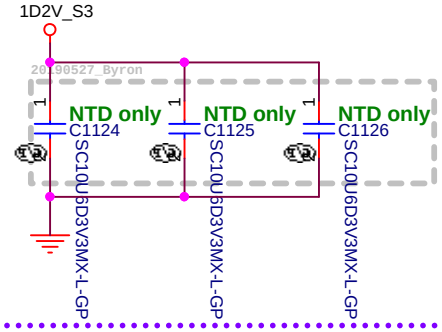
LAR-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

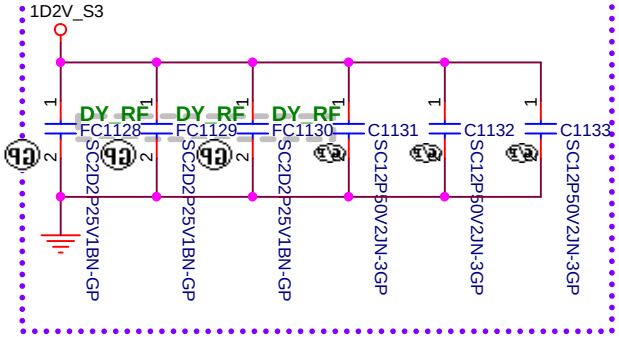
Title	CPU_(Power CAP1)	
Size: Custom	Document Number: ARES-2	Rev: 1
Date: Thursday, August 06, 2020	Sheet 10 of 106	



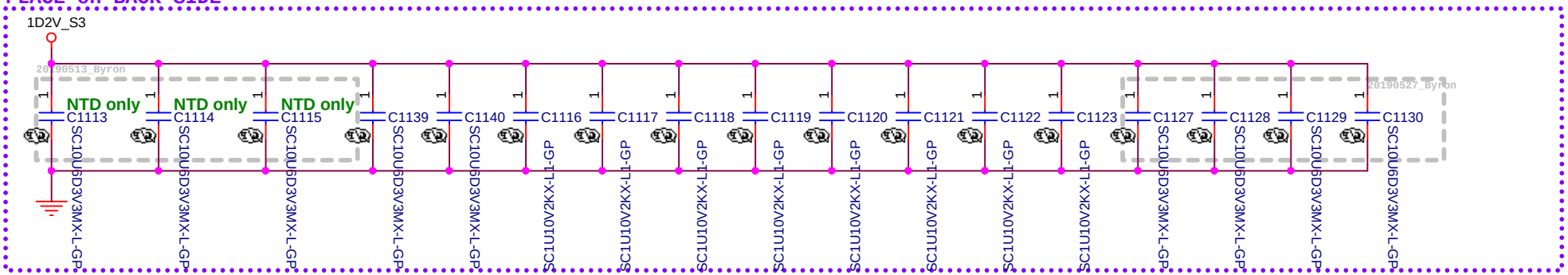
PLACE on CPU Same Side



EMC CAPS - PLACE <4mm FROM SOC VDDQ, WITH EACH PAIR <12mm APART



PLACE on BACK SIDE



LAR-2

緯創資通 **Wistron Corporation**
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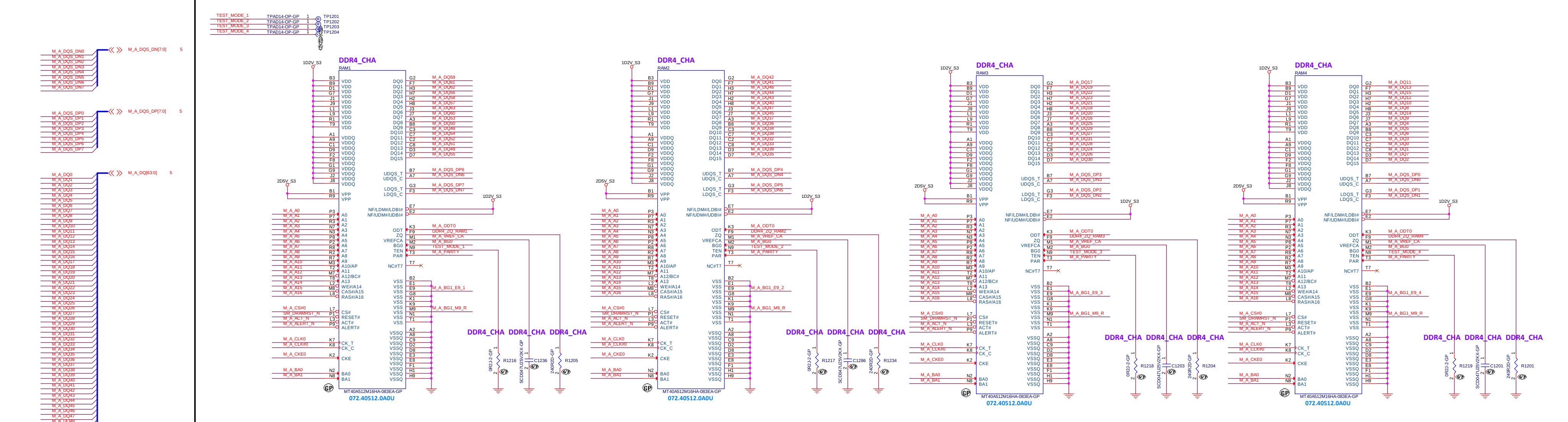
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (Power Cap2)**

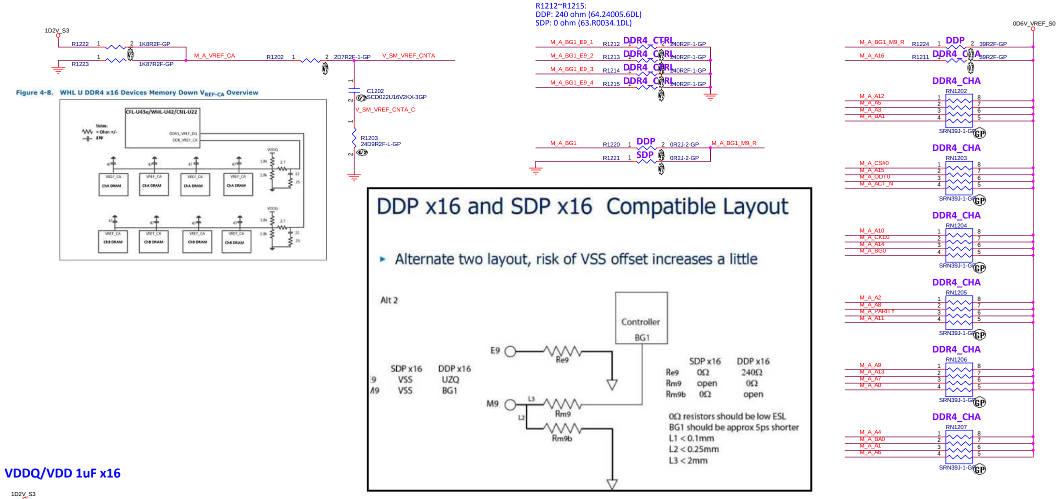
Size	Document Number	Rev
A4	**ARES-2**	1

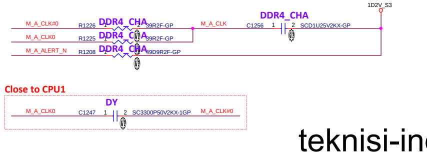
Date: Thursday, August 06, 2020 Sheet 11 of 106



SDP & DDP SETTING

R1212~R1215:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)





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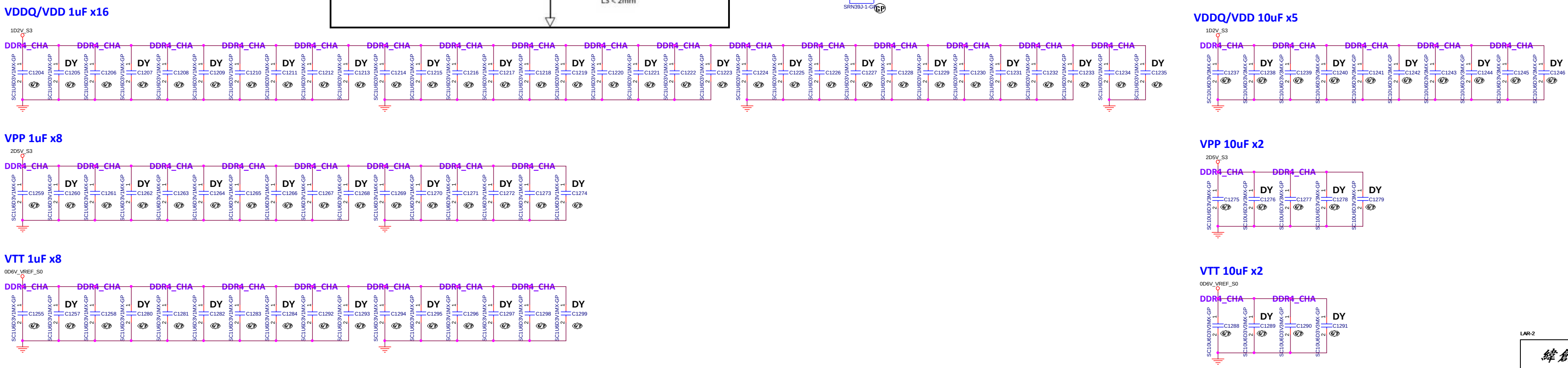
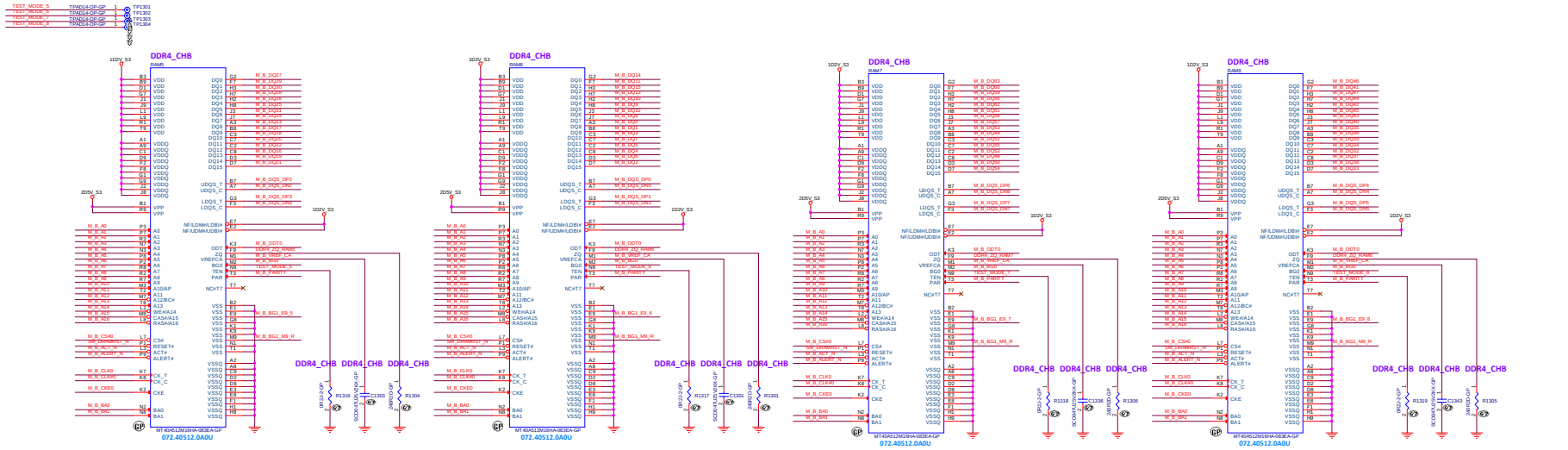
SDP and DDP BOM Control Table

		SDPx16 16Gb			DDPx16 32Gb		
		SM30N76568AA Samsung K4AAG165WA-BCTD	TBD SK Hynix TBD	TBD Micron TBD	SM30N76569AA Samsung K4ABG165WA-MCTD	TBD SK Hynix TBD	TBD Micron TBD
DDR4_CTRL	R1212 R1213 R1214 R1215	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	240R 1% 240R 1% 240R 1% 240R 1%	240R 1% 240R 1% 240R 1% 240R 1%	240R 1% 240R 1% 240R 1% 240R 1%
SDP	R1221	ASM	ASM	ASM	DY	DY	DY
DDP	R1220 R1224	DY DY	DY DY	DY DY	ASM ASM	ASM ASM	ASM ASM





SDP & DDP SETTING

R1331*R1334:
DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)

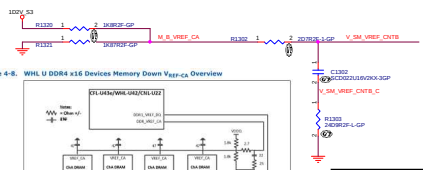
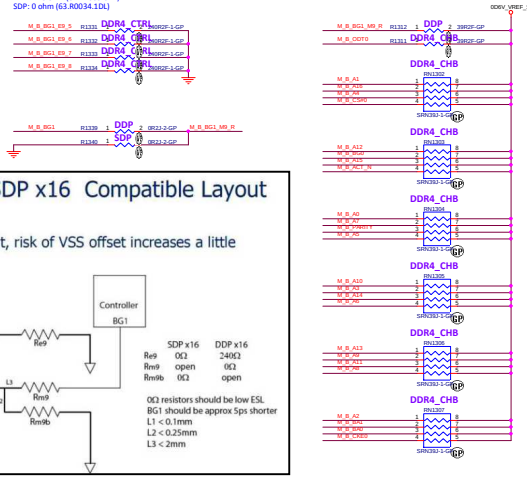
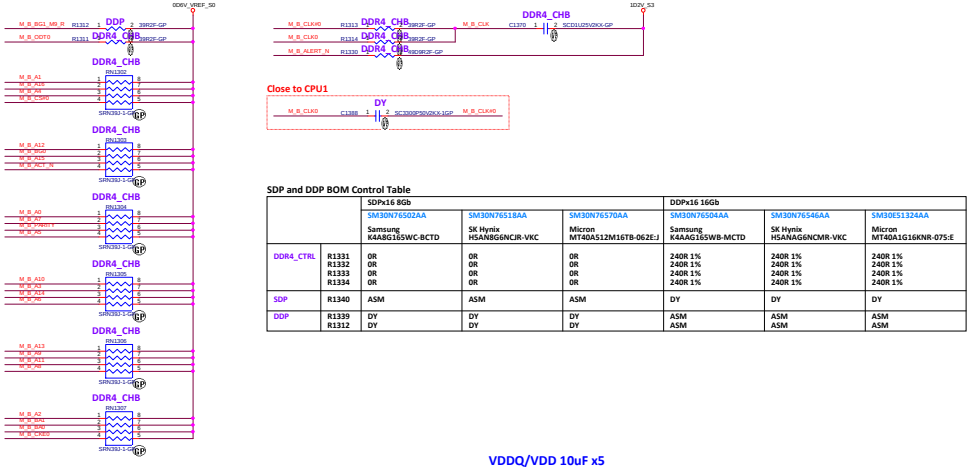


Figure 4-8. WHL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview

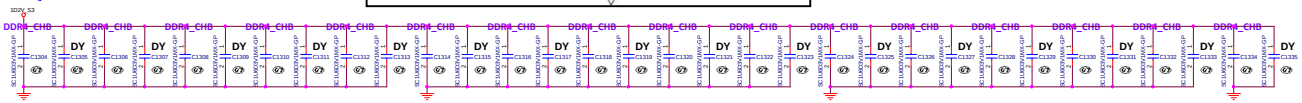




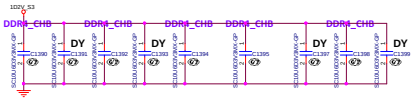
SDP and DDP BOM Control Table

		SDPx16 8Gb			DDPx16 16Gb		
		SM30N76502AA Samsung K4A8G165WC-BCTD	SM30N76518AA SK Hynix H5AN8G6NCJR-VKC	SM30N76570AA Micron MT40A512M16TB-062E:J	SM30N76504AA Samsung K4AAG165WB-MCTD	SM30N76546AA SK Hynix H5ANAG6NCMR-VKC	SM30E51324AA Micron MT40A1G16KNR-075:E
DDR4_CTRL	R1331 R1332 R1333 R1334	0R 0R 0R 0R	0R 0R 0R 0R	0R 0R 0R 0R	240R 1% 240R 1% 240R 1% 240R 1%	240R 1% 240R 1% 240R 1% 240R 1%	240R 1% 240R 1% 240R 1% 240R 1%
SDP	R1340	ASM	ASM	ASM	DY	DY	DY
DDP	R1339 R1312	DY DY	DY DY	DY DY	ASM ASM	ASM ASM	ASM ASM

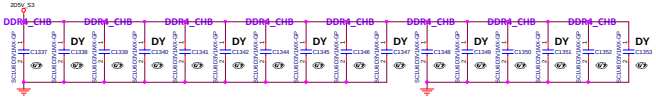
VDDQ/VDD 1uF x16



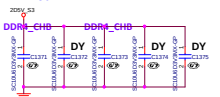
VDDQ/VDD 10uF x5



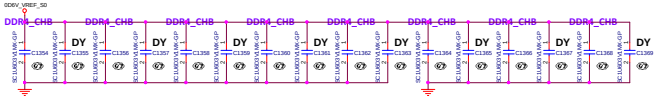
VPP 1uF x8



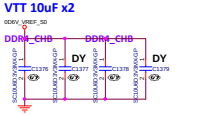
VPP 10uF x2



VTT 1uF x8



VTT 10uF x2



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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHB)

Size	Document Number	Rev
A1	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 13 of 106

LAR-2

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR (RSVD) (DDR4-CHA1)**

Size	Document Number	Rev
A4	**ARES-2**	1

Date: Thursday, August 06, 2020 Sheet 14 of 106

18,25,91,99 SPI_SI_CPU
18,25,99 SPI_WP_CPU
18,25 SPI_HOLD_CPU
24 ME_UNLOCK
21,61 CNV_RGI_DT
18 GPP_C5_ESPI_SEL
18 GPP_E6_JTAG_ODT
19 HDA_SDOUT_CPU
4,71 DK1_TCSS_RX_LSX2
3,99 DBG_PMODE
4 TBT_LSX3_VCC_CONFIG
4 TBT_LSX1_VCC_CONFIG

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic	=20K PD= 3D3V_S5 DY R1501 4K7R2J-L-GP GPP_C5_ESPI_SEL DY R1502 20K5R2F-GP = has internal 20K PD=	=NO INTERNAL= 3D3V_SUS_SPI R1503 4K7R2J-L-GP SPI_SI_CPU BOOT_HALT Close to U2501 DY R1511 4K7R2J-L-GP	=NO INTERNAL= 3D3V_SUS R1504 100KR2J-1-GP GPP_E6_JTAG_ODT DY R1512 4K7R2J-L-GP	=20K PD=	=NO INTERNAL= 3D3V_SUS_SPI R1506 4K7R2J-L-GP SPI_WP_CPU Close to U2501 DY R1514 4K7R2J-L-GP CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	=20K PD= * PH as VCCPGPPR 1D8V_GPPR_SUS DY R1509 4K7R2J-L-GP ME_UNLOCK R1515 DY 2HDA_SDOUT_CPU	=NO INTERNAL= 1D8V_SUS R1507 100KR2J-1-GP CNV_RGI_DT DY R1516 4K7R2J-L-GP
High	ESPI SIDSBLE	Disable Isable	Enal Nble	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Disable Isable	OVERRIDEN VERRIDEN	INTEGRATED CNVI DISABLE NTEGRATED CNVI DISABLE
Low	Enal =default= Nble	Enal Nble	Disable Isable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enal Nble	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE NTEGRATED CNVI ENABLE

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		
Schematic		E21 =20K PD= 3D3V_S5 DY R1519 4K7R2J-L-GP TBT_LSX1_VCC_CONFIG R1522 20KR2J-L3-GP	D10 =20K PD= 3D3V_S5 DY R1520 4K7R2J-L-GP DK1_TCSS_RX_LSX2 R1523 20KR2J-L3-GP	D12 =20K PD= 3D3V_S5 DY R1524 4K7R2J-L-GP TBT_LSX3_VCC_CONFIG R1525 20KR2J-L3-GP	=NO INTERNAL= 3D3V_SUS R1526 4K7R2J-L-GP SPI_HOLD_CPU Close to U2501 DY R1527 100KR2J-1-GP	=20K PU= 1D05V_S5_OUT XDP R1528 1KR2J-1-GP DBG_PMODE DY R1529 1KR2J-1-GP	
High	3.3V	3.3V	3.3V	3.3V	Disable Isable	DXTESTMODE ENABLED FATESTMODE ENABLED	
Low	1.8V	1.8V	1.8V	1.8V	Enal Nble	DEXTESTMODE ENABLED FATESTMODE ENABLED	

Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0	
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	

TBT LSX #1	TBT LSX #2	TBT LSX #3	A0	GPP_E10	GPP_E11	GPP_H0	GPP_H1	GPP_H2
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	RA RB	RA RB	BOOT STRAP 1- BIT 2 WEAK INTERNAL PD 20K SAMPLING - RSMRSTB	BOOT STRAP 2- BIT 3 WEAK INTERNAL PD 20K SAMPLING - RSMRSTB	BOOT STRAP 3- BIT 4 WEAK INTERNAL PD 20K SAMPLING - RSMRSTB

LAR-2

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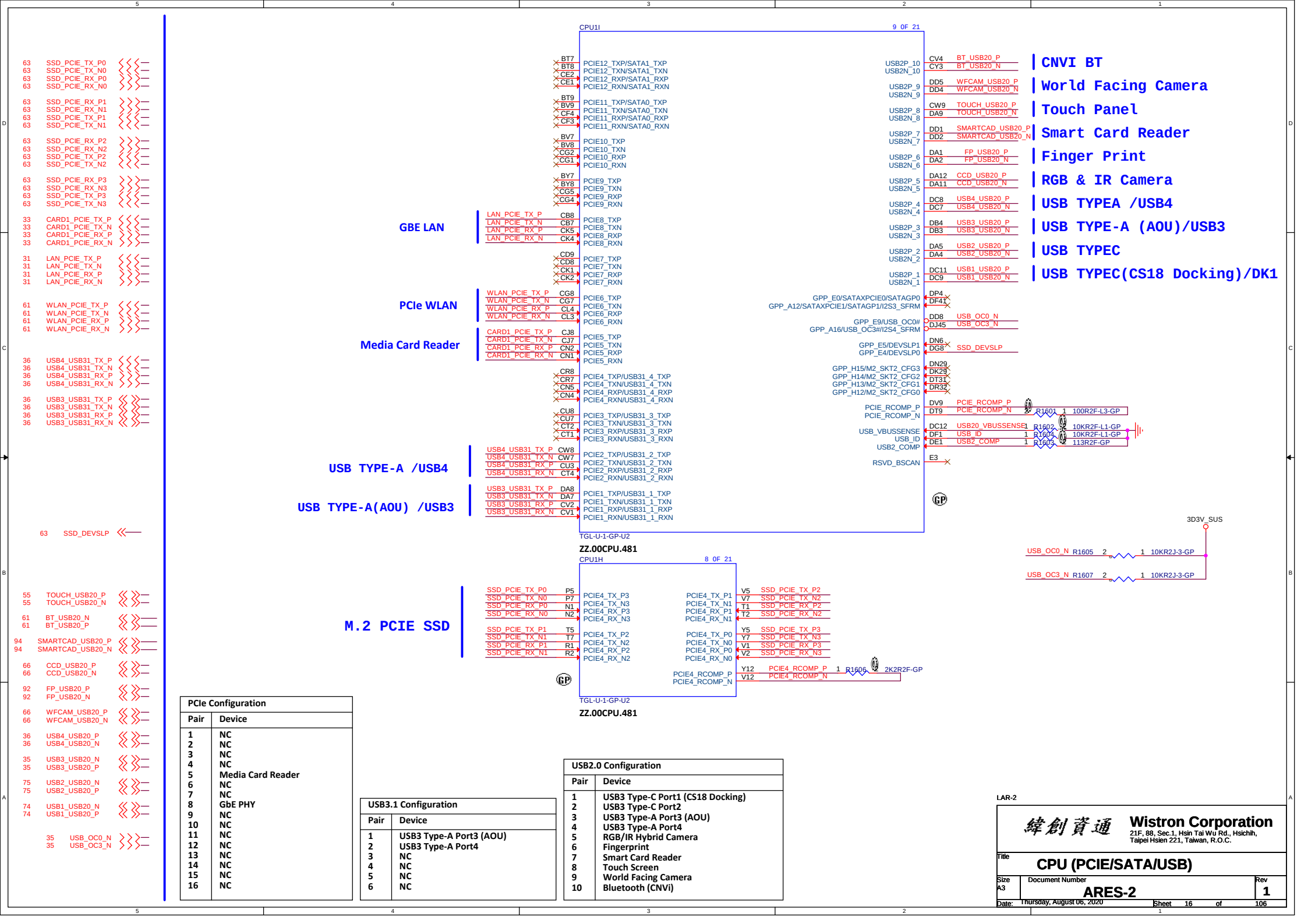
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size	Document Number	Rev
A2	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 15 of 106



PCIe Configuration	
Pair	Device
1	NC
2	NC
3	NC
4	NC
5	Media Card Reader
6	NC
7	NC
8	GbE PHY
9	NC
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
16	NC

USB3.1 Configuration	
Pair	Device
1	USB3 Type-A Port3 (AOU)
2	USB3 Type-A Port4
3	NC
4	NC
5	NC
6	NC

USB2.0 Configuration	
Pair	Device
1	USB3 Type-C Port1 (CS18 Docking)
2	USB3 Type-C Port2
3	USB3 Type-A Port3 (AOU)
4	USB3 Type-A Port4
5	RGB/IR Hybrid Camera
6	Fingerprint
7	Smart Card Reader
8	Touch Screen
9	World Facing Camera
10	Bluetooth (CNVi)

LAR-2

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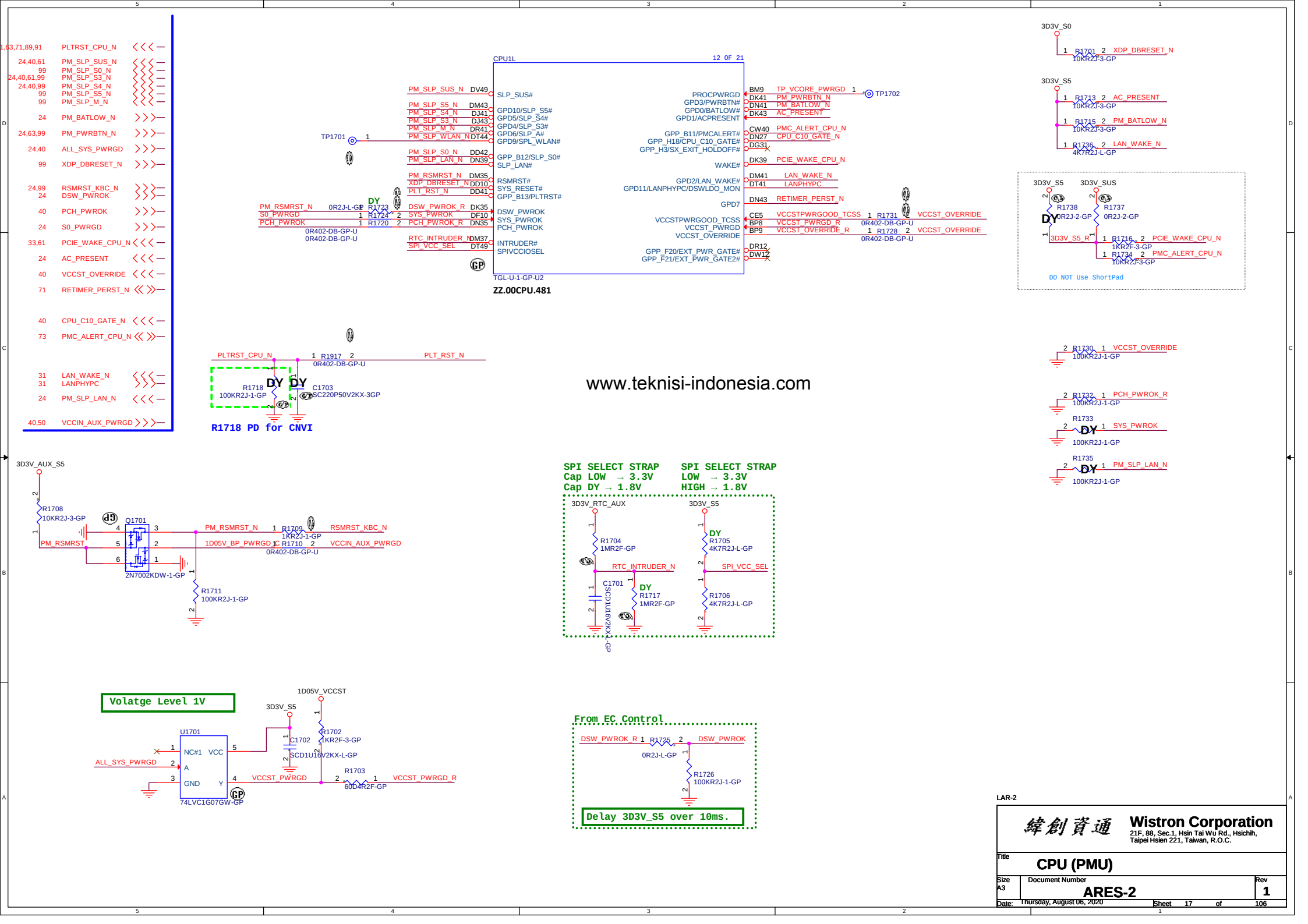
Title: **CPU (PCIE/SATA/USB)**

Size	Document Number	Rev
A3	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 16 of 106


1,63,71,89,91 PLTRST_CPU_N
24,40,61 PM_SLP_SUS_N
99 PM_SLP_S0_N
24,40,61,99 PM_SLP_S3_N
24,40,99 PM_SLP_S4_N
99 PM_SLP_S5_N
99 PM_SLP_M_N
24 PM_BATLOW_N
24,63,99 PM_PWRBTN_N
24,40 ALL_SYS_PWRGD
99 XDP_DBRESET_N
24,99 RSMRST_KBC_N
24 DSW_PWROK
40 PCH_PWROK
24 S0_PWRGD
33,61 PCIE_WAKE_CPU_N
24 AC_PRESENT
40 VCCST_OVERRIDE
71 RETIMER_PERST_N
40 CPU_C10_GATE_N
73 PMC_ALERT_CPU_N
31 LAN_WAKE_N
31 LANPHYPC
24 PM_SLP_LAN_N
40,50 VCCIN_AUX_PWRGD
CPU1L
12 OF 21
SLP_SUS#
GPD10/SLP_S5#
GPD5/SLP_S4#
GPD4/SLP_S3#
GPD6/SLP_A#
GPD9/SPL_WLAN#
GPP_B12/SLP_S0#
SLP_LAN#
RSMRST#
SYS_RESET#
GPP_B13/PLTRST#
DSW_PWROK
SYS_PWROK
PCH_PWROK
INTRUDER#
SPIVCCIOSEL
PROCPWRGD
GPD3/PWRBTN#
GPD0/BATLOW#
GPD1/ACPRESENT
GPP_B11/PMCALERT#
GPP_H18/CPU_C10_GATE#
GPP_H3/SX_EXIT_HOLDOFF#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC/DSWLDO_MON
GPD7
VCCSTPWRGOOD_TCSS
VCCST_PWRGD
VCCST_OVERRIDE
GPP_F20/EXT_PWR_GATE#
GPP_F21/EXT_PWR_GATE2#
TGL-U-1-GP-U2
ZZ.00CPU.481
TP1701
TP1702
TP_VCORE_PWRGD
PM_PWRBTN_N
PM_BATLOW_N
AC_PRESENT
PMC_ALERT_CPU_N
CPU_C10_GATE_N
PCIE_WAKE_CPU_N
LAN_WAKE_N
LANPHYPC
RETIMER_PERST_N
VCCST_OVERRIDE
3D3V_S0
3D3V_S5
3D3V_SUS
XDP_DBRESET_N
AC_PRESENT
PM_BATLOW_N
LAN_WAKE_N
PCIE_WAKE_CPU_N
PMC_ALERT_CPU_N
DO NOT Use ShortPad
PLTRST_CPU_N
PLT_RST_N
R1718 PD for CNVI
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PCH_PWROK_R
SYS_PWROK
PM_SLP_LAN_N
3D3V_AUX_S5
Q1701
2N7002KDW-1-GP
PM_RSMRST
PM_RSMRST_N
RSMRST_KBC_N
1D05V_BP_PWRGD
VCCIN_AUX_PWRGD
SPI SELECT STRAP
Cap LOW → 3.3V
Cap DY → 1.8V
SPI SELECT STRAP
LOW → 3.3V
HIGH → 1.8V
3D3V_RTC_AUX
3D3V_S5
RTC_INTRUDER_N
SPI_VCC_SEL
Volatge Level 1V
1D05V_VCCST
U1701
74LVC1G07GW-GP
ALL_SYS_PWRGD
VCCST_PWRGD
VCCST_PWRGD_R
From EC Control
DSW_PWROK_R
DSW_PWROK
Delay 3D3V_S5 over 10ms.
LAR-2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (PMU)
Size A3
Document Number
ARES-2
Rev 1
Date: Thursday, August 06, 2020
Sheet 17 of 106

SPI ROM

15,25,99 SPI_WP_CPU
15,25 SPI_HOLD_CPU
25,91 SPI_CLK_CPU
25,91 SPI_SO_CPU
15,25,91,99 SPI_SI_CPU
25 SPI_CS_CPU_N0
91 SPI_CS_CPU_N2

WLAN

61 CPU_CLINK_CLK_WLAN
61 CPU_CLINK_DAT_WLAN
61 CPU_CL_RST#_WLAN

Media CardReader

33 CARD1_CLK_CPU_P
33 CARD1_CLK_CPU_N
33 CARD1_CLKREQ_CPU_N

M.2 Pcie SSD

63 SSD_CLK_CPU_N
63 SSD_CLK_CPU_P
63 SSD_CLKREQ_CPU_N

Gbe LAN

31 LAN_CLK_CPU_P
31 LAN_CLK_CPU_N
31 LAN_CLKREQ_CPU_N

PCIe WLAN

61 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N
61 WLAN_CLKREQ_CPU_N

ESPI

24 ESPI_CPU_IO0
24 ESPI_CPU_IO1
24 ESPI_CPU_IO2
24 ESPI_CPU_IO3
24 ESPI_CPU_CS_N
24 ESPI_CPU_RST_N
24 ESPI_CPU_CLK

OTHER

15 GPP_C5_ESPI_SEL
61 SUS_CLK_CPU
25 SRTC_RST_N
25,99 RTC_RST_N
24,25 RTCRST_ON
15 GPP_E6_JTAG_ODT
65 CPU_SMB_SCL_TP
65 CPU_SMB_SDA_TP
31,71 CPU_SMB_SCL_P0
31,71 CPU_SMB_SDA_P0
71,73 CPU_SMB_SCL_P1
71,73 CPU_SMB_SDA_P1

SD_MMC_ID — R1829 SDID_RT 1KR2J-L2-GP — 3D3V_SUS
R1830 SDID_GL 1MR2J-L3-GP

SW Control :		HW Control : *	
GPP_E2		R1829	R1830
SD_MMC_ID	High = REALTEK [RTS5232S]	ASM	DY
	Low = GENESYS [GL9750]	DY	ASM

CPU1E — 5 OF 21 — TGL-U-1-GP-U2 — ZZ.00CPU.481

SPI_CLK_CPU DJ37 SPI0_CLK
SPI_HOLD_CPU DG35 SPI0_IO3
SPI_WP_CPU DJ39 SPI0_IO2
SPI_SO_CPU DJ33 SPI0_MISO
SPI_SI_CPU DJ35 SPI0_MOSI
SPI_CS_CPU_N0 DF35 SPI0_CS1#
SPI_CS_CPU_N2 DG37 SPI0_CS0#
DF39 SPI0_CS2#

SD_MMC_ID DJ6 GPP_E11/SPI1_CLK/THC0_SPI1_CLK
DN5 GPP_E2/SPI1_IO3/THC0_SPI1_IO3
DR9 GPP_E1/SPI1_IO2/THC0_SPI1_IO2
DM6 GPP_E12/SPI1_MISO_IO1/THC0_SPI1_IO1
DK6 GPP_E13/SPI1_MOSI_IO0/THC0_SPI1_IO0
DK8 GPP_E10/SPI1_CS#/THC0_SPI1_CS#
DV11 GPP_E8/SPI1_CS1#/SATA_LED#
DW9 GPP_E17/THC0_SPI1_INT#
GPP_E6_JTAG_ODT DT8 GPP_E6/THC0_SPI1_RST#

SDRAM_ID1 DN15 DK13 GPP_F11/THC1_SPI2_CLK
SDRAM_ID0 DM13 GPP_F15/GSXSRESET#/THC1_SPI2_IO3
GPP_F14/GSXDIN/THC1_SPI2_IO2
DN13 GPP_F13/GSXSLOAD/THC1_SPI2_IO1
SDRAM_ID2 DJ15 DK15 GPP_F12/GSXDOUT/THC1_SPI2_IO0
SDRAM_ID4 DN16 GPP_F16/GSXCLK/THC1_SPI2_CS#
SDRAM_ID3 DV14 GPP_F18/THC1_SPI2_INT#
GPP_F17/THC1_SPI2_RST#

CPU_CLINK_CLK_WLAN DH3 CL_CLK
CPU_CLINK_DAT_WLAN DH4 CL_DATA
CPU_CL_RST#_WLAN DF2 CL_RST#

GPP_C0/SMBCLK DK21 CPU_SMB_SCL_TP
GPP_C1/SMBDATA DM19 CPU_SMB_SDA_TP
GPP_C2/SMBALERT# DN19 CPU_SMB_ALERT_N
GPP_C3/SML0CLK DK19 CPU_SMB_SCL_P0
GPP_C4/SML0DATA DM17 CPU_SMB_SDA_P0
GPP_C5/SML0ALERT# DN17 GPP_C5_ESPI_SEL
GPP_C6/SML1CLK DK17 CPU_SMB_SCL_P1
GPP_C7/SML1DATA DJ17 CPU_SMB_SDA_P1
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1# CY50 GPP_B23_CLK_FREQ

To LAN
To PD/TBT — TP1801

GPP_A5/ESPI_CLK DN53 ESPI_CPU_CLK_R
GPP_A3/ESPI_IO3/SUSACK# DJ53 ESPI_CPU_IO3_R
GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK DH50 ESPI_CPU_IO2_R
GPP_A1/ESPI_IO1 DP50 ESPI_CPU_IO1_R
GPP_A0/ESPI_IO0 DP52 ESPI_CPU_IO0_R
GPP_A4/ESPI_CS# DK52 ESPI_CPU_CS_R_N
GPP_A6/ESPI_RESET# DL50 ESPI_CPU_RST_R_N

2 R1814 1 75KR2J-GP

ESPI_CPU_CLK_R 1 R1804 2 ESPI_CPU_CLK 49D9KR2F-GP
ESPI_CPU_IO0_R 1 R1805 2 ESPI_CPU_IO0 10KR2J-GP
ESPI_CPU_IO1_R 1 R1806 2 ESPI_CPU_IO1 10KR2J-GP
ESPI_CPU_IO2_R 1 R1807 2 ESPI_CPU_IO2 10KR2J-GP
ESPI_CPU_IO3_R 1 R1808 2 ESPI_CPU_IO3 10KR2J-GP
ESPI_CPU_CS_R_N 1 R1809 2 ESPI_CPU_CS_N 0KR2J-L-GP
ESPI_CPU_RST_R_N 1 R1810 2 ESPI_CPU_RST_N 0KR2J-L-GP

3D3V_SUS
RN1801 1 2 4 3 CPU_SMB_SCL_P0 CPU_SMB_SDA_P0 SRN1KJ-7-GP
RN1807 1 2 4 3 CPU_SMB_SCL_P1 CPU_SMB_SDA_P1 SRN1KJ-7-GP
R1901 1 2 CPU_SMB_ALERT_N 4K7R2J-L-GP
1D8V_SUS
DY R1909 1 2 4K7R2J-L-GP

CPU1K — 11 OF 21 — TGL-U-1-GP-U2 — ZZ.00CPU.481

BW1 BW2 CLKOUT_PCIE_P6 CLKOUT_PCIE_N6
CB2 CB1 CLKOUT_PCIE_P5 CLKOUT_PCIE_N5
BW4 BW5 CLKOUT_PCIE_P4 CLKOUT_PCIE_N4
CL7 CL8 CLKOUT_PCIE_P3 CLKOUT_PCIE_N3
CB4 CB5 CLKOUT_PCIE_P2 CLKOUT_PCIE_N2
BY4 BY3 CLKOUT_PCIE_P1 CLKOUT_PCIE_N1
CN7 CN8 CLKOUT_PCIE_P0 CLKOUT_PCIE_N0
DJ5 XCLK_BIASREF

PCIe WLAN — WLAN_CLK_CPU_P / WLAN_CLK_CPU_N
Media CardReader — CARD1_CLK_CPU_P / CARD1_CLK_CPU_N
LAN — LAN_CLK_CPU_P / LAN_CLK_CPU_N
M.2 Pcie SSD — SSD_CLK_CPU_P / SSD_CLK_CPU_N

2 R1819 1 XCLK_BIASREF 60D4R2F-GP

GPP_F19/SRCCLKREQ6# DU14
GPP_H11/SRCCLKREQ5# DF23 WLAN_CLKREQ_CPU_N
GPP_H10/SRCCLKREQ4# DG25 CARD1_CLKREQ_CPU_N
GPP_D8/SRCCLKREQ3# DT24 LAN_CLKREQ_CPU_N
GPP_D7/SRCCLKREQ2# DT30 DV30
GPP_D6/SRCCLKREQ1# DW30 SSD_CLKREQ_CPU_N
GPP_D5/SRCCLKREQ0# DM1 XTL_38D4M_X2_CPU
XTAL_OUT DL1 XTL_38D4M_X1_CPU
XTAL_IN
GPD8/SUSCLK DW41 SUS_CLK_CPU
RTCX2 DT47 XTL_32K_X2_CPU
RTCX1 DR47 XTL_32K_X1_CPU
RTCRST# DN37 RTC_RST_N
SRTCRST# DK37 SRTC_RST_N

3D3V_S0
RN1803 1 2 4 3 CPU_SMB_SCL_TP CPU_SMB_SDA_TP SRN1KJ-7-GP
3D3V_S0
RN1805 1 2 3 4 8 7 6 5 WLAN_CLKREQ_CPU_N SSD_CLKREQ_CPU_N CARD1_CLKREQ_CPU_N LAN_CLKREQ_CPU_N SRN10KJ-12-GP

Ares-2: GPP_H[0:23] is 1.8V.

1D8V_SUS
MEM_ID0_1 R1823 10KR2J-3-GP
MEM_ID1_1 R1825 10KR2J-3-GP
MEM_ID2_1 R1812 10KR2J-3-GP
MEM_ID3_1 R1802 10KR2J-3-GP
MEM_ID4_1 R1818 10KR2J-3-GP
SDRAM_ID0
SDRAM_ID1
SDRAM_ID2
SDRAM_ID3
SDRAM_ID4
MEM_ID0_0 R1824 10KR2J-3-GP
MEM_ID1_0 R1826 10KR2J-3-GP
MEM_ID2_0 R1813 10KR2J-3-GP
MEM_ID3_0 R1803 10KR2J-3-GP
MEM_ID4_0 R1822 10KR2J-3-GP

3D3V_RTC_AUX
R1816 20KR2J-L3-GP SRTC_RST_N C1803 SC1U10V2KX-L1-GP
3D3V_RTC_AUX
R1817 20KR2J-L3-GP RTC_RST_N C1804 SC1U10V2KX-L1-GP

SRTC_RST_N
RTCRST_ON
Q1801 2N7002KDW-1-GP
R1821 100KR2J-1-GP
RTCRST_ON
RTC_RST_N

Memory Configuration	Memory Supplier	Die Revision
00: 8Gb 01: 16Gb (Big Size) 10: 16Gb 11: 32Gb (Big Size)	00: Samsung 01: Micron 10: SK Hynix 11: (Reserve)	

GPP_F18	GPP_F17	GPP_F16	GPP_F15	GPP_F14				
SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1	SDRAM_ID0	Memory ID	Supplier	Capacity	Vendor PN
0	0	0	0	0	0	SAMSUNG	8Gb x 2	K4A8G165WC-BCWE
0	1	0	0	0	8	SAMSUNG	16Gb (Big Size)	2
1	0	0	0	0	16	SAMSUNG	16Gb x 2	K4AAG165WA-BCWE
1	1	0	0	0	24	SAMSUNG	32Gb (Big Size)	4
0	0	0	1	0	2	MICRON	8Gb x 2	MT40A512M16TB-062E:J Z21C
0	1	0	1	0	10			
1	0	0	1	0	18	MICRON	16Gb X 2	MT40A1G16KD-062E:E
1	1	0	1	0	26			
0	0	1	0	0	4	SK HYNIX	8Gb x 2	H5AN8G6NDJR-XNC
0	1	1	0	0	12			
1	0	1	0	0	20	SK HYNIX	16Gb	H5ANAG6NCMR-XNC
1	1	1	0	0	28			
0	0	0	0	1	1	SAMSUNG	8Gb x 1	K4A8G165WC-BCWE
0	0	0	1	1	3	MICRON	8Gb x 1	MT40A512M16TB-062E:J Z21C
0	0	1	0	1	5	SK HYNIX	8Gb x 1	H5AN8G6NDJR-XNC
0	0	1	1	1	7			
0	0	1	1	0	6			
0	1	1	1	0	14			
1	0	1	1	0	22			
1	1	1	1	0	30			

0=L, 1=H

XTL_32K_X_CPU — R1814 10MR2J-GP — X1801 XTAL-32.768KHZ-88-GP — 082.30003.0191
C1802 SC15P50V2JN-L-GP
C1801 SC15P50V2JN-L-GP

XTL_38D4M_X1_CPU — C1805 SC15P50V2JN-L-GP
X1802 XTAL-38D4MHZ-21-GP — 082.30040.0101
R1820 200KR2F-L-GP
XTL_38D4M_X2_CPU — C1806 SC15P50V2JN-L-GP

	C1802(Cg)	C1801(Cd)
EPSON 082.30003.0191	15pF	15pF
SEIKO 082.30003.0301	15pF	15pF
NDK 082.30003.0221	15pF	15pF
TXC	15pF	15pF

LAR-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/LPC/SMBS/XTAL/CLK)
Size: A2 | Document Number: ARES-2 | Rev: 1
Date: Thursday, August 06, 2020 | Sheet 18 of 106

27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC
27 HDA_SDIN0_CPU
15 HDA_SDOUT_CPU

61 CNV_CLKREQ
61 CNV_RF_RST_N

55 TOUCH_RESET_N

71,73 RT_FORCE_PWR

91 PIRQA_N

66 YOGA_DET_N
25 RTC_TEST

RT_FORCE_PWR 1 R1902 2 RETIMER_FORCE_PWR
0R402-DB-GP-U

3D3V_S0
R1906
100KR2F-L1-GP

7 OF 21
CPU1G

20190823_Byron
HDA_BITCLK_CODEC 1 R1904 2 HDA
HDA_SYNC_CODEC 1 R1901 2 HDA
HDA_SDOUT_CODEC 1 R1905 2 HDA
10R2J-2-GP-U

TP1901 1HDA_RST_N_CODEC

2 R1903 1
200R2F-L1-GP

HDA_BITCLK_CPU DR38
HDA_SYNC_CPU DU37
HDA_SDOUT_CPU DT37
HDA_SDIN0_CPU DV37
HDA_RST_N_CODEC DV41
PIRQA_N DL53
CNV_RF_RST_N DG51
DG50
CNV_CLKREQ DL49
RTC_TEST DL52
YOGA_DET_N DH49
SNDW_RCOMP DF33

GPP_R0/HDA_BCLK/I2S0_SCLK
GPP_R1/HDA_SYNC/I2S0_SFRM
GPP_R2/HDA_SDO/I2S0_TXD
GPP_R3/HDA_SDI0/I2S0_RXD
GPP_R4/HDA_RST#
GPP_A7/I2S2_SCLK/DMIC_CLK_A0
GPP_A8/I2S2_SFRM/CNV_RF_RESET#/DMIC_DATA_0
GPP_A10/I2S2_RXD/DMIC_DATA1
GPP_A9/I2S2_TXD/MODEM_CLKREQ/CRF_XTAL_CLKREQ/DMIC_CLK_A1
GPP_A11/PMC_I2C_SDA/I2S3_SCLK
GPP_A13/PMC_I2C_SCL/I2S3_TXD/DMIC_CLK_B0
SNDW_RCOMP

GPP_F8_I2S_MCLK2_INOUT DW15
GPP_D19/I2S_MCLK1 DW24
GPP_A23/I2S1_SCLK DG41
GPP_R7/I2S1_SFRM DT38
GPP_R6/I2S1_TXD DV38
GPP_R5/HDA_SDI1/I2S1_RXD DW38
GPP_S6/SNDW3_CLK/DMIC_CLK_A0 DN31
GPP_S7/SNDW3_DATA/DMIC_DATA0 DM31
GPP_S4/SNDW2_CLK/DMIC_CLK_A1 DK33
GPP_S5/SNDW2_DATA/DMIC_DATA1 DK31
GPP_S2/SNDW1_CLK/DMIC_CLK_B0 DW35
GPP_S3/SNDW1_DATA/DMIC_CLK_B1 DV35
GPP_S0/SNDW0_CLK DT32
GPP_S1/SNDW0_DATA DR35

TOUCH_RESET_N
RETIMER_FORCE_PWR

TGL-U-1-GP-U2
ZZ.00CPU.481

LAR-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HDA/I2S/SD/DMIC)

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 19 of 106

ISH
66,68,70 CPU_I2C_SDA_ISH0
66,68,70 CPU_I2C_SCL_ISH0

EC
24,68 CPU_I2C_SDA_ISH1_EC
24,68 CPU_I2C_SCL_ISH1_EC

68 CPU_UART2_TXD
68 CPU_UART2_RXD

94 SMARTCAD_DTCT_N
25 RTC_DET_N

55 TOUCH_EN
55 TOUCH_STOP_N

24 MODERN_STANDBY

24,67 LID_CLOSE_N
24,67 SENSOR_LID_OPEN_N

68 LID_CLOSE#_D

26 FAN_ID

65 KBD_BL_DTCT_N

66,68,70 ISH_ANGLE_INT_N
68 ISH_ALS_INT_N
68 ISH_GSENSOR_INT_N

68 SENSOR_LID_OPEN_D_N

27 HDA_SPKR

24 TOP_SWAP_EN

66 IR_CAM_DET_N

65 PAD_DISABLE

PCH strap pin: SPKR

	TOP SWAP OVERRIDE
HDA_SPKR	* High = TOP SWAP ENABLED Low = DISABLED (WEAK INTERNAL PD)

The internal pull-up

CPU1F

MODERN_STANDBY DC53 GPP_B16/GSPI0_CLK
DA51 GPP_B18/GSPI0_MOSI
TOUCH_EN DC49 GPP_B17/GSPI0_MISO
HDA_SPKR DC50 GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1# **Strap**
DC52 GPP_B15/GSPI0_CS0#
TOP_SWAP_EN R2002 1 2 0R2J-2-GP
CY49 GPP_B20/GSPI1_CLK
CY53 GPP_B22/GSPI1_MOSI
FAN_ID CY52 GPP_B21/GSPI1_MISO
RTC_DET_N DA50 GPP_B19/GSPI1_CS0#
TOUCH_STOP_N DV21 GPP_C9/UART0_TXD
DT21 GPP_C8/UART0_RXD
66 DMIC_DET_N DR21 GPP_C11/UART0_CTS#
IR_CAM_DET_N DW21 GPP_C10/UART0_RTS#
DV19 GPP_C13/UART1_TXD/ISH_UART1_TXD
DT19 GPP_C12/UART1_RXD/ISH_UART1_RXD
DR18 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
SMARTCAD_DTCT_N DU19 GPP_C14/UART1_RTS#/ISH_UART1_RTS#

3D3V_S0 DEBUG RN2006 SRN47K-2-GP-U
CPU_UART2_TXD DJ21 GPP_C21/UART2_TXD
CPU_UART2_RXD DG23 GPP_C20/UART2_RXD
CPU_UART2_CTS_N DJ19 GPP_C23/UART2_CTS#
CPU_UART2_RTS_N DF21 GPP_C22/UART2_RTS#
DV18 GPP_C17/I2C0_SCL
DW18 GPP_C16/I2C0_SDA
DJ23 GPP_C19/I2C1_SCL
DT18 GPP_C18/I2C1_SDA
DJ29 GPP_H5/I2C2_SCL
DJ31 GPP_H4/I2C2_SDA
DF29 GPP_H7/I2C3_SCL
DG29 GPP_H6/I2C3_SDA
DF25 GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
PAD_DISABLE DF27 GPP_H8/I2C4_SDA/CNV_MFUART2_RXD
R2003 10KR1J-GP
TGL-U-1-GP-U2
ZZ.00CPU.481

6 OF 21
DR27 GPP_D14/ISH_UART0_TXD
DW27 GPP_D13/ISH_UART0_RXD
DV25 GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5 DT25 KBD_BL_DTCT_N
DB45 CPU_I2C_SCL_ISH0 GPP_B6/ISH_I2C0_SCL
DB44 CPU_I2C_SDA_ISH0 GPP_B5/ISH_I2C0_SDA
CY39 CPU_I2C_SCL_ISH1 GPP_B8/ISH_I2C1_SCL
DB47 CPU_I2C_SDA_ISH1 GPP_B7/ISH_I2C1_SDA
DD47 GPP_B10/I2C5_SCL/ISH_I2C2_SCL
DD44 GPP_B9/I2C5_SDA/ISH_I2C2_SDA
DJ8 GPP_E16/ISH_GP7
DR7 GPP_E15/ISH_GP6
DR24 GPP_D18/ISH_GP5
DU25 SENSOR_LID_OPEN_D_N
DV31 LID_CLOSE#_D GPP_D17/ISH_GP4
DU31 ISH_ANGLE_INT_N GPP_D3/ISH_GP3/BK3/SBK3
DT27 ISH_GSENSOR_INT_N GPP_D2/ISH_GP2/BK2/SBK2
DV27 ALS_INT_R_N GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0
GPP_RCOMP DR51 GPP_RCOMP R2021 200R2F-L1-GP
DN33 GPP_T3/I2C7_SCL
DT35 GPP_T2/I2C7_SDA
DG17 GPP_U5/GSPI3_CLK
DG19 GPP_U4/GSPI3_CS0#

3D3V_S0
RN2004 SRN1KJ-7-GP
CPU_I2C_SCL_ISH0
CPU_I2C_SDA_ISH0
RN2003 SRN1KJ-7-GP
CPU_I2C_SCL_ISH1
CPU_I2C_SDA_ISH1

D2007 LRB520S-30T1G-GP SENSOR_LID_OPEN_N
D2001 LRB520S-30T1G-GP LID_CLOSE_N
R2051 20R0201-DB-GP ISH_ALS_INT_N

CPU_I2C_SCL_ISH0
CPU_I2C_SDA_ISH0
CPU_I2C_SCL_ISH1
CPU_I2C_SDA_ISH1
C2001 C2002 C2003 C2004 SC150P50V2KX-GP

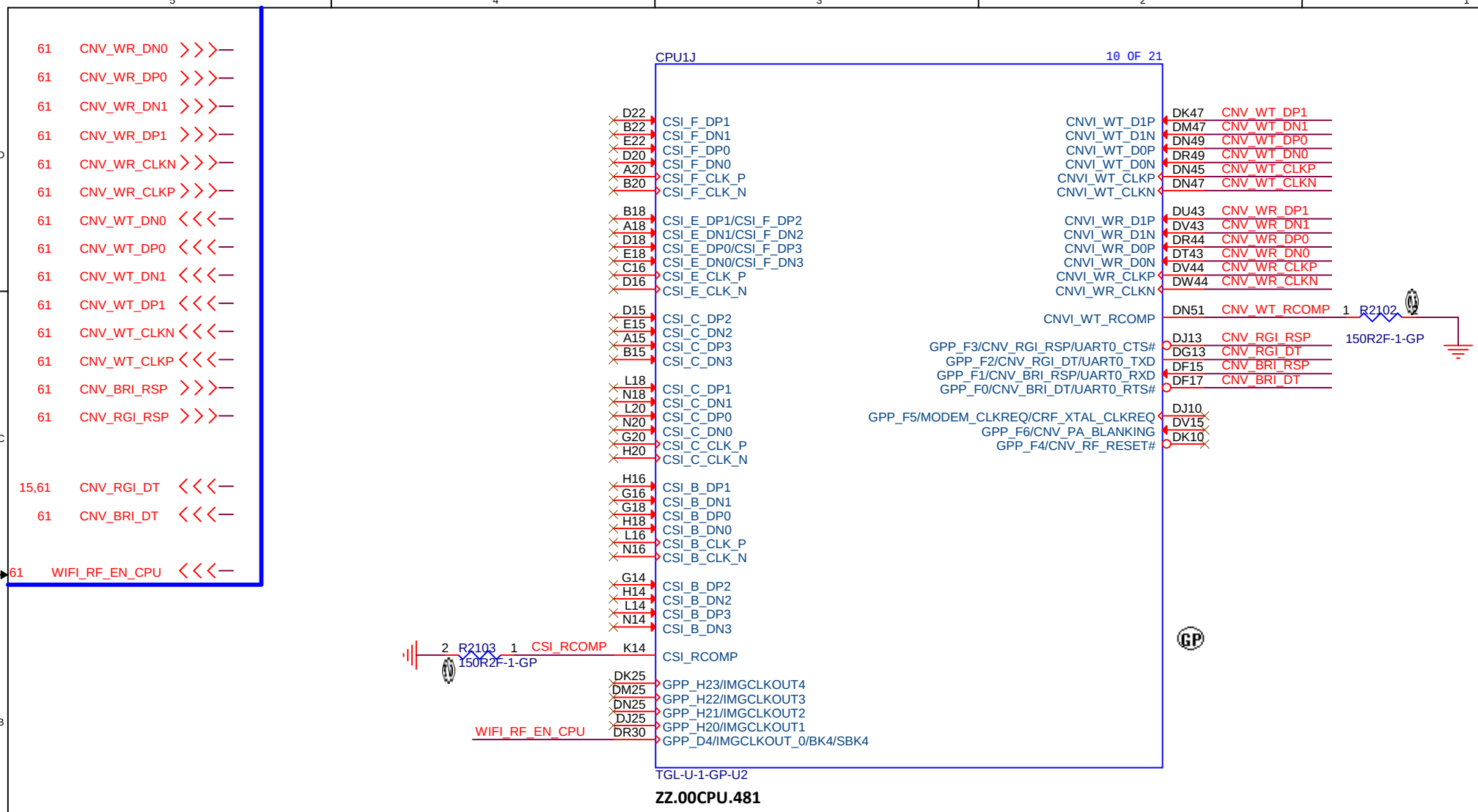
3D3V_S0 3D3V_S0
Q2001 2N7002KDW-1
CPU_I2C_SDA_ISH1 CPU_I2C_SDA_ISH1_EC
CPU_I2C_SCL_ISH1_EC CPU_I2C_SCL_ISH1
C2006 C2005 SC150P50V2KX-GP

3D3V_S0
R2016 10KR2J-L-GP SENSOR_LID_OPEN_D_N
R2015 10KR2F-2-GP LID_CLOSE#_D
R2001 10KR2F-2-GP ISH_ANGLE_INT_N

LAR-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)
Size: A3 | Document Number: ARES-2 | Rev: 1
Date: Thursday, August 06, 2020 | Sheet 20 of 106



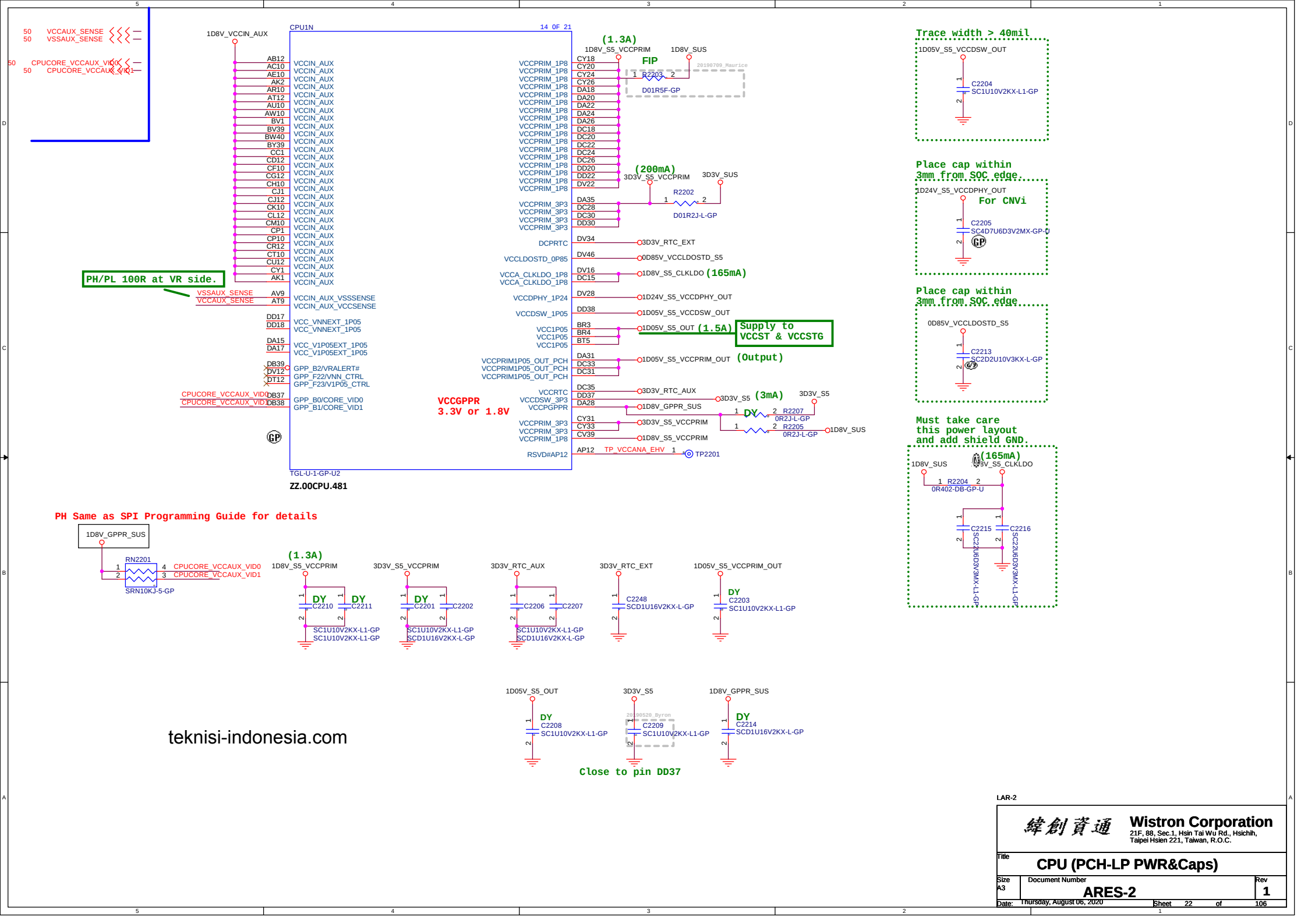
LAR-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (CSI/EMMC/CNVi)**

Size	Document Number	Rev
A4	ARES-2	1

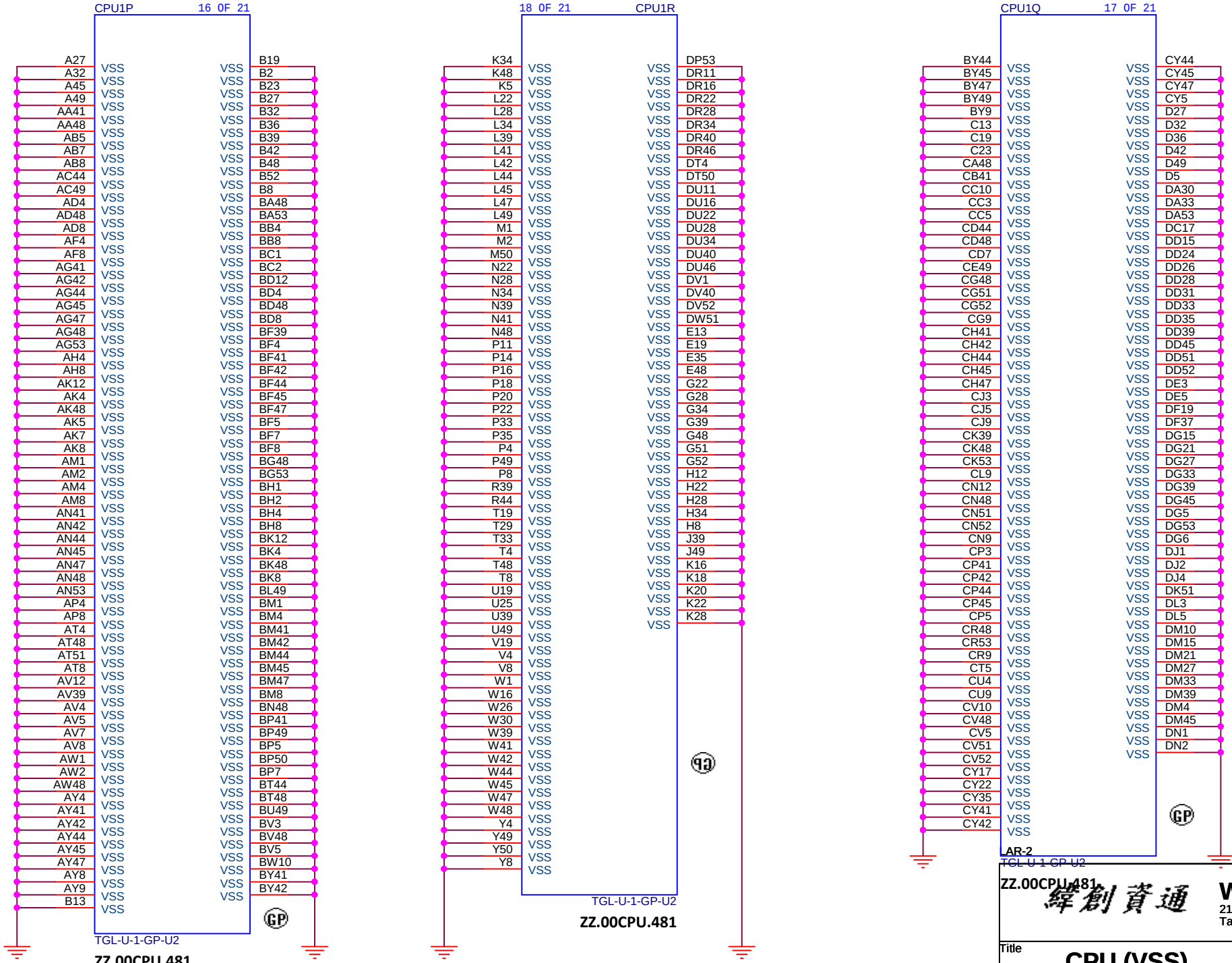
Date: Thursday, August 06, 2020 Sheet 21 of 106



LAR-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (PCH-LP PWR&Caps)	
Size A3	Document Number ARES-2	Rev 1
Date: Thursday, August 06, 2020	Sheet 22 of 106	



緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VSS)**

Size	Document Number	Rev
A4	**ARES-2**	1

Date: Thursday, August 06, 2020 Sheet 23 of 106

Touch Panel

- 4 eDP_BLEN_CPU
- 55 BLON_OUT
- 20,24,67 SENSOR_LID_OPEN_N
- 20,67 LID_CLOSE_N

Others

- 64 CHARGE_LED
- 24,73 3D3V_PD_EN
- 64,74,89 KBC_PWRBTN_N

PD Control

- 73 EC_I2C_SCL_PD
- 73 EC_I2C_SDA_PD
- 68 ES1_TXD_EC
- 35 USB_AO_SEL
- 35 USB_AO_SEL2
- 35 AOU_IFLG_N

BAT&Charger

- 44 AD_IA
- 44 AC_IN_N
- 20,68 CPU_I2C_SCL_ISHI_EC
- 20,68 CPU_I2C_SDA_ISHI_EC
- 26,43,44 EC_SMB_SCL_BAT
- 26,43,44 EC_SMB_SDA_BAT
- 18,71,73 CPU_SMB_SCL_P1
- 18,71,73 CPU_SMB_SDA_P1
- 43 BAT_IN_N
- 30 HP_JACK_IN
- 25 MAIN_BUS_EN_N

KB

- 65 KCOL[15:0]
- 65 KROW[7:0]

CPU

- 17,63,99 PM_PWRBTN_N
- 25 EC_SPI_CS_CPU_N0
- 25 EC_SPI_CLK_CPU
- 25 EC_SPI_SO_CPU
- 25 EC_SPI_SI_CPU
- 18 ESPI_CPU_IO0
- 18 ESPI_CPU_IO1
- 18 ESPI_CPU_IO2
- 18 ESPI_CPU_IO3
- 18 ESPI_CPU_CLK
- 18 ESPI_CPU_CS_N
- 18 ESPI_CPU_RST_N
- 65 -LED_CAPSLOCK
- 27 SPK_MUTE_N
- 3 PECI_CPU
- 17 AC_PRESENT
- 17,99 RSMRST_KBC_N
- 3,44,46,73 PROCHOT_CPU_N
- 17 S0_PWRGD
- 12,31,33,40,61,63,71,89,91 PLTRST_CPU_N
- 15 ME_UNLOCK
- 17,99 PM_SLP_S0_N
- 17,40,61,99 PM_SLP_S3_N
- 17,40,99 PM_SLP_S4_N
- 17,40,61 PM_SLP_SUS_N
- 18,25 RTCRST_ON
- 17 DSW_PWROK
- 17,40 ALL_SYS_PWRGD
- 20 MODERN_STANDBY
- 17 PM_SLP_LAN_N

POWER

- 45 PWR_5V_EN
- 40,45 PWR_3D3V_EN
- 35 USB_PWR_AOU_EN2
- 24,35 USB3_PORT2_ON
- 21,61 WIFI_RF_EN_CPU

FAN/Thermal

- 26 FAN_PWM
- 26 THERM_TACH
- 26,40,42,73 PURE_HW_SHUTDOWN_N
- 27 KBC_BEEP
- 65 TP4_RESET
- 65 EC_PS2_SDA_TPAD
- 65 EC_PS2_SCL_TPAD
- 40 S5_ENABLE
- 66 IR_CAM_WP_N

All SYS_PWRGD Delay 99ms to SYS_PWROK

Delay 10ms

Delay 10ms for non_DSW

KBC PWR supply at PSL mode.

EC_ENABLE#

SYS_PWROK

VeSPI

To LCD

Bom Control use 071.00068.0A0G

SKU ID Settings

SKU_ID_DET(GPIO03)		Pull Low (R2445)	Pull High (R2446)	VOLTAGE
TGL	VPRO	100.0K	10.0K	3.0V
	NON-VPRO	100.0K	20.0K	2.75V
CELERON	VPRO	100.0K	33.0K	2.48V
	NON-VPRO	100.0K	47.0K	2.24V
	VPRO	100.0K	64.9K	2.0V
	NON-VPRO	100.0K	76.8K	1.87V
	VPRO	100.0K	100.0K	1.65V
	NON-VPRO	100.0K	143.0K	1.358V
	VPRO	100.0K	174.0K	1.204V
	NON-VPRO	100.0K	215.0K	1.048V

<-- LOGIC

Board ID Settings

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
19837-SA	100.0K	10.0K	3.0V
19837-SB	100.0K	20.0K	2.75V
19837-SC	100.0K	33.0K	2.48V
19837-SD	100.0K	47.0K	2.24V
19837-1	100.0K	64.9K	2.0V
	100.0K	76.8K	1.87V
	100.0K	100.0K	1.65V
	100.0K	143.0K	1.358V
	100.0K	174.0K	1.204V
	100.0K	215.0K	1.048V

<-- LOGIC

1.Enter PSL mode (Entry S5 after 10sec) : 3D3V_AUX_KBC : OFF (KBC PWR supply)
2.At PSL mode (SPEC: S5<10mW)

S0	S3	S5	DS
H	H	H	L

PSL mode(AC or DC):

EC_PSL_EN#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):

EC_PSL_EN#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

Prevent BIOS data loss solution

HW strapping (Strap1:0)
00: eSPI share mode
11: LPC nonshare mode

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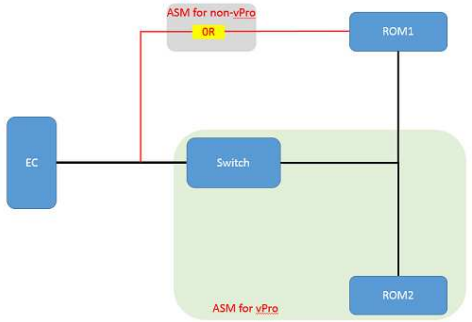
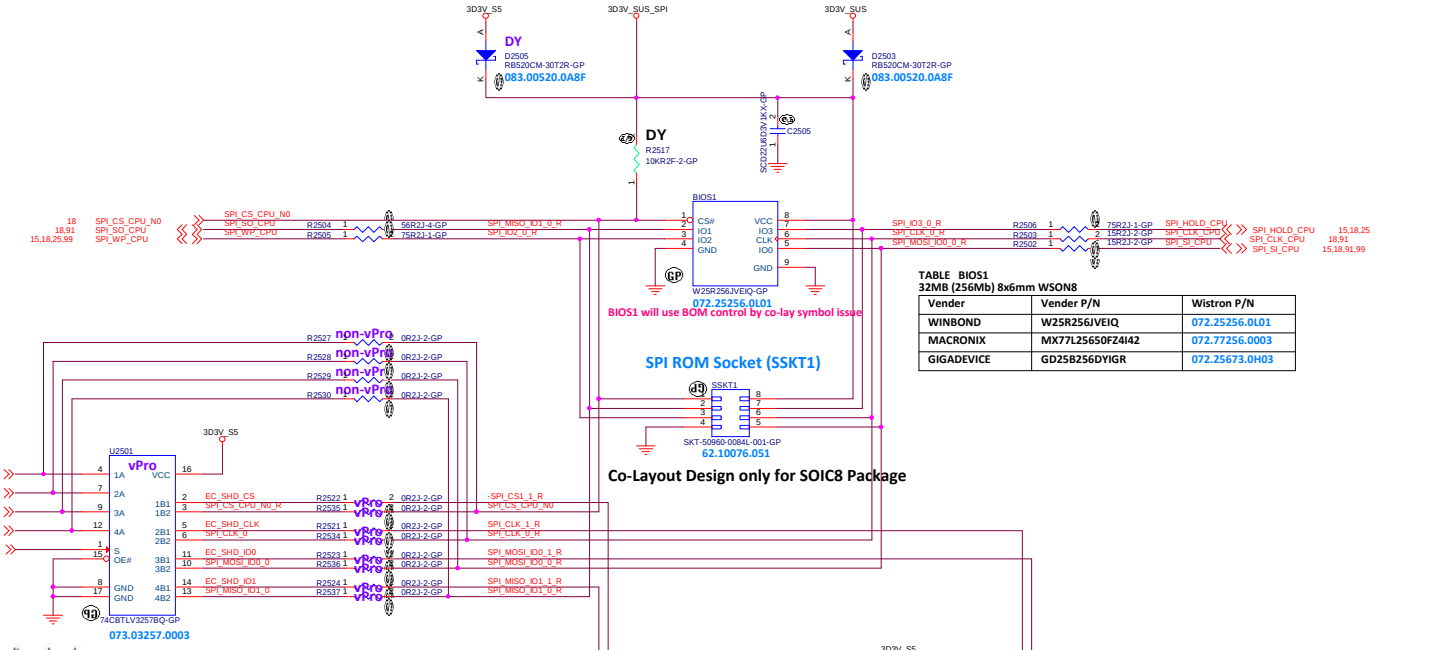
Title	ECIO (Nuvoton NPCE68APA0DX)
Size: Custom	Document Number: ARES-2
Rev: 1	
Date: Thursday, August 06, 2020	Sheet 24 of 106

Main Func = SPI Flash



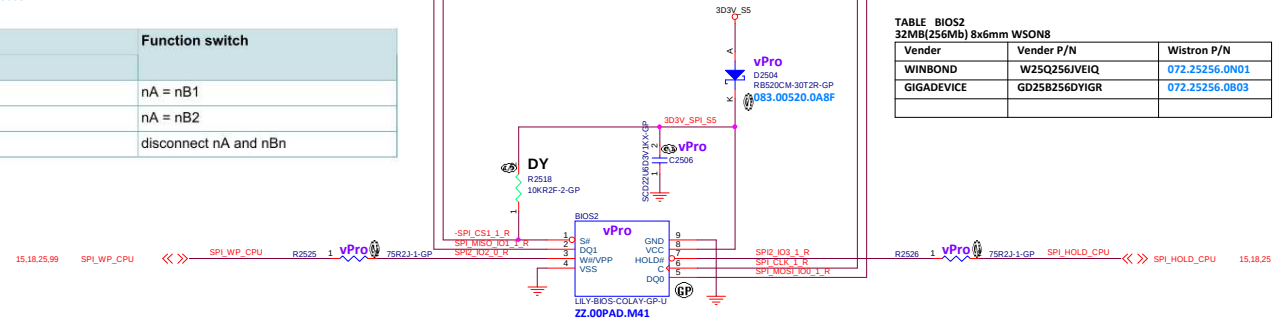


Vender	Vender P/N	Wistron P/N
WINBOND	W25R256JVEIQ	072.25256.0L01
MACRONIX	MX77L25650FZ4I42	072.77256.0003
GIGADEVICE	GD25B256DYIGR	072.25673.0H03

TABLE BIOS1
32MB (256Mb) 8x6mm WSON8

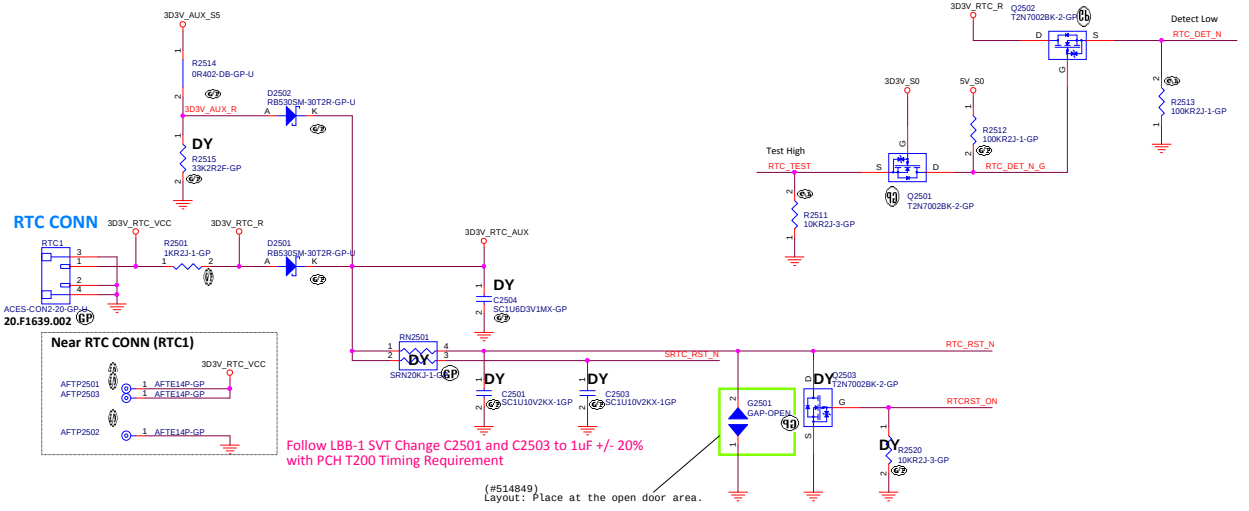
H = HIGH voltage level; L = LOW voltage level.

Inputs		Function switch
OE	S	
L	L	nA = nB1
L	H	nA = nB2
H	X	disconnect nA and nBn



Vender	Vender P/N	Wistron P/N
WINBOND	W25Q256JVEIQ	072.25256.0N01
GIGADEVICE	GD25B256DYIGR	072.25256.0B03

Main Func = RTC



LAR-2

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Title: FLASH/RTC
Size: A2 | Document Number: ARES-2 | Rev: 1
Date: Thursday, August 06, 2020 | Sheet 25 of 106

Main Func = Thermal Sensor

Thermal Sensor

Sensor	Target
U2601	SSD
U2603	DIMM
Q2601	CPU
Q2602	Charger

Close to PL4401(Charger)

Ch2

Close to CPU (CPU1)

2200p close to Thermal Sensor chip

Ch1

T8

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

Layout NOTE:
VDD trace width: 20 mil less

Close to SSD (SSD1)

FAN Controller

NCT718W 's maximum power consumption can be xxx mA (TBD)

Layout NOTE:
VDD trace width: 20 mil less

Close to SODIMM (DM1,DM2)

ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)

NCT7717U Table:

R2619 \ R2620	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125

NCT7718W Table:

R2619 \ R2620	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125

ALERT# point hardware power-on setting

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2kΩ	75
	7.5kΩ	90
	10.5kΩ	100
	14kΩ	105
	18.7kΩ	110

Close to Charger

PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

OR by Project Team requested

FAN CONN

Near FAN CONN (FAN1)

TABLET

ID	Target	Function
RT2601		
RT2602		
RT2603		
RT2605		
RT2606		
RT2607		
RT2608		

5V *100K/(100K+40K) = 3.57V

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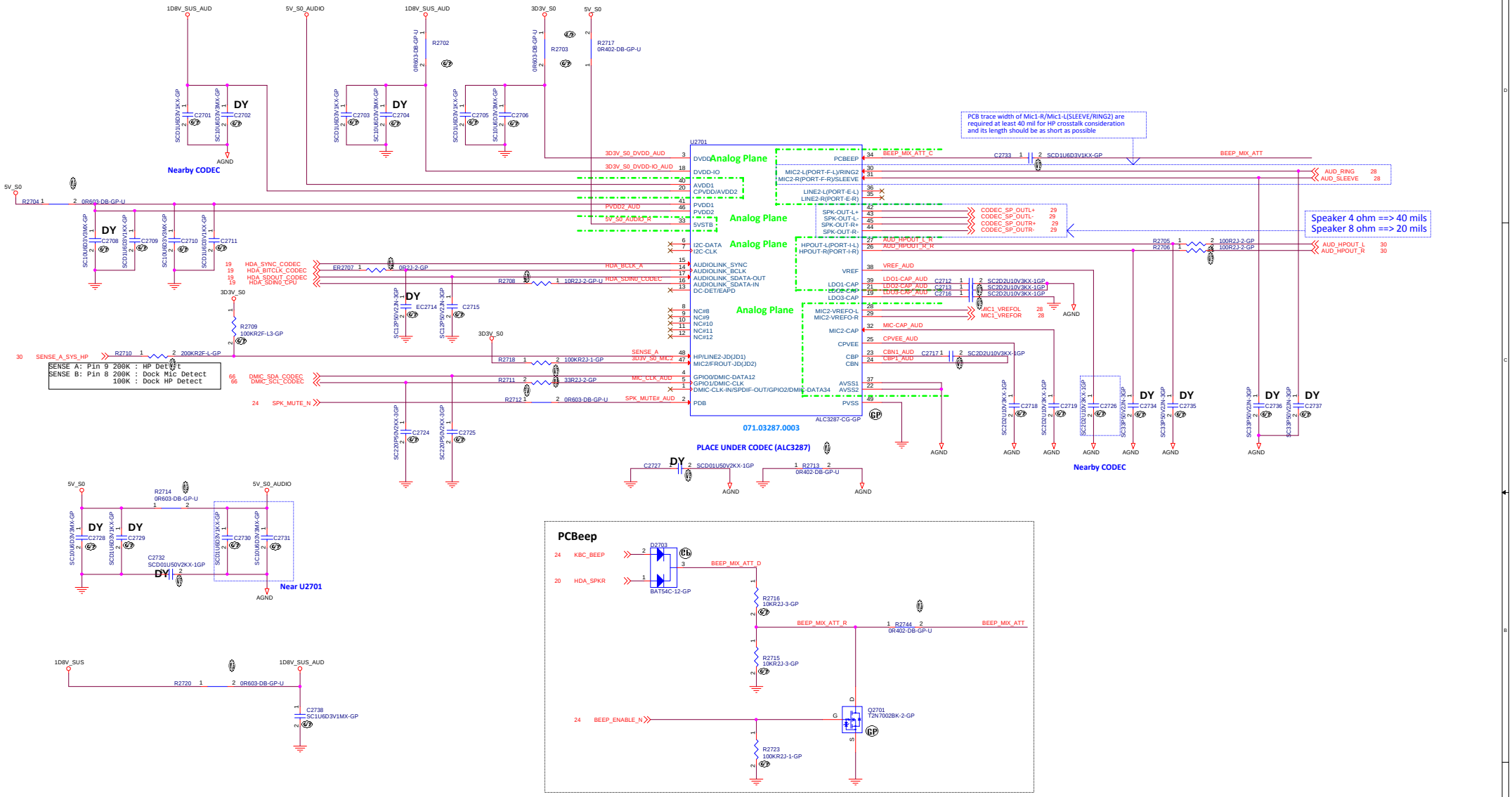
Title: INT IO (THERMAL/FAN)

Size: A1 | Document Number: ARES-2 | Rev: 1

Date: Thursday, August 06, 2020 | Sheet 26 of 106

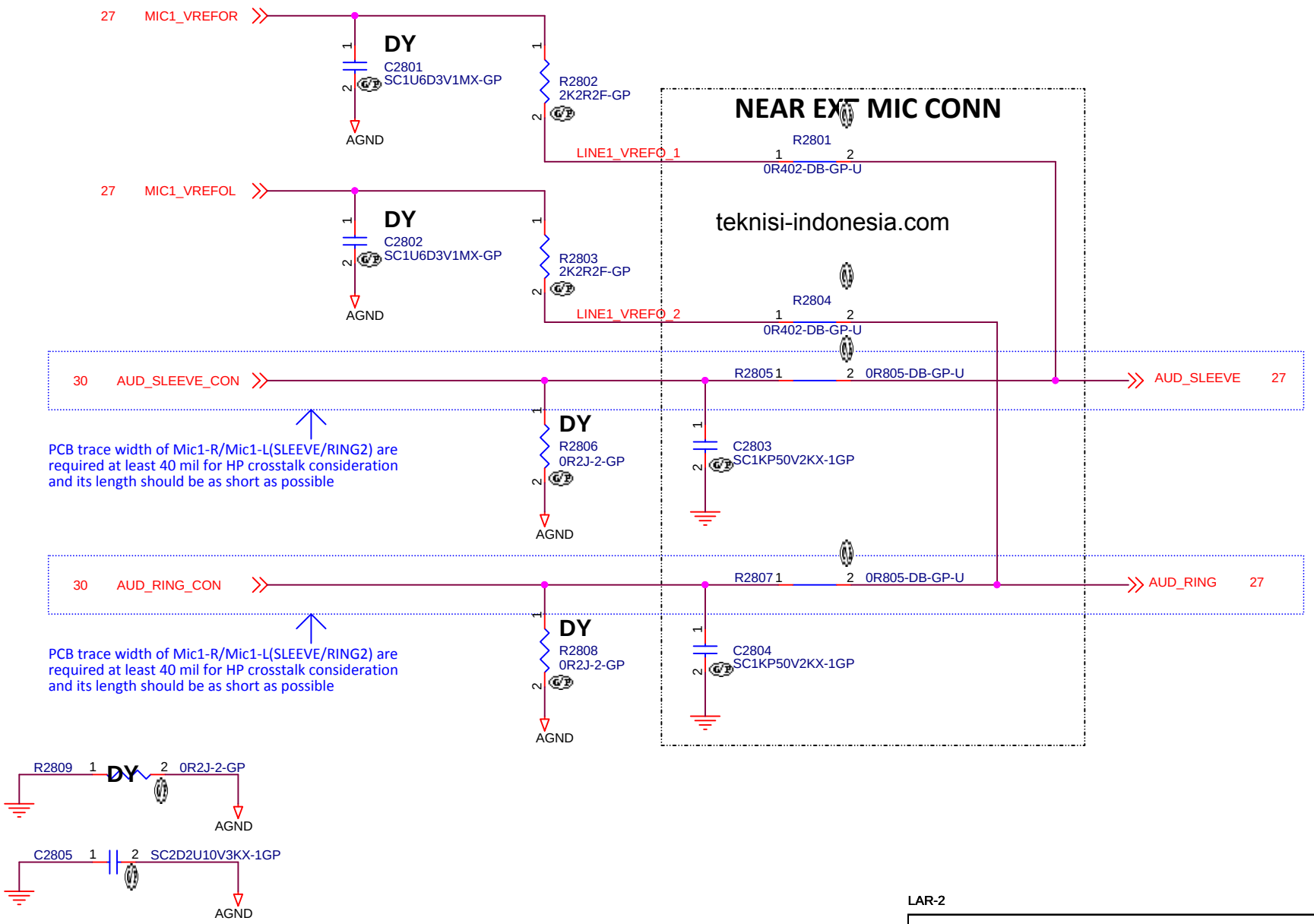
Main Func = Audio



LAR-2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO (CODEC CX11880-11Z)		
Size: A2	Document Number: ARES-2	Rev: 1
Date: Thursday, August 06, 2020	Sheet 27 of 106	

Main Func = Audio



LAR-2

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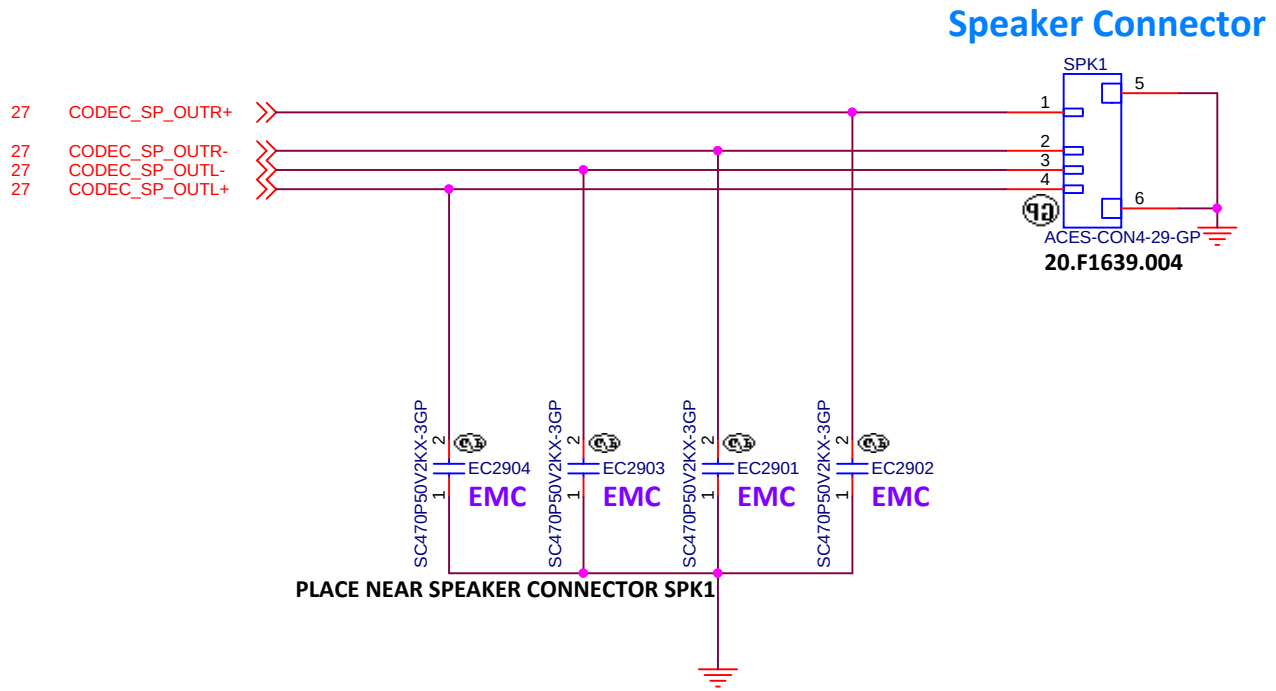
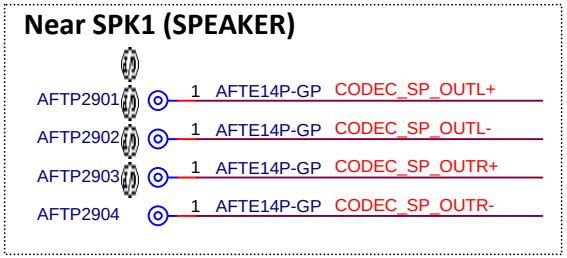
Title: ***AUDIO (MIC I/F)***

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 28 of 106

Main Func = AUDIO





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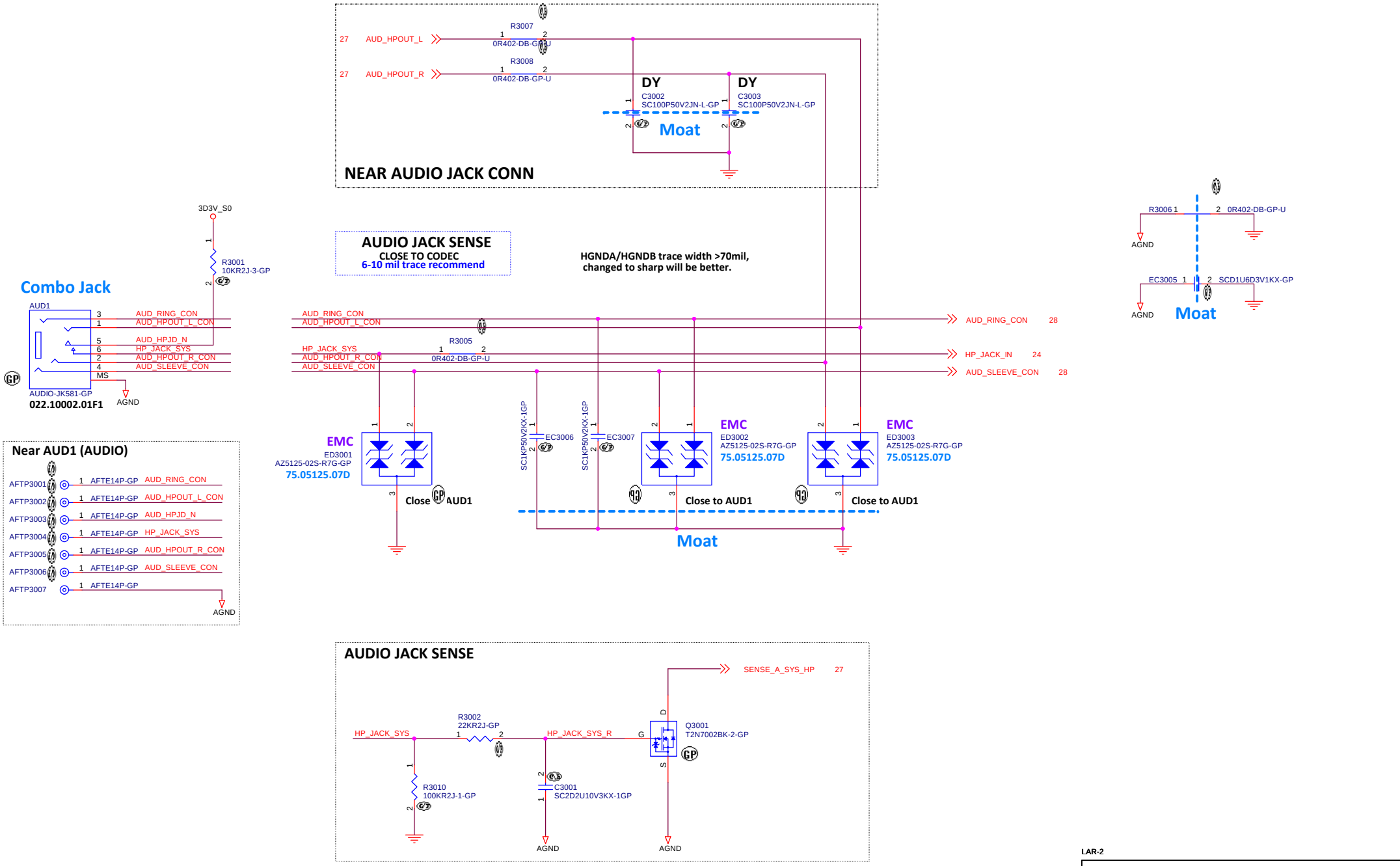
Title: ***AUDIO (SPEAKER)***

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 29 of 106

Main Func = Audio



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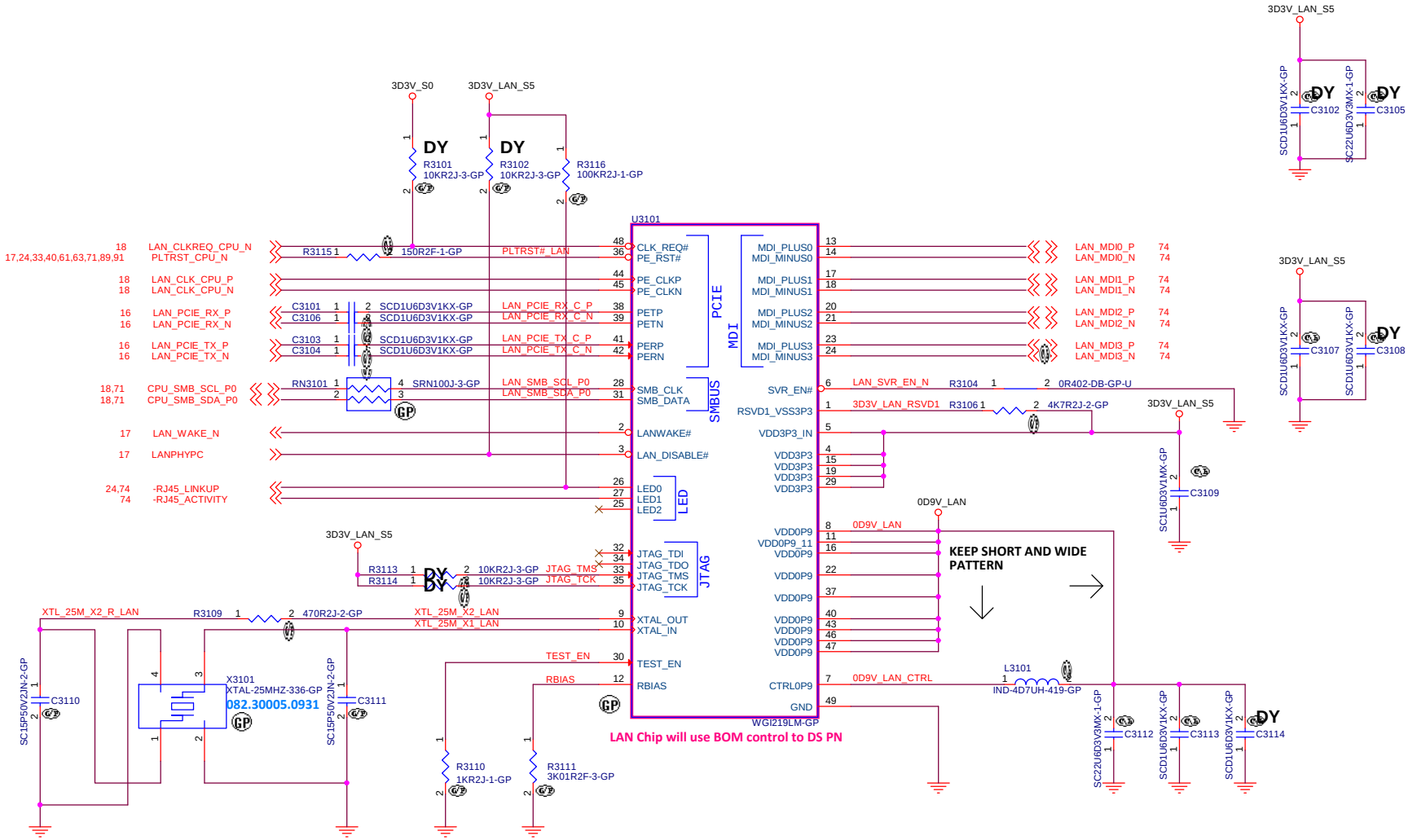
Title: *AUDIO (AUDIO JACK)*		
Size: A3	Document Number: ARES-2	Rev: 1
Date: Thursday, August 06, 2020	Sheet 30 of 106	

Main Func = LAN



25MHz (X3101)

TXC	7R25000008	082.30005.0931
HARMONY	X2V025000DC1H-HU	082.30005.0A81

LAR-2

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Title: ***LAN (GIGA_WGI219LM)***

Size	Document Number	Rev
A3	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 31 of 106

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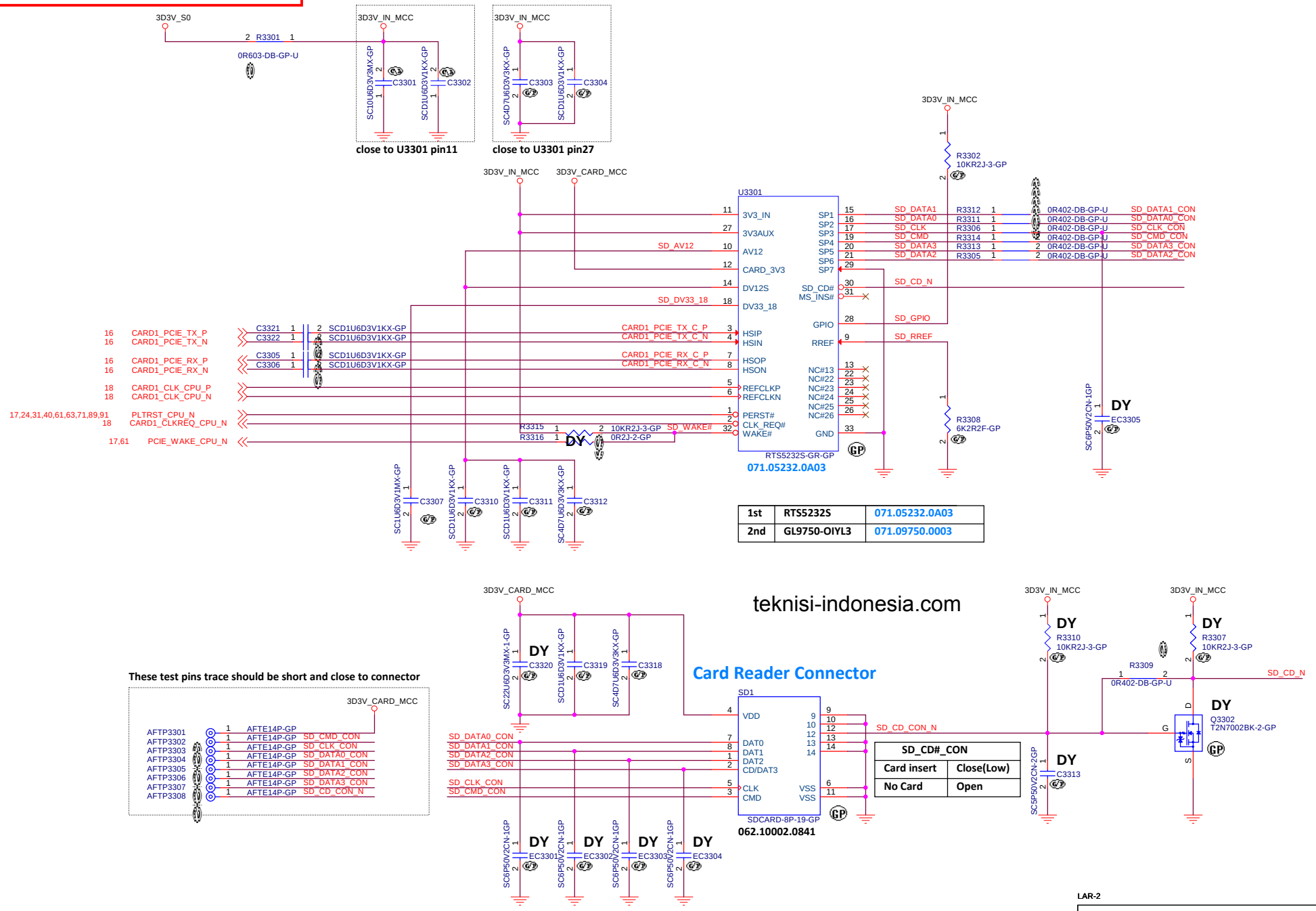
Title ***LAN (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 32 of 106

Main Func = Card Reader



1st	RTS5232S	071.05232.0A03
2nd	GL9750-OIYL3	071.09750.0003

These test pins trace should be short and close to connector

Card Reader Connector

SD_CD#_CON	
Card insert	Close(Low)
No Card	Open

LAR-2

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Title: **CARD READER (SDIO/CONN)**

Size	Document Number	Rev
A3	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 33 of 106

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LAR-2

緯創資通 **Wistron Corporation**
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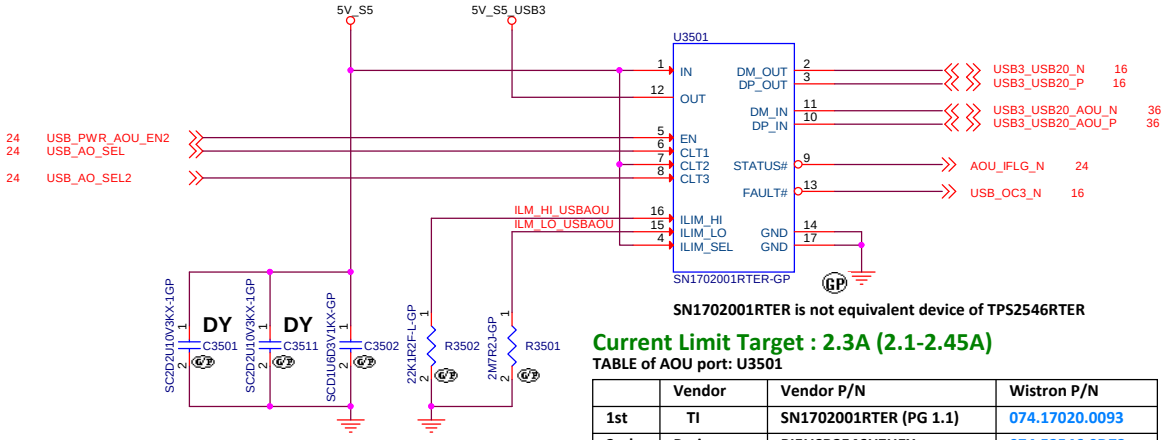
Title: *USB (RSVD)*

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 34 of 106

Main Func = USB Charger

For USB3.0 System Port3 (For AOU)



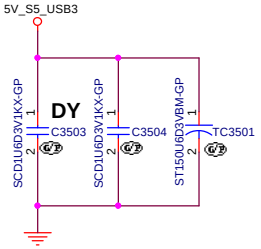
SN1702001RTER is not equivalent device of TPS2546RTER

Current Limit Target : 2.3A (2.1-2.45A)

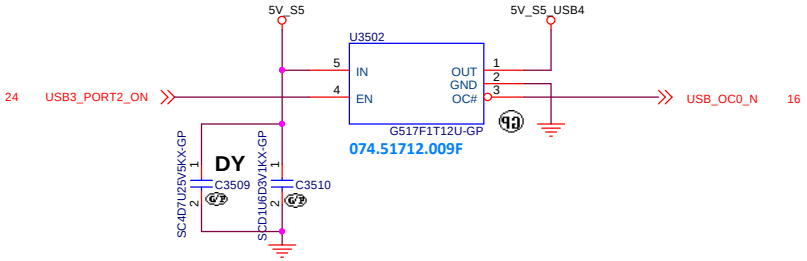
TABLE of AOU port: U3501

	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER (PG 1.1)	074.17020.0093
2nd	Pericom	PI5USB2546HZHEX	074.52546.0D73

Layout Note: Close USB3.0 Port3



For USB3.0 System Port4

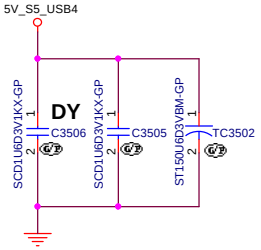


Continous Current Limit 1.5A

TABLE of USB 3.0 port: U3502

	Vendor	Vendor P/N	Wistron P/N
1st	GMT	G517F1T12U	074.51712.009F
2nd	SILERGY	SY6288C20AAC	074.06288.007B

Layout Note: Close USB3.0 Port4



LAR-2

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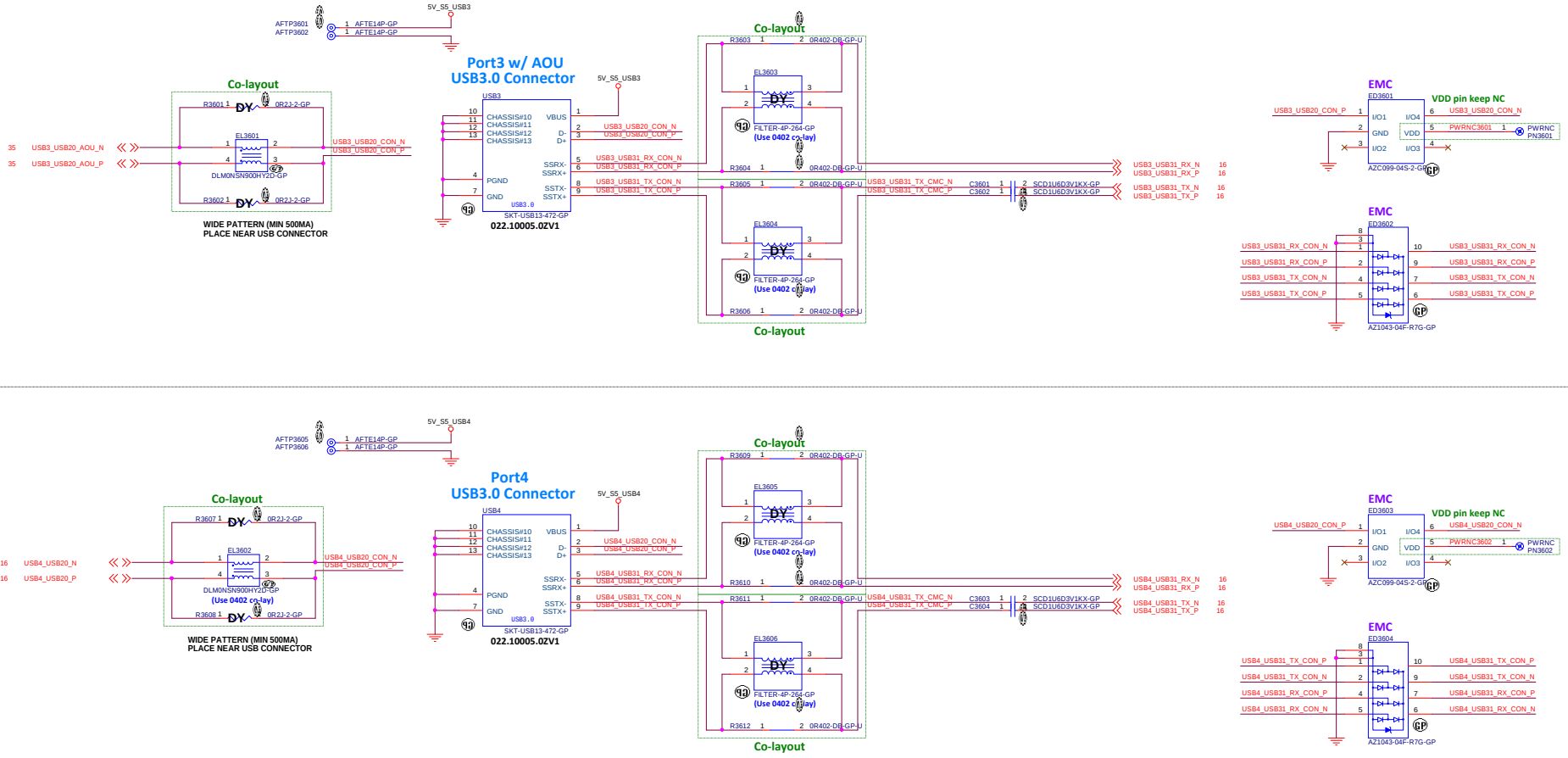
Title: *USB (CHARGER/SWITCH)*

Size	Document Number	Rev
A3	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 35 of 106

Main Func = USB3.0 Port3 w/ AOU

Main Func = USB3.0 Port4



LAR-2

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Title: USB (USB3.0 CONN)

Size: A2 | Document Number: ARES-2 | Rev: 1

Date: Thursday, August 06, 2020 | Sheet 36 of 106

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Title: *USB (RSVD)*

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 37 of 106

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LAR-2

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Title: ***USB (RSVD)***		
Size: A4	Document Number: **ARES-2**	Rev: **1**
Date: Thursday, August 06, 2020	Sheet 38 of 106	

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LAR-2

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Title ***SEQUENCE (RSVD)***

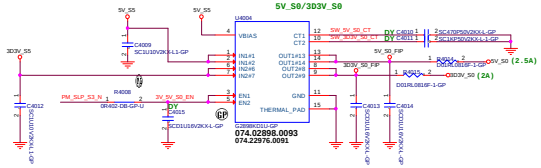
Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 39 of 106

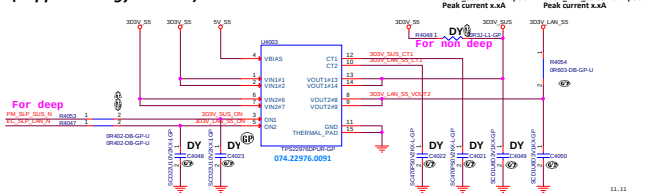
RUN Power

RUN Power

5V_S0/3D3V_S0



For Deep Sx Configured Systrem (Support Energy Star 7.0)

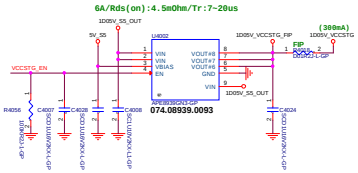


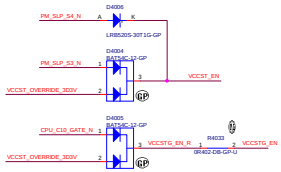
3D3V_SUS

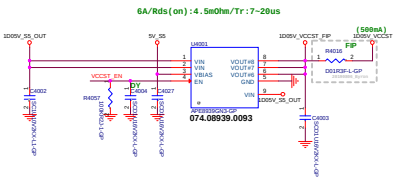
3D3V_SUS Comsumption
Peak current x.xA

3D3V_LAN_S5

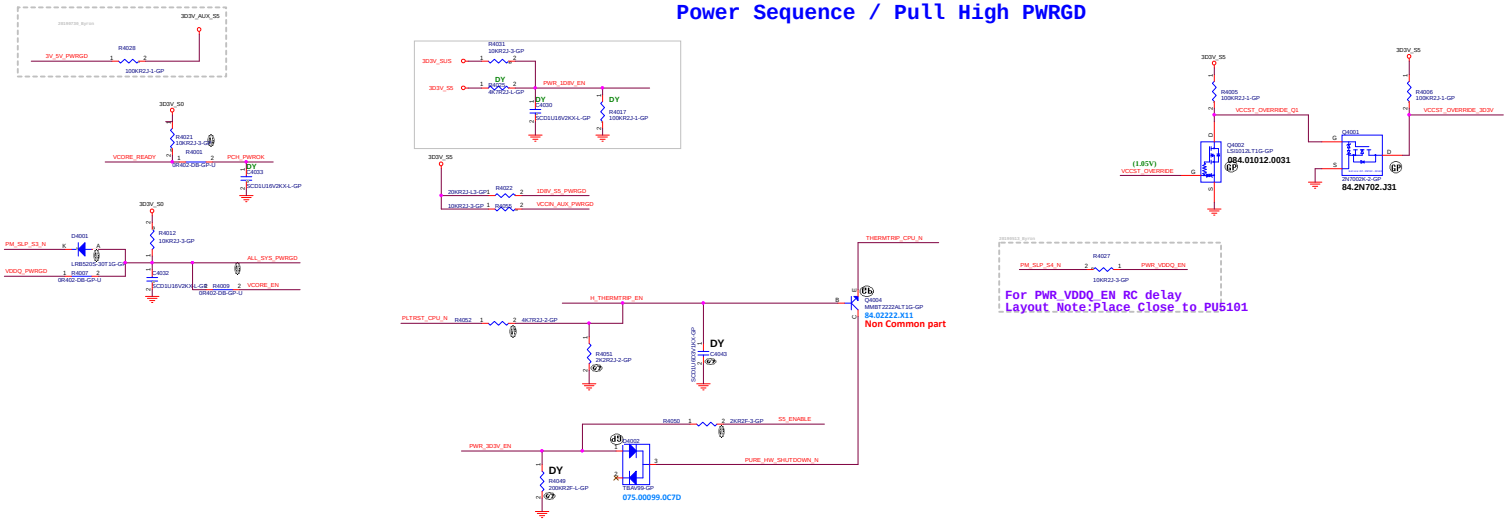
3D3V_LAN_S5 Comsumption
Peak current x.xA







Power Sequence / Pull High PWRGD



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LAR-2

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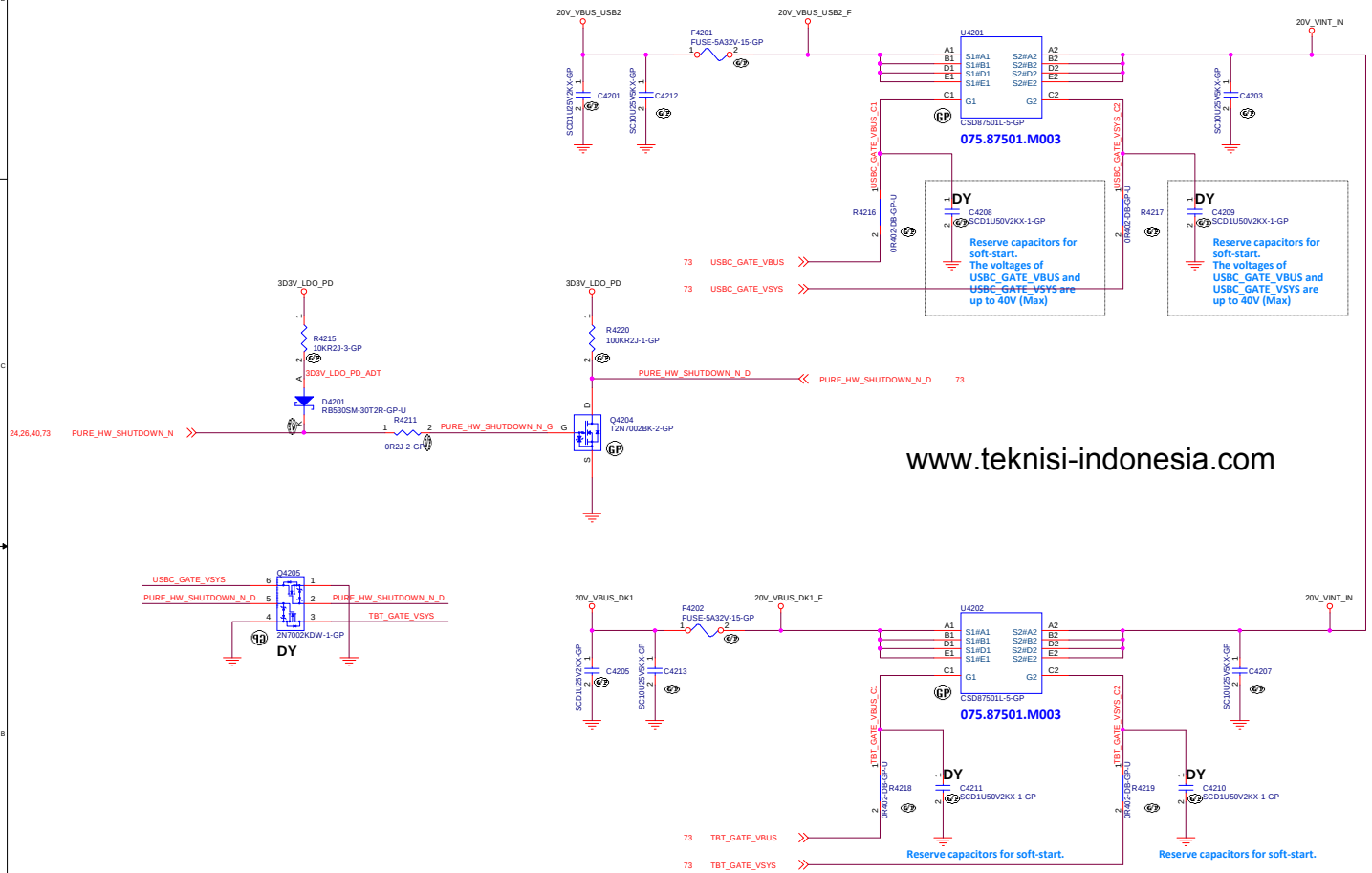
Title ***SEQUENCE (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 41 of 106

Main Func = ADT Input



LAR-2

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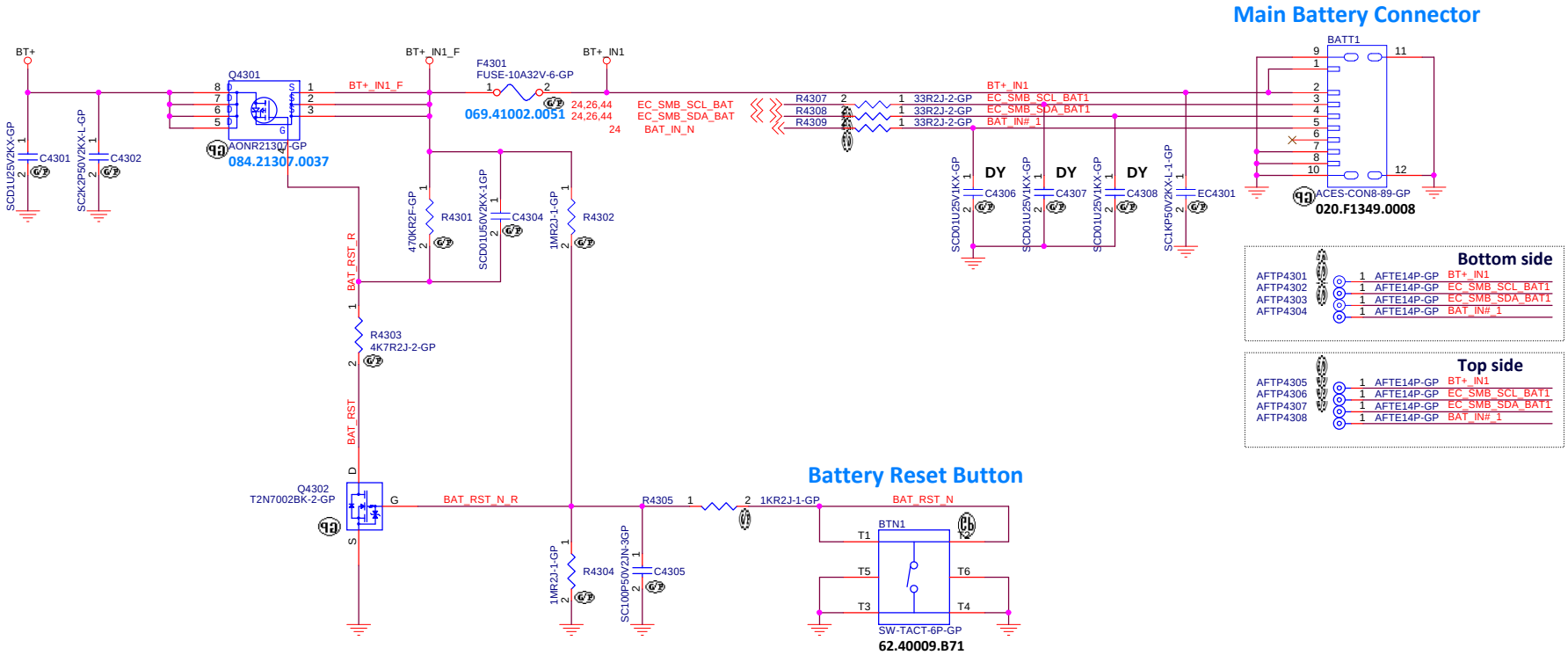
Title: INT IO (DC-IN)

Size: A2 | Document Number: ARES-2 | Rev: 1

Date: Thursday, August 06, 2020 | Sheet 42 of 106

Main Func = M-BAT Input
Main Func = BAT Reset



LAR-2

緯創資通 **Wistron Corporation**
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Title: ***INT IO (BATT CONN)***

Size	Document Number	Rev
A3	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 43 of 106

OFFPAGE - PIC - EE

PH on EE Side

24,26,63 EC_SMB_SCL_BAT ↔ EC_SMB_SCL_BAT
24,26,63 EC_SMB_SDA_BAT ↔ EC_SMB_SDA_BAT

PH on EE Side

3,24,26,73 PROCHOT_CPU_N ↔ PROCHOT_CPU_N

46 CHGR_PSYS_IMVP ↔ CHGR_PSYS_IMVP
24 AC_IN_N ↔ AC_IN_N
24 AD_IA ↔ AD_IA

Device will be transition from normal Buck/Boost operation to PTM operation by:
- Set REGN0 [7] = 0, to disable the EN_EXITILIM.
- Set REGN0[6] = 1.
- Set REGN0[1] = 1.
- Ground ILIM_HIZ pin.

Device will transition out of PTM mode with host control by:
- Set REGN0[1] = 0.
- Pull ILIM_HIZ pin to high.
- Device exits PTM to buck-boost operation if tripping VINDPM or IINDPM.
- Device exits PTM to buck-boost operation under fault conditions (VCOC, TSHUT, BATOC).

EC_SMB_SCL_BAT — PR4459 0R0402-PAD-1-GP — PWR_CHG_SCL
EC_SMB_SDA_BAT — PR4460 0R0402-PAD-1-GP — PWR_CHG_SDA
AD_IA — PR4457 0R0402-PAD-1-GP — PWR_CHG_IADP
PROCHOT_CPU_N — PR4458 0R0402-PAD-1-GP — PWR_PROCHOTB_CPU
CHGR_PSYS_IMVP — PR4461 0R0402-PAD-1-GP — CHGR_CHG_PSYS

For Adapter IN
Confirm with EE

20V_VINT_IN — PR4419 — D01R0721F-GP-U — 20V_VINT_IN_R

CHARGER_HS — PU4403 — PS808BA-GP — 084.00606.0037
CHARGER_LS — PU4404 — PS808BA-GP — 084.00606.0C37

2.2uH, DCR=10-20mohm, ISC=8A, Isat=14A 6.8*6.4*3mm
PL4401 — IND-2D2UH-46-GP-U1

CHARGER_HS — PU4405 — PS808BA-GP — 084.00606.0037
CHARGER_LS — PU4406 — PS808BA-GP — 084.00606.0C37

18V_DCBATOUT

PU4409 — RJH60F7BDPQ-A0#T2 — PWR_CHG_BAT

BT1

	V(ILIM)	PR4623
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Inductor	R(IADP)	Fsw at POR
1.0uH	93K ohm	1200KHz
1.5uH	110K ohm	800KHz
2.2uH	137K ohm	800KHz
3.3uH	169K ohm	800KHz

# of CELL	VCELL_PRES	PR4413
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

Reserve for Power test

Reserve for PTM
If it hasn't more GPIO

$V_{PSYS} = R_{PSYS} \times K_{PSYS} (V_{ACP} \times I_N - V_{BAT} \times I_{BAT})$

0505
buyer: 7"

2N7002K-2-GP
84.2N702.J31
3rd = 84.2N702.W31
3rd = 84.2N702.031

LAN-2

Wistron Corporation	21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	BQ25710R_Charger
Size: Custom	Document Number: ARES-2
Rev: 1	
Date: Wednesday, August 04, 2021	Sheet 44 of 69

OFFPAGE-Signal

24,40 PWR_3D3V_EN >> PWR_3D3V_EN

PH on EE Side

40 3V_5V_PWRGD >> PR4502 1 2 PWR_3D3V_PG

DR0402-PAD-1-GP

24 PWR_5V_EN >> PWR_5V_EN

OFFPAGE-GAP

19V_DCBATOUT — PWR_DCBATOUT_3D3V
PG4515 GAP-CLOSE-PWR-3-GP
PG4516 GAP-CLOSE-PWR-3-GP
PG4517 GAP-CLOSE-PWR-3-GP
PG4518 GAP-CLOSE-PWR-3-GP

3D3V_S5 — PWR_3D3V
PG4519 GAP-CLOSE-PWR-3-GP
PG4520 GAP-CLOSE-PWR-3-GP
PG4521 GAP-CLOSE-PWR-3-GP
PG4522 GAP-CLOSE-PWR-3-GP
PG4523 GAP-CLOSE-PWR-3-GP
PG4524 GAP-CLOSE-PWR-3-GP

3D3V_AUX_S5 — PWR_3D3V_LDO
PG4532 GAP-CLOSE-PWR-3-GP

19V_DCBATOUT — PWR_DCBATOUT_5V
PG4552 GAP-CLOSE-PWR-3-GP
PG4553 GAP-CLOSE-PWR-3-GP
PG4555 GAP-CLOSE-PWR-3-GP
PG4557 GAP-CLOSE-PWR-3-GP
PG4559 GAP-CLOSE-PWR-3-GP
PG4561 GAP-CLOSE-PWR-3-GP

5V_S5 — PWR_5V
PG4551 GAP-CLOSE-PWR-3-GP
PG4554 GAP-CLOSE-PWR-3-GP
PG4556 GAP-CLOSE-PWR-3-GP
PG4558 GAP-CLOSE-PWR-3-GP
PG4560 GAP-CLOSE-PWR-3-GP
PG4563 GAP-CLOSE-PWR-3-GP
PG4564 GAP-CLOSE-PWR-3-GP
PG4566 GAP-CLOSE-PWR-3-GP

5V_AUX_S5 — PWR_5V_LDO
PG4565 GAP-CLOSE-PWR-3-GP

IDC : 6A
OCP : 8A

Vin Operating range : 4~23V
Vin_Max : 25V
Ilimt : 8A

Cyntec. 6.8 x7.3 x 2.4mm
DCR: 17~20mOhm
Idc : 9A , Isat : 15A

PR4501 0R0603-PAD-1-GP-U
PC4506 SCD1U25V2KX-L-GP
PWR_3D3V_BOOT
PWR_3D3V_BOOT_A
PWR_3D3V_VCC
PC4522 SC2D2U10V3KX-L-GP

PWR_DCBATOUT_3D3V
PC4502 SC10U25V5KX-L-GP
PC4503 SC10U25V5KX-L-GP
PC4513 SCD1U25V2KX-L-GP

PU4501 TPS51393PRJER-GP
VIN, SW#6, SW#19, SW#20, NC#10, LDO, NC#16, EN, ENLDO, BOOT, PGOOD, FB, VOUT, VCC, GND
PWR_3D3V_EN
PWR_3D3V_EN2
PWR_3D3V_BOOT
PWR_3D3V_PG
PWR_3D3V_FB
PWR_3D3V_PH
PWR_3D3V_LDO

PL4501 COIL-1D5UH-29-GP
PWR_3D3V
PC4509 PC4510 PC4511 SC22U6D3V3MX-L1-GP
PC4512 DY SC22U6D3V3MX-L1-GP
PC4507 SC10U6D3V3MX-L-GP

PR4514 1MR2J-1-GP

EN rating :5 .5V
EN Rising Threshold :1.5V
EN Falling Threshold : 0.4V
Ilimt : 8A

Place another side , make GND plan bigger

Trace used 10 mil
PWR_3D3V_VOUT
Close to PC4511
PG4530 GAP-CLOSE-PWR-3-GP

PC4526 SC470P50V2KX-L-GP
PWR_3D3V_FB2
PR4506 240KR2F-L-GP

PR4512 300KR2J-GP
PR4513 100KR2J-1-GP
DY PR4505 100KR2J-1-GP
3D3V_AUX_S5

5V_AUX_S5
PR4552 100KR2J-1-GP DY
Place another side , make GND plan bigger

IDC:8A

PWR_DCBATOUT_5V
PC4554 SC10U25V5KX-L-GP
PC4555 SC10U25V5KX-L-GP
PC4564 SCD1U25V2KX-L-GP
For 2cell use

PU4551 TPS51395PRJER-GP
VIN, NC#10, NC#16, VCC, EN, ENLDO, PGOOD, BOOT, SW#6, SW#19, SW#20, VOUT, FB, LDO, GND
PWR_5V_PG
PWR_5V_BOOT
PWR_5V_BOOT_A
PWR_5V_PH
PWR_5V_VOUT
PWR_5V_FB
PWR_5V_FB_A
PWR_5V_VCC
PWR_5V_EN
PWR_5V_EN2
PWR_5V_LDO

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A

PR4554 0R0603-PAD-1-GP-U
PC4553 SCD1U25V2KX-L-GP
PL4551 IND-1D5UH-23-GP-U
PWR_5V
PC4556 PC4557 PC4558 PC4559 PC4560 PC4561 DY SC22U6D3V3MX-L1-GP
For 2cell use

Trace used 10 mil
PG4562 GAP-CLOSE-PWR-3-GP
PR4555 324KR2F-GP
PC4563 SC1KP50V2KX-L-1-GP
PC4562 SC2D2U10V3KX-L-GP
PC4551 SC10U6D3V3MX-L-GP

EN rating :5.5V
EN Rising Threshold : 1.5V
Ilimt : 8A

PR4556 1MR2J-1-GP
PWR_DCBATOUT_5V
PR4511 300KR2J-GP
PR4510 100KR2J-1-GP

LAR-2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51393/TPS51395R_5V/3D3V
Size: Custom | Document Number: ARES-2 | Rev: 1
Date: Thursday, August 06, 2020 | Sheet 45 of 106

OFFPAGE
Check PIC-EE

3,24,44,73 PROCHOT_CPU_N — PROCHOT_CPU_N

7 SVID_CLK_CPU — SVID_CLK_CPU
7 SVID_DATA_CPU — SVID_DATA_CPU
7 SVID_ALERT_CPU_N — SVID_ALERT_CPU_N

PR4603 0R0402-PAD-1-GP
40 VCORE_EN — PWR_VCORE_VR_EN
PR4602 0R0402-PAD-1-GP
40 VCORE_READY — PWR_VCORE_VR_READY

7 VSSCORE_SENSE — VSSCORE_SENSE
7 VCCCORE_SENSE — VCCCORE_SENSE

44 CHGR_PSYS_IMVP — CHGR_PSYS_IMVP

1D05V_VCCST — PG4601 GAP-CLOSE-PWR-3-GP — PWR_VCORE_VCCST

Reserve for Power test

3D3V_S0
PR4607 10KR2F-L1-GP DY
PWR_VCORE_VR_READY

PWR_VCORE_VCCST
PR4613 1KR2F-3-GP DY
PR4688 0R0402-PAD-1-GP
CHGR_PSYS_IMVP — PWR_VCORE_PSYS
PR4689 100R2F-L3-GP
PROCHOT_CPU_N — PWR_VCORE_VRHOT

VBOOT=1.8V
Fsw=568kHz@VIN=7.4V
ICCMAX=80A
Disable QR
Disable DVID LIFT

PU4601

5V_S5
PR4604 6D2R5F-GP
PWR_VCORE_VCC — PC4602 SC10U6D3V3MX-L-GP — VCC 24

PWR_VCORE_VRHOT — VR_HOT# 16

PWR_VCORE_VREF
PR4615 3D9R2F-GP
PWR_VCORE_VREF_A — PWR_VCORE_VREF — VREF06 26
PC4606 SCD47U25V3KX-1GP

PR4619 1K4R2F-1-GP
PR4620 1K21R2F-GP
PR4621 9K09R2F-GP
PR4622 14K4R2F-GP
PWR_VCORE_SET1_A
PWR_VCORE_SET2_A
PWR_VCORE_SET3_A

47 PWR_VCORE_DRVEN — DRVEN 15
PR4670 100KR2F-L1-GP DY

PR4666 57K6R2F-GP
PR4660 14K7R2F-GP
PR4661 100R2F-L1-GP-U
47 PWR_VCORE_TSEN
47 PWR_VCORE_TSEN_A
PWR_VCORE_TSEN_A — PWR_VCORE_TSEN — TSEN 7

ICCMAX = 72A

PWR_VCORE_SET1 — SET1 22
PWR_VCORE_SET2 — SET2 21
PWR_VCORE_SET3 — SET3 20

PR4624 95R3F-GP
PR4625 1K15R2F-GP
PR4626 8K25R2F-GP
PR4627 24K9R2F-L-GP
PWR_VCORE_SET1_B
PWR_VCORE_SET2_B
PWR_VCORE_TSEN_A_A
PWR_VCORE_SET3_B

PR4669 10R2F-GP
PR4668 10R2F-GP
PR4667 100R2F-L1-GP-U
PR4659 200R2F-L-GP

PWR_VCORE_VCCST
PR4630 75R2F-2-GP DY
PR4631 10KR2F-L3-GP
PR4632 45D3R2F-L-GP
PC4609 SCD1U16V2KX-L-GP
PR4634 0R0402-PAD-1-GP
SVID_CLK_CPU — PWR_VCORE_CLK — VCLK 19
PR4636 0R0402-PAD-1-GP
SVID_DATA_CPU — PWR_VCORE_DATA — VDIO 18
PR4674 0R0402-PAD-1-GP
SVID_ALERT_CPU_N — PWR_ALERT#_CPU — ALERT# 17

LL/IMON Compesation
NCP15XH103F03RC
Need confirm with RT If you change Chock

Close to PL4701
PR4639 NTC-100K-12-GP-U
B = 4250
PWR_VCORE_NTC1N

PC4624 SCD1U25V2KX-L-GP DY
PR4637 10KR2F-L1-GP DY
PWR_VCORE_PSYS — PSYS 23

PWR_VCORE_VR_READY — VR_READY 10

PWR_VCORE_VREF
PR4665 1K5R2F-2-GP
PR4677 0R0402-PAD-1-GP
PWR_VCORE_NTC1N_A
PR4643 24K9R2F-L-GP
PWR_VCORE_NTC1P
PR4601 36K5R2F-GP
PWR_VCORE_IMON — IMON 25

RT3613EEGQW-1-GP

19V_DCBATOUT
PR4605 2D2R3F-L-GP
PC4605 SCD22U25V3KX-GP
PWR_VCORE_VIN — VIN 8
PWR_VCORE_VR_EN — VRON 9

PWM1 12 — PWR_VCORE_PWM1 47
PWM2 13 — PWR_VCORE_PWM2 47
PWM3 11
NC#14 14

2K / 0603 Size

ISEN1P 4 — PWR_VCORE_ISEN1P
PR4628 2KR3F-L-GP
PR4655 2KR3F-L-GP
PWR_VCORE_ISEN1P_B — PWR_VCORE_ISEN1P_A 47
ISEN1N 3 — PWR_VCORE_ISEN1N
PR4629 680R2F-GP
PR4662 487R2F-GP
PC4601 SCD1U25V2KX-L-GP
PC4608 SCD1U25V2KX-L-GP
PWR_VCORE_ISEN1N_A 47

ISEN2P 1 — PWR_VCORE_ISEN2P
PR4633 2KR3F-L-GP
PR4646 2KR3F-L-GP
PWR_VCORE_ISEN2P_B — PWR_VCORE_ISEN2P_A 47
ISEN2N 2 — PWR_VCORE_ISEN2N
PR4635 680R2F-GP
PR4663 487R2F-GP
PC4610 SCD1U25V2KX-L-GP
PC4611 SCD1U25V2KX-L-GP
PWR_VCORE_ISEN2N_A 47

2K / 0603 Size

5V_S5
ISEN3P 5
PR4673 10KR2F-L1-GP
PWR_VCORE_ISEN3 — ISEN3N 6

NC#32 32
ANS_EN 31 — PWR_VCORE_ANS_EN
5V_S5
PR4656 10KR2F-L1-GP DY
PR4658 10KR2F-L1-GP

VSEN 28 — PWR_VCORE_VSEN
COMP 29 — PWR_VCORE_COMP
PC4612 SC100P50V2JN-L-GP
PC4613 SC220P50V2KX-3GP
PR4640 31K6R2F-GP
PR4641 10KR2F-2-GP
FB 30 — PWR_VCORE_FB
RGND 27 — PWR_VCORE_RGND
PR4671 0R0402-PAD-1-GP — VCCCORE_SENSE
PR4672 0R0402-PAD-1-GP — VSSCORE_SENSE
GND 33

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LAR-2

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT3613EE_VCORE(1/2)	
Size: Custom	Document Number: ARES-2	Rev: 1
Date: Thursday, August 06, 2020	Sheet 46 of 106	

OFFPAGE

19V_DCBATOUT
PWR_DCBATOUT_VCOREA
PG4702 GAP-CLOSE-PWR-3-GP
PG4703 GAP-CLOSE-PWR-3-GP
PG4704 GAP-CLOSE-PWR-3-GP
PG4705 GAP-CLOSE-PWR-3-GP
PG4706 GAP-CLOSE-PWR-3-GP
PG4707 GAP-CLOSE-PWR-3-GP
PT4703 ST33U25VDM-5-GP

19V_DCBATOUT
PWR_DCBATOUT_VCOREB
PG4710 GAP-CLOSE-PWR-3-GP
PG4711 GAP-CLOSE-PWR-3-GP
PG4712 GAP-CLOSE-PWR-3-GP
PG4713 GAP-CLOSE-PWR-3-GP
PG4714 GAP-CLOSE-PWR-3-GP
PG4715 GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_VCOREA
PC4704 PC4705 PC4706 PC4707 SC10U25V3KX-GP

PR4702 110KR2F-GP
PR4703 NTC-100K-12-GP-U
B = 4250
Close to Phase1 Mosfet
46 PWR_VCORE_TSEN_A
PWR_VCORE_TSEN 46

5V_S5
PR4704 0R0402-PAD-1-GP PWR_VCORE_PVCCA
PR4701 2D2R2F-GP PWR_VCORE_VCCA
PC4731 SC1U10V2KX-L1-GP
PC4702 SC1U10V2KX-L1-GP

PU4701 AOZ5516QI-GP
PR4707 0R0402-PAD-1-GP 46 PWR_VCORE_PWM1
PR4708 0R0402-PAD-1-GP 46,47 PWR_VCORE_DRVEN
PWR_VCORE_PWMA
PWR_VCORE_ZCD_ENA
PWR_VCORE_BOOTA PWR_VCORE_BOOTA_B PC4703 SCD22U25V3KX-GP PWR_VCORE_BOOTA_A PR4706 2D2R3-1-U-GP
PWR_VCORE_PHA
PR4709 2D2R6J-3-GP PWR_VCORE_SNBA
PC4701 SC1KP50V2KX-L-1-GP
46 PWR_VCORE_ISEN1P_A
46 PWR_VCORE_ISEN1N_A

Cyntec. 6.8*7.6*1.8
DCR: 3.28 +- 7% mOhm
Idc : 18A , Isat : 31A
PL4701 IND-D15UH-46-GP
PG4708 GAP-CLOSE-PWR-3-GP
PG4709 GAP-CLOSE-PWR-3-GP
1V_CPU_CORE
PT4701 ST220U2D5VDK-GP

Design Current=39A
Icc(max)=70A
OCP>93A

PWR_DCBATOUT_VCOREB
PC4710 PC4711 PC4712 PC4713 SC10U25V3KX-GP

5V_S5
PR4705 0R0402-PAD-1-GP PWR_VCORE_PVCCB
PR4710 2D2R2F-GP PWR_VCORE_VCCB
PC4734 SC1U10V2KX-L1-GP
PC4708 SC1U10V2KX-L1-GP

PU4702 AOZ5516QI-GP
PR4712 0R0402-PAD-1-GP 46 PWR_VCORE_PWM2
PR4713 0R0402-PAD-1-GP 46,47 PWR_VCORE_DRVEN
PWR_VCORE_PWMB
PWR_VCORE_ZCD_ENB
PWR_VCORE_BOOTB PWR_VCORE_BOOTB_B PC4709 SCD22U25V3KX-GP PWR_VCORE_BOOTB_A PR4711 2D2R3-1-U-GP
PWR_VCORE_PHB
PR4714 2D2R6J-3-GP PWR_VCORE_SNBB
PC4714 SC1KP50V2KX-L-1-GP
46 PWR_VCORE_ISEN2P_A
46 PWR_VCORE_ISEN2N_A

Cyntec. 6.8*7.6*1.8
DCR: 3.28 +- 7% mOhm
Idc : 18A , Isat : 31A
PL4702 IND-D15UH-46-GP
PG4701 GAP-CLOSE-PWR-3-GP
PG4716 GAP-CLOSE-PWR-3-GP
1V_CPU_CORE

LAR-2

緯創資通 Wistron Corporation 2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AOZ5516_VCORE(2/2)		
Size: Custom	Document Number: ARES-2	Rev: 1
Date: Thursday, August 06, 2020	Sheet 47 of 105	

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LAR-2

緯創資通 **Wistron Corporation**
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Title ***POWER (RSVD)***

Size	Document Number	Rev
A	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 48 of 106

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LAR-2

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title **POWER (RSVD)**

Size	Document Number	Rev
A	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 49 of 106

OFFPAGE

40,53 1DBV_S5_PWRGD → 1DBV_S5_PWRGD

PH on EE Side

17,40 VCCIN_AUX_PWRGD → VCCIN_AUX_PWRGD

PH on CPU side

23 CPUCORE_VCCAUX_VID1 → CPUCORE_VCCAUX_VID1

22 CPUCORE_VCCAUX_VID0 → CPUCORE_VCCAUX_VID0

22 VCCAUX_SENSE → VCCAUX_SENSE

22 VSSAUX_SENSE → VSSAUX_SENSE

OFFPAGE_GAP

19V_DCBATOUT — PWR_DCBATOUT_VCCAUX

PG5001 GAP-CLOSE-PWR-3-GP
PG5002 GAP-CLOSE-PWR-3-GP
PG5003 GAP-CLOSE-PWR-3-GP
PG5004 GAP-CLOSE-PWR-3-GP

CPUCORE_VCCAUX_VID1 — PR5034 0R0402-PAD-1-GP — PWR_VCCAUX_VID1
CPUCORE_VCCAUX_VID0 — PR5035 0R0402-PAD-1-GP — PWR_VCCAUX_VID0
1DBV_S5_PWRGD — PR5036 0R0402-PAD-1-GP — PWR_VCCAUX_EN
VCCIN_AUX_PWRGD — PR5037 0R0402-PAD-1-GP — PWR_VCCAUX_PG

1DBV_VCCIN_AUX — PR5017 100R2F-L1-GP-U — VCCAUX_SENSE
VSSAUX_SENSE — PR5018 100R2F-L1-GP-U

OCP : 45A

PR5004 619K0F-GP — PWR_VCCAUX_CS_DIS

5V_S5 — PR5001 5D1R2J-1-GP — PC5001 — 3D3V_S5

PR5002 0R0402-PAD-1-GP — PWR_VCCAUX_PVCC
PR5003 100KR2F-L1-GP — PWR_VCCAUX_VCC
PC5002 — PWR_VCCAUX_PG
PWR_VCCAUX_EN
PWR_VCCAUX_VID1
PWR_VCCAUX_VID0

PR5005 100KR2F-L1-GP
PR5006 100KR2F-L1-GP

DY

HI = 800KHz
Flot = 600KHz
Low = 400KHz

PU5001 RT8543AGQW-GP
074.06543.0073

CS_DIS, PVCC, VCC, PG, EN, VID1, VID0, FSWSEL, BOOT, VSYS, UG, PH, LG, PGND, ISENSEP, ISENSEN, VOUT, COMP, FB, RGND

PWR_VCCAUX_BOOT — PR5007 2D2R5J-2-GP — PC5003 5CD1U25V2K0-L-GP — PWR_VCCAUX_BOOTA
PR5033 1R33-L1-GP — PWR_DCBATOUT_VCCAUX
PC5004 5CD1U25V2K0-L-GP — PWR_VCCAUX_VSYS
PWR_VCCAUX_HG
PWR_VCCAUX_PH
PWR_VCCAUX_LG
PWR_VCCAUX_ISENSEP
PWR_VCCAUX_ISENSEN
PWR_VCCAUX_VOUT
PWR_VCCAUX_COMP
PWR_VCCAUX_FB
PR5038 0R0402-PAD-1-GP
PR5013 0R0603-PAD-1-GP-U — PWR_VCCAUX_VOUTA
PC5032 5C2K2F50V2K-L-GP
PR5014 10K0F-L-GP
PC5011 5C33P50V2J2N-3GP
PR5014 0R0402-PAD-1-GP — PWR_VCCAUX_COMP
PC5012 5C33P50V2J2N-3GP
PR5015 8K45R2F-2-GP
PWR_VCCAUX_FB
VSSAUX_SENSE
VCCAUX_SENSE
PR5016 0R0402-PAD-1-GP
PC5013 5C100P50V2J2N-L-GP

PWR_DCBATOUT_VCCAUX
PU5002 PK6008A-GP
PC5006 — PC5007 — PC5008 — 10U0805K6X-L-GP
PU5003 PK6008A-GP

330uF*1
22uF*9pcs
OCP = 40A
Iccmax= 26A
TDC=10A

Cyntec. 6.8*7.6*1.8
DCR: 3.28 +- 7% mOhm
Idc : 18A , Isat : 31A

PL5003 IND-D15UH-46-GP
1DBV_VCCIN_AUX
PT5001 ST470U2D5VDM-14-GP
ESR: 6 mohm

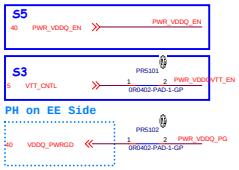
PWR_VCCAUX_PH
PR5019 2D2R5J-3-GP — PWR_VCCAUX_SNB
PC5014 5C1KF50V2K X-L-1-GP

LAR-2

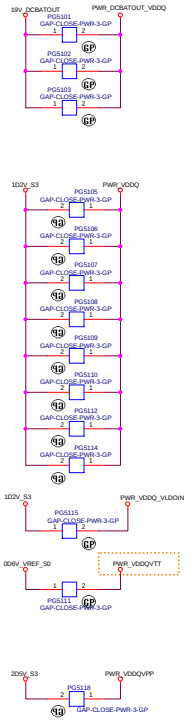
蟑創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8543_VCCAUX**
Size: A1 | Document Number: **ARES-2** | Rev: 1
Date: Thursday, August 06, 2020 | Sheet 59 of 105

OFFPAGE



OFFPAGE_GAP



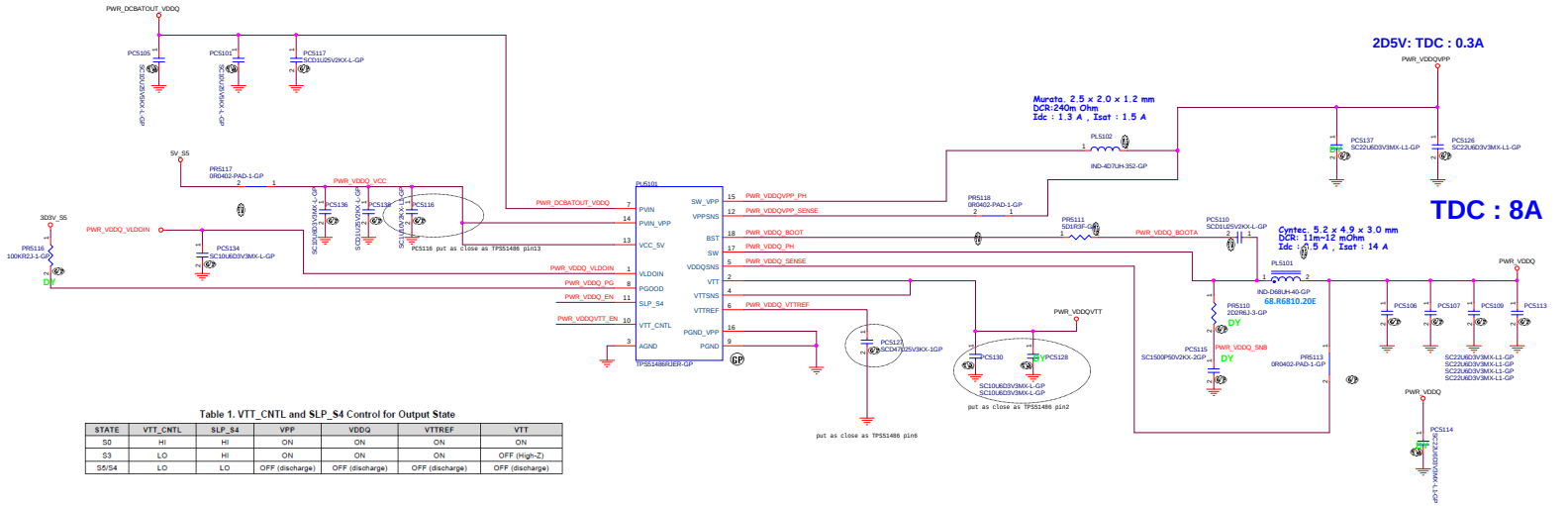


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

LAR-2

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Title: TPS51486_VDDQ/VTT/VPP		
Size: Custom	Document Number: ARES-2	Rev: 1
Date: Thursday, August 06, 2020	Sheet 51 of 106	

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LAR-2

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Title **POWER (RSVD)**

Size	Document Number	Rev
A	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 52 of 106

OFFPAGE

PH on EE Side

PR5302

40,50 1D8V_S5_PWRGD — 1 2 PWR_1D8V_PG — 0R0402-PAD-1-GP

40 PWR_1D8V_EN — PWR_1D8V_EN

OFFPAGE_GAP

3D3V_S5 — PG5301 GAP-CLOSE-PWR-3-GP — PWR_1D8V_VIN

PG5302 GAP-CLOSE-PWR-3-GP

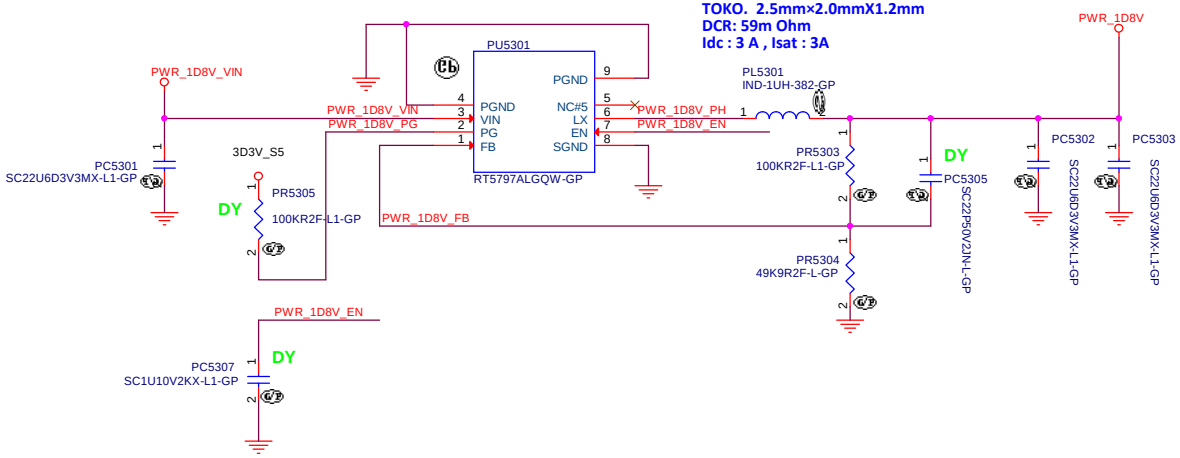
1D8V_SUS — PG5303 GAP-CLOSE-PWR-3-GP — PWR_1D8V

PG5304 GAP-CLOSE-PWR-3-GP

PG5305 GAP-CLOSE-PWR-3-GP

TDC=2A
Imax= 3A

TOKO. 2.5mm×2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 3A



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Title	RT5797_1D8V	
Size A3	Document Number ARES-2	Rev 1
Date: Thursday, August 06, 2020	Sheet 53 of 106	

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LAR-2

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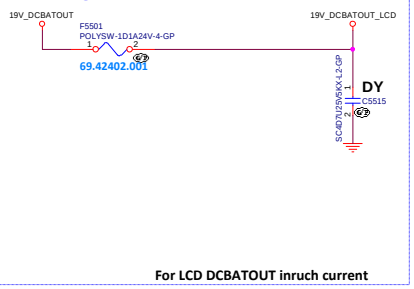
Title ***POWER (RSVD)***

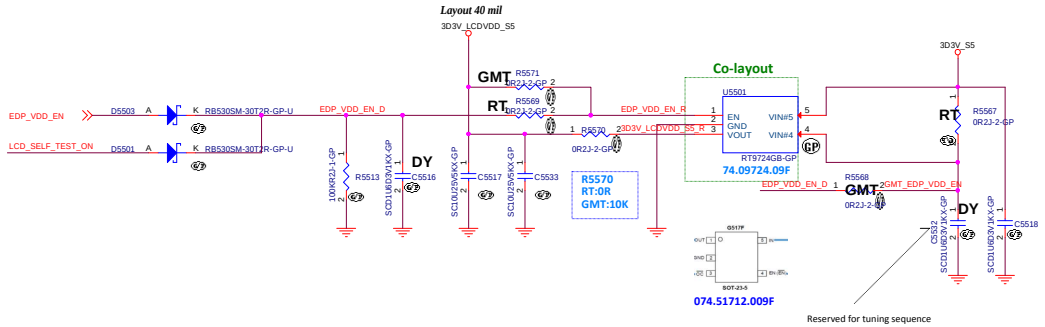
Size	Document Number	Rev
A4	**ARES-2**	1

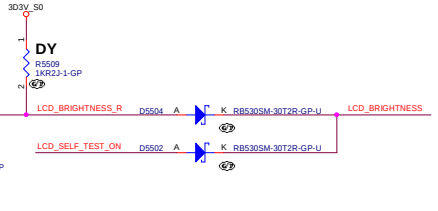
Date: Thursday, August 06, 2020 Sheet 54 of 106

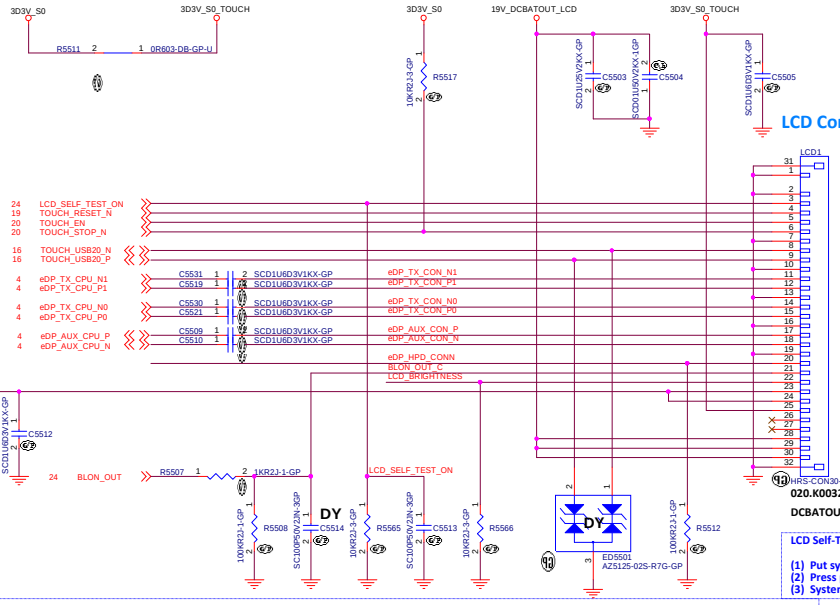
Main Func = LCD

LCD Backlight Power

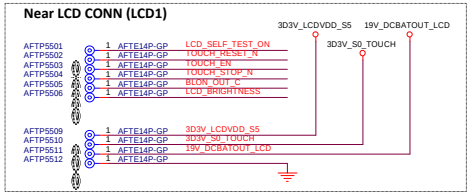


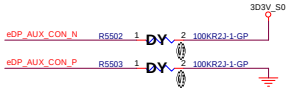






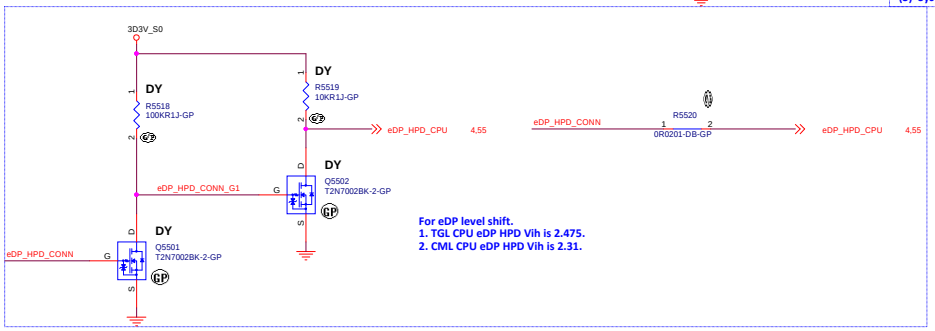
DCBATOUT: Need 1~3 empty-pin from DCBATOUT to the signals or other power net. (Apply to TNB, LNB)





LCD Self-Test is working under S5: (The function should work even CPU doesn't work)

(1) Put system in S5 state
(2) Press power button with Fn + Left-Ctrl
(3) System enter LCD self-test mode



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Title: DISPLAY (LCD/CAM/TOUCH)

Size: A2 | Document Number: ARES-2 | Rev: 1

Date: Thursday, August 06, 2020 | Sheet 55 of 106

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Title ***DISPLAY (CRT/IR Camera)***

Size	Document Number	Rev
A3	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 56 of 106

Main Func HDMI

RF Reserved

NEAR Pin24 NEAR Pin1 NEAR Pin15,18 NEAR Pin43,46 NEAR Pin6,11 NEAR Pin30

074.02553.007P

HDMI Re timer

VDD12's ripple must be lower than 30mVp-p at 20MHz

PS8409AQFN48GTR2-A2-GP

071.08409.0B03

HDMI CONN

SKT-HDMI23-214-GP

022.10025.0431

Co-lay

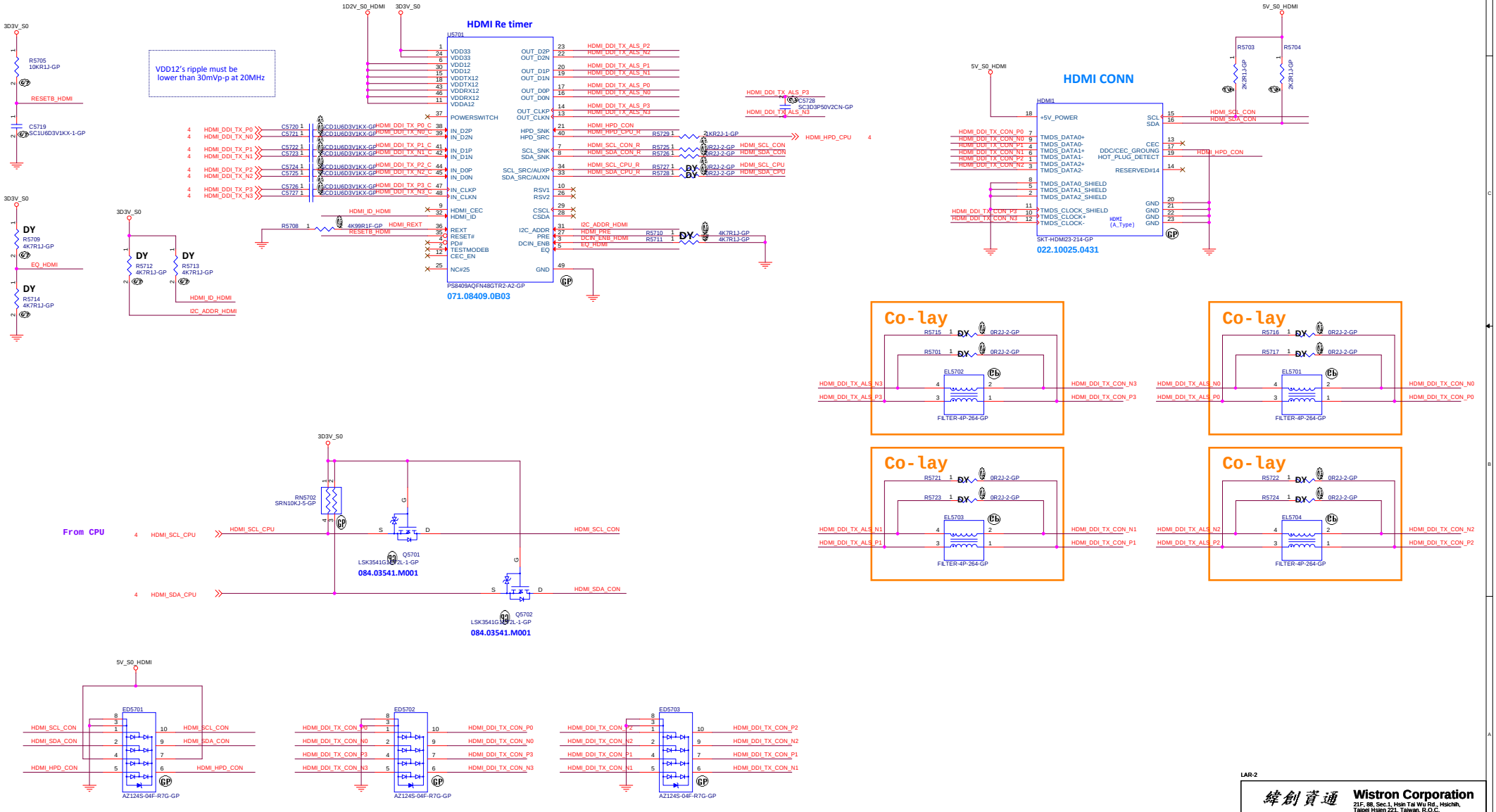
FILTER-4P-264-GP

From CPU

LSK3541GS2L-1-GP

084.03541.M001

AZ1245-04F-R7G-GP



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Title	DISPLAY (HDMI CONN)
Size	A2
Document Number	ARES-2
Rev	1
Date	Thursday, August 06, 2020
Sheet	57 of 106

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LAR-2

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Title ***DISPLAY***

Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 58 of 106

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LAR-2

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Title ***DISPLAY***

Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 59 of 106

BLANK

LAR-2

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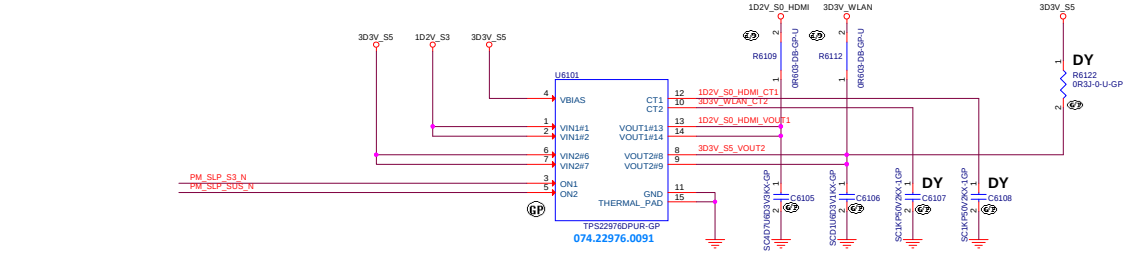
Title: INT IO (RSVD)

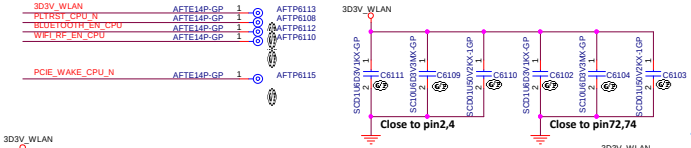
Size: A4 | Document Number: ARES-2 | Rev: 1

Date: Thursday, August 06, 2020 | Sheet 60 of 106

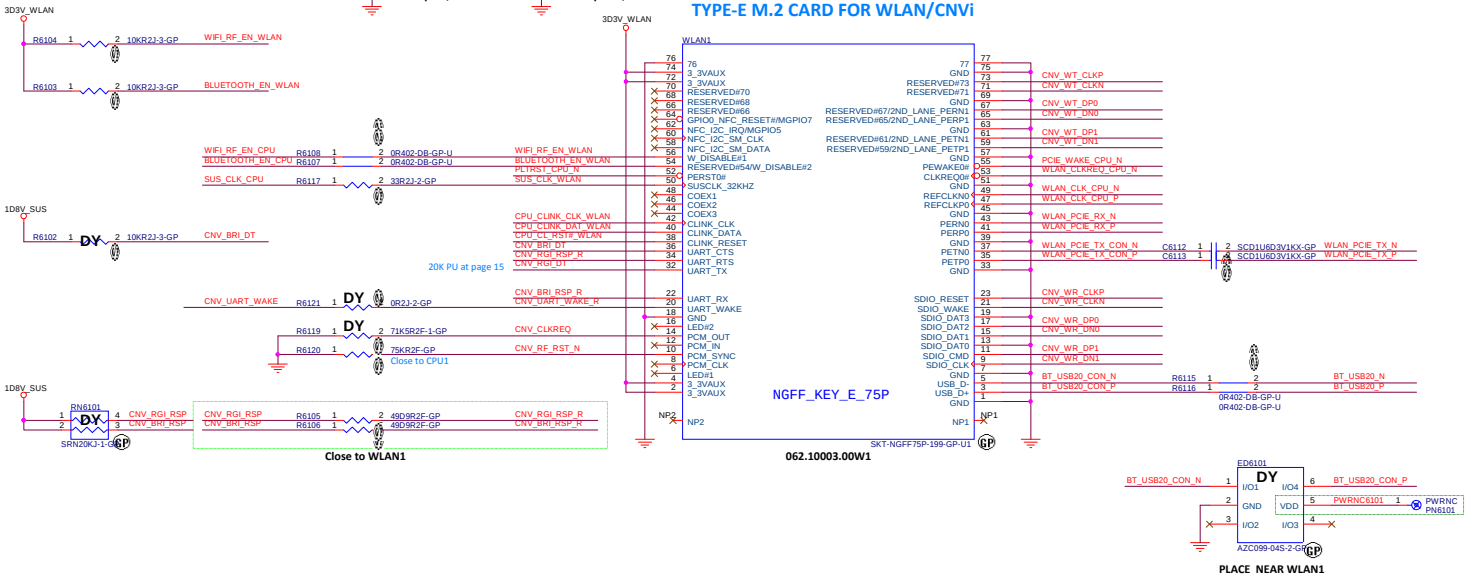
Main Func = WLAN

1D2V_S0_HDMI 3D3V_WLAN





TYPE-E M.2 CARD FOR WLAN/CNVi



17,24,40,99 PM_SLP_S3_N
17,24,40 PM_SLP_SUS_N
17,33 PCIE_WAKE_CPU_N
21 WIFI_RF_EN_CPU
3 BLUETOOTH_EN_CPU
17,24,31,33,40,63,71,89,91 PLTRST_CPU_N
18 SUS_CLK_CPU
3 CNV_UART_WAKE
18 CPU_CLINK_CLK_WLAN
18 CPU_CLINK_DAT_WLAN
18 CPU_CL_RST#_WLAN
21 CNV_BRI_DT
21 CNV_RGI_RSP
15,21 CNV_RGI_DT
21 CNV_BRI_RSP
19 CNV_CLKREQ
19 CNV_RF_RST_N
21 CNV_WT_CLKP
21 CNV_WT_CLKN
21 CNV_WT_DP0
21 CNV_WT_DN0
21 CNV_WT_DP1
21 CNV_WT_DN1
21 CNV_WR_CLKP
21 CNV_WR_CLKN
21 CNV_WR_DP0
21 CNV_WR_DN0
21 CNV_WR_DP1
21 CNV_WR_DN1
18 WLAN_CLKREQ_CPU_N
18 WLAN_CLK_CPU_P
18 WLAN_CLK_CPU_N
16 WLAN_PCIE_RX_P
16 WLAN_PCIE_RX_N
16 WLAN_PCIE_TX_P
16 WLAN_PCIE_TX_N
16 BT_USB20_N
16 BT_USB20_P

LAR-2

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Title: **INT IO (WLAN M.2/CNVi)**

Size: A2 | Document Number: **ARES-2** | Rev: 1

Date: Thursday, August 06, 2020 | Sheet 61 of 106

WWAN

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LAR-2

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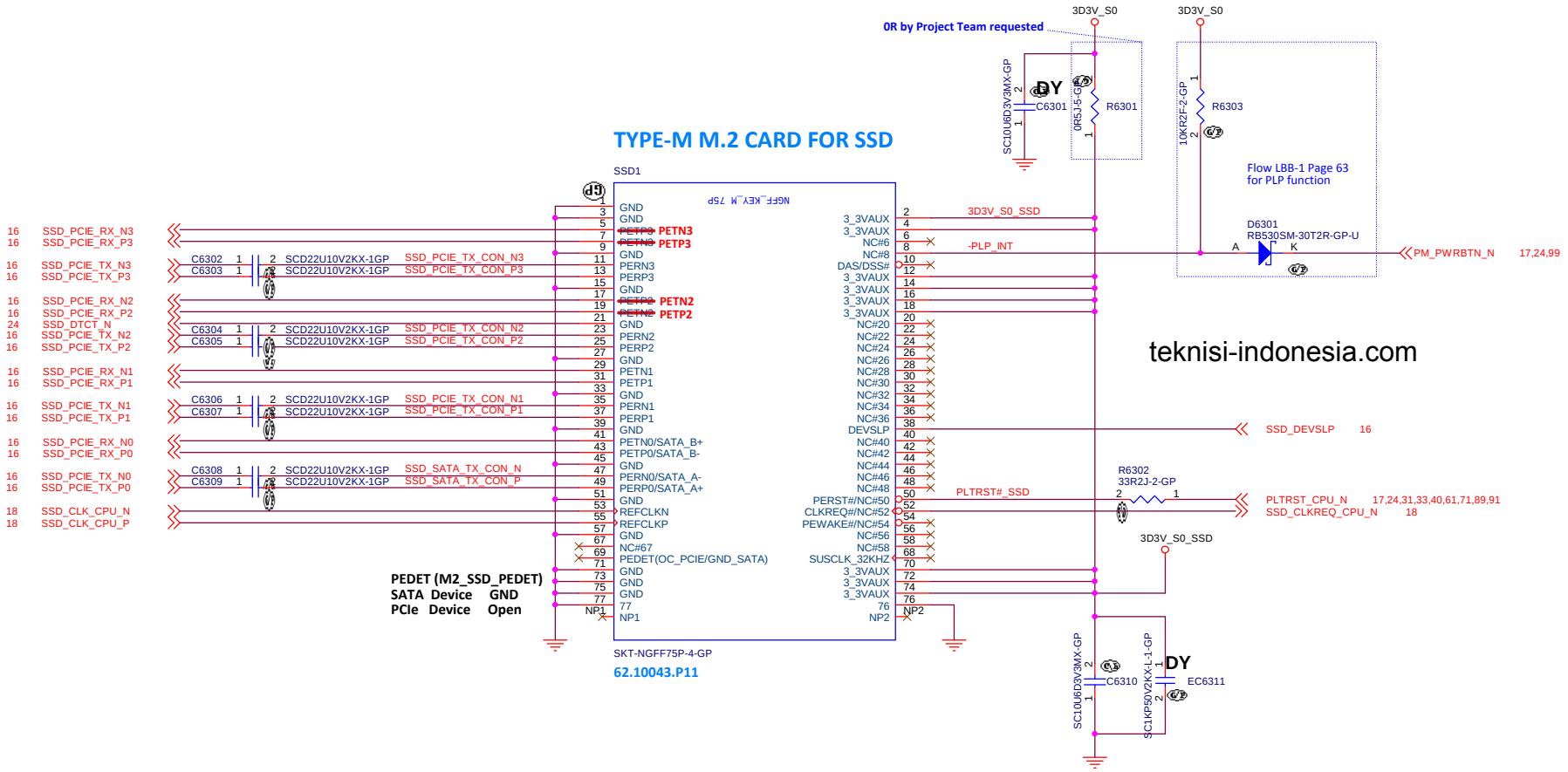
Title ***INT IO (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 62 of 106



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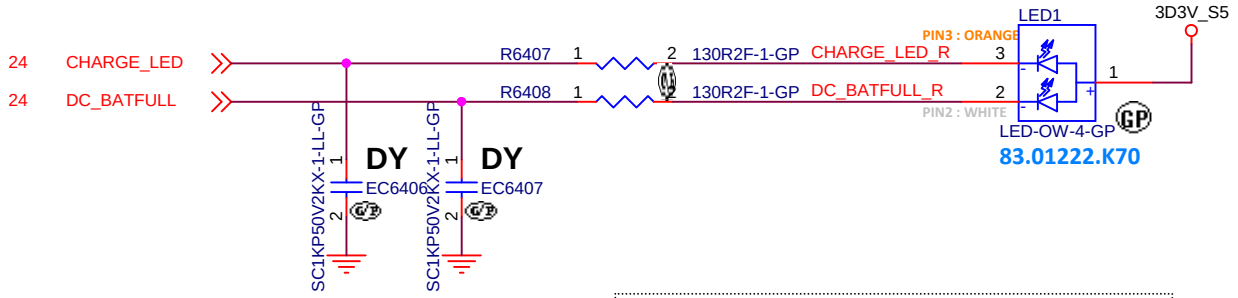
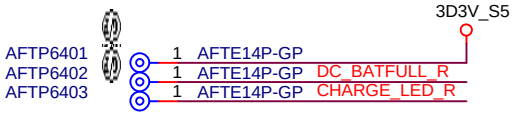
Title: INT IO (SSD M.2)		
Size: A3	Document Number: ARES-2	Rev: 1
Date: Thursday, August 06, 2020	Sheet 63 of 106	

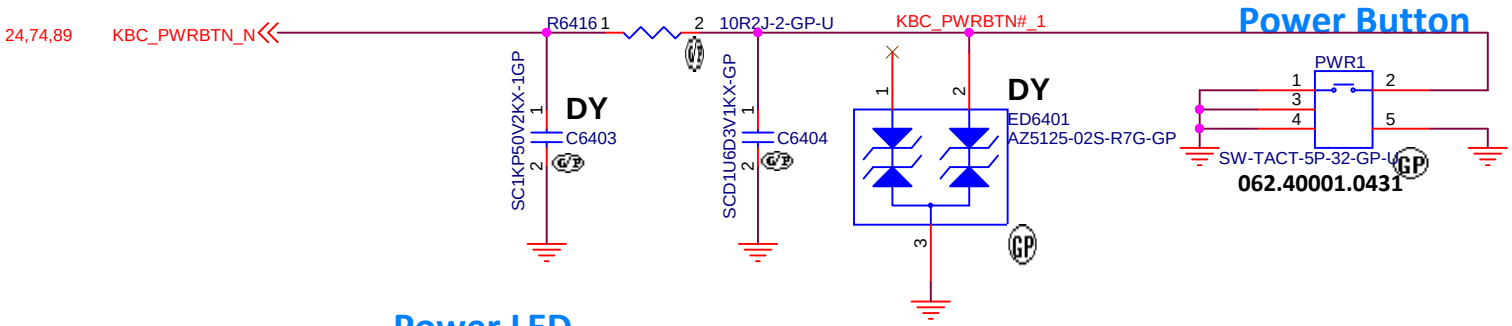
Dual LED



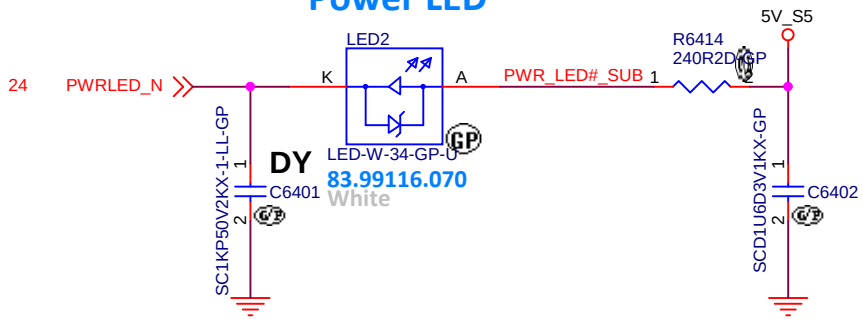
Near LED1



Power Button



Power LED



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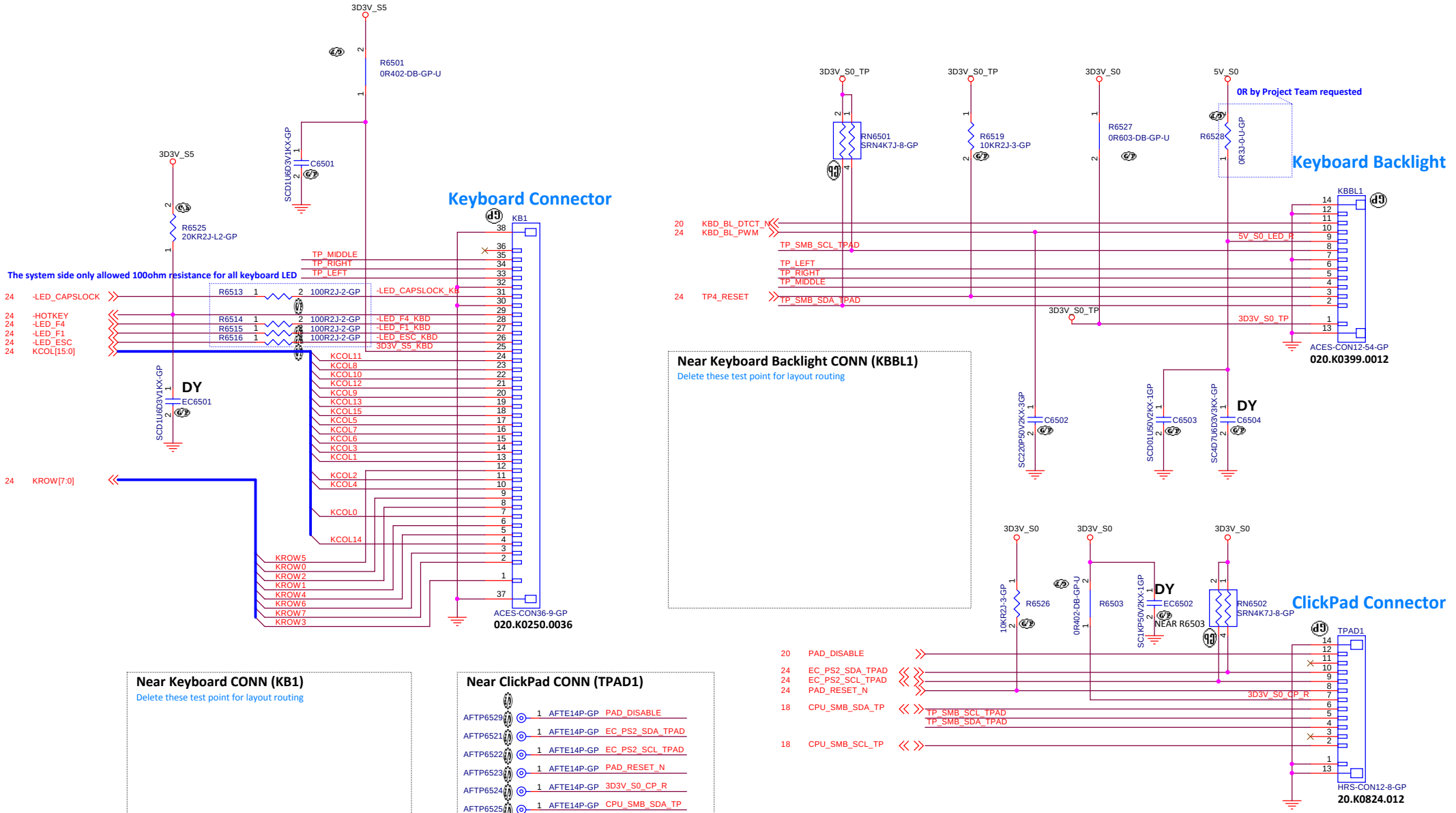
Title: *LED/BTN/POWER BTN*		
Size: A4	Document Number: **ARES-2**	Rev: **1**
Date: Thursday, August 06, 2020	Sheet 64 of 106	



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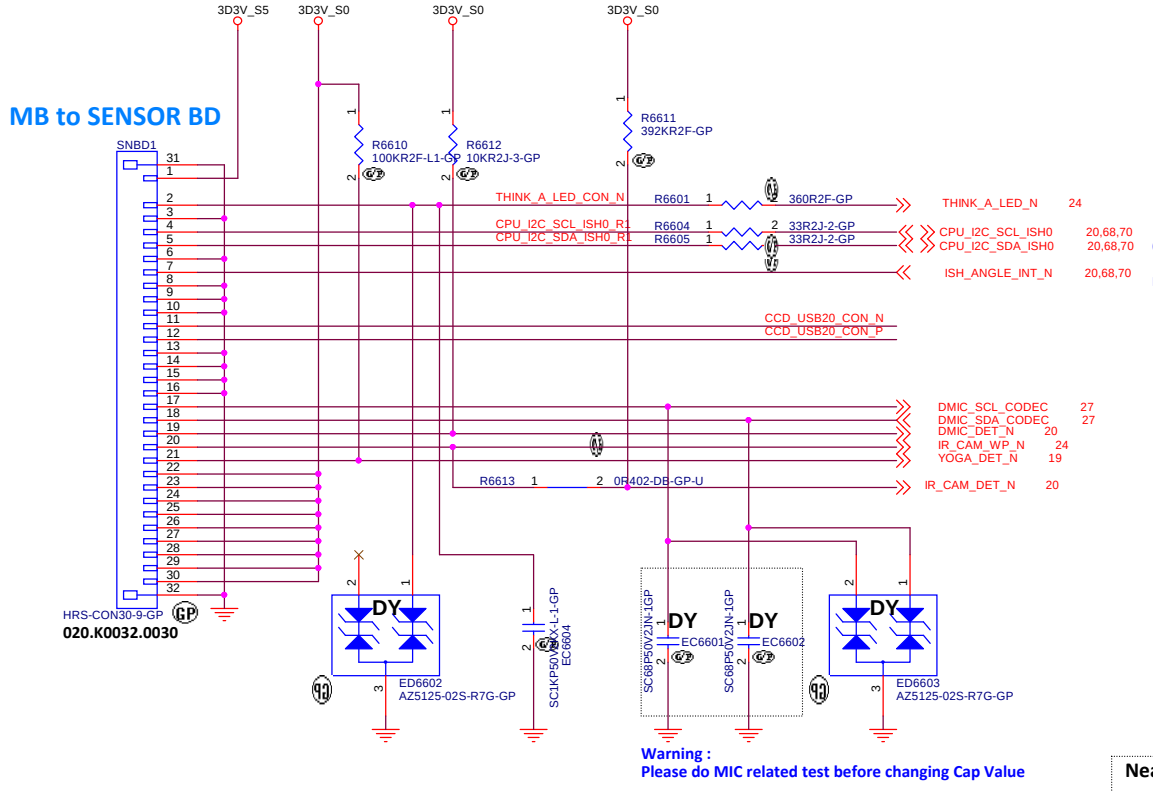
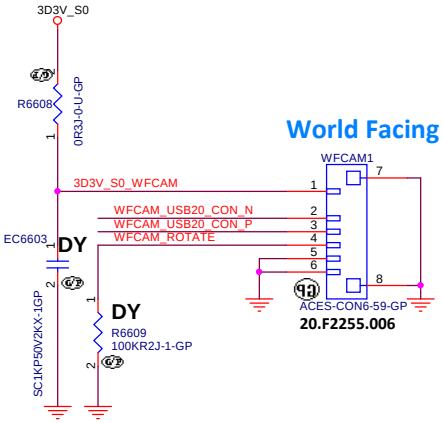
Title: *INT IO (KB/CP/TP)*		
Size: A3	Document Number: **ARES-2**	Rev: **1**
Date: Thursday, August 06, 2020	Sheet 65 of 106	



Camera

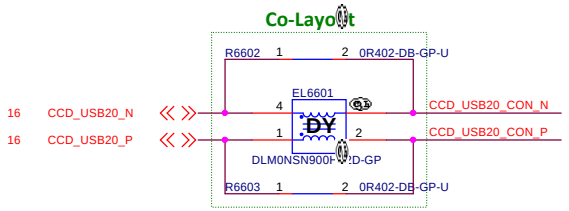
INT for ANGLE

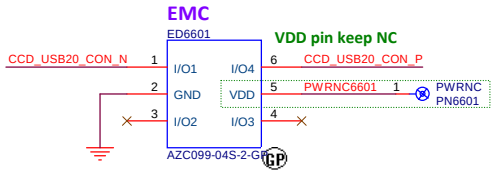


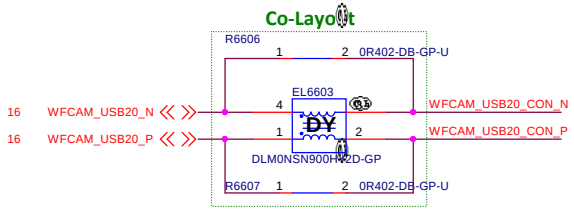
Default camera direction is, LED on the right side of Lens/CMOS.

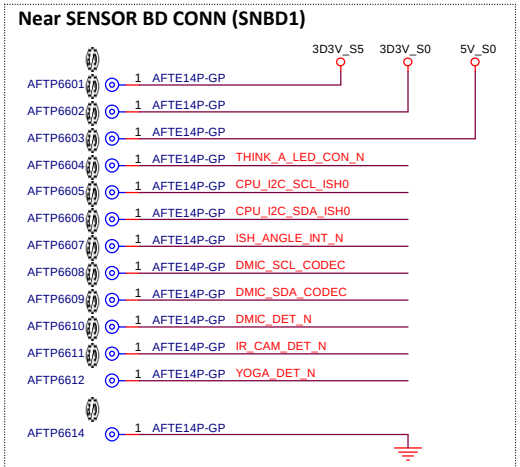
Pin4 supply = High : Normal image (default, and if this pin not be connected = normal image)
Pin4 supply = Low : Upside down image (means if we can rotate camera module 180 degree = LED on left side, use this mode)

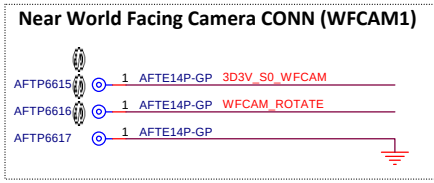
Warning :
Please do MIC related test before changing Cap Value











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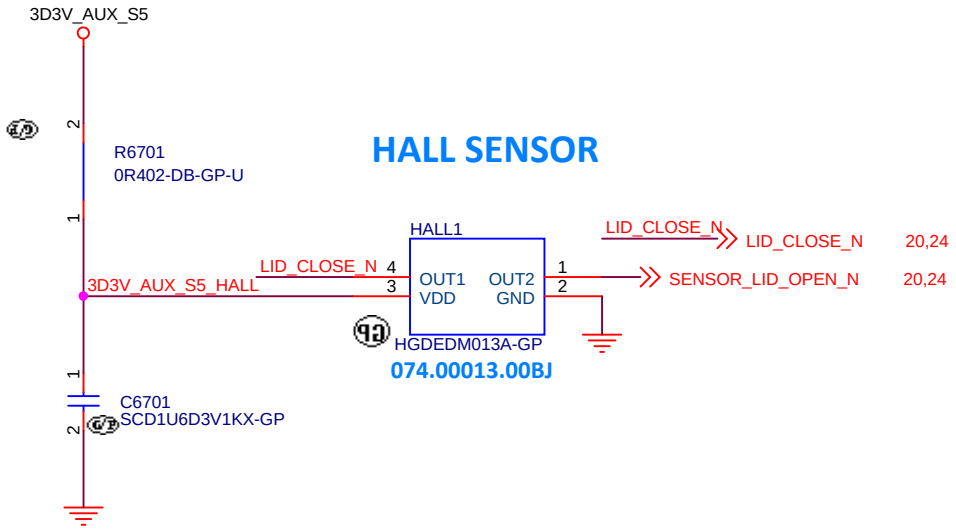
Title: ***IO BOARD CONN (SNBD/WFCAM)***

Size	Document Number	Rev
A3	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 66 of 106



20,24

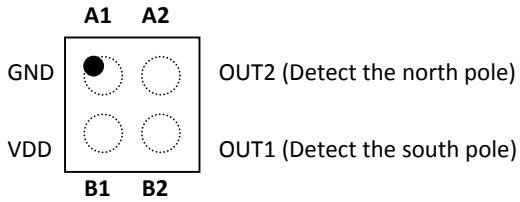
20,24

Pin1 need place at "Upper Right Corner"

LID_CLOSE_N : NB Lid function
SENSOR_LID_OPEN#: Tablet detect function

Pin Configuration

TOP VIEW (pads not visible)



BU52072GWZ-E2

LAR-2

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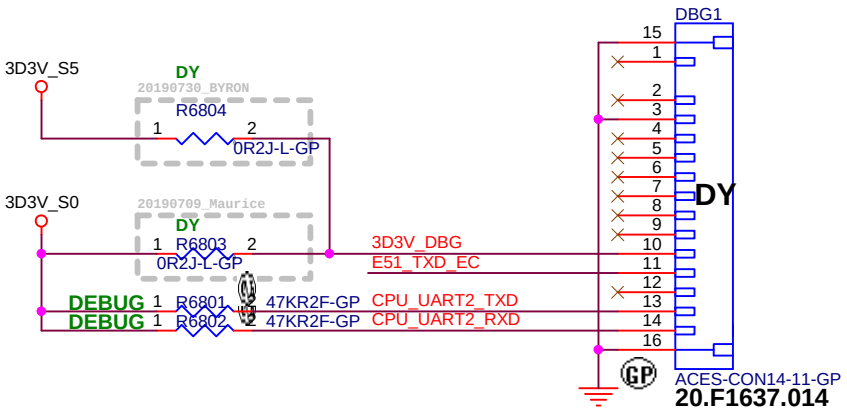
Title ***SENSOR (HALL-SENSOR)***

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 67 of 106

Main Func = Debug

eSPI Debug Port



24 E51_TXD_EC

20 CPU_UART2_TXD
20 CPU_UART2_RXD

Sensors Debug Hooks

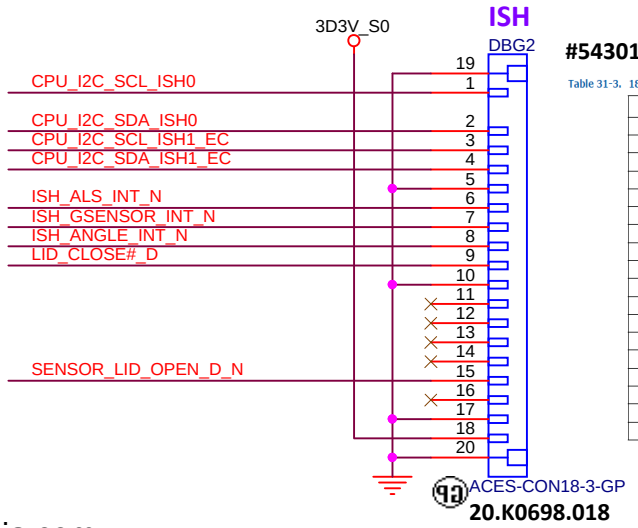


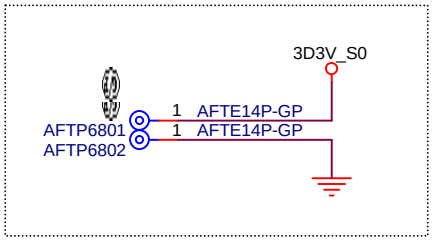
Table 31-3. 18-pin ZIF Connector Pinout

Pin	Pin function	Description
1	ISH_I2C0_SCL	Clock line for the I2C0
2	ISH_I2C0_SDA	Data line for the I2C0
3	ISH_I2C1_SCL	Clock line for the I2C1
4	ISH_I2C1_SDA	Data line for the I2C1
5	GND	System Ground
6	GPIOa (1)	Connect here one of the GPIOs in use
7	GPIOb (1)	Connect here one of the GPIOs in use
8	GPIOc (1)	Connect here one of the GPIOs in use
9	GPIOd (1)	Connect here one of the GPIOs in use
10	GND	System Ground
11	Reserved by Intel	Do not use
12	Reserved by Intel	Do not use
13	Reserved by Intel	Do not use
14	Reserved by Intel	Do not use
15	Reserved by Intel	Do not use
16	Reserved by Intel	Do not use
17	GND	System Ground
18	Vio	Sensors Reference Voltage

20,66,70 CPU_I2C_SCL_ISH0
20,66,70 CPU_I2C_SDA_ISH0
20,24 CPU_I2C_SCL_ISH1_EC
20,24 CPU_I2C_SDA_ISH1_EC

20 ISH_ALS_INT_N
20 ISH_GSENSOR_INT_N
20,66,70 ISH_ANGLE_INT_N
20 LID_CLOSE#_D

20 SENSOR_LID_OPEN_D_N



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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DEBUG (eSPI DEBUG)***

Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 68 of 106

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LAR-2

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Title ***SENSOR (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 69 of 106

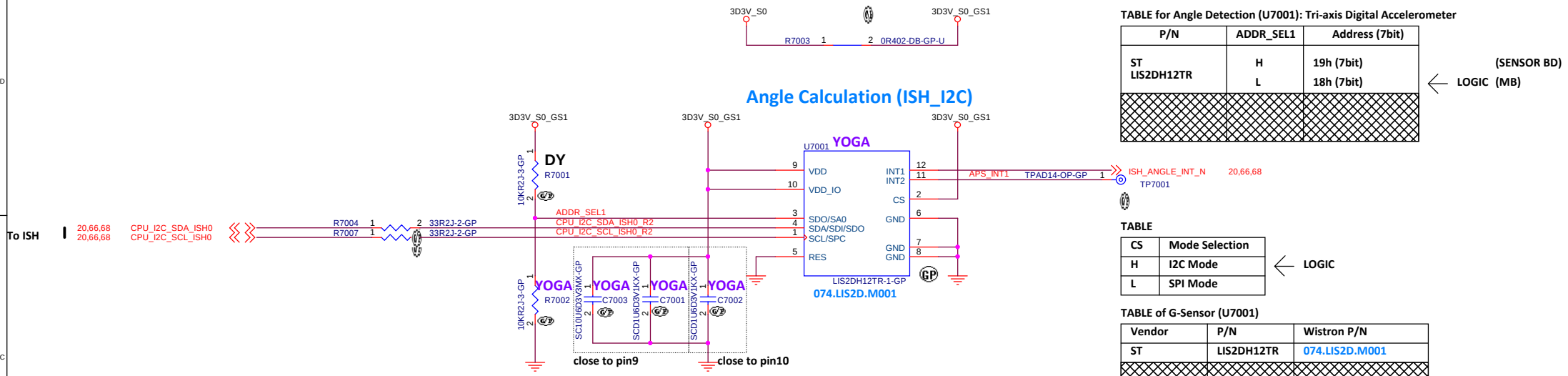

TABLE for Angle Detection (U7001): Tri-axis Digital Accelerometer

P/N	ADDR_SEL1	Address (7bit)
ST LIS2DH12TR	H	19h (7bit)
	L	18h (7bit)

(SENSOR BD)
LOGIC (MB)

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

LOGIC

TABLE of G-Sensor (U7001)

Vendor	P/N	Wistron P/N
ST	LIS2DH12TR	074.LIS2D.M001

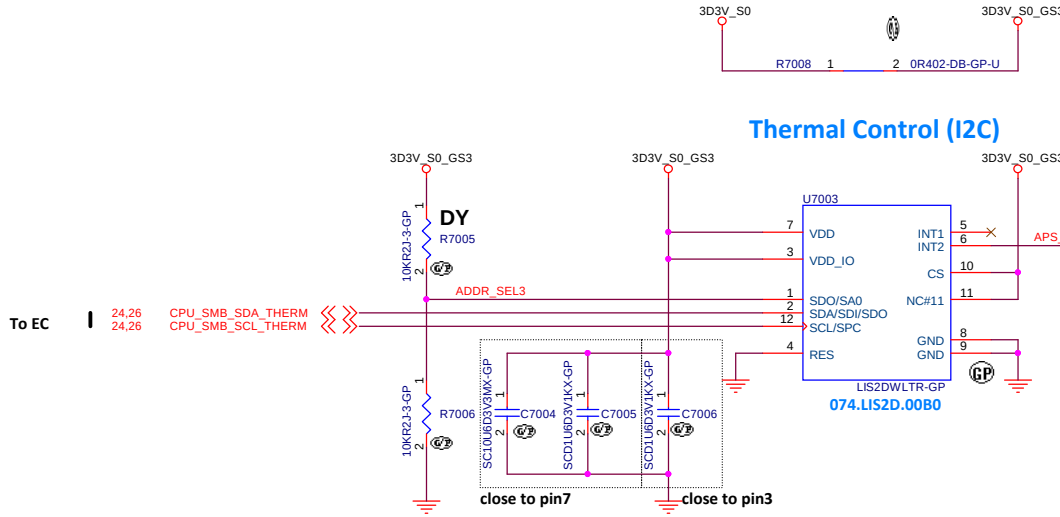

TABLE for ITS Detection (U7003): Tri-axis Digital Accelerometer

P/N	ADDR_SEL3	Address (8bit)
ST LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)

LOGIC

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

LOGIC

TABLE of G-Sensor (U7003)

Vendor	P/N	Wistron P/N
ST	LIS2DWLR	074.LIS2D.00B0
BOSCH	BMA280	074.00280.0AB0

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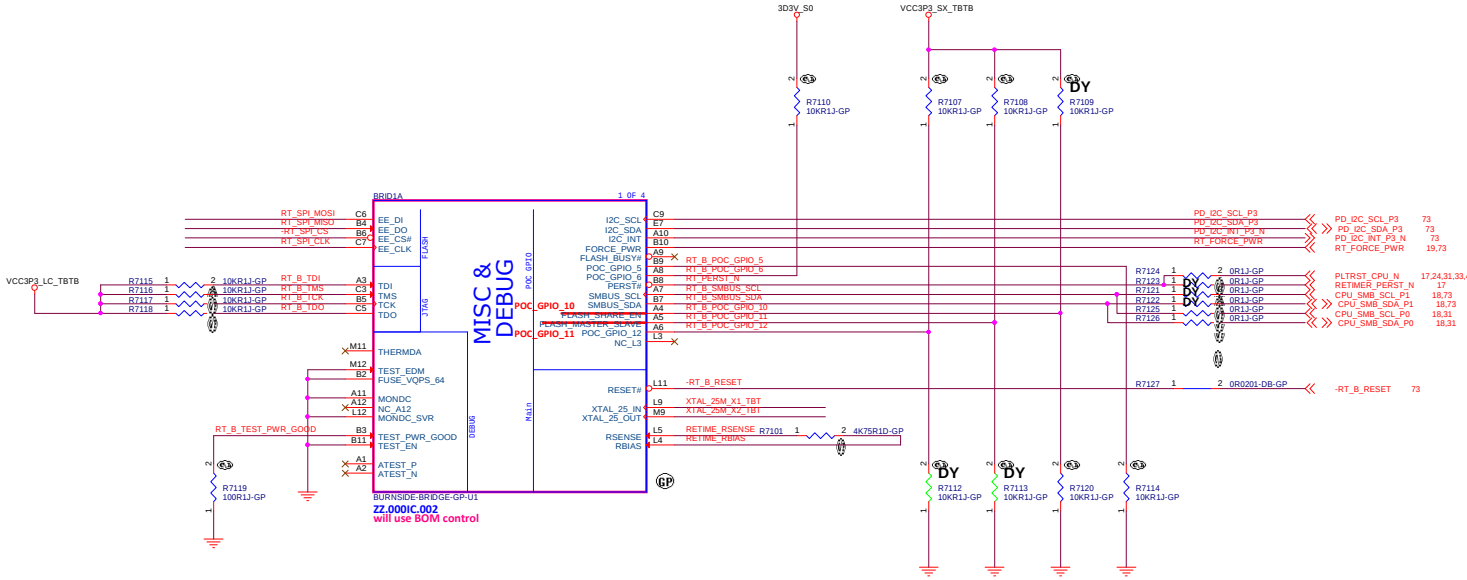
Title: SENSOR (G-SENSOR)

Size: A3 | Document Number: ARES-2 | Rev: 1

Date: Thursday, August 06, 2020 | Sheet 70 of 106



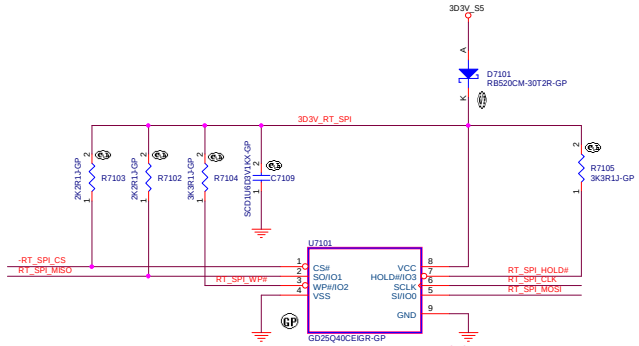
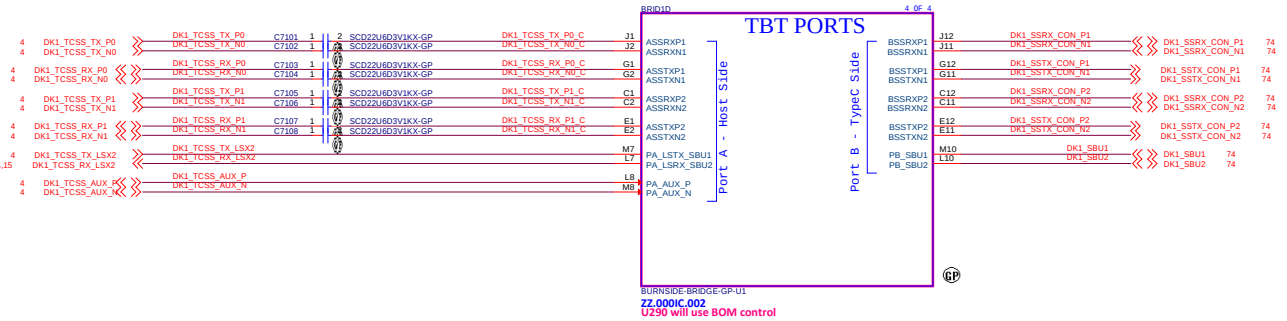


TABLE U7101
1MB (8Mb) 2X3MM USON8

Vender	Vender P/N	Wistron P/N
WINBOND	W25Q80DVUXIE	072.25Q80.0003
GIGADEVICE	GD25Q80CEIG	
Adesto	AT25SF081-MAHD-T	



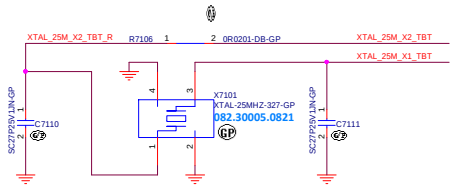


TABLE of X7101 : (25MHz 18pF 30ppm 2016)

Vender	Vender P/N	Wistron P/N
TXC	7R25080003	082.30005.0821
EPSON	Q22FA1280056000	082.30005.0801
KDS	1ZZHAE25000CC0F	082.30005.M008

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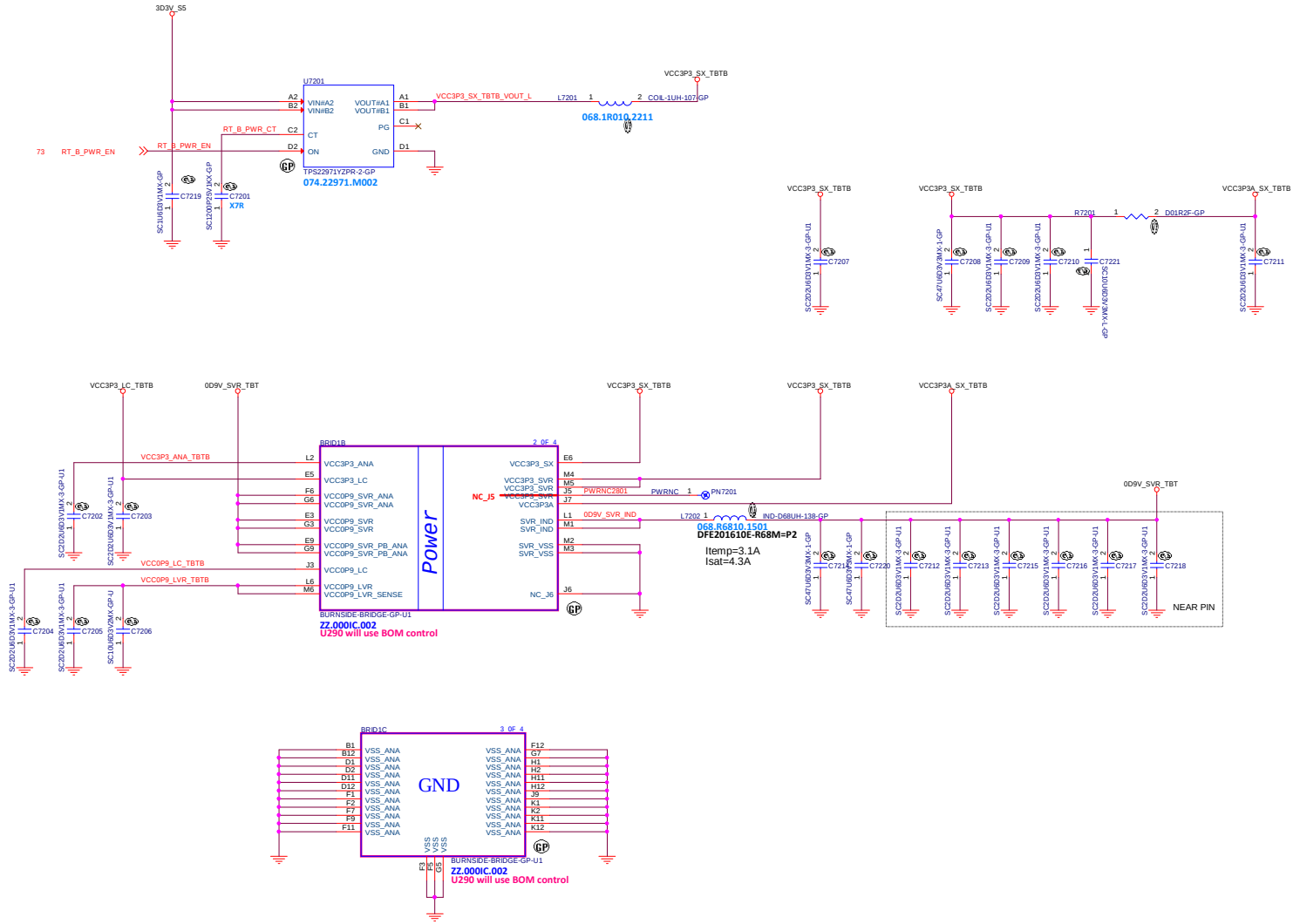
Title: THUNDERBOLT RE TIMER(1/2)

Size: A2 | Document Number: ARES-2 | Rev: 1

Date: Thursday, August 06, 2020 | Sheet 71 of 106



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Title: ***THUNDERBOLT RE TIMER(2/2)***

Size	Document Number	Rev
A2	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 72 of 106

A_0, A_1 and A_2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 3). The next 3 bits, A_2, A_1 and A_0, select one of 8 possible Slave devices. The last bit, R/W, specifies whether a Read (1) or Write (0) operation is to be performed.

1	0	1	0	A_2	A_1	A_0	R/W

DEVICE ADDRESS

Figure 3. Slave Address Bits

TABLE I2C Addressing

I2C1	Master: EC	TBTB PORT	0x24
	Slave: PD	TBTC PORT	0x20
I2C2	Master: PMC	TBTB PORT	T.B.D
	Slave: PD	TBTC PORT	T.B.D
I2C3	Master: PD	TBTB PORT	T.B.D.
	Slave: RT	TBTC PORT	T.B.D.

TABLE I2C Address

I2C SPI	Write	0xA0
	Read	0xA1

CHIP RES 3.3K J 1/20W 0201

add 0ohm between CPU_SMB_INT#_PD and PD pin34, in case PD FW has issue to trigger un-expected INT# which cause no boot(no SLP_S4#)

FROM EC

FROM CPU

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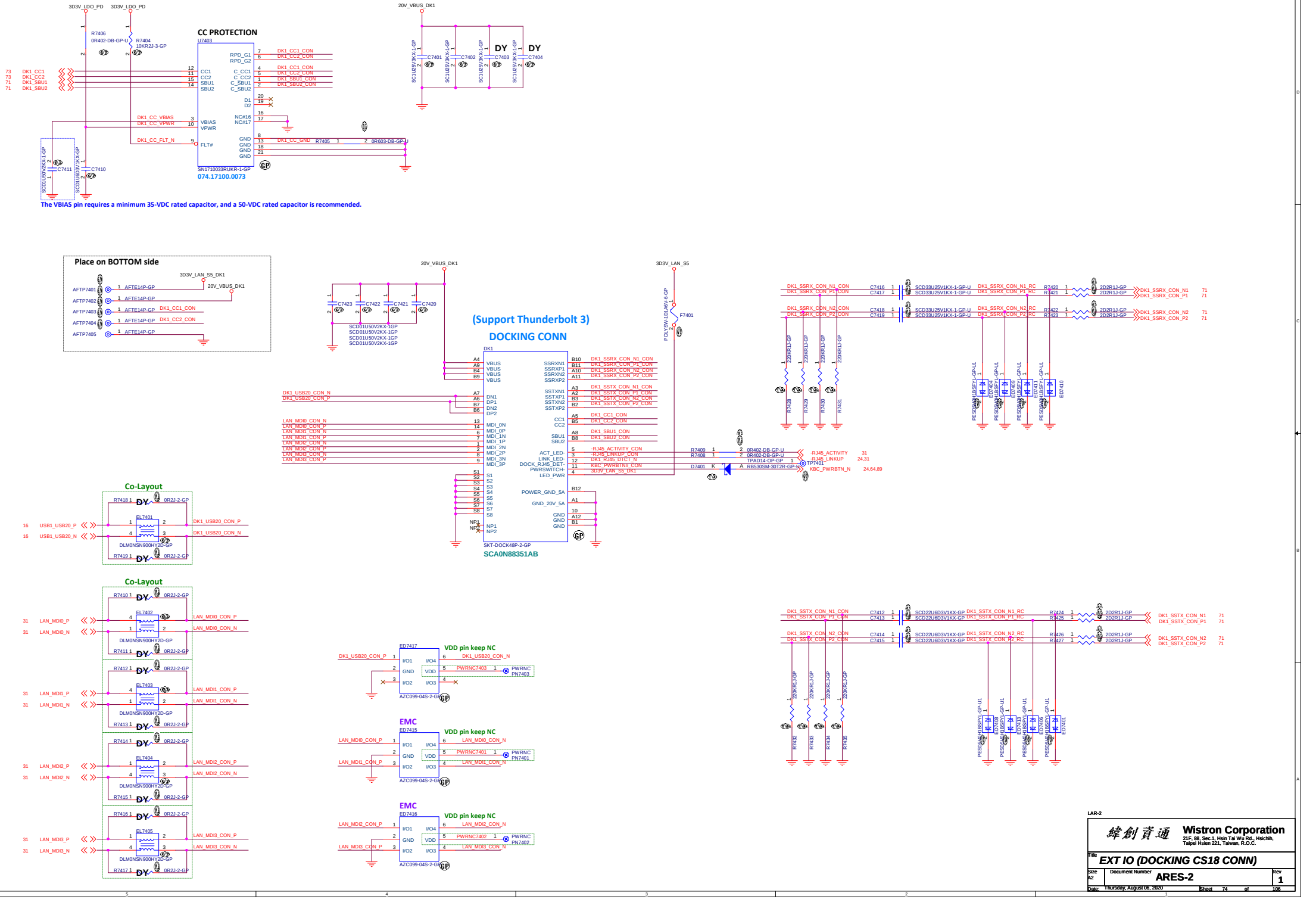
Title: EXT IO (TYPEC PD TPS65994)

Size	Document Number	Rev
A2	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 73 of 106


CC PROTECTION
U7403
SN1710033RUKR-1-GP
074.17100.0073
The VBIAS pin requires a minimum 35-VDC rated capacitor, and a 50-VDC rated capacitor is recommended.
Place on BOTTOM side
(Support Thunderbolt 3)
DOCKING CONN
DK1
SKT-DOCK48P-2-GP
SCA0N88351AB
Co-Layout
Co-Layout
VDD pin keep NC
EMC
VDD pin keep NC
EMC
VDD pin keep NC
Wistron Corporation
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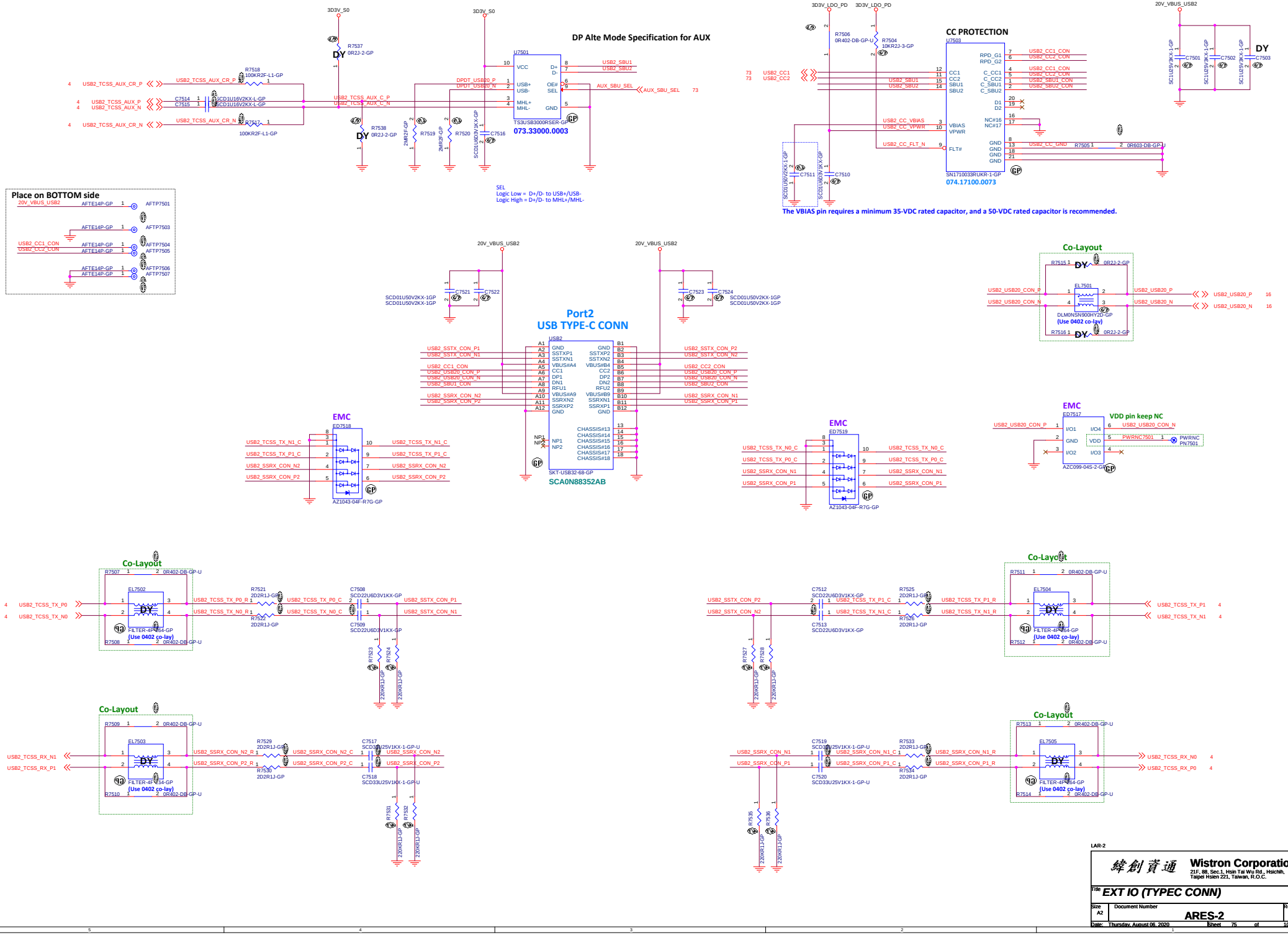
EXT IO (DOCKING CS18 CONN)
ARES-2
Thursday, August 06, 2020


DP Alte Mode Specification for AUX
073.33000.0003
SEL
Logic Low = D+/D- to USB+/USB-
Logic High = D+/D- to MHL+/MHL-
CC PROTECTION
074.17100.0073
The VBIAS pin requires a minimum 35-VDC rated capacitor, and a 50-VDC rated capacitor is recommended.
Place on BOTTOM side
Port2
USB TYPE-C CONN
SCA0N88352AB
EMC
Co-Layout
VDD pin keep NC
(Use 0402 co-lay)
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Wistron Corporation
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EXT IO (TYPEC CONN)
ARES-2
Rev 1
Thursday, August 06, 2020
Sheet 75 of 106

BLANK

LAR-2

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Title: ***GPU (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 76 of 106

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LAR-2

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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 77 of 106

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LAR-2

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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 78 of 106

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LAR-2

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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 79 of 106

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LAR-2

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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 80 of 106

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LAR-2

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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 81 of 106

BLANK

LAR-2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU (RSVD)***
Size A4	Document Number **ARES-2**
Rev **1**	
Date: Thursday, August 06, 2020	Sheet 82 of 106

BLANK

LAR-2

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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 83 of 106

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LAR-2

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Title **GPU (RSVD)**

Size	Document Number	Rev
A4	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 84 of 106

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LAR-2

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Title: ***GPU (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	1

Date: Thursday, August 06, 2020 Sheet 85 of 106

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LAR-2

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Title: ***GPU (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	1

Date: Thursday, August 06, 2020 Sheet 86 of 106

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LAR-2

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Title: ***GPU (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	1

Date: Thursday, August 06, 2020 Sheet 87 of 106

BLANK

LAR-2

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Title: ***GPU (RSVD)***		
Size: A4	Document Number: **ARES-2**	Rev: **1**
Date: Thursday, August 06, 2020	Sheet 88 of 106	

EMI Spring

SPR1
SPRING-64-GP
34.4H602.001

Stand Off

HS1
STFT236B142R128H43-1-GP
34.4EO02.001

HS2
STFT236B142R128H43-1-GP
34.4EO02.001

Screw Pad

H1 HOLE233R150-GP **ZZ.00PAD.WN1**
H2 HOLE233R150-GP **ZZ.00PAD.WN1**
H3 HOLE233R150-GP **ZZ.00PAD.WN1**
H4 HOLE233R150-GP **ZZ.00PAD.WN1**

H6 HOLE276R119-GP **ZZ.PAD02.071**
H7 HOLE276R119-GP **ZZ.PAD02.071**
H8 HOLE237R103-GP **ZZ.00PAD.EJ1**

H10 HOLE276R119-GP **ZZ.PAD02.071**
H11 HOLE276R119-GP **ZZ.PAD02.071**
H12 HOLE237R103-GP **ZZ.00PAD.EJ1**
H13 HOLE276R119-GP **ZZ.PAD02.071**
H14 HOLE237R103-GP **ZZ.00PAD.EJ1**

RF CAPs

Test Point

TP8901 TP8903 — TPAD60 — KBC_PWRBTN_N — 24,64,74,89 — **Place on top side**

TP8902 TP8904 — TPAD60 — KBC_PWRBTN_N — 24,64,74,89 — **Place on bottom side**

AFTP8918 AFTP8921 — AFTE14P-GP — PLTRST_CPU_N, KBC_PWRBTN_N — 17,24,31,33,40,61,63,71,91 / 24,64,74,89

Place on top side

5V_S5 5V_S0 3V3V_S5 3V3V_S0

AFTP8901 AFTP8902 AFTP8903 AFTP8904 AFTP8905 AFTP8907 AFTP8908 AFTP8909 — AFTE14P-GP

AFTP8910 AFTP8911 AFTP8912 — AFTE14P-GP

EMI CAPs

1D2V_S3: EC8901 EC8902 EC8903
1D8V_VCCIN_AUX: EC8904 EC8905
19V_DCBATOUT: EC8906 EC8907 EC8908 EC8909 EC8910
3D3V_S0: EC8911 EC8912 EC8913
5V_S5_USB4: EC8914
5V_S5: EC8915 EC8916 EC8917
3D3V_S0_SSD: EC8918
3D3V_LAN_S5_DK1: EC8919
5V_S5_USB3: EC8920
3D3V_S5: EC8921 EC8922 EC8923
1D05V_S5_OUT: EC8924 EC8925
3D3V_SUS: EC8926 EC8927
1D05V_VCCIO_OUT: EC8928 EC8929

LAR-2

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Title: ***UNUSED PARTS (ME/RF/EMI)***

Size: A2 | Document Number: **ARES-2** | Rev: **1**

Date: Thursday, August 06, 2020 | Sheet 89 of 106

BLANK

LAR-2

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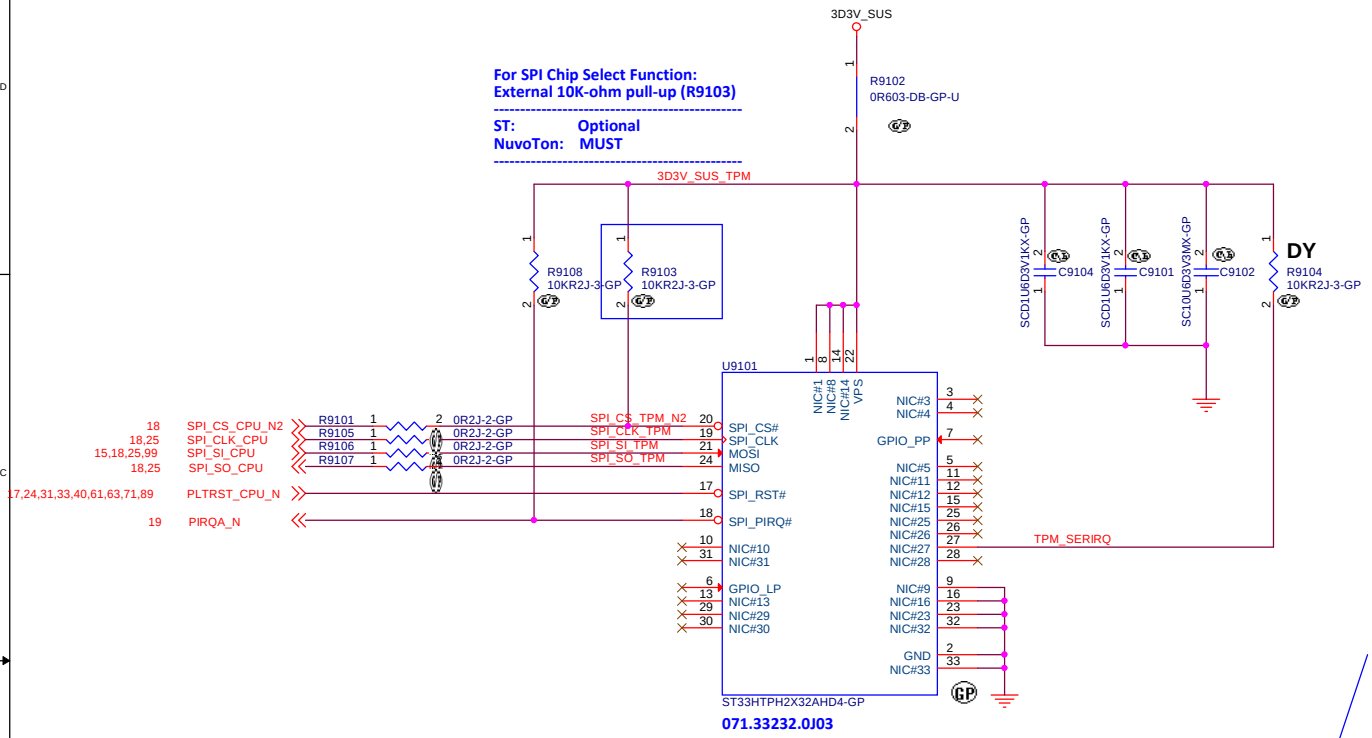
Title: ***INT IO (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	1

Date: Thursday, August 06, 2020 Sheet 90 of 106



SPI Chip Select Pin:
ST (SPI_CS#) Internal pull-up
NuvoTon (SCS#) Internal pull-up is disabled if the pin is part of the recognized host interface

TABLE

1st	ST33HTPH2X32AHD4	071.33232.0J03
2nd	NPCT750LADYX	071.00750.0H03

TABLE

Pin No	TCG PTP Spec(V38)	ST Micro ST33HTPH2X32AHD4	NuvoTon NPCT750LADYX	Infineon SLB9670VQ2.0 FW7.63
1	VDD	NC	VSB	VDD
2	GND	GND	NC	GND
3	NC	NC	NC	NC
4	GPIO	PP	GPIO/PP	NC
5	NC	NC	NC	NC
6	GPIO	NC	GPIO3	GPIO
7	GPIO	GPIO	NC	PP
8	VDD	NC	VHIO	VDD
9	NC	NC	NC	GND
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	NC	GPIO4	NC
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	NC	GND	NC
17	SPI_RST#	SPI_RST#	RST#	RST#
18	SPI_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	PIRQ#
19	SPI_CLK	SPI_CLK	SCLK	SCLK
20	SPI_CS#	SPI_CS#	SCS#/GPIO5	CS#
21	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VPS	VHIO	VDD
23	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	NC	SDA/GPIO0	NC
30	SDA/GPIO0	NC	SCL/GPIO1	NC
31	NC	NC	NC	NC
32	NC	NC	NC	GND

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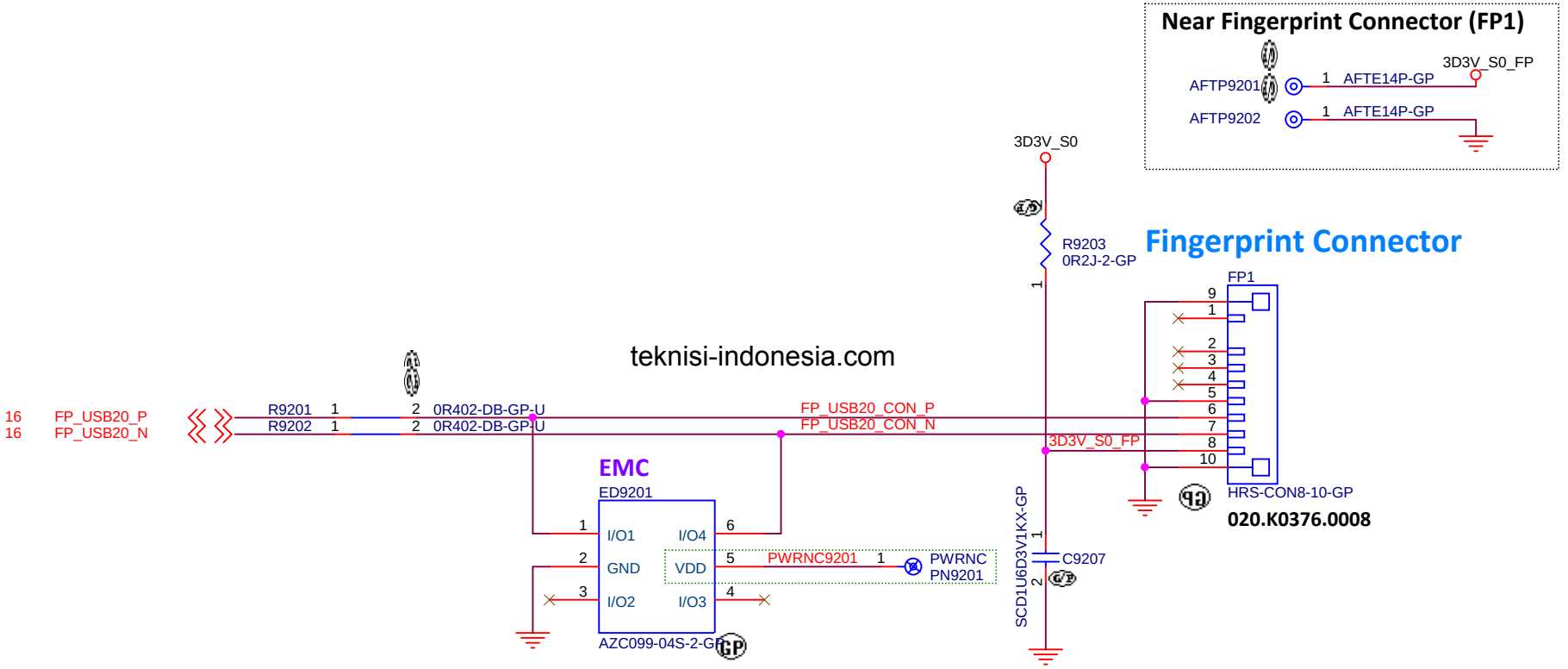
Title: INT IO (TPM 2.0)

Size	Document Number	Rev
A3	ARES-2	1

Date: Thursday, August 06, 2020 Sheet 91 of 106



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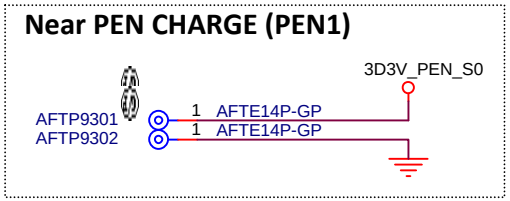
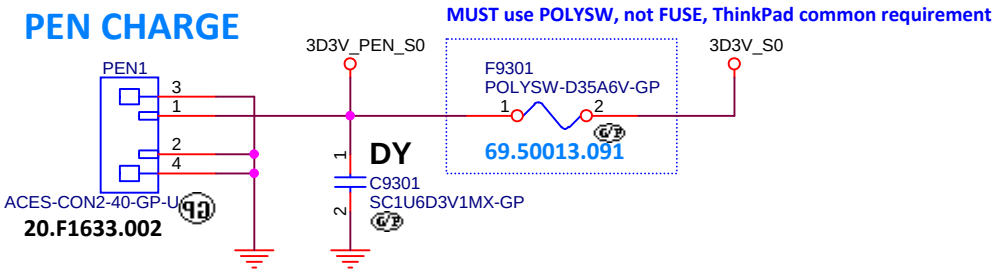
Title	***INT IO (FINGERPRINT)***	
Size A4	Document Number **ARES-2**	Rev **1**
Date: Thursday, August 06, 2020	Sheet 92 of 106	





LAR-2

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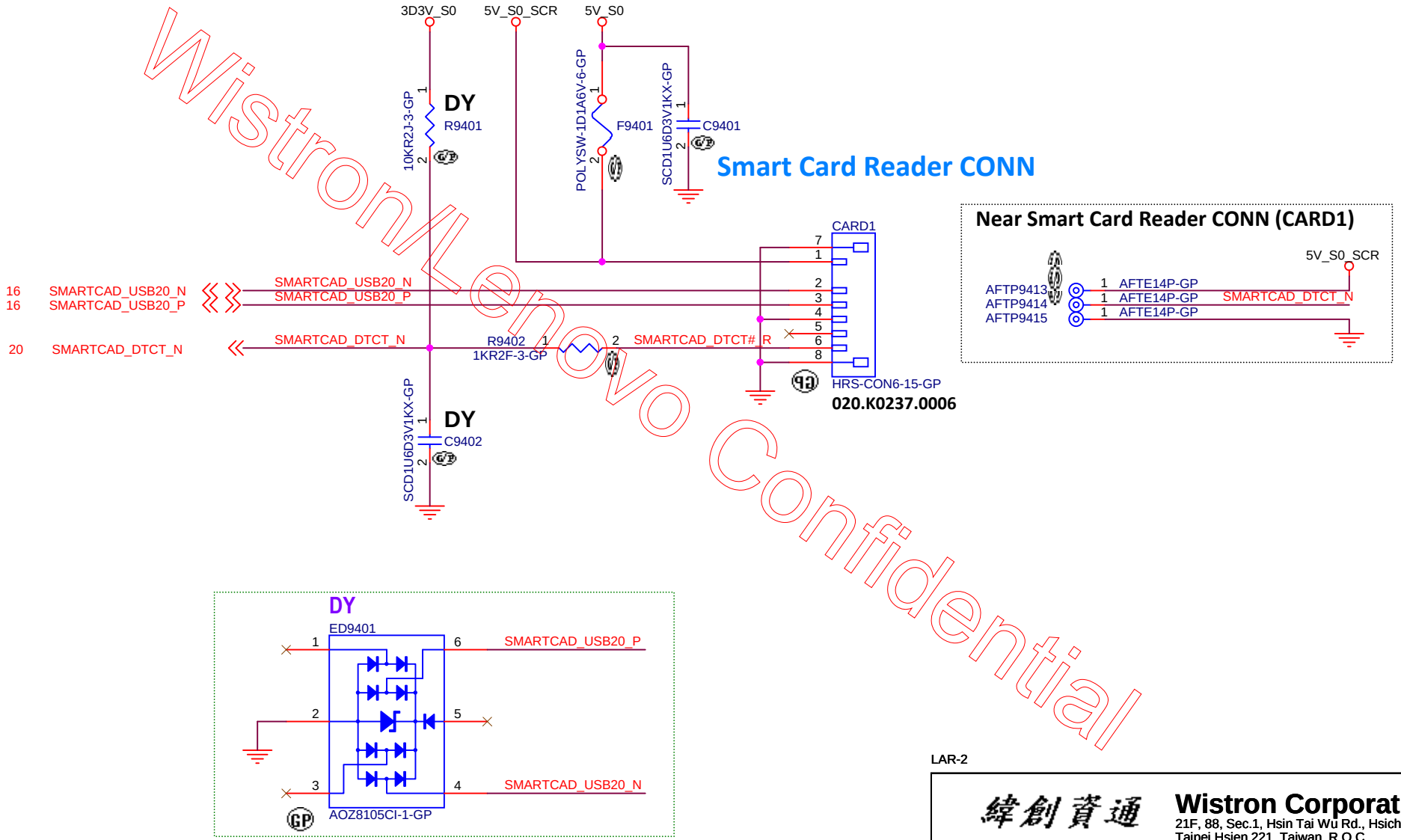
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EXT IO (ACTIVE PEN)***

Size	Document Number	Rev
A4	**ARES-2**	1

Date: Thursday, August 06, 2020 Sheet 93 of 106



LAR-2

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Title	***EXT IO (SMART CARD)***
Size: A4	Document Number: **ARES-2**
Rev: 1	
Date: Thursday, August 06, 2020	Sheet 94 of 106

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LAR-2

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Title: ***EXT IO (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 95 of 106

BLANK

LAR-2

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***COMMERCIAL (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	1

Date: Thursday, August 06, 2020 Sheet 96 of 106

BLANK

LAR-2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***COMMERCIAL (RSVD)***

Size	Document Number	Rev
A4	**ARES-2**	1

Date: Thursday, August 06, 2020 Sheet 97 of 106

BLANK

LAR-2

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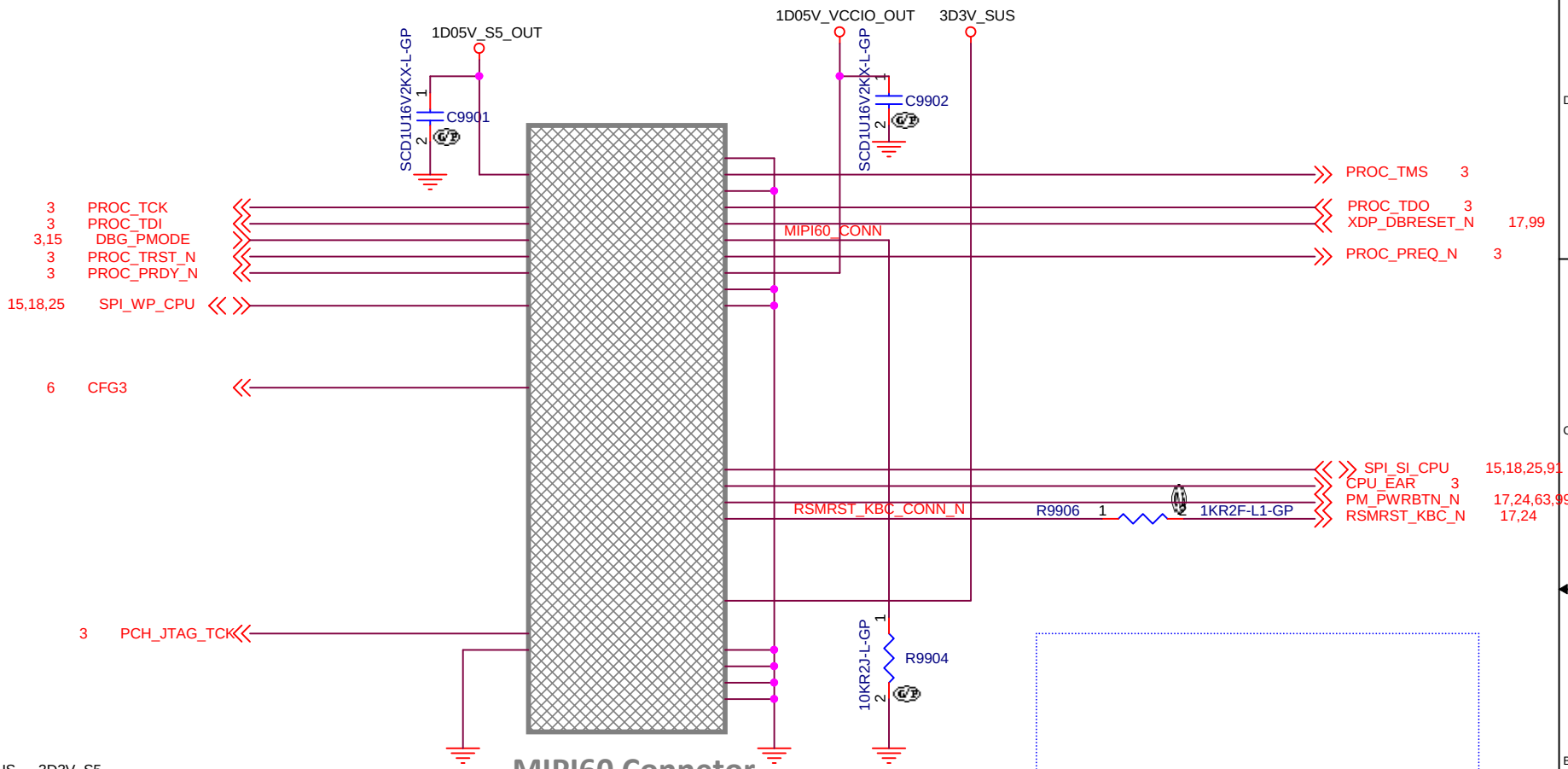
Title
COMMERCIAL (RSVD)

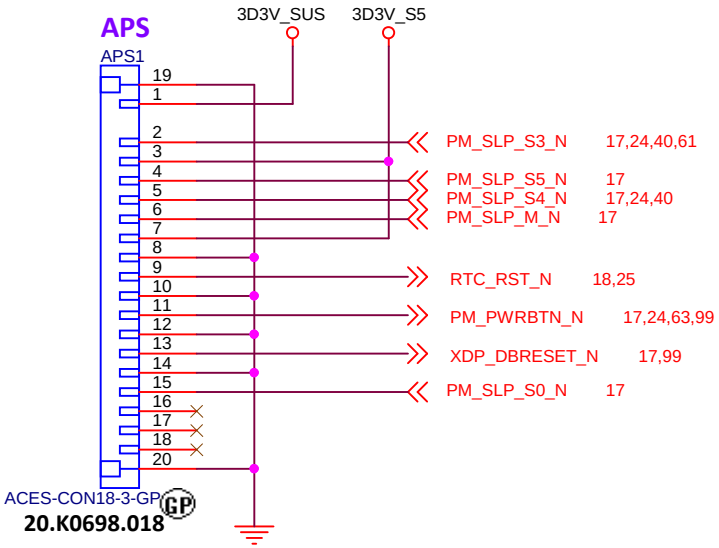
Size	Document Number	Rev
A4	**ARES-2**	**1**

Date: Thursday, August 06, 2020 Sheet 98 of 106

Main Func = Debug



APS Connector



MIPI60 Connetor

Delete MiPi60 CONN for layout space

MIPI60 Test Point

TP9901	1	PROC_TCK
TP9902	1	PROC_TDI
TP9903	1	DBG_PMODE
TP9904	1	PROC_TRST_N
TP9905	1	PROC_PRDY_N
TP9906	1	SPI_WP_CPU
TP9907	1	CFG3
TP9908	1	PCH_JTAG_TCK
TP9909	1	PROC_TMS
TP9910	1	PROC_TDO
TP9911	1	XDP_DBRESET_N
TP9912	1	PROC_PREQ_N
TP9913	1	SPI_SI_CPU
TP9914	1	CPU_EAR
TP9915	1	PM_PWRBTN_N
TP9916	1	RSMRST_KBC_CONN_N
TP9920	1	MIPI60_CONN

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Title: **DEBUG (APS)**

Size	Document Number	Rev
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Date: Thursday, August 06, 2020 Sheet 99 of 106

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Size: A	Document Number: ARES-2
Rev: 1	
Date: Thursday, August 06, 2020	Sheet 100 of 106

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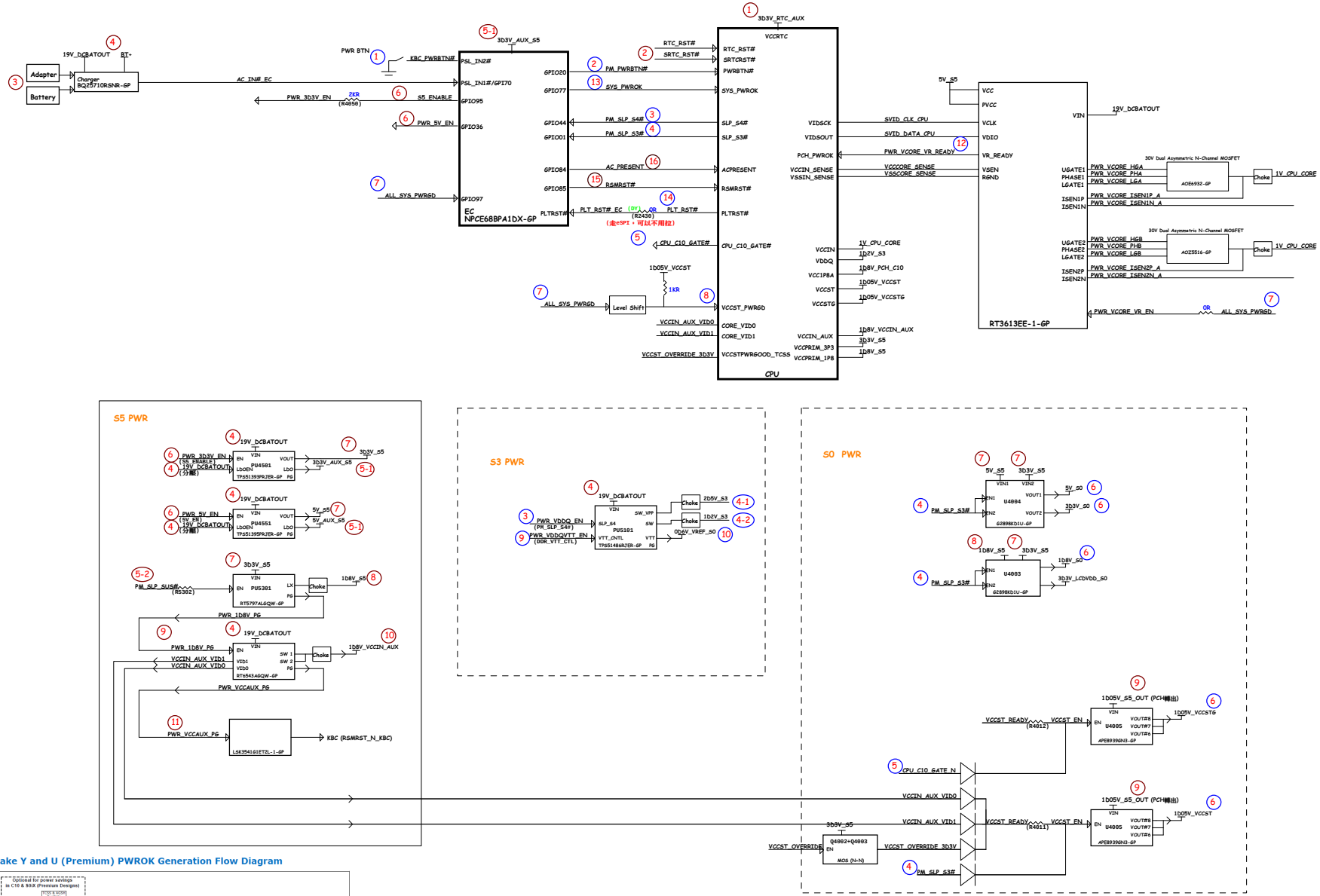
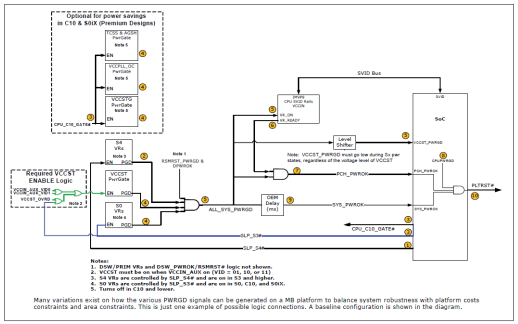
Date: Thursday, August 06, 2020	Sheet 101 of 106	



ure 267. Tiger Lake Y and U (Premium) PWROK Generation Flow Diagram



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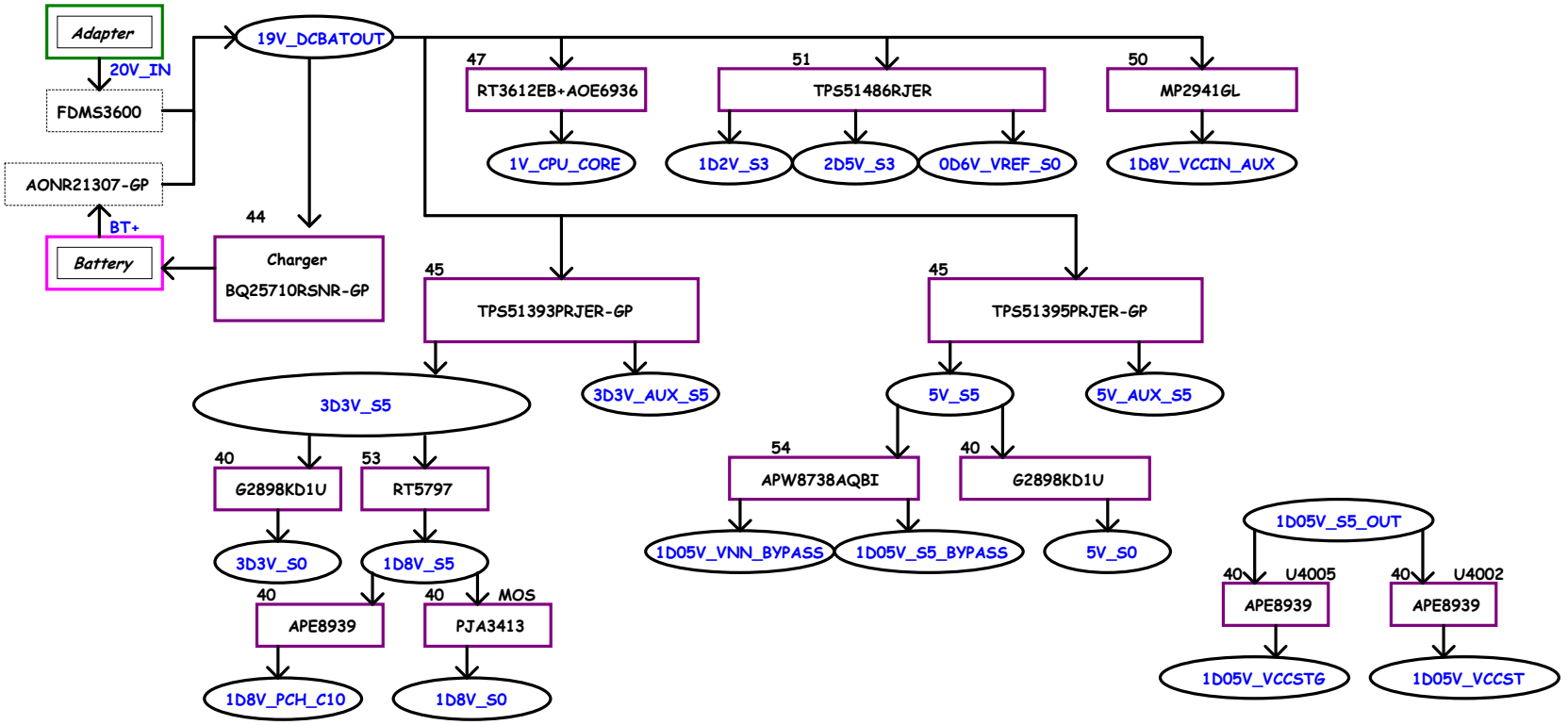
POWER BLOCK DIAGRAM



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Size	Document Number	Rev
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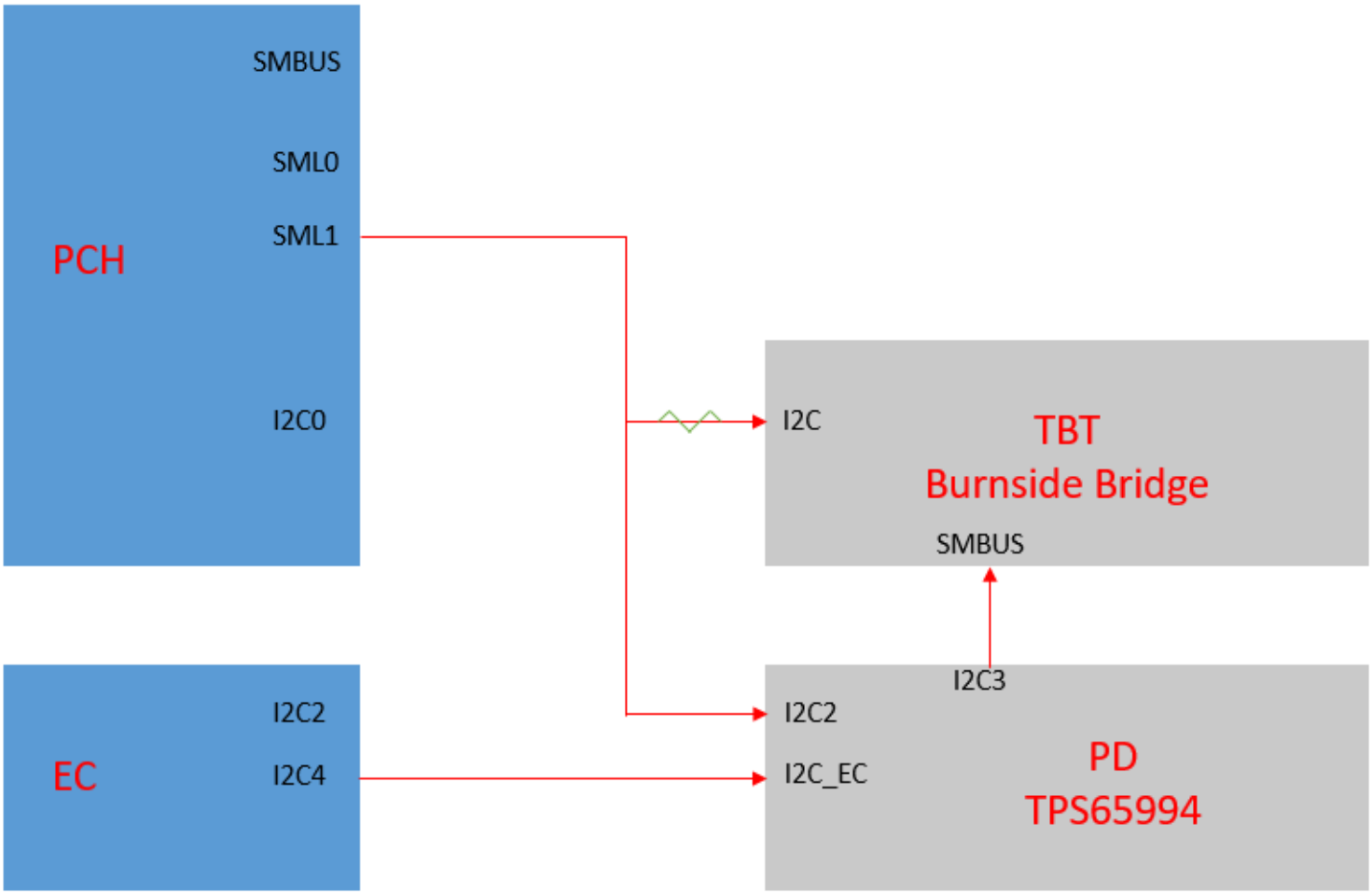
Date: Thursday, August 06, 2020 Sheet 103 of 106



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Title: ***SMB Block Diagram***

Size	Document Number	Rev
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Date: Thursday, August 06, 2020 Sheet 104 of 106

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Size: A	Document Number: ARES-2
Rev: 1	
Date: Thursday, August 06, 2020	Sheet 105 of 106

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Rev: 1	
Date: Thursday, August 06, 2020	Sheet 106 of 106