MS-7A57

ATX
Ver: 20

Z270 Gmaing 7 / Z270 MPOWER

Kabylake Platform

CPU: Kabylake S

PCH: Z270

SPI ROM : 128 MB

Memory: DDR4 * 4 (Dual Channel)

Power Solution:

CPU : UP9508
VCCSA : RT8125E
VCCIO : MPS NB685
DDR : POWERVATION 3205Q (2PH)
PCH : RT8125E

ACPI: MPS

Onboard Chip:

LAN Killer E2500
Dual Codec:ALC1220 *2
SIO:NTC6795D
Type C & A : ASM2142 + ASM1543
Clock Gen : TBD
USB3.1 Host : ASM2142 *2
USB Charger : SLG55583A * 2
USB3 Redrive : ASM1464 * 6
USB2 Redrive : TUSB211 * 2
HDMI:PTN3360D
Flash BIOS : F75504
GPIO : NCT5605 * 2

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X8) Slot * 1
PCI Express (X4) Slot * 1
PCI Express (X1) Slot * 3
M.2 Slot (Socket 3) * 3

Rear I/O Connectors

PS2 + Dual USB2
Clear COMS
Reflash BIOS USB2
DP+HDMI
RJ45 + Dual USB3
USB3.1 (Type C+ A)
Audio Jack 5 Port +SPDIF

Internal Connectors

Dual SATA * 6
U.2 *1
FUSB3 Header * 2
FUSB2 Header * 2
Front type C * 1
Front Audio Header * 1
Front Panel Header * 2
SPI Header * 1
TPM Header * 1
CPU Fan * 1
PUMP_FAN * 1
System Fan * 4

Botton

Power
Reset
Gaming Boost
FLASHB

LED

Debug LED

Internal Pin Header

JLED1
JSLOW1
JLN1
JOC_RT1
JOC_FS1

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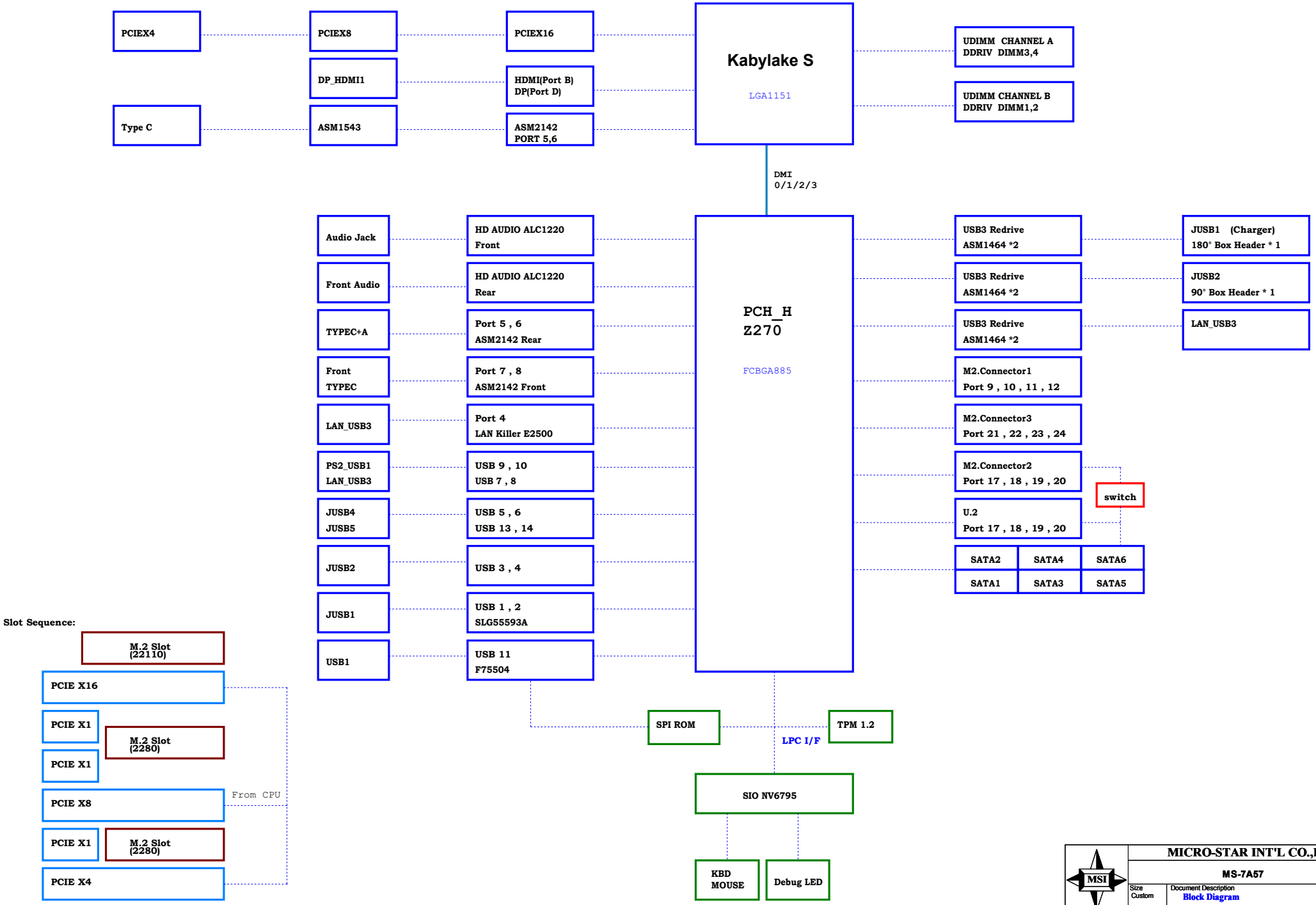
MS-7A57 Block Diagram



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Size: Custom	Document Description: Block Diagram	Rev: 10
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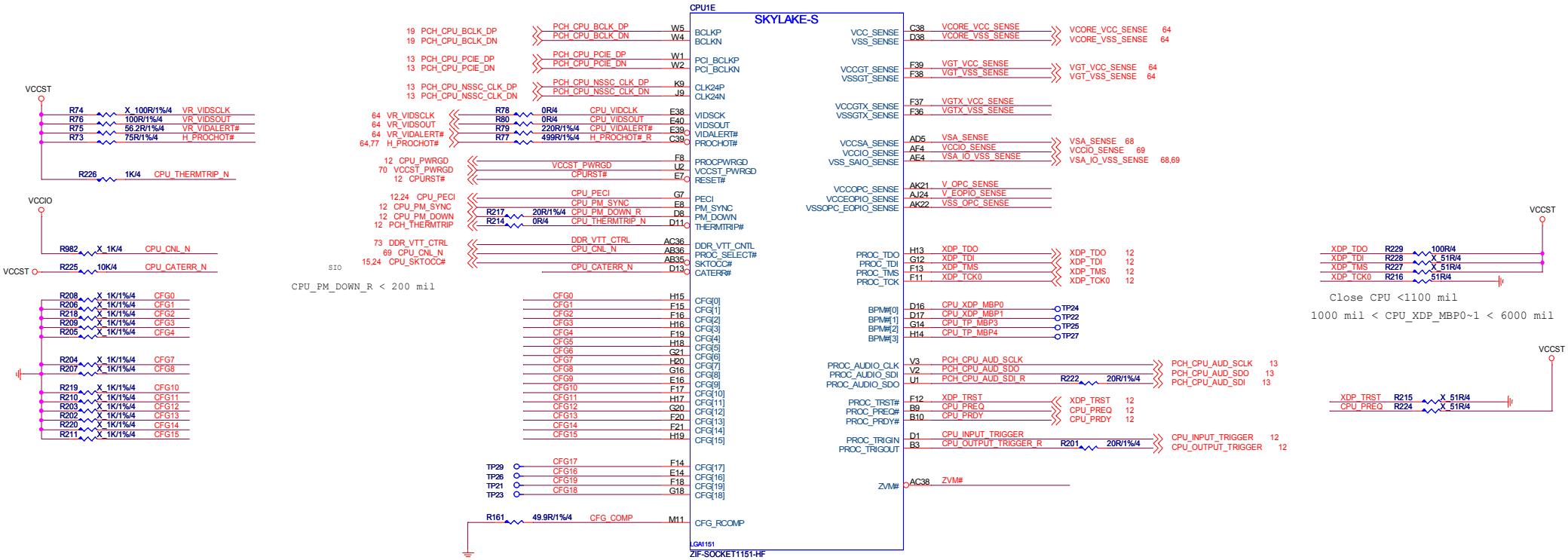
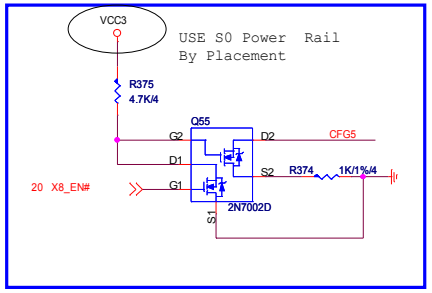
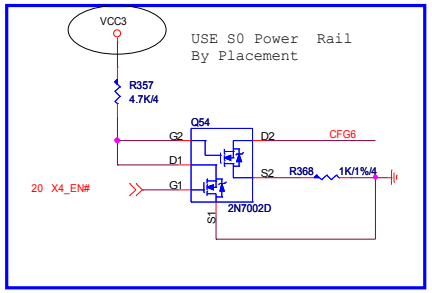
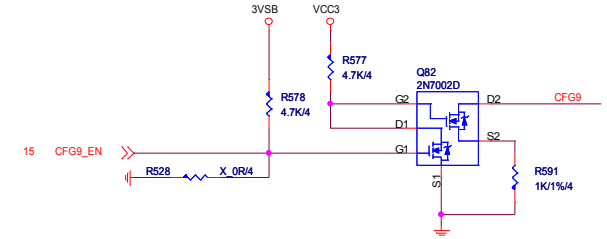


X8 and X4 Ctrl

ENABLE#		SLOT2	SLOT5	SLOT7
X8	X4			
0	0	X8	X4	X4
0	1	X8	X8	X0
1	0	None	None	None
1	1	X16	X0	X0



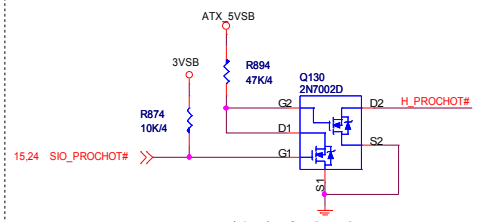




CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU_PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		



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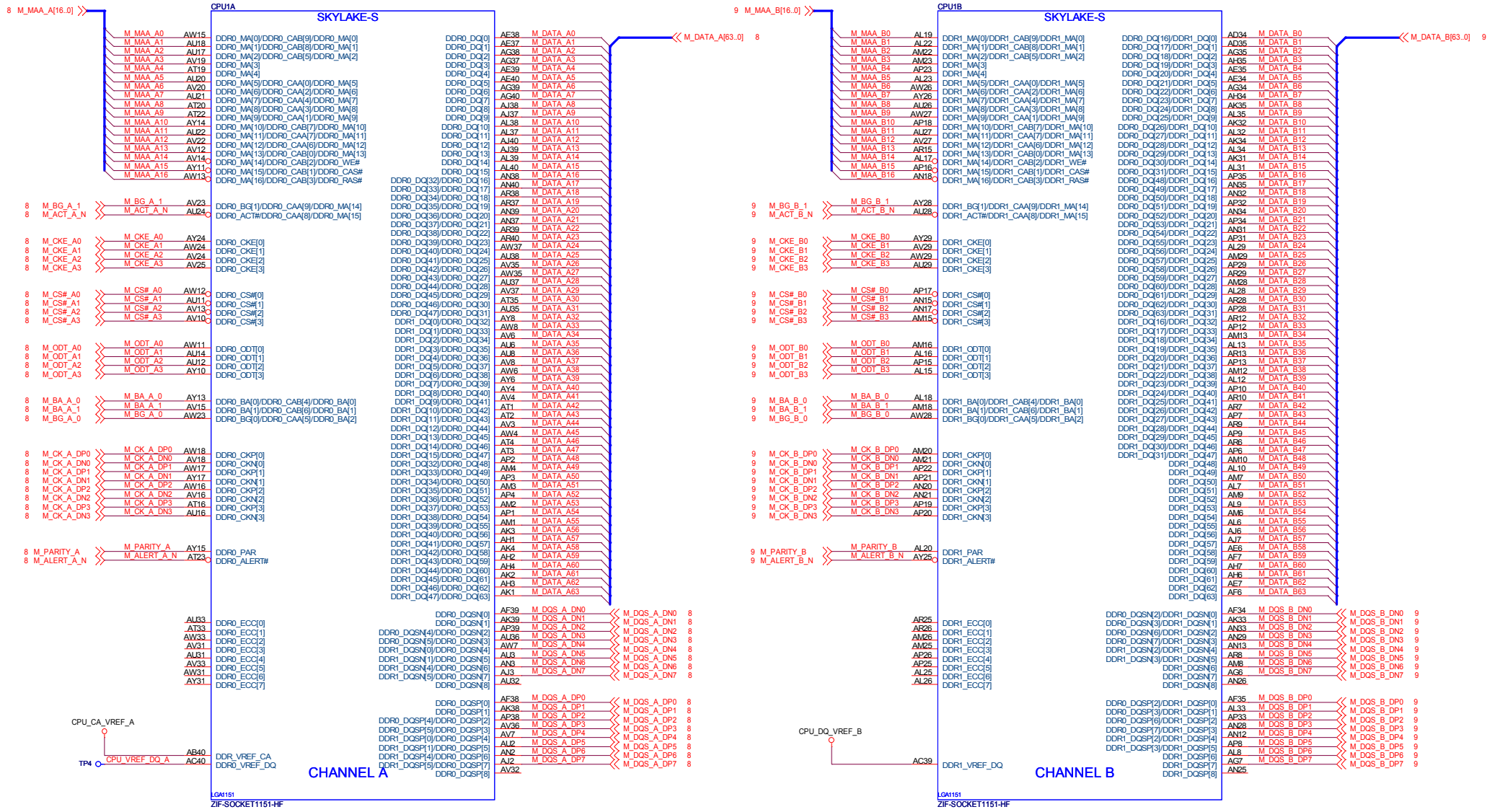
SOCKET PN N12-151A010-L06



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Size: Custom	Document Description: CPU-Memory
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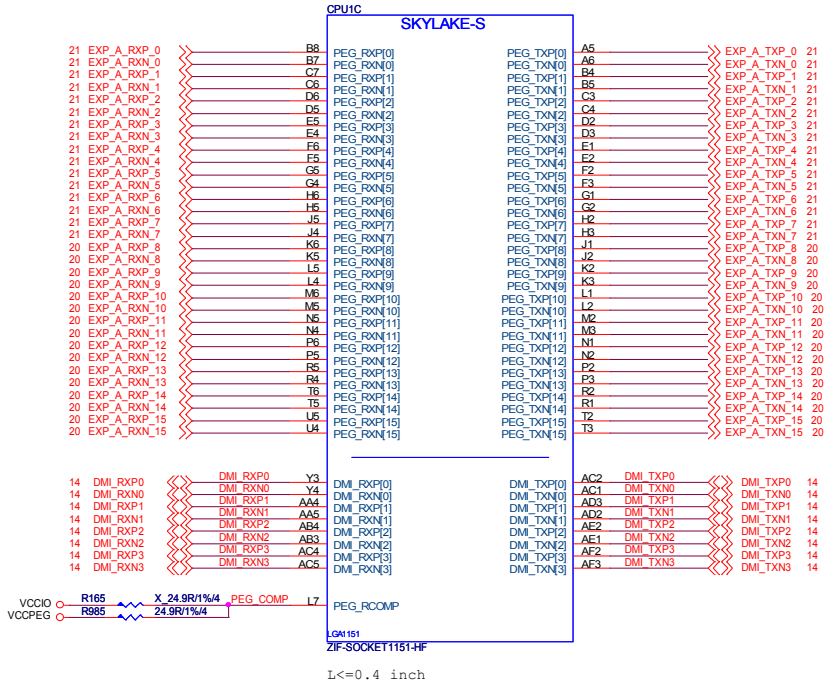
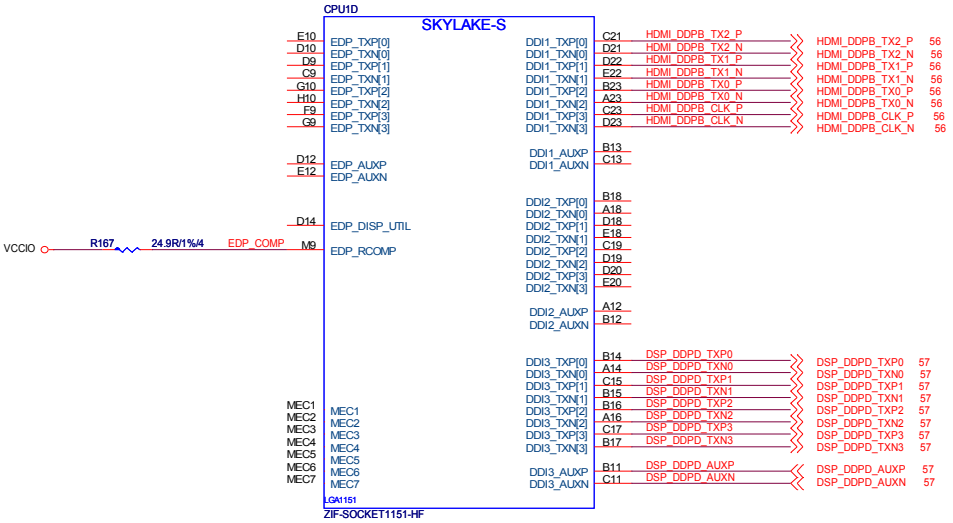
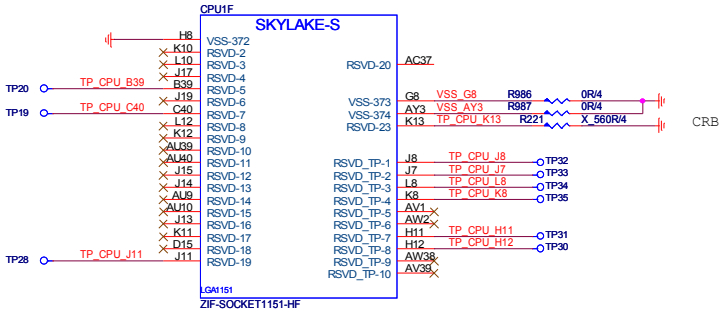


L<=0.4 inch





MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU-PEG/Display/RSD	Rev: 10
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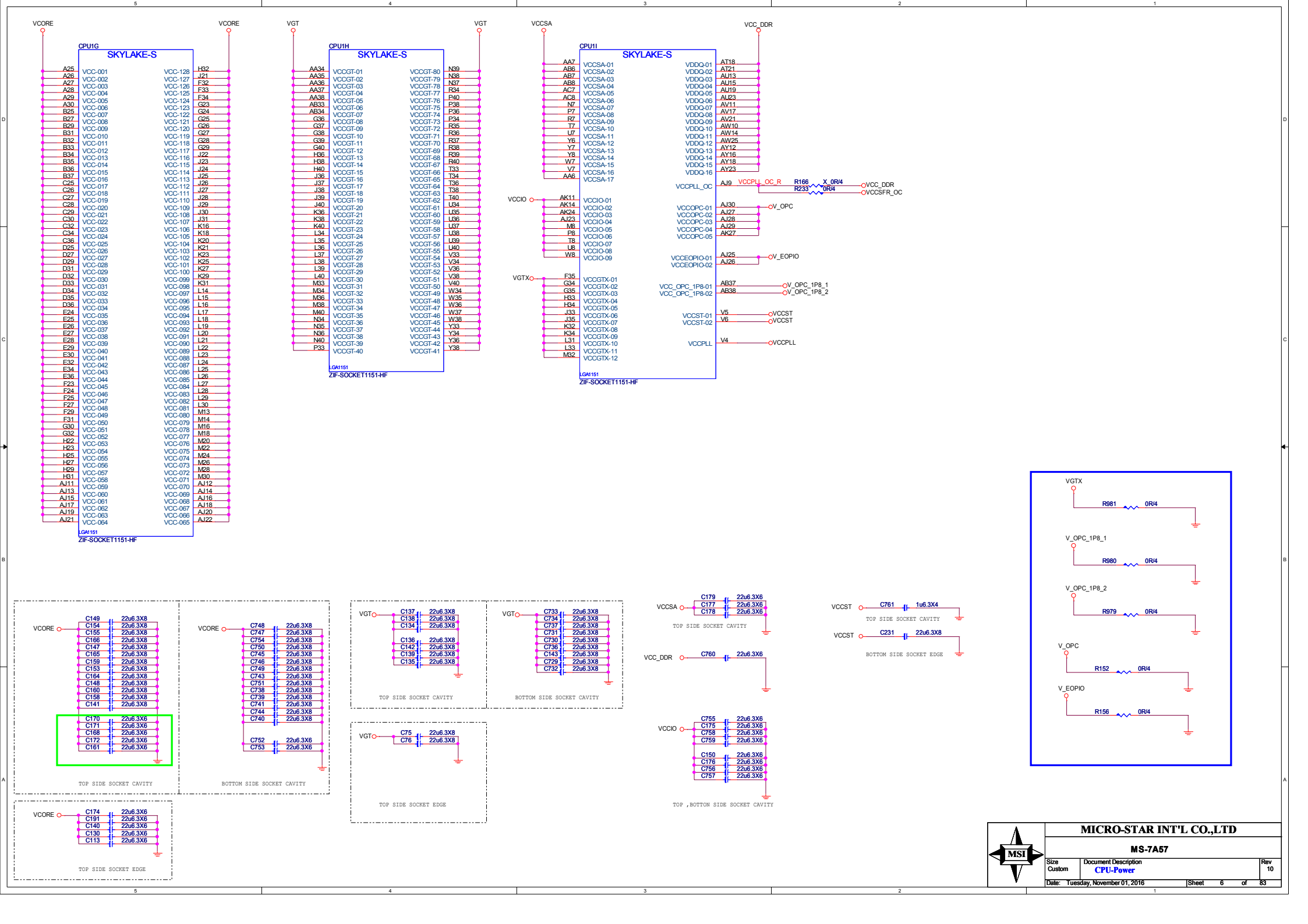
CPU1G
SKYLAKE-S
ZIF-SOCKET1151-HF
CPU1H
SKYLAKE-S
ZIF-SOCKET1151-HF
CPU1I
SKYLAKE-S
ZIF-SOCKET1151-HF
VCORE
VGT
VCCSA
VCC_DDR
VCCPLL_OC_R
R166
X_0R/4
R233
0R/4
VCC_DDR
VCCSFR_OC
V_OPC
V_EOPIO
V_OPC_1P8_1
V_OPC_1P8_2
VCCST
VCCPLL
TOP SIDE SOCKET CAVITY
BOTTOM SIDE SOCKET CAVITY
TOP SIDE SOCKET EDGE
TOP ,BOTTON SIDE SOCKET CAVITY
R981
R980
R979
R152
R156
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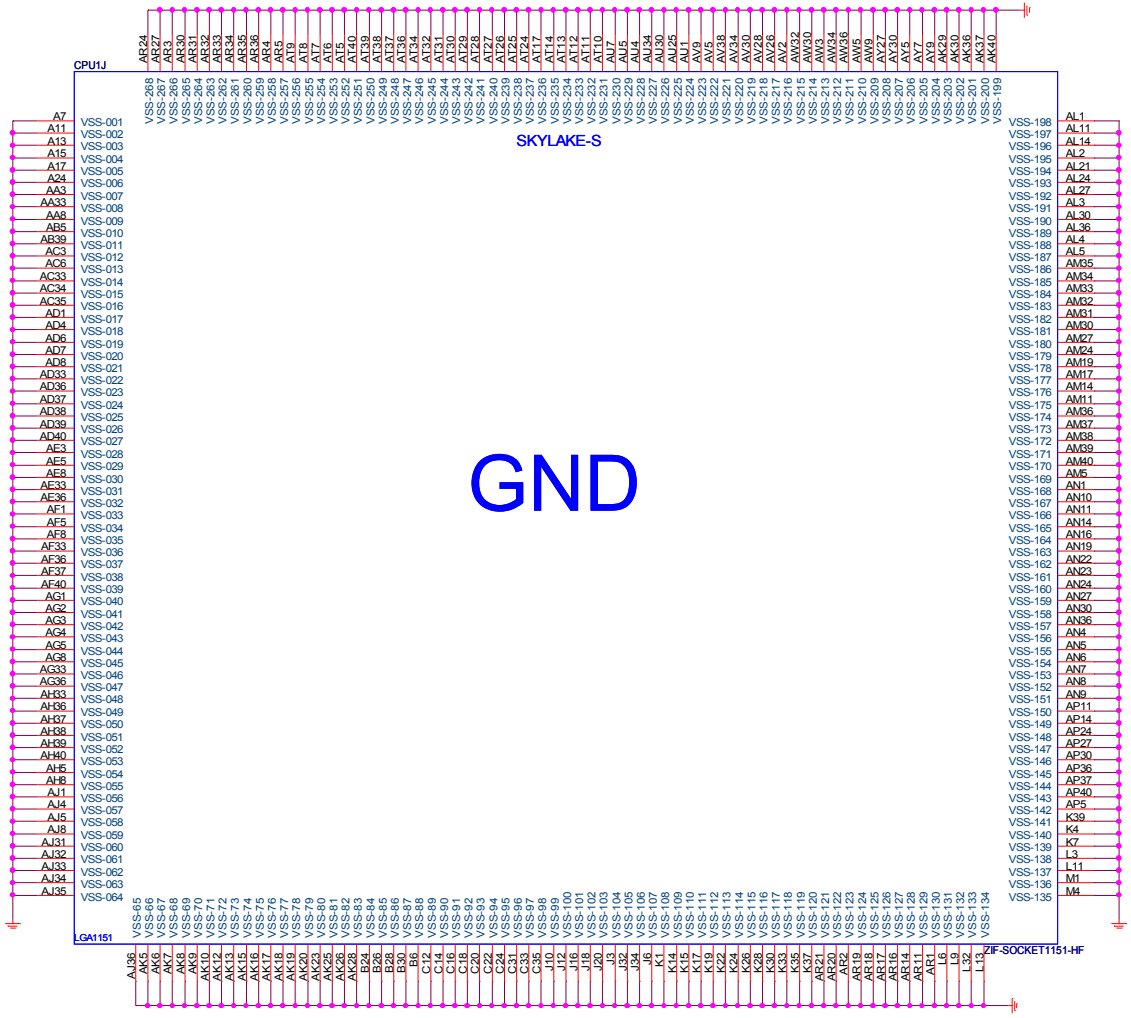

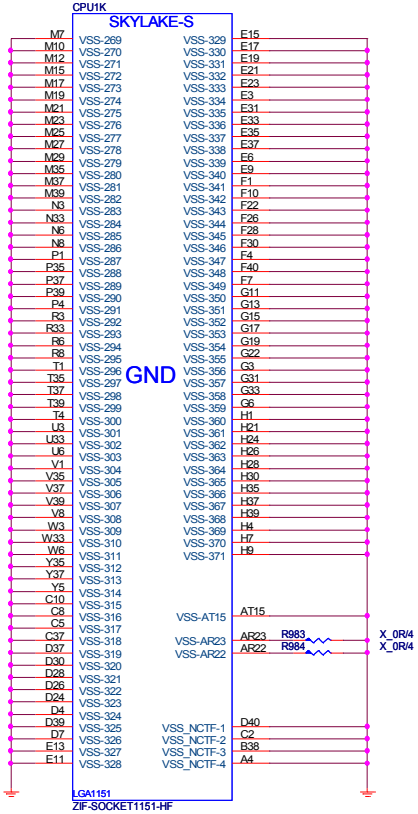

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Size: Custom	Document Description: CPU-GND	Rev: 10
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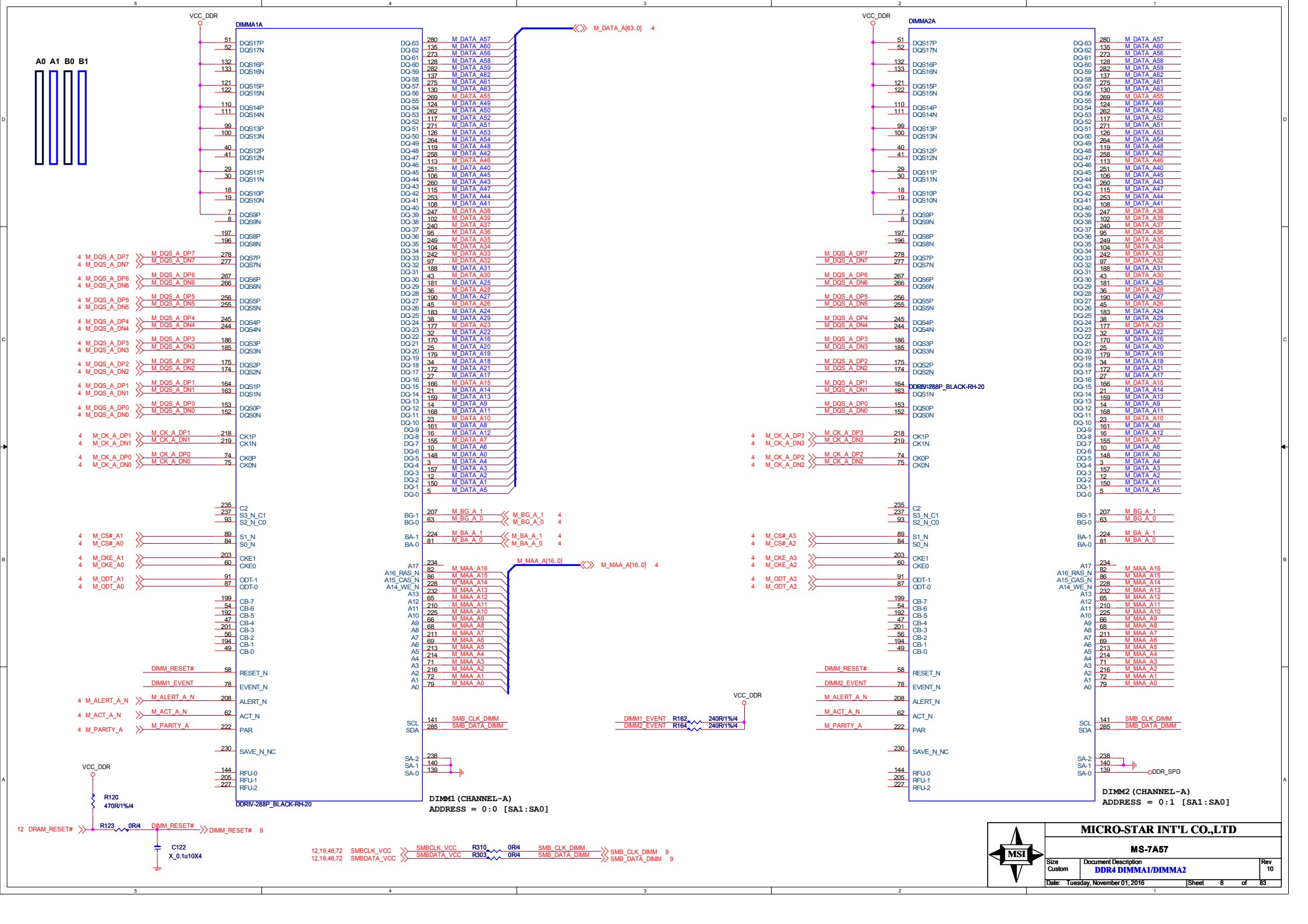

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Size	Document Description	Rev
Custom	DDR4 DIMMA1/DIMMA2	10

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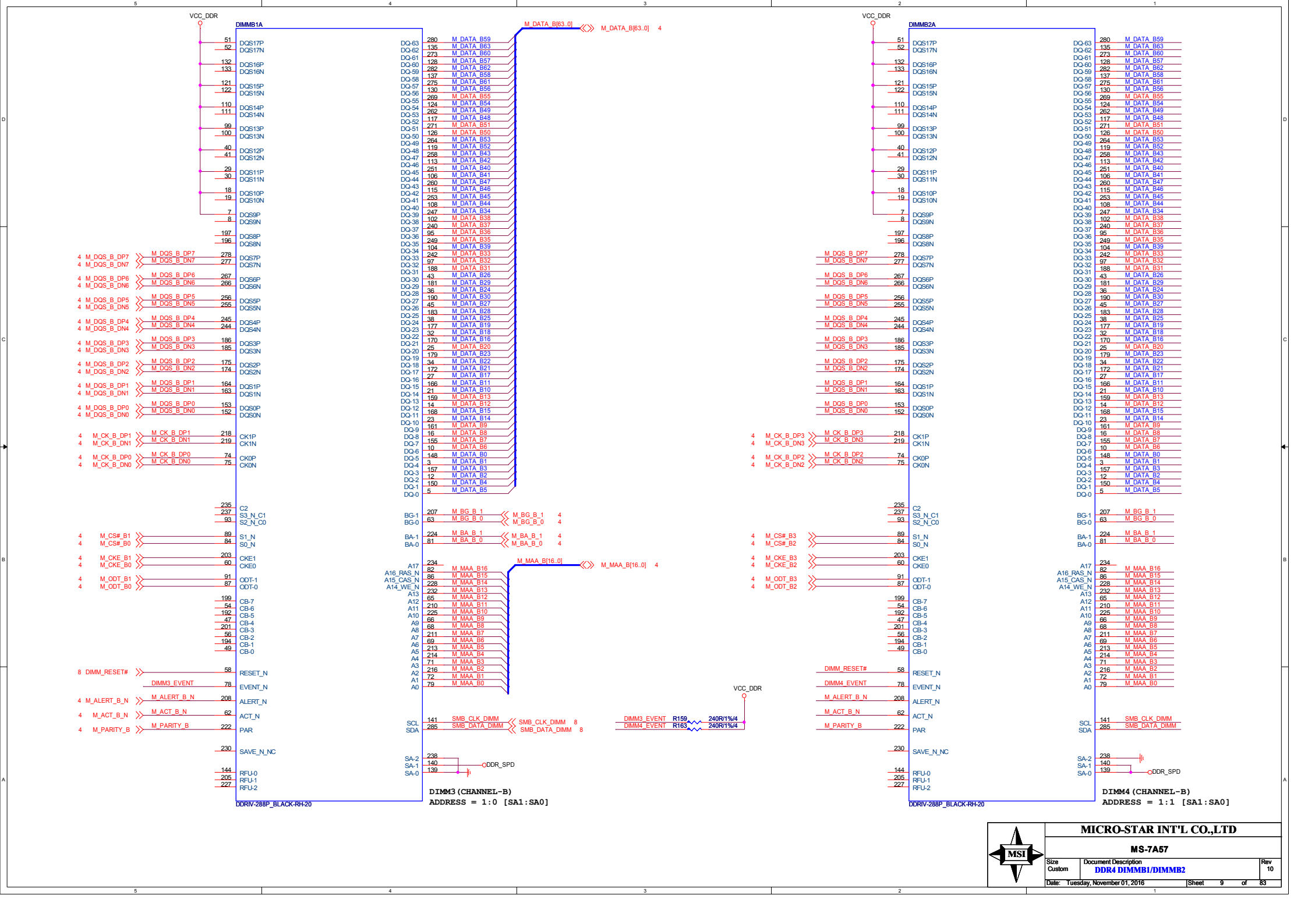

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Size	Document Description	Rev
Custom	DDR4 DIMMB1/DIMMB2	10

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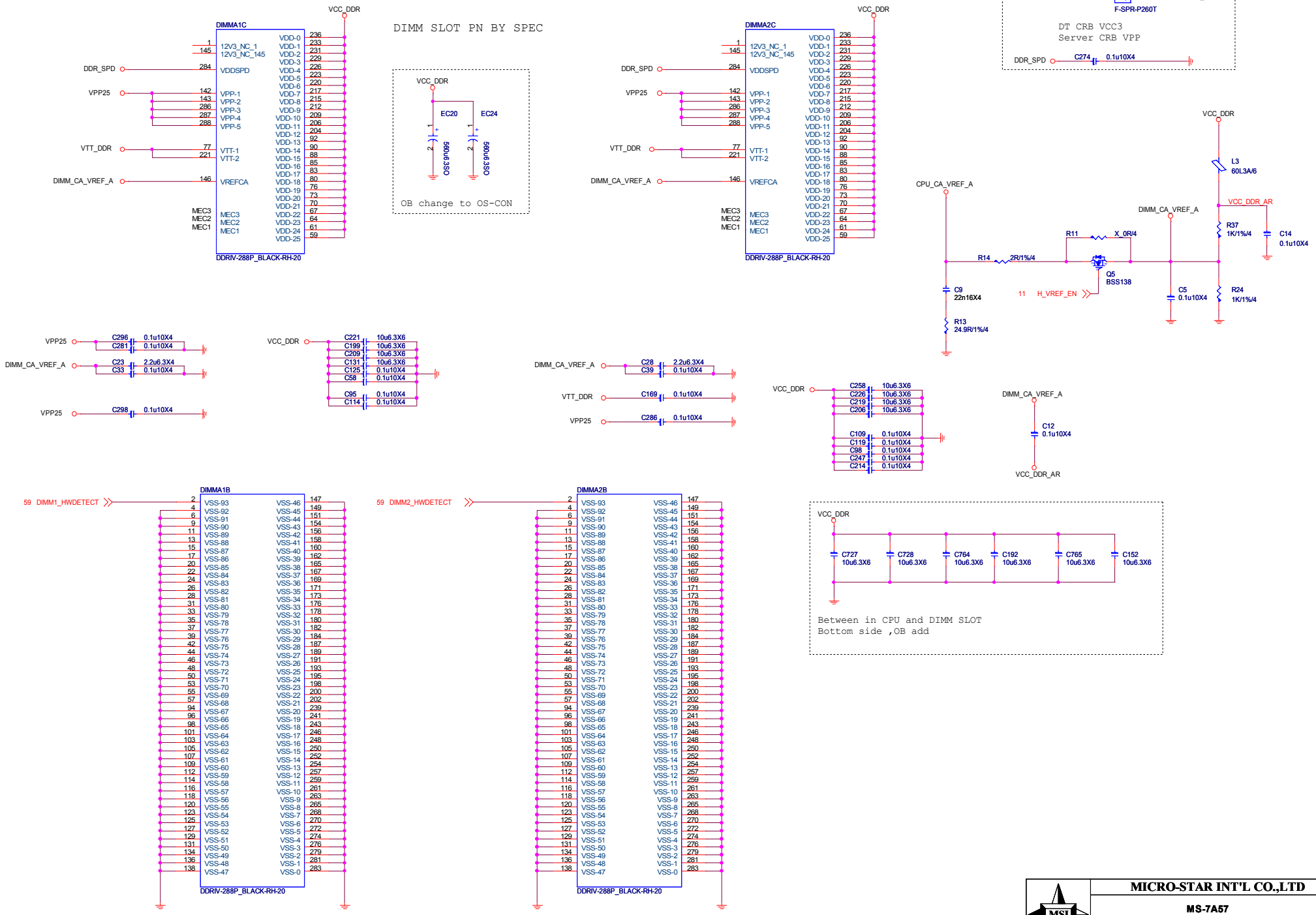

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: DDR4 POWER/GND-1
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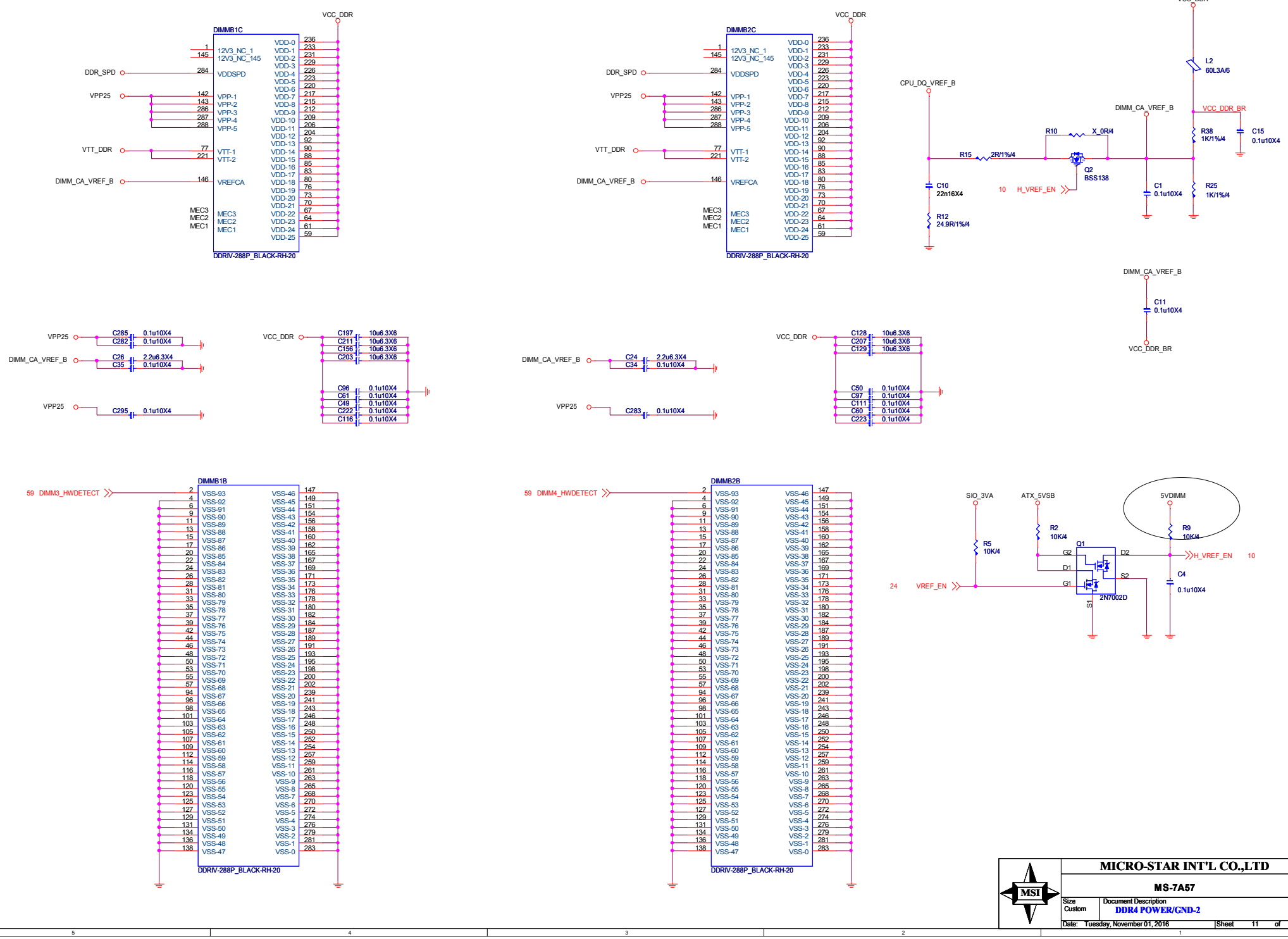

MICRO-STAR INT'L CO.,LTD		
MS-7A57		
Size: Custom	Document Description: DDR4 POWER/GND-2	Rev: 10
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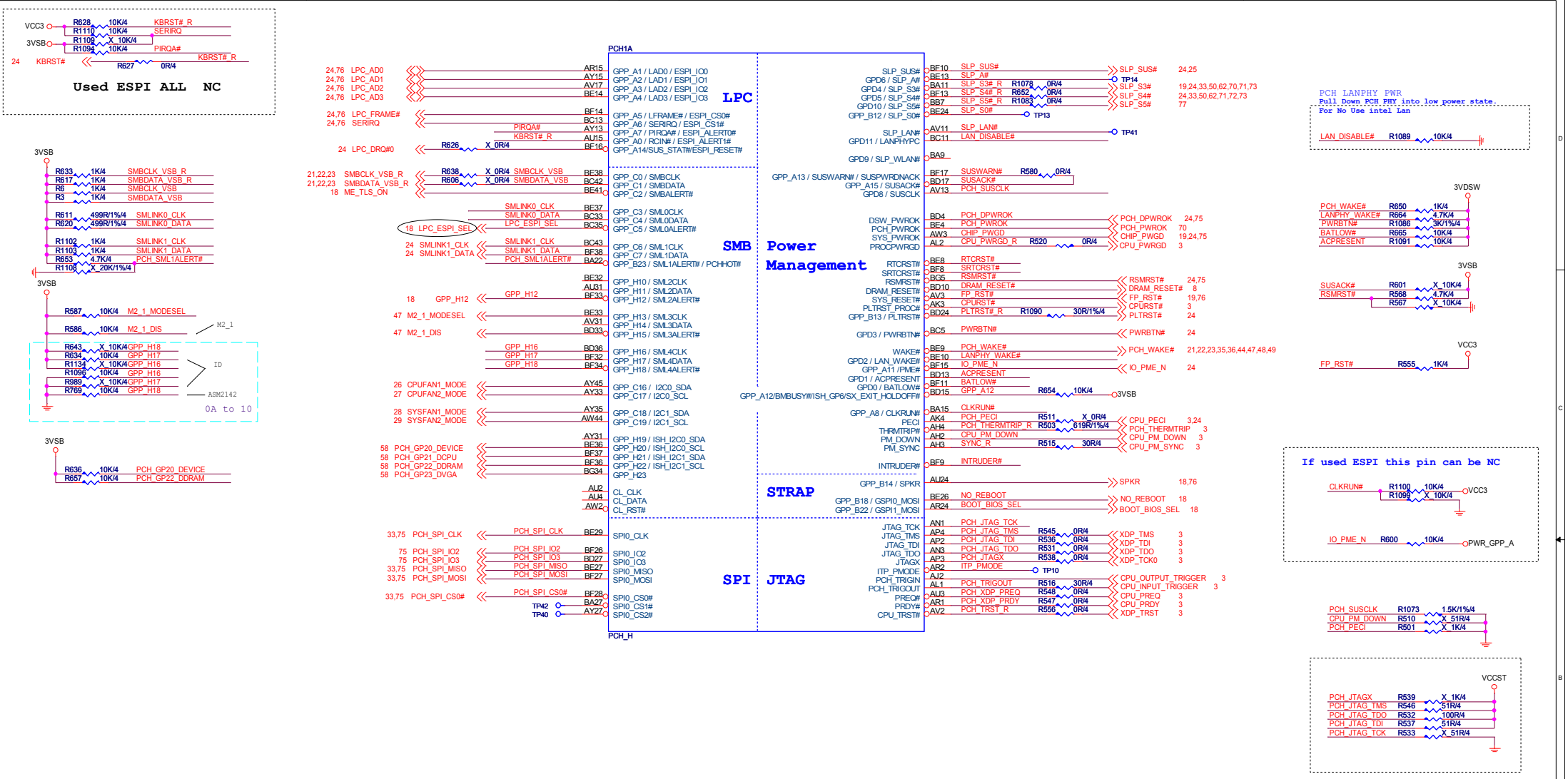

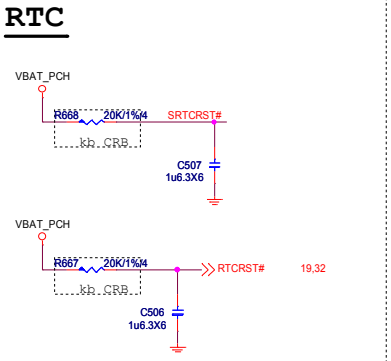

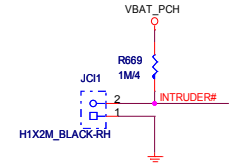

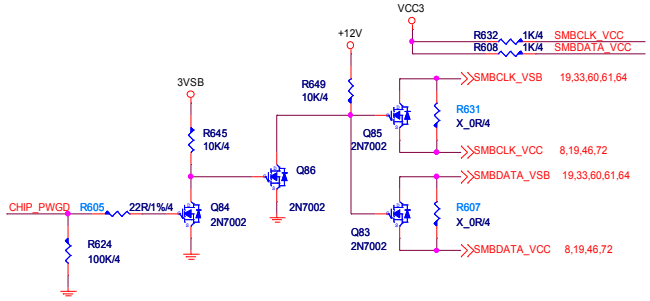

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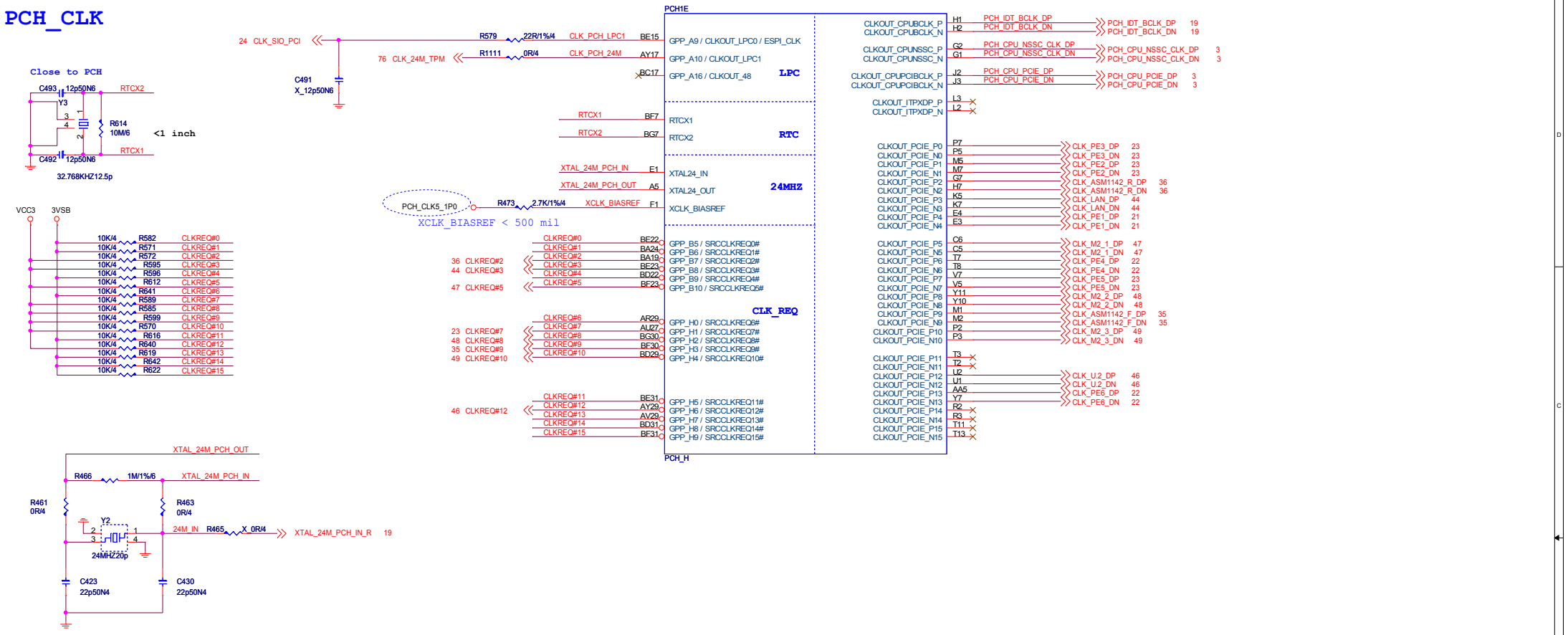
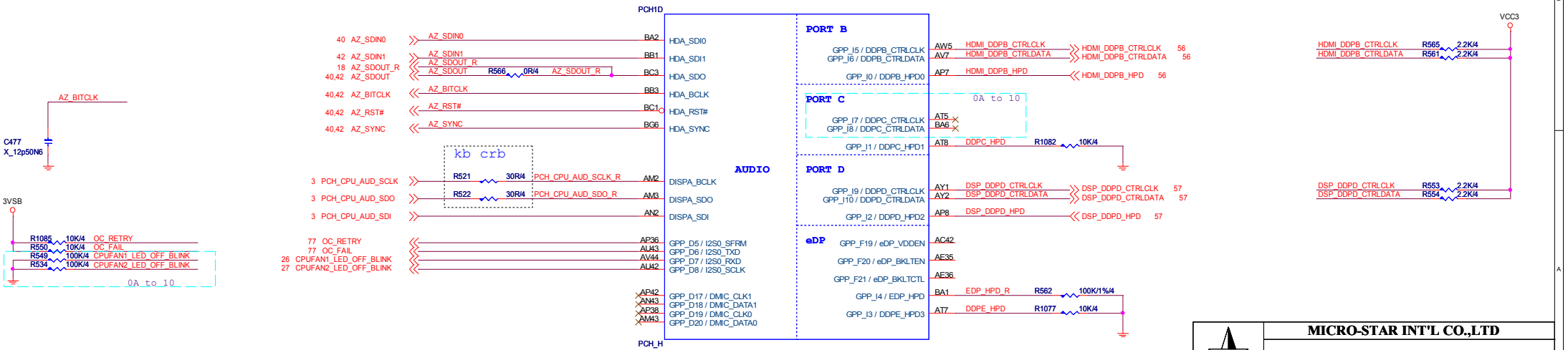
PCH_CLK



PCH_AUDIO



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PCH-Clock/Audio	10

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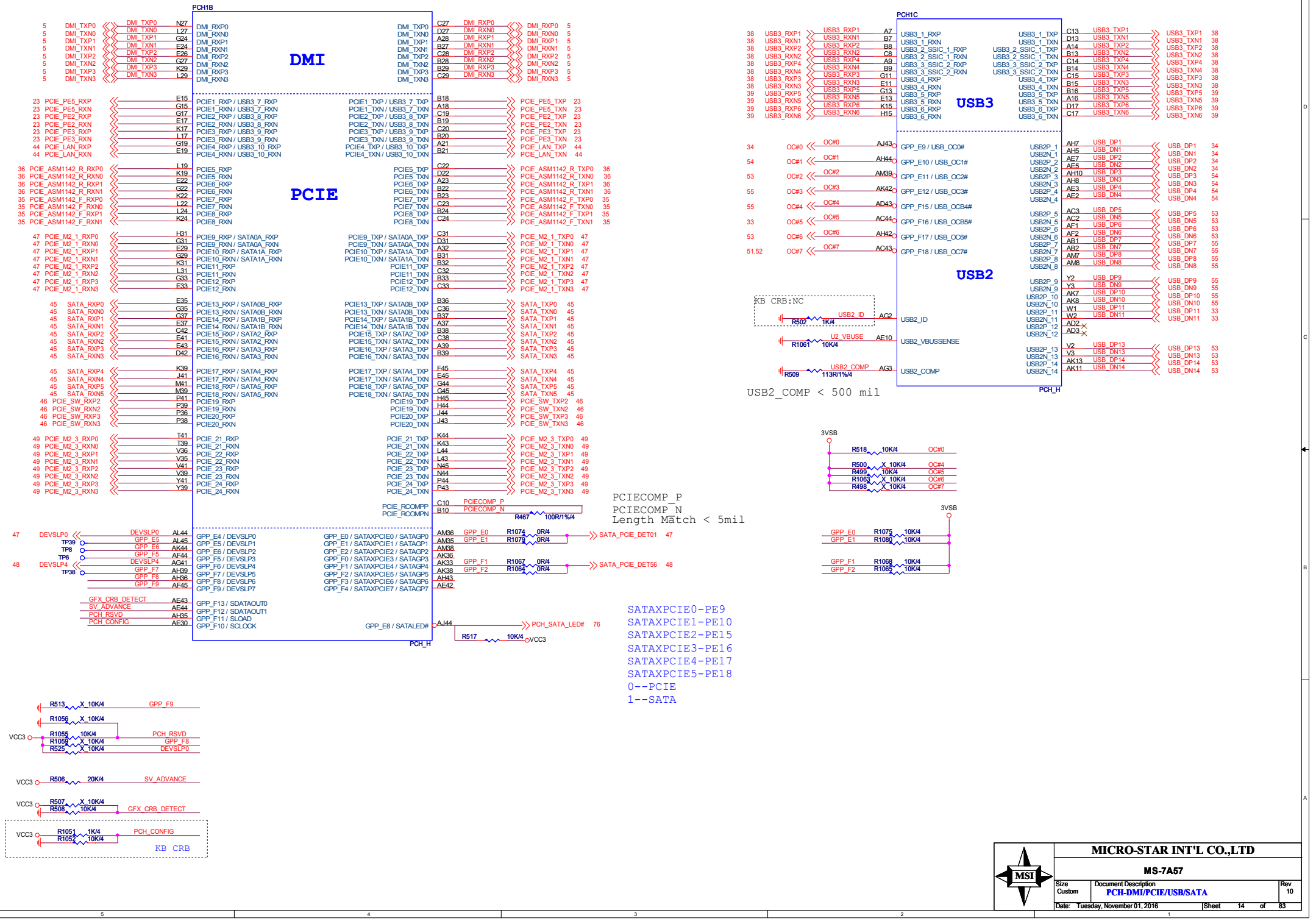

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: PCH-DMI/PCIE/USB/SATA
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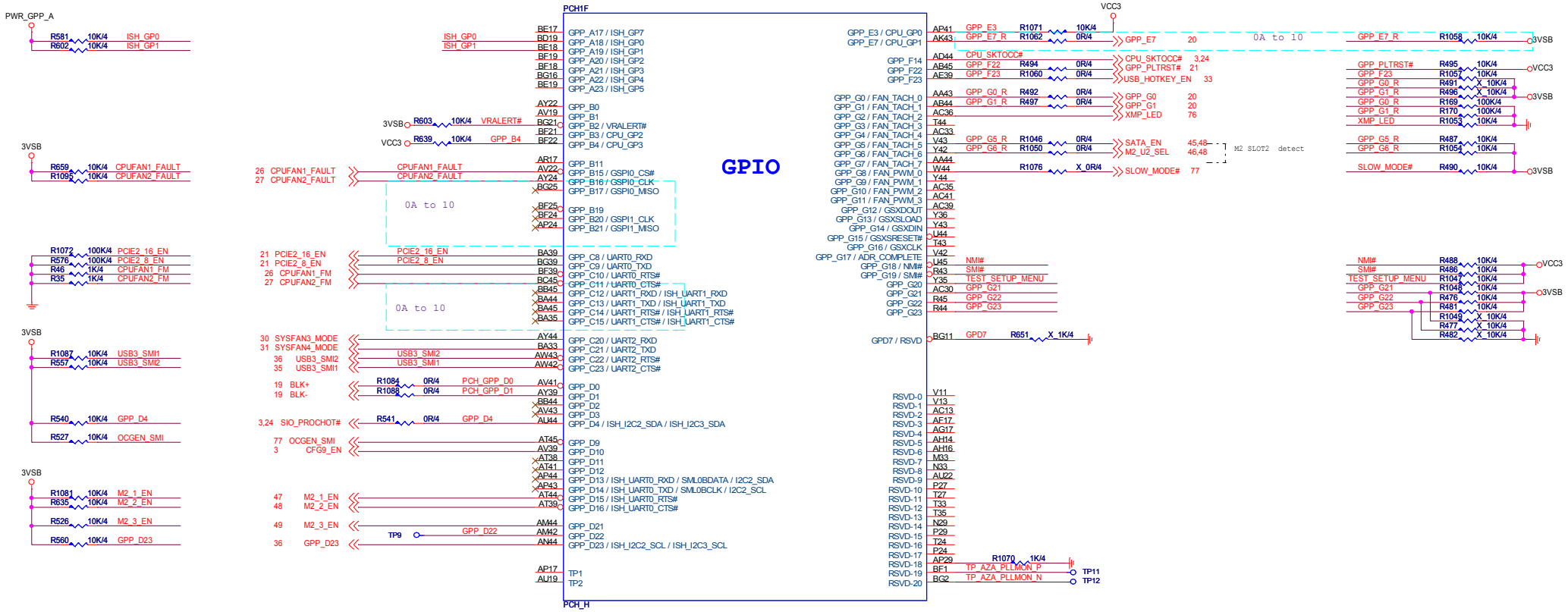
W/ SMI/NMI Funtion
GPP_B[23,20,14]
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: PCH-GPIO/RSVD
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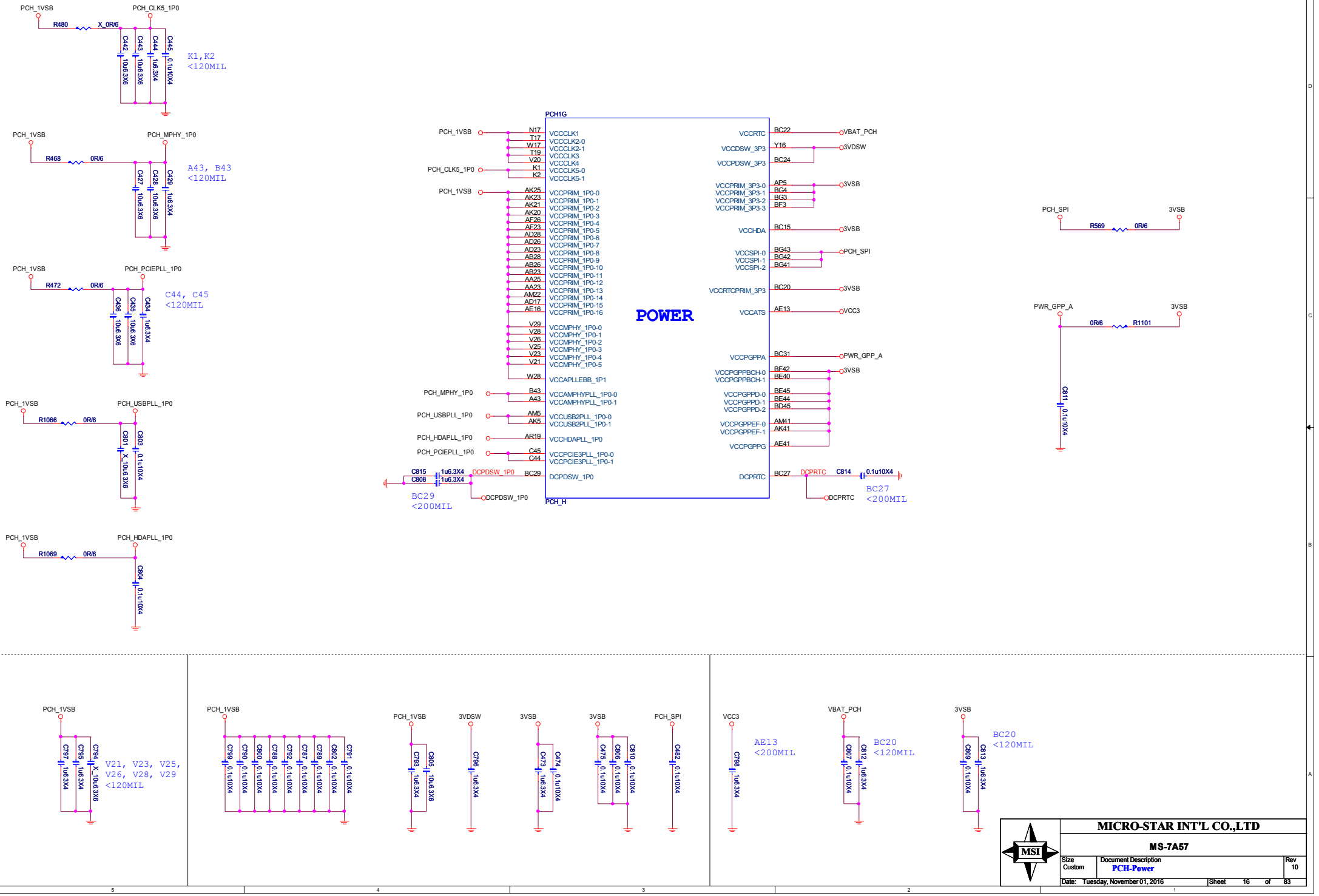

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Size	Document Description	Rev
Custom	PCH-Power	10

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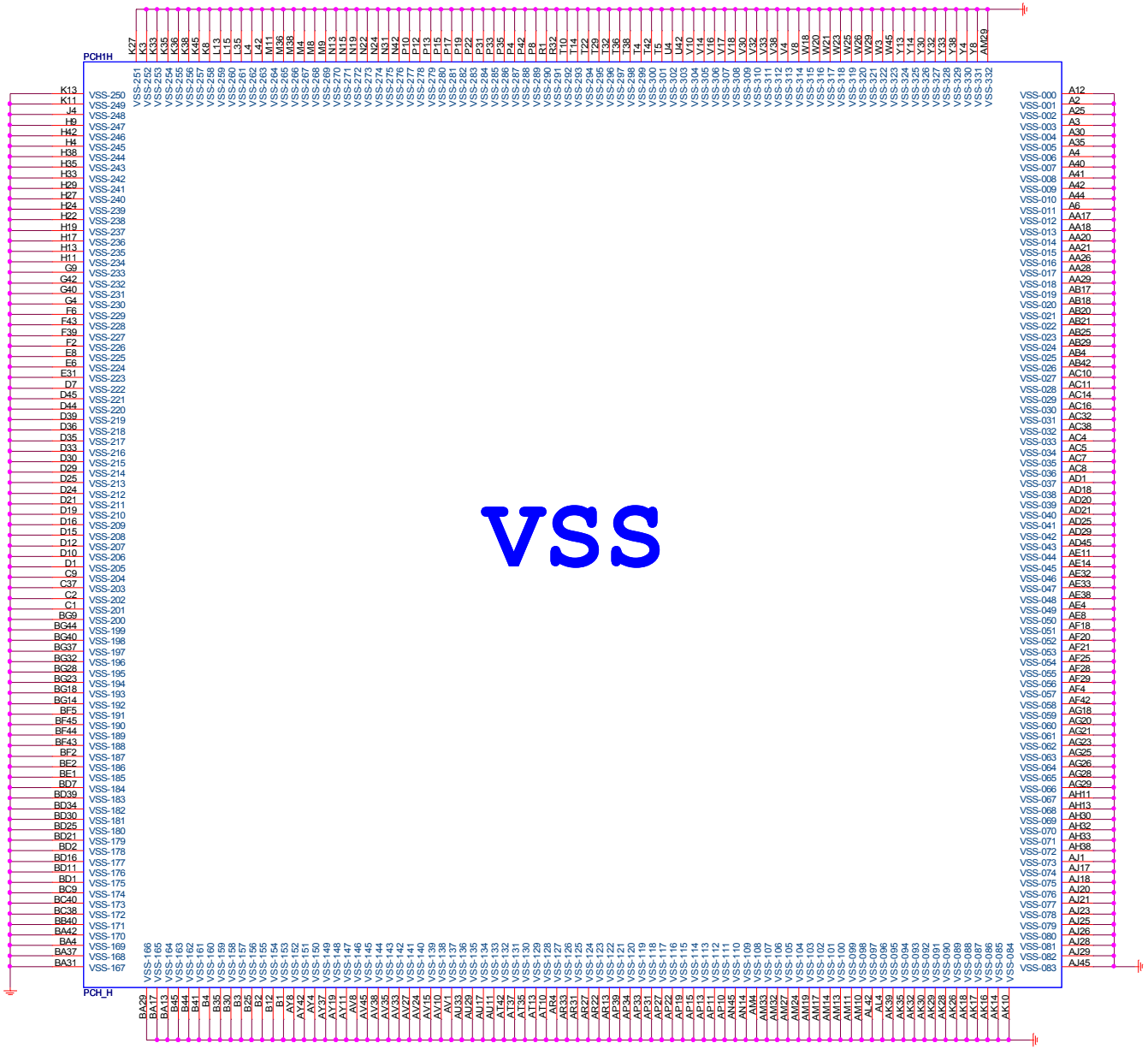

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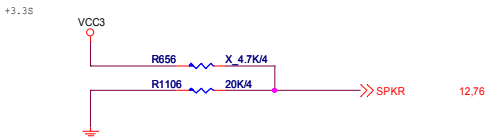
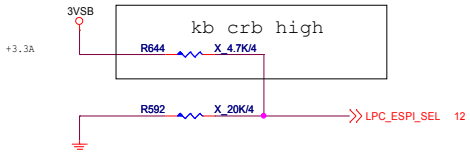
TOP Swap



Internal pull-down is disabled after PLTRST#

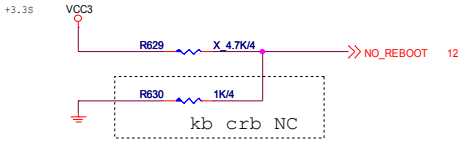
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

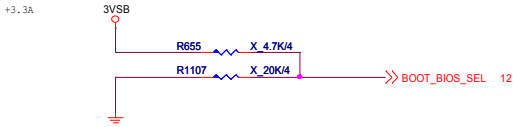
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

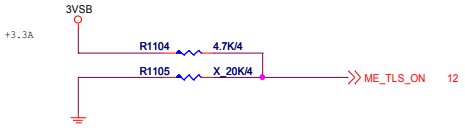
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

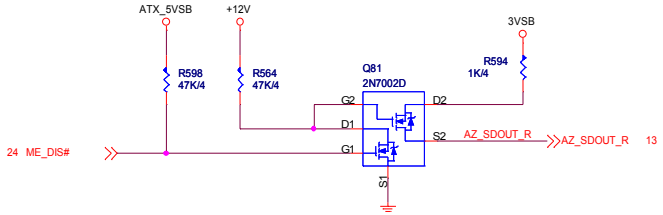
AMT and SBA with confidentiality



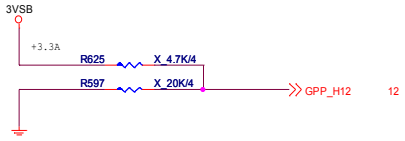
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

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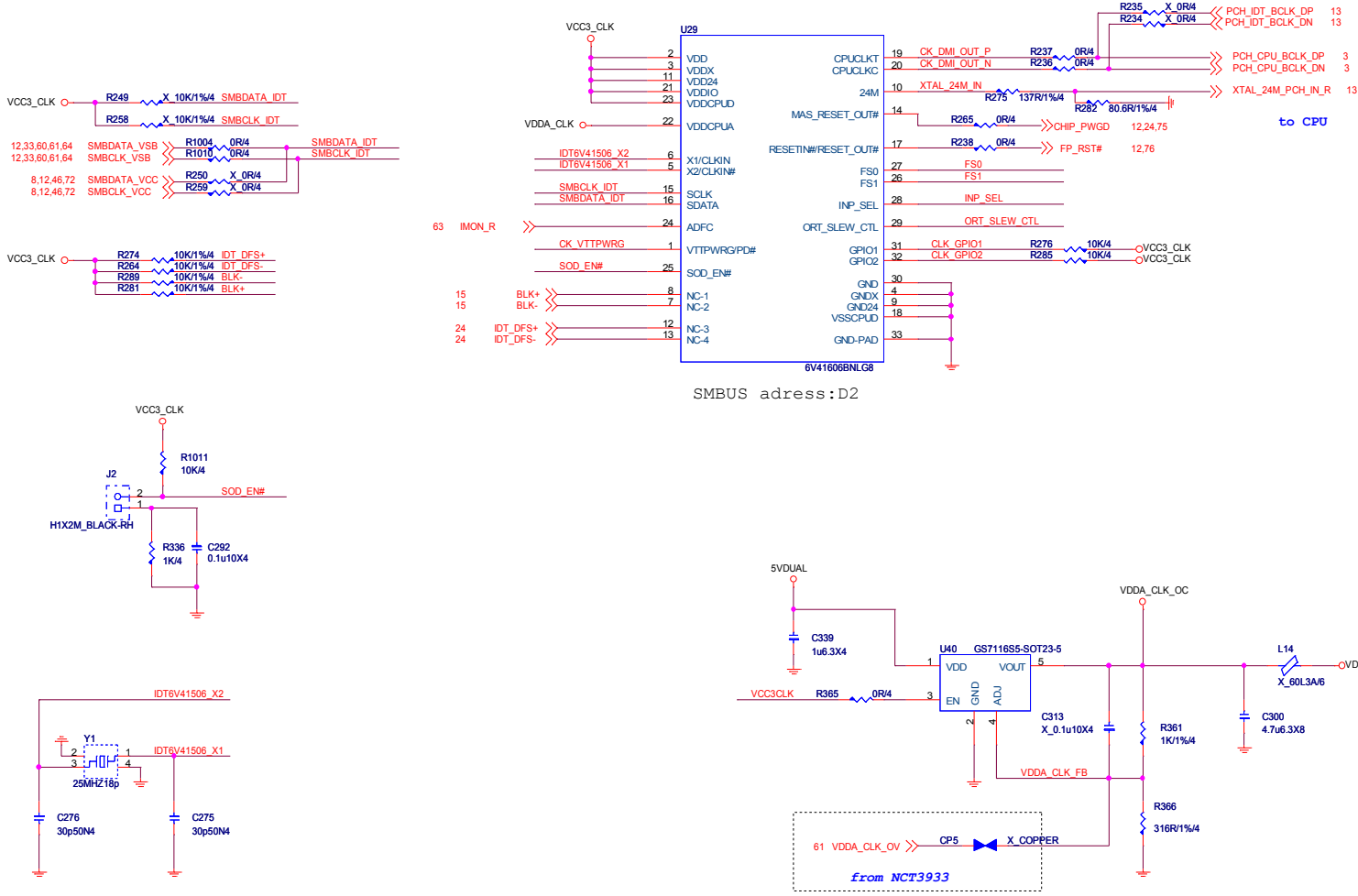
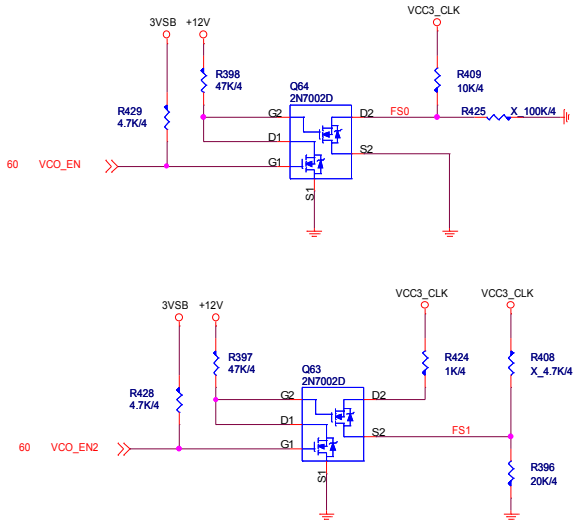
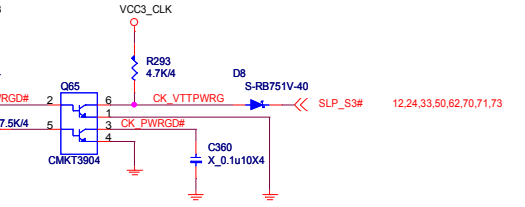




FS1	FS0	VCO Frequency
0	0	VCO 200MHz
0	1	VCO 400MHz (default)
1	0	VCO 1000MHz
1	1	VCO 100MHz

INP_SEL	
0	25MHz crystal input
1	100MHz differential input



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Size: Custom	Document Description: Clock Gen-IDT6V41506
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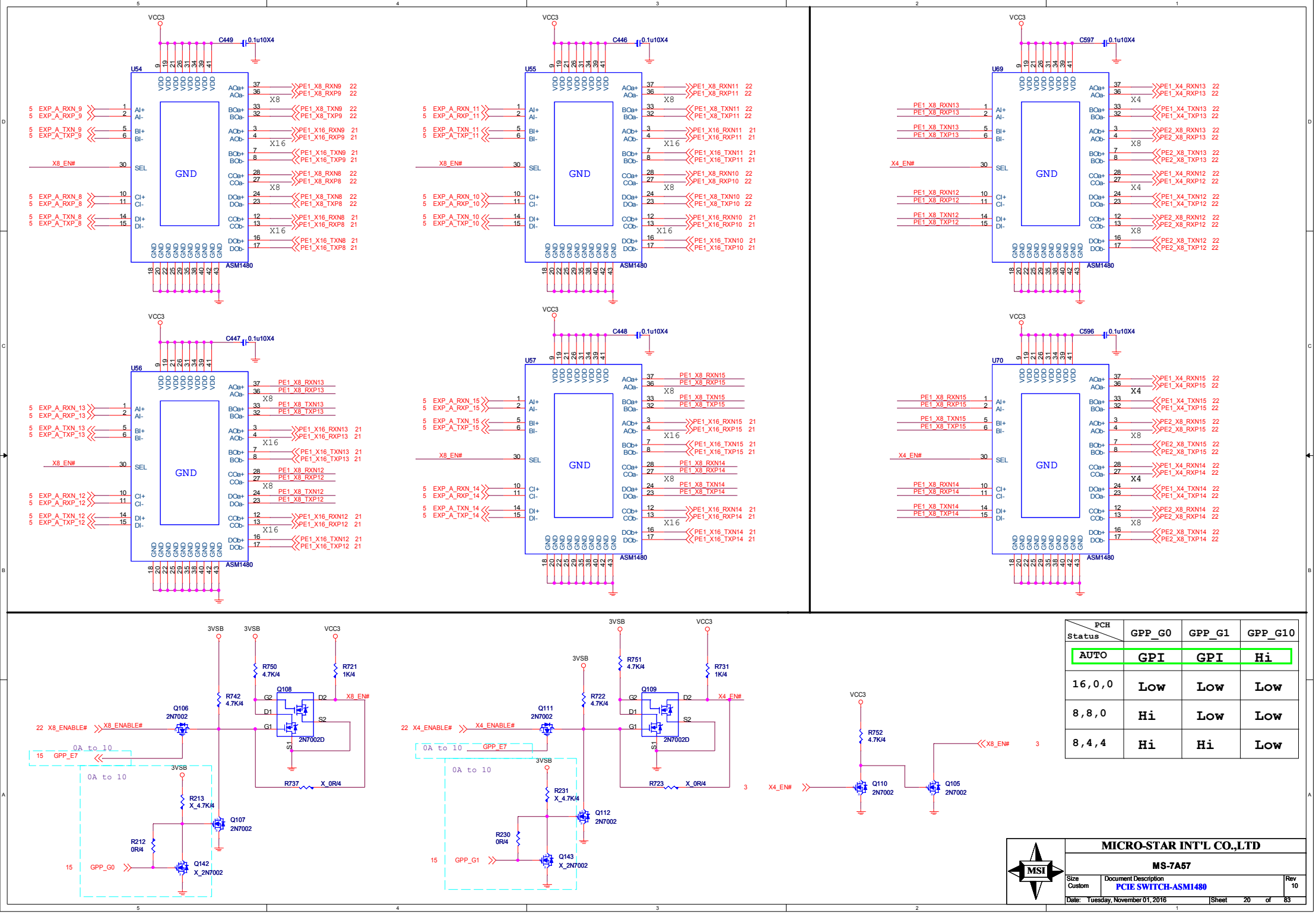

PCH / Status	GPP_G0	GPP_G1	GPP_G10
AUTO	GPI	GPI	Hi
16,0,0	Low	Low	Low
8,8,0	Hi	Low	Low
8,4,4	Hi	Hi	Low

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Size: Custom | Document Description: PCIE SWITCH-ASM1480 | Rev: 10

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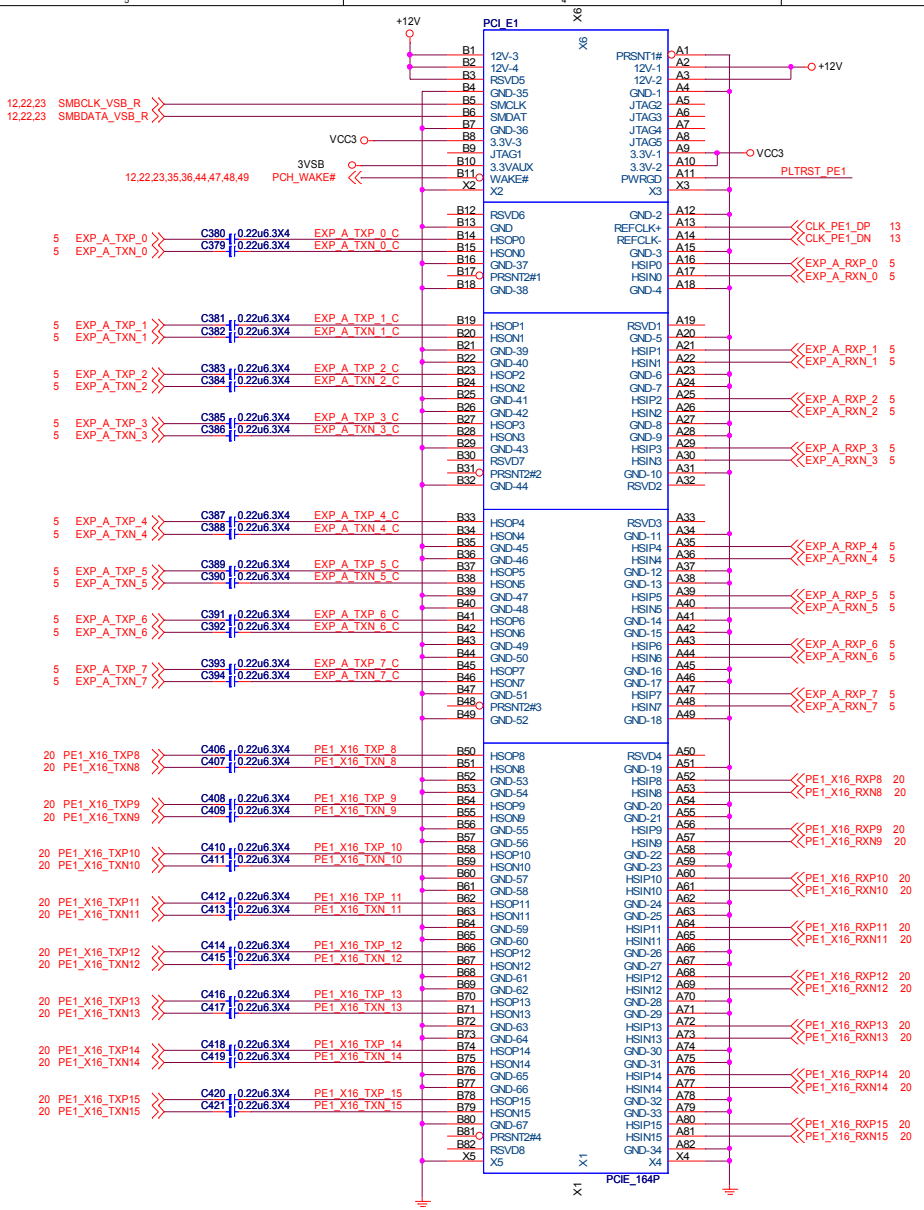

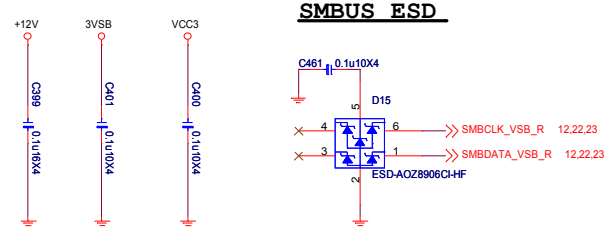

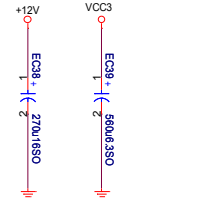

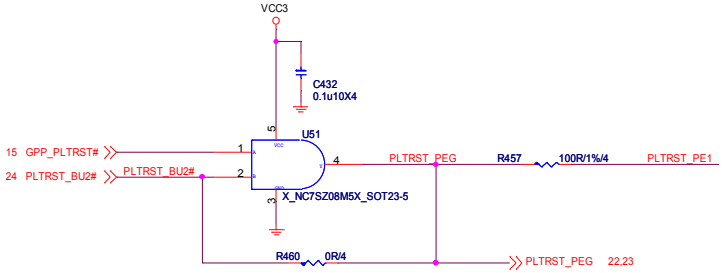

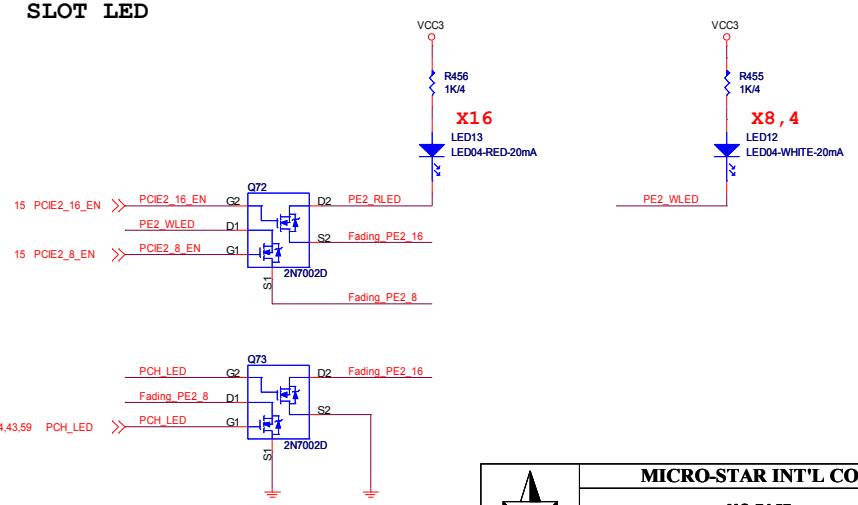

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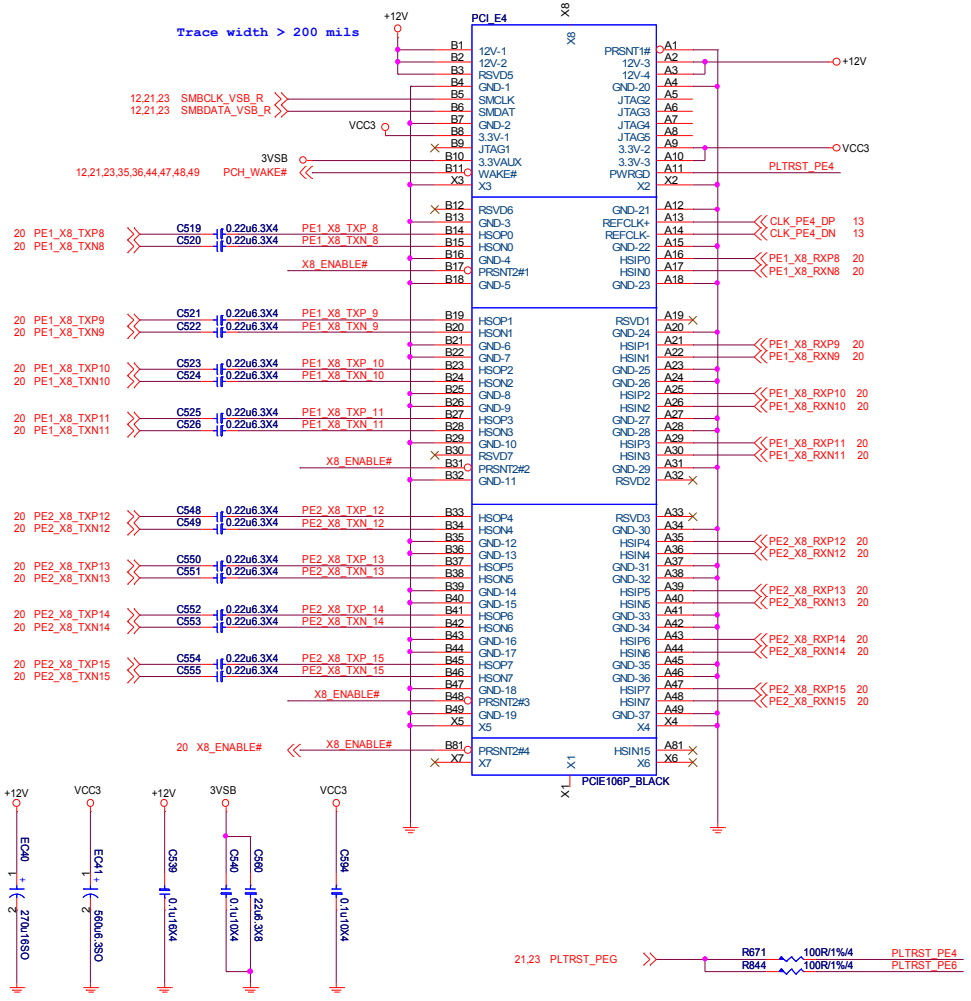
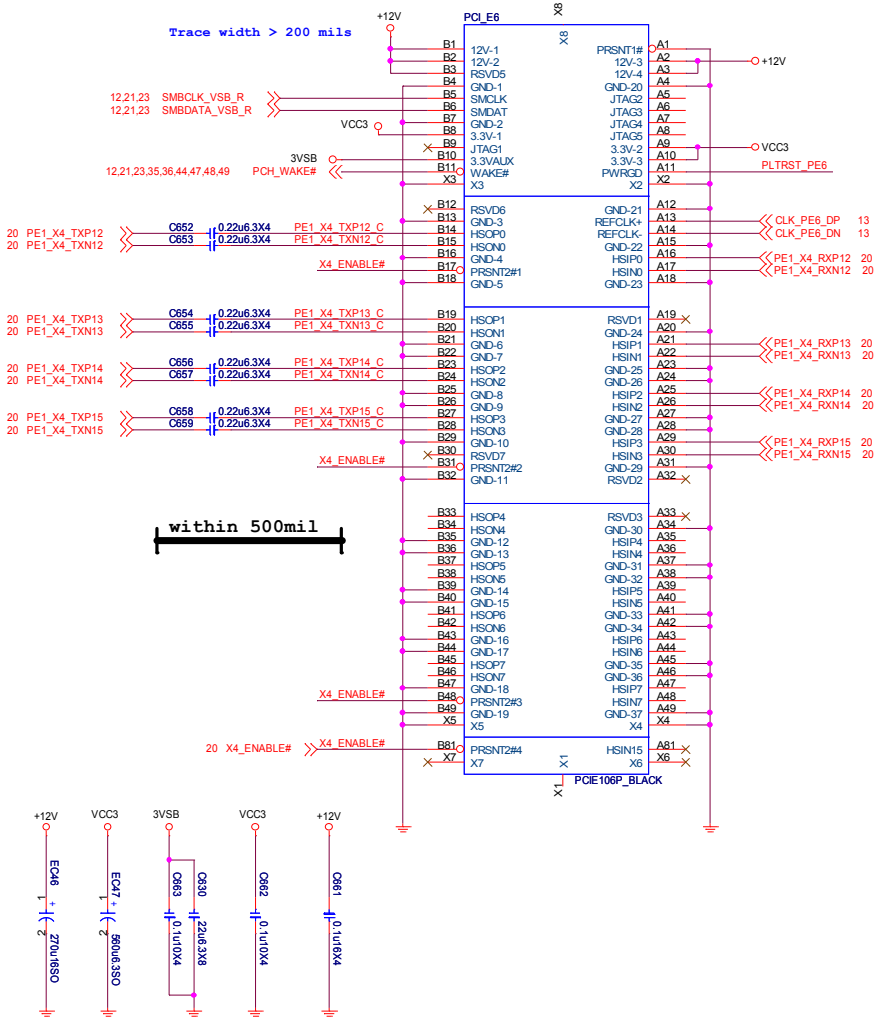
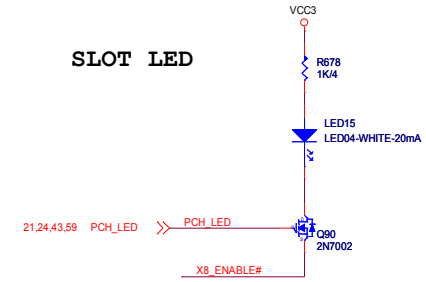
PCI_Express X8 Slot
(Share with PCI_E x16 Slots)



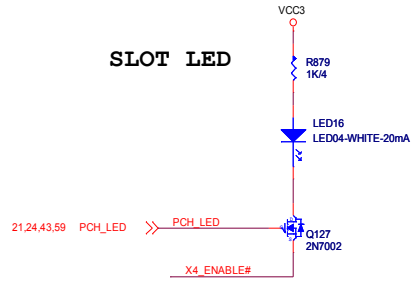
PCI_Express X4 Slot(by CPU)



SLOT LED



SLOT LED



MICRO-STAR INT'L CO.,LTD

MS-7A57

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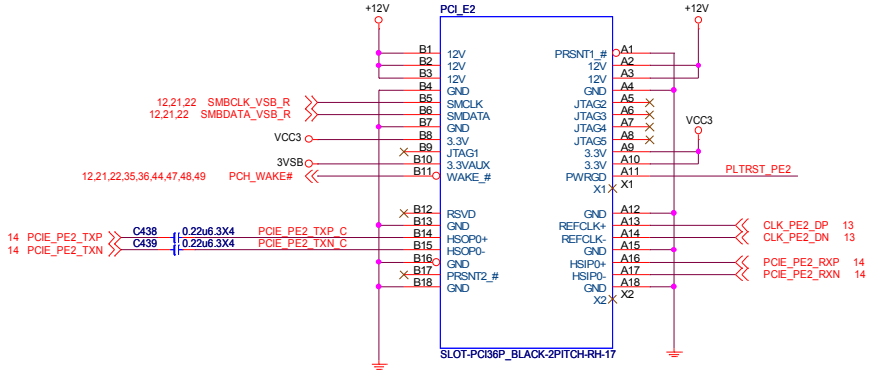
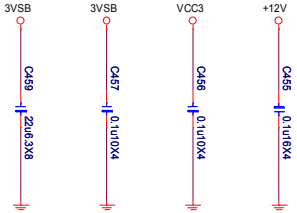
Custom	PCIE SLOT-CPU (X8)(X4)	10

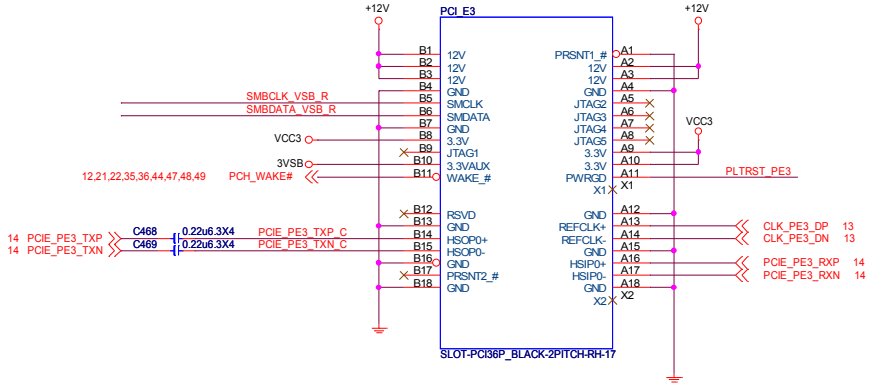
Date: Tuesday, November 01, 2016 Sheet 22 of 83

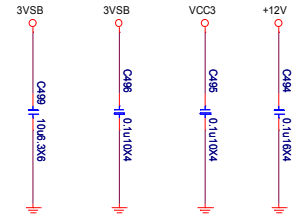
PCH PCIE X1 Slot

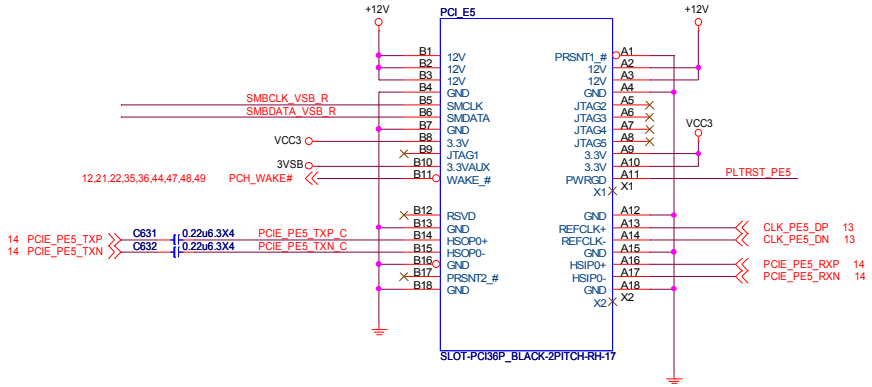
12V - 2.1A
VCC3 - 3A
3VSBV - 375mA

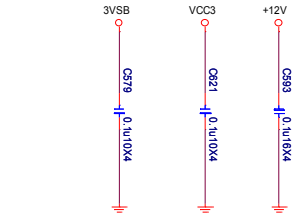












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Size: Custom
Document Description: PCIE SLOT-PCH (X1)
Rev: 10
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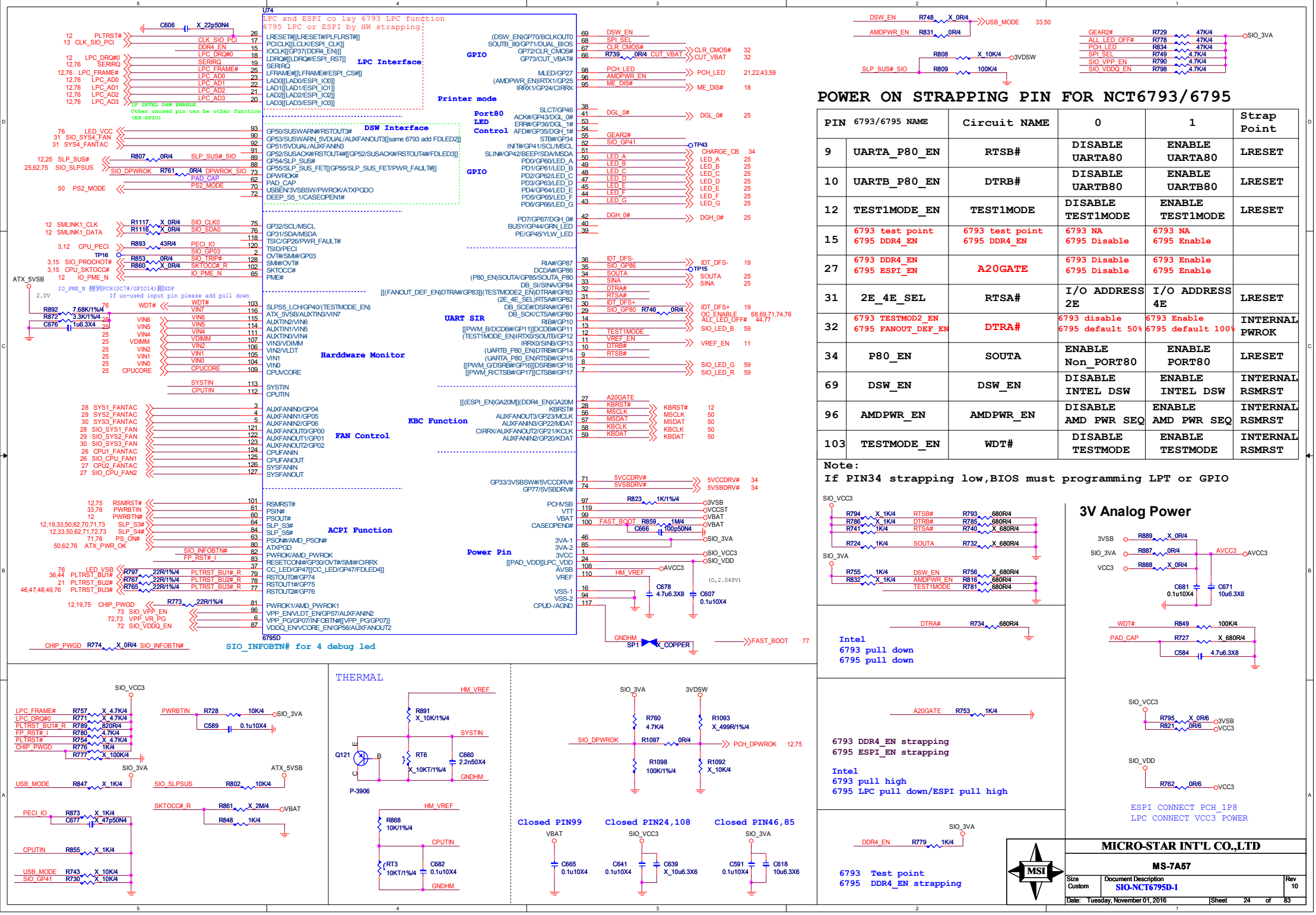

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

Intel
6793 pull down
6795 pull down

6793 DDR4_EN strapping
6795 ESPI_EN strapping

Intel
6793 pull high
6795 LPC pull down/ESPI pull high

6793 Test point
6795 DDR4_EN strapping

3V Analog Power

ESPI CONNECT PCH_1P8
LPC CONNECT VCC3 POWER

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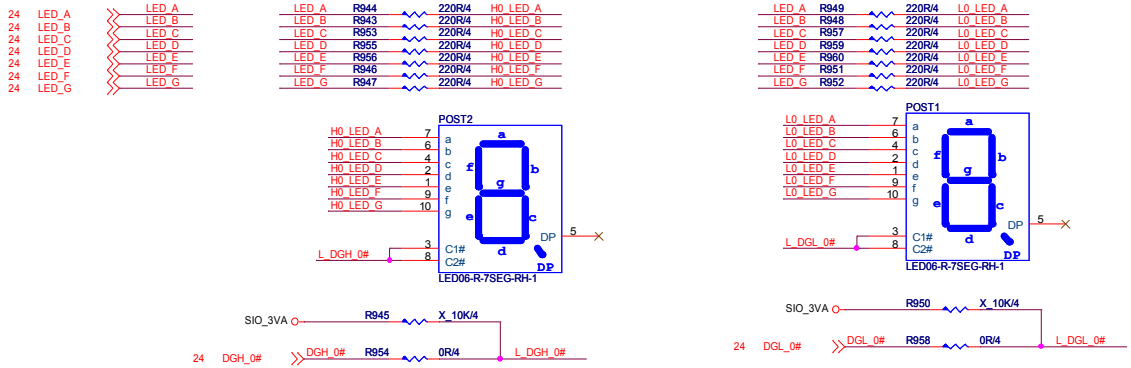
COM Port for BIOS Debug

DEBUG LED

Placement一定要對
(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)

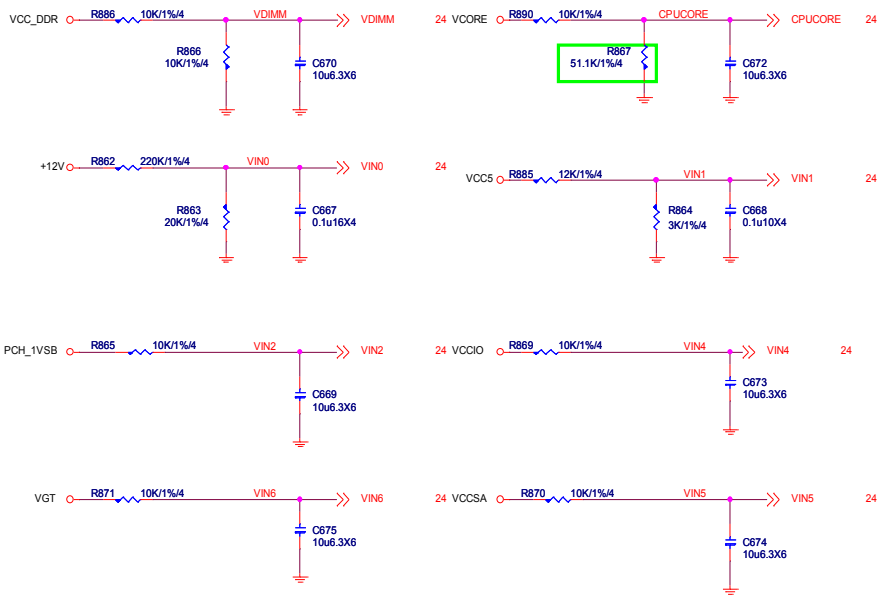
Debug LED OFF BIOS control



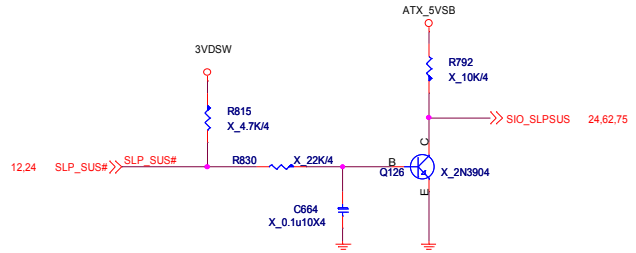
Ver 3.0
Remove Post3,Post4

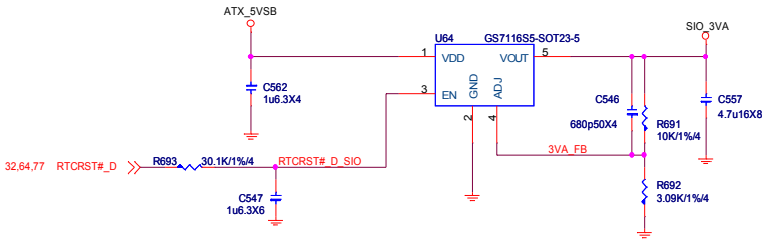
HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect



SLP_SUS Co-lay circuit





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Size: Custom	Document Description: SIO-NCT6795D-2	Rev: 10
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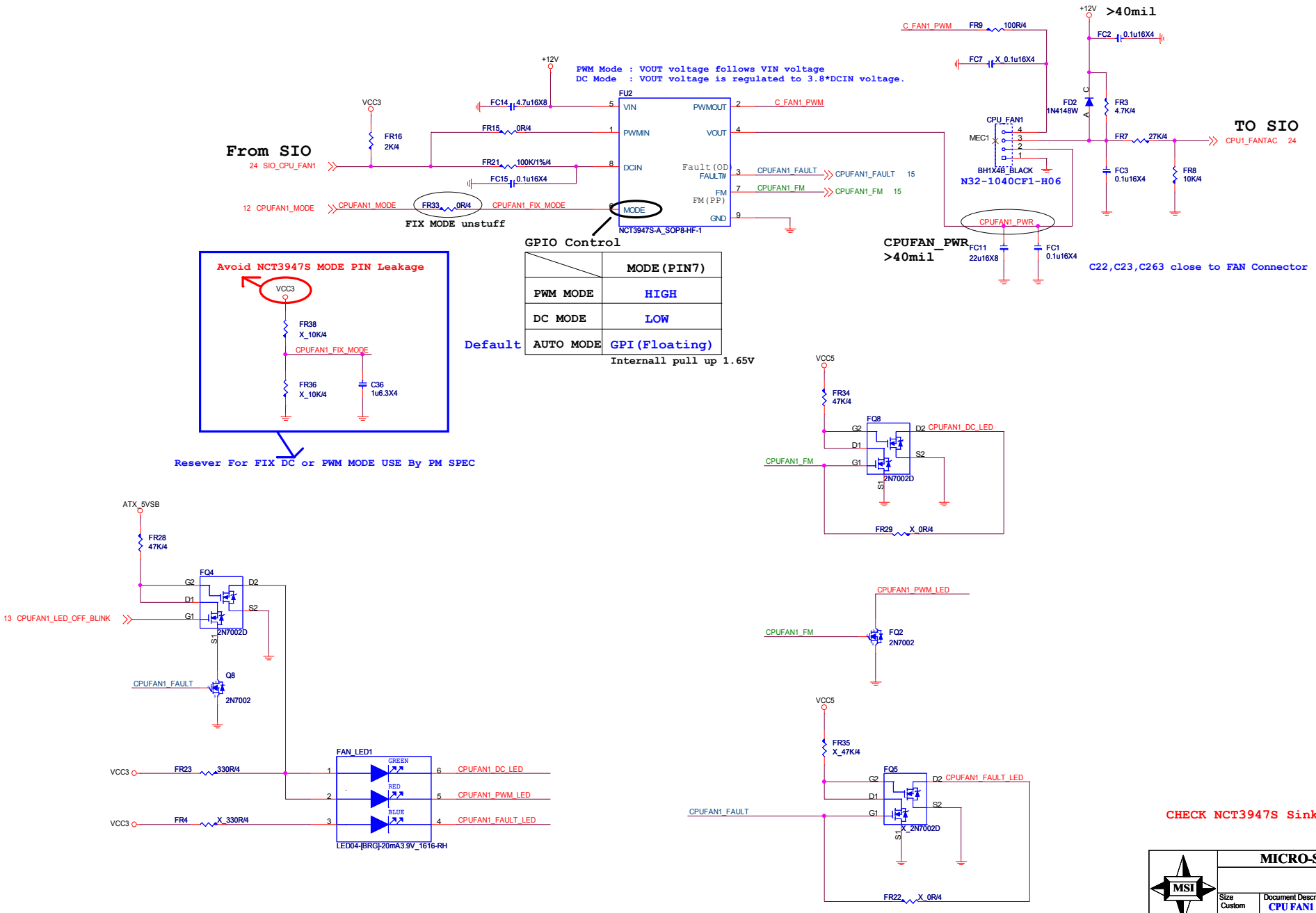
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

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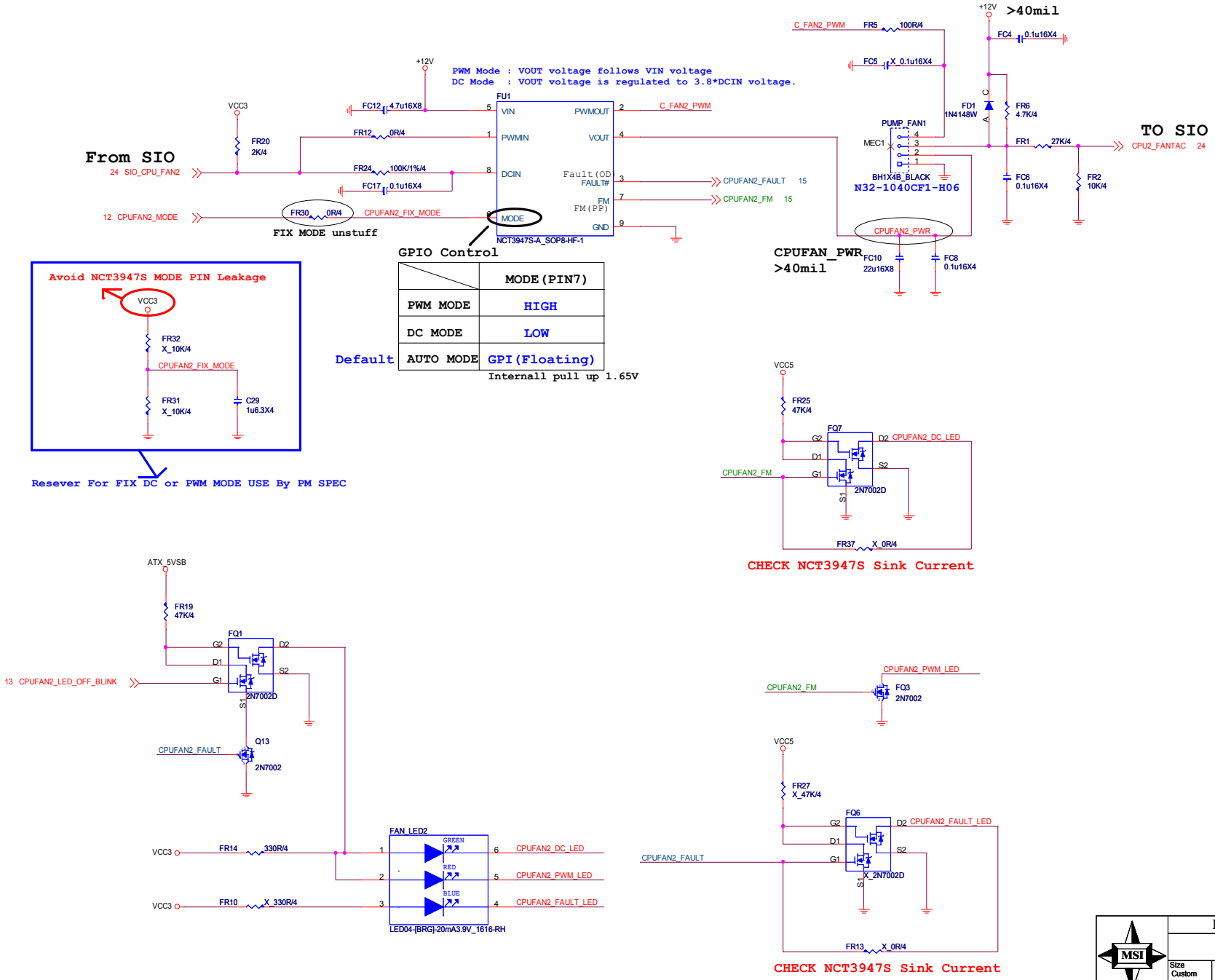
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD		
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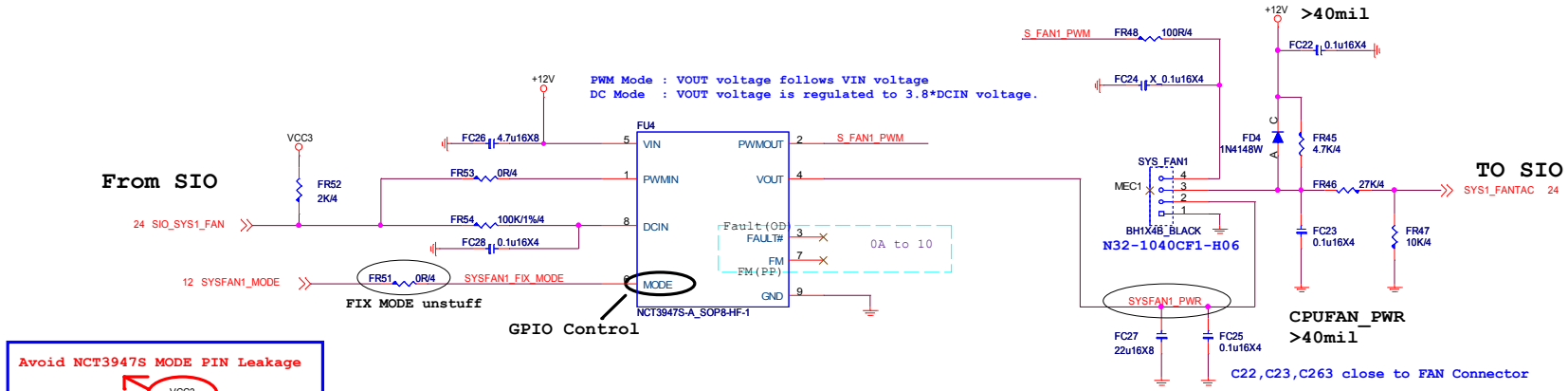
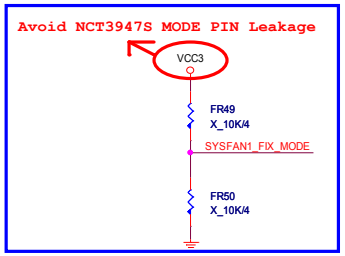
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE





Resever For FIX DC or PWM MODE USE By PM SPEC

GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V

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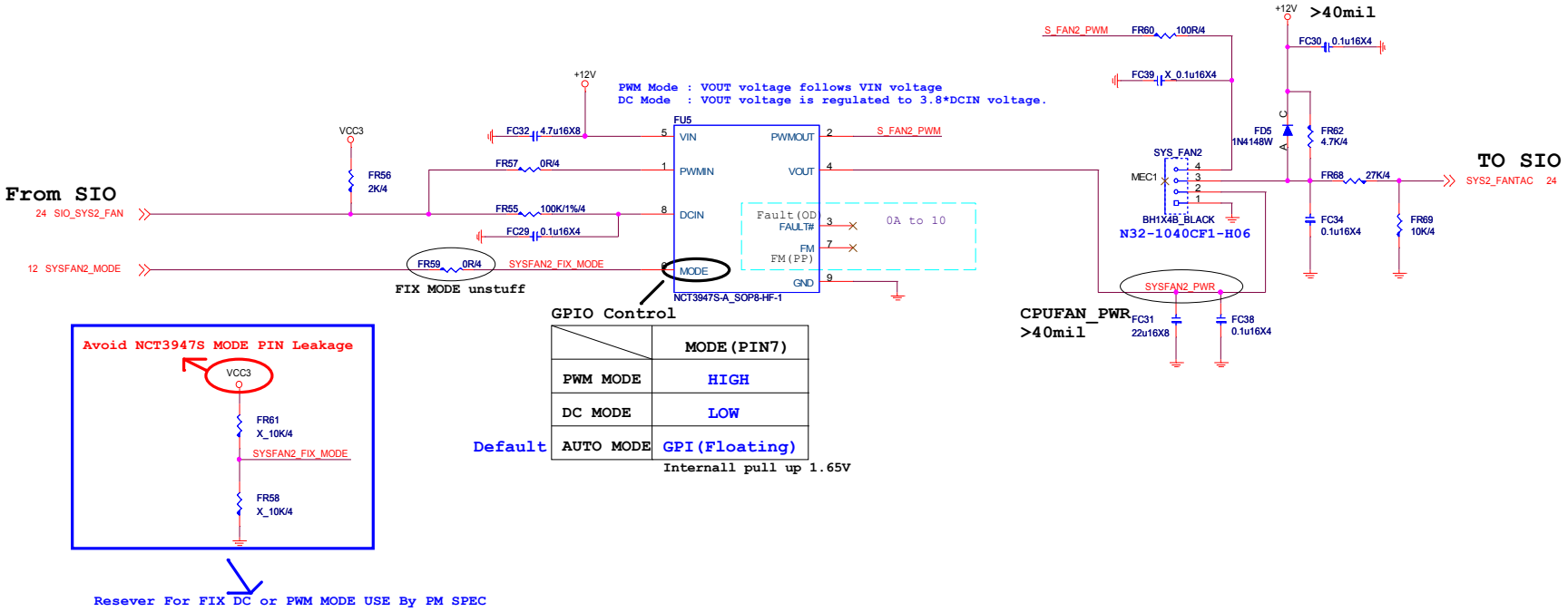
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SYSTEM FAN2	10

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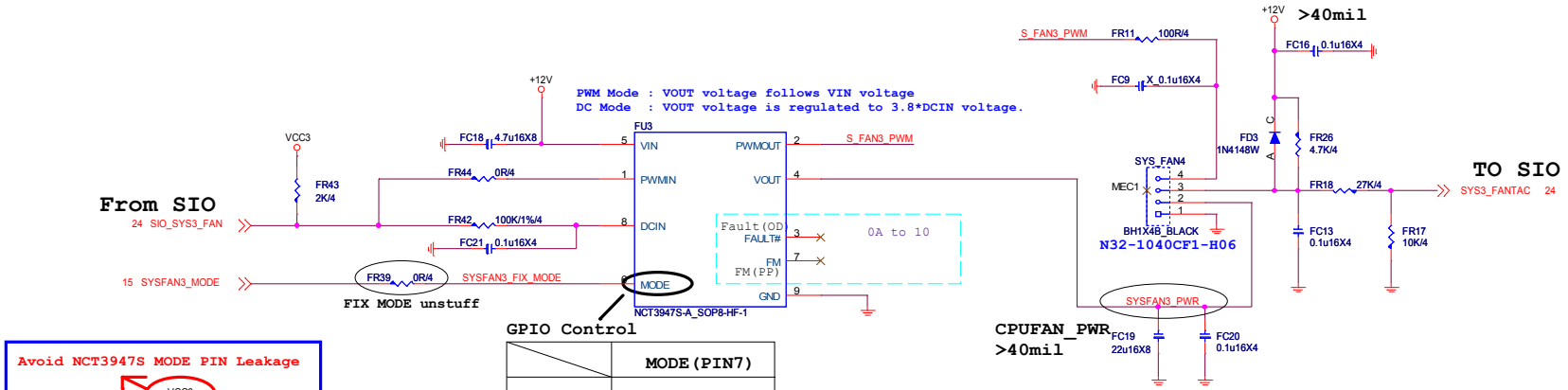
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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Size: Custom | Document Description: SYSTEM FAN3 | Rev: 10

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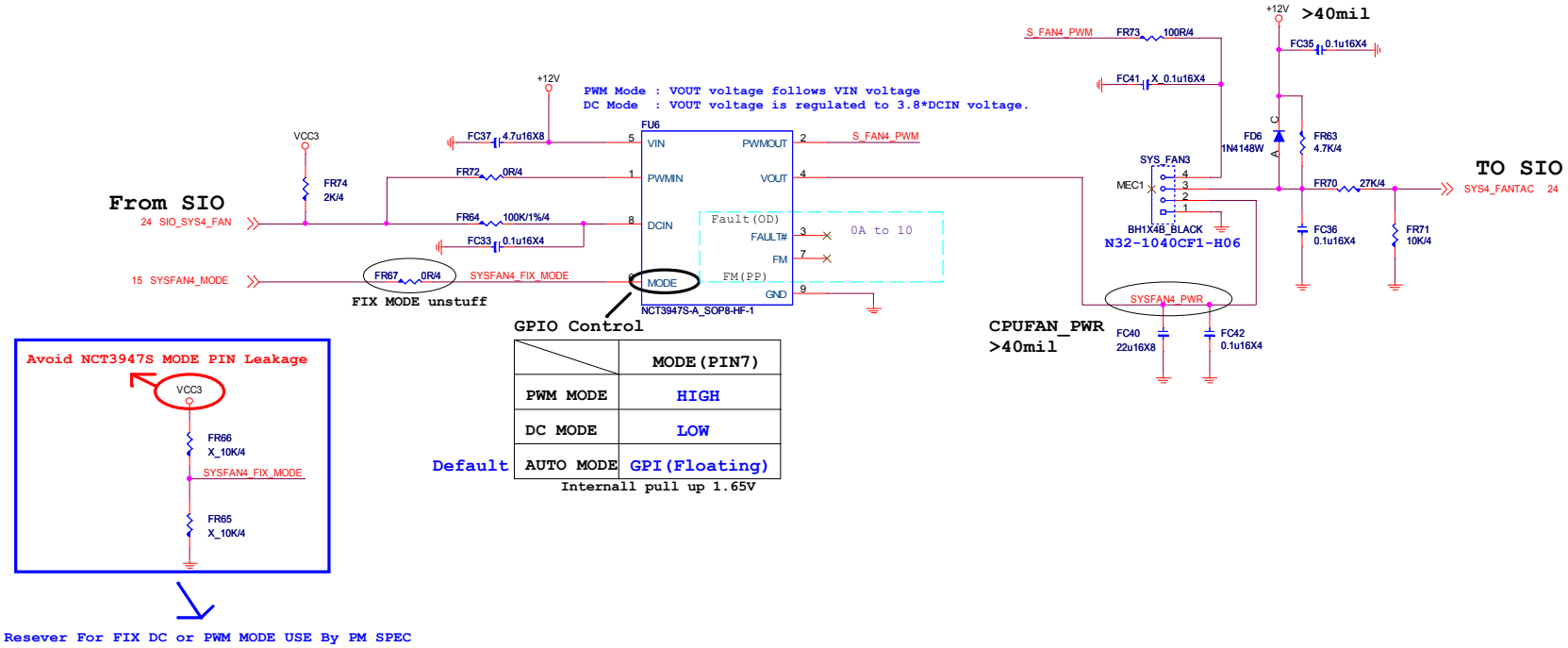
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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MS-7A57

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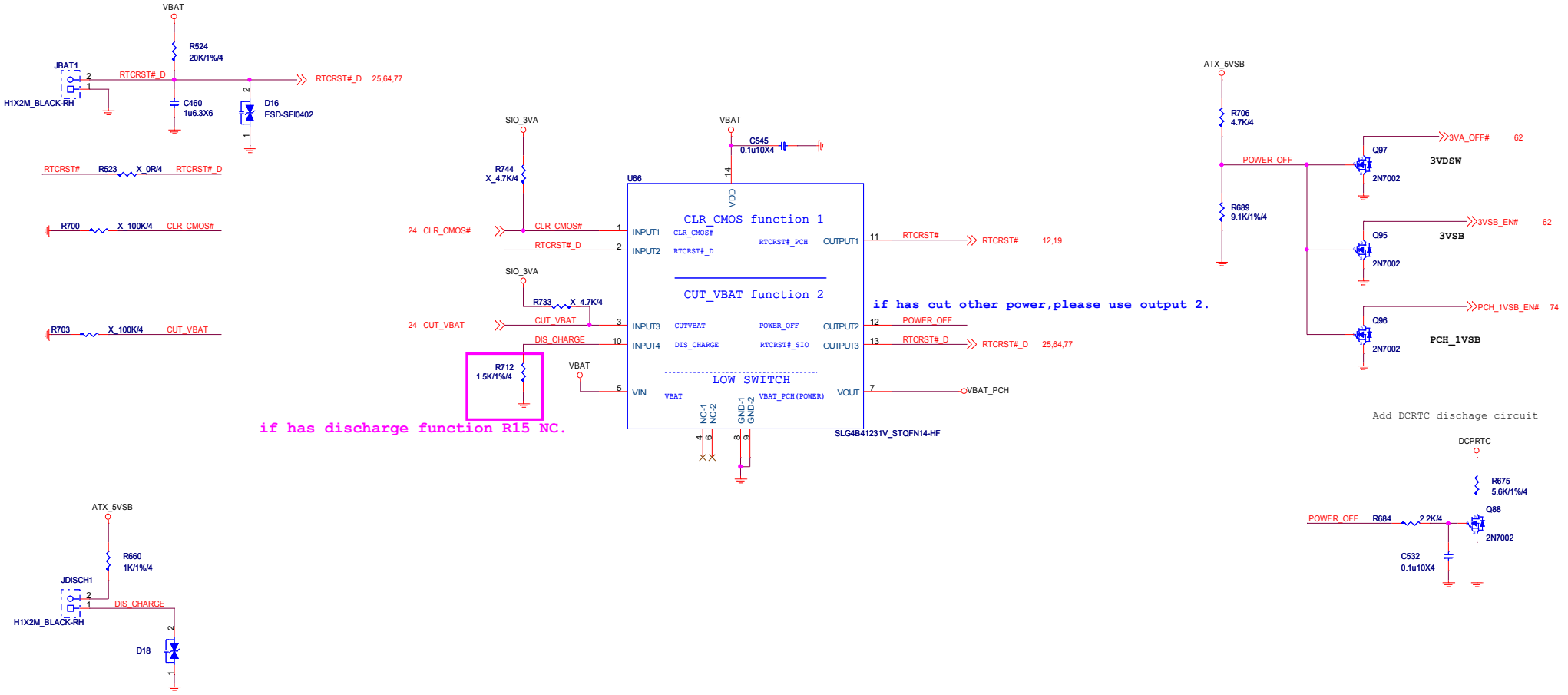
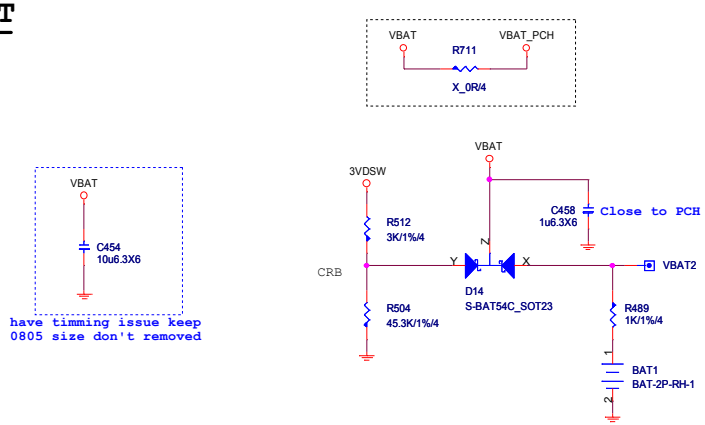
CUT VBAT



VBAT



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Size: Custom	Document Description: CLR COMS/CUT VBAT	Rev: 10
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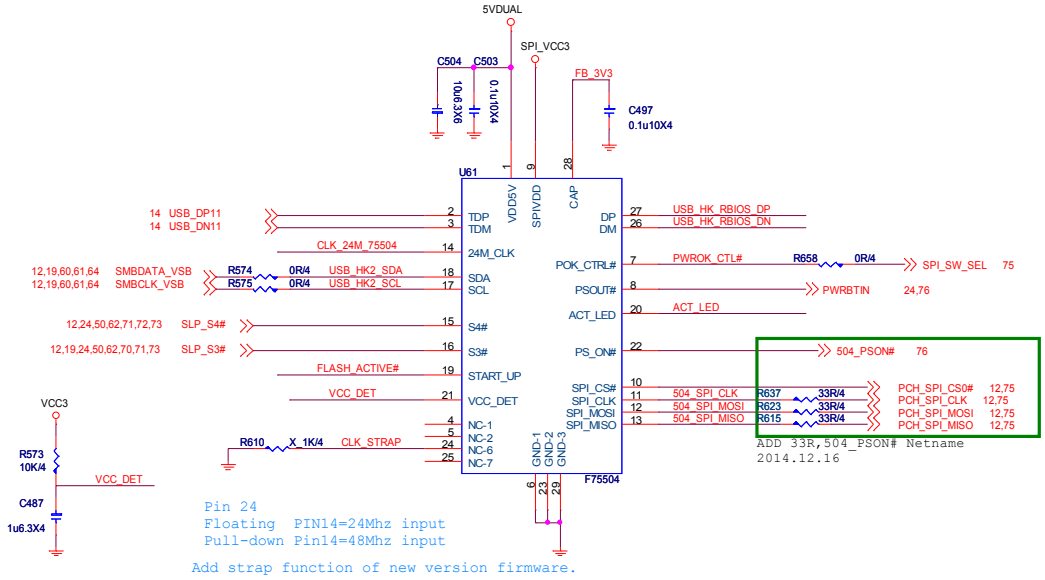
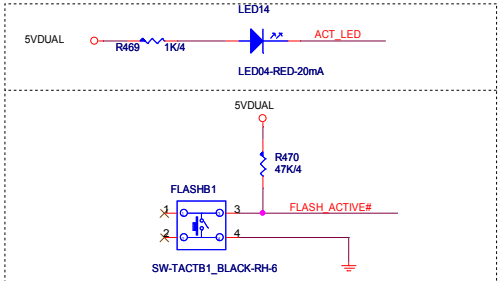
Host USB connector



ADD 33R,504_PSON# Netname
2014.12.16

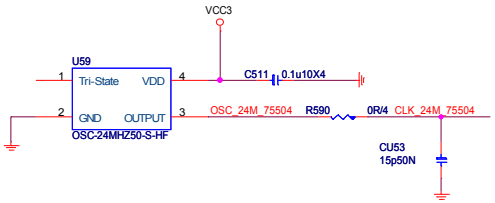
Pin 24
Floating PIN14=24Mhz input
Pull-down Pin14=48Mhz input

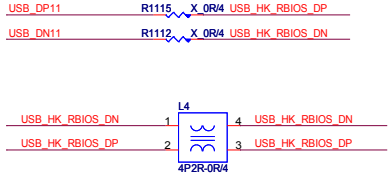
Add strap function of new version firmware.



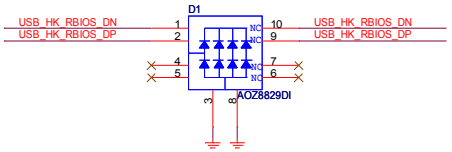
Reserved for when F75501 Hotkey device fail use

* All close to Front IO side

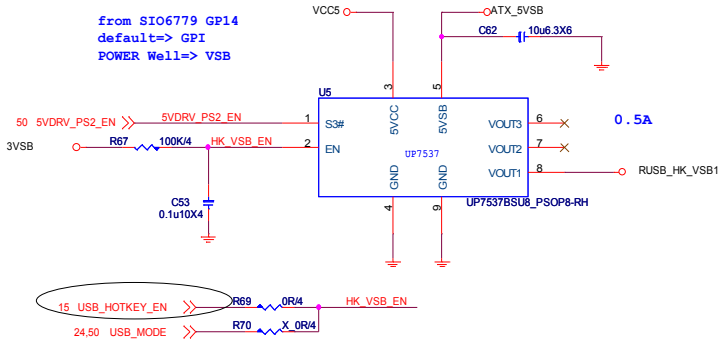


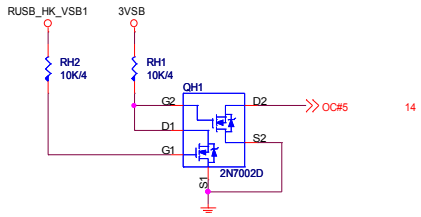


0B add For EMI
2014.12.26



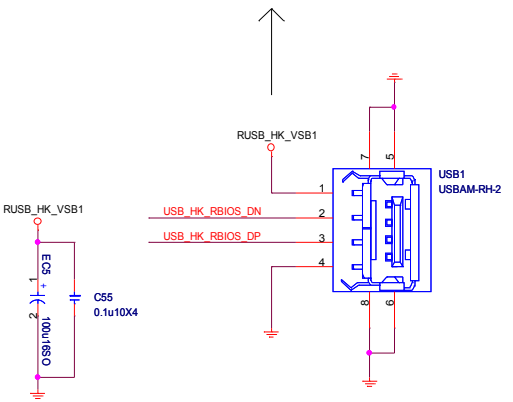
ESD close to connector.
(use usb3.0 ESD for eye diagram)

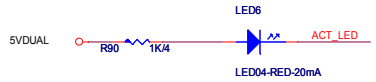




OC# signal connect to
SB OC pin.

USB Connector power come from UP7537
provide(USB Hotkey Connector same)





LED Close Connector

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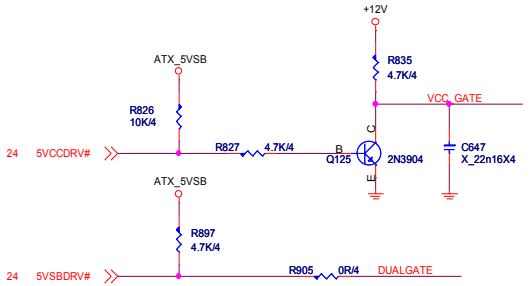
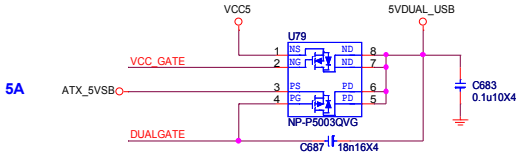
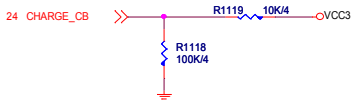
5VDUAL_USB



3~4A

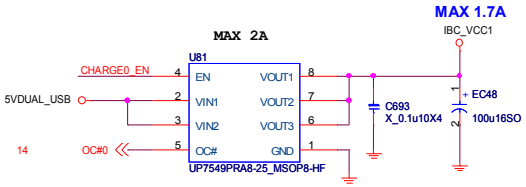


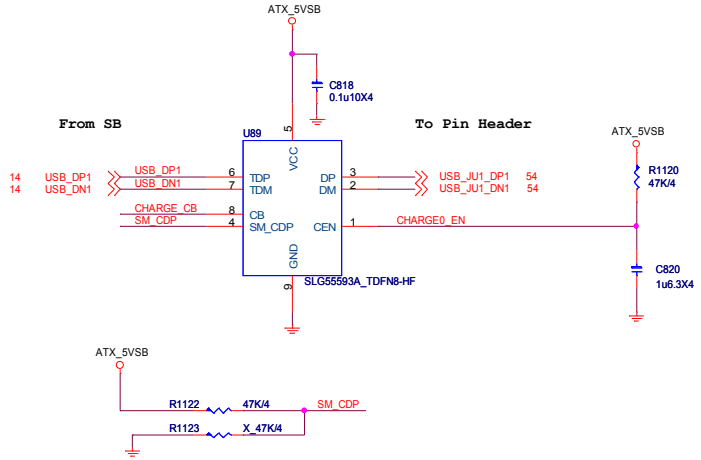
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



USB POWER PORT 0 For USB Charging

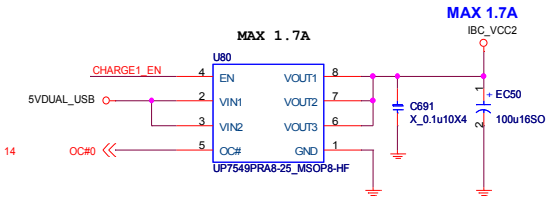
MAX 1.7A

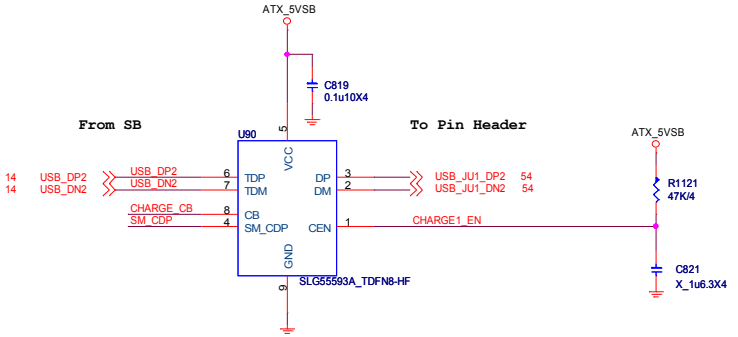




USB POWER PORT 1 For USB Charging

MAX 1.7A





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Size: Custom	Document Description: USB CHARGE_SLG55593A	Rev: 10
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Use 0.22uF cap for GEN3 , Gen2 use 0.1uf by Upstream SPEC

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

USB SS (80Ohm-Diff)
USB HS (90Ohm-Diff)

Power Consumption

	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP
ASM1042AE	95mA	300mA	65mA	9.5mA	NA	852.975(mW)

UU4A ASM2142 — ASM2142-RH

PPON_X Internal Pull-up to VCC3

OCI_X Internal Pull-up to SUS

RX/TX Internal Pull-up

SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

Reset control for ASM2142 only.

UU4B ASM2142 — ASM2142-RH

ASM1142/ASM1042 RU32 O RU29 X
ASM2142 RU32 X RU29 O

ASM1042AE RU67 O RU41 X
ASM2142/ASM1142 RU67 X RU41 O

ASM2142 RU52 X RU53 O
ASM1142/ASM1042 RU52 O RU53 X

UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8
X0/XI (95hm-Diff,Spacing 30mil)

ASM1042AE change to 0.1uF cap

ASM1142 1.2 VCC Power

UU8 MP2143DJ

ASM1142 RU12/RU10 100K/100K_1.2V
ASM2142 RU12/RU10 196K/261K_1.05V

ASM1142 1.2 VSB Power

UU6 GS7116S5-SOT23-5

ASM1142 RU57 19.6K_1.2V
ASM2142 RU57 31.6K_1.05V

CUT POWER

U50 MP5077GG_QFN12-HF

EN:1.3V~1.7V

ASM2142 2.5V Power

UU5 GS7116S5-SOT23-5

ASM1142/ASM1042AE unstuff
ASM2142 stuff

EEPROM

UU7 MX25L1006E

ASM1142 M31-2551222-M24(512K bit)
ASM2142 M31-25L1022-M24(1M bit)

MICRO-STAR INT'L CO.,LTD

MS-7A57

Size: Custom | Document Description: USB3.1-ASM1142AE-Front | Rev: 10

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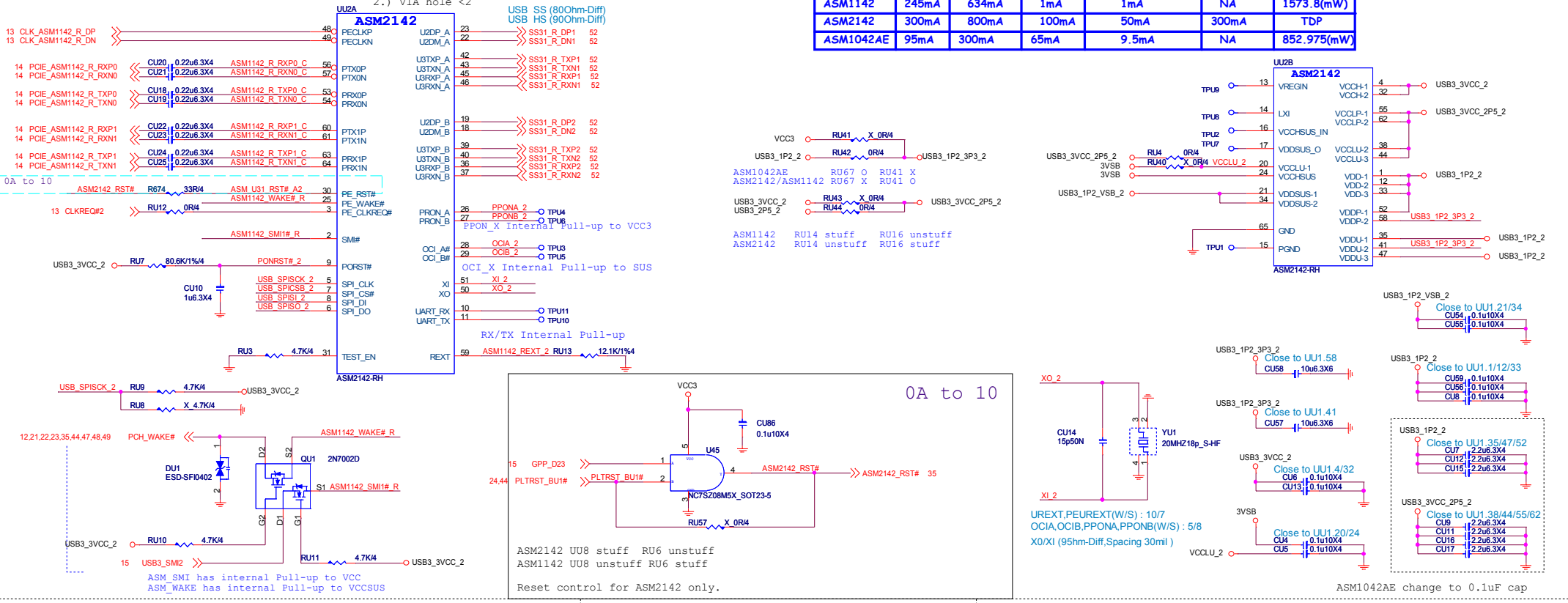
Layout Guide:

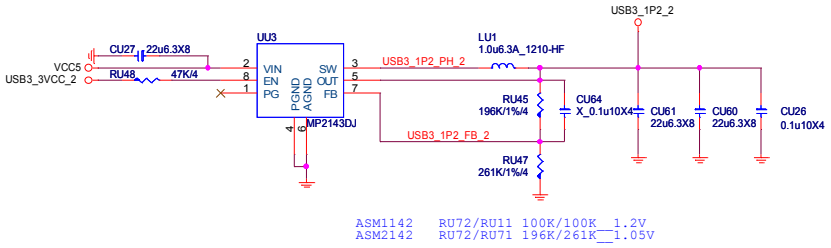
1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

Power Consumption

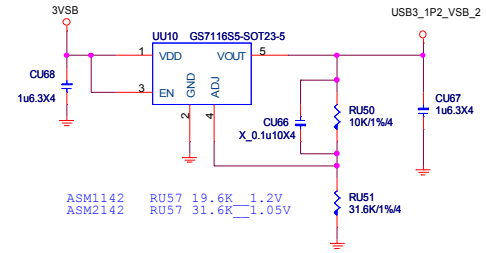
	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP
ASM1042AE	95mA	300mA	65mA	9.5mA	NA	852.975(mW)



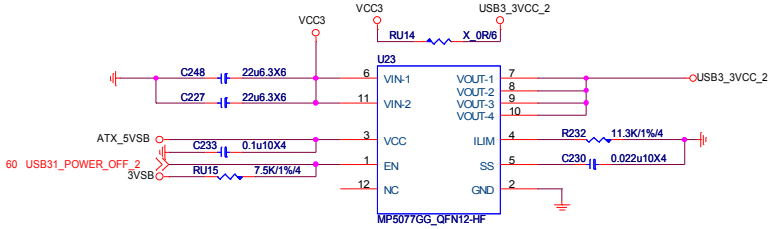
ASM1142 1.2 VCC Power



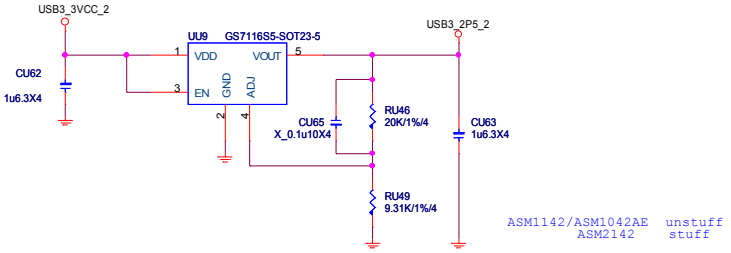
ASM1142 1.2 VSB Power



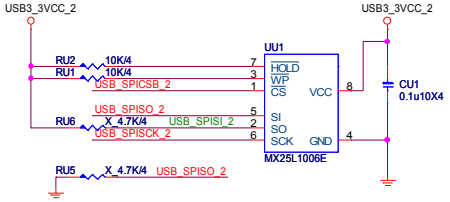
CUT POWER



ASM2142 2.5V Power



EEPROM



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Size: Custom	Document Description: USB3.1-ASM1142AE-Rear
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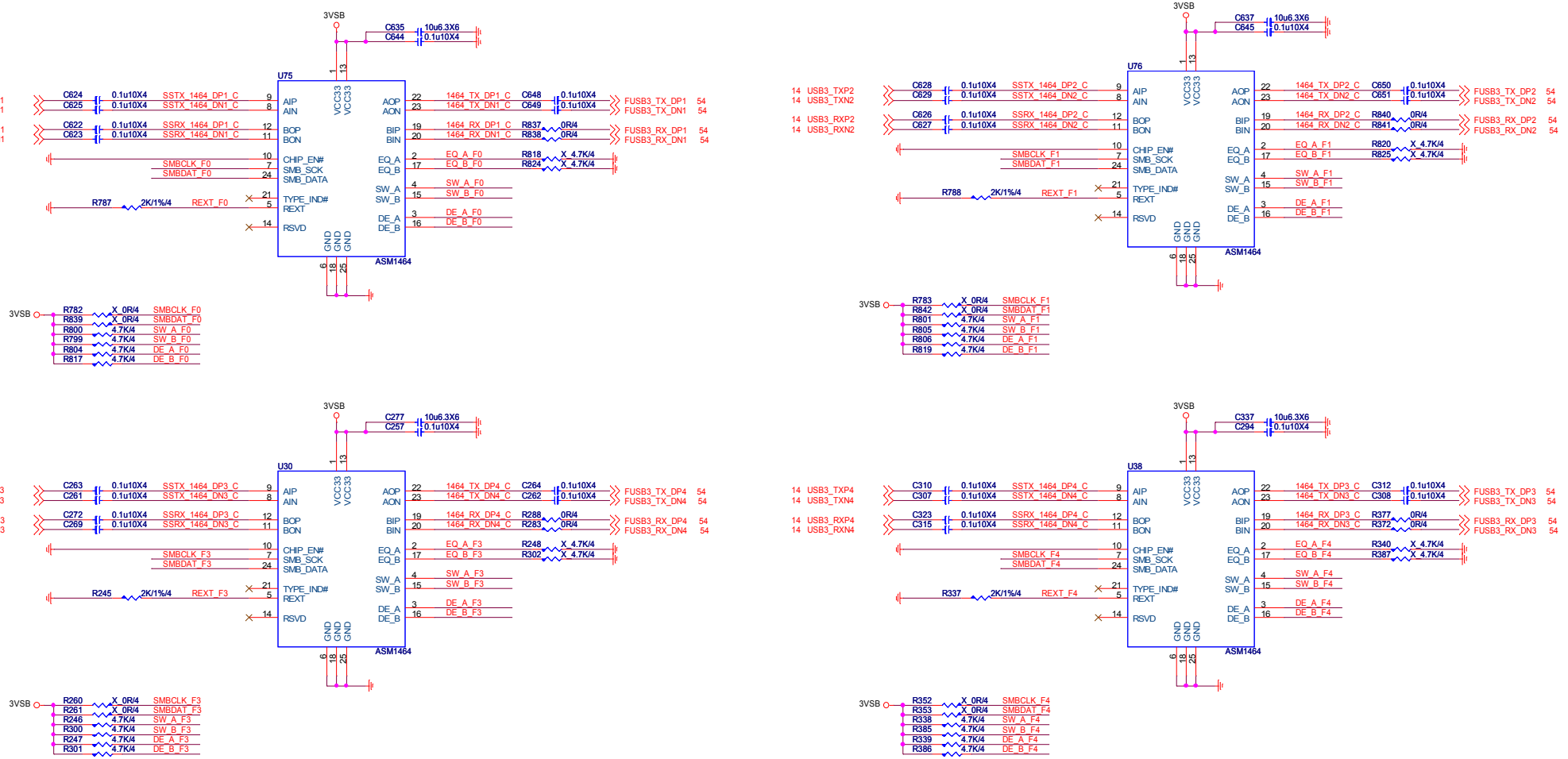

MICRO-STAR INT'L CO.,LTD

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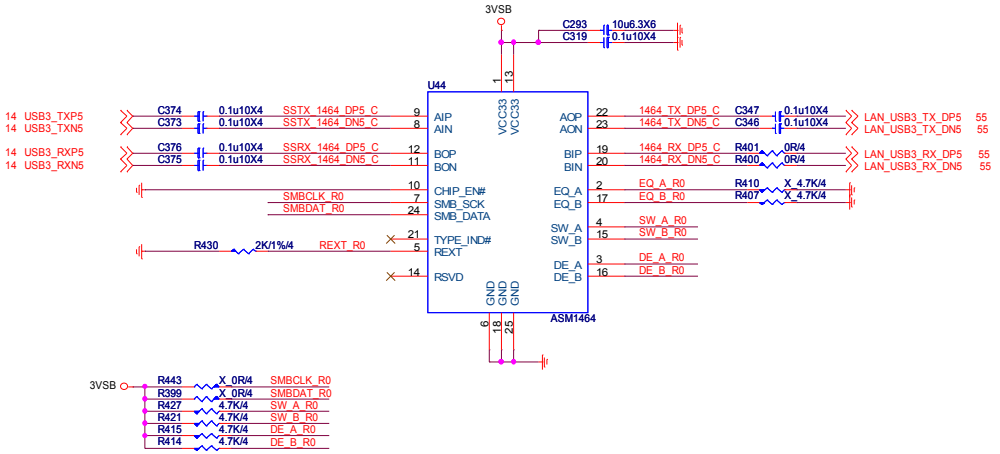

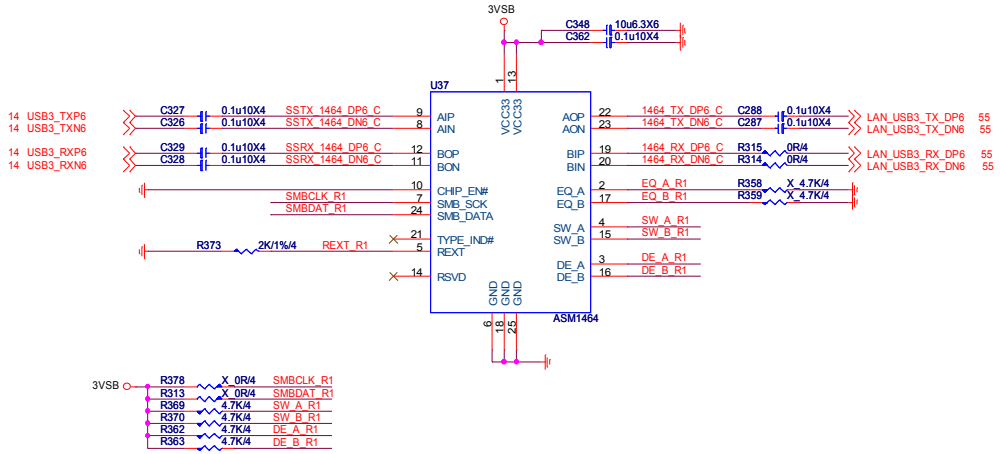

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	USB Redrive-Rear	10

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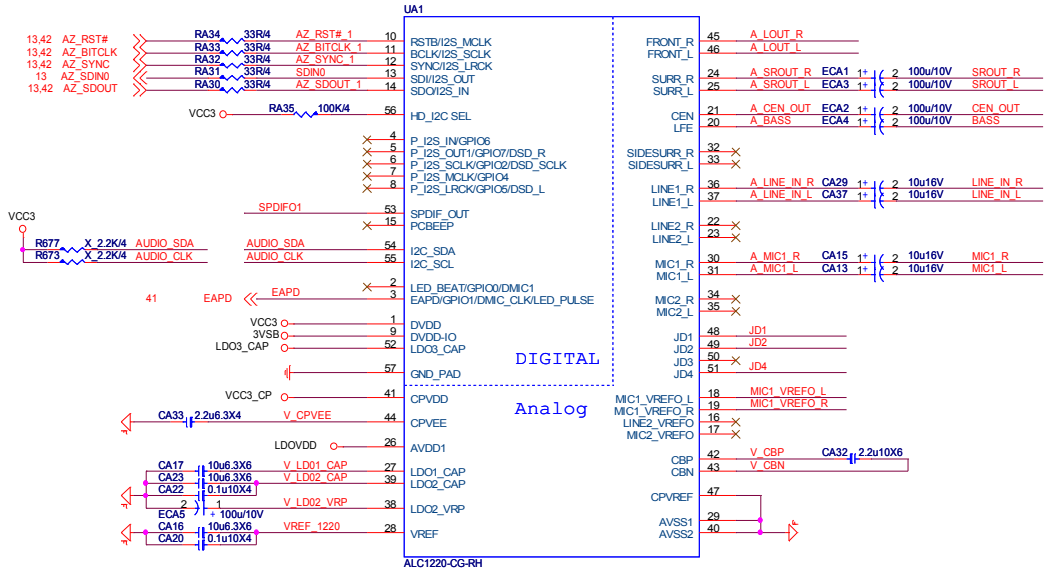
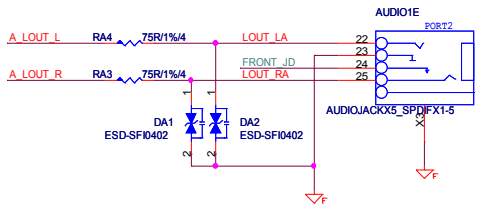
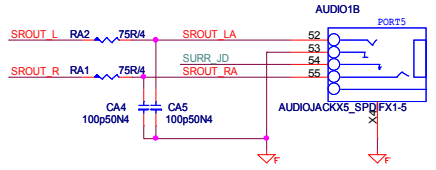
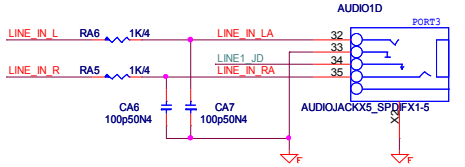
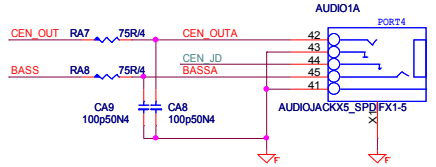
ALC1220

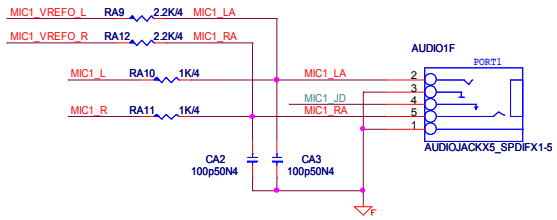


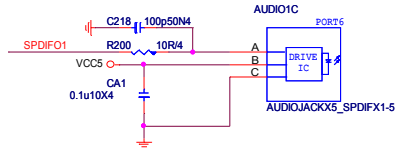


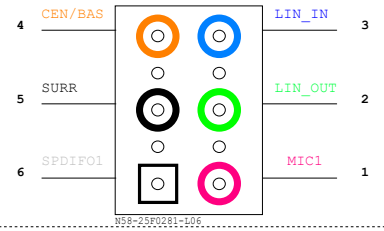


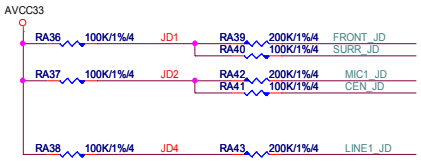


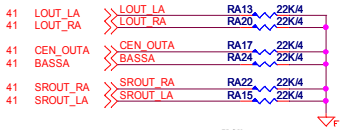


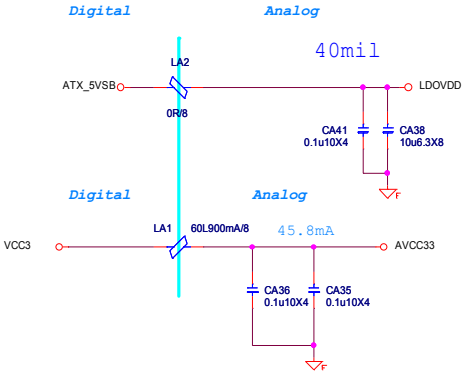




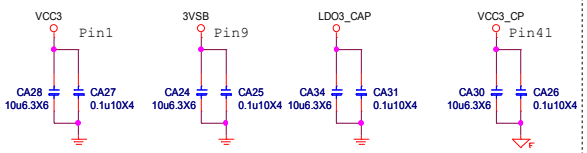


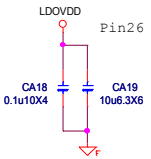




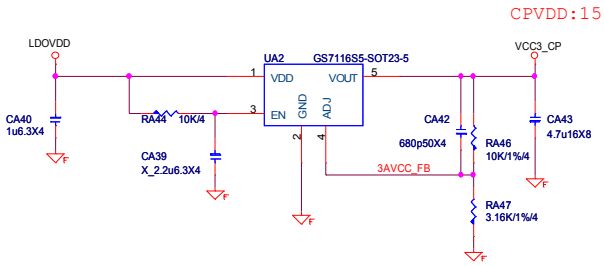


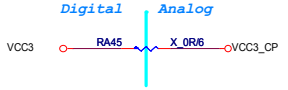
Closed Codec



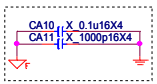


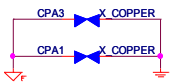
CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V





EMI





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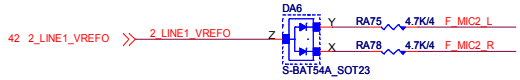
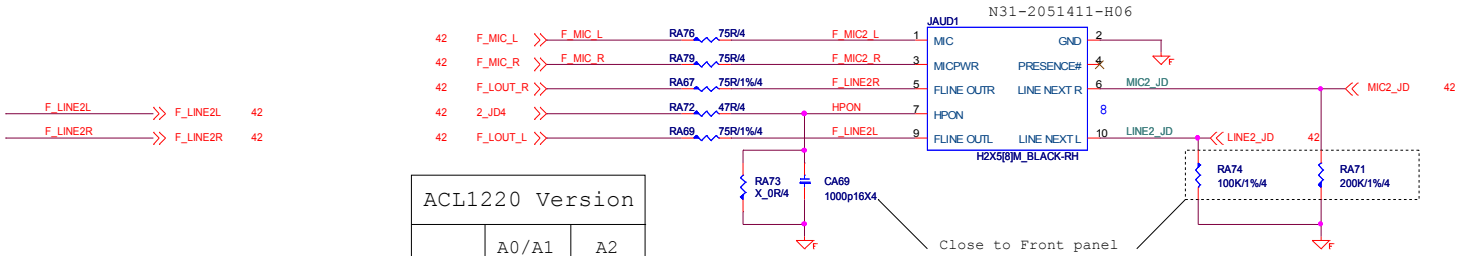
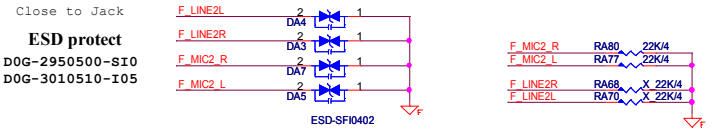


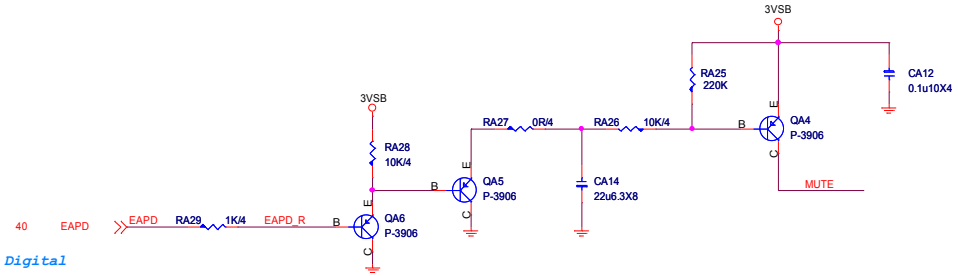


ACL1220 Version		
	A0/A1	A2
RA72	X	O
RA73	O	X
CA69	X	O
RA74	X	O
RA71	X	O

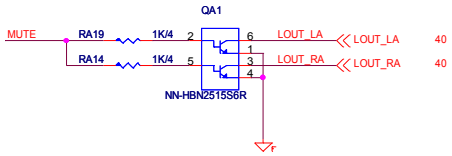


Rear Line OUT De-POP circuit

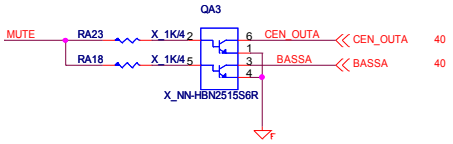
(De-pop circuit for Rear Line out)

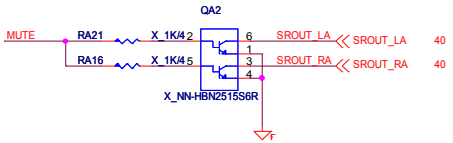


Analog



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)





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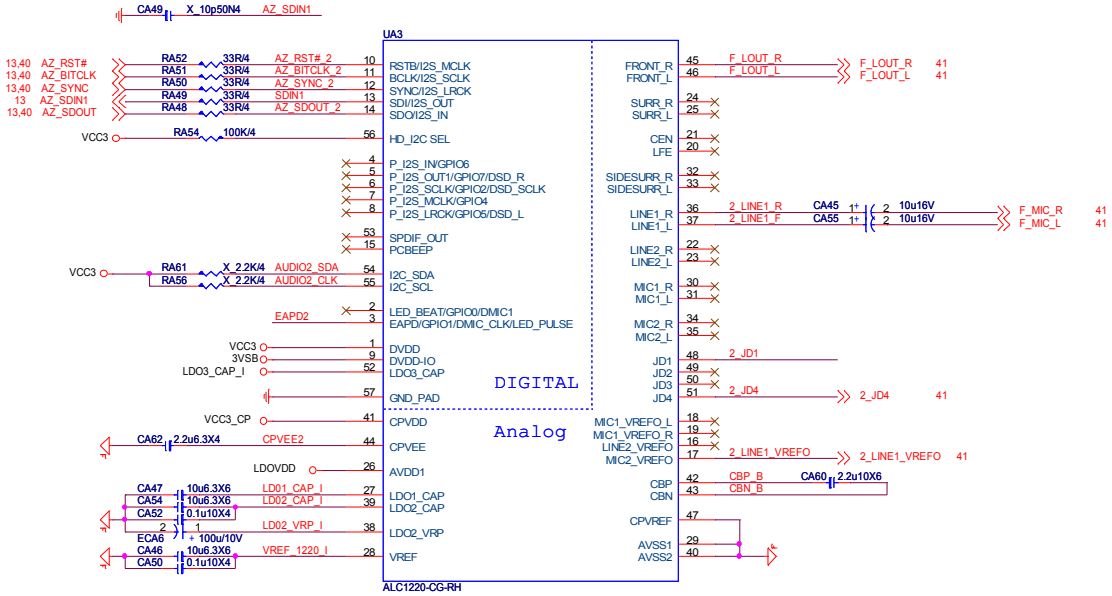
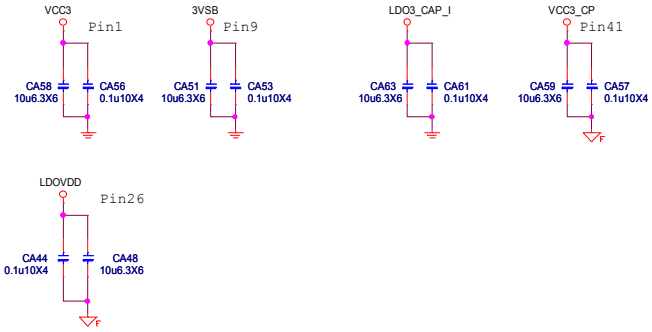
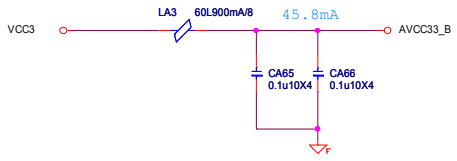
ALC1220



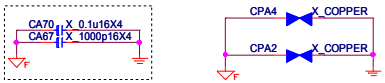
ACL1220 Version		
	A0/A1	A2
RA60	O	X
RA57	O	X
RA58	O	X





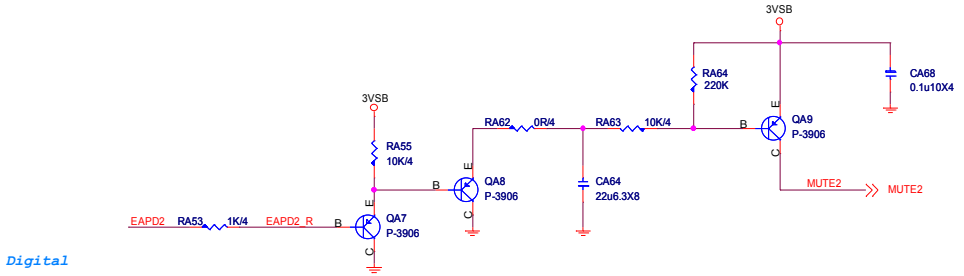
Closed Codec

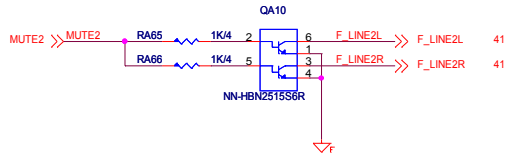
EMI



Front Header De-POP circuit

(De-pop circuit for Front Headphone)





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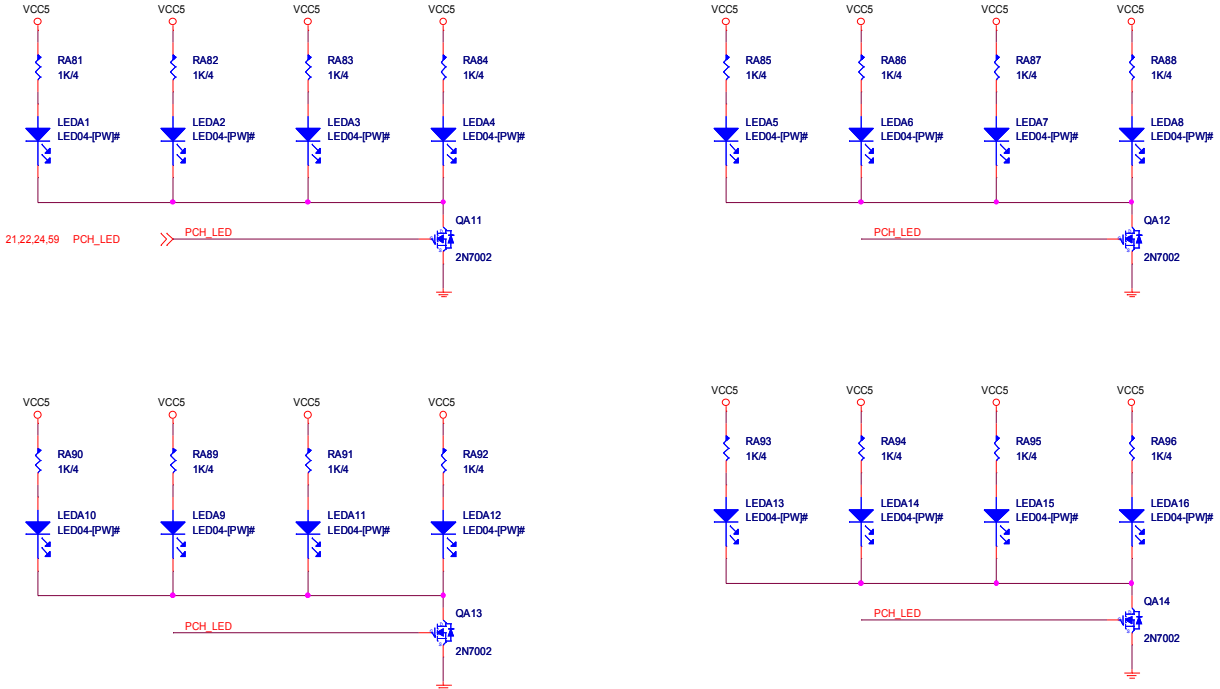
Audio moat is transparent and width 40mil



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E2500 GIGA LAN

151.6mA

3VSB VDD33 CP8 X_COPPER CL21 CL23 CL12 CL14 CL13

VDD33 AVDD33 CP15 X_COPPER CL26 CL27 Close to Pin16

place near pin <200mil

AVDDH 9 9 22 CL7 CL8 CL10

place near pin <200mil

DVDDL CL20 CL22 Close to Pin37

place near pin <200mil

AVDDL 6 6 13 19 31 CL30 CL31 CL28 CL29 CL34

place near pin <200mil

PIN2:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#,

E2400:B06-E24000C-R54
E2500:B06-E25000C-R54

UL1 E2500

PCIE interface: PCIE_LAN_TXP PCIE_LAN_TXN PCIE_LAN_TXP_C PCIE_LAN_TXN_C PCIE_LAN_RXP_C PCIE_LAN_RXN_C PCIE_LAN_RXP PCIE_LAN_RXN
CLK_LAN_DP CLK_LAN_DN REFCLK_P REFCLK_N WAKEn CLKREQn PCH_WAKE# CLKREQ#3
PLTRST_BU1# PLTRST_BU1#_LAN PERSTn RBIAS PPS
Media interface: TRXP0 TRXN0 TRXP1 TRXN1 TRXP2 TRXN2 TRXP3 TRXN3
Power: VDD33 AVDD33 LX DVDDL_REG AVDDL_REG AVDDL-1 AVDDL-2 AVDDL-3 AVDDL-4 AVDDH_REG AVDDH NC GND
Test: DEBUGMODE[0] TESTMODE[0] TESTMODE[1] TESTMODE[2]
LED: LED[0] LED[1] LED[2]
CLOCK: XTLI XTLO

DVDDL Close to pin40 CH-4.7u2A70mS-HF-1 CHOKE1 CL24 CL15 CL25 X_1000p10X
LX should be wider than 30 mils.

CP7 X_COPPER
L27 300L600mA-150
AVDDVCO CL32 CL33 CL35
near pin34 <200mil

Reserve for strap hi
RL10 RL9 RL7 X_10K/4
RL8 30K/4 VDD33
LAN_XTAL1 LAN_XTAL2 CL9 27p50N4 CL11 27p50N4 YL1 25MHZ18p

9 GND via

20141217 update
CHOKE1: L04-47A70E0-T19
AVL: L04-47A7870-C08
L04-47A7690-M26

L2:
L02-3018023-C08
L02-3018023-T19

160926 Modify Y1 to D04-1006700-F07
Main:D04-1006700-F07
AVL:D04-1000640-T16

note:

LED0:
1=High core voltage
0=Low core voltage

LED1:
1=SWR mode
0=LDO mode

LED2:
1=25MHz clock
0=48MHz clock

VDD33 >= 30mils;
AVDD33 >= 30mils;
AVDDH >= 20mils;
AVDDL >= 20mils.
DVDDL >= 20mils.
Pin LX to L1 >= 30mils.

EMC

UL3 AOZ8829DI
TR_D0+ TR_D0- TR_D1+ TR_D1-

UL2 AOZ8829DI
TR_D2+ TR_D2- TR_D3+ TR_D3-

D0G-05A0300-I14
D0G-06A050C-A68
Close to LAN conn.

LED0_ACT LED1_LINK1000# LED2_LINK100#
CL3 CL5 CL6 470p50X4

TCT CL4 0.1u10X4
DL1 ESD-VPORT0603L102KV05-HF
20151109 update
Main:D0G-1020530-I05
AVL :D0G-8010510-SI0
Close to LAN conn.

for EMI
VDD33 RL1 220R/4 CL2 X_0.1u10X4
LANLED_VCC5 LED0 RL2 75R/4 RL3 330R/8
LED1 RL4 220R/4 LED2 RL5 220R/4
LAN_USB1B
LED0_A LED0_ACT TCT TR_D0+ TR_D0- TR_D1+ TR_D1- TR_D2+ TR_D2- TR_D3+ TR_D3-
YELLOW+ YELLOW- LEDVCC RJ1 RJ2 RJ3 RJ4 RJ5 RJ6 RJ7 RJ8 GND
LED1_LINK1000# LED2_LINK100#
GREEN+/ORANGE- GREEN-/ORANGE+
RJ45_USBX2_LEDX2-1000-RH-10

LED1 low is Orange 1000
LED2 low is Green 100

LED ON/OFF by SIO

ATX_5VSB 3VSB R105 47K/4 R106 7.5K/4 Q24 2N7002D
24,77 ALL_LED_OFF#
+12V R114 4.7K/4 VCC5 2N7002 Q29
LANLED_VCC5 CL1 0.1u16X4

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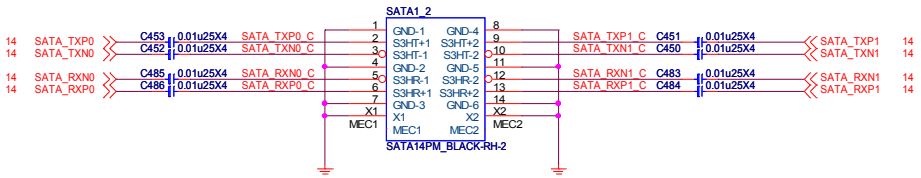
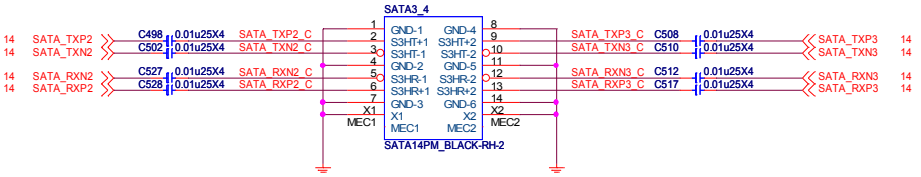
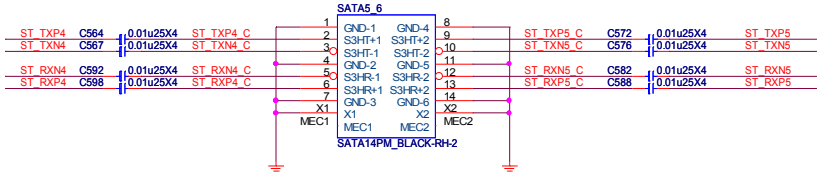
SATA 6G PORT 0.1

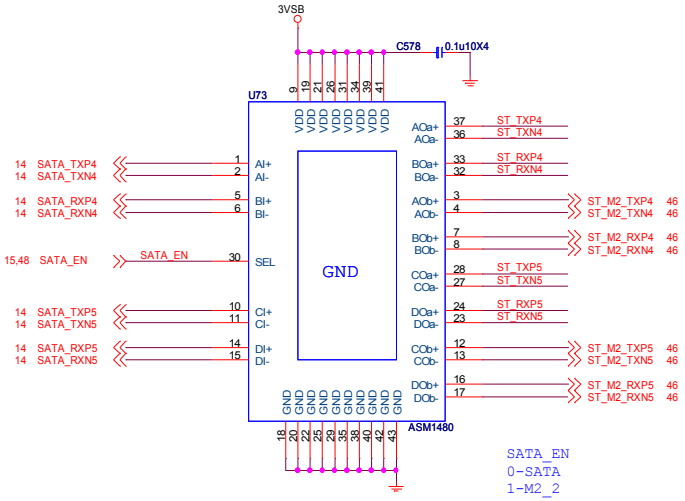


SATA 6G PORT 2.3



SATA 6G PORT 4.5





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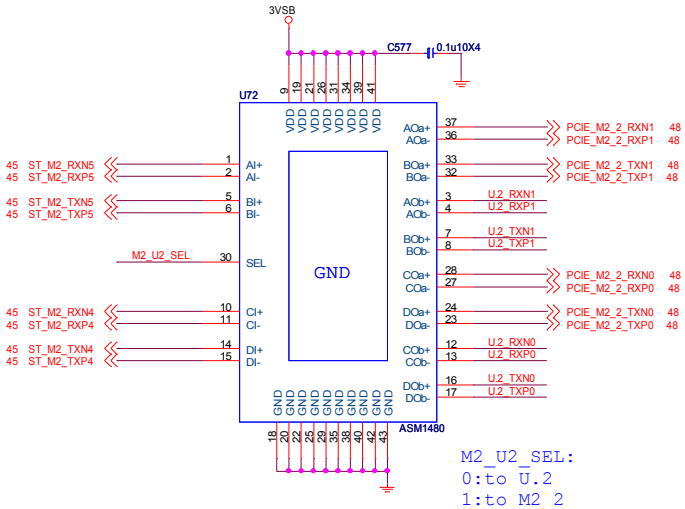
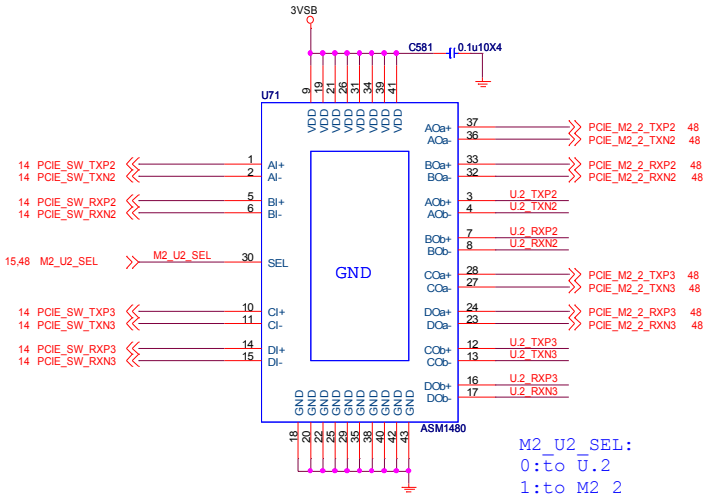
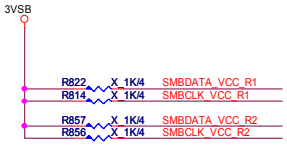
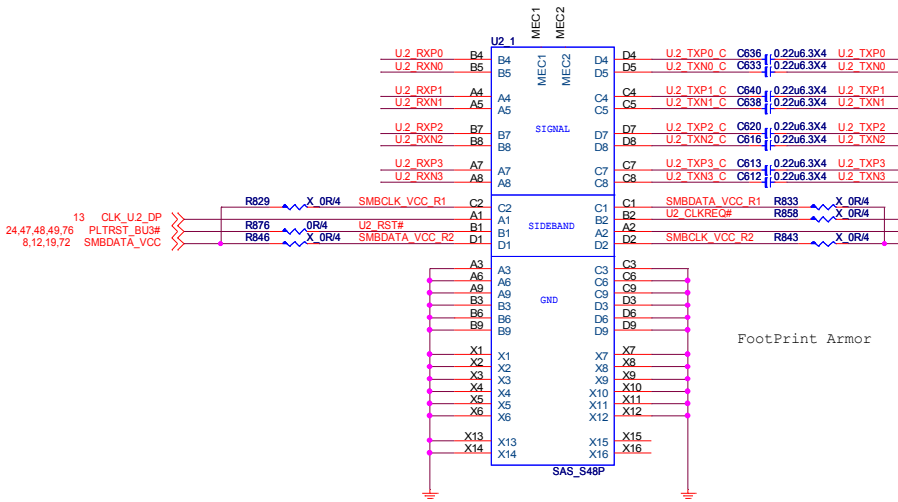


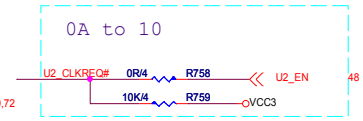
M2_U2_SEL:
0:to U.2
1:to M2_2



M2_U2_SEL:
0:to U.2
1:to M2_2







FootPrint Armor

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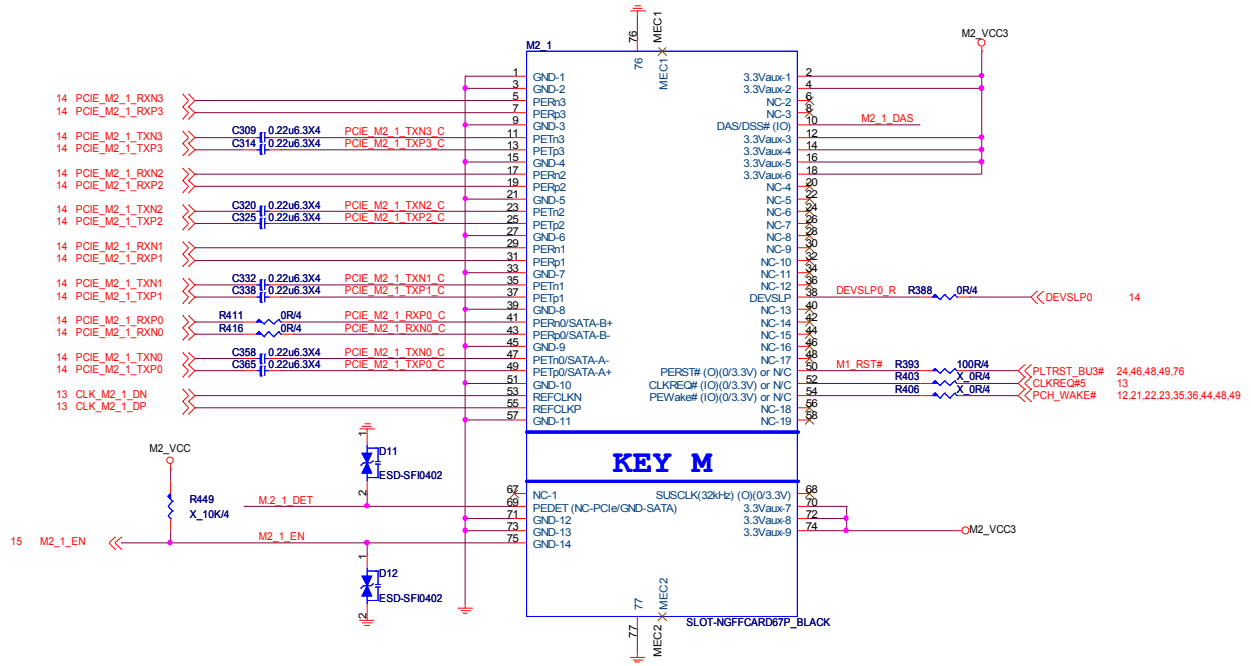
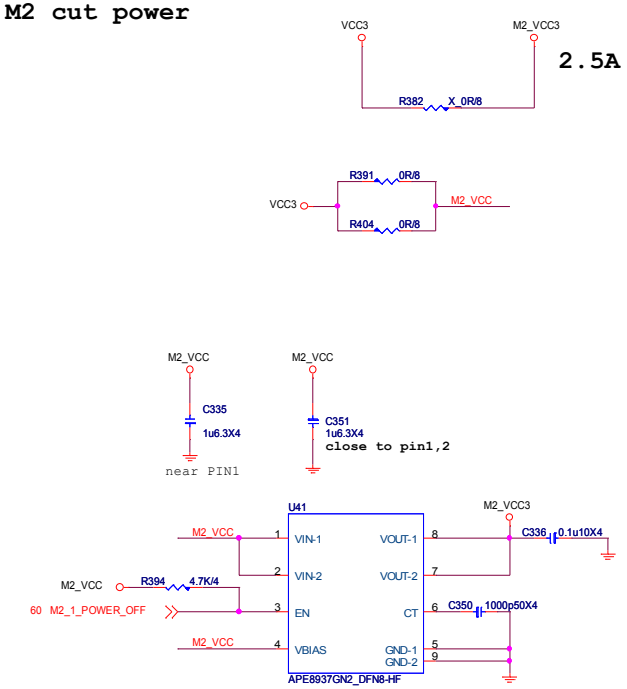
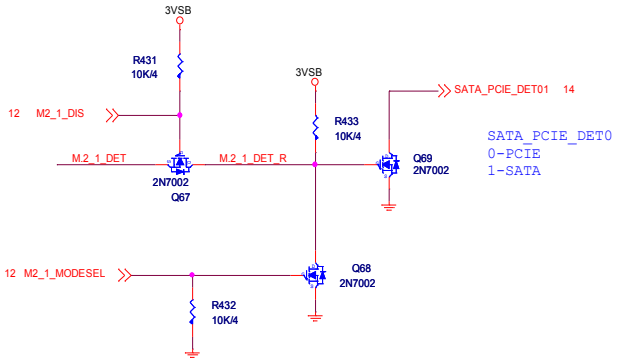


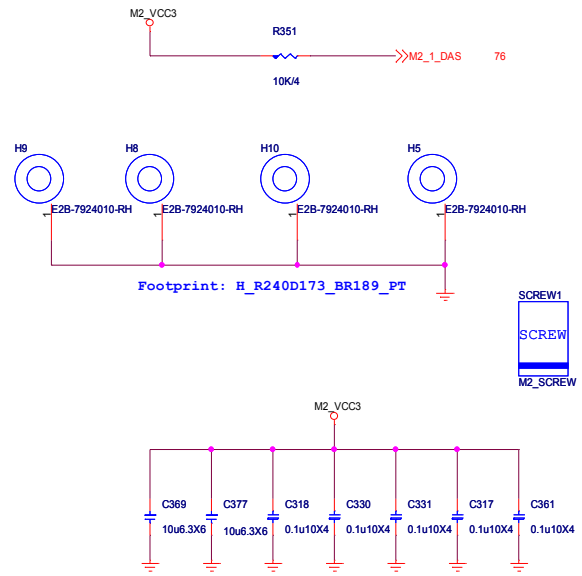
M2 cut power





BIOS_MODE

M2_1_DIS	*M2_1_MODESEL*	*Mode*
0	*1*	*M2-SATA*
0	*0*	*M2-PCIE*
GPI	*GPI*	*AUTO*



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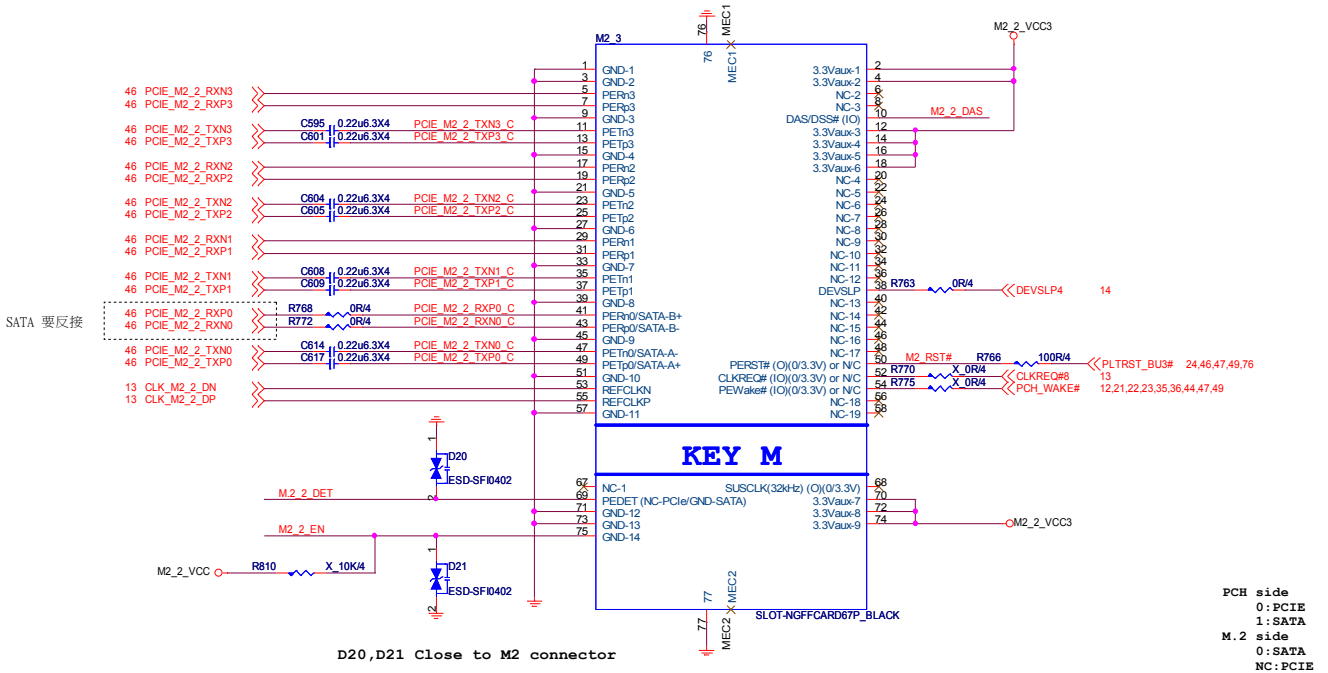
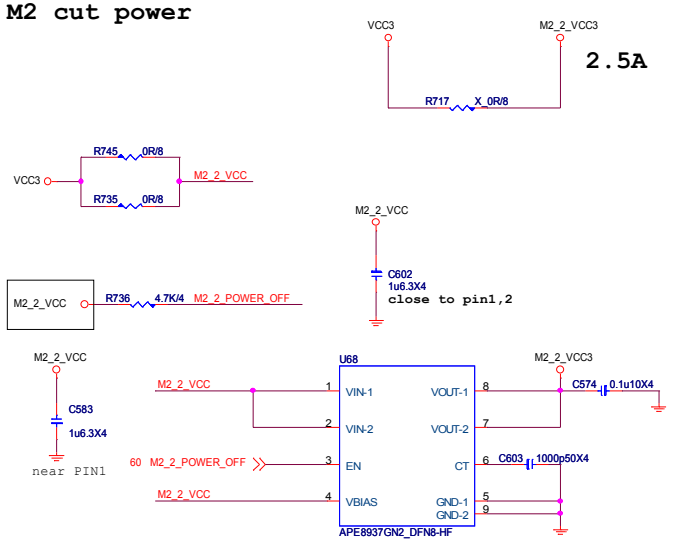
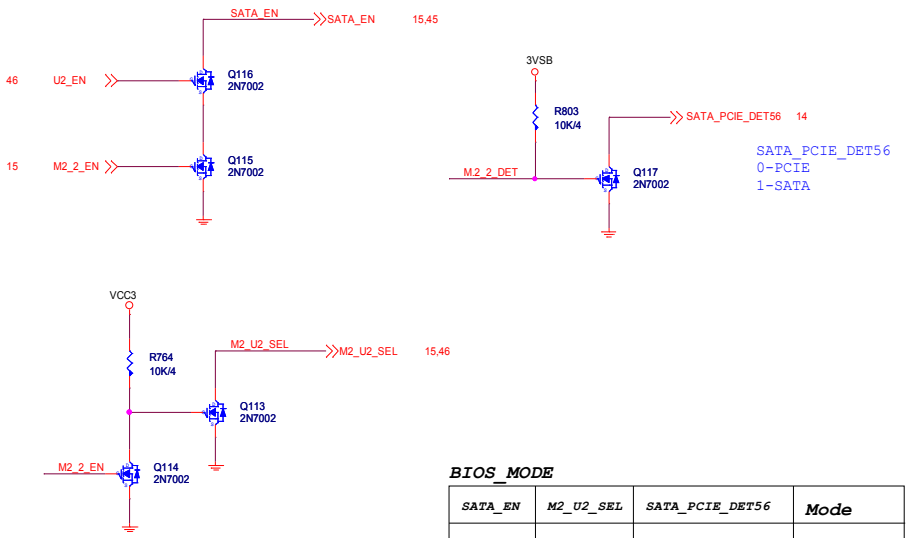


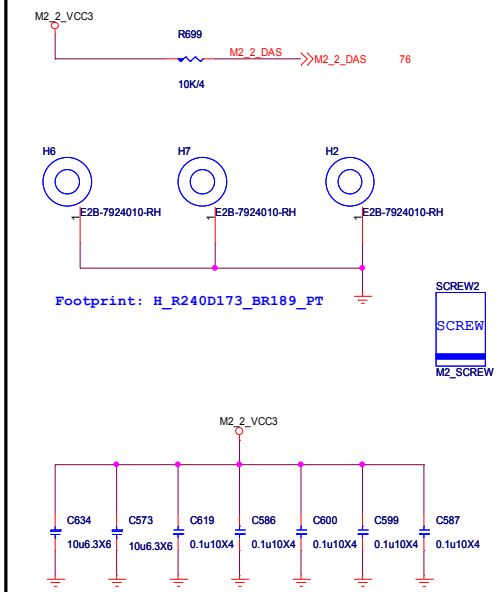
M2 cut power





BIOS_MODE

SATA_EN	M2_U2_SEL	SATA_PCIE_DET56	Mode
0	GPI	GPI	SATA
1	GPI	0	M2-SATA
1	GPI	GPI	M2-PCIE
1	0	GPI	U2-PCIE
GPI	GPI	GPI	AUTO



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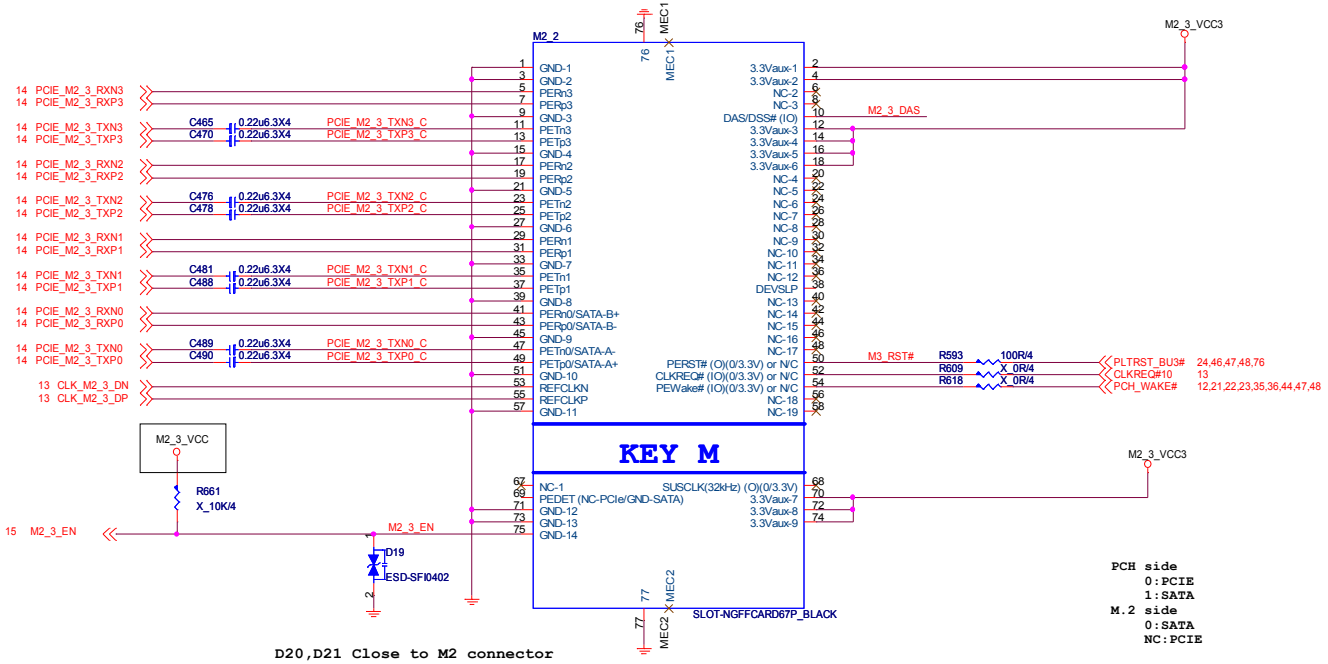
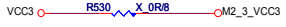
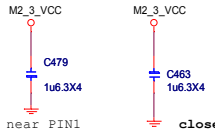


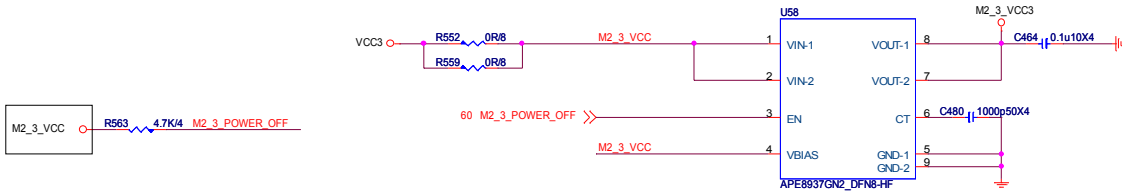
D20,D21 Close to M2 connector

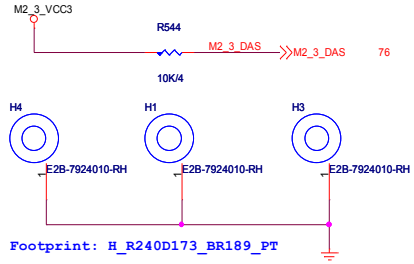
M2 cut power

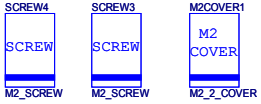


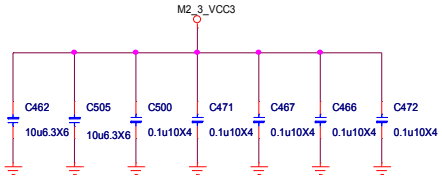
2.5A











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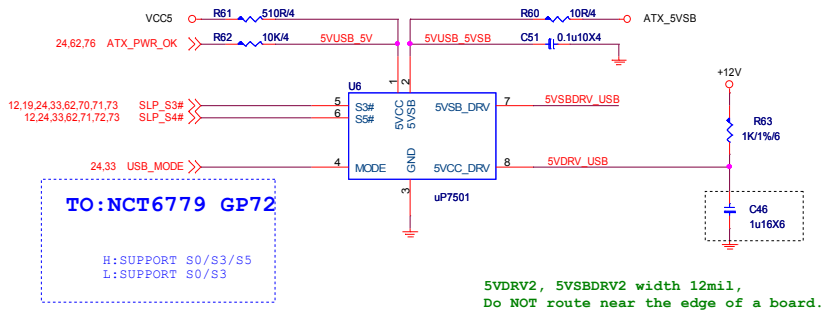
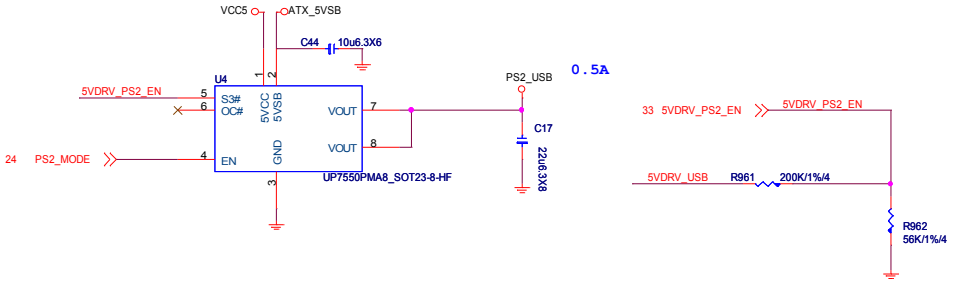
USB POWER



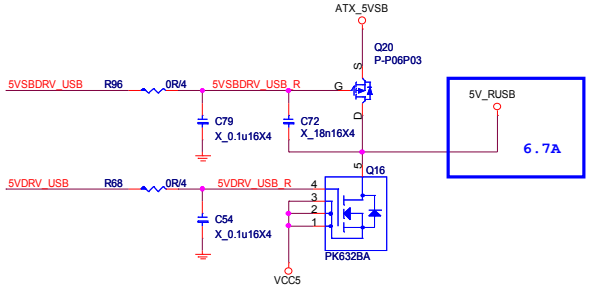
5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

PS2 POWER

USB MODE

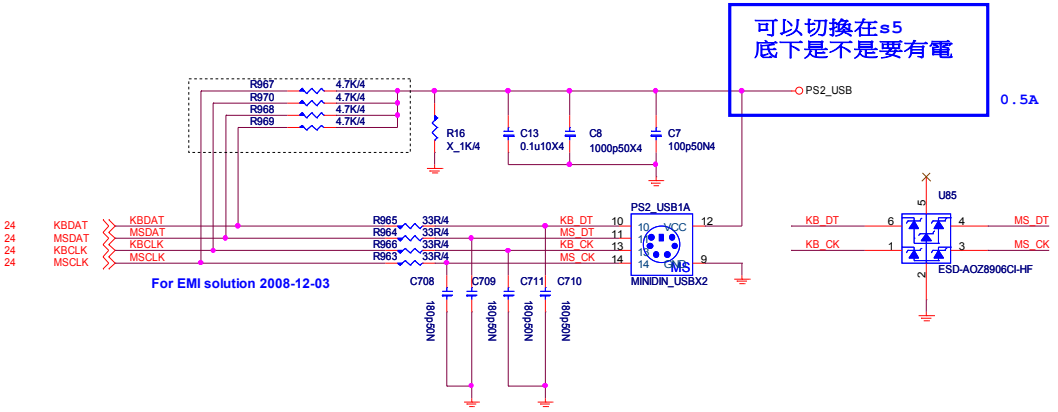


REAR USB PORT POWER



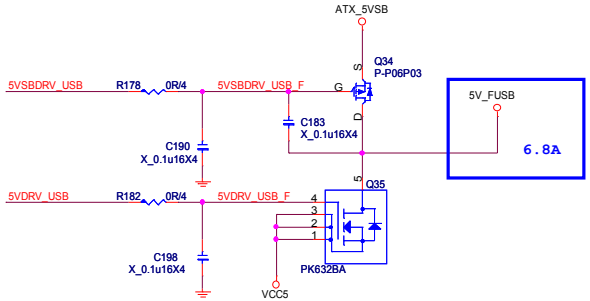
PS2 KEYBOARD & MOUSE CONNECTOR

可以切換在s5
底下是不是要有電



For EMI solution 2008-12-03

FRONT USB PORT POWER



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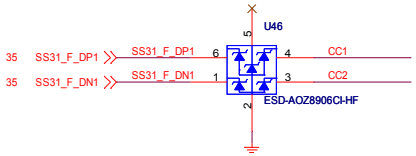
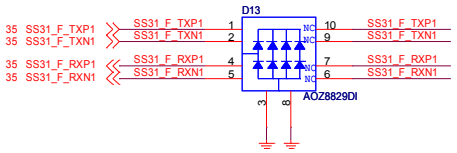
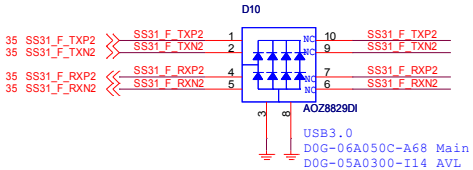
Front TYPE-C

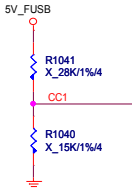
ESD Protection

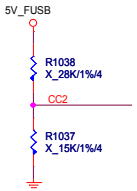
NEAR CONNECTOR

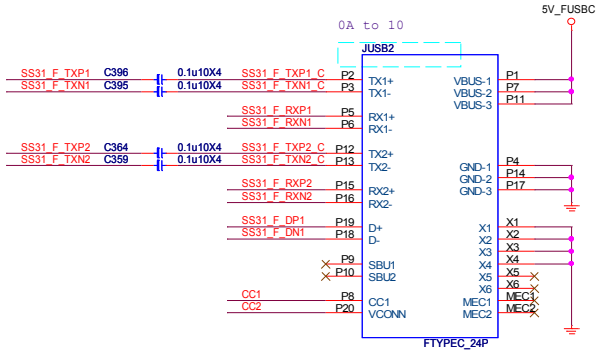


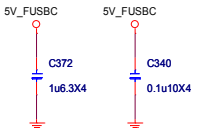




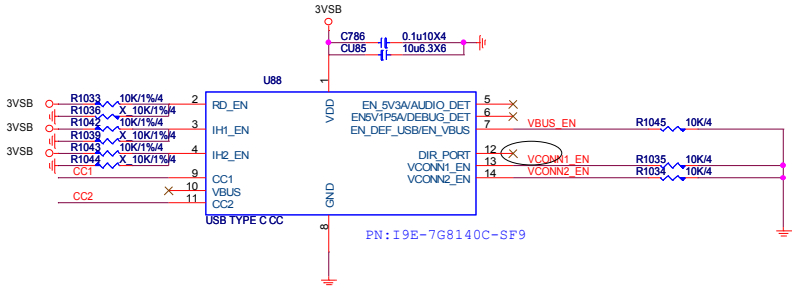




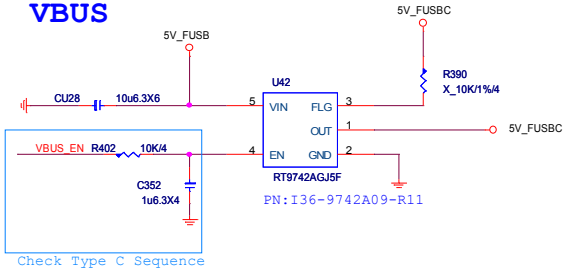




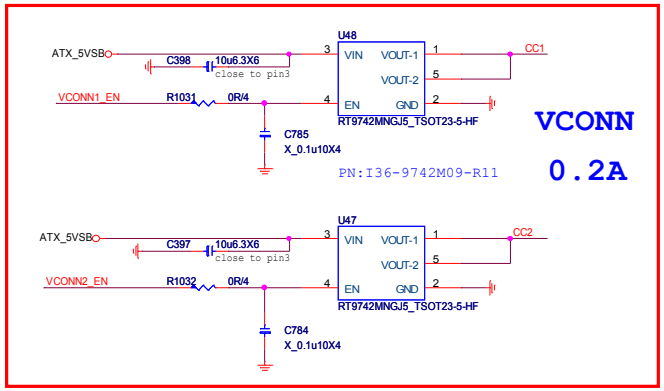
CC Logic CTRL -SLG7G814V

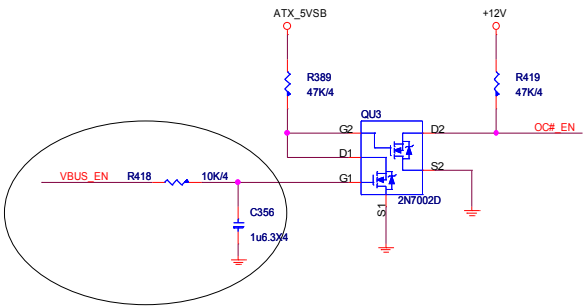


VBUS

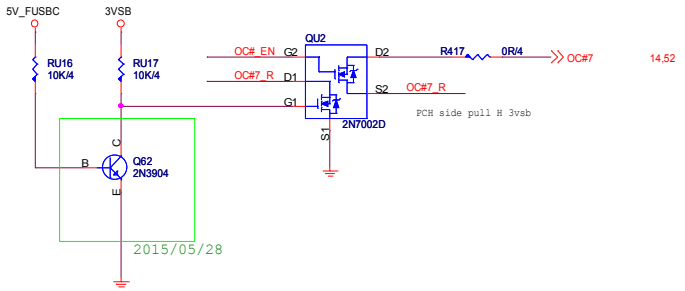


3 A





USB OC# Singal



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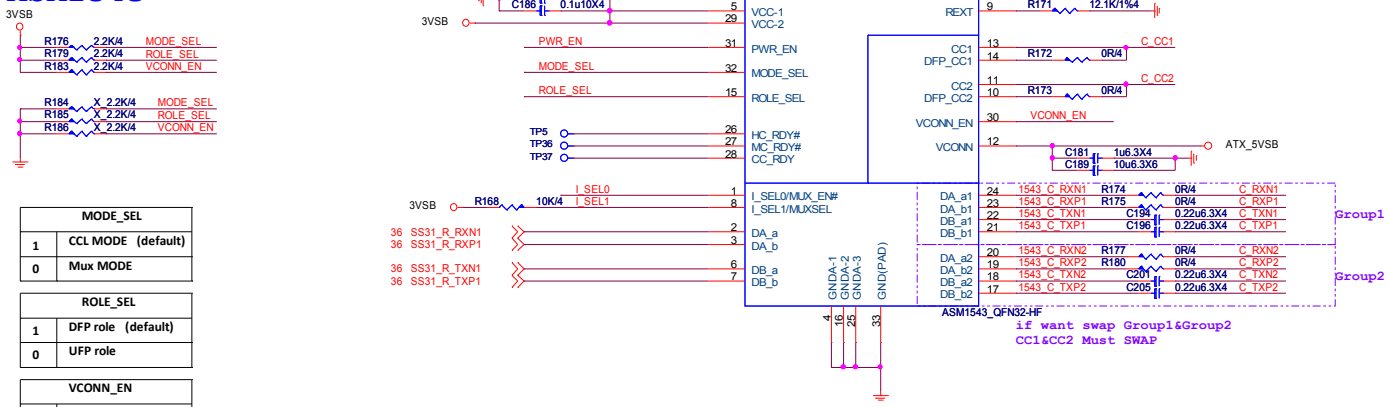
ASM1543

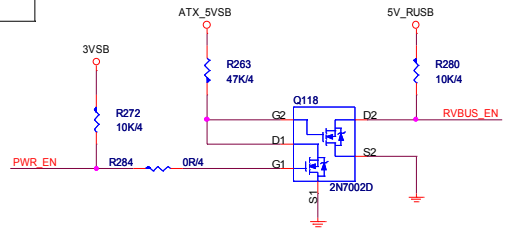


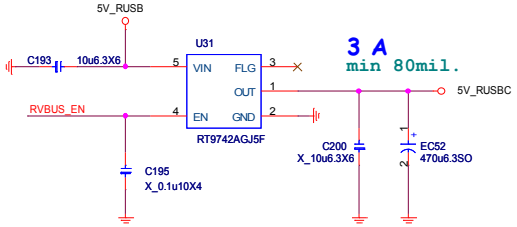
if want swap Group1&Group2
CC1&CC2 Must SWAP

MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

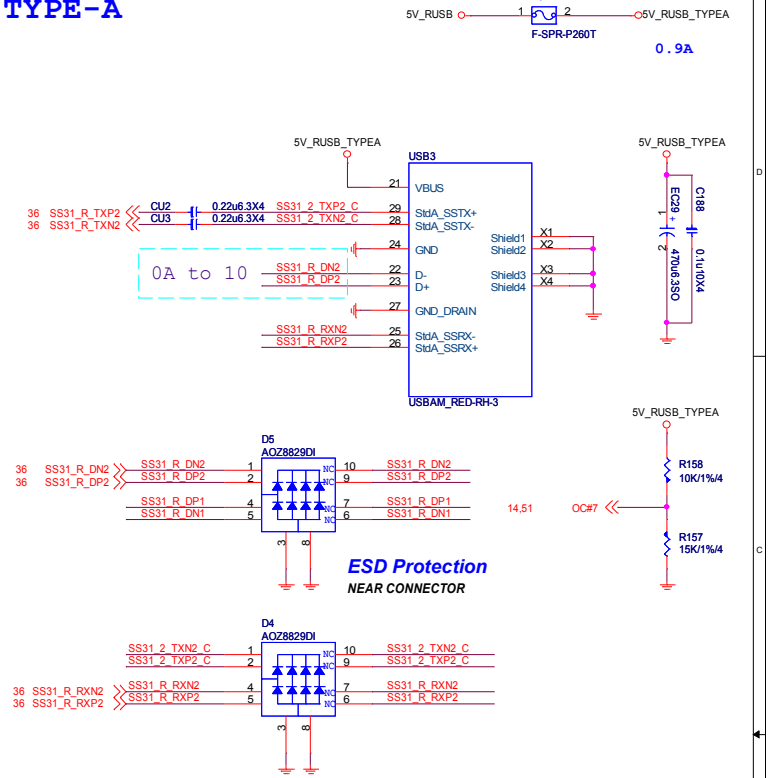
VCONN_EN	
1	enable
0	disable





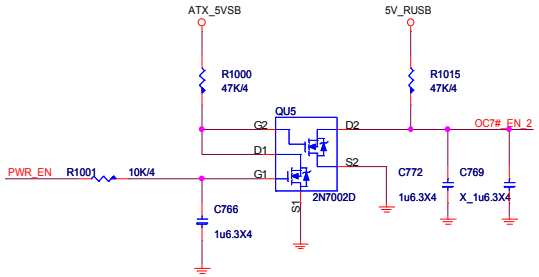
3 A
min 80mil.

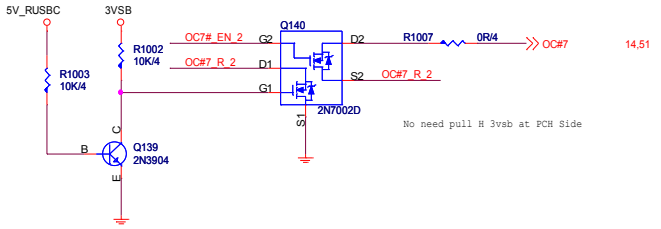
TYPE-A



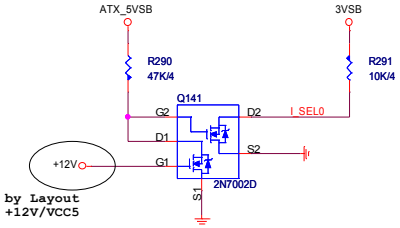
ESD Protection
NEAR CONNECTOR

VBUS OC#





Current Mode



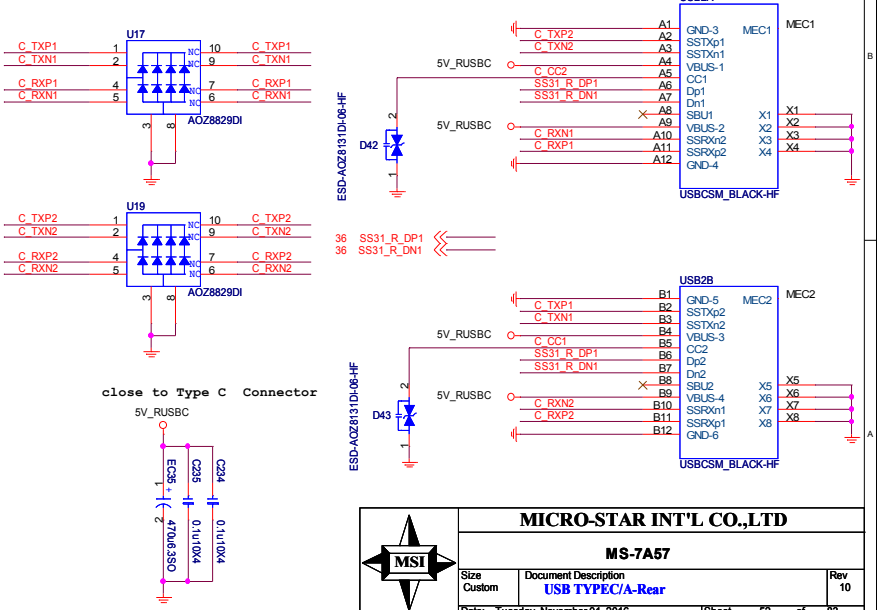
by Layout
+12V/VCC5

I_SEL0 : I_SEL1

X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode

TYPE-C



close to Type C Connector

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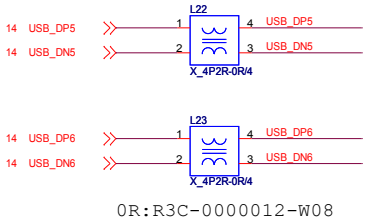
FRONT USB PORT 5,6



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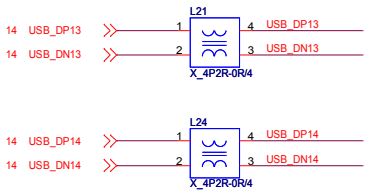

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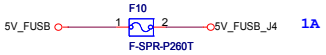

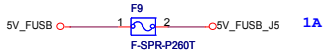

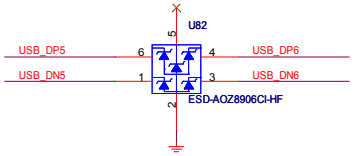

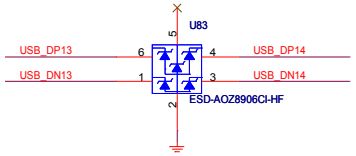

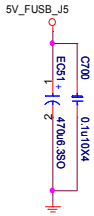

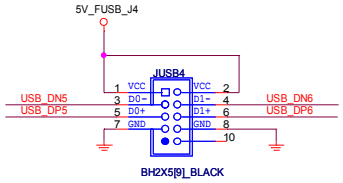

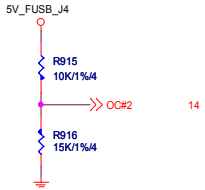

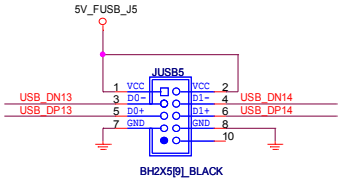

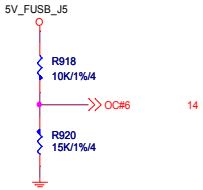

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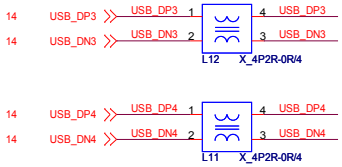
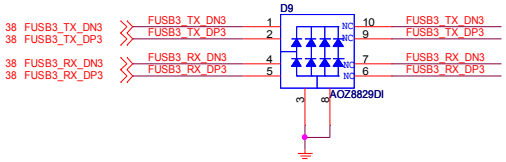
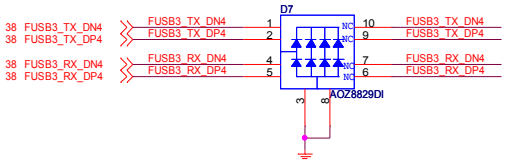
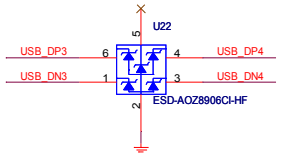
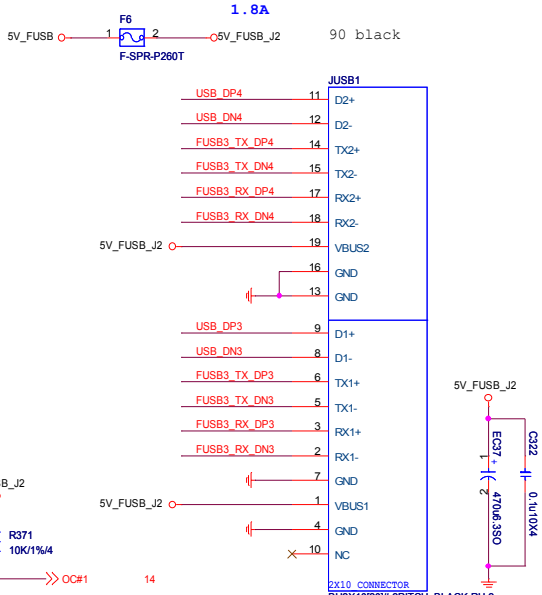
FUSB3 90°



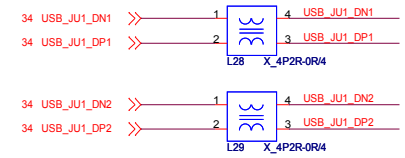


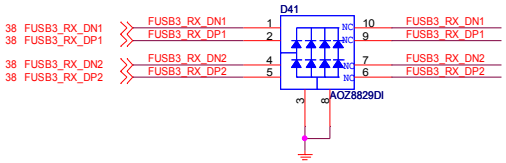


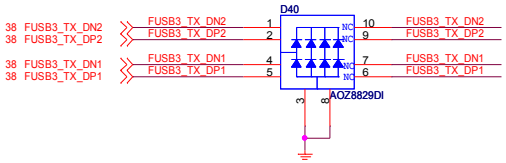


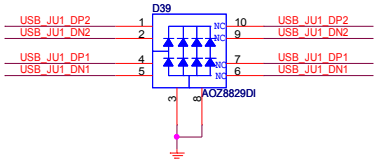


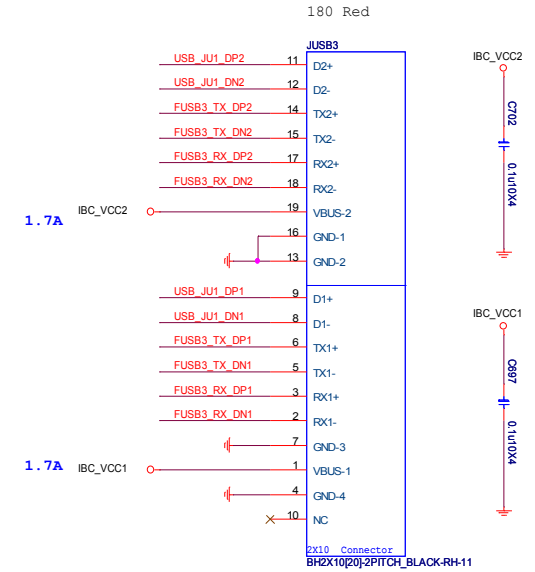
FUSB3 180°











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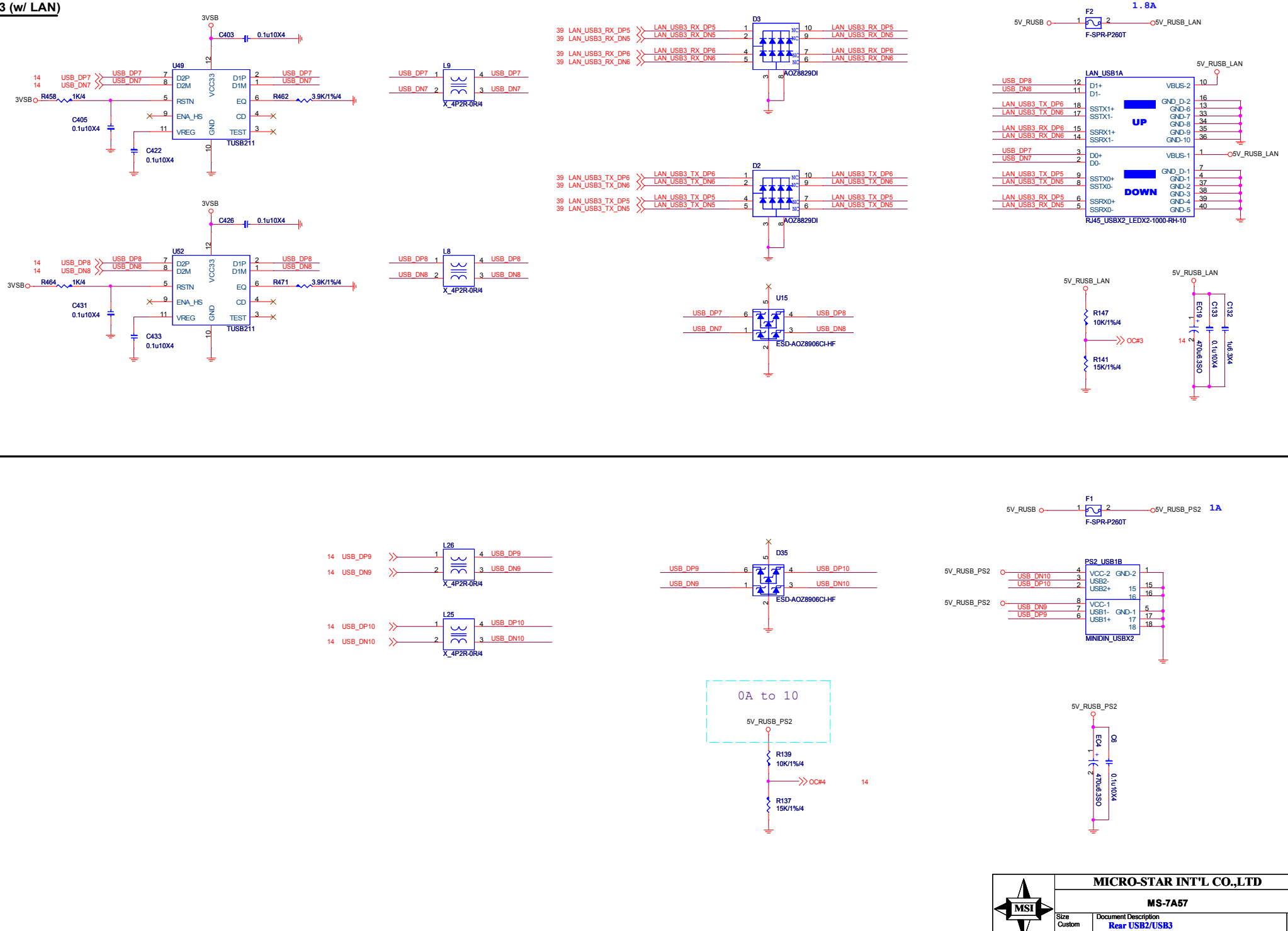
Rear USB3 (w/ LAN)



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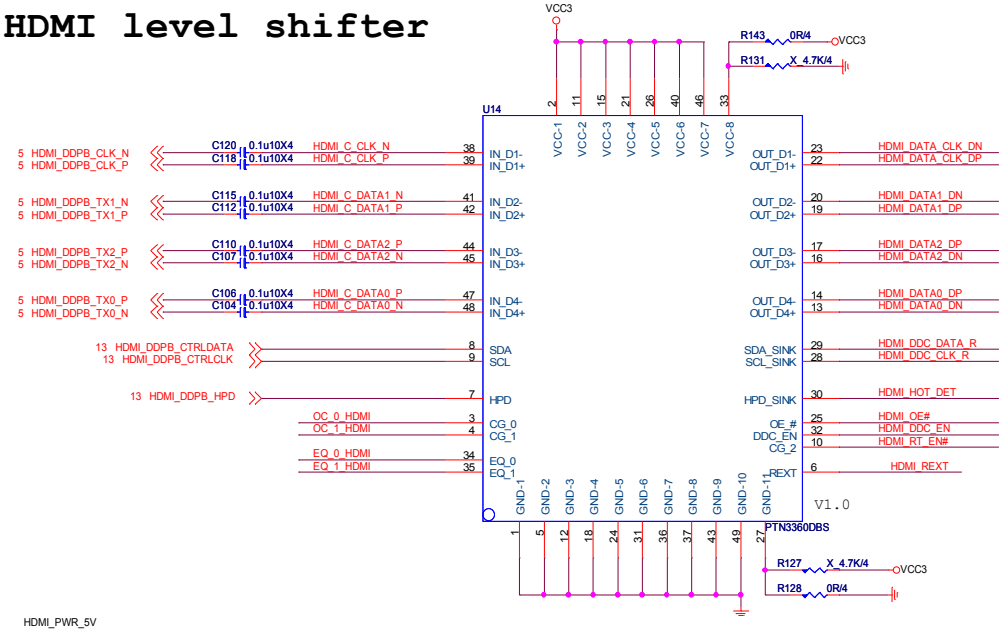
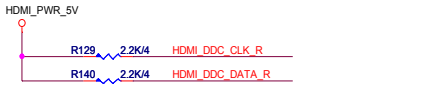
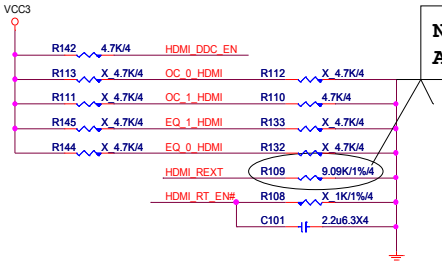
HDMI level shifter

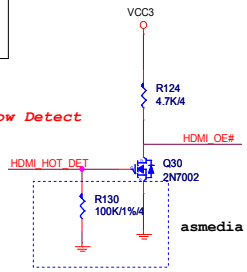






NXP :9.09K
ASMEDIA:3K

注意High/Low Detect



asmedia pull down 20K

	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

EMI

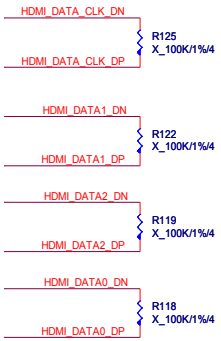
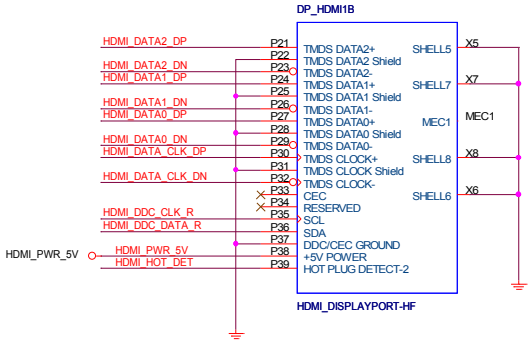
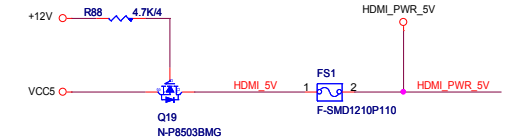
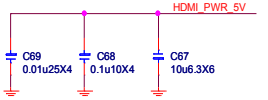


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

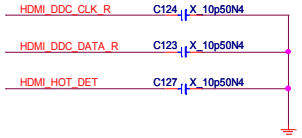
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	

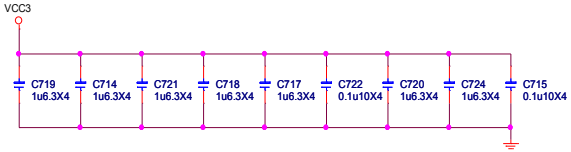






EMI cap.





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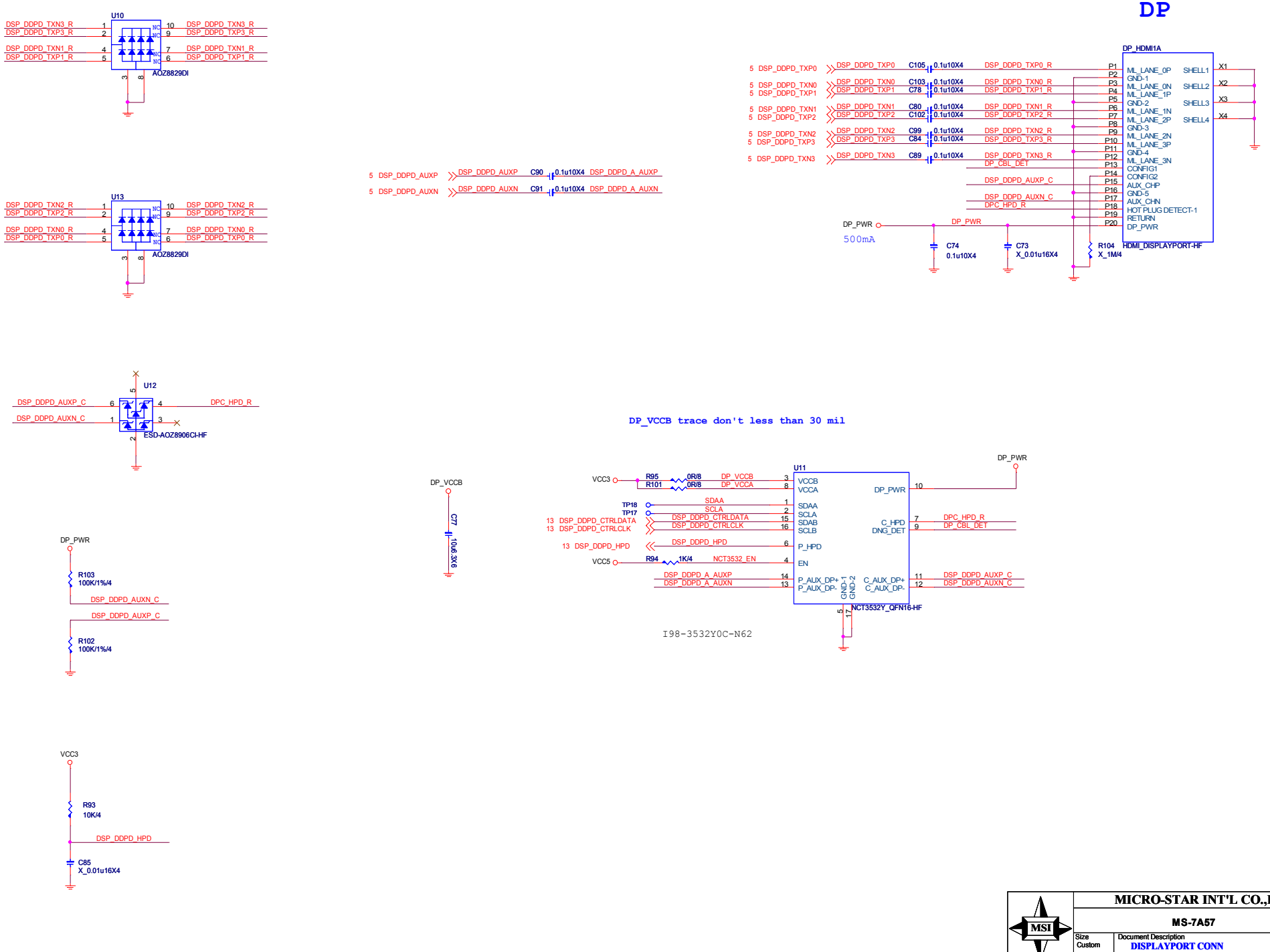
DP



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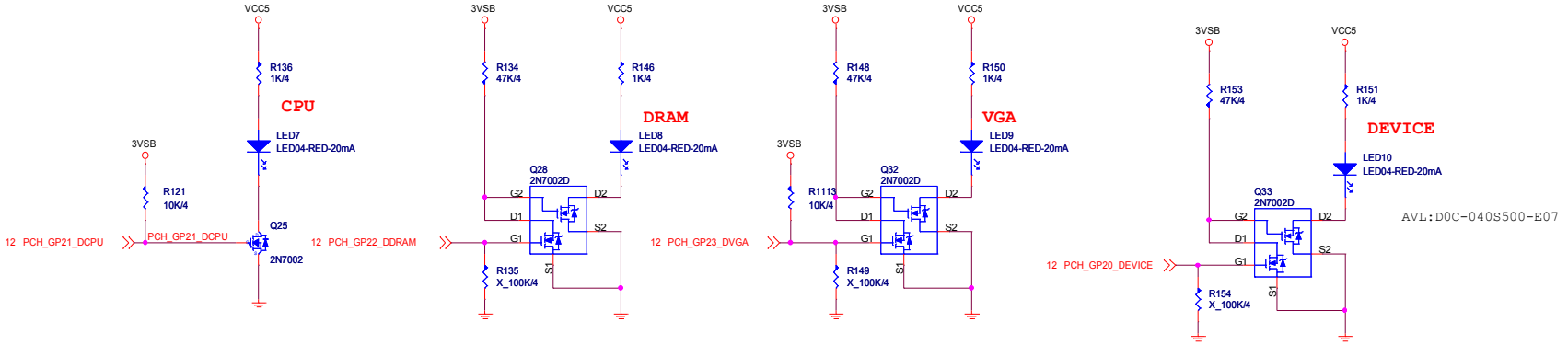

關機斷電狀態下，4個LED先維持default全暗，開機通電後：
1.首先進行CPU check CPU LED 亮，check PASS後則CPU LED滅掉。
2.接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3.VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4.因此最後正常順利開機後，三個LED燈都是滅掉的。
（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

GPIO / LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

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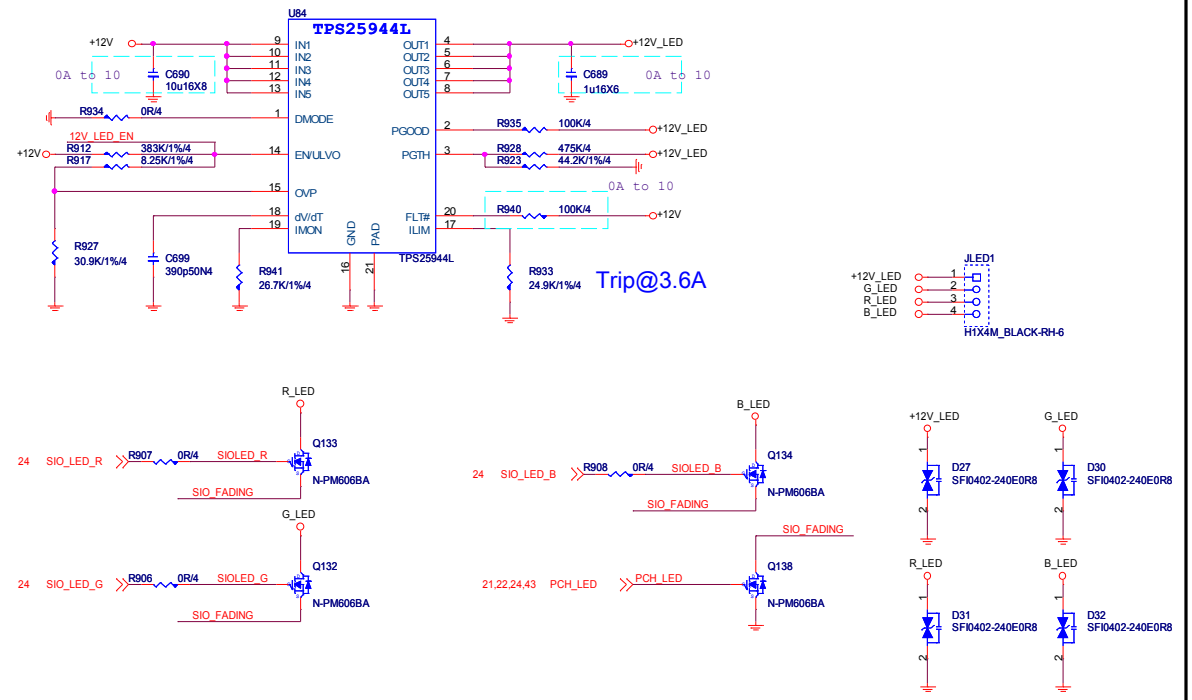
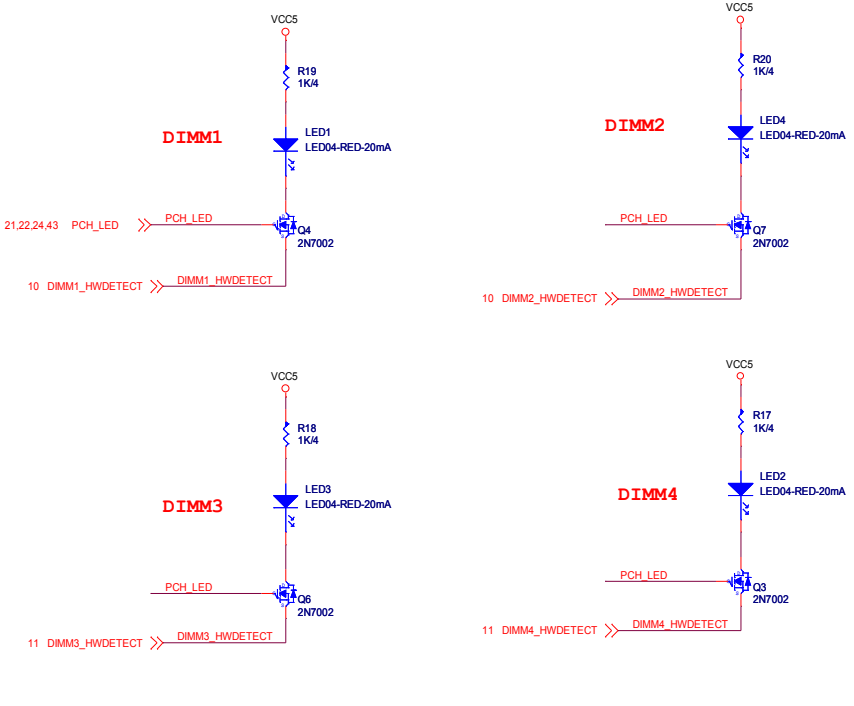
JLED

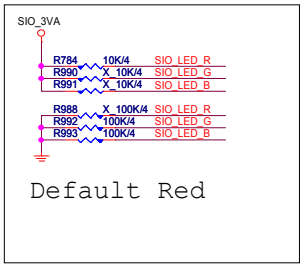


DIMM LED



PCH LED

MPOWER REMOVE



MOS LED

MPOWER REMOVE

AUDIO LED

MPOWER REMOVE

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Custom	RGB LED-JLED/JPCH/JMOS	10

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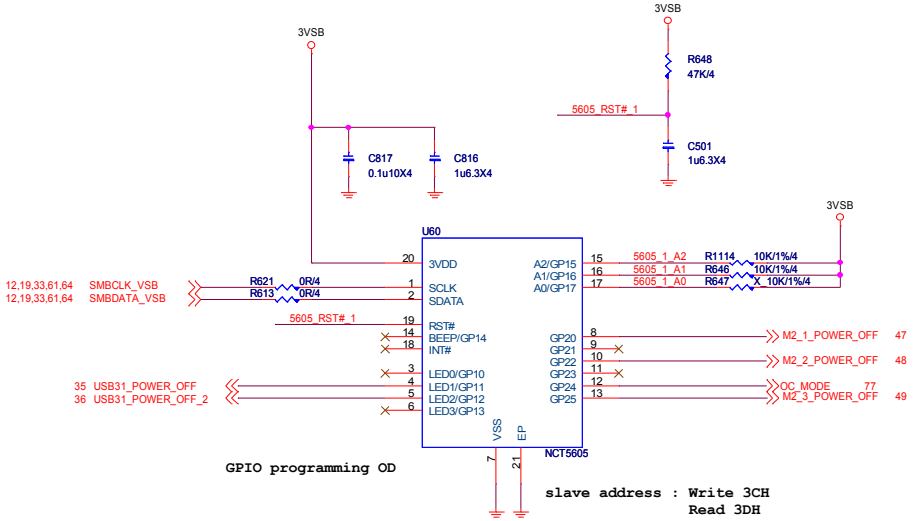
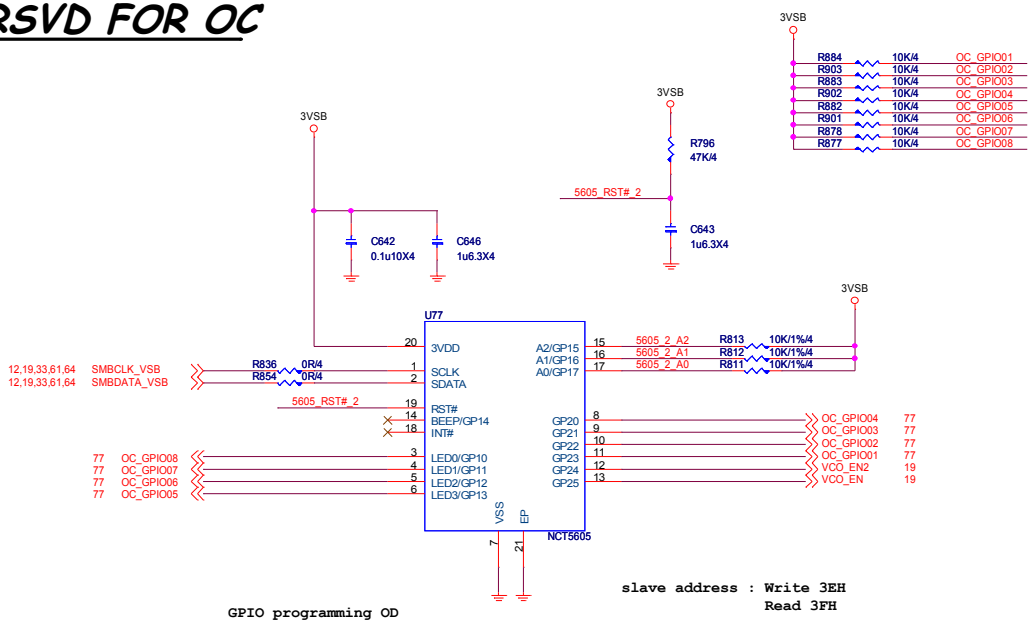
CUT POWER



GPIO programming OD

slave address : Write 3CH
Read 3DH

RSVD FOR OC



GPIO programming OD

slave address : Write 3EH
Read 3FH

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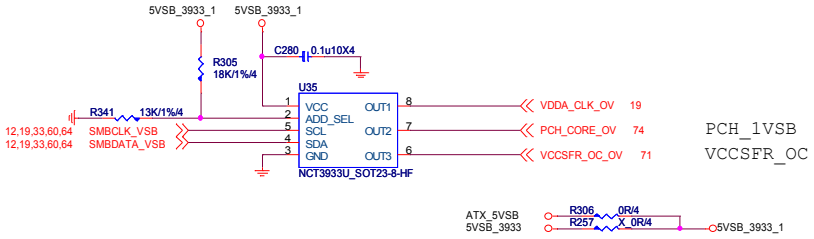
UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

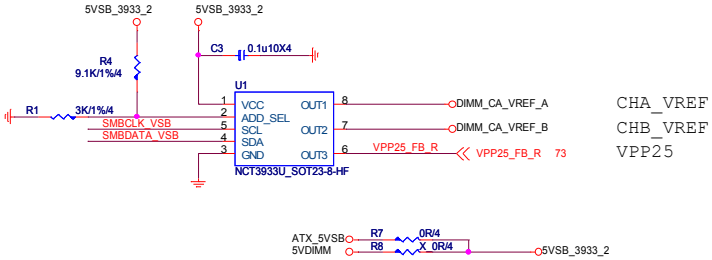
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



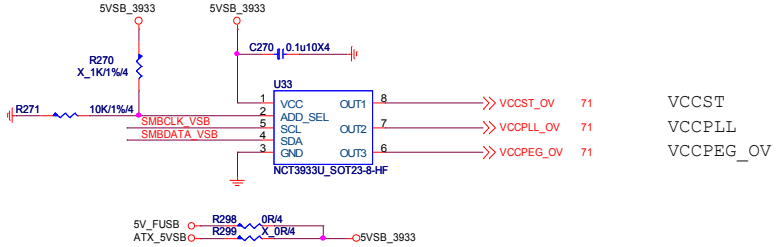
UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K



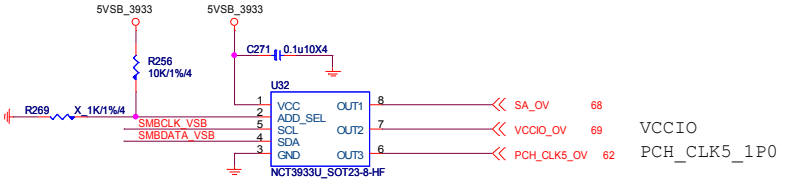
UPI VOLTAGE CONSOLE

0x2A:RH=9.1K,RL=3K



UPI VOLTAGE CONSOLE

0x20:RH=18K,RL=13K



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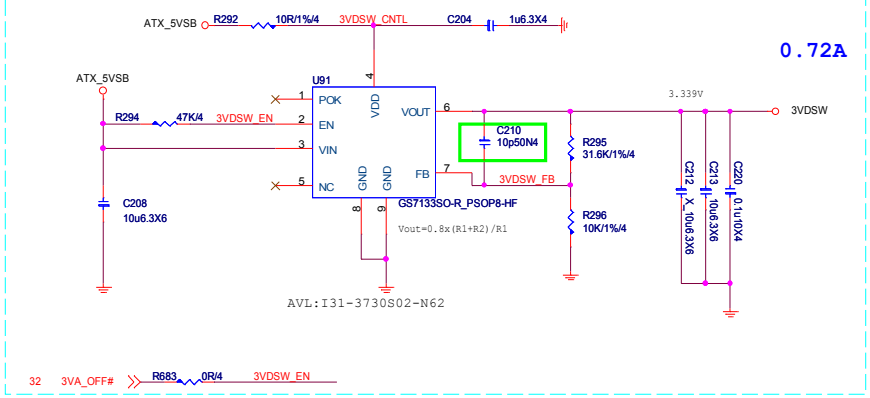
3VDSW

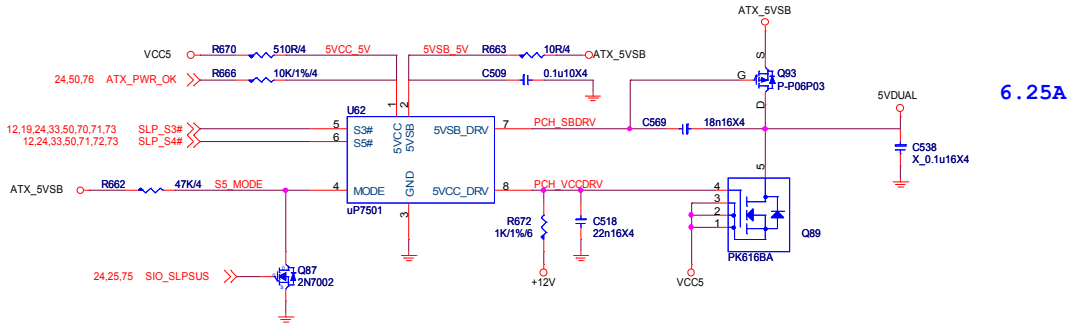
0A to 10

0.72A



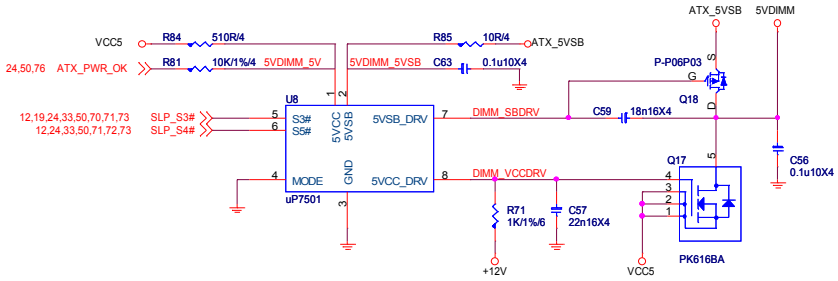
5VDUAL

6.25A



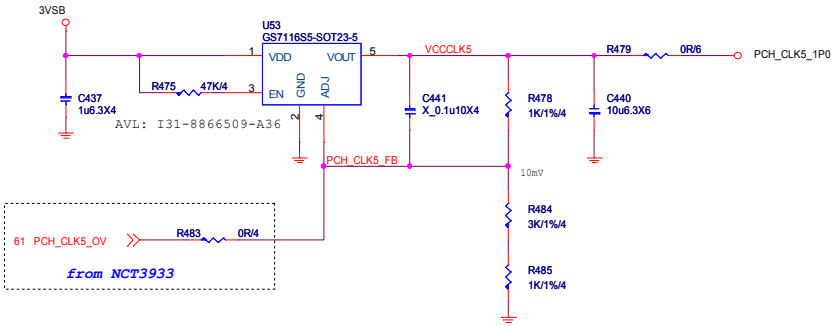
5VDIMM FOR DDR

4.8A



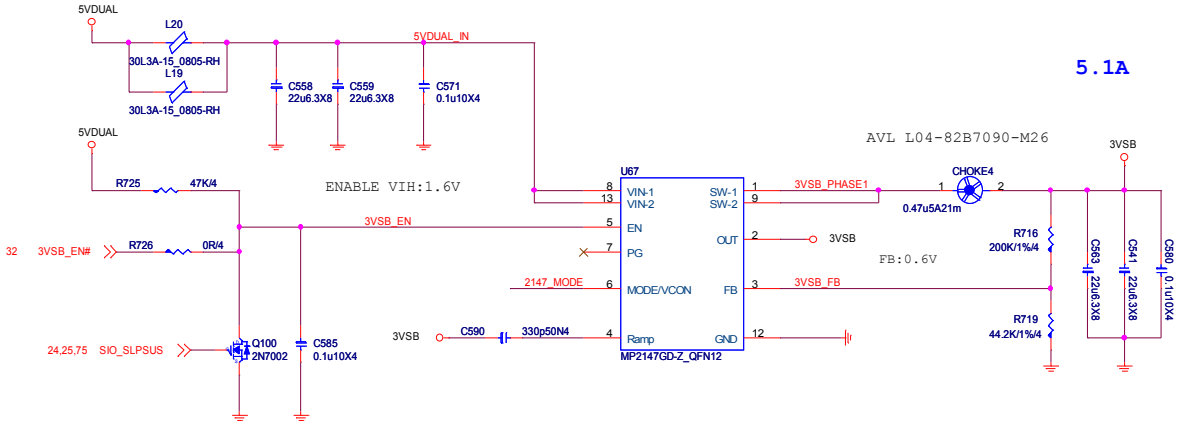
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

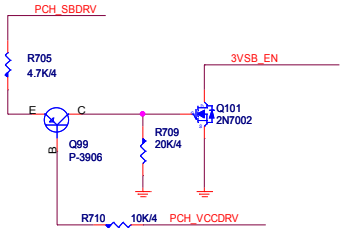
5VDRV1看VCC5起來6-10ms後起來，
因為當初挑power

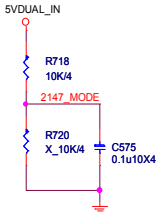


3VSB for OC & Gaming

5.1A







防G3-->S5底下5VSBDRV2瞬間有電變沒電，使得下一級電壓爬升有drop

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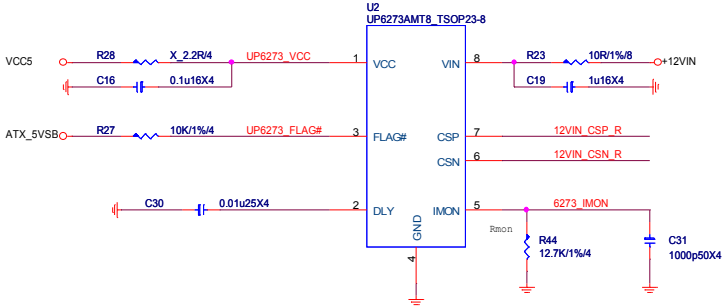
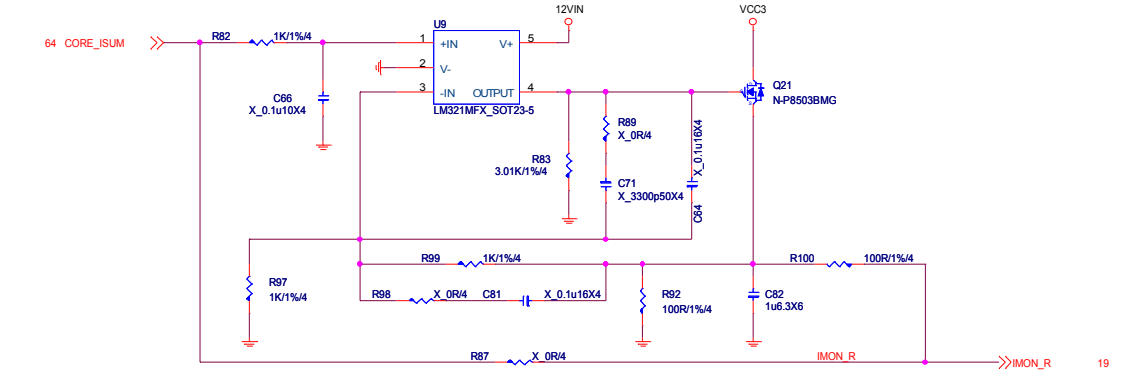
POWER METER

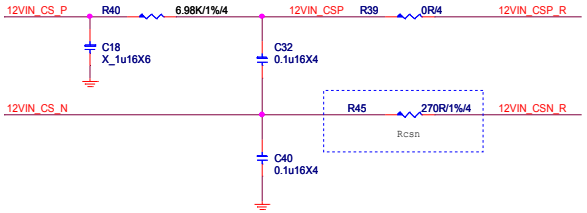
OCP: 35A

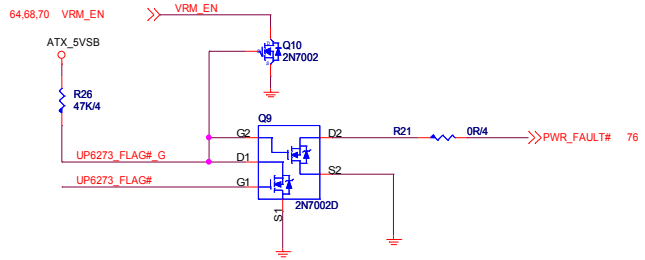


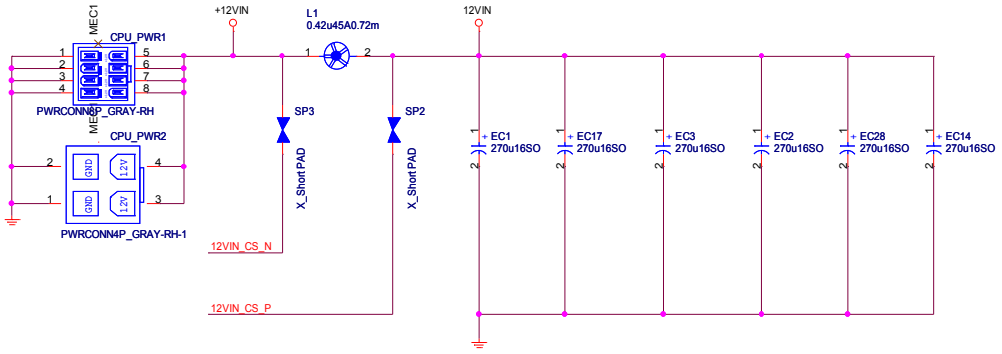
Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon

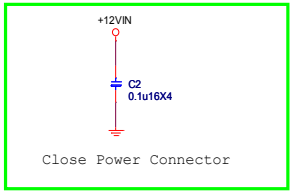
Near PWM IC











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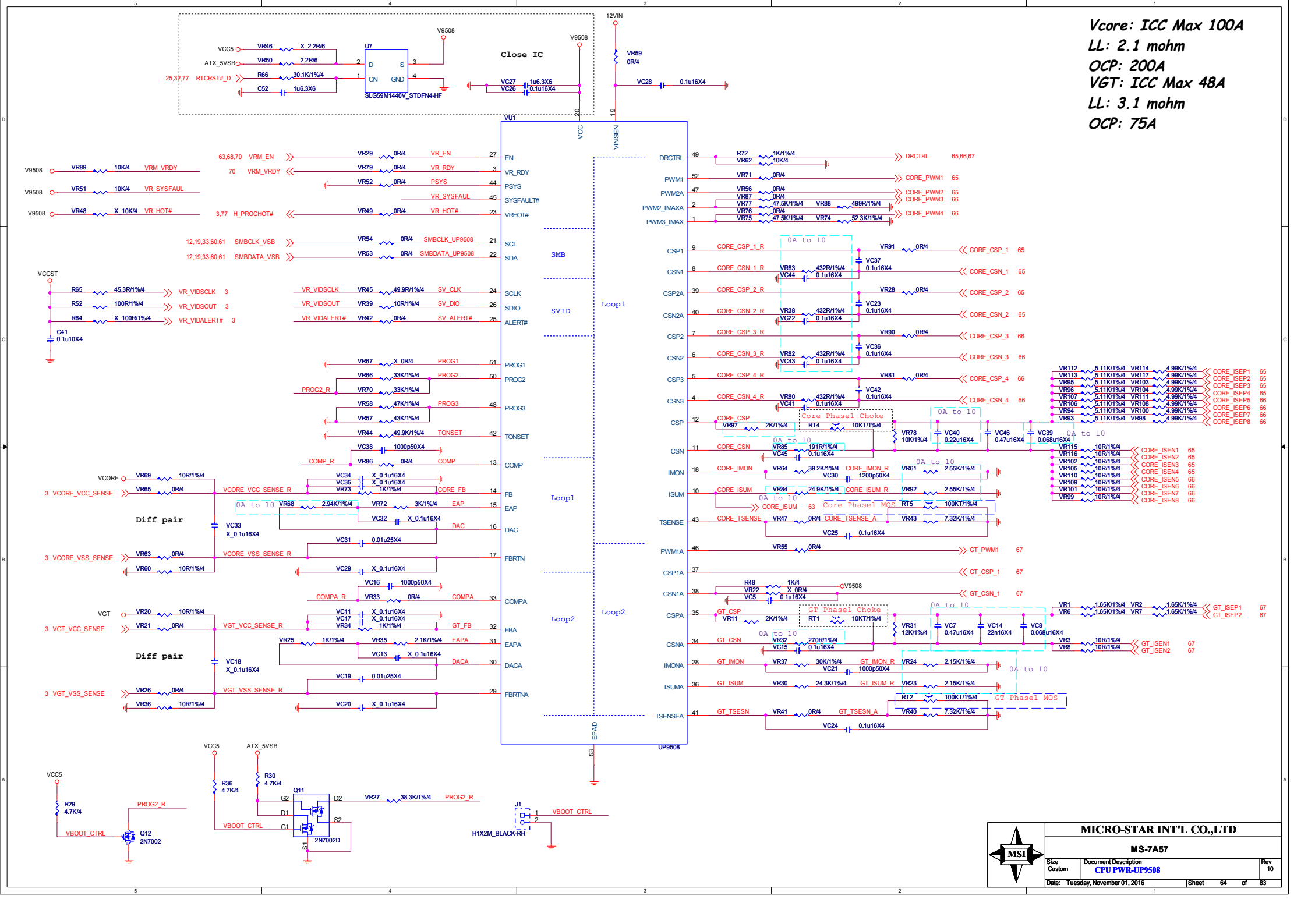
Vcore: ICC Max 100A
LL: 2.1 mohm
OCP: 200A
VGT: ICC Max 48A
LL: 3.1 mohm
OCP: 75A



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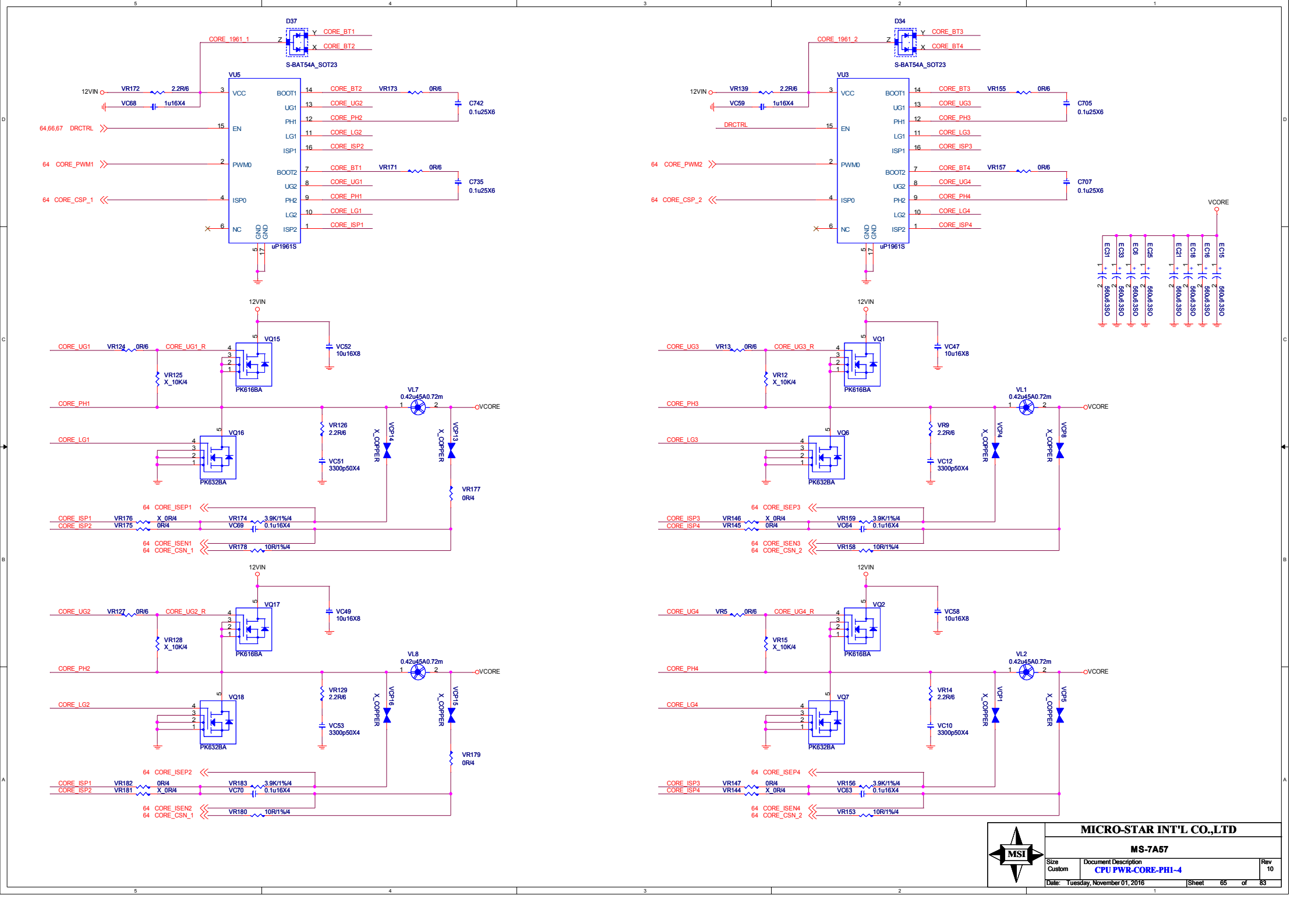
D37
S-BAT54A_SOT23
CORE_1961_1
CORE_BT1
CORE_BT2
VU5
uP1961S
12VIN
VR172 2.2R/6
VC68 1u16X4
64,66,67 DRCTRL
64 CORE_PWM1
64 CORE_CSP_1
VCC
EN
PWM0
ISP0
NC
GND
BOOT1
UG1
PH1
LG1
ISP1
BOOT2
UG2
PH2
LG2
ISP2
CORE_BT2
CORE_UG2
CORE_PH2
CORE_LG2
CORE_ISP2
CORE_BT1
CORE_UG1
CORE_PH1
CORE_LG1
CORE_ISP1
VR173 0R/6
VR171 0R/6
C742 0.1u25X6
C735 0.1u25X6
D34
S-BAT54A_SOT23
CORE_1961_2
CORE_BT3
CORE_BT4
VU3
uP1961S
12VIN
VR139 2.2R/6
VC59 1u16X4
DRCTRL
64 CORE_PWM2
64 CORE_CSP_2
CORE_BT3
CORE_UG3
CORE_PH3
CORE_LG3
CORE_ISP3
CORE_BT4
CORE_UG4
CORE_PH4
CORE_LG4
CORE_ISP4
VR155 0R/6
VR157 0R/6
C705 0.1u25X6
C707 0.1u25X6
VCORE
EC31
EC33
EC6
EC25
EC21
EC18
EC16
EC15
560u6.3SO
12VIN
CORE_UG1
VR124 0R/6
CORE_UG1_R
VQ15
PK616BA
VC52 10u16X8
VR125 X_10K/4
CORE_PH1
VL7 0.42u45A0.72m
VCORE
VQ16
PK632BA
CORE_LG1
VR126 2.2R/6
VC51 3300p50X4
VCP14 X_COPPER
VCP13 X_COPPER
VR177 0R/4
64 CORE_ISEP1
CORE_ISP1 VR176 X_0R/4
CORE_ISP2 VR175 0R/4
VR174 3.9K/1%/4
VC69 0.1u16X4
64 CORE_ISEN1
64 CORE_CSN_1
VR178 10R/1%/4
12VIN
CORE_UG3
VR13 0R/6
CORE_UG3_R
VQ1
PK616BA
VC47 10u16X8
VR12 X_10K/4
CORE_PH3
VL1 0.42u45A0.72m
VCORE
VQ6
PK632BA
CORE_LG3
VR9 2.2R/6
VC12 3300p50X4
VCP4 X_COPPER
VCP8 X_COPPER
64 CORE_ISEP3
CORE_ISP3 VR146 X_0R/4
CORE_ISP4 VR145 0R/4
VR159 3.9K/1%/4
VC64 0.1u16X4
64 CORE_ISEN3
64 CORE_CSN_2
VR158 10R/1%/4
12VIN
CORE_UG2
VR127 0R/6
CORE_UG2_R
VQ17
PK616BA
VC49 10u16X8
VR128 X_10K/4
CORE_PH2
VL8 0.42u45A0.72m
VCORE
VQ18
PK632BA
CORE_LG2
VR129 2.2R/6
VC53 3300p50X4
VCP16 X_COPPER
VCP15 X_COPPER
VR179 0R/4
64 CORE_ISEP2
CORE_ISP1 VR182 0R/4
CORE_ISP2 VR181 X_0R/4
VR183 3.9K/1%/4
VC70 0.1u16X4
64 CORE_ISEN2
64 CORE_CSN_1
VR180 10R/1%/4
12VIN
CORE_UG4
VR5 0R/6
CORE_UG4_R
VQ2
PK616BA
VC58 10u16X8
VR15 X_10K/4
CORE_PH4
VL2 0.42u45A0.72m
VCORE
VQ7
PK632BA
CORE_LG4
VR14 2.2R/6
VC10 3300p50X4
VCP1 X_COPPER
VCP5 X_COPPER
64 CORE_ISEP4
CORE_ISP3 VR147 0R/4
CORE_ISP4 VR144 X_0R/4
VR156 3.9K/1%/4
VC63 0.1u16X4
64 CORE_ISEN4
64 CORE_CSN_2
VR153 10R/1%/4
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CPU PWR-CORE-PH1~4
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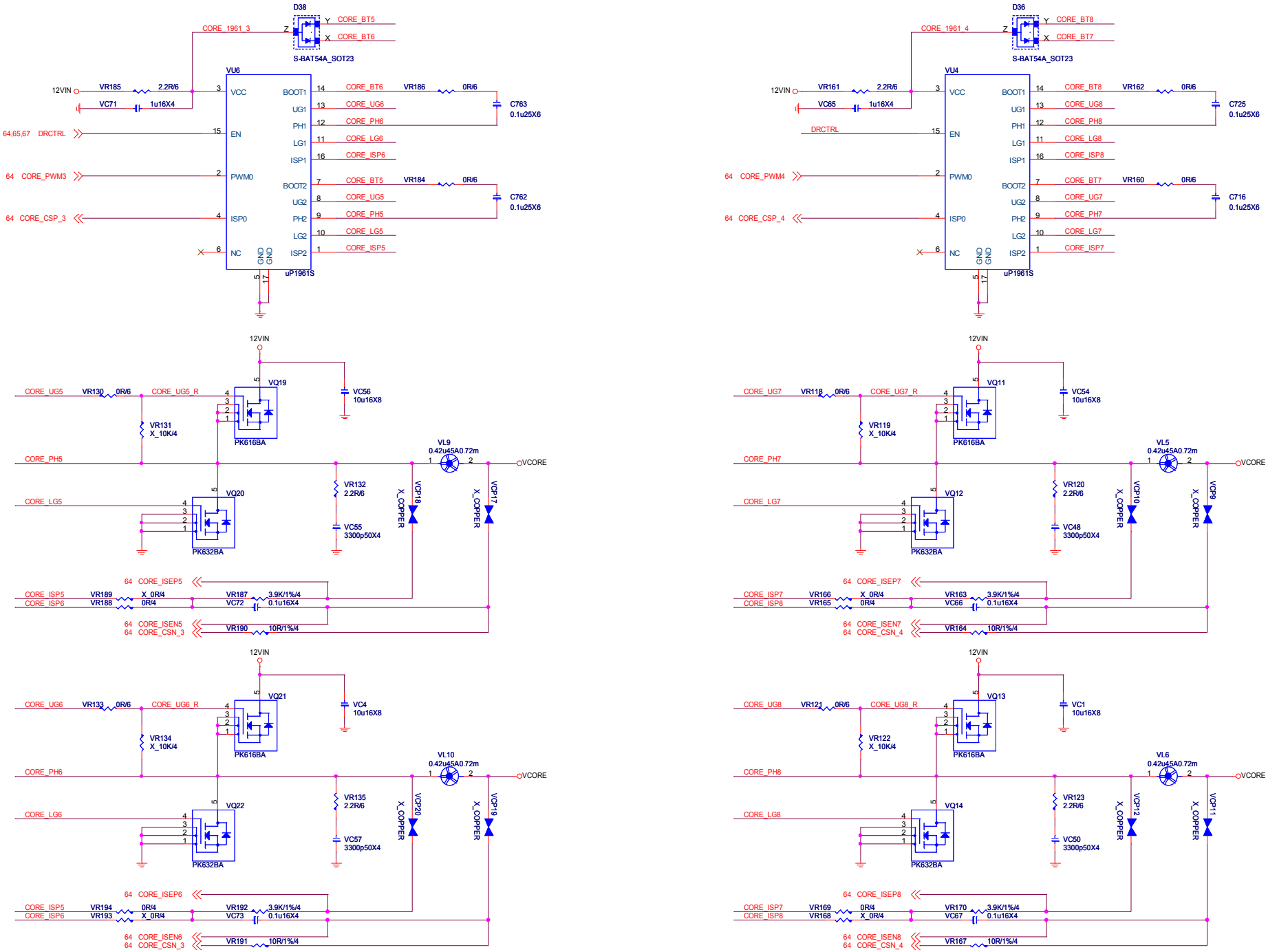

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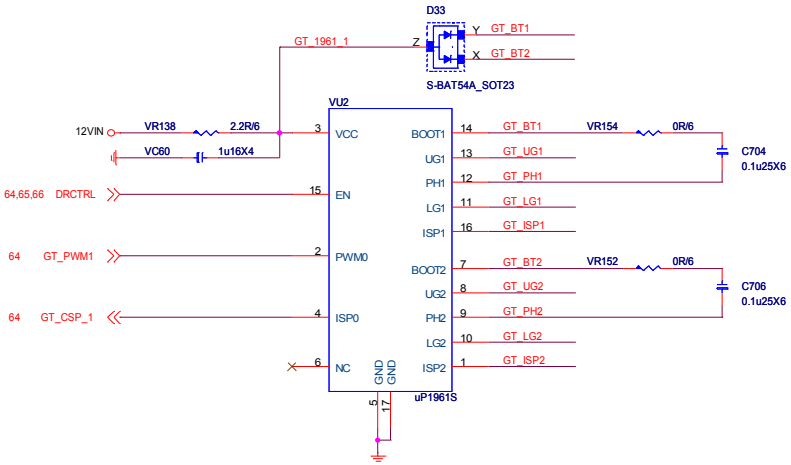

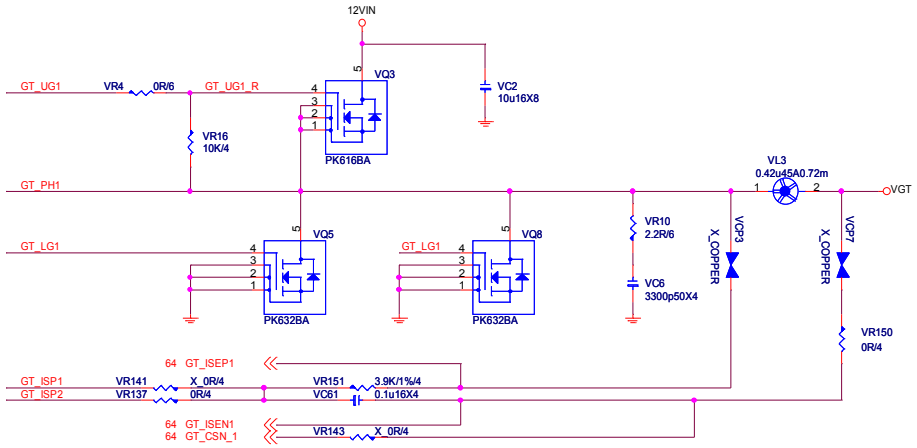

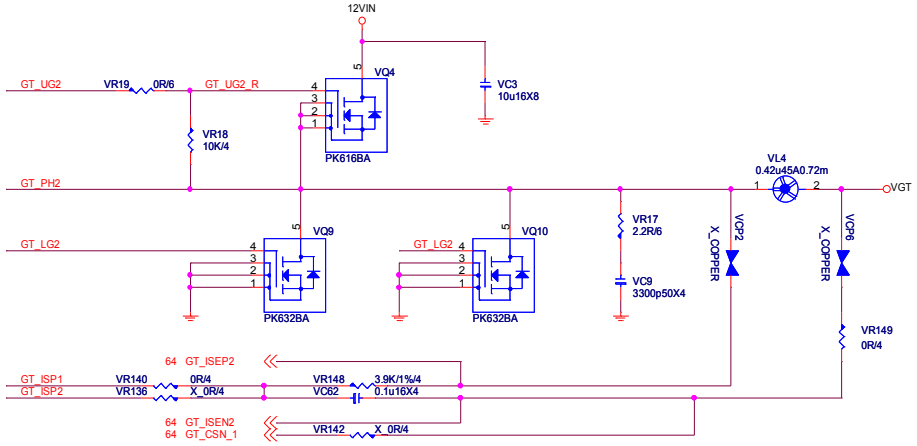

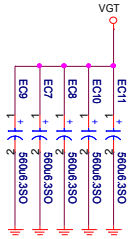

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SA Power:1.05V,11.1A

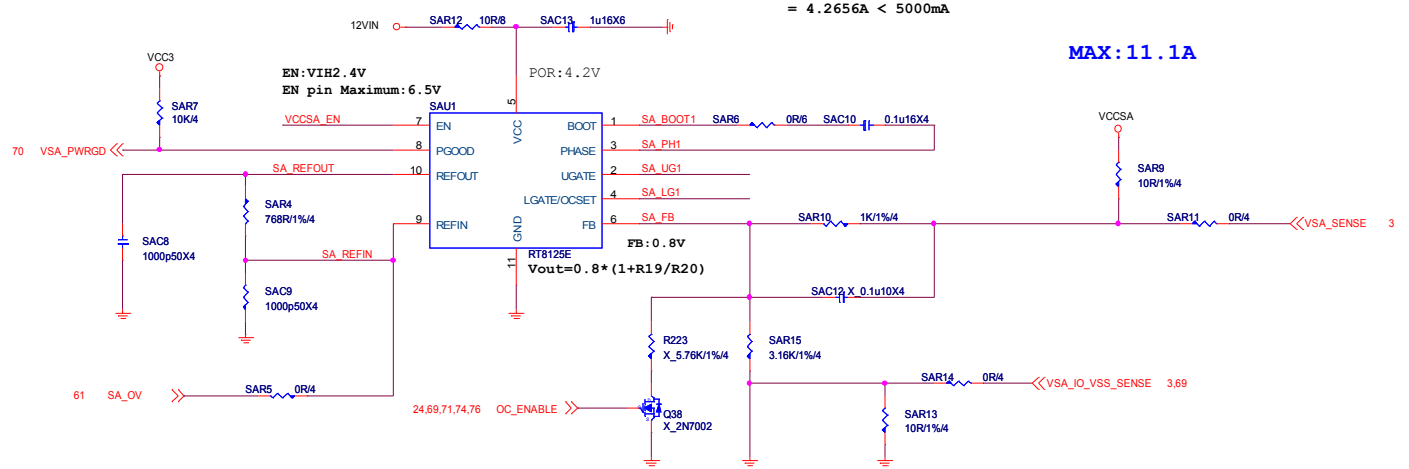
*OCP =11.1A*1.4=15.54A*
*Rocs(R15)=OCP*Rdson(Low side)3.4mohm]/10uA*
=15.54(3.4)mohm/10uA*
=5.2836Kohm

Rocs:5.2836K,OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

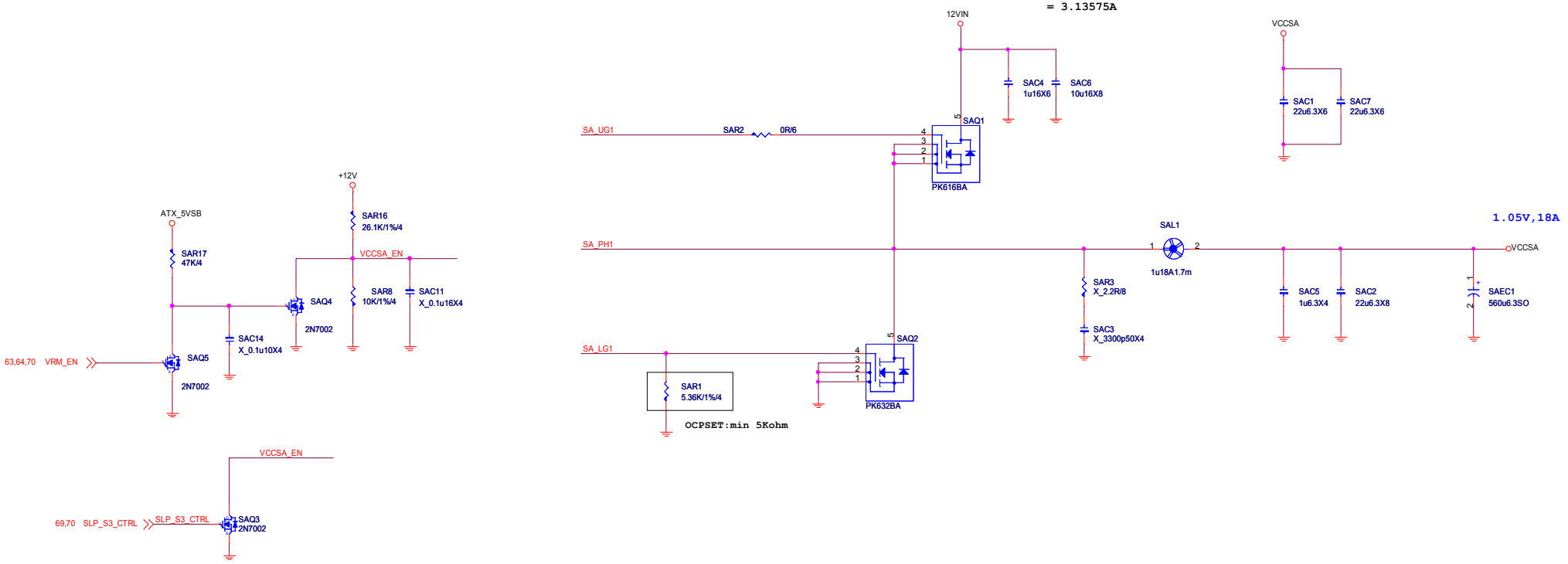
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

MAX:11.1A



Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1* 0.2825
= 3.13575A

1.05V,18A



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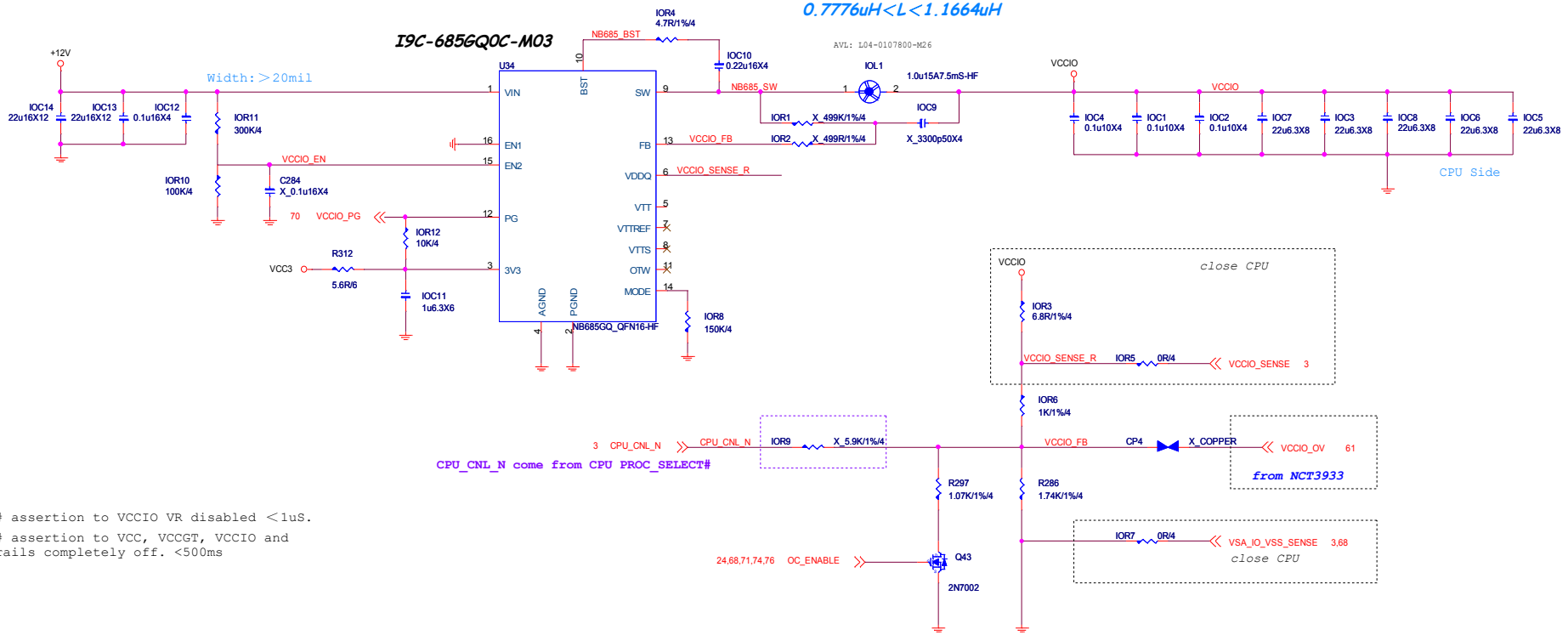
VCCIO Power:0.95V,5.5A

support OV=>NB685

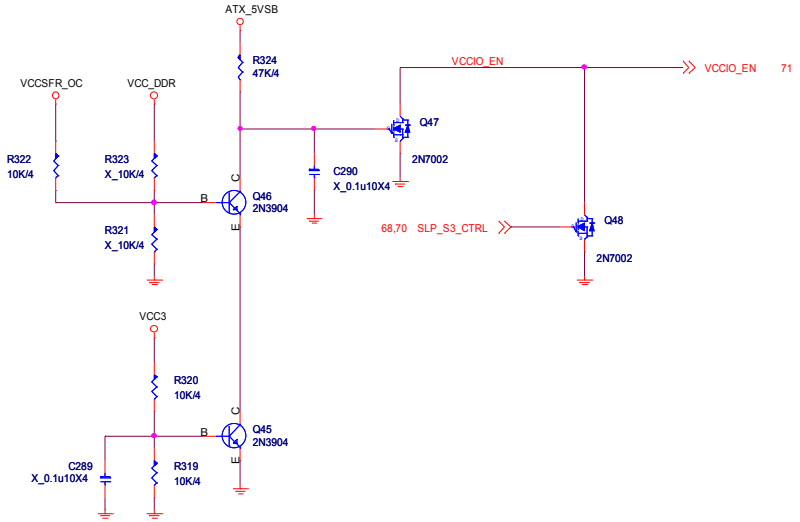
IMAX 10A
ILIMIT=10A~12A
*IOC=ILIMIT+40%*IMAX/2=12A~14A.*

0.7776uH<L<1.1664uH



SLP_S3# assertion to VCCIO VR disabled <1uS.

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms



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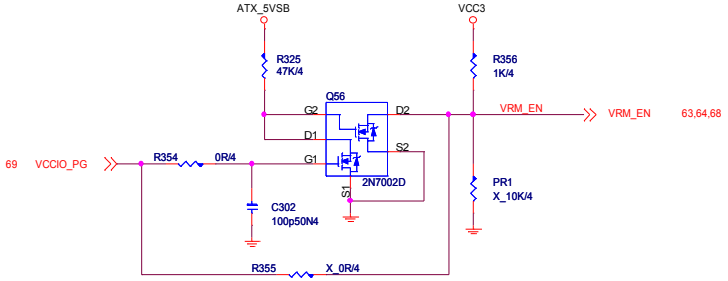

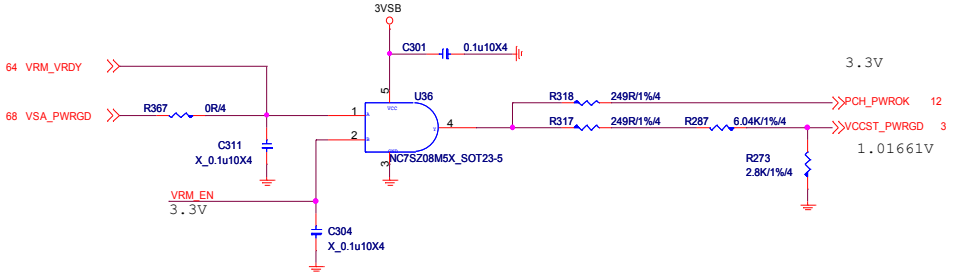

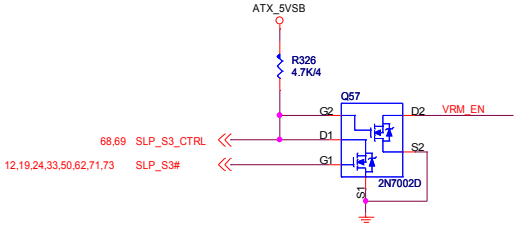

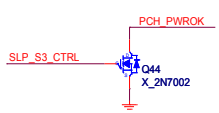

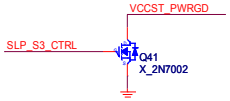

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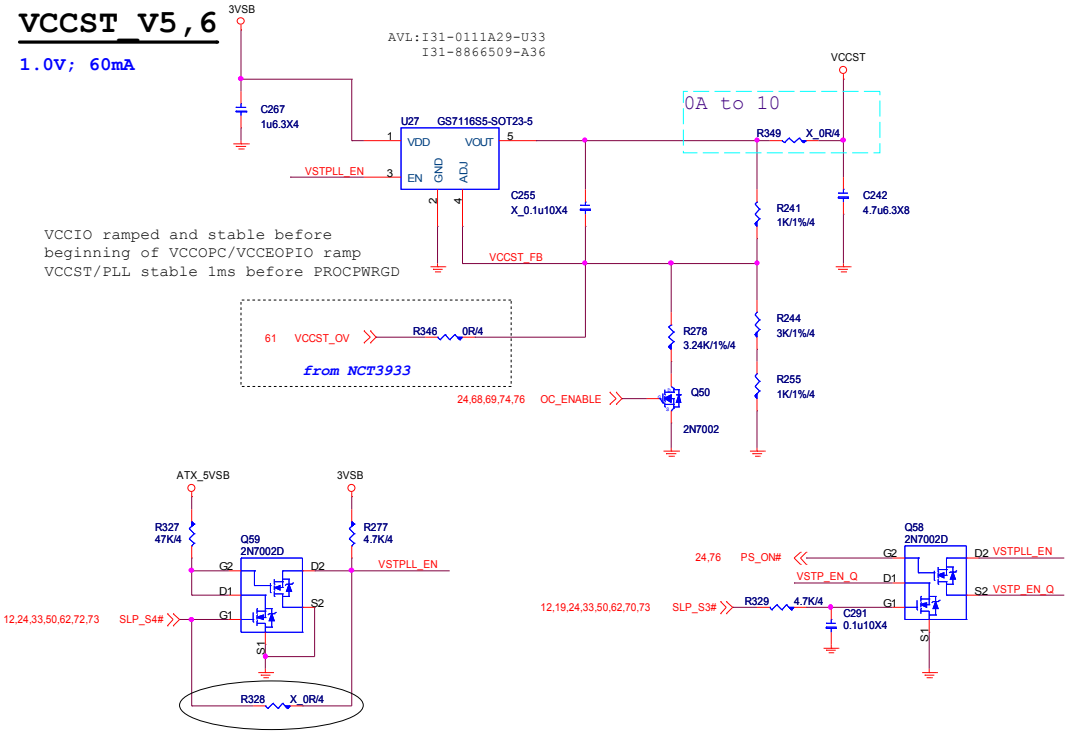
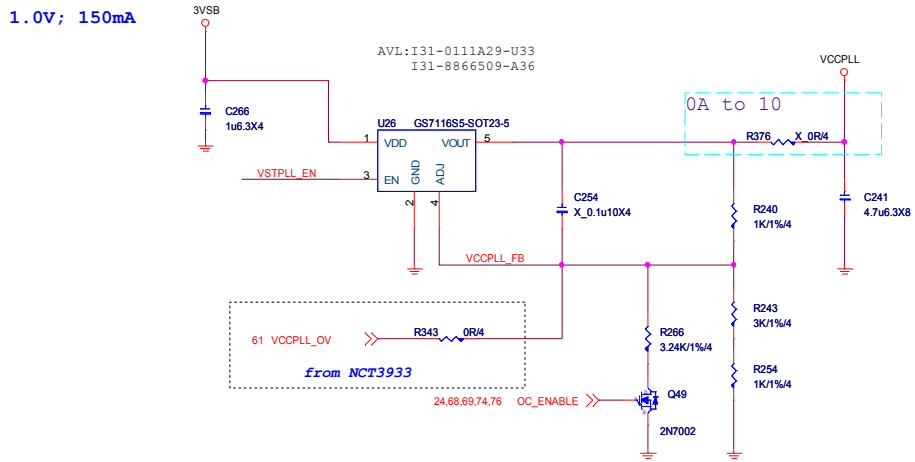
VCCST_V5,6

1.0V; 60mA



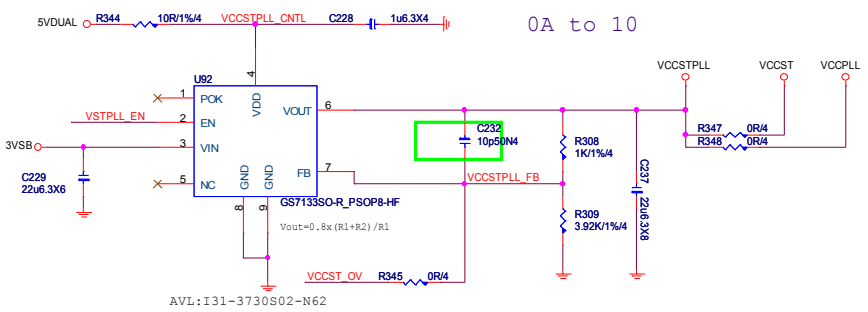
VCCPLL_V4

1.0V; 150mA



VCCSTPLL V4~6

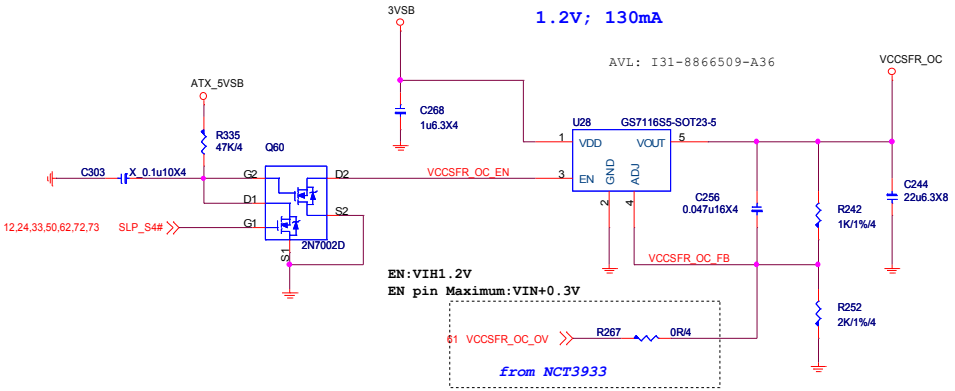
1.0V; 300mA



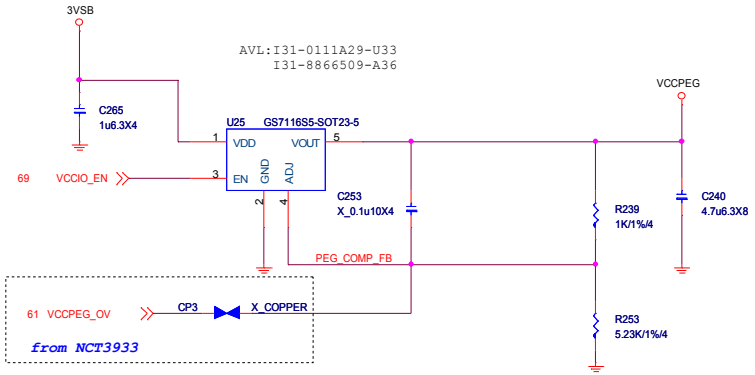
VCCPLL_OC

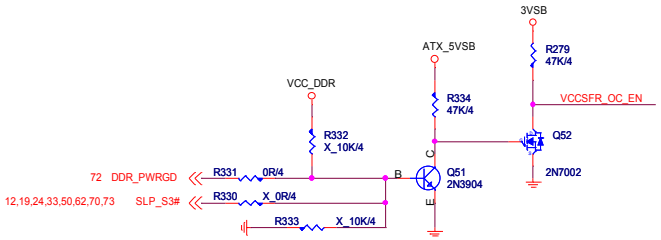
1.2V; 130mA

2014.08.21 update



PEG_COMP





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DDR4 Power:1.2V,13.5A

2.8A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

OCP:XXA for 2Phase

Imax: 13.2A

Iout ripple = 2.255A

L04-47B7730-T15

L04-22B7120-M26

Internal LDO 1.8V

PV Address: 0X21
SMB Address: 0X42

CONFIG: Configuration Table #3

Close to DDR PHASE1 XXX

pull up change by layout,Check level

3.12V

EN:VIH2V
EN pin Maximum:5.5V,RECOMMENDED:3.6V

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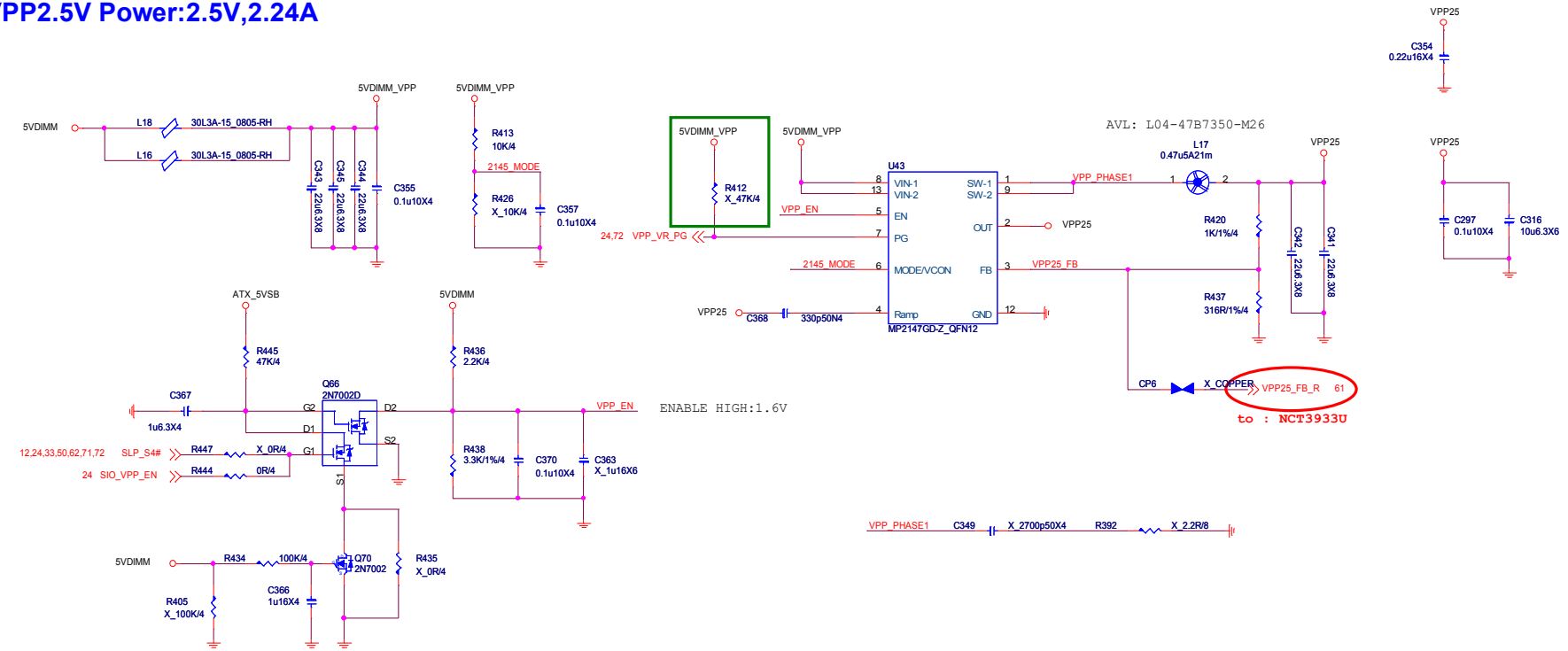
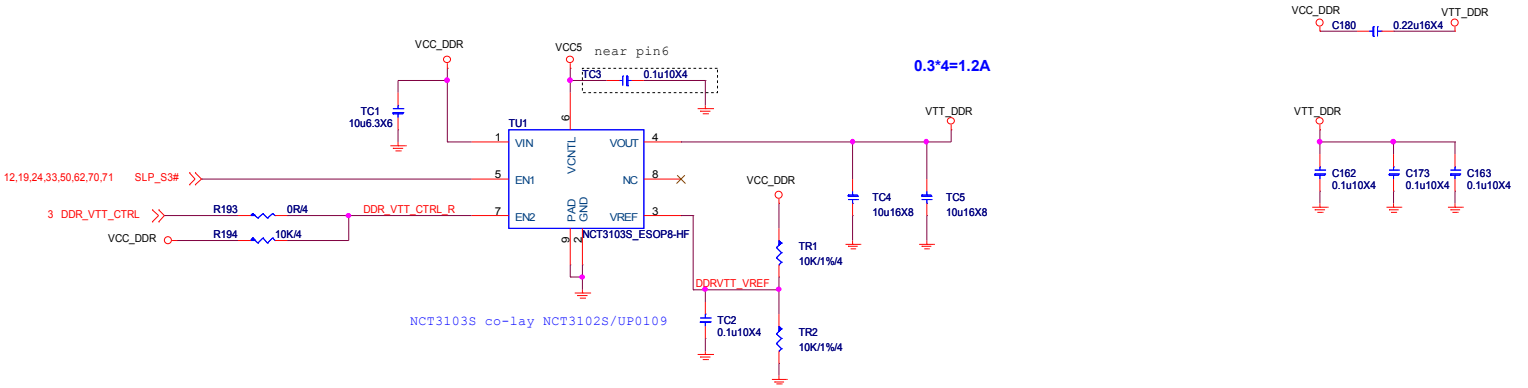
VPP2.5V Power:2.5V,2.24A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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PCH_1VSB Power:1.05V,12A

OCP = 16.21A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 10.664 * 4.2mohm / 10uA
= 6.71K

Rdson(low)
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

AVL: L04-47B7960-C08

MAX:12A

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

PLACE UNDER THE PCH

0728: add

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Part Number:N31-2061341-H06

12,33 PCH_SPI_CS0# — PCH_SPI_CS0#
12,33 PCH_SPI_MOSI — PCH_SPI_MOSI
12,33 PCH_SPI_MISO — PCH_SPI_MISO
12,33 PCH_SPI_CLK — PCH_SPI_CLK
12 PCH_SPI_IO2 — PCH_SPI_IO2
12 PCH_SPI_IO3 — PCH_SPI_IO3

SPI_VCC3 — R909 X_0R/6 — 3VSB

SPI CS# < 25pF
D0G-0402510-SI0

Close to JSPI1

SPI_VCC3 — R1133 X_1K/4 — PCH_SPI_MOSI
SPI_VCC3 — R1131 X_1K/4 — PCH_SPI_MISO

JSPI1
1 PCH_SPI_MISO
2 PCH_SPI_MOSI
3 PCH_SPI_CS0#
4 PCH_SPI_CLK
5 SPI_SW_SEL
6 PCH_SPI_IO2
7 PCH_SPI_IO3
H2X6[10]M-2PITCH_BLACK-RH-1

SPI_VCC3 — C688 0.1u10X4

D26 X_ESDSIS0402
D28 ESD-SFI0402

R895 0R/4

SPI_VCC3 — R880 X_2.2K/4

SPI_VCC3 — R1130 X_1K/4 — PCH_SPI_IO2
SPI_CS1# — PCH_SPI_MISO — R1125 15R/4 — SPI_MISO
R1124 15R/4 — SPI_IO2

SPI1
CS — VCC
DO(IO1) — HOLD(IO3)
WP(IO2) — CLK
GND — DI(IO0)
W25Q128FVSIQ-HF

SPI_VCC3 — C685 0.1u10X4
C686 10u6.3X6
SPI_IO3 — R1127 15R/4 — PCH_SPI_IO3
SPI_CLK — R1129 15R/4 — PCH_SPI_CLK
SPI_MOSI — R1128 15R/4 — PCH_SPI_MOSI

SPI_VCC3 — R1132 X_1K/4
R1126 X_1K/4

ATX_5VSB — R919 10K/4 — SPI_SW_SEL — SPI_SW_SEL 33

Fine tune for SA reset

12,24 RSMRST# — R828 200R/4 — RSMRST#_R — D22 X_S-RB751V-40
12,19,24 CHIP_PWGD — D23 S-RB751V-40
24,25,62 SIO_SLPSUS — D24 S-RB751V-40
12,24 PCH_DPWROK — D25 S-RB751V-40

For TL624-1.1 (SKYLAKE)
In skylake,PCH core is powered by VSB which need sink RSMRST#
to low by SPI_SW_SEL.

ATX_5VSB — C679 1u6.3X4 — R845 47K/4

U78 GS7116S5-SOT23-5
VDD — VOUT
EN — GND — ADJ

SPI_VCC3 — C684 680p50X4 — R881 10K/1%/4
SPI_FB — R875 3.09K/1%/4
C822 22u6.3X8

SIO_SLPSUS — Q124 2N7002

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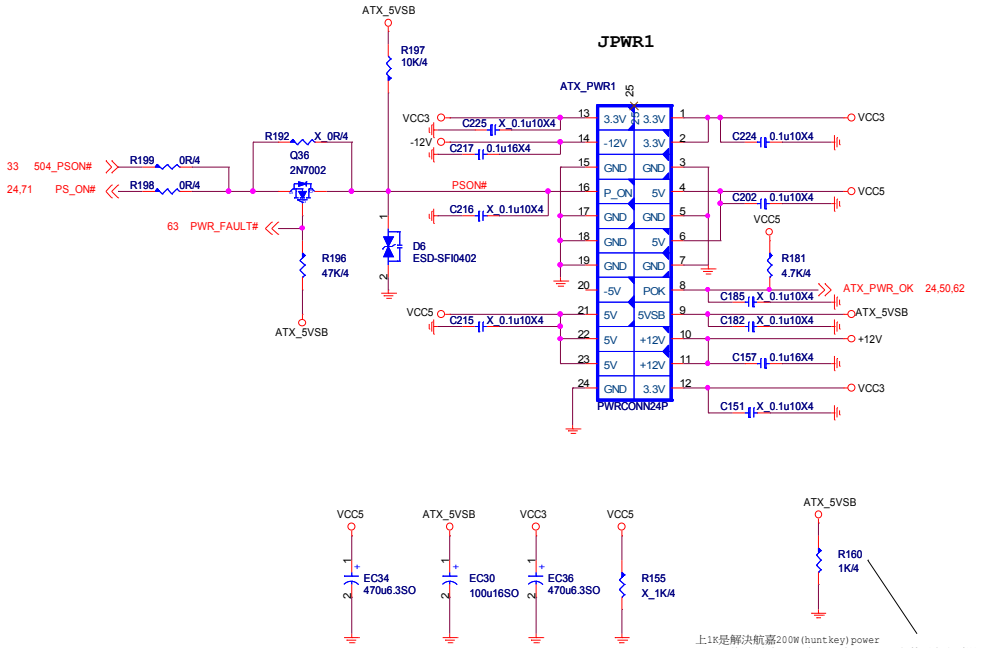
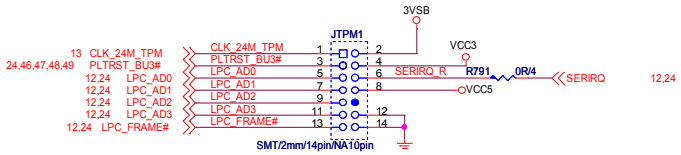
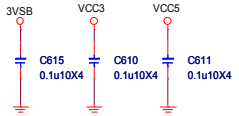
ATX POWER CONNECTOR

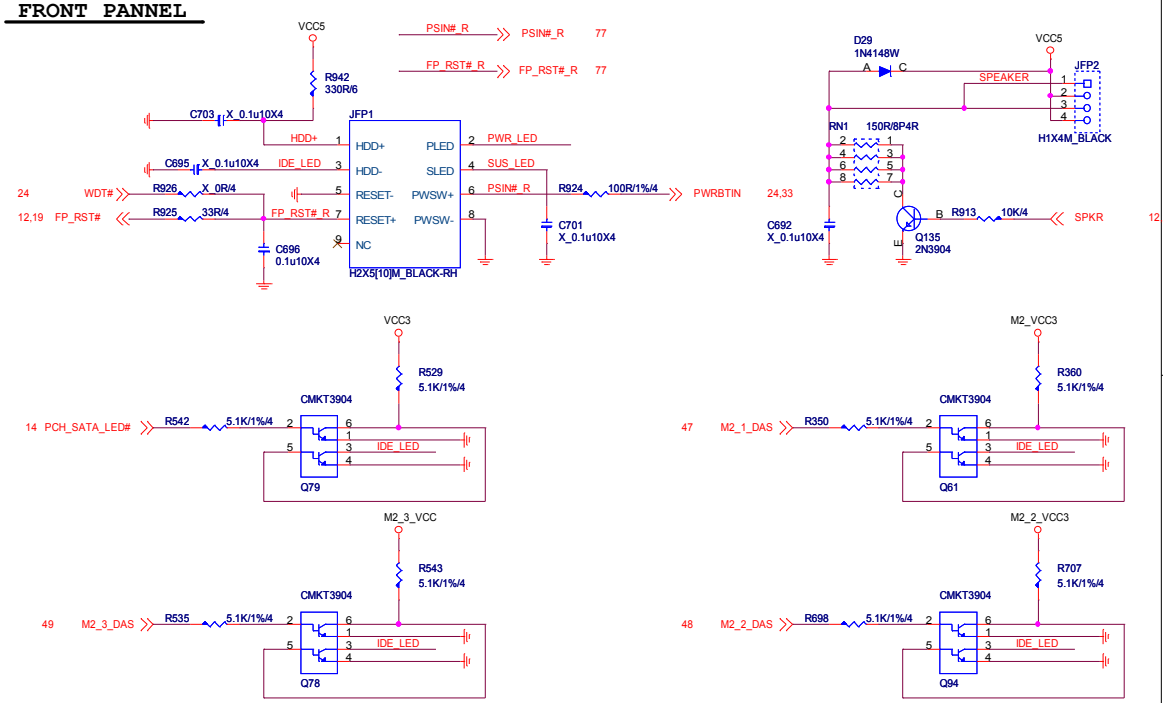


TPM Pin Header

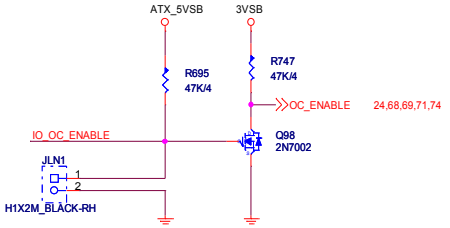




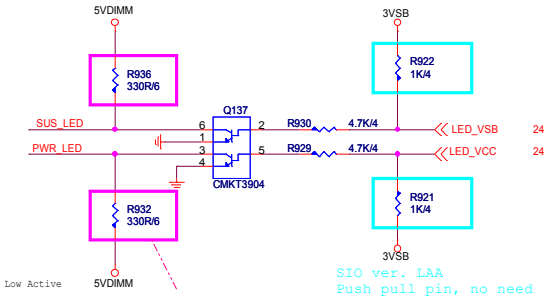
FRONT PANNEL



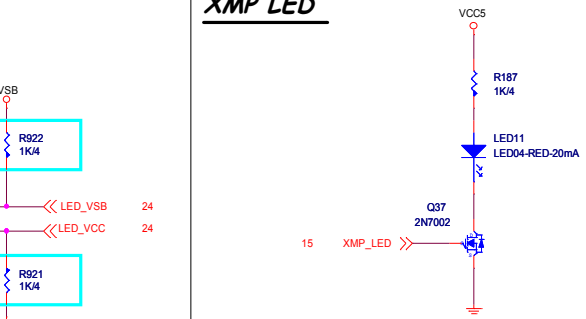
TOP PC USE Only



Front Panel LED



XMP LED



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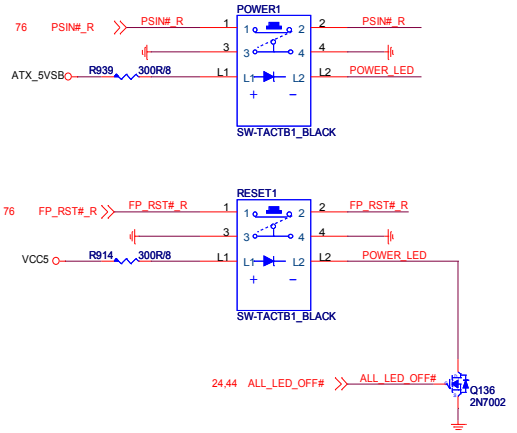
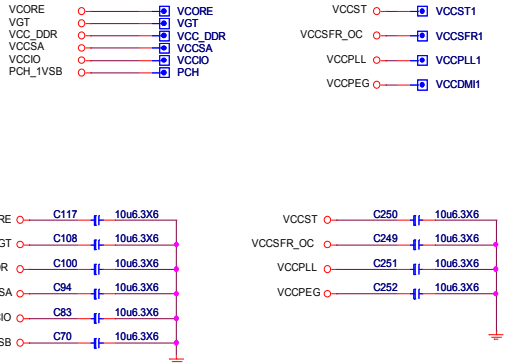
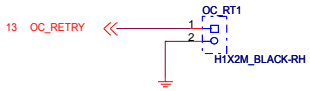
PWR/RST Botton



Vcheck

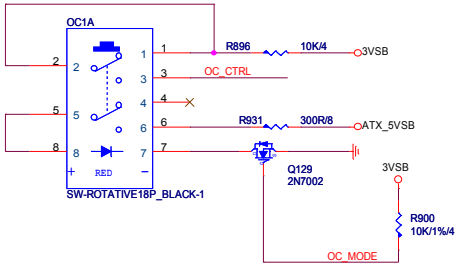


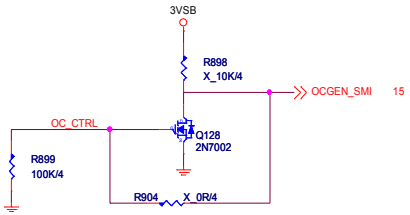
OC retry

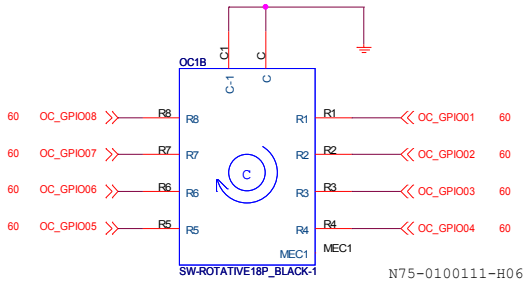


OC fail

OC Genie

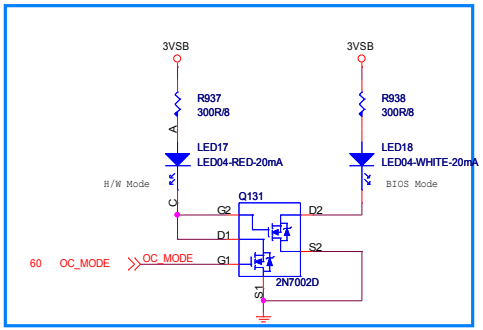




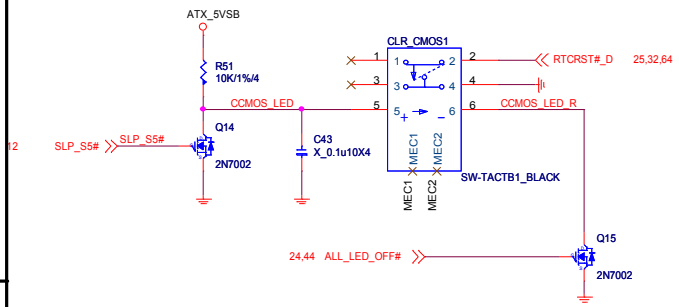


N75-0100111-H06

H/W & BIOS Mode LED

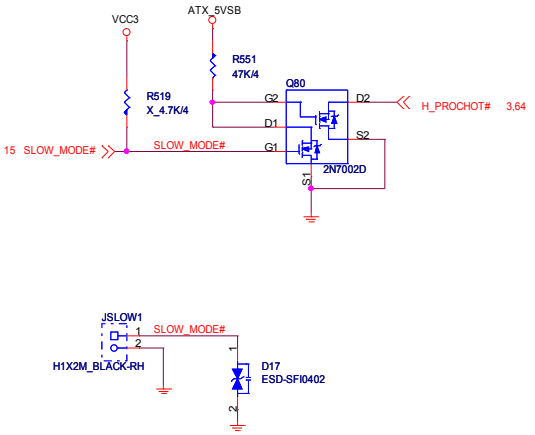


Clear CMOS button



LED LIGHTING RULE
S0/S3/S4 : LED OFF
S5 : LED ON

Slow Mode



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MS-7A57		
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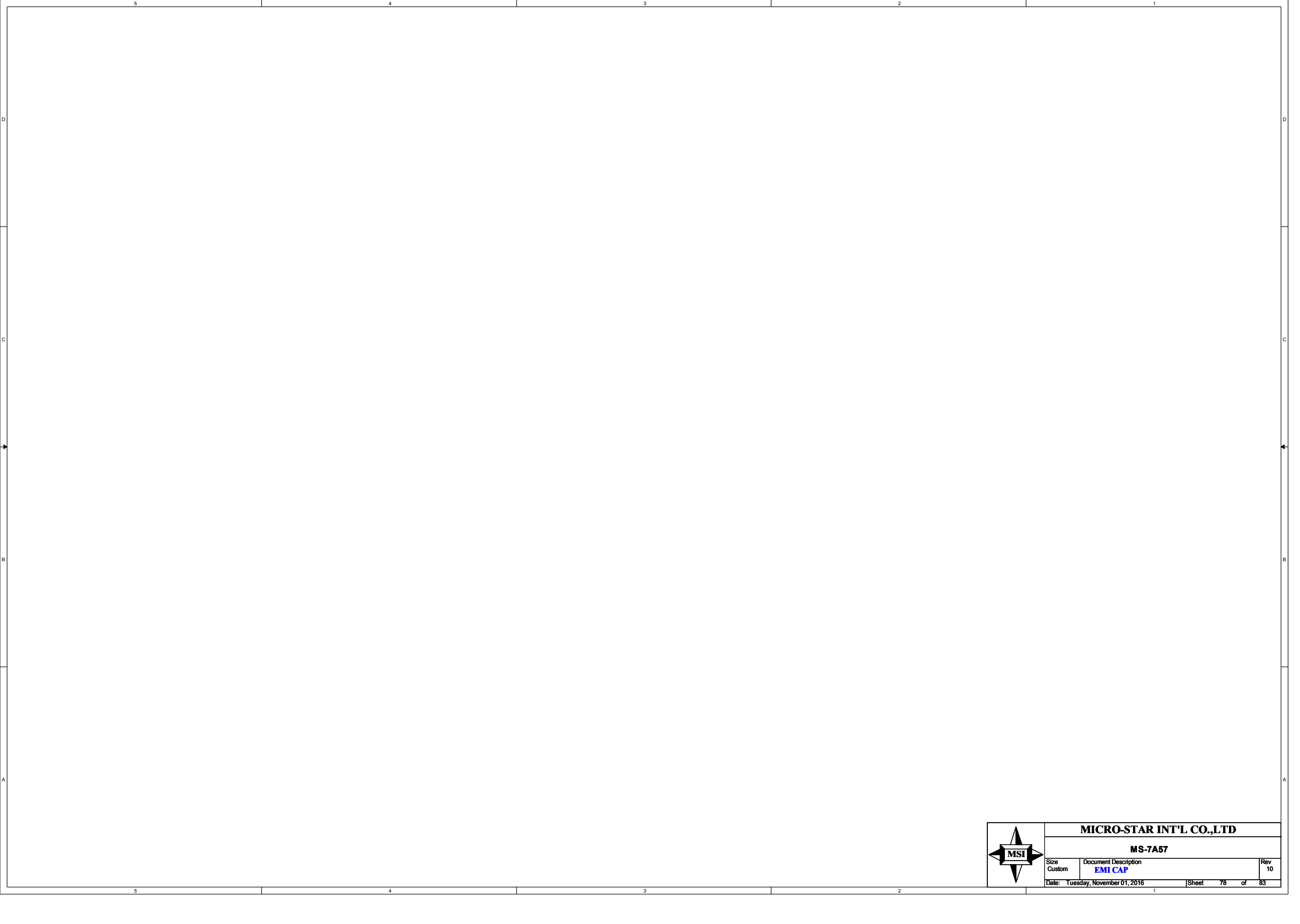

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Size: Custom	Document Description: EMI CAP		Rev: 10
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PCB1

7A57_10

PD0-07A5710-G37,精成-深圳,130,寶安恩斯邁廠(MSIS)
PD0-07A5710-E48,競華,20,寶安恩斯邁廠(MSIS)

CPU_H1

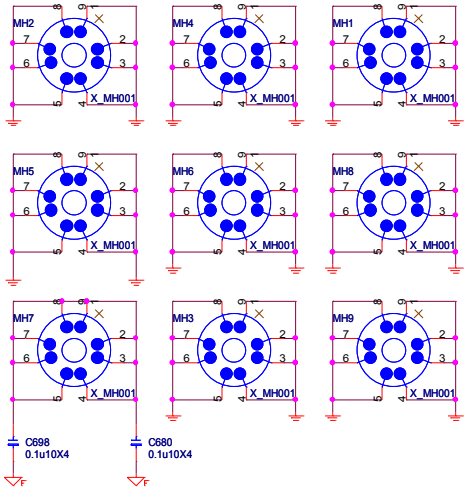
CPU_H1

BAT1_X1

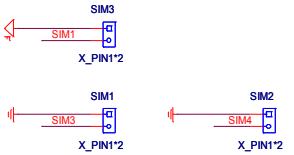
BAT-BCR2032P-RH

VIRTU_LA1 — Label VIRTU — AMI
VIRTU_LA2 — Label VIRTU — HDMI
VIRTU_LA3 — Label VIRTU — NAHIMIC
VIRTU_LA4 — Label VIRTU — SLI
VIRTU_LA5 — Label VIRTU — SSE
VIRTU_LA6 — Label VIRTU — OC_MYLAR

Mounting Holes



Simulation



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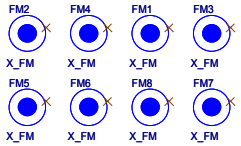
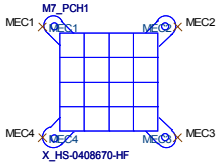
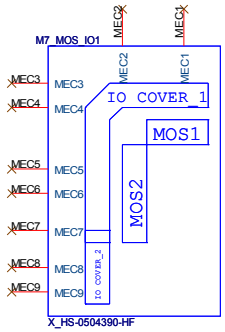


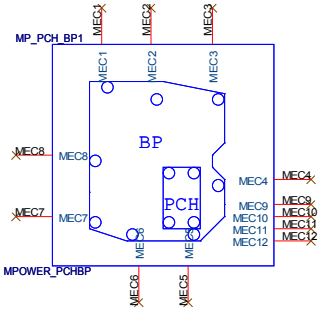
HEATSINK

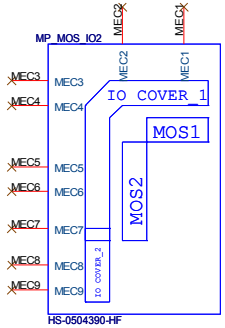
M7

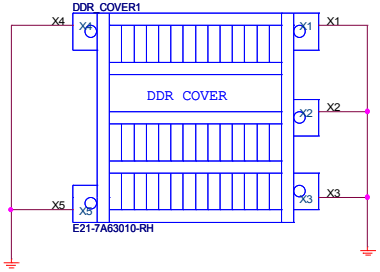


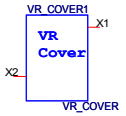


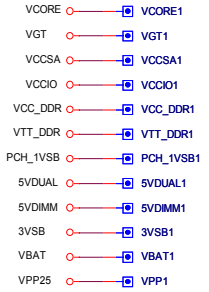
MPOWER











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