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# MS-7176

Version 0A

## CPU:

Intel Prescott ( L2=2MB ) - 3.4G & Above  
 Intel Cendar Mill (65nm) - 3.73G & Above  
 Intel Smithfield (90nm Dual core)

## System Chipset:

Intel Lakeport - GMCH (North Bridge)  
 Intel ICH7R (South Bridge)

## On Board Chipset:

BIOS -- FWH EEPROM  
 Aliza Codec -- ALC882  
 LPC Super I/O -- W83627THF  
 LAN-- Intel Tekoa(82573)/EKronR(82562)  
 CLOCK -- ICS954519  
 1394 Controller -- VT6307 2pots  
 IDE RAID Controller -- VT6410

## Main Memory:


DDR II \* 4 (Max 4GB)

## Expansion Slots:

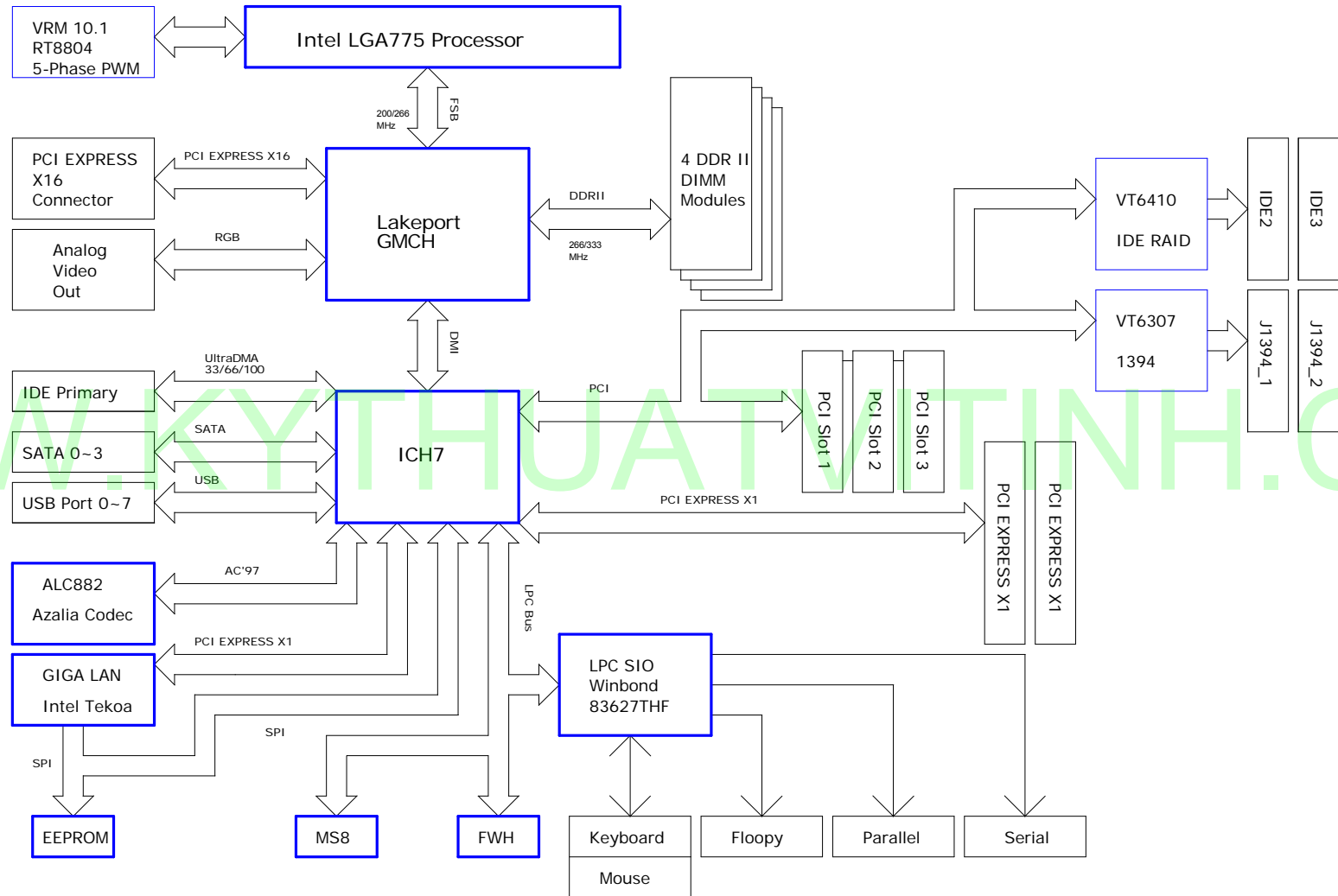
PCI2.3 SLOT \* 3  
 PCI EXPRESS X1 SLOT \* 2  
 PCI EXPRESS X16 SLOT

## RickTek PWM:

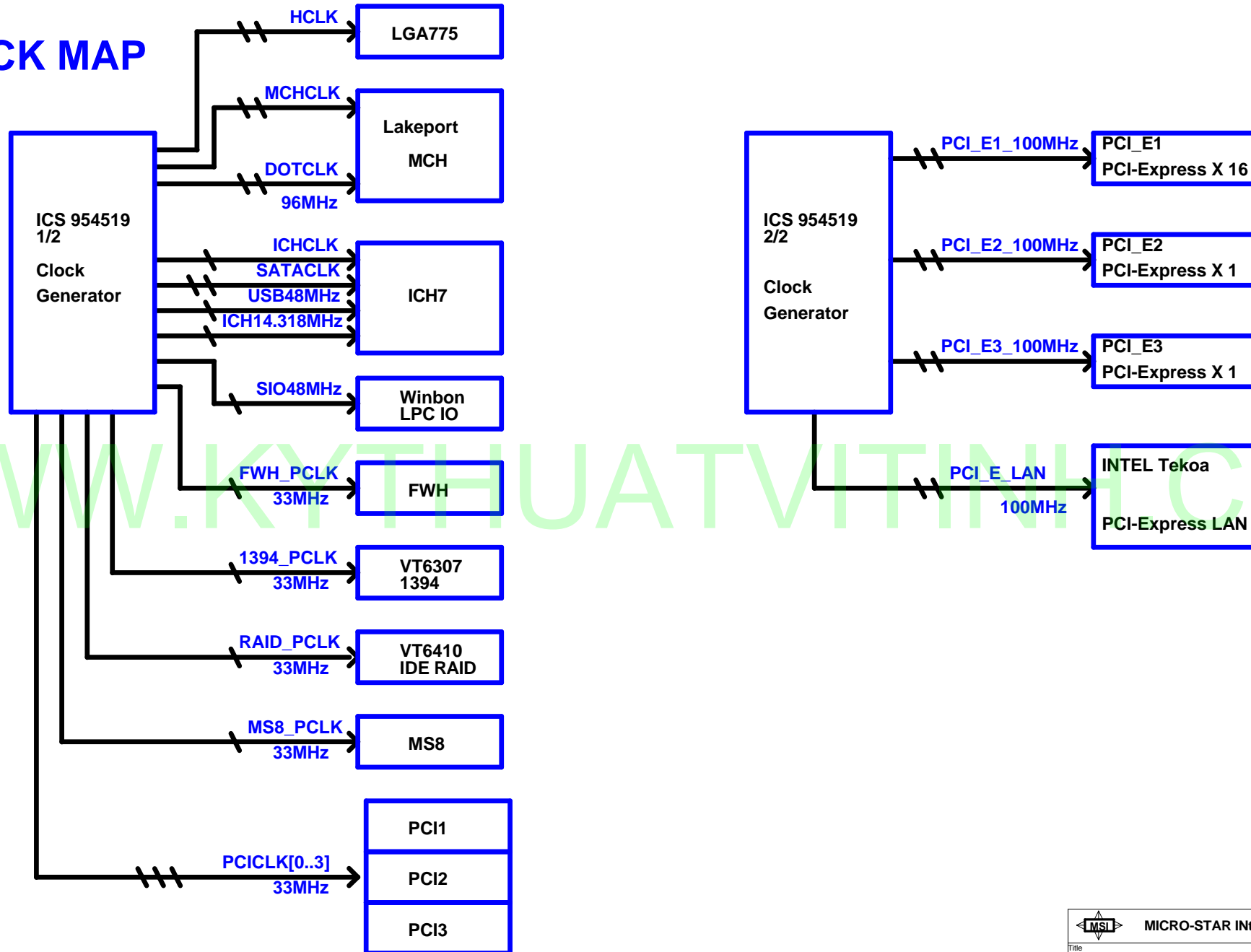
Controller: RT8804 5 Phases

 MICRO-STAR INT'L CO., LTD.	
Title COVER SHEET	
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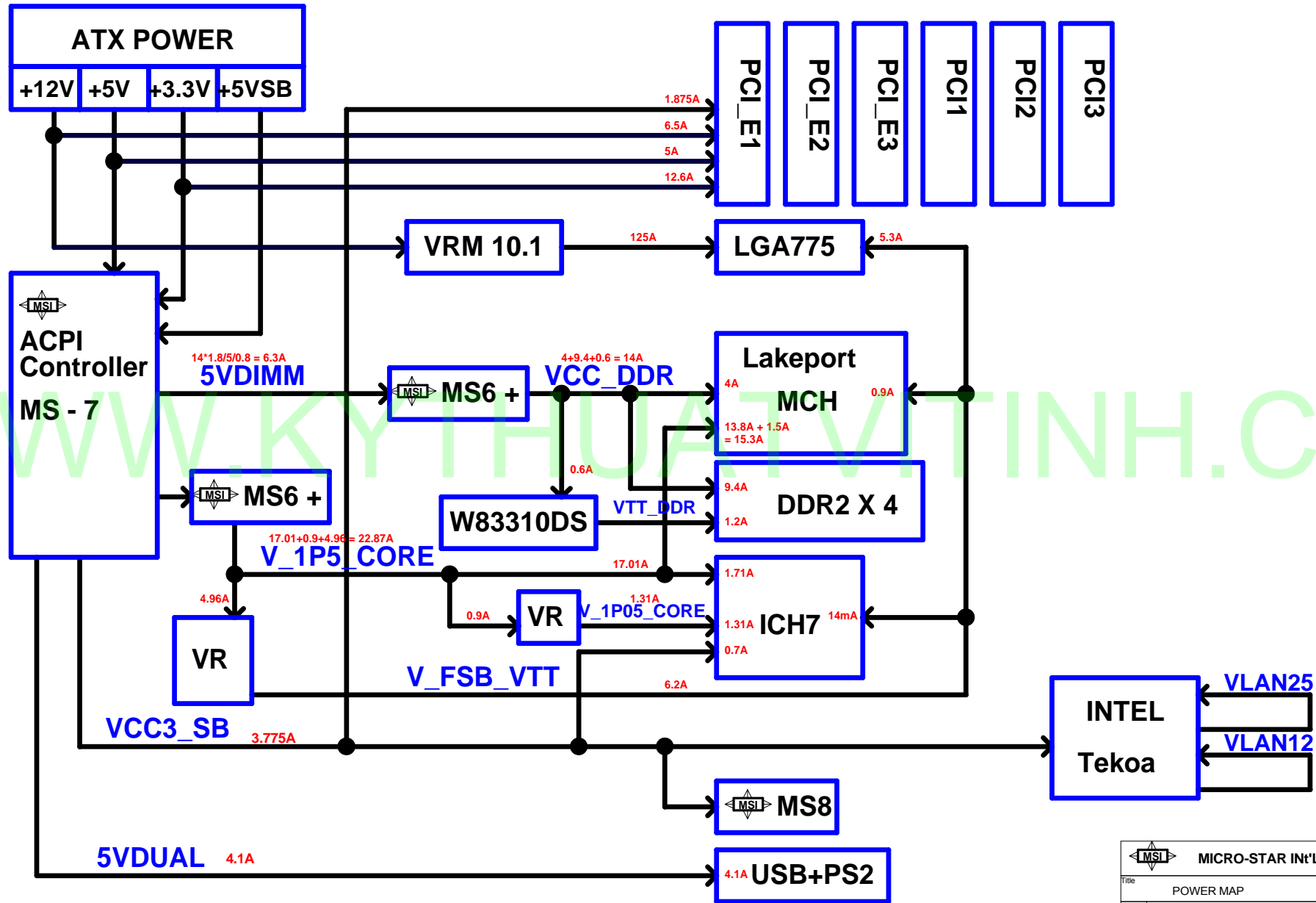
# Block Diagram



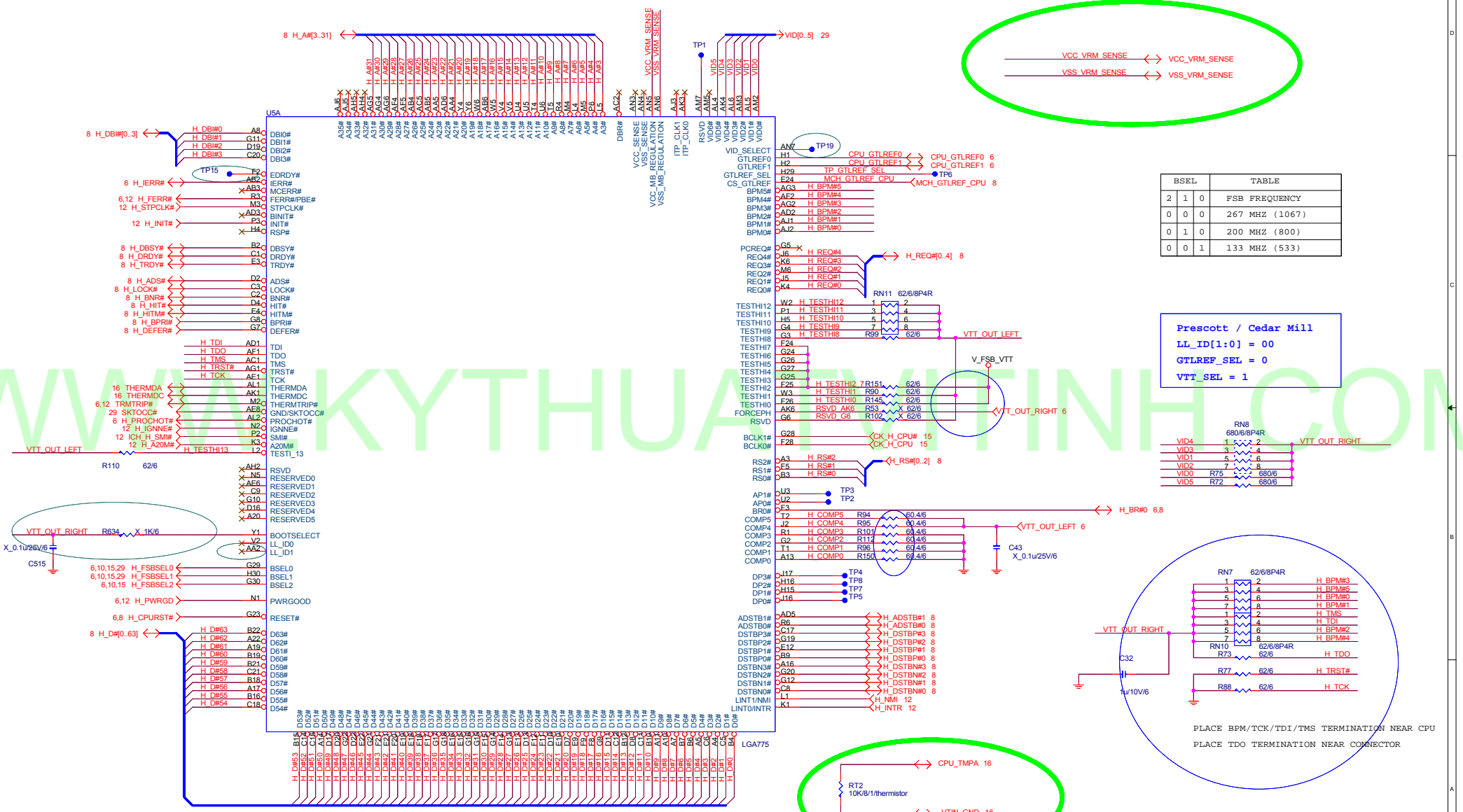
# CLOCK MAP



# POWER MAP

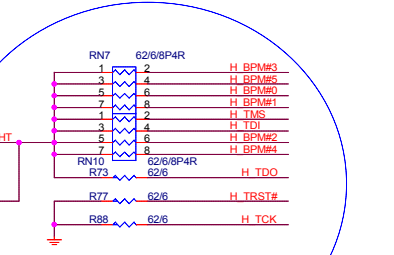
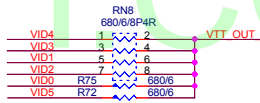


# CPU SIGNAL BLOCK

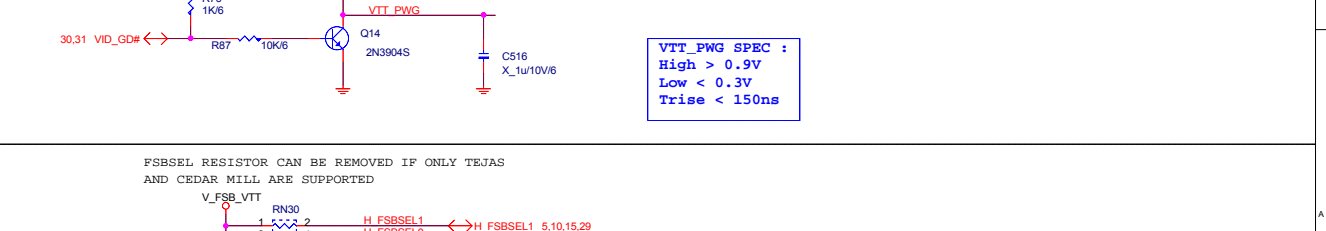
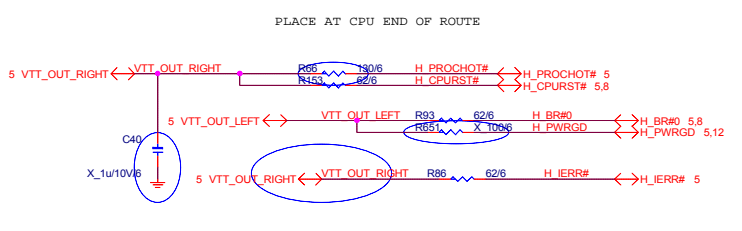
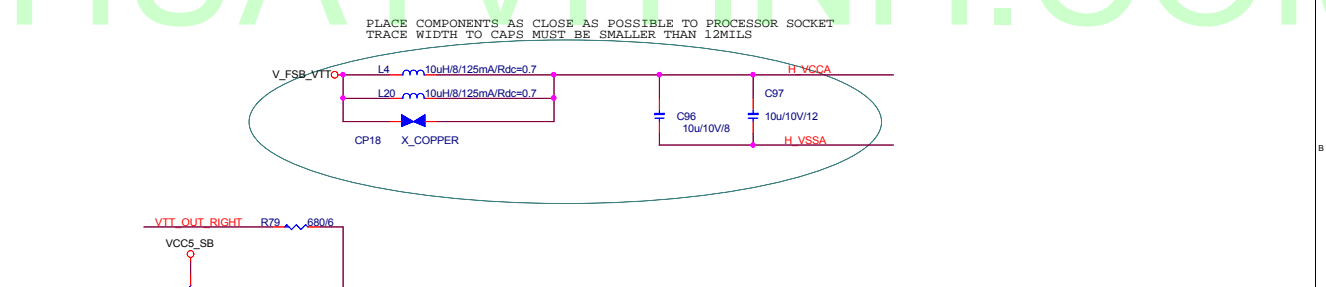
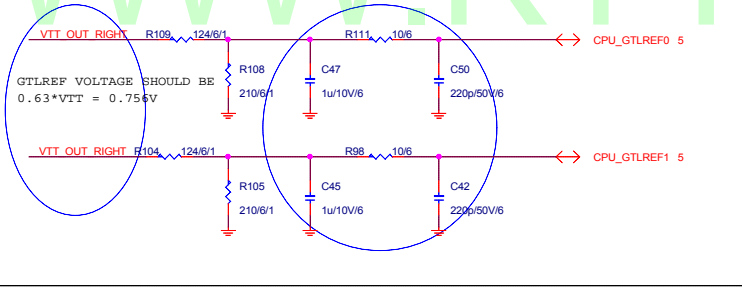
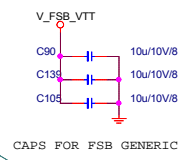
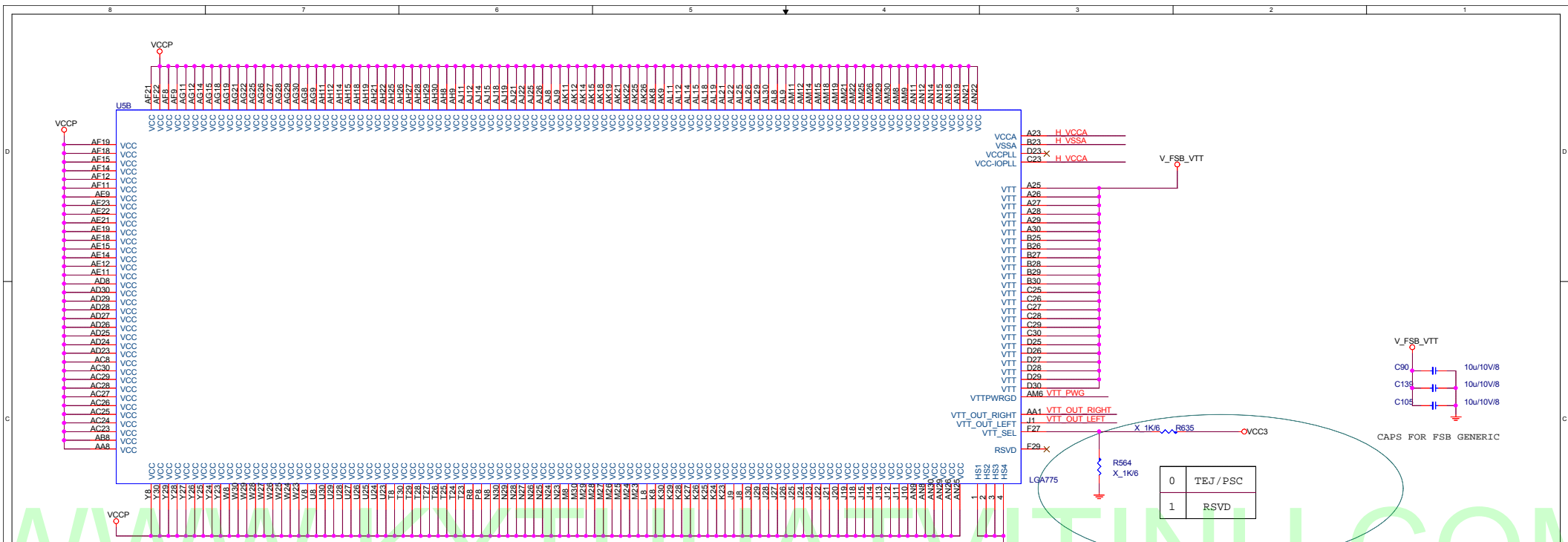


BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	267 MHZ (1067)
0 1 0	200 MHZ (800)
0 0 1	133 MHZ (533)

Prescott / Cedar Mill  
 LL\_ID[1:0] = 00  
 GTLREF\_SEL = 0  
 VTT\_SEL = 1

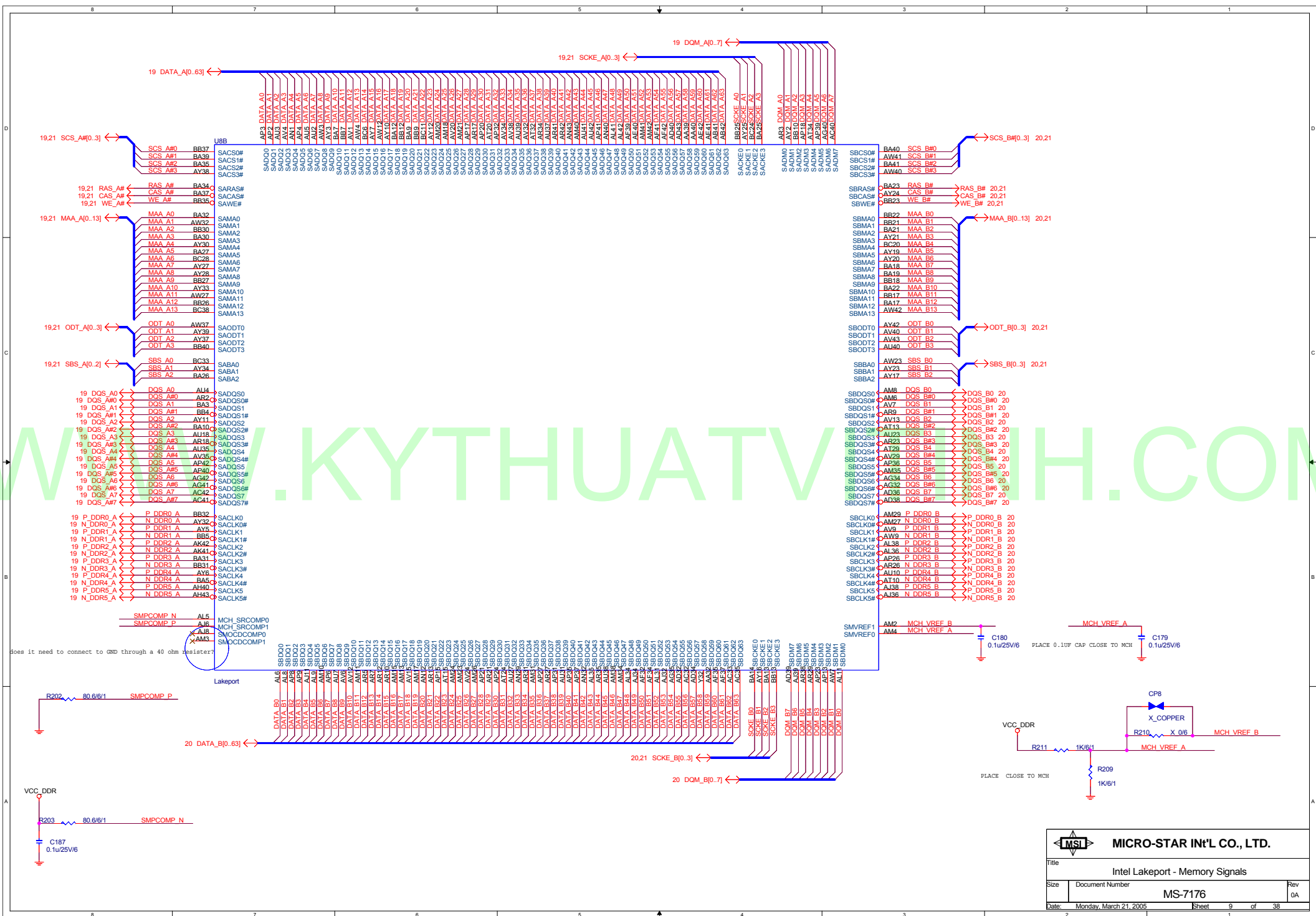


PLACE BPM/TCK/TDI/TMS TERMINATION NEAR CPU  
 PLACE TDO TERMINATION NEAR CONNECTOR









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Does it need to connect to GND through a 40 ohm resistor?

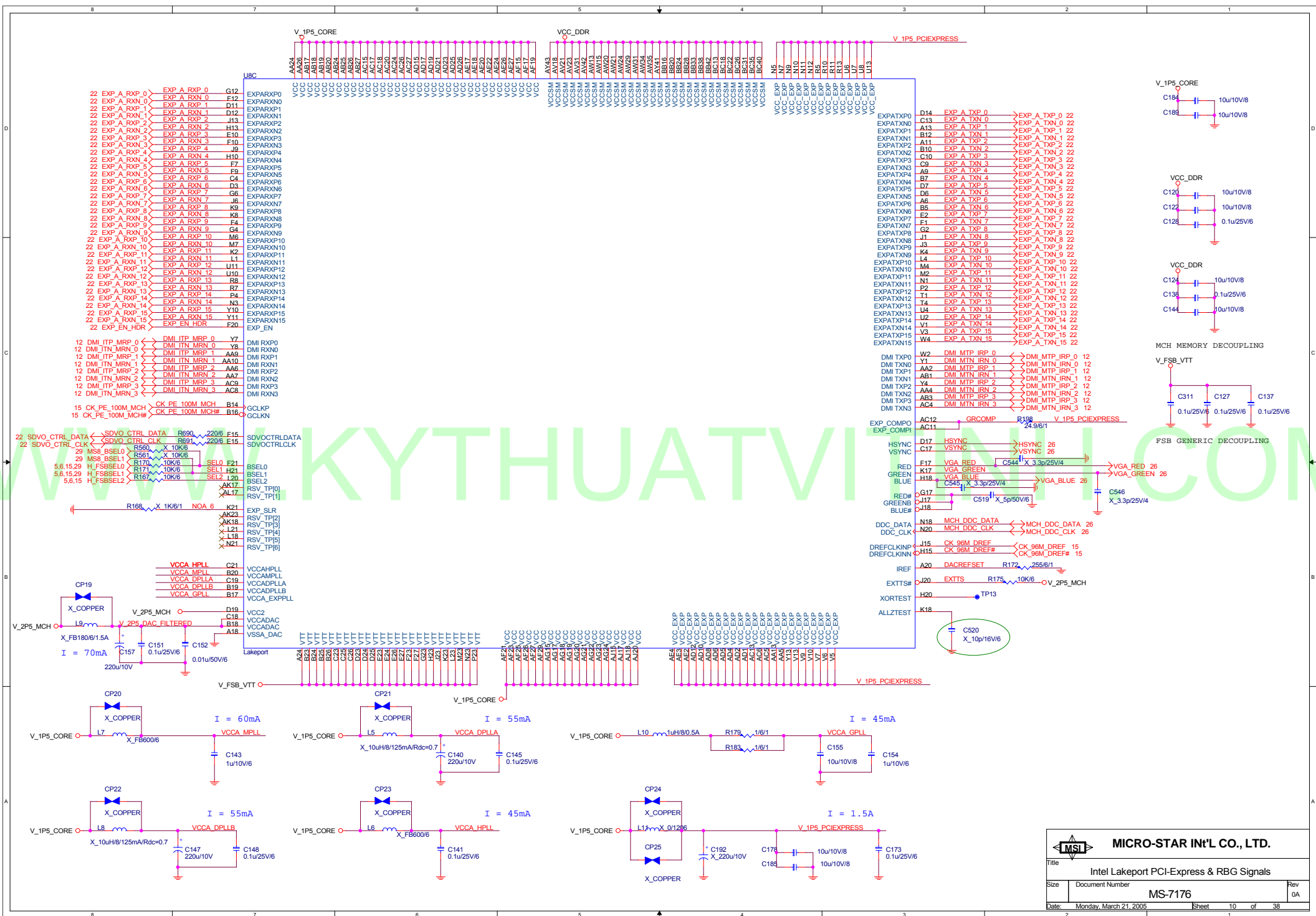
Lakeport

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Title: Intel Lakeport - Memory Signals

Size: Document Number: MS-7176 Rev: 0A

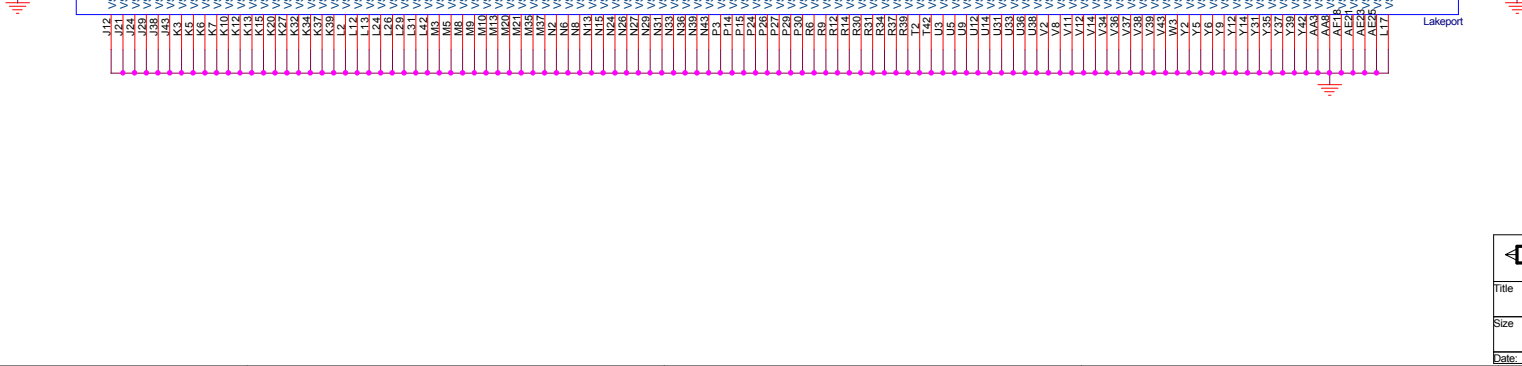
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A16 VSS  
 A22 VSS  
 A26 VSS  
 A31 VSS  
 A35 VSS  
 B4 VSS  
 B6 VSS  
 B9 VSS  
 B11 VSS  
 B13 VSS  
 B21 VSS  
 B22 VSS  
 B28 VSS  
 B33 VSS  
 B38 VSS  
 C3 VSS  
 C5 VSS  
 C7 VSS  
 C12 VSS  
 C14 VSS  
 C22 VSS  
 C43 VSS  
 D2 VSS  
 D5 VSS  
 D10 VSS  
 D16 VSS  
 D20 VSS  
 D21 VSS  
 E3 VSS  
 E4 VSS  
 E7 VSS  
 E9 VSS  
 F12 VSS  
 F13 VSS  
 E17 VSS  
 F18 VSS  
 F20 VSS  
 E21 VSS  
 F32 VSS  
 F2 VSS  
 F6 VSS  
 F13 VSS  
 F18 VSS  
 F26 VSS  
 F34 VSS  
 F42 VSS  
 G3 VSS  
 G5 VSS  
 G7 VSS  
 G9 VSS  
 G10 VSS  
 G13 VSS  
 G16 VSS  
 G18 VSS  
 G20 VSS  
 G21 VSS  
 G24 VSS  
 G27 VSS  
 G29 VSS  
 G32 VSS  
 G35 VSS  
 G38 VSS  
 H12 VSS  
 H17 VSS  
 H26 VSS  
 H27 VSS  
 J2 VSS  
 J5 VSS  
 J7 VSS  
 J10 VSS

VSS AL33  
 VSS AL32  
 VSS AL27  
 VSS AL24  
 VSS AL23  
 VSS AL21  
 VSS AL18  
 VSS AL15  
 VSS AL13  
 VSS AL12  
 VSS AL10  
 VSS AL7  
 VSS AL3  
 VSS AL2  
 VSS AK30  
 VSS AK29  
 VSS AK26  
 VSS AK24  
 VSS AJ37  
 VSS AJ35  
 VSS AJ33  
 VSS AJ31  
 VSS AJ30  
 VSS AH10  
 VSS AH7  
 VSS AH42  
 VSS AG39  
 VSS AG38  
 VSS AG37  
 VSS AG36  
 VSS AG33  
 VSS AG31  
 VSS AG30  
 VSS AF43  
 VSS AF38  
 VSS AF36  
 VSS AF33  
 VSS AE5  
 VSS AE3  
 VSS AE2  
 VSS AE1  
 VSS AD42  
 VSS AD37  
 VSS AD35  
 VSS AD33  
 VSS AD13  
 VSS AD11  
 VSS AD9  
 VSS AD7  
 VSS AC39  
 VSS AC38  
 VSS AC37  
 VSS AC36  
 VSS AC31  
 VSS AC23  
 VSS AC21  
 VSS AC14  
 VSS AC10  
 VSS AC7  
 VSS AC3  
 VSS AC2  
 VSS AB43  
 VSS AB2  
 VSS AA36  
 VSS AA33  
 VSS AA31  
 VSS AA23  
 VSS AA21  
 VSS AA14  
 VSS AA12  
 VSS AA11



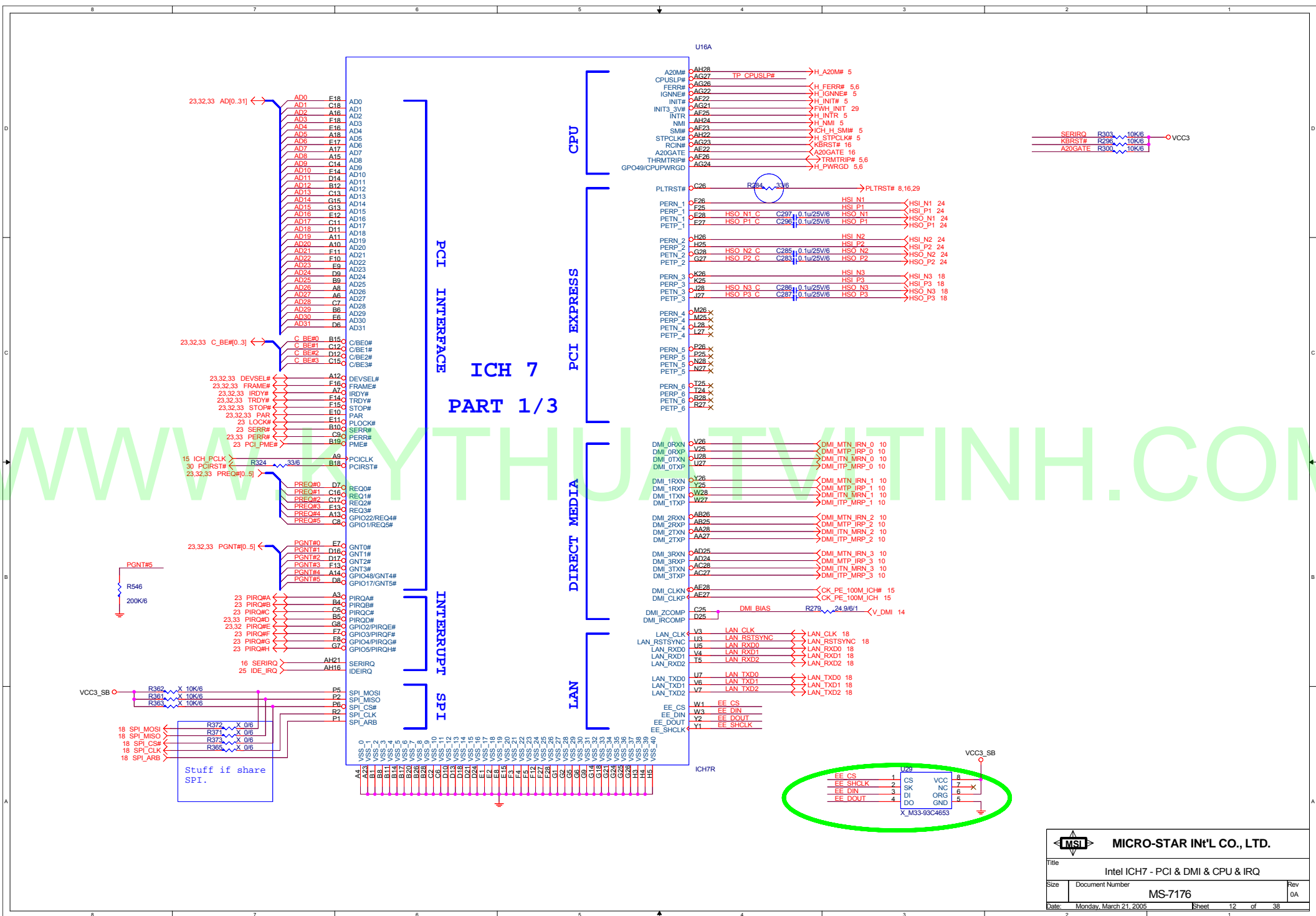
J12 VSS  
 J24 VSS  
 J28 VSS  
 J33 VSS  
 J43 VSS  
 K3 VSS  
 K6 VSS  
 K7 VSS  
 K10 VSS  
 K13 VSS  
 K15 VSS  
 K20 VSS  
 K22 VSS  
 K26 VSS  
 K29 VSS  
 K36 VSS  
 L2 VSS  
 L12 VSS  
 L24 VSS  
 L26 VSS  
 L29 VSS  
 L33 VSS  
 L42 VSS  
 M3 VSS  
 M6 VSS  
 M8 VSS  
 M9 VSS  
 M10 VSS  
 M21 VSS  
 M25 VSS  
 M27 VSS  
 N2 VSS  
 N6 VSS  
 N15 VSS  
 N18 VSS  
 N24 VSS  
 N27 VSS  
 N28 VSS  
 N29 VSS  
 N31 VSS  
 N33 VSS  
 N36 VSS  
 N38 VSS  
 N43 VSS  
 P14 VSS  
 P15 VSS  
 P22 VSS  
 P27 VSS  
 P29 VSS  
 P33 VSS  
 R6 VSS  
 R8 VSS  
 R9 VSS  
 R12 VSS  
 R20 VSS  
 R30 VSS  
 R31 VSS  
 R34 VSS  
 R36 VSS  
 R39 VSS  
 T7 VSS  
 U2 VSS  
 U3 VSS  
 U5 VSS  
 U6 VSS  
 U7 VSS  
 U14 VSS  
 U14 VSS  
 U14 VSS  
 U33 VSS  
 U33 VSS  
 U38 VSS  
 U38 VSS  
 V2 VSS  
 V7 VSS  
 V8 VSS  
 V9 VSS  
 Y14 VSS  
 Y14 VSS  
 Y31 VSS  
 Y35 VSS  
 Y39 VSS  
 Y42 VSS  
 AA3 VSS  
 AA3 VSS  
 AE1 VSS  
 AE1 VSS  
 AE2 VSS  
 AE2 VSS  
 L17 VSS


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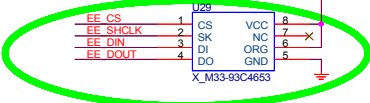
Title: Intel Lakeport - GND

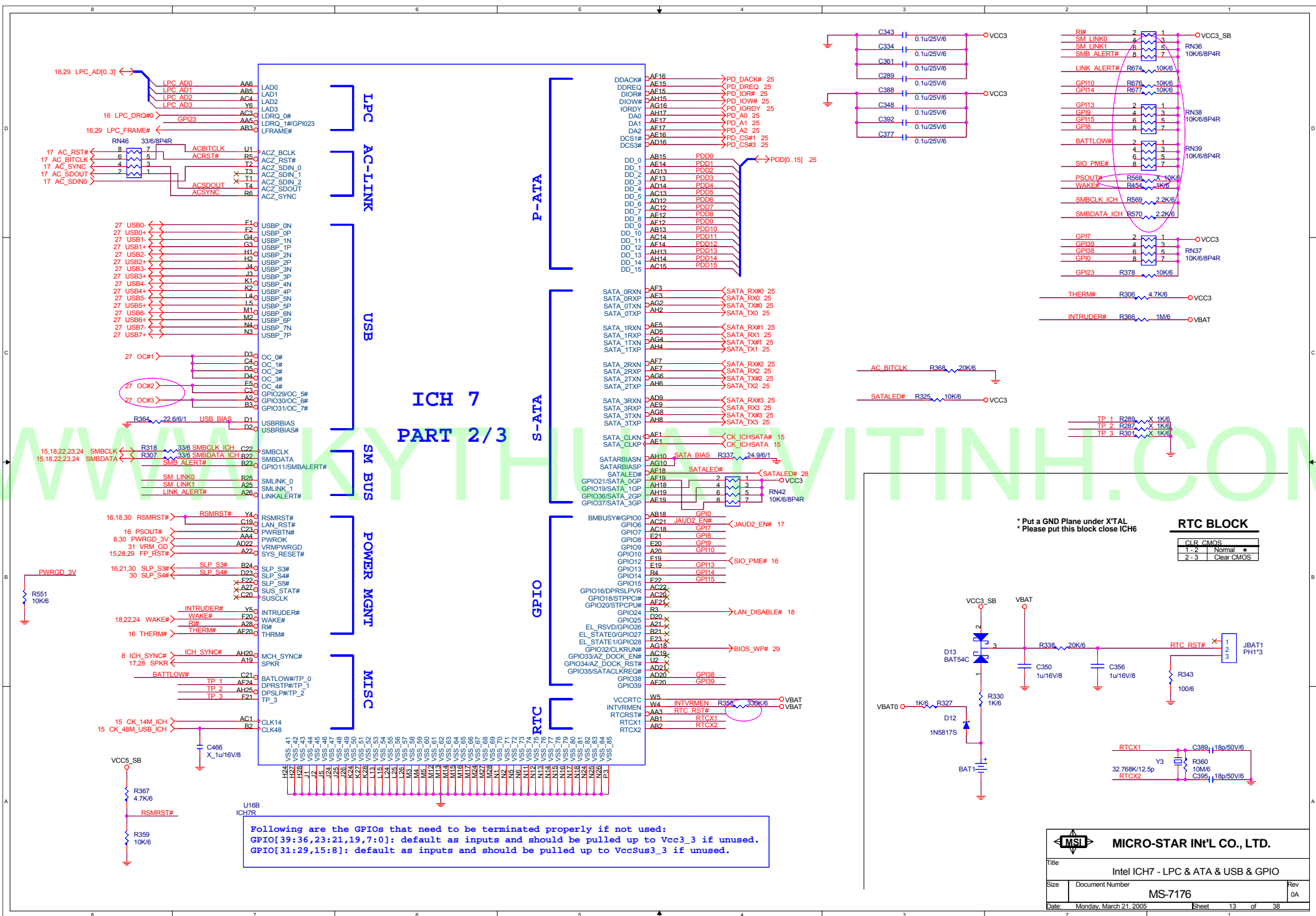
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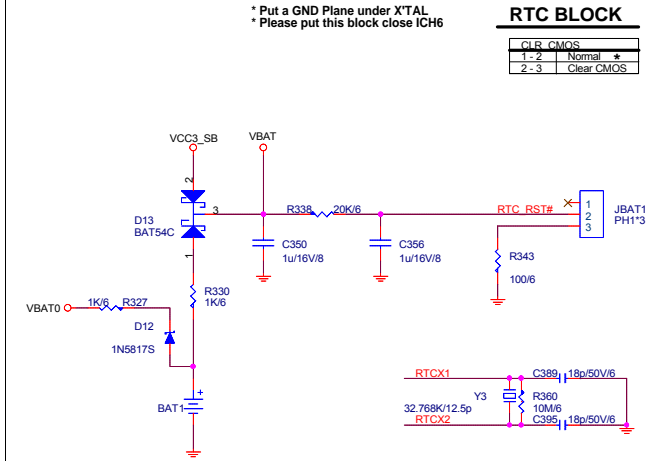
**ICH 7  
PART 1/3**





**ICH 7  
PART 2/3**

Following are the GPIOs that need to be terminated properly if not used:  
 GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3 if unused.  
 GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus\_3\_3 if unused.



\* Put a GND Plane under XTAL  
 \* Please put this block close ICH6

**RTC BLOCK**

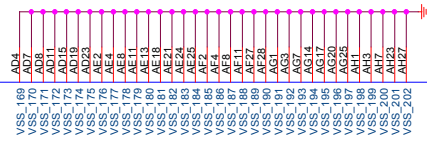
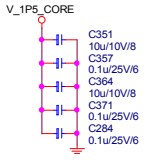
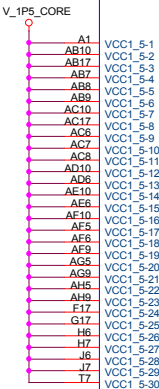
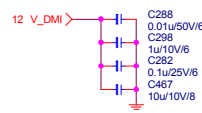
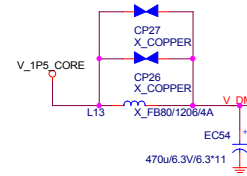
CLR CMOS	
1 - 2	Normal
2 - 3	Clear CMOS

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Title: Intel ICH7 - LPC & ATA & USB & GPIO

Size: Document Number MS-7176 Rev 0A

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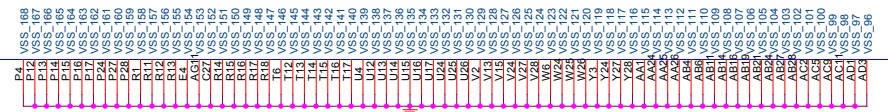
1.5V DMI POWER

ICH 7  
PART 3/3

S0 POWER

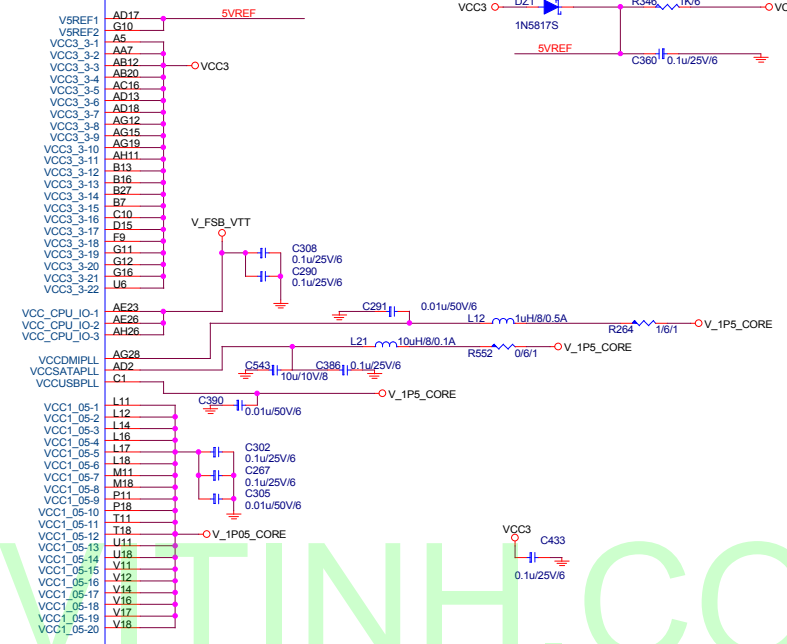
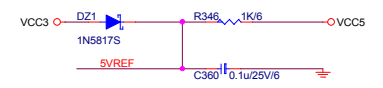
S5 POWER

1.5V CORE WELL POWER



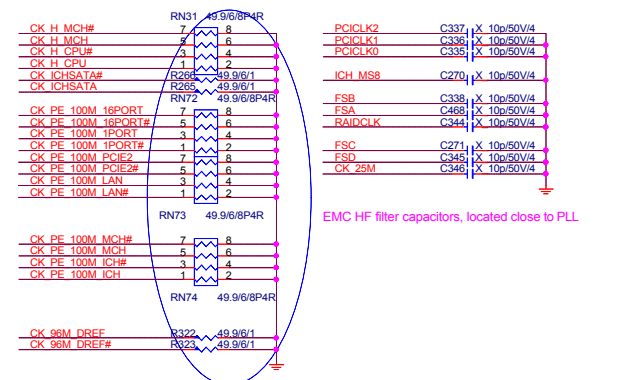
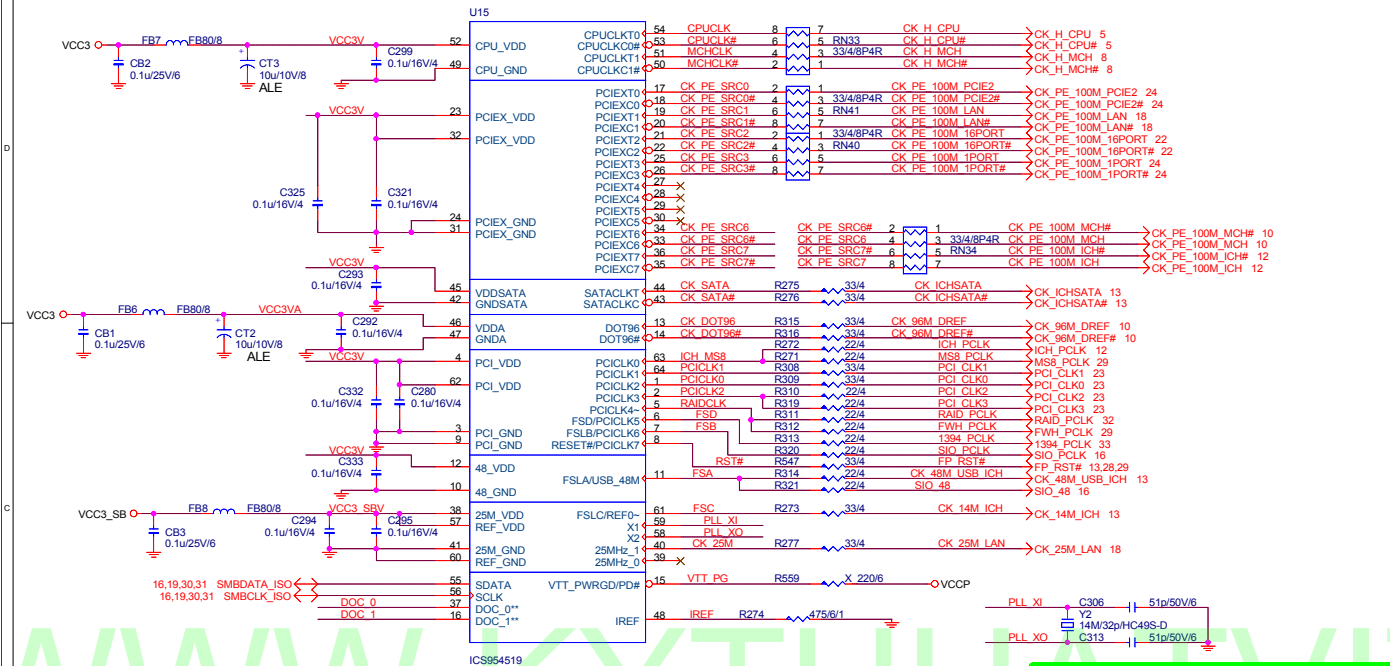
- AA2 TP1 VCCSUS1\_05
- C28 TP2 VCCSUS1\_05
- G20 TP3 VCCSUS1\_05
- K7 TP4 VCCSUS1\_05
- Y7 TP5 VCCSUS1\_05

5VREF Sequencing Circuit

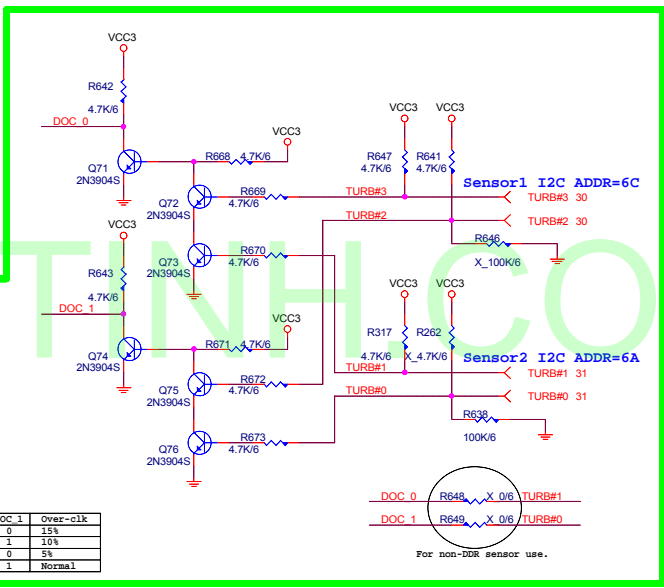


### Clock Generator - ICS954519

Trace length less than 0.5inches



EMC HF filter capacitors, located close to PLL



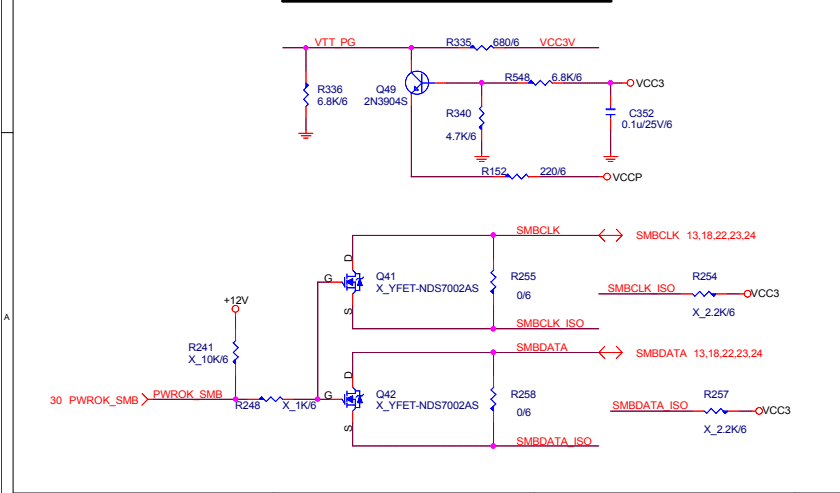
PWM sensor			DDR sensor		
TURB#0	TURB#1	Loading	TURB#2	TURB#3	Loading
0	0	60%	0	0	60%
1	0	50%	0	1	50%
1	0	30%	1	0	30%
1	1	Normal	1	1	Normal

DOC\_0 : TURB#0 AND TURB#2  
DOC\_1 : TURB#1 AND TURB#3

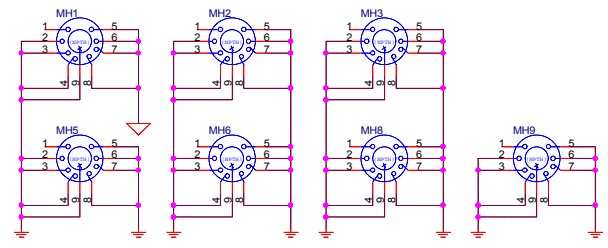
PWM	DDR	DOC(0:1)
00	XX	00
XX	00	00
01	01	01
01	10	00
01	11	01
10	01	00
10	10	10
10	11	10
11	01	01
11	10	10
11	11	11

DOC_0	DOC_1	Over-clk
0	0	15%
0	1	10%
1	0	5%
1	1	Normal

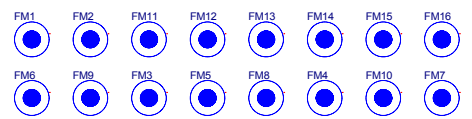
### Clock Generator VTT PowerGood



### Mounting Holes



### Optics Orientation Holes



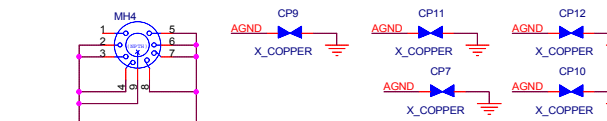
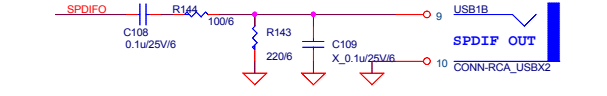
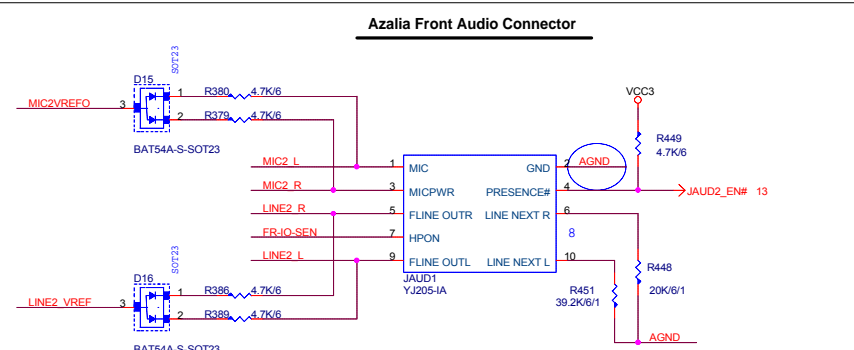
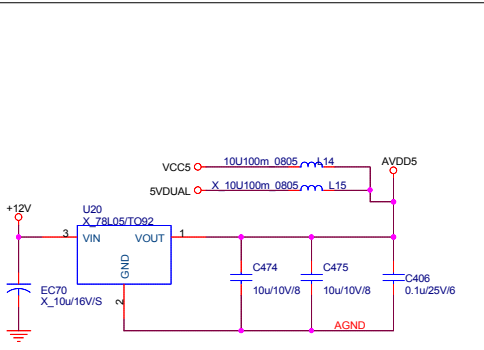
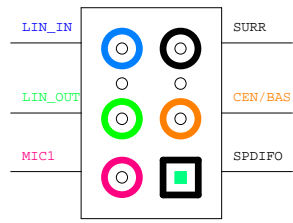
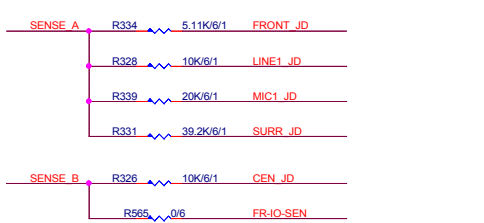
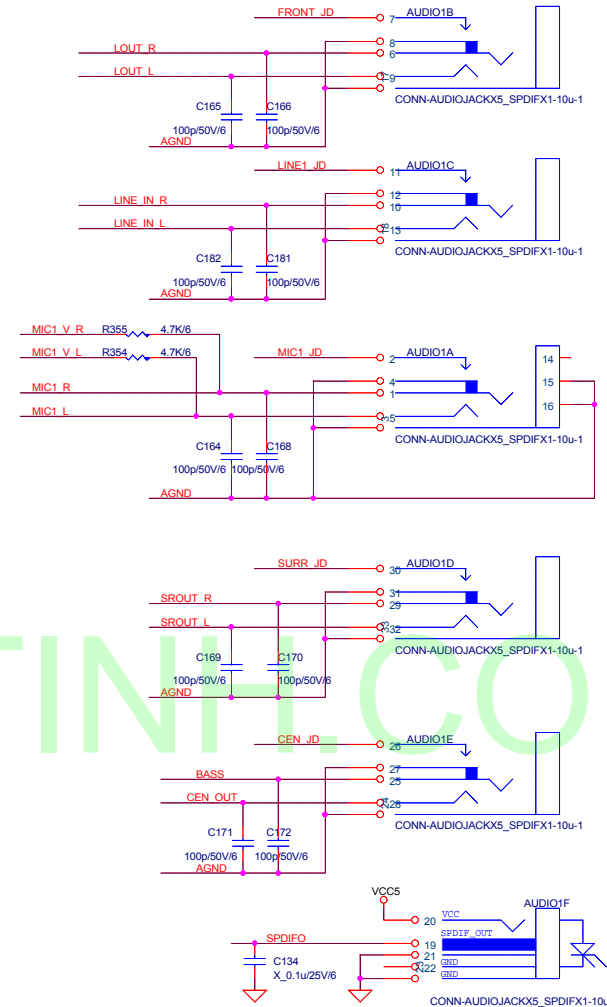
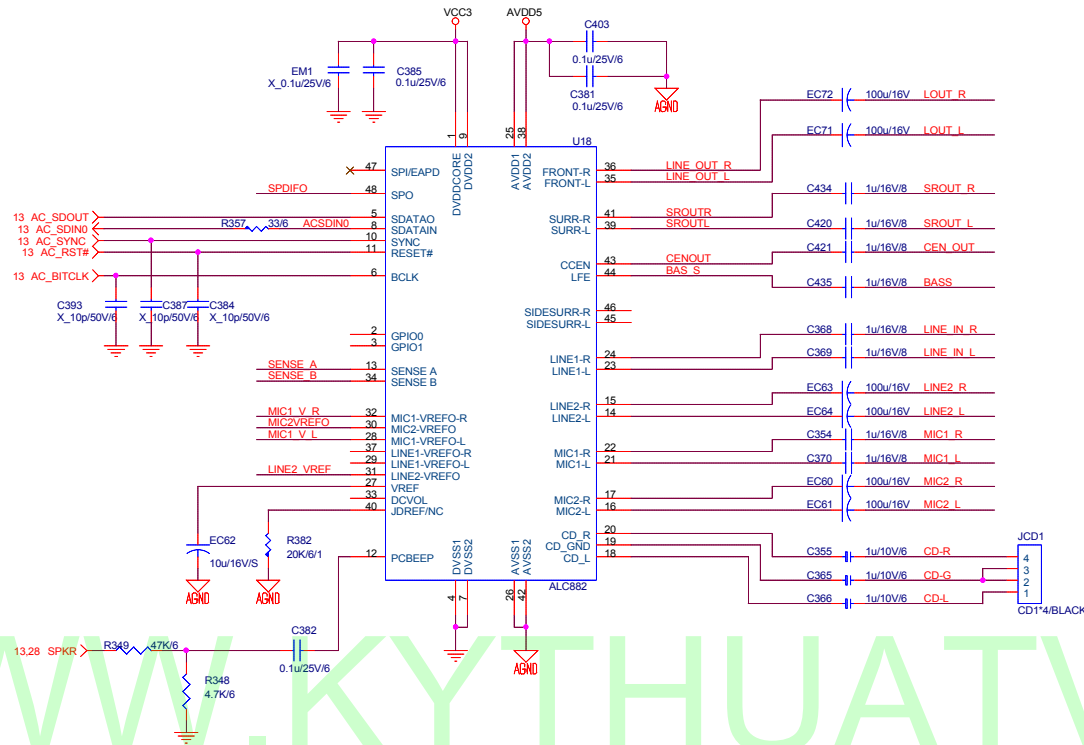
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Title: Clock - ICS954519

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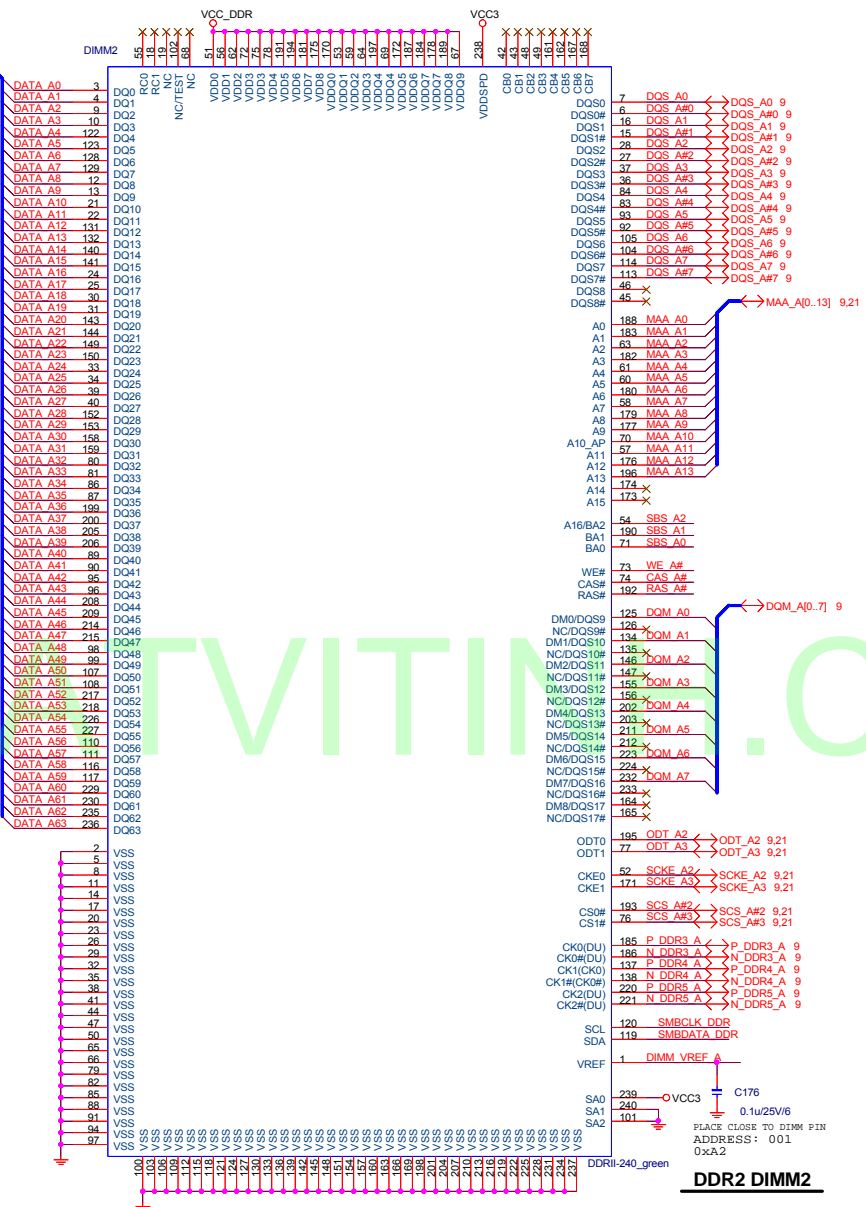
**MSI MICRO-STAR IN'L CO., LTD.**

Title: AC97 AUDIO - ALC882

Size: Document Number: MS-7176

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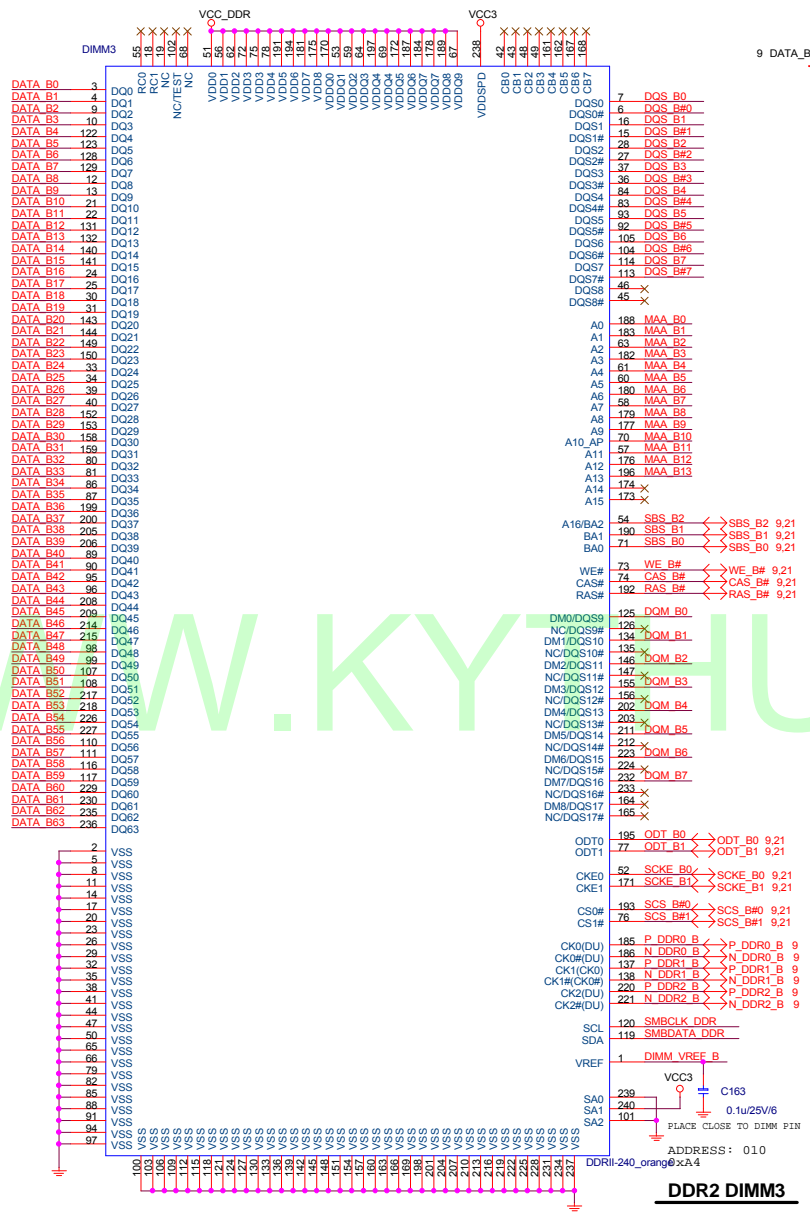
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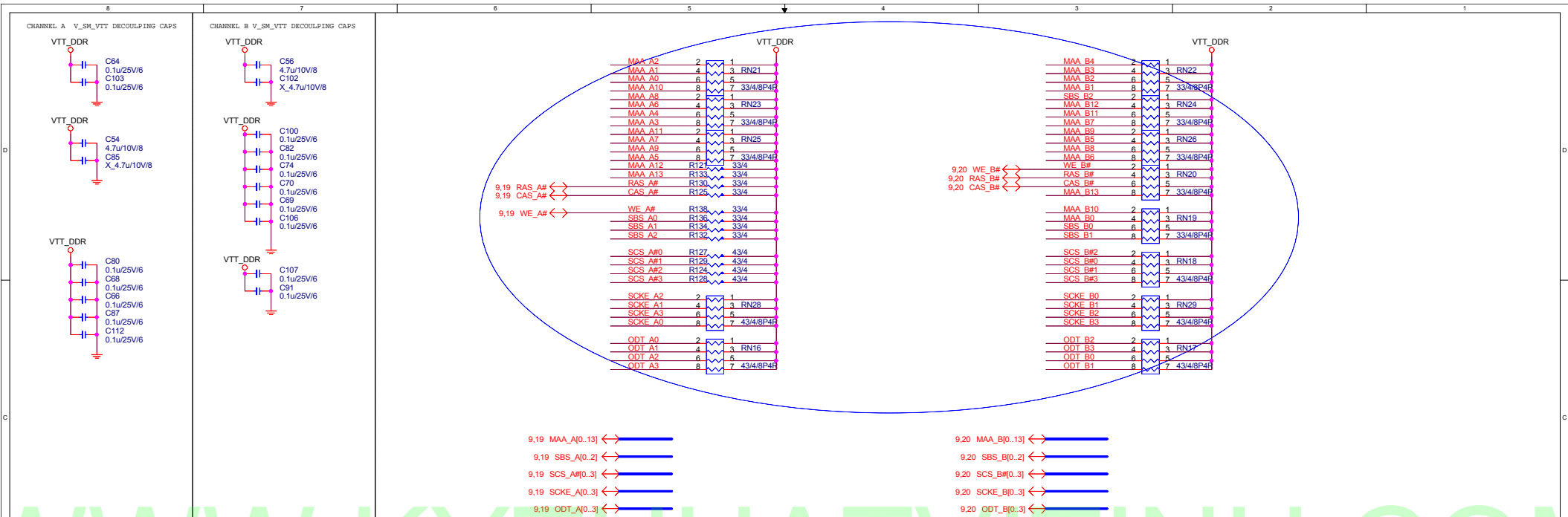
**MSI MICRO-STAR IN'L CO., LTD.**

Title: **DDR II DIMM 1 & 2**

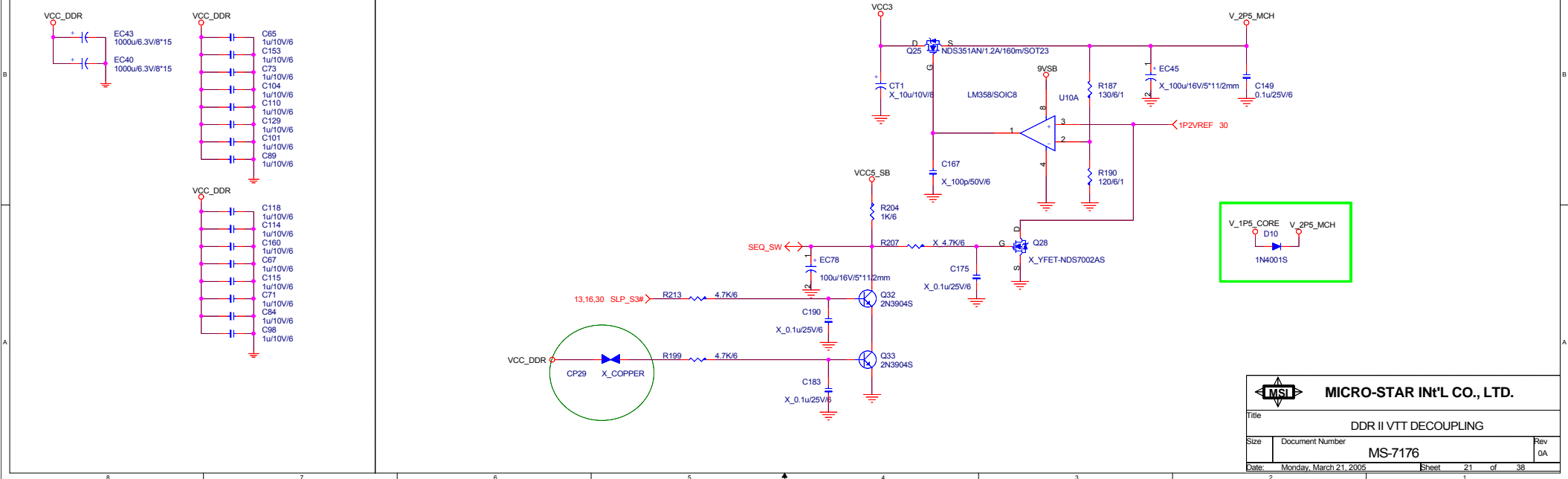
Size: Document Number **MS-7176** Rev 0A

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Grantsdale GMCH Power Sequencing Requirement  
Between 1.5V Core and 2.5V DAC

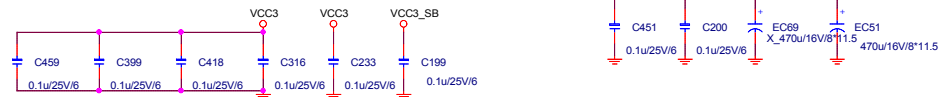
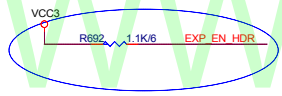
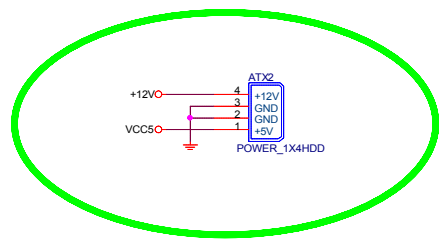
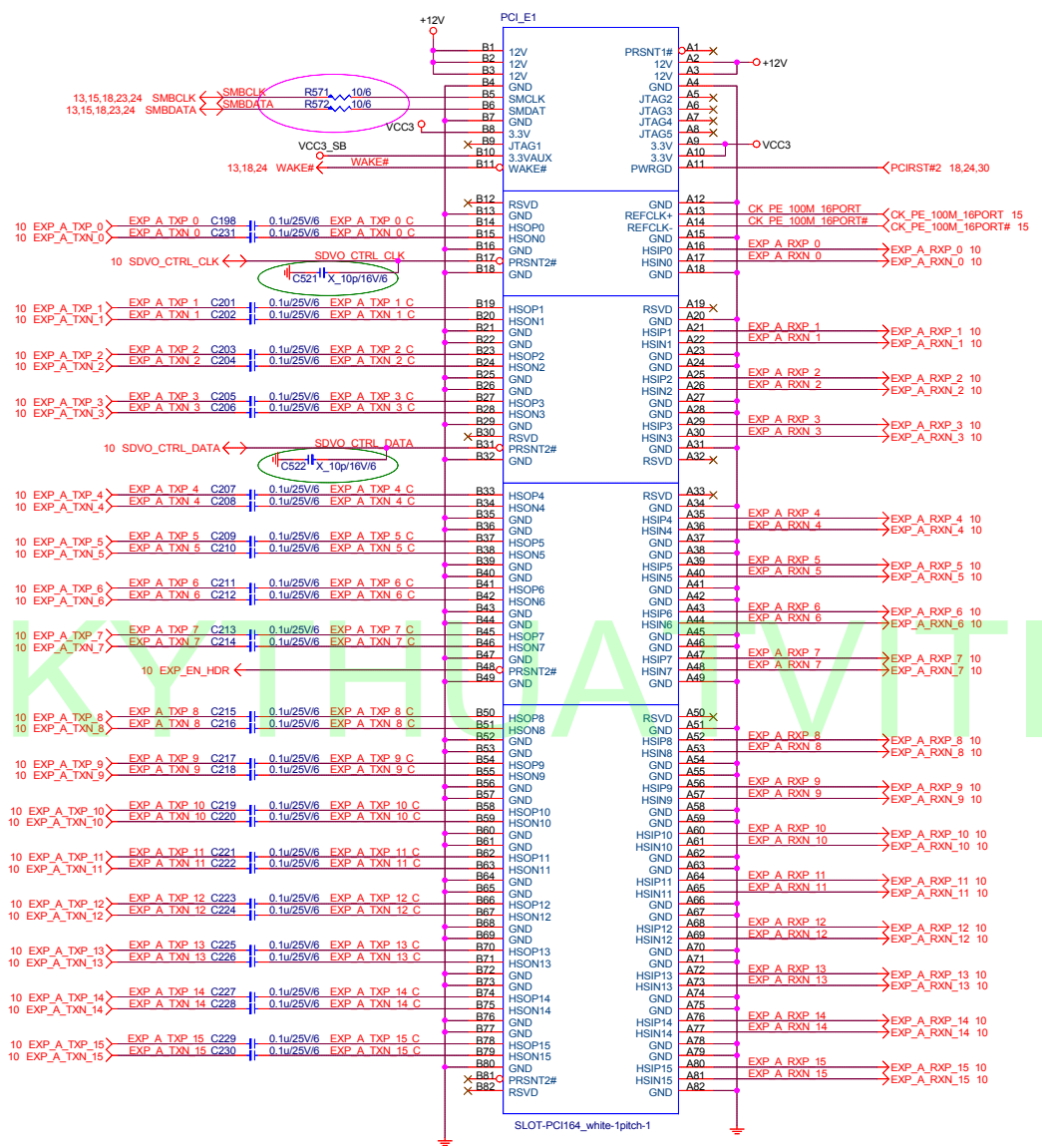


**MSL** MICRO-STAR IN'L CO., LTD.

Title: DDR II VTT DECOUPLING

Size: Document Number: MS-7176 Rev: 0A

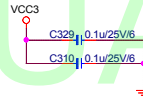
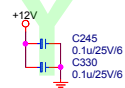
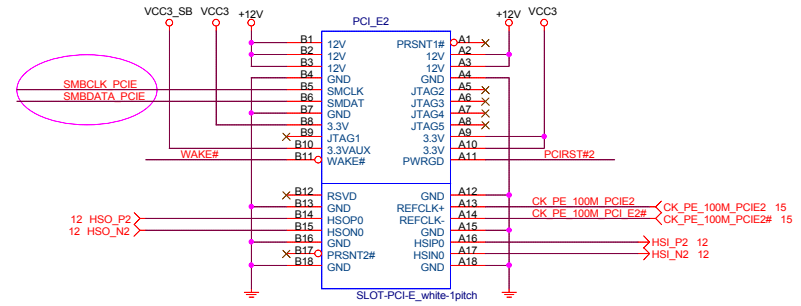
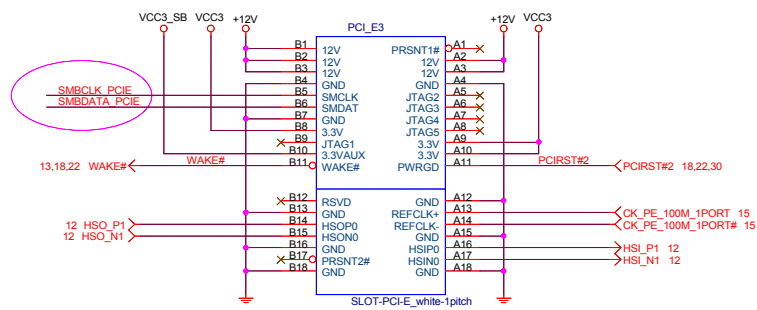
Date: Monday, March 21, 2005 Sheet: 21 of 38



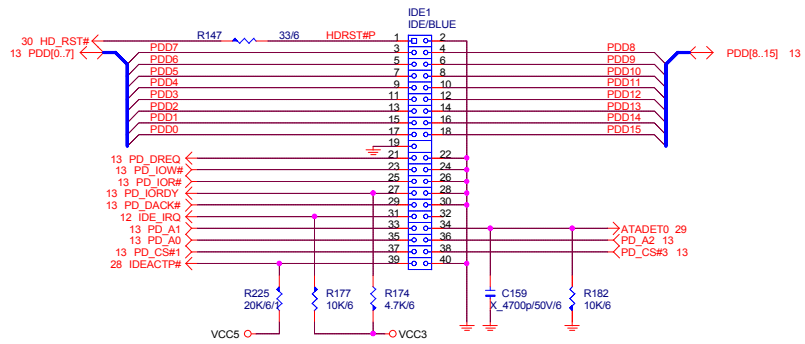
		<b>MICRO-STAR IN'L CO., LTD.</b>	
Title PCI EXPRESS 16 PORT			
Size	Document Number	Rev 0A	
		MS-7176	
Date	Monday, March 21, 2005	Sheet	22 of 38



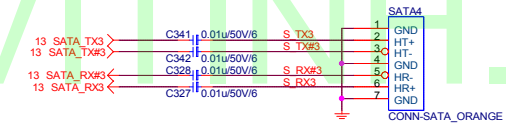
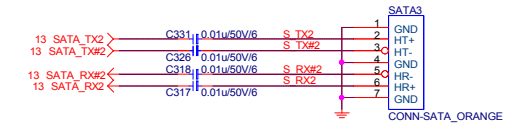
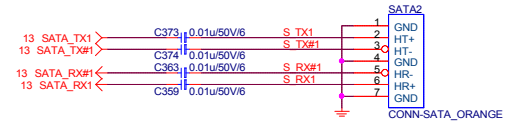
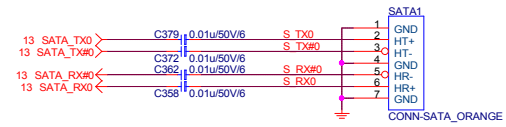
### PCI EXPRESS 1-PORT



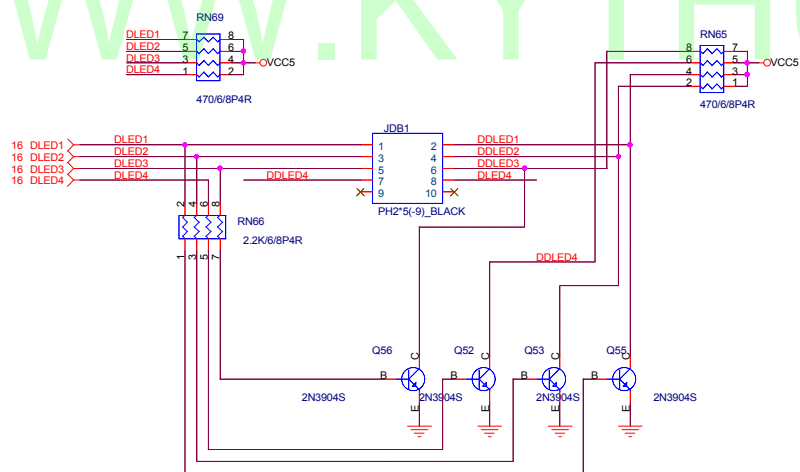
### ATA 33/66/100 IDE Connectors



### SERIAL ATA CONNECTOR BLOCK



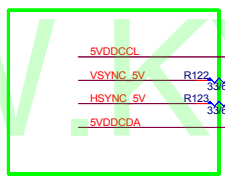
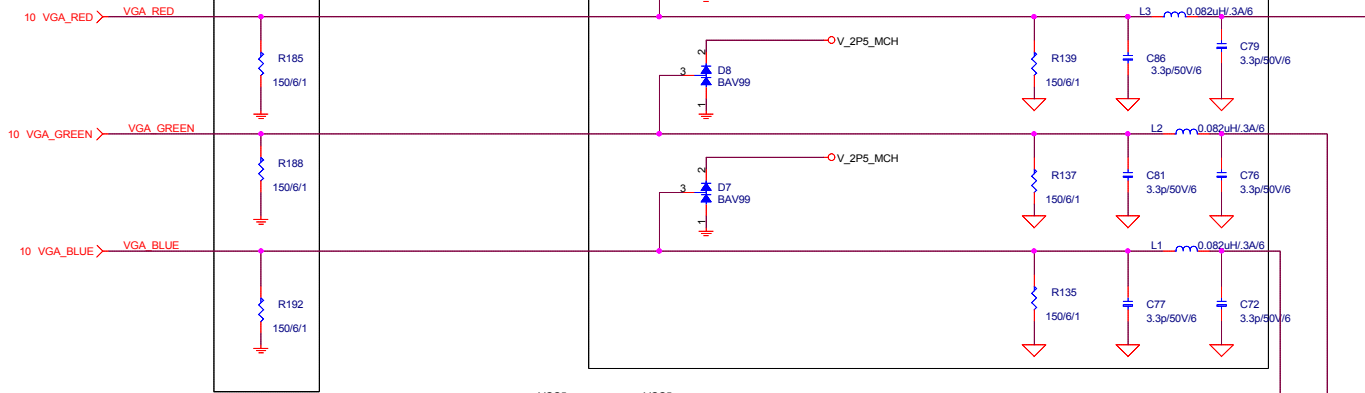
### Diag LED Pin Header



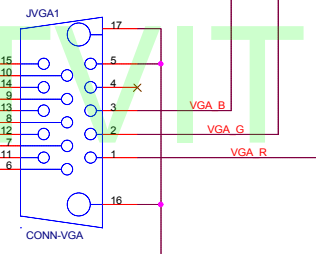
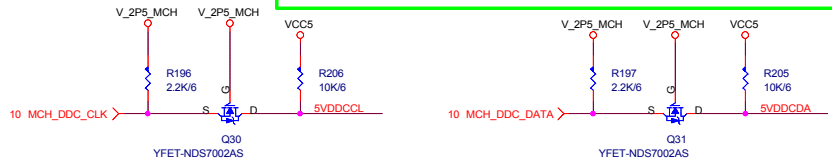
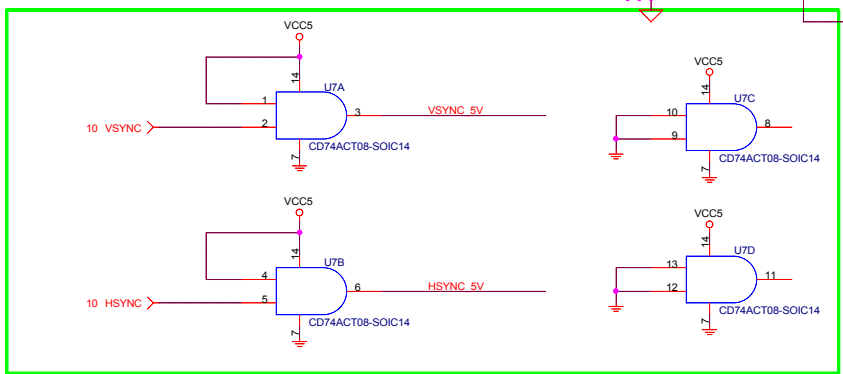
# Video Connector

PLACE CLOSE TO VGA CONNECTOR

PLACE CLOSE TO MCH,  
WITHIN 750 MIL OF PIN

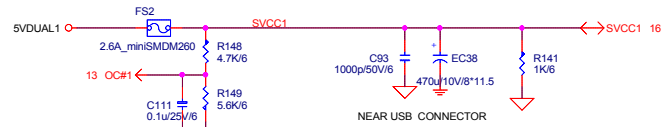


PLACE CLAMPING COMPONENT AND LEVEL  
SHIFT CIRCUIT CLOSE TO VGA CONNECTOR

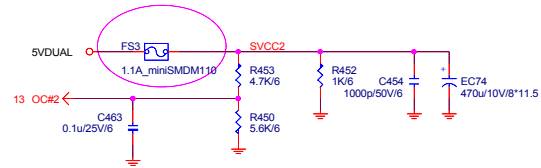


<b>MSI</b> MICRO-STAR INT'L CO., LTD.		
Title VIDEO Connectors		
Size	Document Number MS-7176	Rev 0A
Date	Monday, March 21, 2005	Sheet 26 of 38

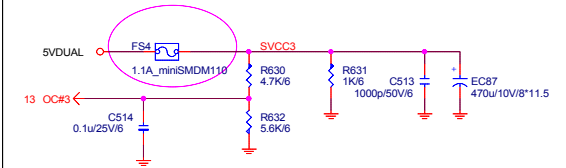
**POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)**



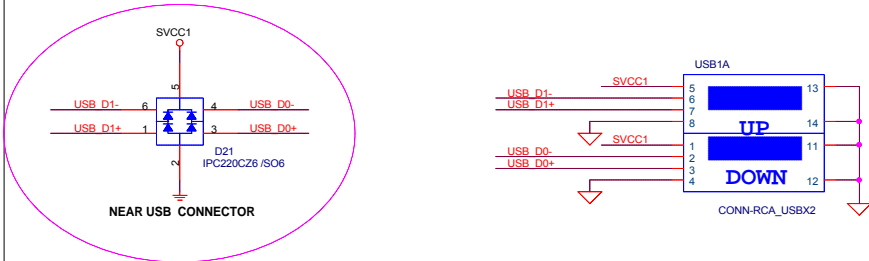
**POWER CIRCUIT FOR USB PORT 4,5 (FRONT)**



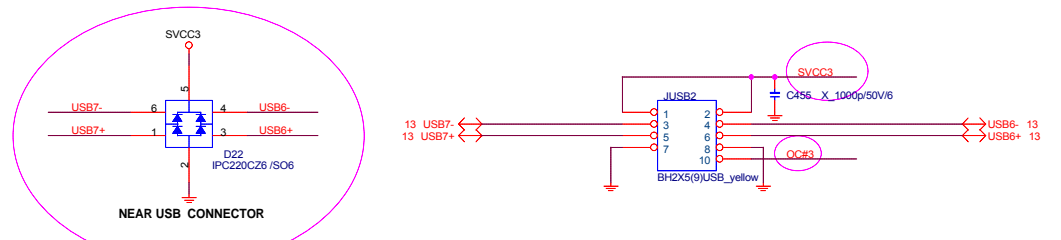
**POWER CIRCUIT FOR USB PORT 6,7 (FRONT)**



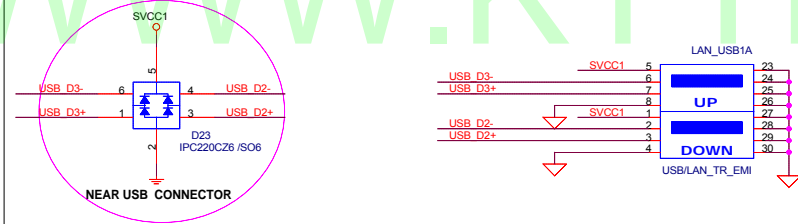
**REAR PANEL USB CONNECTOR FOR USB PORT 0,1**



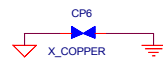
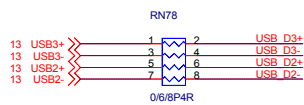
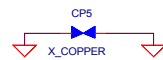
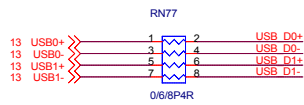
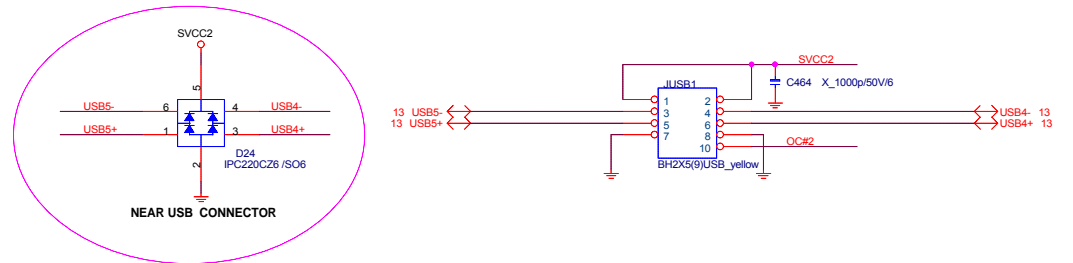
**FRONT PANEL USB CONNECTOR FOR USB PORT 6,7**

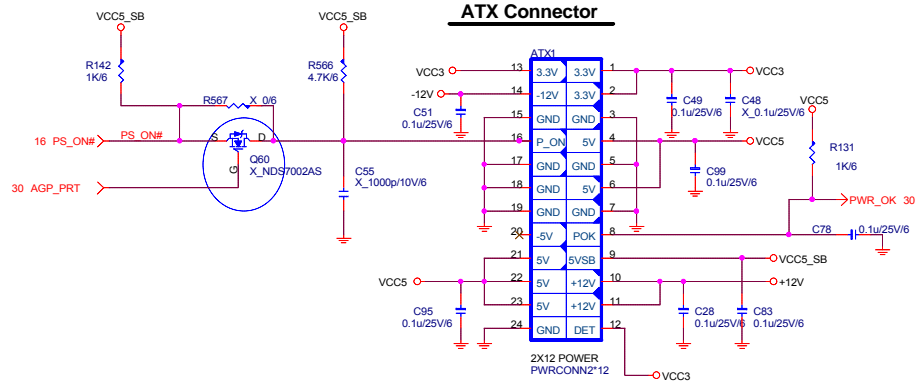


**REAR PANEL USB CONNECTOR FOR USB PORT 2,3**

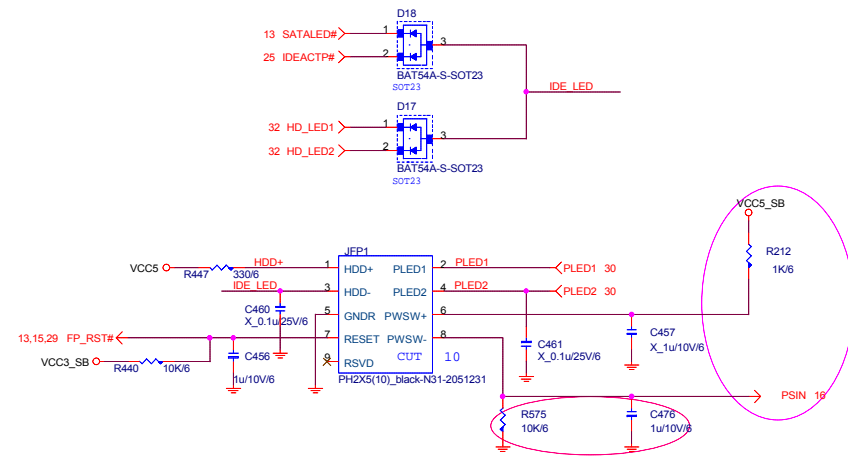


**FRONT PANEL USB CONNECTOR FOR USB PORT 4,5**

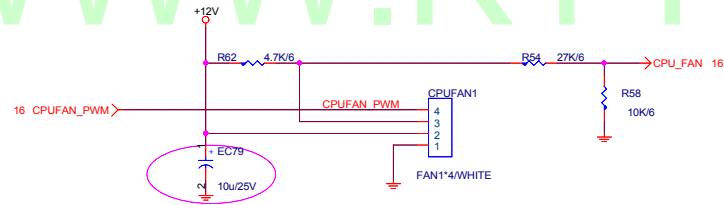




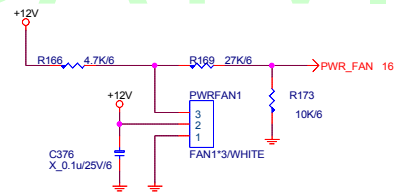
### INTEL/PB Front Panel Connector



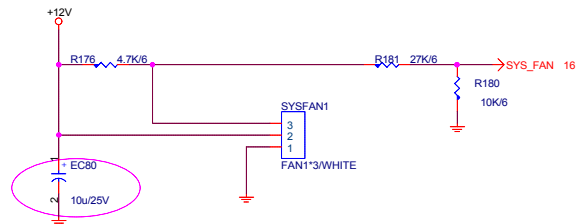
### CPU FAN



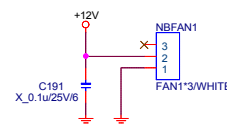
### PWR FAN



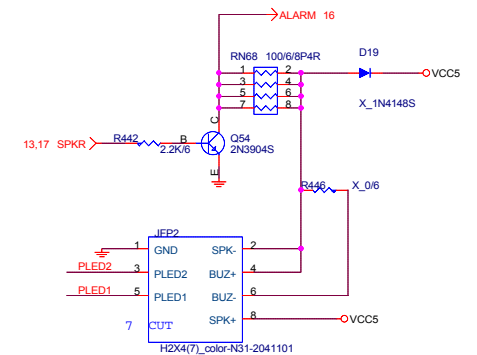
### SYSTEM FAN



### NB FAN

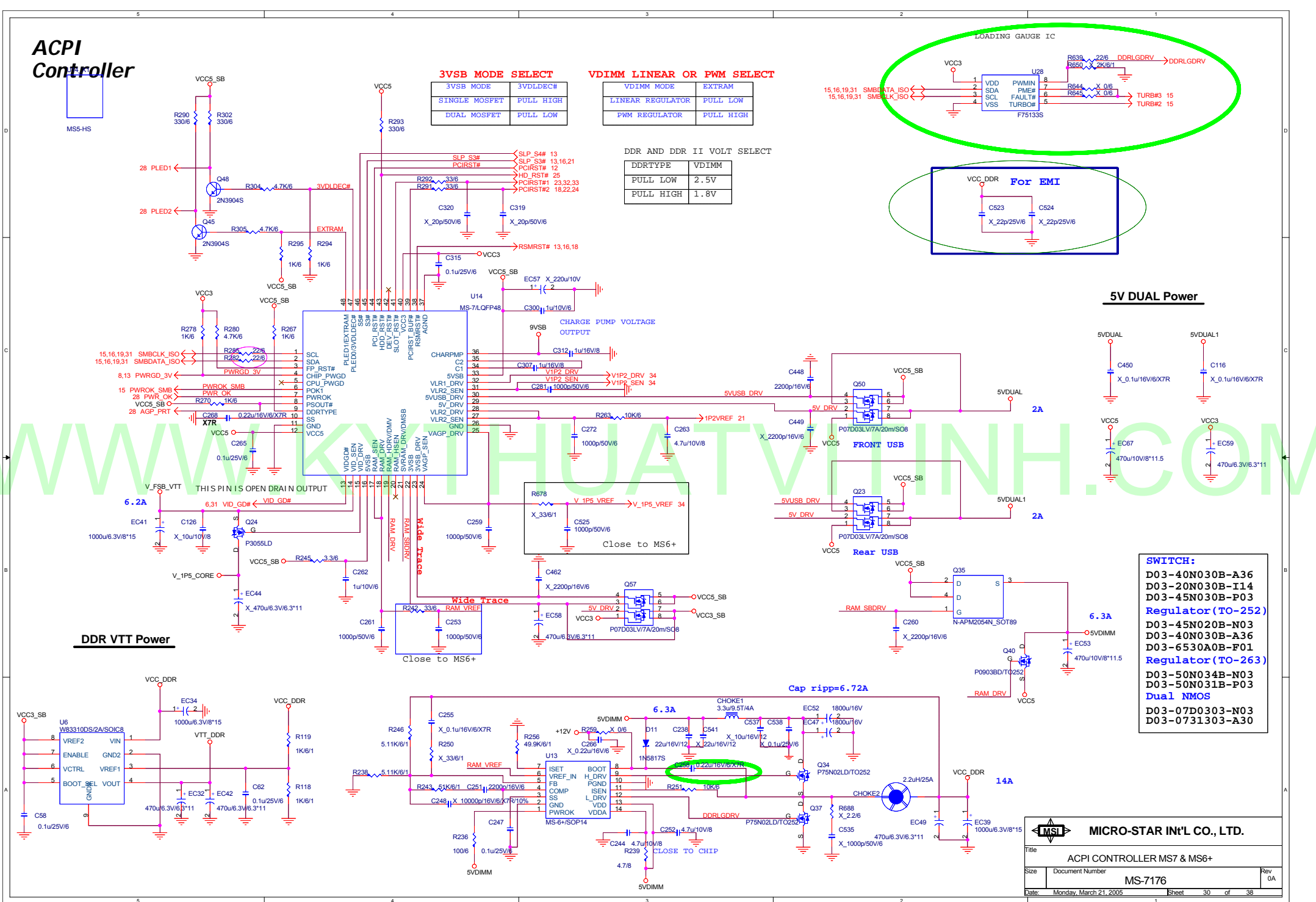


### MSI Front Panel Connector





# ACPI Controller



**3VSB MODE SELECT**

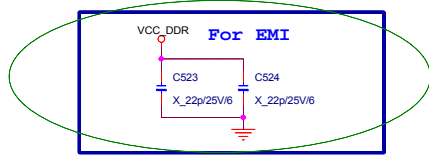
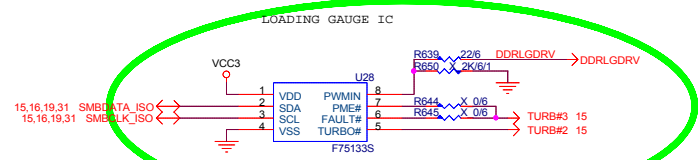
3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

**VDIMM LINEAR OR PWM SELECT**

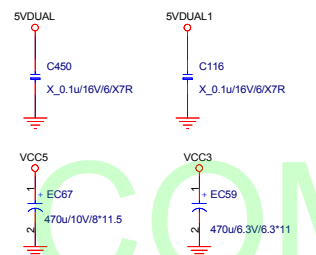
VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

**DDR AND DDR II VOLT SELECT**

DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

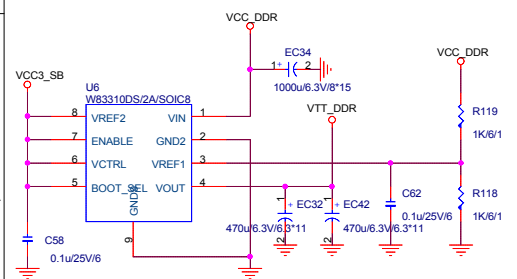


**5V DUAL Power**

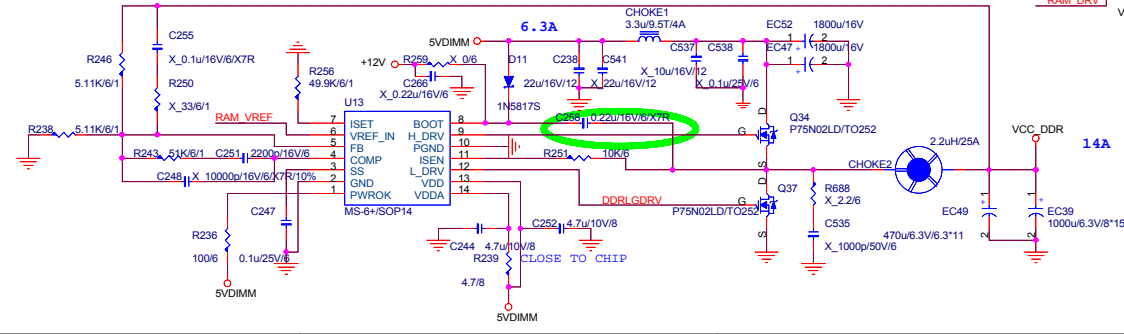


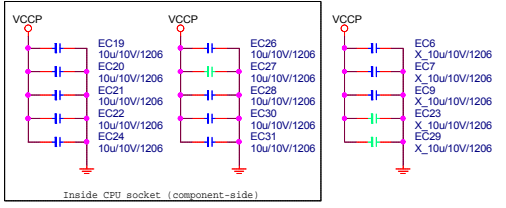
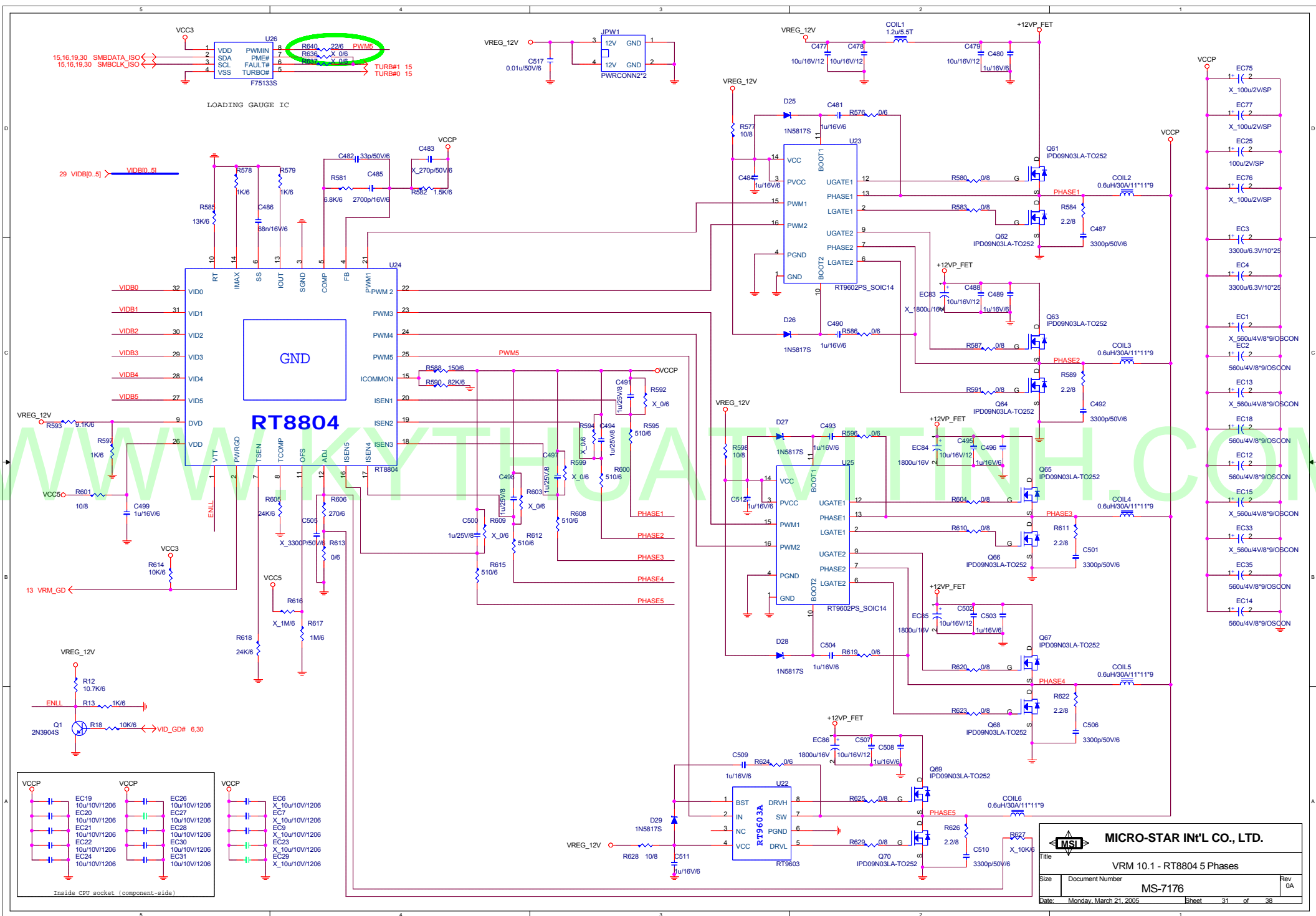
- SWITCH:**
- D03-40N030B-A36
  - D03-20N030B-I14
  - D03-45N030B-P03
  - Regulator (TO-252)
  - D03-45N020B-N03
  - D03-40N030B-A36
  - D03-6530A0B-F01
  - Regulator (TO-263)
  - D03-50N034B-N03
  - D03-50N031B-P03
  - Dual NMOS
  - D03-07D0303-N03
  - D03-0731303-A30

**DDR VTT Power**



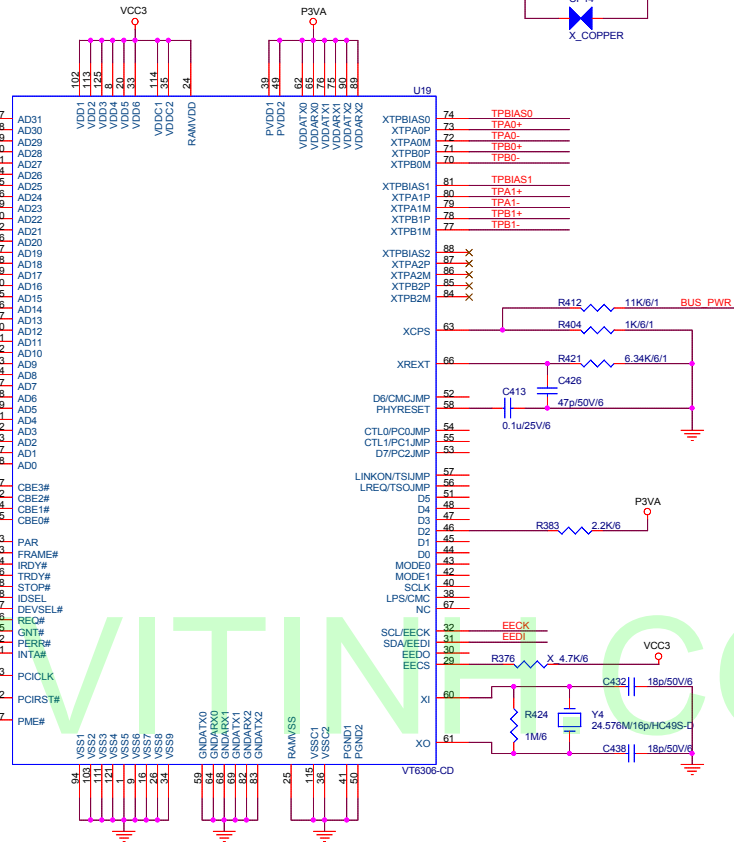
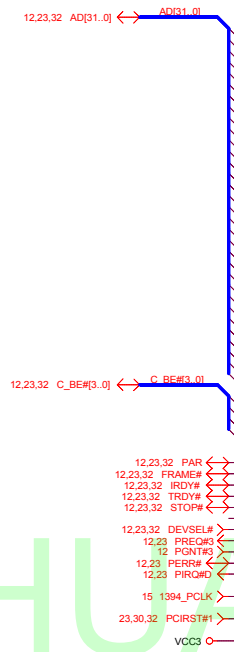
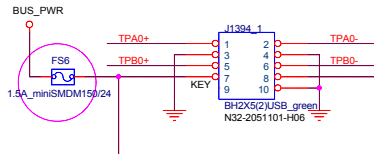
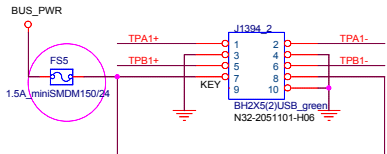
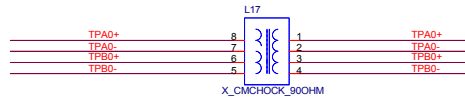
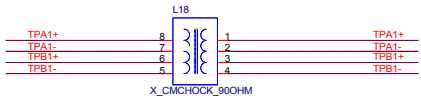
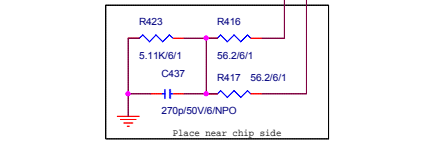
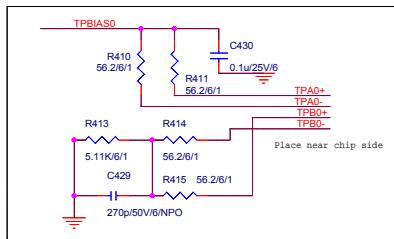
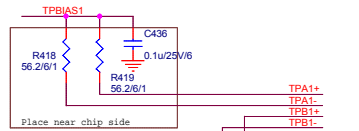
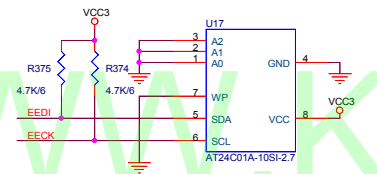
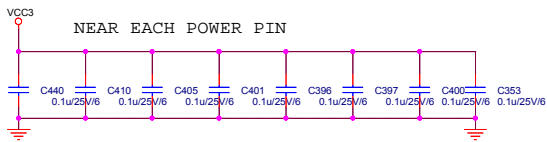
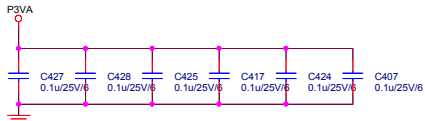
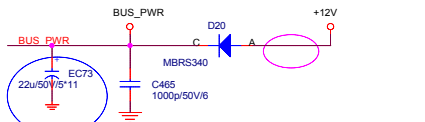
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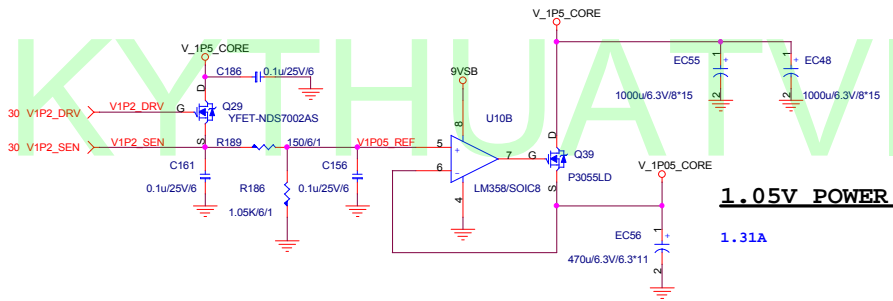
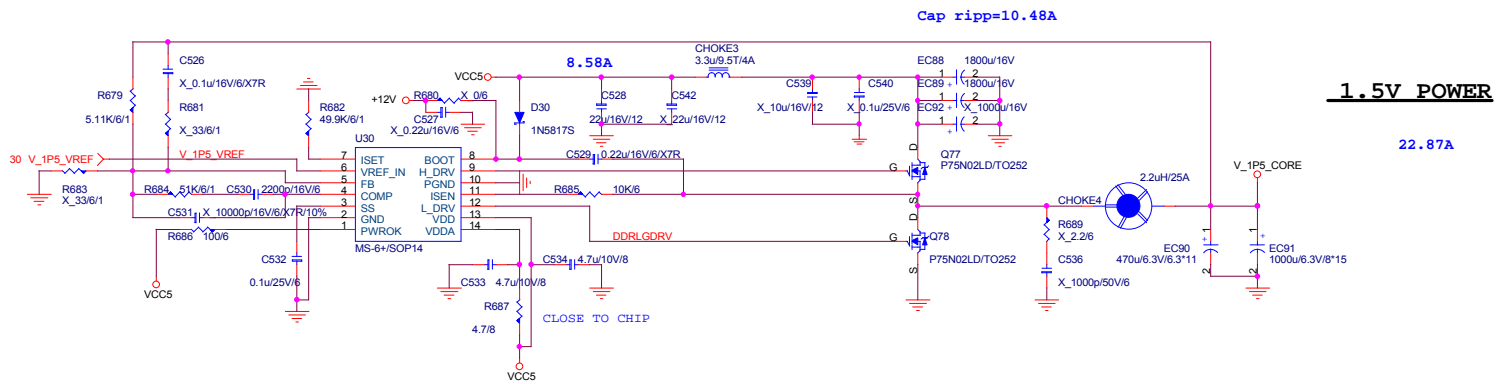




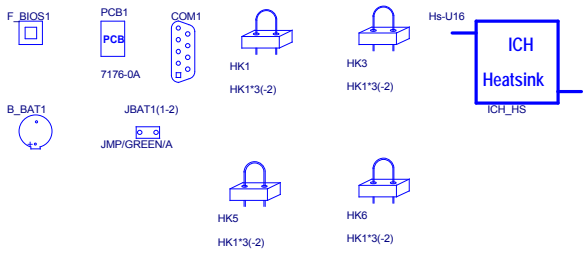
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<b>MICRO-STAR INT'L CO., LTD.</b>		
Title: VRM 10.1 - RT8804 5 Phases		
Size:	Document Number:	Rev: DA
MS-7176		
Date: Monday, March 21, 2005	Sheet: 31	of 38



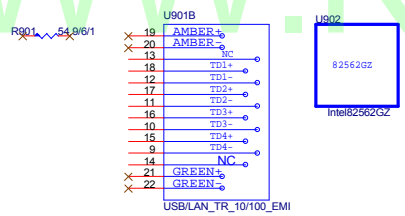




**Auto-BOM Manual Parts**



**Auto-BOM Option Parts**



WWW.KYTHUATVITINH.COM

# ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Signal Name
GPIO[0]	BM_BUSY#	AB18	I/O	Vcc3p3	N	Y	5	Input	strapped
GPIO[1]	PCIREQ[5]#	C8	I/O	V5REF	N	Y	5	Input	PREQ#5
GPIO[2]	PIRQE#	G8	I/OD	V5REF	N	Y	5	Input	PIRQE#E
GPIO[3]	PIRQF#	F7	I/OD	V5REF	N	Y	5	Input	PIRQ#F
GPIO[4]	PIRQG#	F8	I/OD	V5REF	N	Y	5	Input	PIRQ#G
GPIO[5]	PIRQH#	G7	I/OD	V5REF	N	Y	5	Input	PIRQ#H
GPIO[6]	unmuxed	AC21	I/O	Vcc3p3	N	Y	3.3	Input	JAUD2_EN
GPIO[7]	unmuxed	AC18	I/O	Vcc3p3	N	Y	3.3	Input	strapped hi
GPIO[8]	unmuxed	E21	I/O	VccSus3p3	N	Y	3.3	Input	strapped
GPIO[9]	unmuxed	E20	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[10]	unmuxed	A20	I/O	VccSus3p3	N	Y	3.3	Input	strapped
GPIO[11]	SMBALERT#	B23	I/O	VccSus3p3	N	Y	3.3	Input	SMB_ALERT#
GPIO[12]	unmuxed	F19	I/O	VccSus3p3	N	Y	3.3	Input	SIO_PME#
GPIO[13]	unmuxed	E19	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[14]	unmuxed	R4	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[15]	unmuxed	E22	I/O	VccSus3p3	N	Y	3.3	Input	strapped hi
GPIO[16]	unmuxed	AC22	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[17]	PCIGNT[5]#	D8	I/O	Vcc3p3	N	N	3.3	N/A	PGNT#5
GPIO[18]	unmuxed	AC20	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[19]	SATA1GP	AH18	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[20]	unmuxed	AF21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA0GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[22]	PCIREQ[4]#	A13	I/O	Vcc3p3	N	N	3.3	Input	PREQ#4
GPIO[23]	LDRQ1#	AA5	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[24]	unmuxed	R3	I/O	VccSus3p3	N	N	3.3	No Change	LAN_DISABLE#
GPIO[25]	unmuxed	D20	I/O	VccSus3p3	Y	N	3.3	1	NC
GPIO[26]	unmuxed	A21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[28]	unmuxed	E23	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC5#	C3	I/O	VccSus3p3	N	N	3.3	Input	OC#2
GPIO[30]	OC6#	A2	I/O	VccSus3p3	N	N	3.3	Input	OC#3
GPIO[31]	OC7#	B3	I/O	VccSus3p3	N	N	3.3	Input	OC#3
GPIO[32]	unmuxed	AG18	I/O	Vcc3p3	N	N	3.3	1	BIOS_WP#
GPIO[33]	unmuxed	AC19	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[34]	unmuxed	U2	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[35]	unmuxed	AD21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[36]	SATA2GP	AH19	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[37]	SATA3GP	AE19	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[38]	unmuxed	AD20	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[39]	unmuxed	AE20	I/O	Vcc3p3	N	N	3.3	Input	strapped hi
GPIO[48]	GNT4#	A14	I/O	Vcc3p3	N	N	3.3	N/A	PGNT#4
GPIO[49]	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	CPU	N/A	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:  
 GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3\_3 if unused.  
 GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3\_3 if unused.

## SIO W83627THF

PIN NAME	PIN#	USAGE	Input/Output	NOTES
GP43	71	DLED1	OUTPUT OD	Diag LED Output
GP33	89	DLED2	OUTPUT OD	Diag LED Output
GP45	69	DLED3	OUTPUT OD	Diag LED Output
GP35	86	DLED4	OUTPUT OD	Diag LED Output

**FWH** Note: FWH GPs should only be used for static options, do not put dynamic nets on these

GPIO	Pin#	Power	Tol	Signal Name
FPPI[0]	6	Main	3.3	ATADET0
FPPI[1]	5	Main	3.3	pull-up
FPPI[2]	4	Main	3.3	pull-up
FPPI[3]	3	Main	3.3	
FPPI[4]	30	Main	3.3	pull-down

## PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
1394	PIRQ#D	PREQ#3 PGNT#3	AD19	1394_PCLK
IDE RAID	PIRQ#E	PREQ#4 PGNT#4	AD20	RAID_PCLK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1
PCI3	PIRQ#C PIRQ#D PIRQ#A PIRQ#B	PREQ#2 PGNT#2 PREQ#5 PGNT#5	AD18 AD21	PCI_CLK2 PCI_CLK3

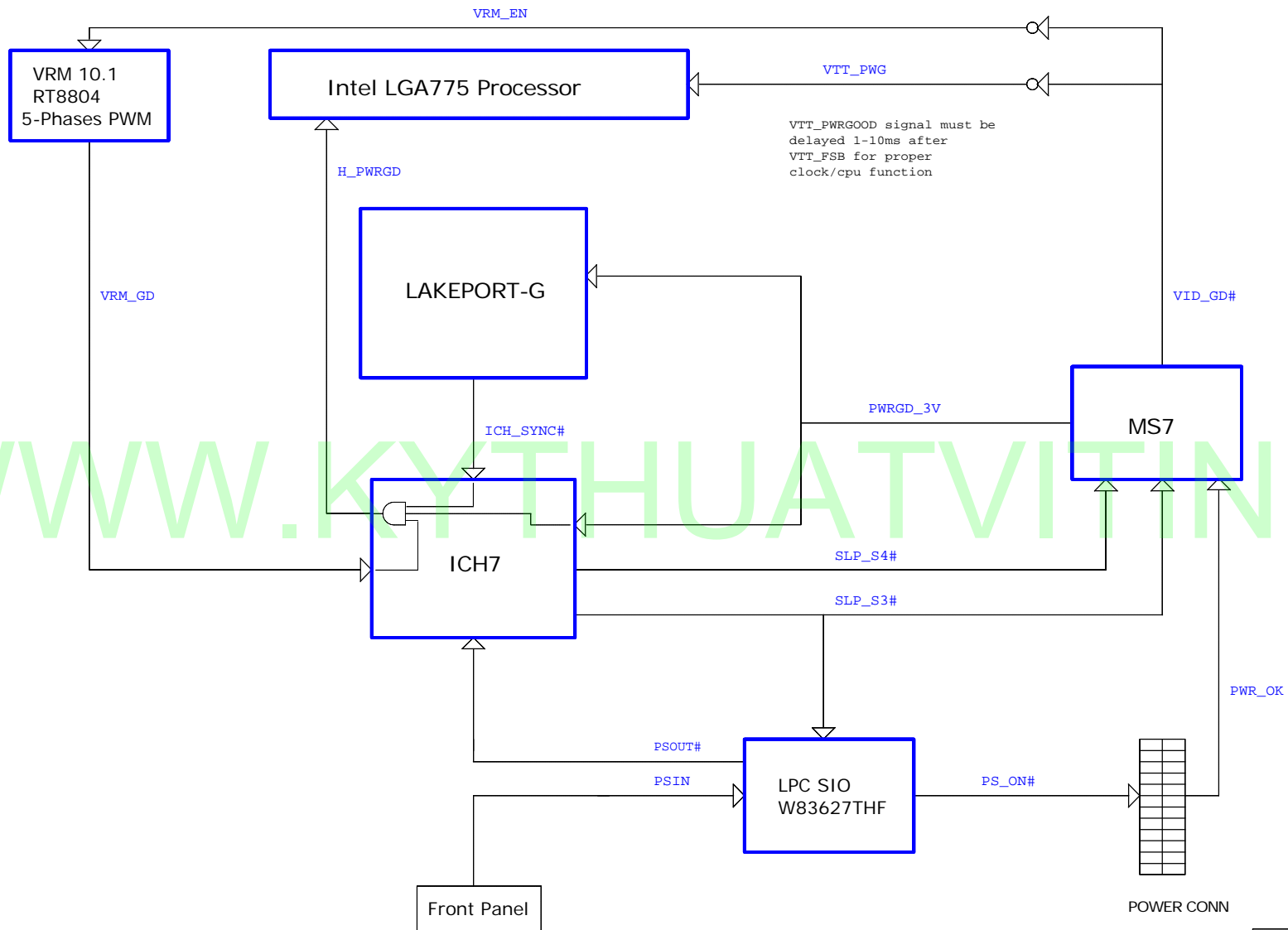
## DDR II DIMM Config.


DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM 3	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM 4	A6H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

## JUMPER SETTING

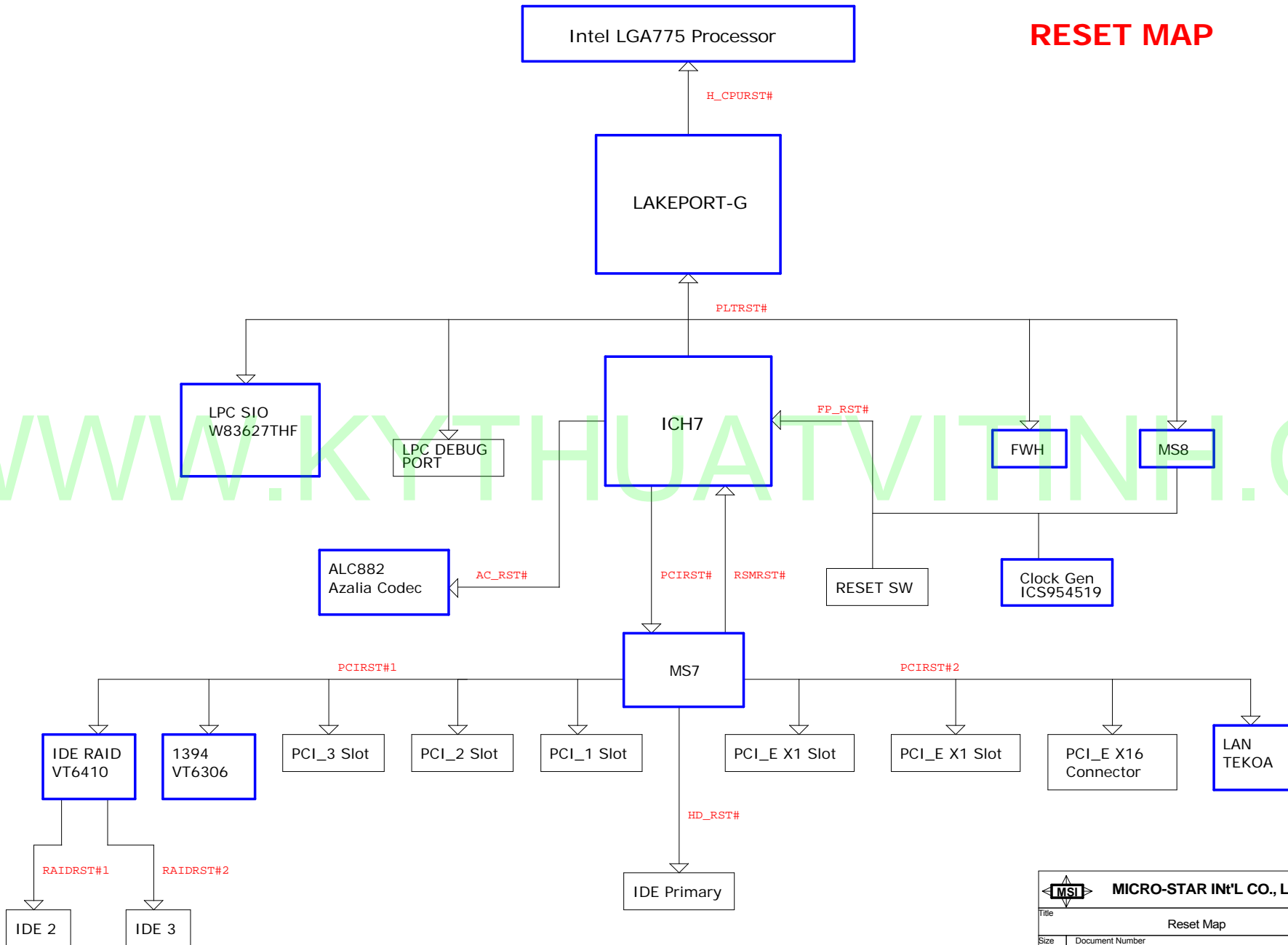
<b>JBAT1</b>	(1-2)NORMAL	(2-3)CLEAR
<b>JCI1</b>	Chassis Intrision	
	Open	Normal
	(1-2)	Chassis Open


# PWROK MAP



 <b>MICRO-STAR INT'L CO., LTD.</b>	
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# RESET MAP



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